

Electronics[®]



CIRCUIT
DESIGNER'S
CASEBOOK



CIRCUIT DESIGNER'S CASEBOOK

Price \$5.50 U.S.A.

Price \$12.00 Outside U.S.A.

PREPARED BY THE EDITORS OF Electronics

MEASUREMENT

| | |
|--|-----|
| Low-distortion modulator tests hi-fi a-m tuners | 12 |
| Data averager for panel meter operates from meter's clock | 29 |
| Ice warning indicator monitors road conditions | 37 |
| Digital clock/calendar offers dual-mode display | 60 |
| Integrated multiplier simplifies wattmeter design | 63 |
| Matching oscilloscope and probe for better measurements | 102 |
| Teaming a scope and a counter clears up ambiguities | 120 |
| Digital storage improves and simplifies analysis of low-frequency signals | 132 |

GENERATION

| | |
|---|---|
| Synchronous ramp generator maintains output linearity | 4 |
| Astable multivibrator needs only one capacitor | 5 |
| Programmable monostable is immune to supply drift | 7 |



| | |
|---|----|
| Programmable multivibrator is four-in-one circuit. | 13 |
| Controlling duty cycle and rep rate independently. | 19 |
| Square-wave generator stresses frequency stability. | 33 |
| Stable crystal oscillator works over wide supply range. | 40 |
| Quad NAND gate package yields two-frequency clock. | 46 |
| Counter and decoder/driver produce staircase voltage. | 52 |
| Binary input determines pulse-generator frequency. | 53 |

AMPLIFIERS

| | |
|---|-----|
| Getting power and gain out of the 741-type op amp. | 8 |
| Eliminating offset error in sense amplifiers. | 39 |
| More applications for the 741-type op amp. | 42 |
| Capacitor corrects drift for analog data amplifier. | 47 |
| CATV transistors function as low-distortion vhf preamplifiers. | 65 |
| Helping a 709-type op amp to outperform itself. | 68 |
| Combined op amps improve over-all amplifier response. | 72 |
| Choosing a sample-and-hold amplifier is not as simple as it used to be. | 147 |
| Norton quad amplifier subtracts from costs, adds to design options. | 173 |

FILTERS

| | |
|--|----|
| Tunable active filter has switchable response. | 3 |
| Two-IC digital filter varies passband easily. | 14 |
| Three-mode network is filter or oscillator. | 26 |
| Narrowband digital filter achieves high Qs. | 75 |

COMMUNICATIONS

| | |
|---|-----|
| Variable-gain amplifier yields linear rf modulator. | 2 |
| Binary rf phase modulator switches in 3 nanoseconds. | 30 |
| Varistor voltage divider improves receiver agc. | 41 |
| Mark/space demodulator employs active filters. | 49 |
| Digital demodulator for phase-shift-keyed data. | 71 |
| Multiplexer adds efficiency to 32-channel telephone system. | 84 |
| Transformer-coupled transceiver speeds two-way data transmission. | 108 |
| Functional redundancy assures greater system reliability. | 116 |

DATA CONVERTERS

| | |
|---|-----|
| Analog-to-digital converter produces logarithmic output. | 44 |
| Adding automatic zeroing to analog-to-digital converter. | 59 |
| Digital-to-analog converter is built from low-cost parts. | 67 |
| No-ladder d-a converter works from one 5-V supply. | 80 |
| The charge-balancing a-d converter: an alternate to dual-slope integration. | 123 |

LOGIC

| | |
|--|-----|
| High-power counter drives 20-watt loads. | 15 |
| Switching large ac loads with logic-level signals. | 17 |
| Up/down synchronous counter takes just four MSI packages. | 23 |
| Simple gating circuit monitors real-time inputs. | 35 |
| TTL interface circuit synchronizes computer clock. | 43 |
| Digital transient suppressor eliminates logic errors. | 51 |
| C-MOS counting circuit accumulates 2^{70} pulses. | 57 |
| Simple logic arrangement identifies first event. | 58 |
| Integrated timer operates as variable Schmitt trigger. | 69 |
| Register-addressing system accesses within nanoseconds. | 74 |
| Gate threshold difference produces initializing pulse. | 76 |
| An easy way to design complex program controllers. | 88 |
| ROMs cut cost, response time of m-out-of-N detectors. | 99 |
| C-MOS may help majority logic win designers' vote. | 137 |
| Designing with microprocessors instead of wired logic asks more of designers. | 160 |

CONTROL

| | |
|--|-----|
| Automobile ignition system is rugged and reliable. | 5 |
| Solid-state dpdt switch provides current reversal. | 9 |
| Negative-resistance generator has controllable response. | 10 |
| Extending time delay with an emitter-follower. | 21 |
| Using transistor arrays for temperature compensation. | 24 |
| Dc motor control circuit cancels armature resistance. | 25 |
| Voltage-to-current converter for process-control systems. | 28 |
| Varying comparator hysteresis without shifting initial trip point. | 31 |
| Circular voltage divider needs fewer resistors. | 31 |
| Link-coupled tank circuit steps up C-MOS drive voltage. | 32 |
| Temperature compensation for high-frequency transistors. | 34 |
| Audio amplitude leveler minimizes signal distortion. | 36 |
| Analog multiplier/divider simplifies frequency locking. | 45 |
| High-speed voltage-follower has only 1-nanosecond delay. | 48 |
| Sampling regulator controls motor speed. | 50 |
| Automatic gain control operates over two decades. | 54 |
| Frequency discriminator uses one-shot and flip-flop. | 56 |
| Precision triac trigger has wide dynamic range. | 62 |
| Miller-effect integrators act as signal separator. | 65 |
| Electronic switch controls automobile air conditioner. | 66 |
| Two-IC pulse discriminator handles wide range of inputs. | 70 |
| All-digital phase shifter handles 5-to-1 bandwidth. | 78 |
| Voltage discriminator has 0.1-mV resolution. | 79 |
| Dc restorer for video use offers ultra-stability. | 81 |
| MOS chip plus level-shifting circuit drives gas-discharge display. | 111 |
| Matching driver circuitry to multidigit numeric displays. | 123 |
| Impedance-sensitivity nomograph aids design of trimming networks. | 156 |
| Analyzing ladder-type networks by a quick arithmetic procedure. | 174 |

POWER SUPPLIES

| | |
|---|-----|
| Doubling breakdown voltage with cascoded transistors. | 1 |
| C-MOS voltage monitor protects Ni-Cd batteries. | 16 |
| Gate bias circuit for n-MOS runs from 5-V TTL supply. | 18 |
| Adding foldback resistor provides overload safety. | 20 |
| Current-sharing design boosts regulator output. | 22 |
| One lamp can monitor battery voltage. | 27 |
| Single-supply reference source uses self-regulated zener. | 38 |
| Regulating high voltages with low-voltage zeners. | 41 |
| Boosting IC regulator current with almost no power loss. | 60 |
| Handy supply provides fixed and variable outputs. | 64 |
| Inexpensive power supply produces zero-ripple output. | 73 |
| Temperature limiting boosts regulator output current. | 77 |
| Regulator for standby supply handles large load currents. | 82 |
| Dual-polarity IC regulators aid design and packaging. | 95 |
| Hybrid approach to regulation solves power-supply problems. | 143 |
| Switching regulators: the efficient way to power. | 151 |

Doubling breakdown voltage with cascoded transistors

by Peter T. Uhler
Tinker Air Force Base, Midwest City, Okla.

When bipolar transistors are connected in series to increase their over-all breakdown voltage for power-circuit applications, high-voltage zener diodes are usually needed to protect the transistors. And generally, besides being expensive, these high-voltage zeners have rather modest power ratings.

An alternate approach, a saturating cascode switch, effectively doubles transistor breakdown voltage without requiring costly zeners. The cascode switch generates 600-volt rectangular positive-going pulses with 350-v transistors. It employs a shunt, rather than series, approach for additional load protection.

In the region of operation where output voltage (V_o) is greater than half the supply voltage ($V_{CC}/2$), the switch works as a conventional cascode amplifier, and the collector currents of transistors Q_1 and Q_2 are equal. The base voltage of Q_2 never exceeds $V_{CC}/2$ (unless Q_2 's reverse collector saturation current, I_{CBO} , becomes significant), because of the voltage divider formed by

the two same-value biasing resistors, labeled R. Therefore, the maximum voltage drop across each transistor is effectively limited, and the need for zener diode clamps is eliminated.

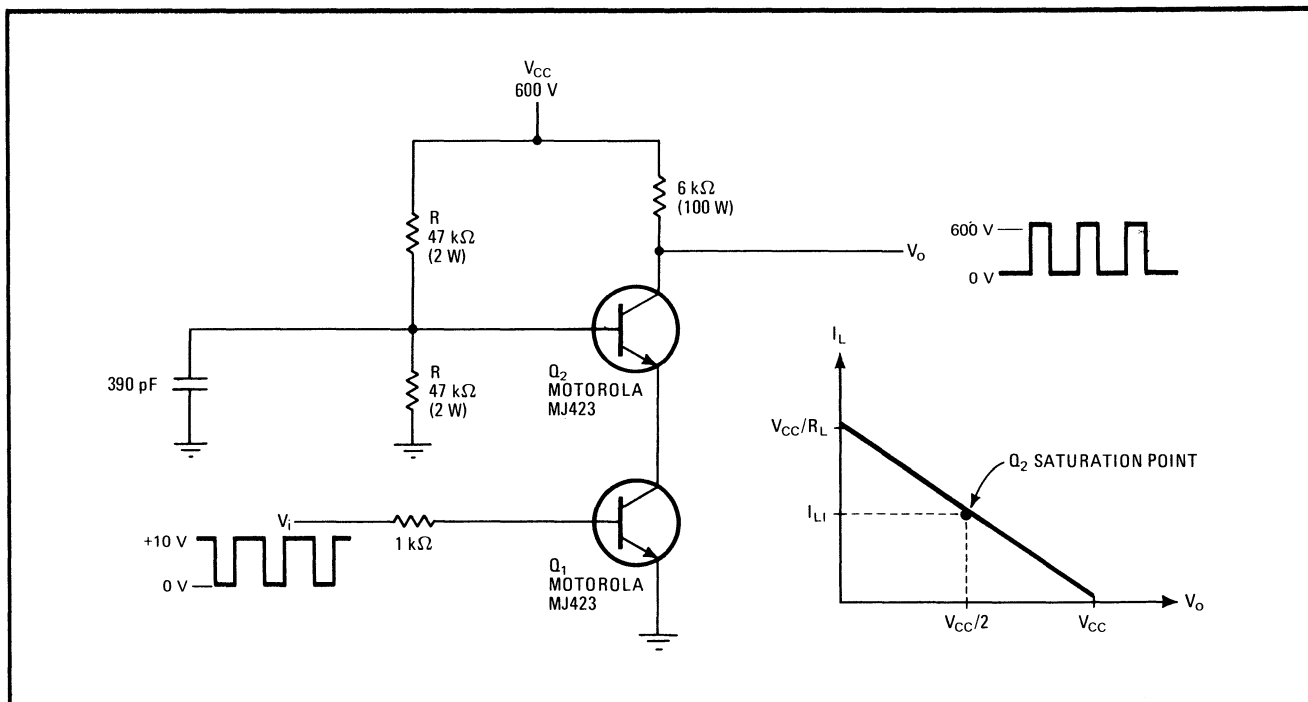
As load current I_L exceeds the midpoint current value (I_{L1}) shown on the static load line, transistor Q_2 saturates and transistor Q_1 becomes the sole controlling element. The load resistance for the switch is now the parallel combination of the load resistance itself and half the biasing resistance ($R_L \parallel R/2$), which is essentially equal to R_L since $R/2$ is much greater than R_L .

Only a slight discontinuity occurs in the load line when transistor Q_2 saturates, so that the circuit's output voltage is practically a continuous function of its input voltage throughout the entire output voltage range of 0 to 600 v. The capacitor at the base of Q_2 eliminates the positive-going charge-storage transient that is generated if this transistor is forced out of saturation rapidly.

The biasing resistance value of $R/2$ must be small enough to prevent Q_2 's reverse saturation current (I_{CBO}) from causing a significant rise in the potential at Q_2 's base. Also, the $R/2$ resistance value must be less than the factor, $h_{FE}R_L$, to assure that Q_2 's collector-emitter voltage is a decreasing function of collector current.

The saturating cascode switch can be modified to handle even higher voltages by using three transistors and two separate biasing resistor pairs to bias the transistors at supply voltages of $2V_{CC}/3$ and $V_{CC}/3$. □

Eliminating high-voltage zeners. Cascoded transistors generate 600-volt pulses without using high-priced high-voltage zener diodes for protection. Biasing resistors limit voltage across transistors to $V_{CC}/2$. When V_o is greater than $V_{CC}/2$, transistors Q_1 and Q_2 behave like conventional cascode amplifier. When V_o is less than $V_{CC}/2$, Q_2 saturates, and only Q_1 determines load current.



Variable-gain amplifier yields linear rf modulator

by Michael F. Black
Equipment Group, Texas Instruments, Dallas, Texas

An rf modulator that offers a linear relationship between input control voltage and output rf voltage can be achieved by using a variable-gain amplifier to compensate for the nonlinear characteristics of a p-i-n diode attenuator. Circuit operation remains linear for an input-signal range of approximately 30 decibels.

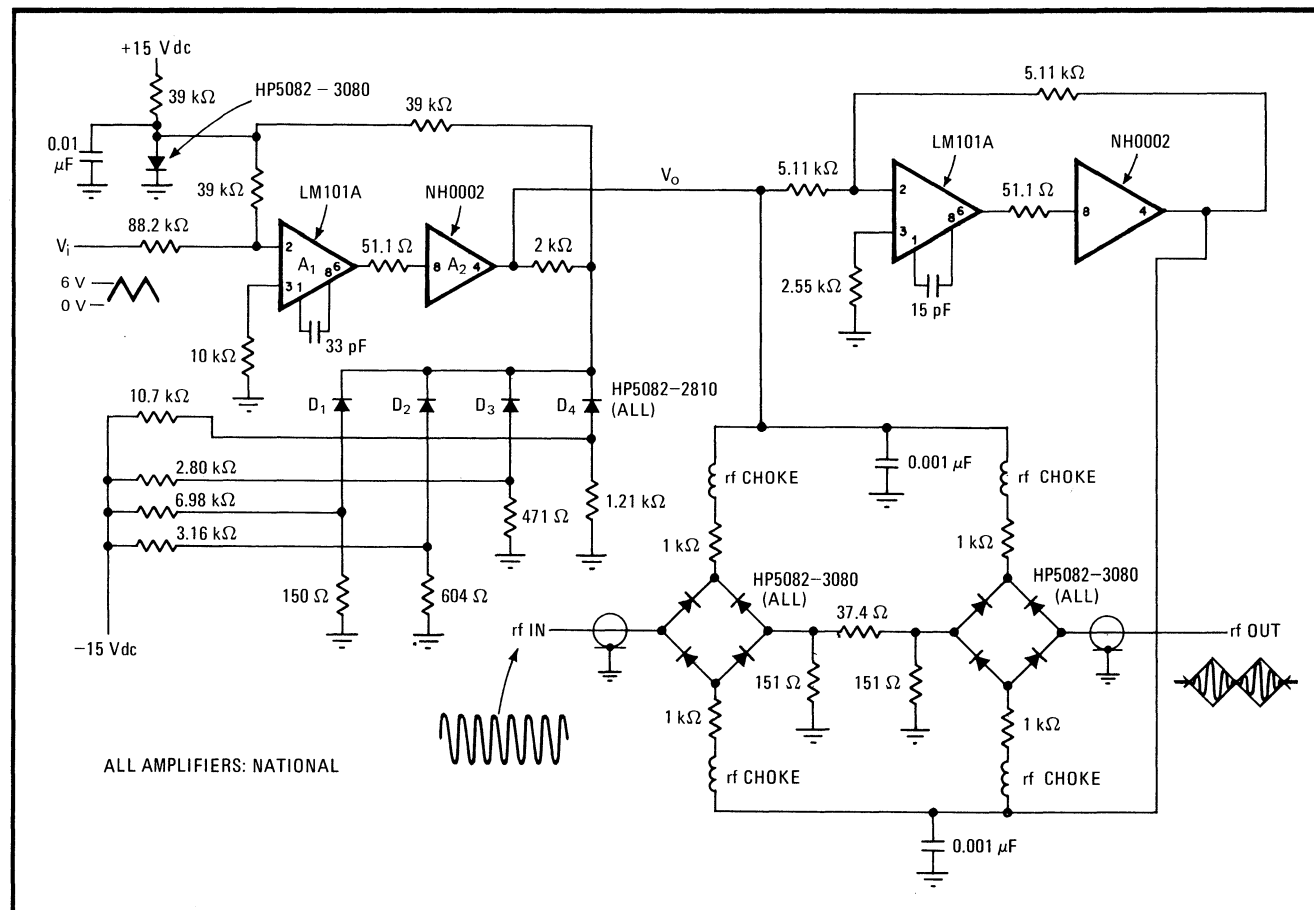
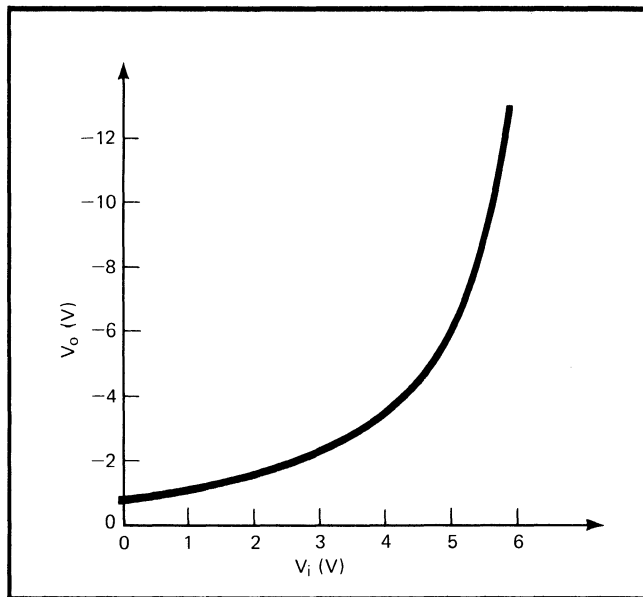
The gain of amplifier A_1 depends on the level of input control voltage V_i . As this modulation voltage increases, diodes D_1 through D_4 conduct, shunting some of A_1 's feedback current to ground and raising this amplifier's gain. The resulting voltage-gain curve for both amplifier A_1 and buffer amplifier A_2 , adjusted for the varying resistance of the p-i-n diodes used in the modulator, is shown in the diagram.

The p-i-n diodes are connected as a reflective at-

Linear rf modulator. For 30-decibel signal range, rf modulator provides output rf voltage that varies linearly with input control voltage. Combined gain of amplifier A_1 and buffer A_2 is curved (as shown) to compensate for nonlinear characteristic of p-i-n diode attenuator. Gain is varied by partially grounding feedback current through diodes D_1 and D_4 . Operating frequency ranges from 60 to 150 MHz.

tenuator that has inherent dc balance and offset characteristics to minimize ringing and transient effects. Here, a pad is placed between the two attenuator sections for isolation purposes, but an amplifier can be substituted for the pad if desired.

The values of the attenuator rf chokes are determined by the operating rf carrier frequency and the upper modulation frequency. The circuit performs well from 60 to 150 megahertz, with modulation frequencies as high as 250 kilohertz. □



Tunable active filter has switchable response

by Philbrook Cushing
La Jolla, Calif.

With a minimum number of components, a positive-feedback active filter that has a continuously tunable cutoff frequency from 20 hertz to 20 kilohertz can be built. Additionally, the inexpensive filter provides switch-selectable low-pass or high-pass responses with either Bessel (RC) or Butterworth (maximally flat) characteristics. The skirt rolloff is 40 decibels per decade.

Basically, the filter consists of amplifier A_1 , two equal variable resistors (designated as R), and two equal capacitors (designated as C). A four-pole switch, S_1 , interchanges the resistors and capacitors to vary filter response between high-pass and low-pass. The filter's

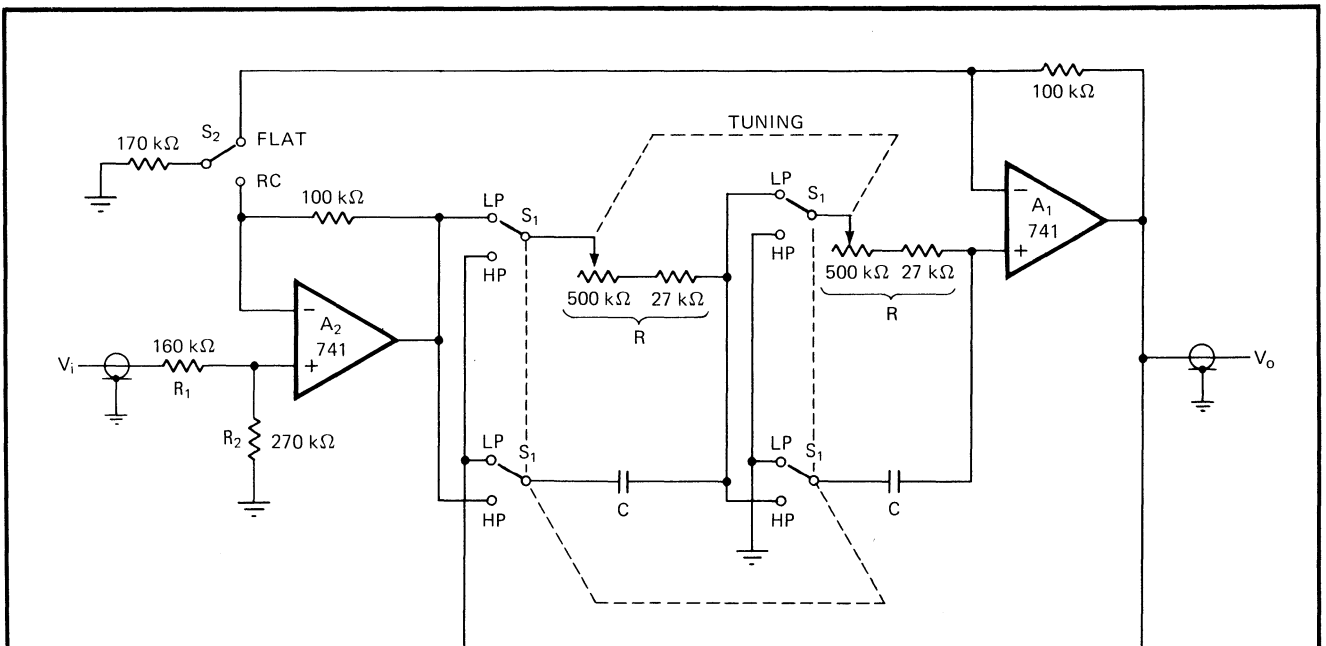
cutoff frequency can be written as:

$$\omega_0 = 1/RC$$

Another switch, S_2 , changes the filter's characteristic. With S_2 at its RC position, the gain of amplifier A_1 is unity, giving the filter a Bessel characteristic. With S_2 at its "flat" position, A_1 's gain becomes 1.59, which produces a Butterworth function. The corresponding gains for amplifier A_2 are 1.59 and unity, so that the gain product from A_2 's noninverting input to the output is 1.59 for either setting of switch S_2 . Resistors R_1 and R_2 reduce over-all gain to unity for easy cascading.

Output offset voltage, as well as its variation with tuning, may be zeroed out by applying conventional nulling methods at amplifier A_1 . The slew rate of the type 741 operational amplifier limits the flat portion of the high-pass response to about 40 kilohertz at a 3-volt peak-to-peak signal level. If two filters are cascaded, bandpass and band-reject responses can be added. □

Versatile filter. Positive-feedback active filter can be tuned continuously from 20 hertz to 20 kilohertz. Two switches provide choice of output—either low-pass (LP) or high-pass (HP) response having either Bessel (RC) or Butterworth (flat) characteristic. Switch S_1 interchanges resistors and capacitors that determine cutoff frequency, while switch S_2 changes gain of amplifiers A_1 and A_2 .



| CUTOFF FREQUENCY | C (μF) |
|------------------|--------|
| 20 Hz – 200 Hz | 0.02 |
| 200 Hz – 2 kHz | 0.002 |
| 2 kHz – 20 kHz | 0.0002 |

R: ALLEN-BRADLEY TYPE J, ±10%
C: POLYSTYRENE, MALLORY TYPE SX, ±5%

Synchronous ramp generator maintains output linearity

by D. M. Brockman
Boeing Co., Seattle, Wash.

With complementary-MOS analog switches, a synchronous ramp generator can be built without the need for expensive ladder networks or costly amplifiers. This circuit is intended for use in a multichannel analog-to-digital converter system where digital words must be developed to represent transducer outputs.

When triggered, the circuit generates a linear ramp having time and voltage parameters that are independent of component tolerances, power-supply voltage, and clock rate. The ramp output is synchronous with a binary or binary-coded-decimal counter and always runs from a negative reference voltage at the counter's zero state to a positive reference voltage at the counter's full-scale state. The generator's ramp output can be used as the reference signal for comparator-type analog-to-digital converters.

The ramp is generated by integrator A_1 . Switch S_2 is initially closed, and switches S_1 and S_3 are open, clamping A_1 's output to $-V_{ref}$. The counter is kept reset by flip-flop FF_1 .

When the circuit is triggered, the counter begins to run, S_2 is opened, and S_1 is closed. Integrator A_1 begins to charge linearly at a rate determined by time constant R_1C_1 and the output voltage produced by integrator A_2 .

After the counter reaches full scale, switch S_1 opens and stops the ramp, while switch S_3 closes and starts the comparison cycle.

During the comparison cycle, A_1 's output is inverted by amplifier A_3 and summed with $+V_{ref}$ by integrator A_2 . If the sum is not zero, A_2 charges toward a voltage (and polarity) that will make the sum zero at the next comparison cycle. When the counter reaches full scale for the second time, the comparison cycle is ended, switch S_3 is opened, switch S_2 is closed, and the counter and flip-flop FF_1 are reset.

This generate/compare process is repeated each time the circuit is triggered. And, after a few cycles, the output voltage of integrator A_2 will be just large enough to drive integrator A_1 to $+V_{ref}$ in the time required for the counter to reach full scale.

Inverter A_3 is provided with a gain adjustment to compensate for tolerances on integrator A_2 's summing resistors and to allow the peak ramp voltage to be set exactly to $+V_{ref}$. Time constant R_1C_1 must be chosen so that integrator A_2 does not saturate. And time constant R_2C_2 must be selected for circuit stability:

$$R_2C_2 = T^2/R_1C_1$$

where T is the ratio of the full-scale count to the clock rate.

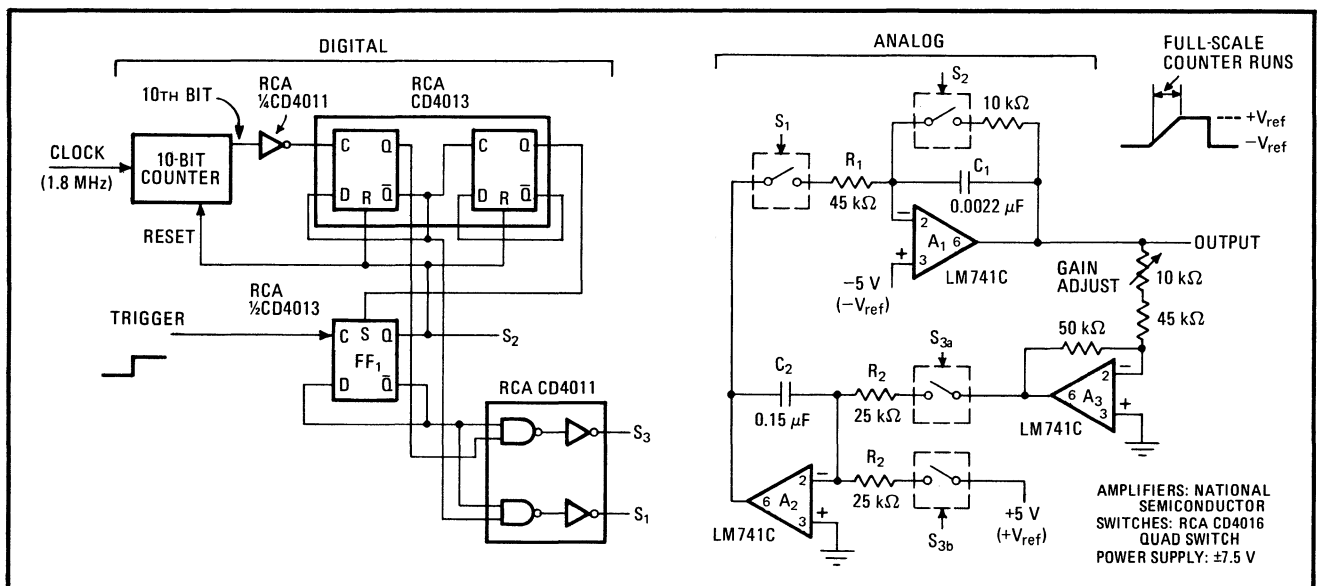
The circuit's stability factor becomes:

$$S.F. = R_1R_2C_1C_2/T^2$$

If the stability factor is equal to one, the circuit will respond to step changes in $+V_{ref}$ without overshoot. If the factor is greater than one, the generator's response will be underdamped.

The component values shown are for a 1.8-megahertz clock rate and a full-scale count of 1,024. □

Automatic compensation. Synchronous ramp generator uses low-cost complementary-MOS analog switches instead of high-priced ladder networks. Closed-loop circuitry automatically corrects ramp slope for small changes in component values, clock rate, or supply voltage. Ramp output climbs from $-V_{ref}$ to $+V_{ref}$ as counter runs from its zero state to its full-scale count. For this circuit, clock rate is 1.8 megahertz.



Astable multivibrator needs only one capacitor

by Glen Coers
Texas Instruments, Dallas, Texas

Two large capacitors are required for most astable multivibrator designs. But, by using a programmable unijunction transistor (PUT), one of these can be eliminated, and only one inexpensive Mylar capacitor is needed.

The multivibrator in the diagram, for example, is designed to operate at 1 hertz. Its output symmetry can be adjusted with timing resistors R_1 and R_2 —resistor R_1 controls the negative output pulse width (t_1), while resistor R_2 controls the positive output pulse width (t_2). The values of R_1 and R_2 , along with the value of capacitor C , determine the output pulse durations:

$$R_1 = 1.4t_1/C$$

$$R_2 = 2.5t_2/C$$

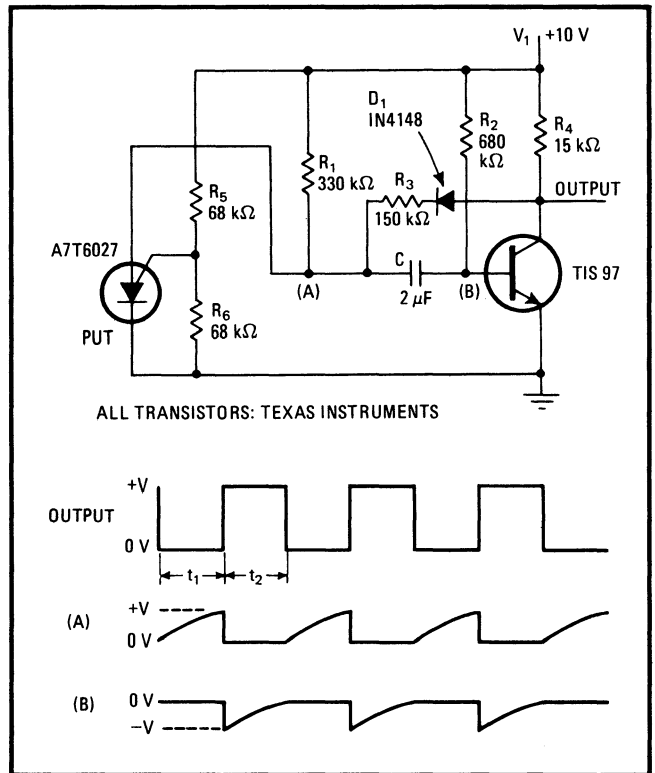
At the start of the circuit's cycle, the PUT is off, the bipolar transistor is on, and capacitor C charges through resistor R_1 . When the PUT's peak-point emitter voltage (V_p) is reached, the PUT triggers and turns off the bipolar transistor, allowing this device's collector voltage to go toward the supply level.

Diode D_1 and resistors R_3 and R_4 provide latching current for the PUT. The value of resistor R_3 can be determined by:

$$R_3 = [V_1 - (V_V + V_D)]/I_V$$

where V_1 is the supply voltage, V_D is the diode drop, V_V is the PUT's valley-point voltage, and I_V is its valley-point current.

When capacitor C discharges through resistor R_2 , the bipolar transistor is turned on so that the latching current is removed from the PUT. This device's gate voltage (V_G) then rises to the level set by the voltage divider formed by resistors R_5 and R_6 . The PUT then turns off,



ALL TRANSISTORS: TEXAS INSTRUMENTS

Trimming down to single capacitor. Programmable unijunction transistor (PUT) eliminates the second capacitor in astable multivibrator circuit. When PUT is off, bipolar transistor is on and capacitor C charges through resistor R_1 until PUT triggers, turning off the bipolar. As capacitor C discharges through resistor R_2 , the PUT remains on until the bipolar conducts. Capacitor C then charges again.

capacitor C again begins to charge through resistor R_1 , and the cycle repeats.

The value of timing resistor R_1 must be small enough to meet the PUT's peak-point current (I_p) requirement. And the value of the other timing resistor, R_2 , must be small enough to assure that the bipolar transistor will turn on. □

Automobile ignition system is rugged and reliable

by J.P. Thomas
Litton Industries, Litton Systems (Canada) Ltd., Rexdale, Ont., Canada

Capacitive-discharge ignition systems permit engine performance to be maintained over an extended period by reducing automotive component degradation due to mechanical wear. With a capacitive-discharge system, ignition voltages are high, allowing sparkplug gap spacing to vary considerably without affecting engine performance. But ignition point current is kept low so that point erosion is significantly reduced.

The failure of a capacitive-discharge ignition system

can usually be attributed to erratic triggering of the silicon-controlled rectifier, the heart of the circuit. Erratic triggering can generally be traced to either poor design of the trigger circuit or improper elimination of point bounce.

In contrast, here is a capacitive-discharge ignition system that provides reliable SCR triggering over a broad range of operating conditions and offers an engine overspeed cutout as an additional feature. The system can operate over the temperature range of -70°F to $+150^\circ\text{F}$ and over the supply-voltage range of 7 to 20 volts.

Unijunction transistor Q_1 generates trigger pulses for the SCR by discharging capacitor C_1 when transistors Q_2 and Q_3 are both saturated. Engine overspeed protection is provided by transistors Q_3 , Q_4 , and Q_5 , diodes D_1 , D_2 , and D_3 , and a speed limit set by the values of resistor R_1 and capacitor C_1 . Transistor Q_4 and its associated components act as a current source that charges capacitor

Programmable monostable is immune to supply drift

by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

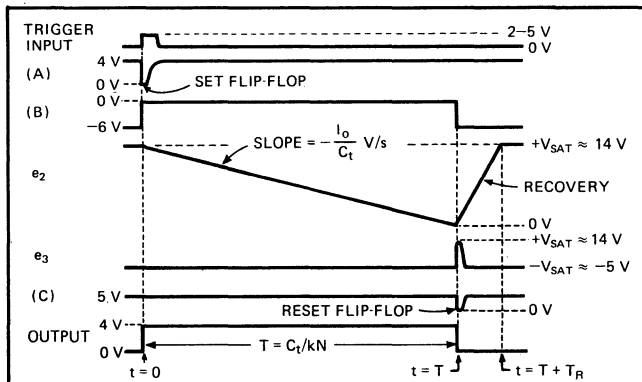
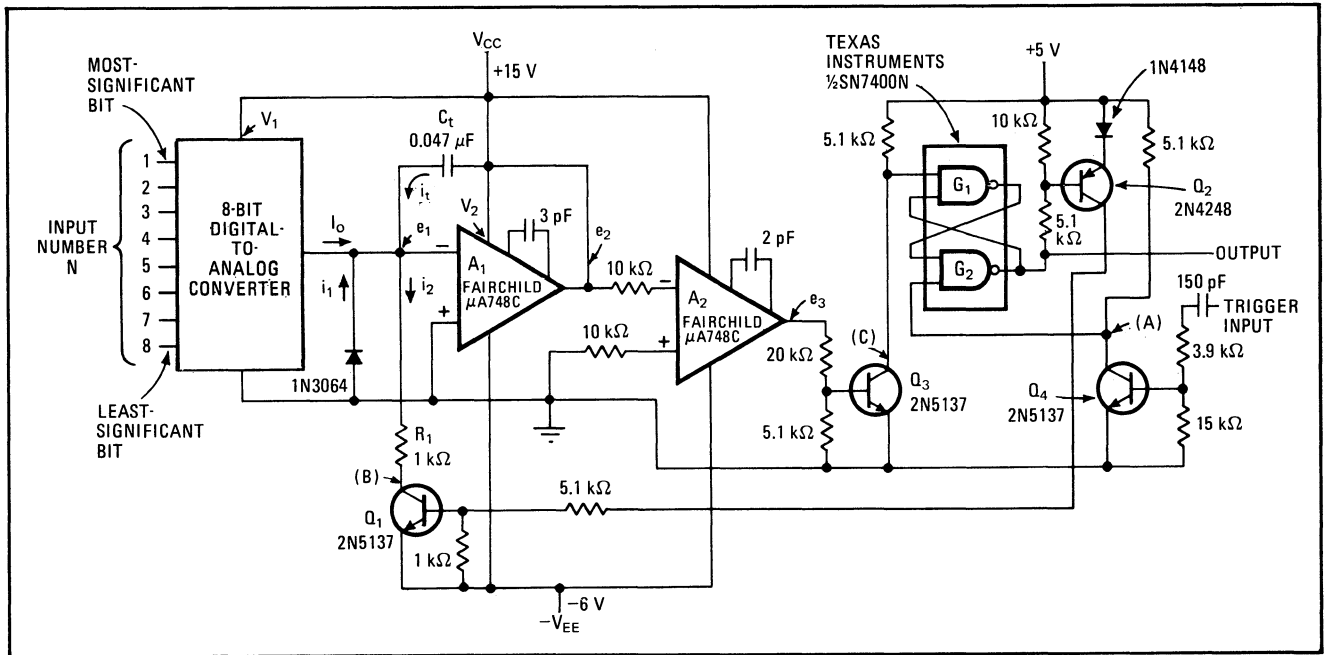
A monostable multivibrator with an output pulse width that is digitally programmable is, for all practical purposes, independent of power supply variations. The circuit's output pulse period varies only -0.0055% for a 1% change in the positive supply voltage and only $+0.0031\%$ for a 1% change in the negative supply voltage. The monostable is useful in computer-controlled test systems and real-time control systems where digit-

ally controlled pulse width or time delay is needed.

The circuit consists of a low-cost eight-bit digital-to-analog converter (one that does not have an internal reference), an integrator, a comparator, a flip-flop, and the necessary set-reset circuitry. Amplifier A_1 and capacitor C_t form the integrator, amplifier A_2 is the comparator, and NAND gates G_1 and G_2 make up the flip-flop. Transistors Q_1 and Q_2 allow the integrator's output voltage to be reset to the positive saturation voltage of amplifier A_1 , while transistors Q_3 and Q_4 enable the flip-flop to be set and reset.

Initially, the monostable's output is low, transistors Q_1 and Q_2 are fully on, and transistors Q_3 and Q_4 are off. Voltage e_1 is at (minus) the forward voltage drop of the diode at the converter's output, voltage e_2 is at $+V_{SAT}$, and voltage e_3 is at $-V_{SAT}$. The current, i_t , flowing through timing capacitor C_t is zero and:

Voltage-stable one-shot. Digitally programmable output pulse width of monostable multivibrator drifts less than 0.005% for 1% change in either positive or negative supply. The table shows that product of input number N and output period T is nearly constant over broad range of values. Amplifier A_1 acts as integrator, amplifier A_2 is comparator, and gates G_1 and G_2 are set-reset flip-flop.



| INPUT NUMBER N | OUTPUT PERIOD T | PRODUCT N x T |
|----------------|-----------------|---------------|
| 1 | 70.5 ms | 70.5 |
| 2 | 35.0 ms | 70.0 |
| 4 | 17.2 ms | 68.8 |
| 8 | 9.0 ms | 72.0 |
| 16 | 4.45 ms | 71.2 |
| 32 | 2.20 ms | 70.4 |
| 64 | 1.10 ms | 70.4 |
| 128 | 0.56 ms | 71.7 |
| 255 | 0.28 ms | 71.4 |
| 000 | 2.5 s | 0.0 |

$i_2 = i_1 + I_0$
 where I_0 is the output current of the d-a converter.

When a trigger input is applied at $t = 0$, it is differentiated, and transistor Q_4 is momentarily turned on fully. This sets the flip-flop, the monostable output goes high, and transistors Q_1 and Q_2 turn off, making currents i_1 and i_2 zero. Now current i_t is equal to $-I_0$, causing voltage e_2 to become a linear ramp that descends from $+V_{SAT}$ towards $-V_{SAT}$ at a rate of $-I_0/C_t$ volts per second. Voltage e_1 is maintained at virtual ground.

Once voltage e_2 reaches zero at $t = T$ (where T is the monostable pulse width), the comparator (A_2) output switches from $-V_{SAT}$ to $+V_{SAT}$. Transistor Q_2 now turns fully on, resetting the flip-flop and causing the monostable output to go low.

Transistors Q_1 and Q_2 then turn fully on, producing a reset current of:

$$i_t = V_{EE}/R_1 - I_0$$

This current causes voltage e_2 to rise linearly towards $+V_{SAT}$ at a rate of $(V_{EE}/R_1 - I_0)/C_t$ volts per second.

Voltage e_2 reaches $+V_{SAT}$ at $t = T + T_R$, where T_R is the monostable recovery time:

$$T_R = V_{SAT}C_t/(V_{EE}/R_1 - I_0)$$

The monostable is now ready to accept the next trigger.

The output current for the d-a converter is given by:

$$I_0 = kV_1N$$

where k is a constant that equals 0.68 micromho, V_1 is the converter's supply voltage, and N is the binary input number. The monostable pulse width can be written as:

$$T = V_{SAT}/(I_0/C_t) = (V_2 - 0.5 \text{ V})/(I_0/C_t)$$

where V_2 is the integrator's positive supply voltage. Substituting for current I_0 in this equation yields:

$$T = (V_2 - 0.5 \text{ V})C_t/kV_1N$$

Since V_1 and V_2 are 15 v—a much higher voltage level than 0.5 v—this equation can be approximated by:

$$T = C_t/kN$$

which indicates that T should be very nearly independent of the power-supply voltage.

The table in the figure shows the product of $N \times T$ to be almost constant over a range of input numbers. □

Getting power and gain out of the 741-type op amp

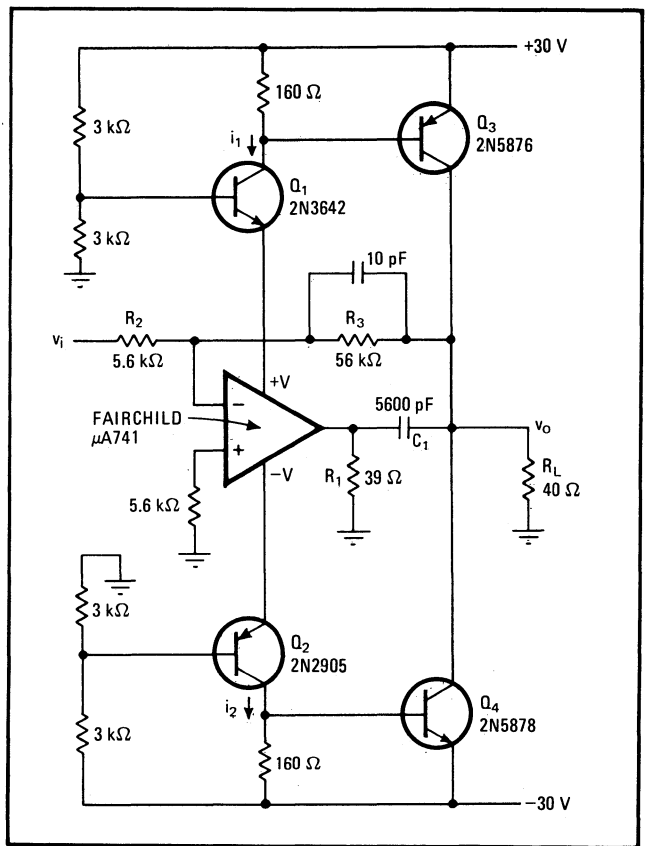
by Pedro P. Garza, Jr.
 General Electric Co., Apollo and Ground Systems, Houston, Texas

The popular 741-type operational amplifier can be used as the basis for a high-voltage power amplifier that is capable of delivering 22 watts of peak power at an output voltage swing of 60 volts. Voltage gain for the amplifier is 10, and its frequency response is flat from dc to 30 kilohertz.

Most integrated-circuit op amps are not designed to accept more than 36 v across their power pins. Here, therefore, transistors Q_1 and Q_2 protect the 741-type op amp by maintaining a 30-v differential across the device's power pins. The base of transistor Q_1 is biased at 15 v by the voltage divider network formed by the 3-kilohm resistors, while Q_1 's emitter is at 15 v minus its base-emitter voltage drop. The biasing arrangement for transistor Q_2 is similar.

Since a 39-ohm resistance (resistor R_1) is connected to the op amp's push-pull output, substantial currents will be drawn by the device. Currents i_1 and i_2 , which appear at the collectors of Q_1 and Q_2 , are used to generate the base drive voltage for the power-output stage, made up of transistors Q_3 and Q_4 . The power-output stage has a wider frequency response than the 741-type op amp. The negative feedback path through capacitor C_1 provides a frequency roll-off characteristic similar to that of the op amp, thus assuring unconditional stability.

The resistance ratio of resistor R_3 to resistor R_2 determines the amplifier's voltage gain. If the op amp's input-offset voltage is nulled out and resistors having tolerances of $\pm 0.25\%$ are used for R_2 and R_3 , the power amplifier's linearity error will be within 0.4% over the output voltage range of $+29.8 \text{ v}$ to -29.8 v .



Power amplifier. Widely used 741-type op amp is heart of 22-watt power amplifier that supplies 60-volt output swing. Transistors Q_1 and Q_2 keep peak-to-peak voltage across op amp's power pins at 30 v so that device's 38-v rating is not exceeded. Using low-value load resistor (R_L) at op-amp output produces currents (i_1 and i_2) large enough to drive output power stage of transistors Q_3 and Q_4 .

Output voltage swings of more than 60 v are possible if transistors with higher collector-base breakdown-voltage ratings are used along with higher power supply voltages. □

Solid-state dpdt switch provides current reversal

by Don DeKold
Santa Fe Junior College, Gainesville, Fla.

When the dc current flowing through a load is periodically reversed, the alternating square-wave voltage developed across the load has a peak-to-peak amplitude that is twice the magnitude of the power-source voltage. A circuit that provides periodic current reversal is useful for driving loads that otherwise might become polarized by the steady passage of a unidirectional current.

Dc-to-ac inverters may be used for periodic current reversal, but they usually require a power transformer of relatively large size and weight. Additionally, these circuits frequently have sizable standby currents because they generally contain saturating transformers, making them inefficient under light load conditions.

The solid-state circuit in the diagram solves these problems. It acts as a double-pole double-throw switch that periodically reverses the current through its load resistor, R_L .

Transistors Q_1 and Q_2 are the active elements in an ordinary astable multivibrator. They alternate between saturation and cutoff at the multivibrator's basic pulse-repetition rate. Transistors Q_3 and Q_4 , which are driven by transistors Q_1 and Q_2 , respectively, also alternate between saturation and cutoff, but are 180° out of phase with Q_1 and Q_2 .

The load-driver section of the circuit is made up of four Darlington pairs, labeled transistors Q_5 through Q_8 in the figure. A single pnp pair, such as the one designated transistor Q_5 , is connected in complementary fashion to an npn pair, such as the one identified as transistor Q_6 . Each Darlington pair is an output stage that is either saturated or cutoff, depending on the operating state of transistors Q_1 through Q_4 .

Diagonally opposite output stages (such as transistors

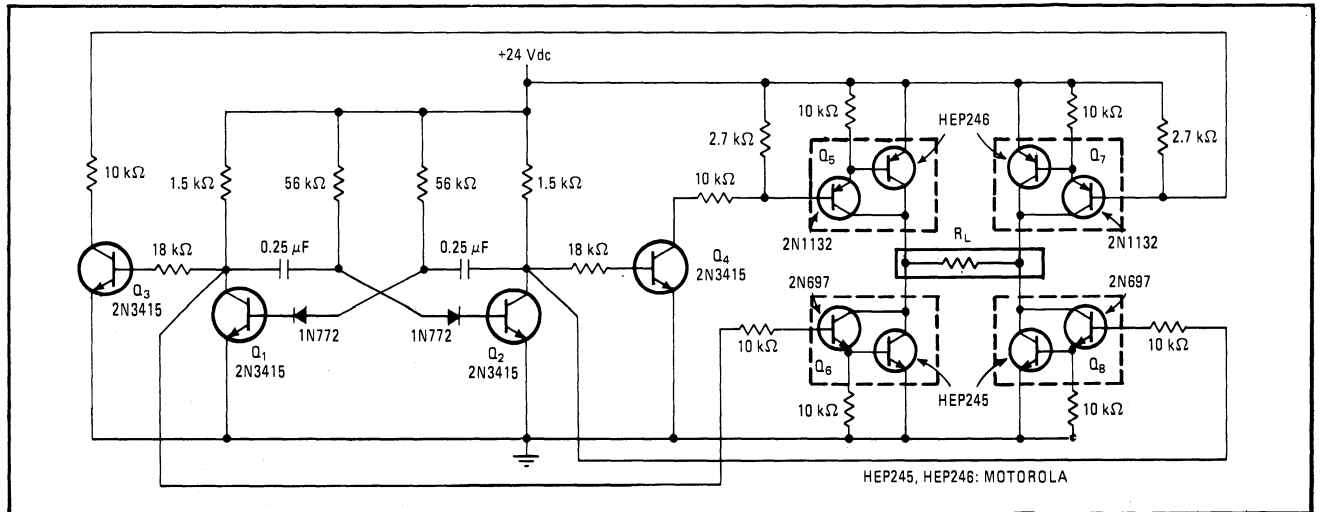
Q_5 and Q_8) are switched on at the same time as the two other diagonally opposite pairs (transistors Q_6 and Q_7) are switched off. This condition holds for half of the multivibrator's period and reverses for the other half, as indicated by the table.

The circuit's efficiency is very high because practically all of the supply voltage is applied across the load during each half of the operating cycle. The transistor states change at the pulse-repetition rate of the multivibrator, producing an alternating current through the load. In effect, the circuit is a solid-state double-pole double-throw switch that is toggled at the frequency of the multivibrator. If the multivibrator stalls or does not start when power is applied, both transistors Q_1 and Q_2 will saturate, cutting off the other devices and preventing any load current from flowing.

With the components shown, the circuit supplies an alternating current of 1.6 amperes to a 24-volt load. Standby current is about 25 milliamperes, and the multivibrator frequency, which is unaffected by loading, is 57 hertz. If desired, a heavier load can be driven, since the type HEP245 and HEP246 transistors are rated at 3 A. The supply voltage, of course, may be any value that does not exceed device-breakdown voltages.

Operating frequencies in the kilohertz range can be achieved by merely decreasing the values of the two multivibrator capacitors. If a higher output voltage is wanted, the circuit can directly drive a step-up transformer, but arc-suppression diodes must be placed across each output stage. Loading of the output must never short either terminal to ground. □

| OPERATING CYCLE | | | |
|-----------------|-----------|-------------|-----------|
| FIRST HALF | | SECOND HALF | |
| Q_1 ON | Q_2 OFF | Q_1 OFF | Q_2 ON |
| Q_3 OFF | Q_4 ON | Q_3 ON | Q_4 OFF |
| Q_6 OFF | Q_7 OFF | Q_6 ON | Q_7 ON |
| | Q_5 ON | | Q_5 OFF |
| | Q_8 ON | | Q_8 OFF |



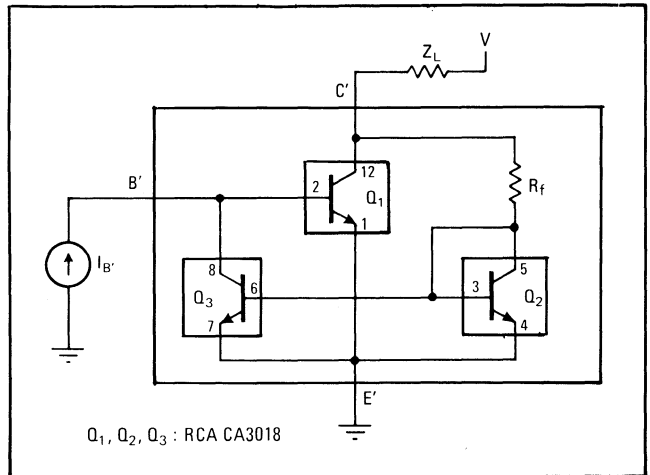
Current-reversal switch. Solid-state circuit periodically reverses load current, making amplitude of square-wave load voltage twice the level of supply voltage. Operating frequency is determined by astable multivibrator formed by transistors Q_1 and Q_2 . Four Darlington pairs, labeled transistors Q_3 through Q_8 , make up the output stages. Diagonally opposite pairs are on while the other two pairs are off.

Negative-resistance generator has controllable response

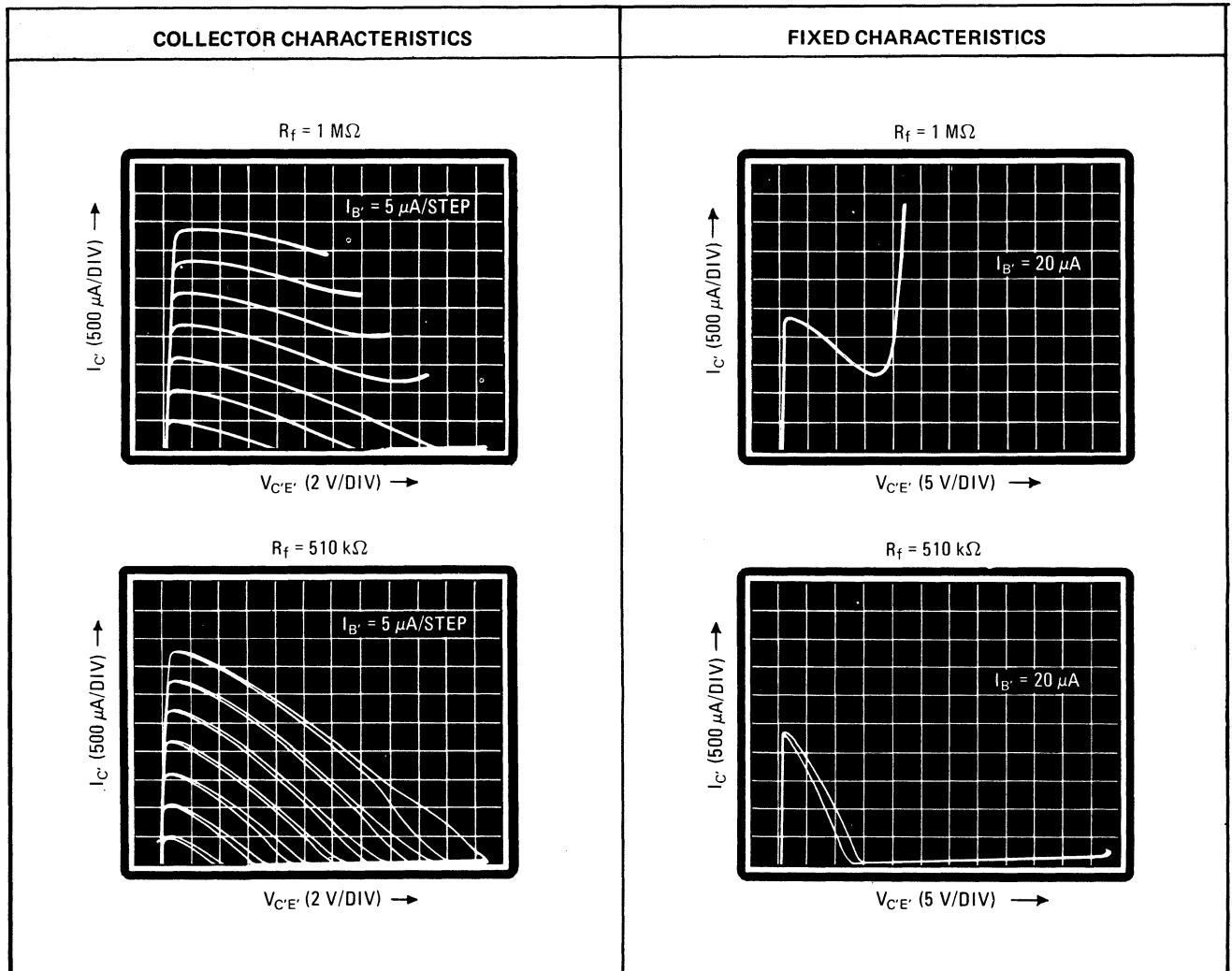
by Samuel E. Bigbie
 IBM General Systems Division, Boca Raton, Fla.

A negative-resistance generator, consisting of three matched transistors, has a current-voltage characteristic that varies with feedback resistance, but not with frequency. When driven by a current source and loaded by an LC resonant circuit, the generator can be operated as a self-starting sinusoidal oscillator. It also can be used for monostable, bistable, or astable pulse generation, as well as oscillator stabilization and switching networks.

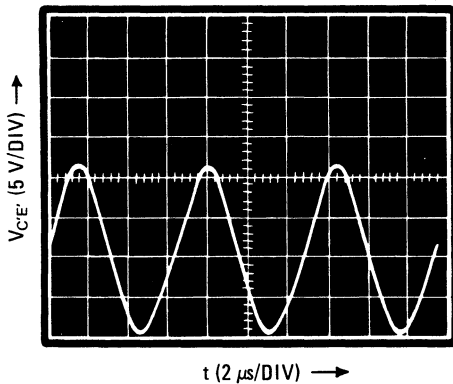
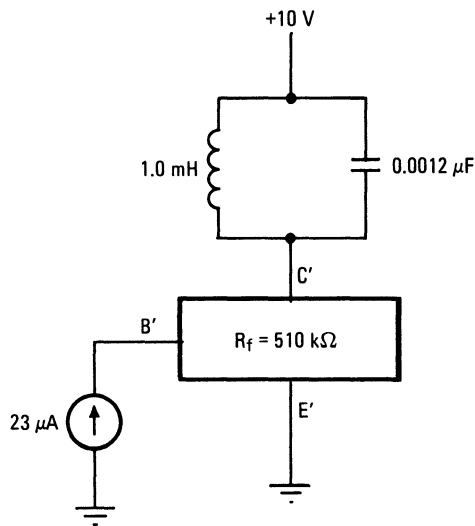
The maximum collector current of transistor Q_1 depends on the amount of bias current available at its base terminal. Feedback resistor R_f , along with transistors Q_2 and Q_3 , make up a voltage-to-current converter that decreases the base drive of transistor Q_1 when this



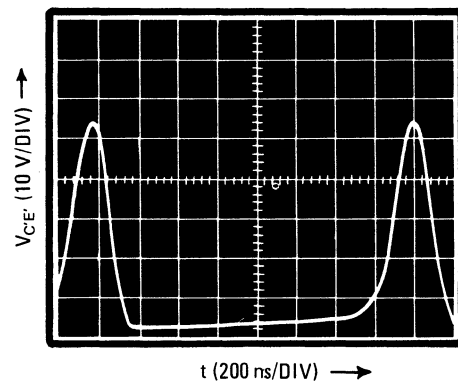
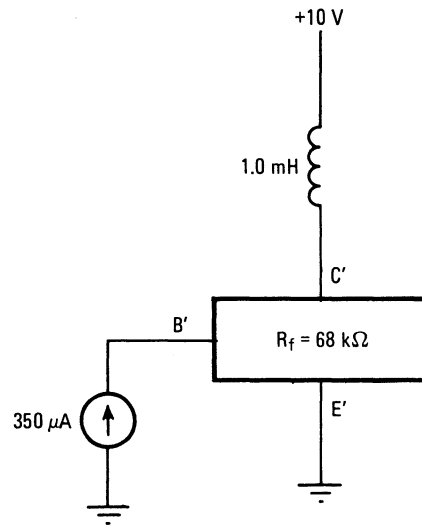
Positively negative. Three matched transistors form negative-resistance generator with stable, predictable operating characteristics. Circuit can be treated as transistor that develops negative impedance at terminal C' . Transistors Q_2 and Q_3 and resistor R_f decrease base current of transistor Q_1 whenever Q_1 's collector voltage increases. Circuit makes dependable oscillator or pulse generator.



SINUSOIDAL OSCILLATOR



ASTABLE PULSE GENERATOR



device's collector voltage is increasing.

The negative resistance appearing at Q_1 's collector is present at frequencies from dc to several megahertz. The upper frequency limit is determined by the frequency response of both transistor Q_1 and the voltage-to-current converter.

The generator circuit is effectively a three-terminal transistor (with pins labeled B', C', and E'). An input current source provides the base current for transistor Q_1 , while resistor R_f determines the amount of current fed back to Q_1 's base. Because transistors Q_2 and Q_3 are a matched pair and their bases are connected in common, their collector currents will be nearly equal.

As the base current supplied to transistor Q_1 increases, the voltage drop across load impedance Z_L also increases, lowering the potential at Q_1 's collector. This lowered potential decreases the collector current through transistors Q_2 and Q_3 . The reduced collector current through transistor Q_3 represents an increased

impedance at Q_1 's base terminal. (A decrease in Q_1 's base current has the opposite effect, since Q_3 's collector current will be reduced.)

The circuit's operating characteristics are illustrated by the scope traces showing generator performance for two different values of resistor R_f , and for both a fixed and changing bias current. As can be seen, the negative-resistance slope becomes steeper as the value of R_f decreases, from 1 megohm to 510 kilohms, in this instance.

When the load impedance is a parallel LC tank circuit, the negative resistance generator acts as a sinusoidal oscillator, as shown in the figure. Using only an inductor as the load impedance yields an astable pulse generator, which has an output pulse amplitude that equals the breakdown voltage of the combined transistors between terminals C' and E'. □

BIBLIOGRAPHY

Millman, Jacob, and Taub, Herbert, *Pulse, Digital and Switching Waveforms*, McGraw-Hill Book Co., New York, 1965, pp.452-512.

Low-distortion modulator tests hi-fi a-m tuners

by M.J. Salvati
Sony Corp. of America, Long Island City, N.Y.

Most commercially available signal generators do not hold distortion to a level that is low enough to test the frequency response and distortion characteristics of the a-m tuners found in today's high-fidelity equipment. The amplitude modulator shown, however, supplies amplitude-modulated rf signals at a distortion level of less than 0.15%.

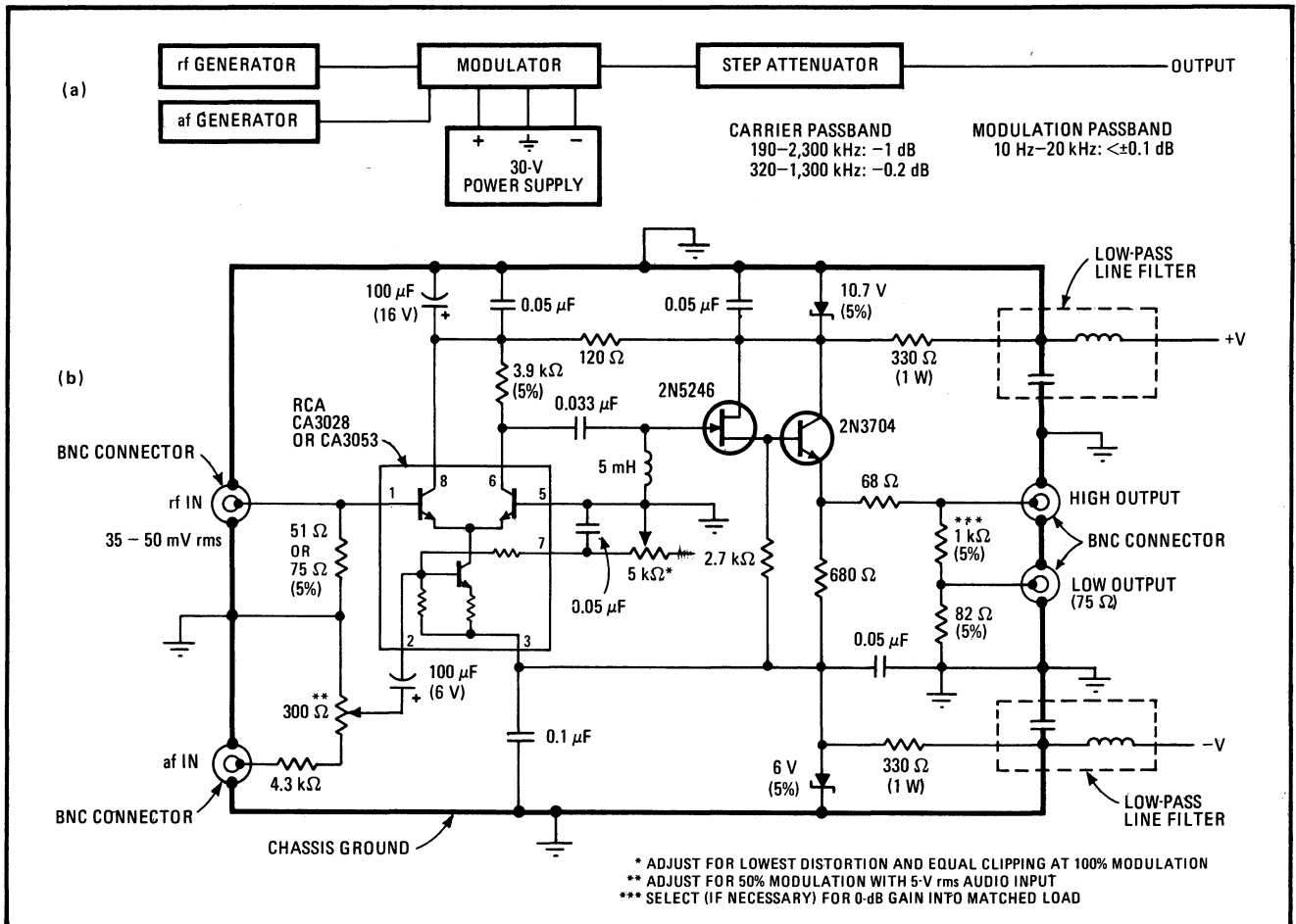
As indicated in the block diagram (a), the modulator (b) is used in conjunction with standard radio-frequency and audio-frequency signal sources. The output level of the over-all test system can be adjusted exactly with the step attenuator that follows the modulator and the vernier level control that is generally included on the rf generator. Also, the modulator gain (for the low-impedance output) can be set at 0 decibels into a matched load, allowing the absolute value of the system's output level to be easily read out from the step attenuator setting and the rf-generator setting.

The rf carrier, which has a root-mean-square amplitude of 35 to 50 millivolts, is applied to the differential input of the IC differential cascode amplifier. And the af signal drives the current-source transistor for this IC's differential transistor pair. Since the current-source transistor controls the gain of the differential pair, the af signal can vary the instantaneous gain of these two transistors, producing up to 100% amplitude modulation of the carrier signal.

The modulated carrier is coupled to the source-follower/emitter-follower combination through a high-pass filter, so that just the carrier and sidebands appear at the circuit's output. The source-follower/emitter-follower combination is essentially an impedance transformer that provides a large current gain for driving low-impedance loads.

The modulator's low output has an impedance of 75 ohms, which can easily be changed to 50 ohms. The circuit's input impedance can also be either 50 or 75 ohms, depending on the value chosen for the input resistor. The high output can drive a low-distortion detector for adjusting or evaluating modulator performance.

Output percent modulation can be indicated by the output-level setting of the af generator (a Krohn-Hite 4100A, in this case) by calibrating the circuit. Although the IC amplifier requires only a 400-mV input for 100% modulation, the modulator can be calibrated with the



Checking out a-m tuners. Amplitude modulator produces less than 0.15% total harmonic distortion. Equipment setup (a) shows that modulator (b) requires only one power supply. Integrated differential cascode amplifier accepts rf carrier input, as well as af modulation input, giving modulated carrier at its output. Combination source-follower/emitter-follower provides high current gain for driving low-impedance loads.

300-ohm potentiometer. Here, the circuit produces 10% modulation per volt rms of the af input.

The modulator exhibits only 0.11% total harmonic distortion when providing 30% modulation for a 400-

hertz af input and a 1-megahertz rf carrier having an amplitude of 50-mv rms. Only a single 30-volt power supply is needed—neither its positive nor negative terminals is grounded. □

Programable multivibrator is four-in-one circuit

by Edward Beach

McGraw-Hill Continuing Education Co., Washington, D.C.

One inexpensive transistor-transistor-logic quad dual-input NAND gate and a few other components make up a multivibrator that can be programmed for four functions—a simple latch, a monostable multivibrator, an astable multivibrator, or a retriggerable monostable multivibrator. The circuit employs a discrete timing circuit, rather than a conventional TTL timer, to allow a wide range of values to be used for timing components.

The table summarizes the operation of the circuit. With input A held low (to ground), gate G_1 shorts out timing capacitor C_t through diode D_1 , and gates G_2 and G_3 operate as a simple reset-set latch. When input A is held high, the circuit becomes a monostable multivibrator. A negative-going trigger (B) sets the latch, removing the short from the capacitor. Now capacitor C_t charges toward the supply voltage (5 v) through resistor R_t until point 1 reaches approximately 3.2 v. The regenerative switch formed by transistors Q_1 and Q_2 then rapidly discharges capacitor C_t , resetting the latch.

The circuit's output pulse duration (T), which equals approximately $1.3R_tC_t$, can be adjusted from about 280 nanoseconds to well over several hours in length. For the longest period, requiring timing component values of 10 megohms and 1,000 microfarads, a very low-leak-

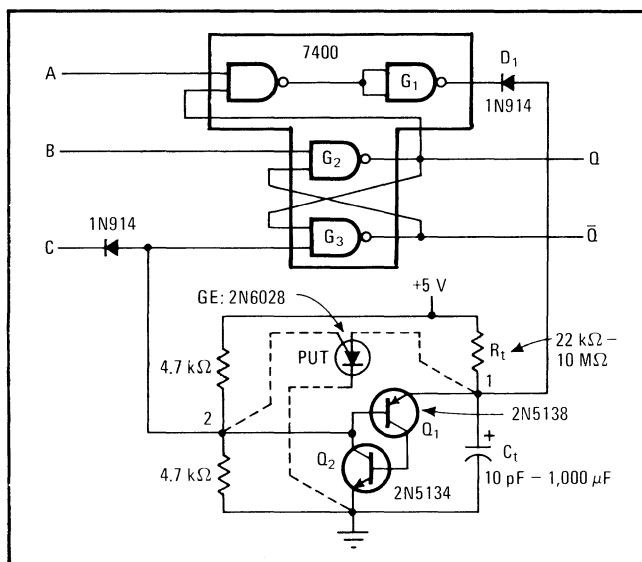
age capacitor must be used.

Input C acts as a direct clear for all circuit functions. Bringing C to ground potential clears the monostable by discharging capacitor C_t so that the circuit is ready for another input signal.

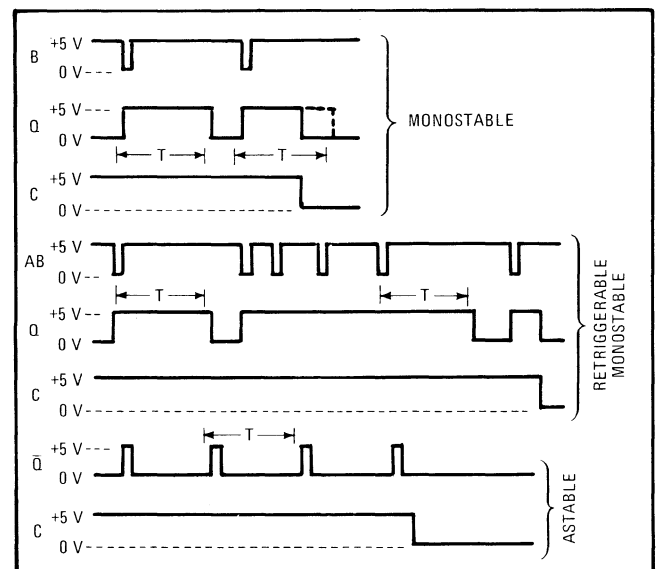
Tying inputs A and B together produces the retriggerable monostable multivibrator. Its timing period begins at the end of a negative-going trigger input. If the circuit has not timed out before the arrival of another trigger, capacitor C_t is discharged, and the timing cycle is started again.

Grounding input B while holding inputs A and C high allows the circuit to act as an astable multivibrator, producing positive pulses at its \bar{Q} output. Negative-going pulses could be taken from point 2, if desired.

A programmable unijunction transistor (PUT) can be used instead of transistors Q_1 and Q_2 . It is connected as shown in the schematic. □



| CIRCUIT FUNCTION | | | |
|------------------|---------|-------|---|
| A | B | C | OPERATING MODE |
| LOW | SET | RESET | R-S LATCH: B = SET, C = CLEAR |
| HIGH | TRIGGER | HIGH | MONOSTABLE: $T = 1.3 R_t C_t$, C = CLEAR |
| HIGH | LOW | HIGH | ASTABLE: \bar{Q} = OUTPUT, C = CONTROL |
| A TIED TO B | | HIGH | RETRIGGERABLE MONOSTABLE: C = CLEAR |



Versatile multivibrator. Input signals determine operating mode of four-function multivibrator, which can be a reset-set latch, a monostable multi, an astable multi, or a retriggerable one-shot. Discrete devices in the timing network permit output pulse period to range from 280 nanoseconds to more than several hours. The programmable unijunction transistor (PUT) can be used to replace transistors Q_1 and Q_2 .

Two-IC digital filter varies passband easily

by Andrew M. Volk
University of Wisconsin, Madison, Wis.

Only two integrated circuits—a dual monostable and a three-input NAND gate—are needed to build a digital filter that offers completely adjustable cutoff frequencies as well as excellent frequency stability. The bandpass filter is also independent of the duty cycle of the input waveform. It can be used in a variety of circuits, for instance, in tone-controlled devices or for fm demodulation of digital codes.

The input RC differentiator makes the filter independent of the duty cycle of the input. In (a), the lower and upper cutoff frequencies of the filter's passband are determined by the retriggerable monostable multivibrators. The output pulse length of the first monostable (MONO₁) is set to the period of the highest frequency of interest, while the output pulse length of the second

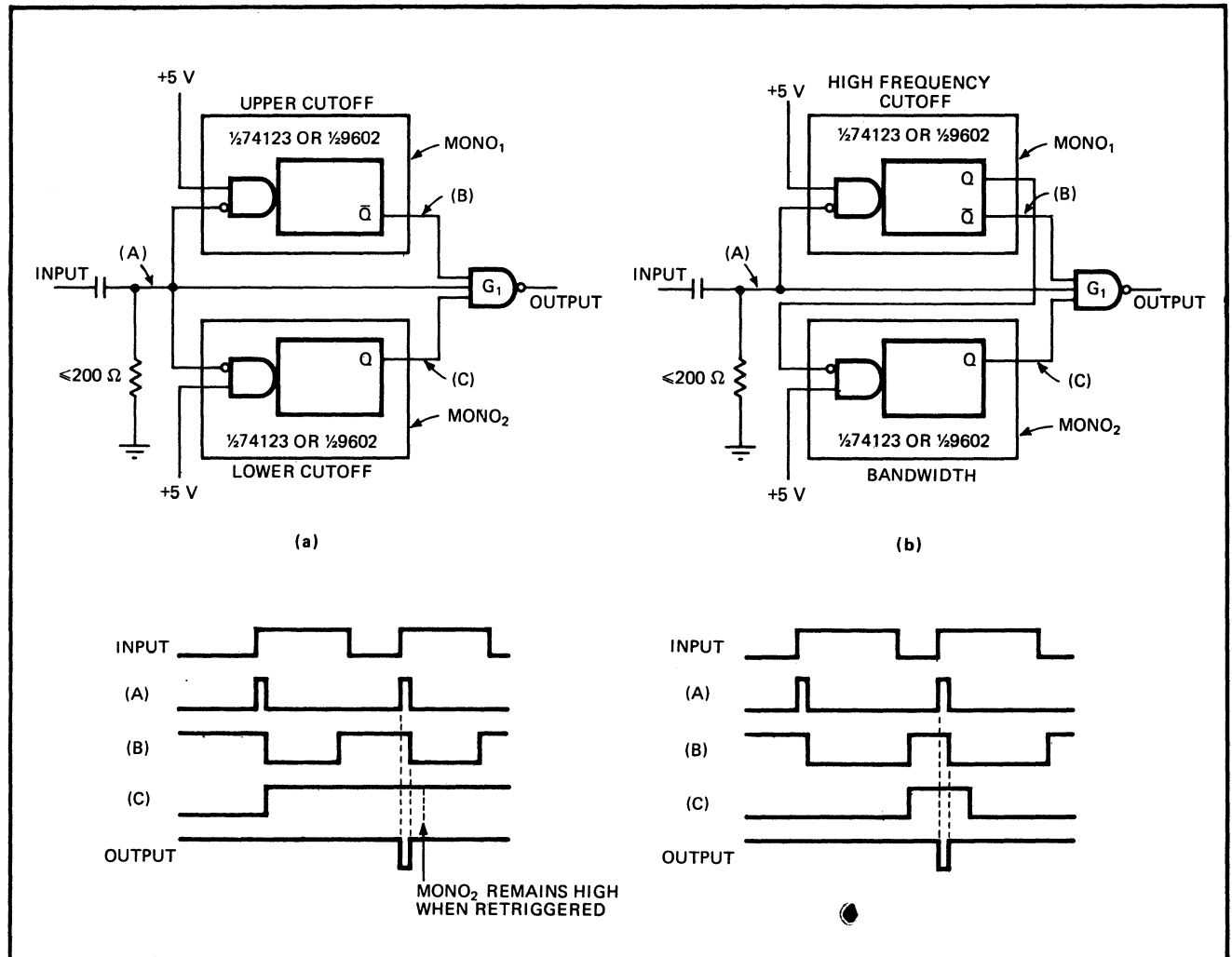
(MONO₂) is set for the lowest frequency wanted.

If an input pulse appears after MONO₁ times out but while MONO₂ is still high, there will be a pulse at the output of gate G₁. When the input frequency exceeds the upper cutoff, MONO₁ stays triggered (its \bar{Q} output remains low). When the input frequency is below the lower cutoff, MONO₂ times out (its Q output goes low). This prevents input pulses from passing through the output gate.

For the circuit in (b), MONO₁ sets the high-frequency cutoff, and MONO₂ sets the filter bandwidth. As in circuit (a), the input pulse reaches the output when MONO₁ has timed out and MONO₂ is high.

To obtain a constant output level when the input frequency is within the filter's passband, a retriggerable monostable that has its pulse length set for $1/f_{\min}$ can be placed at the output. The monostable will remain triggered as long as there are output pulses from gate G₁. However, there will be a time lag in the filter's response of $1/f_{\text{in}}$ for pickup and $1/f_{\min}$ for dropout.

For particularly critical applications or for high-speed operation, the input differentiator, made up of the passive RC network, should be replaced with a regular monostable, like a 74121-type or a 9603-type. □



Digital frequency selection. Bandpass digital filter built with two ICs is easily adjusted for lower and upper passband cutoffs. In (a), output pulse width of retriggerable monostable MONO₁ sets high-frequency cutoff, while MONO₂'s output pulse width sets low-frequency cutoff. In (b), MONO₁ determines upper cutoff frequency and MONO₂ determines bandwidth. The RC network differentiates all input waveforms.

C-MOS voltage monitor protects Ni-Cd batteries

by William Wilke
University of Wisconsin, Madison, Wis.

If nickel-cadmium batteries are permitted to discharge completely, they can be permanently damaged. To prevent this, a voltage monitor can be employed to turn off the equipment being supplied by the batteries when their voltage falls below a safe level. The monitor circuit shown draws as little as 0.5 microampere, has an adjustable voltage trip point and hysteresis, and it turns itself back on when the batteries are recharged.

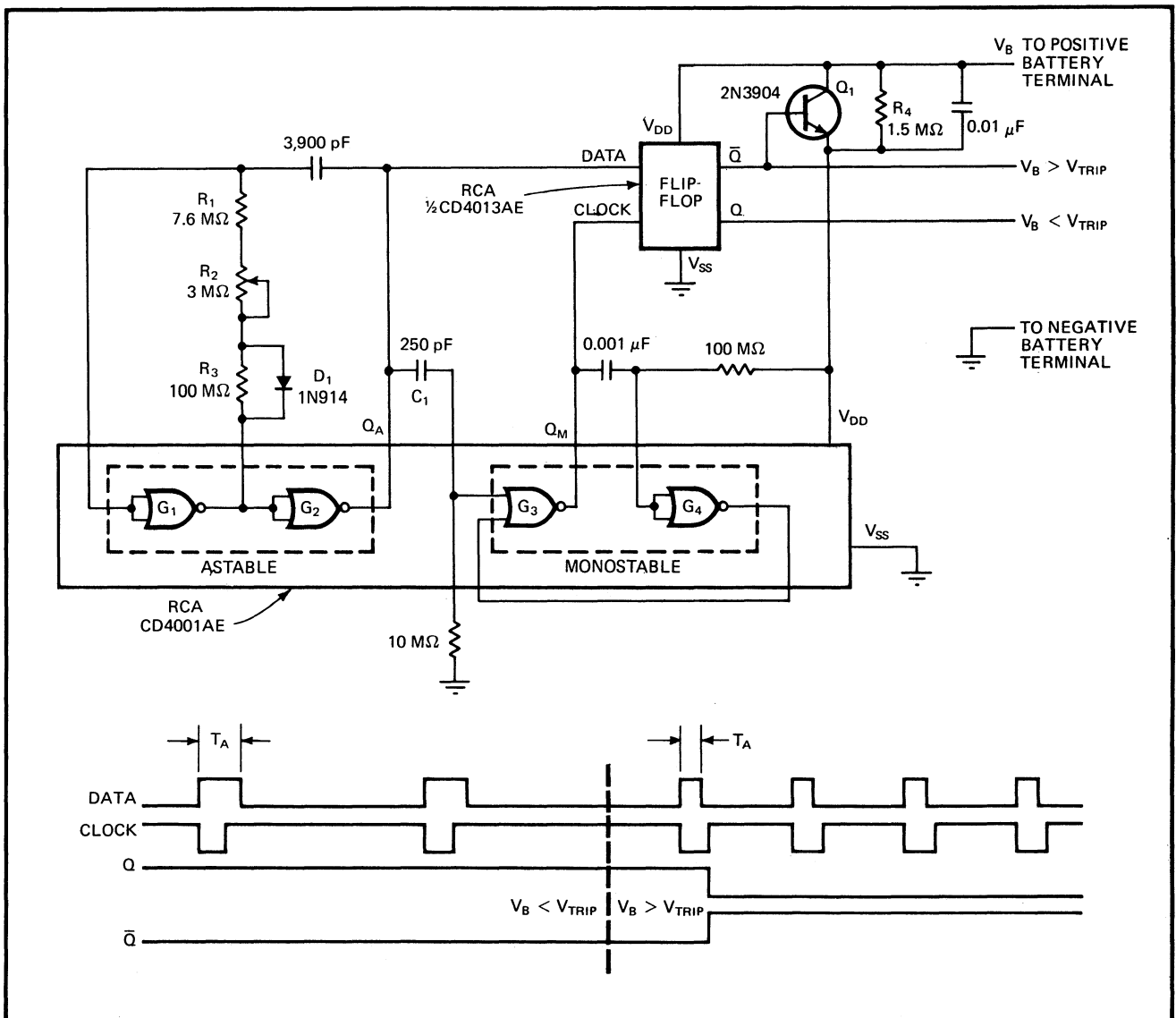
The circuit basically consists of two complementary-MOS multivibrators—a monostable and an astable—and a network that compares their outputs. NOR gates G_1

and G_2 form the astable multivibrator, which has a period that varies with changes in the supply voltage, V_{DD} , obtained from the battery. On the other hand, NOR gates G_3 and G_4 make up a positive-edge-triggered monostable multivibrator that has an output pulse width that remains relatively constant even with some changes in the supply voltage.

The astable output, Q_A , is coupled through capacitor C_1 to fire the monostable, and the output is also fed to the DATA input of a D-type flip-flop. The monostable's output, Q_M , drives the CLOCK input to this flip-flop.

Resistors R_1 and R_2 are adjusted so that the periods of the astable and the monostable are equal to each other when battery voltage V_B is at the desired trip voltage (V_{TRIP}). If battery voltage becomes higher than the trip voltage, the astable's period, T_A , decreases, and when the positive edge of the CLOCK pulse from the monostable reaches the flip-flop, its DATA input is low so that its \bar{Q} output goes high.

At battery voltages below the trip voltage, the



Battery watchdog. Voltage monitor for nickel-cadmium batteries detects when battery voltage (V_B) is above or below desired level (V_{TRIP}). Here the trip point is 3.6 volts, and hysteresis is 0.2 V. C/MOS circuitry keeps current drain to as little as 0.5 microampere. The period of the astable varies with changing battery voltage, while the period of the monostable stays constant. Circuit costs under \$6 to build.

astable's period increases. The flip-flop's DATA input, therefore, is still high when the clock fires, forcing the flip-flop's Q output to be high. In this way, the flip-flop Q and \bar{Q} signals indicate whether battery voltage V_B is less than trip voltage V_{TRIP} or V_B is greater than V_{TRIP} .

Diode D_1 and resistor R_3 are added to give the astable a duty cycle of approximately 10%. This addition assures that the output pulse width of the monostable remains independent of the rate at which the monostable is retriggered.

Circuit hysteresis is proportional to the value of re-

sistor R_4 , which bypasses transistor Q_1 . When battery voltage falls below V_{TRIP} , the flip-flop \bar{Q} signal goes low, shutting transistor Q_1 off and further lowering the effective V_{DD} supply voltage by the size of the IR drop across resistor R_4 .

For the components shown, the voltage monitor has a trip point of 3.6 volts, which is appropriate for three series-connected batteries. Hysteresis is 0.2 V, and current drain is 3 μA when V_B is greater than V_{TRIP} , but only 0.5 μA when V_B is less than V_{TRIP} . Total parts cost is approximately \$5.50. \square

Switching large ac loads with logic-level signals

by Lynn S. Bell, *Bell Engineering, Tucson, Ariz.*,
and R. M. Stitt, *University of Arizona, Tucson, Ariz.*

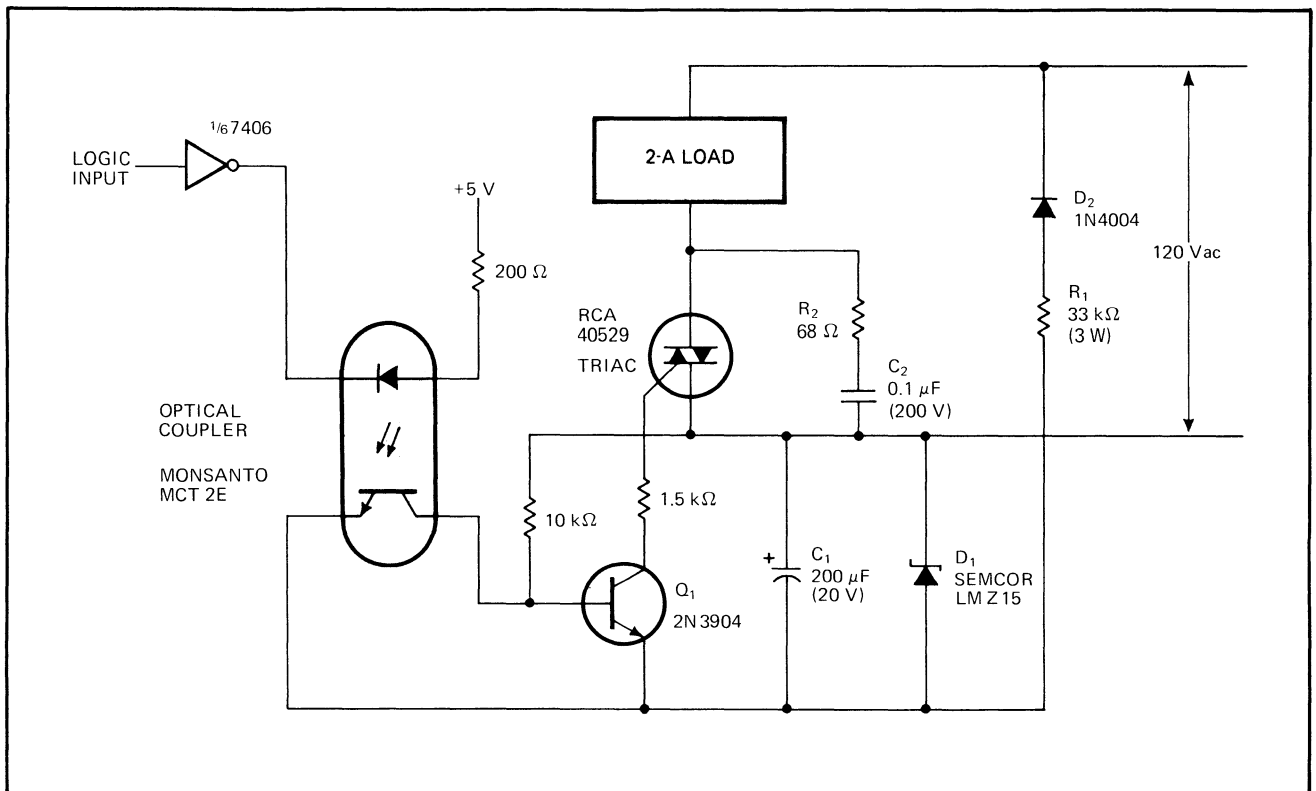
An optical coupler makes it possible for integrated-circuit logic signals to switch safely and without isolation problems ac loads as large as 2 amperes.

In the circuit, capacitor C_1 , zener diode D_1 , diode D_2 , and resistor R_1 provide a -15-volt supply, referenced to point A of the ac line source. A low-input logic signal to the inverter turns off both the light-emitting diode and

the phototransistor in the optical coupler. For this circuit, the coupler provides 2,500 v of isolation.

After the coupler turns off, transistor Q_1 saturates, supplying a current of -10 milliamperes to the gate of the triac and turning this device on so that the load is energized. The triac will stay on through a complete half-cycle of the line voltage, once the logic input to the inverter goes low. The triac turns off at the first zero crossing of the load current that occurs after the logic input goes high.

Resistor R_2 and capacitor C_2 suppress possible radio-frequency interference and provide safe di/dt and dv/dt triac operation when driving inductive loads. \square



Logic-driven ac load switch. Ac loads as large as 2 amperes can be safely switched by logic signals because of optical coupler, which provides up to 2,500 volts of isolation. A low logic input turns off the coupler's LED and phototransistor, causing transistor Q_1 to saturate. This triggers the triac's gate terminal, firing this device and energizing the load. The R_2C_2 network suppresses transients and rfi.

Gate bias circuit for n-MOS runs from 5-V TTL supply

by Bud Broeker
Motorola Semiconductor Products, Phoenix, Ariz.

Complete compatibility with both transistor-transistor-logic circuits and diode-transistor-logic circuits is one of the major advantages that n-channel metal-oxide semiconductors have over p-channel MOS devices. For some n-MOS devices, however, another power supply, in addition to the 5-volt supply used by bipolar logic, is needed to bias the n-MOS gate. Because the current required for this n-MOS gate bias supply is very small—on the order of a leakage current—the higher-voltage n-MOS supply can be made to operate directly from the 5-v bipolar supply.

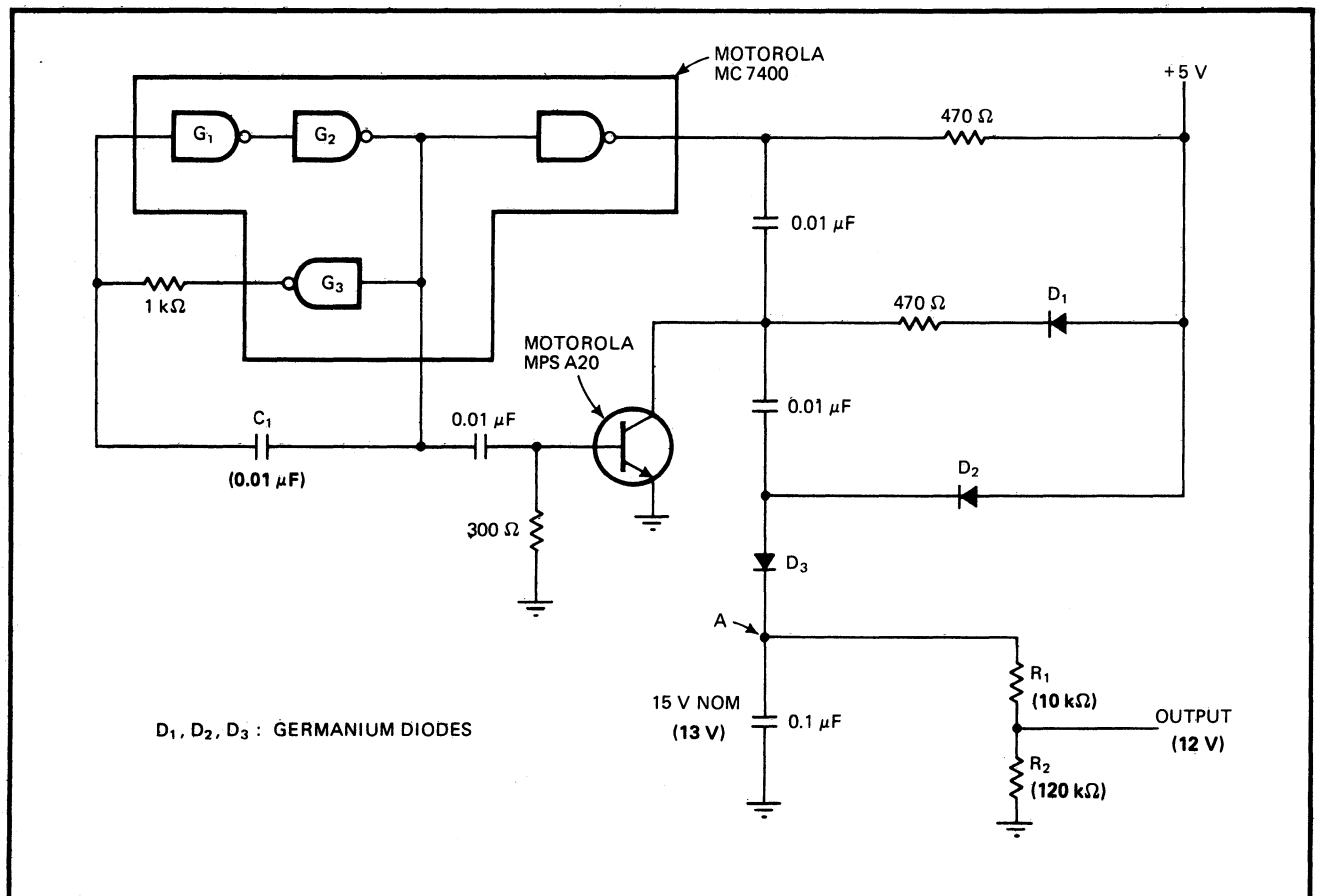
The circuit shown provides a typical bias voltage of 12 V while operating from the bipolar supply. It is pri-

marily intended for a CRT display system that contains mostly TTL circuits, except for a $128 \times 9 \times 7$ n-MOS character generator.

The bias supply consists of a pulse generator formed by gates G_1 , G_2 , and G_3 , and a voltage tripler, which develops a nominal 15-v output (minus three diode drops) at point A. Germanium diodes are used here for D_1 , D_2 , and D_3 to minimize the size of the diode drop, but Schottky diodes can be substituted. A voltage divider network, composed of resistors R_1 and R_2 , is used to reduce the voltage produced by the tripler (at point A) to the desired n-MOS bias voltage.

For the CRT display system, a bias current of not more than 10 microamperes at a bias voltage of 12 V is needed. But if capacitor C_1 is 0.01 microfarad, the voltage at point A is equal to 13 v. To reduce the effect of variations in the n-MOS bias current on the tripler, the divider network, with $R_1 = 10$ kilohms and $R_2 = 120$ kilohms, causes the tripler's load current to be $100 \mu\text{A}$. And the output voltage of the over-all circuit is now at the desired 12-v level and remains within an acceptable tolerance of less than 10% variation. □

An n-MOS voltage booster. Bias supply for n-channel MOS devices operates directly from 5-volt supply used to power TTL devices. The higher potential sometimes required for n-MOS can be derived this way because n-MOS requires only leakage-level bias current. Circuit employs pulse generator (G_1 , G_2 , and G_3), voltage tripler, and voltage divider (R_1 and R_2) to develop 12-V output. Nominal output is 15 V.



Controlling duty cycle and rep rate independently

by W.D. Harrington
University of Florida, Communication Sciences Laboratory, Gainesville, Fla.

A pulse generator with a frequency range of 10 hertz to 10 kilohertz can provide a voltage-controllable output duty cycle that does not change with variations in operating frequency. This constant-duty-cycle generator can be used as a constant-phase triggering source. The falling edges of its output pulse train can trigger another pulse train, producing phase-shifted pulses, with the phase shift being controlled by a voltage.

The duty cycle, D , is adjusted (from 5% to 95%) with voltage V_D , and is a ratio of V_D to supply voltage V_P :

$$D = V_D/V_P = \tau/T$$

where τ is output pulse width, and T is output pulse period. Pulse width τ is determined by the time required for the reference ramp voltage, V_R , to rise from zero to V_1 volts. Voltage V_1 is the feedback voltage that is applied to the inverting input of the comparator.

The ramp, which is formed by charging and discharging capacitor C with a constant current, has a rise time of I_{CC}/C amperes per second. Transistor Q_1 acts as the constant-current source, while transistor Q_2 acts as the shorting switch for discharging capacitor C . The drive

pulses for Q_2 must be significantly narrower than period T , but wide enough to discharge capacitor C .

Feedback voltage V_1 is the amplified difference voltage between the duty-cycle adjustment voltage, V_D , and the dc value of the output pulse train, V_2 . Voltage V_2 is determined by the low-pass filter formed by resistor R_F and capacitor C_F . Since ramp voltage V_R rises at a constant rate, a decrease in voltage V_2 reduces output pulse width τ , while a rise in V_2 increases τ by action of the comparator.

As the circuit's input frequency, f , is made higher (output pulse period T is made smaller), dc filter voltage V_2 tends to rise since:

$$V_2 = V_P \tau f$$

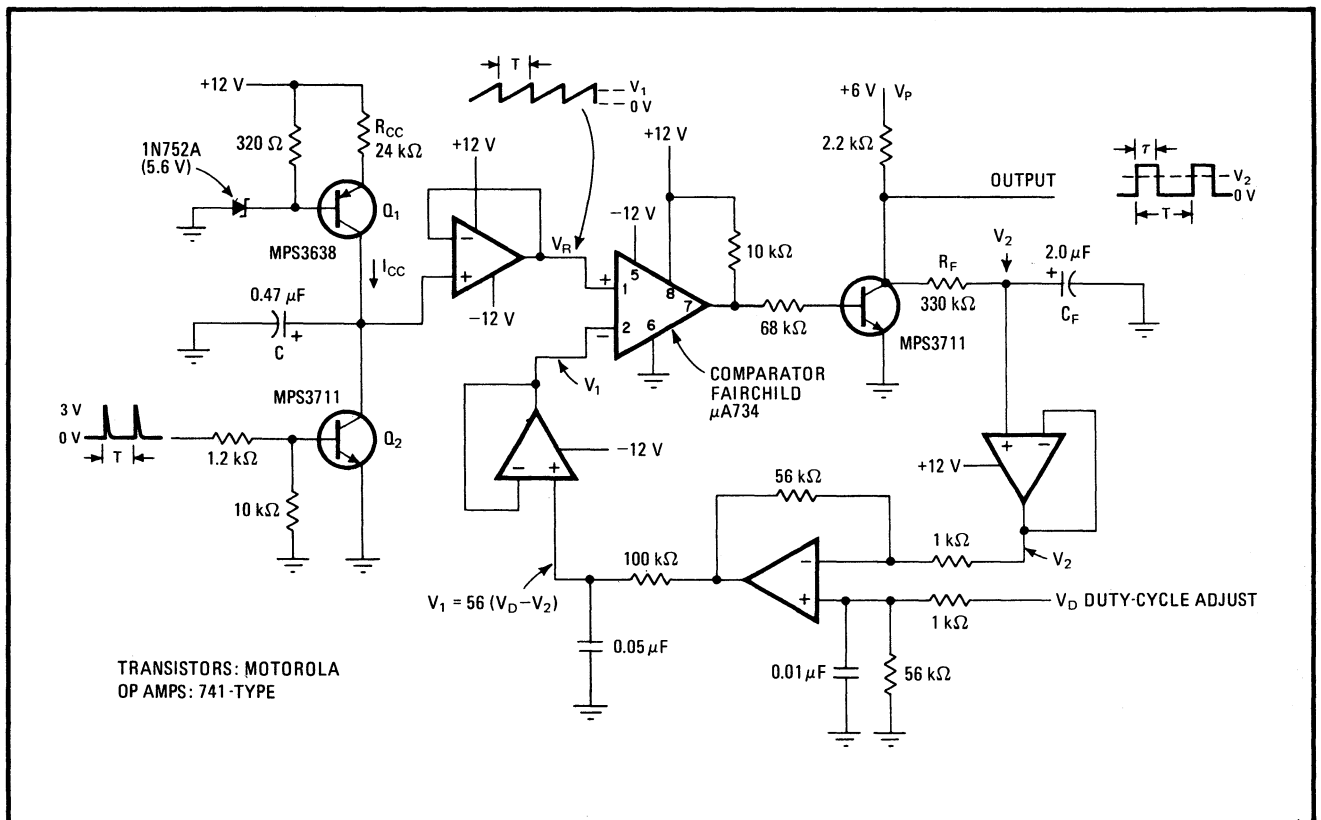
A rise in voltage V_2 causes voltage V_1 to drop, reducing output pulse width τ so that voltage V_2 remains constant. This feedback action, therefore, prevents the duty cycle (τ/T) from changing when the input frequency is varied. The variation of feedback voltage V_1 is:

$$V_1 = I_{CC} V_D / C V_P f$$

which shows that feedback voltage V_1 is inversely proportional to driving frequency f and directly proportional to duty-cycle adjustment voltage V_D .

The circuit can be used as a phase modulator by modulating control voltage V_D , but the modulating frequency is limited by the rolloff of low-pass filter $R_F C_F$. The operating frequency range of the generator may be broadened by changing the value of resistor R_{CC} and using wideband operational amplifiers instead of the general-purpose 741-type units shown. □

Voltage-controlled duty cycle. Pulse generator has separate controls for output pulse period (T), output pulse width (τ), and output duty cycle (τ/T). Duty cycle is varied by changing voltage V_D , the period is controlled by input frequency, and pulse width depends on the ramp input to the comparator. Feedback action prevents duty cycle from changing when input frequency goes from 10 hertz to 10 kilohertz.



Adding foldback resistor provides overload safety

by William J. Riley
General Radio Co., Bolton, Mass.

A single resistor can solve the common problem of dissipating power in a voltage regulator. Including this additional resistor in an ordinary current-limiting power-supply regulator provides effective current-foldback overload protection.

Without resistor R_F , the circuit in the diagram is a typical power-supply regulator. The output current is sensed by resistor R_S and limited to:

$$I_{LIMIT} = V_{BE1} / R_S$$

when transistor Q_1 turns on. (V_{BE1} is Q_1 's base-emitter voltage when Q_1 is conducting.) Although this current-limiting prevents instantaneous damage to series-pass transistor Q_2 , it may not protect Q_2 from overheating under a sustained short-circuit condition.

Current foldback, achieved by simply adding resistor R_F , can overcome the problem. During normal oper-

ation, resistor R_F has no effect but to reduce the current-limiting threshold to approximately:

$$I_{LIMIT} = V_{BE1} - (E_i - E_o)(R_B / R_F) / R_S$$

In the event of an overload, the output voltage falls, and the increasing current through resistor R_F causes the limit current to also fall, approaching a short-circuit value of:

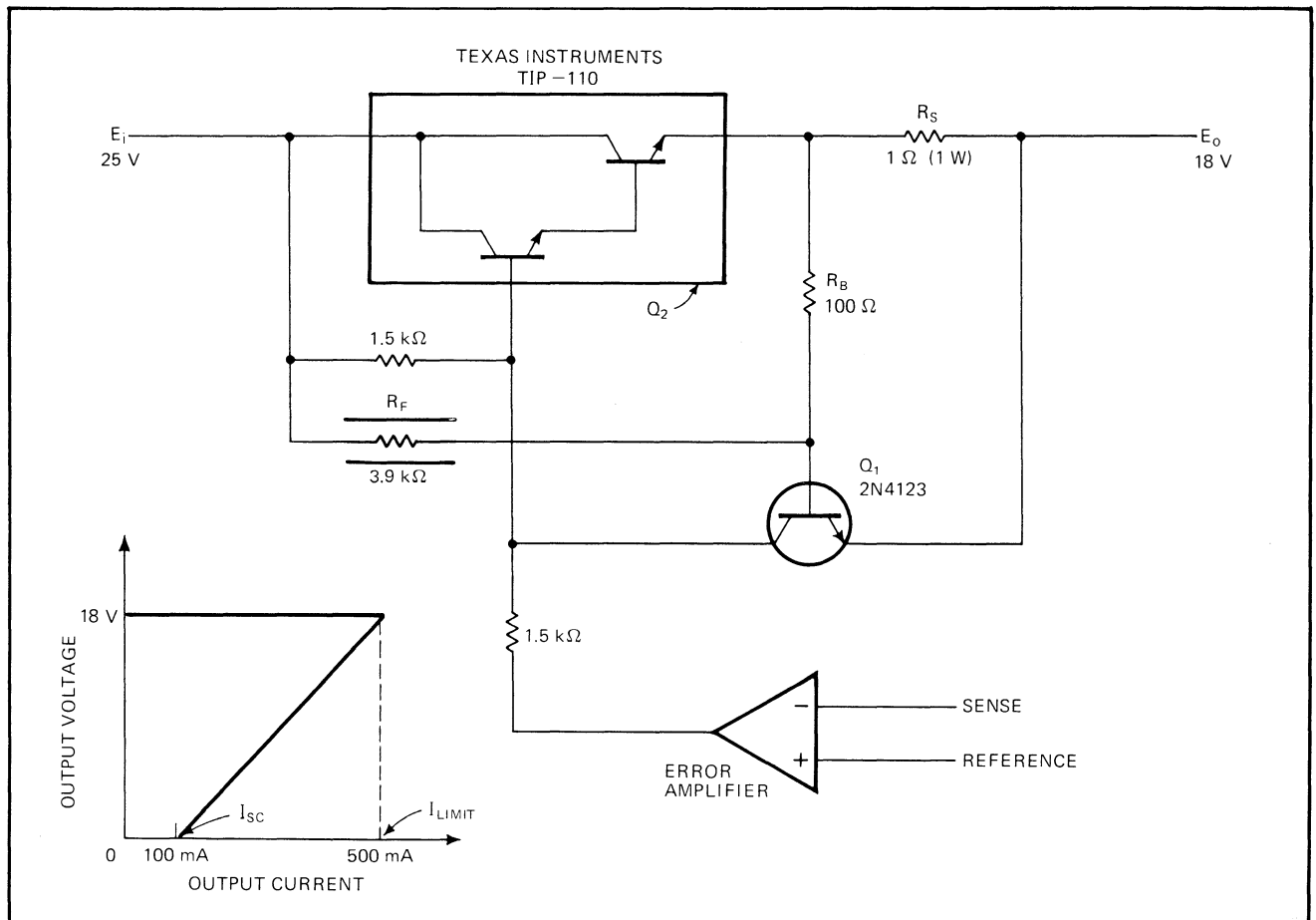
$$I_{SC} = V_{BE1} - E_i(R_B / R_F) / R_S,$$

which is considerably smaller than I_{LIMIT} . Therefore, this current foldback action, illustrated in the volt-ampere characteristic, greatly eases the heat-sinking requirements for series-pass transistor Q_2 .

The output voltage will return to normal after the short is removed, as long as the foldback is not so great that the output current is reduced to zero. The current-limit threshold is sufficiently stable for most applications. It becomes smaller for increasing unregulated input voltage, as well as for increasing ambient temperature. This keeps the dissipation of transistor Q_2 within its rated limit.

Typical nominal component and parameter values are shown in the figure. □

Resistor folds back current. Amount of power dissipated, during overload, in conventional current-limiting voltage regulator can be decreased by adding a foldback resistor between transistor Q_1 and the unregulated input voltage. Resistor R_F eases heat-sinking requirements of transistor Q_2 by folding back current when there is an overload. Output voltage can be returned to normal after overload is removed.



Extending time delay with an emitter-follower

by Victor Hatch
Peripheral Power Systems, San Jose, Calif.

When a long delay is needed between pulses, two unijunction transistors are frequently tied together so that one of them periodically changes the triggering point of the other. A better approach—one that permits very large time constants to be realized—is to use a programmable unijunction transistor (PUT) and an emitter-follower. In this way, the peak point current needed to fire the PUT can be obtained when a high value of resistance is used in the timing network.

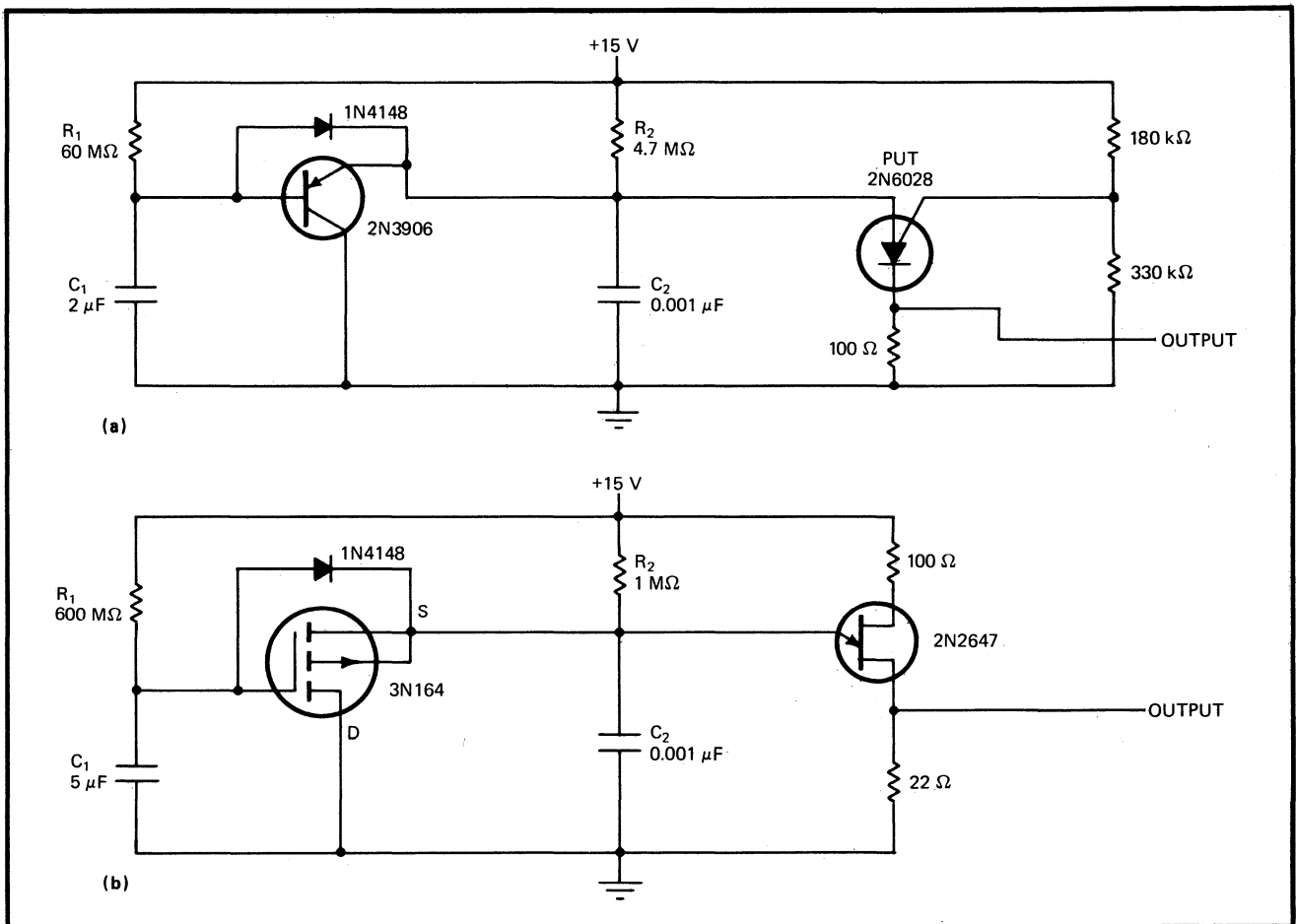
The circuit shown in (a) produces an output pulse every 2½ minutes. Resistor R₁ and capacitor C₁ are the timing components that set the circuit's operating fre-

quency. Resistor R₂ assures that circuit oscillation will be sustained by providing a bias current that is greater than the PUT's peak point current (0.15 microampere in this case) for turning the PUT on and less than the PUT's valley current (25 µA in this case) for turning the PUT off. Capacitor C₂ biases the PUT until the diode conducts and capacitor C₁ begins to discharge.

Even longer time delays can be realized by using the circuit shown in (b)—a unijunction transistor (UJT) and a p-channel enhancement-mode MOSFET that is connected as a source-follower. This particular configuration produces one pulse an hour. Timing resistor R₁ can have a higher value here because the gate current of the MOSFET source-follower is lower than the base current of the transistor emitter-follower.

Again, the value of resistor R₂ determines the proper bias currents. It must supply the UJT with a turn-on bias current that is larger than the sum of the device's peak point current and emitter leakage current, and a turn-off bias current that is smaller than the device's valley current, which is usually several milliamperes. □

Stretching the off time. Emitter-follower (a) allows high values of resistance to be used in timing circuit of programmable unijunction transistor. The resulting large time constant extends the time between output pulses to 2½ minutes for the components shown. With conventional UJT and a source-follower (b), the delay can be made even longer. Here it's one pulse an hour.



Current-sharing design boosts regulator output

by Marvin Vander Kooi
National Semiconductor Corp., Santa Clara, Calif.

When a higher-than-rated current must be supplied by a monolithic voltage regulator, an external boost transistor is usually employed. Most normal current-boosting schemes, however, require additional active devices to duplicate some of the worthwhile safety features of the integrated regulator—for instance, short-circuit current limiting, safe-operating-area protection, and thermal shutdown.

The regulator circuit in the figure retains these safety features by extending them to the external pass transistor through a current-sharing design. This regulator, which is intended for transistor-transistor-logic circuits, has an output voltage of 5 volts at 5 amperes and a typical load regulation of 1.4%.

Resistors R_1 and R_2 provide the necessary current division, assuming that the transistor's base-emitter voltage equals the diode drop. Then the voltage drops across resistors R_1 and R_2 are equal, and the currents through R_1 and R_2 are inversely proportional to their resistances. With the resistance values shown, resistor R_1 has four times the current flow of resistor R_2 .

For reasonable values of transistor beta, the transistor's emitter current (from resistor R_1) will approximately equal its collector current, while the current through resistor R_2 will equal the current flowing through the monolithic regulator. Under overload or short-circuit conditions, therefore, the protection circuitry of the packaged regulator not only limits its output current, but also limits the output current of the

pass transistor to a safe value, thereby preventing device damage.

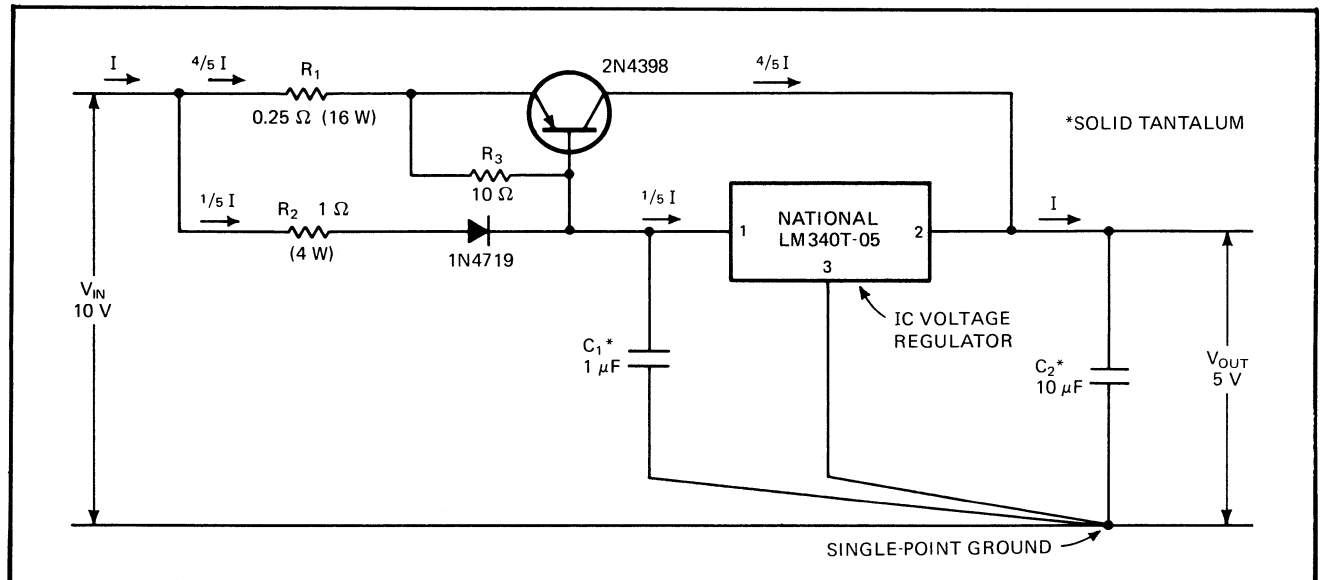
Thermal-overload protection is also extended to the external pass transistor when its heat sink is designed to have at least four times the capacity of the regulator's heat sink. This is because both devices have almost the same input and output voltages and share load current in a 4:1 ratio. During normal operation, up to 1 A of current flows through the regulator, while up to 4 A flow through the outboarded pass transistor.

Under instantaneous overload conditions, the over-all circuit will supply approximately 9 A of output current (for junction temperatures varying from 0°C to 70°C). This reflects the 1.8-A current limit of National's LM340T regulator, causing the times-four current limit for the pass transistor to be 7.2 A. If the short-circuit condition is continuous, the regulator heats up and limits the total steady-state current to about 7.5 A.

For optimum current-sharing between the regulator and the pass transistor as the temperature changes, the diode should be located physically near the pass transistor. Also, the diode's heat-sinking arrangement should keep it at the same temperature as the pass transistor. If the LM340T is used and mounted on the same heat sink as the pass transistor, the regulator should be electrically isolated from the heat sink, since its case (pin 3) is at ground potential, but the case (collector) of the pass transistor is at the regulator's output potential.

Capacitor C_1 prevents unwanted oscillations, while capacitor C_2 improves the output impedance of the over-all circuit. Resistor R_3 provides a path to unload the excessive charge that develops in the base region of the pass transistor when the regulator suddenly goes from full load to no load. The circuit's single-point ground system allows the regulator's sense terminals (pins 2 and 3) to monitor load voltage directly, rather than at some point along a possibly resistive ground-return line carrying up to 5 A of load current. □

Sharing the load for TTL. Current-boosting scheme for IC regulator divides input current in 4:1 ratio between the regulator and an external pass transistor. This current-sharing preserves the IC's short-circuit, overload, and thermal-shutdown safety features. The circuit provides an output of 5 volts at 5 amperes, regulated to 1.4%. The protection diode and the transistor should be kept at the same temperature.



Up/down synchronous counter takes just four MSI packages

by Richard J. Bouchard
Sanders Associates Inc., Nashua, N.H.

An 8-bit synchronous up/down counter with programmable increment-decrement values and a look-ahead overflow-underflow line can be implemented with only four medium-scale integrated circuits. An up/down control line allows the counter to increment either up or down on each clock input pulse by any number from 1 to 7. This type of counter is used in such applications as differential analyzers and X-Y deflection circuits for random-plot cathode-ray-tube displays.

The counter contains an 8-bit latch that is driven by two 4-bit adders. The output of these adders is the sum of the existing latch (counter) output, plus or minus the existing value of the 3-bit increment-decrement control signal. Therefore, at any given time, the input to the latch represents the next counter state, which is synchronously entered into the latch upon receipt of a clock input pulse.

In the count-up mode, the three-bit increment-decrement value is added directly to the existing counter

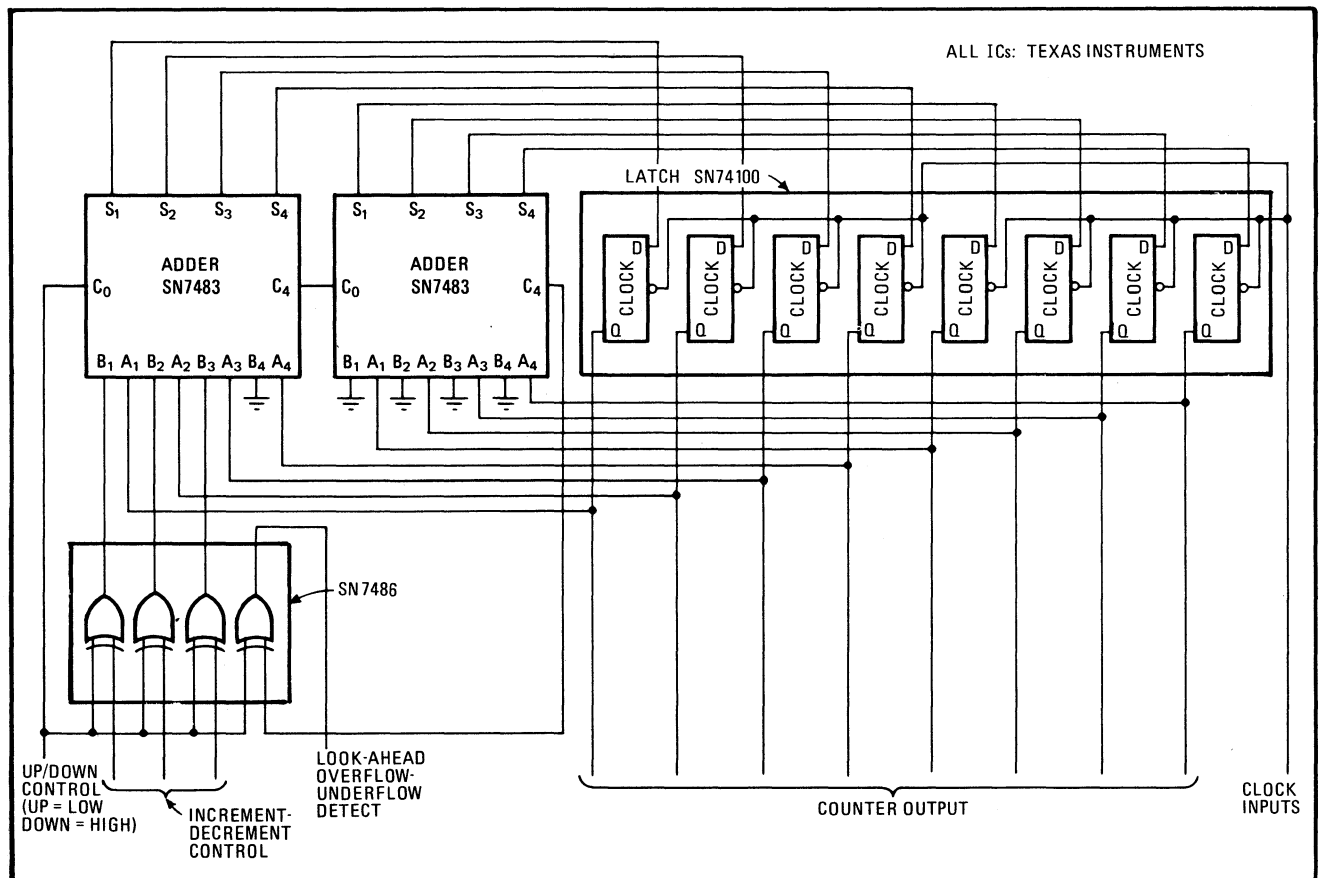
output to provide the next-count input for the latch. In the count-down mode, however, the inputs to the (left) adder from the output lines of the quad exclusive-OR gate represent the 1's complement of the 3-bit increment-decrement value.

The carry input of the least-significant adder stage is activated simultaneously via the count-down control line, and the 2's complement of the existing decrement value is added to the counter output. For the count-down mode, then, the input to the 8-bit latch is less than the existing counter output by the value of the 3-bit increment-decrement control.

One of the stages of the quad exclusive-OR gate is used to generate a positive output signal whenever the next count to be entered into the latch will cause either an overflow or underflow in the counter output. This is accomplished by simply gating the up/down control line with the carry output of the last adder stage. In a vector display, the look-ahead overflow-underflow signal can be used to inhibit the clock input so that vector wrap-around does not occur.

The range of programmable increment-decrement values may be readily extended from the 1-to-7 one shown here to a 1-to-127 one by adding a second quad exclusive-OR element. □

Space-saving counter. Four MSI circuits make up complete 8-bit synchronous up/down counter that includes look-ahead overflow-underflow detection. Output count can be dynamically varied by 3-bit increment-decrement control. For count-up, the value of this signal is added to the existing counter output; for count-down, it is subtracted. The latch input always represents the next counter state.



Using transistor arrays for temperature compensation

by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

Monolithic transistor arrays make handy temperature-compensating devices. For instance, a highly temperature-stable zener reference can be realized by employing one of the transistors as a zener diode, a second transistor as a conventional diode, a third transistor as a chip heater, and a fourth transistor as a chip-temperature sensor.

A typical transistor array is shown in (a), RCA's model CA3046. Only two of the five transistors are needed to implement a temperature-compensated zener diode, which is also shown in (a). It is obtained by reverse-biasing the base-emitter junction of one transistor (Q_3 is used here) and then temperature-compensating this device with the forward-biased base-emitter junction of a second transistor (Q_2 here).

Since all the transistors make good thermal contact with each other, good temperature compensation is provided. For a zener reference current of 200 microamperes, the two-transistor zener develops 7.83 volts and has a temperature coefficient of +196 ppm/°C.

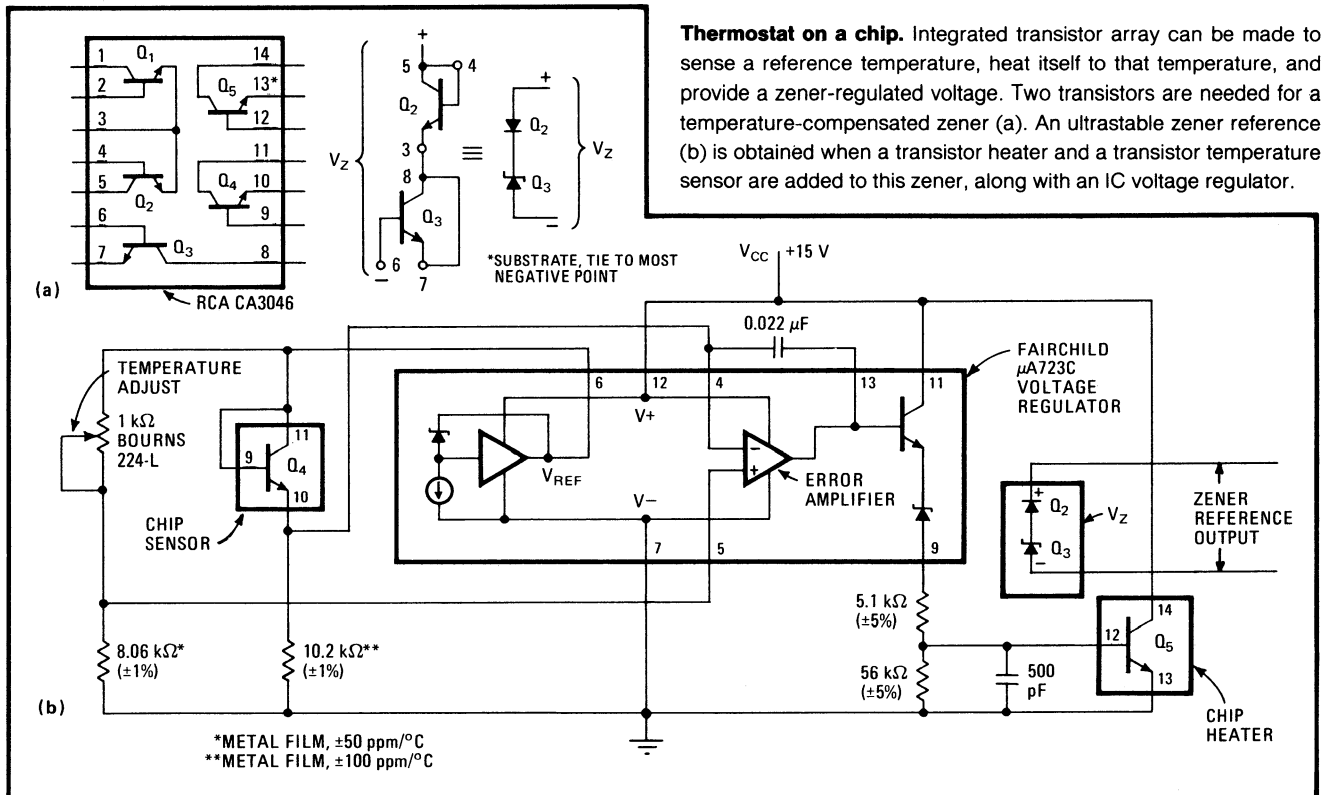
Even better temperature stability can be obtained by

making one of the transistors a chip heater, by connecting its collector to the supply voltage. Whatever heat is dissipated in this transistor heats the entire chip. A fourth transistor, with a forward-biased base-emitter junction, can then act as a chip-temperature sensor. It will have a sensitivity of about -2 millivolts/°C. When the heater/sensor arrangement is used with the temperature-compensated zener of (a), the array exhibits a temperature coefficient of merely -3.1 ppm/°C from 33°C to 50°C.

By adding temperature-reference and temperature-control functions to the array (compensated zener, chip heater, and chip sensor), a highly stable zener reference is formed. In (b), an integrated voltage regulator provides these temperature-reference and temperature-control functions with its internal voltage reference and error amplifier.

The potentiometer sets the circuit's temperature-reference voltage, which is compared with the voltage developed by the chip-temperature sensor (transistor Q_4). Any difference voltage between the two passes through the error amplifier before being applied to the chip heater (transistor Q_5). The heater then brings the chip sensor to the temperature that is set up as the temperature reference, keeping the temperature of the entire transistor array constant.

The zener reference circuit, which uses only one power supply, offers a temperature coefficient of +4.25 ppm/°C from 33°C to 50°C for zener current of 200 μ A. (Transistor Q_1 of the array is not used.)



Thermostat on a chip. Integrated transistor array can be made to sense a reference temperature, heat itself to that temperature, and provide a zener-regulated voltage. Two transistors are needed for a temperature-compensated zener (a). An ultrastable zener reference (b) is obtained when a transistor heater and a transistor temperature sensor are added to this zener, along with an IC voltage regulator.

Dc motor control circuit cancels armature resistance

by Leland N. Van Allen
Ideas Inc., Beltsville, Md.

An ideal permanent-magnet dc motor (or one with a separately excited field) rotates at a speed that is determined solely by applied voltage and is independent of motor load. This is the speed at which the back-emf generated in the rotating armature just equals the applied voltage. Since an ideal motor has no armature resistance, the current drawn can rise to any value necessary to support the load.

But practical motors do have an armature resistance, which degrades their speed regulation with increasing load. This problem can be solved by placing a negative resistance that is exactly equal to the armature resistance in series with the armature.

With the motor-control circuit in the diagram, motor rpm is linearly related to input control voltage, no matter the size of motor load. A high-power operational amplifier is used to drive the motor, and positive current feedback is used to create the necessary negative resistance.

A current-proportional signal is obtained by inserting a small sampling resistor, R_S , at the return side of the motor. This signal, which is applied to the noninverting

input of the op amp, causes the voltage that drives the motor to be just enough higher than what should be needed by an ideal motor to satisfy the armature and sampling resistances. The over-all effect is the same as driving an equivalent ideal direct-current motor from a firm voltage source.

The circuit's supply voltages should be about 3 volts higher than the maximum voltage to be applied to the motor, but less than ± 22 v, unless a different op amp is used. After a reasonable value is chosen for input resistor R_{IN} , say 10 kilohms, feedback resistor R_F can be determined from:

$$R_F = R_{IN}(\text{rpm})/kE_{IN}$$

where k is the motor "tachometer" constant, expressed in units of rpm per volt. The value of this constant can be found experimentally by driving the motor at a known speed and measuring its open-circuit voltage.

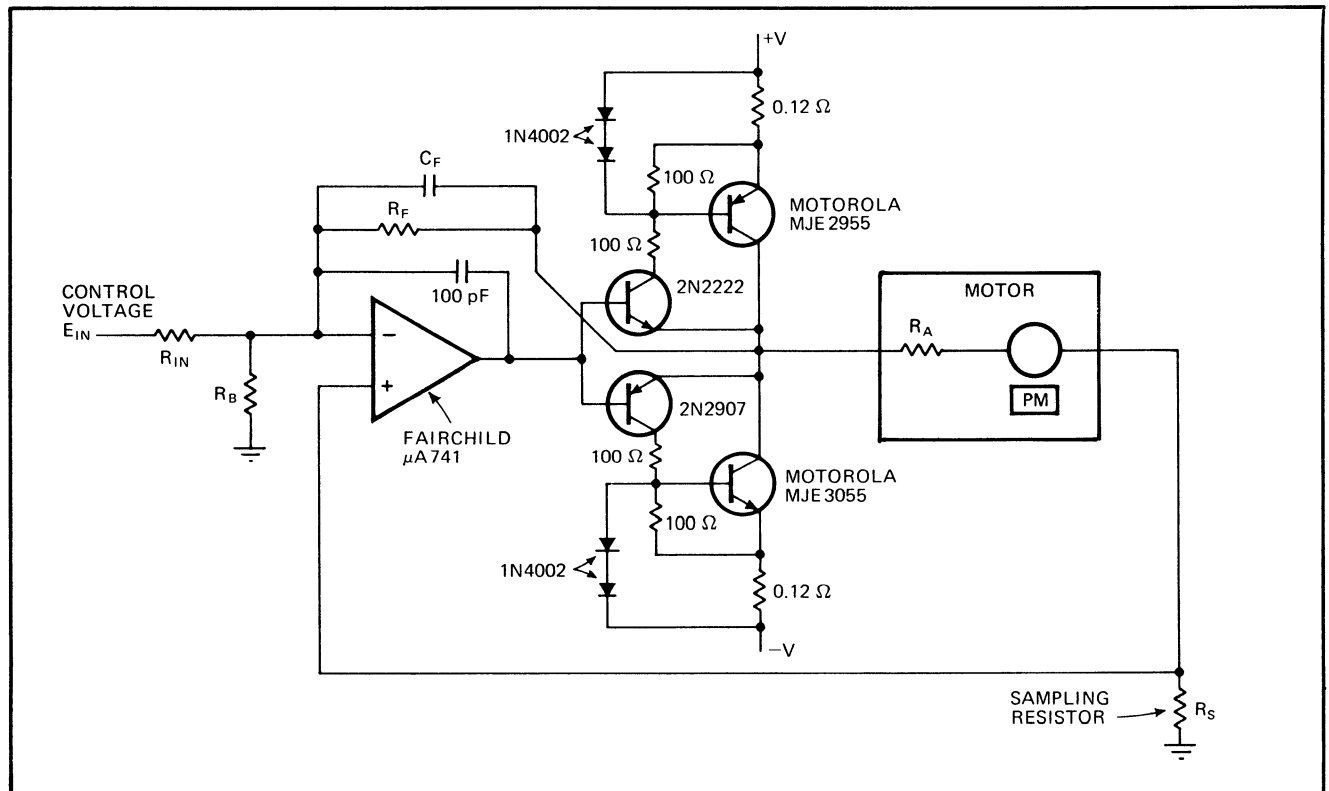
Next, a reasonable value must be selected for the current-sampling resistor, R_S . To minimize power waste, resistor R_S should be considerably smaller than the armature resistance, R_A —for example, $R_A/10$ is a good choice. The value of resistor R_B can then be computed:

$$R_B = R_{IN}R_FR_S/(R_AR_{IN} - R_SR_F)$$

Resistor R_B determines the size of the negative resistance that appears at the output of the op amp. Its value does not affect the motor's rpm-per-volt response.

Capacitor C_F , which is determined experimentally to find the best choice of values, should be as large as possible, but not so large that the motor responds sluggishly. An R_FC_F time constant of 50 milliseconds should serve for most applications. □

Making motor response linear. Permanent-magnet dc motor rotates at rate that is linearly proportional to input control voltage, no matter what the load is. This positive-feedback circuit generates a negative resistance that is equal to the motor's armature resistance, allowing the motor's rpm-per-volt response to be independent of the load. A sampling resistor is used to get current feedback.



Three-mode network is filter or oscillator

by Michel Baril
University of Quebec, Montreal, Quebec, Canada

A triple-function circuit can be built with standard inexpensive components to operate as a bandpass filter, a notch filter, or a sine-wave oscillator. The operating mode is switch-selectable; the operating frequency range is 1 hertz to 20 kilohertz. Both of the filters can be separately adjusted for Q and center frequency.

The circuit (a) functions as a bandpass filter when switch S_1 is in the FLTR position, switch S_2 is open, and switch S_3 is closed. A notch filter is obtained by keeping S_1 in the FLTR position, closing S_2 , and opening S_3 . There are three possible oscillator outputs, one at each amplifier output; they are 180° out of phase with each other. For the oscillator mode, switch S_1 is in the OSC position, switch S_2 is open, and switch S_3 is closed.

The basic functional block of circuit (a) is the phase shifter shown in (b). The transfer function for this network is:

$$e_o/e_i = (1 - RCs)/(1 + RCs)$$

where s is the Laplace transform variable. Although there is no attenuation, the output lags the input by an angle that varies from 0 to π as frequency increases from zero to infinity. Cascading two of these blocks

yields a phase-shifter whose angle is adjustable from 0 to 2π . Its transfer function is:

$$e_o/e_i = [(1 - RCs)/(1 + RCs)]^2$$

When a voltage divider made up of resistors R_1 and R_2 is placed across the two blocks, as shown in (c), the transfer function is modified to:

$$e_o/e_i = R_1/(R_1 + R_2) + [R_2/(R_1 + R_2)] [(1 - RCs)/(1 + RCs)]^2$$

If $R_1 = R_2$, output voltage e_o is a minimum (or equal to zero) when the phase lag is π .

When circuit (c) is used as the feedback element of an operational amplifier, the transfer function becomes that of a bandpass filter:

$$e_o/e_i = (R_1 + R_2)/[R_1 + R_2(1 - RCs)/(1 + RCs)]^2$$

The resulting circuit is the one shown in (a). Amplifiers A_2 and A_3 are the basic phase-shifters in the feedback loop of amplifier A_1 . If amplifier A_3 is used as a buffer, the circuit becomes a notch filter.

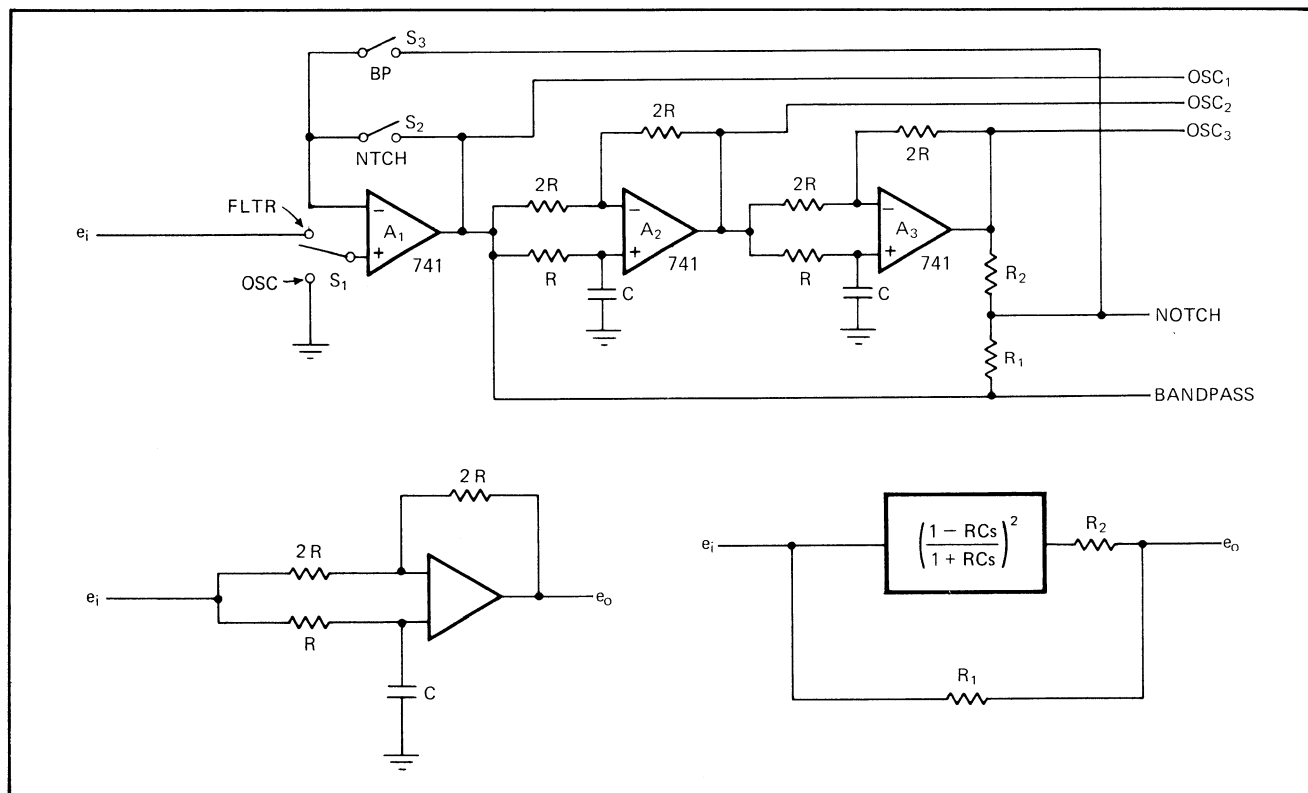
The Q factor of either the bandpass or the notch filter can be adjusted by changing the ratio of $R_1:R_2$ (theoretically, $Q = \infty$ when $R_1 = R_2$). Filter center frequency (f_o) can be varied by changing the values of resistor R and capacitor C:

$$f_o = 1/(2\pi RC)$$

For the circuit to work as an oscillator, the non-inverting input of amplifier A_1 must be grounded and resistor R_1 set equal to resistor R_2 . Again, the operating frequency is set by varying the values of resistor R and capacitor C.

Circuit performance depends principally on the amplifiers, rather than the passive components. It is not

Choice of functions. Circuit (a) has three switch-selectable operating modes—it can be a bandpass filter, a notch filter, or a sine-wave oscillator. The three oscillator outputs differ in phase by 180° . Two of the phase shifters shown in (b) are cascaded and, along with the voltage divider formed by resistors R_1 and R_2 , placed in the feedback loop (c) of a third operational amplifier.



necessary for resistor R or capacitor C to be precision components; resistors having tolerances of $\pm 5\%$ will do. And the resistor labeled 2R in the diagram can actually be much larger than $2 \times R$ without impairing the per-

formance of the circuit. However, to get very high filter Q or to use the circuit as an oscillator, voltage-divider resistors R_1 and R_2 must be precision parts, with tolerances as tight as $\pm 1\%$ or $\pm 0.1\%$. □

One lamp can monitor battery voltage

by N.D. Thai
Huntec Ltd., Toronto, Ont., Canada

A single lamp can monitor an unregulated voltage, for instance from a battery, indicating whether that voltage is high, low, or normal. For a normal voltage, the lamp stays off; for a high voltage, the lamp stays on; and for a low voltage, the lamp flashes on and off. The low and high voltage limits are independently settable, and the flashing frequency is also adjustable.

Two complementary-MOS NOR gates perform the logic for the circuit. The voltage applied to the input of gate G_1 is AV, where A is a constant determined by the setting of potentiometer R_1 . Similarly, the voltage applied to the input of gate G_2 is BV, where B is a constant determined by the setting of potentiometer R_2 . Constant B is made larger than constant A.

A logic 1 is applied to both gate inputs when voltage

V goes high. Voltage BV then exceeds the gate threshold voltage (V_T), or:

$$V \text{ is greater than } V_T/B = V_H$$

where V_H represents the high voltage limit. The output of gate G_2 is low, and the lamp stays on. A logic 0 is applied at both gate inputs if voltage V goes low. Voltage AV is now smaller than the gate threshold voltage, or:

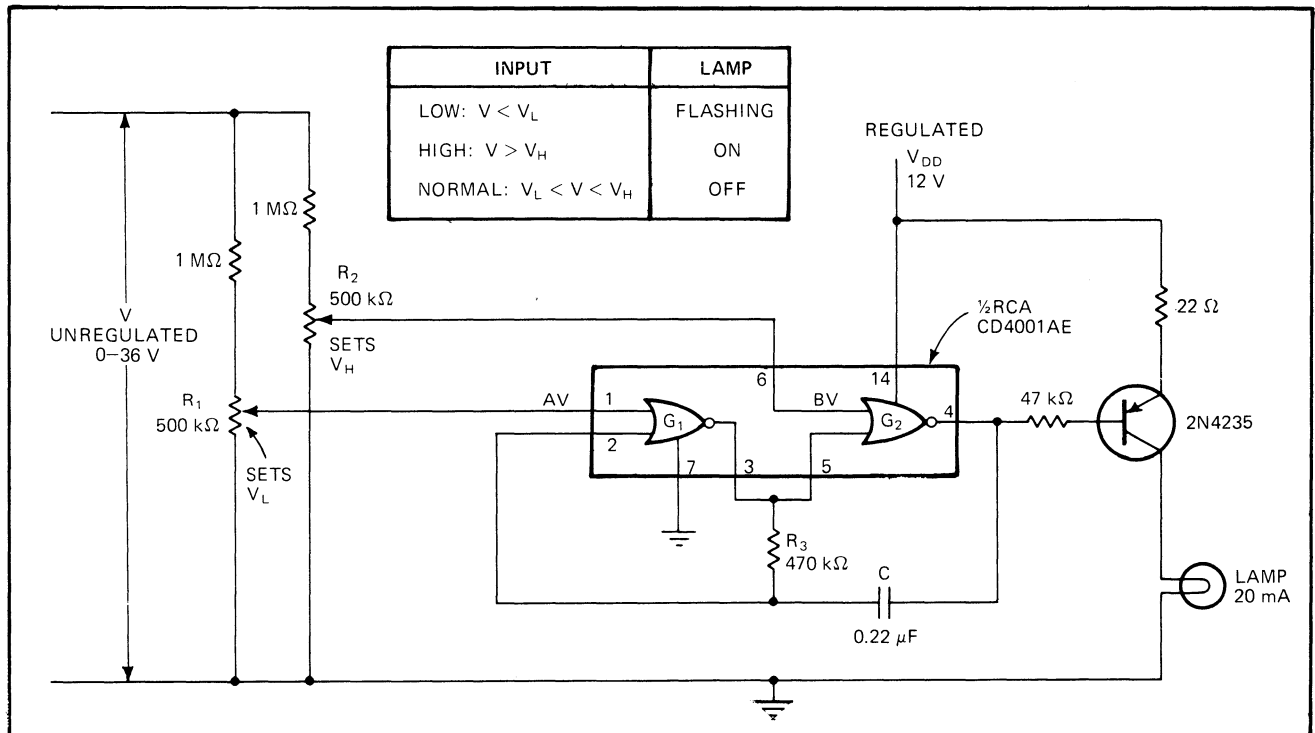
$$V \text{ is less than } V_T/A = V_L$$

where V_L is the low voltage limit. The two NOR gates, resistor R_3 , and capacitor C form a conventional astable multivibrator that drives the lamp with a square wave. The flashing frequency (assuming $V_T = V_{DD}/2$) is approximately equal to:

$$f = 1/(1.4)R_3C$$

When voltage V lies between the low and high limits (that is, if voltage AV is greater than threshold V_T and voltage BV is less than threshold V_T), a logic 1 is applied to the input of gate G_1 , while a logic 0 is applied to the input of gate G_2 . The lamp remains off because the output of gate G_1 is low and the output of gate G_2 is high. □

Lighting the way. Single lamp indicates when unregulated (battery) input voltage is low, high, or normal by flashing, remaining on, or remaining off. The low voltage limit, V_L , is set by potentiometer R_1 , the high voltage limit, V_H , is set by potentiometer R_2 , and the flashing frequency is determined by resistor R_3 and capacitor C. Complementary-MOS NOR gates are used as the logic elements in this voltage monitor.



Voltage-to-current converter for process-control systems

by Harry L. Trietley, Jr.
Taylor Instrument Process Control Div., Sybron Corp., Rochester, N.Y.

To avoid damage to process-control instruments, such as controllers and chart recorders, the maximum value of the signal current that drives these devices must be limited. This signal current, which corresponds to a control signal voltage, can become too large if the control-signal voltage exceeds its normal range or if some other abnormal condition occurs.

Without requiring a series output resistance, the voltage-to-current converter in the diagram limits output current to between 24 and 40 milliamperes, a safe range for much process-control instrumentation. The circuit converts an input signal of 0 to 1 volt to a current of 4 to 20 mA for driving a load of 0 to 1,300 ohms.

Under normal operating conditions, the zener diode does not conduct. The amplifier and transistors Q_1 and

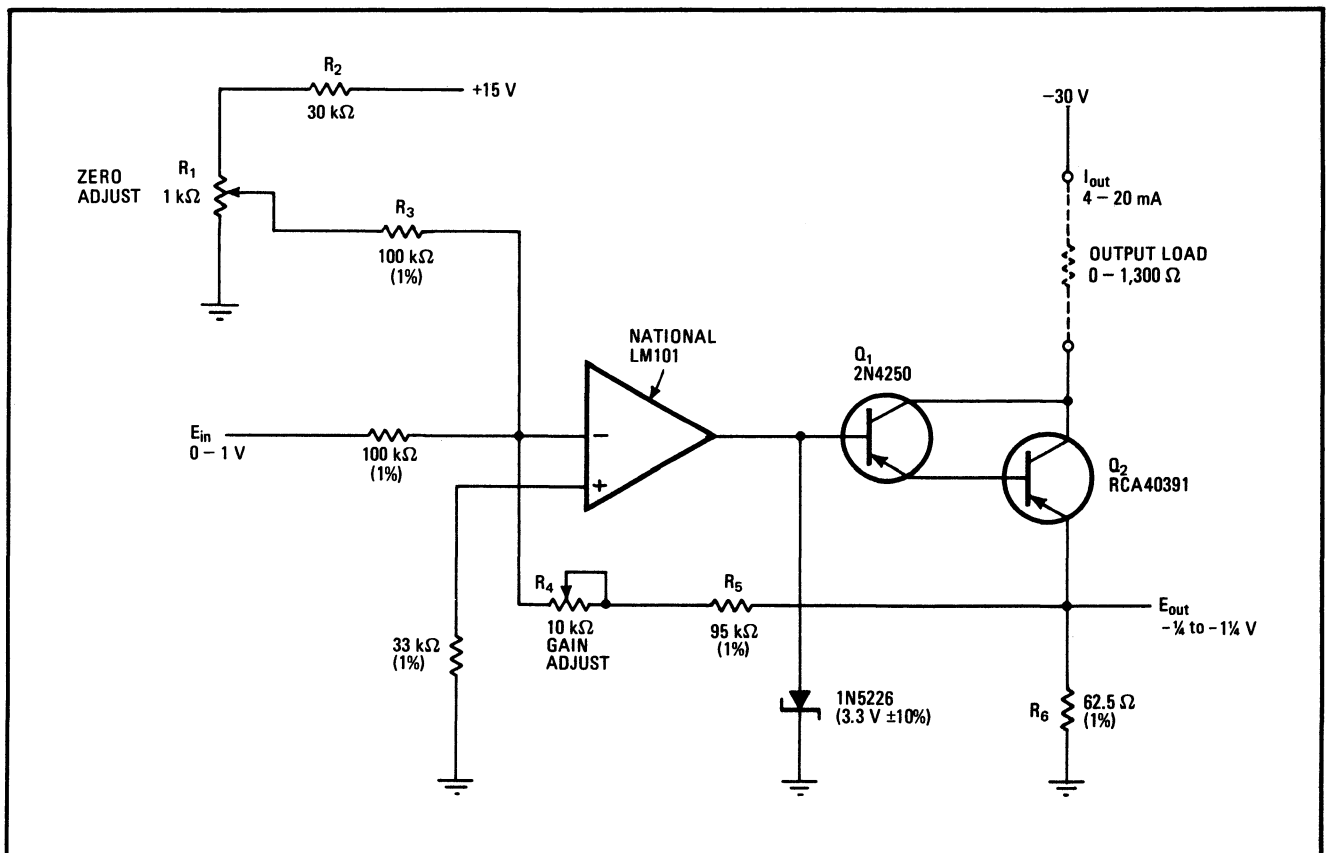
Q_2 perform as an operational amplifier, the output of which is at the emitter of transistor Q_2 . With the resistance values shown, the circuit has a gain of 1. Resistors R_1 , R_2 , and R_3 form an offset zero adjustment, while resistor R_4 provides precision gain adjustment.

The output current, I_{OUT} , equals the sum of the currents in resistors R_5 and R_6 , regardless of the size of the output load. Since resistor R_5 is much larger than resistor R_6 , the output voltage (E_{OUT}), which ranges from $\frac{1}{4}$ to $1\frac{1}{4}$ v, produces a current of 4 to 20 mA.

Integrated op amps, such as the National Semiconductor LM101 used here, are internally limited to output currents of about 25 mA. When the converter's output reaches the zener's voltage, the zener will conduct, grounding the amplifier's output current and clamping the converter's output voltage to a nominal level of 3 v $\pm 10\%$. The output voltage is actually limited to between 1.5 and 2.5 v because of the base-emitter voltage drops of transistors Q_1 and Q_2 . The output current is then limited to a maximum value of between 24 and 40 mA.

If the value of resistor R_6 is lowered to 25 ohms, the output current range becomes 10 to 50 mA, with limiting occurring between 60 and 100 mA. Other outputs, gains, or current limits can also be realized. \square

Instrument interface. Circuit converts control signal voltages to signal currents for driving process-control instruments, such as chart recorders. For the components values shown, this converter limits output current to between 24 and 40 milliamperes to protect the instruments from excessive driving currents due to out-of-range control voltages. The zener diode limits output voltage to 1.5–2.5 volts.



Data averager for panel meter operates from meter's clock

by George Mitchell and Richard D. Spencer
University of Illinois, Urbana, Ill.

In many scientific applications, measurements made with a digital voltmeter require time-averaging to reduce the measurement uncertainty of a noisy signal. A simple averaging circuit can be easily added to a digital panel meter for summing independent measurements so that the uncertainty of the data is reduced.

The averaging circuit shown here causes the DPM to sum 10 or 100 measurements (depending on switch position), thereby reducing data uncertainty by a factor of 3.2 or 10, respectively. Although this circuit is intended for an Electro-Numerics' model 305 4½-digit ratio panel meter, it can be readily adapted to any DPM that uses a dual-slope converter.

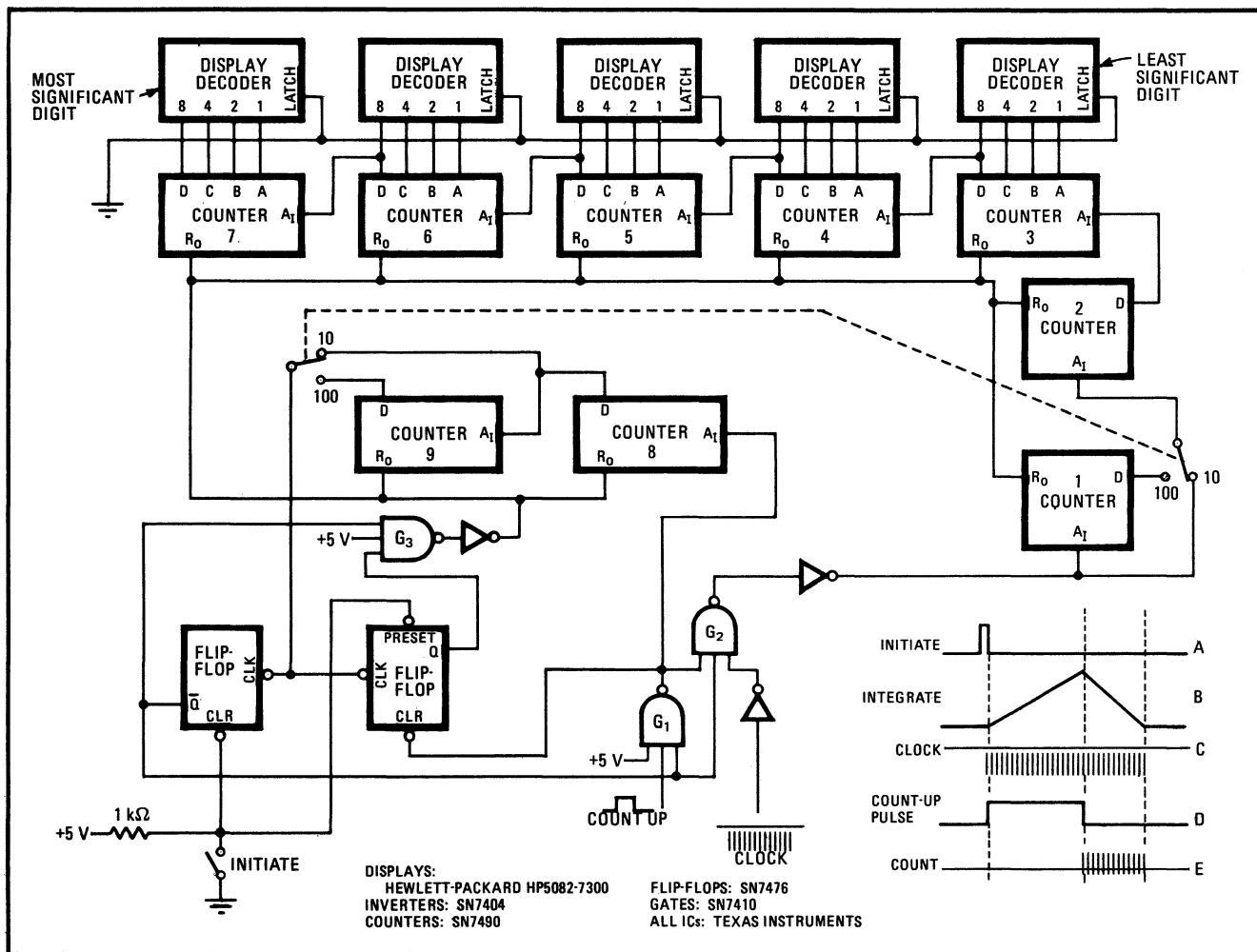
The circuit, which is activated with an initiate pulse (trace A in the figure), takes advantage of the clock

pulse train (trace C) from the DPM's dual-slope converter. The clock train is transmitted during the integration period (trace B) of the analog signal and reference inputs. The count-up pulse (trace D) corresponds to the fixed integration time of the analog signal input.

NAND gates G_1 and G_2 use the count-up pulse to gate the clock output of the DPM's dual-slope converter so that the input to either decade counter 1 or 2 (trace E) is directly proportional to the ratio (in this case) of the analog inputs. As can be seen, counters 1 and 2 are scalars of 10 and 100, respectively, for the gated clock pulse train. Counters 3 through 7 form the decimal accumulator, and counters 8 and 9 are tally registers that inhibit averaging of data past the required number of samples (10 or 100).

The averaging circuitry is synchronized to the DPM's converter cycle by the two flip-flops and three NAND gates. Grounding the initiate line clears the tally registers and scalars, as well as the accumulator, and initiates the accumulation of a new average. The average, or scaled, output is displayed by light-emitting-diode readouts that have their own decoder/drivers. The binary-coded decimal output of the accumulator may also be used to transfer data directly to a printer or computer. □

Averaging out noise. Measurement uncertainty of noisy signals is reduced by time-averaging circuit for digital panel meter. The circuit, which runs from clock of DPM's dual-slope converter, sums 10 to 100 measurements, reducing data uncertainty by 3.2 or 10. Counters 1 and 2 are the scalars, counters 3 through 7 make up the accumulator, and counters 8 and 9 are the tally registers.



Binary rf phase modulator switches in 3 nanoseconds

by Roland J. Turner
AEL Communications Corp., Lansdale, Pa.

By employing a diode-steered current source, binary rf phase modulation is accomplished by translating transistor-transistor-logic levels to a bidirectional current drive in less than 3 nanoseconds. The rf modulator is intended to provide phase coding and correlation in jamming-resistant radar and secure communication links, where transmission and reception are essential in a hostile environment.

The binary (0° and 180°) phase modulation is effected by switching Schottky diodes in a ring modulator at high video/i-f rates. These high data rates require TTL signal levels to be translated to a ± 15 -milliampere current drive for the ring modulator in extremely short time intervals. The complete binary rf phase modulator consists of the video driver (a), which employs stripline techniques, and the ring modulator (b).

When the input logic level to the video driver is at -5 volts, transistor Q_1 is off, diode D_1 is on, and diode D_2 is off. This forces current source Q_2 to deliver 15 mA to the ring modulator. When the input logic level increases positively from -5 v to 0 v, transistor Q_1 turns on, reverse-biasing diode D_1 so that this device turns off.

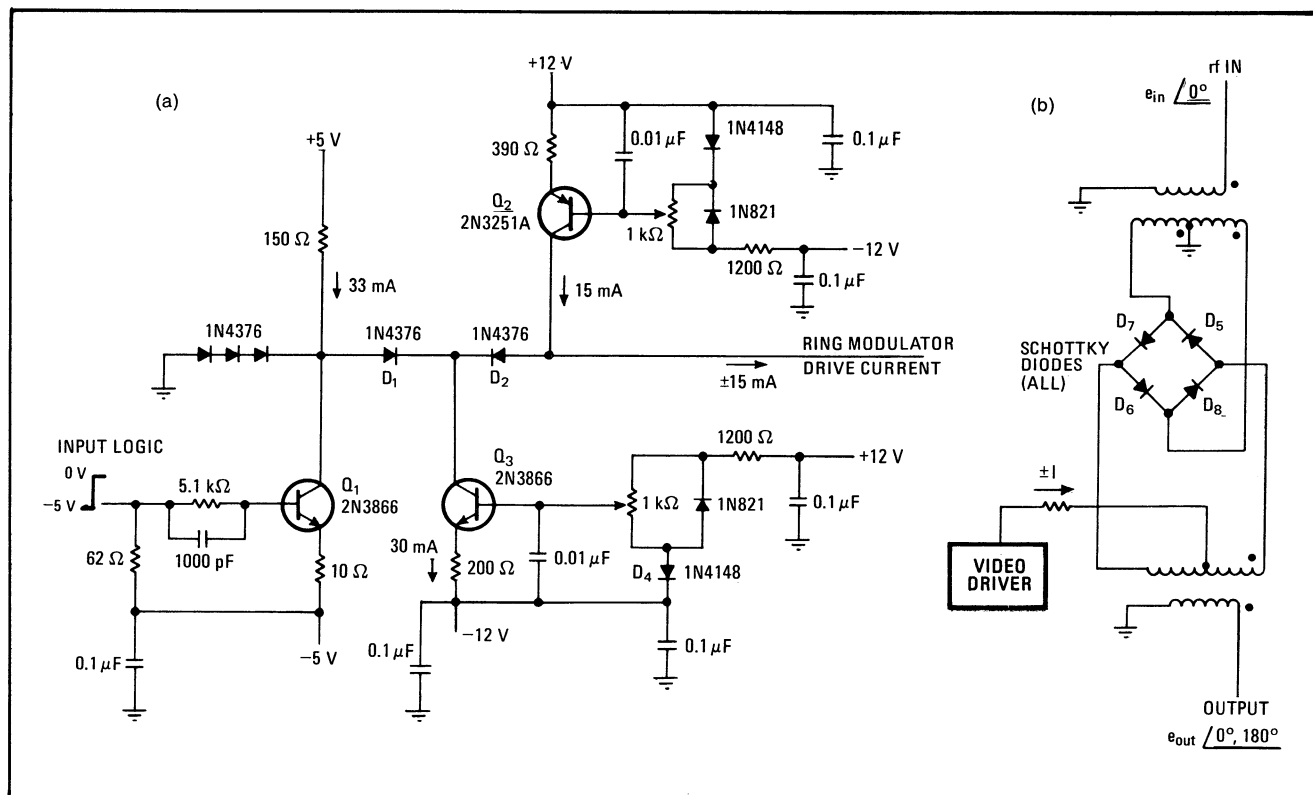
Diode D_2 now turns on, and current source Q_3 forces 15 mA to be drawn from the video port of the ring modulator. The i-f/rf signal phase is then shifted by 180° as it passes through the ring modulator.

This binary phase modulation is accomplished in only 3 ns because the current sources can force rapid charging of any circuit capacitance. Also, load-circuit switching is forced by impressing a large negative or positive voltage on diode D_1 . Since D_1 's switching voltage transition is low relative to the drive voltages, switching can be done in a small time interval. (Current sources Q_2 and Q_3 are temperature-stabilized by diodes D_3 and D_4 .)

The switching current from the video driver is applied to the video port of the ring modulator. When the driver supplies current ($+I$) to the video port, Schottky diodes D_5 and D_6 conduct, and the output phase is 180° . When the driver sinks current ($-I$) from the video port, Schottky diodes D_7 and D_8 are forced to conduct, and the output phase is 0° .

This switching technique is quite useful in applying coded rf phase modulation to an interrogating radar or in applying secure modulation to a secure communication link. The system then becomes very difficult to jam since correlation reception at the receiver enhances detection and suppresses the effects of noise, whether the noise source is Johnson noise or intentional noise jamming. \square

Reversing phase at radio frequencies. Phase modulator switches phase of rf signals between 0° and 180° . Video driver (a) translates TTL inputs to bidirectional switching current for Schottky-diode ring modulator (b) in under 3 nanoseconds. The driver employs diode-steered current sources (transistors Q_2 and Q_3) to supply or sink 15 milliamperes for the video port of the ring modulator.



Varying comparator hysteresis without shifting initial trip point

by Jerald Graeme
Burr-Brown Research Corp., Tucson, Ariz.

An operational amplifier is a convenient device for analog comparator applications that require two different trip points. The addition of a positive-feed-back network will introduce a precise variable hysteresis into the usual comparator switching action.¹ Such feedback develops two comparator trip points centered about the initial trip point or reference point.

In some control applications, one trip point must be maintained at the reference level, while the other trip point is adjusted to develop the hysteresis. This type of comparator action is achieved with the modified feedback circuit shown in the figure.

Signal diode D_1 interrupts only one polarity of the positive feedback supplied through resistor R_2 . Hysteresis, then, is developed for only one comparator state, and one trip point remains at the original level set by the reference voltage, E_R . The second trip point, the one added by hysteresis, is removed from the original trip point by:

$$\Delta V = R_1(V_Z - E_R)/(R_1 + R_2)$$

where V_Z , the zener voltage, is greater than reference voltage E_R . Varying resistor R_2 will adjust the hysteresis without disturbing the trip point at E_R .

The circuit's other performance characteristics are similar to the common op-amp comparator circuit. The accuracy of both trip points is determined by the op amp's input offset voltage, input bias current, and finite gain. Resistor R_3 limits the current drain through the zener diode, and resistor R_4 provides a discharge path for the capacitance of diode D_2 .

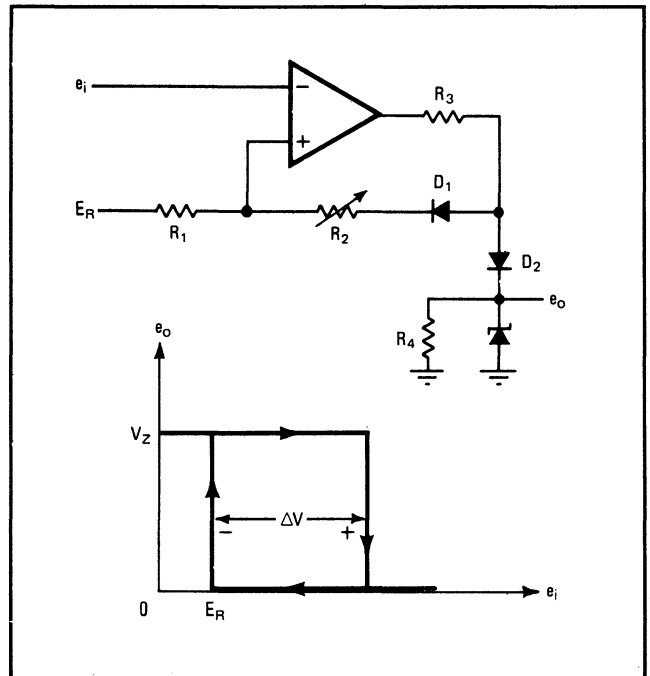
The output signal can be taken either directly from the op-amp output or from the zener diode, as shown. With the latter hookup, the output signal voltage alternates between zero and zener voltage V_Z , which might

be desirable for interfacing with digital logic circuits. It should be noted, however, this output cannot sink current in the 0-volt state.

Switching speed is determined by the op amp's slewing-rate limit for high-level input-drive signals. When the input drive is a low-level signal, the output rate of change is limited by the gain available to multiply the input signal's rate of change. Both the slew-rate limiting and the gain limiting of switching time are eased if phase compensation is removed from the op amp. □

REFERENCE:

1. G. Tobey, J. Graeme, and L. Huelisman, "Operational Amplifiers: Design and Applications," McGraw-Hill, 1971.



Controllable hysteresis. Positive feedback circuit for analog op-amp comparator does not shift the initial reference trip point while introducing hysteresis in the second trip point. The voltage difference, ΔV , between the trip points can be adjusted by varying resistor R_2 . When the output voltage is taken from the zener diode, as shown, it switches between zero and V_Z ; the zener voltage.

Circular voltage divider needs fewer resistors

by Dale Hileman
Physiometrics Inc., Malibu, Calif.

A bridge that provides precision dc voltages from 0 to 10 volts, in steps of 0.01 V, can be easily and economic-

ally realized with a "circular" voltage divider. In this uncomplicated divider arrangement, the point from which the output is taken remains fixed, while the voltage source is moved from one point to another.

In a conventional voltage-divider setup, the fixed voltage is applied across the entire network, and the output voltage is taken from a selectable tap. This approach, however, may involve complex switching and usually requires a large number of resistors, which is undesirable because precision resistors are expensive.

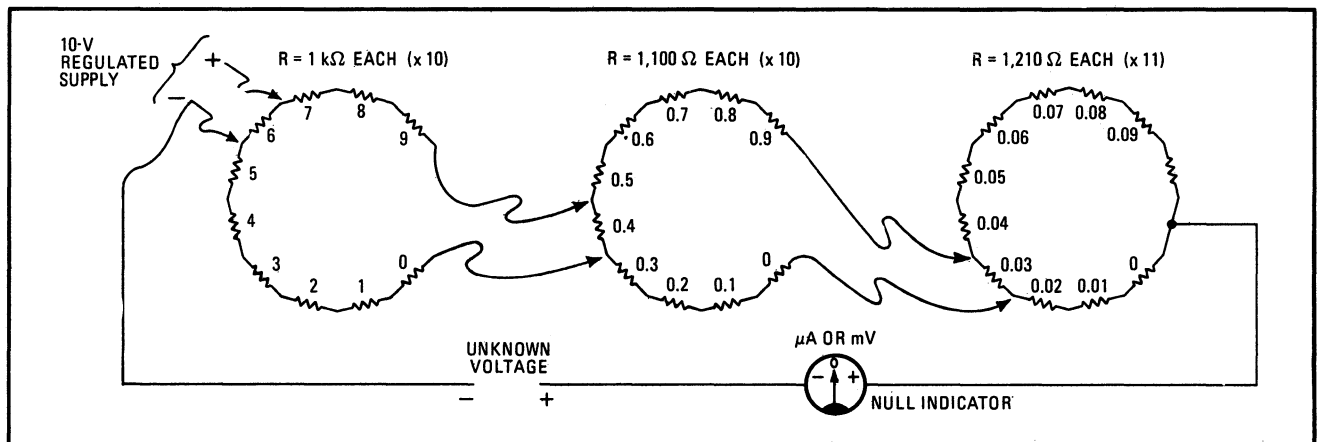
As shown in the diagram, a total of only 31 resistors is

needed to provide a settability to within 0.01 v. Each ring has 10 resistors, except the last, which contains 11. The value of the resistors in a given ring must be 1.1 times the value of the resistors in the preceding ring. The bridge in the illustration is set up to produce an output of 6.43 v.

The tighter the tolerance of the resistors, of course,

the more accurate the output voltage can be. And the more sensitive the null indicator is, the more closely the bridge output can be read. As lower-value resistors are used, the bridge output impedance becomes lower.

The principal limitation of this arrangement is the allowable power dissipation of the resistor in the first ring across which the full supply voltage is applied. □



Dial a voltage. Circular resistor arrangement trims resistor count without sacrificing precision. The output voltage of this bridge can be set from 0 to 10 volts, to within 0.01 V. All resistors in the same ring have the same value, which is 1.1 times larger than the value of the resistors in the preceding ring. Resistors in the first ring must be able to withstand the full supply voltage. Just 31 resistors are used here.

Link-coupled tank circuit steps up C-MOS drive voltage

by R.W. Mouritsen
National Research Council of Canada, Ottawa, Canada

Because of their low power dissipation, low leakage current, and high noise immunity, complementary-MOS devices are a sound design choice for portable or battery-operated equipment—such as counter chains or clocks driven from standard oscillators. However, several volts, typically 5 to 7 volts, are usually required to turn on the C-MOS device, whereas most standard oscillators normally have an output of only about 1 v root-mean-square at 50 ohms.

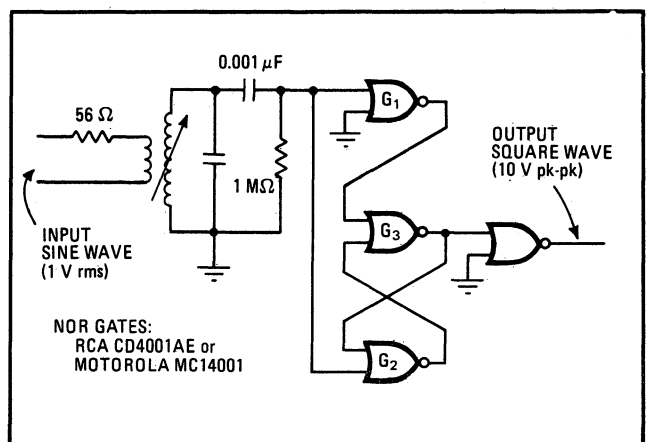
A simple way around this problem is to use a link-coupled tuned circuit as a voltage step-up transformer. Since the input impedance of the C-MOS device is extremely high, the tank circuit is loaded only by the primary source impedance reflected across the secondary winding. This allows the use of a fairly high-Q coil. The link-to-secondary turns ratio is adjusted to produce, across the tuned circuit, a sine wave with a peak-to-peak amplitude of approximately 90% of the supply voltage, when the driving signal is 1 v rms at 50 ohms.

The squaring circuit shown in the figure is an example of this link-coupling technique. It consists of a C-MOS quad two-input NOR gate package, connected as a forced latch.

With the input at 0 v (logic 0), the outputs of gates G_1

and G_2 are logic 1, while the output of gate G_3 is logic 0. As the input rises (towards logic 1), the outputs of gates G_1 and G_2 go to logic 0 when the C-MOS turn-on threshold voltage is reached. This forces the output of gate G_3 to go to logic 1 and remain there until the input falls below the threshold level. At that time, gate G_1 goes to logic 1, allowing gate G_3 to return to logic 0 and causing gate G_2 to go to logic 1.

When the supply voltage is 12 v and the input signal is 1 v rms at 50 ohms and 1 megahertz, the squaring circuit produces an output that approximates a square



Squaring circuit. Link-coupled tuned circuit provides transformer-like action, stepping up the low-level drive signal supplied by most standard oscillators. This permits complementary-MOS gates, the threshold voltages of which are generally 5 to 7 volts, to be used without adding extra active devices. With this squaring circuit, a 1-V sine wave is converted to a 10-V square wave at megahertz rates.

wave with an amplitude of around 10 v pk-pk and with rise and fall times of about 50 nanoseconds. The tuned circuit used here has a narrow operating band. A wider band may be obtained by employing a small toroid

having a bifilar secondary with a link-coupled primary. This will yield about the same output waveform, but operating frequency will range between 500 kilohertz and 3.5 MHz, depending on the ferrite used. □

Square-wave generator stresses frequency stability

by S.F. Aldridge
IBM Corp., General Products Div., San Jose, Calif.

Offering features that are usually found only in more elaborate oscillators, a simplified voltage-controlled square-wave generator produces very symmetrical complementary square-wave outputs that exhibit good frequency stability over a wide operating temperature range. Output frequency repeatability can be held, without adjustment, to within a 5% range, and operating frequencies can exceed 50 megahertz.

The circuit's noise insensitivity is excellent due to its current-source decoupling (provided by capacitors C_1 and C_2). Moreover, noise generation within the generator is held to a minimum because of the constant-current nature of the circuit.

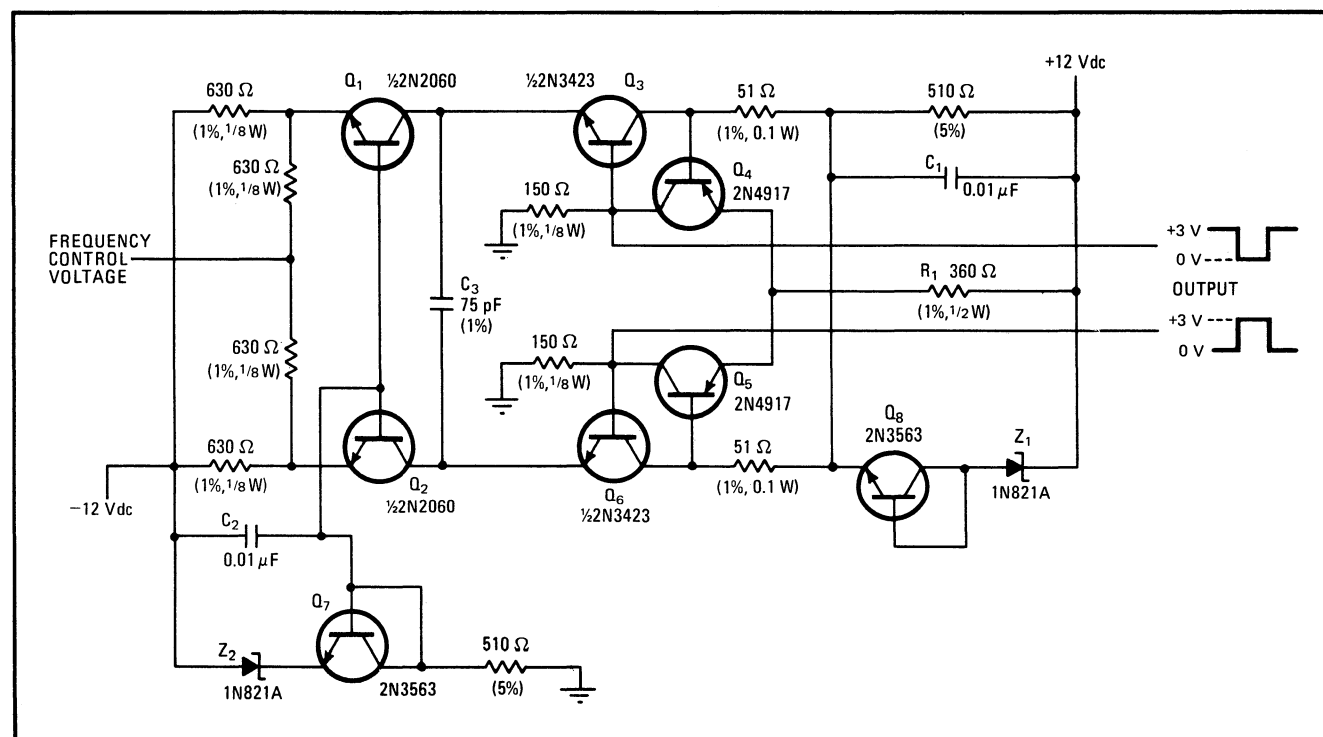
Power-supply variations as large as 15% produce a negligible shift in output frequency because of the action of the circuit's current sources (transistors Q_1 and Q_2) and the configuration of the circuit's oscillator sec-

tion. The generator can be considered to provide linear operation throughout the entire range of its input frequency control voltage.

Basically, the oscillator section consists of two Schmitt triggers: one formed by transistors Q_3 and Q_4 , and the other formed by transistors Q_5 and Q_6 . The triggers share the two current sources (transistors Q_1 and Q_2), as well as resistor R_1 because of capacitor C_3 . Transistors Q_4 and Q_5 form a differential switch that allows only one Schmitt trigger to be on at a time.

The charge rate of capacitor C_3 determines the switching frequency of the Schmitt triggers and, therefore, the output frequency. This charge rate can be controlled by varying the voltage on the frequency-control input line, which, in turn, changes the current of transistors Q_1 and Q_2 . The output frequency can also be altered by changing the value of capacitor C_3 .

Temperature compensation is provided by zener diodes Z_1 and Z_2 . Transistor Q_7 compensates the base-emitter junctions of transistors Q_1 and Q_2 , while transistor Q_8 compensates transistors Q_3 and Q_6 . To achieve the best circuit performance, matched transistors and components having 1% tolerances should be used. □



Simplified design. Square-wave generator supplies complementary outputs whose frequency is determined by an input control voltage. This control voltage determines the current provided by transistors Q_1 and Q_2 to charge capacitor C_3 . The charge rate of this capacitor sets the switching frequency of the two Schmitt triggers, which are formed by transistors Q_3 and Q_4 and transistors Q_5 and Q_6 .

V_{EB} , is easily measured and is often used to find the temperature of the collector depletion layer.² The voltage stability factor is negative because collector current I_C increases as junction voltage V_{EB} decreases.

Since the term, $R_1(1 - \alpha)$, is very small, one way to diminish S_v is to make the load resistance, R_L , as large as possible. Unfortunately, I_C flows through R_L , and the stage's conversion efficiency will be reduced substantially. However, a large R_L can be obtained without the usual voltage drop degradation by using the collector resistance of a second transistor, as in (b).

With the T-model equivalent circuit for the common-emitter transistor, the output resistance of this configuration can be expressed as:

$$r_o = r_c(1 - \alpha) + r_e(r_b + \alpha r_c + R_g)/(r_b + r_e + R_g)$$

For this equation:

$$1/r_c(1 - \alpha) = \Delta i_c / \Delta v_{ce}|_{i_b}$$

$$\beta = \Delta i_c / \Delta i_b|_{v_{ce}}$$

$$\alpha = \beta / (\beta + 1)$$

All of these quantities can be readily obtained from the transistor's collector characteristics.³

The upper transistor in (b) provides an output resistance of 1,200 ohms, which yields a predicted voltage stability factor of 14.9×10^{-3} amperes per volt. If a fixed resistor of 1,200 ohms were used, it would have an IR drop of 60 v across it. But the voltage drop across both the transistor and its emitter resistor is only 3 v.

The graph shows the actual characteristics of the transistor stage as temperature rises from 30°C to 100°C. As temperature increases by 70°C, the base-emitter voltage drops by only 0.15 v and the collector current rises only 5 milliamperes. Without temperature compensation, the collector current would be 32 mA higher. □

REFERENCES

1. M.V. Joyce and K.K. Clark, "Transistor Circuit Analysis," Addison-Wesley, 1964, Chap. 3.
2. R.L. Pritchard, "Electrical Characteristics of Transistors," McGraw-Hill, 1967, p. 613.
3. R.P. Nanavati, "An Introduction to Semiconductor Electronics," McGraw-Hill, 1963, p. 163.

Simple gating circuit monitors real-time inputs

by David F. Hood
Bell-Northern Research, Ottawa, Canada

In normal operation, the set and reset inputs of the simple flip-flop circuit are not allowed to become active simultaneously, although both can remain at logic 0. But if this elementary rule is violated, a new gating function that can arbitrate real-time inputs is realized.

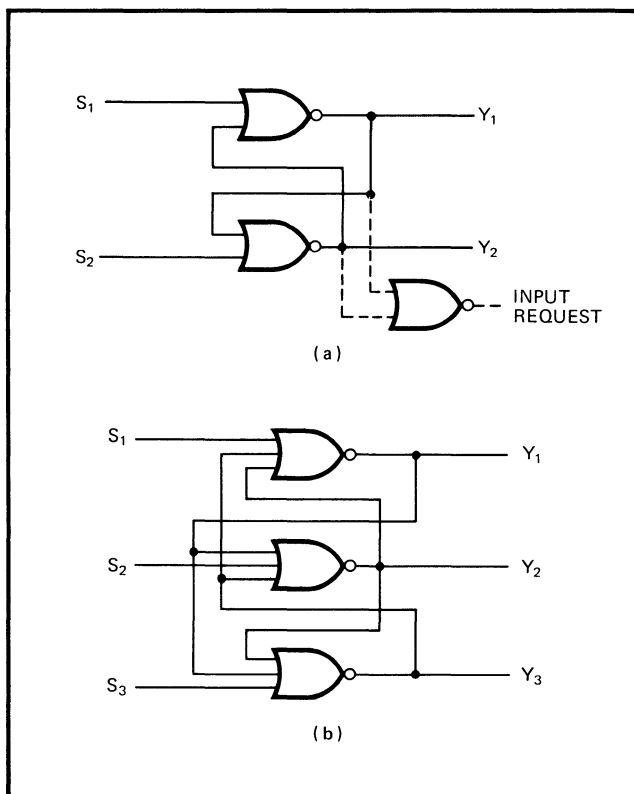
The circuit is particularly useful in signal-processing applications where interrupt requests may arrive asynchronously to be processed by a simple sequencer, rather than by a computing-type device. In such applications, the simplicity of the circuit also makes possible considerable cost savings.

When circuit (a) is used as a flip-flop, its S_1 and S_2 inputs are both low in the quiescent operating state. If the S_1 and S_2 inputs are both high instead, outputs Y_1 and Y_2 are low (in the quiescent mode). Now, when S_1 goes low, Y_1 goes high, and Y_2 does not change. But if S_2 then goes low, neither Y_1 nor Y_2 changes. And since the circuit is symmetrical, if S_2 goes low while S_1 is high, Y_2 will go high and lock out S_1 . The signal paths of S_1 - Y_1 and S_2 - Y_2 may be regarded as inverters with real-time priority arbitration. The addition of a third gate to the circuit provides an INPUT REQUEST lead.

With a third gate, the circuit can also be extended to accept three inputs, as shown in (b). Further extension is done in a similar manner. As with circuit (a), the first input that goes to logic 0 inhibits all the other inputs, while producing an output itself. Two or more inputs going to logic 0 simultaneously will produce a race condition that, nevertheless, can have only a single victor. One input can be handicapped relative to another by

using RC delay networks at the input or output of the handicapped gate.

The same operating description and circuit configurations apply if all the logic levels are inverted, and if NAND gates are substituted for the NOR gates. □



Lock-out gate. Both set and reset (S_1 and S_2) inputs to flip-flop (a) are kept high in quiescent state. When either S_1 or S_2 goes low, its output (Y_1 or Y_2 , respectively) will go high, but the other output stays low even if its input goes low. Since only one signal can pass to the output at a time, this gate can arbitrate asynchronous interrupt signals. An additional gate (b) accommodates another input.

Audio amplitude leveler minimizes signal distortion

by Edward E. Pearson
Burr-Brown Research Corp., Tucson, Ariz.

An ac current-controlled bridge in the feedback loop of an operational amplifier can provide very close control of signal amplitude, while contributing negligible distortion at or near a predetermined optimum input signal level. The resulting circuit is well suited for amplitude leveling in test oscillators, communications equipment, and telemetry systems. It can be built for around \$4 and offers extremely close amplitude control over the entire audio spectrum.

Unlike conventional circuits that apply increasing amounts of feedback along the entire span of input voltage range, this amplitude leveler applies zero feedback (and, therefore, zero distortion) at an optimum input level and produces positive or negative feedback above and below this level. The differential output from a bridge is used to get the desired feedback.

The bridge, which is outlined in color, employs two devices, T_1 and T_2 , whose resistance varies with current. Such components as incandescent lamps, thermistors, or even active devices can be used. Here, T_1 and T_2 are incandescent lamps. Resistors R_1 and R_2 are chosen to be within the resistance range of T_1 and T_2 .

A specific voltage, V , will shift the resistance of T_1 and T_2 , balancing the bridge and producing a zero differential output ($e_1 - e_2$). As voltage V is varied above and below the zero output level, the bridge is unbalanced in opposite directions and develops differential outputs of opposite phase.

Letting $R_1 = R_2 = R$ and $T_1 = T_2 = T$, voltage e_1 can be expressed as:

$$e_1 = TV/(T+R)$$

and voltage e_2 is:

$$e_2 = RV/(T+R)$$

so that the differential voltage becomes:

$$e_1 - e_2 = (T - R)V/(T + R)$$

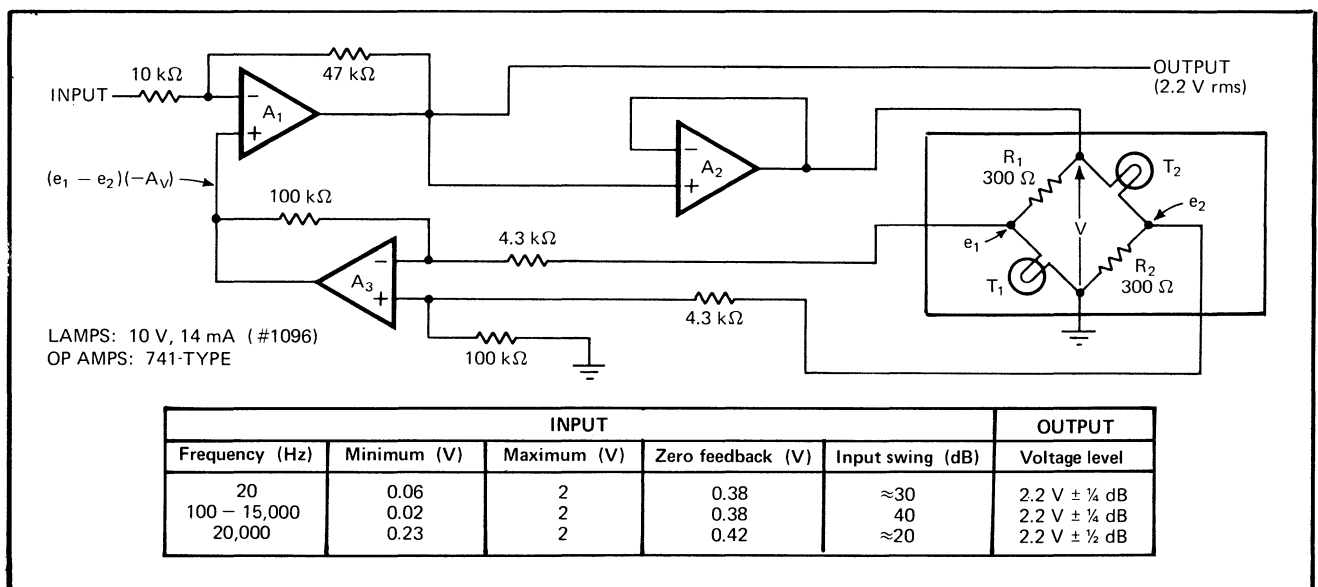
When T is greater than R , $e_1 - e_2$ is more than zero; when $T = R$, $e_1 - e_2 = 0$; and when T is less than R , $e_1 - e_2$ is smaller than zero.

Depending on the input signal level present at amplifier A_1 , the network formed by the bridge and amplifiers A_2 and A_3 produces positive, negative, or zero feedback. For the component values indicated, an input voltage of approximately 0.4 volt is just sufficient to drive the bridge to a balanced condition (zero feedback).

At this input level, the components in the feedback network cannot contribute to distortion in the output. If the input voltage varies from the optimum 0.4-v level, the inputs to amplifier A_3 will become unbalanced, and an amplified differential voltage (from the bridge) will produce gain compensation at amplifier A_1 . The table indicates the range and degree of amplitude control obtained.

The circuit's output voltage can be made higher by increasing the value of resistors R_1 and R_2 ; the higher resistance values increase the voltage needed to balance the bridge. Or, the output voltage can be made smaller by increasing the gain of amplifier A_2 . To lower the optimum input voltage level, the gain of amplifier A_1 is made higher.

Because increasing amounts of positive feedback are present at the input to amplifier A_1 , the circuit becomes unstable at very low or zero input levels. The table shows the minimum permissible input levels; the circuit must be modified to accommodate input signal dropouts. □



Leveling audio signals. Rather than increasing feedback with increasing input voltage, audio amplitude leveler operates at zero feedback for an optimum input voltage. Current-controlled bridge in feedback loop of amplifier A_1 develops the differential voltage needed to keep the output level steady. The incandescent lamps act as current-variable resistors that balance the bridge when input voltage is 0.4 volt.

Ice warning indicator monitors road conditions

by Steven E. Summer
Hauppauge, N.Y.

For more than 10 years, Rover automobiles have had a built-in indicator that warns their drivers of possibly icy roads. With the availability of the versatile and economical integrated quad op amp, this same safety feature can now be installed quite easily in any make of automobile.

The ice warning indicator shown monitors ambient air temperature to alert the driver to the conditions under which ice will start forming on the roads—that is, when air temperature is between 32°F and 36°F in wet weather. The device is rugged and provides good noise rejection.

The circuit produces a variable duty cycle to control the flash rate of a light-emitting diode. At 36°F, low-duty-cycle light flashes are generated, and as the temperature drops towards 32°F, the LED indicator remains on continuously. The flashes occur about once a second.

A thermistor with a nominal resistance of 15 kilohms at 25°C acts as the temperature-sensing probe. It is

mounted in a baffled enclosure that is exposed to ambient air. The baffle prevents erroneous readings due to air movement.

The circuit's three amplifiers are part of the same chip as the quad op amp. Since circuit action depends on current ratios, circuit operation is insensitive to variations in battery voltage, making zener regulation unnecessary.

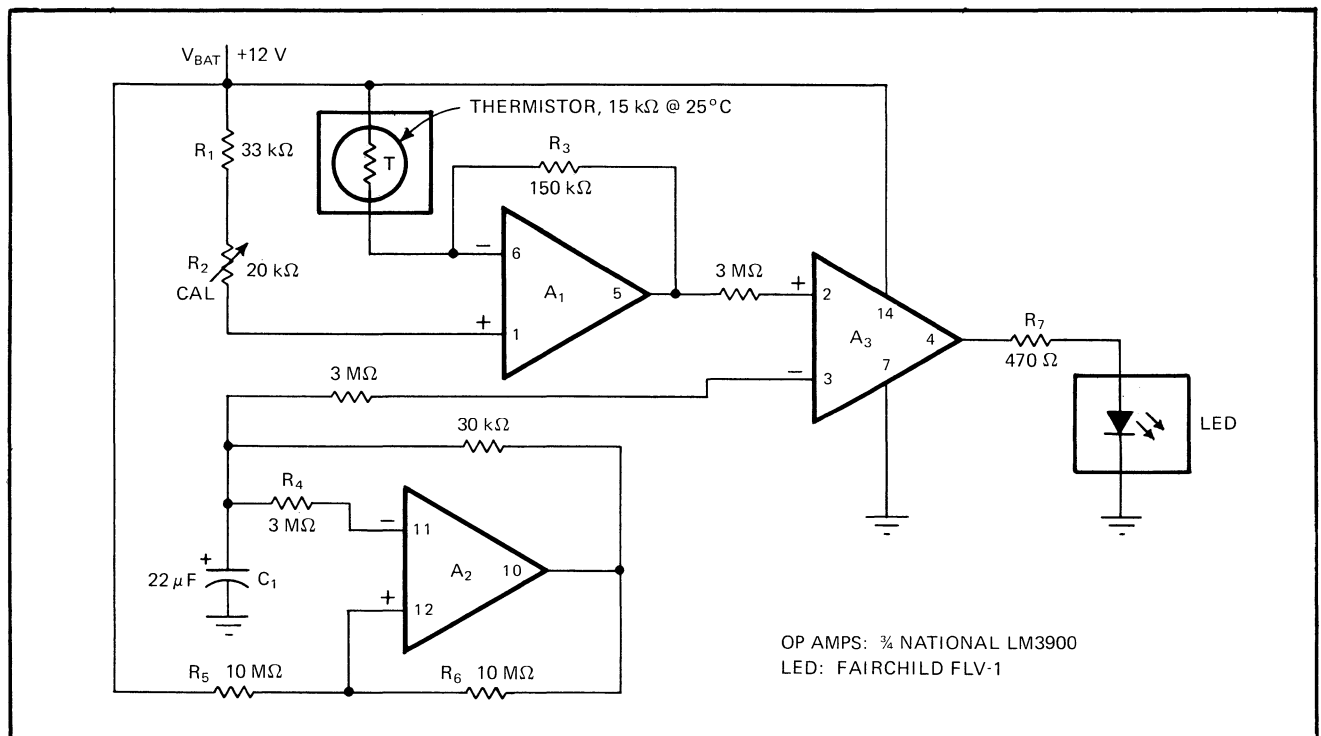
Amplifier A_1 compares the resistance of the thermistor to the series combination of resistors R_1 and R_2 . Feedback resistor R_3 sets the correct slope of A_1 's output-voltage response to temperature. At 32°F, A_1 's output is $0.6V_{BAT}$; at 36°F, it's $0.3V_{BAT}$.

Amplifier A_2 is connected as a free-running multivibrator having a repetition rate of approximately one pulse per second. Three resistors— R_4 , R_5 , and R_6 —set the upper and lower voltage limits for capacitor C_1 at $0.6V_{BAT}$ and $0.3V_{BAT}$, respectively.

The outputs of amplifiers A_1 and A_2 are compared by amplifier A_3 . When the multivibrator (A_2) output is lower than A_1 's output, A_3 's output goes positive, lighting the LED. Resistor R_7 limits LED current to around 25 milliamperes.

Resistor R_2 , which calibrates the circuit, is adjusted by placing the thermistor probe in an ice slurry and setting R_2 so that the LED is always on. Other operating points can be obtained by changing the values of resistors R_1 , R_2 , and R_3 . □

Driving aid. Ice warning indicator, which puts the flexibility and economy of the quad op amp to work, uses a thermistor probe to sense air temperature. At 36°F, the LED indicator flashes once per second. This flash rate increases as temperature approaches 32°F until the LED remains on continuously. A varying-duty-cycle output determines the flash rate. Amplifier A_2 is wired as a free-running multivibrator.



Single-supply reference source uses self-regulated zener

by William Goldfarb
Cornell University, Ithaca, N. Y.

Temperature-compensated zener diodes provide a reference voltage that remains stable despite changes in time and temperature. But they exhibit a rather large dynamic impedance, from 100 to 400 ohms, and current supplied to them must be regulated precisely.

By using voltage comparison, one of these reference zeners can be made to control its own current, eliminating the need for a separately regulated temperature-compensated current source. A precision voltage reference source can then be realized with only a single unregulated power supply. And the cost of the circuit will be dominated by the cost of the zener, keeping parts cost to somewhere around \$6.

The voltage reference source in the diagram provides a nominal output voltage of 10 volts that is stable to within ± 7 millivolts. It can operate over a supply voltage range of 12 to 18 v. With the output voltage at V_{REF} , the current through the zener is:

$$I_Z = V_{REF} - V_Z / R_1$$

Making do with one supply. Voltage reference source, which operates from a single power supply, maintains its output at 10 volts ± 7 millivolts over a 75°C temperature range and with $\pm 10\%$ supply variations. Through voltage comparison, the zener reference regulates its own current, thereby eliminating the usual zener constant-current source. The circuit's maximum output current is 30 milliamperes.

The current-booster transistor actively keeps the voltage at the inverting input of the operational amplifier at:

$$V_1 = V_{REF} R_2 / (R_2 + R_3) = I_Z R_1$$

Zener current I_Z can then be expressed as:

$$I_Z = V_{REF} R_2 / R_1 (R_2 + R_3)$$

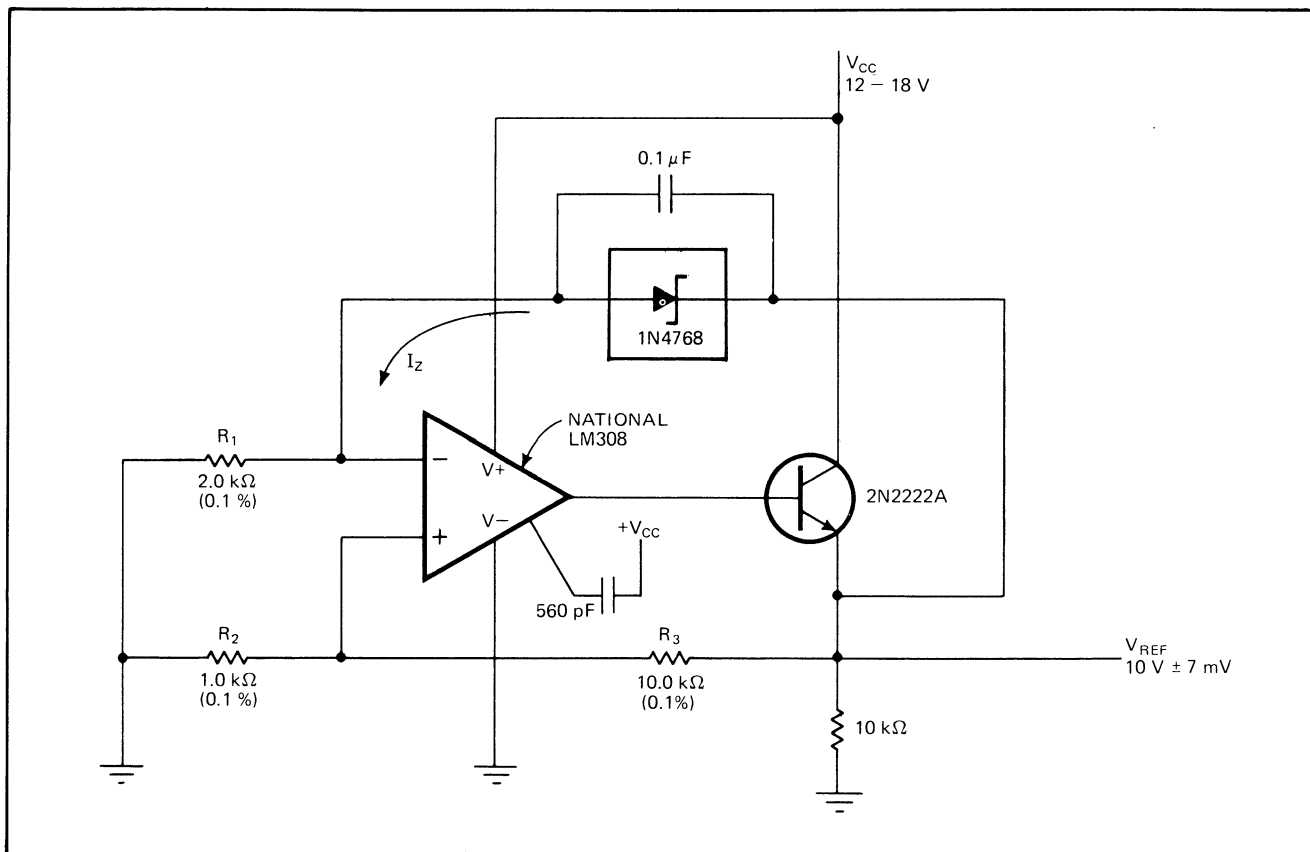
And reference voltage V_{REF} is held to:

$$V_{REF} = V_Z (R_2 + R_3) / R_3$$

A pitfall in any dc bootstrap scheme like this is the possible existence of stable states other than the desired one. For this circuit, such a state exists when the output voltage is zero. Connecting a capacitor between the power supply and the op amp's compensation input prevents the circuit from being locked into the zero-output-voltage state when it is first turned on. The capacitor causes the turn-on transient to put the circuit into the desired condition, with the output voltage at V_{REF} .

For the components shown, the output is stable to within ± 7 mV over a temperature range of 0°C to 75°C, even with a supply variation of $\pm 10\%$. The output current is 30 milliamperes maximum. The capacitor across the zener serves to attenuate noise that may be generated by the zener at high operating frequencies.

A negative output voltage can be obtained by reversing the diode, using a pnp instead of an npn transistor, and grounding the op amp's positive supply input. □



Eliminating offset error in sense amplifiers

by Dan Chin
Cambridge Memories, Newton, Mass.

A sense amplifier for a memory must detect a pulse signal during a gated time interval. But a significant error occurs at the amplifier's output when its input offset voltage is large in comparison with the voltage amplitude of the pulse signal.

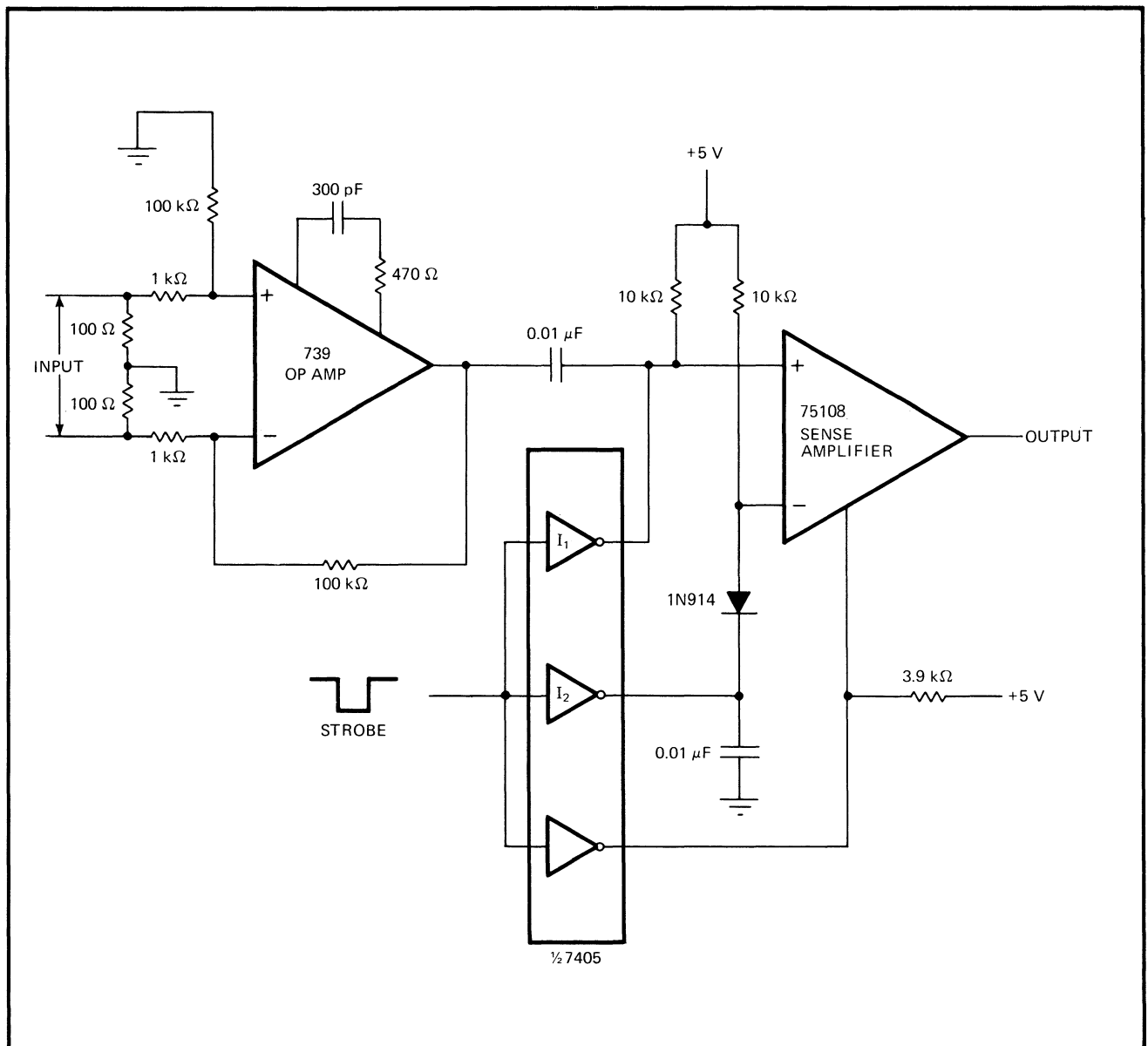
If the offset voltage is removed by ac coupling, however, the pulse's baseline could shift when the readout data pattern changes. But if, in addition to being ac-

coupled, the pulse is held to ground except during the time interval of interest, a reference voltage can be developed and the pulse compared to it.

The dc-restored sense amplifier in the figure makes use of this technique. The input operational amplifier performs as a basic linear amplifier, providing a signal gain of 100. The amplifier's output is ac-coupled to the sense amplifier for detection.

Dc restoration is accomplished by the open-collector inverters connected to the inputs of the sense amplifier. Two of the inverters, I_1 and I_2 , assure that any offset voltage is applied equally to both inputs of the detector, permitting offset error to be eliminated by the detector's common-mode rejection. The diode in series with the detector's negative input sets the threshold level halfway between the pulse baseline and the minimum expected peak voltage. □

Sensing pulses, barring offset errors. Data is ac-coupled from the operational amplifier to the sense amplifier to get rid of offset-voltage error. The dc signal level is then restored by open-collector inverter gates. Any additional offset error is eliminated by the sense amplifier's common-mode rejection because inverters I_1 and I_2 , at each of the sense amplifier's inputs, introduce equal offsets.



Stable crystal oscillator works over wide supply range

by Terence King
Oroco Communications Inc., Middletown, N. Y.

If single-gate MOSFETs are wired as a modified Pierce oscillator and an isolating source-follower, they form a crystal oscillator that has unusual supply-voltage stability. This crystal-controlled clock is not expensive to build, interfaces easily with transistor-transistor-logic circuits, and can operate directly from a 5-volt supply.

Changes in output frequency due to supply-voltage variations are very small because of the high-value source resistors in both stages and the large fixed capacitances in the gate and drain loops of the oscillator stage. Even if the supply voltage increases from 3 to 9 v, output frequency changes by less than 1 hertz from its nominal 1-megahertz value.

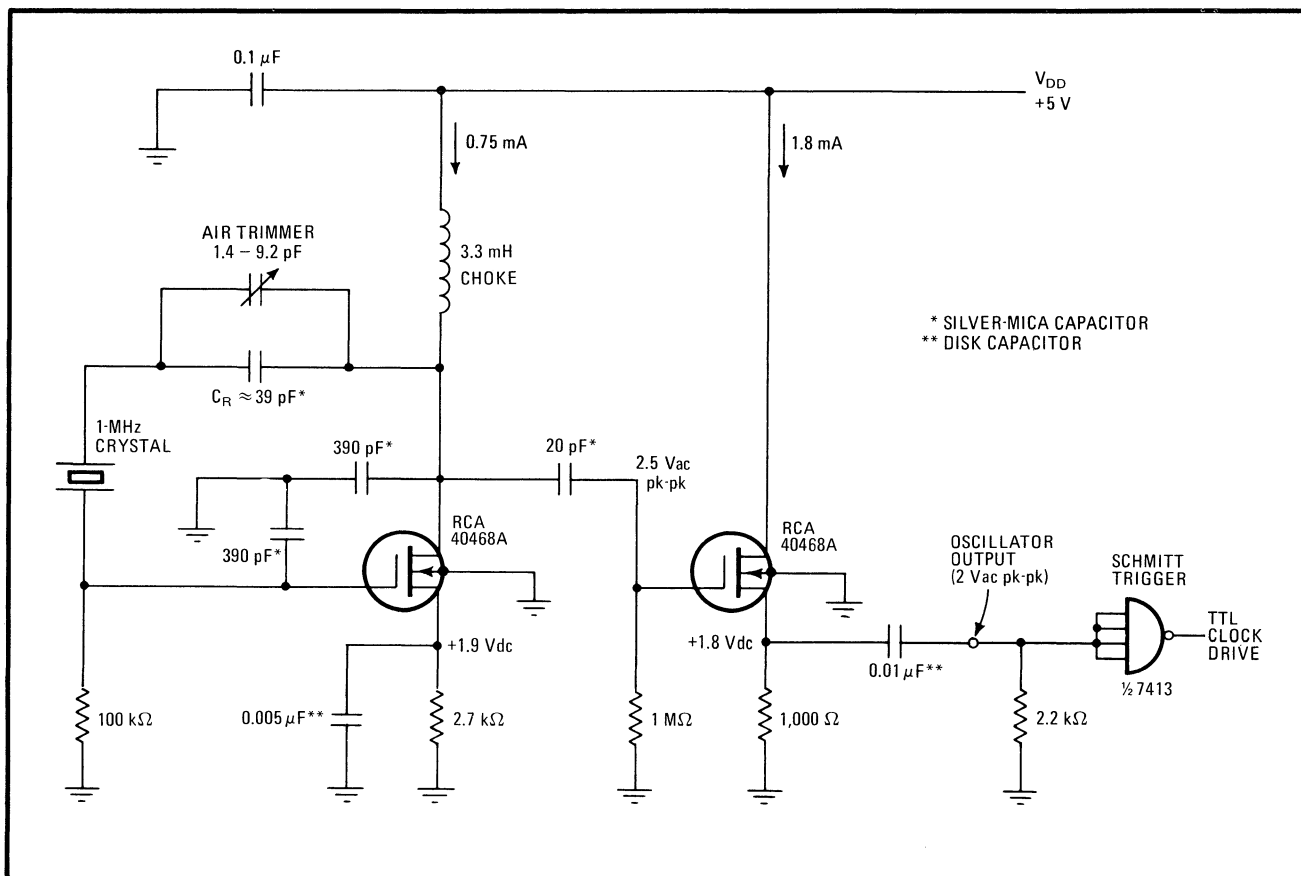
Since the circuit itself is very stable, the over-all performance of the oscillator depends principally on the

quality of the crystal. A good oven-stabilized crystal should maintain a stability of one part in 10^{-8} per day after warmup. And if ambient temperature is fairly stable, the whole circuit will approach this performance.

An excellent interface to TTL circuits can be provided by a type-7413 Schmitt trigger. The pull-down resistor of 2.2 kilohms biases the Schmitt trigger within its hysteresis characteristic without excessively loading the oscillator's source-follower. A type-7413 trigger will provide reliable TTL driving with as little as a 3-v supply applied to the oscillator.

The Schmitt's output is rich in rf harmonics and can be beat against a WWV broadcast of the National Bureau of Standards at 10 MHz, allowing adjustment of the oscillator to within 0.1 Hz of its nominal operating frequency without much difficulty. This sort of monitoring also permits relatively sensitive day-to-day checks of the circuit's short-term and long-term stability. Oscillator performance can then be established as a secondary frequency standard that is traceable directly to the National Bureau of Standards.

Capacitor C_R sets the range of the calibration of the trimmer capacitor. The value of C_R may vary with different makes and types of crystals. □



Supply immunity. Output frequency of crystal-controlled oscillator changes less than 1 hertz even when supply voltage varies from 3 to 9 volts. The circuitry—a modified-Pierce-oscillator MOSFET and a source-follower MOSFET—is so stable that over-all oscillator performance depends mostly on the crystal. A Schmitt trigger makes an excellent interface for using the oscillator to drive TTL devices.

Varistor voltage divider improves receiver agc

by M.J. Salvati

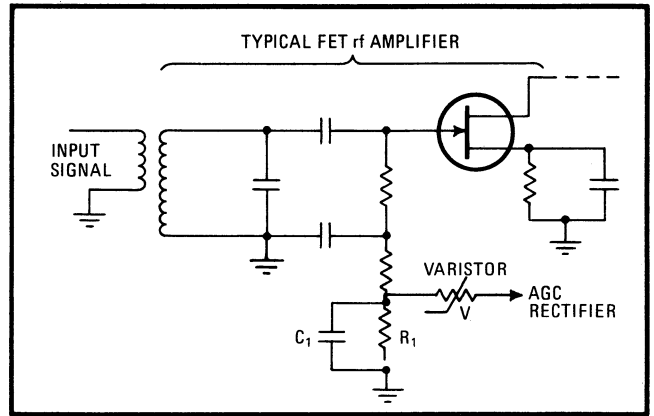
Sony Corp. of America, Long Island City, N.Y.

Adding a varistor to the automatic gain-control circuitry in a communications receiver is a simple way to improve output-signal leveling. The varistor and a fixed resistor make up a variable voltage divider that is placed between the rf amplifier and the agc rectifier.

This arrangement improves the effectiveness of the agc circuitry because the percentage of the agc voltage applied to the controlled rf-amplifier stage varies in the same direction as the input-signal level. Furthermore, at low signal levels, this percentage is very small, allowing the amplifier to operate at maximum gain for the best noise-figure performance. The varistor agc, therefore, provides the benefits of delayed agc (or manually switching off the agc) without the abrupt discontinuity in control characteristic of the latter technique.

When the agc voltage is at its highest level (for a strong signal), the varistor's resistance is low, causing most of the agc voltage to appear across resistor R_1 . This provides maximum gain reduction. When the agc voltage is at its lowest level (for a weak signal), the varistor's resistance is high and only a small agc voltage appears across the resistor, producing very little gain reduction.

The resistance values of the varistor and the resistor are selected so that the varistor is about half the value of the resistor when the agc voltage is at its maximum level (for the largest expected input signal). This selection will provide the best receiver output-signal leveling for inputs ranging from 1 to 1,000 millivolts and the best receiver noise figure (because of nearly complete agc turnoff) for inputs below 10 microvolts.



Varistor agc. Variable voltage divider formed by a varistor and a fixed resistor gives the advantages of delayed automatic gain control without any abrupt discontinuities. The varistor resistance becomes low for strong signals and high for weak signals, thereby varying the agc voltage applied to the controlled rf-amplifier stage. The scheme enhances receiver sensitivity and improves output-signal leveling.

The resistance values actually chosen for the varistor and resistor will depend on the signal levels available at the agc rectifier. In general, resistor R_1 will be about 2 megohms for vacuum-tube receivers and about 100 kilohms for semiconductor receivers. Since the time constant of the agc filter formed by the varistor, the resistor, and capacitor C_1 changes with signal level, the value of the capacitor should be chosen for adequate filtering of modulation variations when the varistor resistance is half the value of the resistor.

When included in all the controlled stages (along with the rf amplifier stage) of a semiconductor receiver, varistor agc can improve receiver sensitivity by 3 decibels, halve the decibel change in receiver output for a given change in input level, and increase the receiver's absolute output level by 8 to 12 dB. □

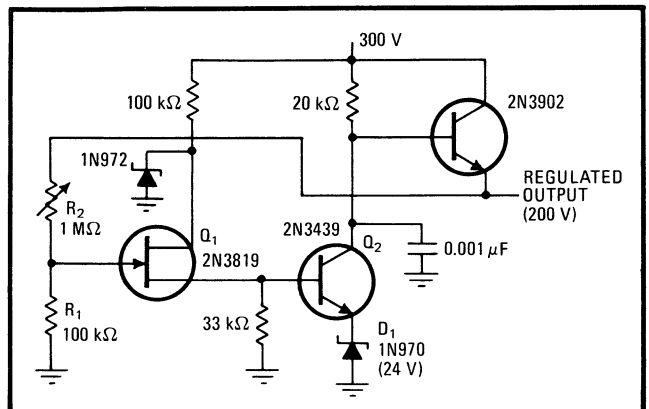
Regulating high voltages with low-voltage zeners

by Glen Coers

Texas Instruments, Components Group, Dallas, Texas

A regulator for a high-voltage power supply can be built with a low-voltage zener acting as the reference-voltage source. The output of this regulator circuit can be adjusted between 50 and 250 volts, and regulation is typically 0.5%. The circuit is particularly useful when operational amplifiers cannot be employed because the low-voltage positive and negative supplies needed to power them are not readily available.

Zener diode D_1 supplies the reference voltage. It should be chosen according to the temperature coefficient desired and the maximum current required. The



Discrete-component regulator. High-voltage power-supply regulator produces output of 50 to 250 volts at a typical regulation of 0.5%. A low-voltage zener, D_1 , provides the reference voltage, establishing the circuit's current output and its temperature coefficient. The field-effect transistor, Q_1 , allows large-value low-wattage resistors to be used for R_1 and R_2 , thereby minimizing loading.

REGULATOR PERFORMANCE

| INPUT VOLTAGE | OUTPUT VOLTAGE | LOAD CURRENT | OUTPUT VOLTAGE |
|-------------------------|----------------------------|--------------------------|----------------------------|
| 270 V } $\Delta = 30$ V | 199.2 V } $\Delta = 1.2$ V | 0 mA } $\Delta = 50$ mA | 200.3 V } $\Delta = 0.3$ V |
| 300 V } $\Delta = 30$ V | 200.4 V } $\Delta = 0.8$ V | 50 mA } $\Delta = 50$ mA | 200.0 V } $\Delta = 0.5$ V |
| 330 V } | 201.2 V } | 100 mA } | 199.5 V } |

field-effect transistor, Q_1 , allows resistors R_1 and R_2 to have high values so that output loading can be kept to a minimum and low-wattage resistors can be used. If these resistors were connected directly to the base of transistor Q_2 , the circuit would provide poor regulation and have a high dynamic output impedance because of Q_2 's low input impedance.

The regulator's output voltage can be written as:

$$V_o = (V_{D1} + V_{BE} + V_{GS})(R_1 + R_2)/R_1$$

The open-loop gain of transistor Q_2 , which is equal to

67 decibels, is a function of the FET's transconductance and the circuit's load resistance. The feedback factor, β , for the regulator is:

$$\beta = R_1 / (R_1 + R_2)$$

where $R_2 = 9R_1$

The closed-loop voltage gain, which equals 20 dB, can be expressed as:

$$A_{VC} = A_{V_o} / (1 - A_{V_o}\beta)$$

And the gain with feedback becomes:

$$A_{Vf} = 67 - 20 = 47 \text{ dB}$$

□

More applications for the 741-type op amp

by Edward Beach

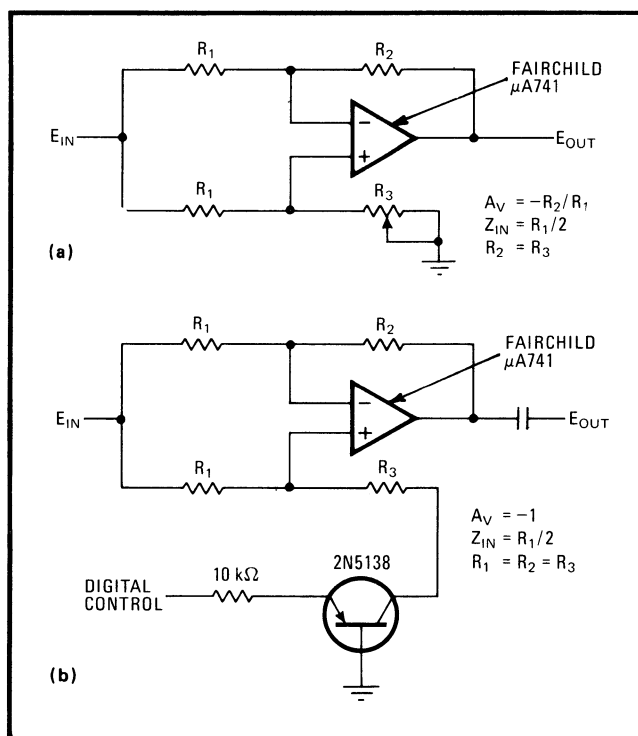
McGraw-Hill Continuing Education Center, Washington, D.C.

The large common-mode rejection ratio of the popular 741-type op amp makes it possible to realize a variable-gain amplifier and even an analog switch quite inexpensively. The gain of an op amp can easily be changed by varying the proportion of the signal applied to both its inputs. If equal signals exist at each input, there is no output because of the op amp's common-mode rejection, but applying more signal to one input than the other will result in useful gain.

For the variable-gain amplifier of (a), resistors R_1 and R_2 are selected in the usual manner—with regard to the required input impedance ($R_1/2$ in this case) and overall gain ($-R_2/R_1$). Feedback resistor R_2 may have to be trimmed to provide maximum attenuation when the gain-control resistor, R_3 , is set to its maximum value ($R_3 = R_2$). In practice, the voltage gain can be varied from zero to $-R_2/R_1$ as the gain control goes from maximum to zero, and there will be no shift in the dc output.

The circuit can also be used as an analog switch, as shown in (b). For this application, however, there are a few restrictions. The output must be capacitively coupled, the input signal must be less than 1.2 volts peak to peak, and the amplifier must be set up for unity gain ($R_1 = R_2 = R_3$). But within these limitations, the circuit makes an excellent analog switch.

When a logic 1 (2.4 to 4 v) is applied to the digital control input, the transistor saturates, effectively grounding resistor R_3 to give an attenuation of 70 to 90 dB. As the transistor turns on, the op amp's noninverting input goes to approximately 0.6 v dc, causing the dc



Handy circuits. Everyday 741-type op amp can be used as a variable-gain amplifier (a) or an analog switch (b). Only four external resistors are needed for the amplifier circuit, which maintains the same dc output as the gain is varied. For the analog switch, the op amp passes the input signal when the digital control line is grounded. The 741's large common-mode rejection permits it to perform well.

output voltage to also be 0.6 v and making an output coupling capacitor necessary.

A logic 0 (ground) input turns the transistor off, allowing the op amp's noninverting input to float so that the signal passes through the amplifier. If the signal becomes positive enough to forward-bias the transistor's base-collector junction, the output signal will be distorted on positive peaks.

□

TTL interface circuit synchronizes computer clock

by Jim Crapuchettes
Stanford University Medical Center, Stanford, Calif.

A clock-synchronization circuit for computer interfacing allows the counter of a continuously running real-time clock to be read by the computer when the counter is not changing. The circuit requires only two TTL IC packages. The normal approach is to use complicated circuits requiring a latch or flip-flop for each bit of the clock counter.

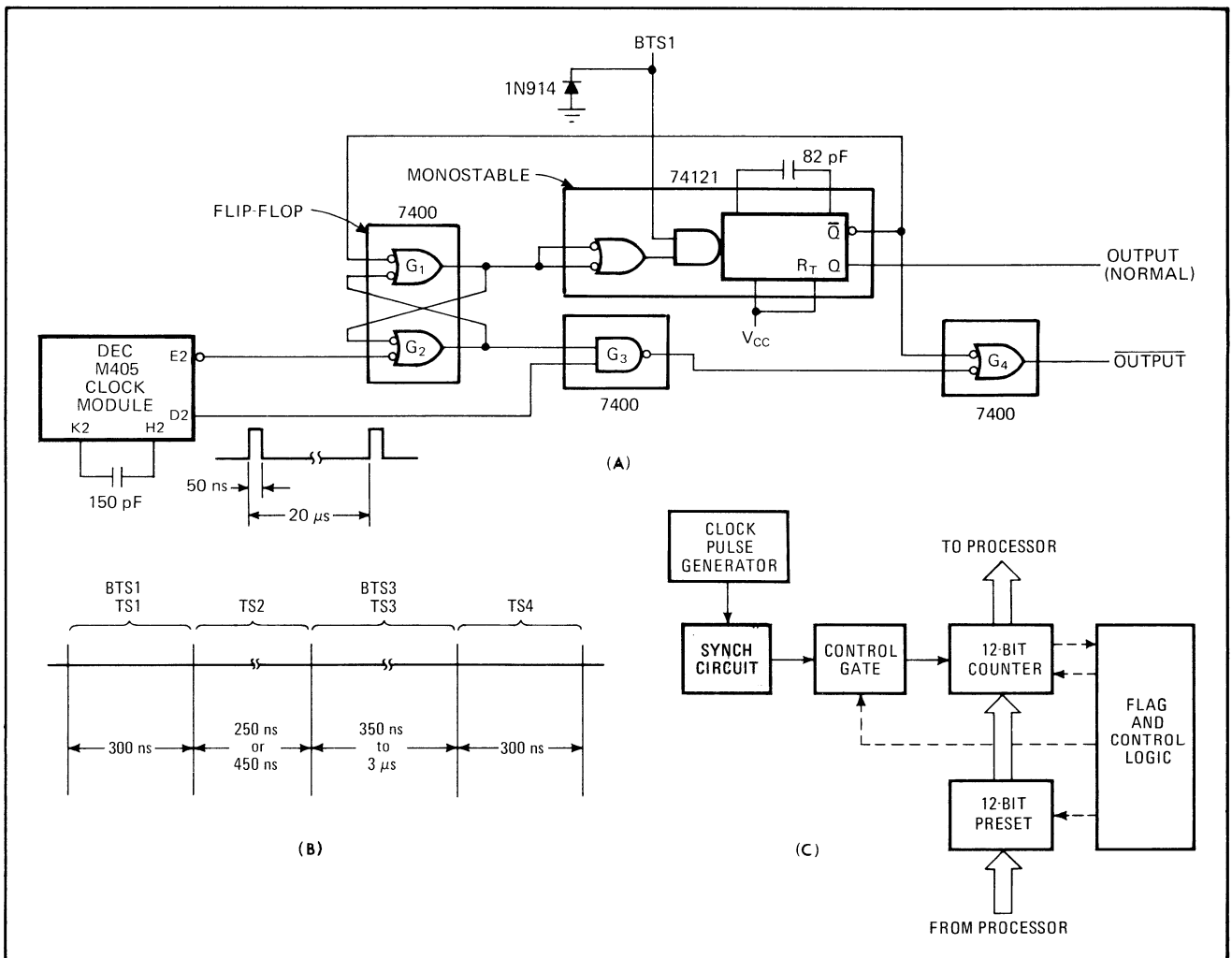
There are only two restrictions on the two-IC clock-synchronization circuit: the computer processor must have time states available for the circuit, and the longest

cycle time for the processor must be shorter than the period between two successive pulses from the system's clock-pulse generator.

Essentially, this simple circuit (a) forces the clock into synchronization with the processor, rather than trying to synchronize the processor with the clock. This is done by letting the contents of the clock counter be changed only during that portion of the processor cycle in which the counter cannot possibly be read by the processor.

This particular synchronization circuit is designed for the PDP-8/E minicomputer with an external I/O bus option, which is made by Digital Equipment Corp. of Maynard, Mass. The circuit can also work directly from DEC's Omnibus bus design, and it can be applied directly to DEC's PDP-8/I, PDP-8/L, and PDP-12 minicomputers.

The processor cycle, which is drawn in (b), is split into four time states, TS1 through TS4. Two of these time states, TS1 and TS3, are brought out from the processor



Reading out data. Synchronization circuit (a) forces real-time counter clock to be in step with computer processor so that data is read only when the counter is not changing. The delay, time state TS2, in the processor's timing cycle (b) between counter changes (TS1) and the execution of I/O instructions (TS3) is used. Block diagram (c) of real-time clock indicates where sync circuit goes.

on the I/O bus as buffered time states, BTS1 and BTS3. All I/O instructions are actually executed during TS3, and there is a minimum delay of 250 nanoseconds between TS1 and TS3. Therefore, as long as the contents of the clock counter changes only during TS1 and all carries across the counter are finished in less than 250 ns, the counter changes and the computer readouts cannot overlap. The diagram (c) of the system's real-time clock shows the circuit's location.

A pulse from the clock-pulse generator sets the R-S flip-flop formed by gates G_1 and G_2 . The next occurrence of time state TS1 (it may be occurring when the flip-flop is set) will trigger the monostable multivibrator. (The 74121 is used here because it produces a fixed-length pulse or none at all, contains part of the necessary gating, and has complementary outputs.) The diode, which is between the monostable and ground, prevents undershoot from the BTS1 line of the I/O bus.

The \bar{Q} pulse output from the monostable resets the flip-flop. To be sure that the flip-flop will always be reset, the duration of this \bar{Q} pulse must be longer than the duration of the pulse from the clock pulse generator. Since this clock pulse is 50 ns, an 82-picofarad capacitor is added to stretch the monostable pulse to about 100 ns.

The flip-flop has no provision for initialization to the reset state, but it will be set correctly within one cycle of

the processor. Initialization is necessary only if the clock control gating is between the clock-pulse generator and the synchronization circuit.

Gates G_3 and G_4 are needed if the clock must continue to run even when the processor is in the halt (pause) state and if the processor does not halt in the time state used for clock counting. In the case of the PDP-8/E, the processor halts in TS1, so these gates are not needed.

When used, they cause the pulses from the clock generator to be gated directly to the circuit's output if the flip-flop is set. As soon as the processor returns to the run state, the flip-flop releases the pulse it has been holding, triggering the monostable and allowing the normal sequence to continue.

The correct number of pulses, therefore, always passes through the circuit, whether the processor is running or not. The only difference will be a long pulse period when the processor is halted and a short pulse period when it continues.

It should be noted that the same synchronization technique could be used with a computer that has only one time state brought out to peripherals. The trailing edge of that time state could be used to trigger a monostable whose output pulse would perform the same function as the BTS1 pulse of this circuit. \square

Analog-to-digital converter produces logarithmic output

by Ronald Ferrie
Communications & Controls Co., Pittsburgh, Pa.

When the logarithm of a signal voltage must be converted to a digital number, a log converter is normally used in conjunction with an analog-to-digital converter. But the circuitry involved becomes much simpler if the a-d converter is made to perform the log conversion itself. The resulting digital log converter has a two-decade dynamic range that can be set over a wide range of voltage levels.

In the circuit, a START pulse sets flip-flop FF_1 and resets the counter to zero. This action closes switch S_1 and opens switch S_2 . (Field-effect transistors are used for these switches.) The unknown input voltage is now applied to the integrator, charging capacitor C through R_1 .

The reference voltage for the comparator is initially set at zero. As the output voltage from the integrator passes through zero, gate G_1 is enabled so that pulses from the oscillator enter the counter at frequency f_0 .

When the counter is filled (N pulses accumulated), the next pulse causes the counter to return to zero and to generate a carry-out pulse that resets flip-flop FF_1 . This opens switch S_1 , disconnecting the input voltage from the integrator, and closes switch S_2 , causing capacitor C to discharge through resistor R_2 . Also, the comparator reference voltage becomes E_R .

The integrator's output voltage decays until it reaches

the comparator reference of E_R . This decay period is:

$$t_x = R_2 C \ln(E_{o(pk)}/E_R) = R_2 C \ln(E_i N / R_1 C f_0 E_R)$$

At time t_x , the comparator output goes to zero, inhibiting gate G_1 and terminating the count. During the decay period, pulses still enter the counter at frequency f_0 and accumulate for a count of:

$$N_x = f_0 t_x = f_0 R_2 C \ln(E_i N / R_1 C f_0 E_R)$$

Since time t_x began with the counter set to zero, this equation represents the total count stored at the end of the decay period. The expression can be rewritten as:

$$N_x = K_0 \ln(E_i / K_1) - \alpha$$

where:

$$K_0 = f_0 R_2 C$$

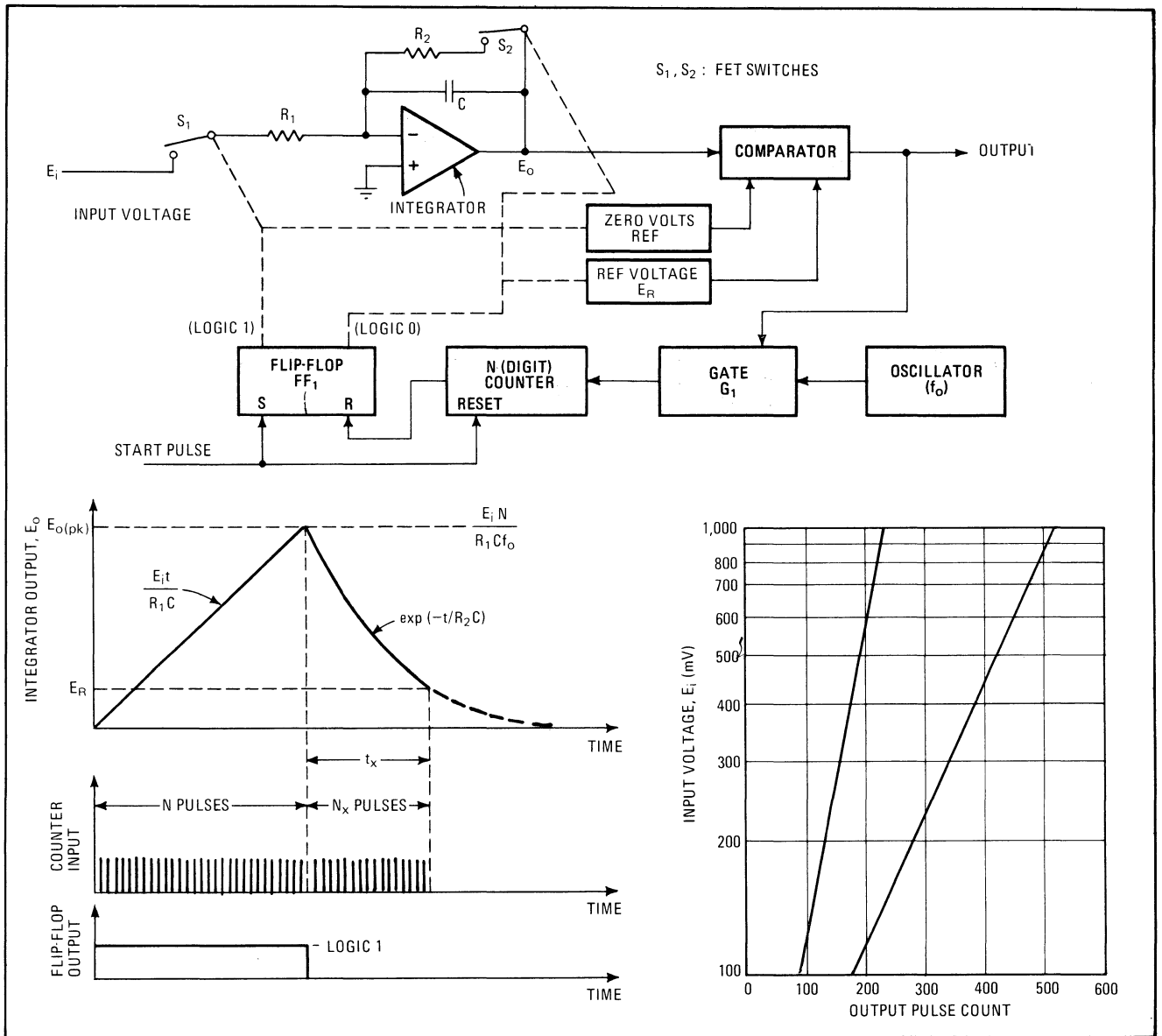
$$K_1 = R_1 C f_0 E_R / N$$

$$\alpha = K_0 \ln(K_1)$$

The second equation for N_x shows that the number stored in the counter at the end of the cycle is proportional to the logarithm of the input voltage minus a constant term, α . The plot of output count versus input voltage shows two typical performance curves for different values of K_0 and α .

The log converter nominally has a two-decade dynamic range, which can be extended to about three decades easily and to about 3.5 decades with some difficulty. This dynamic range can be set at almost any voltage level, depending on the components selected. The low-voltage limit is primarily determined by the drift and offset voltage of the integrator op amp. And resistor voltage ratings limit the high-voltage level.

Typically, a two-decade log converter built this way, and having an α value of zero, will accept inputs of 1 to 100 volts, producing an output pulse count of 0 to 460. For such a converter, $N = 1,000$, $f_0 = 50$ kilohertz, $R_1 = 100$ kilohms, and $C = 2$ microfarads. \square



Digital log converter. Modified a-d converter provides logarithmic output over two-decade dynamic range. Integrator capacitor C charges from input voltage until counter accumulates N pulses. When counter resets and begins to count again, the capacitor discharges until integrator output reaches comparator reference E_R . Converter's output for this decay time, t_x , is proportional to the log of the input.

Analog multiplier/divider simplifies frequency locking

by Moise Hamaoui
Fairchild Semiconductor, Mountain View, Calif.

In phase-locked loops, servo systems, and TV receivers, it is often necessary to lock two different frequencies together. The conventional method is quite cumbersome. First the higher of the two frequencies is divided down to a value close to that of the lower frequency. Then a signal that is proportional to the difference between the stepped-down frequency and the low frequency is generated. Lastly, this signal is used to adjust the high fre-

quency so that it is locked to the low frequency.

The analog multiplier/divider shown, however, locks the two frequencies in one step. The block diagram illustrates how the circuit accepts pulses of frequency f_{in} and generates pulses at frequency $f_{out} = Mf_{in}$, where M is a constant determined by the designer.

Dc voltages V_1 and V_2 are proportional to the two frequencies to be locked together:

$$V_1 = K_1 f_{in}$$

$$V_2 = K_2 f_{out}$$

The output voltage is the difference between these two:

$$V_{out} = A(V_1 - V_2) = A(K_1 f_{in} - K_2 f_{out})$$

where A is the gain of the differential amplifier. The output frequency is given by:

$$f_{out} = K V_{out} = KA(K_1 f_{in} - K_2 f_{out})$$

which can be rewritten as:

$$(K_1 f_{in} - K_2 f_{out}) / f_{out} = 1/KA$$

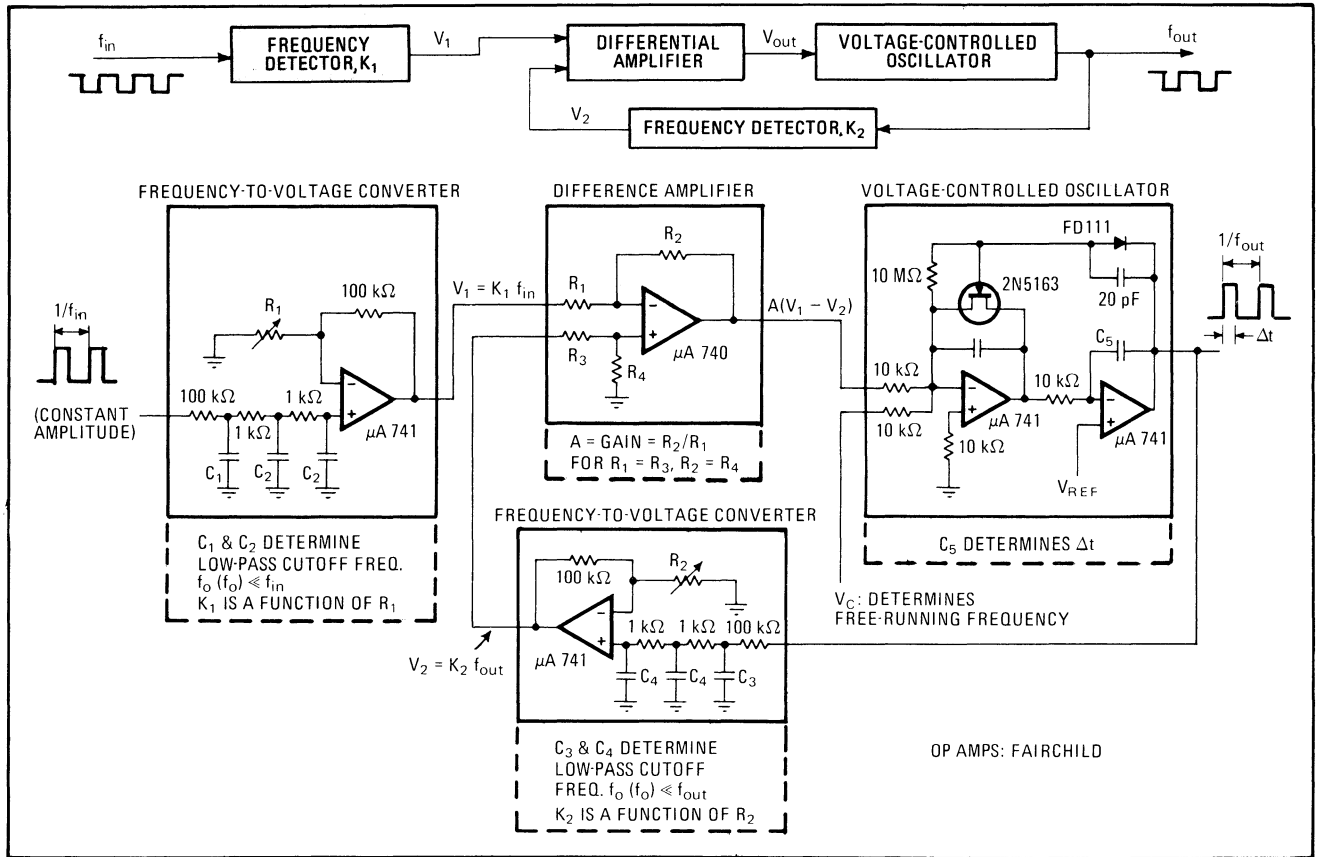
As amplifier gain A becomes very large:

$$K_1 f_{in} - K_2 f_{out} \approx 0$$

Solving for f_{out} yields:

$$f_{out} = (K_1/K_2) f_{in} = M f_{in}$$

By varying K_1 and K_2 , then, the input frequency can be multiplied or divided by any factor. For the hardware implementation shown, either f_{in} or f_{out} may range from 30 hertz to 10 kilohertz. □



Step saver. In single operation, analog multiplier/divider locks two different frequencies together. Differential amplifier accepts voltages V_1 and V_2 , which are proportional to the frequencies to be locked. Varying the constants, K_1 and K_2 , multiplies or divides the frequencies.

Quad NAND gate package yields two-frequency clock

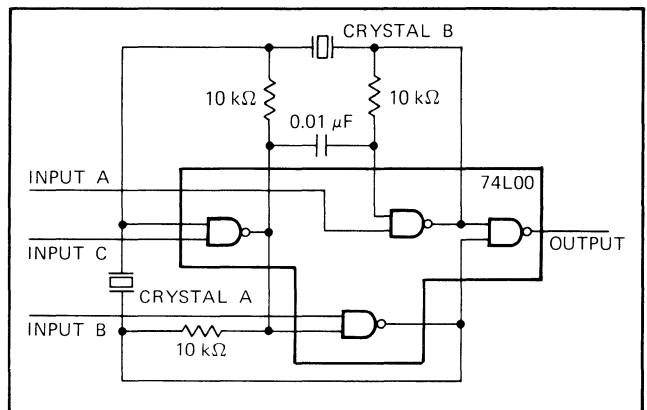
by Howard L. Nurse
Applied Technology Division, Ittek Corp., Palo Alto, Calif.

Crystal-controlled clock oscillators generally require three logic gates to produce a single output frequency. This means that the fourth gate in the common quad-type gate package is not used. But, with just a couple of extra parts, that fourth gate can be put to work.

The two-frequency crystal clock in the diagram takes maximum advantage of a quad TTL NAND gate package with a minimum of external components. And this economical circuit can be remotely programmed by grounding one of its three input lines.

With input A grounded, the circuit oscillates at the frequency of crystal A. With input B grounded, it oscillates at the frequency of crystal B. If input C is grounded, the circuit is inhibited.

The TTL-compatible output of this two-channel clock is a 40% square wave when either input A or input B is grounded. With the low-power TTL NAND-gate package



Two for the price of one. Dual-frequency crystal-clock oscillator utilizes all four gates in a quad package, whereas conventional single-frequency oscillators make use of only three. This inexpensive circuit can be remotely programmed by grounding input A to operate at the frequency of crystal A or by grounding input B to oscillate at crystal B's frequency. Grounding input C inhibits the circuit.

used here, operating frequencies in excess of several megahertz can be achieved. □

Capacitor corrects drift for analog data amplifier

by Charles Walton*
 IBM Corp., Systems Development Division, San Jose, Calif.

Inserting a capacitor in the gain control feedback path of an analog data amplifier can provide automatic offset voltage drift correction. The drift voltage is stored on the capacitor and held to ± 0.1 microvolt/ $^{\circ}\text{C}$.

The gain of the amplifier circuit (a), which is intended to operate in conjunction with a multiplexer, is selectable. Junction field-effect transistors are used to imple-

*Now with Proximity Devices Inc., Sunnyvale, Calif.

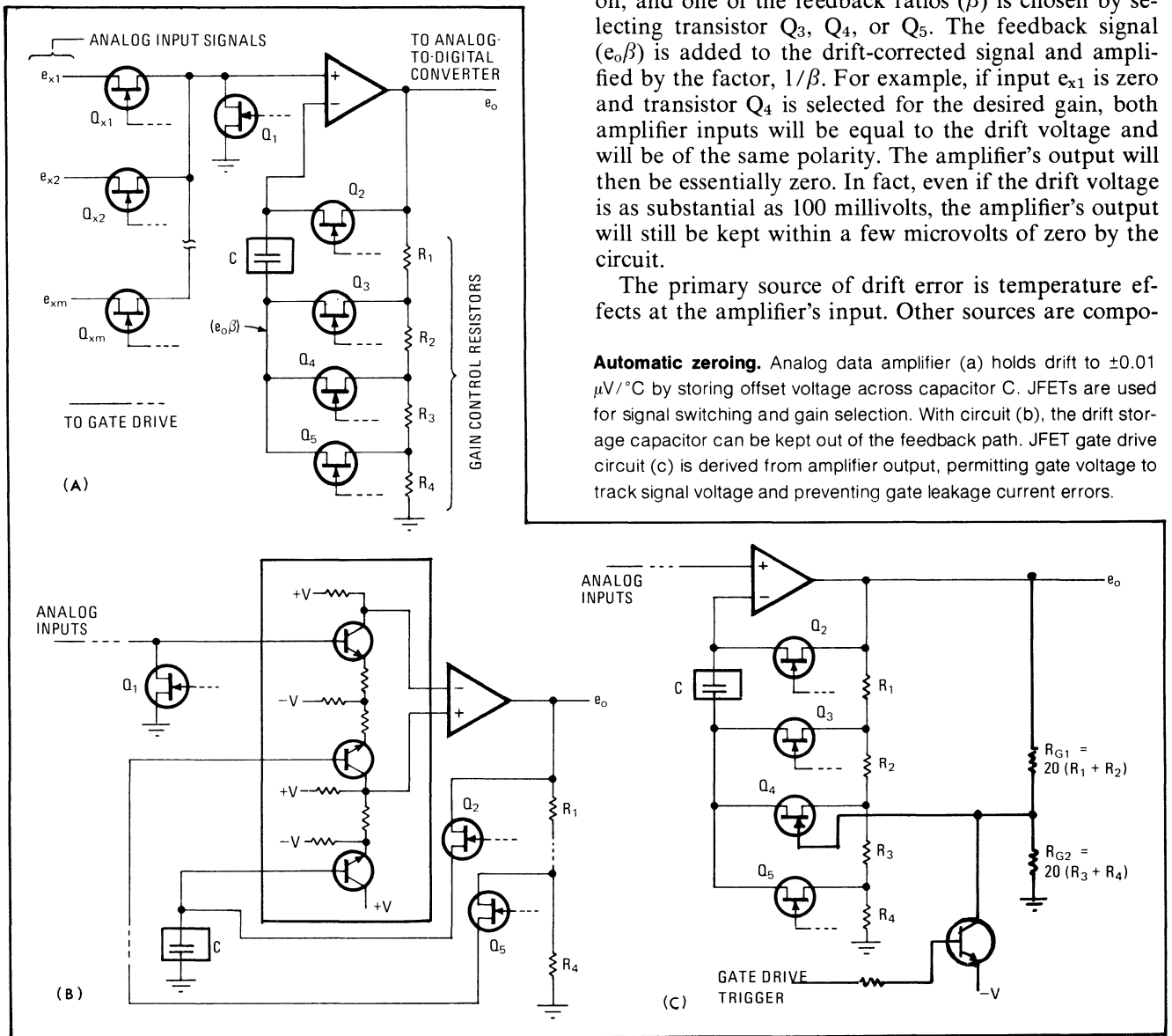
ment the gain control. Their gate voltage is provided by a resistor network that allows the gate voltage to track the signal voltage so that errors due to gate leakage current are eliminated.

Between multiplexing cycles, transistor Q_1 conducts, grounding the amplifier input, and transistor Q_2 also conducts, making amplifier gain equal to unity. As a result, the amplifier's dc offset voltage occurs at its output, as well as at its positive input and at the top of storage capacitor C . The other side of the capacitor may be grounded. Or, if resistor R_4 is relatively small compared to the sum of the other feedback resistors, R_1 through R_3 , as is usually the case, then turning on transistor Q_5 effectively grounds capacitor C . The capacitor behaves as a battery during the ensuing amplifier cycle. Its value is not critical, but should be reasonably large.

To amplify input signal e_{x1} , transistor Q_{x1} is turned on, and one of the feedback ratios (β) is chosen by selecting transistor Q_3 , Q_4 , or Q_5 . The feedback signal ($e_o\beta$) is added to the drift-corrected signal and amplified by the factor, $1/\beta$. For example, if input e_{x1} is zero and transistor Q_4 is selected for the desired gain, both amplifier inputs will be equal to the drift voltage and will be of the same polarity. The amplifier's output will then be essentially zero. In fact, even if the drift voltage is as substantial as 100 millivolts, the amplifier's output will still be kept within a few microvolts of zero by the circuit.

The primary source of drift error is temperature effects at the amplifier's input. Other sources are compo-

Automatic zeroing. Analog data amplifier (a) holds drift to $\pm 0.01 \mu\text{V}/^{\circ}\text{C}$ by storing offset voltage across capacitor C . JFETs are used for signal switching and gain selection. With circuit (b), the drift storage capacitor can be kept out of the feedback path. JFET gate drive circuit (c) is derived from amplifier output, permitting gate voltage to track signal voltage and preventing gate leakage current errors.



ment aging, power supply variations, and the offset of subsequent amplifier stages. But all these effects are slow compared to the amplification cycle time (200 microseconds, in this case). Therefore, the data system simply needs to adjust the stored capacitor voltage between amplification cycles or between a group of amplification cycles.

Placing bipolar transistors at the amplifier's input, as shown in (b), permits the correction capacitor to be kept out of the feedback path. (In most applications, this is only a minor advantage.) When transistors Q_1 and Q_2 are on, the amplifier places a voltage on capacitor C so that the next amplification cycle is automatically corrected for drift.

JFETs are used here for gain control, multiplexing, and zeroing, rather than MOSFETs, because they have more predictable control characteristics, need smaller switching voltages, and cost less. Possible errors due to JFET gate leakage currents can be avoided by utilizing the gate drive circuit of (c).

When a JFET is conducting, its gate voltage need only be within about 0.3 volt of its drain and source voltages. If the gate voltage is slightly less than this, there is a

small increase (for an n-channel JFET) in the drain-source resistance. If the gate voltage is slightly higher, the silicon-diode characteristic of the gate-source junction prevents any error-sized current from flowing.

The gate drive circuit shown meets these JFET gate voltage requirements by employing the amplifier output to drive the gates, thereby allowing the gate voltage to track the input signal. In the figure, the gate voltage for transistor Q_4 is obtained from the voltage divider formed by resistors R_{G1} and R_{G2} . These resistors do not have to have tolerances as tight as those of the feedback resistors ($\pm 5\%$, as against $\pm 0.02\%$).

The high impedance of the gate drive resistors avoids loading the amplifier output. There is a pair of divider resistors for each value of gain. To turn off a gain control transistor, a bipolar transistor is turned on, holding that JFET's gate voltage sufficiently negative to keep it off for all signals. Junction gate leakage current is typically below 100 nanoamperes, minimizing the possibility of errors.

General-purpose JFETs can be used for the amplifier circuit—ones having a source-drain resistance of 50 to 200 ohms. □

High-speed voltage-follower has only 1-nanosecond delay

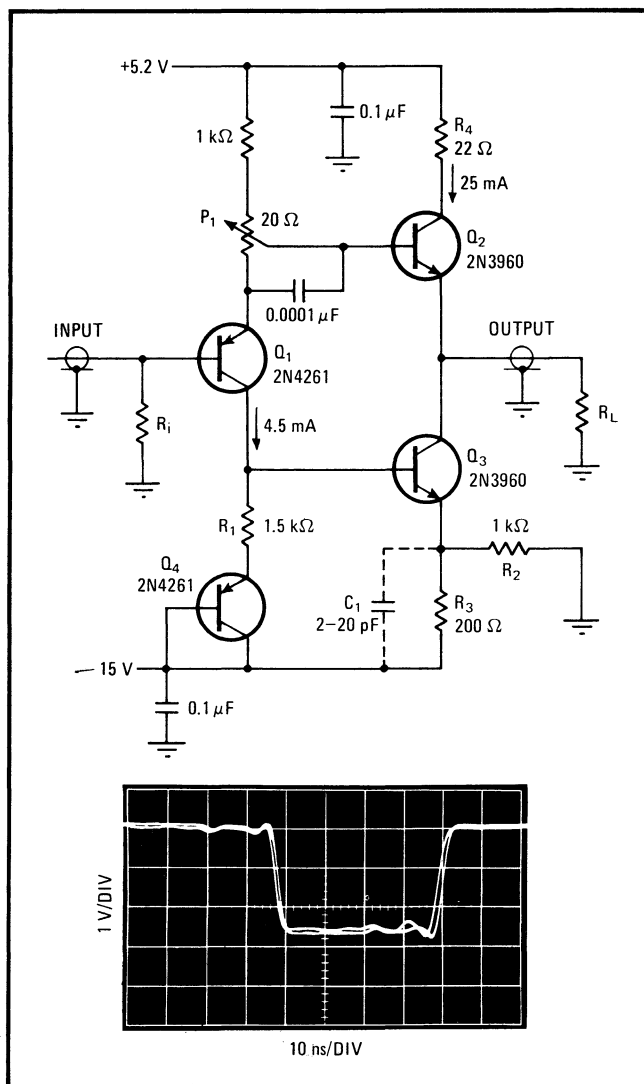
by O.A. Horna
COMSAT Laboratories, Clarksburg, Md.

When a voltage-follower is needed for isolation and/or impedance transformation in fast analog circuits, a simple emitter-follower can be made to give better performance than an integrated operational amplifier. A dual complementary emitter-follower overcomes the disadvantages of the conventional emitter-follower—its input-to-output offset voltage and its relatively low voltage gain. Propagation delay for this complementary circuit is less than 1 nanosecond.

The first emitter-follower, pnp transistor Q_1 , drives a second emitter-follower, npn transistor Q_2 , so that the offset (emitter-base) voltages of these transistors are opposite in polarity. The dc voltage difference between input and output terminals is therefore very small and can be adjusted to almost zero with potentiometer P_1 . Transistors Q_1 and Q_2 should make good thermal contact with each other to compensate for the temperature dependence of their emitter-base voltages.

Output transistor Q_2 is loaded by a variable current source, npn transistor Q_3 , the base of which is connected to the collector of transistor Q_1 . For a given bias current

Fast emitter-follower. Back-to-back emitter-followers, transistors Q_1 and Q_2 , are complements, causing their opposite-polarity offset voltages practically to cancel. (Potentiometer P_1 permits fine offset zero adjustment.) Transistor Q_3 is a variable-load current source, while transistor Q_4 is wired as a diode for Q_3 's temperature compensating. Scope display shows superimposed input and output signals.



(25 milliamperes here), transistor Q_2 can then deliver nearly twice as much current to the load as would be possible with a constant-current source. The last transistor, Q_4 , is connected as a diode to temperature-compensate transistor Q_3 's emitter-base voltage.

When the input voltage goes positive, the emitters of transistors Q_1 and Q_2 also become positive. The current through transistor Q_1 decreases, dropping the voltage across resistor R_1 as well as the current through transistor Q_3 . The opposite action occurs for a negative input.

The voltage gain of transistors Q_1 and Q_3 can be made greater than unity (between 1.1 and 1.2) by adjusting the resistance ratio of resistor R_2 to resistor R_3 . This compensates for the voltage gain of transistors Q_1 and Q_2 , which is less than unity (between 0.9 and 0.95). With an unloaded output, the circuit's total stable voltage gain ranges from 0.985 to 0.995, and the output resistance is less than 1 ohm. (The output is protected against short circuits by resistor R_4 .)

The scope trace shows the circuit's input and output voltages superimposed on each other. With a load resistor of 50 ohms and an output voltage of ± 2.5 volts,

the circuit's propagation delay is less than 1 nanosecond, and the rise and fall times are smaller than 2 ns without overshoot. The maximum voltage swing is ± 4 v, the bandwidth is approximately 200 megahertz, and the slew rate is over 2 kilovolts per microsecond.

When the load resistance is less than 200 ohms, the circuit's transient response and the bandwidth can be substantially improved by adding a speed-up capacitor, C_1 . However, under a no-load condition, when the load resistance is 500 ohms or more, this capacitor can cause the circuit to oscillate.

All four discrete transistors can be replaced by a single quad package, Motorola's MHQ6001, which contains two pairs of pnp and npn transistors. Since these transistors have a gain-bandwidth product of only 400 MHz, as opposed to 1 gigahertz for the discretes, the circuit's propagation delay and rise and fall times will be three to four times longer.

For the bias currents given in the figure, the dc source resistance, R_i , must be less than 2 kilohms. The circuit's input resistance is greater than 50 kilohms for load resistances of 50 ohms or more. □

Mark/space demodulator employs active filters

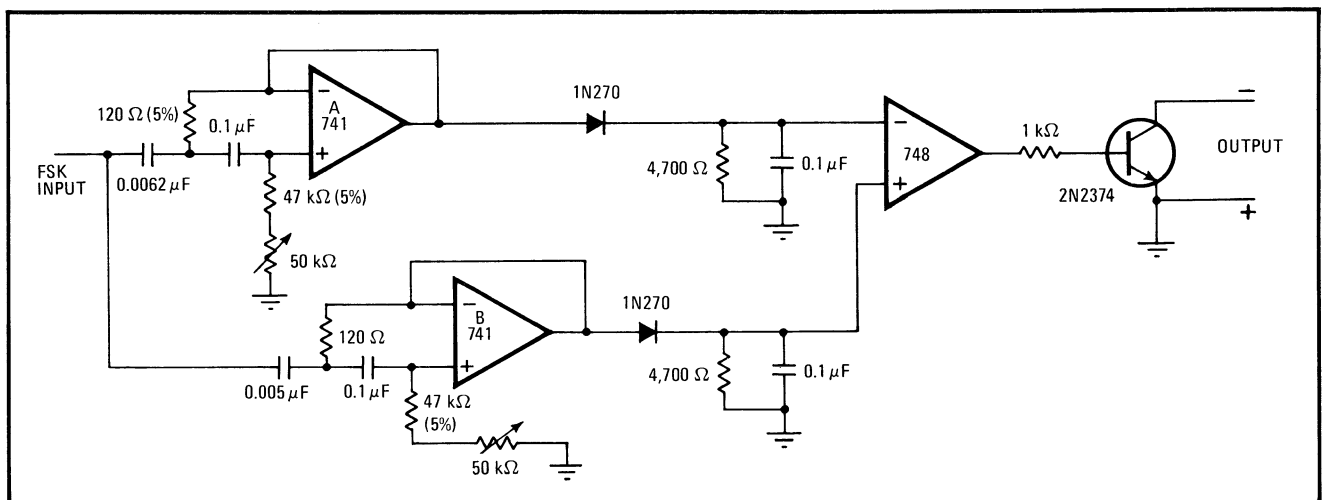
by Michael J. Gordon, Jr.
Psynexus Systems, Wilmette, Ill.

If active filters are used instead of LC-tuned circuits, a frequency-shift-keyed demodulator can be made smaller in size and its performance improved. The active filters eliminate the need for bulky and expensive inductors. The circuit is designed for demodulating 110-baud FSK data. It operates in the originate mode, where a mark equals 2,225 hertz and a space is 2,025 Hz.

When a mark is received, filter B, which is tuned to

2,225 Hz, passes the signal while filter A attenuates it. The outputs of the two filters are then converted to dc and compared by an op amp that is operated in its open-loop mode. Since the output of filter B is sampled by the op amp's noninverting input, the circuit's output transistor is kept in saturation so that the circuit loop is closed. When the input frequency shifts to a space, filter A passes the signal while filter B attenuates it, causing the circuit loop to remain open.

To adjust the circuit, an audio signal is applied at the mark and space frequencies, and the desired peak output produced by varying the two 50-kilohm trimmers. An approximate peak-to-peak voltage of 1.2 volts is required from a low-impedance source. □



Going active. Frequency-shift-keyed demodulator contains two active filters, saving space and improving performance over designs that use conventional LC-tuned circuits. Filter A passes the space frequency of 2,025 hertz, while filter B passes the mark frequency of 2,225 Hz. The op amp operates open loop, summing the filter outputs. For a mark input, the output transistor saturates so that circuit loop closes.

Sampling regulator controls motor speed

by Philip Dempster
Este Instruments, Inc., Richmond, Calif.

A permanent-magnet dc motor can serve as its own tachometer for speed control, allowing considerable cost savings to be realized over an expensive motor-tachometer unit. Sampling is employed in the motor-speed regulator shown to eliminate the errors and uncertainties introduced by the motor's armature and brush resistances. Motor speed can vary over a 20:1 range.

During positive half cycles of the input, the transformer's secondary voltage drives transistor Q_1 through diode D_1 . During negative half cycles of the input, this drive power is removed, and the motor's back emf is compared to reference voltage V_R . Any resulting error

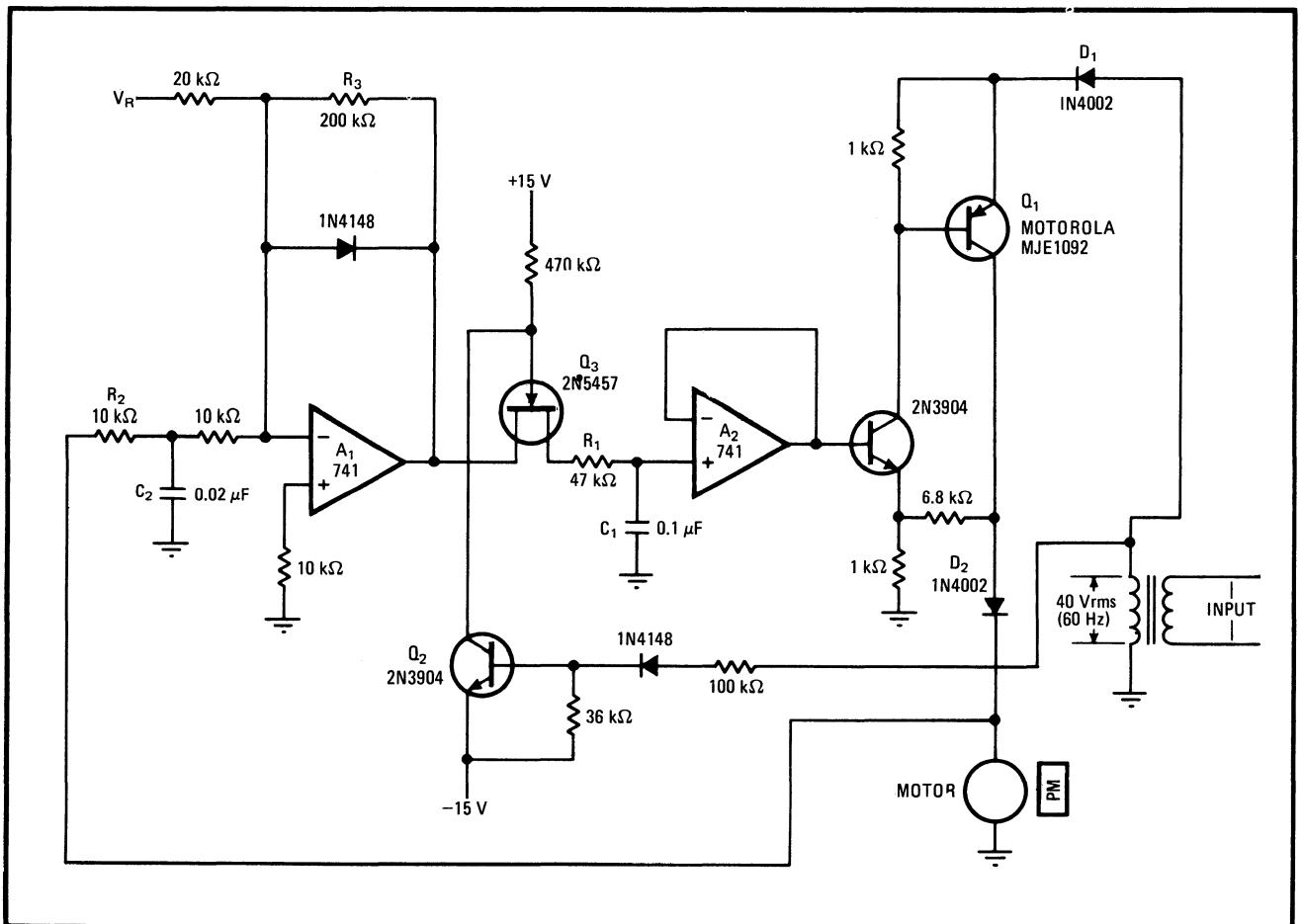
signal is applied to the inverting input of amplifier A_1 .

For a portion of each negative half cycle, transistor Q_2 is switched off by the transformer's secondary voltage, causing field-effect transistor Q_3 to conduct. The amplified error signal at the output of A_1 can then be transferred to capacitor C_1 , where it is stored until the following sampling period. During the next positive half cycle of the input, this stored error signal is amplified again (by amplifier A_2) and then applied to the motor to correct any speed error that may exist.

Diode D_2 decouples the motor from the drive circuitry during each sampling period to prevent errors from being introduced in the sampled voltage. Two RC filters—one formed by resistor R_1 and capacitor C_1 , and the other by resistor R_2 and capacitor C_2 —are intended to reduce brush transients. The R_1C_1 filter has the longer time constant of the two and is located after FET Q_3 to avoid degrading the recovery time of amplifier A .

Resistor R_3 controls the gain in the feedback loop. Its value should be chosen to provide the highest possible gain while preserving good loop stability. □

Motor-speed control. Sampling regulator circuit permits motor speed to be varied over 20:1 range. For portion of negative half cycle of the input, the motor's drive power is removed so that the motor's back emf can be compared to reference voltage V_R . Any resulting error is stored across capacitor C_1 until the next positive half cycle of the input. The error voltage is then applied to the motor for speed correction.



Digital transient suppressor eliminates logic errors

by Christopher Strangio
Villanova University, Villanova, Pa.

In digital systems, switching transients occur most often when there is a transition from logic 0 to logic 1 or from logic 1 to logic 0. These transients can introduce errors if their amplitude is large enough to exceed the logic 0 maximum voltage or the logic 1 minimum voltage. Errors are particularly likely to occur at mechanical-to-electrical couplings, as in switches and relays.

The simple digital circuit in the diagram can eliminate these unwanted transients. Initially, the input is low, and the latch and the two monostable multivibrators, MM₁ and MM₂, are reset. On the first positive-going edge at the input, gate G₁ is enabled, triggering MM₁ and making its Q output go high. This sets the latch so that gate G₁ becomes inhibited and the output goes high. Since gate G₂ is also inhibited after MM₁ is triggered, the input is now blocked both from the latch and from the two monostables. After the first positive-going edge, then, any positive-going transients at the input will have no effect on the output.

The period of monostable MM₁ determines how long positive input transients are prevented from affecting

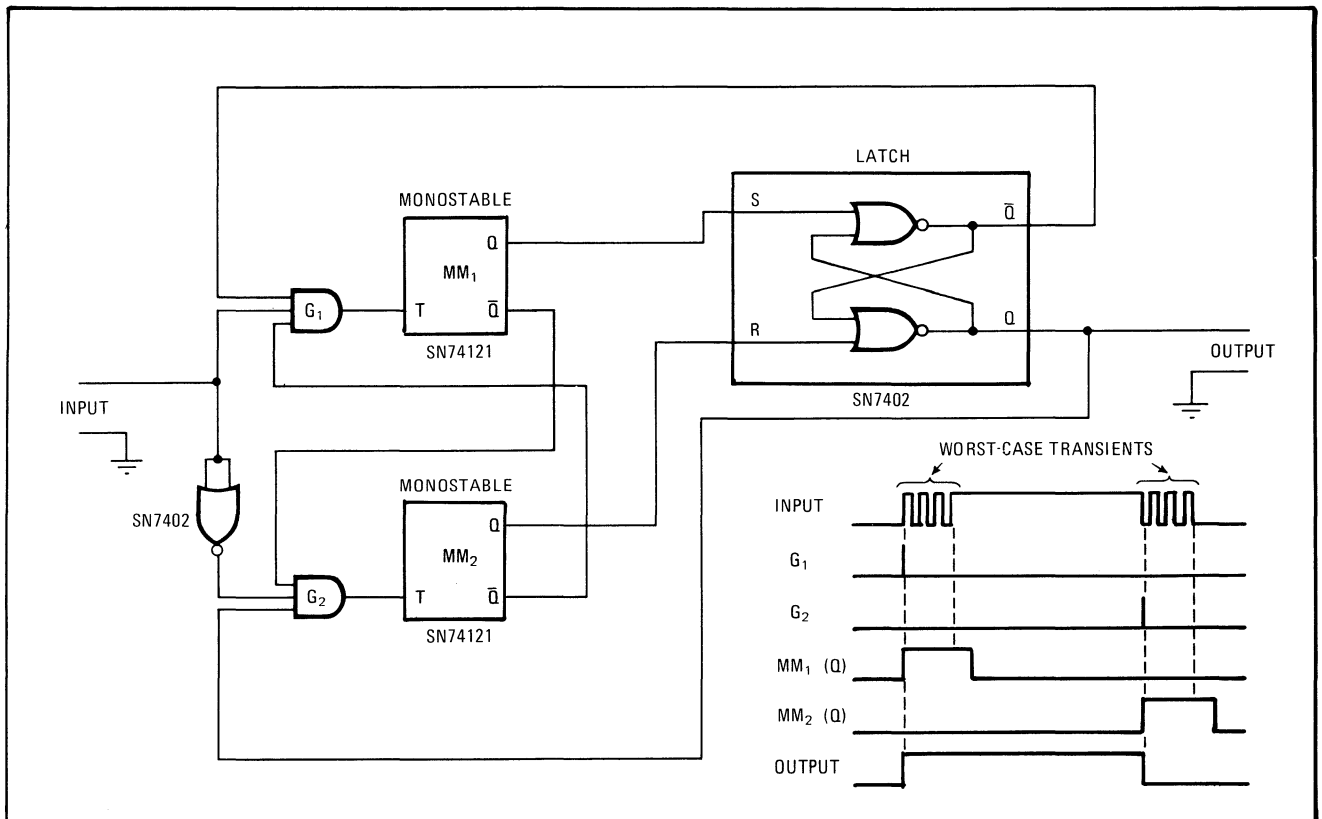
the state of the output. This period should be adjusted to be slightly greater than the longest possible turn-on transient. When the Q output of MM₁ goes low at the end of the timing period, the next negative-going input transition enables gate G₂, triggering monostable MM₂ and resetting the latch so that the output goes low.

As long as the input remains high, the latch stays set and the output will continue to be high. The first negative-going edge at the input enables gate G₂, causing the Q output of monostable MM₂ to go high. This resets the latch so that gate G₂ becomes inhibited and the output goes low. Since gate G₁ also becomes inhibited once MM₂ triggers, the input is again blocked. All negative-going transients will now be prevented from changing the output logic state.

The period of monostable MM₂ establishes the length of time negative transients at the input are stopped from reaching the output. The monostable timing period should be slightly greater than the longest possible turn-off transient. The output will remain low after the timing cycle of MM₂ is complete, provided that the input remains low.

With the components shown, this digital transient suppressor will be triggered by transients as short as 85 nanoseconds. The circuit can be adjusted to block transients that are between 100 ns and 2 seconds wide, occurring after the initial leading or trailing edge at the input. Voltage excursions below 0 volts are handled by the clamping diodes found in most TTL packages; excursions above 5.5 v may be clipped with a zener. □

Transient suppressor. Both positive-going and negative-going logic transients are prevented from causing output errors by this digital suppressor circuit. Timing period of monostable MM₁ fixes the maximum width of positive transients that will be blocked, while the period of monostable MM₂ determines the maximum width of negative transients. The timing diagram shows waveforms for several key circuit points.



Counter and decoder/driver produces staircase voltage

by Donald F. Dekold
 Santa Fe Community College, Gainesville, Fla.

Generating staircase voltage waveforms is easy if some of the newer TTL MSI devices are used. Only two IC packages are needed—a decade counter and a 1-of-10 decoder/driver. Up to 10 distinct staircase voltage steps can be generated, and the steps can be made quite large, up to 65 volts dc, before exceeding the output breakdown limitations of the decoder/driver. The circuit is useful as a building block in a curve tracer or a low-resolution analog-to-digital converter, and in control applications requiring the sequential stepping of voltages.

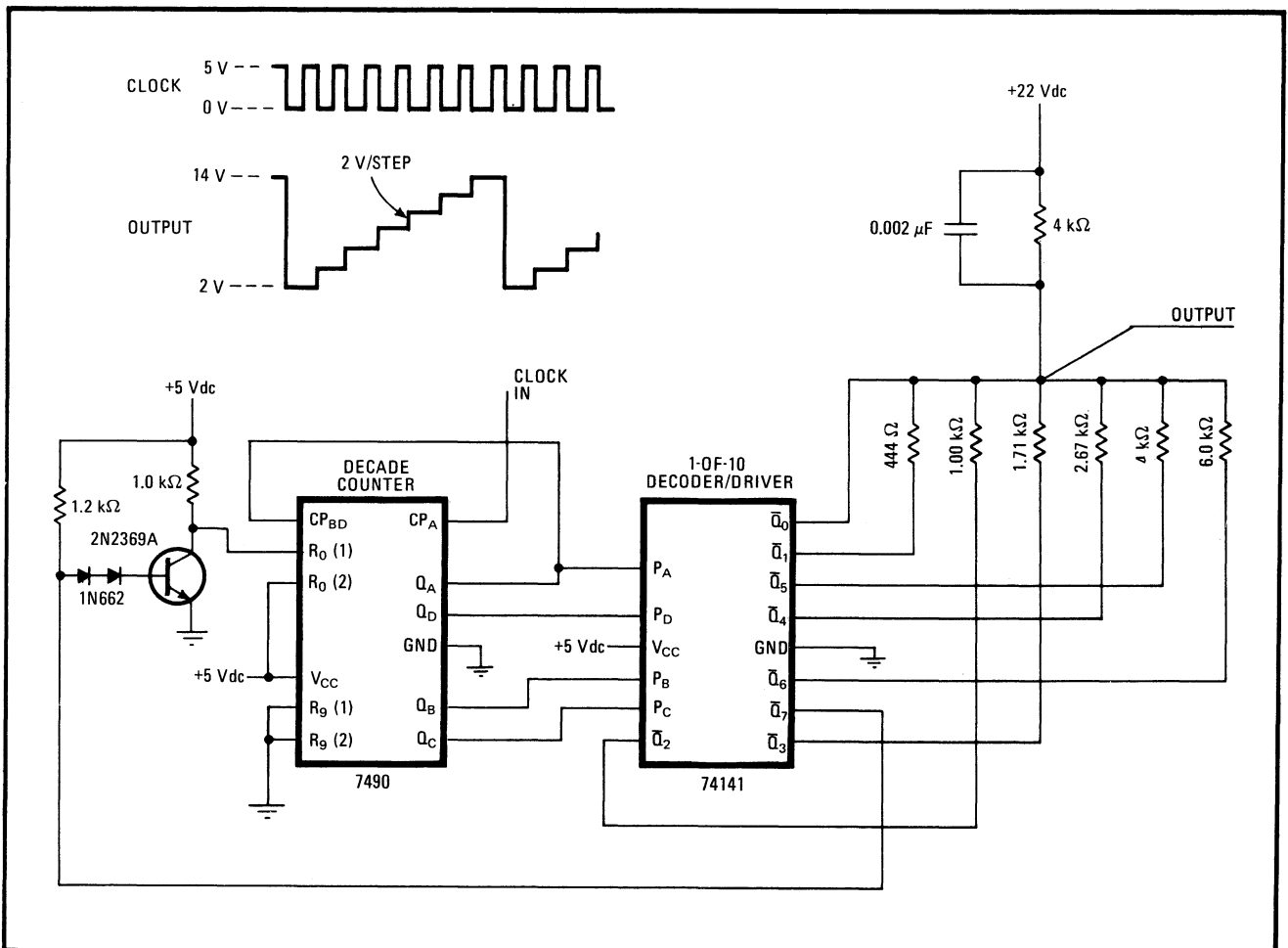
Resistive voltage division is employed (only one output of 10 is on at a time), rather than op-amp summing techniques. This allows the steps to be generated at a rather faster rate than would be possible with an op amp, which is hampered by its slew-rate limitations.

The step levels need not advance with equal increments (or decrements), but can be programmed by selecting the proper resistors in the voltage divider network. However, loading effects must be considered when designing for the output levels wanted.

The circuit in the diagram generates a seven-level staircase output, increasing from 2 to 14 v dc in 2-V increments. The eighth negative clock transition produces a logic low at the corresponding decoder/driver output, \bar{Q}_7 , which resets the counter to zero via the transistor stage. (Without this reset transistor, the counter would automatically reset to zero at the end of the 10th clock cycle.) On the first count, the generator's output is taken from the decoder/driver's \bar{Q}_0 output and is 2 v dc, a typical value for the decoder/driver when it is sinking a 5-milliampere current.

The generator may accept clock frequencies as high as 10 kilohertz, but the transition-time transients that will occur between each output step make the capacitor shown necessary. Although the capacitor provides smoother step transitions, it limits the maximum operating frequency. □

Two-package stepper. Staircase output generated by decade counter and 1-of-10 decoder/driver can have up to 10 voltage steps, each step being as large as 65 volts. The resistor voltage divider network scales the outputs of the decoder/driver to the desired step sizes. Clock frequencies can be as fast as 10 kilohertz. The capacitor smooths the output transients that may occur at the clock transitions.



Binary input determines pulse-generator frequency

by Mahendra J. Shah
University of Wisconsin, Madison, Wis.

A digitally programmable pulse generator for computer-controlled test systems and real-time control systems can be put together quite economically. The generator's output frequency is linearly related to the input binary number, and its output-pulse width can be varied over a 20:1 range by manually adjusting a potentiometer.

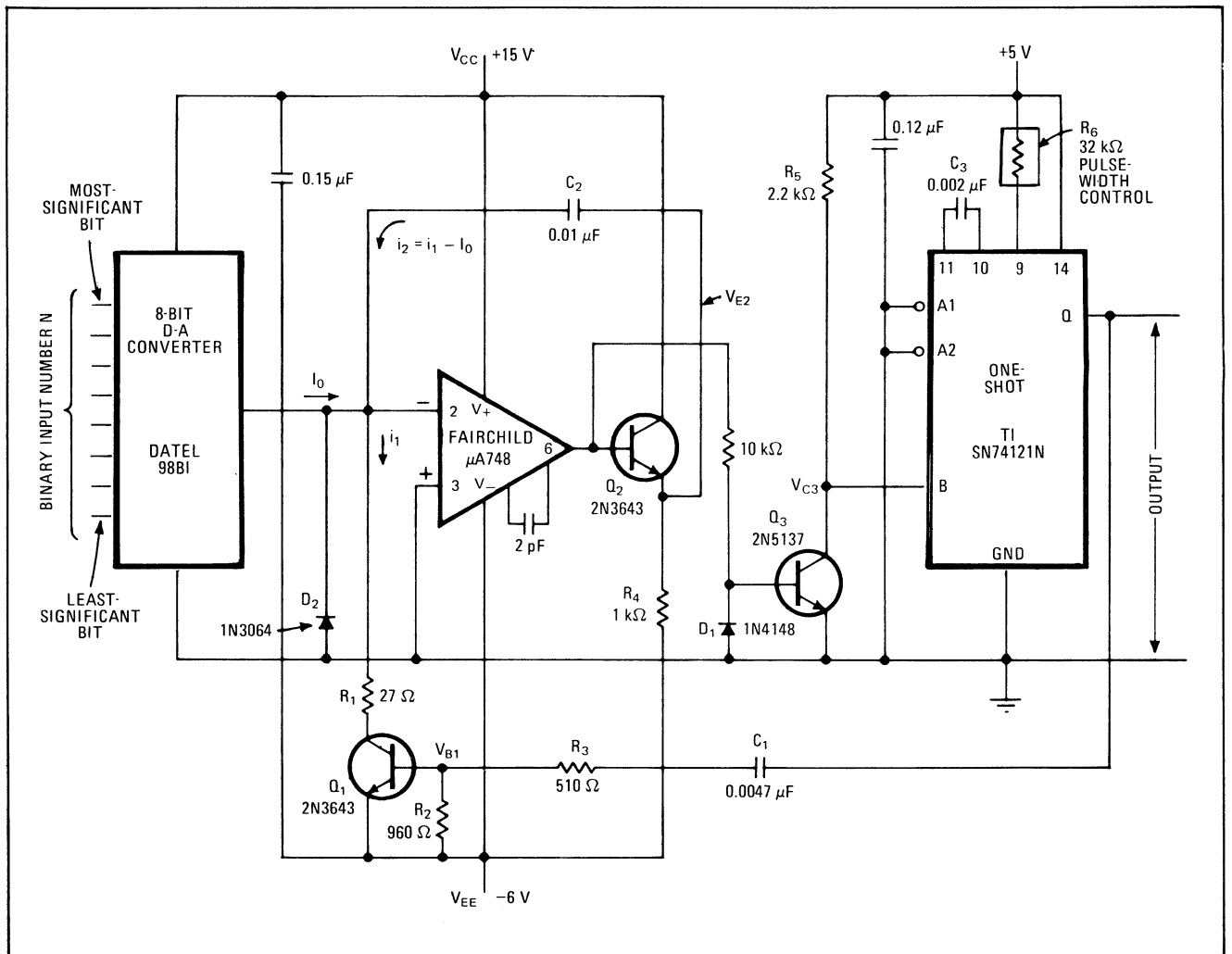
The circuit consists of: a low-cost 8-bit digital-to-analog converter having a current output; an integrated one-shot and its reset circuitry (transistor Q_1 , resistors

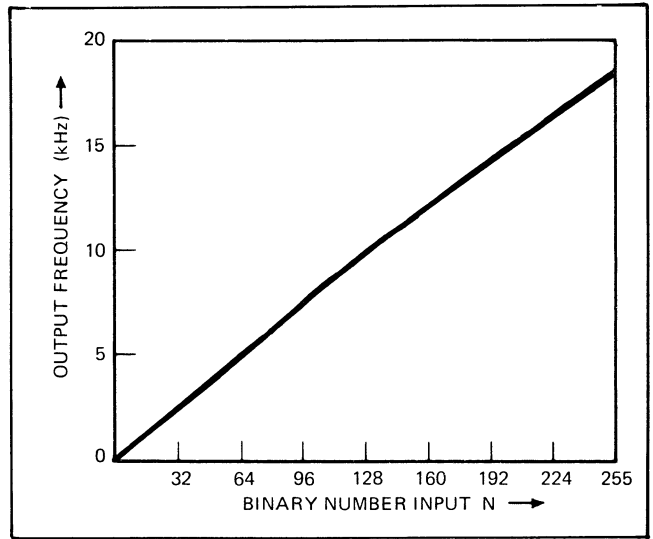
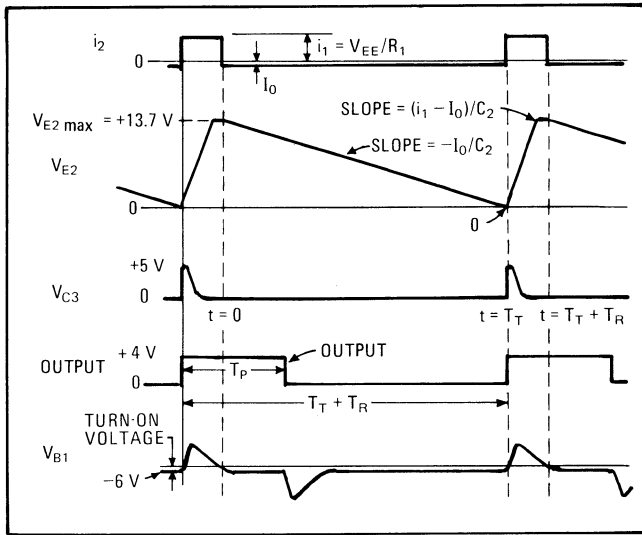
R_1 , R_2 , and R_3 , and capacitor C_1); an op-amp integrator (including emitter-follower Q_2 , resistor R_4 , and capacitor C_2); and a zero-crossing comparator (transistor Q_3 , diode D_1 , and resistor R_5).

With transistor Q_1 off and transistor Q_2 on, the output current from the converter linearly discharges capacitor C_2 to almost zero, turning transistor Q_3 off. This causes Q_3 's collector voltage to rise toward the 5-volt supply level, firing the one-shot and causing its Q output to go high. Reset components R_2 , R_3 , and C_1 differentiate this output transition, producing a positive pulse at the base terminal of transistor Q_1 and turning this device on.

For the interval (recovery time T_R) that transistor Q_1 remains on, capacitor C_2 charges to its maximum voltage. Transistor Q_1 then turns off, permitting the cycle to repeat. Meanwhile, the one-shot completes its timing cycle and generates a pulse of width T_P .

Digitally variable. Pulse generator offers adjustable output frequency and output pulse width; pulse frequency μ changes linearly with the binary input. When transistor Q_1 is off and transistor Q_2 on, converter output current discharges integrator capacitor C_2 until transistor Q_3 turns off. This triggers the one-shot, producing an output pulse and turning on transistor Q_1 so that capacitor C_2 can charge up.





The length of reset interval T_R depends on the threshold voltage of transistor Q_1 , the desired output-signal amplitude, and the time delay provided by resistors R_1 , R_2 , and R_3 , and capacitors C_1 and C_2 . The total output period is given by:

$$T_T = C_2 V_{E2max} / I_0$$

where:

$$I_0 = k N V_{CC}$$

where k is a constant (0.68 micromho), and N is the input binary number. The output-pulse frequency can be written as:

$$f = 1 / (T_T + T_R)$$

When the recovery time is much smaller than the total period, as is the case here, the output frequency for the

pulse generator can be approximated by:

$$f = k N / C_2$$

which is linear with respect to input number N , as indicated by the plot. Output-pulse width is variable and is given by:

$$T_P = 0.69 R_6 C_3$$

The largest value of T_P is limited by the one-shot's recovery time, as well as by the fact that T_P should be greater than the recovery time but smaller than the total period.

Diode D_1 prevents the base-emitter voltage of transistor Q_3 from exceeding its reverse breakdown rating. Diode D_2 protects the d-a converter from possible damage from a large negative voltage at its output. □

Automatic gain control operates over two decades

by Carl Marco
Martin Marietta Corp., Orlando, Fla.

A voltage-controlled junction-field-effect transistor permits an automatic-gain-control circuit to maintain a constant output voltage over a two-decade input-voltage range. The resulting agc circuit is intended for use in a radar seeker device to prevent amplifier overload as the target gets closer. Inputs can range from 40 millivolts to 4.1 volts peak-to-peak, but the output remains a nominal 0.2 V pk-pk.

As shown in the diagram, the JFET is located in the gain-control loop of noninverting amplifier A_1 . The gain of this amplifier can be represented by:

$$A_V = 1 + R_F / R_I$$

where R_I is the series combination of the 1-kilohm resistor plus the FET's drain-source (channel) resistance:

$$r_{ds} \approx r_{ds(on)} / (1 - V_{GS} / V_{GS(off)})$$

For the FET used here, $r_{ds(on)}$ is 25 ohms maximum and

$V_{GS(off)}$ is -10 v maximum. The channel resistance, therefore, stays linear for about half the range of $V_{GS(off)}$, but tends to become nonlinear at voltages above $1/2 V_{GS(off)}$ because of the FET's departure from square-law behavior at high gate-source voltages. Amplifier gain can then be rewritten as:

$$A_V = 1 + (110 \text{ k}\Omega) / [(1 \text{ k}\Omega) + (0.025 \text{ k}\Omega) / (1 - |V_{GS}| / 10)]$$

$$A_V = 1 + 110 / [1 + 0.025 / (1 - |V_{GS}| / 10)]$$

The voltage divider formed by resistors R_1 and R_2 attenuates (by around 20:1) input signal amplitude to prevent distortion at the output. Since the inverting input of amplifier A_1 tries to track its noninverting input, the positive input is the one that determines the FET's drain-source voltage. This channel voltage must be kept small to force the FET to remain in its triode region of operation. A shift in the FET's operating region would introduce large amounts of distortion.

Amplifier A_2 is connected as a half-wave rectifier. When A_1 's output swings positive, diode D_1 conducts, shunting A_2 's feedback resistor (R_3) and bringing the junction of this resistor and diode D_2 to zero. When A_1 's output goes negative, diode D_2 conducts so that amplifier A_2 has a gain of -1 and a positive output.

Resistors R_4 , R_5 , and R_6 provide full-wave rectifica-

tion for A_1 's output signal. Since the resulting rectified signal is supplied from a high-impedance source (and not buffered as is usually done), it is a current drive signal that can feed amplifier A_3 directly. When the circuit is balanced, the current through resistor R_7 is equal in magnitude but opposite in polarity to the full-wave rectified current.

The voltage divider, composed of zener diode D_3 and precision resistors R_8 , R_9 , and R_{10} , determines the signal level applied to amplifier A_3 . This amplifier performs as a comparator/integrator, supplying the very large dc gain needed for the circuit's closed-loop feedback. Capacitor C_1 prevents A_1 's output from oscillating, while resistor R_{11} allows filter capacitor C_2 to be added without creating a "virtual" ground at A_3 's input.

Capacitor C_2 prevents ac ripple from modulating the FET's gate voltage and producing distortion. Its value is chosen by trading off circuit-response time against the amount of filtering. Only a small change in A_3 's input current causes the circuit to adjust itself, producing whatever agc voltage is required to maintain an output of 0.2 v peak-to-peak.

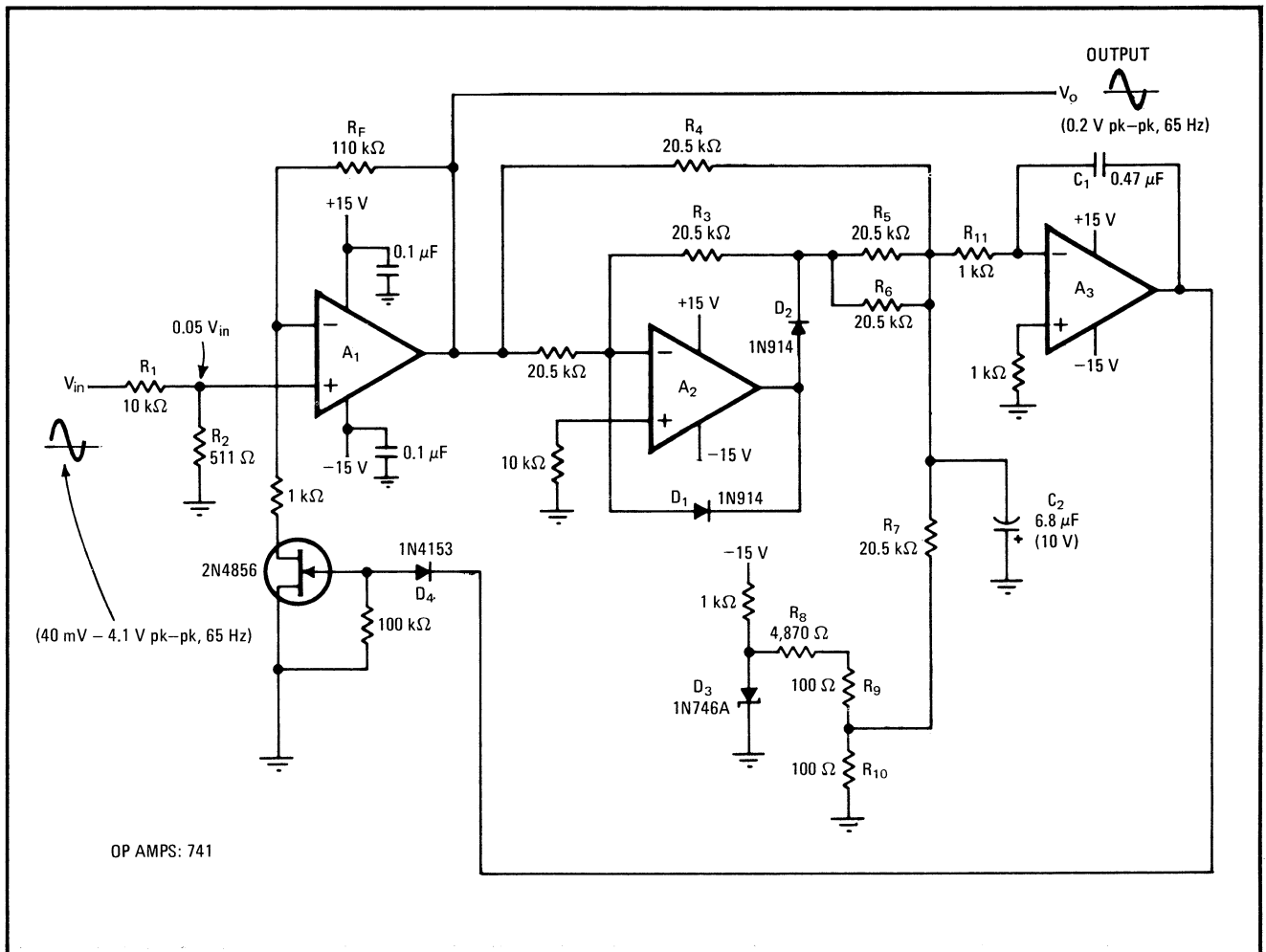
When input-signal amplitude increases, the drive current to amplifier A_3 also increases, causing A_3 's output

to go more negative. This raises the FET's channel resistance and decreases A_1 's gain, thereby maintaining the output level at 0.2 v pk-pk. An input voltage of 4.1 v pk-pk or higher cuts off the FET, making the voltage gain of A_1 equal to unity. Amplifier A_1 then tracks the input, attenuating it by a factor of 20. At an input level of 4.1 v, output distortion is only 1.1%.

For an input below 40 millivolts, the drive current to A_3 becomes negative so that A_3 provides a positive output, back-biasing diode D_4 and bringing the FET's gate-source voltage to zero. The gain of amplifier A_1 is then at its maximum value ($1 + 110/1.025 = 107$), permitting the circuit to track the low-level input and producing an output of $5.35 V_{in}$.

The circuit's output-voltage level can be increased to 0.4 v pk-pk, for an input voltage range of 80 mV to 8.2 v pk-pk, by changing the voltage division at the comparator input—resistor R_7 is connected between resistors R_8 and R_9 , rather than between resistors R_9 and R_{10} . However, this change increases output distortion to 4.4% at the 8.2-v input level. □

FET in the driver's seat. Automatic-gain-control circuit employs voltage-controlled JFET as the variable control element. The FET's channel resistance determines gain of amplifier A_1 , in response to error voltage produced by comparator A_3 . Amplifier A_2 and the surrounding diode/resistor network perform as full-wave rectifier. The output is maintained at 0.2 volt for inputs from 40 millivolts to 4.1 V.



Frequency discriminator uses one-shot and flip-flop

by Peter Alfke
Fairchild Semiconductor, Mountain View, Calif.

A frequency discriminator that is accurate to within about 3% can be built inexpensively with only two integrated-circuit packages. The circuit, which is intended for industrial-control and communications applications, senses whether an incoming frequency falls within a predetermined band, or if the frequency is lower or higher than the band.

A dual retriggerable monostable and a dual flip-flop are the two IC packages. The positive-going edge of the incoming signal clocks both flip-flops and triggers the first monostable, M₁. When this monostable, which has an "on" time of approximately 0.31R₁C₁, completes its timing cycle, it triggers the second monostable, M₂, which has an approximate "on" time of 0.31R₂C₂.

For a low incoming frequency, both monostables have completed their timing cycles before the next positive-going edge of the input occurs. The next edge, then, sets flip-flop FF₁ and resets flip-flop FF₂ (Q₁ and Q̄₂ outputs go high), indicating that the incoming frequency is below the design band:

$$f_L = 1/[0.31(R_1C_1 + R_2C_2)]$$

If the input frequency is increased, the next leading edge occurs while the output from monostable M₂ is still high, so that both FF₁ and FF₂ are set (Q₁ and Q₂ outputs go high). This indicates the incoming frequency is within the design band.

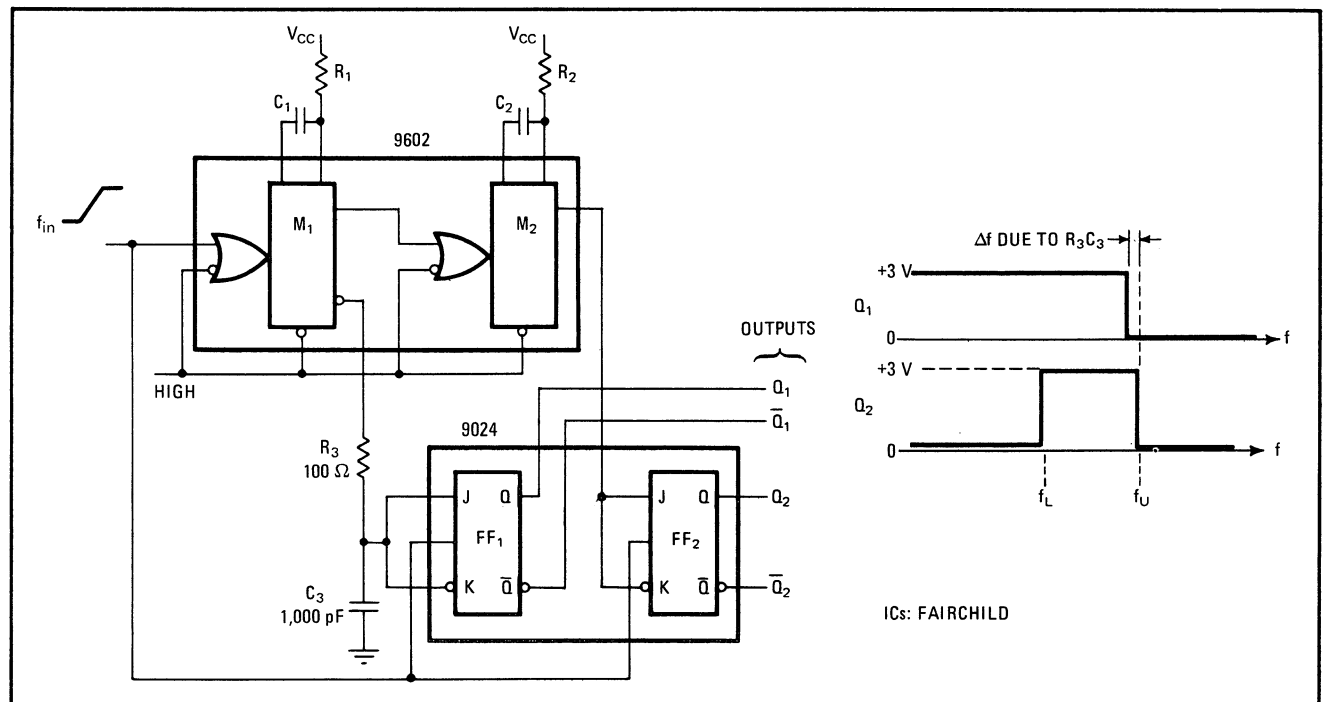
Increasing the input frequency further causes the next leading edge to occur before monostable M₁ has finished its timing cycle, beginning a new period for this retriggerable monostable. The continuing output from M₁ prevents monostable M₂ from triggering so that both flip-flops are reset (Q̄₁ and Q̄₂ outputs go high). This means that the incoming frequency is higher than the design band:

$$f_U = 1/0.31R_1C_1$$

The time constant (about 100 nanoseconds) established by resistor R₃ and capacitor C₃ makes the setup time of flip-flop FF₁ longer than the trigger delay of monostable M₂. This assures that FF₁ will change state at a frequency that is slightly below, rather than above, upper band limit f_U, thereby avoiding ambiguous output codes around f_U.

The circuit's frequency response is limited to a few megahertz because of the inherent delays of the monostables. Whenever the range of operating frequency permits, type 96L02 monostables should be used because they offer better temperature stability than the type 9602 devices. (The 74121 multivibrator cannot be used here because of its duty-cycle limitations.) □

Monitoring frequency. A couple of retriggerable monostables and flip-flops can be connected as a fairly accurate low-cost frequency discriminator. Lower and upper band limits are determined by the monostables' timing circuits. For in-band inputs, outputs Q₁ and Q₂ are high; for low frequencies, Q₁ and Q̄₂ are high; and for high frequencies, Q̄₁ and Q̄₂ are high. The R₃C₃ delay avoids ambiguity at the upper limit.



C-MOS counting circuit accumulates 2^{70} pulses

by Robert M. Owens and Kenneth J. Hintz
Naval Weapons Laboratory, Dahlgren, Va.

An easy-to-build counting circuit satisfies today's increasing need to monitor events or quantities over long periods of time. The circuit, which consists of only five ICs, can count to 2^{70} —that's greater than a sextillion (1×10^{21})! It can be used in any situation where a large number of events must be counted.

Primarily, however, the circuit is intended to provide the integral of temperature over a 30-day period by counting the total cycles of a linear temperature-dependent oscillator. It employs complementary-MOS ICs to reduce power consumption to approximately 4.5 milliwatts for a supply voltage of 9 volts. This allows the circuit to be left unattended in the field for periods of longer than 30 days.

At first, the 64-stage static shift register is reset so that its \bar{Q} and the Q output of flip-flop FF₁ are high. The DATA input of FF₁ is high until a sync ("add one") pulse is generated by the \bar{Q} output of flip-flop FF₂ and the divide-by-64 binary counter, at its Q₆ output.

As the sync pulse goes high, FF₁'s DATA input goes low. On the next clock pulse, then, FF₁'s Q output goes

low, inverting the next bit in the shift register. Since the shift register's \bar{Q} output is high, FF₁'s DATA input returns to its high state after the sync pulse occurs, and the rest of the bits in the shift register are recirculated unchanged. At its Q output, the shift register now contains the serial information, 100 . . . 000.

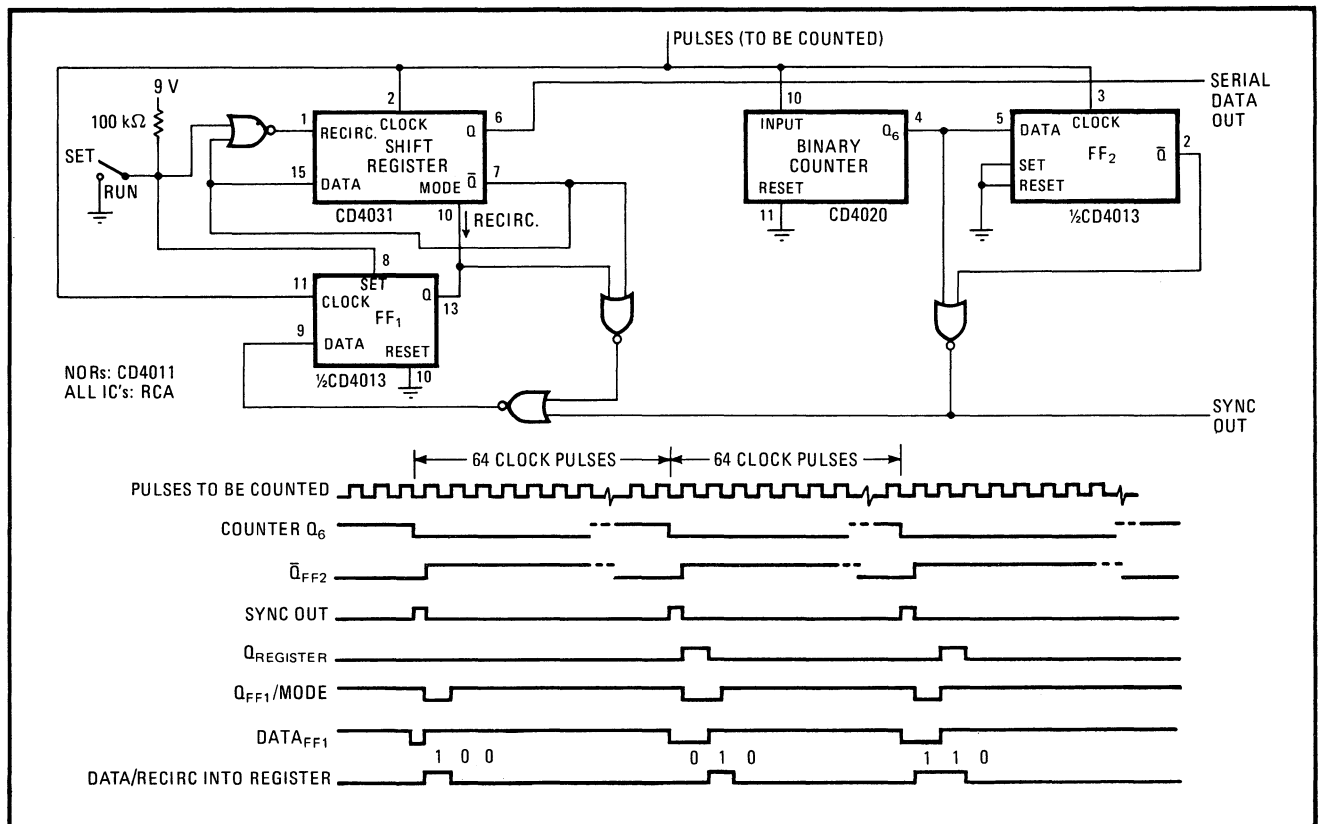
On the next sync pulse, the first register bit is again inverted, but since the register's Q output is low, as is FF₁'s Q output, then FF₁'s DATA input is held low, effectively implementing a "carry one." This "carry one" causes the second register bit to be inverted too. However, because the second bit goes from low to high (\bar{Q} output of the register goes high), FF₁'s DATA input goes high, causing FF₁'s Q output to go high so that the rest of the bits are recirculated unchanged.

The shift register now contains 010 . . . 000. The next sync pulse starts the inversion process again, incrementing the register by one, and resulting in an output of 110 . . . 000.

Essentially, the circuit provides a divide-by-n function, where n is the number of stages in the shift register. Since the register can store n bits of information, the circuit has an effective total count capability of $2^n + n$. The total count can be varied by adjusting the register length and by selecting the tap on the binary counter that provides one sync pulse for every register cycle.

For this circuit, the total count is 2^{70} —a count that would require 37.4 million years to achieve if the circuit is clocked at a rate of 1 megahertz. The circuit's resolution for this period would be ± 64 counts. □

A real old-timer. Low-power counting circuit can keep track of more than a sextillion input pulses—a count that would take over 37 million years to attain at a clock rate of 1 megahertz. The circuit, which is made up of five C-MOS ICs, actually counts to 2^{70} . It "slows" (for counting purposes) the incoming pulse train by combining a divide-by-64 binary counter with a 64-stage static shift register.



Simple logic arrangement identifies first event

by Stephen Phelps
 Santa Fe Community College, Gainesville, Fla.

An inexpensive, straightforward circuit is capable of detecting and indicating which of four switches closes first. This first-response discriminator, which costs less than \$5 to build, can be operated from a 6-volt lantern battery. Since it is made up of TTL integrated circuits, it can resolve "ties" with nanosecond accuracy.

The circuit is useful in behavioral-science applications to determine the first response of any one of four subjects, or in scientific studies where it is important to pinpoint what event is occurring first. Another application, one of more popular interest, is eliminating ambiguity in various entertainment games by identifying which player reacts first or quickest.

Each of the circuit's four input switches, S_1 through S_4 , is initially open, keeping NAND gates G_1 through G_4 inhibited. Flip-flops FF_1 through FF_4 are initially reset by applying a logic 0 to each \overline{RD} input via switch S_5 .

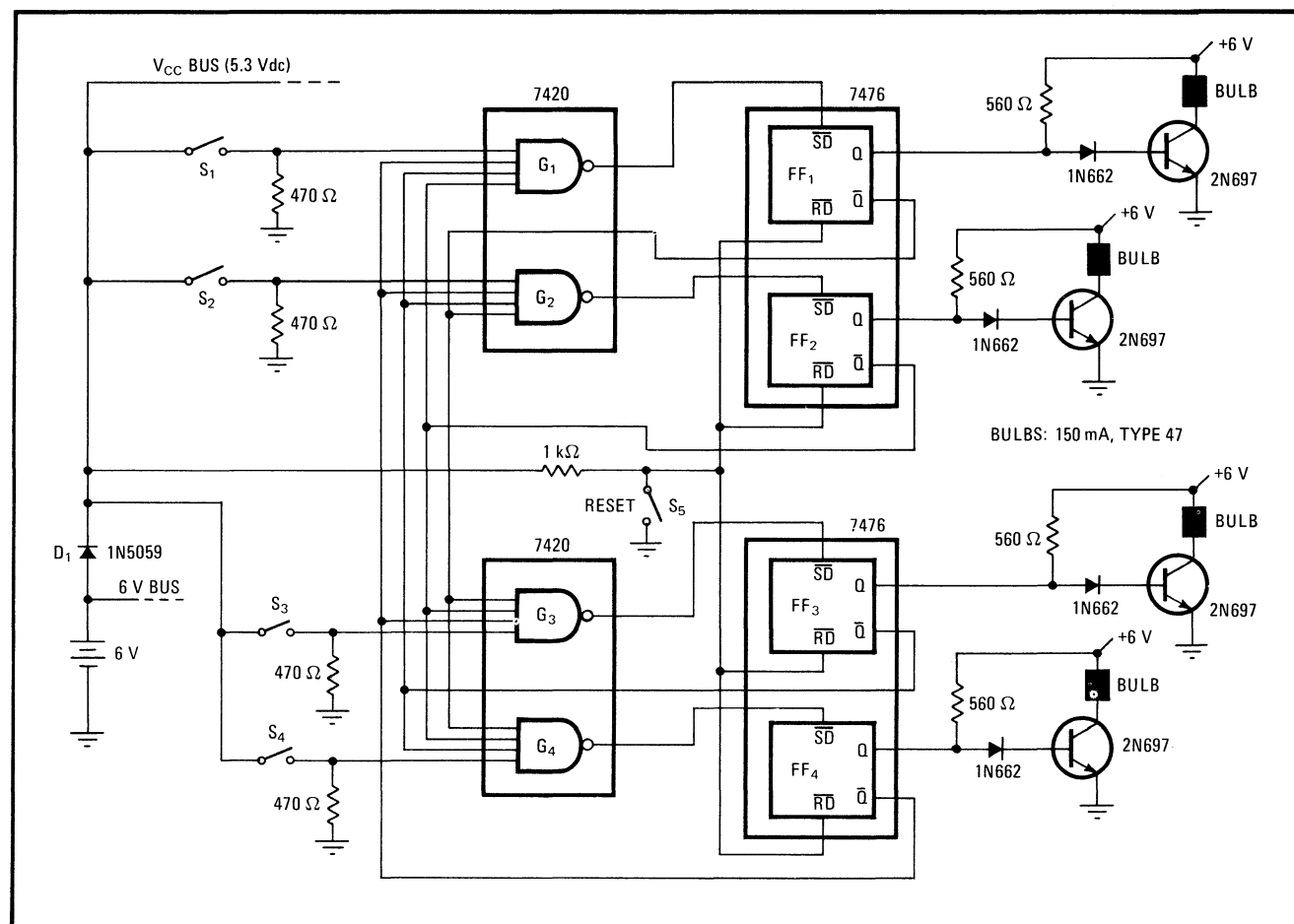
The Q output of each flip-flop is initially low, grounding the base current of the lamp-driver transistors so that all the lamps are dark. And the high \overline{Q} output of each flip-flop is applied to every NAND gate except the one associated with its own flip-flop.

The first switch to close enables its respective NAND gate, producing a low gate output, whose negative-going edge sets the corresponding flip-flop. The Q output of that flip-flop then goes high so that the associated lamp-driver transistor switches on and lights its lamp. Meanwhile, the \overline{Q} output of the triggered flip-flop goes low, inhibiting the other three NAND gates and preventing propagating to the output.

Diode D_1 is a high-current silicon device that is used primarily to drop the lantern-battery voltage to about 5.3 V to observe the limitation on TTL supply voltage of 5.25 V maximum. This diode also protects the logic in the event of a reversal of power-supply polarity. If a 5-V supply is used, the diode is not needed.

This first-response discriminating scheme may be extended to cover N inputs, as long as N N-input NAND gates are used, and TTL loading rules are observed. □

Finding the first. Battery-operable logic circuit indicates which of its four input switches, S_1 through S_4 , closes first. All the flip-flops are initially reset (by switch S_5) with their Q outputs low. The first switch to close enables its associated gate, which then sets the associated flip-flop. This lights the appropriate output lamp and inhibits the other NAND gates so that the other lamps remain dark.



Adding automatic zeroing to analog-to-digital converter

by Tom Birchell
Advanced Electronic Controls, Fremont, Calif.

Automatic zeroing can easily be added to a counting-type analog-to-digital converter by using up/down decade counters and a digital-to-analog converter to generate an error-correction signal. The automatic zero function can be especially useful in a-d applications involving strain gages or other sensors where mechanical considerations can cause minute-to-minute changes in the effective zero point.

Normally, a zero-setting potentiometer must be adjusted constantly, but with the closed logic servo loop shown, it is only necessary to depress a pushbutton switch to produce the activating logic signal. Essentially, the circuit employs the pulse train occurring at the serial output of the counting-type a-d converter to generate

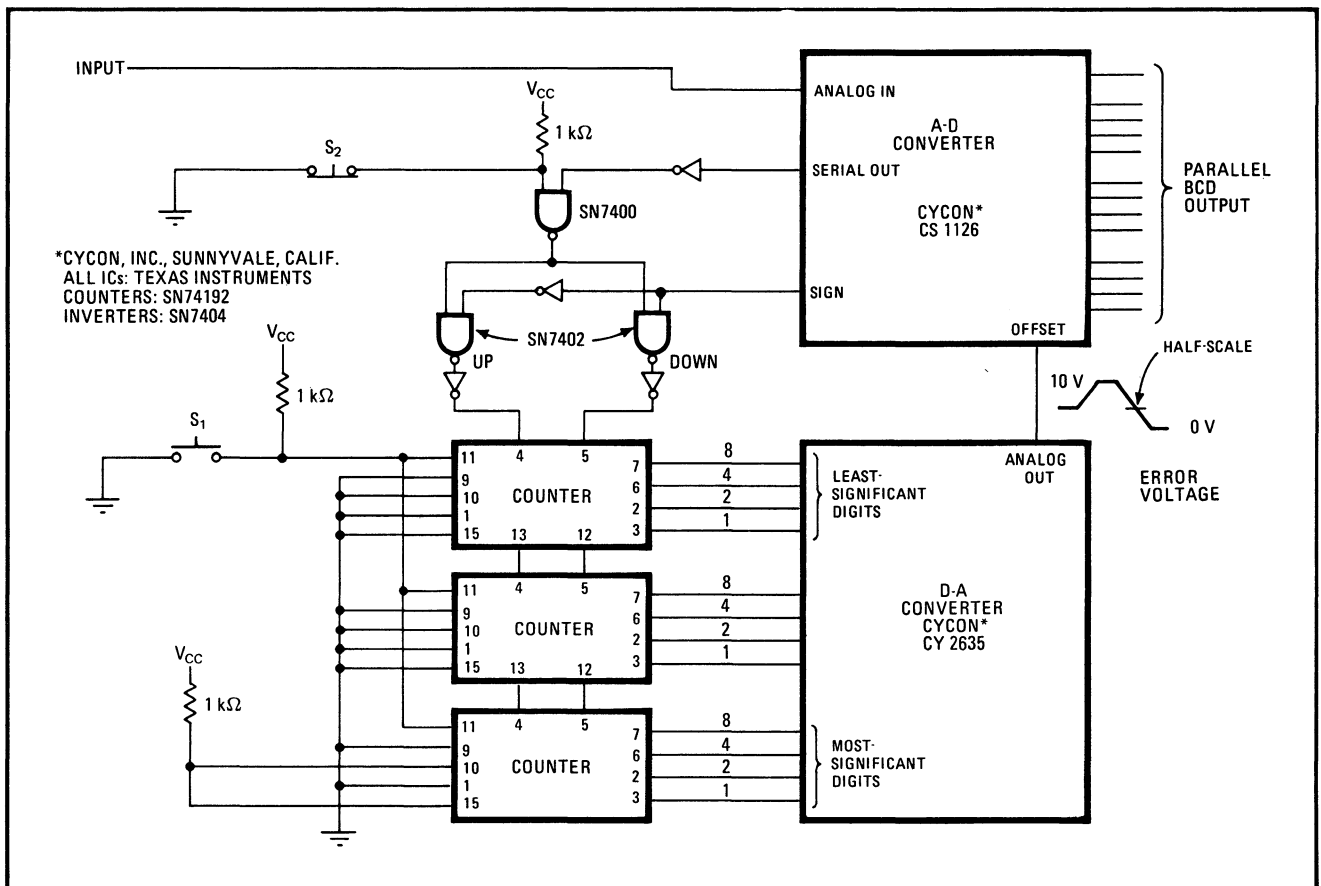
an error voltage. This error voltage is then fed back to the offset-adjustment input of the a-d converter to correct this device's zero setting.

Switch S_1 (which is optional) loads the four-bit synchronous decade counters with a starting number for calibration purposes. Here, the half-scale point of the d-a converter's output is chosen as the calibration number to obtain a symmetrical correction range. If the expected offset variations will occur predominately in one direction, the calibration number should be selected to optimize the correction range.

Once the decade counters are preloaded, switch S_2 initiates the correction cycle. When switch S_2 is depressed, the pulses from the serial output of the a-d converter drive the decade counters either up or down, depending on the error polarity, which is determined by the sign bit. The output voltage of the d-a converter changes accordingly, adjusting the offset input of the a-d converter until no more pulses are produced at this device's serial output. The circuit is now adjusted to the true digital zero point.

For this circuit, the nominal adjustment range is $\pm 7\%$ of the full range of the a-d converter. \square

Eliminating offset error. Closed servo loop containing decade counters and digital-to-analog converter automatically zeroes the offset voltage of analog-to-digital converter. Pulse train from the a-d converter's serial output is used to generate the error voltage. Depending on the sign bit, the counters are driven up or down, adjusting the d-a converter's output and, therefore, the offset input of the a-d converter.



Boosting IC regulator current with almost no power loss

by Don Kesner

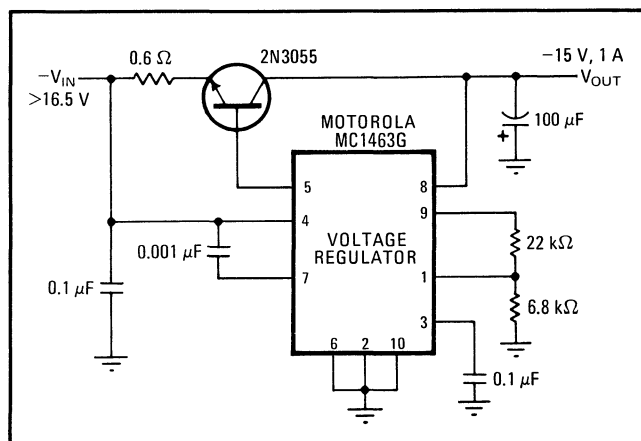
Motorola Inc., Semiconductor Products Div., Phoenix, Ariz.

When the output current of a monolithic voltage regulator is boosted by the addition of a series-pass transistor, the regulator's efficiency is usually lowered because of the base-emitter voltage drop of the outboarded transistor. This added transistor voltage loss raises the input/output voltage differential of the over-all circuit, thereby causing a power loss.

The circuit shown, however, increases regulator current capability without this power loss. The output pin (pin 6 here) of the regulator is grounded so that the device's internal series-pass transistor does not contribute to the over-all input/output saturation characteristics. With this bypass technique, the low voltage differential of the IC alone can be maintained (typically at 1.5 volts here).

For the regulator indicated in the diagram, the absolute minimum differential is based on internal current-source saturation and cannot be lowered, but it is usu-

ally large enough to prevent the external transistor from saturating. Even with a type 2N3055 transistor as the booster, there is no significant difference in the minimum voltage differential with or without current boosting, and with or without a current-limiting resistor. □



Current boosting with minimal power loss. External series-pass transistor increases current capability of monolithic voltage regulator, but decreases power efficiency of over-all circuit. Grounding regulator's normal output terminal (pin 6) bypasses internal series-pass transistor, maintaining over-all circuit's voltage differential ($V_{IN} - V_{OUT}$) at that of the IC alone and making power loss negligible.

Digital clock/calendar offers dual-mode display

by Gregory A. Baxes

BaKad Electronics, Mill Valley, Calif.

Besides indicating whether the time being displayed is a.m. or p.m., an easily assembled digital clock/calendar features a choice of a 12-hour or 24-hour mode. Furthermore, the calendar section has a switch for conveniently setting the number of days in the month. The clock section, of course, also has a switch for selecting either the 12- or 24-hour operating mode.

The entire circuit is built with TTL ICs, and the display is made up of the seven-segment type of readout. MSI devices—presettable decade counters—are used for the units display of both the clock and the calendar. These counters are preset by switch S_1 to reset to 1 in the 12-hour mode and to 0 in the 24-hour mode. Conventional decade counters are used for the tens display for both the clock and the calendar.

Gates G_1 and G_2 and inverters I_1 and I_2 sense the binary outputs of the clock counters, resetting both the tens and units counters upon a "13 o'clock" pulse or a

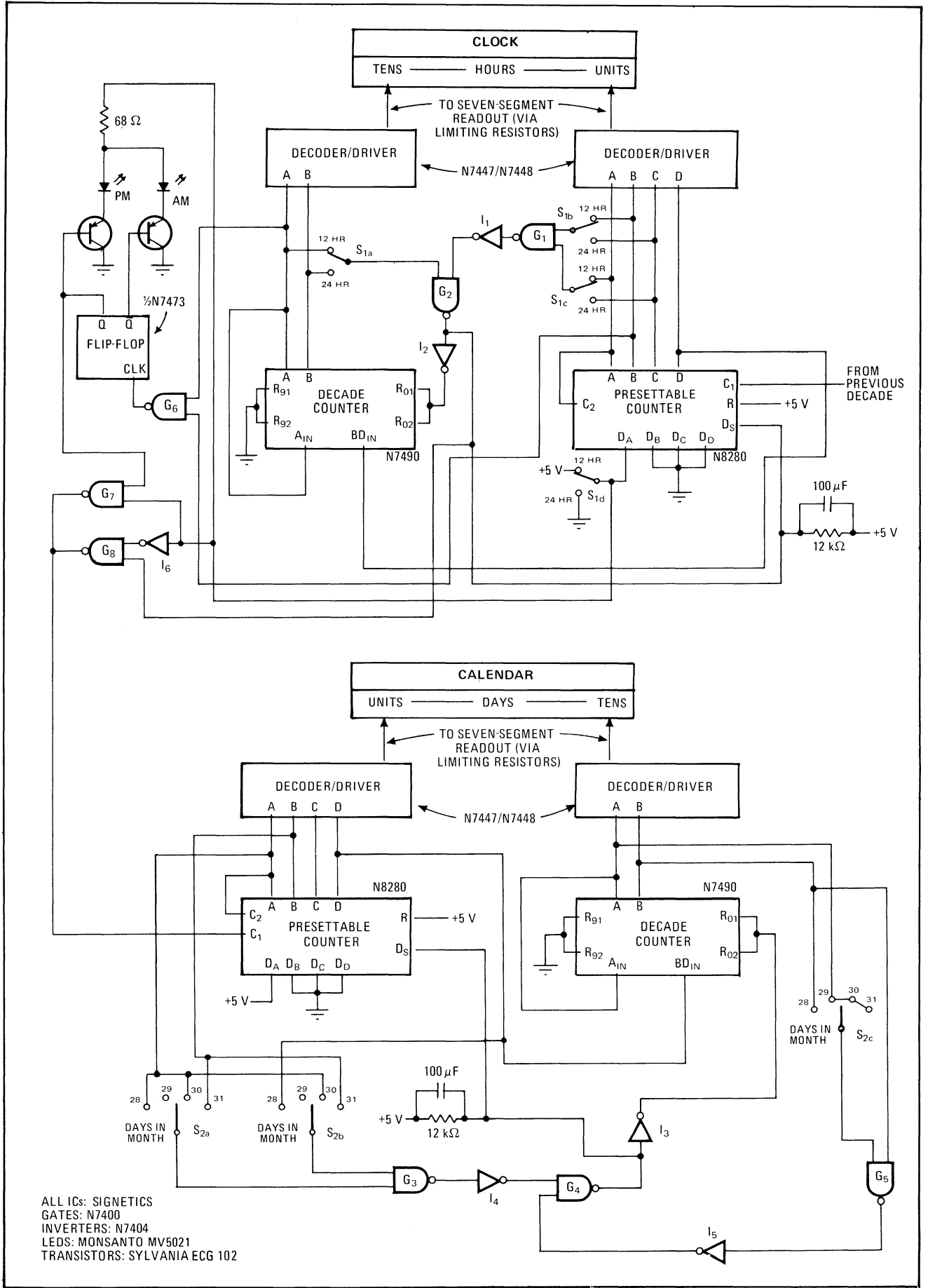
"24 o'clock" pulse, depending on the operating mode. Likewise, in the calendar section, gates G_3 , G_4 , and G_5 and inverters I_3 , I_4 , and I_5 sense the binary outputs of both counters and reset the calendar upon receipt of the "monthly" pulse chosen by the setting of switch S_2 .

Gate G_6 senses the "12 o'clock" output from the clock counters, triggering the flip-flop and also advancing the a.m./p.m. indicator. Gates G_7 and G_8 and inverter I_6 determine when a clock pulse reaches the calendar units counter. In the 12-hour mode, the clock pulse will come from the a.m./p.m. indicator; in the 24-hour mode, the pulse is initiated by inverter I_2 since this device resets the clock tens counter at "24 o'clock."

The reset pulse for both the clock and calendar units counters is a logic high applied to the data strobe (D_S) input of these counters. A reset pulse causes them to strobe their data (D_A , D_B , D_C , and D_D) inputs and, in effect, to reset to either 1 or 0, depending on the operating mode.

Transistors Q_1 and Q_2 can be any small-signal pnp transistor that can drive the light-emitting-diode a.m./p.m. indicators. The 68-ohm resistor limits the current to the LED that is currently lit. In the 24-hour mode, the a.m./p.m. indicator is off. □

Convenient timer. Uncomplicated design for digital clock/calendar keeps the user in mind. The clock section can display time as either a 12-hour or a 24-hour period, depending on the setting of switch S_1 . In the 12-hour mode, the clock lights an LED lamp to indicate whether the time is a.m. or p.m. The calendar section can be set, with switch S_2 , for the number of days in the present month.



ALL ICs: SIGNETICS
 GATES: N7400
 INVERTERS: N7404
 LEDS: MONSANTO MV5021
 TRANSISTORS: SYLVANIA ECG 102

Precision triac trigger has wide dynamic range

by Ronald Sans
Tampa, Fla.

Standard triac triggering circuits do not generally provide an input dynamic range that is broad enough for precise driving of ac loads. But if the ac line is made to synchronize a voltage comparator to a zero-voltage switch, a triac trigger can be built to handle input signals over a 50-decibel dynamic range at frequencies of 10 hertz to 10 kilohertz. The circuit is useful whenever the triggering parameters of a triac must be controlled precisely, as for the currently popular light-box type of music display.

The zero-voltage switch produces a 100-microsecond pulse that begins 50 μ s before the line voltage reaches zero. Every 8.3 milliseconds, therefore, an output pulse from the zero-voltage switch passes through diode D_1 to resistor R_1 and capacitor C_1 . The leading edge of this

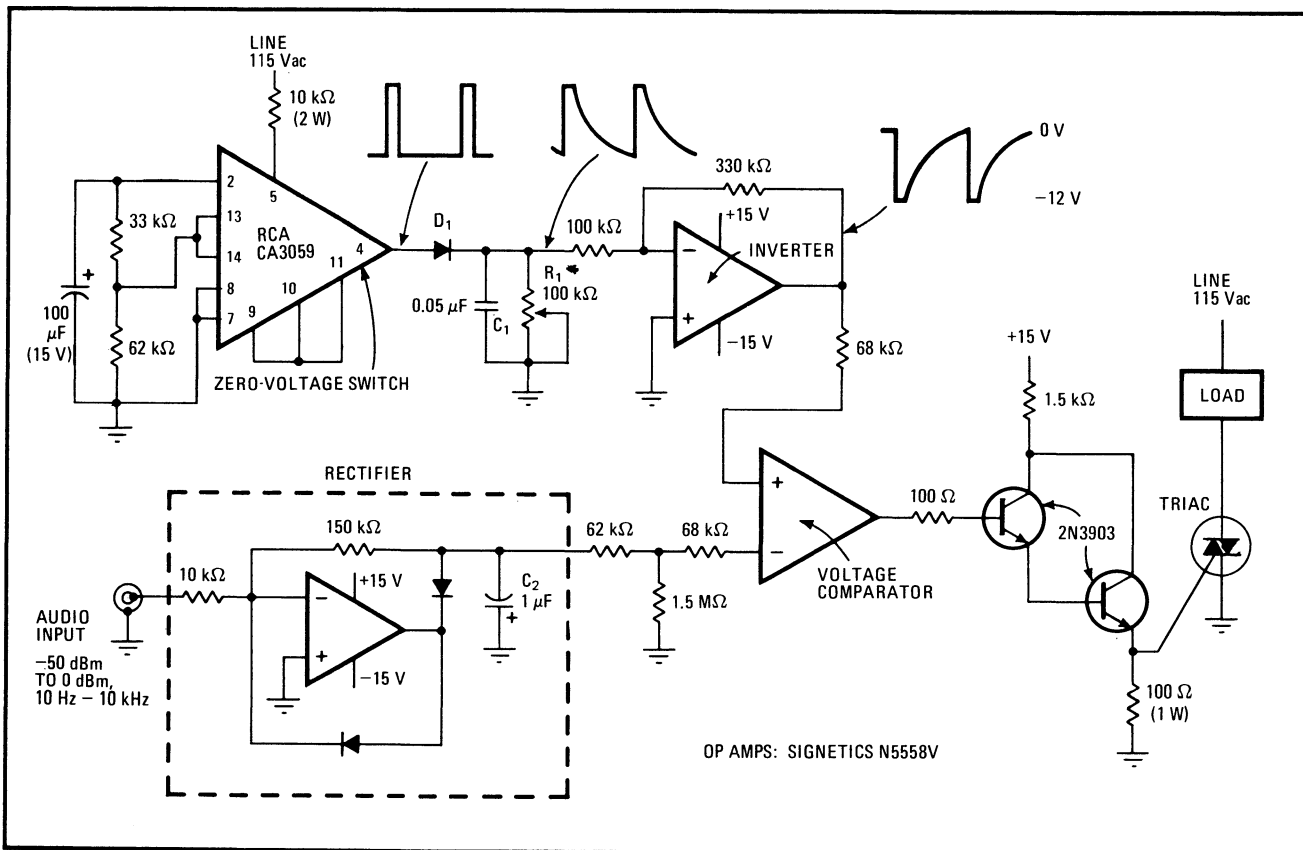
pulse charges capacitor C_1 , while the trailing edge discharges C_1 through resistor R_1 . The dynamic range of the circuit is determined by the setting of resistor R_1 . (When R_1 is set to about 47 kilohms, the dynamic range is approximately 30 dBm.)

Input signals of less than -30 dBm (0 dBm for a 600-ohm reference) turn off the triac; signals equal to -30 dBm just turn on the triac; and signals of 0 dBm or higher produce a full-power output. Since the circuit's output is based on the exponential discharge of capacitor C_1 , the output power of the circuit varies logarithmically and depends on the values chosen for resistor R_1 and capacitor C_1 .

The input signal is applied to the full-wave rectifier, which is capable of accepting signals of less than -50 dBm. The rectifier produces a negative voltage that is filtered by capacitor C_2 and then fed to the inverting input of the voltage comparator. Capacitor C_2 determines how much delay or damping there is; the higher the input frequency, the smaller the capacitor can be.

A conventional Darlington amplifier is used as the output trigger. A higher frequency response can be obtained by using high-frequency operational amplifiers instead. □

Driver for ac loads. Triac triggering circuit operates over wide dynamic range, providing precision control for an ac load like a music display. Audio input power levels can range from -50 to 0 dBm. The setting of resistor R_1 determines the circuit's dynamic range, while the value of capacitor C_2 determines the circuit's damping factor. The circuit is synchronized to the ac line.



Integrated multiplier simplifies wattmeter design

by Donald DeKold
Santa Fe Community College, Gainesville, Fla.

A broadband wattmeter can be built simply and inexpensively with an IC multiplier as the heart of a power-to-voltage transducer circuit that has an output voltage that is directly proportional to the instantaneous load power. The circuit's frequency response extends from dc to several kilohertz. When the output is applied to a simple meter movement or a digital voltmeter, the circuit makes a complete handy power meter.

The maximum load power that the circuit can handle while retaining its proportional output is 2 kilovolt-amperes; this power may be real or reactive. The maximum load voltage, $e_L(t)$, can be 400 volts, while the maximum load current, $i_L(t)$, can be 5 A. The transducer's output voltage is given by:

$$e_{out} = Ke_L(t)i_L(t)$$

where, for the design being shown here, $K = 0.005$ V/VA. Output voltage e_{out} can vary from -10 to $+10$ V, depending on what the instantaneous polarities and

magnitudes of the load voltage and load current are.

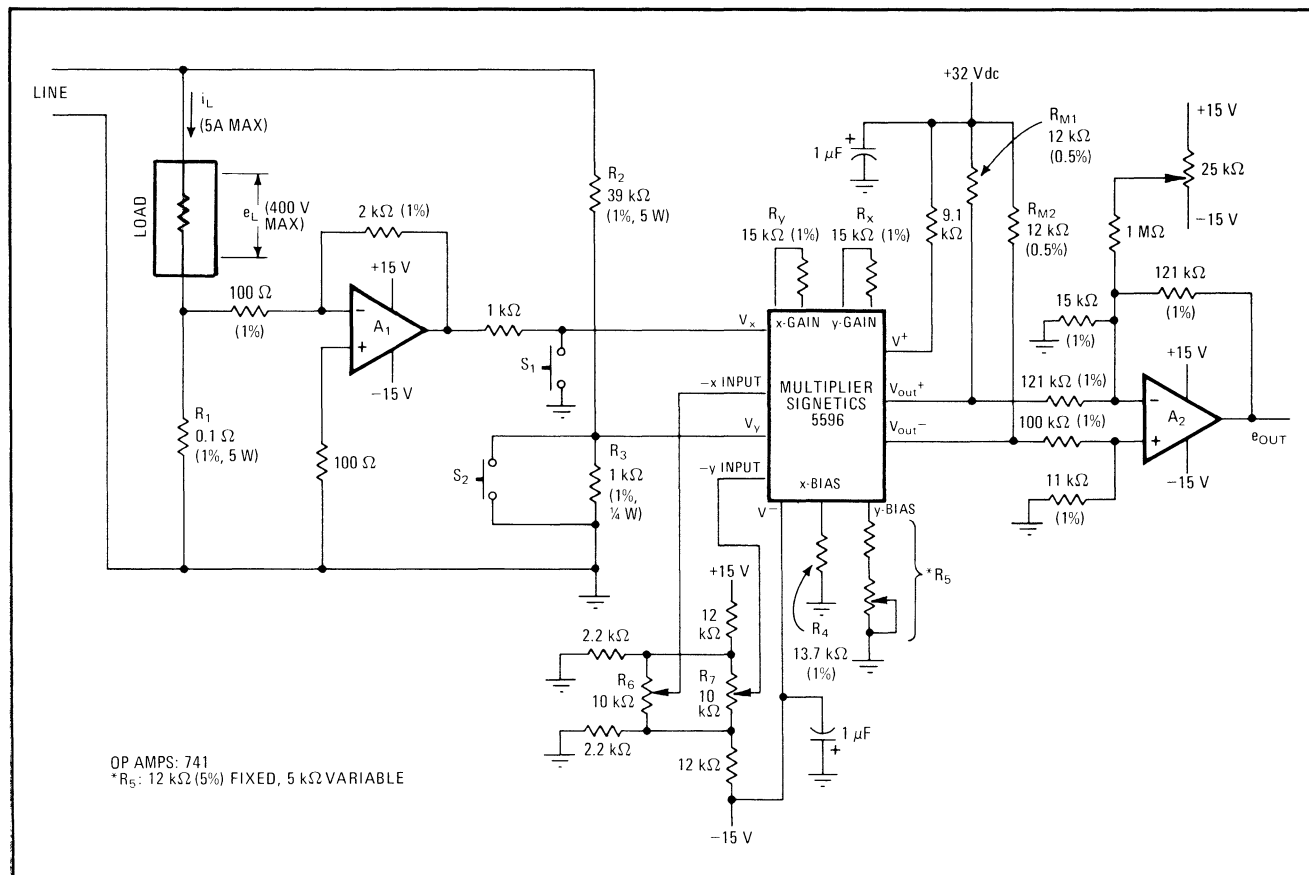
The circuit's voltage and current ranges can be modified easily by simply changing two resistors—resistor R_1 for the current and resistor R_2 for the voltage. Changing the value of these range resistors also alters the value of constant K , thereby producing a wattmeter of whatever range is desired.

Load current is sensed by a current-shunt element, resistor R_1 , and is amplified by a factor of -20 as it passes through operational amplifier A_1 . The output from this op amp is applied to the V_x input of the multiplier. In this case, input V_x must not exceed ± 10 V, restricting load current $i_L(t)$ to a peak value of ± 5 A.

Load voltage, which is derived from the voltage divider set up by resistors R_2 and R_3 , is applied to the V_y input of the multiplier. This multiplier input is also limited to ± 10 V, which holds load voltage to ± 400 V.

The output of the multiplier is a differential voltage (from the V_{out+} and V_{out-} terminals) that is proportional to the product of inputs V_x and V_y . This output depends on a number of factors: the magnitude and polarity of inputs V_x and V_y , the values of gain resistors R_x and R_y , the values of multiplier load resistors R_{M1} and R_{M2} , and the bias currents established by resistors R_4 and R_5 and the supply voltages. For the component values shown, the multiplier's output is approximately $V_x V_y / 10$. (The proportionality constant may be varied somewhat by trimming resistor R_5 .)

Measuring power. IC multiplier produces output that is proportional to the power being dissipated in the load. The circuit is a power-to-voltage transducer that can be used to measure power levels as high as 2 kilovolt-amperes by simply connecting its output to a meter movement or a digital voltmeter. Since all offset voltages are trimmed to zero, fairly accurate measurements can be made over the full output range.



The differential multiplier output is applied to operational amplifier A_2 , which acts as a level shifter and develops a single-ended output voltage. The signal gain through this stage is -1 . Resistor R_6 permits A_2 's offset voltage to be adjusted to within a few millivolts of zero.

In general, when ac power is developed in the load to which the circuit is connected, the load voltage is:

$$e_L(t) = E_{pk} \sin \omega t$$

And the load current becomes:

$$i_L(t) = I_{pk} \sin(\omega t + \phi)$$

so that the power in the load can be expressed as:

$$p(t) = [E_{pk} I_{pk} \cos \phi / 2] - [(E_{pk} I_{pk} / 2) \cos(2\omega t + \phi)]$$

In this last equation, a sinusoidal time-varying component is present that is twice the frequency of the load current or load voltage and that has an average value of zero. The dc term in the power expression represents the average real power dissipated in the load.

The circuit's output voltage reflects these analytical

relationships—it has both a dc component and an ac component of twice the input frequency. When e_{out} is applied to an ordinary average-reading dc meter, the response of the meter is directly proportional to the average real power dissipated in the load.

The transducer circuit is fairly accurate, since the dc offset voltages produced by the multiplier and the level shifter are eliminated. Switches S_1 and S_2 apply a 0-v dc input to the multiplier's V_x and V_y inputs, so that resistors R_6 and R_7 can be used to trim the offset of each of these inputs to zero. (This is most easily accomplished while sensing an ac power signal with an oscilloscope at the output; each voltage input is trimmed for an ac null at the output.)

Precision components, as indicated in the diagram, should be used for best results. It is also essential that the supply voltage be stable since the offset trim voltages are derived from these sources.

Simultaneous readings made with this circuit will deviate nominally from each other by only 1% for the upper 75% of the 2-kVA output range. □

Handy supply provides fixed and variable outputs

By John Predescu
 Buchler Instruments Division, Nuclear-Chicago Corp., Fort Lee, N.J.

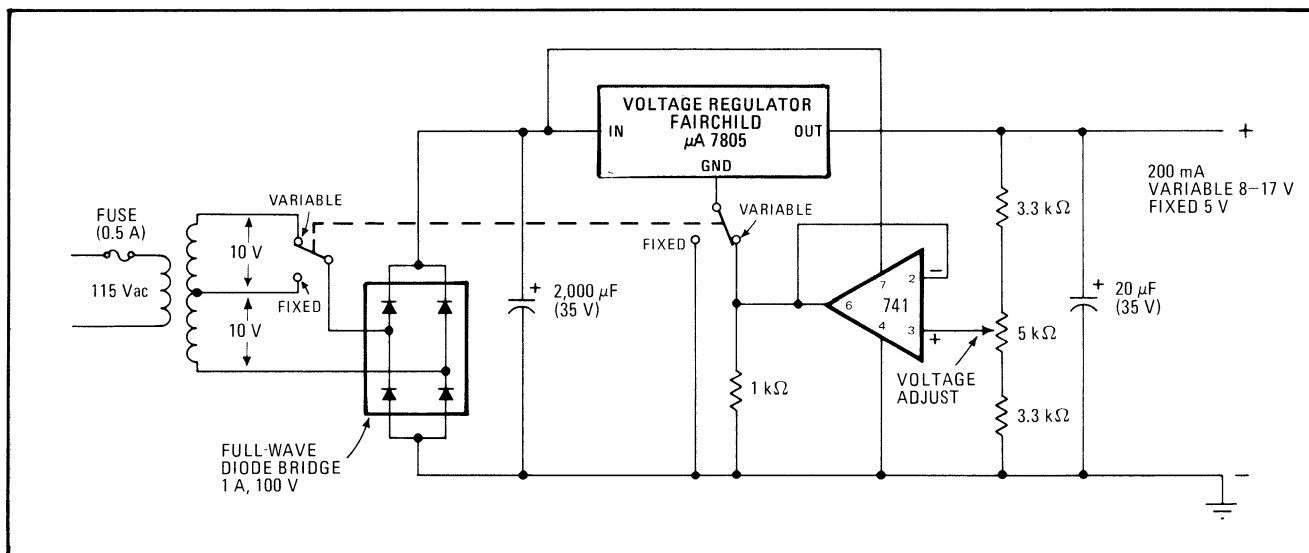
The advantages of today's integrated three-terminal voltage regulators are fully exploited by a versatile power supply that, besides being inexpensive (about \$15) and easy to put together, provides a switch-selectable fixed or variable output. The variable output, which can be adjusted between 8 and 17 volts, is ideal

for C-MOS logic, and the fixed output of 5 v is ideal for TTL circuits. Output current is 200 milliamperes.

The double-pole double-throw switch permits the same IC regulator and diode bridge to be used for both the fixed and variable outputs. The switch bypasses the operational amplifier network and taps the transformer's secondary voltage at the halfway point. A 5-v output can then be obtained from the IC regulator without exceeding this device's power dissipation rating.

If a second supply circuit is built and the positive side of its output grounded, a complete ± 15 -v op-amp supply can be made. Regulation is better than 1%. □

Convenient power supply. Line-powered supply, which makes use of a single three-terminal 5-volt IC regulator, offers switch-selectable fixed and variable outputs. The variable (8- to 17-V) output is obtained by employing a conventional op amp in the regulator's output loop. For the fixed (5-V) output, only half the transformer secondary voltage is taken so that the regulator's power rating is not exceeded.



Miller-effect integrators act as signal separator

by Dale Hileman
Sphygmometrics Inc., Woodland Hills, Calif.

Complementary Miller-effect integrators are better than biased diodes for rectifying a signal and separating it into its positive and negative components. The diodes require enormous integrating capacitors when a dc level in the base line must be retained, and big capacitors commonly have leakage or polarization problems.

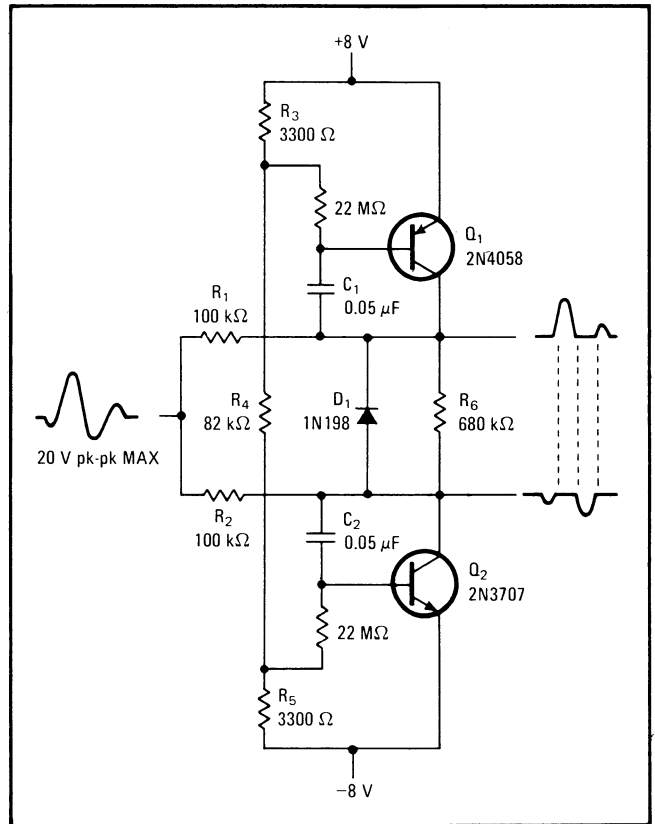
In the signal separator shown, each of the Miller-effect integrator stages serves as a half-wave rectifier. Together with two small 0.05-microfarad integrating capacitors, C_1 and C_2 , they simulate a large effective capacitance that maintains the dc level of the signal's base-line potential.

Negative-going signal excursions cause transistor Q_1 to conduct, clamping the output to the base-line potential. Positive-going excursions, on the other hand, cut off transistor Q_1 and pass directly to the output. The operation of complementary transistor Q_2 , which is the other integrator-rectifier stage, is the same as that of transistor Q_1 , but signal polarity is reversed. A high-impedance load should be used to avoid an excessive voltage drop across either resistor R_1 or resistor R_2 .

The voltage divider set up by resistors R_3 , R_4 , and R_5 holds the base voltages of both transistors close to their conduction threshold so that output signal transitions can be maintained near the base-line potential. Resistor R_6 acts as a collector load for both Q_1 and Q_2 to minimize the effect of their collector-emitter leakage current. Diode D_1 is included to minimize the effect of changing ambient temperature on this leakage current.

Signal separation is best at low frequencies, within

the audio range and down to about 3 hertz. Even lower operating frequencies can be achieved by increasing the values of capacitors C_1 and C_2 , but the rate of base-line integration becomes slower. □



Separating the ups and the downs. Signal separator employs complementary Miller-effect integrators to keep capacitor values low. The circuit permits input dc base-line potential to be retained so that it also is present at the output. Transistor Q_1 prevents negative-going inputs from reaching the output, while transistor Q_2 stops positive-going inputs. The circuit's load impedance should be kept high.

CATV transistors function as low-distortion vhf preamplifiers

by Paolo Antoniazzi
Società Generale Semiconduttori, Milan, Italy

A standard cable-TV transistor makes an excellent vhf preamplifier, minimizing signal distortion over a wide dynamic range. Generally, FETs or MOSFETs are used rather than bipolar transistors because of the cross-modulation distortion created by the nonlinear behav-

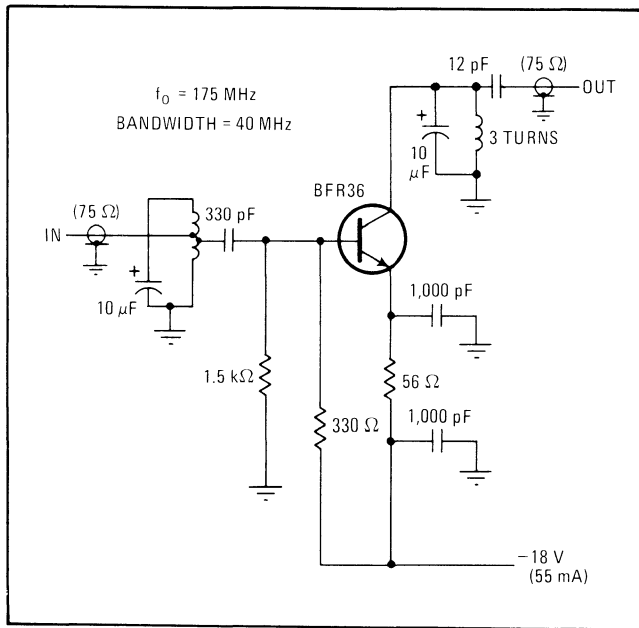
ior of the bipolar's base-emitter junction. CATV transistors, however, operate at currents of 20 to 80 milliamperes, so that their intrinsic emitter resistance is kept small and the effects of input-junction nonlinearities are eliminated.

The single-stage antenna preamplifier shown is intended for mobile fm communications applications and is particularly suitable for use with double-balanced Schottky-diode mixers. It obtains 13 decibels of gain at 175 megahertz from a medium-power CATV transistor.

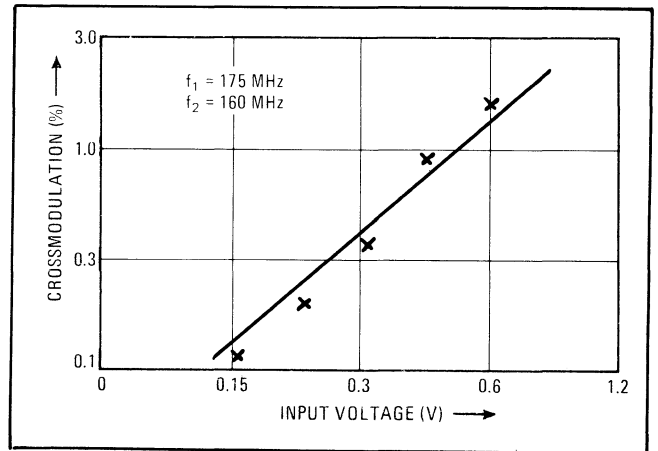
The circuit can handle 0.5-volt inputs with less than 1% cross-modulation, as indicated by the performance plot. Noise figure depends on how large the operating current is. But even for a transistor collector current of

50 mA, the noise figure is typically 5 dB or less.

The transistor used here is designed principally for line-amplifier applications. Its crossover frequency is



1.5 gigahertz, its operating current can range from 20 to 150 mA, and its feedback capacitance is typically 1.7 picofarads at a bias voltage of 15 v. □



Linear performer. Bipolar CATV transistor is heart of vhf antenna preamplifier that can process 0.5-volt inputs with under 1% cross-modulation. The nonlinearities that are normally associated with a bipolar transistor's base-emitter junction and that cause signal distortion are practically eliminated in the CATV transistor because of its high operating current. Circuit gain is 13 dB at 175 MHz.

Electronic switch controls automobile air conditioner

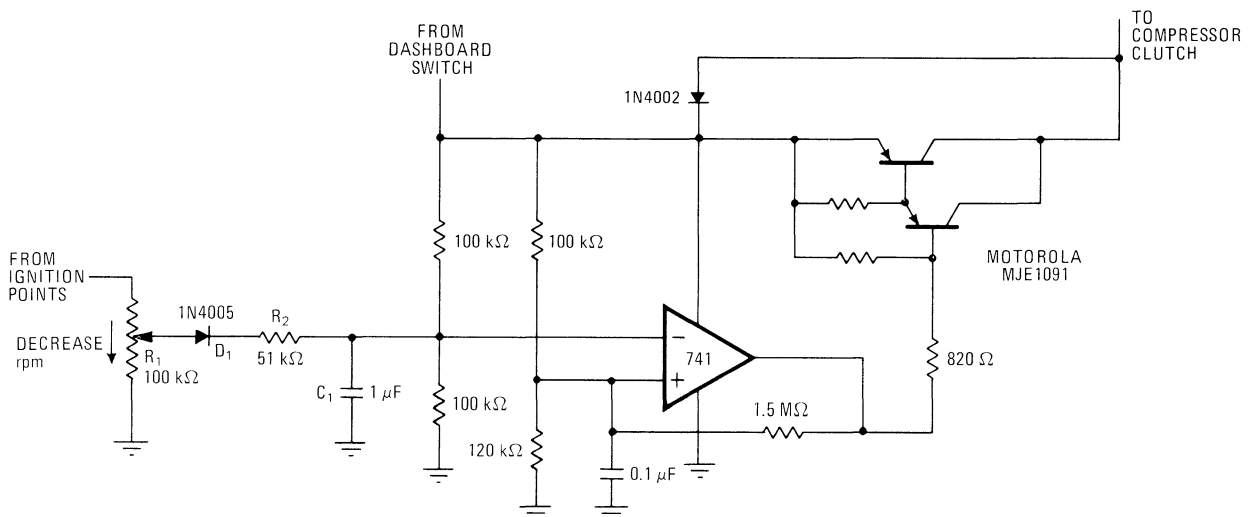
by L.G. Smeins
Ball Brothers Research Corp., Boulder, Colo.

Stalling and overheating often plague an air-conditioned automobile in which the refrigerator compressor continues to run while the engine idles. The solution to the problem is simple—turn the compressor off when

the engine is idling, and turn it on again when the car picks up speed.

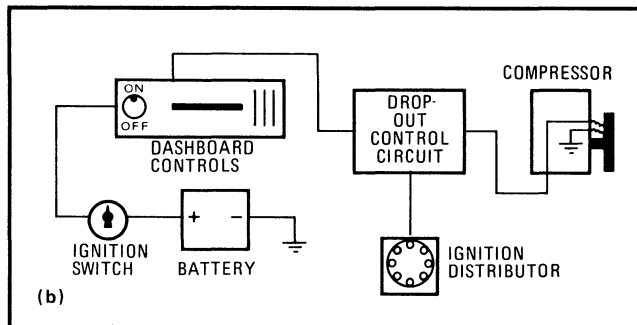
The control circuit shown in (a) does this by monitoring the engine's rpm and electrically disengaging the compressor clutch for as long as the engine is idling. The circuit works well for the electromagnetic compressor clutch found in most cars.

Compressor drop-out and pull-in are controlled by an operational amplifier that is connected as a Schmitt trigger and that drives a series bipolar switch. When engine rpm falls below the drop-out voltage level, which is determined by potentiometer R_1 , power is removed from the magnetic clutch. Hysteresis in the Schmitt trig-



ger prevents the clutch from engaging again until the engine rpm is approximately double the drop-out rpm. The simple charge-pump pulse-rate network, consisting of diode D_1 , resistor R_2 , and capacitor C_1 , performs the rpm sensing.

After the circuit is installed as suggested in (b), the drop-out point should be adjusted for optimum performance. To do this, first start the engine and let it idle with the air conditioner turned on. If the compressor clutch is not engaged, turn potentiometer R_1 (in the direction for decreasing rpm) until the clutch engages. Now turn this same potentiometer (in the direction of increasing rpm) until the compressor clutch just disengages. At this potentiometer setting, the compressor should turn on when engine rpm increases to approximately 1,700 and should turn off when the engine drops back to an idle. □



Keeping cool. Control circuit (a) monitors engine rpm and turns off air conditioner when engine drops to idle, preventing stalling or overheating. The operational amplifier is connected as a Schmitt trigger, whose hysteresis provides the voltage differential needed between compressor turn-on and turn-off. A bipolar switch drives the compressor's clutch. The circuit can be installed easily (b). □

Digital-to-analog converter is built from low-cost parts

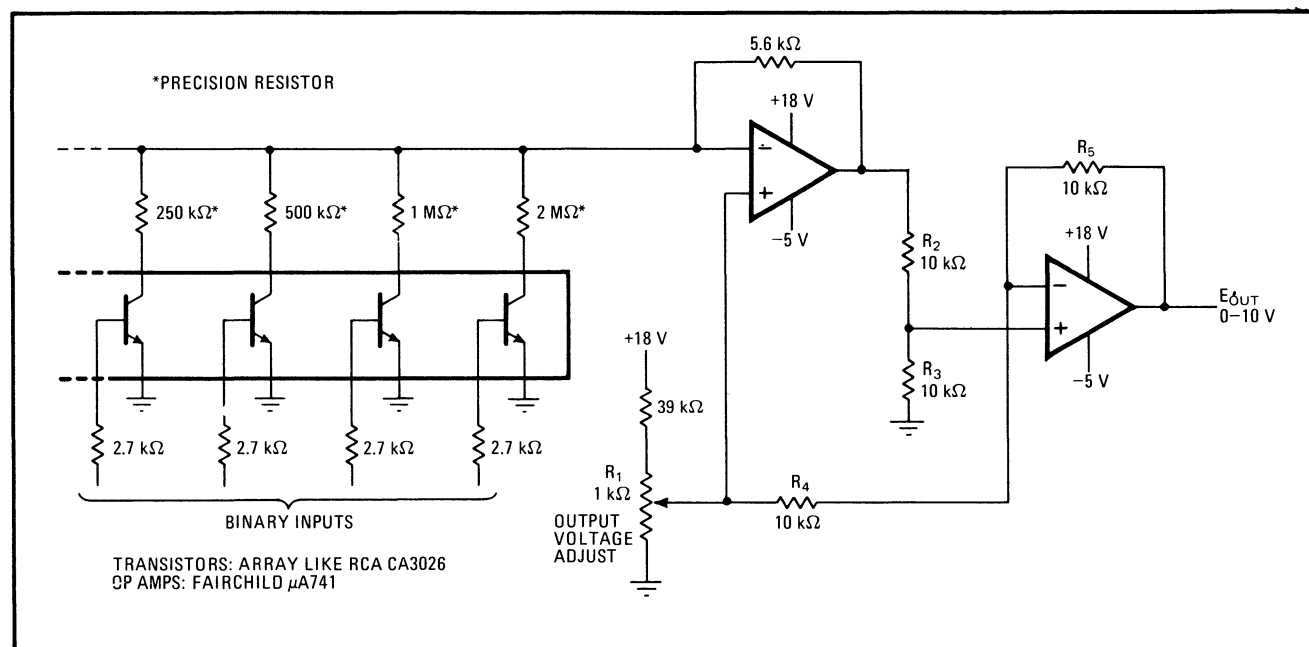
by Phillip J. Storey
Jands Pty. Ltd., Marrickville, N.S.W., Australia

An economical but reliable digital-to-analog converter can be made from readily available IC transistor arrays and general-purpose op amps. The converter is intended to interface with decimal or hexadecimal up/down counters, as well as directly addressed memories. It provides a positive-going output voltage that ranges from 0 to 10 volts and that can be used to control

audio attenuators or light-dimmer units.

Each input transistor clamps its precision resistor to ground when a binary bit is applied to that input line. Input words can be up to 8 or 12 bits in length. Potentiometer R_1 allows the maximum output voltage to be varied about the nominal 10-v level. Additionally, as long as resistors R_2 through R_5 have at least a 1% tolerance, the output dc offset voltage will be only on the order of millivolts.

The converter works best within the frequency range of 3 hertz to 1 kilohertz, but can operate at clock rates as high as 100 kHz. However, output glitches become evident at the faster clock rate. □



Ready-made DAC. This digital-to-analog converter can almost be put together from a spare-parts box, since it is made up of components that are usually right on hand. Input words can be 8 or 12 bits long, and the positive-going analog output varies from 0 to 10 volts. If 1% resistors are used in the output stage, the output offset voltage is within millivolts of zero without any prior adjustment.

Helping a 709-type op amp to outperform itself

by Jiří Dostál
 Research Institute for Mathematical Machines, Prague, Czechoslovakia

A complementary-transistor output stage turns the 709-type operational amplifier into a far better performer than it is by itself. Such a stage can extend the device's unity-gain bandwidth to 15 megahertz, its slew rate to 300 volts/microsecond, its full-power frequency to 5 MHz, and its dc gain to 300,000. Moreover, the resulting over-all amplifier settles in only 3 μ s to within 0.01% of the full-scale output voltage.

The circuit's high-frequency and pulse characteristics are derived from the output stage. Its input offset characteristics are principally those of the op amp.

At dc or low frequencies, the gain of the op amp is multiplied by the gain of the output stage. The equivalent differential resistance between the collectors of transistors Q₁ and Q₂ is designed to be about 100 kilohms, making the gain of the output stage approximately equal to 7. Resistor R₁ is included to keep the

stage's gain at this value, in case the differential resistance changes. Resistor R₂, on the other hand, reduces output distortion by assuring that the op amp's output emitter-follower is effectively biased off.

At the circuit's upper frequency limit, the op amp rolls off rapidly and the gain of the parallel feed-forward path dominates. The transfer function of the op amp becomes that of an integrator, which is formed by series resistor R₃ and the feedback collector capacitances, C_{C1} and C_{C2}, of transistors Q₁ and Q₂. The circuit's small-signal bandwidth can be written as:

$$f_t = 1/[2\pi R_3(C_{C1} + C_{C2})]$$

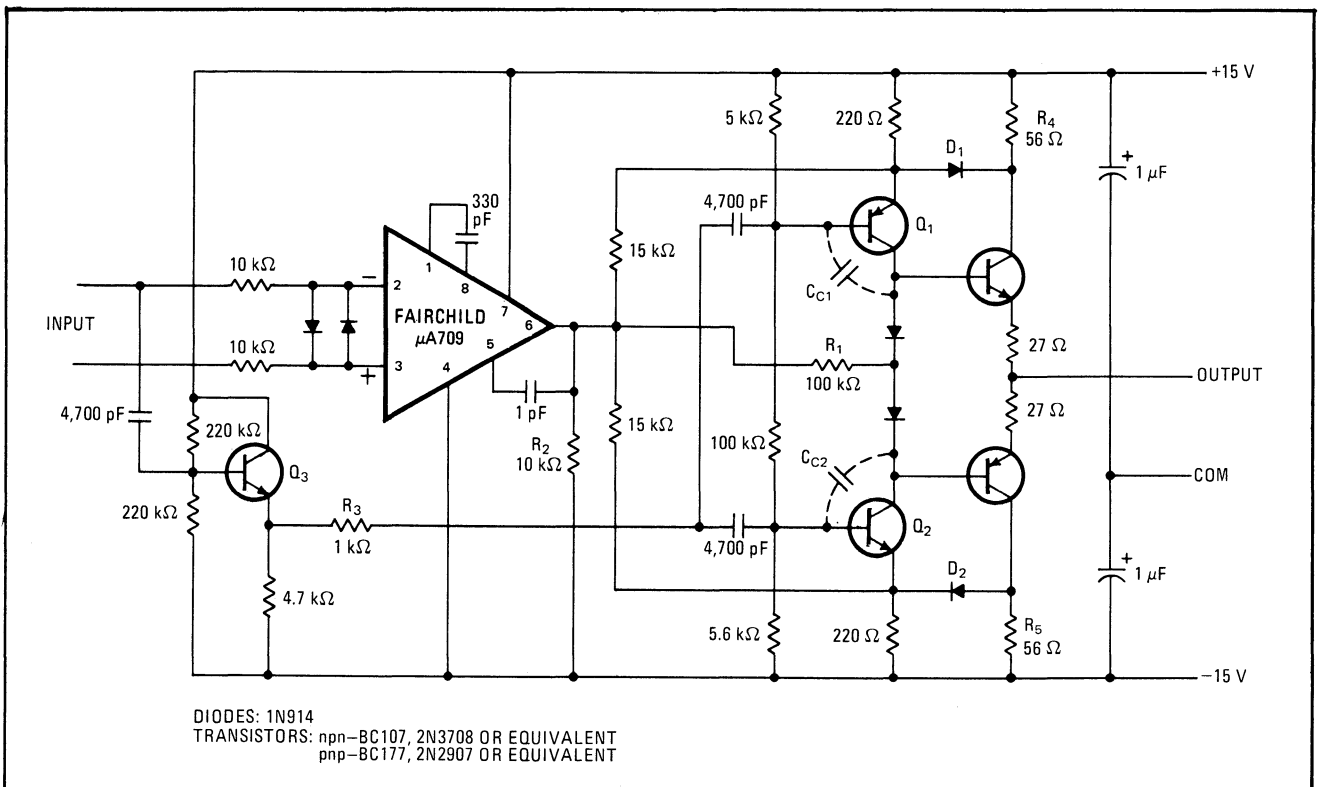
which is approximately 15 MHz when C_{C1} and C_{C2} are each 5 picofarads. The emitter current of transistor Q₃ sets the circuit's slew rate:

$$S.R. = I_{E3}/(C_{C1} + C_{C2})$$

which is around 300 V/ μ s for an emitter current of 3 milliamperes.

The constant base potentials of transistors Q₁ and Q₂ are used to limit any output short-circuit currents, which are sensed by resistors R₄ and R₅ and diodes D₁ and D₂. If desired, the signal line to the op-amp's noninverting input can be biased within the common-mode range of the 709-type op amp. □

Super amplifier. Output stage made up of complementary transistors increases the speed and extends the frequency response of the 709-type op amp. The over-all amplifier, which can be powered by one ± 15 -volt supply, has a unity-gain bandwidth of 15 megahertz and slews at the rate of 300 volts/microsecond. At high frequencies, the op amp is like an integrator, and capacitances C_{C1} and C_{C2} dominate.



Integrated timer operates as variable Schmitt trigger

by Maj. Arthur R. Klinger
United States Air Force, McCoy Air Force Base, Fla.

The bargain-priced 555-type IC timer—already a proven and versatile circuit building block—can also be used as a variable-threshold Schmitt trigger. The triggering circuit has a high input impedance, a latching capability, a threshold voltage that can be adjusted over a wide range, and simultaneous open-collector/totem-pole outputs.

The usual circuit diagrams (a) of the timer can be redrawn with conventional logic symbols to illustrate the operation of the triggering circuit. As shown in (b), the timer can be thought of as a comparator that has a high input impedance and that drives a Schmitt trigger having a high-input-impedance latch and a buffered strobed output.

Transistors Q₁ through Q₈ make up one of the noninverting comparators, while transistors Q₉ through Q₁₃,

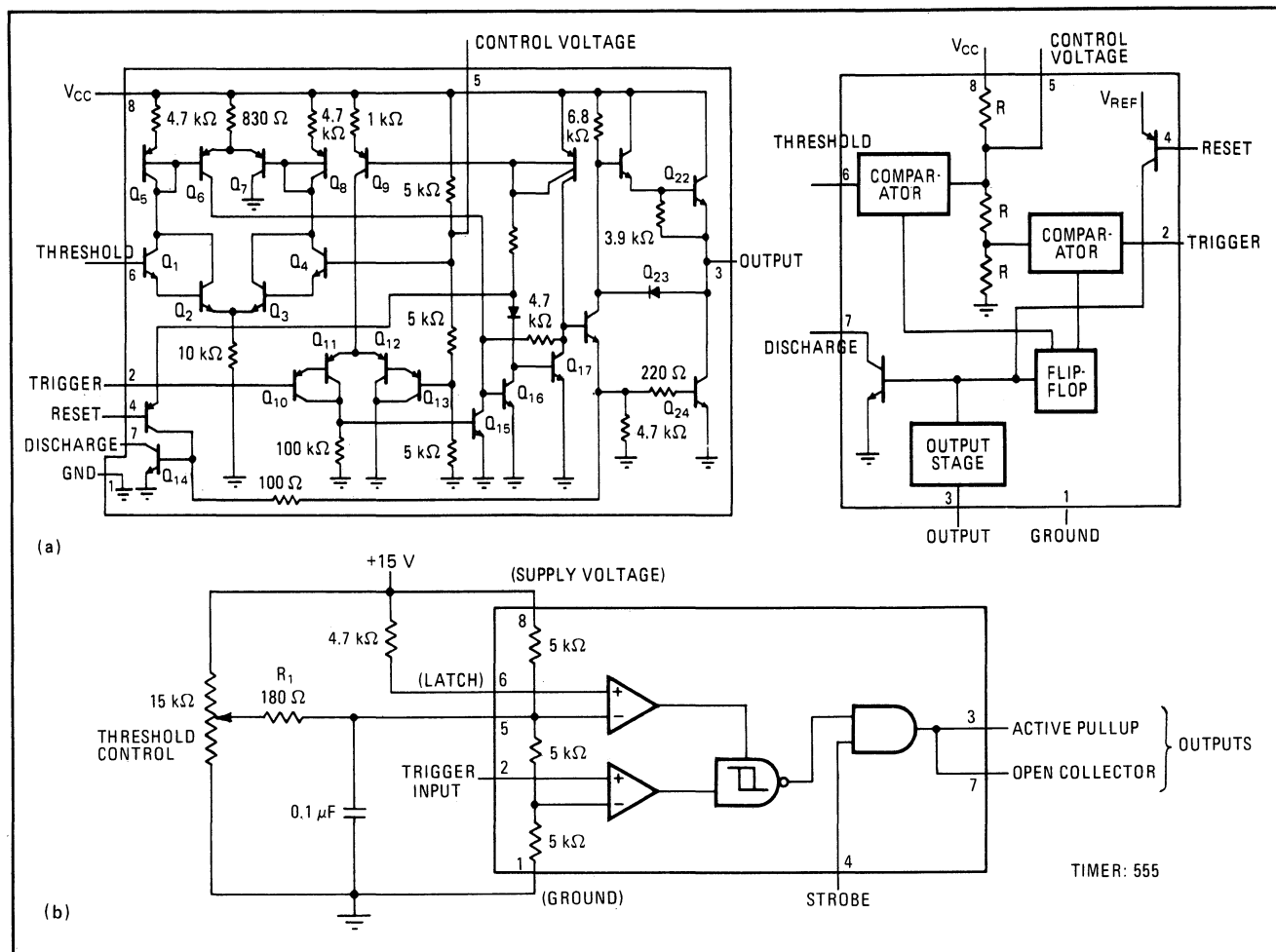
as well as transistor Q₁₅, form the second noninverting comparator. This last comparator drives the Schmitt trigger created by transistors Q₁₆ and Q₁₇.

Although it seems that the two comparators are simply ANDed together at the input of the Schmitt, the limited source/sink current capability of the first comparator allows the second comparator to take precedence. The first comparator, then, merely acts as a latch, allowing the other comparator, in combination with the Schmitt, to be triggered when the latching input (pin 6) is high. When this input goes low, the Schmitt and, therefore, the circuit's output are locked in whatever state the Schmitt is in.

A resistor (of 4 kilohms to 100 kilohms) from the latching input to the supply unlatches the Schmitt and, at the same time, tends to decouple this input from high-frequency line noise. Theoretically, in some applications, the timer's control input (pin 5) and latching input could be tied together directly to the supply, but both inputs are very susceptible to noise.

The timer's trigger input (pin 2), which has an input impedance of approximately 1 megohm, drives the Schmitt. The Schmitt's threshold can be varied from about zero to just below the bias voltage existing at the latching input by controlling the voltage at pin 5.

Analog/digital interface. Standard 555-type timer (a) can be regarded as a Schmitt trigger having two high-impedance driving comparators and a buffered strobed output. Triggering circuit of (b) provides a controlled threshold range, which can be varied from almost zero to 8 volts. Upper comparator acts as a latch, while the lower comparator and the Schmitt provide the normal triggering action.



A normal strobe function is provided by the timer's reset input (pin 4); the timer is active when the reset input is high. The latching input, of course, can be pulled low to catch the last device state whenever desired. Active pull-up and open-collector outputs are available simultaneously at pins 3 and 7. Both of these outputs can sink a considerable amount of current.

If intermediate control voltage levels are used at pin 5, the threshold level at pin 6 will still be predictable, and the impedance level for this input will remain high. Supply voltage can range from 4.5 to 16 v, and operating frequency can range from slowly varying dc to at least 2 or 3 megahertz.

As with any high-speed functional IC, certain precautions should be observed for the timer. Since its com-

parators can respond to pulses as short as 20 nanoseconds, the control and threshold inputs should be bypassed or decoupled from the supply line whenever possible. Also, the source impedances at the two comparator inputs should be kept balanced to minimize the effects of offset currents. Moreover, when the trigger input is overdriven to about -0.2 v or lower, the timer's output returns to its high state, doubling the frequency of recurring input waveforms.

Because of noise and bias levels, problems may arise occasionally when the control input is tied directly to the supply or to less than about 0.5 v. (The latter bias condition corresponds to a 0.25-v input threshold.) Resistor R_1 should be 180 ohms or more to avoid these potential problems. □

Two-IC pulse discriminator handles wide range of inputs

by Steven E. Holzman
ESL Inc., Sunnyvale, Calif.

Just two IC packages will build a pulse-width discriminator having a pulse window that may be as narrow as tens of nanoseconds or as wide as several seconds. Applications for the circuit include radar, communications, and signal-processing systems.

The lower pulse limit (T_L) is determined by the timing period (T_A) of one-shot OS_A , while the upper pulse limit (T_U) is established by the sum of this timing period and the timing period (T_B) of one-shot OS_B :

$$T_L = T_A$$

$$T_U = T_A + T_B$$

Of course, period T_A for one-shot OS_A and period T_B for one-shot OS_B are set by selecting the proper values (from a data sheet) for resistor R_A and capacitor C_A ,

and resistor R_B and capacitor C_B , respectively.

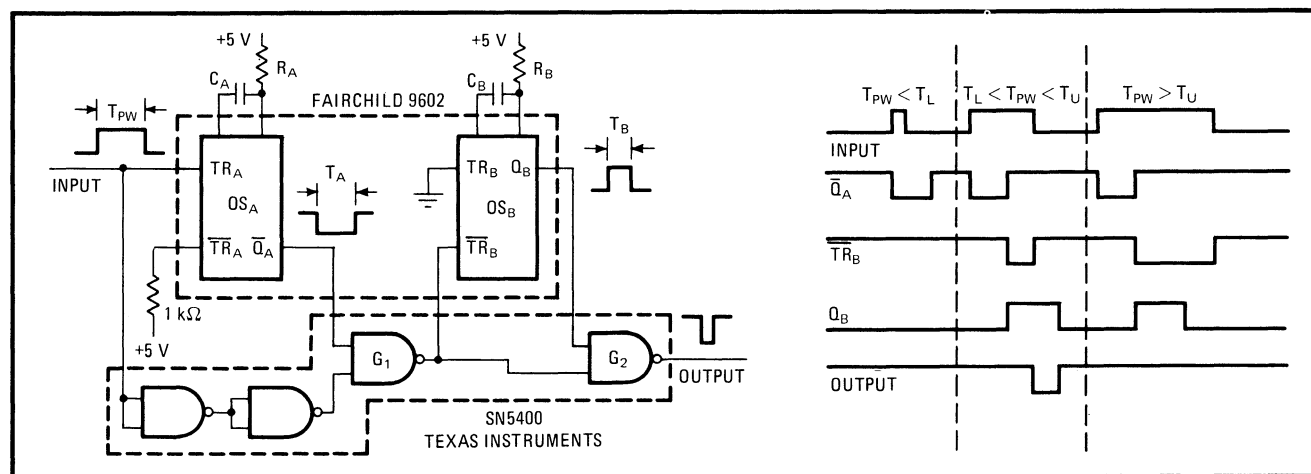
When the input pulse width, T_{PW} , is less than T_A , one-shot OS_A is triggered, but one-shot OS_B is not. The input pulse's leading edge causes the \bar{Q}_A output of OS_A to go low for T_A seconds. However, NAND gate G_1 remains inhibited because the delayed (by two gates) version of the input pulse returns to its low state before the \bar{Q}_A output becomes high again.

If the input pulse is within the circuit's time window, gate G_1 is enabled when \bar{Q}_A returns to its high state, triggering one-shot OS_B so that its Q_B output goes high for T_B seconds. NAND gate G_2 is also enabled, producing an output pulse and indicating that the input pulse width "qualifies."

When the input pulse lasts longer than upper time limit T_U , the Q_B output of one-shot OS_B goes high while gate G_1 is still enabled. This inhibits gate G_2 and prevents an output pulse from being generated.

The two NAND gates between the input and gate G_1 slow up the input pulse so that narrow pulses do not occur at G_1 's output before one-shot OS_A can trigger. □

Pulse-width window. This circuit produces an output only when the input pulse width falls within preset time limits. Timing period (T_A) of one-shot OS_A sets the lower limit (T_L), while the timing periods ($T_A + T_B$) of both one-shots set the upper limit (T_U). Qualified pulses trigger both one-shots and enable all the gates. Short pulses do not trigger one-shot OS_B , and long pulses do not enable gate G_2 .



Digital demodulator for phase-shift-keyed data

by C.A. Herbst
Technology Resources, Paris

Exclusive-OR gates and a repeat-modulation scheme can be combined to produce a digital phase-shift-keyed (PSK) demodulator that allows accurate recovery of the reference-carrier pulse train. The demodulation of binary PSK data usually involves two major problems: recovering the reference carrier, and differentiating between the logic 0 and the logic 1 data pulses. This latter problem is resolved easily with differential coding, assigning a logic 1 when the change in carrier phase is 180° and a logic 0 when there is no change.

The first problem, however, cannot be resolved as simply. Usually, the input PSK-modulated carrier frequency is multiplied by 2 to cancel out the phase changes. But this technique, unfortunately, generally results in a degradation of demodulator performance.

A better method is to remodulate the demodulator's local oscillator with the received data so that the phase changes due to input modulation are cancelled out. This produces a virtually unmodulated reference carrier that is equal in phase to one of the two possible input PSK phase states. The ambiguity between the two phase conditions can be resolved by differential encoding.

The circuit shown employs this improved demodulation technique. A quad exclusive-OR IC is used to perform both the demodulation and remodulation functions. Here the exclusive-OR gates are operated as controlled inverters. In the phase-detector portion of the circuit, the PSK input carrier and the remodulated voltage-controlled-oscillator (VCO) signal are normally at quadrature with each other when the system is in lock. This results in a pulse train having a 50% duty cycle at the output of gate G_1 . The pulse train is then integrated by the low-pass filter into a dc error signal.

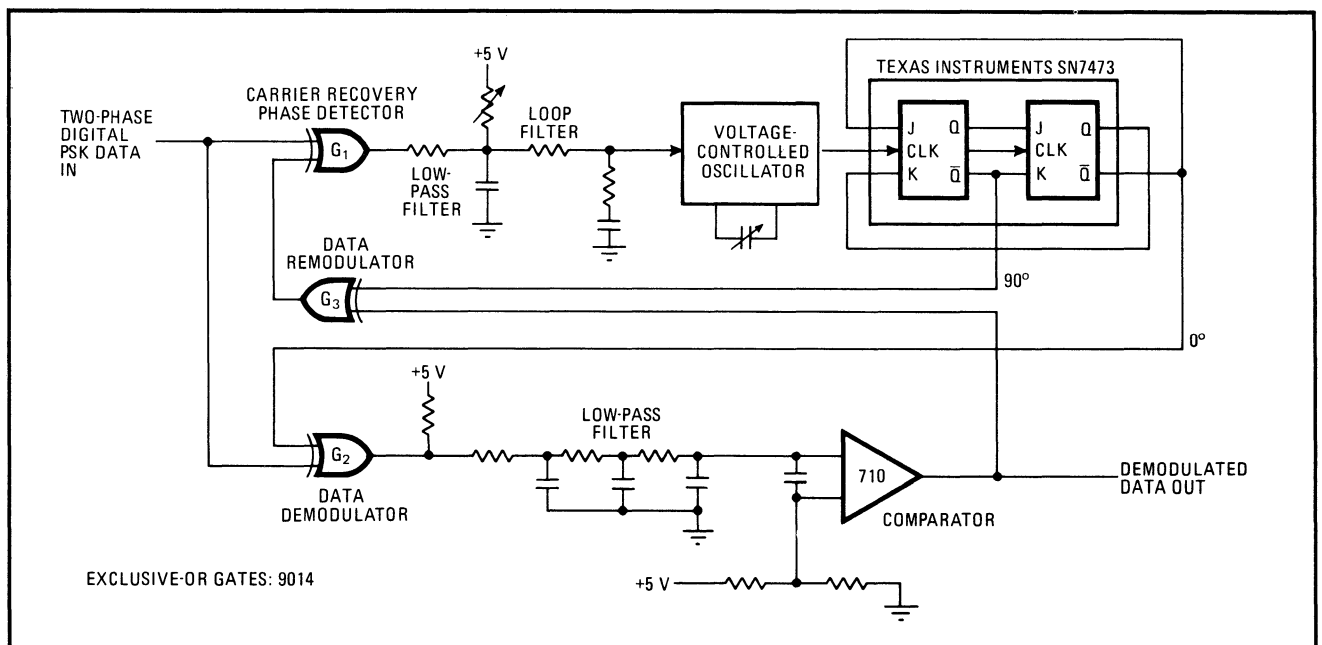
As the phase difference between the input PSK signal and the input VCO signal deviates from its normal 90° shift, the pulse train at gate G_1 's output becomes width-modulated. The average dc error voltage then changes, correcting VCO phase and frequency in the direction that reduces demodulation error.

In the circuit's data-demodulator section, the input signal and the VCO output are either mostly in phase or mostly out of phase with each other, depending on the modulation status of the input PSK signal. Therefore, the output of gate G_2 is either logic 0 or logic 1, according to the status of the PSK data.

A second low-pass filter then integrates G_2 's gate output signal, which is subsequently squared by the comparator to produce the demodulated output data. This final output signal is also used to modulate the VCO by means of gates G_1 and G_3 . □

BIBLIOGRAPHY
C.A. Herbst, "Digital Phase-Locked-Loop with Loss-of-Lock Monitor," EDN/EEE, October 15, 1971.

Unscrambling a binary line. Demodulator for phase-shift-keyed inputs operates exclusive-OR gates as controlled inverters to decode the input data and recover the reference carrier. Input data is remodulated with an error-corrected output from the voltage-controlled oscillator, cancelling out any phase changes from the input modulation. This permits a nearly unmodulated reference carrier to be recovered.



Combined op amps improve over-all amplifier response

by William Ott
Burr-Brown Research Corp., Tucson, Ariz.

By interconnecting a low-drift op amp with a wideband op amp, the best characteristics of both amplifiers can be preserved in a composite amplifier that offers the added benefit of increased open-loop gain. Typically, wideband op amps tend to produce significant errors because they exhibit a large offset voltage drift with time and temperature. But in the composite amplifier, the low-drift op amp can continuously compensate for the input offset voltage of the wideband op amp.

The composite amplifier of (a) is an inverting-only configuration. Low-drift amplifier A_1 senses the offset voltage between ground and the summing junction of wideband amplifier A_2 . Any offset that is present will be integrated by A_1 to develop an offset-compensating voltage at the noninverting input of A_2 .

This integration continues until the summing junction voltage is offset from ground by only the input offset voltage of low-drift A_1 (including the effects of A_1 's input bias currents on resistors R_1 and R_2). The offset voltage of the composite amplifier, therefore, is essentially that of the low-drift op amp.

For the differential-input composite amplifier of (b), A_1 amplifies the offset voltage at the inputs of A_2 . Low-drift amplifier A_1 , then, supplies an offset-compensating voltage for the offset-nulling input of A_2 .

In this way, the output of amplifier A_1 reduces A_2 's offset voltage to that of the low-drift op amp, plus the offset from the bias current in resistors R_1 and R_2 . As with circuit (a), the offset voltage and the offset voltage drift of the wideband op amp are essentially replaced by those of the low-drift op amp.

The open-loop gain of both composite amplifiers is $A_{02}(1 + \alpha A_{01})$, where α is defined as $E_x/A_{01}E_i$, and A_{01} and A_{02} are the dc open-loop gains of amplifiers A_1 and A_2 , respectively. For the inverting-only configuration of (a), the quantity, αA_{01} , is the response of the integrator formed by amplifier A_1 , resistor R_1 , and capacitor C_1 . For the differential-input configuration of (b), α is essentially a constant and is independent of frequency; it is the change in the offset voltage of amplifier A_2 due to a change in A_1 's output voltage, E_x .

If the inverting-only composite amplifier is to have a single pole in its open-loop gain response to insure gain stability, then:

$$R_1 C_1 = A_{02} / 2\pi f_{c2}$$

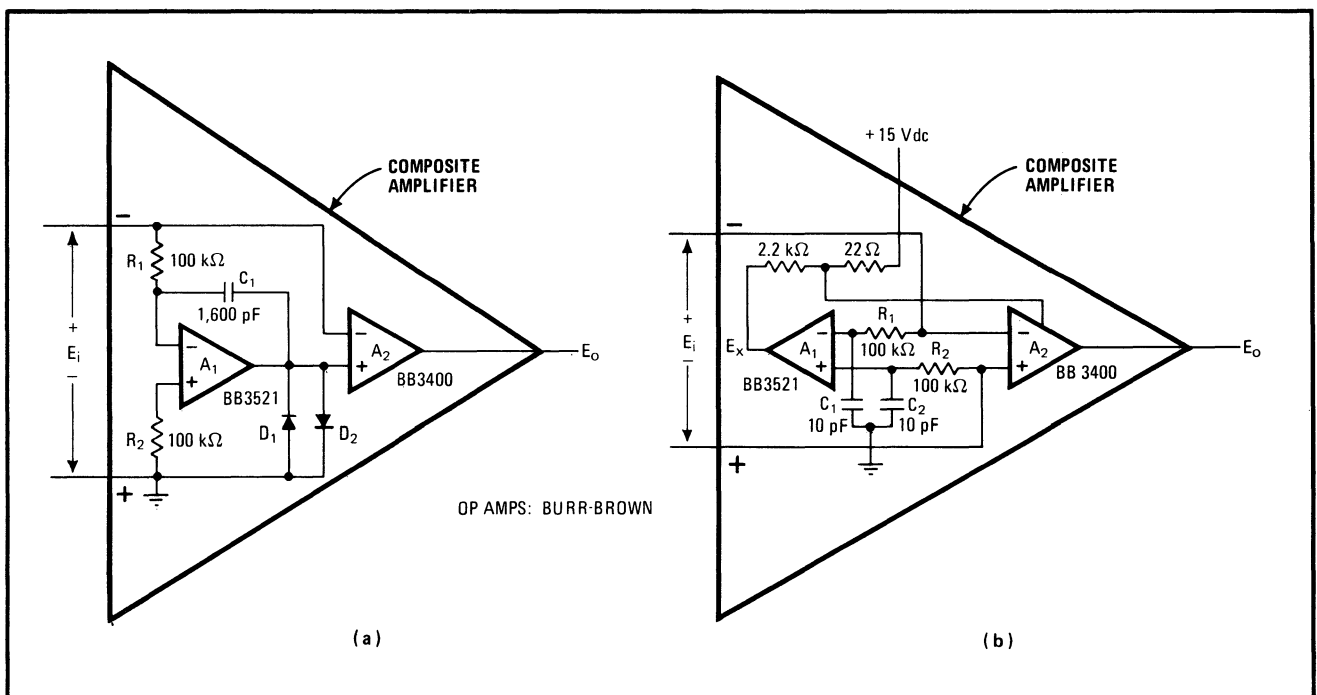
where f_{c2} is the unity-gain bandwidth of amplifier A_2 . The bandwidth of the composite amplifier is essentially equal to f_{c2} , about 100 megahertz. The over-all offset voltage is about 200 microvolts, with a drift of $1 \mu\text{V}/^\circ\text{C}$. The over-all open-loop gain is around 200 decibels.

For the differential-input composite amplifier to have a single pole in its open-loop gain response:

$$\alpha = -f_{c2} / A_{02} f_{c1}$$

where f_{c1} is the unity-gain bandwidth of amplifier A_1 . Like the inverting-only amplifier, the differential-input amplifier has an over-all bandwidth of 100 MHz, an offset voltage of 200 μV , and an offset voltage drift of

A good combination. Two op amps—a low-drift one (A_1) and a wideband one (A_2)—can be wired to produce a composite amplifier that is both fast and stable. Circuit (a) is an inverting amplifier, while circuit (b) is a differential amplifier. Both amplifiers provide an over-all bandwidth of 100 megahertz, an over-all offset voltage of 200 microvolts, and a total offset voltage drift of $1 \mu\text{V}/^\circ\text{C}$.



1 $\mu\text{V}/^\circ\text{C}$. The circuit's over-all open-loop gain, however, is somewhat smaller—140 dB.

Besides less offset voltage drift and more open-loop gain, the differential-input amplifier offers the additional advantage of improved common-mode rejection at low frequencies. For low-frequency operation, the common-mode rejection of the wideband op amp is essentially replaced by that of the low-drift op amp, which typically provides much better common-mode rejection.

In circuit (a), diodes D_1 and D_2 at the output of the

low-drift op amp prevent a latch-up condition from occurring. Latch-up is possible in the composite amplifier when the low-drift op amp's output saturation voltage exceeds the wideband op amp's common-mode range.

And in circuit (b), there are two low-pass filters (formed by resistors R_1 and R_2 and capacitors C_1 and C_2) at the inputs of the low-drift op amp. They prevent high-frequency common-mode voltage swings from unbalancing the input stage of the low-drift op amp and changing its input offset voltage. □

Inexpensive power supply produces zero-ripple output

by Rod Spencer
Chlorescope Systems, Linden, N.J.

Here is an easy way to build a low-cost power supply in which ripple voltage can be brought virtually to zero. Through a feedback arrangement, the ripple voltage is inverted and summed to cancel the normal ripple.

As indicated in the figure, an operational amplifier and a series-pass transistor are connected in the standard manner. However, a portion of the unregulated ripple voltage is fed into the op amp's inverting input.

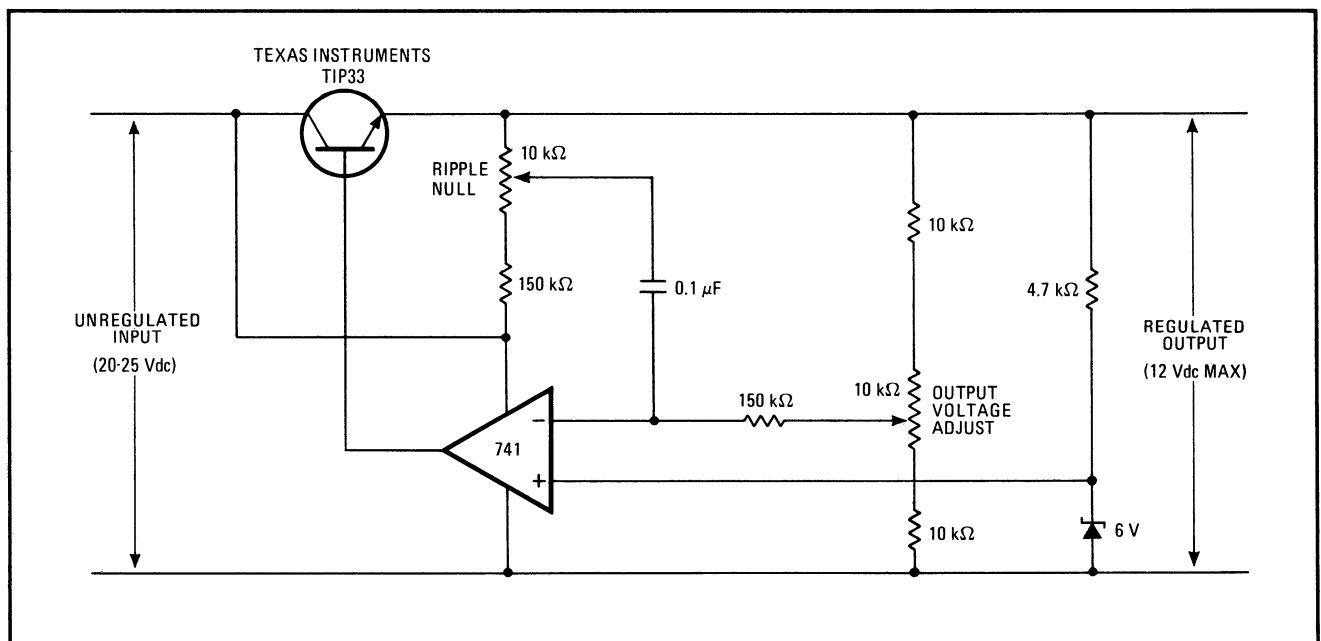
When the wiper of the RIPPLE NULL potentiometer is set up toward the output voltage bus, the supply's ripple is normal. But when the pot wiper is set down toward its

unregulated-input end, a phase shift of 180° is introduced, and the ripple is reversed. If this RIPPLE NULL is adjusted properly, the supply's ripple voltage can be completely eliminated.

To adjust the circuit, first set the regulated output voltage to the desired level and then subject the output to the maximum load condition. Next, use an oscilloscope to monitor load voltage, and trim the output ripple voltage to zero. This supply's ripple will remain essentially zero for any load condition less than the maximum.

Representative component values are shown in the figure, and parts should be chosen to satisfy a particular application. The series-pass transistor, of course, is selected to meet load requirements. And, if an op amp cannot supply a sufficient base drive for the transistor chosen, a Darlington pair can be used instead. □

Cancelling ripple. Low-cost power supply employs inverting feedback loop to eliminate output ripple voltage almost entirely. Some of the circuit's unregulated ripple is applied to the op amp's inverting input, where it is reversed. This "negative" ripple cancels the supply's normal "positive" ripple. The technique can be made to satisfy a variety of application requirements by adjusting the component values.



Register-addressing system accesses within nanoseconds

by C.A.N. Conde, C.A. Correia, and A.D. Figueiredo
University of Coimbra, Portugal

Addressing systems for shift registers with circulating memories need not be slow and complex. A system containing synchronous binary counters and exclusive-OR gates can considerably speed up clock rate while reducing circuit complexity. For an eight-bit system, propagation delay can be reduced to only 37 nanoseconds.

Generally, shift-register-addressing systems are slow because they compare the address of a counter that is triggered by the clock pulse with the address of a reference register. Instead, it is faster to use up/down synchronous counters in their down-counting mode, as shown in the diagram for an eight-bit system.

When the eight-bit binary counter, which is formed

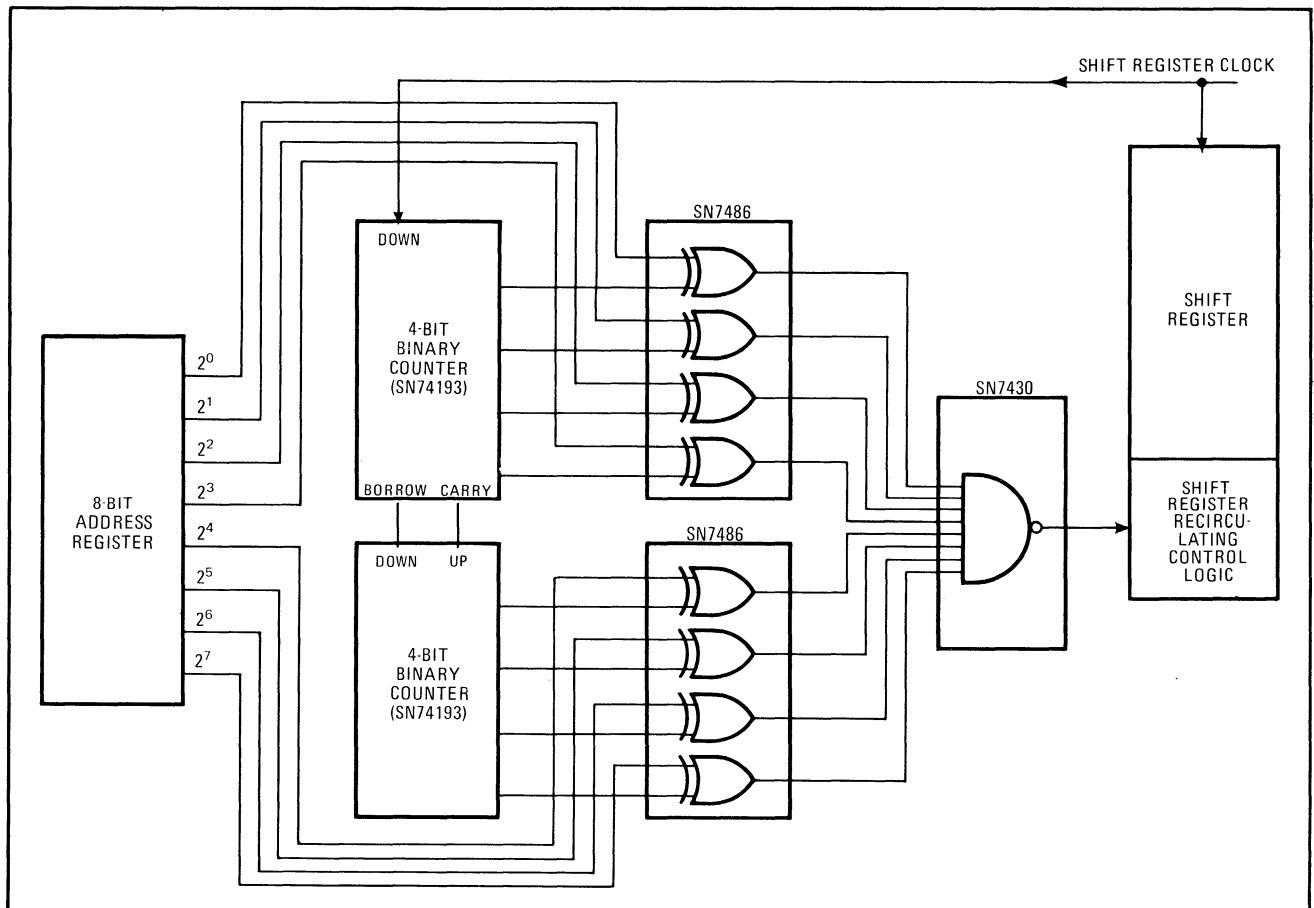
by the two four-bit counter packages, is in its down-counting mode, it generates successive output clock pulses (1111 1110, 1111 1101, . . . , 0000 0001, 0000 0000, 1111 1111). If, for example, the address register is storing the number 3 (binary equivalent 0000 0011) as the address to be referenced, the counter, after three clock pulses, will contain the binary number 1111 1100, which is the complement of the binary equivalent of number 3.

All the outputs of the exclusive-OR gates will then be logic 1, producing a logic 0 output at the NAND gate to the control logic. This logic 0 output can now be used to gain access to the shift-register bit given by the reference address.

For any address, a logic 0 exists at the output of the NAND gate only when the address is the complement of the binary counter state. And this condition will occur only after the counter generates a number of pulses equal to the contents of the address register.

Although quite fast, this system does have a drawback—it works for binary-coded data but not for binary-coded-decimal data. □

Gaining access. High-speed eight-bit addressing system for shift register cuts propagation delay to only 37 nanoseconds. Exclusive-OR gates compare the outputs of the address register to the outputs of the synchronous binary counter. When these outputs are complementary, the output of the NAND gate becomes logic 0, providing access to the control logic for the system's shift register.



Narrowband digital filter achieves high Qs

by Thomas A. Visel
University of Illinois, Urbana, Ill.

A digital filter that is built with conventional logic ICs permits Qs of 2,000 to 10,000 to be readily achieved. Additionally, the filter's bandwidth is entirely independent of its operating frequency. And, as with other active filters, this circuit's upper frequency is primarily limited by the maximum bandwidth of the operational amplifiers used.

The operating frequency (f_0) is determined by the rate at which flip-flop FF₁ is clocked. Flip-flops FF₁ and FF₂ form an N-stage counter ($N = 2$ here), and the applied clock rate is Nf_0 . The decoder functions as an N-line-to- 2^N -line open-collector decoder, dividing the incoming signal into 2^N time periods at resonance. For the circuit shown, when f_0 is 1 kilohertz, each of these periods (T_k) is 250 microseconds long.

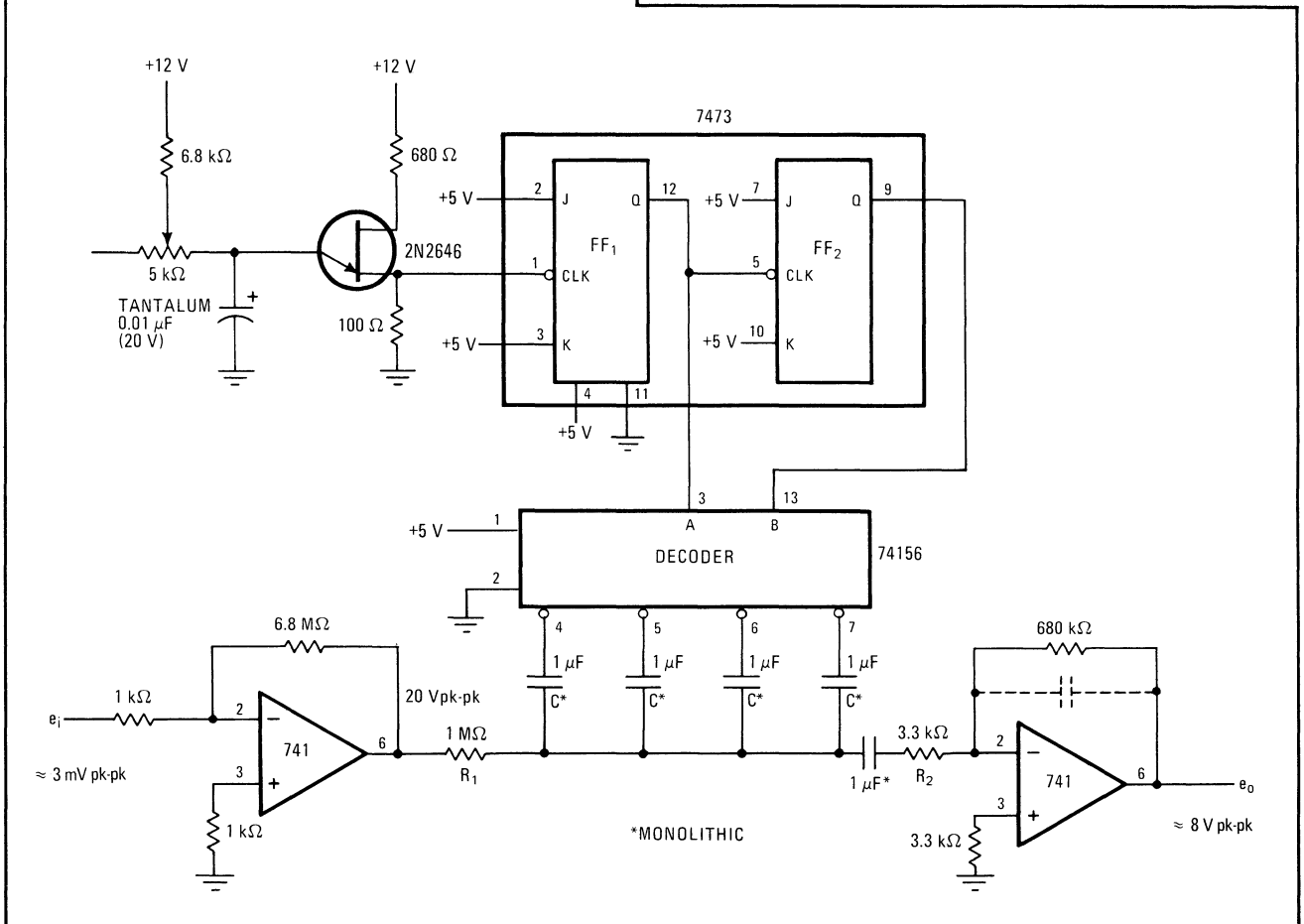
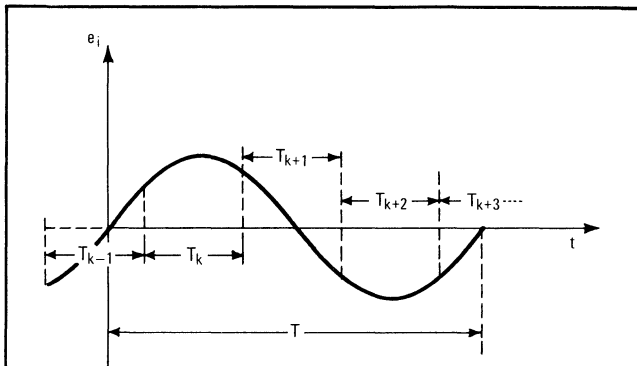
At resonance, each of the four decoder outputs turns on successively for a quarter period of the incoming signal. This successively charges each of the decoder's output capacitors to:

$$V_c = \int_{T_k}^{T_{k+1}} \frac{Ae_i \exp(-t/R_1C) dt}{R_1C}$$

where A is the gain of the input operational amplifier. At resonance, each capacitor reaches an equilibrium charge, drawing very little current through resistor R₁.

When the filter is not at resonance, each T_k period falls during random times of the input signal. This means that up to three of the decoder's external output capacitors may discharge through the collector-base

Simple digital filter. Flip-flops FF₁ and FF₂ function as an N-stage counter ($N = 2$) whose clock rate determines the filter's resonant frequency (clock = Nf_0). The decoder divides the input signal period into 2^N time periods so that the input is continuously sampled. At resonance, the output voltage is maximum because the charge across the decoder capacitors (C) does not change between input cycles.



junctions of the decoder's internal output transistors, while the selected capacitor charges, or vice versa. A rather large net current will then be drawn through resistor R_1 , diminishing the output voltage.

The output waveform, therefore, appears as a sampled version of the input signal. The more counter and decoder stages there are, the more exact will be the output waveform sample. A two-stage counter, like the one used here, is sufficient for such applications as synchronous tone detection in audio spectrum analyzers. Criti-

cal filtering applications will require additional stages.

For the components given, the filter's operating frequency is limited to 2.5 megahertz, and its 3-dB bandwidth is 12 hertz set at an f_0 of 20 kHz. When resistor R_2 is a large value, the filter's bandwidth is:

$$BW = 1/(4\pi R_1 C)$$

For a 500-Hz step in frequency, the output response envelope is about 8 milliseconds from its 10% to 90% points. □

Gate threshold difference produces initializing pulse

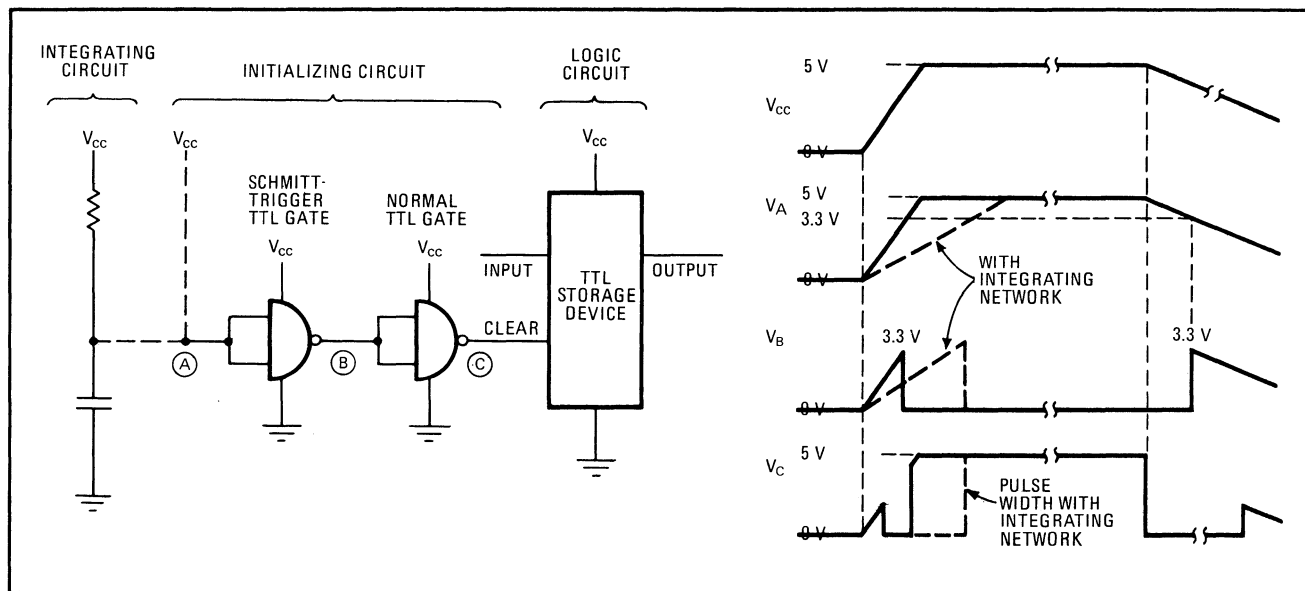
by Jose Souto Martins
GTE Automatic Electric Inc., Northlake, Ill.

Often it is necessary to have a digital circuit assume a predetermined logic state when the supply is turned on. This is not always easy to do, particularly when the digital circuit contains storage devices such as flip-flops and latches. But a simple two-gate circuit, consisting of a standard TTL NAND gate and a Schmitt-trigger TTL NAND gate, can solve this initialization problem without the need of integrating circuits or external reset leads.

The circuit makes use of the difference between operating threshold voltage levels of the two gates to produce an initializing pulse. When the power supply is switched on, the voltage at points A, B, and C rises at the same rate as the applied supply voltage. Neither gate will sink any current until its operating threshold is reached.

Because the operating threshold of the standard gate is lower than that of the Schmitt-trigger gate, the standard gate will respond first. When this gate's threshold is reached, its output goes to logic 0, clearing the storage element. And when the supply voltage reaches the higher operating threshold of the Schmitt trigger, this gate's output goes to logic 0, causing the standard gate to return to its normal operating state so that its output is again logic 1. The circuit, therefore, generates a pulse that can be used to initialize a logic system.

The width of the initializing pulse depends mainly on the power-supply rise time and the voltage difference between the operating thresholds of the two gates. Clearly, if the power-supply rise time is instantaneous, no pulse is generated. This undesirable situation can be avoided by adding an integrating circuit at point A, thereby guaranteeing a minimum width for the initializing pulse. Needless to say, the slower the power-supply rise time, the longer is the initializing pulse. (It should be noted that another pulse is generated when the power supply is turned off.) □



A free pulse. The threshold voltage difference between a regular TTL NAND gate and a Schmitt-trigger TTL NAND gate permits a pulse to be generated for initializing a TTL storage device. As the supply voltage rises, the regular gate changes state twice, producing an output pulse whose duration depends on power-supply rise time. The integrating circuit assures a certain minimum pulse width for the output.

Temperature limiting boosts regulator output current

by Mahendra J. Shah
University of Wisconsin, Space Science & Engineering Center, Madison, Wis.

The efficiency of a precision monolithic voltage regulator can be significantly improved by limiting the junction temperature of the regulator's internal current-limiting transistor.

Conventional current limiting severely restricts the regulator's peak and average output current capability. As an example, consider the 723-type regulator, which can supply an output voltage of 7 to 37 volts. This device has a maximum storage (junction) temperature of 150°, a maximum input/output voltage differential of 40 v, and a maximum load current of 150 milliamperes.

When the regulator's metal-can package is used without a heat sink, its internal power dissipation should be limited to 800 milliwatts at an ambient temperature of 25°C. If the input voltage to the regulator is 40 v, con-

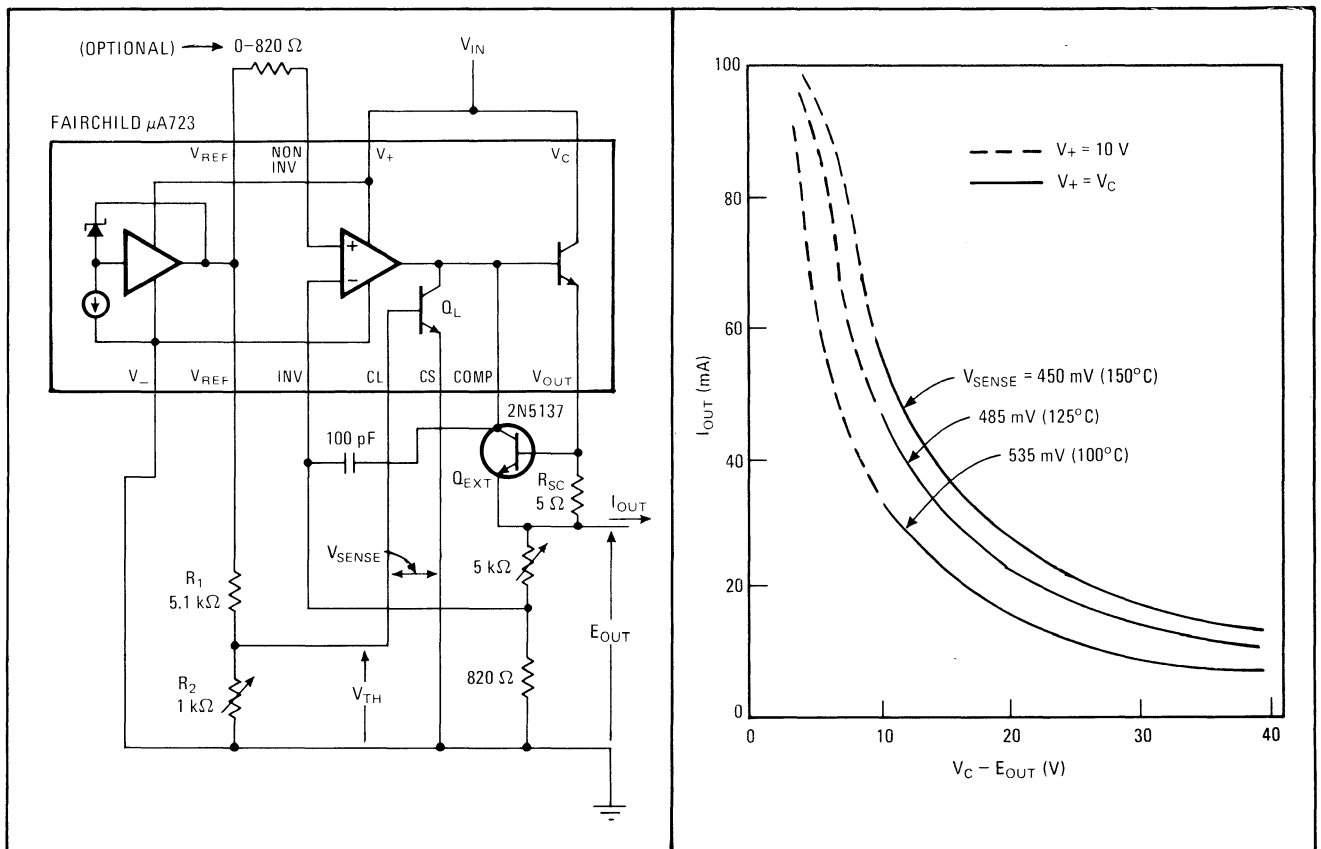
ventional current limiting places the worst-case current limit at 20 mA, or 800 mW/40 v. (The worst-case condition is an output short circuit to ground.) And a fold-back-current-limiting approach requires a limit knee setting of 24.2 mA, or 800 mW/(40 - 7) v.

Both of these approaches significantly limit the regulator's output current capability when the regulator must supply a load continuously at both intermediate and high output voltage levels, or when it must supply peak currents at any output voltage level. In contrast, temperature limiting protects the regulator from burn-out, while allowing it to provide the maximum possible output current (both continuous and pulsed), regardless of output voltage level, ambient temperature, and the amount of heat sinking.

Conveniently, the regulator's own current-limiting transistor, Q_L , can be used to implement this temperature limiting. The transistor's base-emitter junction, which has a temperature sensitivity of -1.8 millivolts/°C, can act as a temperature sensor for the regulator. And the collector terminal of transistor Q_L can be connected to limit the regulator's output current.

A stable voltage source is needed to bias Q_L 's base-emitter junction at the threshold voltage (V_{th}) that cor-

Better short-circuit protection. Current-limiting transistor Q_L of monolithic voltage regulator acts as an on-chip thermostat, controlling its own base-emitter junction temperature and, therefore, limiting regulator output current. The threshold bias voltage (V_b) of Q_L 's base-emitter junction is set to limit this junction's temperature to a value determined by Q_L 's sense voltage (V_{sense}).



responds to Q_L 's sense voltage (V_{sense}) for a given junction temperature. V_{sense} is the voltage required across Q_L 's base-emitter junction to implement output current limiting. Values for sense voltage, limit current, and junction temperature can be obtained from the data-sheet plot of the regulator's current-limiting characteristics as a function of junction temperature.

The threshold bias voltage is easily obtained from the regulator's internal voltage reference source and the voltage divider formed by resistors R_1 and R_2 . Some other regulators, like Motorola's MC1460, MC1560, MC1461, MC1561, MC1463, MC1563, MC1469, and MC1569, have a provision for junction-temperature limiting, but they require an external regulated voltage source.

When the actual junction temperature of transistor

Q_L is lower than the junction-temperature limit, Q_L 's base-emitter voltage is higher than the threshold bias voltage, so that Q_L is off. But when Q_L 's actual junction temperature rises to the junction-temperature limit, Q_L 's base-emitter voltage drops slightly below the threshold bias voltage, and Q_L turns on, limiting its maximum junction temperature by first limiting the regulator's output current.

The external current-limiting transistor, Q_{XT} and its associated resistor, R_{SC} , are needed to limit regulator output current below the 150-mA secondary breakdown limit of the regulator's internal output transistors. (The optional resistor can be included to minimize output voltage drift.) The graph shows the regulator's output current capability over the full range of input/output differential voltage for three sense-voltage settings. □

All-digital phase shifter handles 5-to-1 bandwidth

by Aleardo Salina
Siai Marchetti, Vergiate, Italy

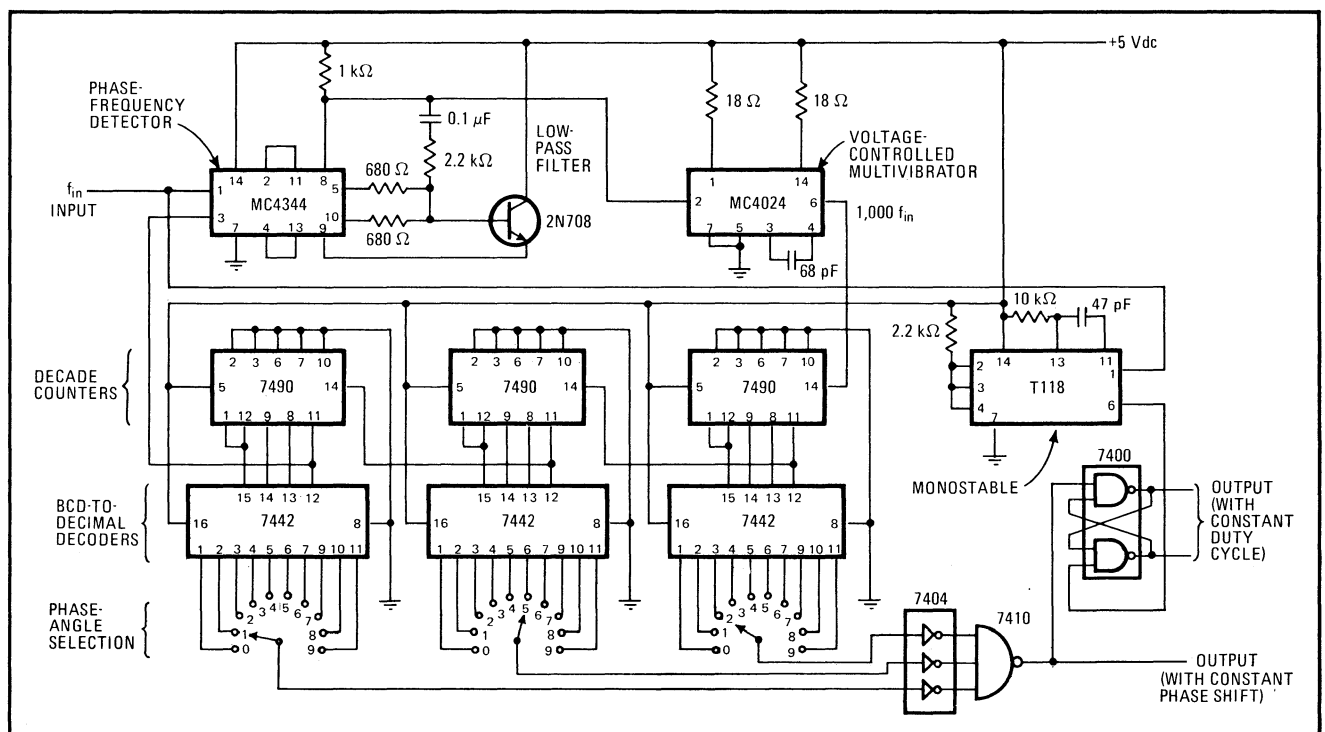
A digitally programmable phase-shift network can be made to maintain the phase shift at its output constant, even though the frequency at its input varies by as much as a factor of five. The circuit consists mainly of digital ICs, including its input-detector stage.

The desired phase shift is switch-selectable through a three-stage counter/decoder network. Any phase shift between 0° and 360° can be chosen. Here, the angle selected is divided into 1,000 bits, but a finer resolution can be obtained by increasing the number of decade counters.

For the component values indicated, the circuit's phase angle stays locked for input frequencies from 2 to 10 kilohertz. This operating frequency range can be shifted by changing the values of the low-pass filter components and the value of the timing capacitor for the voltage-controlled multivibrator.

The circuit also produces an output whose duty cycle remains constant. □

Locking phase digitally. Circuit produces the phase shift (between 0° and 360°) selected by the three switches. This digitally programmed phase angle does not change, although the input-signal frequency may vary from 2 to 10 kilohertz. The circuit's operating frequency can be changed by adjusting the low-pass filter and the timing of the voltage-controlled multivibrator. There is also a constant-duty-cycle output.



Voltage discriminator has 0.1-mV resolution

by Ryszard Bayer
 Institute of Nuclear Research, Swierk, Poland

Positive feedback permits a dual IC comparator to perform as a high-resolution voltage discriminator that can detect either positive or negative pulses having amplitudes ranging from a few millivolts to 5 volts. When driven from such low-impedance sources as operational amplifiers, this discriminator has a linearity of better than 0.03% and a voltage resolution of about 0.1 millivolt.

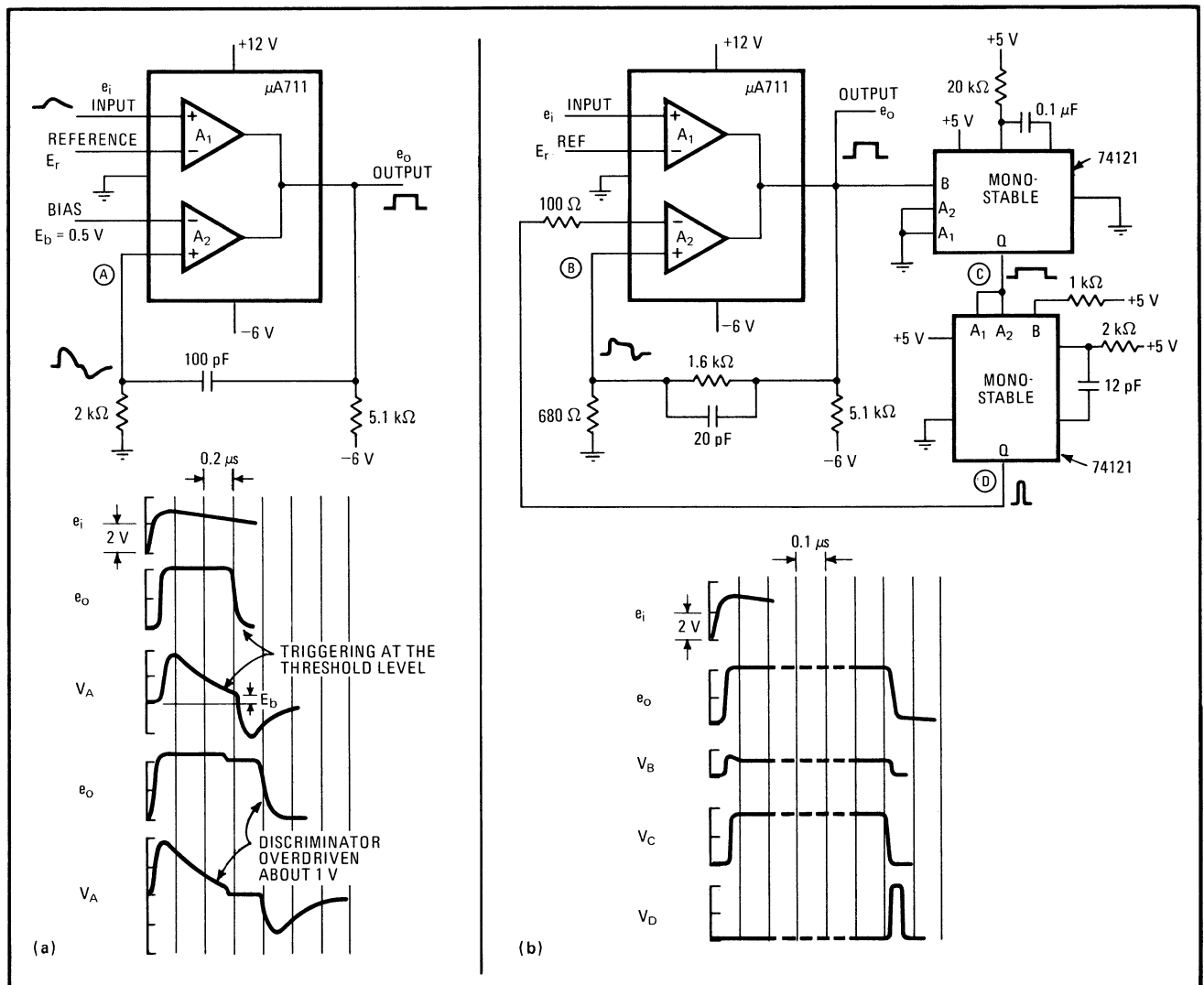
The input signal is compared with the reference voltage by comparator A_1 . The signal appearing at the moment of comparison of these two voltages is taken from the common output of both comparators and fed back

to the noninverting input of comparator A.

Because of this positive-feedback path, the discriminated signal is amplified considerably, reducing the amplifier's offset voltage and improving voltage resolution. Since the feedback signal is introduced to the noninverting input of comparator A^e , both inputs of comparator A_1 can be driven from low-impedance sources for better discriminator accuracy.

With capacitive feedback, as in circuit (a), the discriminator has only one stable state. With dc feedback, as in circuit (b), the discriminator becomes bistable. At the moment the input and reference signals are compared, the bistable discriminator is set to its high level. It can be reset by applying a second pulse to the inverting input of comparator A_2 . This second pulse can be applied after the first pulse has been terminated for a time that exceeds the duration of the first pulse minus the discrimination-level threshold. □

Discriminating comparators. Integrated dual comparators can differentiate between input-signal height and the reference-voltage level to within 0.1 millivolt. This high resolution is due to the positive feedback from the output to the noninverting input of comparator A_2 . Capacitive feedback (a) produces a unistable discriminator, while dc feedback (b) produces a bistable one that can be reset with a second input pulse.



No-ladder d-a converter works from one 5-V supply

by E. Insam
 Chelsea College, University of London, London, England

An 8-bit digital-to-analog converter that operates from a single positive 5-volt supply can be built without the usual front-end ladder network. This is done by creating a pseudo-random binary generator that is driven by a free-running multivibrator at a nominal clock frequency of approximately 5 megahertz. The multivibrator also provides the -5-v supply line for the converter's operational amplifier.

The output from the binary generator is compared (by subtraction) with the 8 input data bits. These can be in either a normal format or a two's-complement format, depending on the control input M. The carry output from the full adders is a pulse train whose mean

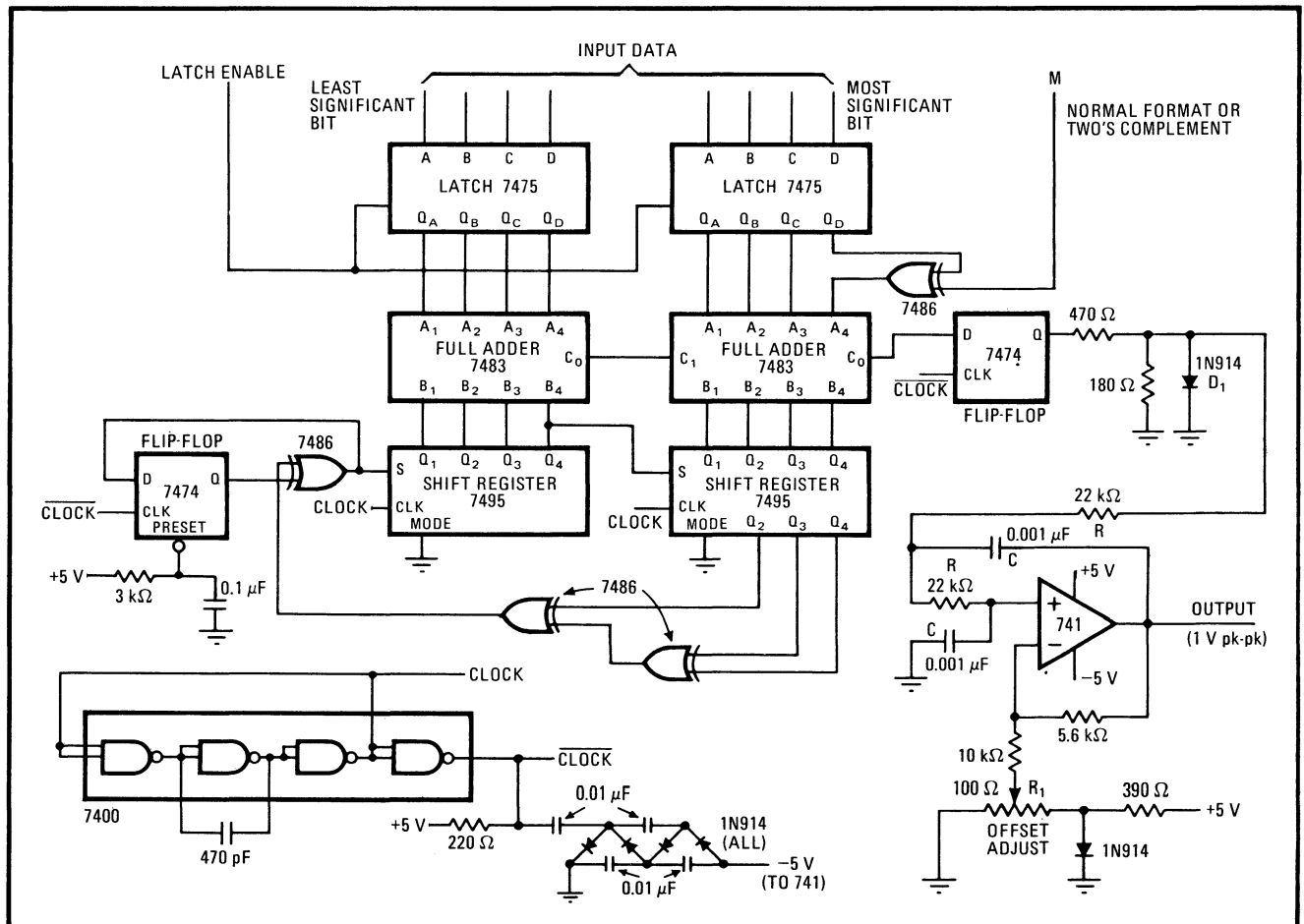
value is proportional to the input data and is clamped to about 0.6 v by diode D₁.

This pulse train is then fed to an active Butterworth low-pass filter formed by the op amp and its associated components. In the circuit given here, the gain of this stage is set at 1.59 to give the necessary filter-pole positions and to bring the peak-to-peak output amplitude of the converter to 1 v. Potentiometer R₁ controls the dc shift of the analog output.

The quantizing noise consists of harmonic multiples of the clock frequency divided by 255. In this case, the lowest harmonic occurs at around 20 kilohertz, which is beyond audibility. The cutoff frequency ($\omega = 1/RC$) of the Butterworth filter is around 7 kHz. The circuit's gain accuracy, which is not a major concern for audio work, depends only on diode D₁ and the closed-loop gain of the op amp.

The transistor-transistor-logic version of this d-a converter consumes around 300 milliamperes. If low power drain is an important design factor, complementary-MOS devices can readily be substituted, reducing the current consumption to around 40 mA. □

From digital to analog. Instead of the conventional ladder network followed by an op amp, this d-a converter employs a pseudo-random binary generator and an active low-pass filter. The generator's outputs and the 8 input data bits are subtracted in the full adders, resulting in a "carry" pulse train that drives the filter. Only one positive 5-volt supply is needed to power the entire circuit.



Dc restorer for video use offers ultra-stability

by Roland J. Turner
AEL Communications Corp., Lansdale, Pa.

A sample-and-hold technique, along with strong degenerative feedback, permits an active dc restorer to operate with very high stability over a wide temperature range. Restoration stability can be maintained to within 30 microvolts, even in the presence of a dc offset voltage as large as 100 millivolts.

The circuit is useful in radar applications, where it is often essential to peak-detect or integrate video signals relative to a stable dc reference. This is especially true if the video sensor contains diodes that have a temperature-dependent offset voltage.

The dc restoration must be performed without any temperature-induced offset voltage, since dc coupling must be preserved in the video processing (peak detection or integration) following dc restoration. Accurate signal detection, then, heavily depends on providing a stabilized dc restoration level. The video output signals must be independent of any thermal variations that may occur in the video detector and dc restorer.

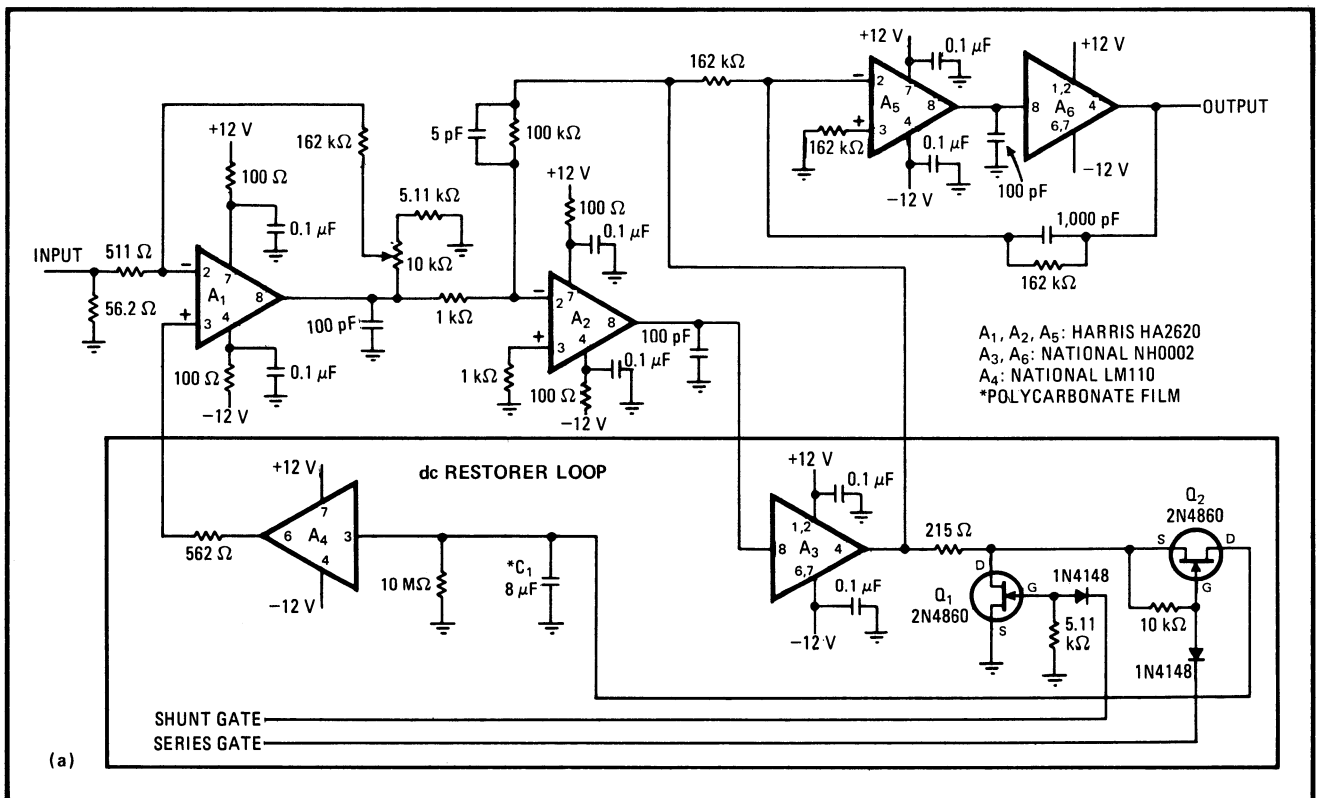
Conventionally, a dc restorer operates at relatively high signal levels and requires considerable video gain prior to dc restoration. Moreover, a dc restorer generally employs a temperature-compensated zener diode,

and two matched diodes to keep the dc restored level relatively constant over a wide temperature range. But even with the best matched diodes and the most stable temperature-compensated zener, the dc restored level cannot be made more stable than ± 10 mV over a 100°C temperature range. With the dc restorer shown here, however, stabilities of $30 \mu\text{V}$ can be established at extremely low video levels.

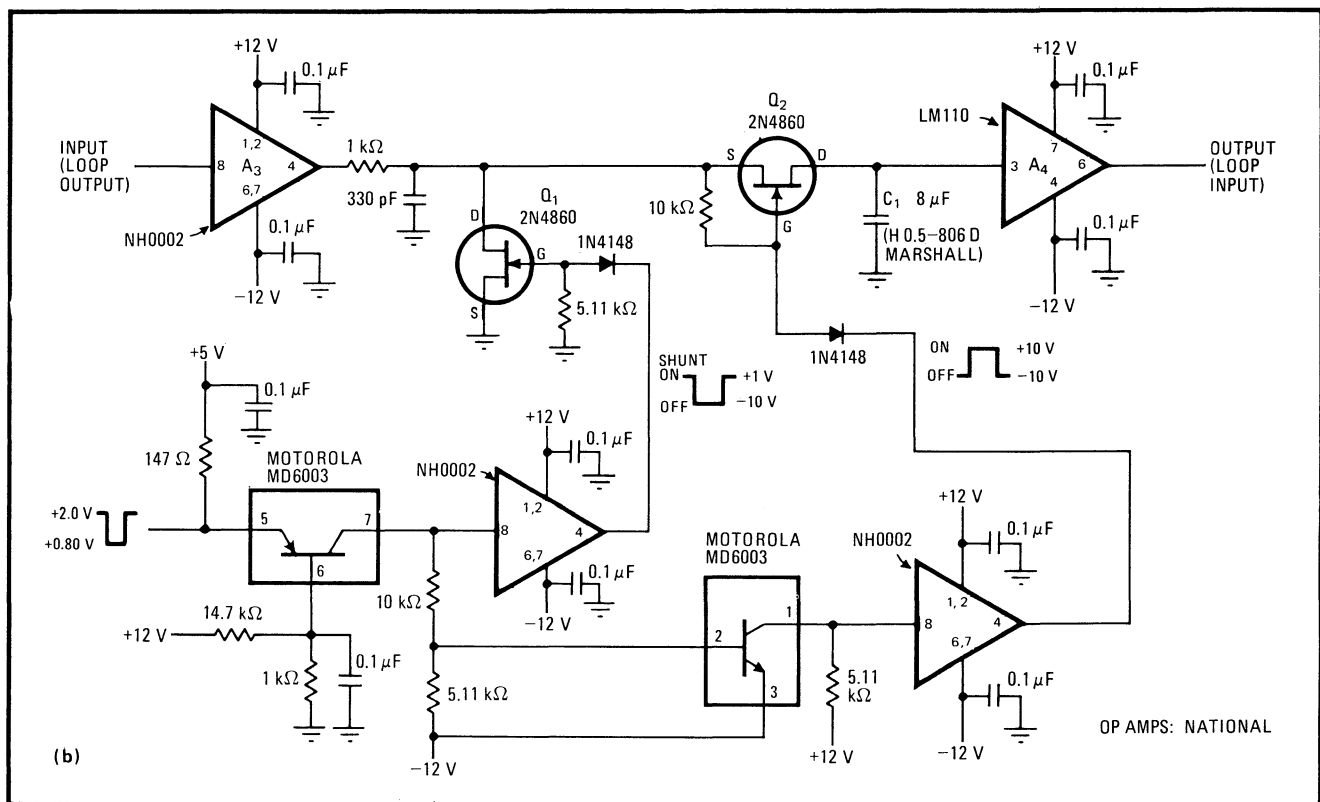
A complete video amplifier employing this improved dc restoration technique is drawn in (a). In this circuit's sample-and-hold scheme, the dc output of a dc-coupled amplifier is sampled over a 50-microsecond gating interval. It should be noted that dc coupling must be maintained from the input (sensor) through to the output integrator or peak detector. As a result, dc signal changes longer than the sensor's thermal time constant, which is typically less than 10 milliseconds, can be recognized as a valid signal/target by the peak detector or integrator.

The full schematic of the dc-restorer section of the video amplifier is given in (b). During the dc-restoration interval, the FET shunt gate, Q_1 , is open, while the FET series gate, Q_2 , is closed. During the gating interval, sampling capacitor C_1 , which is a highly temperature-stable polycarbonate-film capacitor, charges to the average noise level present at the output of amplifier A.

When the sampling gate is closed, the circuit's sampling process activates a degenerative-feedback loop that forces the average signal value at A_3 's output to approach the signal-noise level. In effect, the dc level at the noninverting terminal of input amplifier A_1 is forced to match the dc level at A_1 's inverting terminal to



Emphasizing stability. Dc restoration loop of video amplifier (a) allows the amplifier to match dc input levels to within 30 microvolts, in spite of widely varying temperatures. The sample-and-hold circuitry of the dc restorer loop is shown in (b). During the gating interval, which is 50 microseconds long, FET shunt gate Q_1 is off, FET series gate Q_2 is on, and capacitor C_1 (a temperature-stable unit) charges.



within 30 μV . During the signal processing interval, when shunt FET gate Q_1 is on and series FET gate Q_2 is off, the voltage across capacitor C_1 establishes an ultra-stable dc-restored level at the positive input to amplifier A_1 as a reference for detecting whatever video signals may be present at the negative input of A_1 .

To realize a high degree of dc-restoration stability within the gating aperture, it is essential to select op amps for amplifiers A_1 and A_2 that have fast slew rates. This is why Harris' type HA2620 op amp, which has a gain-bandwidth product of greater than 30 megahertz, is used for both A_1 and A_2 . Amplifier A_4 is a high-stability buffer that serves as a high-input-impedance load for the sampling capacitor, C_1 .

This active dc restorer can reduce a 100-mV dc offset at the sensor to an equivalent dc offset of less than 30 μV . And because of the low leakage of the sampling

gate, the stored charge on capacitor C_1 is not disturbed during the hold interval, even if a 10-v signal is present at the gate input.

The forward gains (80 decibels) of amplifiers A_1 , A_2 , and A_3 contribute to the degenerative-feedback loop during the dc restoration interval, forcing A_1 's positive input to follow the dc offset present at A_1 's negative (sensor) input. The circuit's integrating stage containing amplifiers A_5 and A_6 must be placed outside the dc-restoration loop, since the fast slew rate of the forward-control loop must be preserved during the dc restoration interval.

For the circuit to operate properly, the input-signal condition must be known during the dc-restoration interval. In radar systems, this time occurs between pulse transmission and signal reception; for television signals, this time occurs during the sync tip transmission. \square

Regulator for standby supply handles large load currents

by James Allen
Honeywell Inc., Aerospace Division, St. Petersburg, Fla.

A simple voltage regulator for a standby-power source can supply amperes of current at whatever voltage is required. Additionally, the circuit, which includes current-limiting and short-circuit protection (current foldback), can produce large current pulses.

There are many systems that require noninterruptible power sources—for example: gyro test stands involving long test sequences, volatile semiconductor memories, and computer systems or test systems where a power failure cannot be tolerated because it may destroy components or mean going through long start-up sequences.

If the primary dc supply fails, either because of internal malfunctions or because of some line disturbance that momentarily causes an interruption in its ac source, the standby power supply cuts in and continues to supply the necessary load current. Usually, the power source for this standby or backup supply is a bank of storage batteries. However, the voltage level provided by these storage batteries is not normally the voltage

level needed by the backup supply for the system.

The regulator in the figure offers ample voltage and current capability. And it can be conveniently and easily tailored to suit a specific application. (The figure also contains plots of the regulator's dc-output characteristic and pulse-current performance.)

The zener voltage of the zener diode determines the output voltage at which the regulator begins to conduct. Current limiting is provided by the combination of control transistor Q_1 and field-effect transistor Q_2 , which acts as a voltage-variable resistor. The current-limit level is set by the ratio of resistor R_1 to resistor R_2 :

$$I_{max} = 3.1[I + (R_1/R_2)] \text{ amperes}$$

The current foldback of the regulator is obtained through transistor Q_3 and resistor R_3 . The voltage level (V_f) at which foldback begins is determined by the ratio of resistor R_4 to resistor R_5 :

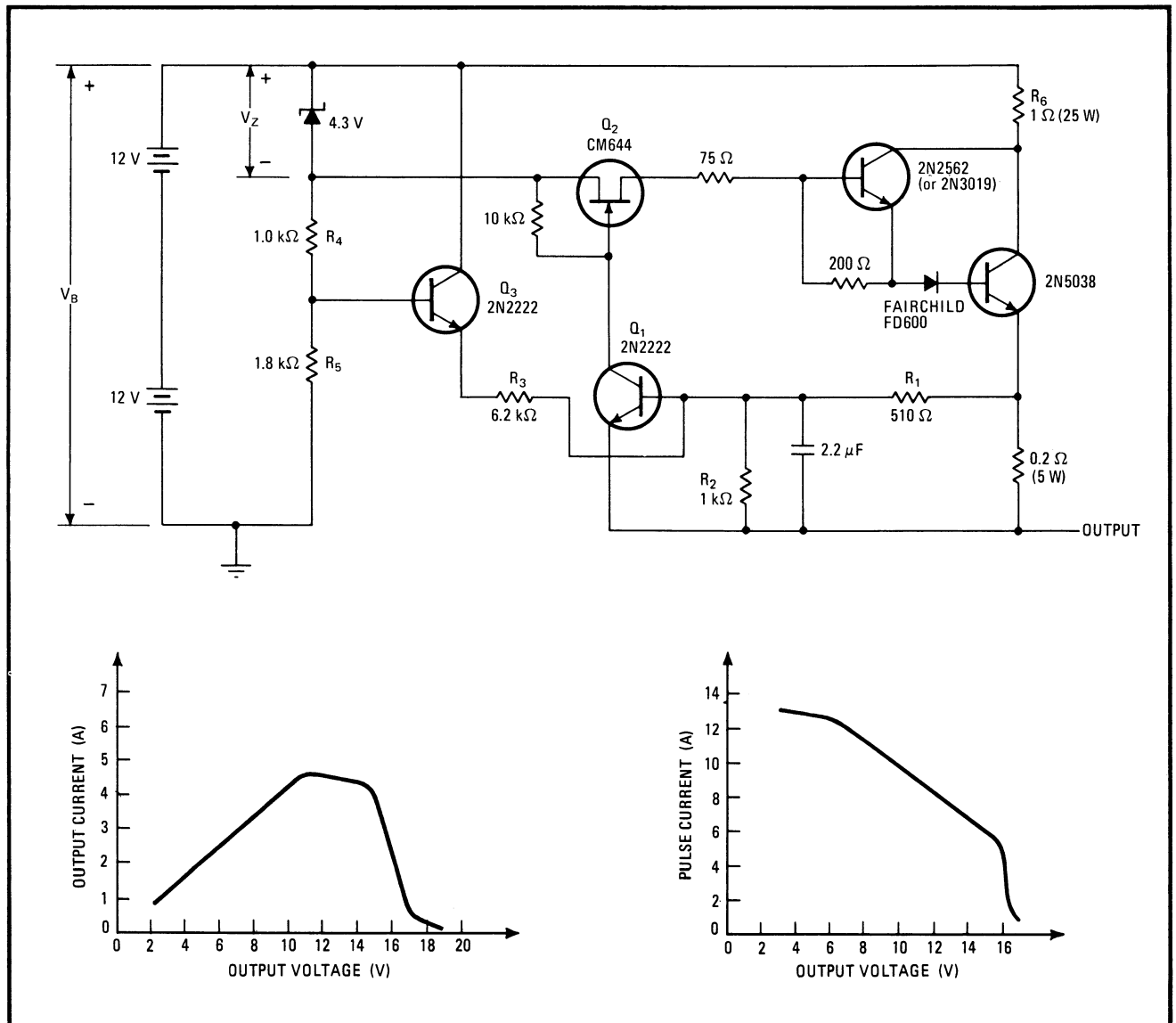
$$V_f = [R_5/(R_4 + R_5)](V_B - V_Z - 2V_{BE3} \text{ volts}$$

where V_B is battery voltage, V_Z is zener voltage, and V_{BE3} is base-emitter voltage of Q_3 . The slope of the current foldback curve is set by the ratio of R_1 and R_3 .

$$\Delta V/\Delta I = 0.2R_3/R_1 \text{ V/A}$$

Since the regulator will normally be operating into a large-capacity load that will probably exhibit large dv/dt variations initially, it should be able to supply a significantly larger amount of charge during turn-on. This pulse current capability is provided by the capacitor, which delays the feedback current so that transistor Q_1 does not conduct for several hundred microseconds. The magnitude of this pulse current is determined by the value of resistor R_6 . □

Watchdog backup power source. Readily adaptable regulated standby-power supply can produce several amperes of current at the desired voltage level, as shown by its output characteristic. The circuit's pulse-current capability (also plotted) is ample and able to satisfy large initial turn-on load current demands. Both current limiting and current foldback are included to protect the regulator circuit.



Multiplexer adds efficiency to 32-channel telephone system

Analog signals are time-division multiplexed by recently developed integrated circuits in a two-level switching scheme; the technique promises to add speed and efficiency to digital telephone systems

by John A. Roberts* and J.O.M. Jenkins, Siliconix Ltd., Swansea, England

□ Time-division multiplexing has gained wide acceptance in recent years as a means of combining multiple telephone channels on wire-pair transmission lines that previously accommodated only one channel. Combined with pulse-code-modulation (PCM) circuitry to convert the sampled signals to a digital format, the multiplexing techniques have generally reduced size, power consumption, and costs of plant equipment.

To achieve minimum signal loss and distortion in

*Now with Microsystems International Ltd., Ottawa, Canada

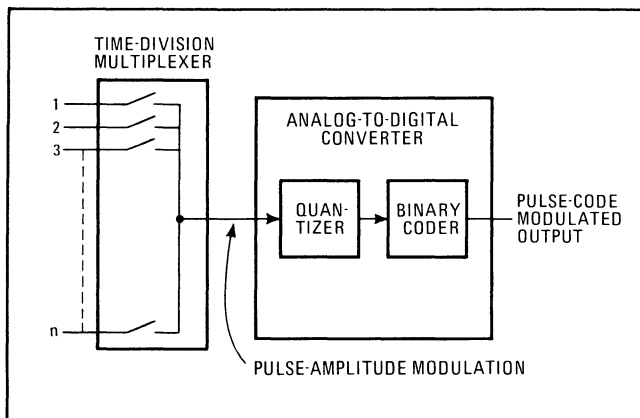
such systems, much effort has been directed toward building multiplexers that switch from channel to channel with minimum output rise and fall times. Such a multiplexer design recently built and tested provides 150-nanosecond switching time, an order of magnitude faster than presently available circuits.

This high-speed switching is achieved by applying biphasic control logic to a two-level multiplexer arrangement that takes advantage of the fast rise times and the break-before-make action of newly developed integrated-circuit multiplexers.

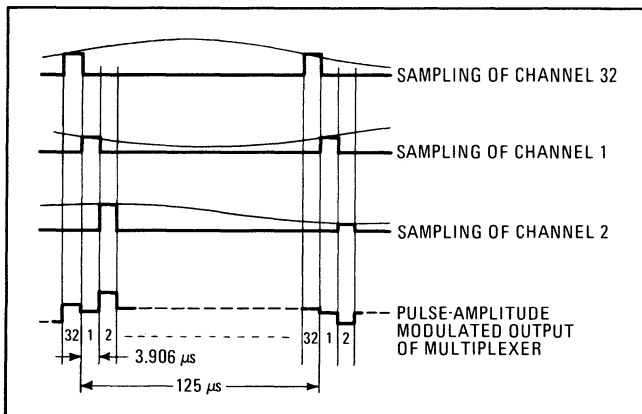
Telephone system requirements

A generalized system used to time-division multiplex voice signals is shown in Fig. 1. After the signals on each of analog channels have been sampled, each sample is quantized and coded into a PCM format. The new design focuses on the analog multiplexer, which feeds the analog-to-digital converter.

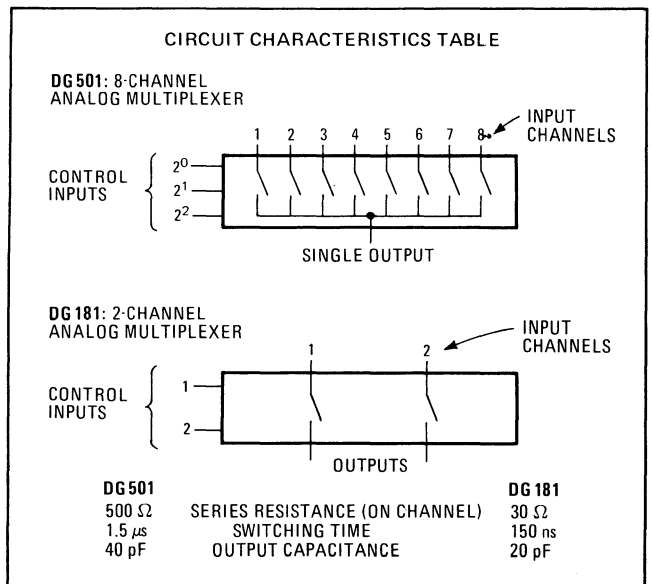
The sampling rate for each of the incoming channels is determined by the desired bandwidth of the voice signals being sampled, while sampling dwell time is fixed by the number of channels that must be sampled. Nyquist's sampling theory^{1,2} states that any transmitted waveform that is band-limited to a maximum frequency of f_L can be accurately reconstructed from periodic sam-

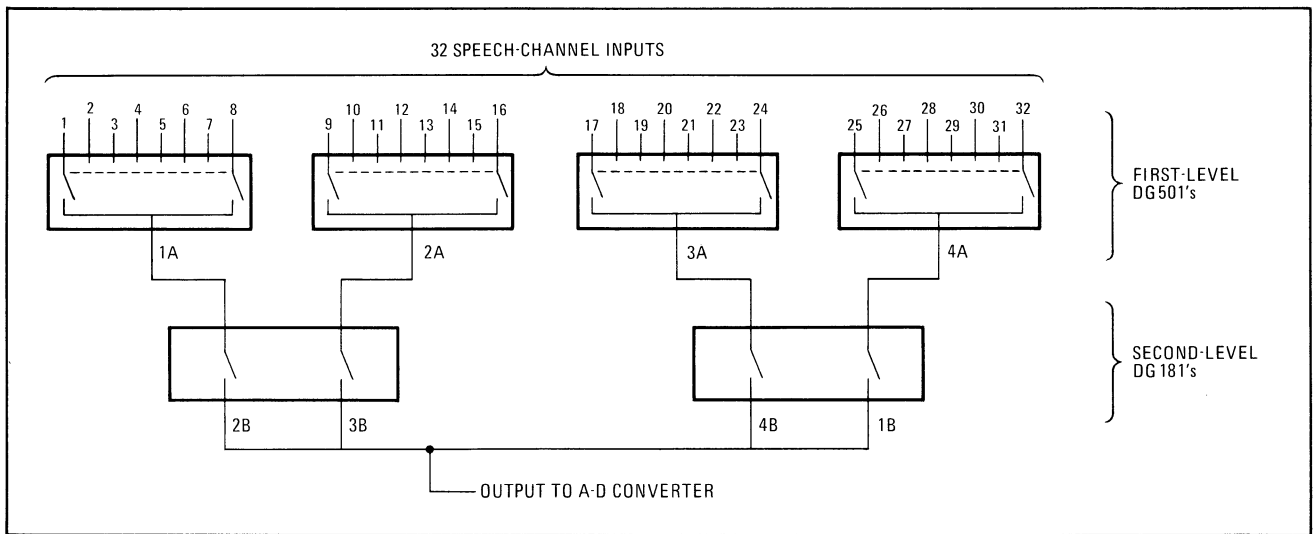


1. Telephone's answer. Problems in overcrowding of wire-pair telephone-transmission lines are lessened by using analog time-division multiplexers followed by a-d converters.



2. Tight fit. For accurate reconstruction of a 3.3-kHz telephone signal, it must be sampled at a rate of about 8 kHz, or once every 125 μ s. The hierarchy of today's telephone system makes it highly desirable to multiplex 32 speech channels during this period.





3. Two-level multiplexing. Output-node capacitance is significantly reduced when a second level of multiplexers is added. Interchannel switching time, however, is still determined primarily by the speed of the first-level switches.

ples taken at a rate as slow as $2f_L$.

In practice, however, filters do not provide ideal cut-off at f_L , and a somewhat higher sampling rate must be tolerated. For example, to achieve less than 1% error in reconstruction accuracy, the sampling rate must be at least twice the frequency at which the unwanted signals above cutoff are reduced by 40 dB.^{2,3} Thus, to relax difficult filtering requirements at the input-to-sampling circuitry, a voice bandwidth that is nominally limited to about 3.3 kHz is usually sampled at an 8-kHz rate, or once every 125 μ s.

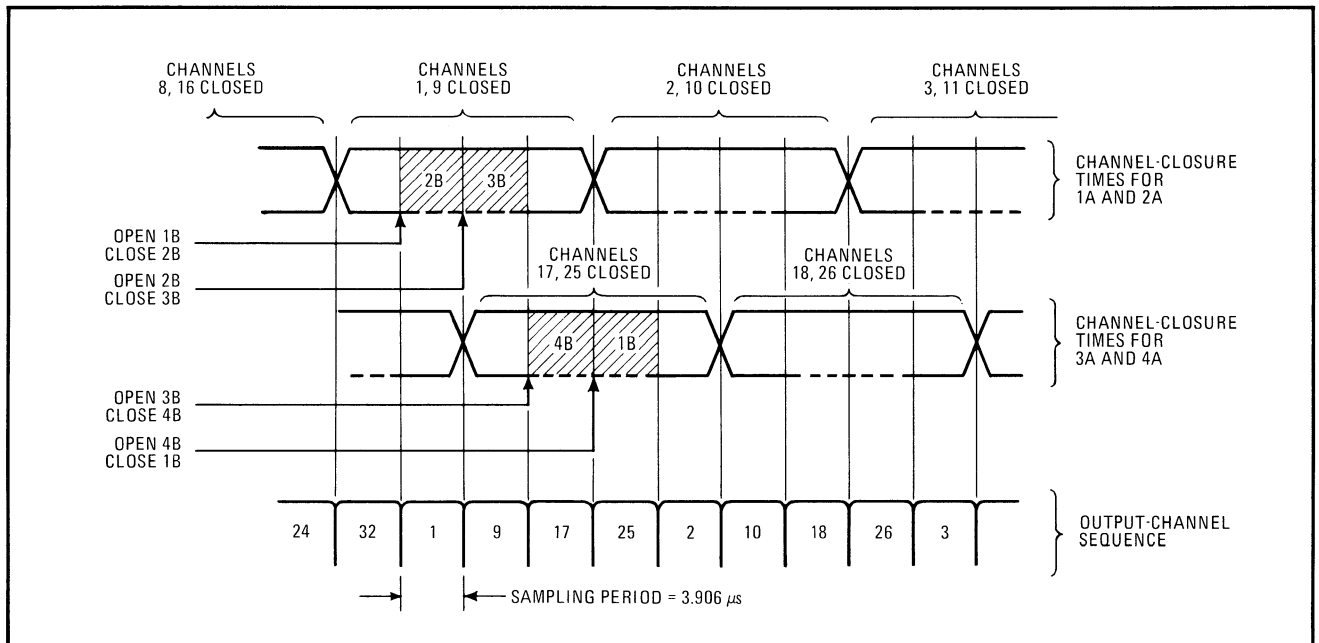
Single-level multiplexers

The standard configurations of today's telephone systems dictate that a fundamental group of 32 channels be multiplexed onto one line. Therefore, with a sample frame time of 125 μ s, each of 32 multiplexed channels is

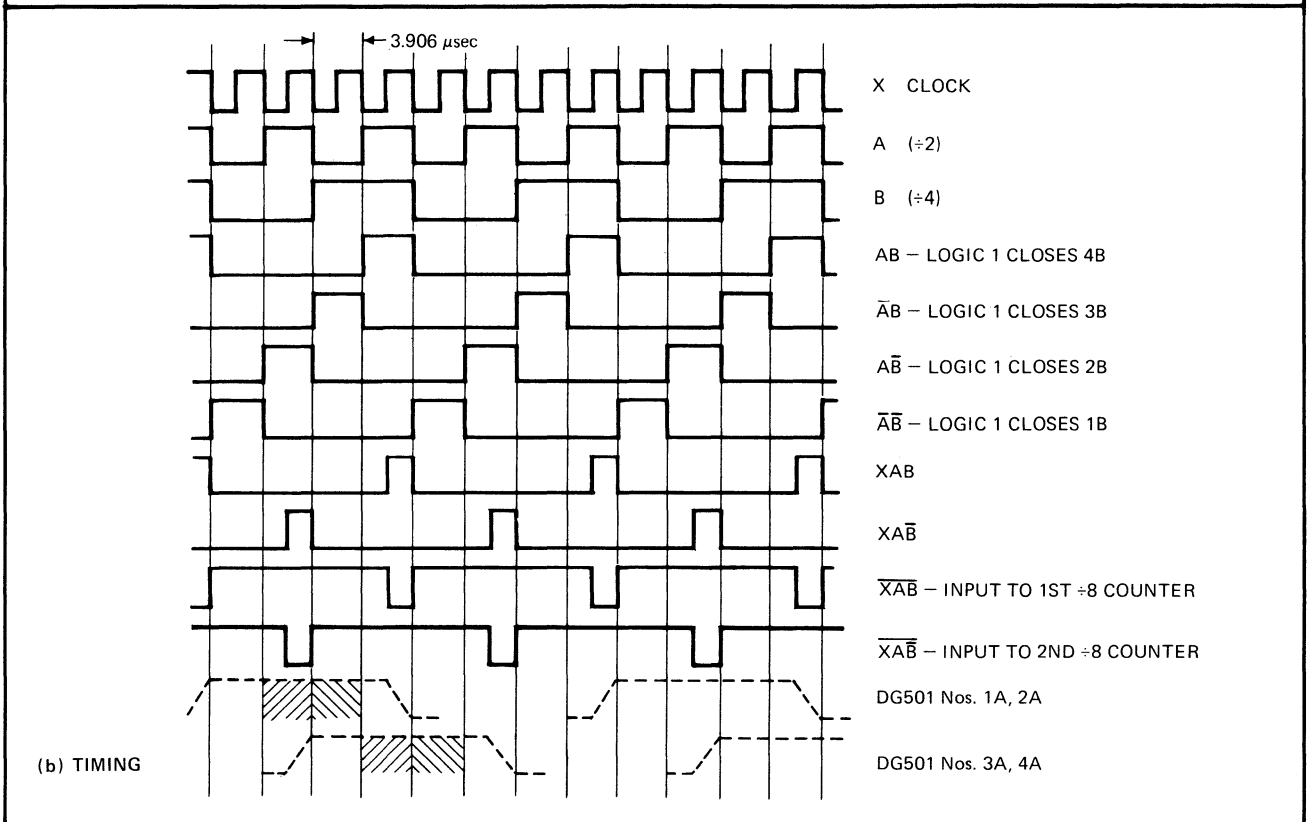
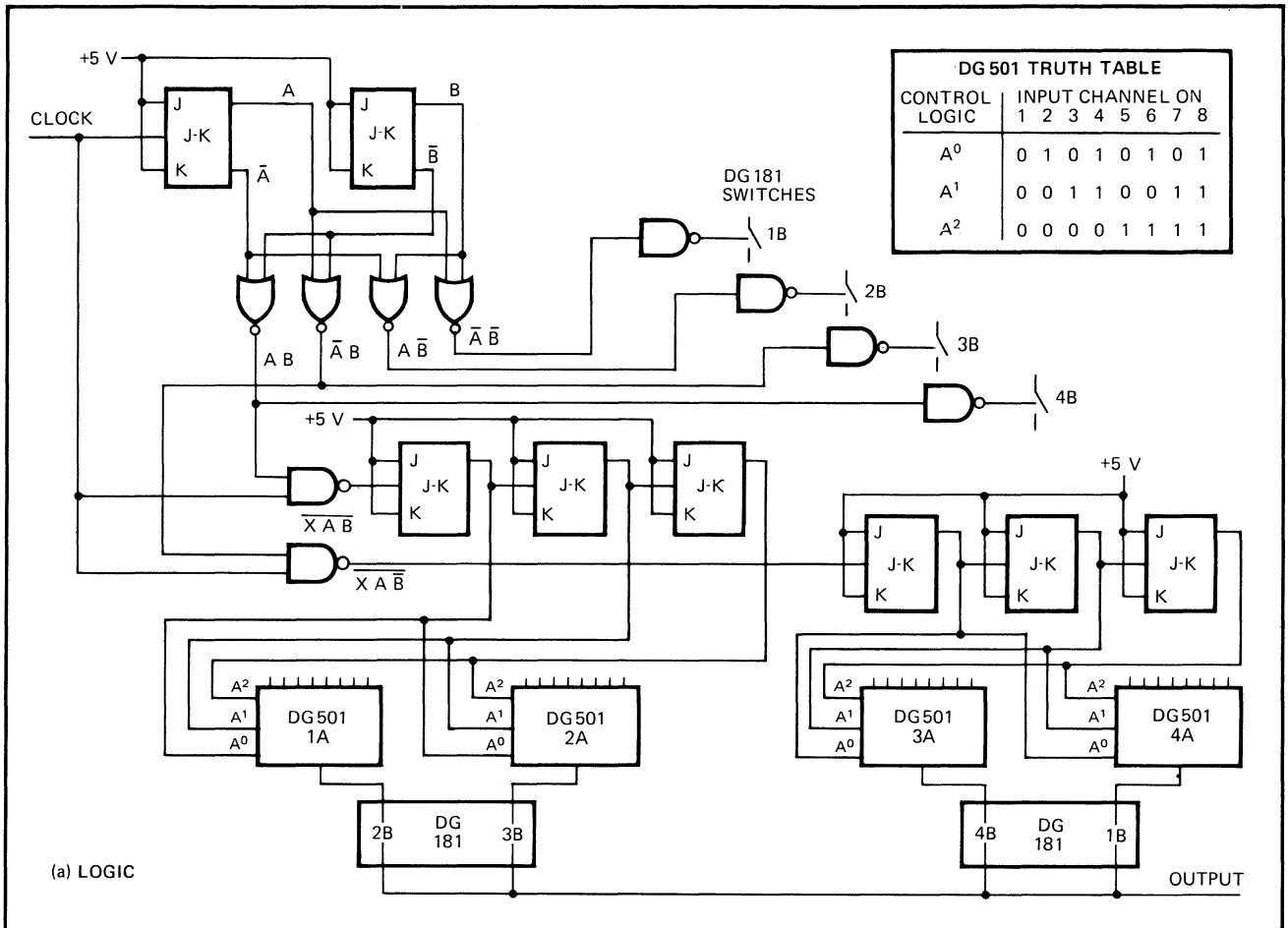
sampled for 125/32, or 3.906 μ s, as Fig. 2 indicates.

Conventional multiplexing networks can be implemented with either discrete components or integrated circuits, such as the Siliconix DG501 (see table). This circuit multiplexes eight input channels with a switching time between channels of 1 to 2 μ s. A 32-channel multiplexer is constructed simply by paralleling four DG501s. Thus, in single-level switching, each of the 32 analog input channels is multiplexed through a single switching bank.

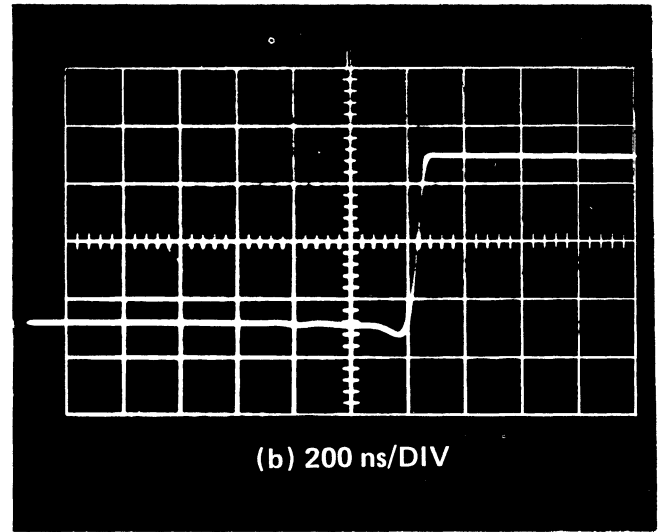
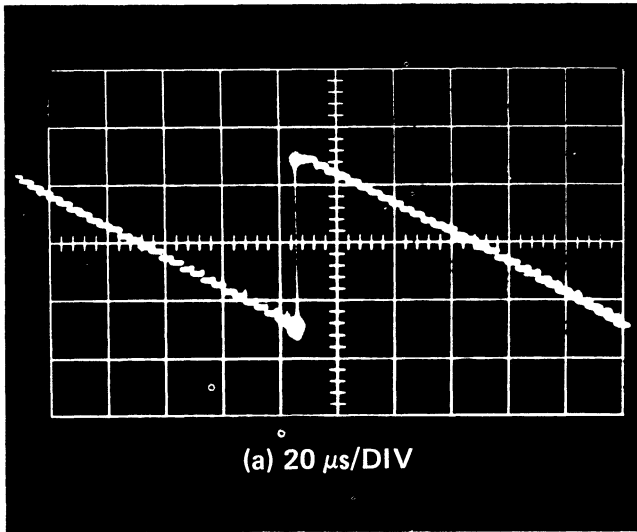
The problem with such a system stems from the relatively slow 1-2- μ s switching times between channels. Depending on the design of the particular multiplexer, there can either be an overlap between sampling pulses, which leads to crosstalk between channels, or a large separation between samples, which reduces the sampling time of a particular channel. The reduced



4. Phase II timing. By adding two-phase control logic to the two-level multiplexer of Fig. 3, the full advantage of the 150-ns switching speed of the DG181 circuits is realized. Channel numbers correspond with those in Fig. 3.



5. Logic hardware. TTL control circuits (a) implement timing (b) required in two-phase, two-level multiplexing system. First-level DG501 switches are MOS circuits, and J-FET technology gives the faster switching times needed in the DG181 second-level switches.



6. Quick switch. Thirty-two dc levels are sampled in a prototype multiplexer to demonstrate switching speed of the two-level two-phase design. Largest single transition, from -3 to $+3$ volts, is expanded in the lower trace. Vertical scale for both traces: 2 V per division.

sampling time results in lower multiplexer efficiency.

Added to the $1\text{--}2\text{-}\mu\text{s}$ switching time is a delay associated with the increased output-node capacitance when multiple channels are combined. For four DG501s (32 channels), the added delay is about 200 ns. These delays further reduce the effective sampling time and bring some uncertainty into the timing strobe for the a-d converter. The node-capacitance problem can be eased to some extent by a high-performance sample-and-hold circuit between the multiplexer and the a-d converter. However, the $1\text{--}2\text{-}\mu\text{s}$ switching times remain, and this problem becomes acute for signals obtained from sources with output impedances of 2 kilohms and above.

Two-level multiplexing

System-response time can be improved by reducing the output-node capacitance. This is achieved by using a two-level multiplexing system as shown in Fig. 3.⁴ Here, circuits with lower output capacitance (such as the DG181, with performance shown in the table) are placed in the second multiplexing level, which feeds the a-d converter.

The DG181 circuits can switch at a speed of 150 ns. The full advantages of these speeds, however, are not realized, since interchannel sampling time is still limited by the $1\text{--}2\text{-}\mu\text{s}$ rise times of the DG501s.

A timing sequence that makes maximum use of the switching rise times of the DG181s (and therefore results in extremely high sampling efficiency) can be achieved by applying control logic to the two-level multiplexer in a manner which will give the sampling sequence shown in Fig. 4. The faster switching speed and the break-before-make action of the DG181 virtually removes the possibility of overlap.

The problems caused by the relatively slow switching time of the DG501 are eliminated by ensuring that the first channels of multiplexer switches 1A and 2A (Fig. 3) are already fully closed when 2B and 3B, respectively, are closed, and that the first channels of switches 3A and 4A are fully closed when 4B and 1B, respectively, are closed. This sequence is then repeated for each of

the eight channels of the DG501s, and the complete cycle is again repeated.

Two-phase control logic

The timing requirement and logic-control layout for the complete circuit are shown in Figs. 5a and 5b. Waveforms A and B are obtained from the input clock waveform by an asynchronous divider. The A and B waveforms are combined to give AB , $A\bar{B}$, $\bar{A}B$ and $\bar{A}\bar{B}$ which are needed to close the DG181 gates sequentially. Functions XAB and $X\bar{A}\bar{B}$ then clock two three-bit asynchronous counters. A delay of two clock periods exists between XAB and $X\bar{A}\bar{B}$ so that the count sequence applied to the second and third multiplexer is suitably delayed.

A prototype multiplexer with two-phase control logic has been constructed and successfully tested. Series 7400 TTL circuitry is used to implement the timing and control logic. First-level DG501 switches are MOS circuits, while J-FET technology gives the faster switching times needed in the DG181 second-level switches.

To simulate all 32 analog inputs to the multiplexer, a voltage-divider network of series resistors is connected across a ± 3 -volt supply. Thus, 32 dc voltage levels are consecutively tapped off the network and applied to the multiplexer input. The multiplexer output is displayed on the oscilloscope, as shown in Fig. 6a. As can be seen, the largest transition is from -3 to $+3$ v. In Fig. 6b, this 6-v transition is demonstrated as being accomplished in less than 100 ns.

If low-power TTL or diode-transistor logic is used in the control circuits, synchronous counters may be necessary to eliminate cumulative flip-flop delays. Although the system shown is designed for negative-edge-triggered J-K flip-flops, the circuitry can be rearranged quite simply for almost any bistable logic element. \square

REFERENCES

1. Schwartz, M., "Information Transmission Modulation and Noise," 2nd ed., p. 174, McGraw-Hill Book Co., 1970.
2. Shannon, C., "A Mathematical Theory of Communication," Bell System Technical Journal, pp. 379-423, July 1948 and pp. 623-656, October 1948.
3. English, M., "Multiplex Systems," Electronic Products, pp. 28-31, May 1969.
4. Yoder, D., "Two-Level Multiplexing for Data-Acquisition Systems," pp. 67-72, EEE, July 1970.

An easy way to design complex program controllers

With less than a handful of functional integrated circuits, an engineer can use a general method to readily put together a logic program controller to direct even the most involved operations

by Charles L. Richards, *Seaco Computer Displays Inc., Garland, Texas**

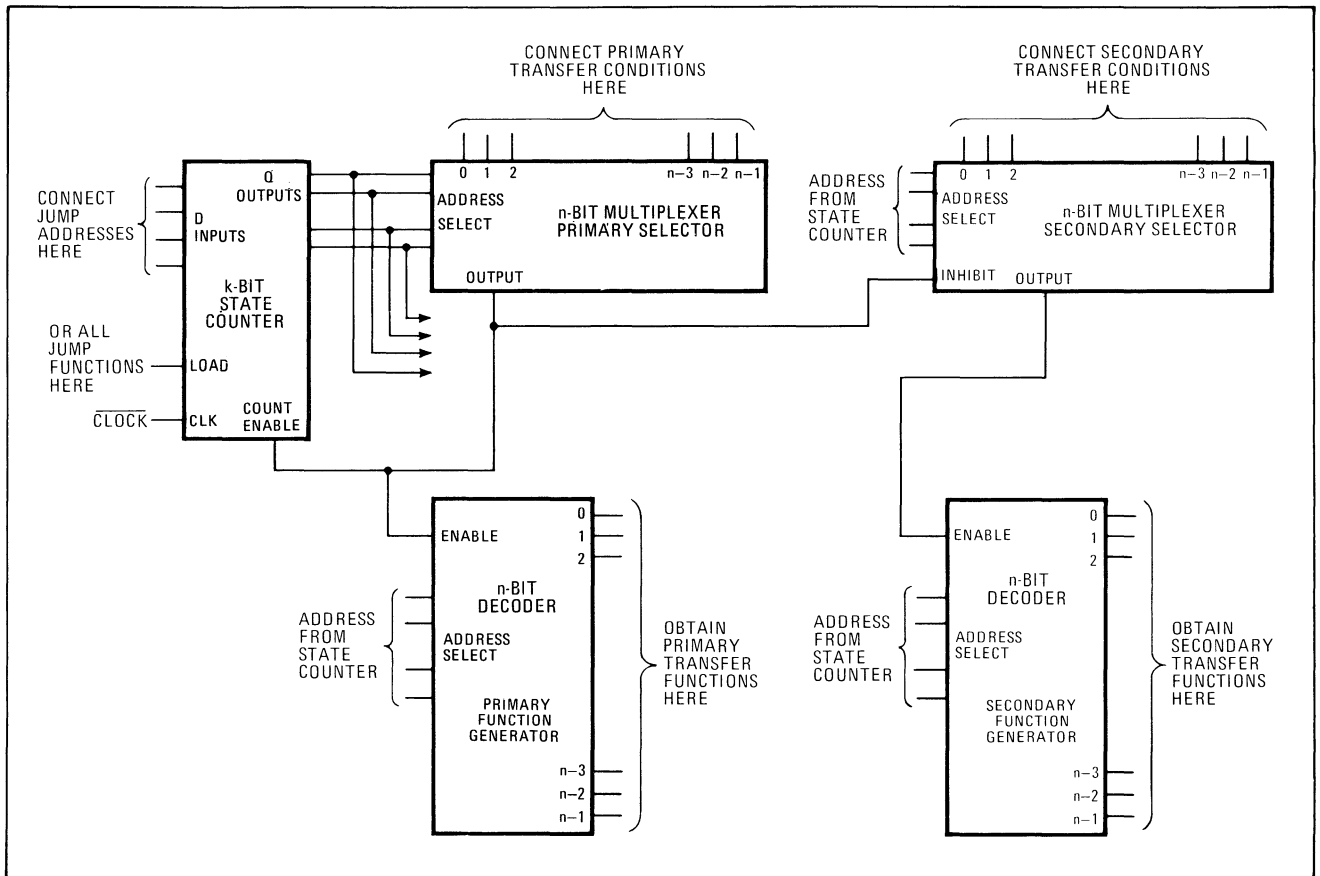
□ When an electronics engineer needs to design a complicated program controller, he may well experience a sinking feeling—it could mean a return to the textbooks to relearn the techniques of transfer tables, combinational and sequential logic, and component minimization. But a new general design method relieves the engineer of these burdens and allows him to configure and prototype even an extremely complex logic controller with a minimum of effort, time, and cost.

What's more, the generalized approach applies not only to straightforward sequential controllers, but also those that implement nonsequential YES-NO and multiple-choice decisions. That is, a controller can be made

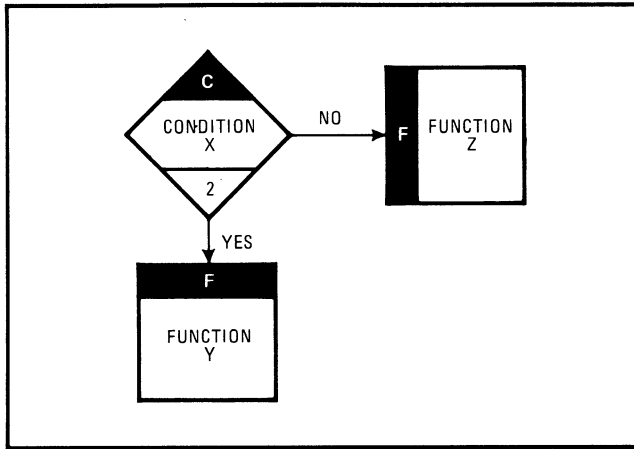
to index one state (or step) at a time, or to jump forward or backward to any predetermined state, or to choose which input condition out of many in the same state is to cause it to either index or jump.

In fact, the method is so easy to learn and apply that an engineer using it for the first time was able to design

1. Key logic elements. The state counter, multiplexer, and decoder, in color, are the main devices needed to produce a sequential controller that indexes from one step to the next. Adding secondary devices permits both nonsequential and priority control actions.



*Now with Texas Instruments Incorporated, Dallas, Texas



2. Transfers defined. Diamond denotes transfer condition, while rectangle denotes transfer function. One function is the action initiated by a transfer condition of YES, while a transfer condition of NO can initiate the other transfer function.

and prototype a controller involving 54 different states, with many states having five decision levels. The controller required 178 integrated circuits, had no logic errors, and worked perfectly the first time power was applied.

The three integrated circuits shown in color in Fig. 1 form the kernel of the logic-program controller. These primary devices are a k-bit state (or step) counter, an n-bit multiplexer, and an n-bit decoder. Here, n, the number of controller states, equals 2^k . For an eight-state controller, the three IC devices in plastic dual in-line packages cost about \$12, even when bought at their maximum, single-unit prices.

By adding another multiplexer and decoder, shown at the right of Fig. 1, to handle secondary input conditions, the controller can be made to perform condition-priority and nonsequential—or jump—operations. Appropriate jump addresses are fed back to the primary state counter through AND and NAND gates. More complicated program control can be obtained simply by adding more multiplexers and decoders.

Flow diagram tells all

The design process starts with a statement relating the controller's inputs to the output actions to be initiated by the inputs. The sequence of events can be represented by a flow diagram of the individual states in the over-all program. The diagram can be readily converted to a group of logic-state equations, which then clearly tell how to connect the inputs and outputs, including address jumps.

To explain how the generalized controller can be applied to three applications of varying complexity, it is necessary to define the terms transfer condition and transfer function. These are shown symbolically as the diamond and square in Fig. 2.

The diamond-shaped box represents the transfer condition, which concerns a YES or NO decision. The number in a diamond is the state (or step) number for that transfer condition. The transfer condition can be implemented physically by such two-state devices as a thermostat switch, a flip-flop, or a pulse.

The transfer function, denoted by the rectangles in

Fig. 2, is an action that is started or stopped by the transfer condition. As examples, the transfer function can gate a digital counter or start a motor. As shown, a YES transfer condition initiates one transfer function and a NO another transfer function.

Furthermore, depending on the controller's application, the transfer conditions can be either independent of or dependent on the transfer functions. In a dependent case, for example, the transfer condition might trigger a transfer function that starts a count of 1,000 events. The occurrence of the 1,000th count then serves as the next transfer condition. In an independent case, the next transfer condition might be an input from a timer occurring 500 milliseconds after the count starts, whether or not the count has reached 1,000.

1. Designing an eight-state sequence controller

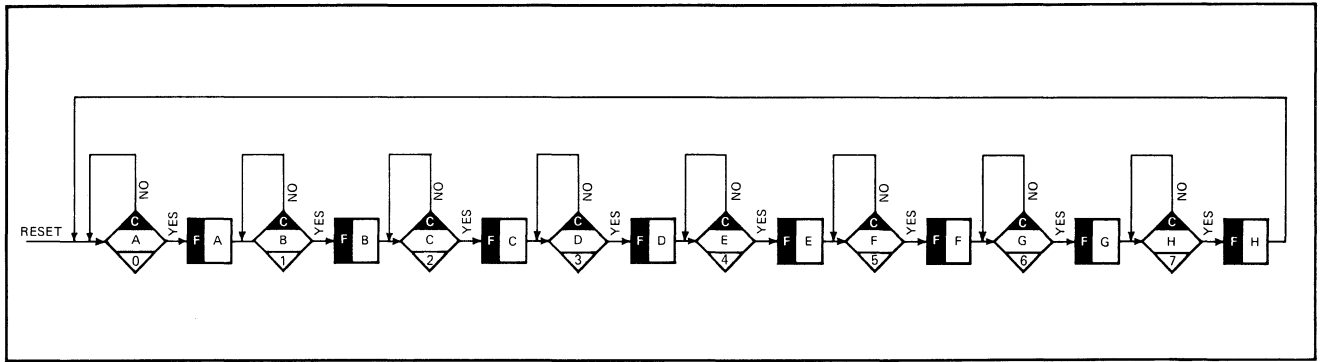
Probably the simplest program controller is one that sequences from one step to the next. Figure 3 contains the flow diagram for an eight-state sequence controller. Transfer functions are not required from any NO conditions, so NO-outputs are simply symbolically looped back as a condition input. The corresponding logic equations are:

- FUNCTION A = (STATE 0) (CONDITION A) Δ
- FUNCTION B = (STATE 1) (CONDITION B) Δ
- FUNCTION C = (STATE 2) (CONDITION C) Δ
- FUNCTION D = (STATE 3) (CONDITION D) Δ
- FUNCTION E = (STATE 4) (CONDITION E) Δ
- FUNCTION F = (STATE 5) (CONDITION F) Δ
- FUNCTION G = (STATE 6) (CONDITION G) Δ
- FUNCTION H = (STATE 7) (CONDITION H) Δ

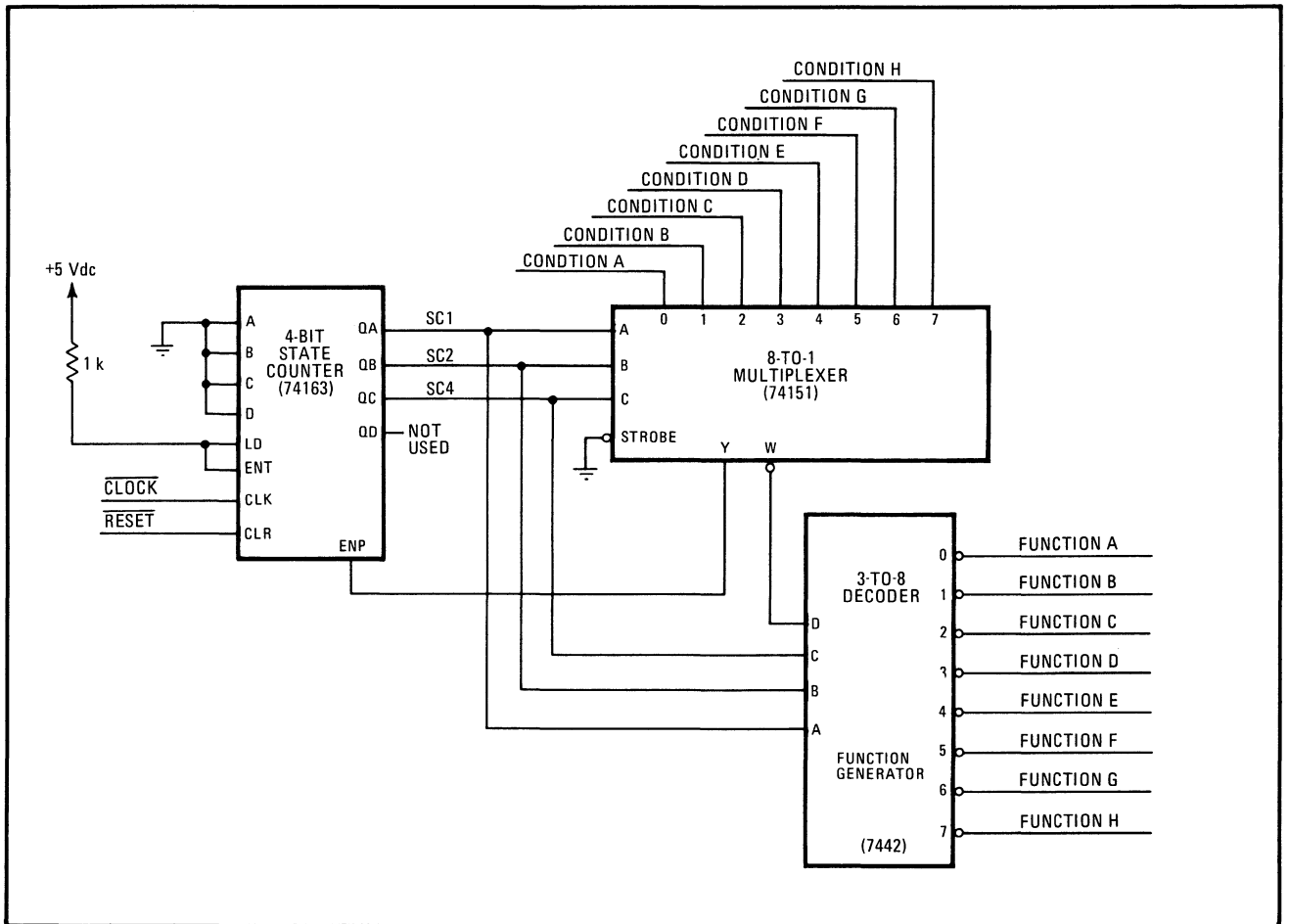
In logic convention, the product of two terms means that an output will occur TRUE when each term is TRUE. That is, for example, FUNCTION A becomes TRUE when both STATE 0 and CONDITION A are TRUE. Thus, the sequence of events is for the controller to remain TRUE in STATE 0 until CONDITION A becomes TRUE, at which point the controller initiates FUNCTION A and steps to STATE 1. Then the controller remains TRUE in STATE 1 until CONDITION B becomes TRUE, initiates FUNCTION B, and steps to STATE 3. When the controller reaches STATE 7, it remains there until CONDITION H becomes TRUE, initiates FUNCTION H, and steps to STATE 0—ready for a new cycle. In the equations above, the delta denotes on increment, or step, to the next state.

This eight-state sequence uses commercial integrated circuits. As shown in Fig. 4, the state counter is a type 74163 four-bit counter. But only three bits are used in this application, since $k = 3$ provides the eight state addresses, binary 000 to 111, corresponding to the 0 to 7 states. The counter's outputs address the 8-to-1 multiplexer (type 74151) to select the corresponding transfer condition and address the 3-to-8 decoder (type 7442) to select the corresponding output transfer function.

For example, when the counter in Fig. 4 outputs 101, the counter thus simultaneously addresses STATE 5. That is, it addresses CONDITION F of the multiplexer and FUNCTION F at the decoder.



3. Flow diagram. Succession of transfer conditions and transfer functions represents the actions needed for the particular application. Here the task is simple sequence control, in which the controller indexes from one step to the next in prescribed order.

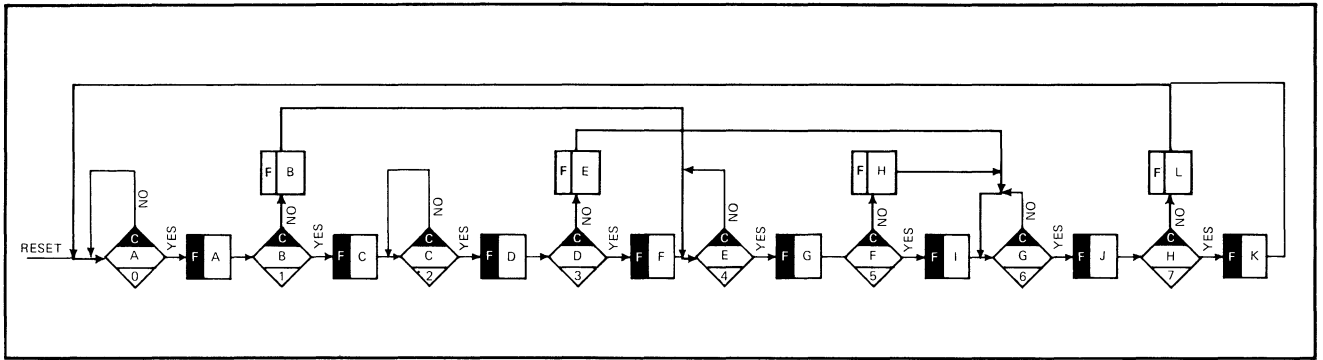


4. Sequence controller. In a step-by-step sequence controller, which can be implemented with as few as three IC packages, the multiplexer's Y-output enables the counter to increment the state address for the multiplexer and decoder to yield the required function.

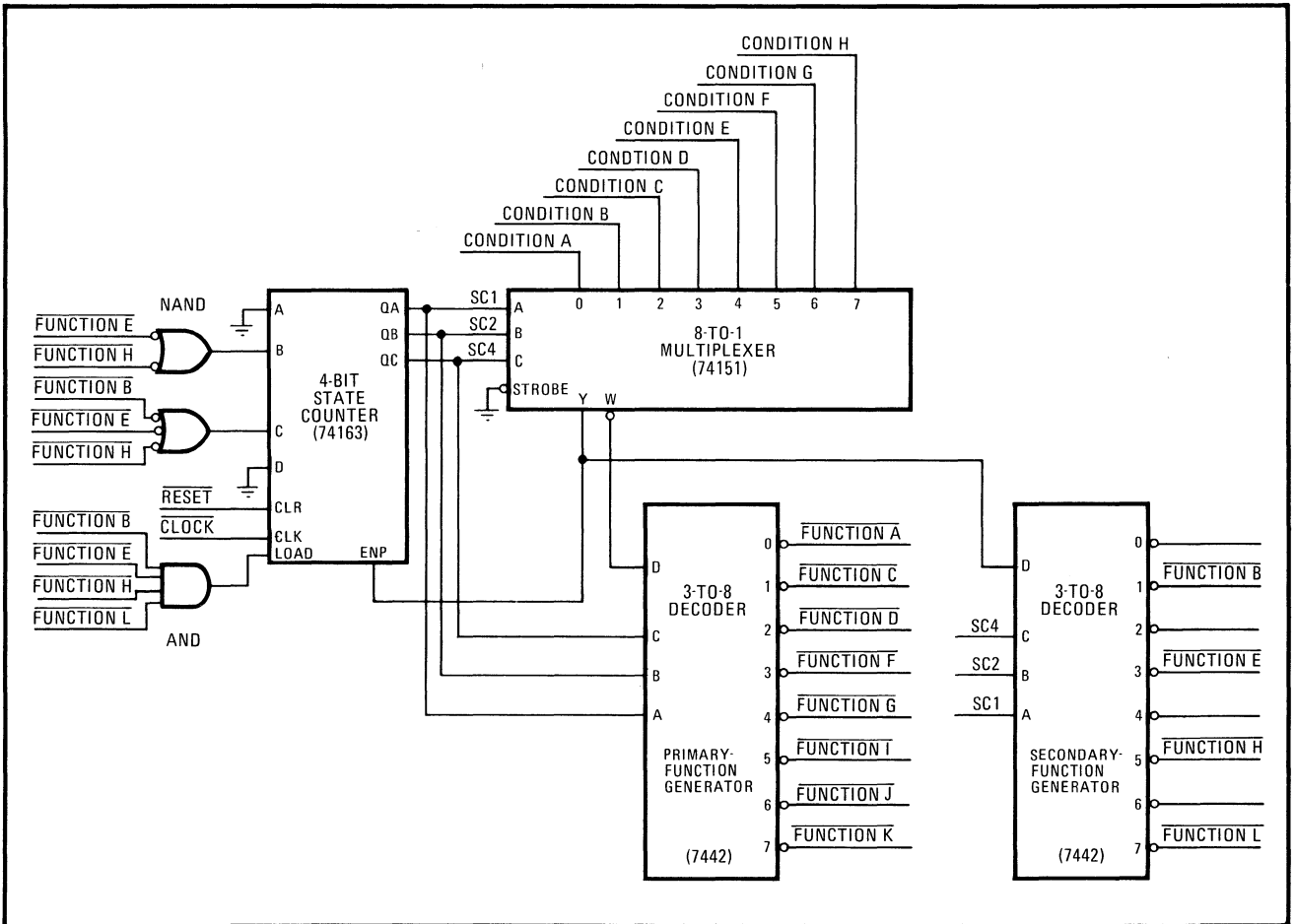
Assume the counter has been RESET to binary 000, corresponding to STATE 0 in the flow chart. This count on the multiplexer's address inputs gates the status of CONDITION A from the multiplexer's input to its complementary Y and W outputs. As long as CONDITION A is NO, the Y output is low and the W output is high. The low Y signal inhibits the counter's ENABLE-P INPUT, so the counter cannot increment even when a CLOCK pulse is present. The W output connects to the decoder's most-significant-bit output (D) which, if high, inhibits the decoder's 0 to 7 outputs. But when multiplexer output W goes low it enables the decoder output addressed by the state counter.

When CONDITION A becomes YES, two things happen: the multiplexer's Y output goes high and allows the state counter to increment on the next CLOCK pulse; and the W output goes low and enables the decoder, addressed to 000, to produce a low output on line 0, thus yielding a signal to initiate FUNCTION A. (Here, a low-voltage output is defined as a TRUE FUNCTION A.)

When the next CLOCK pulse occurs, the state counter increments to 001 (or STATE 1), FUNCTION A goes back high, and the multiplexer's 001-address then gates CONDITION B through the multiplexer, but FUNCTION B from the decoder appears only when CONDITION B becomes YES and the counter increments to the next state. In this



5. Decide and jump. Controller executes steps in sequence unless a condition is NO, in which case—as shown in color—the controller initiates a secondary function and jumps to a new state. Inputs to state counter establish address for multiplexer and decoder.



6. Generating jumps. Adding a secondary decoder (function generator) provides the outputs for the secondary conditions, shown in Fig. 5, which are also fed back to the state-counter's inputs through gates to produce the new jump address for the multiplexer and decoders.

manner, the controller steps through to STATE 7 (111), and when CONDITION H becomes YES, FUNCTION H is generated, the state counter steps to STATE 0 (000), and the controller is ready for the next cycle of operation.

Note in Fig. 4 that the address inputs for the state counter are grounded. The reason is that in this application the required state-by-state indexing is carried out by a CLOCK pulse each time a selected YES condition drives the multiplexer's Y output high to ENABLE the counter. (In more complex controllers, the counter's inputs are addressed according to program requirements, as will shortly be explained.) Simple as it is, however, the sequence controller can prove useful, for example,

where eight conditions must be performed in prescribed order to insure safe and proper operation of a production machine.

2. Designing a nonsequential alternate-function controller

More complex, and certainly more realistic, is a program controller that must trigger one transfer function when a condition is YES and another function if the condition is NO. Also required is that the controller se-

quence to the next state if the condition is YES or jump to a nonsequential state if NO.

Figure 5 contains the flow diagram for a controller that can perform these YES-NO decisions and nonsequential jumps. Here, for example, when it is in STATE 1 and CONDITION B is YES, it will initiate FUNCTION C; but when CONDITION B is NO, it will initiate FUNCTION B and jump to STATE 4. The logic equations, developed from inspection of the flow diagram (Fig. 5), are:

$$\begin{aligned} \overline{\text{FUNCTION A}} &= (\text{STATE 0}) (\overline{\text{CONDITION A}}) \Delta \\ \overline{\text{FUNCTION B}} &= (\text{STATE 1}) (\overline{\text{CONDITION B}}) \rightarrow 4 \\ \overline{\text{FUNCTION C}} &= (\text{STATE 1}) (\text{CONDITION B}) \Delta \\ \overline{\text{FUNCTION D}} &= (\text{STATE 2}) (\overline{\text{CONDITION C}}) \Delta \\ \overline{\text{FUNCTION E}} &= (\text{STATE 3}) (\overline{\text{CONDITION D}}) \rightarrow 6 \\ \overline{\text{FUNCTION F}} &= (\text{STATE 3}) (\text{CONDITION D}) \Delta \\ \overline{\text{FUNCTION G}} &= (\text{STATE 4}) (\overline{\text{CONDITION E}}) \Delta \\ \overline{\text{FUNCTION H}} &= (\text{STATE 5}) (\overline{\text{CONDITION F}}) \rightarrow 6 \\ \overline{\text{FUNCTION I}} &= (\text{STATE 5}) (\text{CONDITION F}) \Delta \\ \overline{\text{FUNCTION J}} &= (\text{STATE 6}) (\overline{\text{CONDITION G}}) \Delta \\ \overline{\text{FUNCTION K}} &= (\text{STATE 7}) (\overline{\text{CONDITION H}}) \Delta \\ \overline{\text{FUNCTION L}} &= (\text{STATE 7}) (\text{CONDITION H}) \rightarrow 0 \end{aligned}$$

The horizontal arrows in the equation point to the required jump state, as determined from the application flow diagram.

Here, the complement (FALSE) of a function—denoted by the bar over, for example, $\overline{\text{FUNCTION A}}$ —must actually be interpreted as the initiation of the required function so as to be internally consistent with the voltage-level convention of the devices in this particular controller. In these devices, a TRUE logic level means a high voltage level; a FALSE logic level means a low voltage level. Thus, the equations above are logically consistent with their electrical circuit (Fig. 6).

This implementation is substantially similar to that of the simple sequence controller, except for the addition of the secondary decoder to develop the nonsequential addresses for those transfer functions generated by the four NO conditions. Also required are NAND gates to drive the state counter to the correct state address and an AND gate to LOAD that address into the counter. If, in Fig. 5, all conditions go YES in sequence, then the operation is the same as that for the previous sequence controller.

Suppose, though, the controller has sequenced through to STATE 3, CONDITION D, which if YES initiates $\overline{\text{FUNCTION F}}$. However, if CONDITION D is NO, the flow diagram indicates the controller should jump to STATE 6, CONDITION G. Referring to Fig. 6, all transfer conditions are inputted through the 8-to-1 multiplexer, with the particular condition gated through the multiplexer (transfer-condition selector) depending on the address produced by the state counter. Also, depending on the counter's state address, the primary decoder will produce one primary function, or the secondary decoder one secondary function. Here, secondary function B occurs at STATE 1, E at STATE 3, H at STATE 5, and L at STATE 7. Thus, the controller uses the secondary decoder's 1, 3, 5, and 7 outputs.

The primary and secondary transfer functions initiate the desired external actions mandated by the particular application. A YES primary condition will cause the controller to index to the next state. But the secondary functions are fed back as inputs to the state counter to

generate a jump address and to load the state counter with that address.

Connecting jump addresses

As shown in Fig. 5 and by the logic equations, the required address jumps are:

$$\text{Function B} \rightarrow 4; \text{E} \rightarrow 6; \text{H} \rightarrow 6; \text{L} \rightarrow 0$$

These state numbers are obtained by addressing the state counter's binary-weighted inputs. The counter's highest-ordered input (D) is permanently set to low level, or binary 0, by grounding, since the A, B, and C inputs can yield the required eight state addresses.

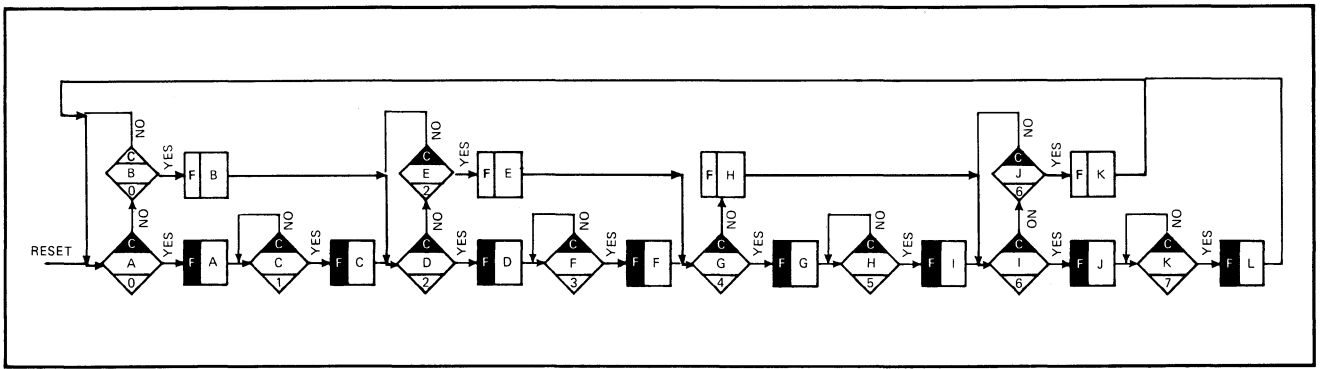
In Fig. 6, these addresses are developed through two NAND gates. $\overline{\text{FUNCTION B}}$ inputted to one NAND gate puts a high-level signal on the counter's C input and generates the 100 which is the jump-to-STATE 4 address applied to the multiplexer and decoders. And $\overline{\text{FUNCTION E}}$ is fed through both NAND gates to activate the B and C inputs to generate 110, the STATE 6 address. The 0 jump address occurs simply when there are no input signals on the NAND gates. Note that since only even-numbered jump addresses are used, the state counter's A input is permanently grounded. In applications requiring odd-numbered addresses, the A input would also be accessed through a NAND gate by the odd-numbered functions.

All secondary-decoder jump outputs serve as inputs to an AND gate that in turn connects to the state counter LOAD input. Because of the voltage-level convention, the AND gate actually performs an OR logic function. Therefore, whenever any jump function appears at the AND gate inputs, the counter's A, B, or C inputs LOAD the counter to set up the jump address at its output.

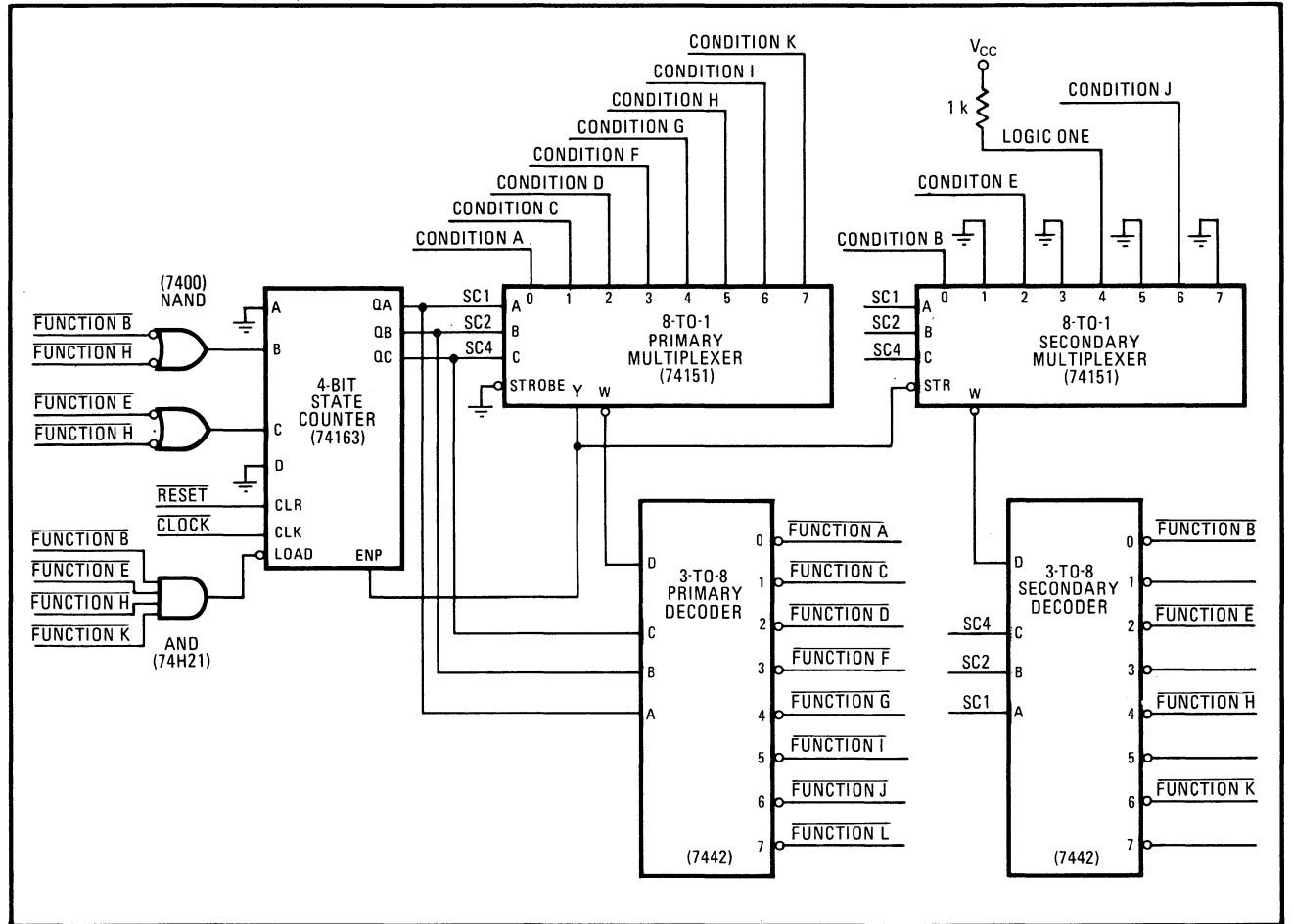
A few other electrical connections are required. The multiplexer must enable the primary function generator for primary (YES) decisions or the secondary-function generator for secondary (NO) decisions. This is accomplished by connecting the multiplexer's Y-output to the D (inhibit) terminal of the secondary decoder and the W output to the D terminal of primary decoder. The Y output also connects to the counter's ENABLE-P terminal.

Assume the controller state counter has been RESET to STATE 0. As long as CONDITION A is NO, the secondary-function generator's 0 output is low—but this output is not used. When CONDITION A becomes YES, the primary-function generator's 0-output goes low to generate $\overline{\text{FUNCTION A}}$. At the same time the multiplexer's Y output goes high to drive the state counter's ENABLE-P input and, on the next CLOCK pulse, the counter increments to STATE 1. Here, as shown in Figs. 5 and 6, if CONDITION B is YES, the primary-function generator is enabled, because W is low, to produce $\overline{\text{FUNCTION C}}$, and, because Y is high, the state counter increments to STATE 2 on the next CLOCK. However, if CONDITION B is NO the low Y signal on the secondary-function generator's D terminal enables that decoder to yield $\overline{\text{FUNCTION B}}$. And the counter must jump to STATE 4. Therefore, $\overline{\text{FUNCTION B}}$ gets fed to the counter's C input through the NAND gate, and to the LOAD input through the AND gate. Thus, the next CLOCK pulse loads the counter to a count of 100, or STATE 4.

In this manner, the controller will either index to the next state or jump to a prescribed state. As shown in



7. Priority control. Flow diagram indicates controller must give first priority, at any state, to primary conditions, at left, but if a primary condition is NO and secondary condition—in color—is YES, then controller initiates secondary function and jumps.



8. Dual decision. Adding a secondary multiplexer, upper right, provides gating of secondary, or low-priority, inputs, with the primary multiplexer's enable and inhibit outputs choosing whether to give priority to primary or secondary transfer conditions.

Fig. 5, initiation of FUNCTION L will bypass FUNCTION K and reset the controller to STATE 0, but if CONDITION H is YES, the controller will first initiate FUNCTION K and then increment to STATE 0.

3. Designing a nonsequential priority-condition controller

Consider now any application in which, at one or more states, two input conditions exist and the program controller has to choose which condition will initiate the

next function. Thus, the controller must follow a set of priority rules. This controller is slightly more complex, electrically, than the previous two examples, but is still easily put together with standard ICs.

In STATE 0 of Fig. 7, for instance CONDITION A could represent a thermostat switch which, if closed (YES) initiates FUNCTION A and indexes the controller to STATE 1. But if the thermostat is open (NO), then CONDITION B should be implemented. Here CONDITION B could be a timer input. In STATE 0 the controller is to give first priority to the temperature input, but if the temperature does not close the thermostat, then after some elapsed time the controller will operate through CONDITION B

and jump to STATE 2. And if the temperature and time are both YES, then the controller is to obey the move dictated by the priority assignment, CONDITION A. Figure 7 includes eight high-priority conditions—A, C, D, F, G, H, I, and K—and three low-priority conditions—B, E, and J—at STATE 0, 2, and 6 with jumps to, respectively, STATES 2, 4, and 0. Also a jump is needed to STATE 6 when CONDITION G, at STATE 4, is NO.

Inspection of the flow diagram (Fig. 7) leads to the following logic equations, which indicate the connections between the devices making up the controller (Fig. 8). Again the delta means index to next state, and the horizontal arrow means jump to the indicated state.

$$\begin{aligned} \overline{\text{FUNCTION A}} &= (\text{STATE 0}) (\text{CONDITION A}) \Delta \\ \overline{\text{FUNCTION B}} &= \\ & (\text{STATE 0}) (\overline{\text{CONDITION A}}) (\text{CONDITION B}) \rightarrow 2 \\ \overline{\text{FUNCTION C}} &= (\text{STATE 1}) (\text{CONDITION C}) \Delta \\ \overline{\text{FUNCTION D}} &= (\text{STATE 2}) (\text{CONDITION D}) \Delta \\ \overline{\text{FUNCTION E}} &= \\ & (\text{STATE 2}) (\overline{\text{CONDITION D}}) (\text{CONDITON E}) \rightarrow 4 \\ \overline{\text{FUNCTION F}} &= (\text{STATE 3}) (\text{CONDITION F}) \Delta \\ \overline{\text{FUNCTION G}} &= (\text{STATE 4}) (\text{CONDITION G}) \Delta \\ \overline{\text{FUNCTION H}} &= (\text{STATE 4}) (\overline{\text{CONDITION G}}) \rightarrow 6 \\ \overline{\text{FUNCTION I}} &= (\text{STATE 5}) (\text{CONDITION H}) \Delta \\ \overline{\text{FUNCTION J}} &= (\text{STATE 6}) (\text{CONDITION I}) \Delta \\ \overline{\text{FUNCTION K}} &= \\ & (\text{STATE 6}) (\overline{\text{CONDITION I}}) (\text{CONDITION J}) \rightarrow 0 \\ \overline{\text{FUNCTION L}} &= (\text{STATE 7}) (\text{CONDITION K}) \Delta \end{aligned}$$

Here again the logic equations show that the required function results when the corresponding decoder output goes low, to be consistent with device electrical levels.

Generating priorities

In Fig. 8, the high-priority conditions are the same as the primary conditions used in the previous examples, and they are gated through the multiplexer generating the high-priority transfer condition. Another multiplexer generates the low-priority transfer conditions. Again two decoders are used, one to output the high-priority functions, the other the low-priority functions. Since this application also requires nonsequential jumps, the jump addresses are obtained by the same procedure of feeding back appropriate secondary (or low-priority) output functions through NAND gates to the state counter. And the presence of any one of these jump functions and the AND gate (operating in an OR mode) loads the address into the state counter. As in the preceding example, the addresses developed by the state counter drive the multiplexers and decoders.

Of particular interest in this example is how the devices are connected so that they properly assess the required priority (if any) in a given state, and enable or inhibit the associated integrated circuits. The Y output of the primary multiplexer connects to the state counter's ENABLE-P terminal to provide sequential indexing when needed. This Y output also goes to the STROBE terminal of the low-priority multiplexer, which inhibits the low-priority transfer-function selector (multiplexer) any time the selected high-priority transfer condition is TRUE. As in the preceding example, when a multiplexer's W output, the complement of Y, is low, it inhibits the function output of the related decoder.

Consider now some of the alternative actions pro-

vided by this program controller that choose and implement a function depending on the priorities assigned to two conditions at a given state. Assume the controller has been RESET to STATE 0. Here, the high-priority (primary) multiplexer is addressed to select CONDITION A and the low-priority (secondary) multiplexer to select CONDITION B.

If CONDITION A is YES (or TRUE), three things happen: the Y output of the primary multiplexer ENABLES the state counter to index to the next step, the W output of the same multiplexer removes the inhibit on the D terminal of the primary decoder and thus generates the addressed FUNCTION A; the Y output, connected to the STROBE terminal of the secondary multiplexer, inhibits—through that multiplexer's W output—the secondary transfer-function generator (decoder). As required, the controller generates FUNCTION A and steps to STATE 1.

However, suppose the controller is in STATE 0 and that CONDITION A is NO and CONDITION B is YES. As shown in Fig. 7, the controller in this situation is to initiate FUNCTION B and jump to STATE 2. Since CONDITION A is NO, the low-priority transfer-function generator is enabled, resulting in FUNCTION B appearing on output line 0, as required. Furthermore, this function is fed back to the state counter's NAND gate which enables input-terminal B to a 100 address so the controller jumps to STATE 4, as required.

For the case where CONDITION A and B are both YES, the controller is to give priority to, and react to, CONDITION A only. This action is the result of the high Y output of the primary multiplexer inhibiting the secondary multiplexer and thus preventing CONDITION B from being gated through to the decoder. Therefore, the controller ignores CONDITION B and the primary Y output enables the state counter to increment to STATE 1. Of course, if CONDITIONS A and B are both NO, the controller stays in STATE 0.

In some states, as for example STATE 3, the controller is required to step to STATE 4 only when a condition (here CONDITION F) becomes YES. Because the secondary multiplexer and decoder are inhibited, the controller indexes in the same manner as in the sequence controller in the first example.

Even without having to make a priority decision, this controller can also perform YES-NO nonsequential jumps, as is required at STATE 4. Here, the controller is to generate FUNCTION G and step to STATE 5 if CONDITION G is YES, or generate FUNCTION H if CONDITION G is NO. In the YES, or primary condition, the primary multiplexer inhibits the secondary multiplexer, so the controller simply generates FUNCTION G and goes to STATE 5. If CONDITION G is NO, the controller must initiate FUNCTION H and jump to STATE 6. To accomplish this, a YES condition is permanently connected to input 4 of the secondary controller, shown as the logic one connection in Fig. 8. Being in STATE 4, with the secondary multiplexer enabled through its STROBE connection and the secondary decoder enabled through its D input, the controller can then "gate" this permanent YES condition through the multiplexer and decoder to generate FUNCTION H, as required. Furthermore, this output is fed to the B and C NAND gates to produce the 110 corresponding to the required jump address of 6. □

Dual-polarity IC regulators aid design and packaging

Mounted in cans or dual in-line packages, voltage regulators that provide both positive and negative outputs from single monolithic chips use little pc-board area, yet they give many electrical options

by Robert A. Mammano, *Silicon General Inc., Westminster, Calif.*

□ Electronic systems using analog integrated circuits have been considerably enhanced by dual-polarity voltage regulators, now available as single monolithic chips. In addition to mounting handily on the printed-circuit boards along with the ICs they are to control, several regulators can be driven from a single remote unregulated power supply. The dual-polarity regulator provides simultaneous positive and negative voltages, with one of the two regulated voltages automatically compensating for fluctuations in the other.

When linear integrated-circuit packages first became available, they permitted the designer to build rather large and complex analog functions on one small printed-circuit board. But energizing several pc boards from one central, but remote, voltage-regulated power supply can create operational problems because of lead inductance and decoupling, and particularly from the voltage drop through leads and connectors. To eliminate these problems, an on-board IC voltage regulator was fed from a separate unregulated power supply. In this way, regulation occurred close to the load.

Initially, these IC regulators could handle voltages of only one polarity, either positive or negative, but two regulators could not be fabricated on the same monolithic chip. However, since most analog circuits require simultaneous positive and negative voltages, single-polarity regulators seemed to beg the question, since each board needed two regulators. Furthermore, two independent regulators still did not meet another basic requirement—that the two regulated voltages match, or track, each other.

Thus, the increasing use of linear integrated circuits created a demand for a dual-polarity voltage regulator built on one monolithic chip so that the adjustment of the voltage of one polarity could automatically adjust the other polarity by the same amount. This tracking capability was achieved by incorporating a single reference diode to regulate one polarity and using that output for the other polarity.

The available dual-polarity voltage regulators are Silicon General's SG1501, SG1501A, and SG1502, Motorola's MC1568, and—recently—Raytheon's RC4195. The SG1501, the first such device, features 100-milliampere output current, ± 30 -v input, factory-set output of ± 15 v, and a sensitivity to full-range load or line variations of typically less than 2 mV. Although the output voltages can be adjusted over a range of ± 8 v

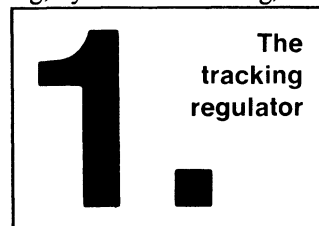
to ± 23 v, this is done with some degradation in temperature stability.

Motorola's MC1568 and Raytheon's RC4195 are substantially the same as the SG1501. All such regulators can be combined with external pass transistors to regulate currents to about 2 A.

The SG1501A handles up to 200 mA of load current, and also it includes a circuit for automatic shutdown when the chip junction temperature exceeds a safe limit. The input voltage has been increased to ± 35 v.

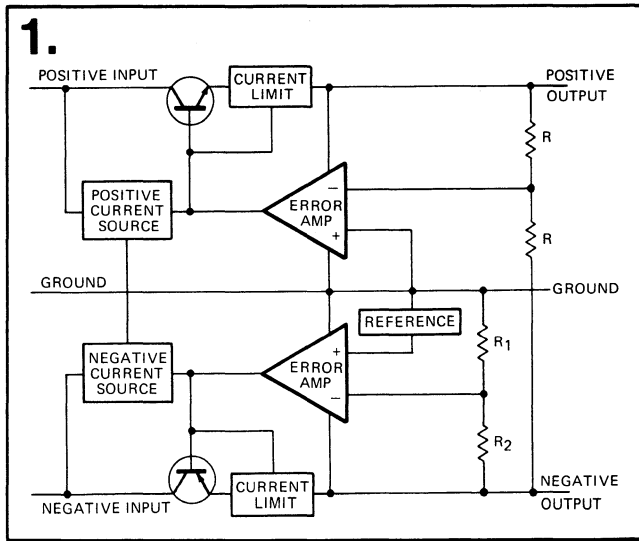
The SG1502 employs the same basic circuit as the SG1501, but it includes two additional features. User-supplied external voltage-setting resistors with small temperature coefficients permit output levels to be adjusted from ± 8 v to ± 28 v while maintaining excellent temperature stability. And instead of limiting the current to some maximum value, the SG1502 includes the capability for foldback circuitry, which actually reduces the short-circuit current to less than the maximum rated load current, thereby limiting internal power dissipation of the pass transistors to a safe value.

Successful applications of these dual-polarity regulators is in the hands of designers, since it is up to them to make sure that the devices do not dissipate enough power to raise internal temperature above allowable limits. The panels that follow discuss regulator operation and detail power-dissipation control by heat-sinking, by current-limiting, and by foldback circuitry.



In this basic circuit for all dual-polarity regulators on single monolithic chips, the constant voltage developed by a zener diode is applied to one input of the negative error amplifier. The other input comes from the tap between R_1 and R_2 , the negative voltage divider, which thus sets the negative output voltage. Because of the closed-loop connection, the output voltage will remain fixed over a wide range of load currents and input voltages.

The reference input to the positive error amplifier is grounded, or zero. Two equal resistances span the negative and positive outputs. The tap between these two resistors goes to the other input of the positive error amplifier. In the steady state, the tap must have a potential equal to zero volts. If it does not, the positive output



voltage will increase or decrease until the input is zero. When this happens, the positive output is equal in magnitude but opposite in polarity to the negative output voltage. (Motorola's MC1568 operates similarly, except the zener reference controls the positive side.)

Any change in the setting of the negative voltage divider will provide exactly the same percentage of change in the positive output voltage. This tracking will hold within 0.5% from slightly above the reference voltage, which is 6.2 V, to about 2 V less than the input supply voltage.

2. Power dissipation

In maintaining a constant output voltage, despite changes in input voltage and output current, the regulator acts like an automatically variable resistance. The power dissipated by this "resistance" is the product of the voltage drop across the regulator and the load current, plus standby power. Standby power, about 10% of maximum power, is dissipated, even when no load current flows.

The maximum total dissipated power cannot allow the junction temperature of any of the many transistors on the chip to exceed 170°C. For maximum reliability, this temperature is usually derated to 150°C.

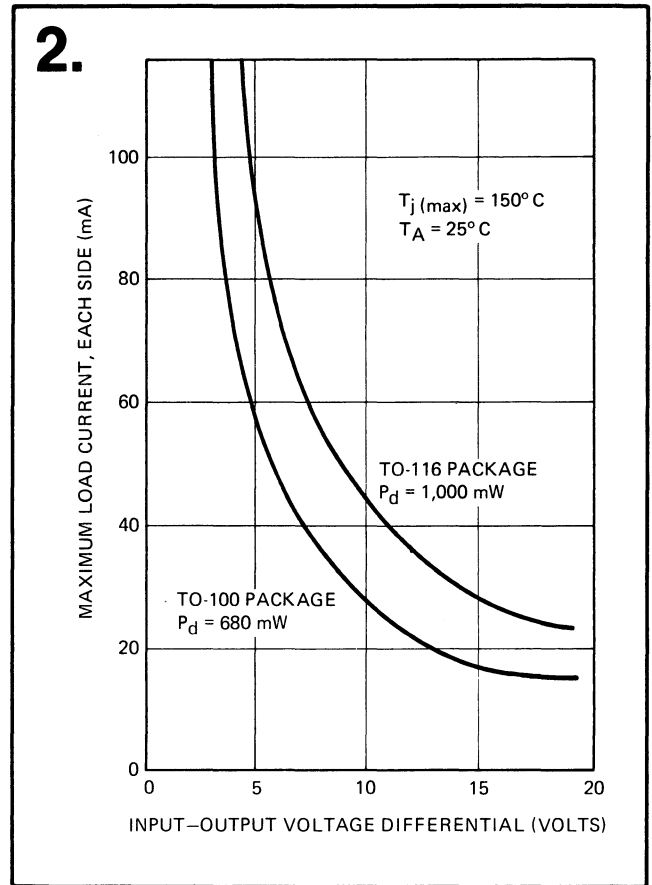
Determining the maximum power-handling capability and the resulting maximum current is a function of the difference between input and output voltages. The allowable maximum junction temperature rise, ΔT_j , is:

$$\Delta T_j = 150^\circ\text{C} - T_{a(\text{max})}$$

where $T_{a(\text{max})}$ is the maximum ambient temperature. The power that can be dissipated, P_d , is:

$$P_d = T_j / \Theta_{ja}$$

where Θ_{ja} is the thermal resistance between the junction and the ambient. The thermal resistance depends on the amount of cooling provided by convection currents, forced air, or heat-sinking. As examples, for a regulator mounted in a TO-100 metal can in open, still air, the thermal resistance is 185°C/w; for a TO-116 ceramic dual in-line package, it's 125°C/w. A heat radiator will



significantly reduce these values. For example, an IERC model TXFB-032-025 top-hat radiator mounted on a TO-100 can bring the thermal resistance down to 130°C/w. A model LIC-214A-2B radiator on the TO-116 reduces the thermal resistance to 50°C/w.

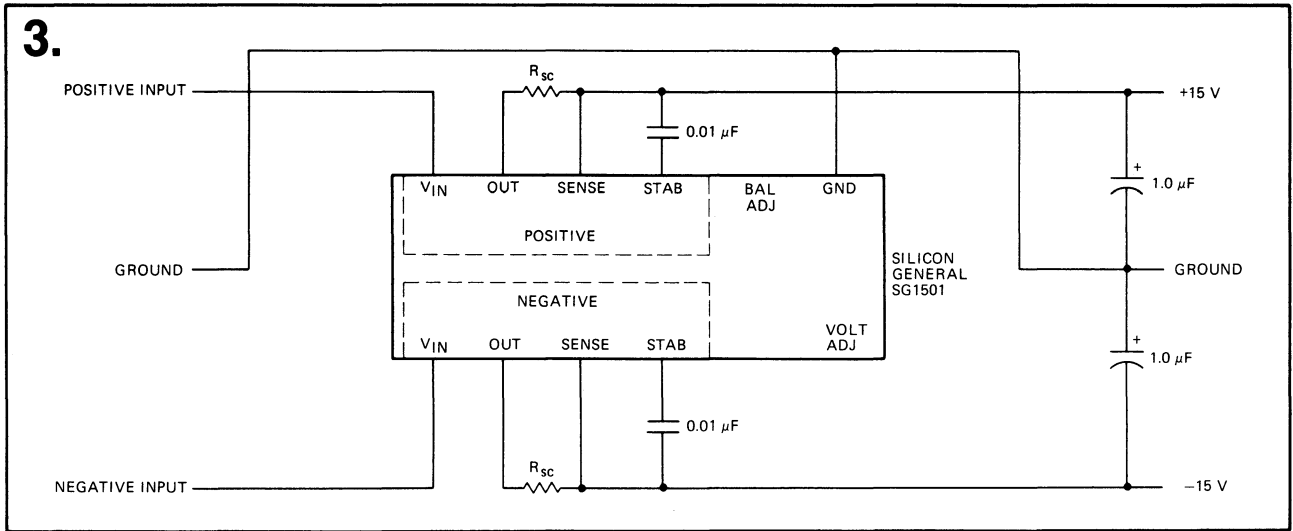
The standby power, P_{sb} , is then subtracted from P_d . The remainder is the amount of power due to the product of load current and input-output voltage differential, for each side, that can be safely dissipated in the regulator. The illustration shows the maximum load current for each side, as a function of a symmetrical voltage differential, for two typical regulator packages.

In this simple application of an SG1501 dual-polarity regulator, the device delivers ± 15 V at the output. For the designer, the main concern is to limit the maximum load current to a value that will not raise junction temperatures above a safe value. Heat-sinking can increase dissipation and hence allowable maximum current.

Each side of the regulator contains a series transistor, through which the load current passes. Current limiting is obtained by diverting, at some prescribed value of load current, the drive signal from the pass transistor. This is accomplished by another transistor which is normally held off, or nonconducting, by an external base-to-emitter resistance, shown as R_{sc} in this circuit. To turn on the current-limit transistor requires a voltage between its base and emitter of about 0.6 V at a junction

3. Current limiting

3.



temperature of 25°C, decreasing to about 0.4 v at 125°C. The load current flowing through R_{sc} develops the sense voltage. Normally, the allowable short-circuit current—the limit—is taken as 150% of maximum operating load current.

Thus the value of the sense resistance is:

$$R_{sc} = \frac{\text{Sense voltage at maximum } T_j}{\text{Allowable short-circuit current}}$$

Because the sense voltage depends on junction temperature, increasing the dissipation within the regulator lowers the value of current at which limiting occurs.

4.

Adding extra power

When the regulator itself cannot handle the required load current, external power transistors can be added on either or both sides. These transistors are selected basically on current and voltage

capability and on mechanical requirements for heat-sinking. However, low-frequency transistors are preferred to reduce risk of oscillation. Capacitors marked by an * should be of solid tantalum because they have lower equivalent series resistance, particularly at high frequencies, than do common electrolytic

capacitors. The 75-ohm base-to-emitter resistors provide a path for the dual-polarity regulator standby current under no-load conditions.

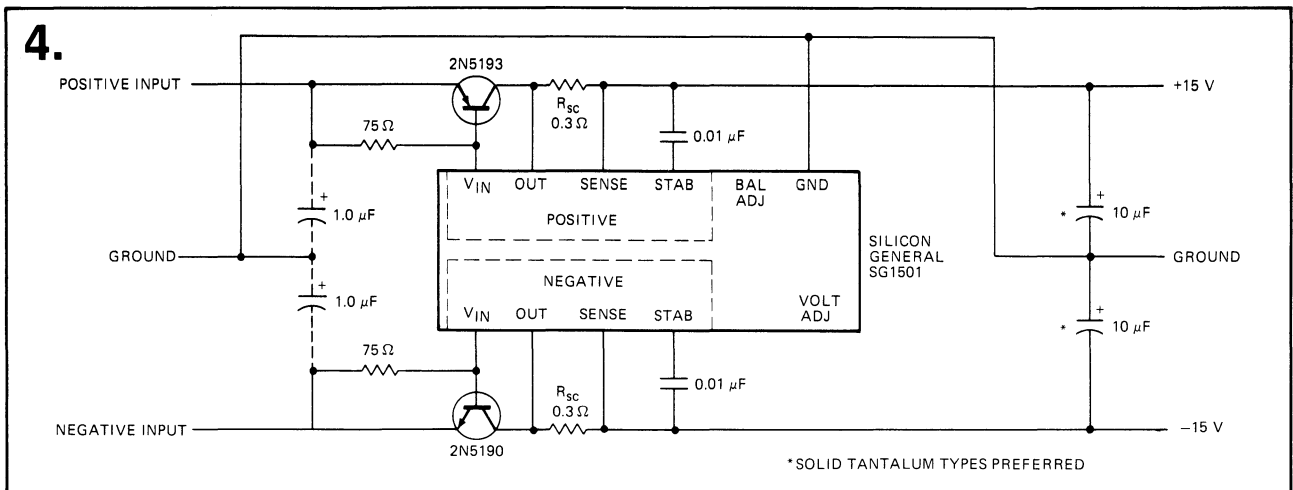
The power dissipated in these external pass transistors under short-circuit conditions can be two or three times more than normal maximum operating levels. Thus, these external transistors may need high-capacity heat sinking. Even the SG1501A, which has an internal circuit for thermal shutdown, cannot help these external pass transistors, since the thermal-shutdown circuit senses internal temperature of the chip, rather than the temperature of the power transistors. To eliminate the need for excessive short-circuit heat-sinking, the SG1502, with its foldback current capability can be used, as discussed in the next panel.

5.

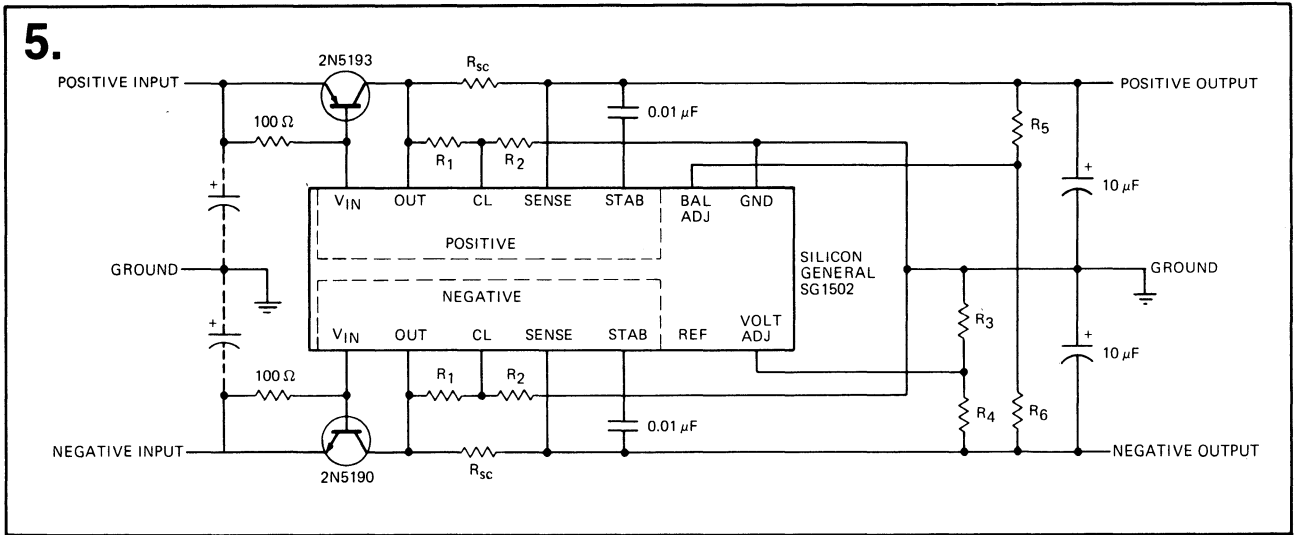
Foldback current limiting

An important added feature in dual-polarity regulators is the inclusion of foldback, the ability to reduce the output current due to a short, to less than normal or maximum operating level. That is, as the output voltage goes to zero with a short circuit—which maximizes input-output voltage differential—the output current is reduced to decrease

4.



5.



power consumption.

Therefore, the use of additional heat-sinking capacity to handle current overloads is not required. Using the SG1502, resistances R_1 and R_2 divide the output voltage, V_o , to essentially increase, or bias, the amount of sense voltage required to turn on the current-limiting transistor.

The values of R_1 and R_2 are determined approximately from an iterative solution of the equations for computing the maximum load current and the short-circuit current;

$$\text{Max load current} = [\text{Sense voltage} + (R_1 V_o / R_2)] / R_{sc}$$

$$\text{Short-circuit current} = \text{Sense voltage} / R_{sc}$$

Inspection of the first equation for normal operation shows that when a short circuit occurs, V_o drops to zero, resulting in the second equation. Hence, foldback reduces the short-circuit current to less than maximum operating current. The larger the voltage drop across the sense resistance, R_{sc} , the larger is the amount of foldback.

Besides limiting foldback current, the SG1502 can also provide output voltages that differ substantially from the normal ± 15 v. Two resistance-divider circuits on the outputs of the regulator allow each side to be set to its own value.

$$\text{Negative } V_o = 6.2(R_3 + R_4) / R_3$$

$$\text{Positive } V_o = R_5 (\text{Negative } V_o) / R_6$$

The 6.2 in the first equation is the voltage of the zener reference, which means that, to retain good tracking, the minimum output is limited to about 8 v.

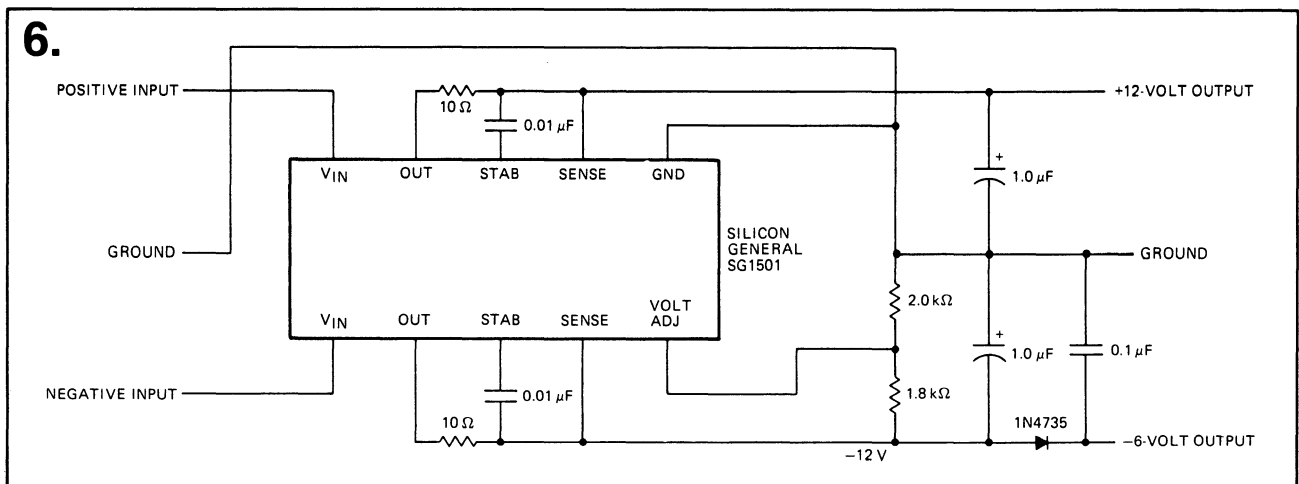
6. Voltage offset

The 710 and 711 IC voltage comparators are widely used in analog circuits. They require +12 v and -6 v for operation. Although 6 v is below the minimum output range of the SG1501,

a more reasonable approach is to reduce the -15 v to -12 v, using the 1,800- and 2,000-ohm divider network. Because of the tracking feature, the +15 v drops to +12 v, as required. Then the -12-v output is reduced to the required -6 v by inserting a 6-v 1N4736 zener diode in the negative-output line.

Since the diode is outside the feedback loop, minor variations in the -6-v output may occur because of changes in temperature and dynamic impedance. However, since the negative voltage is used merely to bias high-impedance current sources in the voltage comparator, these variations will have a negligible effect on comparator operation. □

6.



ROMs cut cost, response time of m-out-of-N detectors

For computer and data-communications applications, the new technique using read-only memories operates faster than present shift register-counter designs and uses fewer ICs than conventional decoding-gate approaches

by A.W. Kobylar, R.L. Lindsay, and S.G. Pitroda, *GTE Automatic Electric Labs., Northlake, Ill.*

□ It is often necessary to examine groups of independent signal leads in large digital systems to determine if a prescribed number of them carry true binary levels. Such a test circuit, which is useful for a variety of functions in computer and data-communications systems, is called an m-out-of-N (m/N) detector. It indicates if m-out-of-N leads carry the true output.

In previous approaches to building m/N detectors, a tradeoff was necessary between high component count and speed. But with the ready availability of monolithic read-only memories, this important function tester can be fabricated with a relatively small number of components and a response time on the order of 150 ns.

A design often used to implement m/N detecting circuitry utilizes decoding gates like those shown in the example of Fig. 1a. With decoding gates, however, a total of $\binom{N}{m}$ * gates are required. Thus, when N exceeds about 15 or 20, the amount of needed hardware becomes unmanageable.

Another common approach that requires less hardware uses a shift register (Fig. 1b). Here, information on each of N parallel lines is stored in an N-bit register. The contents of the register are then counted bit-by-bit as the N-bit word in the register is serially clocked out. The counter is then checked to determine if only m 1s are contained in the N-bit word. This scheme requires

considerably less hardware but, for large values of N, results in a very slow response time because of the serial counting operation.

A simplified special version of the m/N ROM detector—the 1/N decoder—serves to introduce the technique. The 1/N decoder has broad application in testing for one and only one valid signal from a group of parallel lines at any given instant.

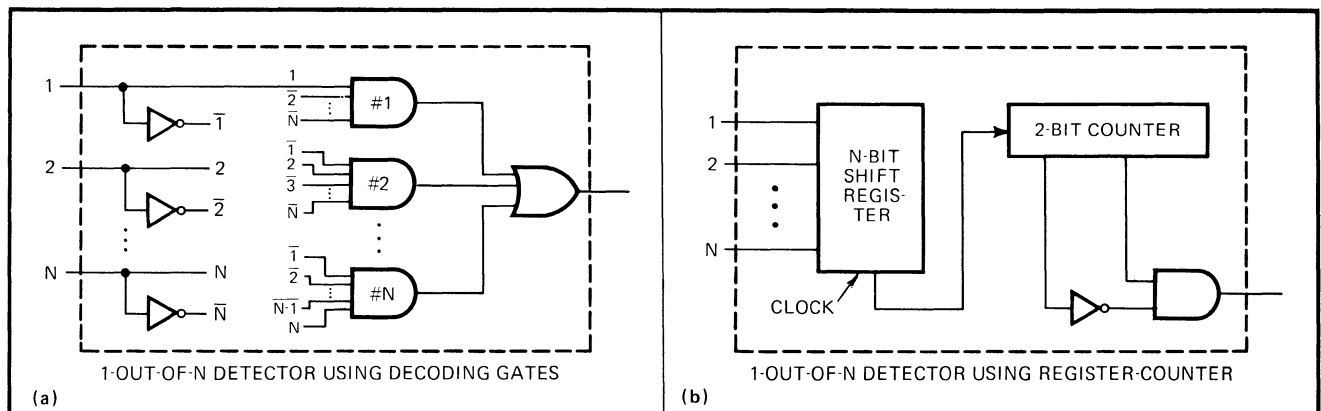
In general, a 1/N decoder requires 2^N bits of binary storage in a ROM. The memory is addressed by the N leads to be checked. The permanently stored information in the ROM contains one “true” state corresponding to all the addresses with a single 1 in the N-bit input word. For the remaining addresses—those containing all 0s, two 1s, and more than two 1s—a “false” is stored.

However, for a large number of inputs, N, the storage capacity for such a single-unit ROM is impractical. For a more versatile system, which uses more easily produced ROMs, a modular design approach has been taken (Fig. 2). For modularity, a large number of input leads, N, are subdivided into smaller groups of n leads. Therefore, a 1/n decoder can be built from commercially available ROMs. The outputs of each smaller ROM are then cascaded to achieve the desired composite output.

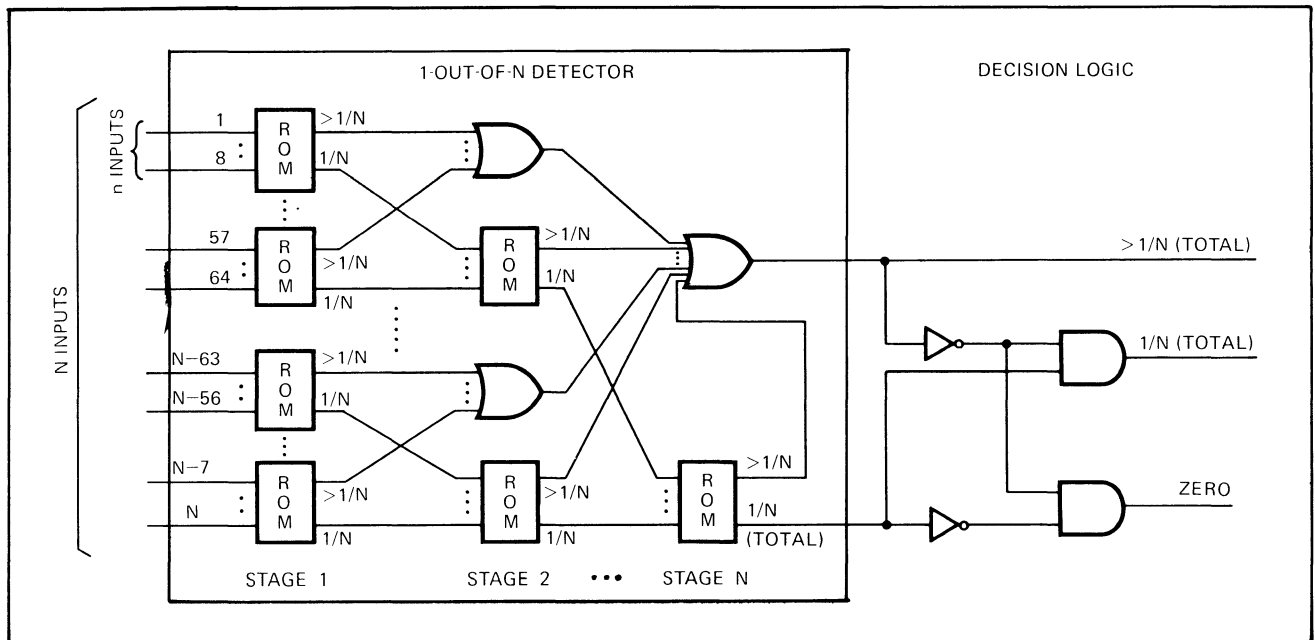
In such a decoder design, where N is divided into a smaller group of n inputs, three states can be distinguished at the output of each ROM module. These states are all 0s, a single 1, and two or more 1s.

Since the all-0s state can be decoded from knowledge of the other two states, only two output lines for each

*This is notation for $N!/[m!(N-m)!]$, or the number of possible combinations of N dissimilar elements taken in groups of m at a time.



1. Speed-size tradeoff. For a large value of N, the decoding gate scheme (a) promises rapid response time, but it requires considerable hardware. The technique using shift registers and counters (b) requires less hardware, but it produces a slow response time.



2. Best of both worlds. A modular design using read-only memories offers a minimum response time with fewer ICs than competing approaches. Here, all 8-input modules are identical. By simply adding modules, 1-out-of-N detection is achieved for any desired value of N.

ROM are needed—one indicating a 1/N condition, one indicating that greater than 1/N input lines are true.

An input word size of 8 bits has been chosen to illustrate the modular design approach shown in Fig. 2. Thus, a 512-bit ROM (2^8 bits for an 8-line input) \times 2 (for the 2-line output) is needed as the basic building block. Multiple stages can then be cascaded to derive a 1-out-of-N detector for any value of N.

The first stage is a set of 8-input ROMs, from which $\lfloor N/8 \rfloor$ sets of outputs are generated. (Note that throughout this article the symbol $\lfloor \dots \rfloor$ indicates the next largest integer value.) The $\lfloor N/8 \rfloor$ outputs, representing greater-than-1/N inputs for each ROM, are ORED together in groups of eight. Then $\lfloor N/8 \rfloor$ outputs representing inputs from stage 1 become the input for the second stage, and so on.

In the second stage, the greater-than-1/N output lines are ORED together and the 1/N outputs form the inputs for the third stage so that $\lfloor N/512 \rfloor$ ROMs are required for this stage. Thus, a detector to decode one input out of as many as 512 can be made with only one ROM in the third stage.

The greater-than-1/N output generated in stage N is Ored with the greater-than-1/N Ored outputs from preceding stages to form a greater-than-1/N (total) output. Likewise, the 1/N line out of the final stage is applied to decision logic to form a 1/N (total) output.

In general, the number of n-bit ROMs required for a 1/N detector can be calculated from

$$\sum_{\alpha=1}^{\lfloor \log_n N \rfloor} \lfloor N/n^\alpha \rfloor$$

A comparison of the number of integrated circuits and the response times required for detectors using individual decoding gates, shift registers, and the ROM decoder are compared in the table for varying values of

N. The advantages of ROM techniques are evident.

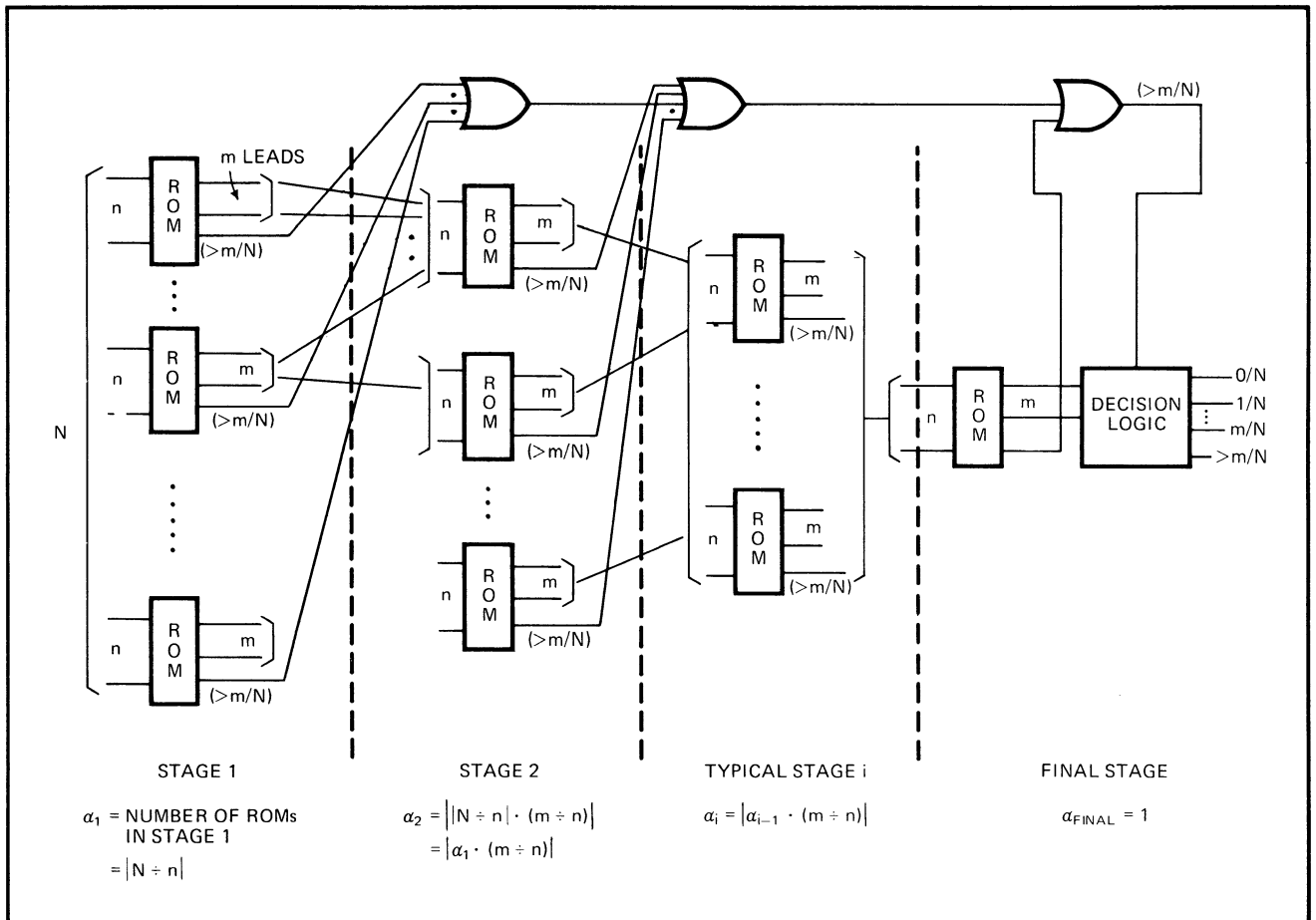
The modular concept can be extended to the more general case where any number, m, lines out of a set, N, can be checked for true conditions. As in the 1/N detector, N is divided into smaller groups of n lines for each module. For such an m-out-of-N detector, the basic module is configured so that its output consists of m leads where (1) if zero out of n inputs is true, then all outputs are 0, (2) if 1-out-of-n inputs is true, then a single output is true, and so on until (3) if m-out-of-n inputs are true, then all m outputs leads are true. An additional output lead for each module indicates that the m-out-of-N condition has already been surpassed (greater than m/N) in that module.

In arranging the ROM truth table in this way, each output lead carries independent information and can be used as an input to any of the memories in the following stage. Notice that, for this modular scheme, m must always be less than n.

The size of the ROM depends on the values of m and n. The total storage required is $2^n(m+1)$ bits, broken down as follows:

| IC REQUIREMENTS AND RESPONSE TIMES FOR 1/N DETECTOR | | | | | | |
|---|----------------|------------|------------------------|------------|------------------|------------|
| N | Decoding gates | | Shift-register counter | | Read-only memory | |
| | T_r (ns)* | IC Packs** | T_r (ns)* | IC Packs** | T_r (ns)* | IC Packs** |
| 10 | 0.10 | 11 | 0.5 | 2 | 0.1 | 4 |
| 50 | 0.10 | 255 | 2.5 | 6 | 0.1 | 10 |
| 80 | 0.10 | 648 | 4.0 | 9 | 0.15 | 16 |
| 800 | 0.10 | 64,080 | 40 | 81 | 0.2 | 130 |
| 5,000 | 0.10 | 2,500,500 | 250 | 501 | 0.3 | 808 |

* A response time of 50 ns per level of logic or shift pulse is assumed.
 ** Assumes a 10-input AND gate, 10-input OR gate, 10-bit shift register, or a single counter for each IC package.



3. Flexible. The general m -out-of- N detector is built with ROMs that are all identical. Each building block is designed for n inputs and $m + 1$ output leads. Simple decoding logic, which derives the desired outputs, follows the final read-only-memory stage

Applications

The concept of checking for m conditions on N parallel lines is useful for a number of applications. One specific installation at Automatic Electric Co. is in a data multiplexing system where 90 terminals are time-division multiplexed onto a single transmission line.

A fault in the control circuitry that multiplexes the data terminals would result in invalid transmissions because more than one terminal is connected at any time. Thus, a 1-out-of-90 detector was designed with ROMs, and with a minimum of hardware, it provides a real-time fault indication.

The communications industry also requires m -out-of- N detectors routinely for other applications. To transmit each digit through standard tone-keyed format, for example, one tone from each of two sets of 4 tones is combined to address the central office; thus, two 1-out-of-4 detectors are required at the central office to locate faulty dialers.

Likewise, signaling between central switching offices is often effected by tone sets that can be checked for errors with a 2-out-of-6 detector.

For the general computing industry, the 2-out-of-5 decimal code (where five binary digits represent values of 0, 1, 2, 4 and 7) is commonly used when simple transmission-error checking is to be implemented. In these and many other applications in the expanding computer and communications fields, m -out-of- N detectors are sure to find greater usage.

- 1 address corresponds to all 0s at the input
- $\binom{n}{1}$ addresses correspond to a single 1 at the input
- $\binom{n}{2}$ addresses correspond to two 1s at the input
- ⋮
- $\binom{n}{m}$ addresses correspond to m 1s at the input
- $\sum_{i=1}^n \binom{n}{i}$ addresses correspond to greater-than- m 1s at the input.

The first stage of the m/N detector divides the N input leads into groups of n . The intermediate outputs up to m/n are necessary, since usually more than one stage is involved in the checking process, and it is essential to know exactly how many input 1s have been detected. The greater-than- m -out-of- n leads are simply ORED together, since any such output, no matter where it is generated, makes the input fail the m/N check.

Each successive stage uses the m outputs from the preceding stages as inputs and further concentrates the detecting process by a factor of m/n . The concentration process continues until the final stage when only one ROM is reached.

The outputs of the final stage then feed simple decoding gates to derive the desired information—usually m/N or $0/N$. However, all intermediate values—from $1/N$ through $(m-1)/N$ are available if the correct decoding logic is provided. □

Matching oscilloscope and probe for better measurements

Several tradeoffs must be weighed for best results; to measure rise time, low input resistance is needed; for amplitude accuracy, it should be high; capacitance can nearly always be ignored when checking for pulse amplitude

by Vic Bunze, Hewlett-Packard Co., Colorado Springs, Colo.

□ The well-known relationship between chains and their weakest links is particularly applicable to measurement systems. One inaccurate or poorly matched component can completely invalidate the results obtained from an otherwise well-designed test setup. Modern oscilloscopes are particularly susceptible to this weak-link phenomenon because their broad bandwidths can be easily compromised by selection of probes that are inappropriate for a given measurement situation.

Nor is this a trivial consideration. Selecting the best combination of scope and probe for a particular measurement and then estimating the errors caused by that scope/probe combination is not necessarily a simple task—especially when high-frequency signals are involved. To understand why, consider how the probe resistance and capacitance act to load down the signal source, and then analyze how this loading affects amplitude and rise-time measurements.

Resistive and capacitive loading

Oscilloscope input impedances come in two basic classes, high and 50-ohm impedance (Fig. 1). Each can be characterized as a resistance shunted by a capacitance. When a probe is added to the scope input, the scope/probe combination may still be represented by a parallel RC circuit. The values and tolerances for R and C are normally specified in the probe data sheet. These values, along with the probe's division ratio, are the basis for estimating the loading effects of the probe/scope input system.

If the input resistance of the probe/scope combination is of the same order of magnitude as that of the signal source, significant measurement errors will result because of resistive loading. Small amounts of loading may simply lower the amplitude of the observed signal, while heavy loading may draw so much current from the signal source that it may force a circuit into saturation or nonlinear operation, or it may cause the circuit under test to stop operating altogether.

Since the probe/scope input resistance, R_{in} , and the signal source resistance, R_g , form a simple resistive voltage divider, the measurement error caused by resistive loading is given by

$$\text{Error in \%} = 100R_g / (R_g + R_{in})$$

A simple rule of thumb for keeping resistive loading errors below 1% is to select a probe/scope combination

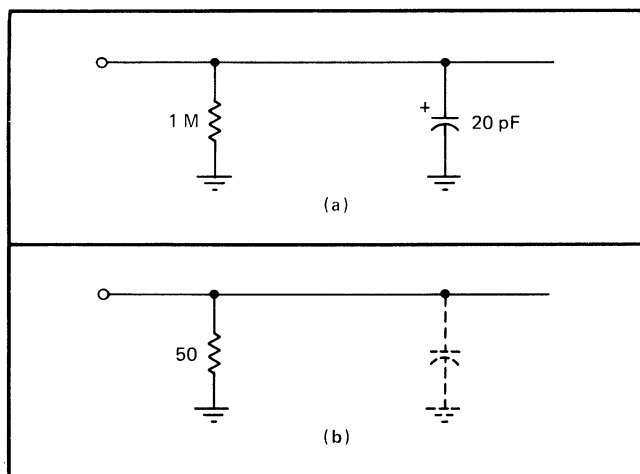
having an R_{in} at least 100 times greater than the source impedance.

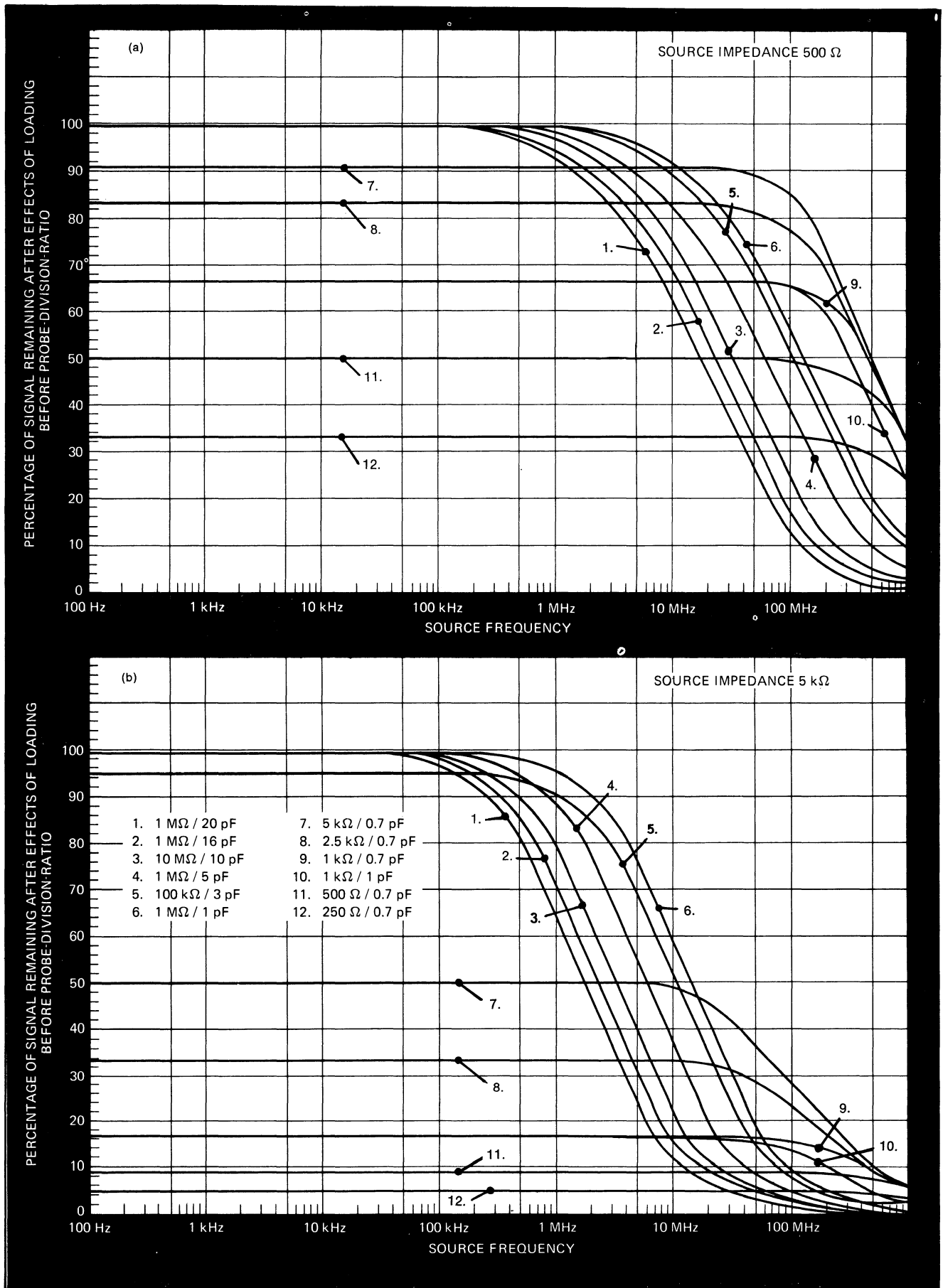
Purely resistive loading effects, of course, are independent of frequency. The shunt capacitance, however, causes measurement errors that are frequency-variable. Like resistive loading, capacitive loading can cause amplitude attenuation and abnormal circuit operation; in addition, it can cause phase shifts and pulse perturbations, and it can introduce errors in rise-time and propagation-delay measurements.

The effect of input shunt capacitance at high frequencies is greater than might at first be assumed: The input characteristics of a high-impedance probe with an input impedance of 1 megohm in parallel with 20 picofarads are almost completely determined by the shunt capacitance at even moderately high frequencies. At 30 megahertz, the capacitive reactance is 265Ω, and at 100 MHz, this drops to 80Ω.

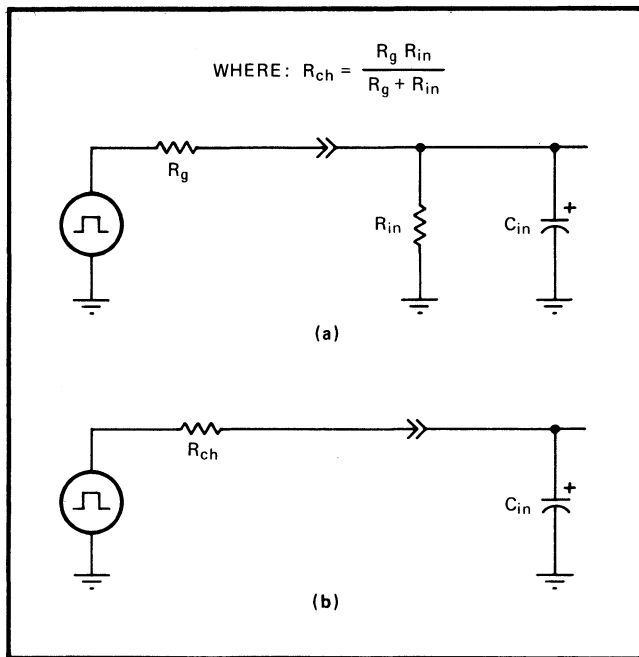
Since the input impedance of a probe/scope pair consists of the parallel combination of R_{in} and X_c , both must be considered in selecting a probe for a given job. To aid in this selection, Figs. 2a and 2b show the effect of source loading by giving in percent the signal remaining as a function of frequency for source impedances of 500 and 5,000Ω. In both figures, the effect of the probes' division ratio is ignored—only losses caused

1. It goes in here. Typical high-impedance input (a) has 1-MΩ resistance shunted by a capacitance of 20 pF. The 50-Ω input (b) is shunted by a capacitance whose X_c is very much larger than 50Ω.





2. Loading effects. Loading of a 500- Ω source caused by various probe/scope resistance-capacitance combinations is shown as a function of frequency (a). For both this case and that of the 5,000- Ω source (b), the effects of the probes' division ratios are ignored.



3. Equivalent circuit. Input circuit consists of C_{in} in parallel with R_{in} and fed from R_g (a). Equivalent circuit (b) shows C_{in} being charged through equivalent charging resistance, $R_{ch} = R_{in} || R_g$.

by loading of the signal source are taken into account.

As an example of the proper use of Fig. 2, assume that a choice must be made between two probes for a cw amplitude measurement from a 500Ω source. Probe 1 is rated $10\text{ M}\Omega$ and 10 pF , with 10:1 division ratio, and probe 2, 500Ω , 0.7 pF , with 10:1 division ratio. The problem is to determine which probe to use for a 50-MHz cw-amplitude measurement. Figure 2a shows that for source frequencies above approximately 33 MHz, probe 2 ($500\Omega/0.7\text{ pF}$) causes less source loading than probe 1, and therefore it provides a more accurate measurement solution. Conversely, for frequencies below 33 MHz, probe 1 ($10\text{ M}\Omega/10\text{ pF}$) creates less loading. The input impedance of probe 2 is lower than probe 1 at dc, it is higher than probe 1 for frequencies above 33 MHz, and it is relatively constant over a broad frequency range. The relatively high input capacitance of probe 1 causes its input impedance to decrease rapidly with an increase in source frequency.

Division is constant, loading is not

This example points out that because of the effects of input capacitance, probes with high values of input resistance can be much less accurate than probes with a much lower input resistance.

It is important to recognize the distinction between signal loss caused by variable loading and signal loss caused by the constant probe-division ratio. Both combine to reduce the signal level available for display. However, the probe-division ratio is specified as constant within a certain percentage over a stated frequency range, and it is therefore easily accounted for. Loading losses, on the other hand, are not easily estimated because they depend on source impedance and frequency. It should be noted here that a probe's division ratio is constant to within a few percentage points only if it is properly compensated so that its RC time-

constant matches that of the input of the scope to which it is connected.

Voltage probes may be grouped according to their ability to minimize resistive, capacitive, or both types of loading. Probes can be classified into three groups that have unique capabilities and limitations. They are group I, high resistance; group II, miniature passive divider; and group III, active. Table 1 lists typical probes available from various manufacturers. Group I probes are noteworthy for their low resistive loading, wide dynamic range, and their ability to withstand signals up to several hundred volts. Their input impedance is high at dc, but due to high input capacitance, impedance falls off rapidly with increasing frequency. Their high input capacitance can be reduced somewhat by high division ratios (100:1) are practical (this depends on the test-signal level and scope vertical-amplifier sensitivity). The group I probe is best used where capacitive loading is not a critical factor; for example, in measuring pulse amplitude or when the source impedance is known to be in the $50\text{-}\Omega$ region.

Group II devices provide the lowest input capacitance available in a probe. They are used mainly when resistive loading is not a major consideration and the fastest possible rise time is desired. They come with divider ratios ranging from 1:1 to 100:1, depending on the divider tips. The maximum input voltage for a group II probe is not as high as that of a group I unit. Group II probes are best used for fast-rise-time measurements, phase-shift measurements, and high-frequency measurements in which some resistive loading is acceptable. Their source loading is relatively high at dc, but since it remains constant over a broad frequency range, loading is easy to predict (see Fig. 2).

The group III probe is probably the best general-purpose probing device within its dynamic range. Two of its disadvantages are larger size (not convenient for very dense circuits) and slightly higher pulse perturbations than passive probes. Group III probes have less capacitive loading than group I probes and more than those in group II. Their resistive loading, however, is negligible. Because they are active devices, they have limited dynamic range. By using divider tips, however, their dynamic range may be extended to as much as $\pm 50\text{ v}$. Offset is commonly available. Group III probes offer the highest R and lowest C of all probe types without reducing the input signals. They are excellent for high-frequency, low-level signals.

Measuring amplitude

The most important factors to be considered in selecting a probe for an amplitude measurement are signal frequency (or pulse-repetition rate), probe/scope impedance, source impedance, scope bandwidth and sensitivity, probe compensation, and division ratio.

For measuring cw amplitude, unlike pulse-rise-time, the main idea is to choose the scope/probe combination that provides the highest input impedance at the source frequency. A group I probe is often an excellent choice at low frequencies, but it is quite possible, as the frequency of the source increases, for the input impedance of the group II probe to overtake that of the group I probe and provide more accurate measurements.

TABLE 1 : TYPICAL PROBES AVAILABLE COMMERCIALY

| Group | Model or Type No. | R _{in} | C _{in} (pF) | Division ratio | Scope input | | Type | Manufacturer |
|-------|-------------------|-----------------|----------------------|----------------|-------------|------|---------|---------------------|
| | | | | | High-Z | 50-Ω | | |
| I | 10004B | 10 MΩ | 10 | 10 | X | | Passive | Hewlett-Packard Co. |
| | 1124A | 10 MΩ | 10 | 10 | | X | Active | Hewlett-Packard Co. |
| | P6007 | 10 MΩ | 25 | 100 | X | | Passive | Tektronix, Inc. |
| | 4290B | 10 MΩ | 11 | 10 | X | | Passive | Dumont |
| | 4292B | 10 MΩ | 11 | 100 | X | | Passive | Dumont |
| | 7994B | 10 MΩ | 7 | 10 | X | | Passive | Dumont |
| | 10000A | 10 MΩ | 9 | 10 | X | | Passive | Dumont |
| II | P6048 | 1 kΩ | 1 | 10 | X | | Passive | Tektronix, Inc. |
| | 10020A | 250 Ω | 0.7 | 5 | | X | Passive | Hewlett-Packard Co. |
| | 10020A | 500 Ω | 0.7 | 10 | | X | Passive | Hewlett-Packard Co. |
| | 10020A | 1 kΩ | 0.7 | 20 | | X | Passive | Hewlett-Packard Co. |
| | 10020A | 2.5 kΩ | 0.7 | 50 | | X | Passive | Hewlett-Packard Co. |
| | 10020A | 5 kΩ | 0.7 | 100 | | X | Passive | Hewlett-Packard Co. |
| III | P6045 | 10 MΩ | 5.5 | 1 | X* | X* | Active | Tektronix, Inc. |
| | P6045 | 10 MΩ | 2.5 | 10 | X* | X* | Active | Tektronix, Inc. |
| | P6045 | 10 MΩ | 1.8 | 100 | X* | X* | Active | Tektronix, Inc. |
| | 1120A | 100 kΩ | < 3 | 1 | | X | Active | Hewlett-Packard Co. |
| | 1120A | 1 MΩ | < 1 | 10 | | X | Active | Hewlett-Packard Co. |
| | 1120A | 1 MΩ | < 1 | 100 | | X | Active | Hewlett-Packard Co. |

*Switchable by means of a control that puts a 50-ohm resistor across a high-Z scope input.

Surprisingly enough, accurate pulse-amplitude measurements pose less of a problem than cw-amplitude measurements. An accurate pulse-amplitude measurement can be made with almost no concern for the input capacitance of the system. The only proviso is that the pulse duration must be at least five times longer than the input RC time-constant of the probe/scope system. This will ensure that the pulse is present long enough to charge the input capacitance to the 100% amplitude level. The main concern when making pulse amplitude measurements is that R_{in} be large, relative to the source impedance.

An error can be introduced by the scope because the vertical-amplifier response changes as a function of frequency. Errors introduced by amplifier rolloff can usually be neglected if the bandwidth is about five times greater than the input-signal frequency.

The probe compensation should be checked and adjusted before any measurement. If not indicated on the probe, the division ratio can be obtained from a data sheet or operating note.

Trading off loading and sensitivity

Here is an example illustrating the major considerations for choosing a probe to measure a 35-MHz signal from a 500-Ω source. The choice is between a 100-kΩ/3 pF probe with a 1:1 division ratio (HP 1120A), and a 5-kΩ/0.7-pF probe with 100:1 division ratio (HP 10020A with 100:1 divider tip).

The 5,000Ω/0.7-pF probe clearly minimizes the loading error (it leaves 89% of the signal vs 76% for the first probe), but its 100:1 divider ratio reduces a 1-V input

signal to only 8.9 mV. This means that for a vertical amplifier with a deflection factor of 10 mv/division, less than 1 centimeter of input signal would be displayed. To minimize reading errors, it is always more accurate to display several divisions of signal. If the signal amplitude in the previous example were 250 mV instead of 1 V, the measurement would be much more difficult. If it were possible to trigger the display properly, there would be a large error resulting from readout accuracy because the signal would only be 2 mm high.

The 100-kΩ/3-pF probe allows a full-screen display of even the 250-mV signal, assuming a vertical-deflection factor of 20 mv/division. The loading error in this case, however, would be 24%, compared with 11% for the other probe.

The choice here is between loading errors and reading errors, and the optimum solution is to estimate both and to try to minimize the combined effect of the two.

General rules for amplitude measurements

In general, maximizing the accuracy of an amplitude measurement involves following three basic rules:

- If there is a choice, select a minimum-impedance source. For example, the emitter-to-base impedance of a transistor is generally lower than the collector-to-base impedance.

- Select a probe with the highest possible Z at the frequency of interest. When measuring pulse amplitude, low capacitance is not as important as having resistance high relative to the source impedance. While probe capacitance distorts pulse shape, the flat portion of the pulse top (maximum amplitude) can provide an accu-

TABLE 2 : CALCULATED PROBE LOADING FROM A 500-OHM SOURCE

| Probe | R_{ch} | $2.2 R_{ch} C_{in} = t_{input}$ | Percent signal loss caused by resistive loading | Probe division ratio | Specified t_r of probe only (25-ohm source) |
|--------------------------|----------|---------------------------------|---|----------------------|---|
| 1. 10 M Ω / 10 pF | 500 | 11 ns | 0 % | 10 : 1 | 2.5 ns |
| 2. 100 k Ω / 3 pF | 500 | 3.3 ns | 0.5 % | 1 : 1 (active) | 0.75 ns |
| 3. 1 M Ω / 1 pF | 500 | 1.1 ns | 0.05 % | 10 : 1 (active) | 0.75 ns |
| 4. 1 k Ω / 0.7 pF | 333 | 0.514 ns | 33 % | 20 : 1 | 0.5 ns |
| 5. 5 k Ω / 0.7 pF | 455 | 0.7 ns | 9.1 % | 100 : 1 | 0.5 ns |

rate amplitude measurement because it contains low-frequency information. Conversely, if the pulse width is short with respect to the measurement-system rise time, input capacitance can introduce errors because the source cannot fully charge the input capacitance while it is present. This problem increases as source impedance increases.

■ If the source voltage is totally unknown, use a 100:1 divider to reduce the possibility of damaging the probe. This will also indicate if there is enough signal available to capitalize on the relatively low capacitance of a 100:1 divider. If the source voltage is too low for a 10:1 divider, then the use of an active probe is advisable.

Measuring rise time

Measuring pulse rise time is one of the most frequent and challenging applications for an oscilloscope. Since there are few alternative devices for this measurement, accuracy of the over-all measuring system is especially important. Conditions affecting the measurement accuracy are:

- Source impedance should be as low as possible to reduce charging resistance of the probe/scope input capacitance.
- Probe rise time should be short relative to the signal rise time because the observed rise time can generally be approximated as the vector sum of the combined rise times of the parts of a system.
- Input R and C of probe/scope combinations both should be as small as possible.
- Oscilloscope rise time should be at least twice as fast as the signal to be measured if errors are to be kept below 10%.
- The signal source should be terminated with an impedance that closely matches the source impedance if reflections and perturbations are to be kept to a minimum. For example, a 50- Ω source does not operate cleanly into a 1 M Ω /20pF input. A feedthrough termination in shunt with a 1-M Ω input can reduce the displayed rise time, which reduces the observed error when working with high-impedance inputs, but reflections remain from the 20-pF input capacitance.
- When the source resistance is much greater than 50 Ω , the displayed rise time error can be reduced by increasing the resistive loading of the source.
- If signal amplitude is small in relation to the oscilloscope vertical-amplifier deflection factor, less flexibility remains for using divider probes because a small dis-

played signal can lead to large readout errors.

■ Vertical-amplifier deflection factor, in combination with the signal amplitude, can be a limiting factor in selecting a probe.

The observed rise time of any displayed signal is approximately the square root of the sum of the squares of all of the rise times in the system. These rise times are the actual rise time of the signal source, the specified probe rise time, the specified scope rise time, and the rise time of the scope/probe input system—including the effects of the source impedance. Other than selecting a fast oscilloscope, the only way the user can minimize rise-time errors is to minimize the rise time of the scope/probe input system— t_{input} .

What is t_{input} ? As Fig. 3 shows, the input capacitance of the scope/probe combination, C_{in} , is charged through the parallel combination of the source resistance, R_g , and the scope/probe input resistance, R_{in} . This parallel combination may be thought of as the charging resistance, R_{ch} of the input capacitance.

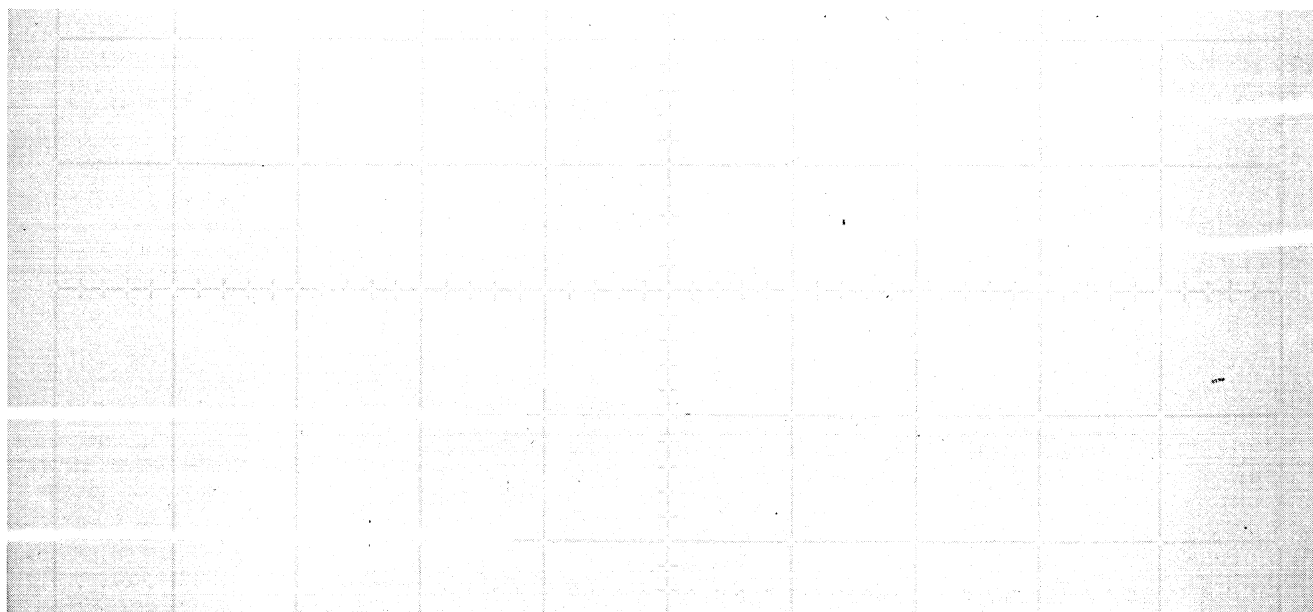
It can be shown that the rise time of the RC network of Fig. 3b is approximately $2.2 R_{ch} C_{in}$, which is also called t_{input} ; thus, to maximize the accuracy of a rise-time measurement, both R_{ch} and C_{in} should be minimized.

Since R_{ch} is the parallel combination of R_g and R_{in} , if either is large, then the other should be kept small. Given a choice, it is preferable to minimize R_g because this will also minimize resistive loading and allow a more accurate amplitude measurement. When R_g is high (say, 500 Ω or more), some resistive loading will be unavoidable to obtain the most accurate rise-time measurement. In this situation, select the lowest R_{in} that the circuit can tolerate without going into an abnormal mode of operation. This is the most difficult type of rise-time measurement because some resistive loading is unavoidable if R_{ch} is to be minimized. A resistive-divider probe set (such as HP 10020A) with several divider tips is convenient for optimizing the tradeoffs of this measurement.

If both R_g and R_{in} are large, then R_{ch} will increase accordingly, and accuracy will be degraded unless C_{in} can be made very small. This is best accomplished by using a 50- Ω oscilloscope input, which has almost zero capacitance. However, if 50 Ω causes too much resistive loading for the circuit, a probe can be added to increase R_{in} to as high as 1 M Ω . There will be a slight increase in input capacitance when the input resistance is raised by



Measuring rise time. When high-impedance ($10\text{M}\Omega/14\text{ pF}$) probe is used, displayed rise time is strongly dependent on source impedance (top). Switching to a $500\text{-}\Omega/0.7\text{-pF}$ probe working into a $50\text{-}\Omega$ input makes the display less dependent on the source impedance (bottom).



a probe.

As an example, consider the selection of the best probe for measuring the rise time of a signal with source impedance of $500\ \Omega$. Assume that the source will saturate if resistive loading exceeds 30%. Five probes are to be considered:

1. $10\ \text{M}\Omega/10\ \text{pF}$, 10:1 (HP 10004B).
2. $100\ \text{k}\Omega/3\ \text{pF}$, 1:1 (HP 1120A)
3. $1\ \text{M}\Omega/1\ \text{pF}$, 10:1 (HP 1120A with 10:1 divider tip).
4. $1\ \text{k}\Omega/0.7\ \text{pF}$, 20:1 (HP 10020A with 20:1 divider tip)
5. $5\ \text{k}\Omega/0.7\ \text{pF}$, 100:1 (HP 10020A with 100:1 divider tip).

This example covers many of the tradeoffs and considerations necessary for selecting the best probe to make an accurate transition-time measurement. Table 2 summarizes the probe-loading effects.

The results in table 2 indicate that probe 4 ($1\ \text{k}\Omega/0.7\ \text{pF}$ 20:1 passive divider) is the fastest, but it fails the ac-

ceptable resistive-loading criterion of 30% signal loss. The reasons this probe is so much faster are that R_{ch} is the lowest, and the input C is very low. The next fastest probe that is capable of meeting the loading criterion is No. 5 ($5\ \text{k}\Omega/0.7\ \text{pF}$, 100:1 divider) with only 9.1% resistive loading. The choice of this probe would depend on whether or not there is sufficient signal remaining after the 100:1 division ratio to present an acceptable display on the CRT. If not, then the next choice would be probe 3 ($1\ \text{M}\Omega/1\ \text{pF}$, active), which is only slightly slower than the 100:1 divider probe.

The general rules for making accurate rise-time measurements can be summed up in two sentences: Always try to probe the lowest impedance point that contains the waveform of interest. The fastest input system will generally have the lowest R_{in} and C_{in} . (This rule is limited only by the maximum resistive loading that the source can tolerate.) \square

Transformer-coupled transceiver speeds two-way data transmission

New line driver/receiver can transmit serial data at 20-MHz rates for several hundred meters and improve cost-effectiveness in certain applications that only parallel-line data buses could previously handle

by Thomas R. Blakeslee, *Consulting engineer, Woodside, Calif.*

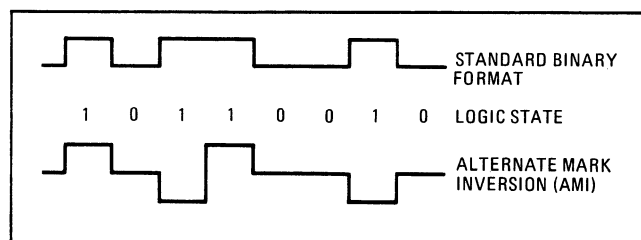
□ The number of interconnections between elements in computer systems is a major factor in determining overall system cost and reliability. Because of the many advantages offered by serial transmission techniques, they are rapidly replacing earlier parallel transmission methods in many applications. Serial transmission, in addition to a radical reduction in the number of wires, connectors, and other system components, cuts crosstalk and usually simplifies parity checking. Serial transmission has not been used extensively because transmission speeds are too low, especially to replace large numbers of parallel lines. However, single serial lines can operate now at speeds to 20 megahertz, which is adequate for many applications.

To reduce the costs of cumbersome parallel lines in a computer-controlled telephone exchange, a serial data-bus system was recently designed, and tests have proved it successful. Since the data transceiver that interfaces with the serial bus is capable of operating at speeds to 20 MHz, the design can be applied to numerous applications where many peripherals time-share a common data bus.

Conversion to serial operation in the exchange decreased by a factor of 48 the number of transmission wires, connector pins, line drivers, and receivers. Furthermore, because the upper limits of the transmission rate imposed by timing skew between parallel lines is eliminated, the total time required for the serial system to transmit a 48-bit word (32 information bits plus 16 address and control lines) remains approximately the same as it was for the parallel system.

Data-bus characteristics

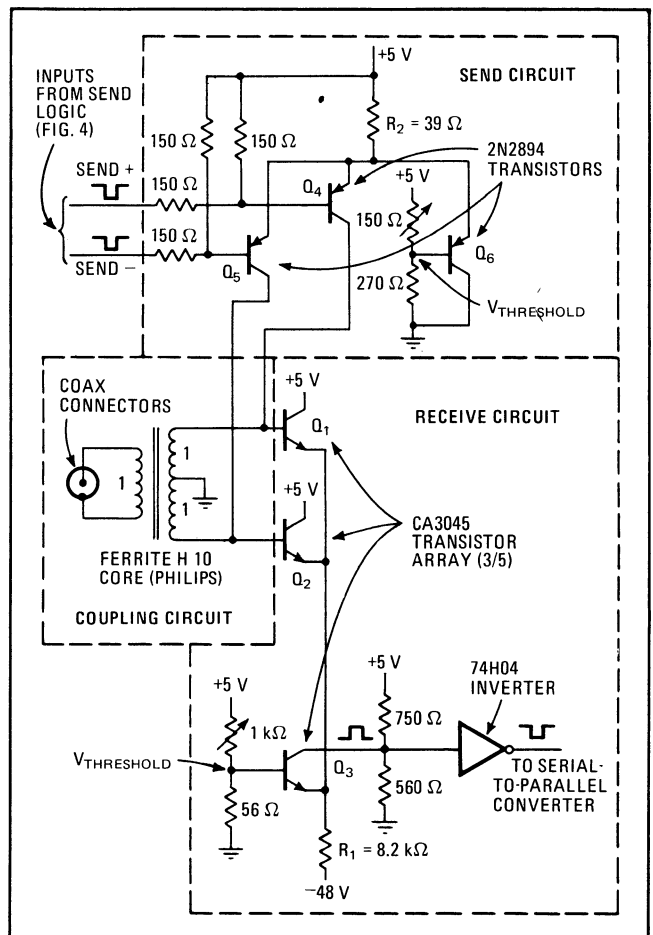
When data is transmitted over distances greater than 1 or 2 meters, either in serial or parallel, it becomes nec-



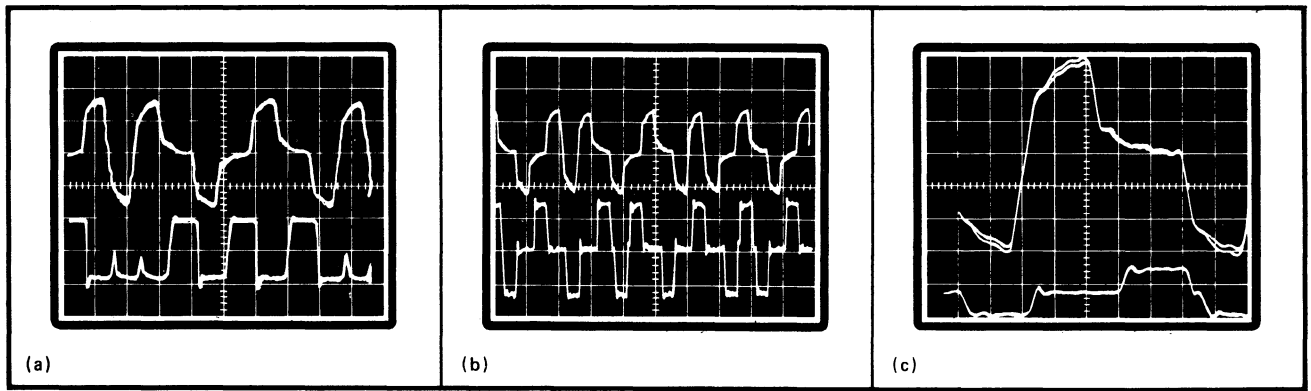
1. Bipolar. Transformer coupling is made possible by the use of alternate-mark-inversion (AMI) coding of binary logic signals. Resulting waveform contains no dc components in its frequency spectrum.

essary to use senders and receivers that are terminated with an impedance that matches that of the transmission line. When the distance is farther than about 15 meters, grounding and noise problems make transformer coupling desirable. And since the dc component of the common binary signal is blocked by the transformer, special coding and decoding of the transmitted signal is required.

Thus, any digital transmission path longer than about 15 meters requires connector pins, transformers, drivers, receivers, and coding and decoding logic at each end.



2. Transformer coupled. Two-way communication is achieved by using a center-tapped transformer. Emitter-coupled-transistor configurations allow higher speeds, since saturation never occurs.



3. Twenty-megabit performance. Receiver accepts bipolar inputs (a, top trace) and converts them to standard TTL format (a, bottom trace) for use by a serial-to-parallel converter. Transmitted waveform (b, bottom trace) is well maintained (b, top trace) after transmission through 150 meters of coax. Amplitude (c) is attenuated little by the addition of one load on a line that already has three loads attached.

As a result, the use of parallel transmission can be quite expensive and unreliable. Moreover, timing skew problems between parallel transmission paths limit the speed of such a system to a transfer rate of about 400 kilohertz for each line.

Why serial transmission helps

Transmitting data serially, however, eliminates skew problems, and the transmission speed is limited only by that of the send and receive circuitry. In fact, transmission rates as high as 6 MHz are commonly used by the telephone industry to send pulse-code-modulated data over ordinary twisted-pair cables with repeaters spaced about one mile apart.

Other characteristics of serial transmission make it more desirable than parallel-line designs. First, the problem of crosstalk in large parallel-line cables is inherently reduced. And since only a single transmission line is needed in serial systems, the use of coaxial cable, which effectively reduces sensitivity to external noise, becomes much more economical.

The use of a serial bus also simplifies parity error checking. While parallel data is usually checked by relatively complex decoding circuitry, serial data is easily processed by a single flip-flop sequential counter as it arrives.

Pulse polarity patterns

In the prototype system, which demonstrates 20-MHz transformer-coupled transmission, a bipolar pulse format removes the dc component that characterizes the normal binary-pulse train. The coding system chosen was alternate mark inversion (AMI), which represents 1s by current flow in either direction, and current direction reverses with each successive logic 1 (Fig. 1). Of major importance is the fact that there is no dc component associated with the AMI format. Thus, AMI-coded data is easily transmitted through the transformer coupler.

Such a bipolar transmission also facilitates transmission-error detection. Erroneous pulses tend to violate the alternating polarity of the AMI pattern, and very simple circuitry in the receiver is easily capable of detecting such errors.

The transformer-coupled line-driver/receiver circuit for the bidirectional bus is shown in Fig. 2. A center tap on the coupling transformer offers a convenient method

of implementing the bipolar format. The single transformer couples both send and receive circuits to the transmission line.

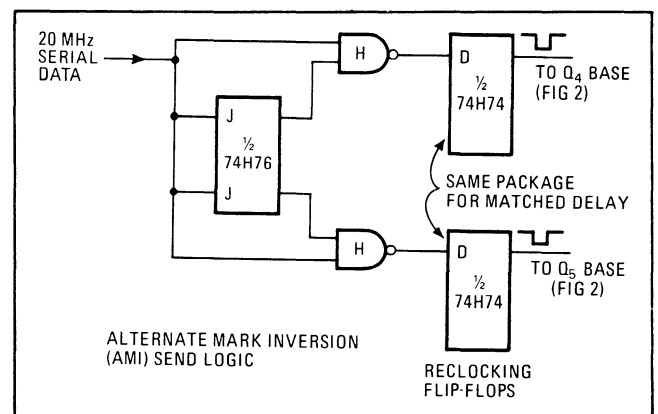
Both send and receive circuits use transistors in an emitter-coupled configuration. This allows the choice of almost any general-purpose transistor, even for the higher operating speeds, since transistor saturation never occurs.

A monolithic transistor-array package (3/5 of an RCA CA3045) is used in the receive circuit. Besides being economical, the matched-transistor integrated circuit allows accurate setting of the decision-level threshold at the base of Q_3 .

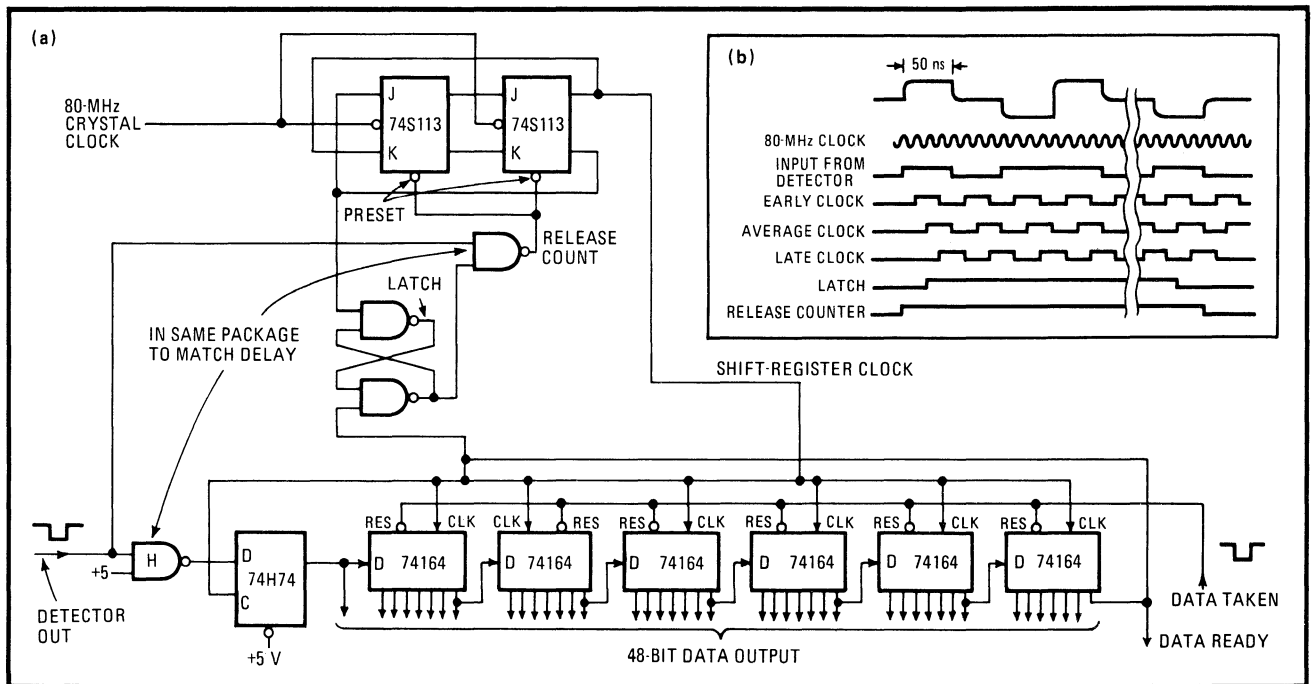
When the signal at the base of Q_1 or Q_2 is below threshold, a current through Q_3 results, placing a logic 0 at the input to the TTL inverter. When a logic 1 is received, the base of Q_1 or Q_2 (depending on polarity) goes more positive than the threshold voltage set at Q_3 , causing Q_3 to switch off and place a logic 1 at the input to the inverter. A sample of the bipolar receiver input, and corresponding output of the inverting gate, are shown in Fig. 3a.

Send circuits

The bipolar send circuit in Fig. 2 is much like that described for the receiver, but it contains pnp transistors (2N2894). The current through R_2 flows through Q_6 to ground in the quiescent, or non-transmitting, state. To transmit pulses, however, input lines feeding transistors



4. Bipolar coding. Simple coding logic converts the unipolar serial data to the two-line format needed by the line driver in Fig. 2.



5. Back to parallel. Serial-to-parallel converter (a) prepares the received serial data for transfer to a parallel-data sink. Converter timing (b) synchronizes incoming pulses with an internal 80-MHz clock. Receipt of a bit at right end of register signals that register is loaded.

Q_4 and Q_5 alternately go negative. Thus, current through R_2 is diverted through Q_4 and Q_5 and into alternate sides of the transformer.

The resulting waveform (Fig. 3b, bottom trace) is well maintained, even after 150 meters of transmission through coaxial cable (Fig. 3b, top trace). The top trace lags by about 675 ns because of propagation delay in the transmission line.

The effect of loading by multiple receivers is illustrated in Fig. 3c. The amplitude of the waveform in the top trace is slightly reduced by the addition of one load on the line, which already has three loads attached. With this loading, a line with 16 receivers has about 60% the amplitude it had with a single load.

The original parallel output of the data source is changed to serial format for transmission simply by loading the parallel data into shift registers and clocking it out with a 20-MHz crystal clock. The circuit shown in Fig. 4 can convert the unipolar serial data to the two-line format that drives the sender in Fig. 2.

Some caution must be exercised to avoid timing distortion in the final logic stage, which drives transistors Q_4 and Q_5 . To reduce such distortion, two flip-flops in the same package (such as the two halves of a 74H74) can be placed in each of these lines to reclock the outputs.

Receiver decoder

To convert back to parallel format at the data receiver, the circuit shown in Fig. 5 is suggested. Since each transmission commences with a logic 1 start bit, the leading edge of this pulse sets the proper phase for a shift-register clocking pulse. The 48-bit serial word is then clocked into the shift register in the same phase.

To accomplish this, a dual J-K flip-flop divides an 80-MHz crystal oscillator down to 20 MHz. This counter circuitry remains inactive until the start bit has been de-

tected and the counter has consequently been released.

If after two 80-MHz clock pulses, the input bit is still present, a latch is set to prevent the reset to the flip-flops from being released until the start bit has progressed all the way through the 49-bit shift register. At this time, the 48 parallel information bits will be available for use by the data sink.

Depending on system requirements, additional logic can be used at each terminal for such functions as acknowledging received data and requesting retransmission. Such functions, however, are generally chosen independently from the type of transmission system and are therefore not considered here.

Farther and faster

The prototype serial transmission system will operate at distances up to 150 meters with a maximum of 16 terminals. However, by use of regenerative repeaters, the length of the data bus and the number of terminals attached can be extended indefinitely.

Each repeater contains two senders, two receivers, and reclocking logic. Thus, timing and-voltage levels out of each repeater are fully reconstructed. An interlock between the two receivers in a repeater must also be included to disable the reverse channel for the duration of a message.

Even higher data-transfer rates can be achieved with multiple data channels. With three 20-MHz parallel channels, for example, 48 bits could be sent between two terminals in slightly more than 80 ns, plus propagation time.

Since each channel in such a three-channel link clocks its data independently, the problem of skewing between parallel transmission lines is overcome. After the start bits have been propagated to the final stage of each shift register, the 48-bit parallel data is ready for transfer into the data sink. □

MOS chip plus level-shifting circuit drives gas-discharge display

The low-voltage output of MOS calculator chips can be made to trigger a high-voltage display if the interface circuit is already maintaining the display electrodes near the potential necessary to fire them

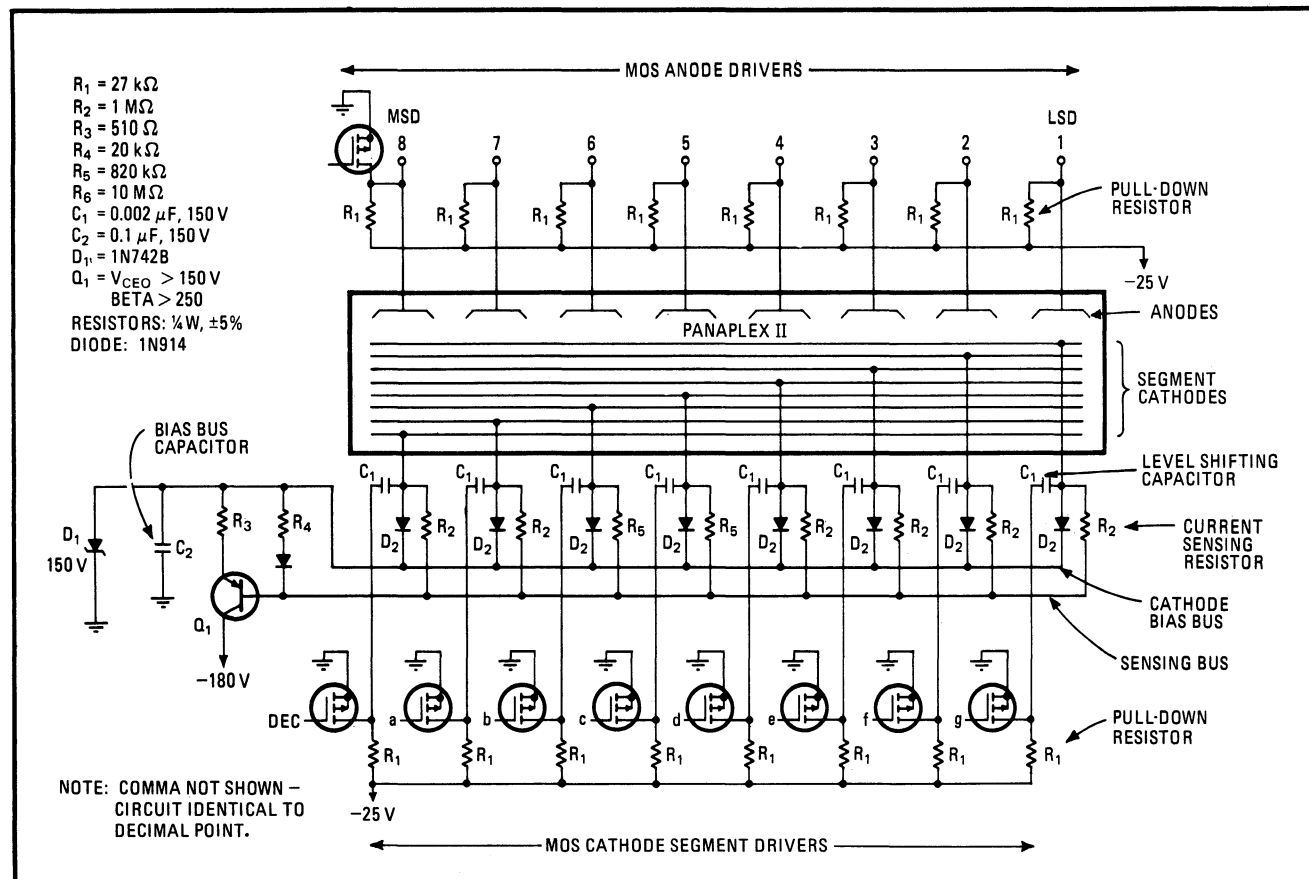
by James Y. Lee and Ed Lord, *Burroughs Corp., Electronics Components Division, Plainfield, N.J.*

□ Although flat-cell gas-discharge displays have been on the market for several years, the high voltages required by such devices have hindered their use in desk calculators, where low-voltage metal-oxide semiconductors are the dominant technology. Changing that situation is a new interface circuit design. It provides a high enough voltage to trigger such a display, while at the same time limiting the voltage on the MOS elements that drive the display.

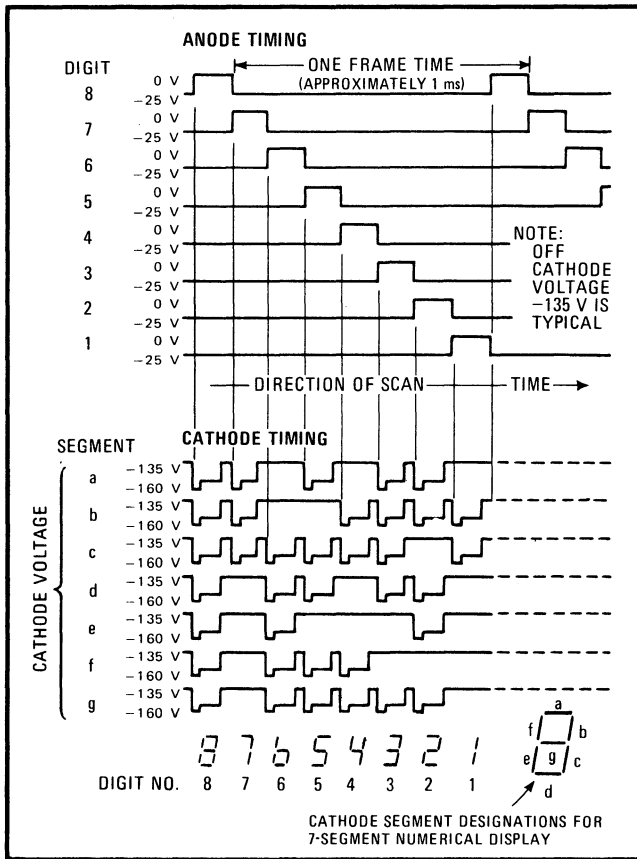
The trick is to regulate the voltage on the electrodes in the display about 50 volts short of the potential necessary to fire the tube. Then the MOS devices can swing the anodes up a mere 25 V and the cathodes down 25 V to provide the firing or ionization voltage.

The display for which the interface circuit was developed is the Panaplex II Panel (see "The search for the ideal display," p. 99). Each digit in the display has its own anode. The corresponding cathode segments of each seven-segment digit are tied together and brought out to a single terminal, so altogether there are only 10 cathode terminals for the seven segments, the decimal point, comma, and minus sign.

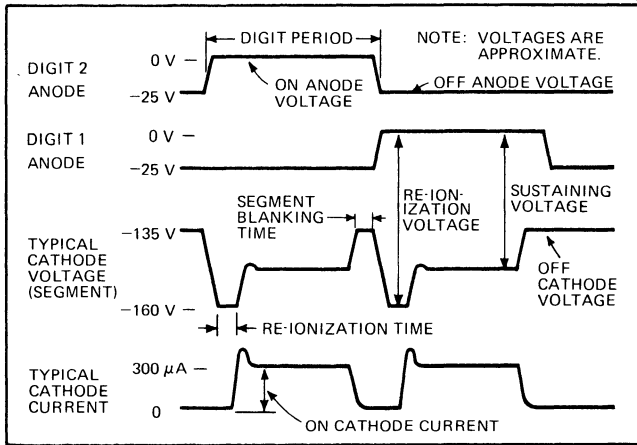
Because there are so few electrodes, a minimum of interface components are needed. As shown in the circuit in Fig. 1, the MOS anode drivers are the digit select devices. When a digit is off, its driver is off, and the anode is clamped to the -25-v bus by a pulldown resistor R_1 . The MOS cathode drivers are the segment select devices,



1. MOS interface. A self-regulating current amplifier Q_1 maintains capacitor C_2 at the cathode bias bus voltage. Capacitor C_2 , in turn, recharges cathode level-shifting capacitors C_1 . Voltage on the MOS anode drivers and MOS cathode segment drivers is limited to 25 V dc.



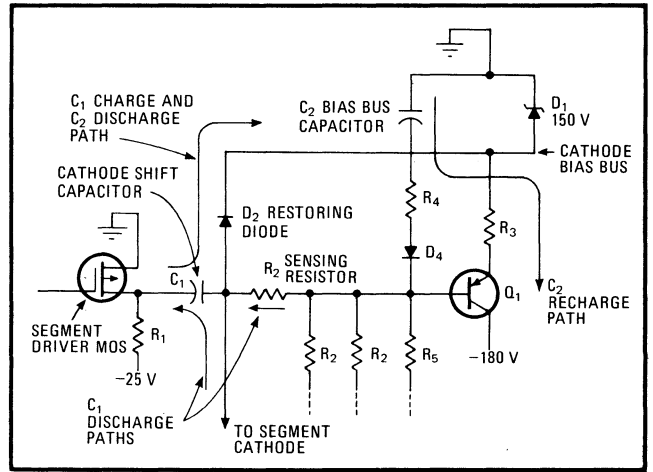
2. Multiplexed. Digits are scanned in reverse order by driving the digit anodes positive. Simultaneously, the selected digit segment cathodes are driven negative.



3. Waveforms. Each digit scan period is divided into portions for re-ionization, on-time and blanking. The blanking time enables the cathode shift capacitors to recharge in preparation for the next digit.

and each is coupled to a segment (decimal point, etc.) through a capacitor C_1 . Under cathode-off conditions, the cathode segment is clamped to the cathode bias bus by diode D_2 . The cathode bias bus potential is regulated by a feedback network at approximately -135 v.

The display timing shown in Fig. 2 represents a time-division multiplexed mode of operation with a scan period of approximately 1 millisecond. Each digit is strobed by driving the anode for that digit with a positive voltage pulse (from -25 v to zero) and by simultaneously driving the selected segment cathodes with a



4. Key capacitor. Capacitor C_2 maintains a cathode bias voltage of approximately -135 volts. Its function is to recharge the cathode shift capacitors during the blanking periods, and it itself is recharged during the re-ionization and sustaining time intervals.

negative voltage pulse (-135 v to -160 v). When this combination of events occurs, the potential exceeds the ionization voltage, and a glow discharge occurs about the selected segments. Following ignition, the anode-to-cathode voltage drops to the sustaining voltage. This voltage, shown in Fig. 3, is the voltage necessary to maintain the discharge.

The voltage and current wave forms are shown in detail in Fig. 3. Note that prior to the firing of a digit the anode-to-cathode potential is $-25 - (-135)$ v = 110 v.

Where the charge goes

The key to circuit operation is the cathode bias bus (Fig. 1), which is regulated at approximately -135 v (depending on the individual panel characteristic). This voltage is developed across bias bus capacitor C_2 , which alternately charges from the -180 -v power source and discharges into various C_1 capacitors through the companion restoring diodes D_2 . The details of this charge-discharge sequence appear in Fig. 4.

When the circuit is first energized, the cathode bias bus voltage is at an arbitrary potential, V_{int} , and zero volts is across capacitor C_1 . When the first segment is selected, the anode of this selected digit is driven from -25 v to 0 v once every millisecond. Assume that only the decimal-point segment at the first digit is driven during the recurrent scans. The first cathode select signal drives the MOS driver for that segment into cutoff, thereby driving the C_1 - R_2 node to -25 v (Fig. 4). The base of transistor Q_1 swings negative, and capacitor C_2 charges so that its voltage shifts from V_{int} to $(V_{int} - \Delta V)$. However, this is insufficient to fire the segment.

The voltage developed across capacitor C_2 is sustained during the next scan, and when the decimal point is next scanned, a millisecond later, the same event occurs, driving the capacitor C_2 from $(V_{int} - \Delta V)$ to $(V_{int} - 2\Delta V)$. This continues until the cathode bus reaches approximately -135 v. Then the cathode shift capacitor C_1 shifts the segment cathode from -135 v to -160 v each time the segment driver MOS is driven into cutoff. When this shift occurs, the drain of the segment driver MOS is pulled down to -25 v. This swing fires the

segment cathode, and C_1 partially discharges.

Toward the conclusion of each digit scan, a blanking signal is applied to each cathode (Fig. 3). This blanking signal, which is applied by the segment select circuits, pulls the cathode up to -135 v. During the blanking period, any cathode shift capacitor C_1 which has been active just prior to blanking is recharged by means of the restoring diode D_2 , along the C_1 charge path shown in Fig. 4. The capacitor is then ready to perform another shift when the segment is again selected.

The cathode bias voltage is the same as the cathode-off voltage and is self-regulated when the system is in equilibrium. This regulated voltage is brought about because the cathode shift capacitors C_1 , which discharge during cathode shifting, regulate the current flow from transistor Q_1 base through a like number of R_2 sensing resistors. (The number of capacitors C_1 that discharge equals the number of segments driven into conduction.) Therefore the charge restored to capacitor C_2 equals the amount of charge lost by capacitor C_1 through the

The search for the ideal display

When the boom in calculators became apparent, display manufacturers began aiming at the optimum design for a calculator display. Such a panel would:

- contain all digits in one envelope, so that no assembly time would have to be spent on straightening and aligning the digits.
- be directly MOS-compatible so that no interface circuits would be required.
- be low-voltage and low-power to reduce power supply costs.

No one has yet built the perfect display, but the Panaplex II Panel makes substantial strides toward it.

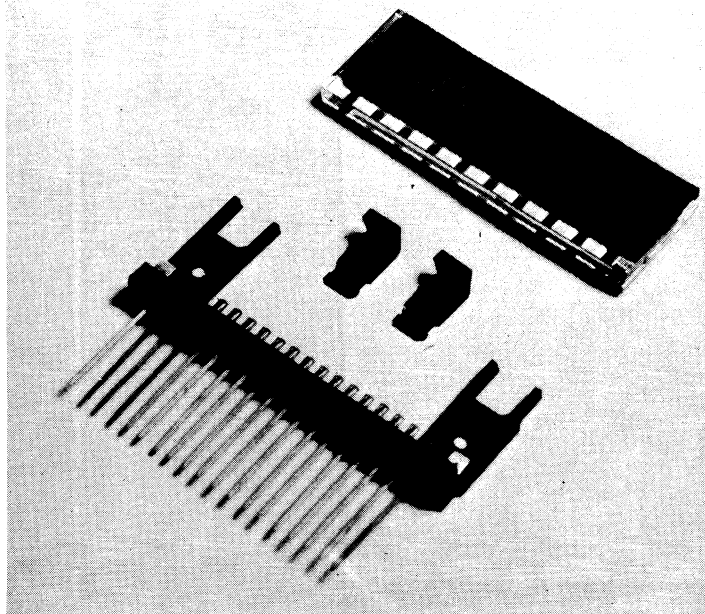
The Panaplex II is a gas-discharge panel display that can mount as many as 16 digits in a single housing. A 12-digit, 0.25-inch-character model is only 3.5 in. long, 0.9 in. high, and 0.2 in. thick (exclusive of the connector). Each digit is made up of seven segments, plus decimal point, comma, and minus sign.

As shown below, a conductive material is screened on a ceramic substrate to form the segment pattern. A black dielectric mask, also screened on the substrate, creates a light-absorbing background that serves to enhance contrast. The digits are neon red and can be read at a distance of about 15 feet.

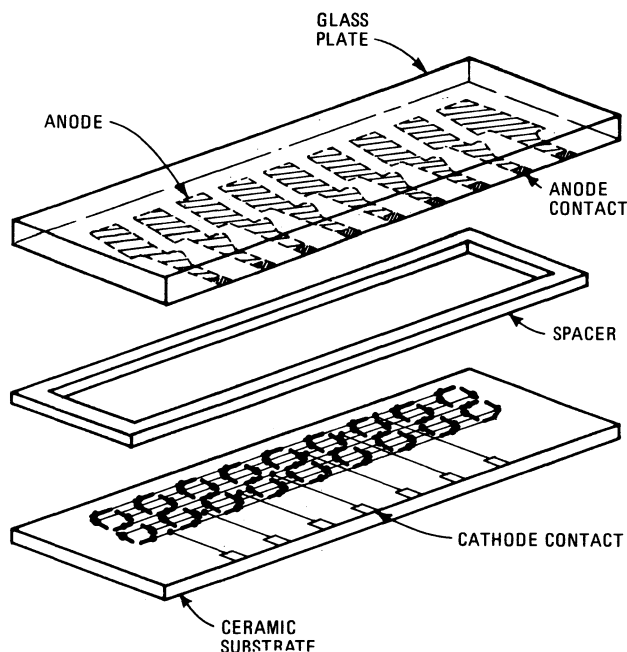
Transparent conducting anodes and anode contacts are applied to the top glass plate, and the plate and substrate are then sealed together, in sandwich fashion, with a spacer providing a hermetic chamber. The device is evacuated and filled with a neon-mercury gas mixture (the mercury reduces cathode sputtering and provides long life).

The interface circuit for the Panaplex II is designed for time-division-multiplex operation of the display. This means that the digits are addressed and illuminated, one at a time, in sequence, so that power need be delivered to only one digit at any instant. The segments require about 5 milliwatts each, and so the worst-case power requirement (assuming all were number eights and a decimal point, a minus sign, and a comma are on) is about 50 milliwatts. If the multiplex (or scan) rate is 80 hertz or higher, then operation will be free of flicker. At that frequency, each segment is refreshed often enough for the eye to be insensitive to the variations in its illumination level.

Direct MOS compatibility remains out of reach. But the interface circuit described in the accompanying article provides direct capacitive coupling between MOS chip and display for a minimum of external components.



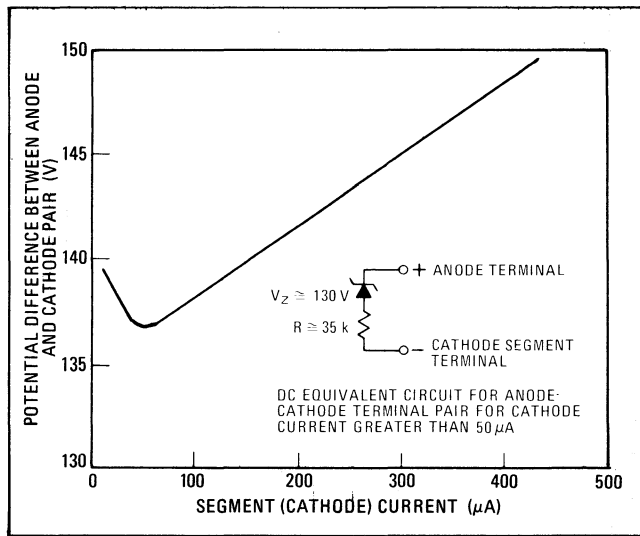
Packaged digits. Up to 16 digits may be enclosed in a single, gas-filled package so that they are in permanent alignment. Entire device may be plugged into a companion socket.



Sandwich. Hermetic package, formed by a rear substrate with screened segment cathodes and glass plate with transparent anodes, become a multidigit, gas-discharge display.

Panaplex II Panel and the sensing resistor R_2 . This same amount of charge is then transferred to the C_1 's during the next blanking interval. This implies that the sum of all charges in all level shift capacitors and the cathode bias bus capacitor C_2 remains constant.

Once the system is in this equilibrium state, it will remain so. Should the cathode bias voltage become more positive than the equilibrium value, there will be a reduction of re-ionization voltage, and the re-ionization voltage will remain longer across the sensing resistor R_2 (see Fig. 4). This will result in a greater Q_1 base current time product which will thereby charge the bias bus capacitor more negatively. The condition is reversed if the restoring bus is more negative than the equilibrium value.



5. Dc behavior. The plot illustrates the volt-ampere characteristic of a single digit segment. The equivalent circuit applies for a current that is in excess of 50 microamperes.

In general, the volt-ampere characteristic of the anode and cathode pair (Fig. 5) is important because it enables a designer to select the proper current-limiting circuits. This current is 300 microamperes for the segments, the comma, and the decimal point, and is the value that ensures uniform cathode illumination of the chosen segments.

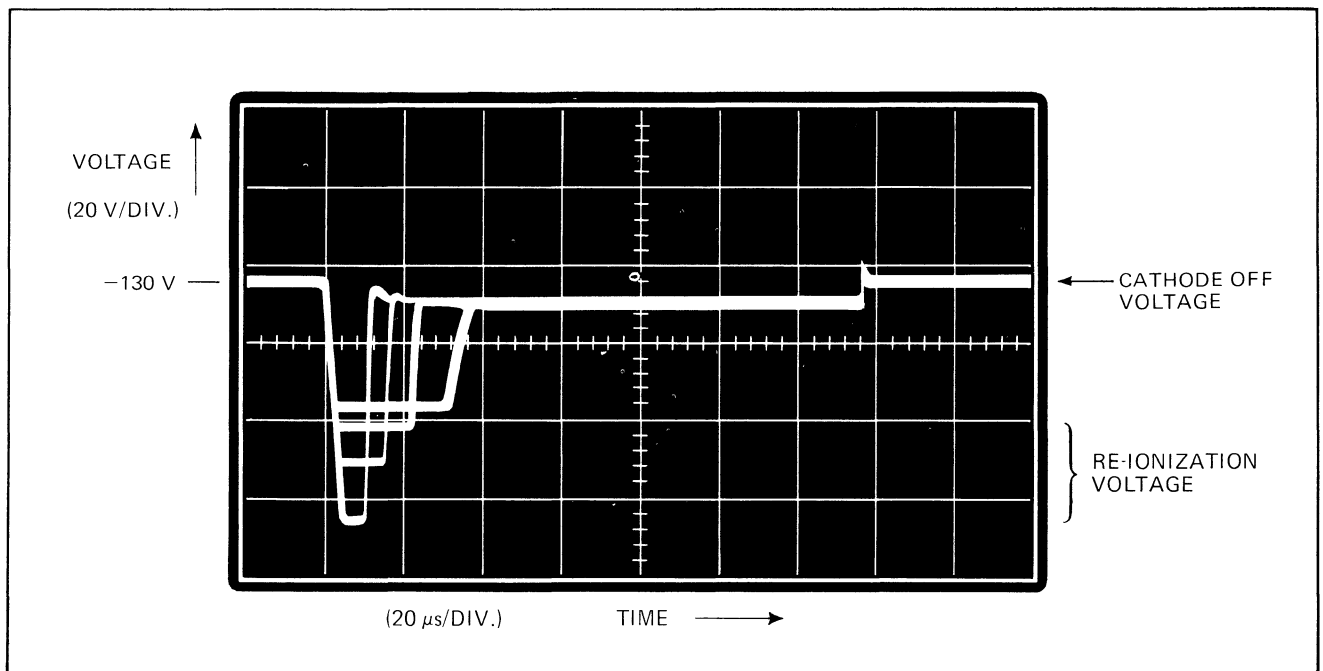
A useful portion of the curve is to the right of the knee, or where the cathode current is above 50 microamperes. A segment operated in this region may be approximated by a zener diode in series with a resistor, as also shown in Fig. 5.

Re-ionization time

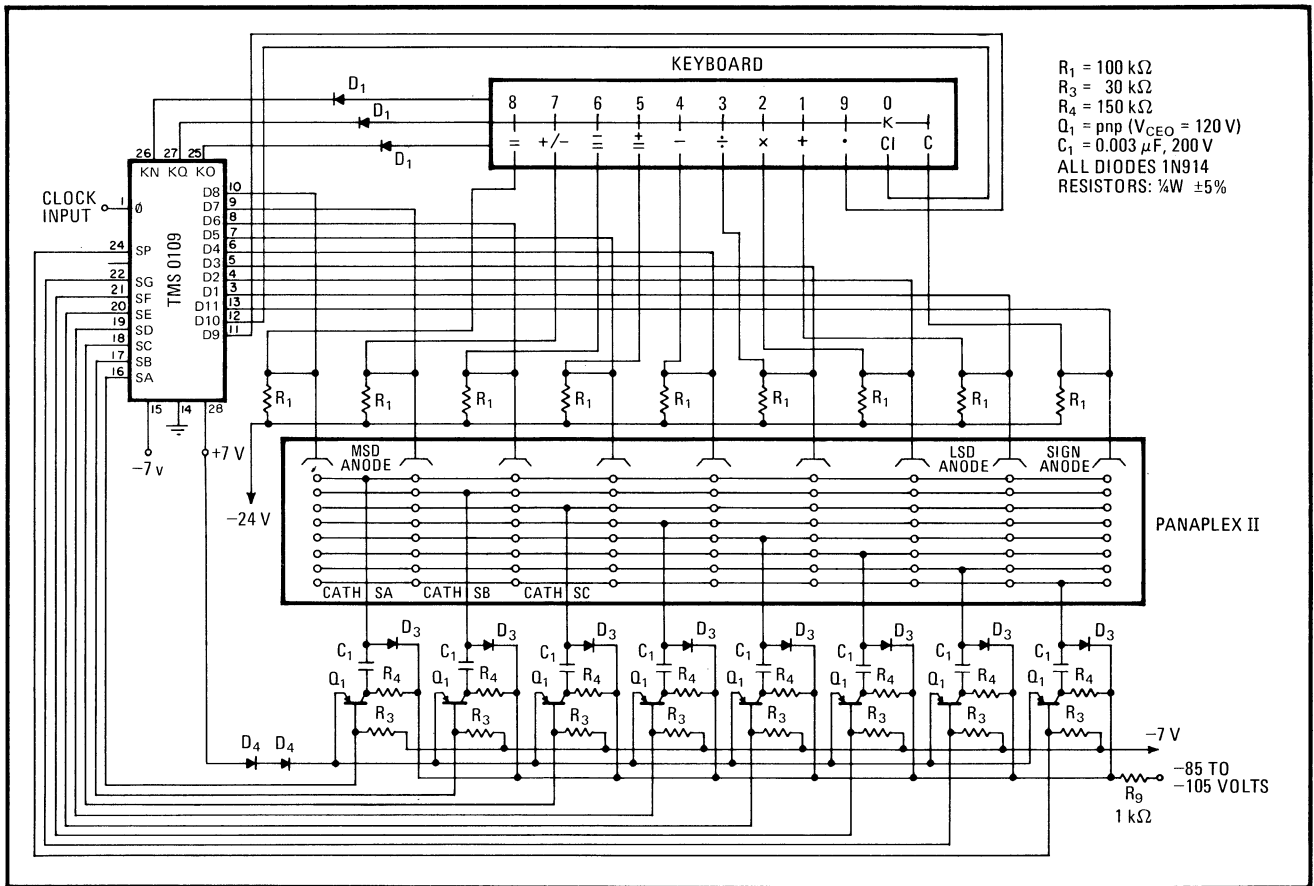
There is a time delay between the instant that the voltage is applied to a given segment and the instant that illumination occurs. This delay is important because it sets an upper limit on the rate at which the digits can be scanned by the multiplex circuits. If the scan rate is too high, then the segments will not glow at all or they will glow for too short a time to provide adequate illumination. This delay is termed re-ionization time.

Shown in Fig. 6 is an oscillograph of the segment cathode voltage which illustrates the re-ionization times for four different applied voltages. The voltage swings negative from -135 v to approximately -160 v to exceed the ionization voltage. After a re-ionization time of 10 to 30 microseconds, depending on the applied voltages, the segment is ignited, and the cathode voltage drops to a value determined by the volt-ampere characteristic of the circuit comprising the display and driver components.

The re-ionization delay time is a function of both the applied voltage and the availability of charged particles. In a multidigit display like the Panaplex II, charged particles are available from an adjacent digit, which means the delay is shorter for a given applied voltage



6. Re-ionization delay. A delay of approximately 20 microseconds occurs following application of the segment re-ionization voltage until conduction occurs. Nine-digit frame period is 1.224 milliseconds, digit period is 136 microseconds for this 0.25-inch-high-character display.



7. Calculator interface. Bipolar transistors interface the Texas Instrument one-chip calculator TMS 0109 with a Panaplex II display. Blanking is provided by the TI device. A doubler circuit (shown in simplified form in Fig. 8) develops a -180-V dc re-ionization voltage.

than if the digits were in individual envelopes.

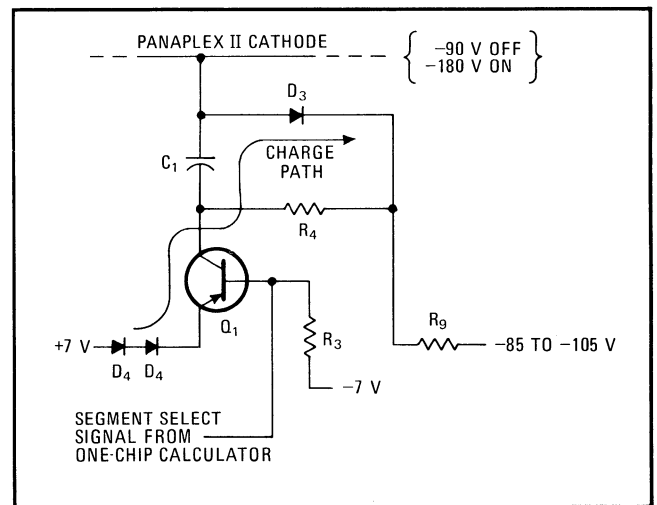
If a designer wants to reduce re-ionization time, then scan rate may be reduced, and/or applied voltage and cathode current increased. The reduction of re-ionization time with increased voltage is apparent in Fig. 6. Of course, decreasing the scan rate much below the recommended 80 hertz will introduce flicker. As for applied voltage and current, if the voltage is increased beyond the maximum limit of 250 v dc or if current is raised beyond 600 microamperes, then the life of the device will suffer.

Other factors that will increase re-ionization time are: the direction of scan when it is opposite the direction of data entry, and the reduced availability of particles that occurs whenever the preceding digit is blanked.

A one-chip calculator interface

Several different versions of this interface circuit have already been designed. The one shown in Fig. 7 was designed for the TI one-chip calculator TMS 0109. This MOS chip itself provides the cathode blanking required by this interface circuit. The anode is a direct-drive configuration with R_1 serving as the pulldown resistor from a -24-V dc bus.

The cathode drivers use a voltage-doubler scheme to provide the necessary cathode ionization potential. This is the sequence of events. When transistor Q_1 saturates, capacitor C_1 charges through diodes D_3 and D_4 to approximately -90 V (Fig. 8). Therefore, when Q_1 cuts off, the cathode is driven to approximately -180 V and trig-



8. Doubler. Transistor Q_1 , capacitor C_1 , resistor R_4 , and diode D_3 perform as a doubler to develop the necessary potential to fire the Panaplex II segment cathodes. Firing occurs following Q_1 cut off.

gers the segment. Resistor R_4 limits cathode current. R_3 provides base current to Q_1 during Q_1 's on period.

The sign anode, which is usually located to the left of the numeric, is shown in Fig. 7 positioned on the right side of the Panaplex II. There are two reasons for this: the right-most character in this display does not function properly with the TMS 0109 if it is a digit; also, a single minus sign in the left-most position represents a difficult initial re-ionization condition. □

Functional redundancy assures greater system reliability

Two parallel electronic systems are more than twice as reliable as one alone: but even greater reliability can be achieved if the system is partitioned into functional blocks and those blocks are made redundant

by Roy J. Hughes Jr., *General Dynamics, Electronics Division, Orlando, Fla.*

□ A popular technique for upgrading the reliability of an electronic system is simply to place two identical units in a parallel configuration, one operational and the other in standby. This redundancy gives the pair more than double the reliability of the single unit. However, failure in one of the two parallel units throws that entire unit out of action.

A more efficient solution is to partition the system into functional blocks and make each block parallel-redundant. This creates two parallel sets of functional blocks, the outputs of each pair of blocks being cross-strapped to the inputs of the succeeding pair. Reliability is increased because if one block in a set fails, the other blocks in that set can still be used.

Application

In a pulse-code-modulated (PCM) encoder proposed for the Air Force's Fleet Communications Satellite program, such functional partitioning reduces the probability of failure by a factor of three or four compared with conventional parallel standby redundancy designs, yet only 7.5% more components are required. Moreover, compared with a triple standby redundant version (one with two units in standby), the functionally redundant system requires much less circuitry, and even so it

achieves greater reliability over the long term.

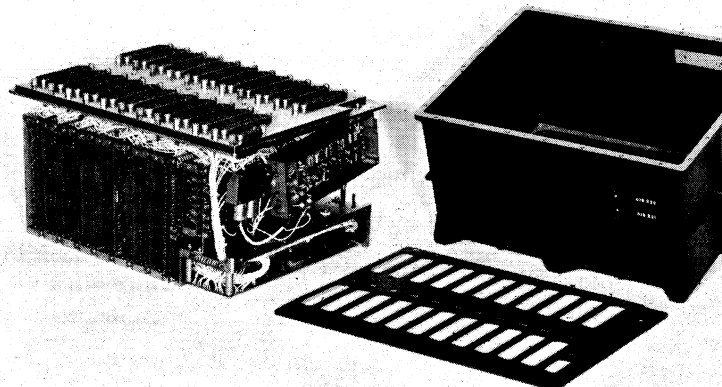
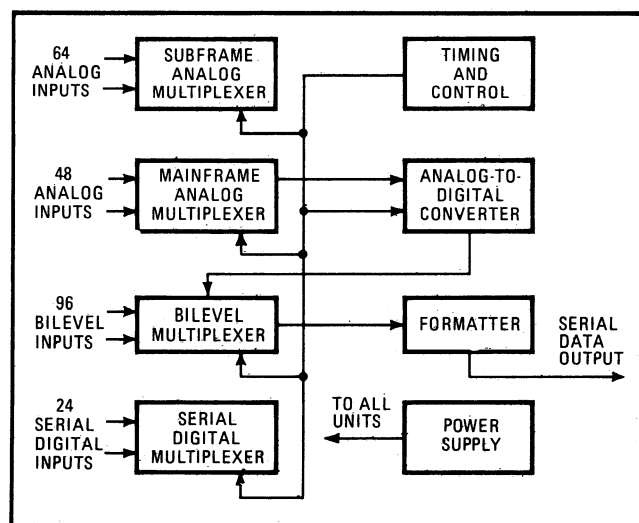
The PCM encoder is illustrated in Fig. 1. It samples both analog and digital information in real time with time-division multiplexers. The analog data is encoded to digital form and formatted with the digital data and synchronization information for data recovery.

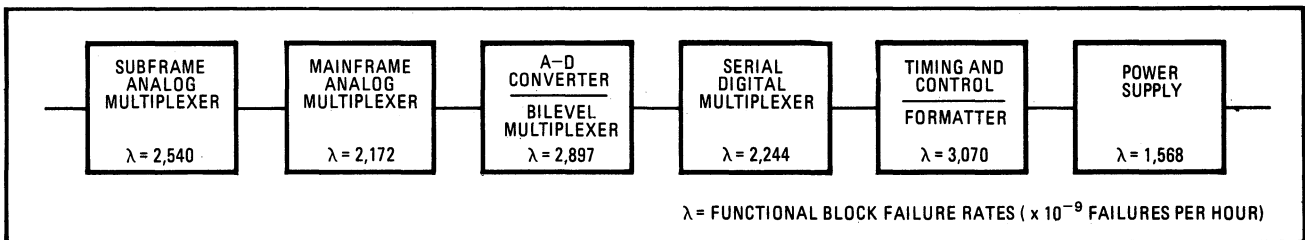
A reliability model of the encoder with each of the main functional areas and its failure rate is shown in Fig. 2. Failure rates are calculated by conventional methods for each function. Total encoder failure rate is simply the sum of the failure rates of each functional block.

Numerous tradeoffs determine the number of functions to be isolated. However, as will be seen later in partitioning for functional redundancy, it is generally desirable to structure the model so that the reliability of each functional block is approximately the same. Otherwise, one particularly unreliable functional block has a dominant effect on the total system reliability, and the capability of switching between parallel redundant functions elsewhere in the system becomes relatively meaningless.

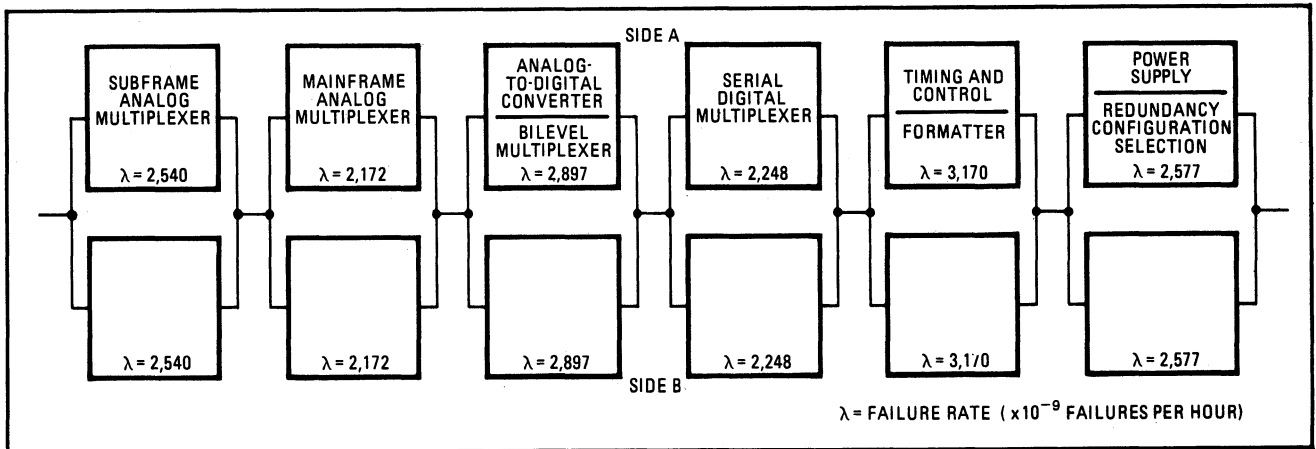
For this reason, the more reliable analog-to-digital converter and the bilevel multiplexer have been lumped together so that they form a single function. So also do

1. Typical subsystem. A PCM encoder is a good example of an electronic subsystem that can be readily partitioned into redundant functional blocks for enhanced reliability. Photo shows hardware required for the parallel-redundant encoder now used.





2. Nonredundant model. Reliability model for the nonredundant encoder shows its vulnerability to failure. Total failure rate (which in this case is $14,491 \times 10^{-9}$ failures per hour) is the sum of the rates for each functional block.



3. Functional redundancy. Reliability model for the functionally partitioned encoder cross-straps outputs of one stage to inputs of subsequent stages. Additional circuitry is needed to control the redundancy configuration through appropriate command switching. This added circuitry increases failure rates in some functional blocks over those in the model of Fig. 2.

the formatter and the timing and control circuitry.

Consider first the case of a nonredundant configuration. The total failure rate of the operating encoder is the sum of the individual component failure rates. In this case, the rate is $14,491 \times 10^{-9}$ failures per hour.

Reliability analysis

System reliability, or probability of the encoder's survival at some time in a given mission, is calculated from:

$$R_S = e^{-\lambda t} \quad (1)$$

where λ = the failure rate in failures per hour, and t = mission operation time, in hours.

The typical power-on operational time of the encoder is 5% of the total mission time. Inactive component failure rates (for components in a power-off or standby state) are estimated at 10% to 50% of the active failure rate. For the present example, a 50% figure will be assumed.

Thus, with an operational duty cycle of 5%, the failure rate becomes:

$$\lambda = (\lambda_{on}t_{on} + \lambda_{off}t_{off})/t = [\lambda_{on}(0.05t) + 0.5\lambda_{on}(0.95t)]/t = 0.525\lambda_{on} \quad (2)$$

where λ_{on} = failure rate of components in powered state

$$\lambda_{off} = 0.5\lambda_{on}$$

$$t_{on} = 5\% \text{ of mission time } t$$

$$t_{off} = 95\% \text{ of mission time } t$$

Substituting equation 2 in equation 1, we get:

$$R_S = e^{-0.525\lambda_{on}t} \quad (3)$$

Now consider two encoders in parallel standby redundancy. The operating unit has a compound failure rate of λ_1 , while the standby unit has a failure rate of λ_2

after it begins to operate, but otherwise has a failure rate of λ_3 . The reliability of such a configuration is: ¹

$$R_P = e^{-\lambda_1 t} + [\lambda_1 / (\lambda_1 + \lambda_3 - \lambda_2)] [e^{-\lambda_2 t} e^{-\lambda_1 t} + e^{-\lambda_3 t}] \quad (4)$$

where R_P = probability of survival of the two units in parallel

$$\lambda_1 = \lambda_2, \text{ since both units are identical}$$

$$\lambda_3 = 0.5\lambda_1$$

The parallel standby redundant configuration, however, is inefficient since the operational circuitry that is not affected by a failure may no longer be used. It is more efficient to partition the system circuitry functionally into smaller blocks of circuitry that can be activated on command, and so make the encoder redundant at this functional-block level. The reliability model of an encoder that has been partitioned in this way is shown in Fig. 3.

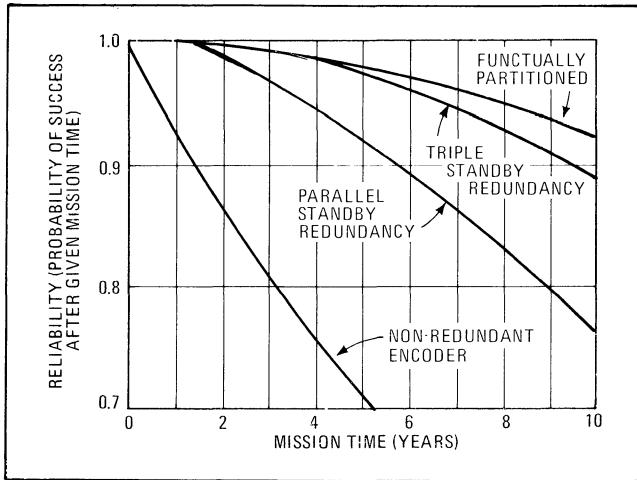
With the encoder partitioned into six parallel-redundant functional blocks, it can now be configured into 2^6 , or 64 possible combinations of functions to circumvent failures should they occur. Functional sections are activated by power switching. The reliability for each parallel stage is calculated using equation 4. The total system reliability is the product of the reliabilities of each of the six stages.

Note that in Fig. 3 the failure rates in some functional blocks have increased over those in the model of Fig. 2. These increases are due to the additional circuitry required to process the redundancy configuration command word, to switch power to activate functional blocks, and to provide fail-safe cross-strapping of signals between blocks. Overall, a 7.5% increase in components is required in this case.

The reliability for the functionally partitioned enco-

der is compared with the parallel redundancy configuration in Fig. 4 for mission times of up to ten years. As the graph indicates, functional partitioning achieves a very significant improvement.

The reliability of a triple redundant configuration (three units in parallel) is also plotted. Here, a marked improvement over parallel redundant configurations is also achieved, but the hardware, weight, and cost are in-



4. Reliability comparisons. By functionally partitioning an encoder into six parallel stages, it's possible to increase its reliability even beyond that achieved by placing three encoders in standby redundancy. At the end of a ten-year mission, the probability of success of such a functionally partitioned encoder is 0.9265.

creased approximately 50%. And for durations that are greater than about five years, triple standby redundancy is still noticeably less reliable than functional partitioning.

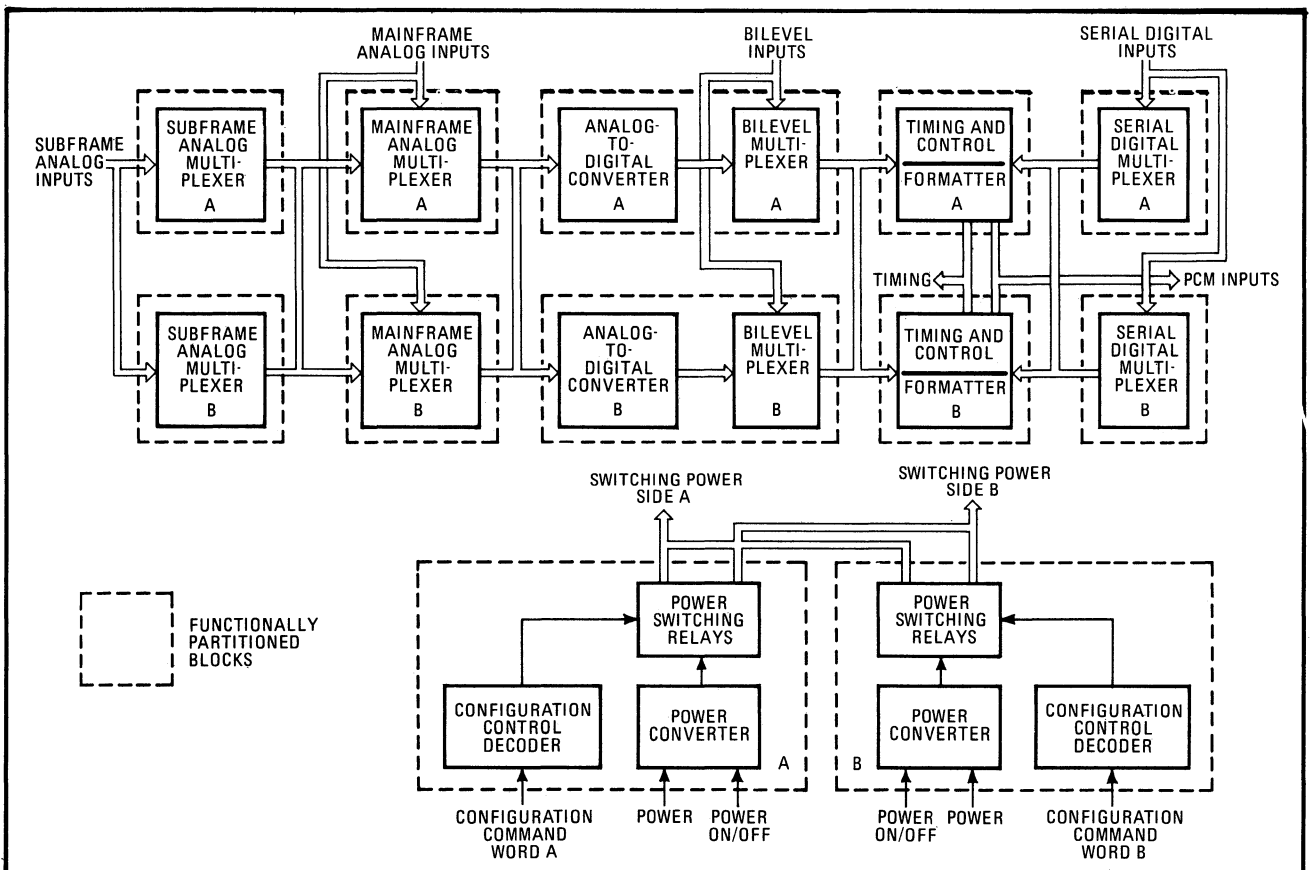
System features

The organization of a functionally partitioned encoder is shown in Fig. 5. Redundancy is controlled by a serial digital command word from a satellite command decoder.

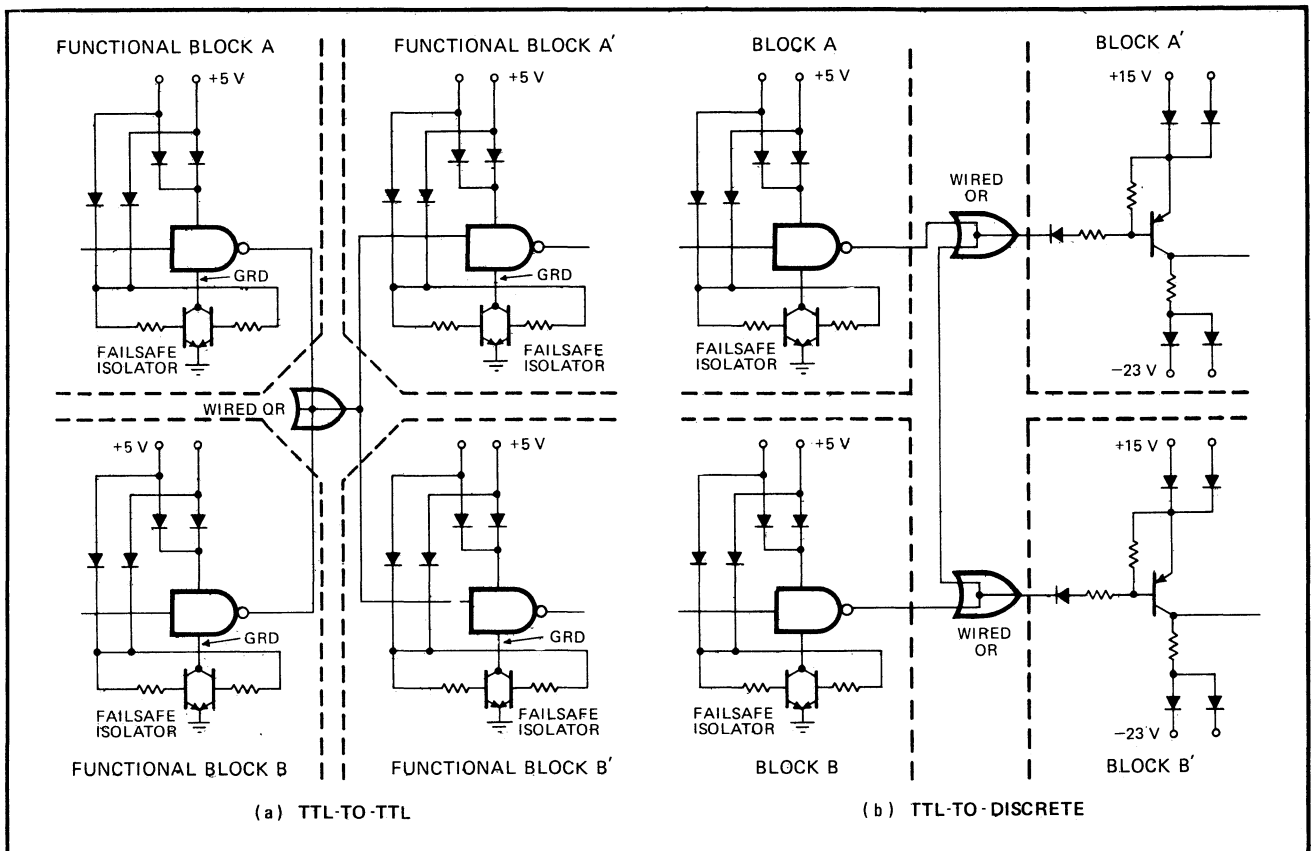
A command word initiates operation of electro-mechanical latching relays, which then switch power to the functional section to be activated. Such relays have the advantage over solid-state power switching, in that they maintain a given redundancy configuration even after a power on-off-on sequence. Because the relays are in a normally inactive state, their reliability is approximately equal to that of solid-state switches.

The state of each latch relay is sampled by the bilevel multiplexer and inserted in the data as a redundancy identification word for ground verification.

For increased reliability, the lines that cross-strap signals between the two sets of functional blocks must be protected against failures in one block that could affect the operation of its parallel-redundant block. A typical cross-strapping arrangement (Fig. 6a) connects TTL output gates in functional blocks A and B to TTL input gates in subsequent blocks A' and B'. To prevent failures due to internal shorting to ground at the TTL input or output, ground isolator circuits are provided to place



5. Signal flow. Redundant configuration is controlled by added decoding circuitry. Electromechanical latching relays select one of 64 possible combinations of operating blocks simply by applying or removing input power to the desired circuit function.



6. Fail-safe cross-strap. In the TTL-to-TTL interfaces generally used between functional blocks, (a), ground isolating circuits prevent a short-circuited input (or output) stage from grounding the signal line and so making the corresponding redundant block inoperable. Similarly, discrete circuits at the input to a functional block (b) can be isolated by input diodes.

a high impedance to ground when bias power is removed. Each ground-isolator transistor-pair is capable of isolating eight output (or input) signal gates from ground.

The diodes in the bias leads isolate the unused power supply. Similarly, Fig. 8 illustrates cross-strap between TTL gates and discrete circuitry. Here, diodes are used to isolate inputs to the discrete-circuit gates.

Controlling the blocks

In the redundancy control scheme, a six-bit word—one bit for each functional block pair—selects the desired redundancy configuration. Bits of synchronization and parity information can be added to the word to reduce the possibility of executing a word containing errors. In addition, the command word may be accompanied by an enable gate that envelops the command word. Then the command is executed on the enable gate's trailing edge.

Where it is not desired to have a serial command capability, a counter or stepping switch can be used which steps through each possible redundancy configuration. The counter or stepping switch is advanced by a transmitted tone burst. Variations of these techniques which allow any desired level of error control can, of course, be employed.

Conventional guidelines for packaging of high-reliability systems should not be overlooked. Of course, the fact that all the circuitry of the functionally redundant encoder is packaged in a single housing, in addition to

decreasing weight and size, also reduces the requirement for relatively unreliable interface connections.

In many cases, the circuitry allocated to a printed-circuit board is limited by the number of functions to be carried on and off the board through a single edge-board connector. Hard wiring of input and output signals circumvents this problem and at the same time increases reliability. Therefore, in high-reliability systems like the encoder, hard wiring of interfaces is preferred to the use of edge-board connectors.

The encoder described has been proposed for FLTSATCOM, the Air Force's next communications satellite program. A similar system has been proposed for the NATO-3 communications satellite, which will also be administered by the U.S. Air Force. And the use of functional redundancy partitioning seems certain in future satellite programs, both military and NASA, especially with a trend toward longer missions with higher investment stakes.

Reliable equipment making use of functional redundancy partitioning could also be incorporated into a number of terrestrial military communications systems, where a combat mission's success depends on uninterrupted communications links. Even in industrial electronic systems, a successful effort in reliability engineering can pay off handsomely in terms of lower maintenance costs and downtime. □

REFERENCE

1. Igor Bazorsky, "Reliability Theory Practice," p. 118, Prentice-Hall Space Technology Series, 1961.

Teaming a scope and counter clears up ambiguities

This combination of instruments, which displays what signals are triggering the counter, can check frequencies, parts of waveforms, pulse widths, timing between pulses, and bursts; the setup can also count errors

by Neil A. Robin, Tektronix Inc., Beaverton, Ore.

□ Most engineers have probably connected a counter to a circuit at one time or another and found more than one stable answer. There's something wrong, but the question is—where?

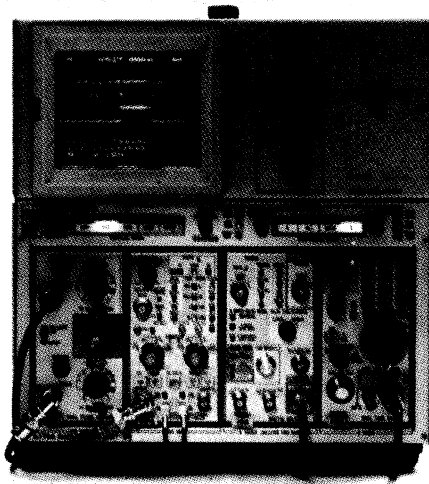
The problem probably isn't in the counter, but in certain characteristics of the signal that cause the counter's trigger circuits to fire at the wrong time. It would help to be able to see what the signal looks like, and more importantly, to understand how the counter's trigger circuits recognize it.

One of the best ways to solve this problem for most counter measurements is to use a dual-trace oscilloscope to display certain signals from the counter, along with the input signal. There isn't much of a problem with an ideal source, such as a signal generator, but most measurements are far from ideal. In addition, counter specifications usually cover sensitivity, bandwidth, and impedance, but the engineer doesn't always know his counter's overdrive characteristics or what happens under certain noise conditions.

For example, an input signal may have an amplitude of 11 volts peak-to-peak with a signal-to-noise ratio of 40 decibels. If the counter has a sensitivity of 100 millivolts peak-to-peak, the counter will be sensitive enough to respond to the noise, as the noise level equals 110 mV peak-to-peak. The net result can be a serious malfunction of the counter.

Whether dealing with random or synchronous noise or using the instrument in frequency- or time-measurement mode, the net result of the reading can vary considerably. One example is ringing on the baseline, which may be greatly exaggerated in the counter's trigger circuits, thanks to the counter's sensitivity. Such errors can be overcome by adding a dual-trace oscilloscope to the counter.

For measuring frequency, the Schmitt trigger of the counter would be valuable as a waveform. In time-measurement modes, the counter gate would be effective. This dynamic combination can selectively measure part of a waveform, use the delayed-sweep gate to measure



pulse width and timing between two pulses, measure bursts, and count errors. The user enjoys an added measure of confidence when he can see on a scope the true representation of the signals in these situations.

Figure 1, an example of a frequency measurement with the Schmitt-trigger output displayed, shows how misleading an answer can be. It's one thing to know there is something wrong, but with the scope display, the user can see what's going on and make adjustments to correct the misleading counter reading.

Selective measurements are also easier to set up by combining the dual-trace oscilloscope with the counter. When the user wants to check a particular segment of the waveform with the counter, the scope is almost a must because it can verify the part of the waveform actually being measured. The upper trace in Fig. 2 is from a time-division-multiplex (TDM) pulse-width-modulation (PWM) system. If the width of the third pulse is to be measured, the digital counter is "armed" by the delayed-sweep gate, shown as an intensified zone. A glance at the lower trace, representing the counter-gating response, verifies that the measurement is, in fact, being made during the third pulse interval.

Not all counters have these signals available at the rear panel. For those that do, delays between input signal and counter signal should be matched when presented to the oscilloscope.

Using the scope's delayed-sweep gate

The delayed-sweep gate of a dual-time-base oscilloscope is a useful signal that can be applied to counters. In most such oscilloscopes, the first time base is called the main, or delaying, sweep. This is the normal sweep used for the majority of applications. The other time base is derived from the delayed sweep, which obtains its trigger from a comparator circuit on the main sweep.

When the comparison voltage and the sawtooth voltage of the main sweep reach equal magnitudes, a comparator circuit either triggers the delayed sweep to begin at that time or allows it to accept a trigger pulse that

starts it from that period of time. Thus, by changing the comparison through the front-panel control, it is possible to “walk” the start of the delayed sweep across the entire width of the interval of the delaying sweep.

The delayed-sweep gate is the logic signal that corresponds in time to the interval of the delayed sweep. It is used to unblank the CRT trace internally whenever the delayed sweep is used, but it is often available externally, as well. On some scopes, its magnitude is +5 volts unterminated, about +0.5 v into a 50-ohm load. The low state is about 0 v.

Now the measurement in Fig. 2 becomes clearer. The figure shows a TDM/PWM telemetry signal. Each pulse represents an individual channel of information, and its width represents the analog magnitude of the modulating voltage for that channel.

To measure the width of the third pulse by a digital time-interval counter, the main sweep for the scope must first be synchronized with the framing pulse of the telemetry signal so that it's possible to display the various channels of the signals at fixed points on the CRT.

By running the delay-time control of a delayed-sweep time base over to a point just ahead of the third pulse of the sequence, it's possible to start the counter just before that pulse; that is, if the counter has the correct input circuits to perform this type of measurement. This requires a counter that can be armed by using the delayed-sweep gate to accept an input signal.

This arming method adds visual control to the measurement, while retaining the full accuracy of the counter. For long intervals, analog methods of measuring time cannot compare to this digital method.

In addition, the intensification of the trace, caused by the delayed sweep gate in Fig. 2, makes it easier to locate the gate's position. Because the start point of the delayed sweep is arbitrarily selected by the delay-time control, it's just as easy to select any other pulse. In any case, the feedback to ensure that the measurement was made in the correct place is the gating response of the counter, shown as the lower trace on the CRT.

The example of measurement by a delayed-sweep gate covers a signal only four channels long. For a signal containing hundreds of channels, lining up all the pulses on one trace of the CRT would create a mean-

ingless blur. Instead, digital delay by events-counting can be a worthwhile means to measure some characteristic of a long sequence of pulses. The idea is to count out the prescribed number of pulses to be measured to the starting point.

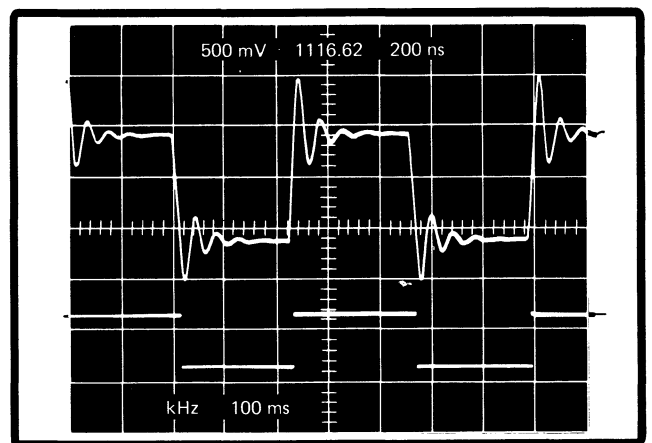
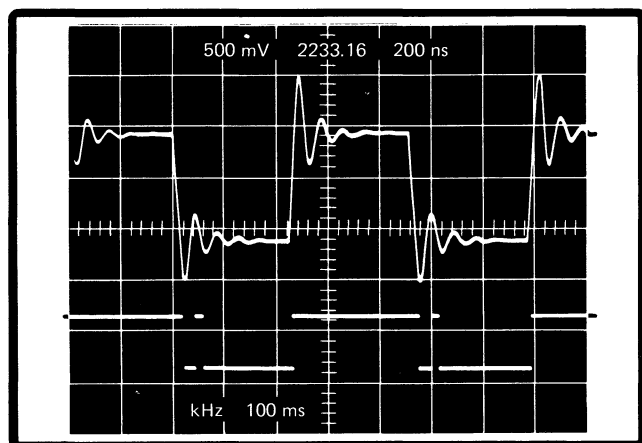
For example, Fig. 3 shows a long sequence of pulses for which the time elapses between two specific but nonconsecutive pulses. This is shown at the top of Fig. 3. The middle trace (counter gate) has revealed that the counter has indeed measured the elapsed time between the two nonconsecutive pulses. The procedure is similar to that of Fig. 2, but here a plug-in digital-delay unit is used to delay the main sweep starting point.

The technique demonstrated in Figs. 2 and 3 suggests another advantage in using the delayed-sweep gate to control counter measurements. Because the width of this gate and its corresponding sweep length are continuously adjustable, both the start and stop points of the digital time-interval counter can be armed, thus providing a selective window for making a measurement at any point desired, which can be identified on the scope.

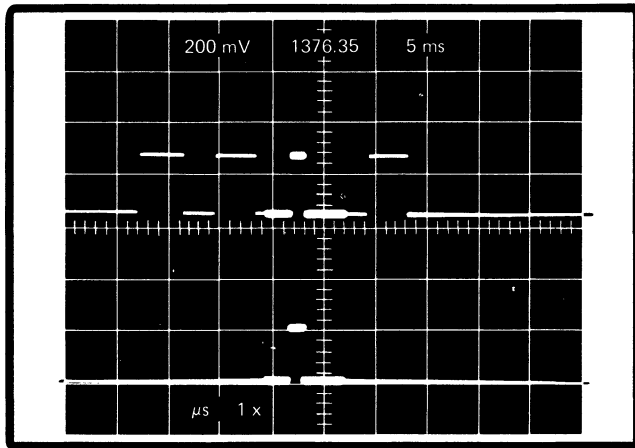
To take advantage of this technique, it's necessary to have a counter that is designed to accept a positive signal for arming the start point and a negative signal for the stop. This means when the delayed-sweep gate triggers a logic 1, the counter is armed for a new measurement, and when the gate flips to logic 0, the counter accepts a stop pulse. Thus, the variable width of the delayed-sweep gate gives added control.

This feature is especially important when the logic of conventional universal-counter timers is not adequate to perform an elapsed-time measurement. For example, in Fig. 3, one pulse in the measurement is ignored. This is because the width of the delayed-sweep gate is wide enough to prevent arming of the stop circuits until after this ignored pulse has passed. The width of the delayed-sweep gate is adjustable so that it can determine start and stop points, as in Fig. 3. Here again, the scope shows exactly what the counter is measuring—that is, that the counter is ignoring one pulse.

Besides the capability to arm a counter for time-interval measurements, the technique can determine the frequency and period of waveforms. An example is burst measurements. Many electronic systems contain keyed



1. Counter ringing. A lower trace, left, represents response of counter Schmitt trigger to the upper trace, and the frequency count—2,233.16 kHz—is steady, but incorrect, because of double counting caused by the counter's sensitivity. After the trigger level disappears, and the reading at the right—1,116.62 kHz—is correct.



2. Armed for counting. To measure width of third pulse, digital counter is armed by delayed-sweep gate (intensified zone). Lower trace represents counter's gating response, which verifies measurement is made during third pulse interval.

tones or keyed rf signals, and it is often necessary to know the frequency of the signal during the burst interval. Frequency measurement by conventional digital counting is not always effective for this type of signal because the duration of the burst is usually too short.

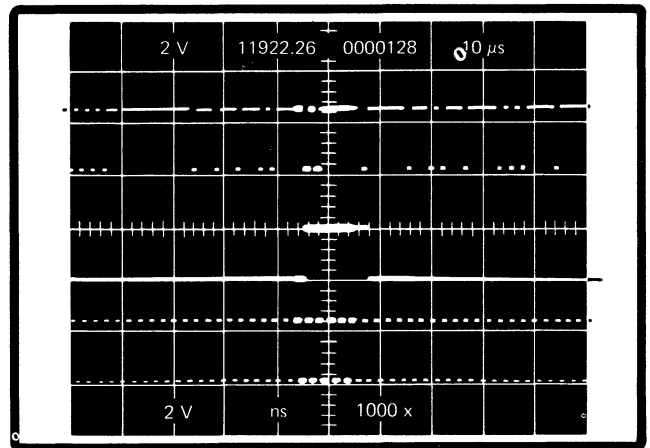
Computing counters of various degrees of sophistication that can measure the period of the signal and compute the frequency have been on the market for several years. Not all can be armed, however. For those with arming capability, a dual-trace oscilloscope makes this type of measurement and computation comparatively simple. In the typical situation shown in Fig. 4, the counter is armed well into the burst interval. This helps to prevent any distortion of the signal at the turn-on point from causing a false answer. Of course, the period can be averaged, so long as the measurement is terminated before the end of the burst interval.

Another handy task the delayed-sweep gate can perform is error-counting. If the counter is gated to accept an input signal for the width of the delayed gate, it is possible to count events that occur during this interval. This is a good feature when not only the number of error pulses is important, but also their timing.

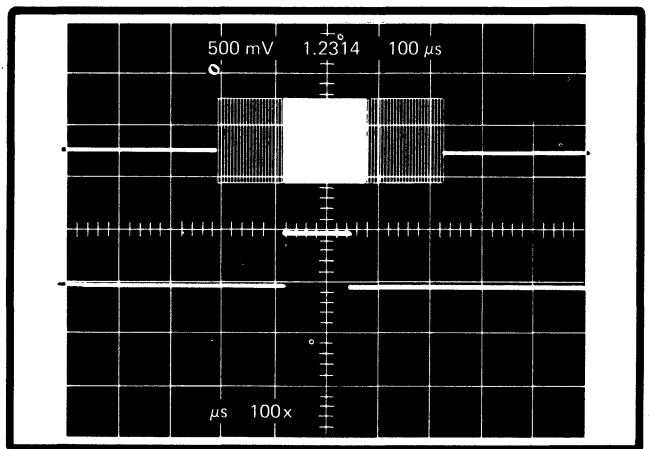
Various comparison measurements can also be made by measuring the width of the delayed-sweep gate with the digital counter and displaying the counter-gate signal on the screen. This technique doesn't have nearly the accuracy potential of the arming methods, but it is convenient, and the results are probably better than those obtained by simply reading divisions off the graticule, which may introduce errors caused by horizontal time-base nonlinearity.

A slightly different approach is to measure a digital time interval from the sawtooth waveform of the sweep. The start and stop points can be picked off independently and smoothly, since the ramp waveform has a gradual slope. However, noise can be a significant factor in determining the start and stop points accurately.

On most oscilloscopes, whenever the main sweep is displayed and the delayed sweep is running, an intensified zone on the screen corresponds to the period during which the delayed sweep coincides with the main or delaying sweep. Some users have contended that the Z-



3. Good timing. For determining interval between two non-consecutive pulses, measurement is made from negative edge of first pulse (intensified) to positive edge of second pulse following. Answer, an average of 1,000 samples, is 11,922.26 ns.



4. In a burst. Upper trace represents a typical burst waveform. The counter is armed to measure the period of the burst signal—answer, an average of 100 periods, is 1.2314 microseconds.

axis modulation could show timing relationships when a digital counter is used. However, this method is not advisable because of the signal delays involved. The vertical-amplifier signal usually travels through a delay line, while that of the Z axis does not. Also the Z-axis bandwidth is usually far short of the vertical channel's bandwidth.

The scope as preamplifier

Many overlook the vertical amplifier section of an oscilloscope. On a scope equipped with a vertical amplifier, it's often easy to connect a counter to the "vert sig out" jack and take advantage of the much more sensitive unit that results. Typical output levels run about 0.5 V per division unloaded. With a high-gain vertical amplifier, net sensitivities of the counter will amount to 2 microvolts if the counter has a built-in sensitivity of 100 mV peak-to-peak.

In a plug-in oscilloscope, such as the Tektronix 7000 series, a counter-timer that is available can, when plugged directly into the mainframe, route the preamplified vertical signal internally to the counter. Usually referred to as the trigger-source signal, this signal triggers the horizontal time bases in the internal mode. □

Matching driver circuitry to multidigit numeric displays

It is worthwhile for the designer to choose the optimum combination of parallel and serial circuitry to drive the output elements, rather than simply making tradeoffs between various readout devices

by Alan Sobel, Zenith Radio Corp., Chicago, Ill.

□ All too often, the design of an electronic numeric display system is based primarily on the characteristics of the various display devices available, with only secondary regard for the necessary driver circuitry. However, the display-system designer will find it profitable to consider such important criteria as driver power, element-switching time, and decoding-circuit complexity.

For a particular application, there may be several system organizations that can give low total cost and good performance. To find these, however, the characteristics of the output elements and the drive electronics must be considered together.

Display-system organization

The design of a display system must begin at the source of the information to be displayed. This may be the output of a counter or an analog-to-digital converter, for example, and it may have such outputs as binary or binary-coded-decimal (BCD). The display device, on the other hand, may require a drive system for seven-segment digits, seven-by-five-element dot matrixes, or some other format. All digital readouts considered in this discussion contain more than one digit, and it is therefore often desirable for corresponding segments of several digits to time-share a common driver.

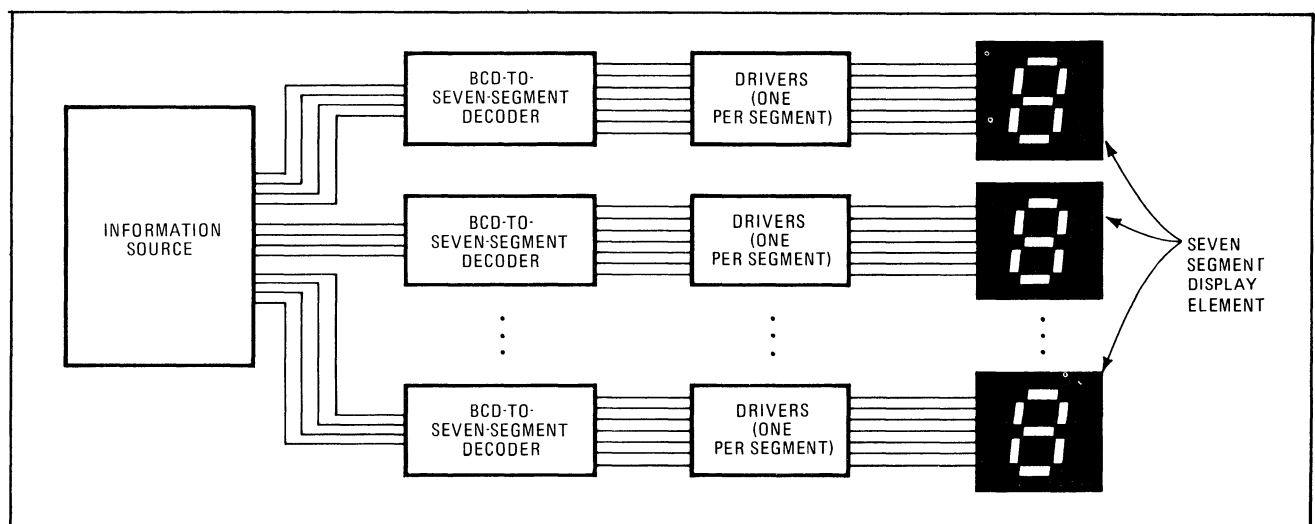
For such multidigit display systems, there are two fundamental drive-system configurations—full-parallel and matrix. Most practical display-system designs are compromises between the two. The “full-parallel” configuration (Fig. 1) is simpler, but usually more expensive. Because separate lines from the information source are routed to each individual digit in the display, each set of lines from the source is translated in the decoder to the format required by the drivers and the display devices. Using the full-parallel configuration, the duty cycle of each of the energized digits is, for all practical purposes, 100%.

Such a full-parallel display, however, requires a maximum amount of circuitry, since a decoder and driver must be supplied for each digit. The “matrix-drive” configuration (Fig. 2), which reduces this hardware requirement, is also called a “full-serial,” “strobed,” or “multiplexed” display system.

Matrix-driven display

Although it reduces hardware needs, the matrix design is more complex, and it makes tougher demands on the display elements. Thus, a careful analysis of the total system is necessary in order to make a proper choice between the two.

In matrix configurations, data from the source feeds a



1. Full parallel. In the most straightforward approach to display-system design, one decoder and seven drivers are required for each digit. Such designs, however, are generally wasteful of decoding and drive-circuit hardware in displays of more than three or four digits.

single decoder, either over a single set of lines, which is switched in the source from digit to digit, or via a switch that takes the information from the individual digit sources and transmits it sequentially to the decoder. Corresponding segments of each digit are connected together, and the particular digit to be energized is selected by activating another switch.

Besides reducing the number of decoders, the number of drivers required in a multidigit display can also be substantially reduced. In a 10-digit display with seven elements per digit, for example, the matrix configuration would require 17 drivers, in contrast to the 70 that would be required in the full-parallel approach.

Most numeric display and driver configurations today fall somewhere between the full-parallel and the matrix systems. For example, a single decoder can be time-shared among separate sets of drivers for each digit, but the drivers may include storage capability to keep each element energized for a duty factor close to 100%. Such an arrangement, shown in Fig. 3, has 28 drivers (seven segments times four digits). The particular design shown has been used for a digital-voltmeter readout.

Duty factor and repetition rate

In the matrix arrangement, the operating duty factor for each digit cannot be larger than $1/n$, where n is the number of digits in the display. The duty factor will usually be less, since time must be allowed for the new information for each digit to be transmitted to the decoder. Some display devices (multiple-digit gas-discharge devices, for example) may require dead times between adjacent digits to avoid inadvertent illumination of elements when they should be off.

Average light output is the peak output times the duty factor. Therefore, to radiate, say, 50 foot-lamberts average luminance from each element in a 10-digit display, each digit must generate at least 500 foot-lamberts

while on. Some devices, like gallium-arsenide-phosphide light-emitting diodes, thrive on this pulsed treatment. Other devices, however, simply cannot meet the instantaneous requirements in some applications. Limitations on the peak-output capabilities for some devices, then, limit the number of digits that can be multiplexed. Thus, to maintain adequate luminance for each display element, it may be necessary to divide a display-drive matrix into several smaller matrixes.

The lowest frame-repetition rate is fixed as the lowest rate at which the devices can be operated without noticeable flicker. This is typically 30 frames per second, although in applications where the device is subjected to a great deal of vibration, it may be desirable to use repetition rates as high as several hundred frames per second to avoid annoying breakup of the display. On the other hand, the highest frame rate is sometimes limited by switching times of the display elements used (see table, p. 99).

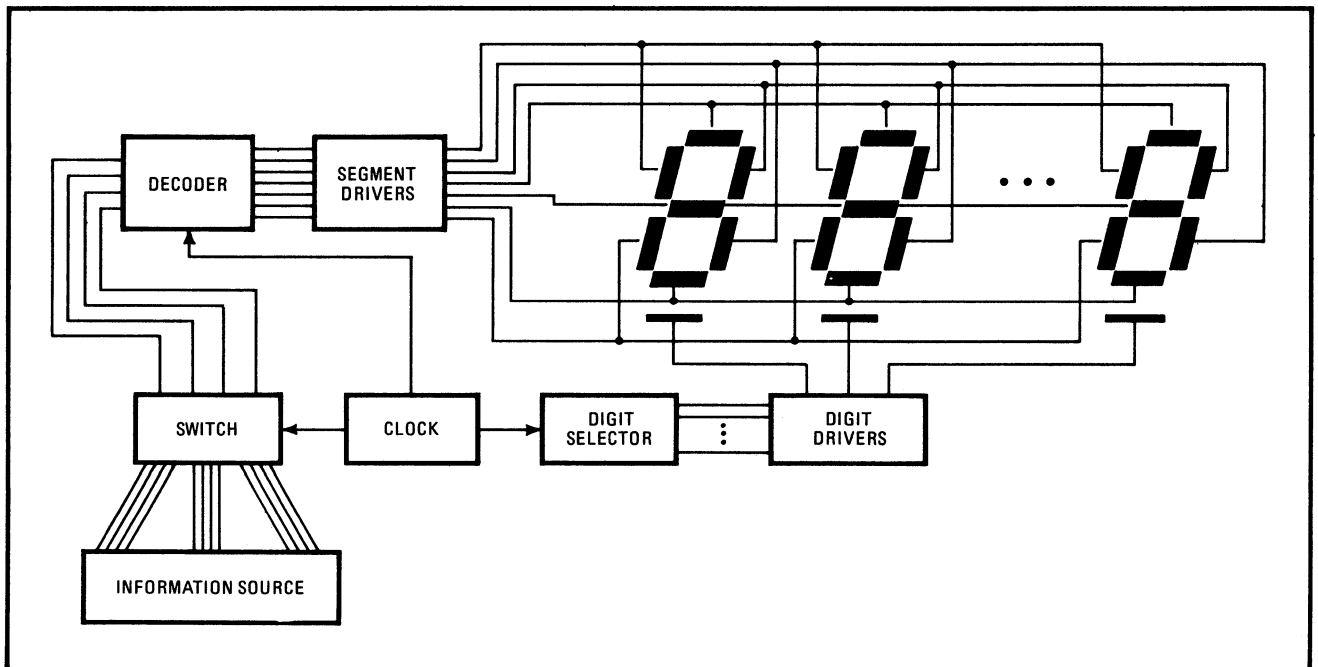
How duty factor affects contrast

Specifications concerning brightness and ease of viewing a display are partly established on the basis of subjective factors, but probably the most important criterion for legibility—and an important factor in designing matrix-drive systems—is contrast. If the duty factor is less than unity, both the output of the display and the contrast, that is, the ratio of output from an on segment to that from an off segment, will be reduced. (The ratio of output from a segment to light scattered from the surroundings will also be reduced.)

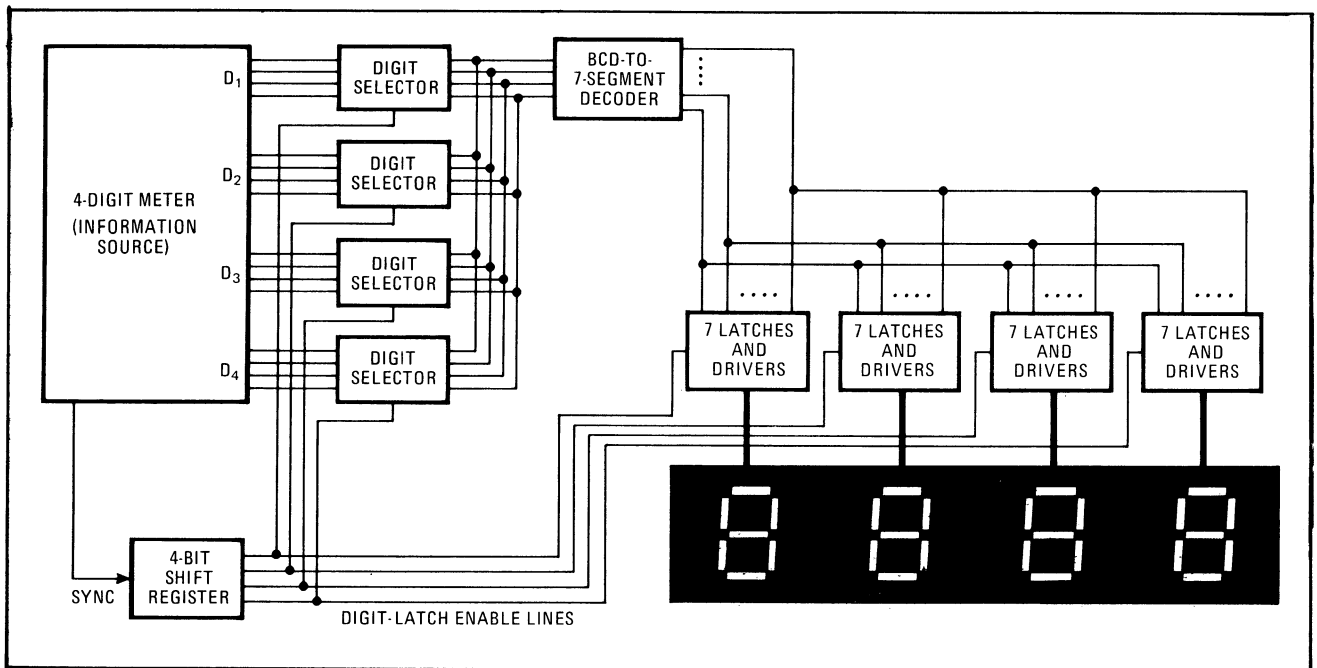
An off segment is not totally blank; it scatters some ambient light, and it may also be energized partially by undesired current paths in the drive matrix. The output of an energized device, then, is:

$$L_{on} = CL_{off} \quad (1)$$

where C is the contrast ratio and L_{off} is the output of the



2. **Matrix magic.** When displays are matrixed, fewer decoders and drivers are required than in the full-parallel system in Fig. 1. The relative advantage of the matrix system is increased further as more digits are added to the display.



3. Voltmeter readout. For use as a voltmeter readout, this system trades an increase in decoder circuits for less complex selector switches and latching circuits. Latches are synchronized with the digit selectors. Thus, each element is energized with a duty factor of nearly 100%.

device that is off. Because of the duty factor, F , of matrix displays, the effective contrast ratio is:

$$C_{\text{eff}} = [FL_{\text{on}} + (1 - F)L_{\text{off}}]/L_{\text{off}} \quad (2)$$

which combined with Eq. 1, reduces to:

$$C_{\text{eff}} = F(C - 1) + 1 \quad (3)$$

The importance of the difference between contrast and effective contrast can be seen by plugging numbers in for typical display situations. In an LED display, for example, if $C = 10$ and $F = 1/4$, then the effective contrast is only $3\frac{1}{4}$, while for a display contrast of 50 and $F = 1/10$, C_{eff} is only 5.9.

Alternatively, if an effective contrast of 10 is needed in a particular application, and the duty factor is $1/10$, then a display element must be chosen with contrast of 99. Such a requirement is not impossible for a light-emitting display, particularly if appropriate filters are used over the elements.

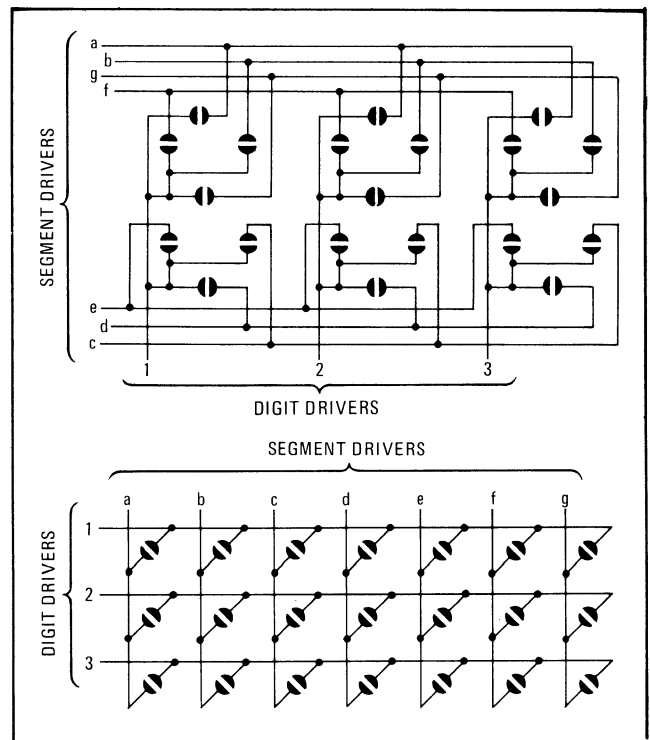
Filter can optimize contrast

If the effective contrast is found to be less than desirable for a given combination of drive technique and display elements, filters can often be used to improve viewing ease. A neutral filter (one with a constant output over a broad range of light wavelengths) attenuates both the ambient light and the output of the device equally.

However, the ambient light is attenuated in two transits of the filter, while the light from the display passes through the filter in only one direction. The result is a net gain in contrast at the expense of luminance. It has been shown¹ that the effective contrast when using such a filter is:

$$C_{\text{eff}} = [F(L_{\text{on}} - L_n)/L_n + L_aSG] + 1 \quad (4)$$

where L_n is the light output from an unenergized element with no ambient light, L_a is the ambient illuminance, and G is the filter transmission. The quantity L_aS is the output of scattered light from a display ele-



4. Three-digit multiplex. Three seven-segment numeric elements (a) are multiplexed for better drive-circuit utilization. The same circuit is redrawn in (b) to illustrate the three-row, seven-column matrix configuration, and the matrix is further restructured in Fig. 5 to better explain the effects of parasitic driver currents.

ment, assumed to be unaffected by whether the element is energized or not.

From Eq. 4, it is readily seen that the effective contrast increases substantially as the filter transmission decreases. Again, plugging in numbers for a typical 10-digit LED matrix-driven display illustrates the point. In

such a system, $F = 1/10$, $L_{on} = 500 \text{ fL}$, L_n is negligibly small, and $L_a S = 30 \text{ fL}$. Then for $G = 1$, $C_{eff} = 2.67$; or $G = 0.5$, $C_{eff} = 4.3$, and for $G = 0.1$, $C_{eff} = 17.7$.

These increases in contrast come at the expense of luminance, which in this example decreases from 50 fL for $G = 1$ to 5 fL for $G = 0.1$, since output luminance is $L_{on}FG$. Sacrificing luminance for increased contrast is generally desirable, however, because in low-light environments, display brightness is not needed, while in brighter surroundings, there is usually still sufficient contrast for the display to be read.

The use of a colored filter that matches the wavelength of the display element output can be even more effective than the neutral filter. A typical red filter matched to a red GaAsP LED, for example, can increase contrast by as much as tenfold without attenuating the desired output by more than 30%.

Depending on the application and the environment, circular polarizers and other types of filters may also dramatically attenuate light reflected from the display device and impose a relatively small penalty on the device output. For devices such as some liquid-crystal displays that operate by modulating ambient light, performance cannot be improved by neutral filters, since these will attenuate both useful and undesired light by the same amount.

Many light-modulating displays exhibit persistence, a sometimes desirable characteristic that has the effect of making the duty factor larger than the ratio of excitation time to frame time.

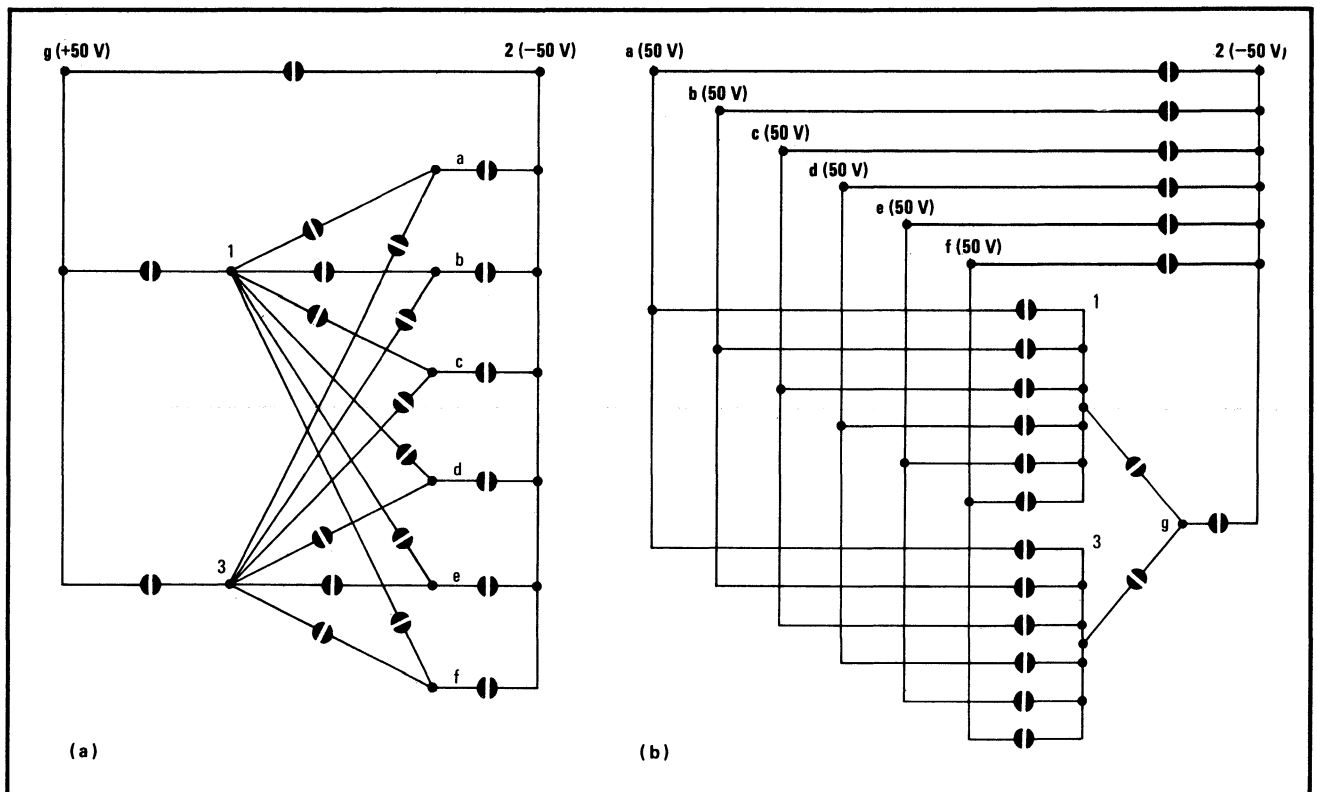
To illustrate the effect of persistence, consider a display with element contrast of 10 and a duty factor of $1/4$. If the element turns on rapidly but turns off slowly, so that once energized, it remains on for $3/4$ of the frame time, the effective duty factor is $3/4$. In such a display, the effective contrast will be improved from $3\frac{1}{4}$ to $7\frac{3}{4}$. This is one of the reasons that some liquid-crystal devices can be multiplexed effectively, despite their lower contrast. The slow response of the liquid crystal, however, may be unacceptable in some applications.

Keeping off-elements off

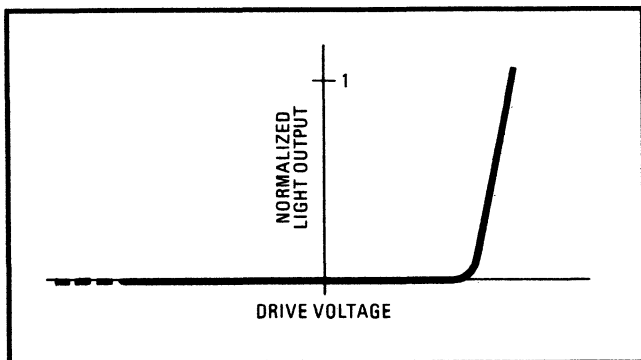
A second fundamental limitation of matrix-drive systems—the unwanted energizing of unselected segments because of parasitic currents in the matrix—is illustrated by the three-digit display in Fig. 4a. Each digit in the example consists of gas-discharge elements, arranged in seven segments. The same array is redrawn in Fig. 4b to show more clearly the matrix arrangement.

If a single segment of the second digit is energized (as shown in Fig. 5a for the display of a minus sign), a full 100 volts appears across the desired segment.^{2,3} In this case, the signal path is from segment-driver g to digit-driver 2.

However, a substantial fraction of this voltage can appear across the g segments of digits 1 and 3, as well as across all the other segments of digit 2. Depending on source impedances and current-sinking capabilities of the drive circuits, unselected segments may be lit. The problem of turning on unwanted segments gets worse as



5. Sneaky currents. Parasitic currents within a display matrix must not inadvertently turn on unselected segments. In case (a), where only segment g of digit 2 is biased on, a total of 100 volts is placed between nodes g and 2. All other nodes are driven at 0.0 V. Since most gas-discharge segments start to turn on at about 80 V, no other segment will light up. However, if two segments are driven on (as for displaying the number 1) some of the unselected segment driver outputs may begin to rise above 0 V. This problem becomes most severe when all but one segment is biased on (as for displaying a zero, shown in b).



6. Ideal matrix device. Ideal element for matrix displays is highly nonlinear (there is no light output when biased below a given threshold) when forward-biased, and it emits no light when reverse-biased.

more selected segments are biased on, and it is worst when all but one segment are biased on (as for displaying a 0 in 5b). Here, parasitic currents from six segments converge on nodes 1 and 3. If not adequately clamped to 0 volts, segment g of digit 2 could be turned on. To keep this unselected segment from turning on, it is therefore necessary to provide a low impedance with adequate current-sinking capability at the digit-drivers so that they are clamped to 0 v.

On the other hand, segment-drivers should generally have high output impedances. This makes the drivers look like constant-current sources to the segment elements, and it gives uniform illumination from each diode in the display.

The matrix arrangement will work only if each display element is nonlinear and has a well-defined threshold, as shown in Fig. 6. Even if the digit drivers in Fig. 5b have zero impedance, half the applied voltage will appear across all segments, except g of digits 1 and 3. If half the applied voltage is below the knee of the curve in Fig. 6, there will be no output, but if the knee of the input-output curve is not well-defined, the unselected segments will begin to light up.

Choosing the best element

For display devices that do not have sharp thresholds, nonlinear elements can be inserted in series (such as diodes in series with incandescent filaments). Or for dynamic-scattering nematic liquid crystals, two-frequency operation can be used.^{4,5,6} The amount of softness of the knee that can be tolerated depends on the number of digits in the matrix and the contrast required. Because of the additional display elements needed, the nonlinearity requirement is generally more rigorous for dot-matrix digits than for seven-segment digits.

Typical characteristics of the more common display elements are compared in the table. The quantities provided are intended only to give general comparisons of today's performance. Detailed data must, of course, be obtained from each manufacturer's product specification sheets.

The over-all attractiveness of the LED for matrix displays is readily apparent in the table. In addition to having excellent input-output curves, LEDs can be switched in about 1 microsecond, and they have excellent luminance. Their efficiencies are low, however, and their deep red output is difficult for some people to see.

TABLE: LEADING DISPLAY ELEMENT CANDIDATES WITH TYPICAL CHARACTERISTICS MOST AFFECTING DRIVE CIRCUIT CONFIGURATION

| Device type | Relative brightness/contrast | Typical switching time | | Input-output curve* |
|-------------------------------|------------------------------|------------------------|-------------|---------------------|
| | | On | Off | |
| Light-emitting diode | Good to excellent | 1 ns | 1 ns | |
| Gas-discharge tube | Excellent | 5-10 μs | 100 μs | |
| Thin-film electro-luminescent | Excellent | 100 μs | 1 μs | |
| Liquid crystal | Fair to good | 5 to 10 ms | 10 to 20 ms | |
| Incandescent | Excellent | 15 ms | 20 ms | |
| Vacuum fluorescent | Good | 5 μs | 50 μs | |

*Curves normalized to typical full-scale light output (Y-axis) and to drive excitation magnitude (X-axis)

Gas-discharge devices also lend themselves to matrix displays, while liquid crystals, with their more linear input-output curve and their dependence on ambient light, have thus far been primarily limited to use with parallel-type drive systems.

Incandescent elements have been used in multiplexed displays of two to four digits, but difficulties in obtaining the higher peak power required in displays with more than about four digits have so far tended to inhibit their use in larger displays.

There are also a few less-well-known candidates for use in matrix displays. Fluorescent displays have been used successfully in multidigit matrix-type displays, especially where small size has been a requirement. Also, electroluminescent displays, while requiring a high-voltage ac drive, are capable of excellent contrast. □

REFERENCES:

1. Sobel, Alan, "Duty Factor and Contrast in Scanned Displays," Proc. IEEE, Vol. 57 pp. 1,758-1,761, October 1969.
2. Sobel, Alan "Selection Limits in Matrix Displays," Proc. 1970 IEEE Conf. on Display Devices.
3. Sobel, Alan, "Some Constraints on the Operation of Matrix Displays," IEEE Trans. Electron Devices, Vol. ED-18, pp. 797-798 September 1971.
4. Wild, Peter J., and Nehring, Jurgen, "Turn-on Time Reduction and Contrast Enhancement in Matrix-Addressed Liquid-Crystal Light Valves," Appl. Phys. Letters, Vol. 19, pp. 335-336, Nov. 1, 1971.
5. Stein, C.R., and Kashnow, R.A., "A Two-Frequency Coincidence Addressing Scheme for Nematic-Liquid-Crystal Displays," Appl. Phys. Letters, Vol. 19, pp. 343-345, Nov. 1, 1971.
6. Gooch, C.H., and Low, J.J., "Matrix-Addressed Liquid-Crystal Displays," J. Phys D: Appl. Phys., Vol. 5, pp. 1,218-1,225, 1972.

The charge-balancing a-d converter: an alternative to dual-slope integration

Like dual-slope analog-to-digital conversion, the new technique basically is an integration scheme; but simple design and relaxed tolerances on components may give it an economic edge in some applications

by Robert C. Kime, Jr., *Keithley Instruments Inc., Cleveland, Ohio*

□ Given the problem of designing a cheap, simple, reliable analog-to-digital converter that exhibits high accuracy and low power consumption, most engineers will probably first think of the dual-slope converter. Recently, however, the charge-balancing converter was developed for pretty much the same purpose.

The two circuits have much in common. Both center on charging and discharging a capacitor, both are integrating circuits, both are quite economical, and neither will ever set a conversion speed record.

But the techniques are not identical, and one or the other may prove superior in any given application. The dual-slope unit can be designed to have outstanding normal-mode rejection at one particular frequency, so that line rejection is very easy, while the charge-balancing converter can generally be implemented with fewer parts and with looser component specs.

Basically the dual-slope converter works by applying the unknown input signal to an uncharged capacitor for a fixed length of time, and then measuring the time needed to discharge the capacitor at a constant rate. In the charge-balancing converter, however, there is no fixed charging period, and the charging continues for as long as necessary to get the capacitor voltage to cross a fixed threshold level; then a reference current is subtracted from the input current, and the capacitor discharges until the threshold level is crossed again. The process repeats itself until the conversion period is over. At that time, a counter, which only accumulates clock pulses when both the input signal and the reference current are applied to the capacitor, contains a number of counts proportional to the input voltage.

One conversion cycle

The charge-balancing unit got its name from the fact that the net charge put into an integrator over one integration cycle is zero. The converter (Fig. 1), which accepts only positive input voltages, operates as follows. Initially the current switch is open, and only the input voltage is applied to the integrator. Since the integrator contains an inverting operational amplifier and a capacitor, the output voltage, V_o , is a negative-going ramp that has a slope proportional to V_{in} .

As V_o passes the threshold level, V_d , of the threshold detector, the detector's output voltage, V_t , switches to a logic 1 state which, among other things, opens a gate that allows the counter to start accumulating clock pulses.

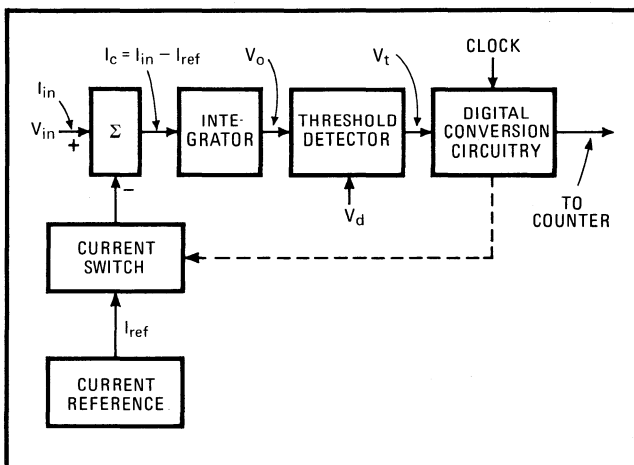
It also makes a flip-flop close the current switch on the next clock pulse. Closing this switch causes the known, constant reference current to be subtracted from the input current. The difference current is applied to the integrator as before.

The reference current is chosen to be greater than the input current for all allowable input voltages, so that subtracting the reference current, I_{ref} , from the input current, I_{in} , is guaranteed both to change the polarity of the input to the integrator and to start V_o on a positive-going ramp.

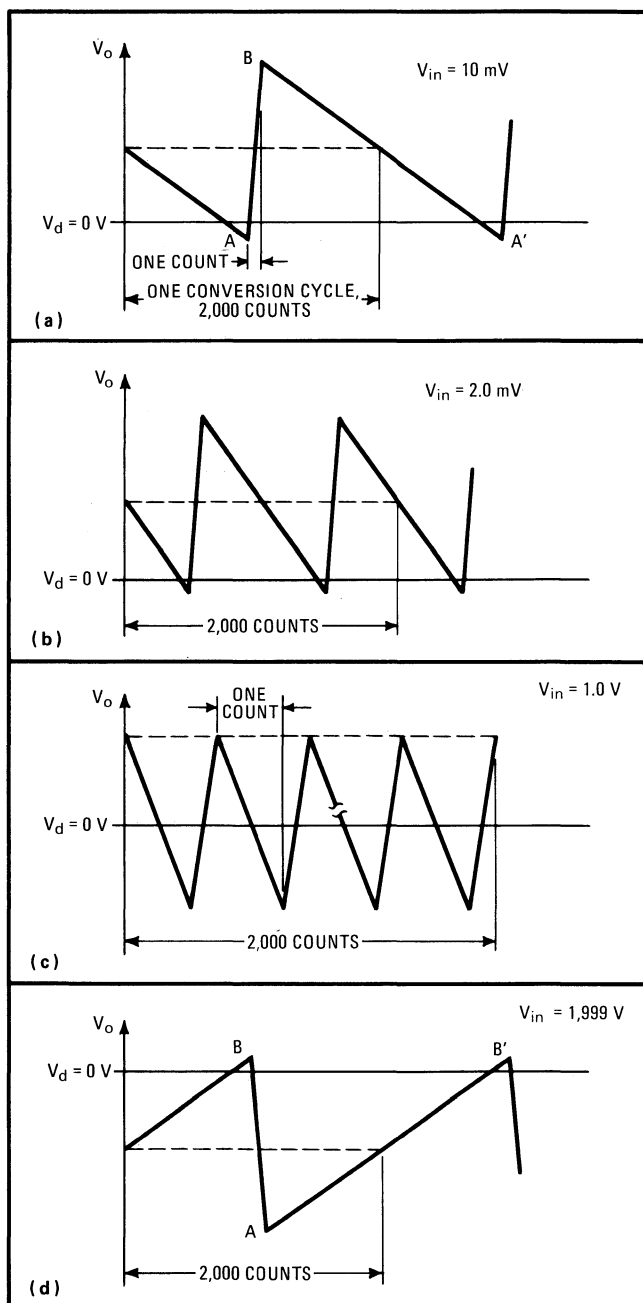
During this part of the integration cycle, gated clock pulses are being fed to the counter and accumulated. When V_o again passes V_d , V_t switches to a logic 0 state, and the next clock pulse opens the current switch and closes the clock gate.

Since the converter is a free-running system, this process keeps repeating itself until the conversion period is over. The conversion period is defined as a certain number of clock pulses, N_t , received by the digital conversion circuitry. N_t is a system constant and is fixed when the converter is designed. The number of clock pulses accumulated by the counter during one conversion cycle, N_f , is a variable quantity that is directly proportional to the input voltage. N_f , in fact, is the digital output of the converter.

Probably the most unusual feature of the charge-balancing converter is the diversity among the waveforms



1. **Balanced.** By switching reference current on and off, a-d converter puts zero net charge into integrator over full integration cycle.



2. Timing. Number of integration cycles in one conversion cycle depends upon input voltage. When voltage is very small, negative ramp is very slow, and converter makes only one integration per conversion (a). Doubling input voltage doubles number of integration cycles (b). After half-way point (c), trend reverses and at top of measurement range unit is back at one integration per conversion (d).

observed at the output of the integrator. In one conversion cycle, there can be anywhere from zero integration cycles to approximately $N_t/2$ integration cycles, depending on the value of the input voltage.

Changing waveform

For instance, assume that $N_t = 2,000$, $I_{ref} = 1.0$ milliamperes, and R_{in} —the converter input resistance—is 2 kilohms. Now, if a small input voltage, say 1.0 millivolt, is applied to the input, I_{in} will be only 0.5 microamperes and V_o will move very slowly in the negative direction until it crosses zero (Fig. 2a). Then, at the next clock

pulse, I_{ref} is connected to the integrator (point A), causing it to climb steeply in the positive direction. A zero crossing occurs almost immediately, and the next clock pulse disconnects I_{ref} , leaving V_o at point B. From here on the process repeats itself, with V_o dropping slowly toward point A'.

Since this is a charge-balancing converter, the charge removed from the integrator between points A and B must equal the charge applied between points B and A'. Because I_{ref} is 1.0 mA and I_{in} is 0.5 μ A, the reference current must be off for about 2,000 times as long as it is on. Thus, if I_{ref} is on for the minimum duration of one clock pulse, it will be off the 2,000 clock pulses and there will be only one integration cycle in the conversion cycle.

But if V_{in} is twice as large—2.0 mV— I_{in} becomes 1.0 μ A, and there are two integrations per conversion (Fig. 2b). The negative-going ramp is twice as steep as in the preceding case, while the positive-going portion has practically the same slope. (To be exact, the charging current, $I_c = I_{in} - I_{ref}$, is 0.9995 mA in the first case and 0.9990 mA in the second.) As the input voltage increases further, the slope of V_o from B to A' becomes steeper because I_{in} increases, while the slope from A to B becomes less steep because I_c decreases.

Again, when the input voltage is 1,000 volts, $I_{in} = 0.5$ mA, and $I_c = 0.5$ mA too. Thus the two slopes of the V_o waveform are equal and opposite, and the wave shape is a triangular wave centered about zero (Fig. 2c). Also, the peak amplitude of V_o is half of what it was when V_{in} was 0.001 v, and there are 1,000 integration cycles in one conversion cycle.

Finally, when the input voltage is 1.999 v, I_{in} is 0.9995 mA and the waveform picture is an inverted version of the situation pertaining to the 1-mV input (Fig. 2d). The segment of the V_o waveform from B to A in Fig. 2d corresponds to the segment from A to B in Fig. 2a. The reference current is connected for all but one count during a conversion cycle, so there is one integration per conversion again. If the input voltage is 2,000 v or greater, V_o never gets back to zero, and the counting is continuous.

How it works

An implementation of the converter block diagram (Fig. 3) shows one of the advantages of the charge-balancing converter—its simplicity. The integrator, for example, consists of only an op amp, a capacitor, and a resistor. Since the high open-loop gain of the op amp keeps node A at ground potential, the resistor in the input lead determines the input resistance of the converter. Note that the system is designed to work properly only with positive inputs.

The threshold detector is even simpler. Although two different threshold levels could have been used—one for when V_o is moving in the positive direction, and one for the negative direction—this is not necessary. For the implementation shown here, it was sufficient to choose $V_{d+} = V_{d-} = 0$. The only further requirement is that the threshold voltages remain stable for at least one conversion cycle (about 200 milliseconds in this case).

Usually, a threshold detector contains a positive feedback that, by setting up a hysteresis voltage at the

switching levels, assures positive switching when the input is moving slowly nearly the threshold level and also prevents the detector from oscillating under the influence of input noise, input bias voltage shifts, and so on. But in the charge-balancing a-d converter, the detector requires only an open-loop operational amplifier, and the hysteresis is provided instead by the digital portion of the circuitry.

The digital section consists of J-K flip-flop, an inverter, an AND gate, and a few diodes. The circuitry works as follows: first, assume that Q is low, \bar{Q} is high, and V_t is low. Since Q is low, there are no pulses coming through the AND gate. Since \bar{Q} is high, it supplies the current I_{ref} through D_2 , and D_1 is back-biased so that I_{ref} is not connected to node A of the integrator. Under these conditions V_o ramps negatively and eventually passes zero—the threshold voltage—causing V_t to go high. This puts a high level on J and a low level on K.

At the next clock pulse, Q goes high and \bar{Q} goes low. The AND gate now starts to pass clock pulses which go to a counter. At the same time I_{ref} is switched to node A because D_2 is reverse-biased, and reference current is drawn from the integrator.

When the integrator output V_o again passes V_d , V_t again goes negative, putting a low level on J and a high level on K. At the next clock pulse, Q goes low and \bar{Q} goes high, which stops clock pulses from passing through the AND gate and disconnects I_{ref} from the integrator. A known current has now been removed from the integrator over a measured integral number of clock cycles and thus a known amount of charge has been removed. This process continues as long as V_{in} is positive.

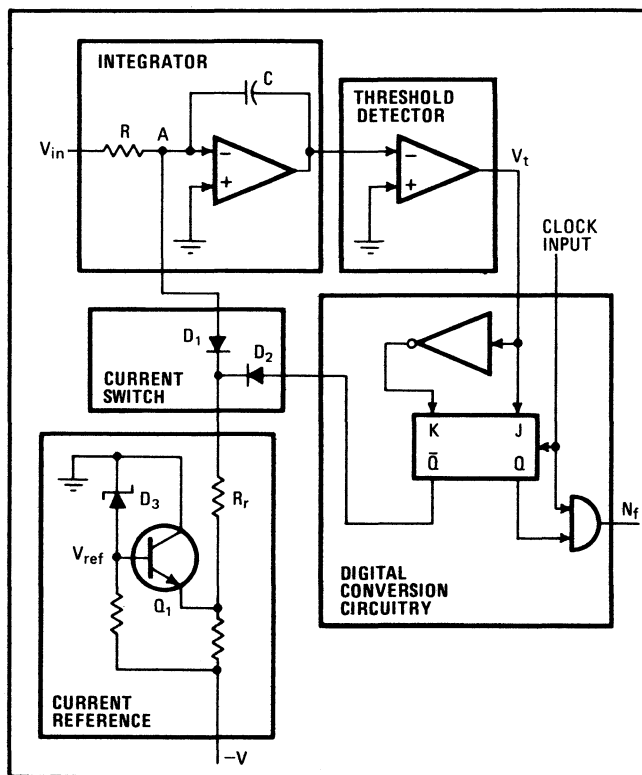
The variable time period between when V_t changes state and when the clock pulse changes the state of the J-K flip-flop is the digitally generated hysteresis of the system. This time can vary from zero to one clock cycle. After a period of time, under the application of a constant input voltage V_{in} , the output of the integrator establishes an average voltage. For this to occur, the average voltage on the integrating capacitor must be constant. Consequently the charge removed must equal—or balance—the charge applied.

The current reference is really a voltage reference and a resistor. It makes use of the fact that the integrator summing junction (node A) is at 0 V which makes $I_{ref} = V_{ref}/R_r$ (see Fig. 3). Since diode D_1 is also in the circuit when I_{ref} is connected to node A, transistor Q_1 is used to buck out and temperature-compensate D_1 . D_3 is a temperature-compensated zener diode.

Fixing the variables

Since the same capacitor is used for both the applied and removed charge, the charge-balancing equations can be written in terms of currents. Over any conversion cycle, the average input current, $I_{in} = V_{in}/R$ must equal the average current removed from the integrator, $I_o = I_{ref}N_f/N_t$. Here, N_f is the number of clock pulses over which current was removed from the integrator, and N_t is the total number of clock pulses in one conversion cycle. Thus, $V_{in}/R = I_{ref}N_f/N_t$, or $V_{in} = RI_{ref}N_f/N_t$.

The only variable on the right-hand side of this equation is N_f . Thus, by proper selection of R, I_{ref} , and N_t ,



3. Simplicity. Major advantages of charge-balancing converter are its few parts and the loose tolerances of most parts. Threshold detector, for example, is simply an op amp operated at full open-loop gain. Current switch consists of only two diodes.

the converter can easily be scaled to cover any desired voltage range. For example, choosing $R = 2$ kilohms, $I_{ref} = 1.0$ mA, and $N_t = 2,048$ counts provides a $3\frac{1}{2}$ -digit converter that can measure up to 2.000 v with 1.0-mV resolution.

Actually, only 2,000 counts are needed for a $3\frac{1}{2}$ -digit machine; the extra 48 clock pulses are used for such housekeeping chores as transferring the contents of the counter into some type of memory (so that the count can be displayed during the next conversion cycle) and resetting the counter to zero.

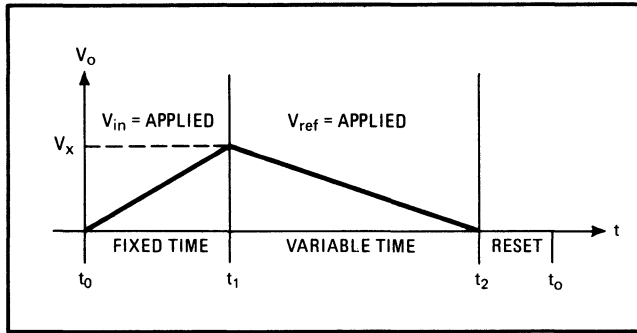
Limitations

The major disadvantage of the charge-balancing converter is its speed. It requires at least as many clock pulses as the maximum count to complete a conversion cycle. As an example, a $3\frac{1}{2}$ -digit (13-bit) converter requires more than 2,000 clock pulses to effect a conversion. A successive-approximation converter could probably do the job in 14 to 16 clock cycles.

Inexpensive linear ICs have sufficient gain-bandwidth product and slew rate for satisfactory operation at clock frequencies of 10 to 20 kilohertz, which allow a conversion cycle time of 0.1 second. If 10-ms conversion times were required, faster devices would be needed.

As for sensitivity, the $3\frac{1}{2}$ -digit system described here can resolve 1 mV. To achieve 100-microvolt resolution would require either an integrator amplifier with less than $30 \mu V/^\circ C$ of drift, or an autozero circuit.

Precision, too, must be considered. The present system is free-running—each conversion cycle does not necessarily start with the same initial integrator condi-



4. Competitor. In dual-slope converter, input voltage is applied for fixed period, and time needed to return integrator voltage to zero at constant discharge rate provides measure of applied input voltage.

tions. This leads to a ± 1 -digit error. The converter could be synchronized to remove this source of imprecision.

Finally, as already mentioned, this a-d converter is unipolar, so that an input must be preconditioned before a-d conversion can take place.

Still, despite these disadvantages, all of which can be overcome with the exception of speed, the performance of this system is quite impressive in light of its low cost and simplicity.

Comparison with dual-slope conversion

The speed limitation of the charge-balancing converter is shared by the dual-slope converter, so it should prove worthwhile to compare these two approaches in some detail. Different versions of the dual-slope converter can be made to handle bipolar inputs, to be auto-zeroed, to reject power-line interference, and to be insensitive to variations in the values of some of its components. But for purposes of comparison with the charge-balancing circuit, a unipolar system with the same input configuration will be used. (Actually, many of the input-circuit variations used with the dual-slope technique can also be applied to the charge-balancing converter.)

A dual-slope converter has basically the same parts complement and block diagram as the charge-balancing unit. Of course, the digital conversion circuitry would have to be different.

For the dual-slope circuit in Fig. 4, input voltage V_{in} is converted to a current and applied to the integrator for a fixed period of time, which allows the integrator to ramp to some arbitrary voltage, V_x . Then a reference current of opposite polarity is connected to the integrator until the integrator crosses zero. Once V_{ref} is connected to the integrator, the counter starts, and clock pulses are counted until the zero crossing occurs. Since the voltage on the integrating capacitor is again zero, the charge applied equals the charge removed, and a digital conversion has been performed. A small reset time is needed to strobe the latches and reset the counter.

From the standpoint of a circuit complexity, the digital sections of the dual-slope and charge-balancing converters would be about the same complexity with slightly different timing. The dual-slope circuit would need more counts for the conversion cycle for the period that V_{in} alone is applied, which would increase the size of the required ripple counter.

The analog sections would also be about the same with two exceptions: the threshold detector and the switching devices. In the dual-slope circuit, the threshold detector must have good long-term zero stability; in the charge-balancing circuit, good zero stability for one conversion cycle is all that's required. For both converter types the integrating capacitance and the system clock frequency must be stable for one conversion cycle.

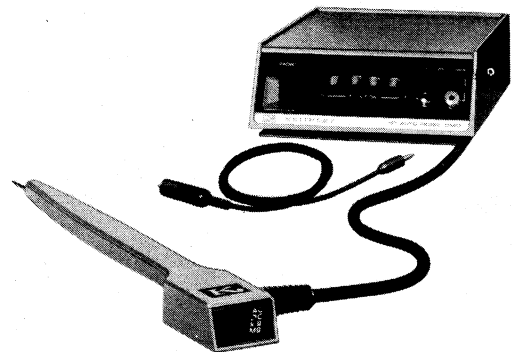
To connect the reference, the same diode switching could be used in the dual-slope as in the charge-balancing technique, but for reset, additional switching devices would be required for the former. The integrator in the dual-slope circuit must be initialized before the start of a conversion cycle because its starting level determines the accuracy of a conversion.

Consequently, the charge-balancing approach winds up using fewer components, which are less critical, than does an equivalent dual-slope circuit.

Dual-slope converters can be made bipolar—by adding an opposite-polarity reference, another high-quality threshold detector, and polarity-sensing circuitry to determine which reference and which threshold detector to use. To give the charge-balancing converter bipolar capability, an absolute-value detector can be used in front of it. In this case, over-all complexity and cost of each system are about equal. Even so, the charge-balancing circuit still enjoys an advantage over the dual-slope circuit because the absolute-value detector doubles as an ac-dc converter, which adds ac measurement capability at no extra cost.

The dual-slope converter has one distinct advantage over the charge-balancing converter. By proper selection of the period for which the input is applied, the dual-slope converter can be made to reject a specific frequency (such as line frequency) and its harmonics. This is impossible to do with the charge-balancing converter. Ac rejection must be accomplished with input filtering techniques.

The operation of the charge-balancing converter has been proven by over a year of use in the Keithley 167 Autoprobe Digital Multimeter (Fig. 5). This instrument is fully auto-ranging, measures ac and dc voltage and resistance, and is battery-operated. In fact, the charge-balancing converter seems to have met the meter's over-all design objectives as well as or better than any other a-d conversion system. □



5. Proven performance. Charge-balancing converter is heart of this portable multimeter. Extensive field experience proves that new conversion technique is worth considering for new system designs.

Digital storage improves and simplifies analysis of low-frequency signals

A spectrum analyzer in which a digital memory takes over the storage function needs only an inexpensive cathode-ray tube yet achieves high resolution; an adaptive sweep also speeds up presentation of a signal

by Jerry Weibel and Larry Whatley, *Hewlett-Packard Co., Loveland, Colo.*

□ Spectrum analysis of low-frequency signals is a well-established technique in such diverse areas as communications, geophysical and oceanographic studies, and vibration analysis. Conventional methods of studying spectra in this range use either expensive storage tubes or slow X-Y recorders to display the signals.

But now a combination of digital storage and adaptive sweep techniques, in the 3580 analyzer, makes it possible to display and store such signals with high resolution and at relatively high speed. What's more, the digital storage provides more flexibility for signal analysis than was previously available. And digital storage makes it possible to use an ordinary, inexpensive cathode-ray tube for the display, instead of a special storage tube.

The digital display

Using digital storage for the display has many advantages over storage-tube approaches. Display adjustments need not be made when the sweep speed of the analyzer is changed. The display automatically updates the trace at the correct rate. And the instrument's intensity and focus controls, once set, do not have to be re-adjusted.

Digital storage is also free from the loss-of-contrast problems that come up when a variable-persistence tube is used at slow sweep rates. As a new sweep is gen-

erated by the analyzer, the old trace is automatically cleared, and the new trace is put in its place (Fig. 1a). If a single sweep is made, the trace that was generated will continue to be displayed until it is either cleared or replaced by another sweep.

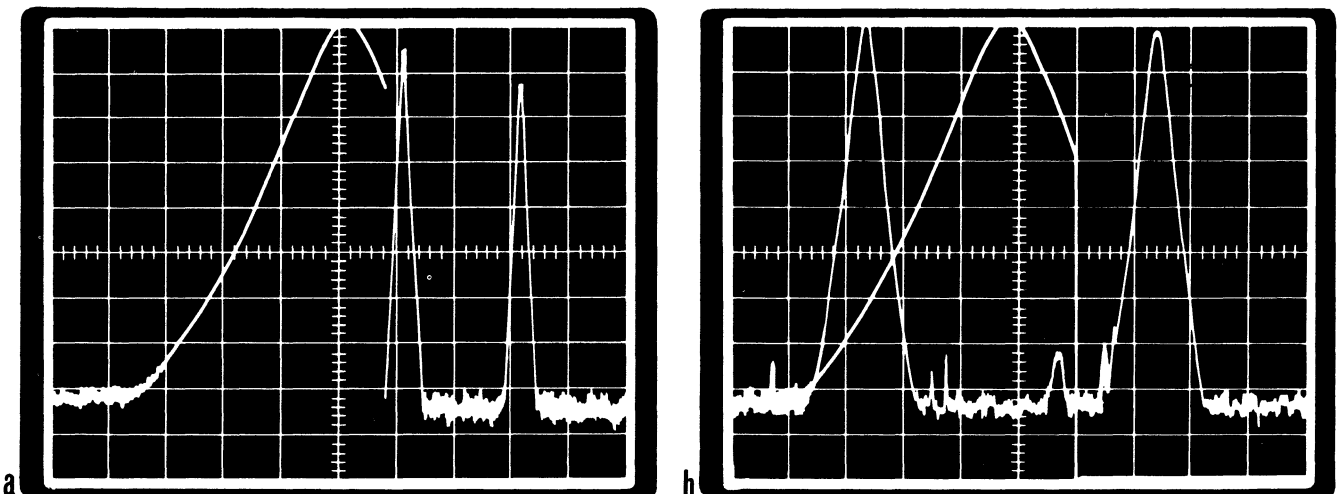
If a trace is needed for future reference, it can be stored in the digital memory, allowing both this stored trace and the input trace to be displayed simultaneously (Fig. 1b). To add to the usefulness of the store made, the stored trace may be blanked from the display, and recalled when desired.

Design considerations

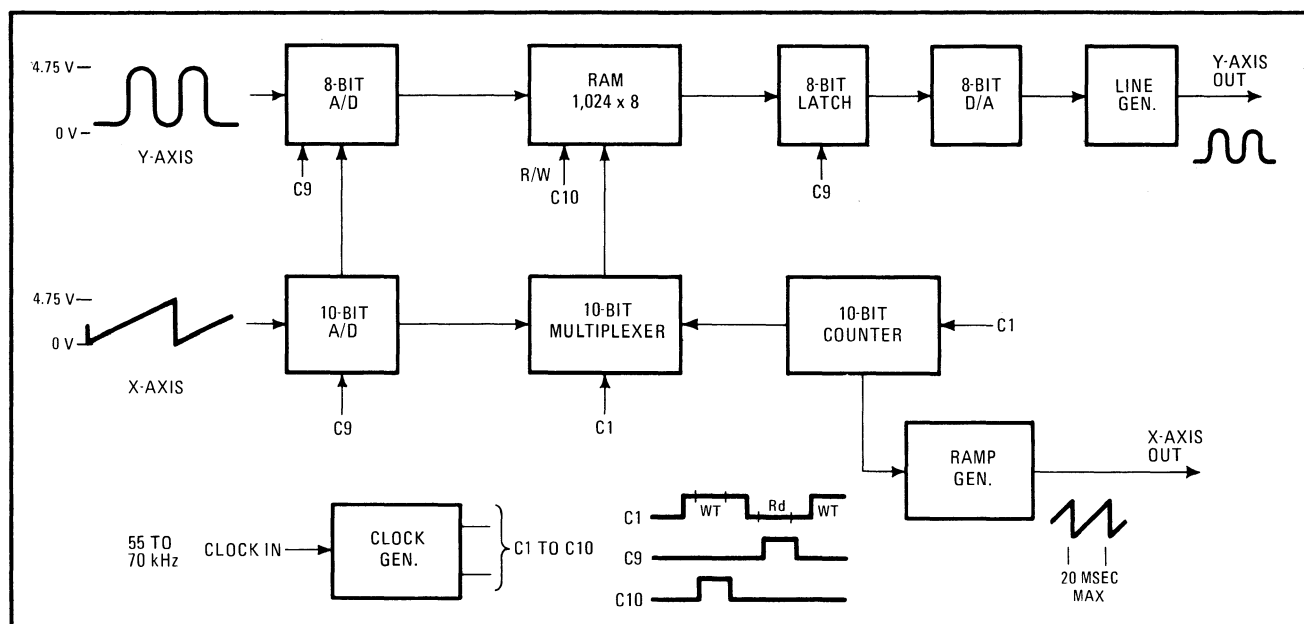
Since the spectrum analyzer was meant to be a portable, battery-operated instrument, as well as a laboratory tool, power consumption was minimized. Complementary metal-oxide-semiconductor logic was used wherever possible, and a standard CRT with a low-power filament allows the instrument to operate for five to six hours from its internal rechargeable battery.

Perhaps the most unusual design requirement for the digital display was an ability to deal with the extremely slow sweep speeds of the analyzer. These slow sweeps must be transformed in time to sweeps on the CRT that are faster than 20 milliseconds to avoid flicker when a standard P31 phosphor is used.

Resolution is also an important consideration. Since



1. **Digital advantages.** As each new sweep is made, it takes the place of the old one, which is retained until the very last moment (a). Simultaneous display of a stored trace along with the one being updated is accomplished at the touch of a button (b).



2. Digital system. Partial block diagram shows 10-bit analog-to-digital converter for the X axis and the 8-bit converters for the Y axis. The multiplexer's function is to switch the RAM address inputs between the X-axis converter and the 10-bit address counter.

the display is digital, both the X and Y axes must be broken up into discrete segments. It was found that 1,000 X-axis segments provide as much resolution as can be discerned on a CRT.

Even when 1,000 X-axis segments are used, the Y-axis magnitude can vary greatly over a given segment. In the digitally stored display, only one number may be picked to represent the value of the Y axis in each segment. Since the magnitude of the response is the important measurement, the peak value of the signal in each segment must be chosen. The accuracy of this number is determined by the Y-axis resolution, and it must be chosen so that it does not contribute appreciable errors to the measurement. Also, the display must be able to show small changes in the Y-axis analog signal. The resolution of 256 segments provides 0.4% of full-scale resolution and satisfies both of these requirements.

Display implementation

A partial block diagram of the system that meets these requirements is shown in Fig. 2. The clock generator provides the timing for the whole system. The input to the generator is the high-voltage supply oscillator, which generates the operating voltage for the CRT. This can be any fixed frequency from 55 kilohertz to 70 kHz. For ease of discussion, this clock frequency will be considered to be 50 kHz, which corresponds to a period of 20 microseconds.

The X-axis analog input to the display system is converted to a 10-bit digital word by the input analog-to-digital converter. The conversion gives 1,024 segments of X-axis resolution. This 10-bit word becomes the input address to the random-access memory. The system RAM consists of eight 1,024-by-1-bit static n-channel MOS RAMs.

The Y-axis analog input is made into an 8-bit word by the Y-axis a-d converter. This gives 256 segments of resolution. This 8-bit digital word is stored in memory at the address generated by the X-axis converter.

The 10-bit multiplexer switches the RAM address between the X-axis converter and the 10-bit address counter. The switching input to the multiplexer is the C1 output from the clock generator. This is a 50-kHz square wave; the first half is the write phase and the second the read phase.

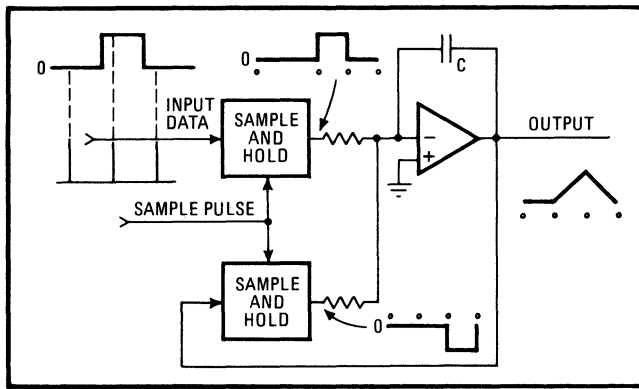
During the write phase of C1, the multiplexer switches the 10-bit address lines for the RAM to the X-axis converter. The write command (C10) is then given to the RAM, and the 8-bit Y-axis word is written into the address corresponding to the X-axis analog input.

During the read phase of C1, the address to the RAM is supplied by the 10-bit address counter. The 8-bit word at this address is latched out to the output d-a converter. Every C1 period, or every 20 μ s, the counter is advanced one count. Therefore, a new word is supplied to the output converter every 20 μ s, and all 1,024 8-bit output words are generated approximately every 20 ms. Each set of words constitutes one CRT sweep. This process is continuously repeated to provide a stable CRT presentation.

The d-a converter output consists of a series of discrete levels that cannot be applied directly to the CRT. The samples would generate a display of dots that would be satisfactory in some low-resolution displays but not in this application. Therefore, the signal first goes to the line generator, which draws lines between the dots. One means of doing this would be to calculate the vectors between points and slew X and Y axes accordingly. However, it is simpler to sweep the X axis linearly and slew the Y axis at a rate that connects each point.

A Y-axis line generator that can do this job is shown in Fig. 3. It accepts the input data consisting of discrete voltage levels, and a sample pulse indicating that the data are valid, and gives an output signal composed of connected line segments for driving the Y-axis deflection amplifier.

The operation of this circuit, sometimes called a



3. Connect the dots. Linear point connector takes discrete input-voltage levels and uses them to generate connected line segments that will drive the Y-axis deflection amplifier.

linear point connector, can most easily be understood by using a single nonzero input point and observing the time functions at various points. The output always slews at a rate proportional to the difference between the current data sample and the previous sample, considering the inversion of the integrator. For zero input, zero output is observed. When the input datum occurs, the output slews at a proportional rate. During the next period, however, the integrator input consists of the zero input data and the value of the output at the end of the previous sample period. The output accordingly slews back to zero.

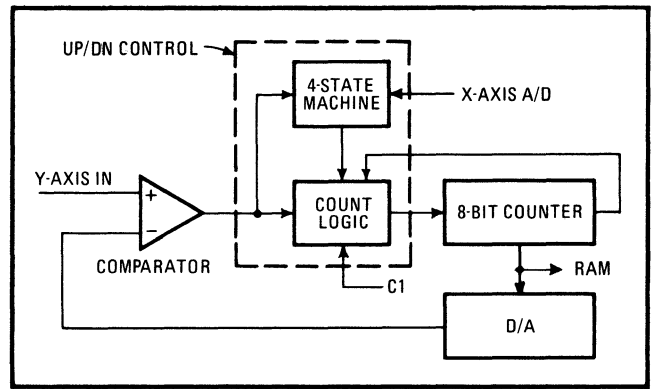
The working system

As was noted, it is essential to sample and digitize the peak value of the Y-axis signal in each X-axis segment. Therefore, a peak-detecting a-d converter is needed for the Y-axis signal. Such a converter, shown in Fig. 4, has three input signals: the Y-axis input, a clock input, and an input from the X-axis a-d converter that indicates when a new X-axis segment begins.

The 8-bit up/down counter supplies eight lines to the d-a converter and the input to the RAM. The output of the converter is compared with the Y-axis analog input by the comparator. The comparator output indicates whether the count to the converter is too high or too low and supplies the appropriate count-up or count-down signal.

The up/down control logic controls the clocking of the counter and the direction in which it counts. The lines into the up/down control logic, other than those of the comparator, are from the X-axis a-d converter, the clock generator, and the counter's carry-out. The carry-out holds off the clock to the counter whenever it contains all logic 1s and a count-up is given, or when the counter contains all logic 0s and a count-down is given. Stopping the clock holds the counter at all 1s or all 0s when the input voltage is higher or lower than the maximum or minimum output voltage of the d-a converter.

The input from the X-axis a-d converter is a pulse—actually the clock to the X-axis a-d converter counter—that occurs at the beginning of a new X-axis segment. This signal resets the four-state machine to state A (Fig. 5). The counter is allowed to count in the direction indicated by the comparator in each state with the exception of state D, in which the four-state machine allows



4. Peak-detecting converter. Y-axis analog-to-digital converter operates under the control of the four-state machine. The unit acts as a peak-detector, except in the case of rapidly decreasing inputs.

the counter to count only in the up direction.

The operation of the four-state machine is controlled by the condition of the Y-axis analog input. There are three input conditions of concern: input moving up, input holding steady at some dc level, and input moving down.

In the first case, when the Y-axis input signal is climbing as the X axis is swept, the output of the comparator can do one of two things, depending on whether the input is climbing rapidly or slowly. If the input is climbing rapidly, the comparator output will remain high after each clock pulse, because the d-a converter output is too low and the counter is trying to catch up to the Y-axis input. Under these conditions, after two clock pulses the four-state machine will go to state D and remain there until it is reset. Since the counter can only count up when the machine is in this state, the converter acts as a peak detector of the Y-axis input over the given X-axis segment.

If the input is climbing slowly, the comparator switches between count-up and count-down with each clock pulse, with an occasional extra count up. When this happens, the machine again arrives at state D and causes the counter to peak-detect, but this time it may take as many as three or four clock pulses to arrive at state D.

In the second case, when the Y-axis input is a dc level, the alternating high and low comparator output will again cause the four-state machine to reach state D and peak-detect the inputs.

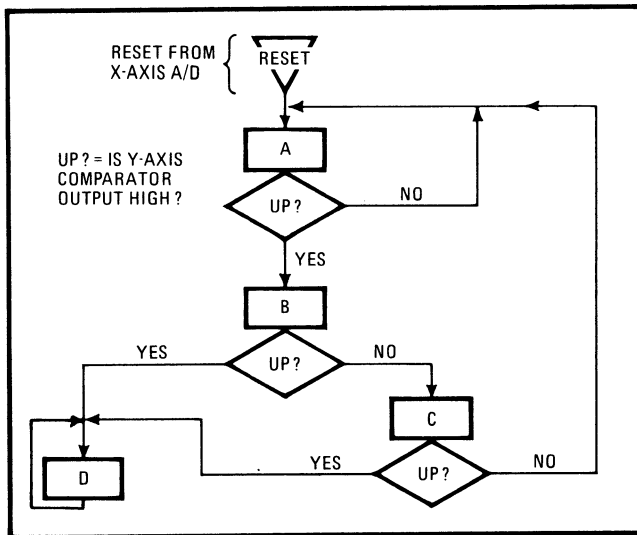
The third input condition occurs when the value of the input signal moves down with the X-axis sweep. If the Y-axis signal moves down more than one least significant bit of the d-a converter every three clock pulses, the four-state machine will not reach state D. If this occurs, the signal is not peak-detected and the value at the end of the segment is the chosen Y-axis value.

If the down movement of the input is slower than one least significant bit of the d-a converter, the Y axis will be peak-detected at a value equal to the Y-axis input near the start of the X-axis segment. If the movement continues down throughout the segment, the Y-axis counter must catch up at the beginning of the next segment. The counter will always be able to catch up within the first third of the X-axis segment. This type of peak-detecting control is one that provides a more accu-

rate representation of the negative input slope.

The system also has a mode of operation in which the presentation being displayed may be stored as a permanent record. The trace is stored by depressing the STORE button, which causes two traces to appear on the screen. One is the trace that has been stored, and the other is the trace that represents the analyzer's present output. These traces are displayed alternately, each taking 10 milliseconds. A four-state machine is incorporated in the system to control the store operation. In the store mode, half of the memory, or 512 words, is used for the stored trace and the other 512 words are available for the input.

However, this storage technique has a drawback. The splitting of the memory cuts the resolution of the display in half. Still, this reduced resolution is adequate for almost all the measurements made by the analyzer. Moreover, the reduced resolution is justified because doing without an extra memory just for the store oper-



5. **Controller.** Flow chart for four-state machine in Y-axis a-d converter is controlled by value of Y-axis analog input.

ation reduced cost and power drain. The cost of the auxiliary control circuits is about the same for splitting the memory or having two memories.

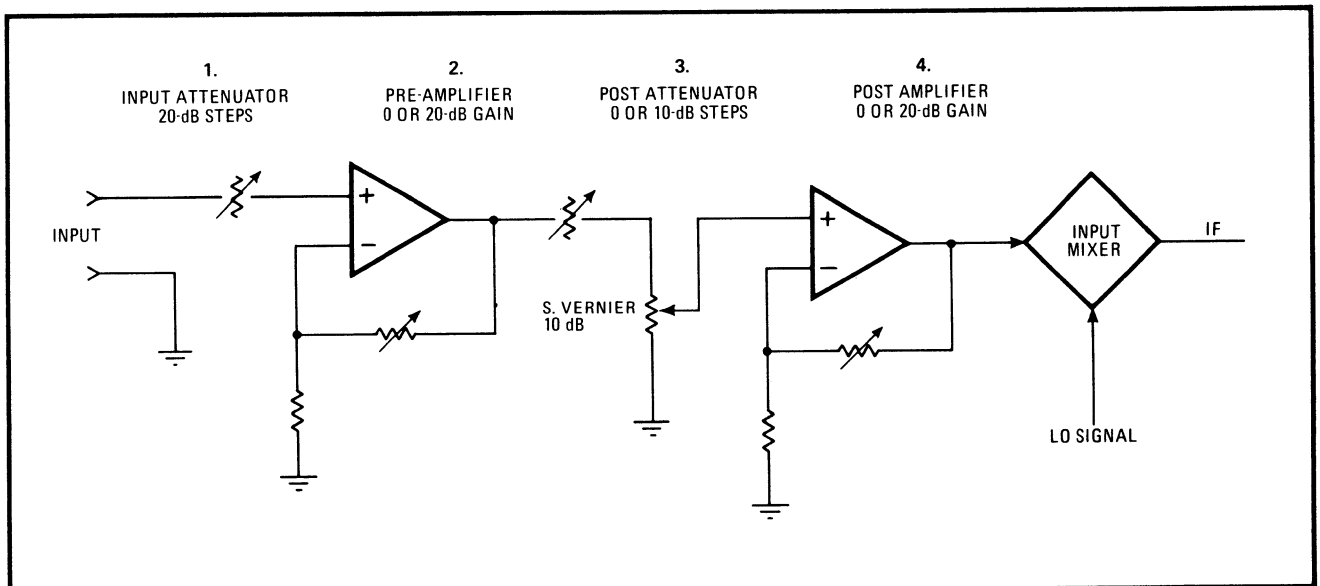
Several design goals determined the configuration of the input section of the analyzer. The 1-hertz bandwidth was considered necessary to meet high-resolution applications, and low cost was a second important objective. A single-conversion configuration was chosen to satisfy these two requirements.

The analog analyzer at work

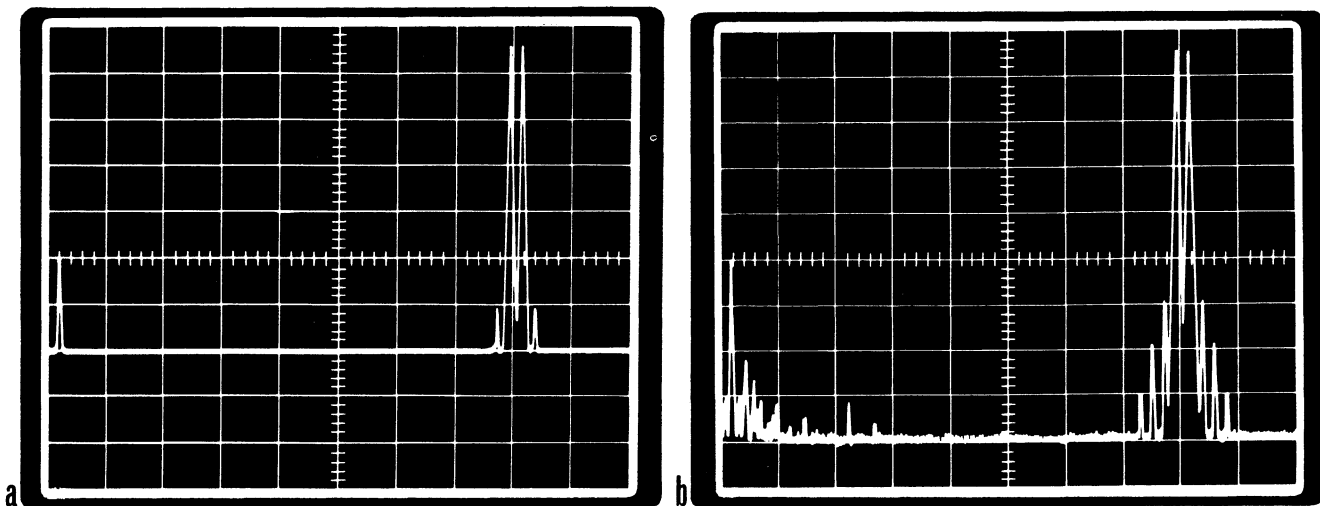
Input signals from 5 Hz to 50 kHz are mixed with the local oscillator signal operating from about 100 kHz to 150 kHz. Signals falling at the difference frequency of 100 kHz are passed by the intermediate-frequency filter, having a center frequency of 100 kHz and a bandwidth selectable from 1 Hz to 300 Hz. The signal is then passed through either a linear or logarithmic amplifier, detected, and then fed to the digital display circuitry or an X-Y recorder. This is a very basic configuration. The i-f is determined by a practical matter: how high a frequency can crystals or other resonators achieve while maintaining a high enough Q for the 1-Hz bandwidth? To eliminate the analyzer's sensitivity to signals outside its frequency range, the local oscillator's tuning range is limited to about half the i-f.

In this respect, the design of a spectrum analyzer can be considered as a serial chain of objective-conclusion decisions. Low cost leads to a single-conversion scheme, and a 1-Hz bandwidth implies a 100-kHz i-f, which in turn, determines the maximum tuning range.

Applications of spectrum analysis to the audio-frequency range demand a high dynamic range (low distortion and spurious responses) and a wide range of selectable input sensitivity. The analyzer's input-sensitivity control changes the signal level at five locations (Fig. 6). The requirements leading to this configuration are 1-megohm input impedance, 90-decibel dynamic range for this segment of the signal path, 10-dB attenuation steps, a continuously variable 10-dB vernier,



6. **Sensitivity control.** Configuration of input circuitry is dictated by requirements listed in text. Signal attenuation (or gain) must be adjusted at five points along signal path when input sensitivity is changed with this front-end design.



7. Sweep speeder. Trace made with a conventional sweep at optimum speed takes 100 seconds (a). Adaptive sweep, however, reduces dynamic range, eliminates noisy signal floor, and cuts sweep time to 10 seconds (b). The adaptive-sweep cutoff threshold is adjustable.

and sensitivity limited predominantly by noise riding on the input to the pre-amplifier.

Altering any one of these requirements leads to a different configuration. For a single example, lowering the input impedance requirement would allow use of a 10-dB-step input attenuator and a simpler configuration. Thermal noise of a 10-dB pad with 1-megohm input impedance is too great for the dynamic range objective, however. A 20-dB pad has lower output impedance and consequently less thermal noise. The two amplifiers must be made with discrete components rather than off-the-shelf ICs because of the requirement for low noise, low distortion, and high input impedance. An IC was chosen for the input mixer, however, because of favorable specifications of noise, distortion, gain, and cost.

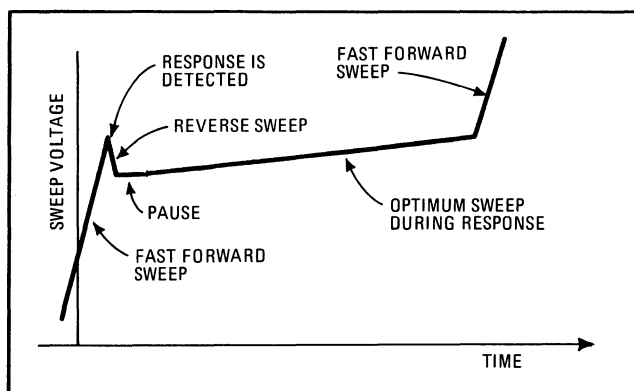
The i-f filter is truly the heart of a spectrum analyzer. It determines the selectivity of a spectrum analysis and how fast the spectrum can be swept. Since sweep time is such an important consideration for a high-resolution analyzer, synchronously tuned stages of filtering were used. This type of filter is a close approximation of a Gaussian filter, considered optimum for sweeping, and it is easy to align it and to switch bandwidth.

Adaptive sweep

For the first time, a spectrum analyzer incorporates a sweep feature that can substantially reduce measurement time in certain applications. Figures 7a and 7b show two spectrum displays, the first using a conventional optimum sweep, the second an adaptive sweep. The first display took 100 seconds to generate; the second only 10 seconds.

The idea behind the adaptive sweep is to speed up the sweep when the signal is below some adjustable threshold level, and to slow it down to the optimum speed when the input exceeds the threshold. A speed factor of 20 is used in the analyzer described. This approach, of course, reduces the dynamic range of the measurement, but in many applications the lower part of the spectrum consists of noise, anyway, so no information is sacrificed.

This more complicated sweep can be implemented with combinational logic. But though this was done in a



8. Adaptive-sweep control. The operation of the adaptive-sweep circuitry is controlled by a dedicated eight-state machine. The four states through which the sweep voltage must pass whenever an above-threshold signal has been detected are illustrated here.

prototype, synchronous logic controlling an eight-state machine proved to be superior. In this hardware, the eight states correspond to various sweep conditions such as "fast forward sweep," "reverse sweep" (a necessary condition for sweeping an entire response after it has been detected), and "pause" for allowing transients to decay. For each response in Fig. 7b, the sweep voltage as a function of time goes through the sequence shown in Fig. 8.

In addition to these design ideas, the special capabilities of the analyzer include selection of the frequency control to indicate start-of-sweep or center-of-sweep frequency, an indicator lamp to warn of input overloading that may be causing spurious responses, and a tracking oscillator signal, available from the back panel, that can be used to measure the swept-frequency response of a device. This last feature allows the analyzer to be used effectively as a network analyzer—but without the network analyzer's ability to measure phase.

The 3580 has been optimized for frequencies between 5 Hz and 50 kHz. The combination of digital storage, adaptive sweep, 1-Hz bandwidth, 30-nanovolt sensitivity, and battery operation makes this instrument suitable for communications, geophysical, and other applications, in the lab and the field. □

C-MOS may help majority logic win designers' vote

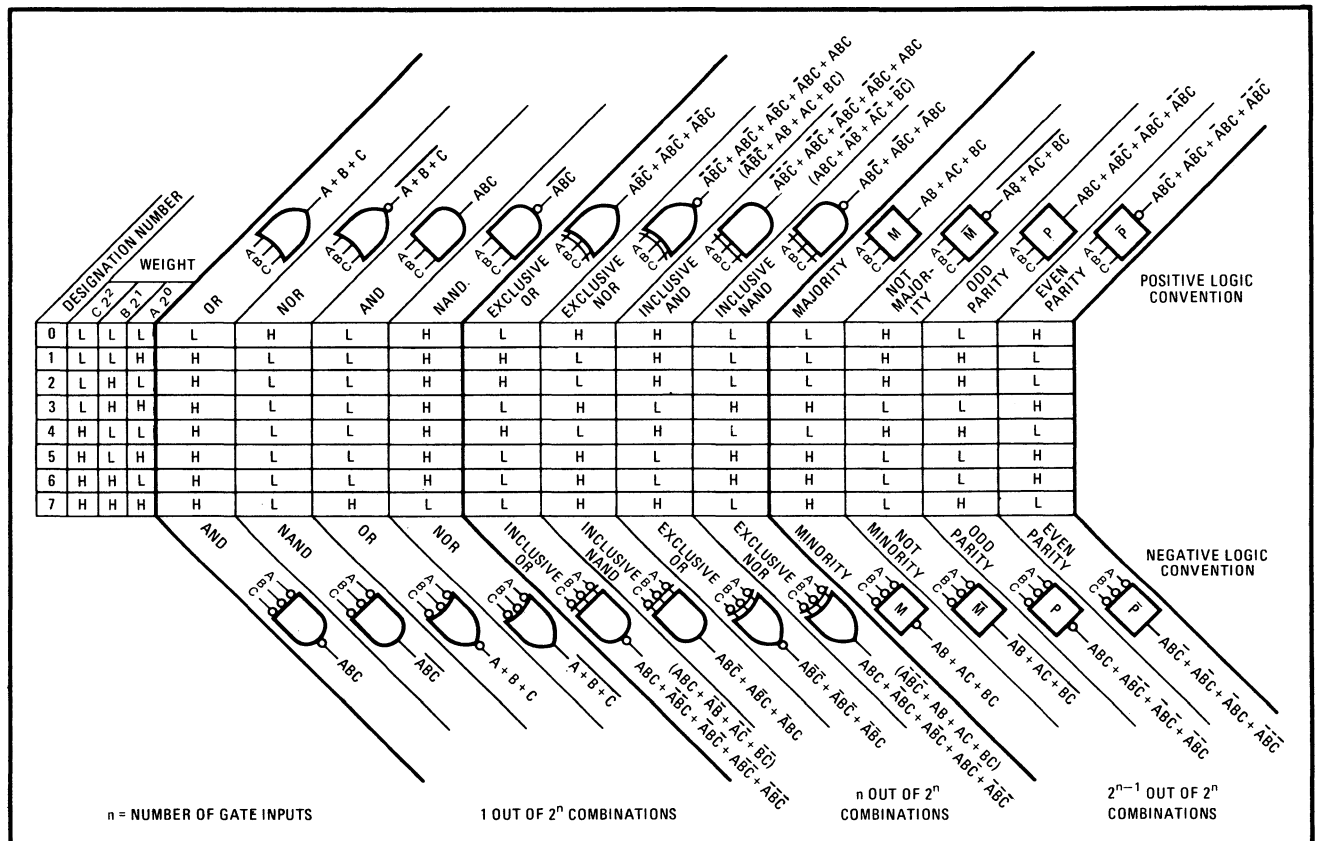
Majority logic, in which output depends on the state of a majority of inputs, has just been introduced on an economical IC; it can markedly reduce the number of gates needed to implement a function

by Lane Garrett, *Motorola Semiconductor Products Division, Phoenix, Ariz.*

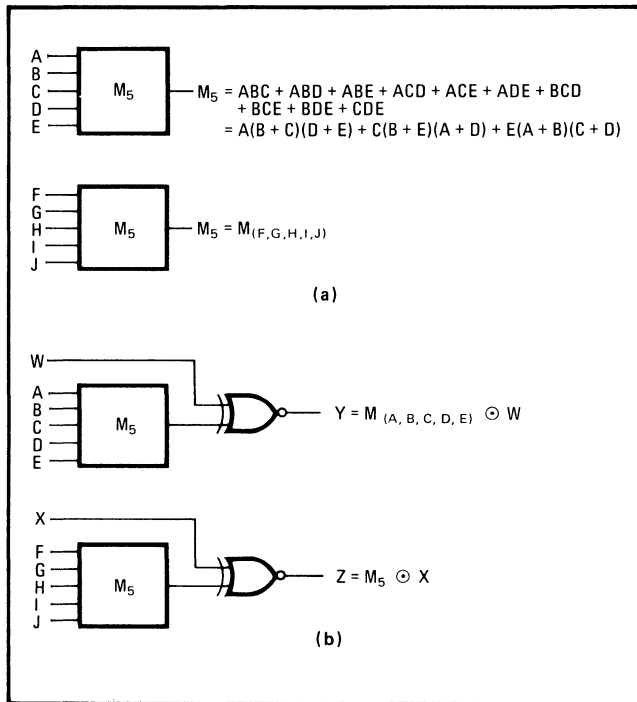
□ The class of logic functions called "majority logic," which has long been dormant, is now being used as basic logic building blocks alongside conventional AND, NAND, OR, and NOR functions. Broadening the logic and system designer's list of useful tools, majority logic is defined simply as a function whose output depends on the state of the majority of its inputs. Devices having this capability often significantly reduce the total number of logic gates required to implement a function.

Already a new majority-logic chip built with complementary-MOS technology is available for functions that are otherwise difficult to realize—for example, in correlation techniques dealing with weighted variable values and in communications systems where information must be retrieved from noisy backgrounds.

For many years, the generic class of threshold logic, of which majority logic is a member, has been known to logic designers, but its use has been confined to special or custom applications because no method existed to turn these designs into economical standard products. A threshold-logic function is defined as a decision block in which the output is true if the arithmetical sum of the inputs (each of which may have its own numerical weight) is greater than a predetermined number. Major-



1. The family. In this chart relating majority logic to the other basic gating functions, the left margin gives designation numbers and the eight possible high-low combinations of three input variables, while the logic symbols and Boolean expressions are given at the top and bottom.



2. Doubly flexible. The first majority-logic product, a dual five-input chip whose function is shown in (a), has good tradeoffs to get logic flexibility and low production costs. Moreover, adding an exclusive-NOR gate to each M_5 gate (b) enables the output to be logically inverted by applying a logic 0 to the W input. W may also be used as a variable to compare to the majority of the other inputs.

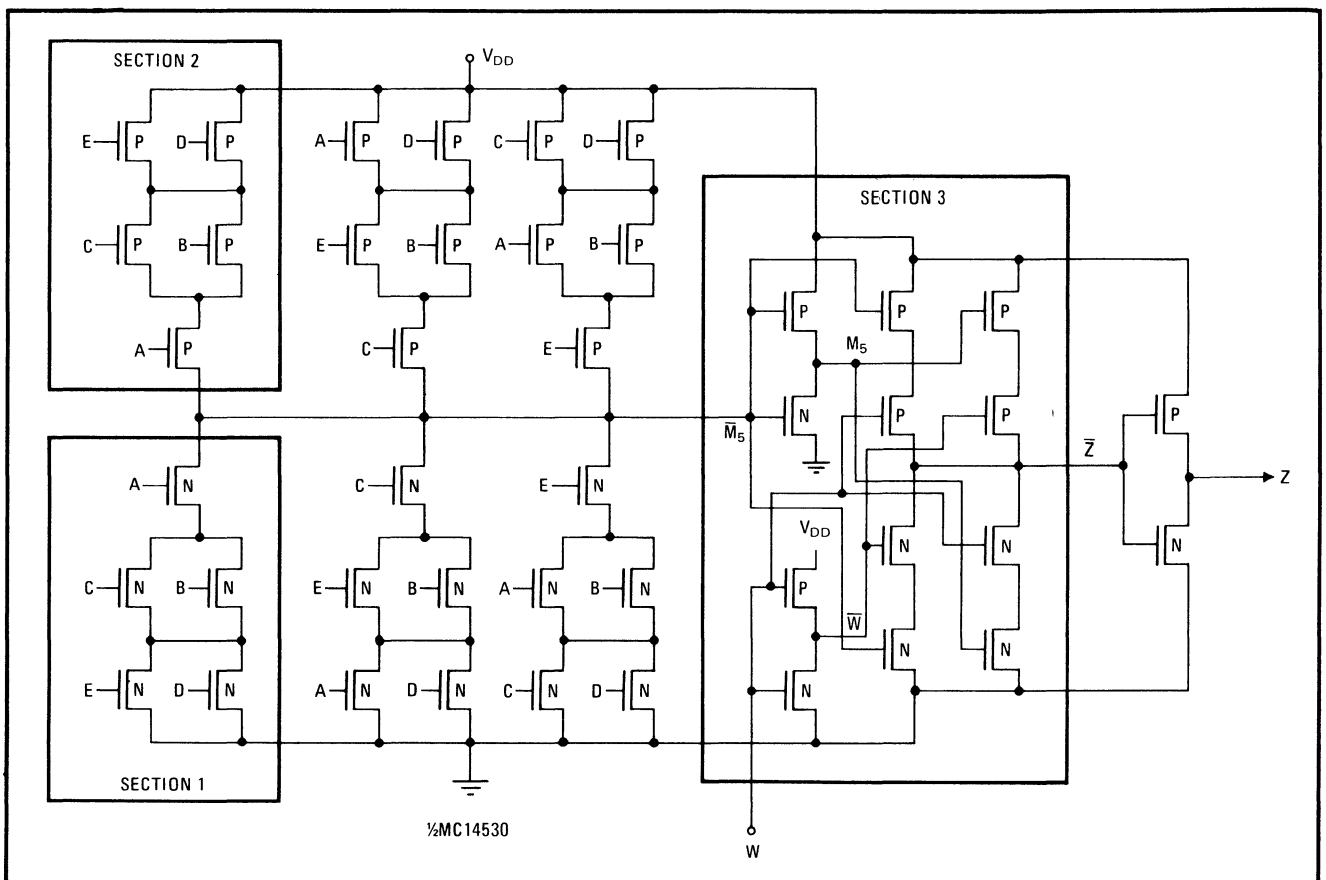
ity logic, which is most easily built in IC form, has, in every case, an odd number of inputs, each with a numerical weight of 1; thus, when more than half the inputs are true, the output is true.

Figure 1 relates majority logic to other basic gating functions. The left margin of the chart gives designation numbers and the eight possible high-low combinations of three input variables, A , B , and C . The logic symbols and Boolean expressions at the top of the chart are for the positive logic convention, while those at the bottom are for negative logic.

The majority-logic function

The four most common gating functions are shown in the left third of the chart: OR, NOR, AND, and NAND. It should be noted that, unlike majority logic, each of these gates detects one unique input combination out of all possible combinations. For example, the NOR detects the unique condition when all inputs are low and gives a high output. The next group of four gates makes up the exclusive and inclusive functions that have been defined for more than two inputs.

Taking n as the number of inputs to a gate, these functions sense n unique combinations out of 2^n total combinations. Out of a possible 2^n combinations, the last grouping of gates senses 2^{n-1} combinations, and these are the majority and parity functions. It should be noted that if all inputs are random in nature, the output of these functions can be expected to be true half of the time. The majority-logic function is most useful because



3. Operation. In half the logic chip shown here, each n -channel device of section 1 will be turned on when its gate goes high, while in section 2, conduction will occur when gate-input variables are low. Section 3 implements the exclusive-NOR function.

inputs may be used for both logic and control.

This new member of the C-MOS family is a dual five-input majority-logic gate (M_5). Because of the tradeoffs of production cost and logic flexibility, a five-input device was chosen, since five inputs are sufficient to demonstrate the flexibility of majority logic but are not too many to unduly complicate fabrication. Because present production costs of a 16-pin dual in-line package are almost the same as those for a 14-pin package, and the additional pins result in a significant increase in flexibility, the function shown in Fig. 2a was packaged in a 16-pin DIP instead of the conventional 14-pin DIP.

Inverting output

The two additional pins allow an exclusive-NOR gate to be added to each M_5 gate, providing two significant advantages as shown in Fig. 2b. The output may be logically inverted by applying a logic 0 to the W input. Also, the W input may be used as a variable that is logically compared to the majority of the other inputs, a function that cannot be easily implemented with conventional gates. The resulting logic component lends itself to numerous applications that were not heretofore economically practical.

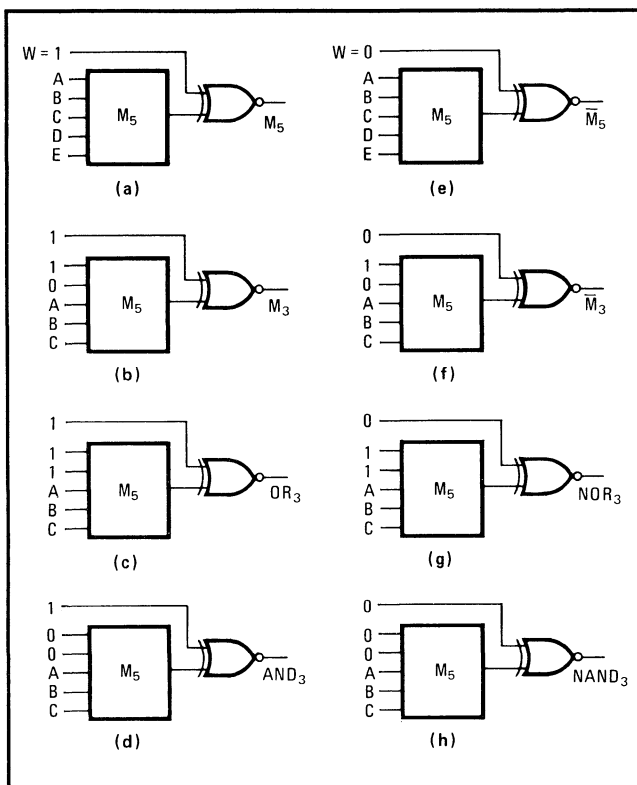
C-MOS was chosen as the most effective technology for this function because it affords excellent packing density for complex functions otherwise uneconomical with such conventional bipolar technologies as transistor-transistor logic. And with C-MOS, speed is not significantly decreased with increasing complexity because

devices can be built in tight arrays where chip delays are short. In addition, since the majority-logic function is symmetrical, it lends itself to easy implementation with standard C-MOS symmetry. On the other hand, the most economical bipolar technique for the implementation of complex majority logic is the summation of switched current sources—most effectively accomplished with emitter-coupled-logic design techniques that require more chip area and consume more power.

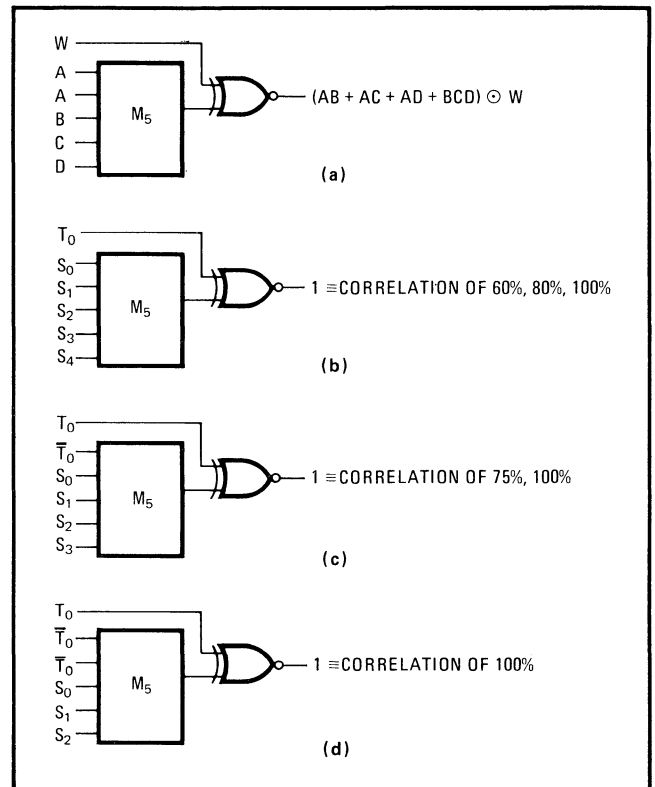
Majority-logic chip layout

The key to the design of economical, standard majority-logic C-MOS chips is the ability to make several on-chip devices do multiple functions so that complex majority-logic equations can be handled by fewer on-chip components. Consider the example $A(B+C)(D+E) + C(B+E)(A+D) + E(A+B)(C+D)$. Figure 3, which shows half of the M_5 layout, illustrates how the M_5 chip would implement this function. The n- and p-channel devices have been drawn with simplified symbols for the sake of clarity.

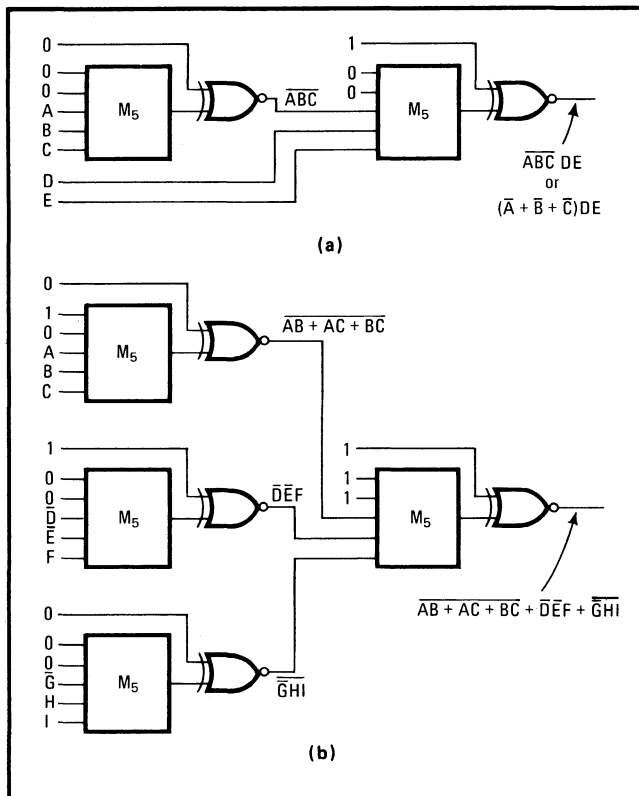
Each n-channel device shown in section 1 of Fig. 3 will be turned on if its gate goes high. Conduction can take place if A and (B or C) and (D or E) are true (high). Note that if conduction through the n-channel devices can take place, there is no corresponding conduction path possible through the upper p-channel devices. Conversely, section 2 will conduct if the input variables are low for the same expression, $A(B+C)(D+E)$. The next two series sections of Fig. 3



4. The M_5 chip's many combinational functions. Functions (a) through (d) represent the majority of five inputs and three inputs, the OR of three inputs, and the AND of three inputs. Functions (e) through (h) will give the complements of these expressions when the W input of the exclusive-NOR is changed from 1 to 0.



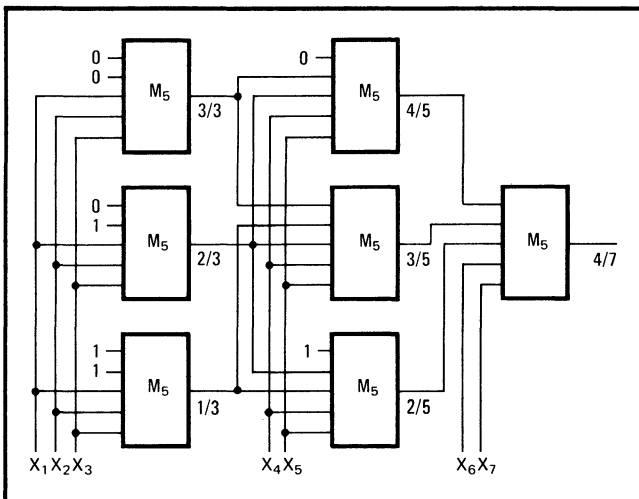
5. Weighing in. In correlation applications, special weight must often be given to a particular input. In (a), the input A is given a weight of two by repeating it once. Correlation of a test bit, T_0 , with various input variables is also possible. The schematic in (b) illustrates correlation of 100% for a true or logic 1 output.



6. Levels of flexibility. The versatility of majority gates is increased by using two levels of the M_5 chip. In (a), the NAND of three variables is ANDed with two more variables. In (b), only two packages are required to get these complex combinational functions.

implement the last two major terms of the above expression.

The illustrated array implements the not-majority function, which is simply the complement of the majority function. Section 3 implements the exclusive-NOR logic function with only 12 MOS transistors. The last two transistors implement an inverter/buffer to drive off-the-chip capacitance. This last stage converts the logic expression into the exclusive-OR of not- M_5 and the W



7. More than five. Majority gates with more than five inputs can be built from M_5 arrays. In this seven-input configuration the output 4/7 is true only when four or more inputs are true. The array can also be rearranged so that it will provide a 5/7 true output.

input, $(\overline{M_5} \oplus W)$ which is the logical equivalent of the original expression that was to have been implemented. Only 88 transistors are required to complete the entire function. This is less than half the number of devices required to build an equivalent TTL realization of the same function.

Fabrication of the chip in a small area is accomplished with a symmetrical layout. High-speed MOS devices are included to minimize gate-propagation-delay times and give good output-drive capability. At a nominal 10-v supply voltage, the over-all propagation delay varies between 100 and 200 nanoseconds with nominal load capacitance, depending upon the combination and number of inputs being switched.

As a standard product, the dual-majority-logic gate, (MC14530), is specified to operate over a supply range of 3 to 18 v with the same low quiescent power dissipation (typically 50 nW) common in standard logic families of C-MOS logic. For maximum compatibility, input and output characteristics are the same as other devices of the C-MOS family. Conversely, a TTL approach would yield a faster but more costly function that would dissipate significantly more power.

Applying the dual M_5 gate

The basic M_5 gate with exclusive-NOR is a powerful combinatorial logic function. In Fig. 4, which shows the basic M_5 configurations, the functions in Fig. 4a through 4d represent the majority of five inputs and three inputs, and the OR of three inputs, and the AND of three inputs, respectively. By changing the W input of the exclusive-NOR from a 1 to a 0, the complements of the previous four functions are obtained (functions 4e through 4h).

Figure 5a illustrates a method used for increasing the "weight" of a variable. Here the A input is given a weight of two by repeating it once, with the resultant Boolean output expression shown. The majority gate may also be used to indicate if the correlation between a test bit (T_0) and various input variables is greater than or equal to a predetermined value.

For example, Fig. 5b illustrates correlation greater than or equal to 60%, in Fig. 5c, it is 75%, and in Fig. 5d, correlation of 100% is required for a true or logical 1 output. By using arrays of these gates, it is possible to check the correlation factor between words stored in a memory and multiple samples of word data that have a large noise content. Thus, this correlation technique can be used for enhancing radar signatures and improving the performance of recognition equipment.

The versatility of majority logic can be appreciated from Fig. 6, which shows two combinational uses of M_5 gates. Figure 6a provides the NAND of three variables ANDed with two more variables, impossible with a single package in other logic families. By using only two packages in the configuration of Fig. 6b, many combinational functions of a large number of variables can be obtained with a significant savings in package count over other approaches. For the example shown, TTL requires twice as many packages.

The majority-logic gates may also be formed into arrays that are useful for detecting whether or not n bits out of m bits of a given word are true. This is useful in

conjunction with certain types of coding schemes involving a fixed number of 1s. Majority gates with more than five inputs can also be built with arrays, as illustrated in Fig. 7a. The general symbology n/m is used to illustrate that the majority gate is wired to detect whether n or more inputs are true out of a possible m input bits. For example, $\frac{2}{3}$ states that the output is true if two or more of three inputs are true, i.e., M_3 . The array in Fig. 7a is best understood by following through the array from left to right for the seven input bits, X_1 through X_7 . It will be noted that the output $\frac{4}{7}$ is true only when four or more inputs are true, i.e., M_7 .

A general-purpose array is easily formed so that all possible cases of n/m can be detected. This is illustrated in Fig. 8a, where 15 M_5 gates ($7\frac{1}{2}$ packages) are required. If the exact number of true bits in the input word is required, the output of the array may be encoded into a 3-bit binary word through the use of a priority encoder (Fig. 8b). A priority encoder is an MSI function in which each input is assigned a fixed priority (0 through 7 in the example shown) and the output is the encoded binary equivalent of the highest-priority input that is true. This array is useful for checking the correctness of n/m codes and determining the number of bits in a word that correlates with a test word.

More correlation

Because of the ability to weight inputs in majority-logic sequencing, M_5 chips are ideal for applications where sensed data is to be compared to standards or various test words, and the degree of comparison or correlation is desired. Examples are in character-recognition equipment, speech recognition, radar-return analysis, recognition of various codes, and the recovery of information from noisy data samples.

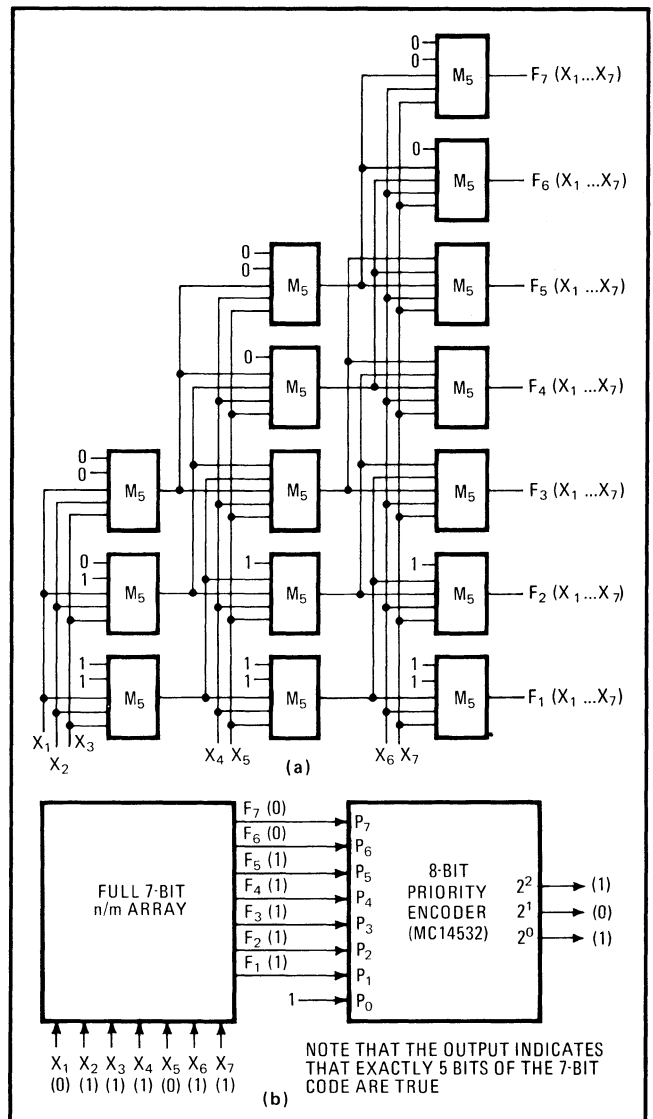
The array shown in Fig. 9, generic in nature, has been generalized for use in many correlation applications. Although this array may not be optimized for some applications, it presents a typical method of solution for many correlation problems.

In operation, the portion to the left of the figure consists of seven shift-register segments. Five flip-flops from each shift register are shown containing five time-sequential samples (S_1 through S_5) of one bit of a 7-bit data word.

The first seven M_5 gates vote on the five data-word samples. The majority of the five samples of each bit are then compared bit by bit with a test word (test bits 1 to 7). The result of each comparison is then available at the bit-correlation outputs.

Moreover, it is possible, by the method shown in Fig. 5, based upon the bit-correlation outputs, to deliberately feed back complements of the test bits to check for a higher correlation factor. These complements may be fed back in a serial manner and mixed with the data word in a predetermined manner.

The over-all correlation factor (on a word basis) is sensed by the 11 M_5 gates shown to the right. This configuration senses from 4 out of 7 up to 7 out of 7 bits in agreement with the test word. If none of the four outputs is true, the anticorrelation factor may be obtained by inverting all 7 test bits; e.g., the $\frac{7}{7}$ output would then be true if no original bits were in agreement.

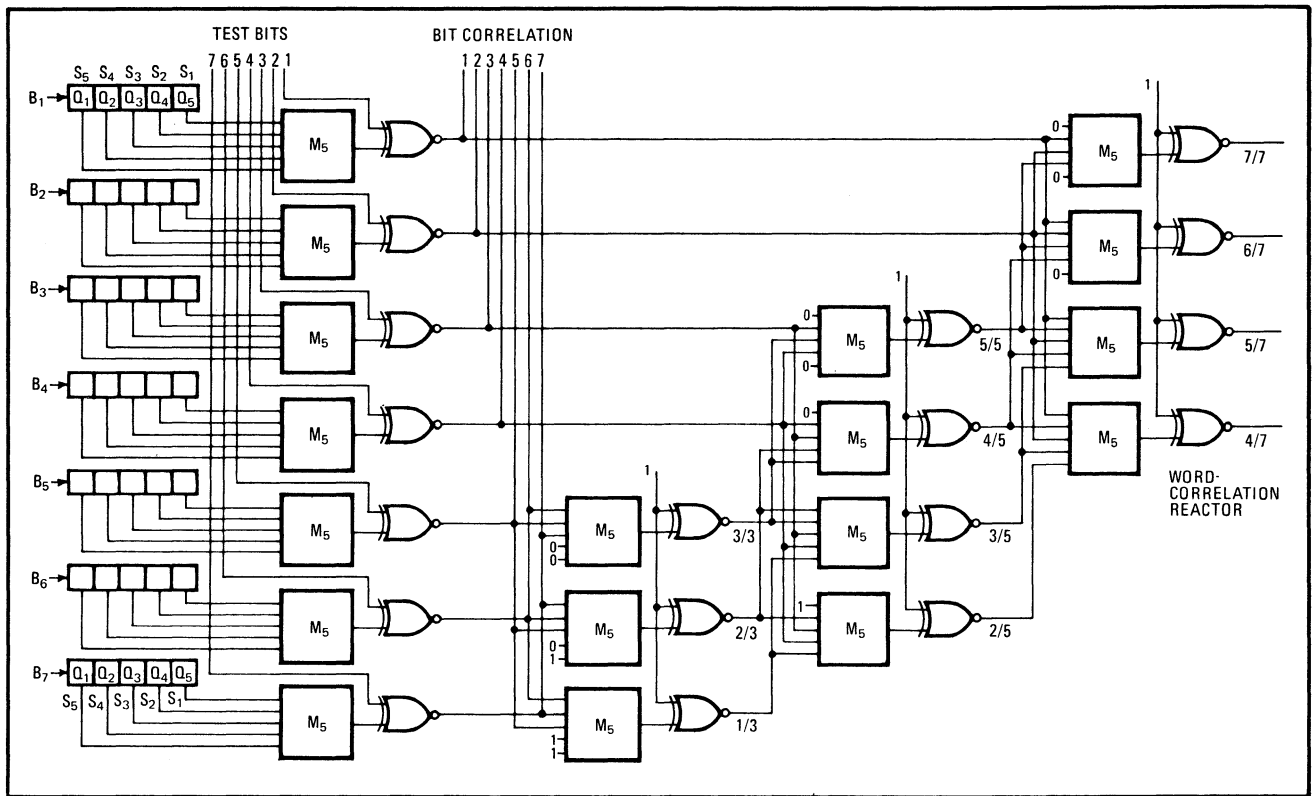


8. In general. General-purpose arrays can be formed to detect n/m possible cases; (a) shows the configuration for 7 bits, which uses 15 M_5 gates ($7\frac{1}{2}$ packages). For an encoded output, a priority encoder (b) is used to get the exact number of true bits in an input word; here the output of the array is encoded into a 3-bit binary word.

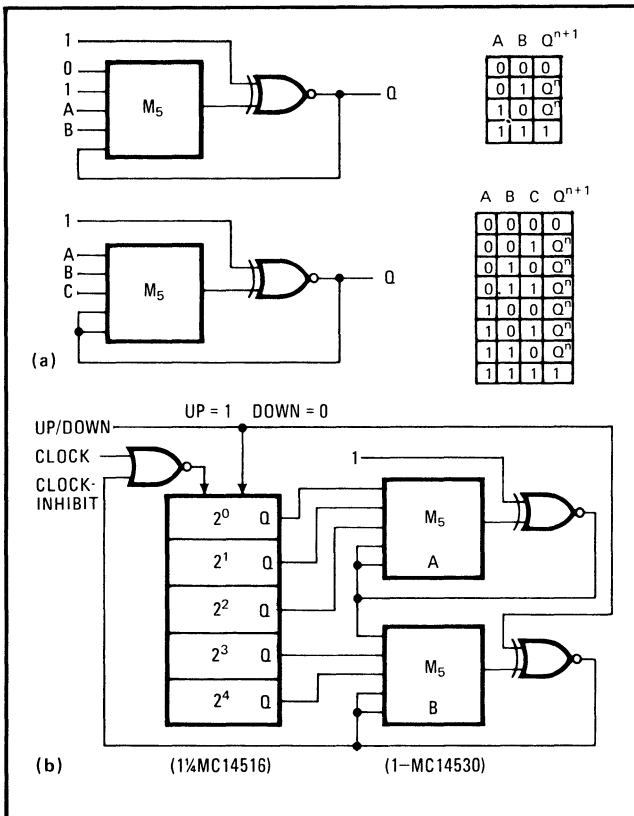
In addition to performing combinational logic with M_5 gates, sequential logic can also be implemented by feeding the output of a majority gate back to one or more inputs. Figure 10a illustrates this application for both three-input and five-input configurations. As the truth tables show, this type of flip-flop will change states only when there is coincidence of all inputs. For changing inputs, the device will hold the state of last coincidence until the opposite coincidence occurs.

One area where this scheme is useful is in the control of UP/DOWN counters. Frequently, when a maximum or minimum count is reached, further counting must be inhibited to prevent spillover—the counter will change all states (all 1s to all 0s, or vice versa). An example is shown in Fig. 10b, where the dual M_5 gate detects all 0s or all 1s, for a 32-state UP/DOWN counter.

The first gate, A, senses whether all 1s or 0s are present from the first 3 bits of the counter. The output of gate A feeds back to two of its inputs and one of the



9. Correlation is the thing. In this 7-bit five-sample correlation array, the first seven M_5 gates on the left vote on the five data-word samples S_1 through S_5 . The majority state of the five samples of each bit is then compared bit by bit with a test word (test bits 1–7). The over-all correlation factor is sensed by the 11 gates on the right, which sense 4 out of 7 to 7 out of 7 bits in agreement with the test word.



10. In sequence. Sequential logic is possible with majority gates by feeding the output of a gate back to one or more inputs. Three-input and five-input configurations are shown in (a). In (b), the dual M_5 gate detects all 0s or all 1s for a 32-state UP/DOWN counter.

inputs of gate B. Only when the remaining two stages of the UP/DOWN counter agree with the output of A can the output of B change.

If the counter is in the UP mode (1 on the control line), and a maximum count is obtained (all 1s), the output of gate B will be a 1, inhibiting the clock and thus preventing further counting. On the other hand, if the mode control goes low while the clock is still high, counting will occur downward on the next clock edge, until all 0s result. The counter will then be inhibited again, thus preventing roll-over.

The future of majority logic

Now that majority logic has become economically practical through MSI, the function may become an industry standard. As familiarity grows, the M_5 gate will be used in applications to reduce package count and provide logic that is programmable as a result of its own decisions or external computer control. Correlation arrays that are useful for character and speech recognition are natural applications.

The symmetry of the majority-logic layout, using C-MOS devices, lends itself to high-density packing. By using minimum-geometry devices, large majority-logic-gate arrays of more than 200 gates can be fabricated by means of present production technology. Arrays of this size could easily usher in whole new philosophies in system architecture that would lend themselves to what is sometimes referred to as probabilistic processing, where many variables are not necessarily 100% true but instead may be mixed with noise or have assigned weights or degrees of confidence. □

Hybrid approach to regulation solves power-supply problems

Series-shunt voltage regulator combines series-regulator efficiency with the high output-to-input isolation characteristic of shunt units; technique proves successful for -15-volt source in secure radio system

by Jerry B. Denker and David A. Johnson, Cincinnati Electronics Corp., Cincinnati, Ohio

□ A hybrid series-shunt regulator has been built to combine the high output-to-input current isolation characteristic of the shunt regulator with the high efficiency of the series regulator. Tests indicate that the hybrid maintains more than 30 dB greater isolation than a series-only regulator, and it achieves some 85% efficiency for a range from less than 10% of load to full load.

Shunt regulators, with their inherently high isolation, are commonly used in critical applications where the prime source must be protected against changes in load. Such a regulator, however, is very inefficient, especially in systems with wide load variations, because the power into the regulator is constant and the regulator dissipates more power when the load is reduced. Therefore, series regulators are generally used to achieve high efficiency in systems that can tolerate poor isolation.

However, high electrical isolation between the outputs of multiple voltage regulators and the unregulated direct-current power source is sometimes required. Without the isolation, large current transients can occur at the regulated outputs (Fig. 1).

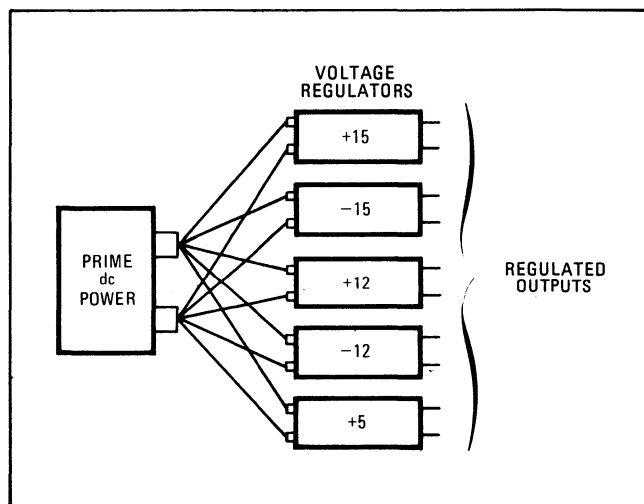
In designing secure radio-communications systems, for example, current variations on the prime power source caused by poorly isolated supplies for crypto-

graphic equipment might be transferred to the voltage regulator supplying the radio-frequency transmitter. As a result, the encrypting equipment could inadvertently modulate the rf output, which could compromise the encryption system. Moreover, in all applications for power supply systems, it is generally desirable to maintain high isolation between voltage-regulator outputs and the prime source simply to reduce the over-all electromagnetic-interference level in the source.

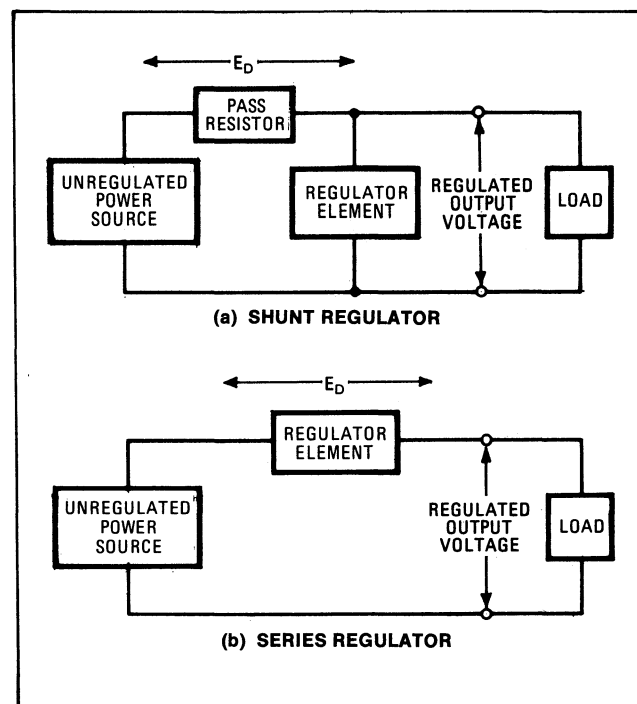
Regulator characteristics

Both shunt and series regulators control the output to the load in the same way—by causing a voltage drop (E_D in Fig. 2), which is varied automatically to subtract exactly the required voltage from the raw unregulated source to maintain a constant voltage on the load.

The shunt regulator causes a current flow through the pass resistor (Fig. 2a) to drop the voltage. When not ex-



1. Isolation needed. To prevent large current transients from contaminating the prime dc power source in a large electronic system, each voltage regulator in the system must be designed so that transients on its output do not bounce back to its input.



2. Regulator basics. The shunt regulator (a) responds to load changes by varying the current flowing in its regulating element. The series regulator (b), however, simply draws less current from the prime source when load power is reduced.

ternally loaded, a shunt regulator conducts the maximum current needed to establish the voltage drop, E_D . When a shunt regulator is loaded at the output, current through the regulator element is reduced by an amount equal to the load current so that the total current through the shunt regulator remains constant so long as there is a constant voltage source.

Such a design dissipates the maximum amount of internal power when its output terminals are open and unloaded. When fully loaded externally, the current through the regulator element is reduced to a minimum. Dissipation in the pass resistor is constant, irrespective of loading.

A series regulator (Fig. 2b) functions in much the same way, except that the regulator element takes the voltage drop directly across its own terminals, instead of through a pass resistor. Thus, when a series regulator is not loaded, only enough current to keep it active flows through the regulator element, so that its power dissipation is quite small. Then as load-current requirements increase, the power dissipated in the regulator increases proportionately.

The sensing parameter commonly used for both types of regulators is the voltage across the load. This information is then fed back to control the current through the regulator element. By combining the series and shunt regulator elements and using a proper selection of feedback information, a hybrid regulator is capable of efficient operation for a wide variation of loads and with high output-to-input isolation. In such a series-shunt configuration, the series arm is programmed to limit the unregulated source input current to a value slightly greater than is required by the load.

For a hybrid series-shunt regulator that has been designed for a secure military mobile radio, control signals

indicating load changes were derived from the radio's mode-control switch. Thus, the load current requirements for the regulator are predetermined by known demands on that regulator for each operating mode.

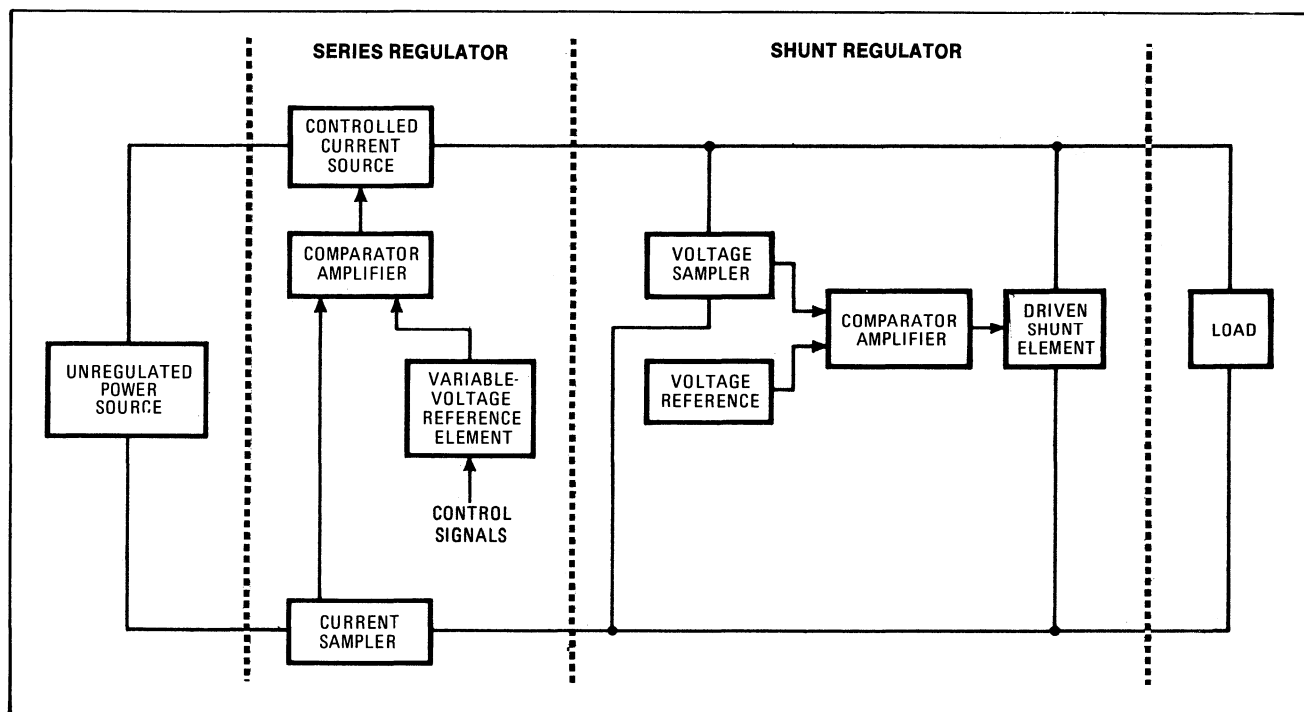
Series-shunt hybrid

A block diagram of the combined series-shunt regulator is shown in Fig. 3. To maintain a constant output voltage across the load, a feedback element in the shunt regulator senses the output voltage and varies conduction of the shunt element accordingly. As shown, the basic components of the shunt arm are a voltage reference, a voltage sampler, a comparator amplifier, and a driven shunt element.

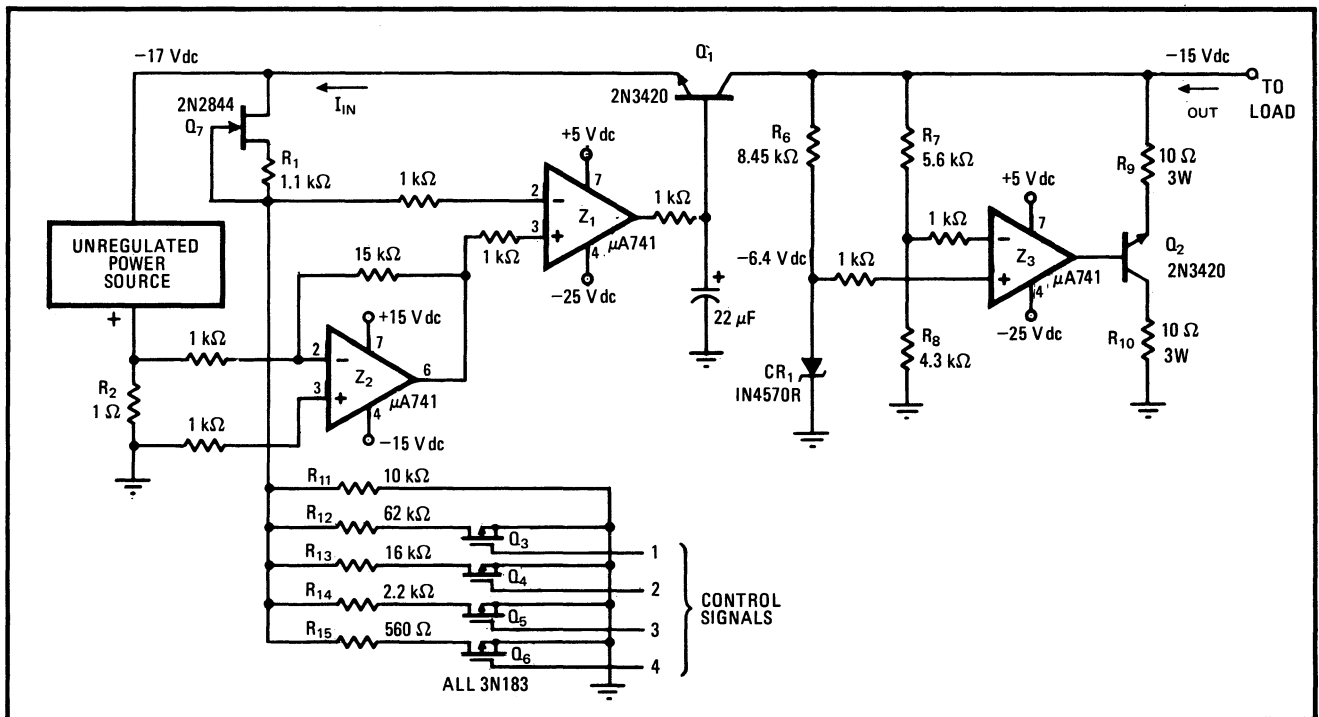
The comparator amplifier compares the reference voltage on one input to a sample of the output voltage on the other input. The resulting amplified error signal drives the shunt element, which conducts to the degree necessary to maintain the output voltage at the level established by the voltage sampler.

When a series regulator element (controlled-current source) is inserted into the series arm of the regulator to supply current to both the driven shunt element and the load, the result is a highly efficient regulator that can be programmed for any given load.

Here's how the regulator controls the current: For a given load, a control signal establishes a reference voltage on one input of the series arm comparator amplifier (Fig. 3). Then a current sampler establishes a voltage, which is directly proportional to the power-source current, on the other input of the comparator. The resulting amplified error signal drives the series-regulator element, which conducts to the degree necessary to maintain a constant current from the power source at the level established by the external control signal. To



3. Series-shunt hybrid. Combining the series and shunt regulator elements provides a hybrid regulator capable of operating over a wide load variation, with both the high output-to-input isolation of the shunt unit and the high efficiency of the series unit.



4. Circuit details. In the 15-volt regulator circuit, control signals that correspond to predetermined system load requirements set the maximum current level through the series-regulator element. Within that limit, the shunt regulator compensates for changes in load requirements.

ensure maximum efficiency for all load conditions, the unregulated source-input current for each load condition is adjusted so that there is a large ratio of load current to shunt-element current.

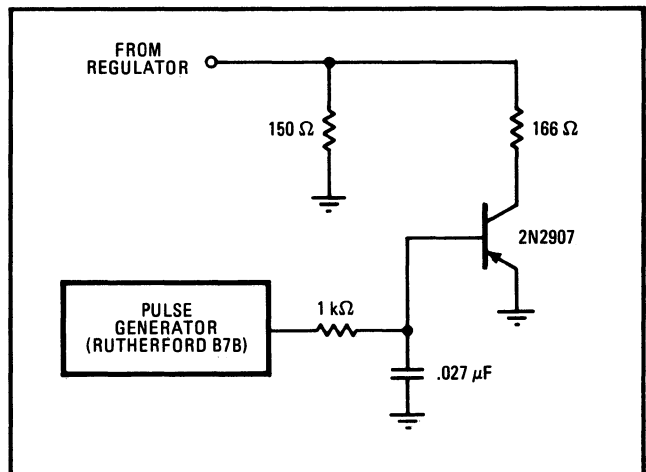
A working system

In a power supply for a given system application, the regulator configuration shown in Fig. 3 would be repeated for each subsystem needing isolation, and, of course, for each voltage level required by the system. The actual circuit for a -15-volt regulator in the radio system is shown in Fig. 4. The voltage-sampling circuit for the shunt regulator consists of the resistive divider R₇ and R₈, while the voltage reference is obtained from resistor R₆ and zener diode CR₁.

The sampled voltage and reference voltage are compared by amplifier Z₃. The output error-signal varies the conductance of the regulator shunt element, npn transistor Q₂, to maintain a constant output voltage.

In the series-regulator arm, a variable reference voltage at the input to Z₁ is established by a constant-current source feeding resistors, which are switched in and out of the current path by control signals from the mode switch. The constant-current source, consisting of R₁ and Q₇, is selected to guarantee a constant current over all operating variations of input voltage and temperature conditions. This constant current flows through resistor R₁₁ and a combination of resistors R₁₂, R₁₃, R₁₄, and R₁₅ and is controlled by signals through p-channel MOS field-effect transistors Q₃, Q₄, Q₅, and Q₆.

Current through the unregulated source flows through sampling resistor R₂ and produces a voltage which is amplified in Z₂. Amplifier Z₂ allows the use of resistor, R₂, whose resistance should be much smaller than the smallest load resistance. This amplified signal, proportional to the power-source input current, is then



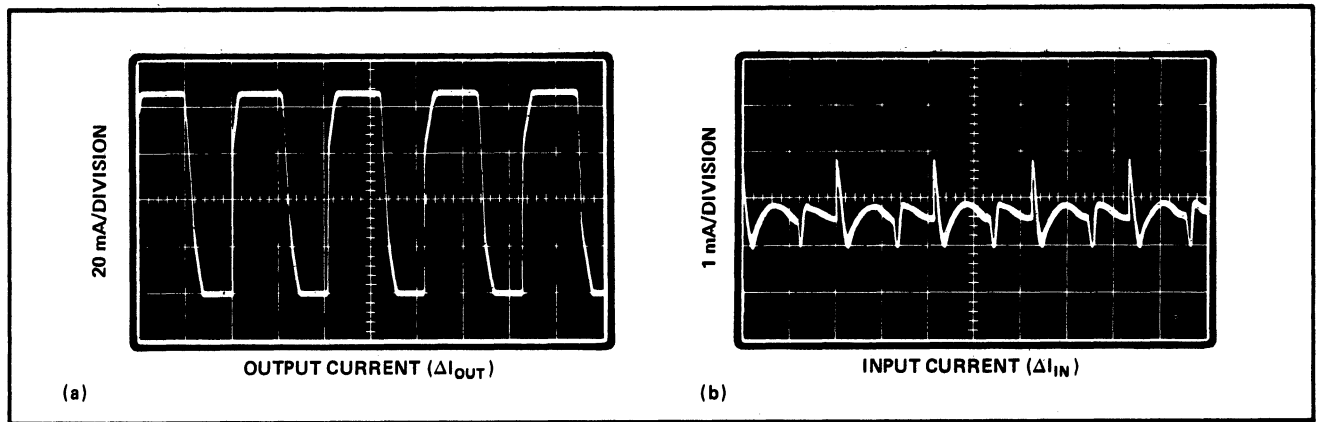
5. Load change. To test the isolation achieved in the series-shunt regulator, a 166-ohm resistor load was switched in parallel across a 150-ohm load. Switching rate was 10 kHz.

applied to comparator amplifier Z₁. In turn, the output of amplifier Z₁ drives the series regulator element Q₁.

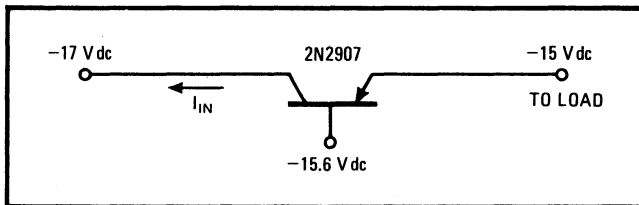
The -15-volt regulator has been operated over a full range of loads with about 85% efficiency and with excellent output-to-input insulation.

System-control signals for the operating regulator, with their corresponding input and output currents are shown in the table. As indicated, the regulator was tested at a maximum current of 400 milliamperes (R_L = 37.5 ohms) down to a minimum current of 25 mA (R_L = 600 ohms).

For all control-voltage settings and load variations, the regulated output voltage shows no change. For any given load setting, so long as series current is sufficient to maintain satisfactory conduction through the shunt element, efficiency can be increased by decreasing cur-



6. Isolated. The ratio of the current at the output (above) to the input (below) of the hybrid regulator shows that isolation of greater than 30 dB is achieved. Isolation of high-frequency components can be further improved by adding a capacitor across the output.



7. Series-check circuit. For comparison with the hybrid regulator, a simple series regulator has been constructed and isolation data taken. No noticeable output-to-input isolation is observed, since virtually all of the current variations caused by the load are transferred back to the prime dc power source.

rent through the series regulator. As indicated above, this series current is controlled by the series-element drive level at the output of Z_1 .

Isolation tests

Tests were also performed to obtain a quantitative measure for the improvement in isolation achieved in using the series-shunt regulator. In these tests, a 2N2907 transistor was driven by a 10-kHz square wave to alternately switch a 166-ohm resistor in and out of the load circuit (Fig. 5). For a regulated output of -15 volts, such load-switching action produces a load-current variation of approximately 86mA at the regulator output.

The control-signal input for the series-shunt regulator was set at -3 volts to allow approximately 200 mA current to pass through the regulator's series arm. The resulting output and input current waveforms for the load-

ed regulator are shown in Fig. 6a and 6b, respectively.

From Fig. 6, the output-to-input isolation for the series-shunt regulator, including all frequency components, is:

$$20 \log(\Delta I_{out}/\Delta I_{in}) = 20 \log(86/1.8) = 33.6 \text{ dB}$$

For comparison, a simple series voltage-regulator circuit (Fig. 7) was constructed and tested with the same switched load. The resulting output and input current waveforms show that there is no isolation whatsoever.

The isolation in the series-shunt regulator can further be improved by placing a capacitor across the output of the series-shunt test circuit, thus removing the high-frequency switching components.

The ability of the regulator output to respond rapidly to load change is limited by the response time of its feedback-control circuitry, and during this response time, the output voltage will decrease. To prevent such voltage fallout, the shunt-regulator control signal is applied for a certain length of time before the regulator load is allowed to change. This permits the regulator to be idling at the higher current, and when the load is increased, the response time is negligible.

The hybrid regulator system has built-in short-circuit protection that the power source input current is limited to the maximum series-element load current for a given load selection. Such a design also lends itself to hybrid integrated-circuit design, especially for low-current applications. For high-current requirements, the shunt and series elements would be discrete devices. □

HYBRID REGULATOR TEST RESULTS

| CONTROL SIGNAL | | | | INPUT CURRENT @ -17 V dc | LOAD CURRENT @ -15 V dc | LOAD | EFFICIENCY |
|----------------|-------|-------|-------|-----------------------------|----------------------------|-------|------------|
| #1 | #2 | #3 | #4 | | | | |
| Gnd | Gnd | Gnd | Gnd | 410 mA | 400 mA | 38 Ω | 86% |
| -15 V | Gnd | Gnd | Gnd | 360 mA | 350 mA | 43 Ω | 86% |
| Gnd | -15 V | Gnd | Gnd | 260 mA | 250 mA | 62 Ω | 85% |
| Gnd | Gnd | -15 V | Gnd | 90 mA | 85 mA | 175 Ω | 84% |
| Gnd | Gnd | Gnd | -15 V | 30 mA | 28 mA | 600 Ω | 82% |

Choosing a sample-and-hold amplifier is not as simple as it used to be

Sample-and-hold modules, which are particularly useful in high-speed data acquisition systems, are now available in unprecedented variety; a grasp of how they work makes it easier to pick the right one for a given job

by Walter Patstone and Craig Dunbar, *Teledyne Philbrick, Dedham, Mass.*

□ As a naturally analog world goes steadily digital, the sample-and-hold amplifiers that often accompany analog-to-digital converters also increase in variety. The modules now available range from general-purpose units to high-speed, high-accuracy versions and cost anywhere from \$40 to \$400. Unless their characteristics are understood, it's no longer simple to select the right sample-and-hold for a given application.

Functionally, every sample-and-hold amplifier tracks an analog signal and, when directed by an external digital command, freezes its output at the instantaneous value of the input. But the individual parameters of this performance vary in importance with the particular application.

And the applications are numerous. Sample-and-hold amplifiers are particularly useful where fast-changing

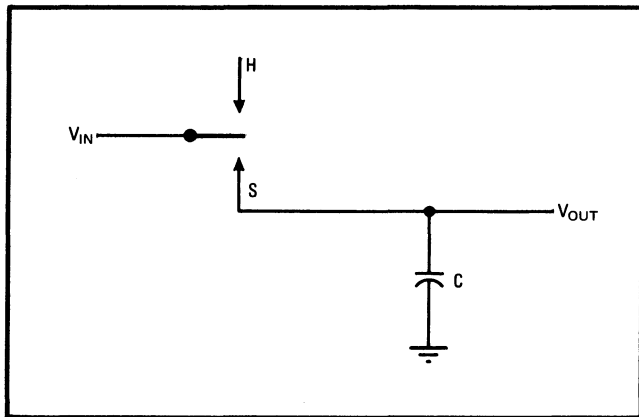
signals must be multiplexed in data acquisition systems or where momentary signals must be captured and held. They are frequently used in sampled-data systems to decrease system aperture time with a-d converters, and in display systems to provide smooth, glitch-free outputs from d-a converters. Other applications include pulse stretching, data distribution to multiple readouts, peak and valley following, and ratio-measurement of time-averaged variables.

The basic circuits

Probably the simplest form of sample-and-hold amplifier is the capacitor-switch combination shown in Fig. 1. With this circuit, the hold command is given when the switch is thrown from position S to position H. But though the circuit works effectively with very slowly

Experience. Authors Walter Patstone (foreground) and Craig S. Dunbar have been working together at Teledyne Philbrick for the past four years on the application of circuit modules. One result of their study of applications problems is the model 4853 sample-and-hold amplifier.





1. Simplest. If speed and circuit loading are not too important, a capacitor and a switch make an effective sample-and-hold circuit.

changing signals, it causes too much source and output loading to be of much practical use.

Most practical modular sample-and-holds are designed for noninverting unity-gain operation, but important new inverting designs are now available. In both types, the control inputs are normally operated at standard logic levels and are usually TTL-compatible. Typically logic 1 is the sample command and logic 0 is the hold command.

The basic noninverting sample-and-hold amplifier consists of a resistor, a switch, a capacitor, and an op amp (Fig. 2a). When the switch is closed, the capacitor charges (or discharges) exponentially to the input voltage just as in the simple capacitor example. The output of the operational amplifier follows the capacitor voltage precisely. Again, when the switch is opened, the capacitor holds the instantaneous value of the input voltage. The advantage of the op-amp follower in this circuit is that, once the charge is acquired and the switch is opened, output loading will not discharge the capacitor.

In such a circuit, a FET switch would most probably be used, and the op amp would have a FET input. However, the storage capacitor still loads the input sources, and this loading, if R is too low, may make the source oscillate or overload it. When the source is overloaded at acquisition time, recovery time normally is long.

Increasing R to prevent these problems will slow the response time, and instead, a buffer amplifier can be added in front of the capacitor (Fig. 2b). Here the input is isolated from the holding capacitor, and the buffer amplifier provides the capacitor charging current.

This circuit is pretty fast, but since the amplifiers work independently, a summation of errors results. Consequently, if low-frequency tracking accuracy is more important than speed, the feedback loop can be closed around both amplifiers, forcing both to track as one amplifier (Fig. 2c).

The other basic type of sample-and-hold amplifier—the inverting, or integrating, circuit—is shown in Fig. 3. Because the capacitor is in the feedback loop, the input is isolated, and the FET switch operates at ground potential, minimizing leakage current and switching time, while the amplifier is not bothered by a common-mode signal. Although this type of circuit does not require a buffer amplifier to charge the capacitor or isolate the in-

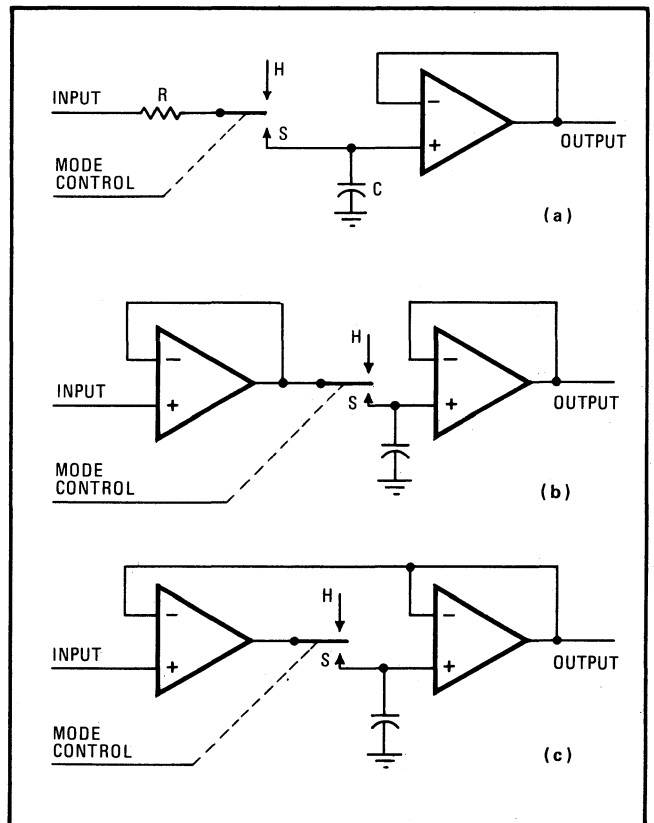
put, its input impedance is significantly lower than in the buffered noninverting types. Therefore, the signal source must have a reasonable drive capability and a low output impedance. No problem will arise, however, if an op amp is used as a preamp.

The modification of the inverting sample-and-hold amplifier shown in Fig. 3b places an inverting buffer amplifier in front of the switch but within the feedback loop. Since the inverting input is floating, high-input impedance is provided. If a FET buffer is used, the current required to drive the circuit will be in the picoampere range. However, the addition of the input buffer introduces common-mode error, and additional nonlinearity error, besides reducing speed.

The parameters

In selecting the proper sample-and-hold for a given application, certain specifications are more critical than others. The nomenclature for these is not yet standardized, but the following discussion is based on terms generally accepted in the industry.

Aperture time is the apparent time elapsed between the hold command and the effective opening of the hold switch (Fig. 4a). As the diagram shows, the error caused by the aperture time increases both with the aperture time itself and with the rate of change of the input signal. In actual practice, properly designed FET switching circuits can keep the aperture time, or turn-off time, down to a few nanoseconds.



2. Noninverting circuit. Basic circuit (a) overcomes the capacitor-switch circuit's sensitivity to output loading. Source loading, however, remains a problem unless an input buffer amplifier is added (b). Putting a feedback loop around both amplifiers improves low-frequency performance but slows the system (c).

Aperture time, by itself, is not a problem for most applications; it may be regarded as a timing delay. Therefore, to the extent that it is repeatable, it may be compensated for by advancing the control timing. Typical values of aperture time for high-performance sample-and-hold range from 5 to 40 nanoseconds.

Aperture-time uncertainty is the term for the repeatability of the aperture time. It can also be thought of as the uncertainty in the sample-to-hold transition time, or the difference between the maximum and the minimum aperture times experienced with a particular amplifier. This parameter is a major factor in determining the maximum signal frequency which can be accurately sampled. Commercially available sample-and-hold amplifiers with maximum aperture uncertainty times of ± 1 nanosecond will permit the sampling of 16-kilohertz signals to a 12-bit (.01%) accuracy.

In digitizing a continuously varying audio or video signal the aperture uncertainty time must be low to minimize jitter and the noise it causes on the reconstructed signal. Note, too, that in this application the delay identified with aperture time is usually unimportant, and no delay compensation is necessary.

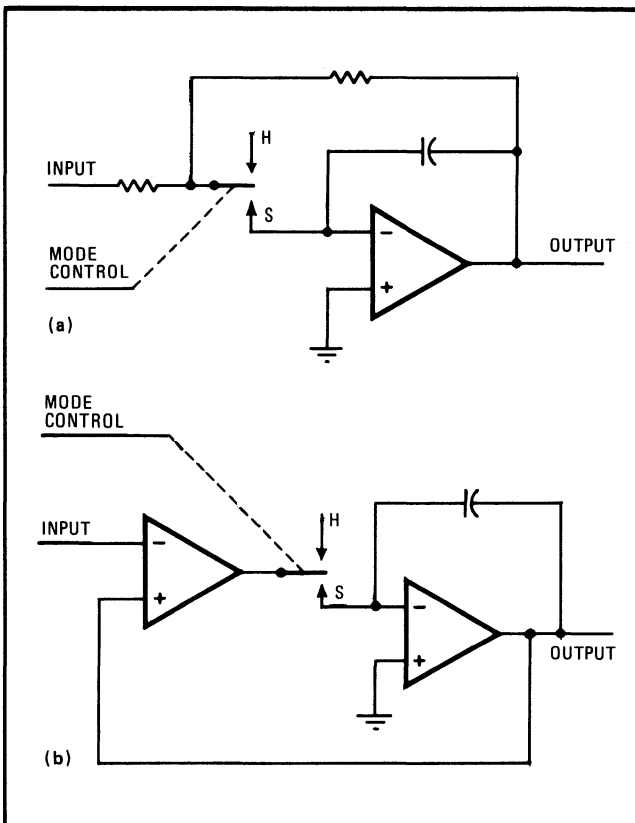
Acquisition time is the length of time that elapses between the sample command and the precise instant at which the output voltage is tracking the input voltage to within a specified accuracy (Fig. 4b). For the switch-capacitor circuit, acquisition time depends on the charging current available from the driving source current. When

the switch is closed, the capacitor charges or discharges exponentially with a time constant that is a function of the source impedance and hold capacitance.

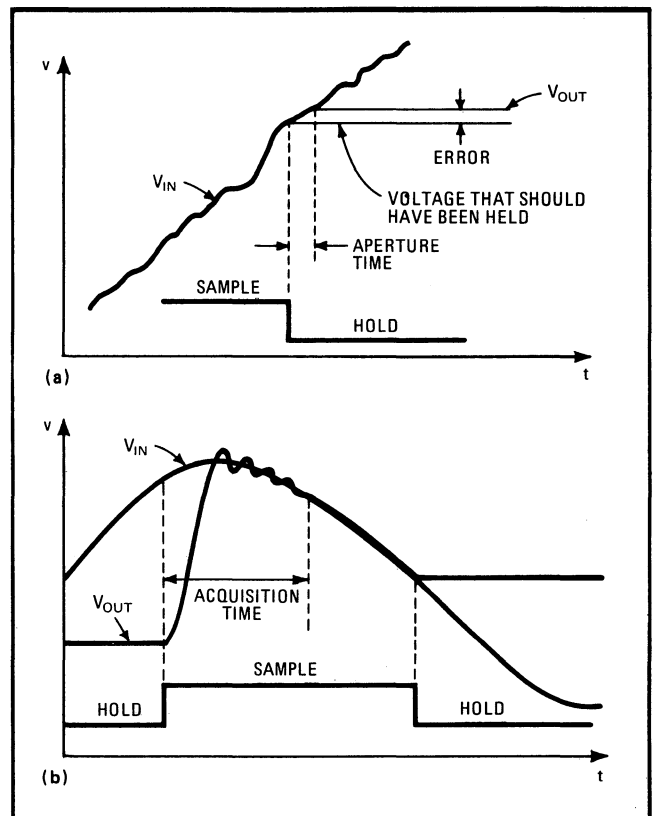
The worst-case acquisition time occurs when the sample-and-hold circuit must change full scale. Therefore, specifications are normally written in terms of a full-scale voltage step, and the specified accuracy is usually stated as a fraction of a percent of full scale, for example 0.01% or 0.1%. Acquisition time in simple circuits consists primarily of time constants; in more sophisticated designs, amplifier slew rate and settling time have to be included.

One problem that occurs even in the simplest sample-and-circuit hold is the presence of voltage spikes associated with switching transients. These spikes are not only annoying in themselves but also constitute a major source of circuit error. When the capacitor is switched from sample to hold, some charge is transferred to the holding capacitor due to the inter-electrode capacitance of the switch. This charge, translated into an error voltage, is called the *hold jump voltage* by some manufacturers and the *sample-to-hold offset* by others. In packaged circuits, it's usually possible to trim out the jump voltage, but necessary to live with the spikes.

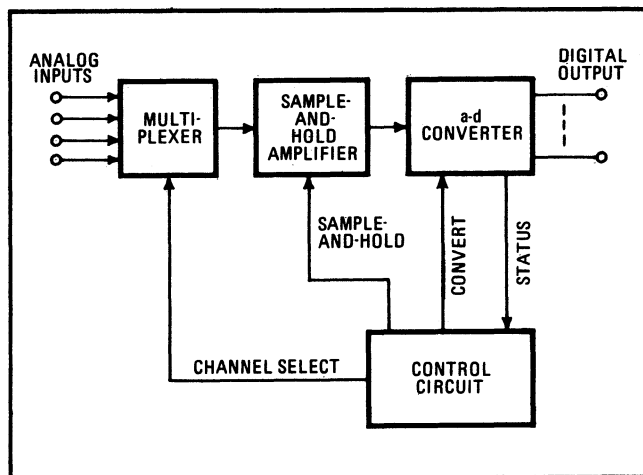
Related specifications are the *sample offset voltage* (the error voltage encountered in the sample mode, which is basically due to the offset voltage of the internal op amp) and the *hold offset voltage* (the error voltage encountered in the hold mode and composed of the



3. Inverting circuit. When a capacitor is inserted in the feedback loop, the inverter effectively isolates the input and minimizes the switching time (a). This approach is used in Teledyne Philbrick's 4853 sample-and-hold amplifier. Input impedance is low, however, unless an input buffer amplifier is added (b).



4. Definitions. Aperture time is the delay between the arrival of the hold command and the actual opening of the switch (a). Acquisition time is the length of time that will elapse before the amplifier starts tracking the input signal to within some specified accuracy after it has been commanded to do so (b).



5. Working within the system. By providing a constant input voltage to the a-d converter while the multiplexer is switching channels, the sample-and-hold circuit eases the converter's speed constraints.

hold jump voltage and the sample offset voltage). These three voltages are not major sources of error in most applications because all are trimmable to zero. For driving an a-d converter, it is normally sufficient to trim only the hold offset to zero.

During hold, a small part of the input signal feeds through the capacitance of the switch to the output. This *feedthrough*, which is usually a function of the level and frequency of the input signal, can be thought of as the input-output transfer function of the sample-and-hold amplifier while in the hold mode. Ideally, feedthrough should be zero.

If a data acquisition system contained an ideal sample-and-hold amplifier, the basic limitation on its throughput (or rate of transmission of data) would be the conversion speed of its a-d converter, because the multiplexer could be switching to another channel during the conversion. However, many commercially available sample-and-hold amplifiers demonstrate such high feedthrough that switching the multiplexer during the conversion period would give rise to intolerable errors. Some modules therefore use a clamping network to limit feedthrough to ± 1 millivolt maximum for a ± 20 -V input step. This permits increased throughput for 12-bit data acquisition systems.

Decay rate

Also while in the hold mode, a typical sample-and-hold amplifier will exhibit a decay of its output voltage over a period of time. This relatively constant output drift, termed the *decay rate*, is usually specified in microvolts per second. For the simple switch-capacitor circuit, it is caused by leakage currents through both the switch and the hold capacitor. In more complex circuits, it should be noted that the decay can be either positive or negative, depending on the polarity of the buffer amplifier bias current. Further, it is usually sensitive to temperature—with FET buffers, at any rate, the bias current doubles for each 10°C rise in ambient temperature.

The importance of the decay rate depends on the length of the hold time and the desired accuracy. In high-speed applications the hold periods are seldom longer than 100 microseconds, so decay rate errors are



6. Fast and accurate. Philbrick's 4853 is suitable for use with 12-bit converters at speeds up to 20 kHz. Input voltage range is ± 10 V, input impedance is 2 k Ω , and aperture time uncertainty is ± 1 ns.

unimportant even when the decay rate is as high as 1 microvolt per microsecond.

Perhaps the most difficult and sophisticated application for a sample-and-hold amplifier is in a very-high-speed data acquisition system, like the one outlined by the simplified block diagram of Fig. 5. The sample-and-hold circuitry maintains a constant input to the a-d converter during the conversion period while the multiplexer is seeking the next channel to be converted. After the first conversion is complete the sample-and-hold amplifier samples the next input, and the cycle is repeated. Sampling can be synchronized with the other system components, or it can be performed asynchronously.

In such a system, nearly all parameters are important except decay rate—that is, acquisition time, aperture time, aperture uncertainty time, bandwidth and feedthrough must all be considered in the designer's error budget because they all can affect the throughput data rate. The feedthrough is especially critical in multiplexed systems.

Note that the designer of a data acquisition system frequently has a choice of approaches for handling a known throughput rate. For example, many applications allow the use of a sample-and-hold amplifier with a moderate-speed a-d converter as an alternative to a very-high-speed a-d converter. Use of the moderate-speed combination often results in significant cost savings.

In the fast system, decay rate is not very important because the signal is usually not held for any significant length of time. The opposite is true of slow applications, where the most important parameter would be decay rate and all others would be of minor consequence.

One example of such a slow application is the mechanical test system measuring deformation in a titanium aircraft forging that is being subjected to a constantly increasing load. At predetermined points in time the sample-and-hold freezes the transducer signal so that it can be read out and displayed. Here the decay rate should be low enough to keep the reading within the desired accuracy right to the end of the maximum hold period. □

Switching regulators: the efficient way to power

The switching regulator, which offers the advantages of high efficiency, small size, and cool operation, can be made to supply a low-noise output through careful filter design and prudent semiconductor selection

by Robert S. Olla, *Diablo Systems Inc., a subsidiary of Xerox Corp., Hayward, Calif.*

□ Although switching regulators make power supplies that are two to three times more efficient than the dissipative type, while remaining cost-competitive, many designers believe they are noisy and avoid using them. But with today's wide selection of fast-switching low-noise power semiconductors, reliable switching regulators can easily be built that are almost free of noise. What's more, careful filter design will also enhance semiconductor performance. For example, a switching-regulator power supply can provide an output of 2 to 200 volts at 5 to 50 amperes, holding regulation to 0.01% and ripple and noise voltage to 1 millivolt.

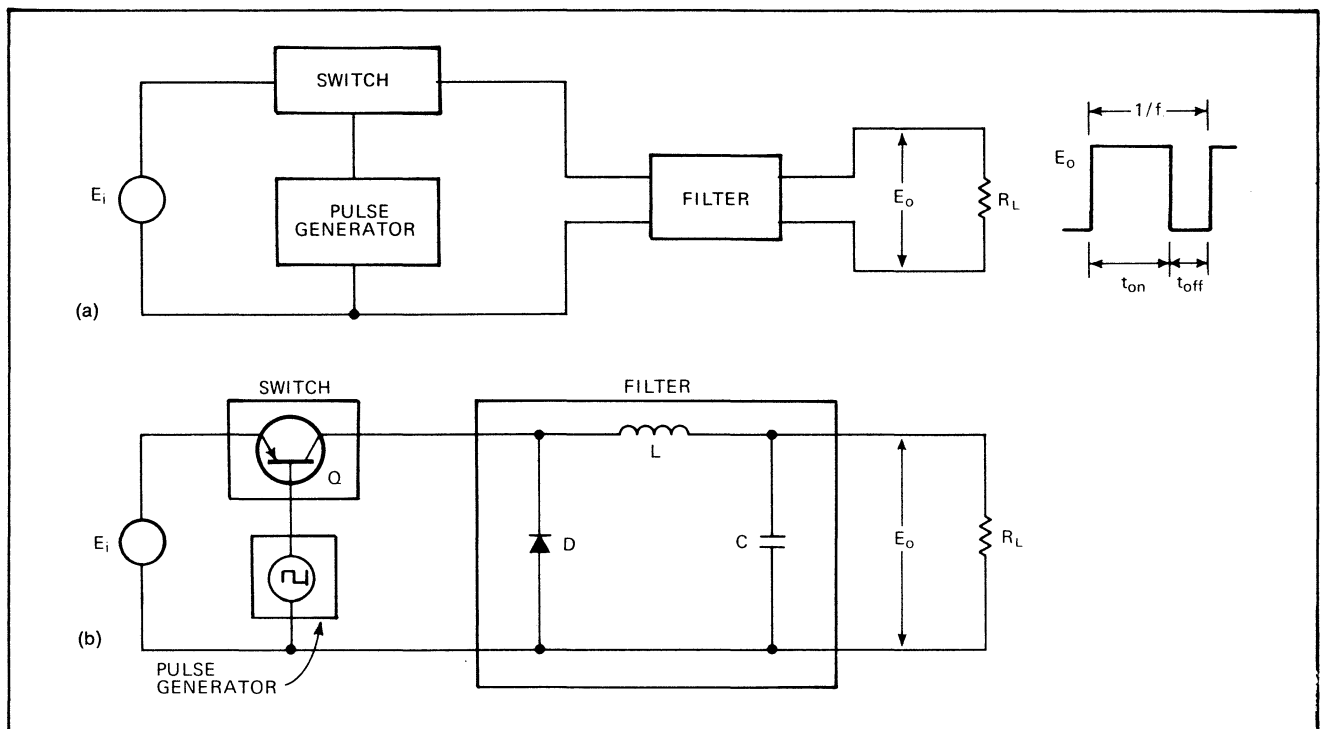
Besides having lower noise, switching regulators are more reliable than dissipative regulators because they operate at lower temperatures. This also extends the life of the supply, since its components do not age as quickly. Other advantages are its smaller size and lower weight, while, as fringe benefits, its higher operating fre-

quencies permit inductors and transformers to be less bulky and its lower temperatures allow smaller heat sinks.

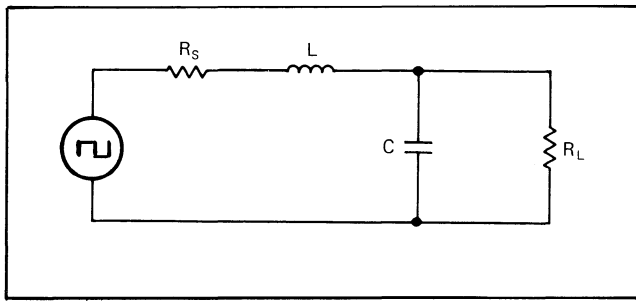
The basic switching regulator

As shown in Fig. 1a, a switching regulator basically consists of three sections: a switch, a pulse generator, and a filter. The voltage source, E_i , may be any dc voltage requiring regulation, like a battery or the output of a rectifier. Generally, E_i must be at least twice as large as the desired output voltage, and the input power must be large enough to supply the output power needed.

The switch is usually a transistor or thyristor power device, which is switched between its saturation and cutoff regions. The pulse generator does this on/off switching by varying its output pulse rate or pulse width as a function of line and load conditions. When pulse-width modulation is used, the generator produces a



1. Elementary regulator. Block diagram (a) of basic switching regulator outlines the principal circuit sections, which are then detailed in (b). Input voltage E_i can be any unregulated dc source. Regulator operating frequency is determined by the rate at which the pulse generator turns the transistor switch on and off. The filter and commutating diode average the pulses from the switch to some dc voltage.



2. The right filter. Series-parallel RLC filter works best in regulator applications because its inductor and its capacitor can be chosen, almost independently, to optimize regulator performance. The inductor influences overshoot, transient response, and load current, while the capacitor establishes noise and ripple characteristics.

nonsymmetrical square wave that has a frequency usually on the order of tens of kilohertz.

The filter is perhaps the single most important section of the switching regulator. To a large extent, it determines the regulator's efficiency and transient response, as well as ripple and noise voltages. In addition to averaging the pulses from the switch, the filter must remove the high-frequency components of these pulses. Regulator output voltage, E_o , can be expressed by:

$$E_o = t_{on}E_i / (t_{on} + t_{off}) \quad (1)$$

with:

$$t_{on} + t_{off} = 1/f \quad (2)$$

where f is the pulse generator frequency.

For regulator applications, the RLC filter (Fig. 1b) is the best choice because it permits high power efficiency to be achieved. For instance, even though the transistor switch is off, the inductor's induced voltage continues to charge the capacitor through the commutating diode, thereby increasing efficiency. Moreover, during light load demands, the energy stored in the capacitor supplies the load, while during heavy load demands the energy stored in the inductor supplies the load. This means that both L and C can be chosen for optimum regulator performance. (Of course, their values must be kept within reasonable limits.)

Besides storing energy for the regulator, the inductor limits the regulator's transient response as well as the peak load (capacitor) current. The capacitor, on the other hand, primarily determines the regulator's ripple and noise voltages. Both the inductor and the capacitor, therefore, are critical components and, needless to say, must be selected carefully.

Filter considerations

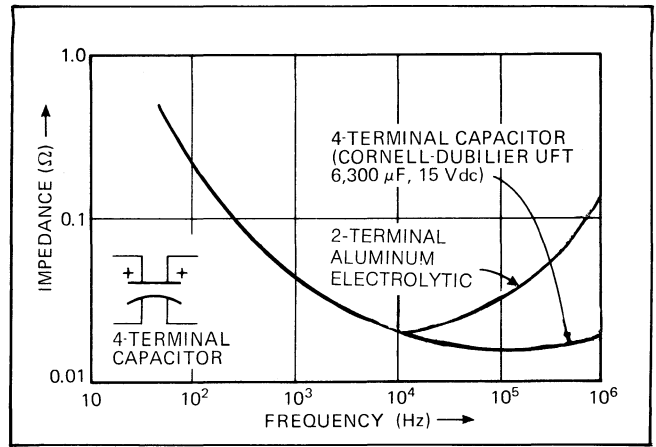
The RLC filter that is best for switching regulator applications can be represented by the series-parallel RLC circuit of Fig. 2, where R_S is the source resistance of the pulse generator. The circuit must be prevented from oscillating because of the power losses that will result. To avoid this underdamped condition when there is no load:

$$R_S^2/4L^2 \text{ must be greater than } 1/LC \quad (3)$$

or, with a load:

$$1/4R_L^2C^2 \text{ must be greater than } 1/LC \quad (4)$$

If R_S is small and R_L large, the circuit will oscillate. Since R_S is fixed under light or no-load conditions, the first inequality may not be met, making it necessary to



3. Special capacitors. Four-terminal capacitors are ideal for regulator circuits, providing good noise filtering and isolation from ground loops. The graph shows how a special capacitor exhibits low impedance even at high frequencies, while the impedance of a conventional capacitor increases beyond 10 kilohertz. These four-terminal units can be used at the regulator's input and output.

find a minimum R_L that meets the second inequality. Because the load seldom goes to zero, the load alone may be large enough to prevent oscillations. If it is not, the power supply should be preloaded.

The transient overshoot of the regulator can be found from classic inductor and capacitor relationships:

$$dt = L(di)/e_L = C(dv)/i_C$$

where $di = i_C =$ capacitor current, dv is capacitor voltage, and e_L is inductor voltage. The change in capacitor voltage is the transient overshoot:

$$\Delta E_o = dv = L(\Delta i)^2 / C e_L$$

For increasing loads:

$$\Delta E_o = L(\Delta i)^2 / C(E_i - E_o) \quad (5)$$

For decreasing loads:

$$\Delta E_o = L(\Delta i)^2 / C E_o \quad (6)$$

Similarly, the regulator's transient response, or recovery time, can be computed. For increasing loads:

$$t_r = 2L\Delta i / (E_i - E_o) \quad (7)$$

For decreasing loads:

$$t_r = 2L\Delta i / E_o \quad (8)$$

Since the load current increases in a linear fashion, the value of inductor L can be expressed as:

$$L = (E_i - E_o)t_{on} / 2(I_{pk} - I_o) \quad (9)$$

where I_{pk} is the peak load current and I_o is the rated load current. Other considerations (besides value) for selecting inductor L include core size, core shape, core material, gap size, and the number of wire turns. For predictable and stable results, L should have a fairly linear inductance.

Choosing the filter capacitor is equally important for a well-designed switching regulator—a poor selection will result in a regulator that is plagued with noise problems. The capacitor's value depends on the output ripple voltage permitted:

$$C = (E_i - E_o) / 4\pi^2 f^2 L E_r \quad (10)$$

where C is expressed in farads, L in henries, f in hertz, and E_r is the maximum allowed peak-to-peak ripple voltage. The capacitor's voltage rating should be at least 1.2 times larger than E_o .

There are even special four-terminal capacitors that are intended mainly for switching regulator appli-

cations. They are low-inductance devices exhibiting excellent high-frequency characteristics. Figure 3 compares the impedance of a four-terminal capacitor with that of a quality two-terminal aluminum electrolytic capacitor. At high frequencies, the four-terminal device is clearly superior for regulator applications because of its lower impedance. Also, four-terminal capacitors provide good isolation from ground loops and good noise filtering for both the source and output voltages.

Picking the semiconductors

Choosing a commutating diode for the filter is a relatively simple task—a matter of simply looking through manufacturers' data sheets. In addition to safely handling all peak currents, the diode must have a short recovery time, a small forward voltage drop, and a peak inverse voltage rating that is at least twice as large as the input voltage.

The diode's recovery time is important because of its influence on output noise. After the switching transistor shuts off, the diode conducts, charging capacitor C. When transistor Q turns on again, diode D is still in its conducting state and shorts Q to ground for a little while. This double conduction dissipates power in both transistor Q and diode D and is a prime source of noise.

Like selecting a commutating diode, choosing a switching transistor also involves going through manufacturers' data sheets. The transistor must provide sufficient peak and average current-handling capabilities, as well as a safe collector-emitter breakdown voltage rating. (This voltage is generally 1.2 times larger than E_i .) Additionally, the transistor's saturation voltage should be as small as possible when collector current is at its maximum.

Switching time is the most important transistor specification. Maximum efficiency is achieved when the transistor is either saturated or in cutoff. However, since

transistors cannot switch instantaneously, a considerable amount of power (say 10%) can be dissipated during the switching time. Keeping switching times small compared to the period of the switching frequency will minimize these switching losses.

The switching frequency should be high enough to keep the values of inductor L and capacitor C small, but not so high that transistor Q and diode D become expensive. Typical operating frequencies range from 10 to 50 kilohertz. The source voltage should be from two to five times larger than the output voltage, keeping in mind any high-voltage constraints that apply.

Design procedure

Designing the simple regulator circuit of Fig. 4 will illustrate how to use the equations just given. For this example: $E_i = 5E_o = 25$ volts, $E_o = 5$ v, $I_o = 2$ amperes, and $f = 20$ kHz.

Before calculating component values, some other important circuit parameters must be found. From Eqs. 1 and 2, the on-time of transistor Q can be computed:

$$t_{on} + t_{off} = 1/f = 1/(20 \times 10^3) = 5 \times 10^{-5} \text{ seconds}$$

$$t_{on} = E_o(t_{on} + t_{off})/E_i = E_o(1/f)/E_i$$

$$t_{on} = (5)(5 \times 10^{-5})/(25) = 10^{-5} \text{ seconds}$$

Another important consideration is the regulator's peak current, which is usually 5% to 20% greater than I_o . The smaller the peak current becomes, the larger the transient response is. In this case, let the peak current be 5% larger than I_o , so that $0.05(2 \text{ A}) = 0.1 \text{ A}$. The change in load current becomes:

$$\Delta I_L = 2(I_{pk} - I_o)$$

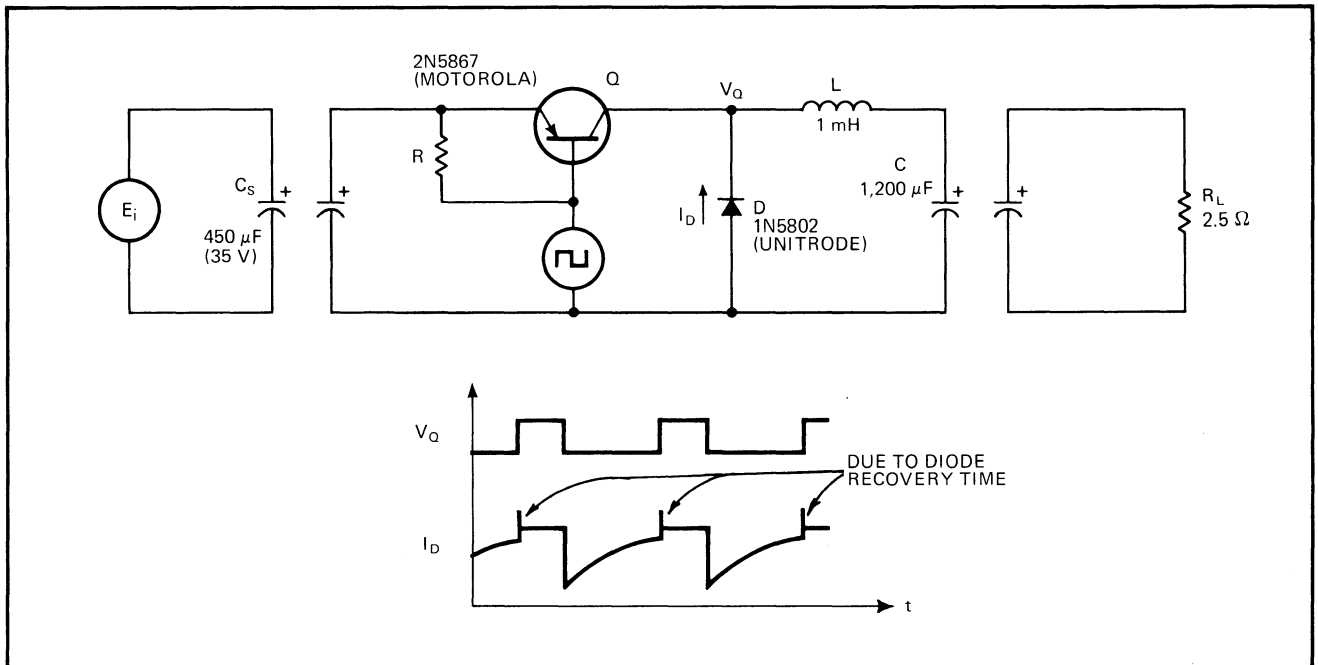
$$\Delta I_L = 2(2.1 - 2) = 0.2 \text{ A}$$

The value of inductor L can now be computed from Eq. 9:

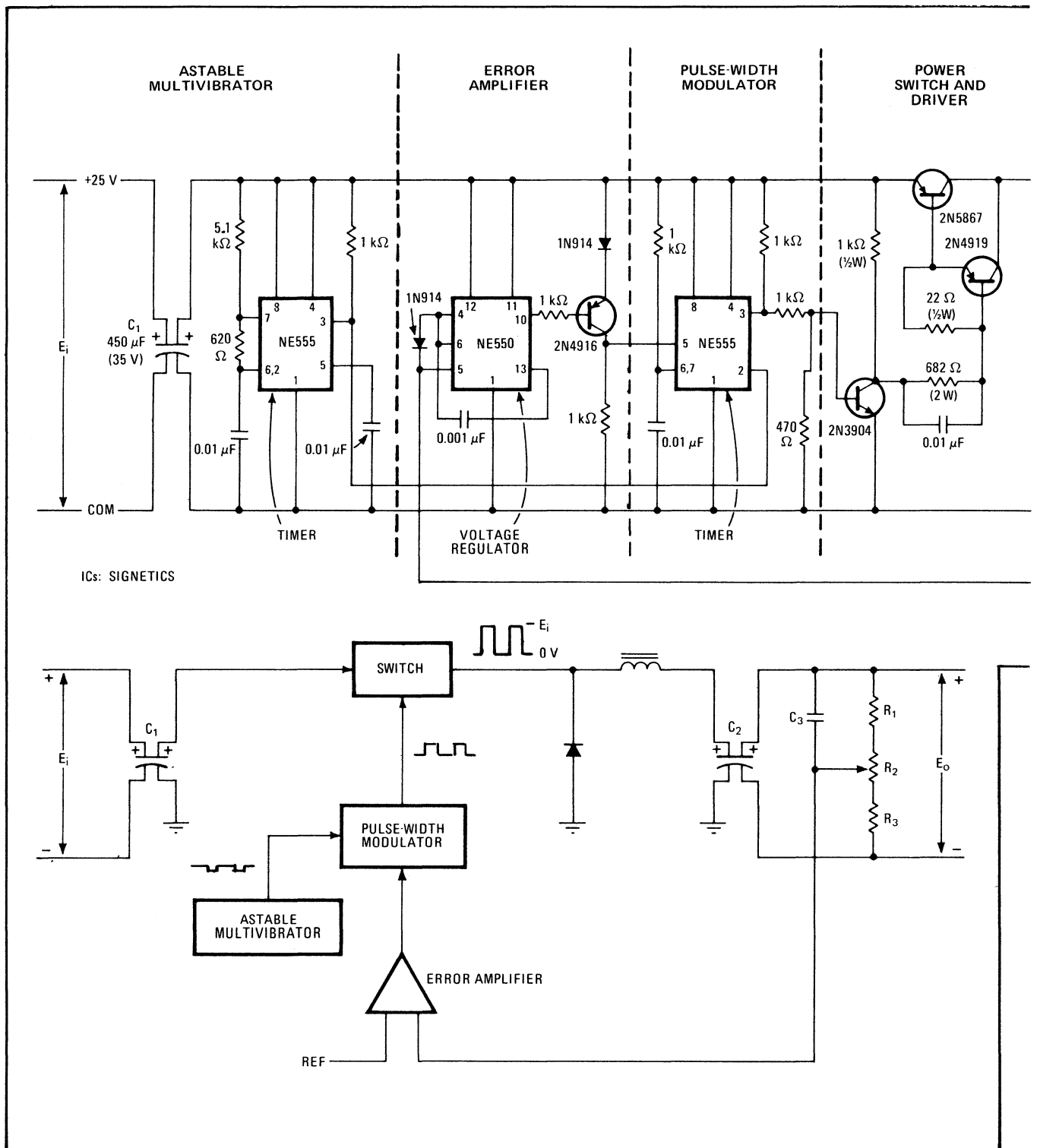
$$L = (E_i - E_o)t_{on}/2(I_{pk} - I_o)$$

$$L = (25 - 5)(10^{-5})/(0.2) = 10^{-3} \text{ H}$$

The value of capacitor C can also be computed. Using



4. Typical design. Once the desired regulator characteristics are known, values for the filter's inductor and capacitor can be computed quite easily. The transistor and the diode are selected from manufacturers' data sheets. Capacitor C_s limits input ripple.



5. Complete circuit. Basic regulator of Fig. 4 is shown here with its associated timing and pulse-generating circuitry. The block diagram illustrates how the over-all regulator works. The multivibrator determines switching frequency, and the error amplifier adjusts the pulse width of the modulator to maintain regulator output voltage at the desired level. The output resistor divider provides the sensing voltage.

Eq. 10 and restricting output ripple to a typical value of 1 millivolt yields:

$$C = (E_i - E_o) / 4\pi^2 f^2 E_r$$

$$C = (25 - 5) / 4(9.85)(4 \times 10^8)(10^{-3})(10^{-3})$$

$$C = 1,200 \text{ microfarads}$$

Once L and C are known, the circuit's stability can be determined. To account for the source impedance as

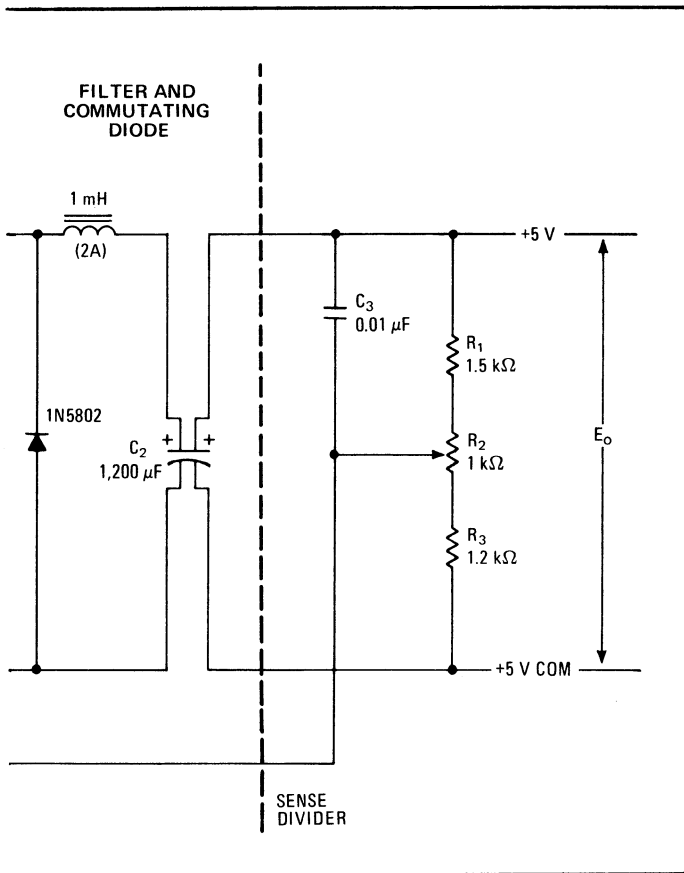
well as all lead resistances and their associated losses, let:

$$R_s = 2 \text{ ohms}$$

The load resistance is:

$$R_L = E_o / I_o = (5 \text{ V}) / (2 \text{ A}) = 2.5 \text{ ohms}$$

Now the circuit's quality factor can be checked with the inequalities of Eqs. 3 and 4. For the no-load condition:



$$CR_s^2/L \text{ must be greater than } 4$$

$$(1.2 \times 10^{-3})(2)^2/(10^{-3}) = 4.8$$

4.8 is greater than 4

Since this inequality holds, the regulator will not oscillate when there is no load. With a load present:

$$L/R_L^2C \text{ must be greater than } 4$$

$$(10^{-3})/(2.5^2)(1.2 \times 10^{-3}) = 0.13$$

0.13 is not greater than 4

which is an oscillatory condition, although the circuit will not oscillate under full load or even half load. If it were to operate with no load, then the last inequality would have to be solved for a minimum R_L .

The regulator's transient response can be calculated by assuming that load current increases from half load to full load (from 1 to 2 A). From Eq. 7, the recovery time for an increasing load is:

$$t_r = 2L\Delta i/(E_i - E_o)$$

$$t_r = 2(10^{-3})(1)/(25 - 5) = 10^{-4} \text{ seconds}$$

For decreasing loads, Eq. 8 applies:

$$t_r = 2L\Delta i/E_o$$

$$t_r = 2(10^{-3})(1)/5 = 4 \times 10^{-4} \text{ seconds}$$

Overshoot can be found from the same conditions just used to compute the transient response. For increasing loads (Eq. 5):

$$\Delta E_o = L(\Delta i)^2/C(E_i - E_o)$$

$$\Delta E_o = (10^{-3})(1)^2/(1.2 \times 10^{-3})(25 - 5) = 40 \text{ mV}$$

For decreasing loads (Eq. 6):

$$\Delta E_o = L(\Delta i)^2/CE_o$$

$$\Delta E_o = (10^{-3})(1)^2/(1.2 \times 10^{-3})(5) = 160 \text{ mV}$$

As shown in the figure, a capacitor, C_s , is placed across the input to keep the source voltage free of high-frequency ripple. If this ripple voltage is to be held to

50 mV or less, as is usually the case, then:

$$C_s = I_{pk}t_{on}/E_r$$

$$C_s = (2.1)(10^{-5})/(50 \times 10^{-3}) = 420 \mu\text{F}$$

A type 2N5867 pnp power transistor can act as the switch for the regulator. Its collector-emitter breakdown voltage is 60 V, its maximum saturation voltage is 1 V, its average collector current is 5 A, and its switching rise time is 0.7 microsecond. When no switching signal is present, resistor R will turn off the transistor.

A high-efficiency fast-recovery diode, a type 1N5802, makes an excellent commutating diode for the regulator's filter. It offers a peak inverse voltage rating of 50 V, handles average currents of 2.5 A, withstands peak currents of 35 A, has a forward voltage drop of 0.875 V, and switches in only 25 nanoseconds.

The complete regulator

All the components for this basic regulator circuit are now determined. A complete switching regulator, one that includes all the necessary pulse-generating and timing circuitry, is illustrated in Fig. 5, along with its block diagram. It includes the basic regulator just designed.

As indicated, there are five major sections: an astable multivibrator, an error amplifier, a pulse-width modulator, a power switch and driver, and a filter and commutating diode. The multivibrator, which employs an IC timer, determines the regulator's switching frequency. The error amplifier is an integrated voltage regulator that contains its own precision internal reference; it establishes a feedback path from the output. Like the multivibrator, the modulator makes use of an IC timer, but this one is wired as an adjustable monostable multivibrator. The power switch is a complementary Darlington pair. Four-terminal capacitors are used at both the regulator's input and output.

The block diagram sums up how the regulator works. The multivibrator triggers the pulse-width modulator approximately every 50 μs , turning the switch on and off. The modulator's pulse width is determined by the output of the error amplifier. The filter averages the voltage output from the switch to some dc level.

The voltage divider formed by resistors R_1 , R_2 , and R_3 samples the output voltage. This voltage is then compared, by the error amplifier, with a reference voltage, permitting an error voltage to be generated. The error voltage increases the modulator's pulse width if the output voltage is low with respect to the reference voltage. If the output voltage is higher than the reference voltage, the error voltage decreases pulse width.

Capacitor C_3 bypasses the resistor divider for ac voltages, resulting in lower output ripple. □

BIBLIOGRAPHY

- A.E. Richmond, "Calculus for Electronics," McGraw-Hill Book Co., New York, 1958.
- Egon Brenner, and Javid Mansour, "Analysis of Electric Circuits," McGraw-Hill Book Co., New York, 1959.
- Phillip Cutler, "Electronic Circuit Analysis (Vol. 1: Passive Networks)," McGraw-Hill Book Co., New York, 1969.
- Jerry Eimbiner (ed.), "Designing with Linear Integrated Circuits," John Wiley & Sons Inc., New York, 1969.
- Michael English, "Need to Design A Switching Regulator?" Electronic Design, Jan. 4, 1970, pp.106-111.
- RCA Designer's Handbook, "Solid State Power Circuits," Technical Series SP-52, Somerville, N.J., RCA Solid State Division, 1971.
- Cornell-Dubilier Electronics, "Aluminum Electrolytic Capacitors, Low Inductance Type UFT (Class 210.68)," Division of Federal Pacific Electric Company, September, 1972.
- R.S. Olla, "Designing Switching Regulators," Cornell-Dubilier, 1973.
- Triad Distribution Division, "Inductors—Toroidal and Power."

Impedance-sensitivity nomograph aids design of trimming networks

Adding a fixed-value impedance to a trimming network makes the circuit less sensitive to the variable component's value so that the stability of the variable resistor, inductor, or capacitor is not so critical

by Lawrence R. Odess, *Motorola Israel Ltd., Tel-Aviv, Israel*

□ Most circuits require final adjustment to meet specified design parameters. This adjustment is often accomplished by varying one or more of the circuit's impedance values. Unfortunately, variable-impedance components—like potentiometers, trimmer capacitors, and variable inductors—are usually considerably less stable than comparable fixed-value components, with respect to temperature, humidity, and time. And those variable components that provide good stability tend to be rather costly.

To utilize a variable impedance without degrading circuit stability, the circuit's sensitivity to the value of the variable component must be minimized. This can be done by adding an extra fixed-impedance component to the trimming network for the circuit. The technique is useful for all three types of trimming networks—resistive, inductive, and capacitive.

Generally, a trimming network consists of a fixed impedance as well as a variable impedance. The impedance ratio of these two components determines the network's trimming range and sensitivity. Typical trimming networks for the three kinds of passive components are shown in Fig. 1.

The addition of a second fixed impedance to any one of these trimming networks results in the circuit of Fig. 2. It is less sensitive to the value of the variable impedance, and the arrangement can be used for a resistive or capacitive trimming network.

The sensitivity function—the sensitivity of the total network impedance to the variable impedance—for any one of these trimming networks can be defined as:

$$S(Z_T, Z_v) = \left(\frac{Z_v}{Z_T} \right) \left(\frac{dZ_T}{dZ_v} \right)$$

where Z_v is the actual value of the variable impedance, and Z_T is the total network impedance. For the network of Fig. 1a, the sensitivity function becomes:

$$S(R_T, R_v) = (R_v/R_F) / [1 + (R_v/R_F)]$$

This function reaches a maximum when R_v is adjusted to its highest value ($R_v = R_V$). Similarly, both the inductive and capacitive trimming networks of Fig. 1 are most sensitive when the variable component is at its maximum value.

On the other hand, the sensitivity function for the network of Fig. 2 reaches a maximum value at a specific setting of the variable impedance. The total impedance of this circuit can be written as:

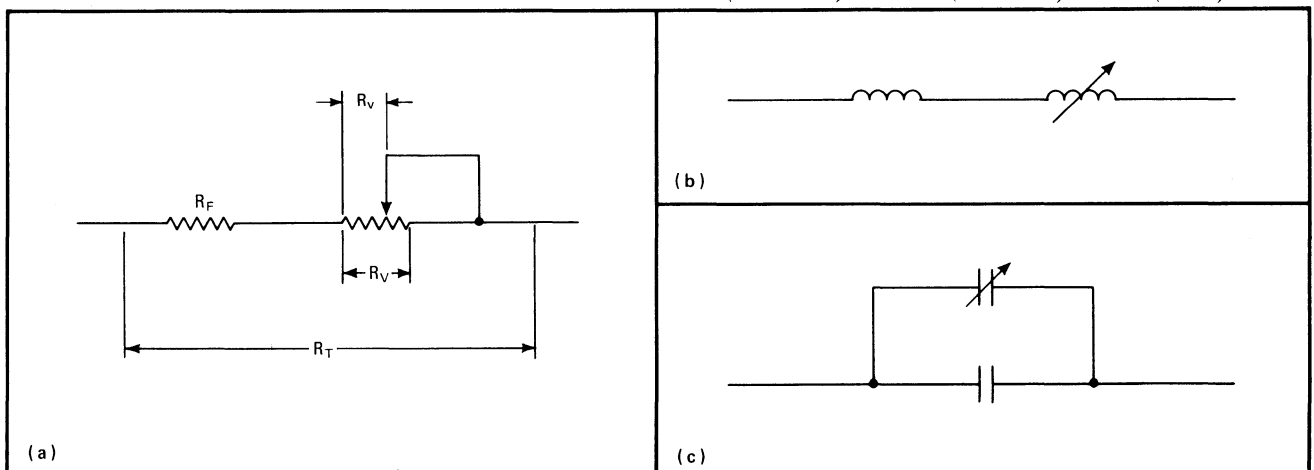
$$Z_T = Z_{F1} + \frac{Z_{F2}Z_v}{Z_{F2} + Z_v} = Z_{F1} + \frac{Z_{F2}}{k + 1}$$

where:

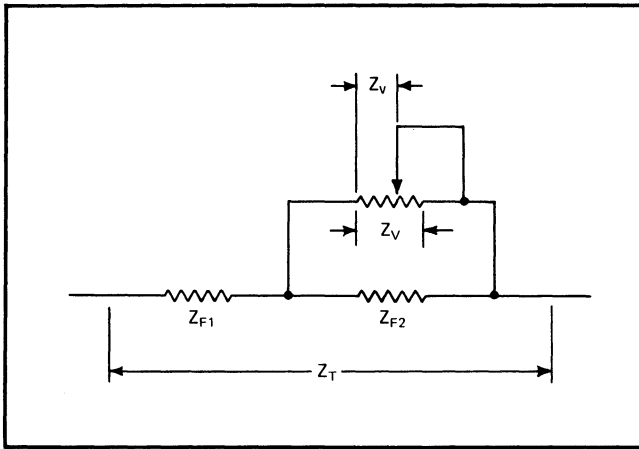
$$k = Z_{F2}/Z_v$$

Differentiating Z_T with respect to Z_v yields:

$$(dZ_T/dZ_v) = Z_{F2}^2 / (Z_{F2} + Z_v)^2 = k^2 / (k + 1)^2$$



1. Conventional configurations. These standard trimming networks are highly sensitive to the value of the variable resistor (a), inductor (b), or capacitor (c). The variable component, therefore, can be expensive if the network must provide reasonably good stability.



2. A better arrangement. Two fixed-value impedances, rather than just one as in the circuits of Fig. 1, reduce the sensitivity of this trimming network to the value of the variable impedance. Less-expensive less-stable adjustable components can then be used.

The sensitivity function can now be computed:

$$S(Z_T, Z_v) = [Z_v / (Z_{F1} + Z_{F2} / (k + 1))] [k^2 / (k + 1)^2]$$

which can be reduced to:

$$S(Z_T, Z_v) = k / [(k + 1) \{ (k + 1)(Z_{F1} / Z_{F2}) + 1 \}] \quad (1)$$

The maximum value of this sensitivity function can

be found by differentiating Eq. 1 and then equating the differential to zero:

$$Z_{F2} [1 + (Z_{F1} / Z_{F2}) - (Z_{F1} Z_{F2} / \hat{Z}_v^2)] = 0$$

where \$\hat{Z}_v\$ is the value of variable impedance that maximizes the sensitivity. The equation can be rewritten as:

$$Z_{F1} + Z_{F2} - Z_{F1} \hat{k}^2 = 0$$

where \$\hat{k}\$ is the value of impedance ratio that maximizes the sensitivity. This equation becomes:

$$Z_{F2} / Z_{F1} = \hat{k}^2 - 1 \quad (2)$$

Substituting for \$Z_{F2} / Z_{F1}\$ in Eq. 1 yields an expression for the maximum sensitivity:

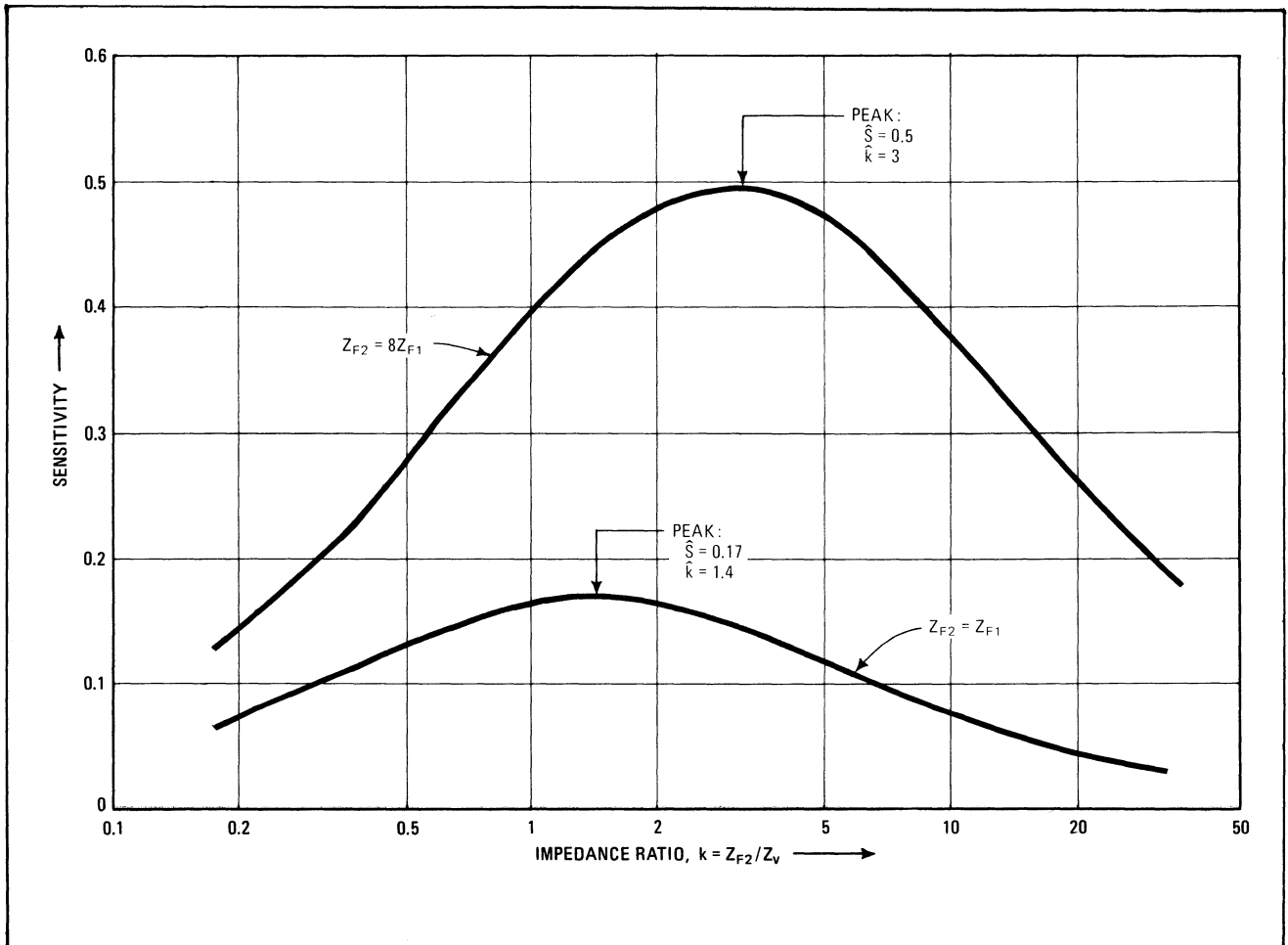
$$\hat{S}(Z_T, Z_v) = (\hat{k} - 1) / (\hat{k} + 1) \quad (3)$$

or:

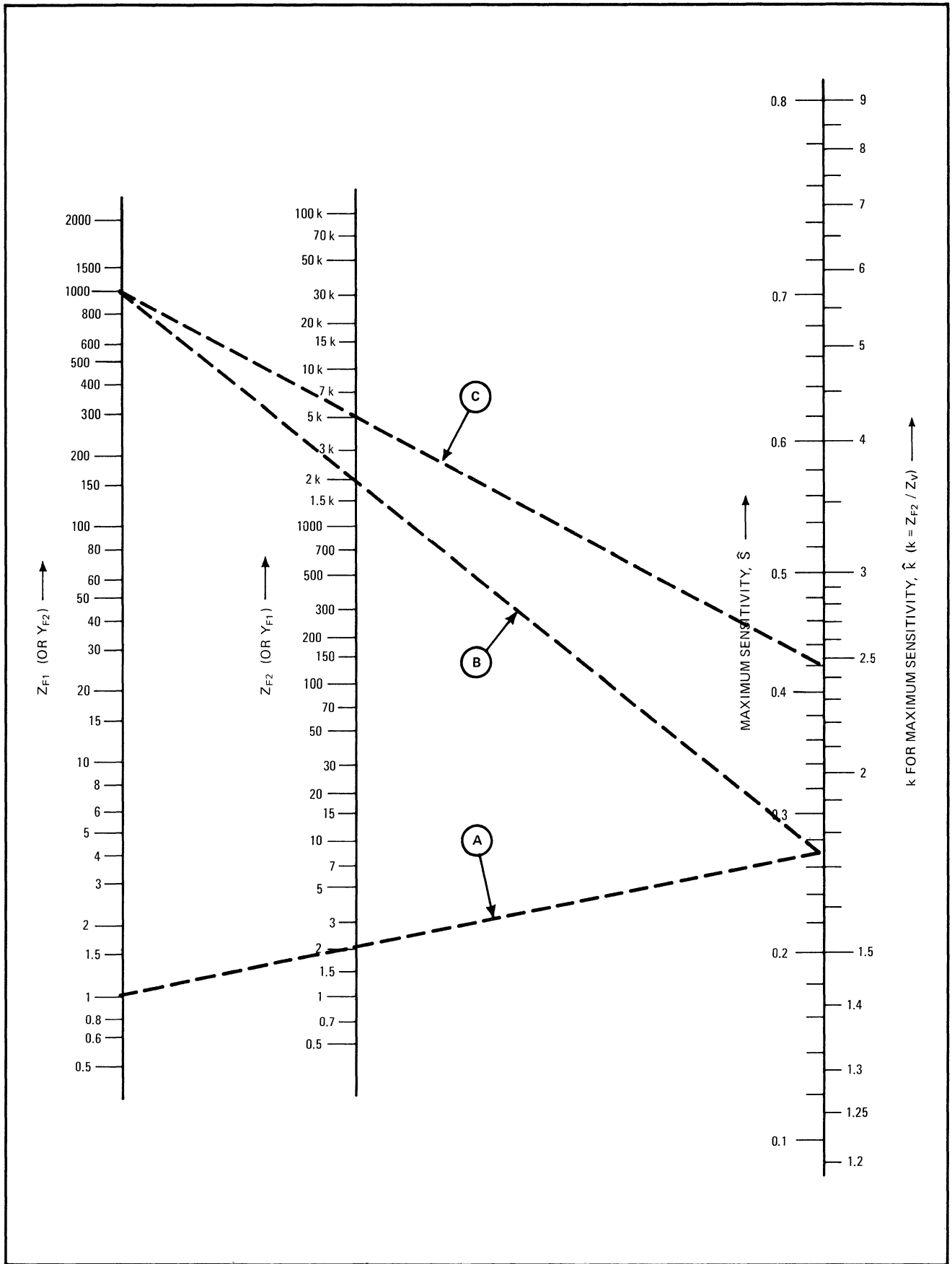
$$\hat{S}(Z_T, Z_v) = 1 - 2 / [1 + Z_{F2} / Z_{F1}]^{1-2} + 1]$$

Figure 3 shows how the sensitivity function varies with impedance ratio \$k\$ for two different ratios of fixed impedances \$Z_{F1}\$ and \$Z_{F2}\$. The upper curve is for a fixed impedance ratio (\$Z_{F1} / Z_{F2}\$) of 1:8 and the lower curve for a ratio of 1:1.

The two fixed impedance values can be chosen so that the sensitivity does not exceed a desired value. Solving for \$\hat{k}\$ in Eq. 3 gives:



3. A look at sensitivity. Variation of the sensitivity function of the network of Fig. 2 is plotted for two different ratios of the fixed impedances, \$Z_{F1}\$ and \$Z_{F2}\$. The peak value of sensitivity, \$\hat{S}\$, occurs at impedance ratio \$\hat{k}\$, which is not necessarily the maximum value of impedance ratio \$k\$.



4. Design aid. Nomograph helps to determine the fixed-component values needed to limit the maximum sensitivity of the improved network. The value of impedance ratio \hat{k} can also be read from the same right-hand axis. The left-hand and center axes can be used for impedances (resistors and inductors) or admittances (capacitors). Units for values must be consistent within the same determination.

$$\hat{k} = (1 + \hat{S}) / (1 - \hat{S})$$

where \hat{S} is the maximum value of $S(Z_T, Z_V)$. Substituting this result into Eq. 2 yields:

$$Z_{F2}/Z_{F1} = 4\hat{S}/(1 - \hat{S})^2$$

which determines the ratio of fixed impedances needed to limit sensitivity to the desired value.

Comparing sensitivities

Since the variation of sensitivity with impedance ratio k is fairly flat at peak value \hat{S} over a wide range of k , the maximum value of sensitivity is a good figure of merit for comparing the various trimming networks. (The network that provides the smallest maximum sensitivity is the most desirable.)

To compare the networks of Fig. 1 with the network of Fig. 2, the trimming range must first be computed. For the resistive network of Fig. 1a:

$$R_{Tmax}/R_{Tmin} = (R_F + R_V)/R_F = 1 + (R_V/R_F) \quad (4)$$

and the maximum sensitivity is:

$$\hat{S}_R = R_V/(R_F + R_V) = (R_V/R_F)/[1 + (R_V/R_F)] \quad (5)$$

For the impedance network of Fig. 2:

$$\frac{Z_{Tmax}}{Z_{Tmin}} = Z_{F1} + \frac{Z_{F2}Z_V/(Z_{F2} + Z_V)}{Z_{F1}}$$

or:

$$\frac{Z_{Tmax}}{Z_{Tmin}} = 1 + \frac{Z_{F2}}{Z_{F1}} \left[\frac{1}{(1+n)} \right] \quad (6)$$

where:

$$n = Z_{F2}/Z_V = k_{min}$$

which is less than 1 for most practical cases. For equal ranges, Eqs. 4 and 6 are equal:

$$R_V/R_F = (Z_{F2}/Z_{F1})[1/(1+n)]$$

Substituting for Z_{F2}/Z_{F1} (Eq. 2) yields:

$$R_V/R_F = (\hat{k}^2 - 1)/(1+n)$$

Maximum sensitivity \hat{S}_R (Eq. 5) can now be expressed in terms of the impedance ratio, \hat{k} :

$$S_R = \frac{(\hat{k}^2 - 1)}{(\hat{k}^2 - 1) + (1+n)} = \frac{(\hat{k} - 1)(\hat{k} + 1)}{\hat{k}^2 + n}$$

Dividing this last equation by Eq. 3 gives the ratio of the maximum sensitivity of the resistive network (\hat{S}_R) to that of the impedance network (\hat{S}_Z):

$$\frac{\hat{S}_R}{\hat{S}_Z} = \frac{(\hat{k} + 1)^2}{(\hat{k}^2 + n)} = 1 + \frac{2\hat{k} + 1 - n}{\hat{k}^2 + n}$$

Since \hat{k} is usually greater than 1 and n is usually less than 1, then:

$$(2\hat{k} + 1) \text{ is greater than } n$$

and:

$$\hat{S}_R/\hat{S}_Z \text{ is greater than } 1$$

This means that the maximum sensitivity of the resistive trimming network is generally larger than that of the impedance network, making the circuit of Fig. 2 the better design choice. For example, suppose $Z_{F2} = 2Z_{F1}$ and $Z_V = 2Z_{F2}$, then $\hat{k} = 1.732$ and $n = 0.5$, and $\hat{S}_R = 2.13\hat{S}_Z$, indicating that the sensitivity of the impedance

network is twice as good as that of the resistive network.

The same sensitivity comparison can be made between the inductive network of Fig. 1b and the network of Fig. 2; it will produce identical results. Similarly, an analysis for the capacitive network of Fig. 1c gives a sensitivity ratio of:

$$\hat{S}_C/\hat{S}_Z = 1 + (2k + 1 - m)/(\hat{k}^2 + m)$$

where \hat{S}_C is the maximum sensitivity of the capacitive network and m represents an admittance factor for the network of Fig. 2:

$$m = (Y_{F1} + Y_{F2})/Y_V$$

Since this factor is usually less than 1, maximum sensitivity \hat{S}_C is almost always greater than maximum sensitivity \hat{S}_Z .

Selecting component values

The nomograph of Fig. 4 provides a convenient method of determining \hat{S}_Z and \hat{k} from the values of fixed impedances Z_{F1} and Z_{F2} (or fixed admittances Y_{F1} and Y_{F2}). And, of course, the nomograph can also be used to determine Z_{F2} , given \hat{S}_Z and Z_{F1} . The units employed for the component values of the left-hand and center axes must be the same for each determination; the units may be ohms, kilohms, microhenries, picofarads, etc.

If the impedance (resistance or inductance) values of Z_{F1} and Z_{F2} are known, align a straight-edge to intersect the value of Z_{F1} on the left-hand axis, and the value of Z_{F2} on the center axis. At the intersection of the straight-edge with the right-hand axis, read the value of \hat{k} to the right of the right-hand axis and the value of \hat{S} to the left of the right-hand axis.

In the same way, if the admittance (capacitance) values of Y_{F1} and Y_{F2} are known, use a straight-edge to intersect the value of Y_{F2} on the left-hand axis, and the value of Y_{F1} on the center axis. Then the values of \hat{k} and \hat{S} can be read at the intersection of the straight-edge with the right-hand axis.

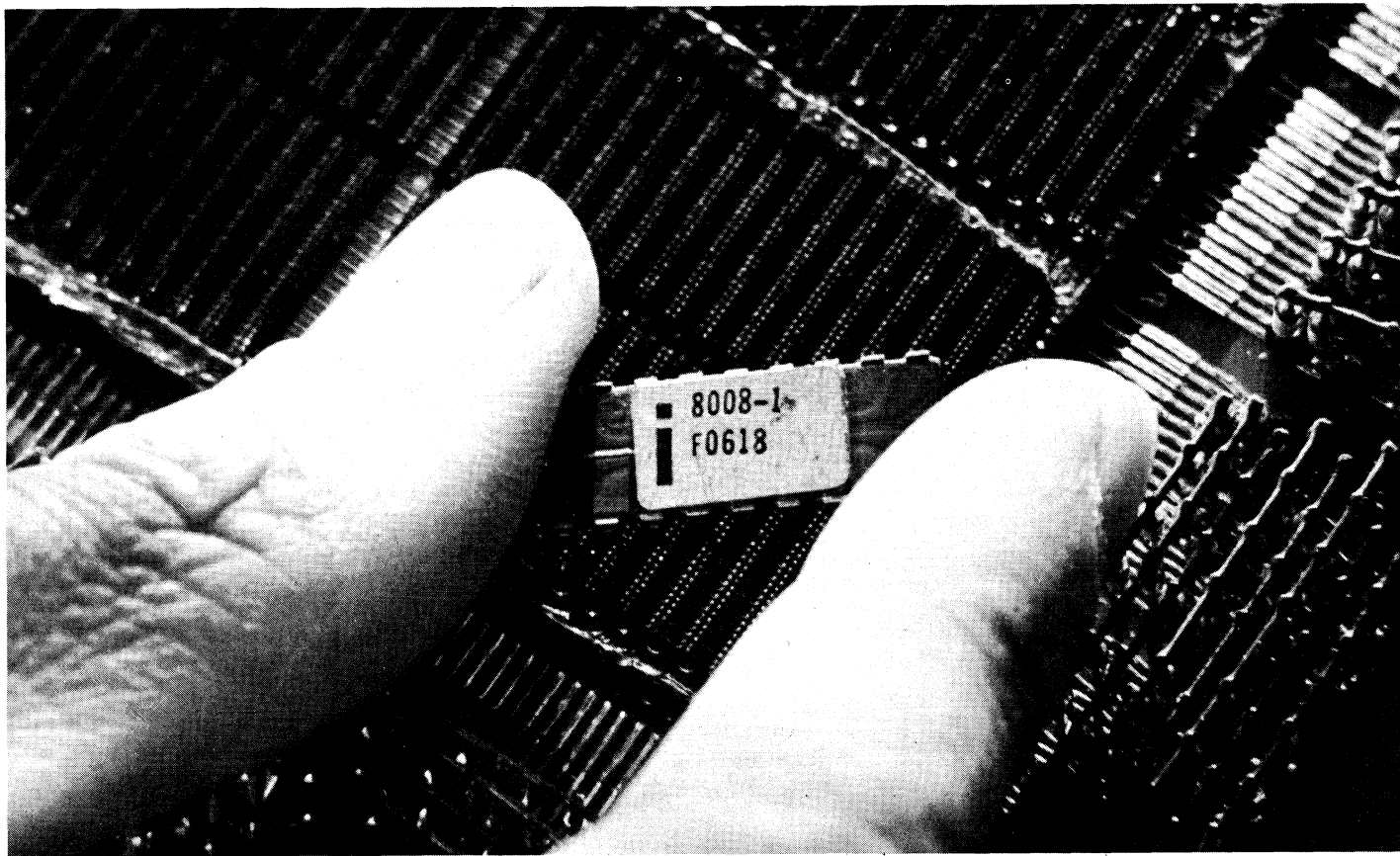
For instance, when $Z_{F1} = 1 \text{ kilohm}$ and $Z_{F2} = 2 \text{ kilohms}$, the lower dashed color line (A) may be drawn, intersecting the right-hand axis at $\hat{S} = 0.268$ and $\hat{k} = 1.732$. The same result can be obtained with the middle dashed color line (B) if the axes are considered to be scaled in ohms. For the upper dashed color line (C), aligning $Z_{F1} = 1 \text{ kilohm}$ with $Z_{F2} = 5 \text{ kilohms}$ produces an intersection at $\hat{S} = 0.420$ and $\hat{k} = 2.45$.

Occasionally, the value of \hat{k} may fall outside the available range of k . For the case of resistors and inductors, this situation can occur if the largest possible variable impedance, Z_V , is less than the value of Z_V needed to produce \hat{k} . For a capacitive network, this will occur if Y_V is less than the value of Y_V corresponding to \hat{k} . If such is the case, the nomograph should not be used. Instead, the value of the maximum sensitivity is found by substituting $k = Z_{F2}/Z_V$ in Eq. 1:

$$S(Z_T, Z_V)_{max} = Z_{F2}Z_P/[Z_{F1}(Z_{F2} + Z_V)]$$

where Z_P is Z_{F1} , Z_{F2} , and Z_V in parallel.

Moreover, besides improving the sensitivity function, this modified trimming arrangement increases resolution during trimming, which permits a further reduction in the cost of the variable component. □



Designing with microprocessors instead of wired logic asks more of designers

When engineers accustomed to hardware logic gates tackle a job with the new microprocessors—as they're almost sure to do sooner or later—they'll need to know some of these programming techniques

by Bruce Gladstone, Varitel Inc., Sherman Oaks, Calif.

□ The microprocessors recently introduced by various semiconductor companies foreshadow wide changes in the design of many electronic products and systems. These miniature computers substitute programming for logic design—an alternative that seems to surface for all but tiny specialized systems and ultrahigh-speed systems. The primary advantage of microprocessors is the short design turnaround time they make possible.

But to realize this advantage, as well as the corollary advantages of easy field alterations and inexpensive customizing, the logic or system designer will need to use new tools—some of which may be unfamiliar to him. Thus, instead of gate networks, he will use masks, comparisons, and jumps; and instead of time delays, he will use circulating loops.

Basically a microprocessor is no more—and no less—than a full-fledged processing unit essentially like the processor at the center of any computer system of any size. It has three major differences from a conventional processor: it is fabricated entirely as one integrated circuit or as a small number of such circuits; it is relatively slow, compared to most minicomputers, partly to enable its fabrication as an IC; and it sells for \$300 or less. Required with the microprocessor in any working system are a read-write memory for data, another memory—possibly read/write but usually read-only—for a program, and circuits for obtaining access to limited-performance input/output gear. Generally, these periph-

eral circuits, each on its own IC, are used in larger quantities than the microprocessors, so that the working system fills up one or more good-sized printed-circuit boards.

When a designer uses a microprocessor instead of hard-wired logic, he determines the system functions by a program—a sequence of instructions—stored in a memory. If he uses a read-only memory, the program is immune to inadvertent alteration. Replacing the program can completely alter the function of the machine that contains the microprocessor.

Using a genuine read-only memory, of course, would run counter to the flexibility advantages of using a microprocessor, except in large-volume applications. But using a programmable read-only memory, or better yet, a reprogrammable read-only memory, allows an

existing system to be altered quickly—in a matter of hours. As a result, a manufacturer can become much more responsive to his market.

Microprocessor characteristics

The most significant characteristics of today's microprocessors (not counting calculator sets and serial processors) are their speed, addressing modes, interrupt capabilities, and the number of internal registers. These and other characteristics are summarized in the table on this page.

The value of speed, in those applications that require it, is obvious. (Some techniques for speeding up the slower microprocessors are described later.) The more addressing modes and the more internal registers that are present in the microprocessors, the less external

TABLE 1. MICROPROCESSOR CHARACTERISTICS

| | Intel MCS-4 | Rockwell PPS | Intel MCS-8 | Intel 8080 | Signetics PIP | National GPC/P | AMI 7300 | |
|---------------------------------|--|--|--|--|--|--|--|-------------------------|
| Word size (bits) | 4 | 4 | 8 | 8 | 8 | 4-16 | 8 | |
| Instruction time (microseconds) | 10.8 – 21.6 | 5 – 10 | 7.5–22.5 12–44 (Note 1) | 2–6 | <5 – <10 | 3.3 – 9.6 | 4–32 (Note 2) | |
| Memory size | Pgm | 4,096 bytes | 16,384 bytes | 16,384 bytes | 65,536 bytes | 8,192 bytes | 65,536 bytes | 4,096 words (Note 4) |
| | Data | 1280 nibbles (Note 3) | 8,192 nibbles (Note 3) | | | | | 65,536 bytes |
| No. of instructions | 45 | 54 | 48 | 48+ | 64 | Micro-program | Micro-program | |
| Interrupt capability | Reset to 0 only | None | 1-level vector to 8 locations | Multi-level vector to 8 locations | 1-level stack to store machine state | 1-level stack to store machine state (Note 5) | 3-level | |
| Address modes | Pointer Indirect Immediate Register | Pointer Immediate | Pointer Immediate Register | Pointer Immediate Register | Direct Indirect Relative Immediate Register Indexed | Direct Indirect Relative Immediate Register Indexed | Direct Indirect Relative Immediate Register Indexed | |
| Registers | 16 x 4 bits pc + 3 stack | 2 x 4 bits pc + 2 stack 1 pointer | 5 x 8 bits pc + 7 stack 1 pointer | 5 x 8 bits pc + unlimited stack 1 pointer (Note 6) | 4 x 8 bits pc + 7 stack | 4 x 16 bits pc + 16 stack (Note 7) | 16 x 8 bits pc + 32 x 8 stack (Note 7) | |
| RAM & ROM | Special or standard (Note 8) | Special | Standard | Standard | Standard | Standard | Standard and special microprogram | |
| TTL chips | Clock only | None | 20–40 | Clock & buffers | 4–6 | 15–20 | Clock & buffers | |

- Notes:
- (1) 8008-1 instruction times are 0.6 x (8008 instruction times)
 - (2) Executes microinstructions from 512 x 22 microprogrammed ROM at 4 μs/microinstruction.
 - (3) One nibble = 4 bits = ½ byte
 - (4) Microprogram
 - (5) Conditional jump MUX external to chips allows 2-level interrupt very simply.
 - (6) Pc stack is stored in main memory and is accessible to programmer
 - (7) Stack is general-purpose to store pc, registers, and flags.
 - (8) 4008 & 4009 chips allow easy interface to standard RAM & ROM

memory capacity is likely to be required. The requirement for external memory is important because, in most systems, the memory cost dominates all other considerations. If the microprocessor can handle interrupts, it can perform more than one task at a time, and it can also do single tasks more quickly because it can overlap processing and input/output.

Many microprocessors, as indicated in the table, have a pointer-address mode. This permits a machine with a short word length to address a large memory array. And because such large arrays may require more bits in an address representation than can be contained in an instruction word, the address is kept in a special register or pair of registers preloaded by an instruction in the program. Subsequent instructions then refer to locations in the memory, which are addressed by the contents of the pointer register. However, the preloading instruction adds to the overhead in machine operation, reducing the over-all performance.

Some microprocessors also have immediate and indirect-address modes. These modes are to be distinguished from direct addressing—the simplest and most common. In any processor, an instruction word consists of an operation code (op code) and an operand code (that which is to be operated upon). When the operand code is a direct address, the processor executes the instruction on data in the location specified by that address (Fig. 1). When the operand code is an immediate address, the processor executes the instruction on the operand code itself. And when the operand code is an indirect address, the processor executes the instruction on data found at the address specified by the operand.

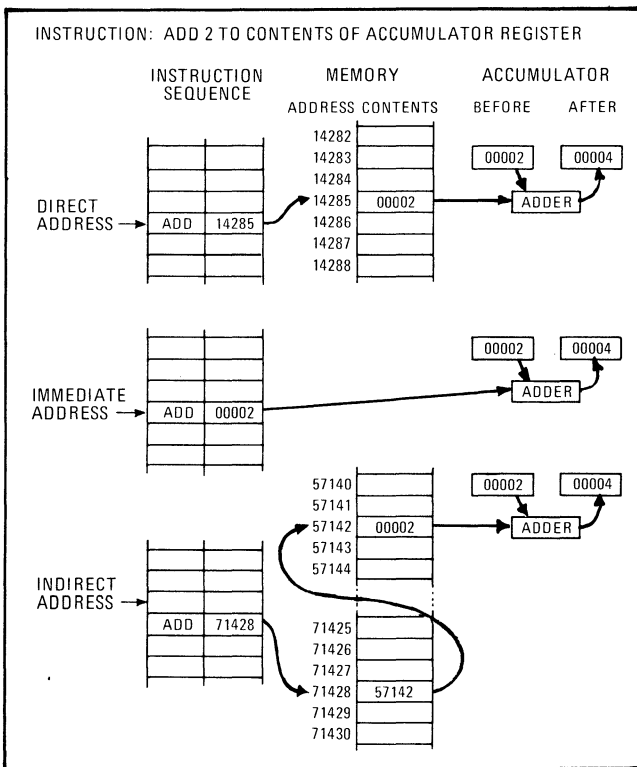
Indirect addressing and pointer addressing are similar, except that the address pointer is in an internal register instead of in a main-memory location. The particular mode of address is identified by the op code itself or by a flag bit associated with the op code.

Indirect addressing is a powerful tool in all software systems. It's particularly powerful in minicomputers, where the limited word length prevents direct access to more than a small part of the memory, and for the same reason, it can be equally powerful in microprocessors.

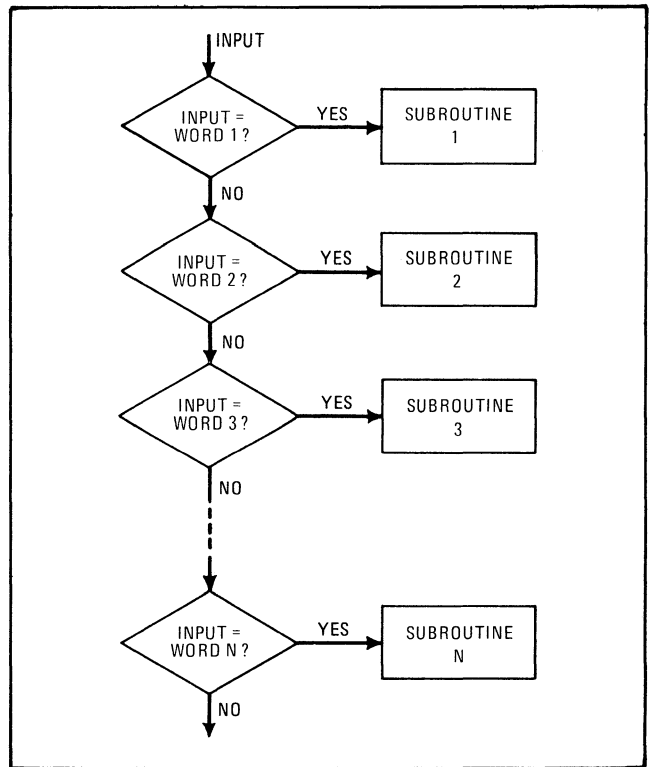
Some microprocessors are microprogrammed—that is, their control sequences are stored in read-only memories in the same way as object programs, which determine each machine's function. These microprograms are functionally similar to those used in large machines and minicomputers, in which, during the last few years, they have largely replaced hard-wired control.

Available software is an important aspects of the use of microprocessors. Writing a program in machine language (directly in binary notation) is—like walking from Portland, Maine, to Portland, Ore.—not impossible, but exceedingly difficult. At the very least, an assembler or cross-assembler is necessary to convert a program written in a symbolic language into machine language. Even new assemblers are written in symbolic notation.

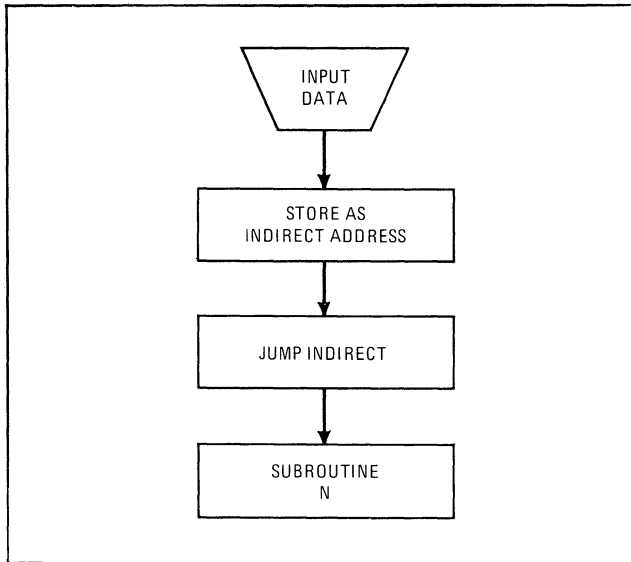
An assembler is executed on the same machine that is to run the object program; a cross-assembler would be executed on a different machine—most likely a mini-computer—but would produce a machine-language program that is executable on the microprocessor. Simulators, debuggers, and canned subroutines are other desirable software packages. Here, a microprogrammed



1. Address modes. Three ways of addressing memory are in common use, and some microprocessors use all three. Direct mode is the simplest, immediate is handy when working with constants, and indirect often simplifies the handling of subroutines.



2. Sequential test. An external signal can be identified and used to trigger an internal routine by comparing it successively with several test words. A match causes a program jump out of comparing sequence to a subroutine that processes the external signal.

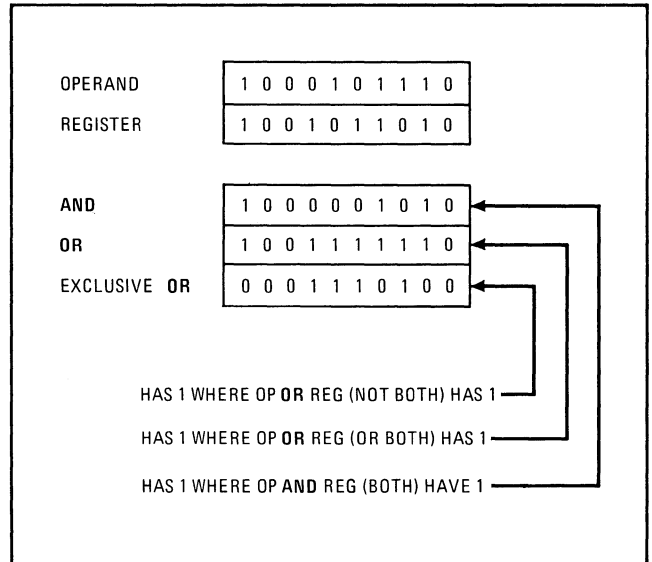


3. Indirect jump. To simplify the task of locating a subroutine, sometimes an incoming signal can itself identify the location, and the program jumps indirectly to the subroutine via the input buffer.

microprocessor has a distinct advantage—because the microprogram can be recast to make one machine emulate another, the microprocessor may be able to utilize existing software at minimal cost.

Design tools

Logic designers are accustomed to using a number of standard tools, including gate networks, time delays, counters, and discrete input/output controls. Each of these has its counterpart in a microprocessor program, but applying the programmed counterparts by rote may yield an uneconomical solution to a design problem.



4. Logic operations. These instructions can be used to mask certain unwanted bits in a register or to generate signals that are to be sent outside the microprocessor.

However, careful analysis of requirements and knowledge of microprocessor programing techniques will simplify design of an optimum system.

For example, programed logic is time-shared—it works only when the program reaches a particular point in its execution. But gate networks are always available; when the correct combination of inputs appears, they generate outputs, whether the rest of the system is ready for them or not.

Gate networks consist of ANDs, ORs, and NOTs; their inputs combine in the way determined by the combination of logic blocks to produce either an output from the

Features of microprocessors

Two widely used microprocessors are the Intel 4-bit MCS-4 and 8-bit MCS-8 chip sets, which can be put together in various combinations to produce systems of different capabilities.^{2,3} The processor chips in these two sets are, respectively, the 4004 and the 8008, for which several program routines are listed in this article. To make these routines more intelligible, brief functional descriptions of these two chips follow.

The Intel 4004 contains five functional sections: an address register and stack with an address-incrementing circuit, a set of 16 4-bit registers for indexing and general-purpose temporary storage, a 4-bit arithmetic and logic unit, an 8-bit instruction register and decoder, and peripheral circuitry.

The 16-bit registers and the instruction register are the most important sections in the present context. The index registers can be used either singly for temporary storage during computations, or in pairs to address memory and to store data fetched from the read-only memory.

The 8-bit instruction register can hold at any one time a 4-bit operation code and a 4-bit operand. Some instructions in the 4004 are of double length (16 bits instead of 8), have multiple operands, and are stored in successive read-only memory locations; they take two system cycles for execution instead of one.

The 4004 has a total of 45 instructions in its repertoire, plus a no-operation dummy instruction that uses up one instruction cycle but doesn't do anything. The 4-bit operand code in an instruction can specify, among other things, one of the 16 individual registers, or, with 3 bits, one of the eight register pairs. The upper end (most significant bits) of the register pair is the same as one of the even-numbered individual registers.

The Intel 8008 contains four functional sections: an instruction register, a local memory, an arithmetic-logic unit, and input/output buffers. The arithmetic-logic unit includes four control flip-flops—carry, zero, sign, and parity—which indicate conditions that arise during each instruction execution and are the basis for executing subsequent conditional jumps.

Part of the local memory consists of seven 8-bit registers. Of these, one, designated A, is the accumulator, which contains one of the operands and the result of every arithmetic operation. Four others, registers B, C, D, and E, may be used for any temporary storage, while the remaining two, registers H and L, contain respectively the high- and low-order bits of an indirect address in external memory. (Because external memory is limited to 16,384 words, addressed by 14 bits, register H in this application contains only 6 bits.)

processor itself or an alteration in the execution of the program. These functions are executed in a microprocessor by three basic operators—MASK, COMPARE, and JUMP. (A specific microprocessor may not have these particular instructions, but it should be able to execute their equivalent in some form.) The MASK excludes from subsequent operations any bits in an operand that are unwanted or are optional or “don’t-care” bits, the COMPARE matches the operand against another bit pattern, and the JUMP transfers the sequence of instructions being executed in the program to one that will perform the desired action as a result of the COMPARE operation.

Instructions are ordinarily executed directly in sequence, as they occur in the program; this sequential operation continues undisturbed if, for example, the match attempted in a COMPARE is unsuccessful. But if the match succeeds, the operation executed after the JUMP (second operation after the COMPARE) is not the one immediately following the JUMP (Fig. 2). Here the microprocessor receives a signal from the outside world. This signal may be a pulse or level on a single wire, a series of pulses placed in order in a shift register to create a processor word, or a word received simultaneously in parallel on a group of wires.

This input, in whatever form, is compared successively with each of several previously stored words in the memory. Whenever any comparison shows that the input and a stored word are equal, the program, instead of executing the next comparison, jumps directly to a sub-routine stored elsewhere in the memory. The address of the beginning of this subroutine is the JUMP instruction’s operand. Although the diagram doesn’t show it, in many applications the subroutine would return to

the next comparison at its completion.

In an alternative procedure (Fig. 3), the input signal, whatever its nature, causes an indirect jump to the proper subroutine. The input signal loads an address in a particular location in the memory, which is not the location of the JUMP instruction. Then, following a successful comparison, the program jumps indirectly to the subroutine via this intermediate location.

Logic operators

In some microprocessors, pure logic operators, corresponding to the gate functions of hardware logic, are available. These operators, usually the AND, OR, and exclusive-OR functions, are convenient to generate signals to be sent out from the microprocessor in response to incoming signals. (These functions are not to be confused with the AND, OR, and NOT of hardware logic.) In a program, the AND operator is the most straightforward way to perform the MASK function.

Logic operators retain 1 bits in a specified register where called for by logic 1 bits in the operand (Fig. 4)—in both the register and the operand for an AND, in either that register or the operand, or both, for an OR, and in either that register or the operand, but not both, for an exclusive-OR.

Not all microprocessors have all three of these logic operators in their instruction sets, but the designer will

TABLE 2. JUMP INDIRECT ROUTINE
(INTEL 4004 CODING)

| Mnemonic | Operand | Action |
|----------|---------|---|
| FIM | 1P 2 | FETCH IMMEDIATE, A TWO-WORD INSTRUCTION; TRANSFERS CONTENTS OF 2ND WORD TO REGISTER PAIR SPECIFIED BY OPERAND IN FIRST WORD. (P IN AN OPERAND DESIGNATES A REGISTER PAIR.) HERE REGISTER PAIR 1 IS LOADED WITH THE NUMBER 2 -- AN ARBITRARY NUMBER THAT DEPENDS ON PREVIOUS ACTIONS IN A PROGRAM OF WHICH THIS ROUTINE IS A PART. |
| SRC | 1P | SEND REGISTER CONTROL; ADDRESSES THE READ-ONLY OR READ-WRITE MEMORY WITH THE CONTENTS OF THE REGISTER PAIR SPECIFIED. HERE PAIR 1 IS SPECIFIED; SINCE PAIR 1 WAS PREVIOUSLY LOADED WITH THE NUMBER 2, MEMORY LOCATION 2 IS CALLED FOR. |
| RDR | | READ DATA FROM THE SELECTED MEMORY LOCATION INTO THE ACCUMULATOR. |
| XCH | 4 | EXCHANGE THE CONTENTS OF THE ACCUMULATOR AND THE INDEX REGISTER SPECIFIED. HERE REGISTER 4 IS SPECIFIED; IT IS THE UPPER HALF OF PAIR 2. THUS WHATEVER WAS READ FROM MEMORY IS NOW IN REGISTER 4. |
| JIN | 2P | JUMP INDIRECT TO THE ADDRESS CONTAINED IN REGISTER PAIR SPECIFIED -- HERE PAIR 2. PAIR 2 COMPRISES REGISTERS 4 AND 5; SINCE REGISTER 4 CONTAINS A NUMBER BROUGHT FROM MEMORY, AND REGISTER 5 IS EMPTY, PAIR 2 CONTAINS A MULTIPLE OF 16. THE JUMP IS TO THE BEGINNING OF A 16-WORD SUBROUTINE. |

TABLE 3. LOOPING ROUTINE — MULTIPLE WORD TEST
(INTEL 8008 CODING)

| Mnemonic | Operand | Action |
|----------|---------|--|
| LCI | | LOAD REGISTER IMMEDIATE (2 WORDS). HERE DATA FROM THE 2ND WORD OF INSTRUCTION IS PLACED IN REGISTER C. |
| LLI | | THE SAME; REGISTER L. |
| LHI | | THE SAME; REGISTER H. |
| INP | | READ DATA SUPPLIED BY INPUT DEVICE 1 INTO ACCUMULATOR (REGISTER A). |
| NDM | | FORM LOGIC "AND" OF MEMORY LOCATION SPECIFIED BY CONTENTS OF REGISTERS H&L WITH ACCUMULATOR. |
| INL | | INCREMENT REGISTER L, TO SPECIFY LOCATION OF TEST WORD. |
| CPM | | COMPARE CONTENTS OF MEMORY LOCATION SPECIFIED BY H&L WITH THE ACCUMULATOR; IF THEY ARE EQUAL, SET THE ZERO CONDITION FLIP-FLOP. |
| JTZ | MATCH | CONDITIONAL JUMP, A 3-WORD INSTRUCTION; JUMP TO INSTRUCTION (SYMBOLIC ADDRESS "MATCH") SPECIFIED BY 2ND AND 3RD WORDS OF THIS INSTRUCTION IF THE ZERO FLIP-FLOP IS ON. |
| DCC | | DECREMENT REGISTER C; IF RESULT IS ZERO, SET THE ZERO FLIP-FLOP. |
| JTZ | NMATCH | CONDITIONAL JUMP TO THE FIRST INSTRUCTION (SYMBOLIC ADDRESS "NMATCH") OF NEXT ROUTINE. |
| INL | | INCREMENT REGISTER L AGAIN. |
| JMP | *-12 | UNCONDITIONAL JUMP, A 3-WORD INSTRUCTION, TO THE ADDRESS SPECIFIED BY THE 2ND AND 3RD WORDS; * MEANS THIS INSTRUCTION AND *-12 MEANS THE INSTRUCTION 12 WORDS BACK -- THE "INP" INSTRUCTION. |

TABLE 4. LOOPING ROUTINE – TIME RELAY
(INTEL 4004 CODING)

| Mnemonic | Operand | Action |
|----------|---------|--|
| FIM | OP 12 | FETCH IMMEDIATE (2 WORDS). LOADS 2ND WORD OF INSTRUCTION -- 12 -- INTO REGISTER PAIR SPECIFIED -- PAIR 0. |
| ISZ | 0 * | INCREMENT AND SKIP IF ZERO (2 WORDS). INCREMENT CONTENTS OF REGISTER SPECIFIED IN OPERAND OF FIRST WORD, AND IF THE RESULT IS 0, EXECUTE THE NEXT INSTRUCTION IN SEQUENCE (SKIPPING 2ND WORD OF THIS INSTRUCTION). IF THE RESULT IS NOT 0, JUMP TO THE ADDRESS SPECIFIED IN THE 2ND WORD. HERE THAT ADDRESS IS THIS INSTRUCTION'S OWN, INDICATED BY *, SO IT KEEPS JUMPING BACK TO ITSELF UNTIL REGISTER 0 AGAIN CONTAINS 0 -- 16 REPETITIONS. |
| ISZ | 1 *-2 | INCREMENT AND SKIP IF 0 (2 WORDS). THIS HAPPENS JUST ONCE BEFORE RETURNING TO THE PREVIOUS ISZ FOR 16 MORE REPEATS, AND FOUR TIMES BEFORE EXITING PERMANENTLY -- A TOTAL OF 64 STEPS IN THE DOUBLE LOOP. |
| BBL | 0 | BRANCH BACK AND LOAD; THE OPERAND IS PLACED IN THE ACCUMULATOR. THIS RETURNS TO THE ROUTINE DELAYED BY THIS DOUBLE LOOP; THE 0 OPERAND CLEARS THE ACCUMULATOR. |

soon find that at some cost in memory space and running time, almost any operator not explicitly included can be made up from available instructions. Because of this cost, implementing the gate functions is likely to be more economical in hardware outside the microprocessor than in the program, if their outputs are required externally. These functions pay off, however, if there is some regularity in the task they perform—for example, if one group of bits is to be compared to many test words.

In some microprocessors, this multiple comparison can be programmed very compactly. For example, in the Intel 4004, the contents of any memory location can be loaded into a general-purpose register, which is specified in a JUMP INDIRECT instruction. Thus, data can modify the flow of instructions, and a multiple branch is no more than a simple procedure of looking up numbers in a table.

The routine (Table 2) requires only five instructions occupying six words. Four instructions identify the memory location—in this case an input/output device—and they bring data from that location into the accumulator and then put it into an even-numbered register—one of 16 4-bit registers in the 4004 that can also be addressed as eight 8-bit register pairs. Each even-numbered register is the upper half of a register pair, so that loading anything into an even-numbered register and leaving 0s in the lower half is equivalent to loading a multiple of 16 into the register pair. The last instruction in the routine is the JUMP INDIRECT, which refers to the register pair for the address of its destination—the beginning of a 16-byte subroutine. A maximum of 16 such subroutines can be selected.

Programed AND-OR

Another very useful technique in microprocessor programming is the use of a routine that branches back to it-

TABLE 5. DISCRETE EXTERNAL CONTROLS – LAMP BANK
(INTEL 8008 CODING)

| Mnemonic | Operand | Action |
|----------|---------|---|
| LAC | | LOAD ACCUMULATOR WITH CONTENTS OF REGISTER C. |
| LLI | | LOAD REGISTER IMMEDIATE; 2ND WORD OF THIS INSTRUCTION TO REGISTER L. |
| LHI | | SAME; REGISTER H. L&H NOW CONTAIN THE ADDRESS OF THE LAMP-BANK IMAGE IN THE MEMORY. |
| ORM | | FORM LOGIC "OR" OF MEMORY LOCATION SPECIFIED BY REGISTERS H&L WITH THE ACCUMULATOR. LOCATION CONTAINS LAMP-BANK IMAGE. |
| NDD | | FORM LOGIC "AND" OF REGISTER D WITH THE ACCUMULATOR. |
| LMA | | MOVE CONTENTS OF ACCUMULATOR INTO MEMORY LOCATION M (SPECIFIED BY H&L). THIS IS THE NEW IMAGE OF THE LAMP-BANK. |
| LAI | 4 | LOAD ACCUMULATOR WITH CONTENTS OF 2ND WORD OF THIS INSTRUCTION -- THE NUMBER 4. |
| OUT | ADD | MOVE CONTENTS OF ACCUMULATOR TO OUTPUT CHANNEL, IDENTIFYING THE DEVICE FOR A SUBSEQUENT OUTPUT OPERATION. THE DEVICE IS THE LAMP-BANK. |
| LAM | | MOVE MEMORY LOCATION M INTO THE ACCUMULATOR. THIS BRINGS OUT THE NEW IMAGE OF THE LAMP-BANK AGAIN. |
| OUT | WR | MOVE CONTENTS OF ACCUMULATOR ONTO PREVIOUSLY SELECTED OUTPUT CHANNEL, THUS ALTERING THE CONDITION OF THE LAMP-BANK TO MATCH THE NEW IMAGE IN MEMORY LOCATION M. |

self in a continuous loop, together with a provision to count or otherwise limit the number of times the program executes the loop. (Without such a provision, the processor will continue executing the looped program indefinitely—chasing its tail, so to speak.)

The equivalent of an extensive hardware AND-OR network can be implemented with a looped program. Using the Intel 8008, the program (Table 3) can be written in 12 instructions occupying 21 words, only 15 of which are actually part of the loop.

First, the number of times the loop is to be executed is entered in one of the general-purpose registers; this corresponds to the number of AND gates in the hardware equivalent. Each pass through the loop brings an 8-bit word into the accumulator register, masks out any unwanted bits in that word, and compares it with a test word previously stored in the memory.

For each input word, the mask and the test word are stored in adjacent locations in the memory. Masks and tests for successive inputs are stored in successive pairs of locations. Thus, after specifying the number of passes through the loop, a pair of general-purpose registers is loaded with the address of the mask to be applied to the first input (one register can't hold a complete address). Then the program enters the loop for the first pass.

During each pass, the program fetches an input word, forms the logic AND of that word with the mask in memory, and compares the result with the test word next to the mask. If the two match, the program branches to a routine to process the input word. If the match is unsuccessful, the loop counter is decremented

by 1 and tested to find out if it now contains 0. If it does, the loop has been executed the prescribed number of times, and the program branches to another task; if not, the two pointer registers that track the masks and test words are incremented, and the program goes back to fetch another input word.

Looping is also the obvious way to generate time delays. For example, to program a delay with the Intel 4004, a four-instruction seven-word routine (Table 4) can be used. Initially, the number 12 is loaded into register pair 0, which then contains 0000 1100. (In fact, the number is in the single register 1, while register 0—the upper half of pair 0—contains four 0s.) A one-instruction loop then increments register 0 over and over again, testing the contents each time until the register again contains 0000—a total of 16 steps. Another single instruction then increments register 1 once and returns to the one-instruction loop, unless the increment has placed four 0s in register 1.

Because register 1 initially contains 12, it is incremented four times—each time preceded by 16 repetitions of the incrementing of register 0; therefore, a total of 64 incrementing steps are taken by these two instructions alone. Finally, when register 1 turns up with contents 0000, the program returns to the routine that has been waiting for the completion of this time-delay loop—perhaps to permit some mechanical operation to take place. As described here, the delay is slightly more than 1.5 milliseconds, but it can be set to any amount by changing the numbers loaded into the registers and fine-tuned to a certain extent by inserting dummy instructions (no-ops) in the routine. A no-op uses up one instruction cycle—10.8 microseconds in the 4004—but doesn't do anything.

Input-output images

In designing such logic systems as digital controllers, sensing discrete conditions and generating discrete outputs are important. The conditions include switch closures, status bits, and the like. Typical outputs perform such functions as lighting lamps and energizing relays, tasks that data-processing systems rarely perform.

Designing systems around microprocessors

Electronic lock illustrates power of chip set to handle complex operations; adding such capabilities as I/O controllers and interrupts can expand a system

Translating logic-gate networks into program sequences, as described in the previous section of this article, is the first step toward a microprocessor-based system—but only the first step. Program sequences must then be gathered into a completed design that will perform the desired function.

An example shows how to accomplish this conversion. The logic design¹ is an electronic lock—the buzzer type often used in apartment houses, banks, and other secure areas—with a sequential combination instead of a simple button. In its standby state, the lock is closed. To open it, a button is pressed, starting the sequence. After a short time delay—a few seconds—a light begins

A microprocessor controls and monitors these signals in a unique way—it maintains an image of them in its memory. For example, one 8-bit word can sense eight status lines, treating each input signal as new data to be read and stored in one bit position of the word. And by programmed bit manipulation, another word can control the lighting of eight lamps.

For instance, a program to light lamp No. 3 and extinguish lamp No. 4 in a bank of eight lamps can be written for the Intel 8008 with 10 instructions that occupy 13 words. The program (Table 5) assumes that one general-purpose register—say, register C—has previously been loaded with 0000 0100, which identifies lamp 3 (counting from the right) as the one to be turned on, while another register, D, contains 1111 0111 to point out lamp 4 as the one to be turned off; a location in memory contains an image of the bank of eight lamps, with their prior on-off status.

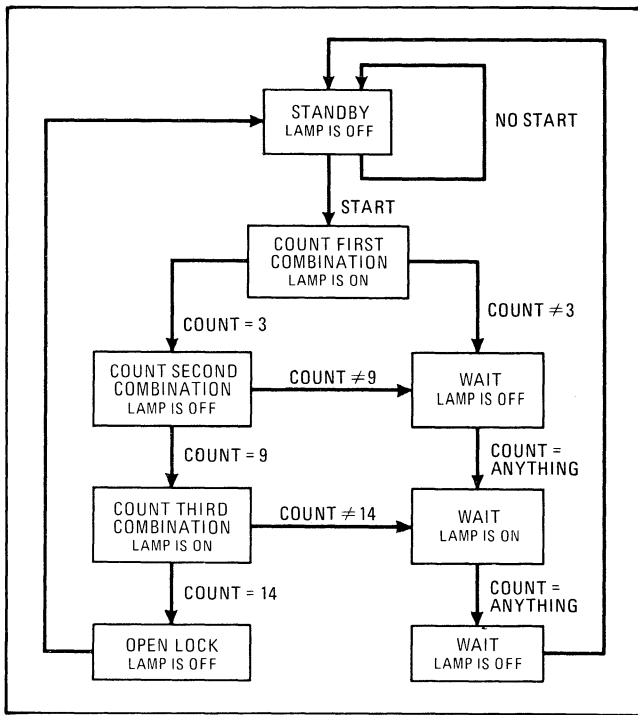
The contents of register C are first loaded into the accumulator, where the logic OR is formed with the image of the bank of lamps, and then the logic AND is formed with the contents of register D. The OR operation leaves a 1 in the accumulator for each lamp that should be on at the end of the routine; the AND leaves a 0 for all lamps that should be off. Because the accumulator contained only a single 1 bit before these two logic steps, only one lamp changes from 0 to 1; and since register D contains only one 0, only one lamp changes from 1 to 0.

Now the accumulator contains the updated image of the bank of lamps, which is stored back in the main memory temporarily, while the address of the actual bank is sent out through the output port. The image is then brought back into the accumulator and sent out after the address to switch the lamps.

Functions like these can be implemented with a small input/output card or subassembly containing two 8-bit registers. One of these, an input register, stores changes in external conditions that are to be sensed, and input commands transfer its contents, as required, into memory. Similarly, output commands transfer data into the other register, from which output signals can be generated as needed.

to flash on and off at a low frequency, several seconds for each half-cycle. During each half-cycle, the button must again be pressed a prescribed number of times. If the sequence is executed correctly, a signal energizes the lock and opens it one half-cycle later, and then the circuitry returns to its standby state, reclosing the lock. A mistake in the sequence returns the circuit to standby without opening the lock.

For a half-cycle time of 4 seconds and a combination of 3-6-5—the number of times the button is pressed during each half-cycle—the state diagram appears in Fig. 5. This diagram defines the successive states the sequential circuit must occupy, and it is the starting point for either



5. Electronic lock. Lock opens only when button has been pressed the correct number of times during three successive time periods. Its operation is described in this state diagram, which is the starting point for either a hardware or a programed design.

a hardware-logic design or a microprocessor program.

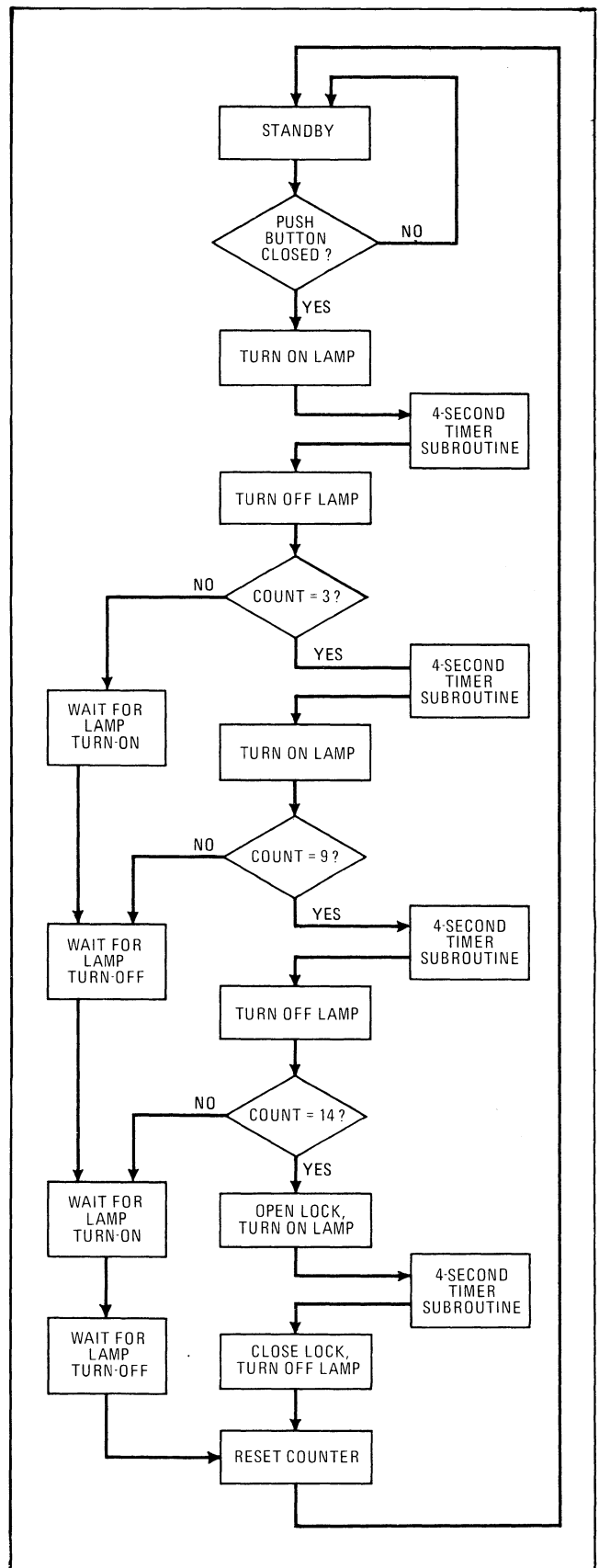
Because the diagram contains eight states, the sequential logic would require a minimum of three flip-flops, which together have eight combinations of on and off. The system control also would require input and output gates for these flip-flops, a four-stage binary counter, four more flip-flops, and a decoder, although all of these can be obtained as small- or medium-scale integrated circuits.

Another flip-flop or latch circuit is necessary to take the inevitable "bounce" out of the pushbutton contacts. Beyond these are a clock, which would be most easily made from an oscillator running at a kilohertz or so and another counter—more flip-flops—to divide the oscillator output down to the fractional-hertz level.

Finally, either the combination must be fixed when the lock circuit is put together, which calls for a rewiring job to change the combination, or additional complications—such as rotary switches on the protected side of the locked door—would have to be included in the design. (Driver circuits for the lamp and the electric lock are also required, but the microprocessor design will require them too.)

This list of parts that the electronic lock would require—nearly a dozen packages of small-scale and medium-scale integrated circuits—is intended to emphasize its complexity if it is designed with hardware logic. On the other hand, it is quite simple if programed for a microprocessor, which has its own counting capability.

In the Intel 8008 microprocessor, for example, the controller requires only an 85-byte program, for which a flow chart is shown in Fig. 6. The program can be stored in either an alterable or a read-only memory. In a ROM, at about 2 cents per byte, the incremental cost is \$1.70.



6. Counting signals. The sequence of events in the electronic lock is defined in this flow chart, which describes exactly what happens from the internal viewpoint, as opposed to the external view, of the state diagram. Blocks in the flow chart are readily translated into a program routine in any machine code or symbolic code.

Furthermore, the combination can be changed simply by reprogramming. The new program could be stored in a read-only memory, to be inserted in place of the old one, or in an alterable memory that is reloaded. In the same way, more complex combinations or additional functions can be added through programming.

Thus, new functions are inexpensive, once the basic cost of the microprocessor has been paid, and the hardware logic diagram shows why the microprocessor is so powerful. The most important parts of the electronic lock are the 16-line decoder and the gate elements that compare the decoder outputs with the previous state of the three sequential-logic flip-flops. But the bulk of the logic is in the counter itself, and the microprocessor can generate any counter sequence trivially—that is, the program itself is the counter.

Input/output controllers

To do anything useful, any processor, micro or otherwise, must have one or more input/output devices connected to it so that it can acquire data to process and it can dispose of the results. I/O devices may be as simple as lamps and switches or as complex as disk storage units, but for microprocessors, they fall generally into three distinct groups: serial-bit-stream devices, single-character devices, and block-transfer devices. The first class is not discussed further here because, for those devices, the microprocessor is its own I/O controller, but for the other two classes, external control logic is required.

Many designs for I/O systems are possible, and there are many tradeoffs between cost, speed, number of lines serviced, and so on. But all controllers share four common functions: buffering, address-recognition, command-decoding, and timing and control. All these functions can be included in a rather simple design.

Buffering is necessary in the path along which data is transferred in either direction between an I/O device and the microprocessor because the two units have separate clocks and therefore are not synchronized. Synchronizing, or equivalently controlling the I/O unit from the microprocessor clock, is not advisable because the connection between the two units may be lengthy and therefore subject to difficulties with noise and delays.

Address-recognition is necessary when (as is usually the case) more than one I/O unit is used with a microprocessor. Command-decoding is necessary for I/O devices that are capable of actions other than the transfer of data—for example, rewinding a tape drive. Finally, all of these functions require timing and control.

For a typical microprocessor system, the controller diagramed in Fig. 7 provides all four functions. It includes three buffer registers, which store input data, output data, and device status. A typical write sequence involves four steps:

First, the microprocessor sends out the address of the device in which it wants to write. This address travels along a common bus that also carries data, and serves the memory, as well as the I/O system. Therefore, the address is accompanied on separate lines by an address-command and an I/O request. The address-command identifies the signals on the bus as an address, and the I/O request directs it to the controllers instead of to the

memory. A synchronizing signal strobes the address into the selected controller and effectively establishes a temporary link between the separate clocks of the microprocessor and the controller at the moment the address is transferred.

Second, the addressed controller sets its address flip-flop, which generates a ready signal to the microprocessor. All the signals sent out by the microprocessor went to all the controllers, but the address identified only one of them. That controller, with ready signal, thus acknowledges receipt of the address command and indicates that it is in a condition to begin operation.

Third, the microprocessor sends out a write command and a word or block of data—again with an I/O request and a synchronizing pulse. Only the previously selected controller responds to these signals. The data goes to the controller's storage register, and it returns another ready signal. The data goes to the controller on the same lines as the address, but the write command identifies it as data instead of an address. This step may be repeated as many times as needed to complete the write operation, and between write steps, the controller forwards the data to the device it is operating.

Finally, the microprocessor sends out another address command to select a different controller. This resets the address flip-flop in the previously selected controller and takes it out of operation until it is again selected.

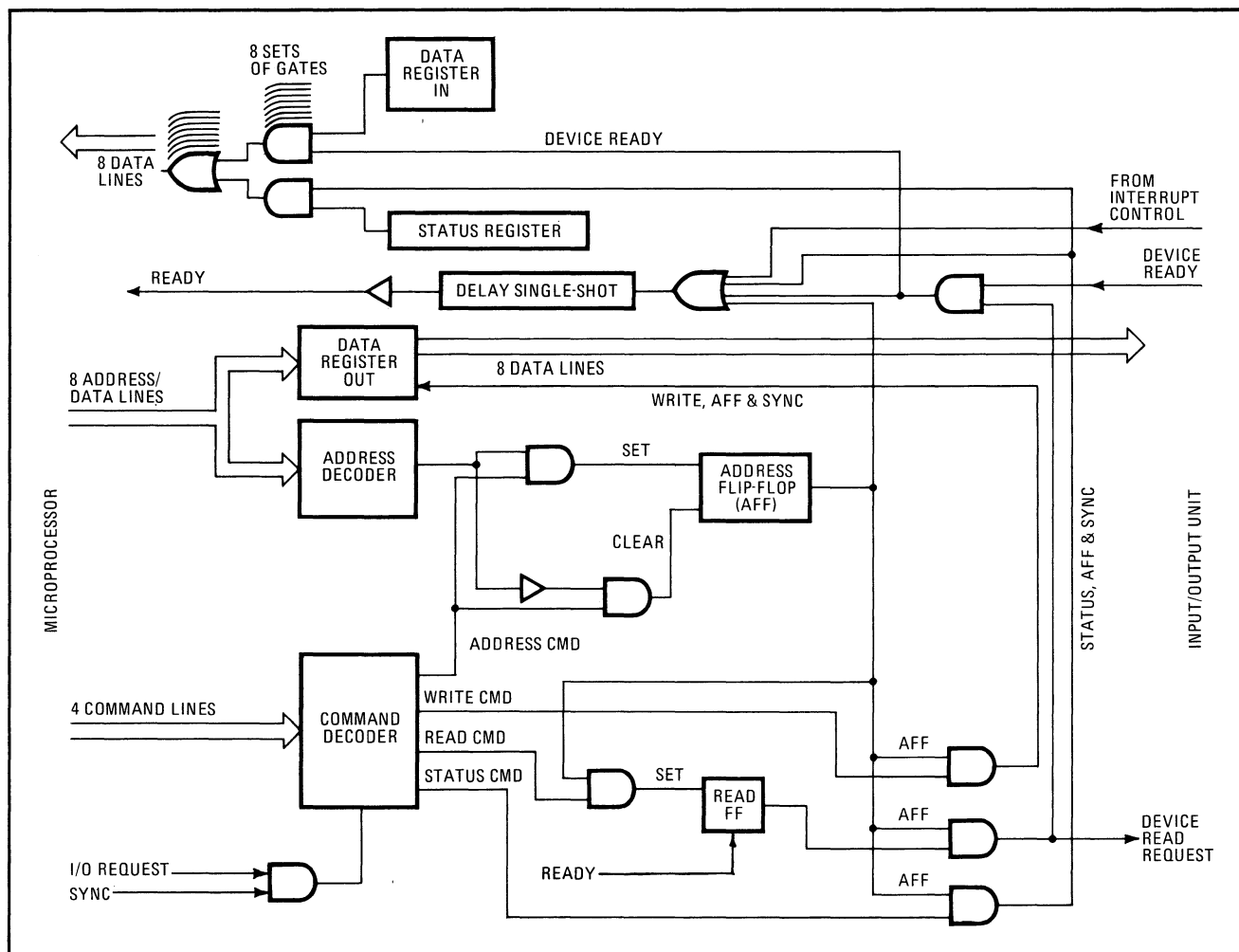
The first two steps of a read sequence are the same as those for write. But in the third step, the read command goes out, and the microprocessor waits for data to come back. The presence of data on the lines for the microprocessor to accept is announced by a ready signal. This cycle can be repeated as many times as needed—until a new controller is selected.

Generally, a read operation requires a delay while the mechanical device providing the data accelerates to its normal operating speed. The microprocessor can also request the controller to transfer its status information into the memory—an operation essentially identical to a read, except for the delay. The status is always immediately available in the controller, and finding it involves no mechanical processes.

Figure 7 shows the four commands—READ, WRITE, ADDRESS, and STATUS—as coming to the controller on four different lines. These could be encoded on two lines, or the four lines could be encoded with as many as 12 more commands if the I/O functions are to be expanded.

Interrupt

One such expansion might be the addition of interrupt capability to the system. In the example of the electronic combination lock, a loop at the start of the programmed sequence represents the standby state. While in this loop, the microprocessor effectively runs around in circles waiting for something to happen—for someone to push the button. Similar standby loops are often incorporated in programs, but if the events they wait for are infrequent—less than once every 50 instructions or every 100 to 1,000 microseconds—the microprocessor could be doing useful work while waiting for the external event. That event must be able to cause the microprocessor to change its course of action. This capability,



7. Input/output controller. This simple assembly provides all basic functions of any controller: buffering, address recognition, command decoding, timing, and control. These functions are required, regardless of its speed or how many lines it services.

available on some microprocessors, is called interrupt.

Interrupt is especially valuable in communications applications. Since the microprocessor often has no control over when data is to be transmitted or received, the capability to work while waiting is desirable.

Resolving an interrupt is a rather complicated procedure. First of all, once an interrupt has been recognized, the microprocessor can't afford to recognize any others until the first one is out of the way. (In large computers, interrupt priorities are sometimes installed so that a high-priority interrupt can bump a low-priority interrupt. Such complex design seems undesirable with microprocessors at present.)

Second, before the microprocessor can process an interrupt, it has to store its own state—that is, effectively to take note of where it was when it was interrupted so that it can pick up where it left off after the interrupt processing is finished. This involves transferring into a reserved part of the memory the instruction counter, which identifies the next instruction, the contents of the accumulator, and other key registers and flip-flops. The existence of only one such reserved area is the reason for recognizing only one interrupt at a time.

In general, the implementation of an interrupt system consists of replacing the wait loop in the program with an equivalent loop in hardware, which tests for the pres-

ence of an interrupt at regular intervals during machine operation. For example, the test might occur just before every instruction fetch so that the fetch is blocked if an interrupt has occurred.

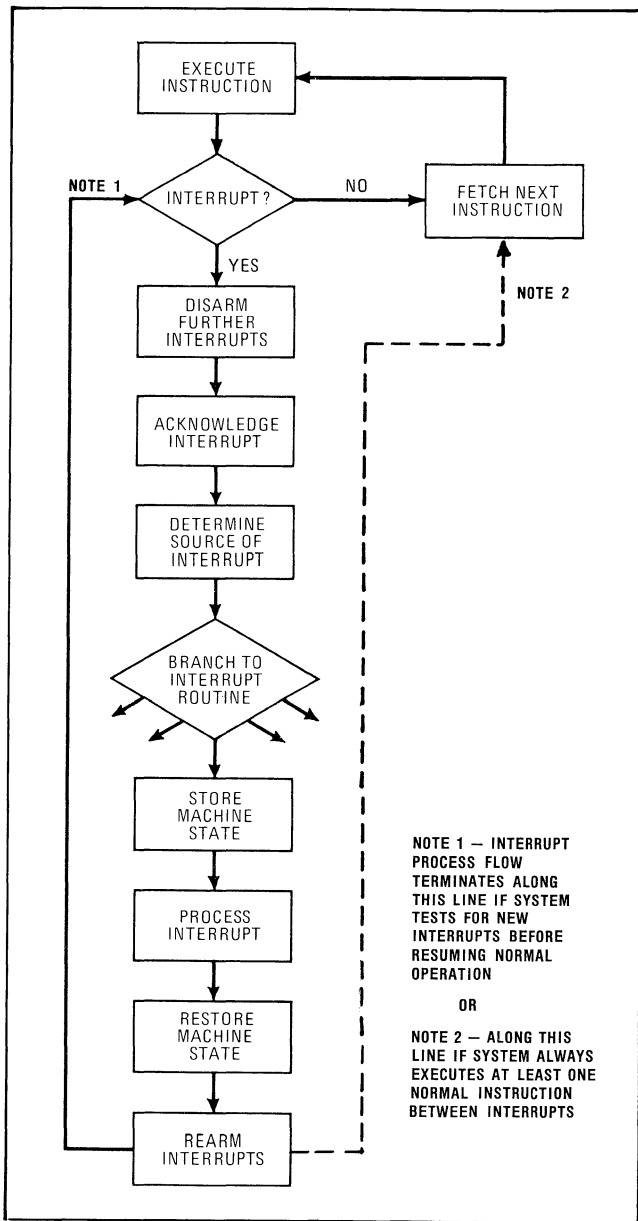
An interrupt-processing routine is shown in the flow chart in Fig. 8. The degree of complication varies widely from one microprocessor to another—some have processing interrupts that are more automatic than others. For example, the National Semiconductor GPC/P has a stack memory that can completely store the machine state in only five instructions. This highly efficient technique qualifies the GPC/P for excellent real-time process control.

Daisy-chain signal

After disabling further interrupts, as described previously, the microprocessor must acknowledge the current interrupt and determine its source. For this purpose, the interrupt-acknowledge line passes through all controllers in a "daisy-chain" fashion—the acknowledge signal passes from each one to the next until the source of the interrupt stops it. By this means, I/O priority is established by proximity to the microprocessor. Arrival of the interrupt-acknowledge signal triggers the sending by the controller to the microprocessor of its address, from which the microprocessor determines the location

of the routine to service the interrupt. In some systems, the controller can send, not its own address, but the actual address of the routine, so that the microprocessor can reach the routine via an indirect jump instruction; this is called a vectored interrupt.

In all interrupt routines, the machine state must be stored before anything else happens. Then, after much ado, the interrupt itself can be processed. When it is finished, the previous steps must be undone—the machine state is restored, and the interrupts are re-enabled. Depending on how the word “disabled” is defined, new interrupts that occurred during the previous interrupt process may have been ignored totally, or they may merely have been kept waiting. In a completely interrupt-oriented system, when re-enabled, the disabling signal can start the whole interrupt-resolving cycle



8. Sleeve puller. A microprocessor need not stand idle while waiting for an external event—if it can keep track of what it was doing when the event finally occurs. This flow chart outlines how it can mark its place in a secondary routine while processing an interrupt.

again before the microprocessor can get back to its main routine. If such new interrupts are unlikely, the microprocessor may get an automatic chance to execute one more instruction in its main program before checking again for interrupts.

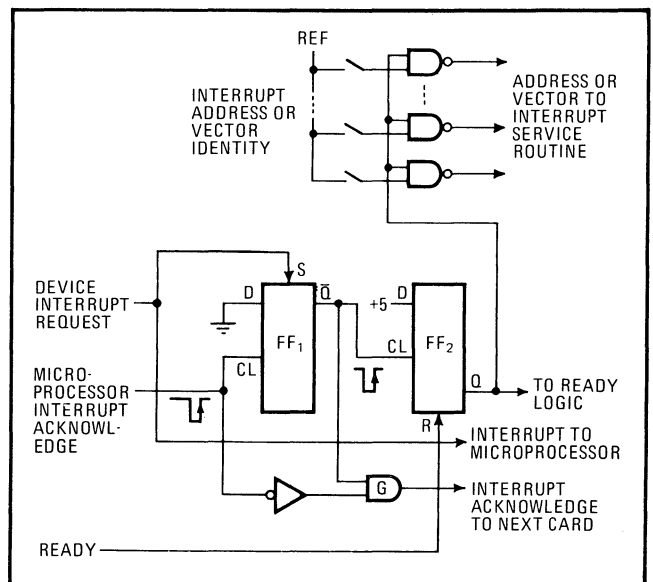
By adding the logic shown in Fig. 9, the previously described I/O controller can be easily modified to work on an interrupt basis. Usually the interrupt signal is the result of something that happens in the controlled I/O device, although it can be an event in the controller itself. Either way, the signal sets the flip-flop FF₁, and sends an interrupt request to the microprocessor. The microprocessor's acknowledgment passes, daisy-chain fashion, through all controllers via gate G until it reaches the one that originated the request, where G is blocked by the ON state of FF₁. The trailing edge of the acknowledge pulse resets FF₁, and the turning-off action sets another flip-flop, FF₂, which, in turn, opens gates admitting the controller's address to the data lines. FF₂ also generates a ready signal to the microprocessor, and the ready, delayed, turns off FF₂.

When interrupts aren't wanted

Because the entire process of handling interrupts may require many hundreds of microseconds, external events that occur, on the average, more than once every 4 or 5 milliseconds, will severely impede the main program if they depend on interrupts to obtain service. Therefore, if progress in the main program is important, or if many interrupts are expected, another technique should be used to service the external events.

An example of a process that can't depend on an interrupt for service is the refreshing of a cathode-ray-tube display. Suppose that the display has a capacity of 30 lines at 60 characters per line—a total of 1,800 characters to be refreshed 60 times per second. Refreshing requires 108,000 characters per second to be delivered to the display, or one character every 9.2 microseconds.

Many high-speed I/O processes, such as the preceding example, can tolerate relatively slow processing if the



9. Additional logic. These logic blocks must be added to the simple input/output controller of Fig. 6 to enable it to handle interrupts.

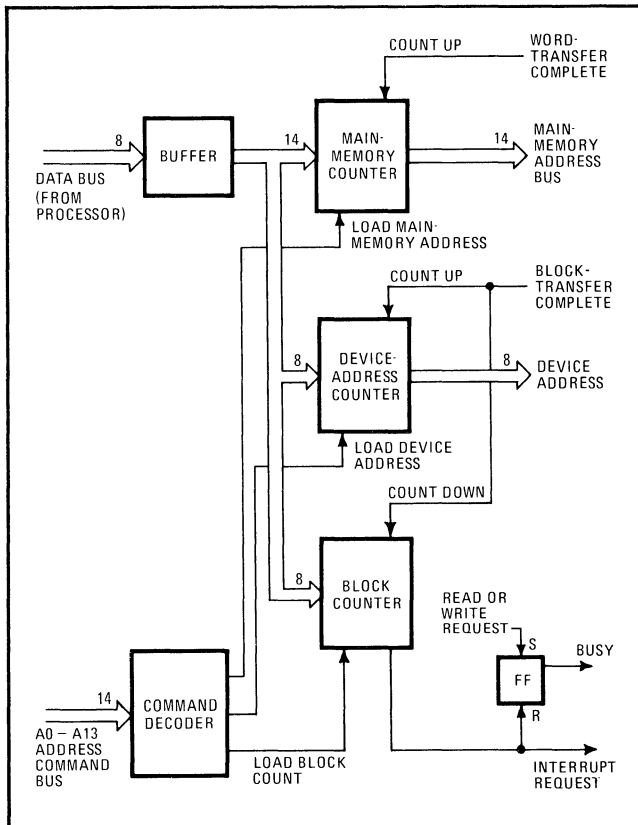
data transfer to and from the unit can be fast. These processes can therefore make use of a direct memory-access channel, or DMA, the next step up in complexity and performance from a simple interrupt.

A DMA channel in a microprocessor system requires a few more controls than those in the individual I/O-device controllers, which are not affected directly by their connection through a channel to memory instead of to the processor. The microprocessor obtains access to its own memory through these channel controls in the same way that the input/output controllers do, and, since conflicts can arise, the channel's main function is to detect and resolve them. They are less likely to occur with microprocessors than with minicomputers and large computers, however, because the microprocessor usually runs slower than its memory, not faster. Conflicts in systems of any size are always resolved in favor of the input/output, because the device is usually in mechanical motion and can't afford much delay.

Once the channel is under way, the channel controller takes over the task of selecting addresses, I/O sequences, and data handling. As a result, both I/O and processing operations are expedited—the first because it is limited only by the memory cycle rate, not the instruction rate, and the second because the microprocessor need not pause in its own work to run an I/O operation.

Block input/output

Channel input/output leads quite directly to block I/O, in which large blocks of data are transferred in or



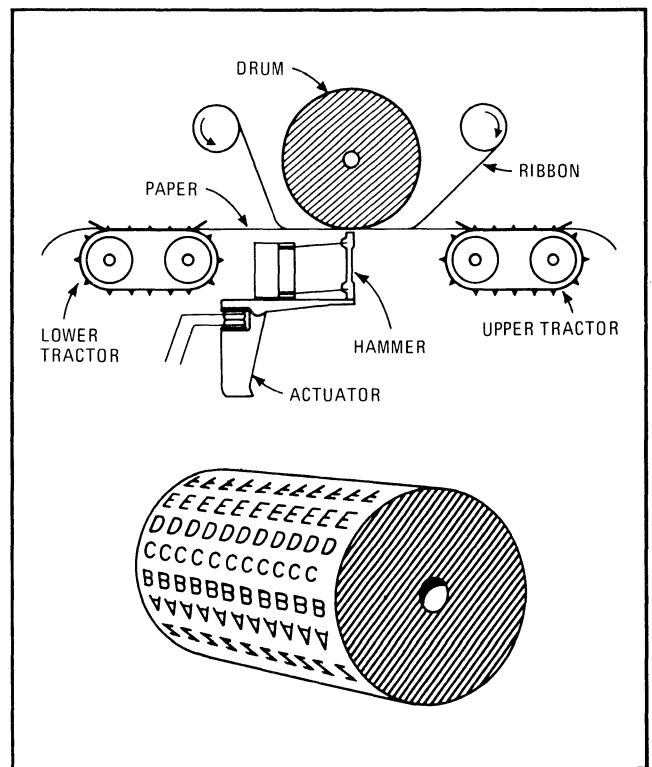
10. Block input/output. To transfer large blocks of data to or from memory, this logic is added to the basic input/output controller. It must not interfere with other microprocessor tasks, yet it must work with both internal device addresses and with memory.

out of the microprocessor by a single command sequence. Additional logic in the I/O controller is required to work, not only with addresses in the main memory and addresses of individual devices, but also with addresses within the device—such as tracks and sectors on a disk drive, files on tape, and so on.

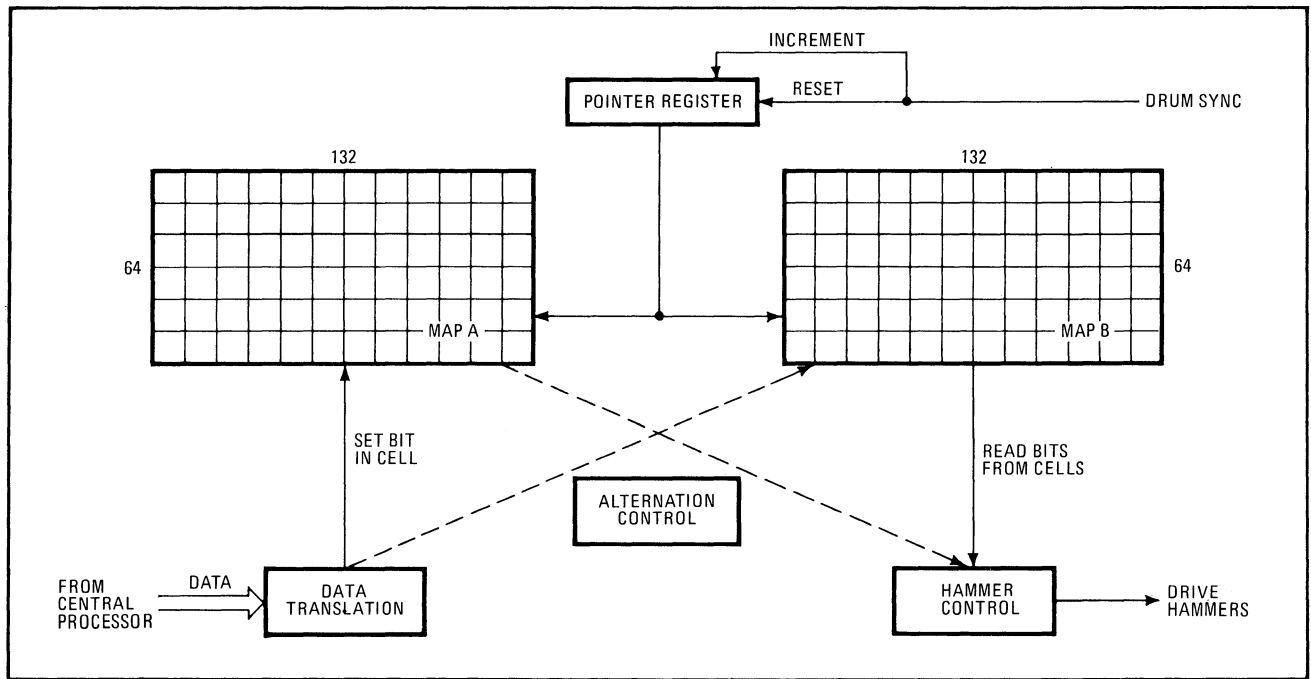
Three major elements (Fig. 10) must be added to a basic I/O controller to permit it to handle block input/output: an I/O device-address counter, a main-memory counter, and a block counter. At the start of an operation, the device-address counter is loaded with the device's internal address—such as the sector number—the main memory counter has the address to or from which the transfer of the block begins, and the block counter contains the number of blocks to be transferred. The first READ or WRITE command sets a BUSY flip-flop. As each word is transferred, the main-memory counter is incremented, and as each block is transferred, the block counter is decremented until it passes 0, generating a borrow signal. This signal resets the BUSY flip-flop and sends an interrupt signal to the microprocessor, which is thus informed that an I/O operation has been completed.

A drum-printer controller

The preceding sections have shown how a few common logic-design problems can be solved with a microprocessor, and how controllers for use with microprocessors can be easily and quickly designed. Many of these concepts can be combined in the design of a controller for a drum printer that takes advantage of a microprocessor to control the format of the data transfer



11. Drum printer. Rotating drum carries complete alphabet on its surface, repeated for each printing position across page. Separate actuator-hammer pairs for each position press the paper against the drum to pick up the imprint as the desired character passes.



12. Printer control. Microprocessor translates data from central processor into bits in map. These, in turn, identify the hammers to be actuated to print the data in the prescribed format. Two maps are used alternately; one fills with data while the other is printing.

between a larger central processor and the printer.

Microprocessors aren't suitable as controllers in every I/O application. For example, many magnetic-tape or disk units have data transfer rates that are far beyond the capabilities of any present or contemplated microprocessor. In fact, the fastest microprocessor now on the market is the National Semiconductor GPC/P, capable of a maximum of about 30,000 bytes per second, and the forthcoming Intel 8080 is limited to about 60,000. But since disks and tapes routinely spew forth data at hundreds of thousands and even millions of bytes per second, controllers for these devices must be built out of conventional logic circuits, and high-speed ones at that—emitter-coupled logic, in many cases—using microprocessors at best within the controller for certain process-monitoring tasks that do not involve data-handling.

But other I/O systems and subsystems are well suited for control by a microprocessor—among them, data-communications channels using telephone lines, card readers and punches, tape cassettes, floppy disks, and drum printers.

A typical drum printer prints a maximum of 132 columns of characters from a 64-character set at 1,800 lines per minute. To achieve this level of performance, the machine contains a drum (Fig. 11) with 132 complete sets of 64 characters in circumferential columns, and like characters in each set are lined up along an axial row. Close to its surface is a bank of 132 electromechanical hammers that can be driven toward the drum as it spins on its axis. But between the hammers and the drum is the web of paper upon which the printed characters are to appear, plus an inked ribbon to record the imprints.

As the drum turns, its position is monitored by the controller. As each of its character slugs to be printed in the 132 positions of a line approaches a point opposite

the corresponding hammer, the hammer is driven forward—timed in such a way that as it reaches the limit of its travel, it prints in the desired position by pinching the paper and the ribbon between it and the drum when the desired character slug is exactly opposite it. When the drum has made one complete revolution, a complete line has been printed on the paper, and the paper moves up into position for printing the next line. To allow time for paper movement, the characters do not fill the entire circumference of the drum.

One common controller design contains 132 6-bit counters. The controller translates the data in each printing position into a particular counting step. Such a straightforward but complex controller is not necessary when a microprocessor is employed.

Instead, the data to be printed is loaded in the form of a map into a large area of the microprocessor's main memory. This area can be visualized as a rectangular array of bit cells, 132 wide and 64 high (Fig. 12). Each 64-cell vertical column corresponds to one of the 132 printing positions on the paper, and each of the 64 cells in the column corresponds to one of the characters in that position on the drum. Two such maps in the memory enable the processor to fill one while a line is being printed from the other, and their roles are reversed for alternate lines of printing.

At 1,800 lines and 1,800 revolutions per minute, the drum makes one revolution in 1/30 second; during this interval the central processor must provide the map with up to 132 characters. This is 3,960 characters per second or one character every 252 microseconds—a data rate that is well within the capabilities of a microprocessor.

The microprocessor, working as a controller, uses simple arithmetic and masking instructions to translate data received from the central processor into bits placed in the map. The character to be printed identifies the bit

Cranking up the microprocessor

Now that the engineer has read how to apply microprocessors to every-day design problems, assume that he orders one—from Intel, or National, or anybody. The microprocessor has an adequate quantity of read-only and read-write memory and all the necessary extraneous parts. Now, suppose that the engineer writes a program to fit his application; and assume that the program is right the first time and that it's been put into a programmable ROM connected to the microprocessor system. Now, how does he start the machine?

Large general-purpose computers always come with software that helps load programs into the memory and ensures that the computer starts running the program when it is turned on. This software is so cleverly designed that it seems to melt right into the scenery. The rules followed in writing the program may have been imposed, in part, by the computer hardware, but some of them were imposed by the software. However, the microprocessor doesn't have any software like this.

To start any processor, some kind of number must be

loaded into the program counter, which will then indicate the first instruction in the program, and the processor clock has to be started. In Intel's 4004 microprocessor, this is brutally simple—an external line, when grounded, forces the program counter to 0, and when the ground is removed, the clock starts running. If the first instruction of the program has been placed in memory location 0, grounding the reset line makes the program counter point to that first instruction, and removing the ground starts the processor.

The 8008 is also simple to start, but the process is not quite so straightforward. Essentially, the machine can be made to execute an instruction that is not in the program, but which forces the program to jump to a location whose address is a multiple of 8. Any address between 0 and 56 can be used; if the first instruction of a program is in that location, the processor starts running as soon as the jump has been executed.

Other microprocessors also have similar simple means of starting.

cell in the column of 64, and sets that cell to 1; all other cells in that column remain 0s. Successive characters in the line set corresponding bits in successive columns in the map.

When the map has been filled with bits corresponding to data to be printed, the map turns to the control of the spinning drum. Once per revolution, the drum generates a synchronizing signal that says the first character in the set of 64 is in a position to be printed anywhere it may be required along the line—possibly, but improbably, in all 132 positions at once. This synchronizing signal sets a pointer at row 1 in the map. If any of the 132 bits in that row is 1, the hammer corresponding to the bit position fires to print the first character in the proper column. The pointer then is incremented to row 2 as the drum continues to rotate into the next character position. This process is repeated for all 64 rows in the map and all 64 print positions on the drum.

But in reading out these map cells, the microprocessor can take, say, 8 bits at a time (assuming that it is an Intel 8008 or similar system). Thus, to print in 132 character positions, the microprocessor can take 17 memory accesses—16 of 8 bits each and one of 4 bits. (A standard line length for printers is 132 characters, but unfortunately, 132 is not divisible by 8.)

Meanwhile, the spinning drum passes one of the 64 character positions in $1/30 \times 1/64 = 1/1,920$ second, or about 521 microseconds. However, during this period, for accurately aligned smudge-free printing, all the hammers that are to be pulsed to print a given character must be pulsed within a 66- μ s window. This ratio of 66 to 521 represents a rather relaxed duty cycle for the printer mechanism, allowing plenty of time for the hammers to settle back into position after firing, but during the window, the microprocessor must peel off 17 8-bit bytes from the map—less than 4 μ s per byte. To handle this data rate, the microprocessor must have a DMA channel.

This printer-control algorithm can be coded for the Intel 8008 microprocessor or the new 8080 with only 72

bytes in the program. The memory maps—two—require 2,176 bytes. The 8008 isn't fast enough to run the hypothetical printer, but it can handle about 500 lines per minute, a respectable speed for some applications. The 8080, on the other hand, can handle about 5,000 lines per minute.

In an actual application, of course, a full controller would be required—with other functions, such as sequencing, vertical forms control, and various alarm functions. But the basic simplicity of a controller built around a microprocessor is apparent.

This design has several important aspects. No gate-level logic design was necessary, and no state diagrams were used. Also, only slight program changes would be necessary to control a printer with a larger or smaller character set, a different input code from the central processor, or even a more complex printer, such as a chain printer. □

REFERENCES

1. John B. Peatman, "Design of Digital Systems," pp. 211–216 and secs. 6–6, 6–7, McGraw-Hill Book Co., 1972.
2. "MCS-4 Microcomputer Set User's Manual," Intel Corp., July 1972.
3. "8008 8-bit Parallel Central Processor Unit," Intel Corp., November 1972.

BIBLIOGRAPHY

- "Product Description, General Purpose Controller/Processor (GPC/P) MOS/LSI System Kit," National Semiconductor Corp., March 1972.
- W. H. Davidow, "General-Purpose Microcontrollers, Part 2: Design and Applications," Computer Design, August 1972, p. 69.
- Michael Davis, "Processor Interrupt Scheme Speeds Response and Minimizes Overhead," EDN, Sept. 15, 1972, p. 49.
- Gerald Lapidus, "MOS/LSI Launches the Low-Cost Processor," IEEE Spectrum, November 1972, p. 33.
- Yaohan Chu, "Computer Organization and Microprogramming," Chapter 8, Prentice-Hall Inc., 1972.
- "How to Use the CPS/1 Microcomputer System," Microsystems International Ltd., 1972.

Analyzing ladder-type networks by a quick arithmetic procedure

Many ladder networks can be analyzed virtually by inspection through the generation of an impedance matrix that can be rapidly checked to find network voltage transfer characteristic and input impedance

by Einar C. Johnson, Naval Air Development Center, Warminster, Pa.

□ Since most filter, equalization, and phase-shift networks can be reduced to ladder form, a simple analysis procedure for ladder-type networks can be a significant time-saver. One technique that involves only simple division and determinant evaluation allows many networks to be analyzed quickly by inspection for input-to-output voltage transfer ratio, as well as input impedance.

The procedure is easy to follow. As shown in Fig. 1 for an n-mesh ladder network, an impedance matrix can be generated. A large square is drawn and then divided into n smaller squares, which are filled with impedance values taken from the ladder network. The large outer square is called the impedance matrix (\dot{Z}). For an n-mesh network, the impedance matrix has an nth-order determinant that is designated as D_n .

The inner squares along the main diagonal are filled with the impedance sums accumulated by going around each mesh. The squares adjacent to and parallel with the main diagonal contain the shunt impedances of the network. (These shunt impedances are negative because of the direction chosen for positive mesh-current flow.) All the other squares are left blank, indicating an entry of zero.

Network voltage and impedance analysis

To find the voltage transfer ratio, e_1/e_2 , only the nth mesh current, i_n , must be computed, since:

$$e_2 = i_n Z_{2n}$$

The matrix form of Ohm's law is:

$$\dot{i} = (\dot{Z})^{-1} \dot{e}$$

In this case, only the last mesh current, i_n , in current matrix \dot{i} is needed. And the only non-zero entry in voltage matrix \dot{e} is e_1 . Additionally, the only pertinent element of inverted impedance matrix $(\dot{Z})^{-1}$ is $(Z_2 Z_4 Z_6 \dots Z_{2n-2})/D_n$. Rewriting the last equation yields:

$$i_n = e_1 (Z_2 Z_4 Z_6 \dots Z_{2n-2}) / D_n$$

since:

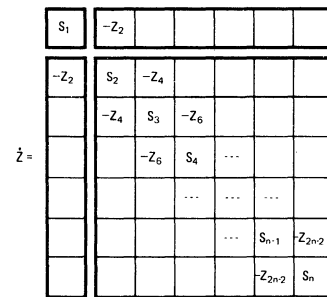
$$e_2 = i_n Z_{2n} = e_1 (Z_2 Z_4 Z_6 \dots Z_{2n}) / D_n$$

then:

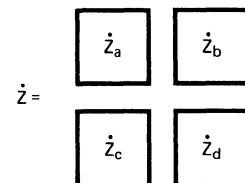
$$e_1/e_2 = D_n / (Z_2 Z_4 Z_6 \dots Z_{2n}) \quad (1a)$$

or:
$$\frac{e_1}{e_2} = \frac{\text{determinant of impedance matrix}}{\text{product of all shunt impedances}} \quad (1b)$$

To show how the input impedance of an n-mesh network can be evaluated, the impedance matrix is cut into four submatrices so that the S_1 sum is isolated:



For simplicity, the four submatrices of \dot{Z} are labeled as \dot{Z}_a , \dot{Z}_b , \dot{Z}_c , and \dot{Z}_d :



In terms of these submatrices, the network's input impedance can be expressed as:

$$Z_{in} = \dot{Z}_a - \dot{Z}_b (\dot{Z}_d)^{-1} \dot{Z}_c$$

Since $\dot{Z}_a = S_1$, this equation can be rewritten as:

$$Z_{in} = S_1 - \dot{Z}_b (\dot{Z}_d)^{-1} \dot{Z}_c \quad (2)$$

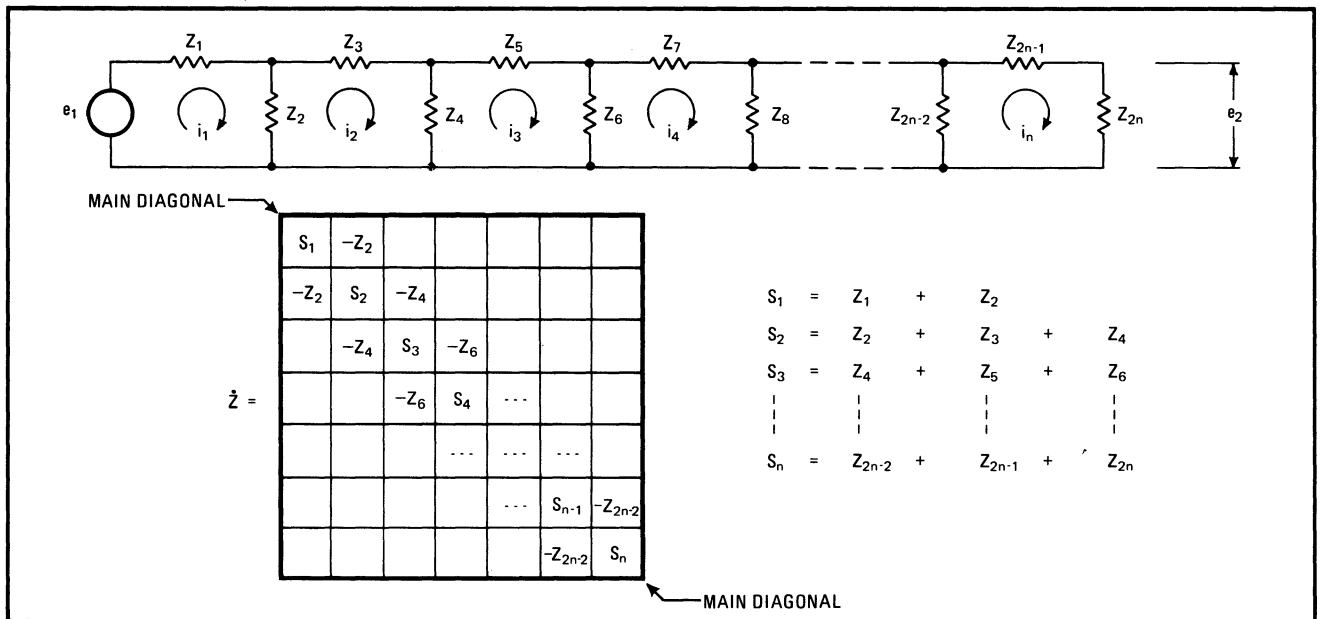
Because submatrices \dot{Z}_b and \dot{Z}_c contain a single common entry, $-Z_2$, only the element in the first row and column of inverted matrix $(\dot{Z}_d)^{-1}$ is needed. This element is D_{n-2}/D_{n-1} , where D_{n-1} is the determinant remaining after the first row and column are eliminated from determinant D_n . Likewise, D_{n-2} is the determinant remaining after the first two rows and columns are eliminated from D_n . Substituting impedance values for the submatrices in Eq. 2 yields:

$$\begin{aligned} Z_{in} &= S_1 - (-Z_2)(D_{n-2}/D_{n-1})(-Z_2) \\ &= S_1 - Z_2^2 D_{n-2}/D_{n-1} \end{aligned}$$

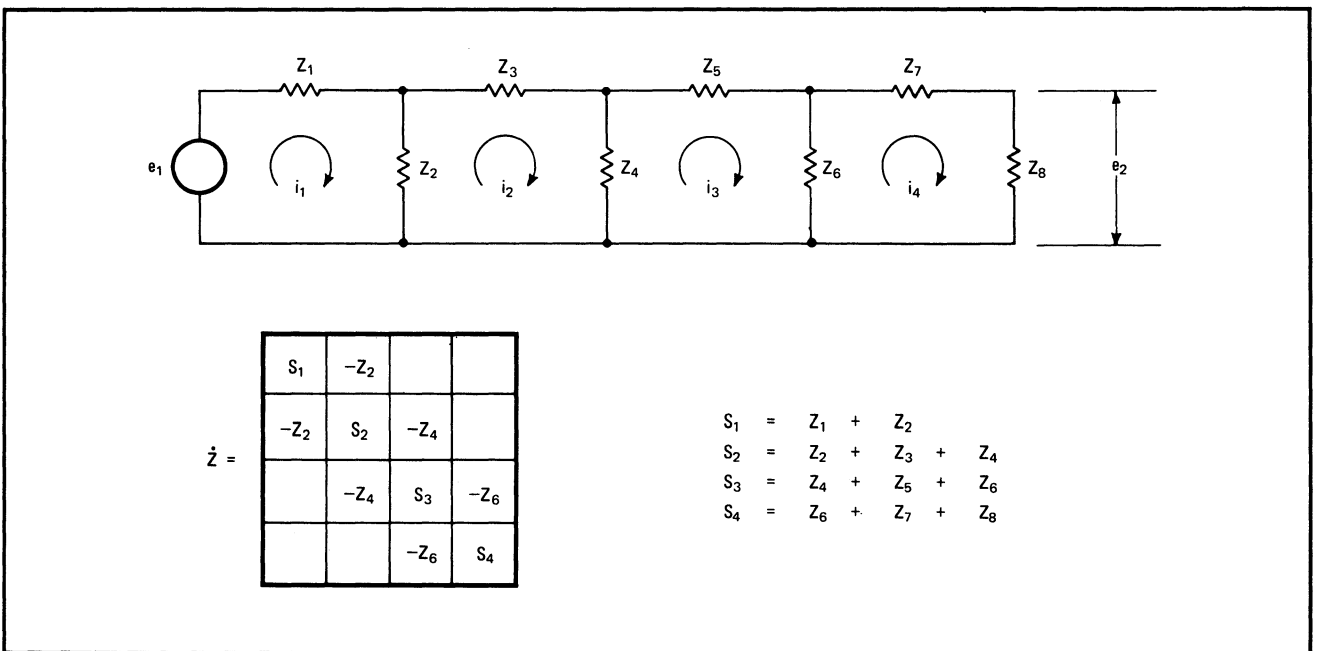
or:

$$Z_{in} = (S_1 D_{n-1} - Z_2^2 D_{n-2}) / D_{n-1}$$

Since the numerator of this equation is simply a mathe-



1. Generalized configuration. Ladder network, consisting of n meshes, can be represented by an impedance matrix, \hat{Z} . Since this matrix is a square array, it can be handled as an n th-order determinant, where n is the number of meshes. The impedance sums for each mesh are placed along the matrix's main diagonal, while the shunt impedances are alongside of these; the other spaces remain blank.



2. Four-mesh ladder. Here, impedance matrix \hat{Z} is only a fourth-order determinant. But, no matter how large the ladder network is, the impedance matrix can be evaluated quickly because there are always many zeroes (blank spaces). Once the impedance-matrix determinant is evaluated, the network's voltage transfer ratio can be found by simply dividing the determinant by the product of the shunt impedances.

$$\frac{e_1}{e_2} = -G = \frac{[R^3 - 5R/(\omega C)^2] + j[(1/\omega C)^3 - 6R^2/\omega C]}{R^3}$$

or:

$$GR^3 = [5R/(\omega C)^2 - R^3] + j[6R^2/\omega C - 1/(\omega C)^3] \quad (6)$$

The left side of this equation is a pure real number, allowing the imaginary term on the right side to be equated to zero:

$$\begin{aligned} j[6R^2/\omega C - 1/(\omega C)^3] &= 0 \\ 6R^2 &= 1/(\omega C)^2 \end{aligned}$$

which can be solved for the frequency of oscillation:

$$\omega = 1/\sqrt{6} RC \text{ radians/second}$$

or:

$$f = 1/(2\pi\sqrt{6} RC) \text{ hertz}$$

By substituting the quantity $6R^2$ for $1/(\omega C)^2$ in the real part of Eq. 6, amplifier gain can be found:

$$\begin{aligned} GR^3 &= 5R(6R^2) - R^3 \\ G &= 29 \text{ or } 29.5 \text{ decibels} \end{aligned}$$

This is the amplifier voltage gain required to sustain oscillation. To find input impedance, the network's D_{n-1} determinant must be evaluated:

$$D_{n-1} = D_2 = S^2 - R^2 = [3R^2 - 1/(\omega C)^2] - j[4R/\omega C]$$

But since:

$$6R^2 = 1/(\omega C)^2$$

then:

$$D_2 = -R^2(3 + j4\sqrt{6})$$

Applying Eq. 3 gives:

$$Z_{in} = D_3/D_2 = 29R/(3 + j4\sqrt{6})$$

$$= R(0.829 - j2.706)$$

Changing network impedance level

Additionally, this analysis technique permits the impedance level of the ladder network to be changed readily. If each impedance element in an n-mesh ladder is multiplied by a factor of K, then each element in the impedance-matrix determinant is multiplied by K. When every element of an nth-order determinant is multiplied by the same factor, the entire determinant is

effectively multiplied by a factor of K^n . The network's voltage transfer ratio becomes:

$$e_1/e_2 = K^n D_n / (KZ_2)(KZ_4)(KZ_6) \dots (KZ_{2n})$$

or:

$$e_1/e_2 = D_n / Z_2 Z_4 Z_6 \dots Z_{2n}$$

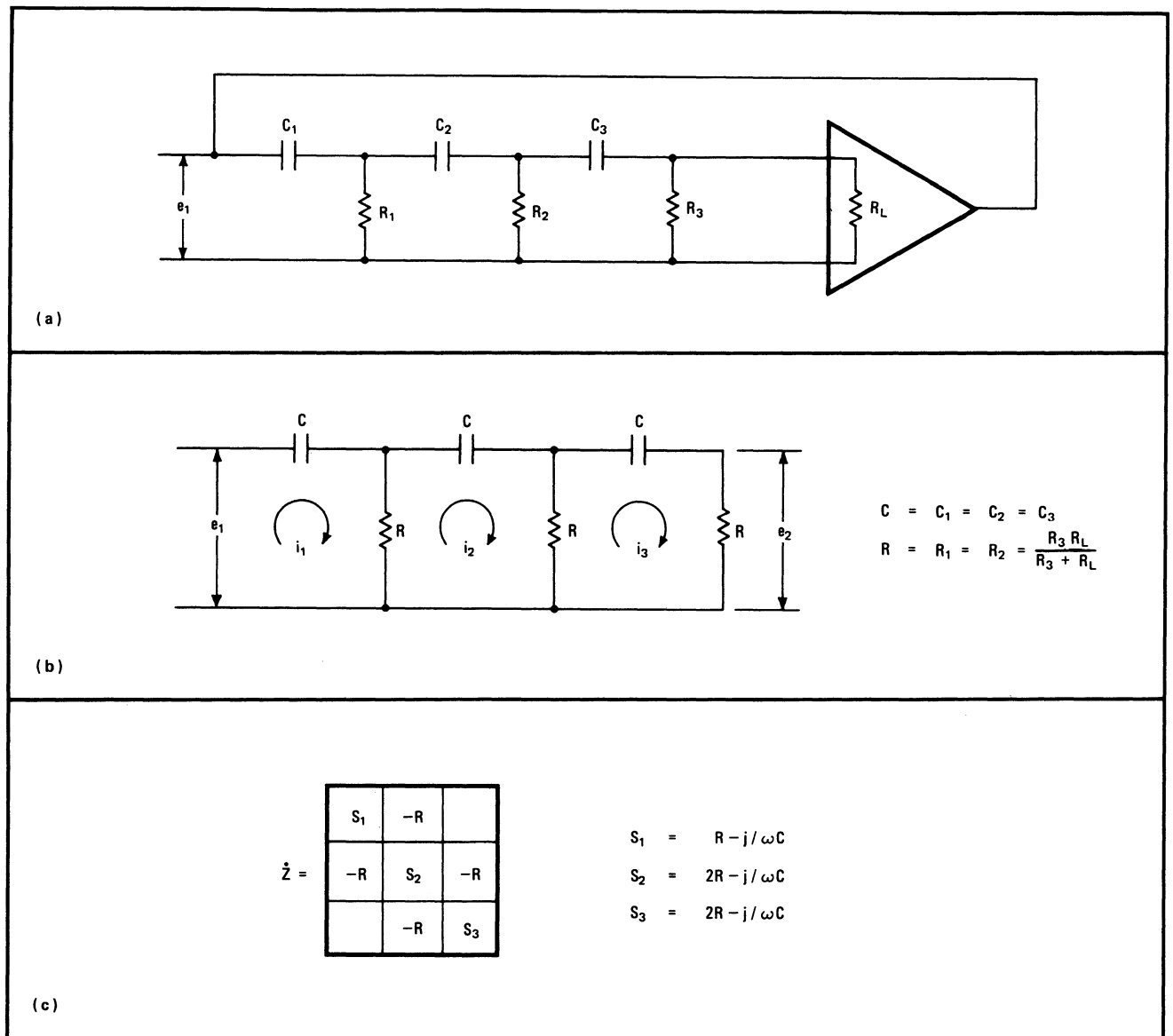
which is identical to Eq. 1. Therefore, changing a network's impedance level has no effect on the voltage transfer ratio.

Network input impedance, however, does change. Since multiplying all the elements of the impedance-matrix determinant by K multiplies the entire determinant by K^n , then the D_{n-1} determinant is multiplied by K^{n-1} . From Eq. 3:

$$Z_{in} = K^n D_n / K^{n-1} D_{n-1} = K D_n / D_{n-1}$$

The input impedance of the ladder network, therefore, is multiplied, by the same factor as the individual network impedances. □

3. Oscillator circuit. Three-mesh ladder of RC oscillator (a) can be reduced to network drawn in (b) for analysis. Impedance matrix of (c) simplifies computation of oscillator's operating frequency, input impedance, phase shift, and the gain of the amplifier.



Norton quad amplifier subtracts from costs, adds to design options

Consisting of four identical linear circuits on one chip, the Norton quad amplifier operates off a single power supply; biasing is simplified, and so too is the design of several waveform-generating circuits

by Thomas M. Frederiksen, *National Semiconductor Corp., Santa Clara, Calif.*

□ Pressured by the demands of the automobile industry, consumer electronics manufacturers, and other mass-production customers into finding new ways of producing ever cheaper components, semiconductor makers have developed a new family of linear integrated circuits. These linear ICs each contain, in a single package, four identical but independent devices—four comparators, or four conventional inverting-type operational amplifiers, or four of the rather less conventional, so-called Norton amplifiers.

All three types are available from a growing number of manufacturers. Not only do the quads each cost far less than four devices bought separately, but industrial and communications equipment designers are also attracted by their promise of reducing system cost while maintaining high levels of component operation.

The fact is that many linear circuit functions do require more than one of a similar type of comparator or amplifier. Comparators are often used in pairs, in limiting comparator circuits and crystal-controlled oscillators, for instance, while a two-decade high-frequency voltage-controlled oscillator needs three. Similarly, a simple by-pass filter requires two op amps, a phase-locked loop needs three, and a sine-wave oscillator or sawtooth generator needs four.

But even if only one component of the quad is required in a given circuit, the others can be used for dozens of auxiliary circuit purposes. Examples are biasing or gain-control networks or simple gain blocks.

Most important, the new Norton quads need only a single-ended power-supply voltage and operate well over a wide range of power-supply voltages, from 3 volts dc to 32 v dc. Moreover, a typical quad Norton amplifier draws a constant low supply current of 1.3 milliamperes, and both the comparator and the operational amplifier draw a constant 0.2-mA supply current per circuit function.

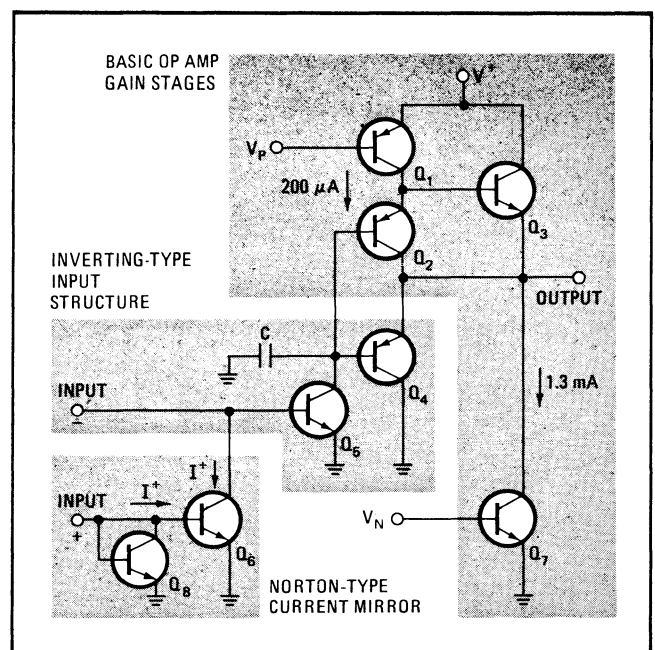
The Norton quad amplifier

The most radical of all the three quad designs is the Norton amplifier, the LM3900. To obtain noninverting input signals, op-amp designs use a standard transistor differential amplifier—a fairly elaborate circuit that unfortunately requires two (a positive and a negative) supply voltages. In the Norton amplifier, this requirement was eliminated by putting the simplest type of inverting amplifier (that is, a common-emitter stage) at the input

(Fig. 1) and then adding a “current mirror” circuit across the inverting input terminal to provide a noninverting input.

Just about all the positive input current is forced into becoming collector current in the diode-connected input transistor, Q_8 . At this level of conduction, an “on” biasing voltage (V_{BE}) results across the base-emitter junction of the transistor. The same biasing voltage is applied to a second matched transistor, Q_6 , which therefore conducts the same amount of current as in Q_8 . Consequently, the current from the output of this stage equals the input current, I_{in} , which has thus been “mirrored” or reflected about ground.

In this scheme all of the voltage gain in the basic amplifier is provided by the gain transistor, Q_5 , and the output emitter-follower transistor, Q_3 , serves simply to isolate the load impedance from the high impedance that exists at the collector of Q_5 . Closed-loop stability is guaranteed by an on-chip 3-picofarad capacitor, C , which provides the single dominant open-loop pole.



1. Inverted inversion. In the Norton amplifier, a current-mirroring circuit has been added to a conventional inverting-type input structure so that a noninverting input signal can be achieved from a single +5-V power supply. Such an input usually requires two supplies.

The output emitter-follower is biased for class A operation by the current source, Q_7 .

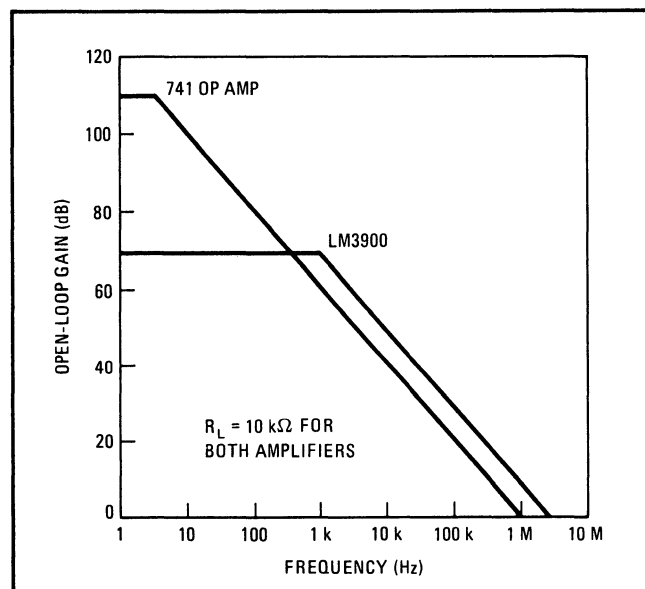
In the design of the LM3900, two pnp transistor stages have been added. The lateral pnp, Q_2 , reduces the input current and provides additional load isolation. The vertical pnp, Q_4 , converts the class A output stage to a class B stage for large signal cases. This allows the amplifier to sink larger load currents than the 1.3-mA pull-down current source would provide.

Big gain

It should be pointed out that the Norton amplifier, by making use of current source loads, achieves a large voltage gain which is constant over a wide range of power-supply voltages. The output voltage has a large dynamic voltage range—essentially from ground to the power supply voltage minus V_{BE} . Power-supply current drain is almost independent of the power-supply voltage, and ripple on the supply line is also rejected. Furthermore, a very small input biasing current allows high-impedance feedback elements to be used.

Besides simplifying the circuit configuration, the use of only a single power supply results in many biasing advantages. Since the bias currents are all derived from diode forward-voltage drops, a bias current changes only slightly in magnitude as the power-supply voltage is varied. The open-loop gain also changes only slightly over the complete power-supply voltage range and is essentially independent of temperature changes.

The open-loop frequency response of the LM3900 is compared with the 741 op amp in Fig. 2. The higher unity gain crossover frequency is seen to provide an additional 10 decibels of gain for all frequencies greater than 1 kilohertz. Also, because currents can be passed between the input terminals, designers can apply this amplifier to jobs that generally are hard for standard op amp configurations to do, like function generators and some phase-locked-loop circuits. Moreover, if external large-valued input resistors are used to convert from in-



2. Greater gain. The open-loop gain characteristics of the LM3900, when compared with those of a conventional 741, reveal its advantage at higher frequencies—an extra 10 dB of gain above 10 kHz.

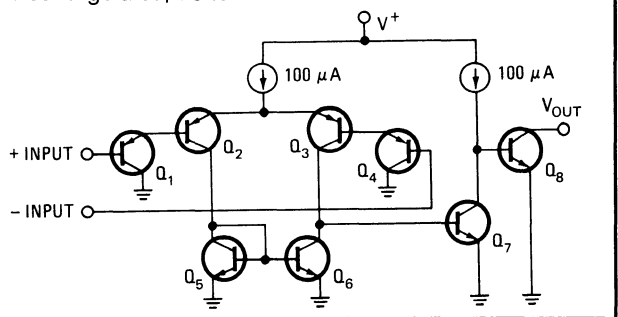
Another quad for comparison

Versatility is also a feature of another member of the quad family—the quad comparator, National's version of which is designated the LM339. The basic circuit, of which there are four per chip, shows high gain and low input current. It comprises a Darlington pnp single-supply differential-input stage, a current source as the load for the second stages, and a grounded-emitter npn output transistor (see figure). Flexibility is achieved by leaving the collector of this output transistor, Q_8 , uncommitted. As a result, the voltage to which the external load is returned is independent of the magnitude of the power-supply voltage, and the outputs of more than one comparator can be connected to a common load to provide an output OR-ing function.

The total biasing current for this comparator is only 200 microamperes, yet it achieves a transconductance of 5 mhos (the output will fully switch 1 milliampere of current for a change in the differential input voltage of 0.2 millivolt). The input currents and offset voltage are 35 nanoamperes and 3 mV respectively. Because of their simplicity, four of these comparators are easily fabricated on one die.

These comparators are also unique in that, even though they are operated from a single positive power-supply voltage, the input common-mode voltage range includes ground. Operation is possible over a wide single-supply voltage range (2 to 36 V dc) or from dual supplies (± 1 to ± 18 V dc), adding to the design's flexibility. Moreover, the supply current drain of 800 microamperes is essentially independent of the magnitude of the power supply voltage, which with a +5-V dc digital supply amounts to 1 milliwatt per comparator.

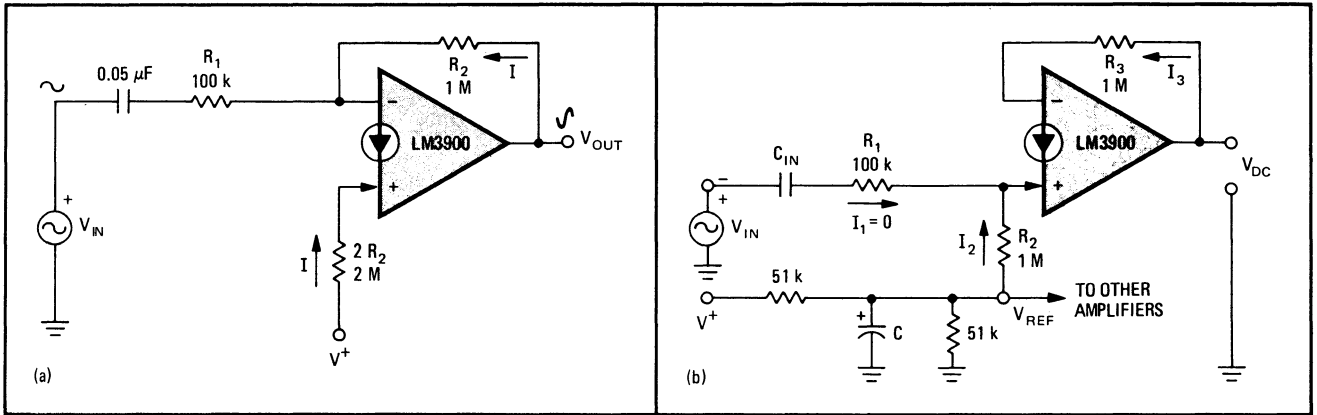
Large differential input voltages can be accommodated, and a special design for the output transistor provides an offset voltage of 1 mV. This last feature is important when the output of the comparator is used, for example, as a single-pole, single-throw switch to ground in an RC sweep circuit to precisely discharge a capacitor.



put voltages to input currents, most of the standard op-amp applications can be realized as well.

The LM 3900 Norton amplifier can be biased in several different ways. The circuit in Fig. 3a, a standard inverting ac amplifier, has been biased from the power supply that is also used to operate the amplifier. Note that if ac ripple voltages are present on the V^+ power-supply line, they will couple to the output with a gain of $\frac{1}{2}$. To eliminate this, a single source of ripple-filtered voltage can be provided for many amplifiers.

Figure 3b shows both a noninverting ac amplifier and



3. Straightforward biasing. One way of biasing the LM3900 takes a standard inverting ac amplifier and biases it from the supply that also powers it (a). In the dc biasing method, (b), the amplifier gain is set by the ratio of feedback resistor to input resistor.

a second method for dc biasing. The ac gain of the amplifier is set by the ratio of feedback resistor to input resistor. The small-signal impedance of the diode at the noninverting (+) input should be added to the value of R_1 when calculating gain.

By making $R_2 = R_3$, the dc voltage output will be equal to the reference voltage that is applied to resistor R_2 . This filtered ($V\theta/2$) reference voltage can easily be used for other amplifiers.

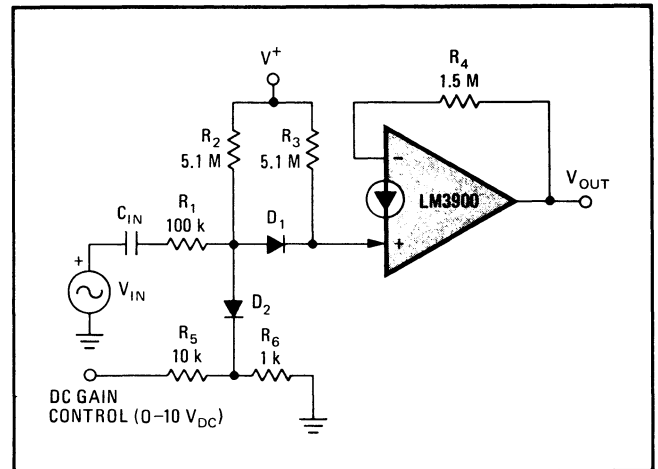
Another interesting feature of this setup is that the input resistor, R_1 , is isolated from the inverting (-) input terminal by the output impedance of the transistor of the current mirror. The amplifier is therefore not operating in an input-voltage to output-voltage feedback mode but, instead, along with the feedback resistor, R_3 forms a feedback-stabilized transimpedance amplifier with a gain equal to R_3 . As R_1 is isolated from the (-) input, this represents essentially unity voltage feedback, and the resulting bandwidth is the unity gain crossover frequency (2.5 MHz) of the basic amplifier. Consequently, the value of input resistor R_1 can be made small and, by thus increasing the voltage gain without affecting the feedback factor of the basic transimpedance amplifier, can help provide large gain at high frequency.

A gain of over 100 (40 dB) is possible at 1 MHz—and the high frequency limit is now set by the slew rate of the amplifier. This is useful for many applications where gain at signal frequencies above the standard op amp limits is required.

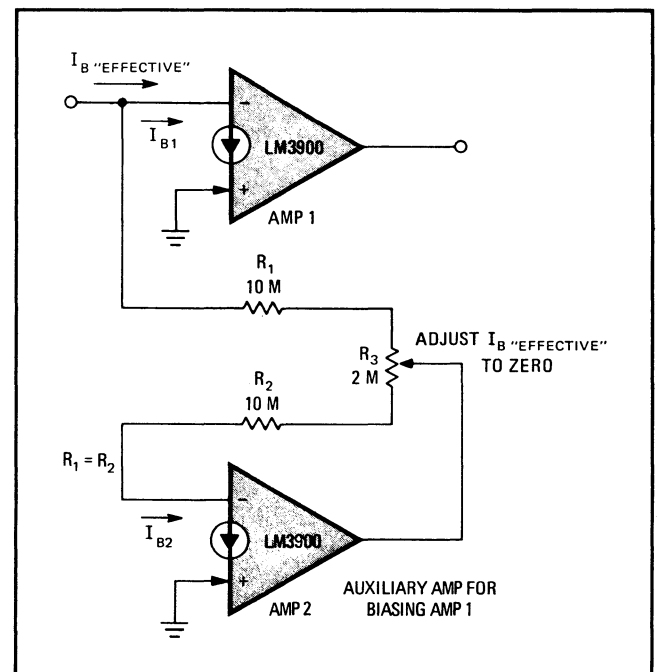
The same effect, incidentally, could be obtained by adding a current mirror to the 741 operational amplifier. But this mirror circuit would have to be made with closely matched discrete transistors, something that is done on the chip with the LM3900.

Adding dc gain control

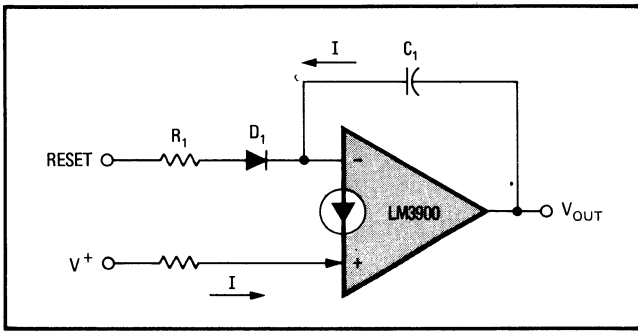
A dc gain control can be added to the noninverting Norton amplifier as shown in Fig. 4. A minimum biasing current passed through R_3 prevents the output of the amplifier from going into saturation as this dc gain control is varied. For maximum gain, the control rectifier D_2 is off, so that the current through R_2 as well as R_3 can enter the (+) input and cause the output of the amplifier to be biased at approximately 6.0 v (with a 10-v supply). For minimum gain, D_2 is on, and only the



4. In control. In this simple dc gain control circuit, input voltages range from 0 V dc for maximum gain, to less than 10 V dc for minimum gain. A biasing current through R_3 prevents saturation.



5. Useful symmetry. Four independent amplifiers available in each LM3900 package make it easy to exploit the symmetry that exists between the individual devices. Here, one amplifier is biasing another.



6. To and fro. In the basic Norton quad sweep circuit, current entering the noninverting (+) input causes the output to sweep linearly in a positive direction. Conversely, current entering the inverting (-) input causes the output to sweep linearly but negatively.

current through R_3 can enter the (+) input to bias the output at approximately +3.0 v. The proper output bias for large output signal accommodation is provided for the maximum gain situation. The dc gain control input ranges from 0 v dc for maximum gain, to less than 10 v dc for minimum gain.

Symmetrical amplifier designs

From these multiple amplifier packages, it is now possible to produce symmetrical designs. Historically, resistors have been the most predictable electronic components, and they gave rise to feedback amplifiers in which closed-loop amplifier performance depended only on resistors. Following this, two matched transistors were placed in a single can to make improved input stages for discrete op amps. Later still, integrated circuits derived performance advantages from their inherent resistor and transistor matching. And now multiple amplifiers in a single monolithic quad package allow designers to exploit the symmetry existing between the individual amplifiers.

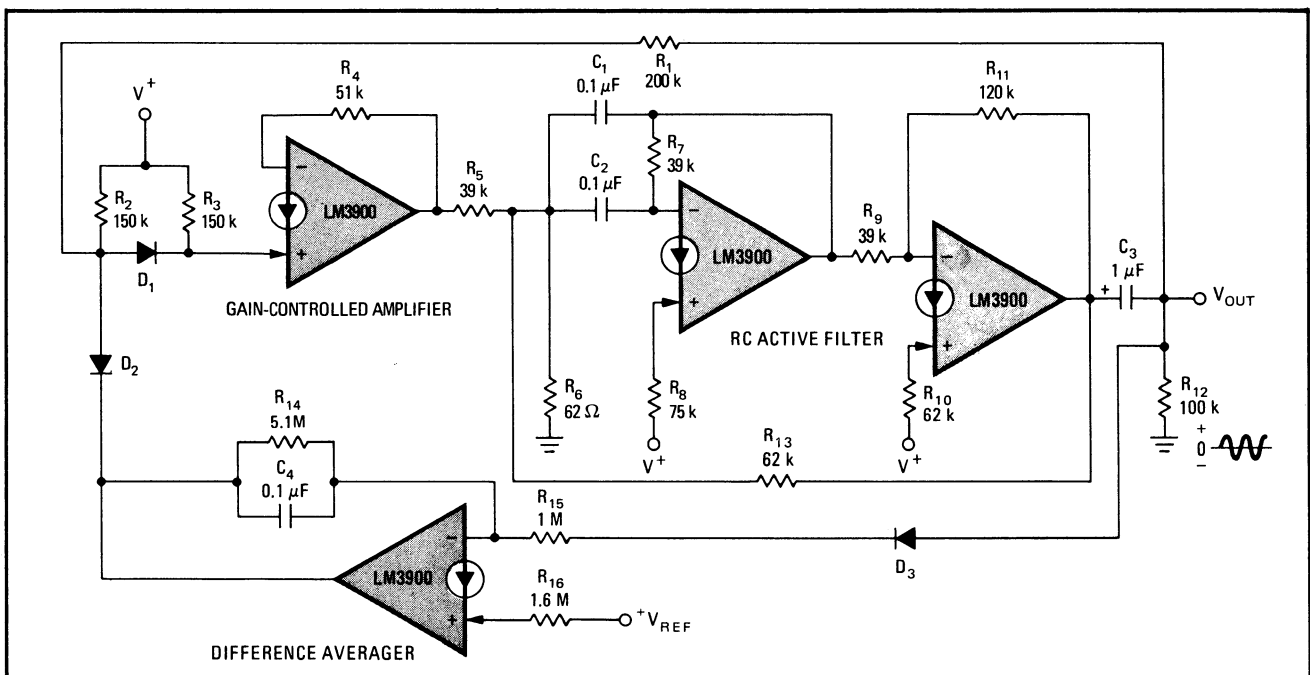
The example of symmetry shown in Fig. 5 has one amplifier biasing one or more additional amplifiers. So long as the dc biasing current, I_B , is accurately supplied via R_1 , the input terminal of amplifier 1 needs supply only enough current for the amplifier signal. The adjustment, R_3 , allows a zeroing of I_B which is useful in such circuit functions as sample-and-hold, where small values of I_B are desirable. Otherwise, if R_3 were omitted, simply letting $R_1 = R_2$, and relying on amplifier symmetry could cause the effective I_B to be less than $I_B/10$ (3 nanoamperes).

Clean sweeps

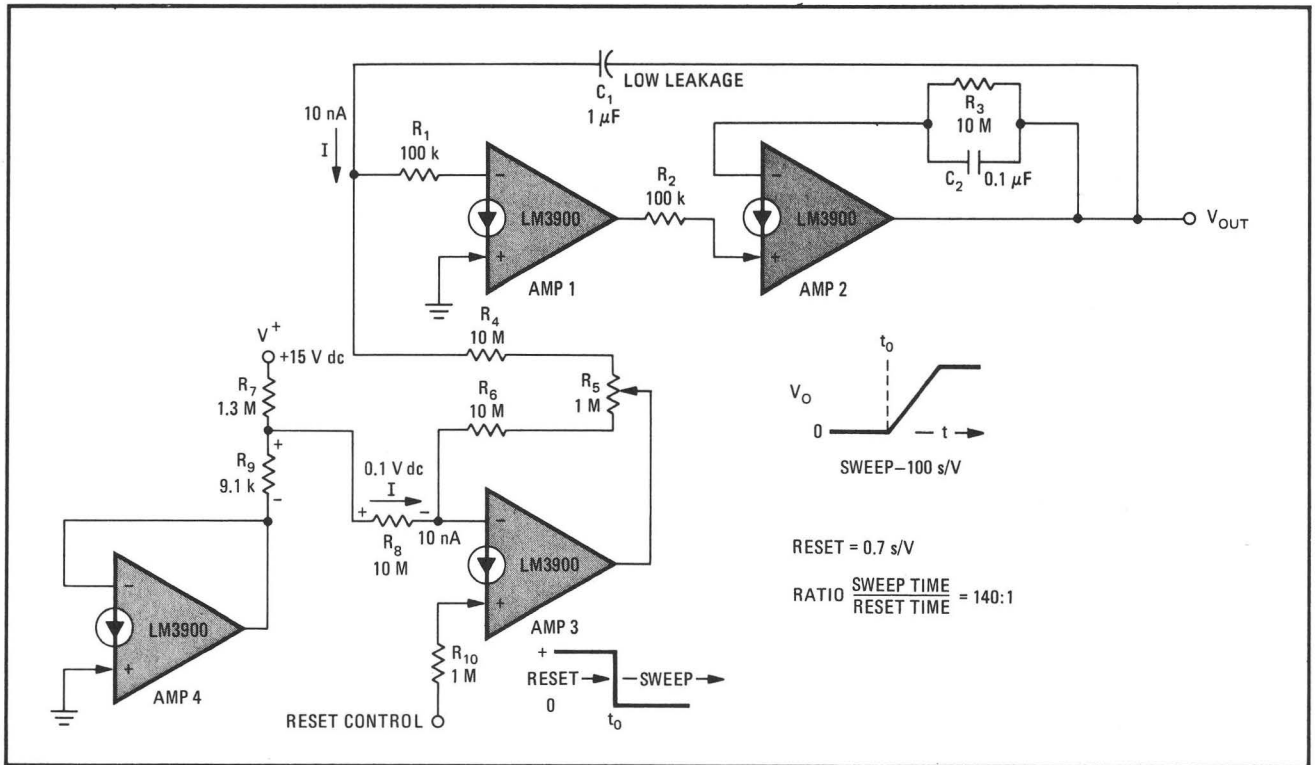
Many waveform-generating circuits can be realized with the Norton quads. The basic sweep circuit is shown in the integrator circuit of Fig. 6. Current entering the noninverting (+) input causes the output voltage to sweep linearly in a positive direction, and current entering the inverting (-) input causes the output to sweep negatively. The diode isolates the inverting input when the input voltage is zero. Either input can be used as a reset control, and the faster negative-going slew rate of the LM3900 generates excellent positive-going sawtooth waveforms with a very short reset time.

A sine-wave oscillator built round the LM3900 is shown in Fig. 7. The two-amplifier RC active filter requires only two capacitors to provide the proper over-all noninverting phase characteristic. If a noninverting gain-controlled amplifier is then added around the filter, the desired oscillator configuration is obtained. Finally, the sine-wave output voltage is sensed and regulated by a differential averaging circuit, so that its average value is compared to a dc reference voltage, V_{REF} .

The averaging circuit also provides a simple way to keep the peak magnitude of the output sine wave equal to twice the value of V_{REF} . This is essentially indepen-



7. Sine-wave oscillator. Four Norton amplifiers can easily be interconnected to make a sine-wave oscillator. A two-amplifier RC filter and a noninverting gain-controlled amplifier are added to a differential averaging circuit for regulation.



8. Slow sawtooths, too. The four amplifiers of the Norton quad work together to generate very slow sawtooth waveforms. To guarantee the required high impedance, the printed-circuit boards used with the packages should be coated with silicon to minimize surface leakage.

dent of both temperature and the magnitude of the power-supply voltage, provided V_{REF} is derived from a stable voltage source.

The LM3900 can also be used to generate a very slow sawtooth waveform, which can in turn be used to generate long time-delay intervals. This is one of the toughest circuit functions to obtain in IC form. The circuit shown in Fig. 8 uses four amplifiers. Amplifiers 1 and 2, which have the desired very slow sawtooth waveform output, are cascaded to increase the gain of the integrator, while amplifier 3 supplies the bias current to amplifier 1. Amplifier 4 provides a bias reference equal to the dc voltage at the (-) input of amplifier 3.

With resistor R_8 opened up and the reset control at zero volts, the potentiometer, R_5 is adjusted to minimize the drift in the output voltage of amplifier 2 (this output must be kept in the linear range to insure that amplifier 2 is not in saturation). The resistor divider, R_7 and R_9 , provides a 0.1-v dc reference voltage across R_9 that also appears across R_8 . The current that flows through R_8 enters the (-) input of amplifier 3 and causes the current through R_6 to drop by this amount. This causes an imbalance because now the current flow through R_4 is no longer adequate to supply the input current of amplifier 1. The net result is that this same current is drawn from capacitor C_1 and causes the output voltage of amplifier 2 to sweep slowly positive.

To guarantee obtaining the high impedance values needed for the slow sweeps, the printed-circuit board used must be cleaned and then coated with silicone rubber to eliminate the occurrence of leakage currents across the surface. Also, the dc leakage currents of the capacitor C_1 must be kept small compared to the 10-nA charging current. For example, an insulation resistance

of 100,000 megohms will leak 0.1 nA with 10 v dc across the capacitor—a leakage that increases rapidly at higher temperatures.

With the basic circuits, other sweep rates can be obtained by scaling resistor R_8 and capacitor C_1 . For the values shown in Fig. 9, the 10-nA current and the 1-microfarad capacitor establish a sweep rate of 100 seconds per volt. The reset control pulse at amplifier 3's (+) input causes that amplifier to go into positive output saturation, while the 10 megohms of R_4 provides a reset rate of 0.7 s/v.

The resistor, R_1 , prevents C_1 from discharging larger currents and thus from overdriving the (-) input and overloading the input clamp device. For larger charging currents, a resistor divider can be placed from the output of amplifier 4 to ground, and R_8 can tie from this tap point directly to the (-) input of amplifier 1.

Digital and switching circuits

A unique feature of the new Norton quad amplifiers is that they can be overdriven to provide a large number of low-speed digital and switching circuit applications. This is particularly attractive for control systems that operate from single power-supply voltages larger than the standard +5-v dc digital limit. The large voltage swing and slower speeds of the LM3900 are advantages for most industrial control systems. In this context each amplifier can be thought of as a super transistor with a β of 1,000,000 (25-nA input current and 25-mA output current) and with a noninverting input feature. In addition, the active pullups and pulldowns which exist at the output will supply larger currents than the simple resistor pullups used in digital logic gates. □