FAULT FINDING ON THE DH/DM and VMZ32 and VMZ32N

The DH/DM is a sophisticated micro-processor emulation of the DEC DH11 + DM11-BB.

The information contained here is intended to supplement chapter 3 of the DH/DM Users Guide and enable you to find faults and repair the DH/DM.

WARNING Unskilled personnel should NOT attempt to remove components from the DH/DM.

The board is multi-layer and can be damaged during removal of components unless care is taken.

The information is in two parts

A. Using Self-test to isolate a fault

B. Relating DEC DIAGNOSTIC ZDHM to DH/DM errors.

EVEN IF THE SELF-TEST DIAGNOSTIC PASSES, THE DH/DM MAY FAIL IN EMULATION. THEREFORE IT IS IMPORTANT TO TEST IT USING THE DEC DIAGNOSTIC - A SMALL MACHINE CODE PROGRAM IS INCLUDED FOR SITUATIONS WHERE THE DEC DIAGNOSTIC IS NOT AVAILABLE..

90% of errors in the ABLE DH/DM will be found to be caused by chips which transmit or receive data, either on the UNIBUS or as EIA data. The remaining 10% of failures can often be found by using the checklist provided below.

The micro diagnostic contained in the DH/DM proms will show most failures as a code in the LED display lamps ERR,1,2,and 3.

DIAGNOSTIC LED EROR REPORT	LIKELY AREA OF FAILURE	TYPICAL % OCCURENCE	OPTION TO USER
UART	UART OR TRANSMIT OR RECEIVE EIA LOGIC	90%	FOLLOW REPAIR PROCEDURE AND CHANGE CHIPS
BUS (NPR,BR)	U27 OR U54 PAL CHIP	8%	CHANGE CHIPS OR RETURN TO ABL
SEQ DATA DBIT PROM BUFF	MICRO ENGINE RAM OR STEERING LOGIC	2%	RETURN TO ABLE FOR REPAIR

CONTD....

NOTE THAT UART/MODEM CONTROL errors are also caused by damaged cables. Also, if the cables are inserted 180^{o} round this will give errors and will damage the $\pm$ 15V diodes if the distribution panel is a 20mA loop version.

SELF TEST PROCEDURE

EQUIPMENT REQUIRED:

ABLE DH/DM + DISTRIBUTION PANEL + CABLES
PDP11 CPU WITH 64 KB MEMORY

OSCILLOSCOPE

REPLACEMENT CHIPS U27 PART NO 347-600-100
U25 PART NO 347-600-086

EXTENDER BOARD FOR DH/DM

SET UP METHOD:

SET SWITCHES ON DH/DM

SW6-1 CLOSED
SW5-1 CLOSED
SW5-2 OPEN
SW4-6 OPEN
SW4-7 OPEN

ATTACH DATA CABLES AND CONNECT TO J7,J8, ON THE ABLE DISTRIBUTION PANEL

SWITCH ON POWER

LOAD ADDRESS 00000 IN THE UNIBUS MEMORY, DEPOSIT DATA 000777

START EXECUTION OF PROGRAM AT 0

CPU WILL BRANCH SELF

OPEN SW5-1 AND CLOSE SW5-1 AGAIN

DETERMINE FROM LED DISPLAY ON DH/DM

IF THE ERR LAMP IS LIT

REPEAT PROCEDURE WITH SW4-6 CLOSED SW4-7 OPEN
AND SW4-6 OPEN SW4-7 CLOSED

DETERMINE IF ERR LAMP LIGHTS UNDER ANY CONDITION. NOTE: CPU MUST EXECUTE BRANCH SELF.

DISPLAY				DESCRIPTION
ERR	1	2	3	
off	off	off	off	END PASS / EMULATION
off	off	off	on	Testing Section 1 - DBIT
off	off	on	off	Testing Section 2 - UART
off	off	on	on	Testing Section 3 - DATA (2901)
off	on	off	off	Testing Section 4 - BUF
off	on	off	on	Testing Section 5 - PROM
off	on	on	off	Testing Section 6 - BUS (NPR, BR)
off	on	on	on	Testing Section 7 - SEQ
on	off	off	off	Error - Undefined problem
on	off	off	on	Error in Section 1 - DBIT Error
on	off	on	off	Error in Section 2 - UART Error
on	off	on	on	Error in Section 3 - DATA (2901) Error
on	on	off	off	Error in Section 4 - Error BUF
on	on	off	on	Error in Section 5 - Error PROM
on	on	on	off	Error in Section 6 - Error BUS
on	on	on	on	Error in Section 7 - SEQ Error

ERRORS OF THE TYPE DBIT, DATA, BUF, PROM AND SEQ REQUIRE MORE SPECIALISED TEST EQUIPMENT. RETURN THESE FAILURES TO ABLE SUPPORT FOR REPAIR. HOWEVER 90% OF FAILURES WILL BE UART OR BUS.

BUS ERRORS

IF THE PREVIOUS TEST SEQUENCE HAS SHOWN A BUS ERROR DETERMINE IF IT IS CAUSED BY BR-BUS TEST (SW4-6) OR NPR-BUS TEST (SW4-7)

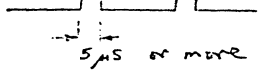
ALWAYS SWITCH OFF POWER BEFORE REMOVING ANY BOARD OR COMPONENT

BR-BUS TEST ERROR

1. IF CLOSING SW4-6 CAUSES A FAILURE CHECK THAT THERE ARE NO MISSING BUS GRANT CARDS IN THE BACKPLANE
2. REPLACE U27 WITH A KNOWN GOOD CHIP, TAKING CARE NOT TO BEND ANY PINS ON REMOVAL OR INSERTION. DO NOT INSERT CHIP UPSIDE DOWN! AND RE-TEST.
3. REPLACE U54 WITH A KNOWN GOOD CHIP AND RE-TEST.
4. IF REPLACING U27 AND U54 DOES NOT SOLVE THE PROBLEM THEN AFTER CHECKING THAT THE CPU IS STILL EXECUTING BRANCH SELF.....
5. OPEN SW5-1 WHILE THE MACHINE IS LIVE

THE ERROR LAMP WILL REMAIN ON BUT THE SELF-TEST WILL CONTINUE TO RE-TRY THE BR TEST.

6. MONITOR THE FOLLOWING POINTS WITH AN OSCILLOSCOPE, IF THE BR TEST IS FAILING YOU WILL SEE PULSES LIKE THIS :



5μS or more

A GOOD SEQUENCE IS :

DRAWING SET PAGE	CHIP NO + PIN NO	COMMENTS
16	U53-7	XBRA-H SEND BUS REQUEST "A"
19	U68-4	BUS-BRA-L = BR5 UNIBUS SIGNAL
21	U74-5	BGIA-H = BG5 UNIBUS SIGNAL
21	U74-3	RBGA-L = BG5 BUFFERED
16	U66-16	SBGA-L = BG5 STATICISED
20	U54-12	XBBSY) NOT NECESSARY FOR
	U54-13	XGRNT) SELF TEST AS THE
	U54-14	XSACK) INTERRUPT NEVER
	U54-18	BRAI) COMPLETED, BUT THE
19	U9-15	SACK-L) SIGNALS SHOULD BE VISIBLE

IF A SIGNAL IS PRESENT ON ONLY ONE SIDE OF A CHIP THEN THE CHIP IS PROBABLY FAULTY. CAREFULLY REMOVE CHIP FROM MULTI-LAYER BOARD - ONLY SKILLED PERSONNEL SHOULD ATTEMPT THIS - REPLACE CHIP - FOR FUTURE THERE SHOULD BE A RECORD MADE OF ALL CHIP CHANGING TO BOARD AND A COPY SENT TO ABLE IF THE BOARD IS RETURNED FOR REPAIR.

NPR - BUS TEST ERROR

1. IF CLOSING SW4-7 CAUSES A FAILURE CHECK THAT THERE ARE NO NPG-GRANT LINKS MISSING FROM THE UNUSED BACKPLANE SLOTS AND ALSO THAT THE GRANT LINK IS REMOVED FROM THE SLOT USED FOR THE DH/DM.
2. EXAMINE THE FOLLOWING LOCATIONS IN UNIBUS MEMORY. THE NPR-TEST WRITES DATA INTO MEMORY, AND CHECKS CONTENTS - FAILURE IN TEST MAY BE DUE TO A DATA ERROR.

LOCATION	CONTENTS	DATA=ADRS
2	2	D1
4	4	D2
10	10	D3
20	20	D4
40	40	D5
100	100	D6
200	200	D7
400	400	D8
1000	1000	D9
2000	2000	D10
4000	4000	D11
10,000	10,000	D12
20,000	20,000	D13
40,000	40,000	D14
100,000	100,000	D15

3. THERE ARE SOME POSSIBILITIES

   A - ALL DATA IS CORRECT BUT TEST STILL FAILS
   B - BAD DATA IN ONE OR MORE LOCATIONS
   C - ALL DATA IS BAD

4. A) IF THE DATA IS CORRECT BUT THE TEST FAILS - THERE MAY BE A FAILING CHIP ON DATA BEING READ BACK INTO THE DH/DM - SEND THE BOARD BACK TO ABLE SUPPORT BECAUSE THIS REQUIRES MORE TEST EQUIPMENT.

   B) IF ONE LOCATION HAS BAD DATA YOU MAY SUSPECT EITHER THE BUS DRIVER CHIP FOR THE ADDRESS OR FOR THE DATA - REPLACE CHIP TAKING CARE NOT TO DAMAGE THE BOARD AND RE-TEST

ADDRESS	CHIP	DATA	CHIP
A00-A03	U33	D00-D03	U81
A04-A07	U32	D04-D07	U87
A08-A11	U45	D08-D11	U94
A12-A15	U39	D12-D15	U97

C) IF ALL DATA IS BAD YOU MAY SUSPECT THE SIGNALS NPR, NPG, SACK BBSY, MSYN AND SSYN AND CO,C1

NOTE, THAT SINCE THE CPU IS EXECUTING A BRANCH SELF THE SIGNALS MAY BE CONFUSED - THIS DOES NOT MATTER. XMSYN IS ONLY SET BY DH/DM WHEN ACCESSING MEMORY. RSSYN WILL CONFIRM IF BUS-SSYN IS PROPAGATED I.E. IF NO RSSYN AT ALL THEN U63-14→15 FAILED.

5. REPLACE U27 AND/OR U54 AS THE NEXT STEP. RE-TEST AND DECIDE IF THE FAULT IS THE CHIP.
6. OPEN SW5-1 WHILE THE MACHINE IS LIVE, THE NPR SELF TEST WILL CONTINUE TO RE-TEST, MONITOR THE FOLLOWING POINTS USING AN OSCILLOSCOPE

DRAWING SET PAGE	CHIP NO + PIN NO	COMMENTS
16	U53-5	XNPR SEND NPR REQUEST
19	U9-1	BUS-NPR = NPR UNIBUS SIGNAL
21	U74-12	BUS-NPG = NPG UNIBUS SIGNAL
21	U74-13	RNPG = NPG BUFFERED
16	U66-19	SNPG = NPG STATICISED
20	U54,12,14	SACK,BBSY SEND SACK,BBSY
	U54,15,17	DMAI DMA IN PROGRESS
16	U53-9	XMSYN = SEND MSYN TO MEMORY
16	U63-13	RSSYN = SSYN BUFFERED
16	U66-2	SSSYN = SSYN STATICISED
16	U42-15	SBBSY = BBSY STATICISED
19	U9-15	SACK = SACK UNIBUS SIGNAL
19	U9-12	BBSY = BBSY UNIBUS SIGNAL

MICRODIAGNOSTIC CONTINUES TO RE-TEST. MONITOR FOLLOWING POINTS WITH AN OSCILLOSCOPE.

MONITOR	-SIDE	+SIDE	
CR2	-12v	-15v	CR2 BY U83
CR3	+12v	+15v	CR3 BY U87

CHANNEL

	0	1	2	3	ETC
RECEIVED DATA	U89-3	U90-3	U91-3	U92-3	
TRANSMIT DATA	U89-19	U90-19	U91-19	U92-19	
RECEIVED RING	U89-22	U90-22	U91-22	U92-22	
TRANSMIT RING	U89-24	U90-24	U91-24	U92-22	

IT THESE SIGNALS AND THOSE FOR CHANNEL 0-15 ARE OK THEN ANY UART FAILURE IS ON THE SELECT AND D-BUS WHICH IS TOO COMPLEX TO FAULT FIND HERE - RETURN TO ABLE FOR REPAIR.
IF THERE IS NO TRANSMIT DATA FOR A SINGLE UART, THEN CHANGE THE UART.
IF THERE IS NO TRANSMIT DATA FOR ANY UART THEN RETURN BOARD TO ABLE.
IF THERE IS NO RECEIVED DATA FOR A SINGLE UART THEN FOLLOW THE MONITOR POINTS LISTED BELOW.

ONLY CHANNEL ZERO SHOWN

DRAWING SET PAGE	CHIP NO + PIN NO	COMMENTS
32	U89-19	SD00 SERIAL DATA OUT
32	U89-24	DTR00 DTR OUT
36	U88-10	BRK00 BREAK SHOULD ALWAYS BE HIGH DURING SELF TEST
36	U88-8	TXD00 +15v EIA TRANSMIT DATA
37	U77-6	SDI00 RECEIVED DATA (TTL)
32	U89-3	SDI00 RECEIVED DATA AT UART
40	U88-3	DTR00 +15v EIA DTR
39	U98-3	RING00 RECEIVED DTR= RING

WHEN TXD $\pm$15V EIA IS MONITORED THE SIGNAL SHOULD BE AT LEAST +6V AND -6V SIMILARLY DTR +15V EIA SHOULD BE MINIMUM $\pm$6V.
IF THE SIGNAL IS MISSING OR FAILS TO GO POSITIVE AND NEGATIVE, REMOVE THE CABLES FROM THE BOARD AND MONITOR TXD AND DTR AGAIN. IF THE SIGNAL IS NOW GOOD, REPLACE THE EIA RECEIVER FOR THAT SIGNAL. (U77 or U98 IN CHANNEL Ø) THIS IS BECAUSE A DAMAGED RECEIVER CHIP (1489) CAN DRAG DOWN TRANSMIT SIGNAL.

IF THE SIGNAL BRK (U88-10 IN CHANNEL Ø) IS SEEN TO PULSE OR FOLLOW THE TRANSMIT DATA, THEN THE UART IS FAULTY.

TEST USING DEC DIAGNOSTIC

THE DH/DM EMULATION WILL RUN DEC DIAGNOSTIC ZDHM??
WITHOUT MODIFICATION
A SAMPLE PRINTOUT IS GIVEN BELOW

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.R ZDHM??

SWR = 000000  NEW=104002
CZDM-D-0      DH11 DIAGNOSTIC
DH11, MODEM CONTROL MAP

DH11          DH11        MODEM          MODEM
ADRS          VECT        ADRS           VECT
160020        340         170500         300

TESTING DH00
END PASS 1
TESTING DH00
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NOTE: SWR=104002 GIVES HALT ON ERROR/QUICK PASS/PRINT DH-DM ADRS, VECTORS.

ERROR MESSAGES	SIGNIFICANCE
NO DH'S FOUND	NO SSYN FROM ANY DH, U54 FAILURE OR EMULATION FAILURE CHECK IF ERR LED IS LIT.
DH REGISTER TIMEOUT XX REGISTER ERROR	DATA/ADRS BUS DRIVER FAILURE OR MICRO-ENGINE RAM ERROR - RETURN TO ABLE
STORAGE OVERFLOW BIT FAILED LINE nn	IF ONLY ONE CHANNEL FAILS -DIA ERROR OR UART ERROR. IF ALL CHANNELS 0-7 or 8-15 CABLES MAY BE INSTERTED BACKWARDS, CHECK DIODES CR2/CR3 MAY BE DAMAGED
UART TRANSMIT/RECV TIMING ERROR	UART IS FAULTY - IF FAILURE IS FOR SPEED 6 OR SPEED 7 CHECK SW3, SW4, SET FOR 200 BAUD
TIMEOUT WAITING FOR XMIT DONE LINE nn	NPR IN U54 IF ALL LINES FAIL, UART FAULT IF ONLY ONE LIN
MODEM CONTROL ERROR RUN ZDHK	DM ERROR RING/DTR EIA ERROR - CHECK IF SW4-2 IS CLOSED!!