LH-DH/11.MM.PVØØ7-B
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JNC

LOCAL/DISTANT HOST CONTROLLER

Model Numbers LH-DH/11C and LH-DH/11B

MAINTENANCE MANUAL

VOLUME I

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CHAPTER 1

INTRODUCTION

CHAPTER 1

1.0 INTRODUCTION

1.1 Technical Manual Contents - This manual contains information on the application, maintenance, and operation of a network interface controller referred to as the LH-DH/11. The LH-DH/11 controller is used to provide the interconnection between a Digital Equipment Corporation PDP-11 computer system and an Interface Message Processor (IMP) on an ARPA-Style computer telecommunications network.

1.2 Technical Manual Organization - The LH-DH/11 Technical Manual is divided into three volumes as follows:

Volume I - Details of Programming and Interface Operation. Includes Installation Instructions, Cable Diagrams, and References.

Volume II - Logic Layouts, Logic Diagrams, and Parts List.

Volume III - LH-DH/11 Diagnostic Program Description.

1.3 Technical Manual Reference Notes - The text and diagrams in this manual, plus information included in the referenced material, are sufficient to understand, check-out, modify, and maintain the controller. If modifications are made, the appropriate wire list, logic diagram, and other manual entries must be updated. The following paragraphs clarify some reference notations:

1.3.1 All Sockets 16 Pin - All sockets for integrated circuits used in the controller are of the 16-pin variety and all references to pin numbers in diagrams are on a 16-pin basis. The documentation within the manual, including equations and layout sheets, are consistent in this numbering system.

1.3.2 Logic Level Indicator -The voltage level of a given logical name (signal) is conveyed by the name itself. If a given logical element is "asserted" ("true", "set", etc.) then the voltage level of its output is reflected in the name as follows: the logical name EDD represents a signal that will reside at a plus (+) level when the LH-DH/11 is to place data on the Unibus. Alternately, the logical name and signal, EDD- will reside at 0 volts for the same condition. A bar (-) following a logical name implies that it resides at ground level when the circuit is asserted.

1.3.3 Ground Notation - Throughout the manual, the notation of a bar (-) following a logical name is identically equal to a bar over the logical name (IRQ≡$\overline{\text{IRQ}}$).

1.3.4 Mil-Standard Symbols - The logic symbols employed in the diagrams are according to Mil-Standard.

1.3.5 Localized Ground Signals - The grounded input to circuitry is specified in the logic diagrams as GRN-. All circuit grounds within the system are localized to the socket into which the circuit is plugged. For example, the ground for the IC socket is made by a solder clip on pin 7 (or 8) as dictated by the circuit itself. Any other grounded terms on a given IC are provided by wired jumpers emanating from that ground clip.

1.3.6 Coordinate References - On the logic diagrams, the location in the diagrams for the source of a given signal is indicated by a coordinate reference. For example, 05B3 indicates Drawing Number 5, coordinate B3 (See 7.1).

1.4 Interface Application - The LH-DH/11 is a full-duplex Direct Memory Access (DMA) controller that attaches to a DEC PDP-11 Unibus and provides external communication according to BBN Specification #1822.* Figure 1-1 is an overall block diagram showing the LH-DH/11 connected between the PDP-11 Unibus and the IMP. By means of plug-in circuits interchange the controller can be used for Local Host (30' cable limit) or Distant Host (2000' cable limit) application.

*BBN=Bolt Beranek and Newman, Inc., Report #1822, "Specification for Interconnecting a Host and an IMP".

1.5 Interface Organization - The logic for the LH-DH/11 is separated into two sections as shown in Figure 1-1. The first section deals with the input from the IMP and the other section deals with the output to the IMP. Each section has its own wire-wrapped logic panel with plug-in components and cable connectors.

1.6 Interface-Unibus Interconnection - Interconnection to the Unibus is by means of an adaptor plug at the rear of the Input panel.* Both the Input and the Output sections provide for data transfer on a Director Memory Access (DMA) basis, that is, once the controller is started by the program within the processor it moves information into and out of the core memory without involving the programmed I/O within the processor. It is only upon completion of a data transfer that the programmed I/O is alerted so that subsequent transfers can take place and so that errors can be accommodated.

1.7 Interface-IMP Interconnection - Connection to the IMP is by means of an externally mounted MS receptable that connects to the Output panel by way of a short cable and I.C. socket plug. A set of 10 signal lines interconnect the IMP and the LH-DH/11. Four of these are used for data transfer into the LH-DH/11 Input section and four to transfer from the Output section to the IMP. The remaining signal lines are used to indicate the operational status of the LH-DH/11 or the IMP.

1.7.1 Bit Serial Transfer on IMP Connection -Of the four signal lines used for transfering data to the IMP from the LH-DH/11 (and the four used for transfer from the IMP), one line is used for data bits, two lines "handshake" to bring about the transfer, and one line identifies the presence of the last bit to be transferred.

1.8 Interface Maintenance Feature - Since data transfer to and from the IMP uses an identical set of four signal lines, maintenance testing of the LH-DH/11 is made easier by the "Bus-Back" connection of the Output section to the Input section. Data may be transferred in this fashion internally, under diagnostic program control, or externally by replacing the IMP cable with a wired-back connector.

* On the LH-DH/11B, or "B" version, the Unibus cable connection is made through a free-standing block and signals are conducted to both the Input Section and the Output Section by separate cables (See Figure 3-2).

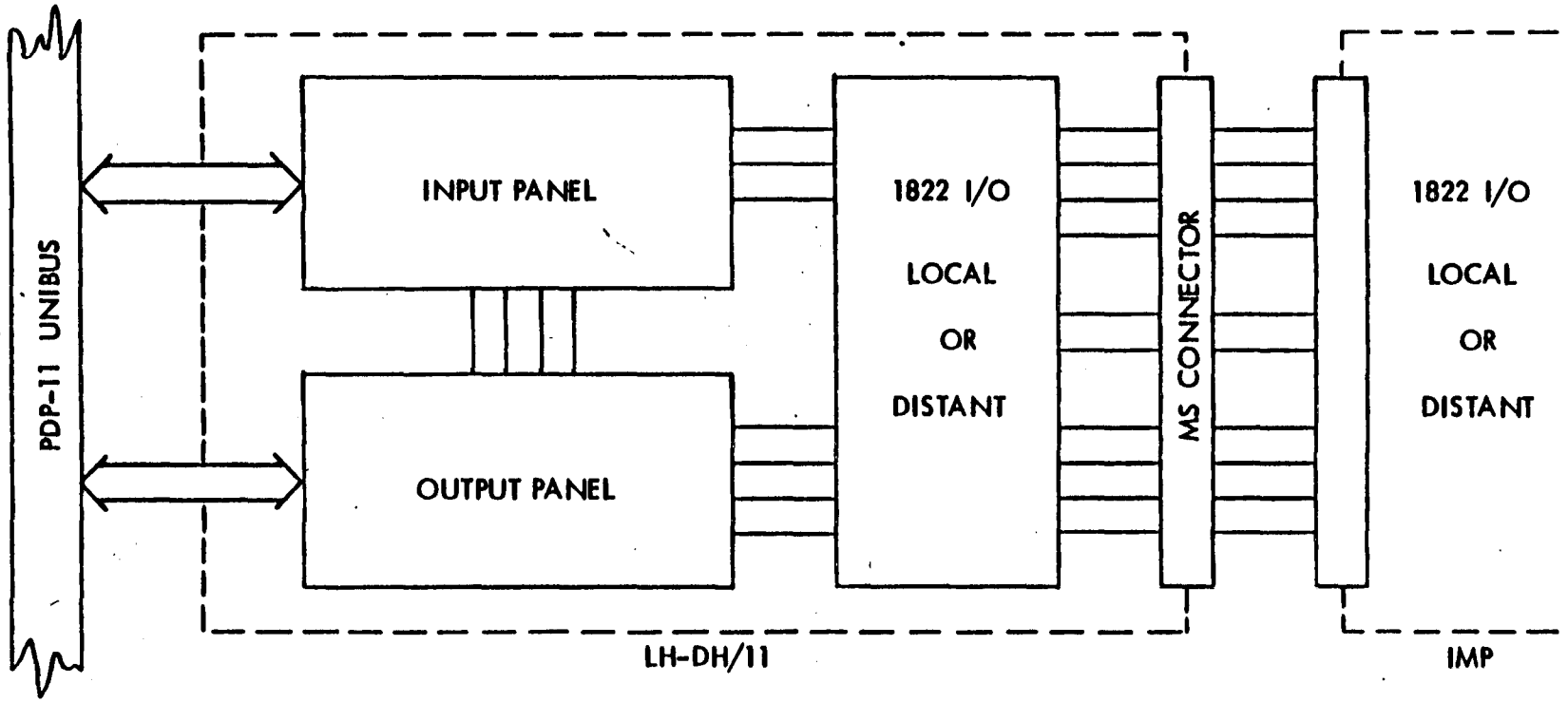

Figure 1-1 OVERALL BLOCK DIAGRAM

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CHAPTER 2

REFERENCES

CHAPTER 2

2.0 REFERENCES

2.1 Reference Documents - Certain support documents may be utilized for LH-DH/11 users, programmers, and maintenance personnel. These are summarized below:

2.1.1 Digital Equipment Corporation Documents

PDP-11 Programming Handbook
PDP-11 Peripherals Handbook

2.1.2 Bolt Beranek and Newman Inc.

Report Number 1822 "Specifications for Connecting a Host and an IMP"

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CHAPTER 3

INSTALLATION CONSIDERATIONS LH-DH/11

CHAPTER 3

3.0 INSTALLATION CONSIDERATIONS LH-DH/11

3.1 Common Requirements for "C" and "B" Versions - The following paragraphs obtain when planning installation of either version.

3.1.1 Physical Dimensions - The LH-DH/11 is manufactured on two machine wire-wrapped planes mounted within a single, rack-mounted unit. The controller occupies 10.5 inches of vertical rack space when mounted in a PDP-11 standard cabinet. Chassis slides are provided for ease in maintenance.

3.1.2 Primary And Logic Power - The LH-DH/11 contains its own +5 volt power supply. Primary power is brought to the rear of the chassis by means of a standard, removable, power cord. The unit requires 3 Amperes of 50-60 Hz, 120 vac primary power. It is expected that the LH-DH/11 will be powered through the DEC Switched power source.

3.1.3 External Connection - Figure 3-1 illustrates the rear panel of the LH-DH/11 "C" version. The rear of the "B" version is configured differently; however, the features are the same. The following paragraphs describe external connections.

3.1.3.1 IMP Connection - The LH-DH/11 is connected to an IMP in either a Local or a Distant Host made by means of the 31-pin connector labeled "IMP" (See Figure 3-1).

3.1.3.2 Logic Power Output - The connector labeled "+5v" is used so that an external device such as ACC's BT-11 * can be powered. Several Amperes of this +5 vdc logic power are available.

3.1.3.3 Primary Power Connector - AC power is connected to the LH-DH/11 through this receptacle.

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* The BT-11 is a device that allows a system "Boot" to be made. In the Front End Processor application the BT-11 is mounted in a separate, unpowered, frame that requires +5 vdc.

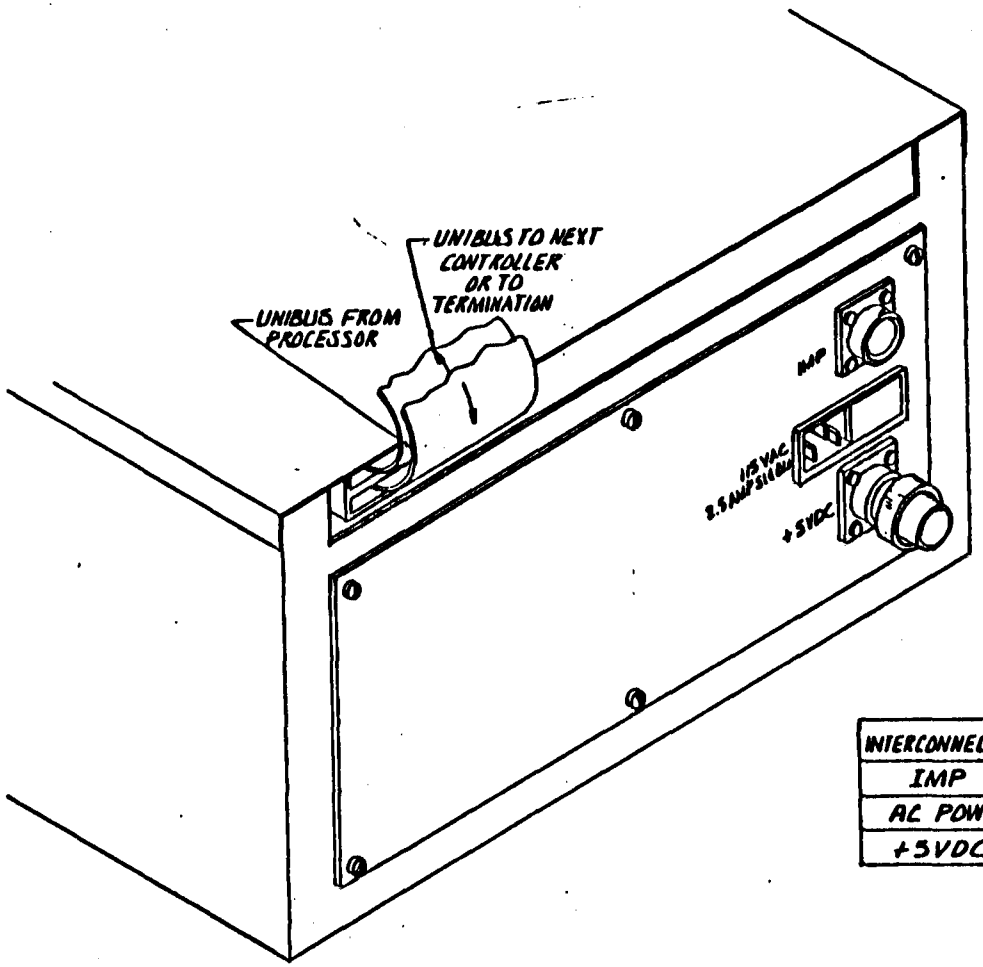
3.2 Unibus Attachment - Figure 3-2 illustrates the location where Unibus connection takes place in the LH-DH/11C, and the LH-DH/11B. The primary difference between the two versions is the method of attaching the Unibus. In the "C" version the cables are brought directly to an adaptor plug which inserts into the Input Panel. In the "B" version the cables are inserted into a separate connector block from below and wires are brought to each plane separately through twisted pair cables.

3.3 Device and Vector Address Set-Up - In order to operate the LH-DH/11 each section must have its unique Device Address and Interrupt Vector Address. In the "C" version, switches are used. In the "B" version, Jumper platforms are used. See Volume II, page 4 for Output (Transmit) and page 10 for Input (Receive). Also review Volume I, Sections 4.7, 4.8, 4.9, 4.10, 6.5, and 6.6.

3.4 Pre-Set Address and Interrupt Parameters - The following list specifies the addresses and interrupt priority selections that are pre-set during final testing of the LH-DH/11 prior to shipment (See reference in 3.3).

Address for Interrupt - Input (Vector) = 270
Address for Interrupt - Output (Vector) = 274
Priority for Interrupt Requests = Priority 5
Addresses (Octal) for LH-DH/11 Registers (See Programming - Chapter 5)

767600	Control & Status Register - Input (CSRI)
767602	Data Buffer Register - Input (DBRI)
767604	Current Word Address Register - Input (CWAI)
767606	Word Count - Input (WCI)
767610	Control & Status Register - Output (CSRO)
767612	Data Buffer Register - Output (DBRO)
767614	Current Word Address Register - Output (CWAO)
767616	Word Count - Output (WCO)

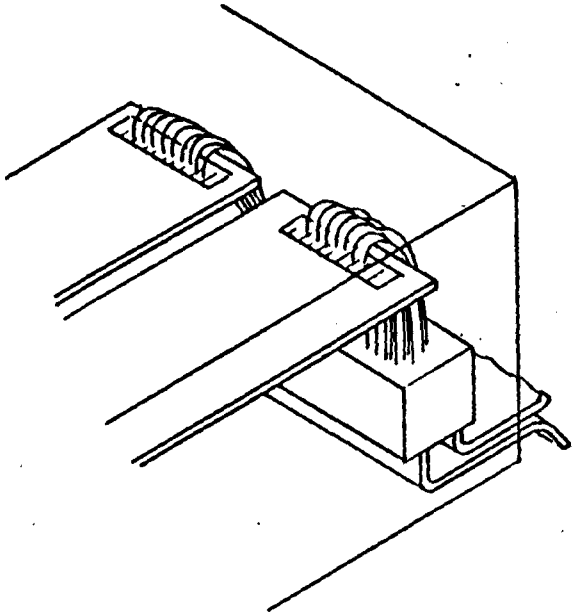


INTERCONNECTION	PANEL MOUNTED PART NO.	CABLE CONNECTOR PART NO.
IMP	48-10R18-31S AMPHENOL	48-16R18-31P AMPHENOL
AC POWER	CORCOM 6J1	C-3170-008-BL PACIFIC ELECTRO CORD CO.
+5VDC	WR5-31SL CANNON	WR-5-27C-5/16 CANNON

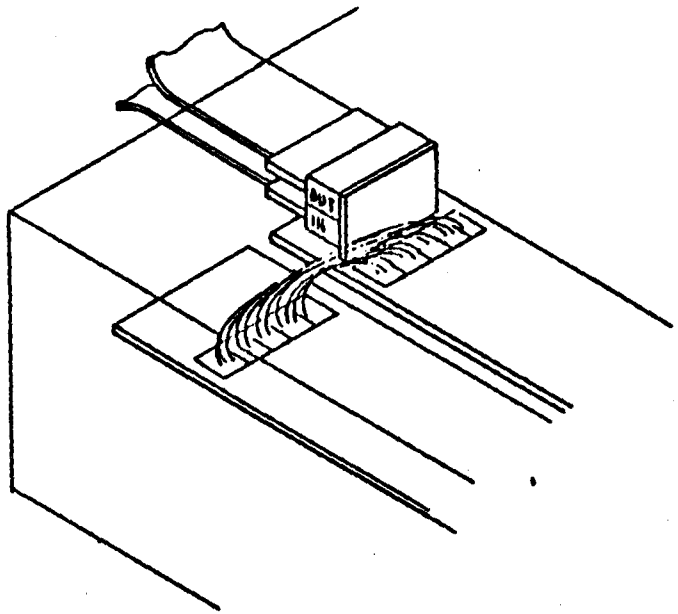
FIGURE 3-1 REAR PANEL LH-DH/C3

	A	B	
	UNIBUS CABLE –	FROM PROCESSOR	1
			2
REAR OF CABINET			3
	UNIBUS CABLE –	TO TERMINATION	4

	A	B
1	UNIBUS CABLE	TO TERMINATION
2	UNIBUS CABLE	FROM PROCESSOR



B VERSION



C VERSION

FIGURE 3-2 UNIBUS INTERCONNECTION

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CHAPTER 4

GENERAL DESCRIPTION

CHAPTER 4

4.0 GENERAL DESCRIPTION

4.1 Packaging - The LH-DH/11 is packaged on two machine wire-wrapped planes that are enclosed within a standard DEC 19" mounting box. The mounting box is equipped with chassis slides and is intended for installation within a DEC PDP-11 cabinet. Integrated circuits are plugged into the sockets in these planes.

4.1.1 Separate Controllers - The Input Controller occupies one of the planes and the Output Controller the other. The only common logic is the synchronizing clock for operating the active elements within the two controllers. This clock is crystal controlled with its fastest rate at 16 MHz.

4.2 Interconnection - The cable that connects the IMP to these two controllers is brought into a connector which is located at the rear of the chassis. Connection to the PDP-11 Unibus is by means of a Unibus cable brought into the box through a slot in the rear. In the C version this cable is plugged into a special adaptor plug located on the Input panel. In the B version twisted pair wiring brings the UNIBUS signals to the driver and receiver circuits on the Controller planes from a connector block (See Figure 4-1 and Figure 3-2).

4.3 Input Controller Operation - The Input Controller is responsible for moving a serial data stream from the IMP into the memory of the PDP-11 computer. In order to do this, the program within the computer must first establish a location within the memory into which the data can be transferred. Once this is done the program issues a command to the controller to begin the receiving process.

4.3.1 IMP to LH-DH/11 Signal Lines - The IMP provides the Input Controller with a single data line upon which a series of data bits appear in a serial manner, a control line to indicate the presence of the data bit, and a control line which indicates when it is the last data bit.* Only one signal line is returned to the IMP and this indicates that the Input

* See Figure 7-3

Controller has "taken" the data bit. Each bit is transferred by means of the interlocking action of the two control lines. When the Input Controller raises the "Ready for Next Bit" signal, the IMP places the next data bit onto the data line and raises the "There's Your Next Bit" signal. This interchange creates a "Shift" pulse within the Input Controller. The pulse causes the Input Shift Register to load the data bit. After 16 shifts, the shift register is full and its contents must be transferred to the Input Buffer Register.

4.3.2 Last Bit In - The data input operation continues until the IMP raises the "Last Bit" signal line in coincidence with presentation of the data bit. This will normally occur on a 16-bit boundary, but if not, the shift register will fill in with "0" bits until 16 shifts have taken place.

4.4 Major Active Logic Elements - Input Controller - The major active elements of the Input Controller are shown in Figure 4-2 and are described below:

4.4.1 IMP Drivers and Receivers - This circuitry is used to convert the signal levels on the cable to the logical levels used within the Input Controller.

4.4.2 Shift Interlock Circuitry - This circuitry controls the transfer of data bits from the IMP cable.

4.4.3 Input Shift Register - This 16-bit register is used to accumulate the bits that constitute a PDP-11 word. Once 16 bits are present within the shift register, they are transferred to the Input Buffer Register.

4.4.4 Bit Counter - This counter overflows at 16 counts and is used to determine when the Input Shift Register is full. Upon overflow, a load pulse is sent to the Input Buffer Register to cause the shift register contents to transfer.

4.4.5 Input Buffer Register - This register is 16 bits in length. When the Input Shift Register contains 16 bits they are transferred to the Input Buffer Register. This transfer only occurs, however, if the buffer register is empty. If the previous contents have not been placed in memory, the shifting process halts. No data is lost since the serial transfer is completely interlocked. Once a word is stored in memory the transfer resumes.

4.4.6 Memory Address Register - This register is also referred to as the Current Word Address Register (CWA) and contains the address of the location in core into which a data word is to be placed. The contents of this register are set up by the program within the processor and are incremented each time a data word is placed into storage. Successive data words are placed in successive locations within storage.

4.4.7 Word Count Register - This incrementing register keeps track of the number of incoming words inserted into storage. The program initially sets a 2's complement value into this register and this value is incremented until the word count is equal to 0 (WC = 0) or until the last word from the IMP is transferred to memory. An interrupt informs the program within the PDP-11 that completion has occurred. If WC = 0 happens before a complete transfer has taken place, the program is required to set up additional storage area or to "flush" the remaining data by setting an appropriate bit in the Control and Status Register.

4.4.8 Control and Status Register - This register contains "function" bits that control operations and "flag" bits that are used to indicate Status. This register can be read at any time by the program, but most particularly upon completion of an incoming data transfer, at which time the Input Controller interrupts the program.

4.4.9 Control State Counter - The state counter is responsible for sequencing all the operations within the Input Controller. This counter advances from state (0) during which the controller is in an "inactive" mode; to state (1) which tests the WC ≠ 0 and Input Buffer Full; to state (2) which causes the DMA transfer to storage. The (1) - (2) - (1) .... action takes place until completion of an entire block of data words. Upon completion (WC = 0) the state counter goes to (0) and interrupts the PDP-11 program.

4.4.10 Slave Control and Address Decode - This control logic comes into operation during the time that the program within the processor is directing, or initializing the Input Controller. The controller address is decoded from the address bus out of the central processor; the logic assumes the "slave" condition whereby it accepts commands from the computer program. Commands include the setting of the Control and Status Register, the Memory Address Register, and the Word Counter.

4.4.11 Data Bus Multiplexor - This set of logic "gates" any one of four sources to the driver circuits of the data bus into the processor or its memory. The sources include the Word Counter, the Input Buffer Register, the Control and Status Register, or the Memory Address Registers.

4.4.12 Unibus Drivers and Receivers - These circuits connect the Input Controller logic to the data, address, and control signals of the processor Unibus.

4.4.13 Fixed Interrupt Address - This address is used at the time an interrupt is presented to the program in the processor. It specifies a dedicated location within memory that contains the interrupt sequence. The address can be changed according to the requirements of a particular site, by changing jumpers on the platform provided (See Sections 4.9).*

4.5 Output Controller Operation - The Output Controller is responsible for transferring data from the memory of the PDP-11 to the IMP. Data words are obtained by Direct Memory Access, after the program within the processor has initialized the Output Controller. These 16-bit words are placed in the Output Buffer Register for subsequent transfer into the Output Shift Register.

4.5.1 LH-DH/11 to IMP Signal Lines - The Output Shift Register produces a serial bit-stream in response to a "shift" clock, and these bits are sent to the IMP by way of a single data line. The shift clock is produced by the action of a pair of control lines, one of which indicates the presence of a new data bit and one which indicates that the bit has been taken. The action is completely interlocked since the IMP raises the line that indicates "Ready for Next Bit" and the Output Controller raises its "There's Your Host Bit" signal when a new data bit is placed on the data line. By dropping the Ready for Next Bit signal, the IMP indicates that it has "taken" the bit. This line is not raised again until the Controller drops its companion signal. After 16 shifts, the next word is transferred into the Shift Register. This action continues until the Word Count goes to zero (WC = 0), at which time the processor is interrupted.

4.5.2 Resuming an Output Message - The program may cause the transfer of a given message to resume, starting with a subsequent data block, without the IMP knowing that there has been a re-start. In this way, a "gather" from various locations in storage can be accomplished.

* Switches are used for this purpose in the C version (See Volume II, Page 10).

4.5.3 Last Bit Out - When the last block of a given message is being transferred, the I/O program must set a flag in the Control and Status Register to cause the "Last Bit" signal to be sent to the IMP in coincidence with the placing of the last data bit on the data line. This is sent on the fourth signal line to the IMP.

4.6 Major Active Logic Elements - Output Controller - The major logical elements within the Output Controller are illustrated in Figure 4-3. A discussion of these major elements follows:

4.6.1 IMP Drivers and Receivers - This circuitry is used to convert the levels required for external connection into levels that are useful to the internal logic of the Output Controller. The data signal driver is fed from the Output Shift Register.

4.6.2 Shift Interlock Circuitry - This circuitry controls the transfer of data bits to the IMP cable.

4.6.3 Output Shift Register - This register is 16 bits in length and is loaded from the Output Buffer Register. The load pulse occurs when the Shift Register is empty and the Output Buffer Register is full.

4.6.4 Bit Counter - This counter overflows at 16 counts and is used to determine when the Output Shift Register is empty. Upon overflow, a clear pulse is sent to the Output Buffer Register to allow the shift register to be loaded.

4.6.5 Output Buffer Register - This 16-bit register is loaded directly from the memory of the processor each time the Output Controller is ready to accept a new data word. A "flag" is used to indicate that the Register has been loaded. This flag is reset upon transfer of the Data-word to the Output Shift Register.

4.6.6 Memory Address Register - This register is loaded after the program establishes the data block within core that will be used for transmission. This register and the Word Count Register are loaded so that the controller knows where in the core memory the data resides and how long the data block is. The Memory Address Register is incremented each time a data word is taken from memory. It is sometimes referred to as the Current Word Address Register (See Programming - Chapter 5).

4.6.7 Word Count Register -The word counter is loaded by the program to control the length of the data block to be sent. When the word counter increments to 0 (2's complement) the Output Controller interrupts the I/O program so that a subsequent block can be sent. The last block of data is identified by a status bit and when set, the Output Controller completes the transfer to the IMP with a "Last Bit" indication.

4.6.8 Control and Status Register - This register is loaded by the program or by the Output Controller. At the time the transmission is to begin, the "Go" bit is pulsed by the I/O program. If an error occurs, a flag is set in this register that will alert the program when the output is completed.

4.6.9 Control State Counter - This counter is responsible for all of the sequences that take place within the Output Controller. This counter begins in State (0), which is maintained until the "Go" bit is pulsed to move it into State (1). State (1) tests the Output Buffer Register Loaded flag and holds until it is empty. If the Register is empty, State (2) is entered. State (2) requests a DMA operation to obtain a subsequent data-word and then the counter moves back to State (1). The State Counter alternates (1) - (2) - (1) - (2) .... until the WC = 0. At this time, State (0) is set and an interrupt is given to the I/O program.

4.6.10 Data Multiplexor - The Data Multiplexor gathers its input from any one of four sources within the Output Controller and gates one of those sources to the Unibus. This occurs either upon command by the central processor program or in order to store data within core memory.

4.6.11 Interrupt Vector Address - This address is sent to the processor and is used at the time of interrupt to allow the processor to point at an allocated interrupt location within memory. This address can be changed according to requirements of a particular site by moving jumper wires on the platform provided (See Section 4.10).*

4.6.12 Slave Control and Address Decode - During the issuing of a command to the Output Controller by the program, this logic assumes a "slave" position and accepts the command as given. The address is decoded by this logic and the appropriate action taken. Some of the commands sent by the processor are load commands which will set the various registers discussed previously. The processor may also read the contents of each of these registers.

4.6.13 Unibus Drivers and Receivers - These drivers and receivers are used to interface the logic of the Output Controller to the data, address, and control signals of the processor Unibus.

* Switches are used for this purpose in the C version (See Volume II, Page 4).

4.7 Device Address Input Section - The device addresses for the Input Registers can be changed by setting switches in locations 105-10 and 106-10. The layout of the present wiring is shown on Page 10 in Volume II. The low order bits (02, 01) of the address are used to select one of the four possible registers. The high order bits (17,16,15) are understood to be "1". The address shown in Volume II, Page 10 is the same as shown in the Installation Considerations of Section 3.4.

4.7.1 Address Acceptance - The address which will be accepted by the controller is the result of a comparison between the address specified by the switches and that which is given on the Unibus by the program.

4.8 Device Address Output Section - The four registers of the Output section are accessed by sequential device addresses. The switches for specifying the Output Controller addresses are located in sockets 005-10 and 006-10. See the logic diagram in Volume II, Page 4.

4.9 Interrupt Vector Input Section - The interrupt Vector for the Input Controller is established by switches in location 106-10. See Page 10 in Volume II.

4.10 Interrupt Vector Output Section - The Output Interrupt Vector is established by switches in location 006-10. This is shown in Page 4 of Volume II.

4.11 Bus Acquisition Logic - The Bus Acquisition Logic enables the LH-DH/11 Input and Output controllers to become UNIBUS Masters, so that they can perform either a Nonprocess Data Transfer (NPR) or a Bus Request for Interrupt. There exists separate logic to perform these NPR and Bus Request functions. The two sections of logic are virtually identical with only name changes as the major difference. Also, the Input controller and Output controller have nearly identical logic for these functions, with only name changes. Logic diagrams in Volume II pages 12 and 3 illustrate the circuitry that produces the signal sequence shown in the Timing diagram of Figure 6-3.

4.12 NPR and Interrupt Sequences - Similar logic structure is used for both Non-Process Request (data transfer) and Bus Request (interrupt). The only difference between Bus Acquisition For Data transfer and For Interrupt is the hardwired priority level. Data transfers are done on the Non-Process Transfer level which does not allow interrupts (see 4.12.1). Interrupts are done on one of the four Bus Priority levels. Servicing of these four Bus levels is controlled by the processor priority (see 4.12.2).

4.12.1 NPR Bus Acquisition Sequence - The Acquisition sequence begins with the logic in a quiescent state, with the selected (NPS) and master (NPM) Flip-Flops reset. When the need for Bus Control arises, an internal signal (GWRD) is raised. This, in conjunction with the reset state of the "selected" Flip-Flop (NPS), causes a request (NPR) to be driven onto the UNIBUS. Subsequently, the following sequence occurs (see Figure 6-3 and Volume II, pages 3 and 11).

1. Some time after the request, the controller receives a response on the grant line of the UNIBUS (NPG). This is indicated by a positive transition on that line. The grant signal is synchronized to the internal master clock (MCLK) before application to internal logic.

2. The synchronized grant signal (NPGI) is applied to a delay Flip-Flop for decision whether to propagate the grant to the next controller on the UNIBUS. Grant propagation is blocked when the LH-DH/11 controller is requesting service. The grant signal is also used to set the "selected" Flip-Flop if the LH-DH/11 is requesting.

3. When the "selected" Flip-Flop is set, the "selection acknowledge" signal (SACK) is driven on the UNIBUS. During the time SACK is being driven, the grant signal is blocked from propagation. In response to the SACK signal (NPG) will be removed from the BUS by the processor. At this time, the controller can become master when the UNIBUS becomes idle.

4. The UNIBUS is idle when the grant signal (NPG), the Bus Busy signal (BBSY), and the Slave Sync signal (SSYN) are all inactive. The controller becomes master by turning on Bus Busy (BBSY) and removing SACK. This occurs by setting the "Master" Flip-Flop (NPM). The gate NPC indicates this condition to the internal logic.

5. The Controller uses the UNIBUS in Master Mode to transfer one word to memory. When the data transfer is complete, the internal request (GWRD) is removed, causing the Bus Acquisition Logic to be reset. With the Acquisition Logic reset, the UNIBUS becomes idle, allowing the next device, requesting service, to become Master.

4.12.2 Bus Request and Bus Grant - A platform is provided for selection of the priority level at which the LH-DH/11 will operate on the UNIBUS. The platform for the Input, or Receive, section is shown in diagram 10, Volume II. The platform for the Output, or Transmit, section is shown in diagram 4. Several jumpers are required. The Bus Request signal from the logic (BRA-) must be connected to the chosen Bus Request signal on the Unibus (such as BR5-). The unused request signals must be left "open". The chosen Bus Grant level (such as BG5) must be jumpered to signal BGA to allow the Grant to be seen by the logic. The propagated Bus Grant signal, generated by the logic is BGAX. This must be jumpered to the selected priority level (such as BG5X) so that it may be seen by the next controller on the Unibus. All unused priority levels from the processor must be "bussed" through.

4.13 Clock and Timing Sources - Located with the Input Controller is a crystal oscillator with the output of 32 MHz. This source oscillator feeds a divider circuit which provides several slower clocks.

4.14 Display Panel Wiring - The LED indicators on the display panel are driven from circuits located on the Output panel. Connector slot O 14-03 is used to connect the front panel printed circuit board to the O panel. Page 7 in Volume II shows both the drivers and the connector.

4.15 Unibus Connection - In the C version signals to and from the Unibus enter at the connector on the Input Panel and are distributed to both panels. A set of eight cables are brought from the Input Panel to the Output Panel. Unibus Interconnection signals are illustrated as applicable throughout the Logic Diagrams in Volume II.

4.16 IMP Cable Wiring - Two panel connectors are used to bring the IMP signals into the Output panel. These connectors are plugged into slots O 14-04 and O 14-05. Figure 7-3 shows the connectors and the cable to the rear panel. Other reference is made as appropriate in Volume II on pages 6 and 7.

4.17 Host Master Ready - The relay shown on Page 7 of Volume II is used to couple the "test" line from the IMP, back to its source. The relay is pulled in under program control by the setting of bit 02 of the Input Control and Status Register. When bit 02 is made a "1", the drive circuit HRLD- operates the relay. After a suitable delay to off-set contact bounce, bit 11 of the same register will be made a "1" so that the program may proceed with the transmission of information to the IMP. The IMP tests this closure to find out if the controller is up and operational.

4.18 Changing Local Host to Distant Host - Signal lines between the LH-DH/11 and the IMP are carried on twisted-pair or coax wire. The return current path is made on the second wire of each pair or upon the coax shield. For Local Host operation, the return path is brought to one side of its differential driver or receiver circuit. In order to make the change from LH to DH an easy matter, the LH-DH/11 has been wired to allow an interchange of plug-in platforms and circuitry to accommodate the change. Pages 6 and 7 in Volume II illustrate the circuitry involved.

Figure 4-1 Physical Layout B Version

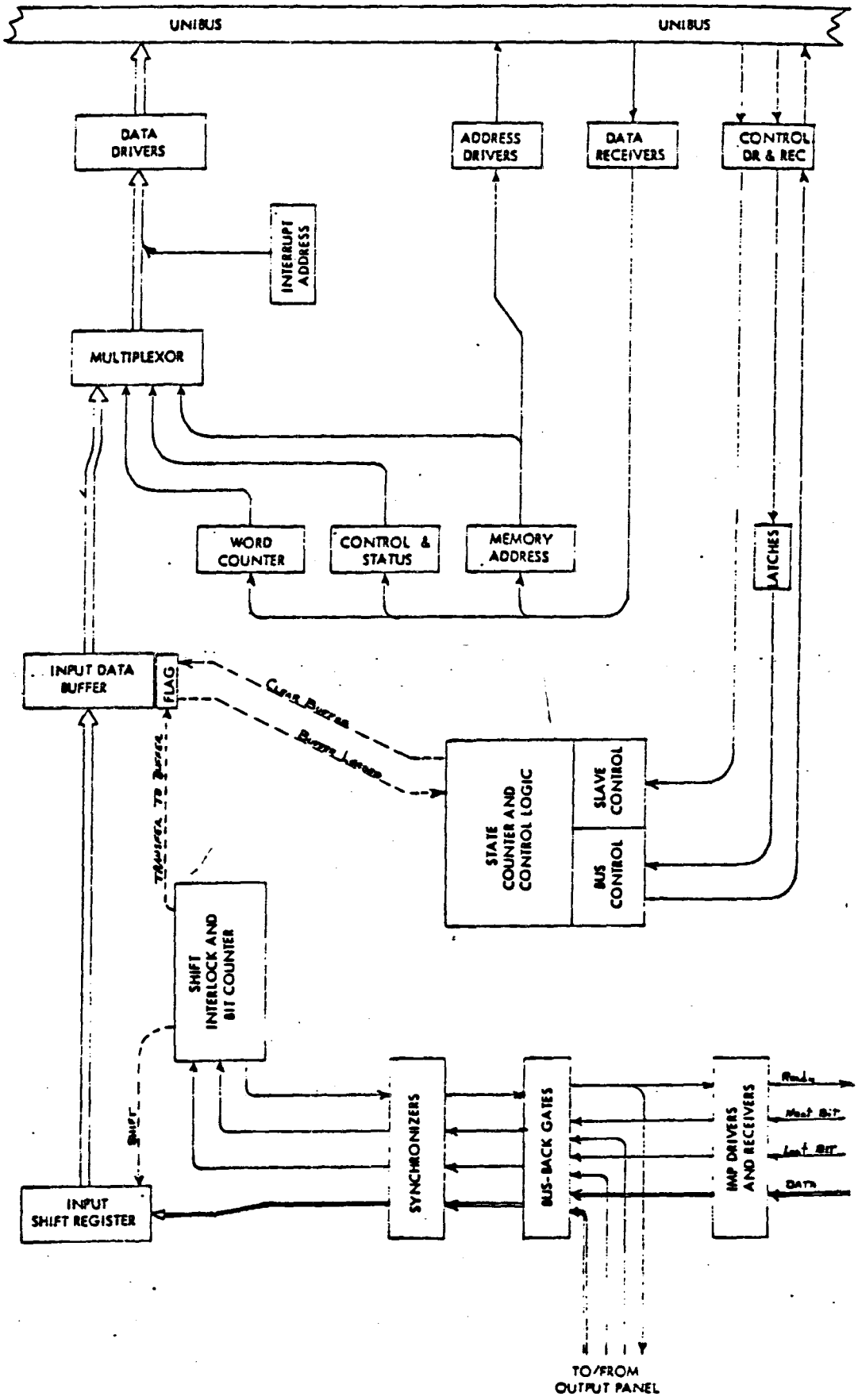

Figure 4-2 INPUT BLOCK DIAGRAM

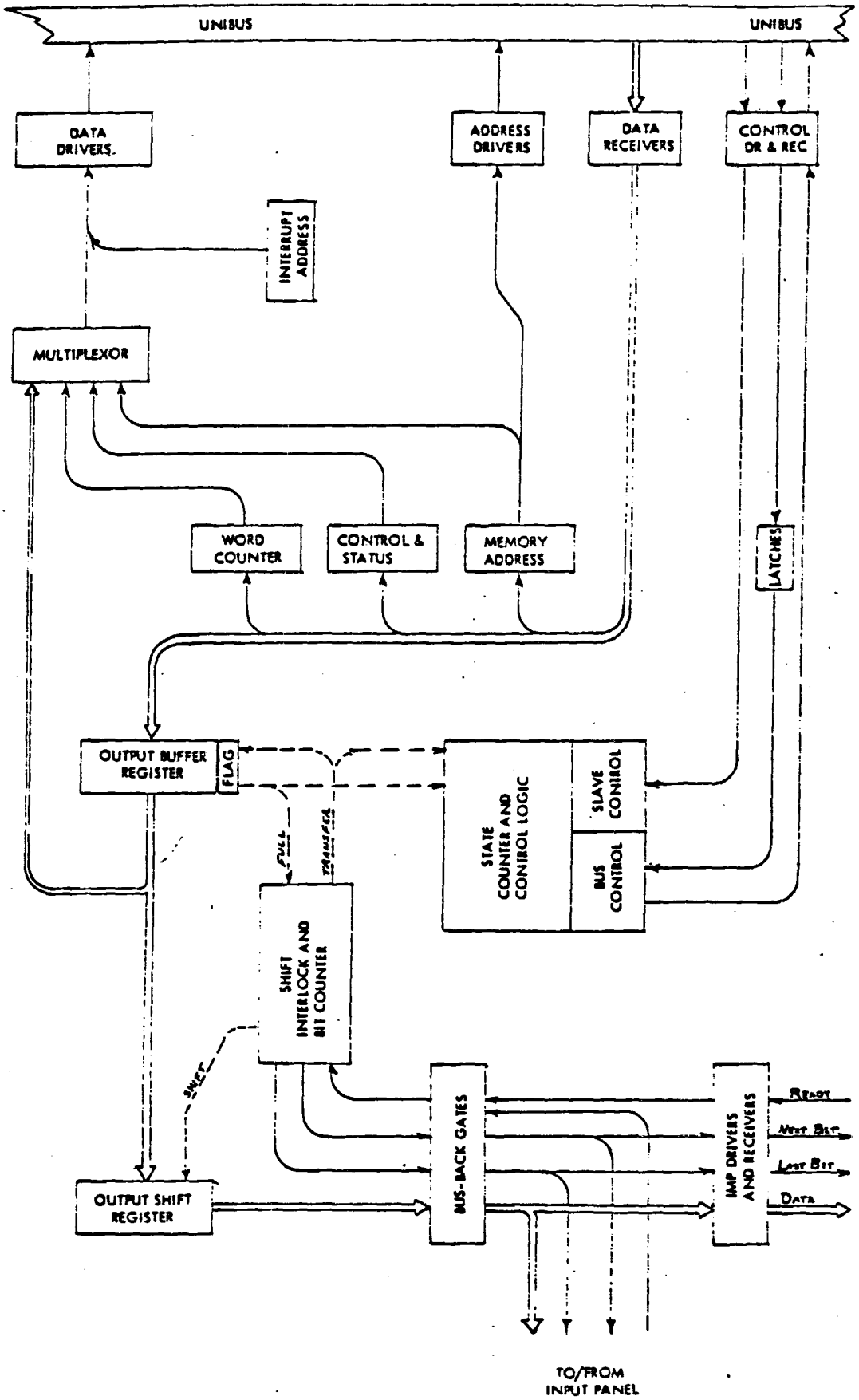

Figure 4-3 OUTPUT BLOCK DIAGRAM

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LH-DH/11C AND LH-DH/11B

CHAPTER 5

PROGRAMMING

CHAPTER 5

5.0 PROGRAMMING

5.1 LH-DH/11 Structure - The LH-DH/11 interface consists of two Direct Memory Access (DMA) devices on the PDP-11 Unibus. One device is used for input and the other for output. These two devices are physically and logically independent.

5.2 Device Addressing - Each device responds to four Unibus addresses in order to provide program access to their internal registers. All registers are full 16-bit Word Registers and must only be accessed by word instructions. The registers are referred to as follows:

1. Control and Status Register (CSR)
2. Data Buffer Register (DBR)
3. Current Word Address Register (CWAR)
4. Word Count Register (WCR)

5.3 Register Addresses - Typical octal addresses for the registers of both the Input and the Output sections are shown below. These may be changed (except for the low order bits) by relocating jumpers on platforms in the B version or resetting switches in the C version. See 4.7 and 4.8.

CSRI	Control & Status In	767600
DBRI	Data Buffer In	767602
CWAI	Current Word Address In	767604
WCI	Word Count In	767606
CSRO	Control & Status Out	767610
DBRO	Data Buffer Out	767612
CWAO	Current Word Address Out	767614
WCO	Word Count Out	767616

5.4 DMA Memory Pointer and Word Count - In the case of each device, the Current Word Address Register is initialized to an even address* in storage and the Word Count Register is initialized to contain the 2's complement number of 16-bit words to be transferred.

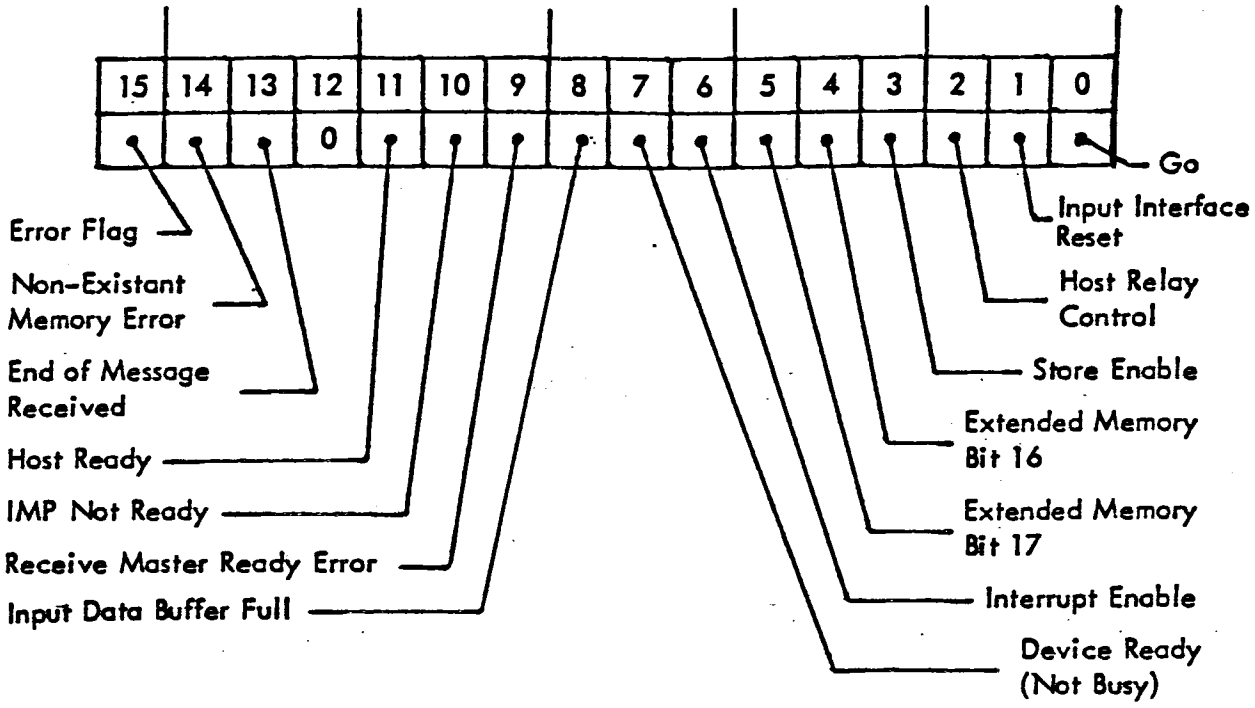

Figure 5-1 Control and Status Register - Input

5.5 Bit Assignment, Input Control and Status Register - Figure 5-1 shows the bit structure of the Input Control and Status Register (CSRI). The test which follows describes the meaning or use of each of these bits.

Bit 15 = Composite Error Indicator - This is the logical "or" of significant error conditions. In the standard LH-DH/11 this is comprised of only CSR Bit 14.

Bit 14 = Non Existent Memory - Indicates that the Input Controller tried to access a memory address that did not respond, most likely meaning an address for which memory does not exist.

*The LH-DH/11 uses full 16-bit word transfers and the PDP-11 requires full words to be stored on even 8-bit byte boundaries.

Bit 13 = End of Message Received - Indicates that the IMP has completed transmission of a message.

Bit 11 = Host Ready - Indicates that the Host Master Ready Relay in the LH-DH/11 is closed, and has had time to settle. This condition should be true before transmission to the IMP proceeds.

Bit 10 = IMP Not Ready - Shows the state of IMP Master Ready line. Bit 10 being "1" means that the IMP is not ready for communication.

Bit 9 = Receive, Master Ready Error - This bit indicates that either the IMP Master Ready or the Host Master Ready condition dropped "off". This may mean that a given transfer could have erroneous data.

Bit 8 = Input Data Buffer Full - Indicates when input data available during programmed I/O.

Bit 7 = Device Ready (Not Busy) - Indicates that the Input device is in a non-DMA state. Modification of the device's registers should only be done while the controller is in this state.

Bit 6 = Interrupt Enable - This is the Interrupt Enable Bit. Interrupt requests will be allowed to interrupt the processor if this bit is a "1".

Bit 5 = Extended Memory Bit 17 - This is Extended Memory Address Bit 17. Used with status Bit 4 for Addressing Extended Memory in the PDP-11 system.

Bit 4 = Extended Memory Bit 16 - Used with status bit 5 for addressing extended memory in the PDP-11.

Bit 3 = Store Enable - When this bit is in the off or "0" state, the Input Controller will drain any data from the IMP without causing DMA activity. When this bit is a "1", the controller will store in memory any data received from the IMP.

Bit 2 = Host Relay Control - When this bit is a "1", the Host Master Ready Relay will close, unless the "Bus-Back" Bit is set in the Output Controller.

Bit 1 = Input Interface Reset - When a "1" is written in this bit, the Input logic will be reset in the same manner as a Unibus reset. This bit always reads as a "0" and does not need to be cleared.

Bit 0 = Go - The "Go" or Start DMA Control Bit. Attempting to write a "1" in this Bit will cause the Input Controller to enter a DMA state. Bit 0 always reads as a "0" since it only pulses the state counter and does not latch.

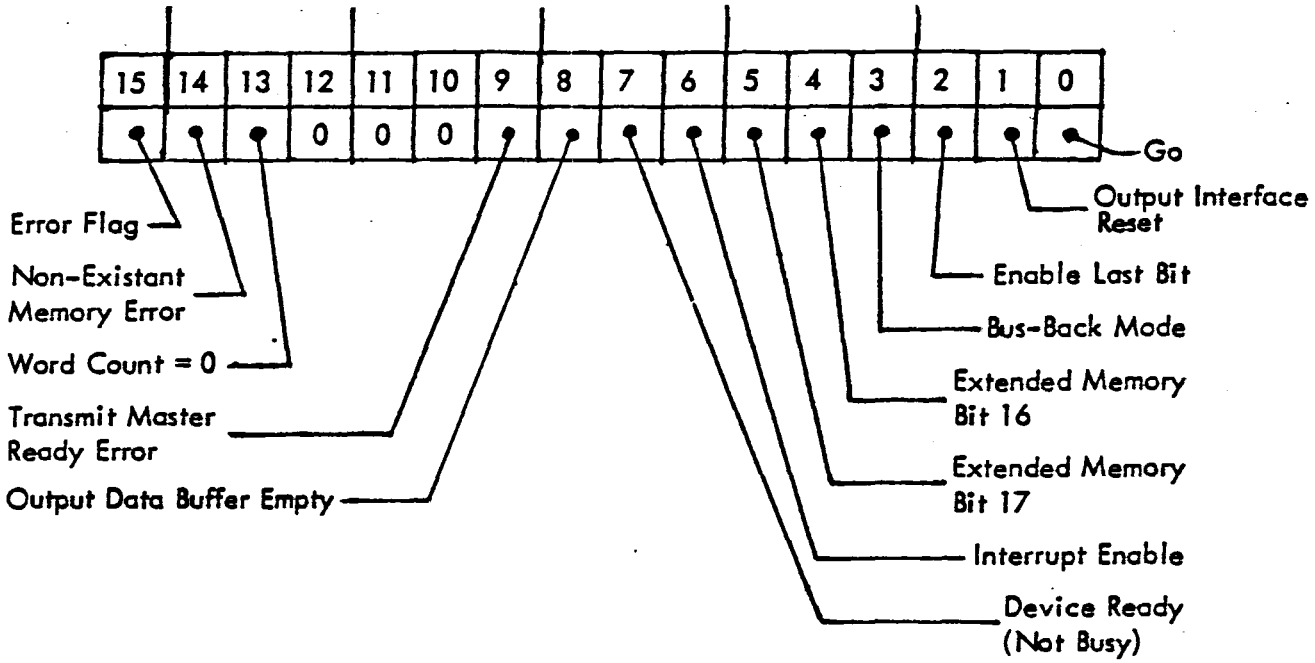

Figure 5-2 Control and Status Register - Output

5.6 Bit Assignment, Output Control and Status Register - Figure 5-2 shows the bit structure of the Output Control and Status Register (CSRO). The text that follows describes the meaning or use of each of these bits.

Bit 15 = Composite Error Indicator - The logical "or" of significant error conditions. In the standard LH-DH/11 this is comprised of only Bit 14.

Bit 14 = Non-Existent Memory - Indicates that the Output Controller tried to access a memory address which did not respond, most likely meaning an address for which no memory exists.

Bit 13 = Word Count = 0 - Indicates that the Output Controller's word count is zero.

Bit 9 = Transmit Master Ready Error - Indicates that either the IMP or Host Master Ready condition went False.

Bit 8 = Output Data Buffer Empty - Indicates when data may be sent during programmed I/O.

Bit 7 = Device Ready (Not Busy) - Indicates the Output device is in a non-DMA state. Modification of the device's registers should only be done in this state.

Bit 6 = Interrupt Enable - Interrupt requests will be allowed to interrupt the processor if this bit is a "1".

Bit 5 = Extended Memory Bit (17) - This is the Extended Memory Address Bit 17. Used with status Bit 4 for addressing Extended Memory in the PDP-11 system.

Bit 4 = Extended Memory Bit (16) - This is the Extended Memory Address Bit 16. Used with status Bit 5 for addressing extended memory in the PDP-11.

Bit 3 = Bus-Back - The Internal Bus-Back Control Bit. With this bit a "1", the Host Master Ready Relay will be open. The Output Controller and Input Controller will communicate with each other rather than with the IMP.

Bit 2 = Enable Last Bit - This is the Last Bit Indication control.. When this Bit is a "1" the End of Message Indication will be sent to the IMP when the current output DMA operation completes.

Bit 1 = Output Interface Reset - When a "1" is written into this bit, the Output logic will be reset in the same manner as a Unibus reset. This bit always reads as a "0" and does not need to be cleared.

Bit 0 = Go - The "Go" or Start DMA Control Bit. Attempting to write a "one" in this Bit will cause the Output Controller to enter a DMA state. Bit 0 always reads as a "0".

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CHAPTER 6

DETAILED DESCRIPTION CONTROL STATES

CHAPTER 6

6.0 DETAILED DESCRIPTION CONTROL STATES

6.1 Input Controller Details - Details of Input Controller operations are provided below. Reference to Figure 4-2 and Section 4.4 will provide information about the major logical elements of the Input Controller.

6.2 Input Controller States - Figure 6-1 illustrates the states through which the Input Controller sequences. These states are described in subsequent paragraphs.

6.2.1 Input State (0) - Referred to as the "Ready" State. In Input State (0) no DMA activity can occur. This state is entered upon completion of a previous DMA operation. Entry into State (0) always generates an interrupt request. Setting the "GO" bit in the CSR will cause a transition to State (1) . State (0) is indicated in the CSR by the "Ready" bit. State (0) is the state in which the Memory address and the Word Count Register should be set for the next DMA operation.

6.2.2 Input State (1) - Referred to as the "Idling" State. In Input State (1) the controller is enabled for DMA operation, but has no data to transfer to memory. If the word count is zero in State (1) , the controller will proceed to State (0) . When the Input Buffer Register has data to be stored in memory, the controller will proceed from State (1) to State (2) .

6.2.3 Input State (2) - Referred to as the "DMA" State. In Input State (2) this state the Input Controller obtains DMA control from the Unibus and transfer the contents of the Input Buffer Register to memory. The DMA operation will also cause the Memory Address to be incremented and the Word Count to be incremented. If, during a DMA operation, there is no response from memory within 20 useconds, an error indicator will be set and the controller will proceed to State (0) . If the transfer is successful and the End Of Message indication has been received from the IMP, the controller will proceed to State (0) . If the End Of Message indication has not been received, the controller will return to State (1) .

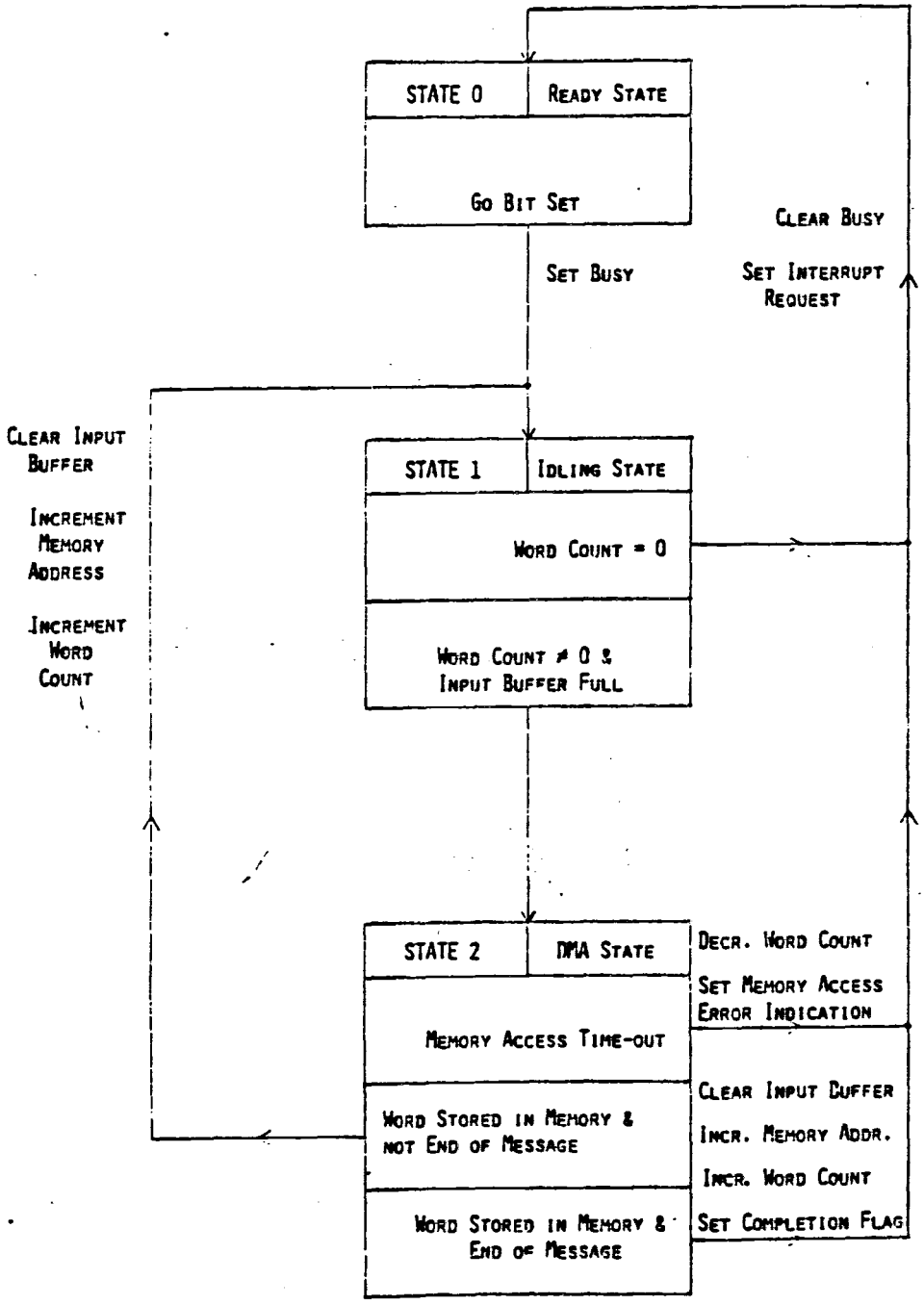


FIGURE 6-1 INPUT-STATE FLOW DIAGRAM

SS0 = (ST1•WCZR)+(DSTD•EOM)+MMER

SS1 = (ST0•LRC•DI00)+(DSTD•EOM-)

SS2 = ST1•IBF•WCZR-

1-25-78

6.3 Output Controller Details - Details of Output Controller operations are provided below. Reference to Figure 4-3 and Section 4.6 will provide information about the major logical elements of the Output Controller.

6.4 Output Controller States - Figure 6-2 illustrates the states through which the Output Controller Sequences following program set-up. Once the program in the CPU establishes a block of data in memory which is to be transferred out of the processor and onto the communications network, the program goes through a sequence of commands which insert the starting location of the block of data into the Memory Address Register and the block length of the data block into the Word Count Register. The program then enables the Output Controller by setting the GO flag in the Control and Status Register. Output States are described in subsequent paragraphs.

6.4.1 Output State (0) - Referred to as the "Ready" State. Output State (0) no DMA activity can occur. This state is entered upon completion of a previous DMA. operation. Entry into State (0) always generates an interrupt request. Setting the "GO" bit in the CSR will cause a transition to State (1) . State (0) is indicated in the CSR by the "Ready" bit. State (0) is the state in which the Memory Address and the Word Count Register should be set for the next DMA operation.

6.4.2 Output State (1) - Referred to as the "Idling" State. In Output State (1) the controller is enabled for DMA operation, but does not need data from memory. If the Word Count is zero in State (1) , the controller will proceed to State (0) . When the Output Buffer Register becomes empty and needs data from memory the controller will proceed to State (2) .

6.4.3 Output State (2) - Referred to as the "DMA" State. In Output State (2) the Output Controller obtains DMA control from the UNIBUS and transfers data from memory to the Output Buffer Register. The DMA operation will also cause the Memory Address to be incremented and the Word Count to be incremented. If, during a DMA operation, there is no response from memory within 20 us., an error indicator will be set and the Controller will proceed to State (0) . If the transfer is successful, the Controller will return to State (1) . If the Last Bit Indicator in the CSR is set, and the Word Count becomes zero with the current DMA operation, an End Of Message indication will be sent to the IMP upon completion of transmission of the current data block.

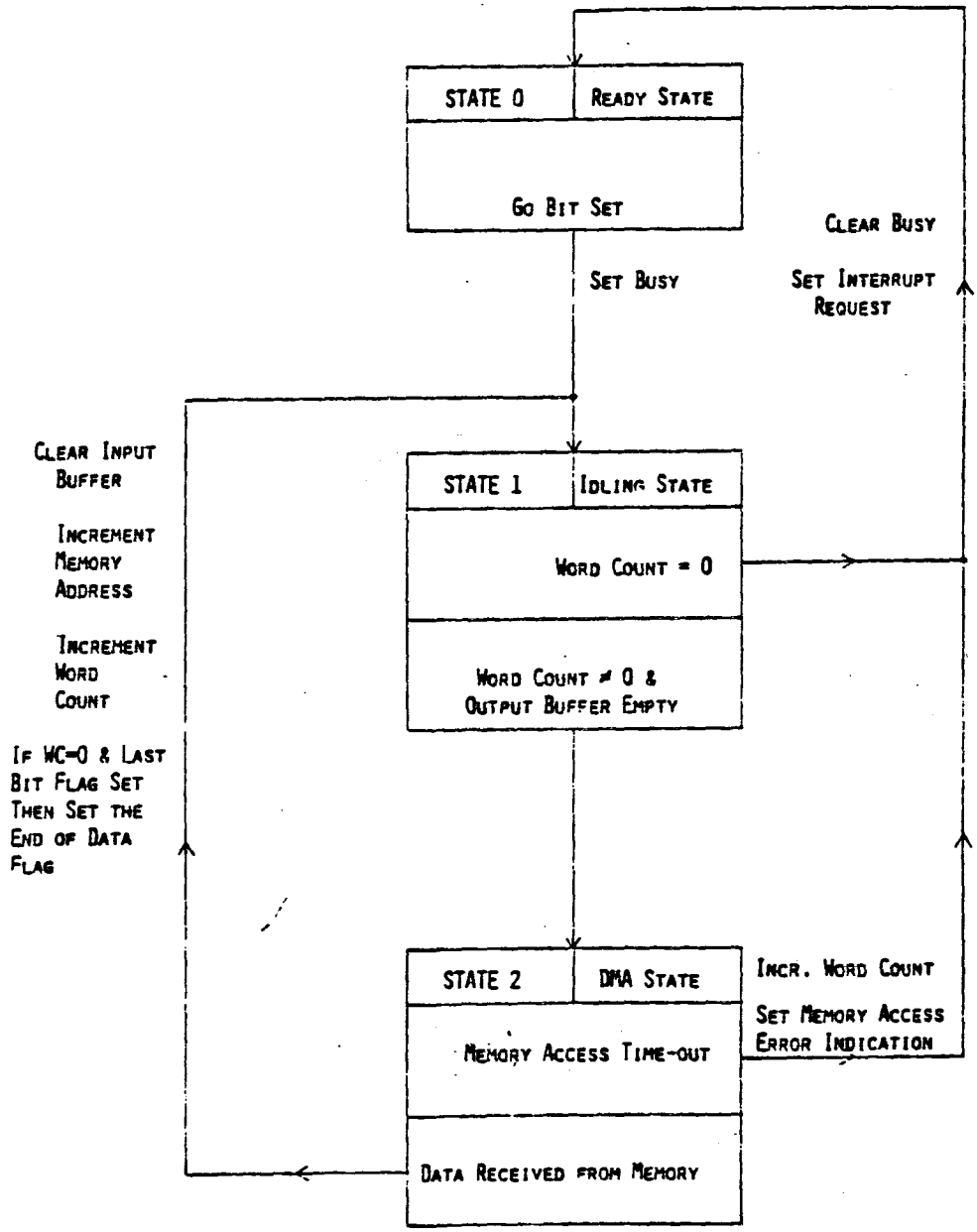


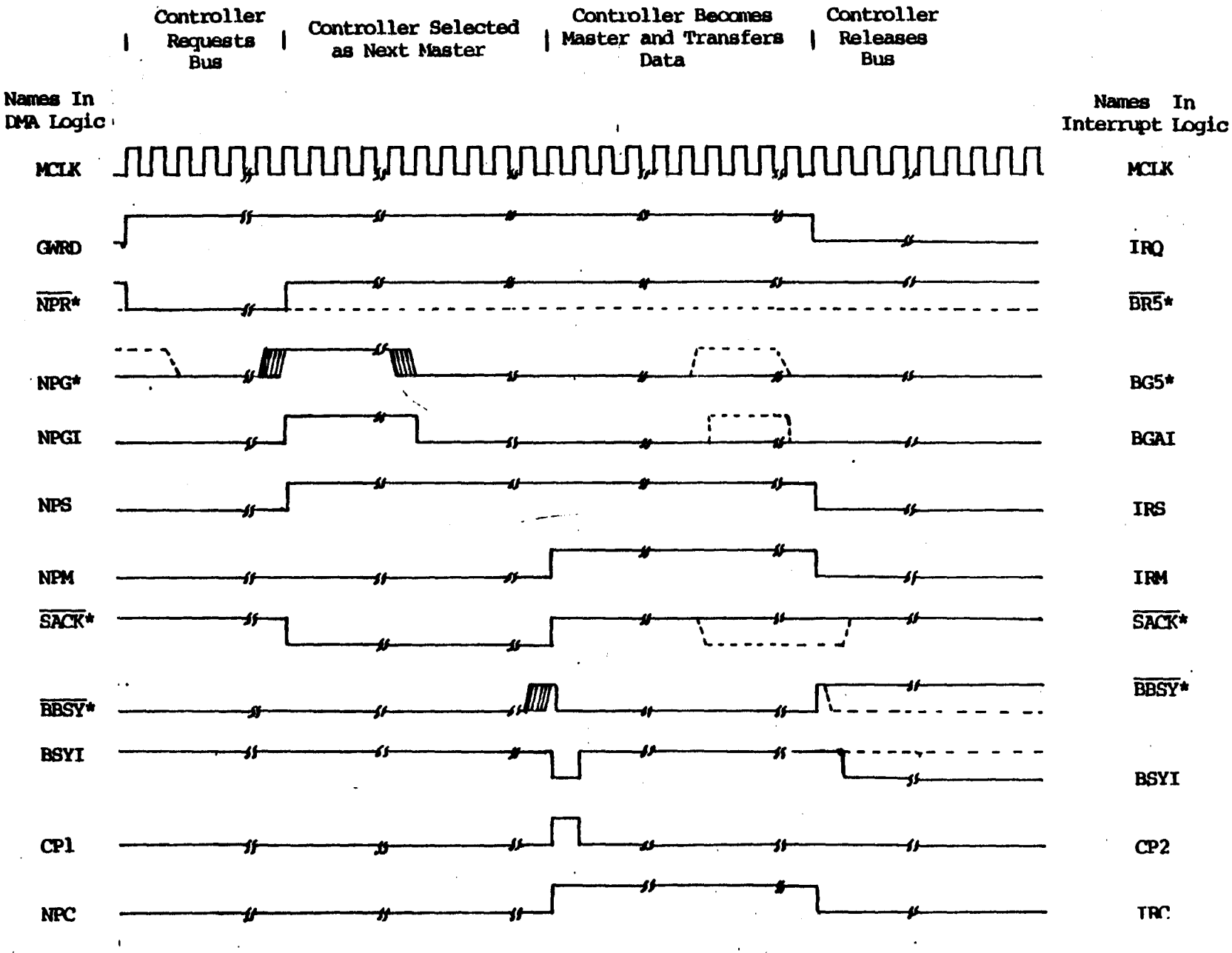
FIGURE 6-2 OUTPUT-STATE FLOW DIAGRAM

SS0 = (WCZR•ST1)+S2T0

SS1 = (ST0•LR0•DI00)+DRCV

SS2 = ST1•OBF-•WCZR-

1-25-78



*UNIBUS Signal

Figure 6-3 BUS ACQUISITION TIMING

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LH-DH/11C AND LH-DH/11B

CHAPTER 7

DETAILED DESCRIPTION OF LOGIC DIAGRAMS

CHAPTER 7

7.0 DETAILED DESCRIPTION OF LOGIC DIAGRAMS

7.1 Logic Cross References - Each logic diagram of Volume II has a signal cross reference chart in the left-hand margin. Two alphabetical lists are provided. One list provides coordinate references of each signal name shown on the associated diagram with an appended (*) to show the coordinate of its cource. The second list refers to other diagrams where the same signal is used or sourced (*). (See Volume I):

> In diagram 01, the name AGO is shown to be illustrated at coordinates A7 and A8(*). This source is the circuit located at coordinate A8 due to the (*) and it does not go to any other drawing since it is not listed in the second column.

7.2 - Additional Cross Reference - Chapter 9 provides a complete coordinate cross reference for all signals in the LH-DH/11. The list is separated into two parts, one for Input and one for Output.

7.3 Glossary - Chapter 8 provides a brief definition of all logic terms in the LH-DH/11.

(Continued)

7.4 Input Logic Diagrams/Description - The following paragraphs describe the logic elements presented on the diagrams in Volume II. Please note the drawing page numbers in the right hand margin, adjacent to each paragraph.

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7.4.1 Data Transceivers and Multiplexers - This drawing illustrates the circuitry which operates on the UNIBUS to facilitate the bi-directional transfer of parallel data words for use by the Input (Receive) section. Also shown are the multiplexer circuits for gating the contents of various registers and status bits onto the UNIBUS data lines. Four sources drive each multiplexer in order to actuate a given data bit. Selection is controlled by low-order address bits presented by the processor. These bits (A101, A102) enter circuitry in the lower left of the diagram. The actual gating of the multiplexer output onto the UNIBUS is controlled by the term EDD-. The additional 2:1 multiplexers used for gating data bits 0 through 7 are used to select between the output of the 4:1 multiplexers and the Interrupt Vector Address. The source of the Interrupt Vector Address is either a set of toggle switches for the "C" version or a set of jumpers located on platform 106-10.* Refer to notes (1) through (5) on drawing number 10. 8

7.4.2 Memory Address Registers and Transceivers - The address transceivers that operate on the UNIBUS are gated "on" by term NPC-. Once turned on, the transceivers allow the contents of the Memory Address Register/Counter to reach the address lines of the UNIBUS. The contents of the Memory Address Register, including the memory extension bits, are pre-set by a data-word received from the processor. The register is incremented by the term IMA-. 9

7.4.3 Slave Control and UNIBUS Address Selector - This drawing illustrates the technique for comparing the address on the UNIBUS with the established Device Address of the Input Controller. In the "C" version, the Device Address is established by toggle switches located in position 105-10 and 106-10. The address selection switches are illustrated in the upper left of the drawing. In the "B" version, jumper platforms are used instead of toggle switches (see Note (5)). Once address comparison is made, the Unit Select term (USL) is gated with the Master Sync allowing the Slave Sync flip-flop to be set. Since the address presented on the UNIBUS by the process is used to select one of the internal registers of the input controller, register pulses are selected by the two low-order bits of the address. Terms LR0 through LR3 present load pulses to their respective registers when the C11 term designates a "Write" operation on the UNIBUS. Terms RR0 and RR1 are pulsed according to the low-order address bits when the term C11 designates a "Read". The drawing also illustrates the clock source for the entire LH-DH/11. Beginning with a 32 MHZ 10

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*106-10 refers to Input Panel location, Colume 06, Row 10.

crystal oscillator, the signal is shaped and presented to a binary counter. The counter is tapped at the 4 MC and the 16 MC points; these signals are shaped and passed through driver circuits to be used as clocking terms throughout the device. The term ROSTR- is used throughout the controller to clock the Input Control and Status Register (CSRI) in response to pulse LR0 gated with the Master Clock. Illustrated on this drawing is the setting of RMRE if a Receive Master Ready Error occurs. This latch is reset by a CSRI load with bit 09 = "0". Initialization of the controller (INTI) takes place either by program control (PINI) when register 0 is selected and data line 01 is raised, or by the system reset (INIR). 10

7.4.4 Word Count and State Control - The Word Counter affects the state control logic by means of the term WCZR - which indicates that the counter has reached zero. The counter is pre-set from the UNIBUS data lines when the term LR3- is raised. The counter is incremented each time a memory cycle that stores the data received by the Input section is completed. State count logic is the result of decoding SB0 and SB1. The terms ST0, ST1 and ST2 are raised as the State Counter passes through its sequence as shown in Figure 6-1. Action that takes place in each of these input states is described in Section 6.2. The one-shot MEMTO measures a period of time following a memory access request. Should a "time-out" occur, the Memory Error Indicator (MMER) is "set". The error latch NOMM is cleared by the processor when it selects CSRI (by ROSTR-) and inserts a "0" into the flip-flop (bit 14). During a memory transfer, the Master Sync and Slave Sync are used to cause "Data Stored" (DSTD) and to clear the Input Buffer (IBC). 11

7.4.5 Bus Acquisition and Control Transceivers - Control lines reaching the Input Section from the UNIBUS transceivers are strobbed by means of clocked latches. The result is that Slave Sync (SSNR), Bus Busy (BSYR), Non Process Grant (NPGR-), and Bus Grant (BGAR-) are all synchronized and stored in flip-flops. They become SSNI, BSYI, NPGI-, and BGAI-, respectively. These signals are used throughout the controller in a synchronous fashion. The logic dealing with Non Process Request and Bus Request (lower right side); and that dealing with Non Process Grant and Gus Grant (upper right side) is discussed in detail in Sections 4.11 and 4.12. The timing sequence of these signals is provided in Figure 6-3. The Non Process Request (NPR-) is a single transceiver that is turned on when the Input Controller wishes to place a word into memory. Response to this request is the Non Process Grant. Transceivers for UNIBUS Select Acknowledge (SACK-) and Interrupt (INTR-) are located in A2 as well. Interrupt Enable (IEN) and Interrupt Request (IRQ) are shown in the lower center of the drawing. The Jumper platform (Note (1)) is used to allow user selection of a particular Bus Grant signal, priority 4, 5, 6 or 7. Three of these signals are shown as jumpered through, with Bus Grant 5 being utilized by the Input Controller. If the LH-DH/11 input is not requesting service, then the Bus Grant is propagated immediately to the next device down the line through the transceiver BGAX. Similarly, Note (2) illustrates the platform for Bus Request. Only one of the four possible bus requests is jumpered to the transceiver BRA-. This is Bus Request 5 and must be associated exactly with that described under Note (1). 12 12

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7.4.6 Input Data Register and IMP Control Logic - The Input Data Register is used to accumulate a serial stream of data bits presented to the Input Controller by the Interface Message Processor (IMP). Signal lines to and from the IMP are illustrated in drawings 6 and 7. Signals used in the Input Section are brought between the panels by jumper plugs. The serial data stream (DA) is passed into the shift register by the clocking term SHB-. Once the 16 bits of a given word have been loaded, indicated by BCT15 from the 16 bit counter, the word is transferred in parallel to the Input Buffer (IB00 through IB15). Serial data is allowed to continue shifting bits into the shift register while the buffer retains the word for stoarge into the memory of the PDP-11. The transfer from shift registers to buffer causes the state control request service from the processor. If the serial data coming from the IMP is less than 16 bits (indicated by Last Bit) shifting continues until the incoming data is justified. This "padding" action fills the remaining bits with zeros. The PAD flip-flop is used to cause this process. As the parallel word is transferred into the Input Buffer, a request is made from the State Counter to pass the contents of this register into the UNIBUS memory. All signals used for handshaking with the IMP connection are clocked by means of flip-flops.* The term Host Ready For Next Bit (HRFNB) is turned on when the IMP indicates that it is "on-line" (IRDY) and that the IMP Bit Ready line (IBR-) is "off". After the IMP places a data bit on the line (IDA) ir raises There's Your Bit signal causing IBR to be raised as an internal indication that the bit is ready. These two control lines raised simultaneously, causes the term HRR to reset HRFNB. This transition causes the shifting in of a data bit by SHB; the incrementing of the Bit Counter; and informing the IMP that the bit has been loaded. When the IMP drops its, There's Your Bit line, the clocked term IBR is dropped as well. HRFNB will be raised again unless the last shift filled the input shift register. The term HRDY indicates to the IMP that the PDP-11 is on-line and ready to receive data. This term is referred to as the Host Master Ready. It is set by data bit 2 when loading the Command and Status Register. The related term from the IMP is latched into the flip-flop IRDY and no action takes place within the controller unless IRDY is "on". The status of IRDY is accessible in the status register for program assessment. Upon receiving the last bit of a transfer, the status bit EOM is raised indicating End Of Message. 13 13

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* See Timing Diagram, Figure 7-1 for IMP to LH-DH/11 signal sequencing. See also Figure 7-3.

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7.5 Output Logic Diagram Description - Please refer to Volume II pages 1 through 7 for the diagrams that are being described in this section. The numbers on the right hand margin are keyed to the diagram discussed in the adjacent paragraph.

7.5.1 Data Transceivers and Multiplexers - This drawing illustrates the circuitry which operates on the UNIBUS to facilitate the bi-directional transfer of parallel data words for use by the Output (Transmit) section. Also shown are the multiplexer circuits for gating the contents of various registers and status bits onto the UNIBUS data lines. Four sources drive each multiplexer in order to actuate a given data bit. Selection is controlled by low-order address bits presented by the processor. These bits (AI01, AI02) enter circuitry in the lower left of the diagram. The actual gating of the multiplexer output onto the UNIBUS is controlled by the term EDD-. The additional 2:1 multiplexers used for gating data bits 0 through 7 are used to select between the output of the 4:1 multiplexers and the Interrupt Vector Address. The source of the Interrupt Vector Address is either a set of toggle switches for the "C" version or a set of jumpers located on platform O06-10.* Refer to notes (1) through (5) on drawing number 4. 1

7.5.2 Memory Address Registers and Transceivers - The address transceivers that operate on the UNIBUS are gated "on" by term NPC-. Once turned on, the transceivers allow the contents of the Memory Address Register/Counter to reach the address lines of the UNIBUS. The contents of the Memory Address Register, including the memory extension bits, are pre-set by a data-word received from the processor. The register is incremented by the term IMA-. 2

7.5.3 Bus Acquisition and Control Transceivers - Control lines reaching the Input Section from the UNIBUS transceivers are strobbed by means of blocked latches. The result is that Slave Sync (SSNR), Bus Busy (BSYR), Non Process Grant (NPGR-), and Bus Grant (BGAR-) are all synchronized and stored in flip-flops. They become SSNI, BSYI, NPGI-, and BGAI-, respectively. These signals are used throughout the controller in a synchronous fashion. The logic dealing with Non Process Request and Bus Request (lower right side); and that dealing with Non Process Grant and Bus Grant (upper right side) is discussed in detail in Sections 4.11 and 4.12. The timing sequence of these signals is provided in Figure 6-3. The Non Process Request (NPR-) is a single transceiver that is turned on when the Output Controller wishes to take a word from memory. Response to this request is the Non Process Grant. Transceivers for UNIBUS Select Acknowledge (SACK-) and Interrupt (INTR-) are located in A2 as well. Interrupt Enable (IEN) and Interrupt Request (IRQ) are shown in the lower center of the drawing. The Jumper platform (Note (1)) is used to allow user selection of a particular Bus Grant signal, priority 4, 5, 6 or 7. Three of these signals are shown as jumpered through, with Bus Grant 5 being utilized by the Output Controller. If the LH-DH/11 output is not 3

* O06-10 refers to Output Panel location, Column 06, Row 10.

requesting service, then the Bus Grant is propagated immediately to the next device down the line through the transceiver BGAX. Similarly, Note (2) illustrates the platform for Bus Request. Only one of the four possible bus requests is jumpered to the transceiver BRA-. This is Bus Request 5 and must be associated exactly with that described under Note (1). 3

7.5.4 Slave Control and UNIBUS Address Selector - This drawing illustrates the technique for comparing the address on the UNIBUS with the established Device Address of the Output Controller. In the "C" version, the Device Address is established by toggle switches located in position O05-10 and O06-10. The address selection switches are illustrated in the upper left of the drawing. In the "B" version, jumper platforms are used instead of toggle switches (see Note (5)). Once address comparison is made, the Unit Select term (USL) is gated with the Master Sync allowing the Slave Sync flip-flop to be set. Since the address presented on the UNIBUS by the process is used to select one of the internal registers of the input controller, register pulses are selected by the two low-order bits of the address. Terms LR0 through LR3 present load pulses to their respective registers when the C11 term designates a "Write" operation on the UNIBUS. Terms RR0 and RR1 are pulsed according to the low-order address bits when the term C11 designates a "Read". Clock signals for 4MC and 16MC are brought over from the Input Panel. These signals are shaped and passed through driver circuits to be used as clocking terms throughout the Output Panel. The term R0STR- is used to clock the Output Control and Status Register (CSR0)in response to pulse LR0 gated with the Master Clock. Illustrated on this drawing is the setting of XMRE if a Transmit Master Ready Error occurs. This latch is reset by a CSR0 load with bit 09="0". Initialization of the controller (INTI) takes place either by program control (PINI) when register 0 is selected and data line 01 is raised, or by the system reset (INIR). 4 4

7.5.5 Word Count and State Control - The Word Counter affects the state control logic by means of the term WCZR - which indicates that the counter has reached zero. The counter is pre-set from the UNIBUS data lines when the term LR3- is raised. The counter is incremented each time a memory access cycle is completed. State count logic is the result of decoding SB0 and SB1. The terms ST0, ST1 and ST2 are raised as the State Counter passes through its sequence as shown in Figure 6-2. Action that takes place in each of these output states is described in Section 6.4. The one-shot MEMTO measures a period of time following a memory access request. Should a "time-out" occur, the Memory Error Indicator (S2T0) is "set". The error latch NOMM is cleared by the processor when it selects CSR0 (by R0STR-) and inserts a "0" into the flip-flop (bit 14). During a memory transfer, the Master Sync and Slave Sync are used to cause "Data Received" (DRCV) and Output Buffer Load (OBL). 5

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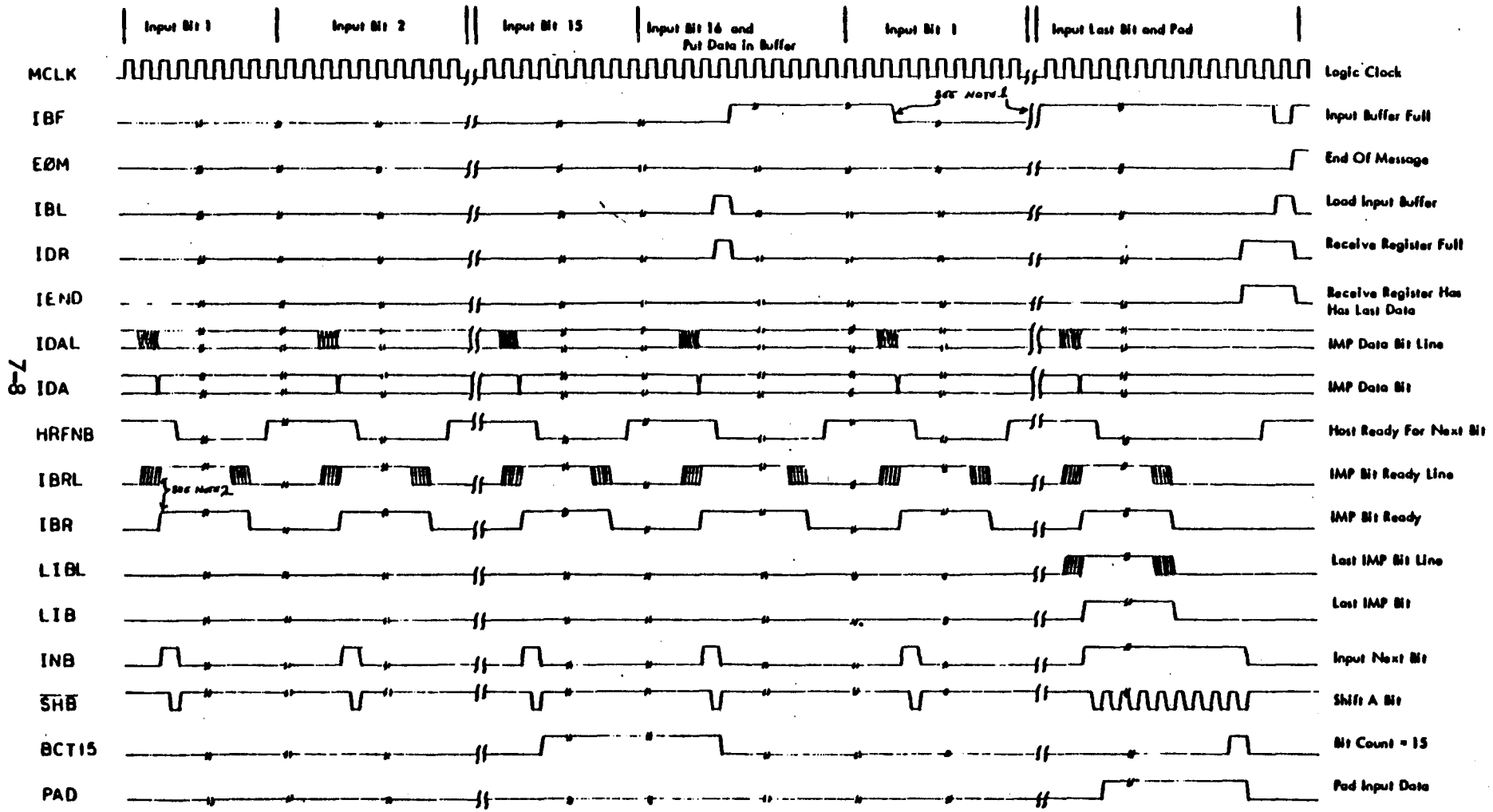
7.5.6 Data Transmit Register, IMP Control and Local/Distant Host Drivers - The Output Buffer Register is pre-set from the UNIBUS data transceivers. The 16-bit word that is loaded into this buffer is passed to the Output Shift Register which is a serial shifter producing a series of bits on the term HDA. HDA feeds directly into the driver to the IMP called Host Data Driver (HDAD). As the bit is made available for the IMP, the line Host Bit Ready (or "There's Your Host Bit") is raised. Host Bit Ready (HBR) is only raised when the IMP indicates "IMP Ready for Next Bit" (IRFNB) and if the Send Data latch is "on" (SDA). The Output Shift Register is loaded by the term LSR-. This occurs on the 16 MHz clock when the register is empty and the data buffer is full (OBE). The shifting operation is caused by SHB- which also increments a 16-bit counter. The term BCT15 indicates when the 16th bit is present upon the Host Data Line and if it is the Last Host Bit (LHB) is raised. Transfer of each bit to the IMP is controlled by Host Bit Ready (HBR). As indicated in the drawing by Notes (1) and (2), the output panel can be equipped with either a local host driver configuration or a distant host driver configuration. The local host configuration (2) utilizes resister and jumper platforms in O13-06 and O14-06. For distant host operation, these platforms are replaced by differential drivers and receivers (1). Internal bus-back of the controller, so that signals will pass from the output panel to the input panel without going through the external circuits, is controlled by the flip-flop BBAK. This latch is set by CSRO bit 13. All of the drivers to the IMP are disabled if BBAK is set. Similarly all the receivers are disabled when BBAK is set. 6 6

7.5.7 Local/Distant Host Receivers and Indicator Drivers - This drawing illustrates both the distant host and the local host receiver configurations. In the local host configuration (2) the signals from the IMP are passed through jumper platforms in locations O13-08 and O14-08. In this case, the return signal is grounded and the active signal is passed forward into a selector circuit. For distant host operation (1) differential receivers are inserted in place of the platforms. Signals from the IMP, IDAL, IBRL, LIBL, and IRYL are received into a selector circuit. It is at this point that the receivers are disabled when in bus-back mode. When BBAK is "on", the internal signals from the circuits on drawing 6 are fed into the control logic instead. Control lines from the IMP that established IMP Bit Ready (IBRL) and IMP Ready For Next Bit (IRYL) are passed through a clocking and latching circuit. The signals IMP Data (IDAL) and Last IMP Bit (LIBL) are passed directly into registers in control circuitry after passing the multiplexor. The Host Master Ready relay is closed by the turning on of the bit in the status register. When this relay is closed, the signal from the IMP HMRA is coupled to HMRB. The IMP uses this closure to test whether the LH-DH/11 is "on-line". The front panel indicators are as shown in the drawing, each one with a light driver and all lines exiting the output panel from position O14-03. 7



NOTE 1: The DMA controller will store a data word whenever the Input Buffer is full (IBF="1"). Also, End Of Message (EOM) will cause Input DMA to terminate.

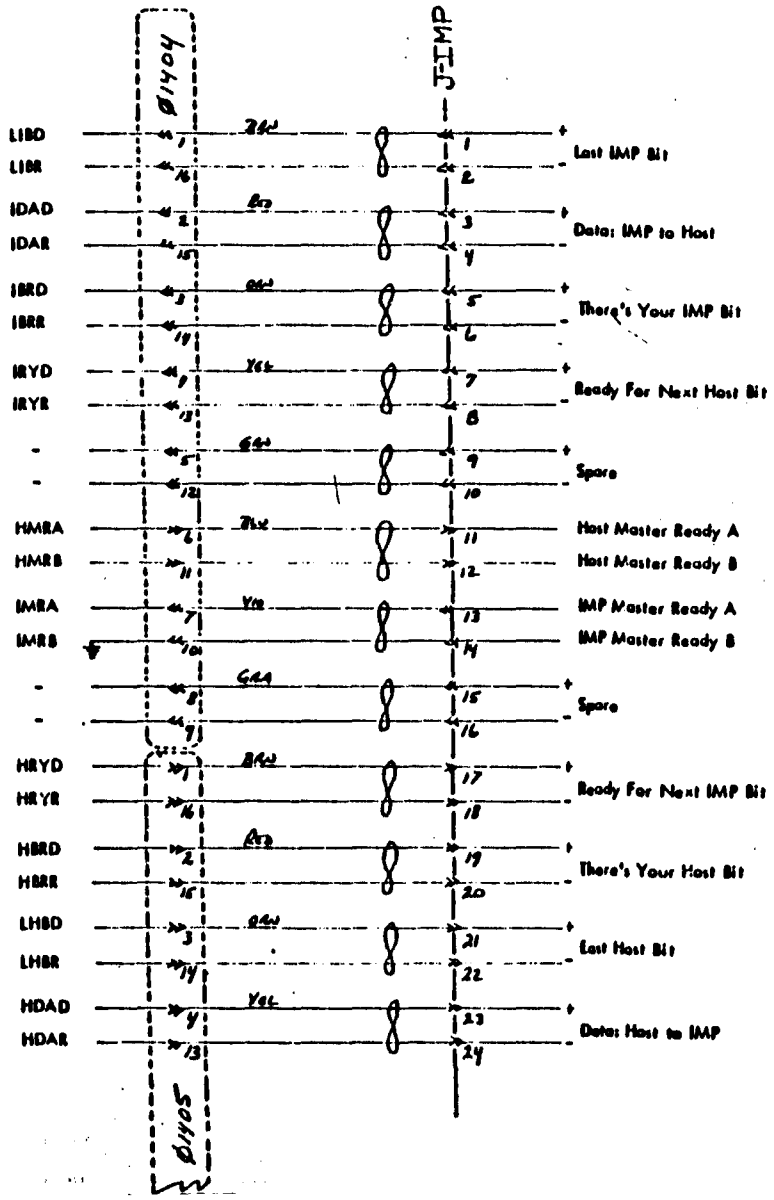
NOTE 2: Signals from the IMP are not synchronous with the internal clock (MCLK) so transitions can occur anywhere in a clock cycle. The internal signal will follow the IMP signal but will change at clock-times.

Figure 7-1 INPUT-TIMING DIAGRAM IMP SIGNALS

NOTE 1: The DMA controller will fetch another data word whenever the Output Buffer is empty (OBF="0"). Also, the Last Word signal (LSTWD) will be concurrent with OBF.

NOTE 2: Signals from the IMP are not synchronous with the internal clock (MCLK) so transitions can occur anywhere in a clock cycle. The internal signal will follow the IMP signal but will change at clock-times.

Figure 7-2 OUTPUT - TIMING DIAGRAM IMP SIGNALS



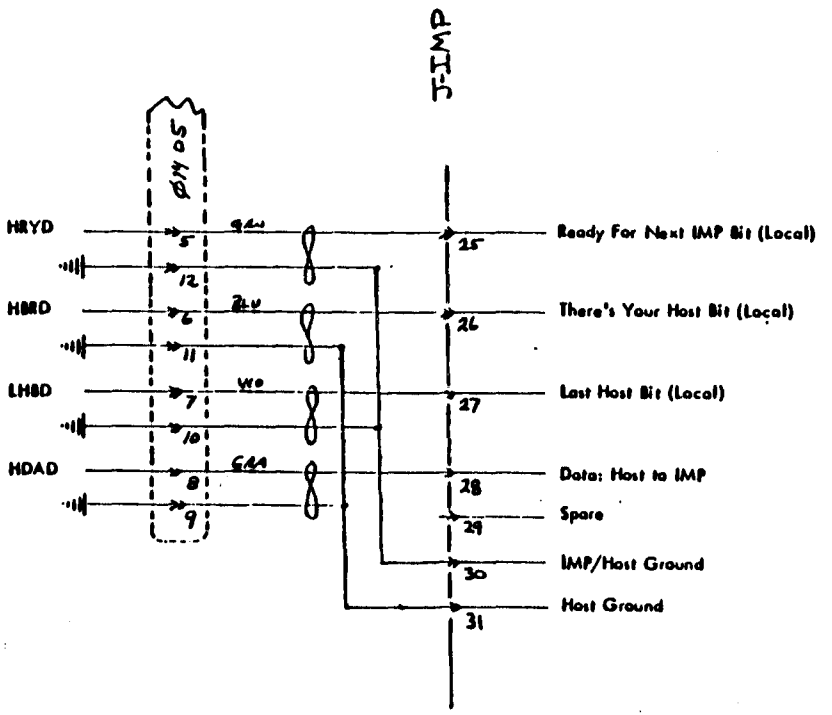


Figure 7-3 IMP CABLE DIAGRAM

MAINTENANCE MANUAL

LH-DH/11C AND LH-DH/11B

CHAPTER 8

COMPOSITE GLOSSARY OF LOGIC SIGNAL NAMES

4 MC	4 MHz Clock Source
4 MHz	4 MHz Clock Source
16 CK	16 MHz Clock Driver
16 MC	16 MHz Clock Source
32 MC	32 MHz Clock Crystal
AØØ- thru A17-	UNIBUS Address Lines
ACB0 thru ACB2	Address Counter borrow terms
ACC0 thru ACC2	Address Counter carry terms
AIØØ thru AI17	Address bits in from receivers
ASØ3 thru AS14	Address selection bits
BBAK	Bus-back Mode
BBSY-	UNIBUS Busy
BCT15	Bit count equals fifteen
BG4 thru BG7	UNIBUS Bus Grant level 4 thru level 7
BG4X thru BG7X	UNIBUS Bus Grant level 4 thru 7 propagated
BGA	UNIBUS Bus Grant
BGAD	Bus Grant delayed
BGAI	Clocked Bus Grant in
BGAO-	Bus Grant out to driver
BGAR-	Bus Grant in from receiver
BGAS-	"or" of BGAI and BGAD
BGAX	UNIBUS Bus Grant propagated
BGXI-	Not used
BIDL	Bus idle
BR4- thru BR7-	UNIBUS Bus Request level 4 thru level 7
BRA-	UNIBUS Bus Request
BRAO	Bus Request to Driver
BSY1	Bus Busy signal clocked
BSYI	Clocked Bus Busy In
BSYO	Bus Busy to Driver
BSYR	Bus Busy from Receiver
BUSY	Input Device Busy
CØ-	UNIBUS Control bit Ø
C1-	UNIBUS Control bit 1
CIØ	Bus Control from Receiver bit Ø
CI1	Bus Control from Receiver bit 1
CP1	Clocking Pulse 1
CP2	Clocking Pulse 2
CXØØ thru CXØ1	External Capacitor leads
DØØ- thru DI5-	UNIBUS Data Lines
DANS	Memory answers LH-DH/11 Master Sync
DBØØ thru DBØ7	Lower eight bits of Data Multiplexer
DIØØ thru DI15	Bus Data in from Receivers
DOØØ thru DO15	Bus Data out to Drivers
DRCV	Data received from Memory
DSTD	Data stored in Memory
ED1	Data Driver Enable 1
ED2	Data Driver Enable 2
EDD-	Enable Data Drivers
EOM	End of Message
EROR	Error Indicator
GNB	Get Next Bit
GRN-	Grounding Term - Localized
GWRD	Get a Word from Memory
HBR	Host Bit Ready
HBRD	Host Bit Ready Driver
HBRR	Host Bit Ready Return
HBRS	Set Host Bit Ready
HBRX	Host Bit Ready signal ahead of series resistor
HDA	Host Data Line
HDAD	Host Data Line Driver
HDAR	Host Data Line Return
HDAX	Host Data signal ahead of series resistor
HMRA	Host Master Ready Relay Line A
HMRB	Host Master Ready Relay Line B
HRC	Host Ready Control
HRDY	Host Ready
HRFNB	Host Ready For Next Bit
HRLD	Host Relay Drive
HRR	Reset HRFNB
HRS	Set HRFNB
HRTO	Host Ready Time Out
HRYD	Host Ready For Next Bit Driver
HRYR	Host Ready For Next Bit Return
HRYX	Host Ready For Next Bit signal ahead of series resistor
HSRC	Transmit Shift Register Carry
IBØØ thru IBl5	Input Buffer bits ØØ-15
IBC	Clear Input Buffer
IBE	Clear Receive Register
IBF	Input Buffer Full
IBL	Load Input Buffer
IBR	IMP Bit Ready clocked and latched
IBRD	IMP Bit Ready Driver
IBRL	IMP Bit Ready Line
IBRR	IMP Bit Ready Return
IBRS	IMP Bit Ready Selected
IDA	IMP Data Bit
IDAD	IMP Data Bit Driver
IDAL	IMP Data Bit Line
IDAQ	IMP Data Bit clocked and latched
IDAR	IMP Data Bit Return
IDR	Receiver Register Full
IDS	Set IDR
IEND	Receiver Register has Last Data
IMA-	Increment Memory Address Counter
IMRA	IMP Master Ready Relay Line A
IMRB	IMP Master Ready Relay Line B
INB	Input Next Bit
INEN	Interrupt Enable
INIT-	UNIBUS Initialize
INTI	Device Initialize
INTR-	UNIBUS Interrupt
IRC	Device Interrupting
IRDY	IMP Ready
IRFNB	IMP Ready for Next Bit clocked and latched
IRL	Interrupt Request Latch
IRM	Interrupting Device is Bus Master
IRQ	Interrupt Request
IRQC-	Clear Interrupt Request
IRQS	Set Interrupt Request
IRS	Interrupting Device Selected for Bus Control
IRYD	IMP Ready for Next Bit Driver
IRYL	IMP Ready for Next Bit Line
IRYR	IMP Ready for Next Bit Return
IRYS	IMP Ready for Next Bit Selected
ISR	Input Buffer Strobe
ITB	And of IRDY and IBR-
IWC	Increment Word Counter
LBT	Last Bit being Inputted
LHB	Last Host Bit
LHBD	Last Host Bit Driver
LHBR	Last Host Bit Return
LHBX	Last Host Bit signal ahead of series resistor
LIØØ thru LI15	Receive Register bits ØØ-15
LIB	Last IMP Bit
LIBD	Last IMP Bit Driven
LIBL	Last IMP Bit Line
LIBQ	Last IMP Bit clocked and latched
LIBR	Last IMP Bit Return
LRØ	Load Register Ø (Command and Status Register)
LR1	Load Register 1 (Data Register)
LR2	Load Register 2 (Memory Address Register)
LR3	Load Register 3 (Word Count Register)
LSD	Output Register has Last Data
LSDS	Set LSD
LSR-	Load Output Register
LSTWD	Output Buffer has Last Data
LTØ1- thru LT11-	Indicator Lamp Drivers

MA∅1 thru MA15	Memory Address Bits to Bus
MCLK-	Master Clock Source
MCLK1	Master Clock 1
MCLK2	Master Clock 2
MEC-	Clear Memory Error Indicator
MEMTO	Memory Access Time Out
MMER	Memory Error Indicator
MSNI	Clocked Master Sync In
MSNO	Master Sync to Driver
MSNR	Master Sync from Receiver
MSS	Set Master Sync Out
MSTU	Master Sync for this Unit
MSYN-	UNIBUS Master Sync
MTOC-	Clear Memory Access Time Out
MXD1	Data Multiplexer Disable 1
MXD2	Data Multiplexer Disable 2
MXS∅	Data Multiplexer Select bit ∅
NOMM	Memory Access Error
NPC	Non Process Control (Device Doing DMA)
NPG	UNIBUS Non Process Grant
NPG1	Non Process Grant signal clocked
NPGD	Non Process Grant Delayed
NPGI	Clocked Non Process Grant In
NPGO-	Non Process Grant to Driver
NPGR-	Non Process Grant from Receiver
NPGS-	"OR" of NPGI and NPGD
NPGX	UNIBUS Non Process Grant Propagate
NPM	Device is Bus Master for DMA
NPR-	UNIBUS Non Process Request
NPR1	Not used
NPRQ	Non Process Request to Driver
NPS	DMA Device Selected for Bus Master
OB∅∅ thru OB15	Output Buffer bit ∅∅-15
OBE	Empty Output Buffer
OBF	Output Buffer Full
OBL	Load Output Buffer
OBSTR	Output Buffer Load Pulse
OBT	
PAD	Pad Input Data
PDR	Reset PAD
PDS	Set PAD
PINI	Programmed Initialize (Reset)
PSE∅ thru PSL1	Miscellaneous Address Decode Terms
PUSL	Partial Unit Selection
PWRD	Put Data Word in Memory
R∅STR-	Register ∅ Strobe
RBC-	Reset Bit Counter
REM	Reset End of Message Latch
RGE-	Register Enable
RGO	Register Output
RLER-	Ready Line Error
RLR	Relay Ready
RMRE	Receive Master Ready Error
RR∅-	Read Register ∅
RR1	Read Register 1
RR2-	Read Register 2
RR3-	Read Register 3
S∅T1	Go to State 1 from State ∅
S1T∅	Go to State ∅ from State 1
S2N	EOM Exit of State 2
S2T∅	Go to State ∅ from State 2
S2T1	Go to State 1 from State 2
SACK-	UNIBUS Selection Acknowledge
SACO	Selection Acknowledge to Driver
SAC1	Non Process Selection Acknowledge
SAC2	Interrupt Selection Acknowledge
SB∅	State Counter bit ∅
SB∅R	Reset State Counter bit ∅
SB1	State Counter bit 1
SB1R	Reset State Counter Bit 1
SDA	Output Register has Data
SDE	Reset SDA
SHB-	Shift a Bit
SIR	Set IMP Ready
SS∅	Set State ∅
SS1	Set State 1
SS2	Set State 2
SSNI	Clocked Slave Sync In
SSNO	Slave Sync to Driver
SSNR	Slave Sync from Receiver
SSYN-	UNIBUS Slave Sync
ST∅	State ∅
ST1	State 1
ST2	State 2
STLW	Set LSTWD
USL	Unit Selection
V+∅	Logical One Source ∅
V+1	Logical One Source 1
V+2	Logical One Source 2
V+3	Logical One Source 3
VS∅∅ thru VS∅7	Interrupt Vectors bits ∅∅-∅7
WC∅∅ thru WC15	Word Counter bits ∅∅-15
WCB∅ thru WCB2	Word Counter Borrow Terms
WCC∅ thru WCC2	Word Counter Carry Terms
WCDA thru WCDD	Word Counter Decoding Terms
WCZR	Word Count Equals Zero
WRD	Flush Data Control
XA16	Extended Address bit 16
XA17	Extended Address bit 17
XMRE	Transmit Master Ready Error