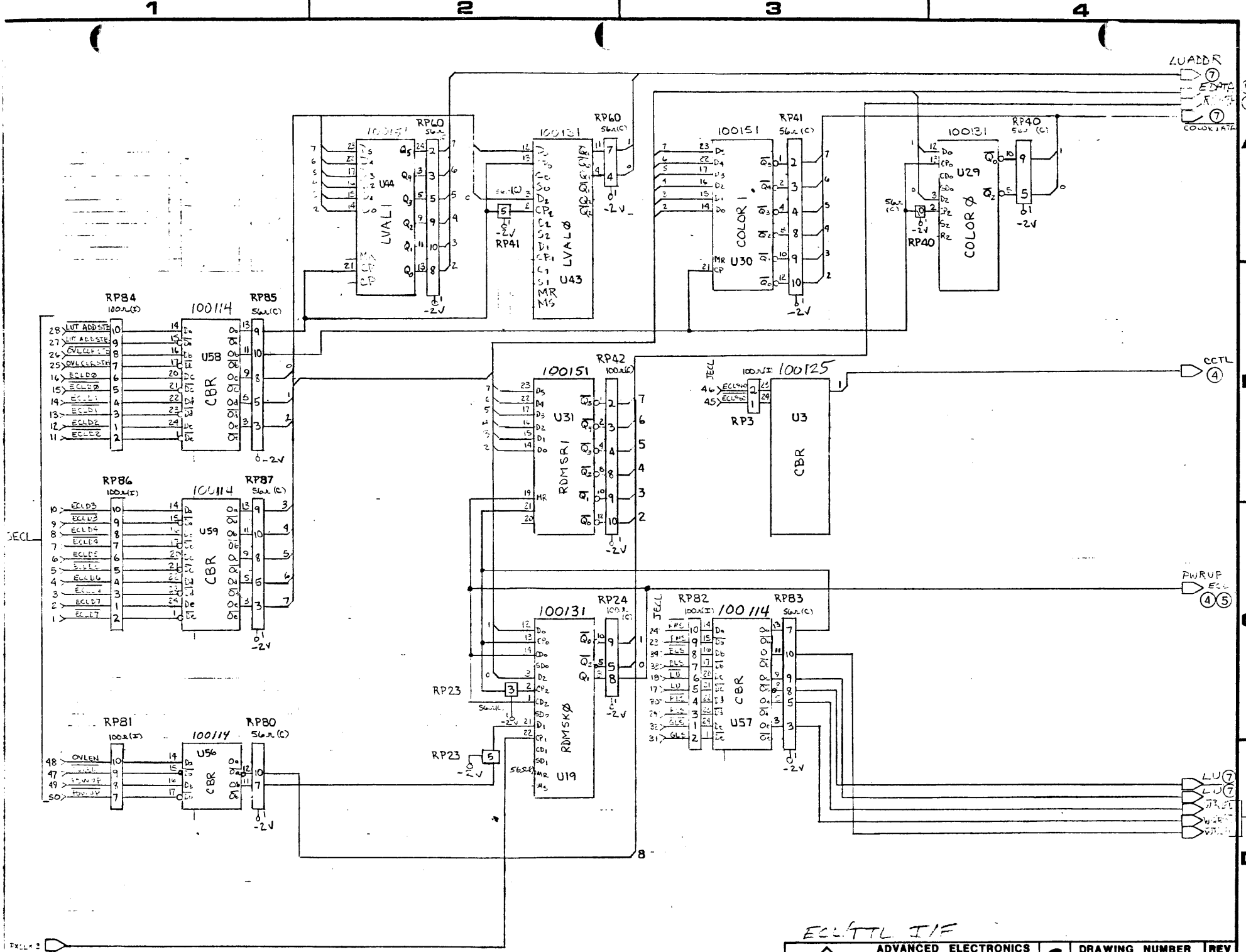


1		
2		
3		5-85

NOTE: ALL 100Ω AND 562Ω RESISTOR NETWORKS ARE 10PIN SIP PACKS.

ECL CLOCK I/F

	ADVANCED ELECTRONICS DESIGN, INC. SUNNYVALE, CALIF. 94086	<b>C</b>	DRAWING NUMBER	REV
			120255-01	A



EXCL 3  
1

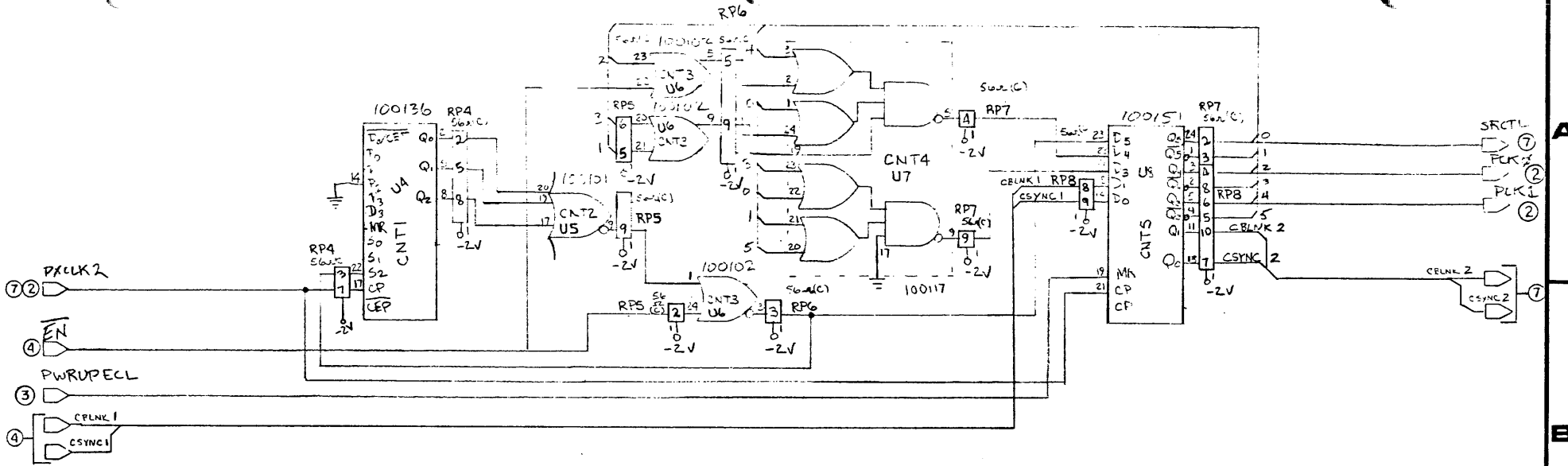
ECL/TTL I/F

ADVANCED ELECTRONICS  
DESIGN, INC.  
SUNNYVALE, CALIF. 94086

DRAWING NUMBER  
12D255-01  
REV  
A

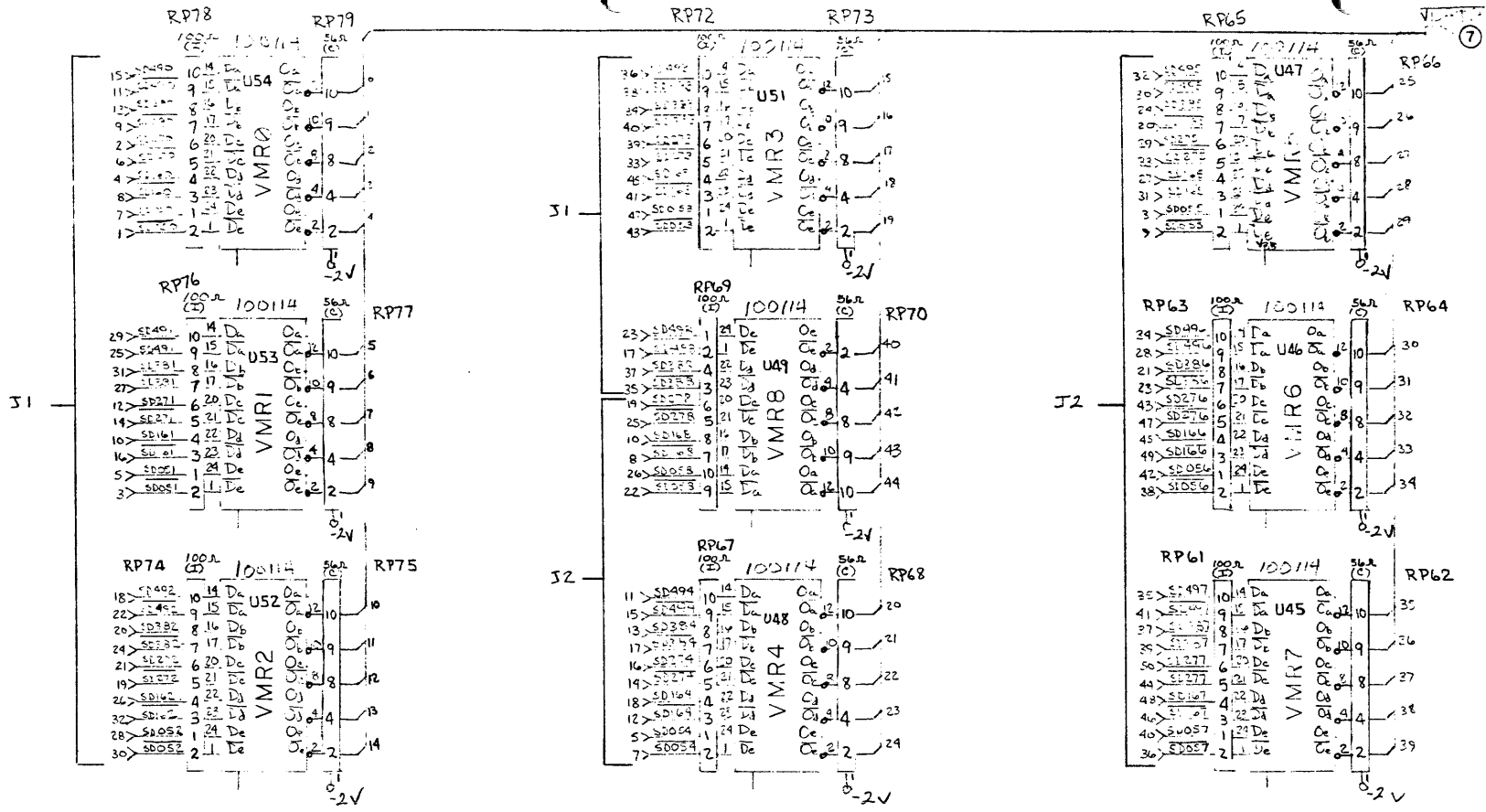
SHEET 2 OF 12





ECL DATA CTL

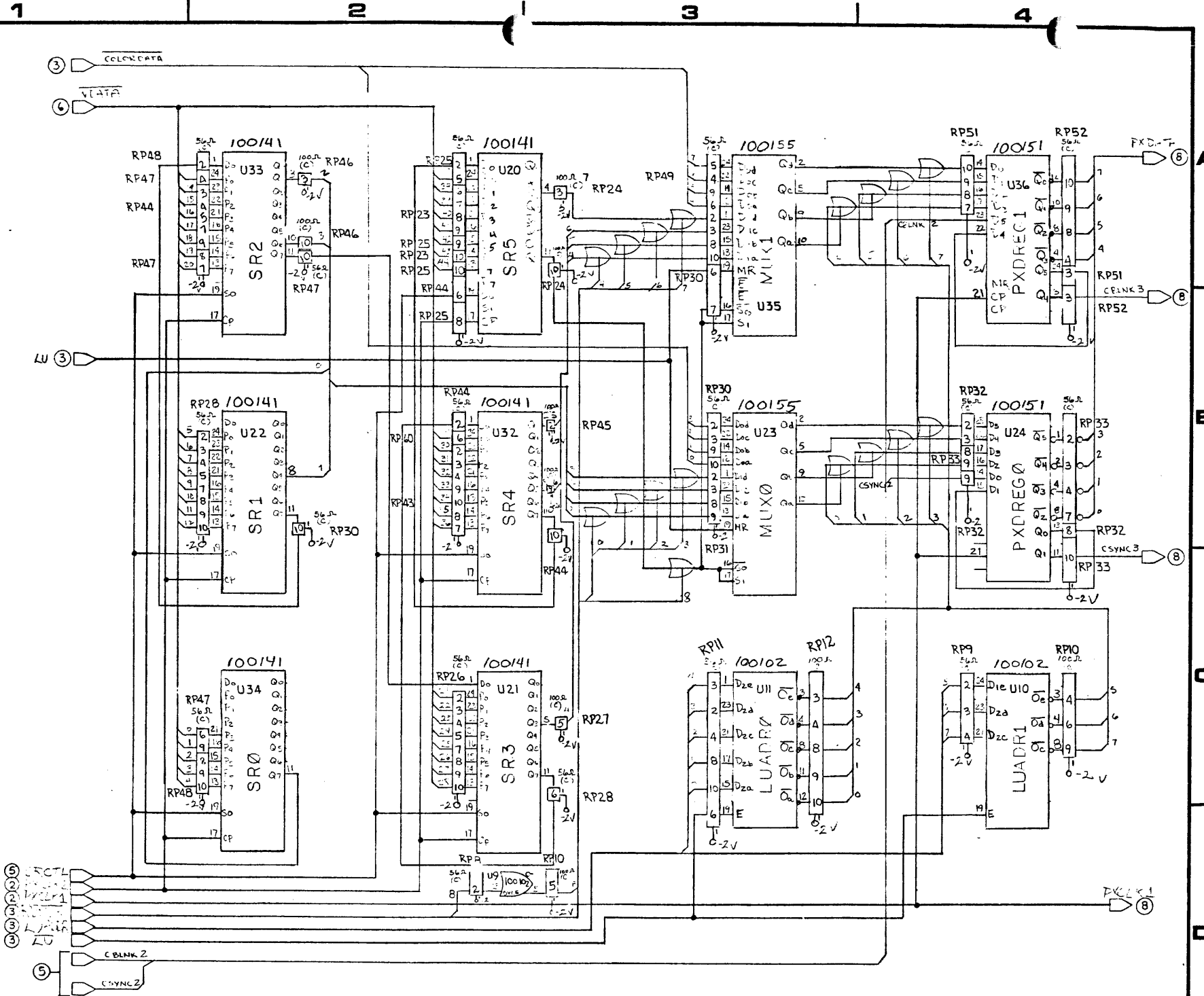
	ADVANCED ELECTRONICS DESIGN, INC. SUNNYVALE, CALIF. 94086	<b>C</b>	DRAWING NUMBER 120258-01	REV A
---------------------------------------------------------------------------------------	-----------------------------------------------------------------	----------	-----------------------------	----------



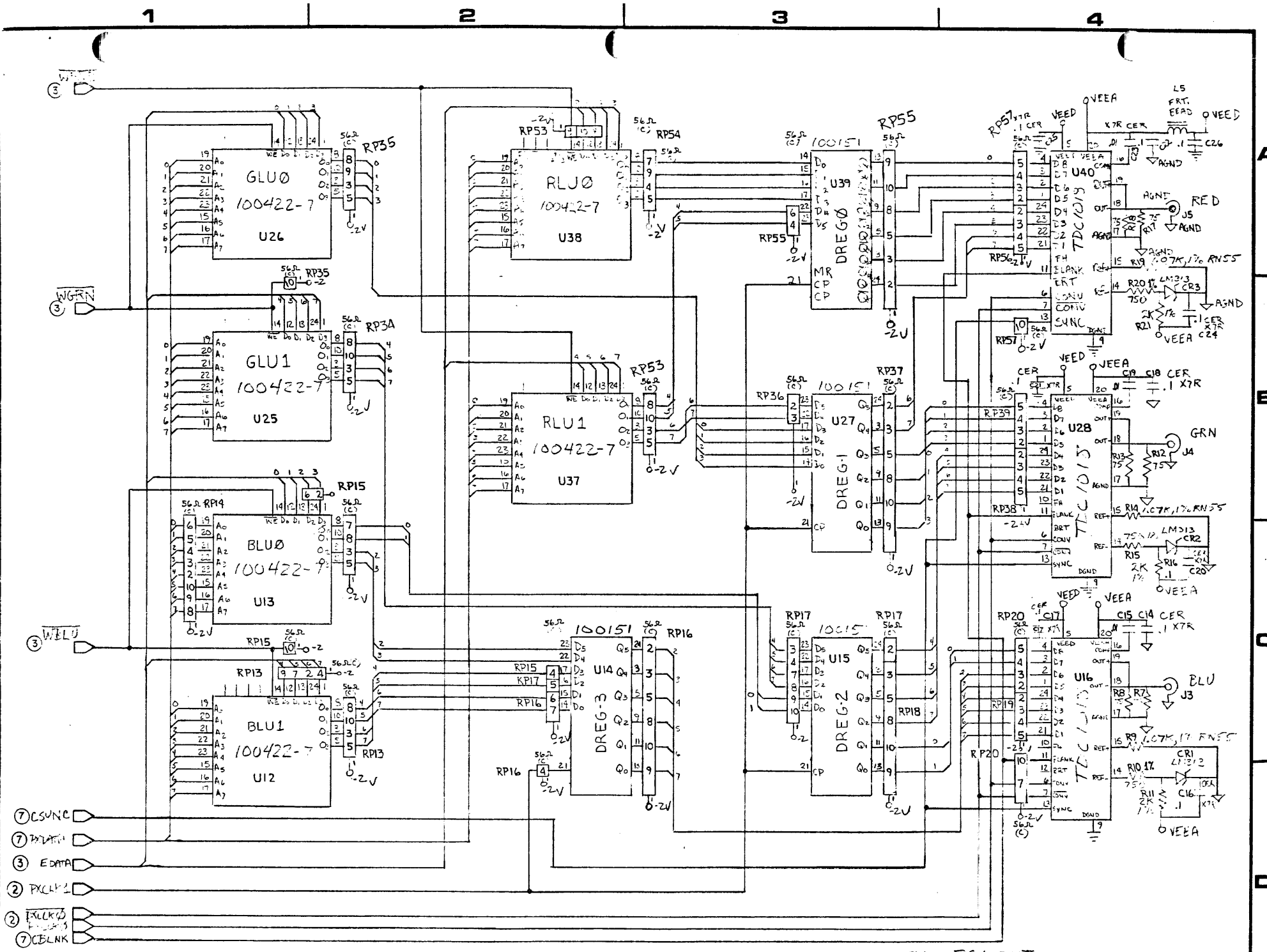
A  
B  
C  
D

VILEDATA

	<b>ADVANCED ELECTRONICS DESIGN, INC.</b> SUNNYVALE, CALIF. 94086	<b>C</b>	<b>DRAWING NUMBER</b> 100253-01	<b>REV</b> A
	SHEET 1 OF 10			



VID SR./ MASK CTL



- ⑦ CSUNC
- ⑦ DATA
- ③ EDATA
- ② PCLK1
- ② PCLK2
- ⑦ CELNK

128 PIN ECOUT



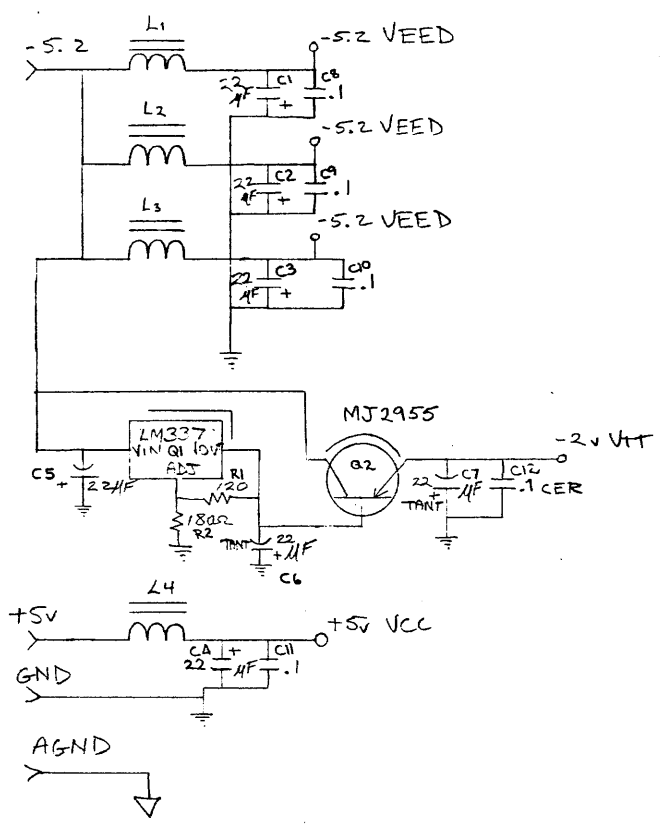
1

2

3

4

NOTES  
 L1-L4 are Fair-Rite shield Beads FA 2643168801 @ 2 TURNS #22 AWG SOLID WIRE  
 22μF, 50V filter caps are Mallory Solid Tantalum Type THF or equivalent  
 .4μF, 50V are Monolithic Ceramic Type Z5U  
 .01, 50V are Monolithic Ceramic Type X7R  
 RESISTORS ARE 5% 1/4 WATT UNLESS NOTED OTHERWISE



ECL ZONER

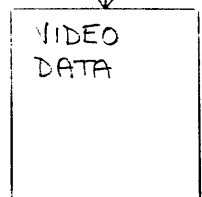
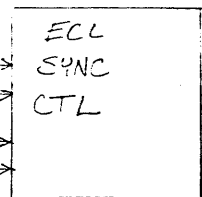
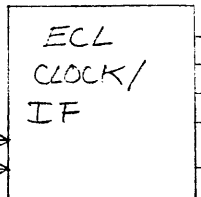
 ADVANCED ELECTRONICS DESIGN, INC. SUNNYVALE, CALIF. 94086	<b>C</b>	DRAWING NUMBER	REV
		120258-01	A

FROM MEMORY PCB

VSD

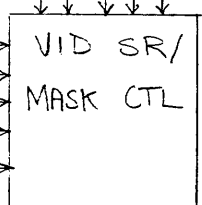
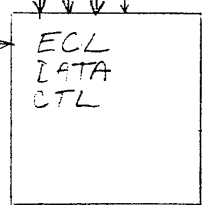
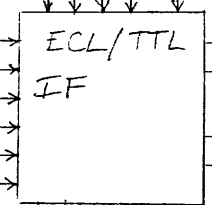
90 (differential)

2 PXCLK/2 (DIFF) TO CONTROL PCB



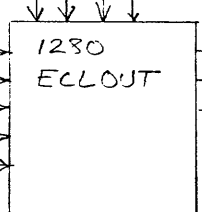
FROM CONTROL PCB

- > GLS 7
- > RLS 2
- > LU 2
- > BLS 2

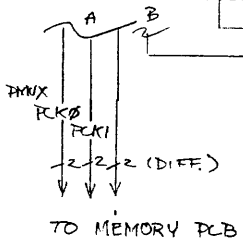


TO CONTROL PCB

- COLORDATA 8
- RDMSK 9
- LDADDR 8
- EDATA 8
- WRFB
- WGRN
- WBLU

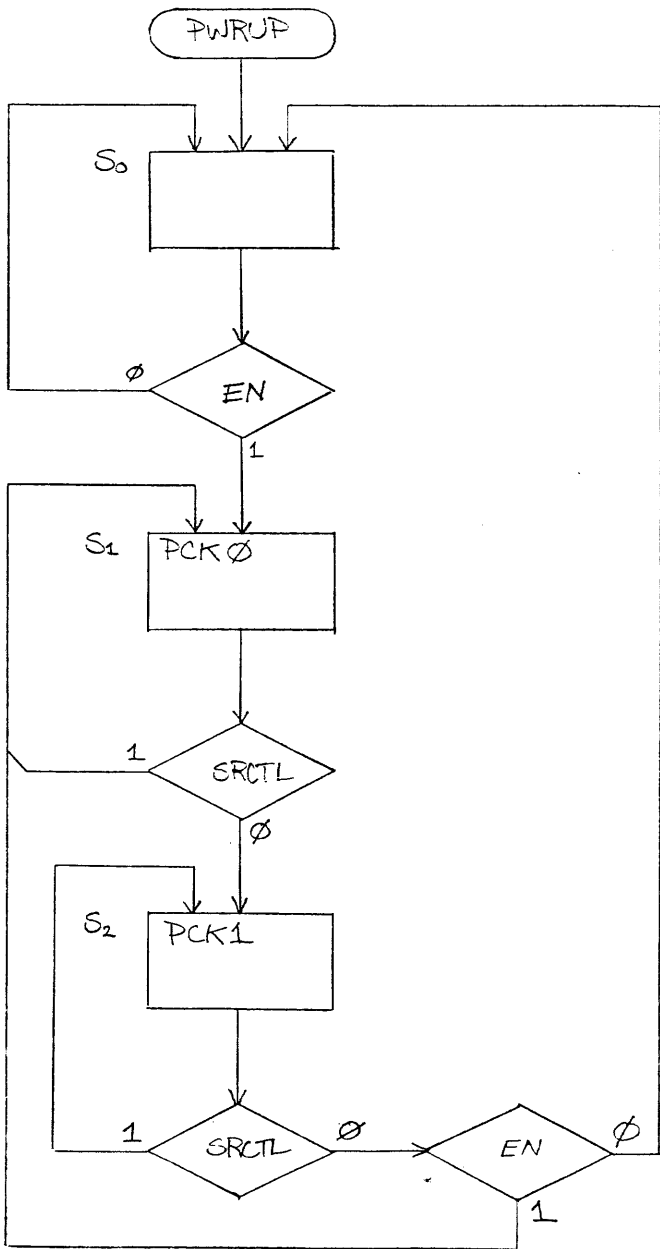


TO BACK PANEL



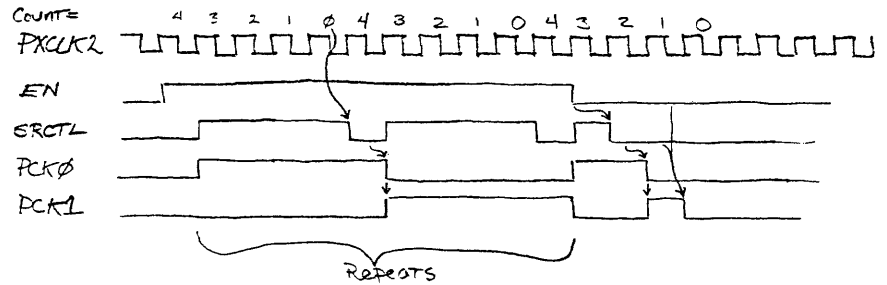
ECL PCB BLOCK DIA

	<b>ADVANCED ELECTRONICS DESIGN, INC.</b> SUNNYVALE, CALIF. 94086	<b>DRAWING NUMBER</b> 120258-01	<b>REV</b> A
	<b>C</b>		<b>REV</b> A



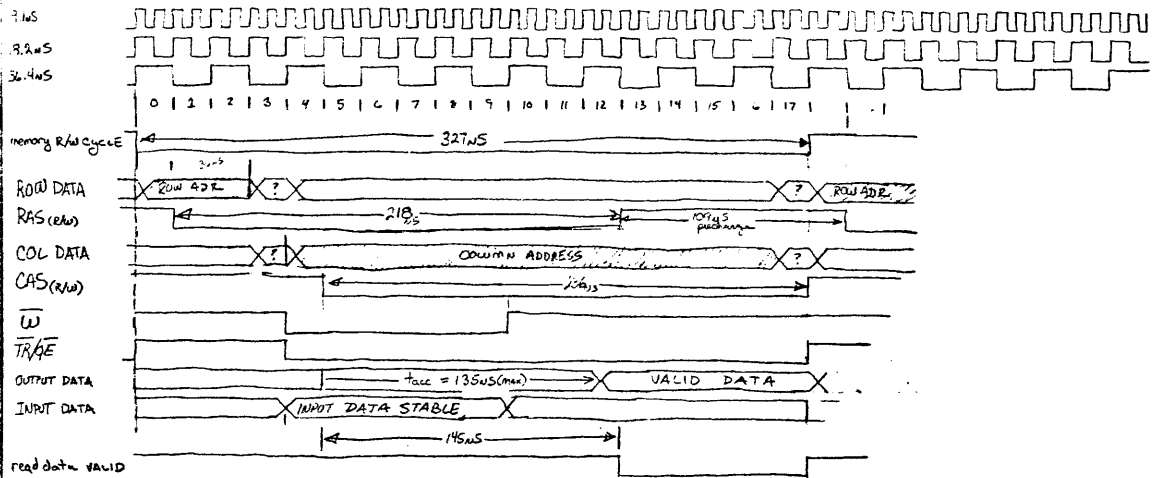
$$\overline{PCK0} = (\overline{PCK0} + \overline{SRCTL}) \cdot (\overline{EN} + PCK0 + PCK1) \cdot (PCK0 + \overline{EN} + SRCTL)$$

$$\overline{PCK1} = (\overline{PCK0} + SRCTL) \cdot (\overline{SRCTL} + \overline{PCK1})$$

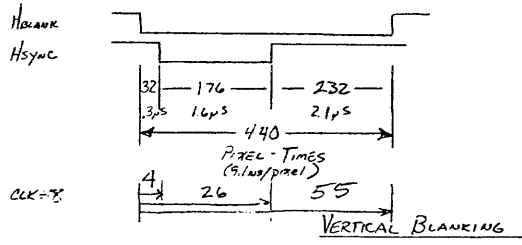


PCK0 = PMUX (switches memory PCB mux between groups of 5x9 4161 Shift Registers)

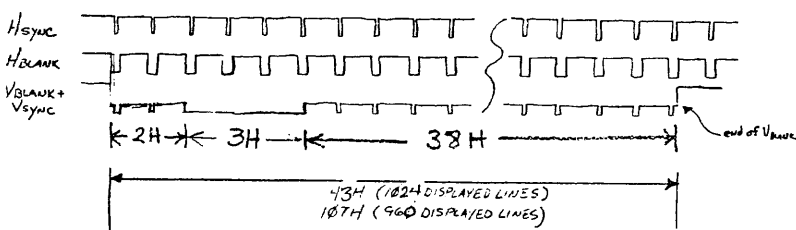
ECL DATA CONTROL SM.



HORIZONTAL BLANKING



VERTICAL BLANKING



1280 MASTER TIMING

$f_{DOT} = 1720 \times 64,000 = 110.080 \text{ MHz}$   
 $f_{VERT} = 64,000 / 1067 = 60.0 \text{ Hz}$

OVERALL DISPLAY TIMING

