DATA DISC, INC.

PRELIMINARY SPECIFICATION

8020 DISC MEMORY SYSTEM

For

DIGITAL EQUIPMENT CORPORATION PDP-11 SERIES COMPUTERS

1.0 General

The 8020 Disc Memory System consists of one Model 8020-C Controller and one to four 8400 or 8500 Series Disc Memory Units. This system operates with any PDP-11 type computer and is compatible with Digital Equipment Corporation operating software. The Disc Memory System is functionally equivalent to the DEC RC-11/RS-64 Disc and Control. The 8020 can be expanded beyond the RC-11/RS-64 maximum storage capacity of 262K words to a total capacity of 8,388K words. Data is available at either 8.6 or 17.2 milliseconds average access time.

2.0 Reference Documents

2.1 PDP-11 Processor Handbook

2.2 PDP-11 Peripherals and Interfacing Handbook

2.3 Data Disc 8400 Series Disc Memory Interface Manual

3.0 Data Format

Capacity (16 bit words)	131,072 to 8,388,608
Words per Track	8,192
Words per Sector	32
Sectors per Track	256
Tracks per Disc Unit	16 to 256

4.0 Timing Specifications

	Disc Model	
	8410	8430
Average Access Time	17.2 msec	8.6 msec
Worst Case Access Time	34.4 msec	17.2 msec
Peak Data Transfer Rate	3.48 usec/wd	1.74 usec/wd

Average Data Transfer Rate	8410	8430
at 1:1 interlace	4.24 usec/wd	2.12 usec/wd
at 2:1 interlace	8.48 usec/wd	4.24 usec/wd
at 4:1 interlace	16.96 usec/wd	8.48 usec/wd
at 8:1 interlace	33.92 usec/wd	16.96 usec/wd

(Timing shown at 60Hz and 50Hz with disc pulley/belt modification kit. At 50Hz without modification kit, increase indicated timing characteristics by a factor of 1.2)

5.0 System Operation

Each disc track is divided into 256 sectors, each of which contains 32 words of data plus a 16-bit cyclic check word. The cyclic code word is generated and checked automatically by the controller. Sectors are interspersed across the track depending on the interlace factor wired for the controller. If the interlace factor is N, then there are N-1 sectors located between two consecutively numbered sectors. Sector interlacing is used to change the average data transfer rate of the disc memory. It allows the disc speed to match the transfer speeds desired on the PDP-11 computers. The interlace factors specifiable on the controller are 1:1, 2:1, 4:1, and 8:1.

The 8020-C controller will interface to the PDP-11 using standard UNIBUS™ conventions. The controller can be strapped to interrupt on any BR level (BR5 standard). The interrupt vector is settable (210_8 standard). Control and status word transfers use the UNIBUS with the controller as slave. Data transfers to and from the disc use the NPR bus controls.

6.0 Controller Instructions

The Controller has six registers that are accessible to the programmer.

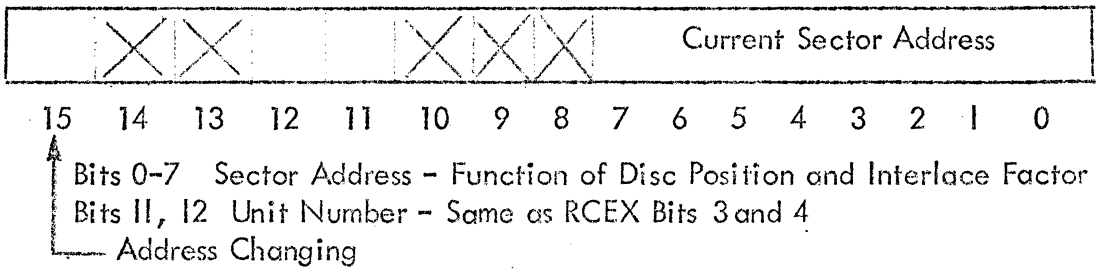
Register Description	UNIBUS Address	Comments
Look Ahead Register RCLA	777440	Read Only
Disc Address Register RCDA	777442	Read/Write
Disc Error Status Register RCER	777444	Read Only
Command & Status Register RCCS	777446	Read/Write
Word Count Register RCWC	777450	Read/Write
Current Address Register RCCA	777452	Read/Write
Disc Address Extension Register RCEX	777454	Read/Write
Data Buffer	777456	Not Implemented

sync on u91-1 thur 9 see 20

6.1 Look Ahead Register (RCLA = 777440)

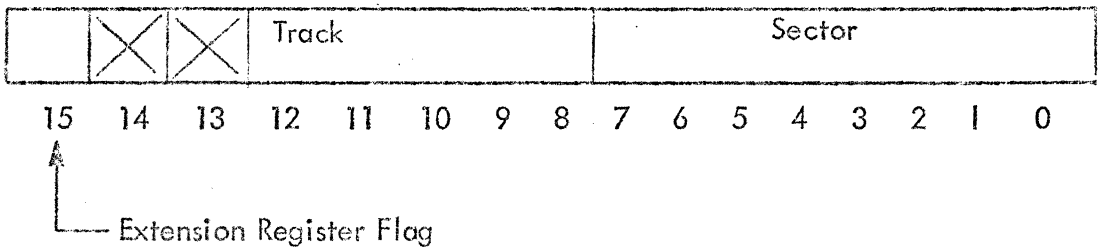
This register contains the address of the sector currently under the Read/Write head. Because the sectors are interlaced, the contents of the look ahead register do not indicate consecutively numbered sectors. For a 2:1 interlace factor the sector addresses encountered are:

0, 128, 1, 129, ... 126, 254, 127, 0, 128, ...



When bit 15 is set, an unstable address condition is indicated. The register should be read again.

6.2 Disc Address Register (RCDA = 777442)



Before any transfer between the controller and disc memory, the controller must locate the addressed Sector. The Disc Address Register is loaded with a number that selects one specific Sector of one Track. If multiple sector operation is required (word count is greater than 32) the RCDA is automatically incremented.

The RCDA is read/write register, all bits initialized to zero.

6.3 Disc Error Status Register (RCER = 777444)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		X		X	X	X	X	X	X			X	X	X	X

Bit 4: MT — Missed Transfer - Sets to indicate that the Controller did not make a NPR for data transfer since initiating a function and the disc revolved more than once.

5: EOD — If the disc address register (RCDA) overflows (a carry out of RCDA12 occurs), the unit number changes from disc unit 3 to disc unit 0. This bit is set to prevent wraparound transfers. This bit is read-only; it is cleared by initialization or by starting an RCII operation.

Bit 12: NEM — Non-Existent Memory - Sets if Controller initiates a UNIBUS data transfer and does not receive a slave sync signal (SSYN) within 20 microseconds after it asserted Master Sync (MSYN). This condition usually indicates that no register or memory has been assigned to that address.

14 BCER — Block-Check-Error - Sets if the Cyclic Redundancy Check (CRC) that is read back from the disc does not agree with the computed check on the data just read. The current operation will not be absorbed if BCER sets.

15: DRL — Data Overrun - This bit is set to indicate that the computer has failed to keep pace with the disc. This is generally due to conflicts on the bus slowing the effective transfer rate.

The RCER is read only. All bits are initialized to zero.

6.4 Disc Command and Status Register (RCCS = 777446

Bit 0: GO -Setting initiates the function specified. Write only and initialized to zero.

1,2 FUNCTION - Specify the desired operation. Controller decodes these bits as follows:

Bit 2	Bit 1	Function
0	0	No operation
0	1	Write
1	0	Read
1	1	Write Check

These bits are read/write and initialized to zero.

3 DIAGNOSTIC - This Bit does nothing and is Read/Write

4,5 EXTENDED MEMORY - Two most significant bits when 18 bit address is in effect. These two bits are logical extension of the Current Address Register (RCCA). These are read/write and initialized to zero.

6: INTERRUPT ENABLE - Program Interrupt will be allowed to occur only when this bit is "1". This bit is read/write and initialized to zero.

7: READY -Controller sets this bit to indicate completion (or abortion) of an operation and is ready for the next operation. This bit is read only and initialized to "1".

8: ABORT -If declared as "1" any operation in program is aborted, and interrupt generated (if Enabled). This bit is write only and initialized to zero.

10 WRITE CHECK This bit is set if, during a write check operation, the comparison of the data from the Unibus and from the disc indicates any differences. This error condition does not cause an immediate halt to the write check operation; the operation is completed to compare the block check words. This bit is read-only; it is cleared by initialization or by starting an RCII operation

11: NON-EXISTENT DISC - Indicates that the contents of the Disc Address Register (RCDA) and Address Extension Register (RCEX) exceeds the actual number of tracks available and the word transfer did not finish yet.

Note that this bit will be "1" only when the Word Count Register did not overflow so that last Sector of the last Track can be operated on without getting an error status.

12: WRITE LOCK - Set to indicate that a write attempt was made on a write-protected area of the disc. This bit is read only and initialized to zero.

13: ADDRESS ERROR - Logical OR of Error Status bits NEM (bit 12) and MT (bit 4) of RCER register.

This bit is read only and initialized to zero.

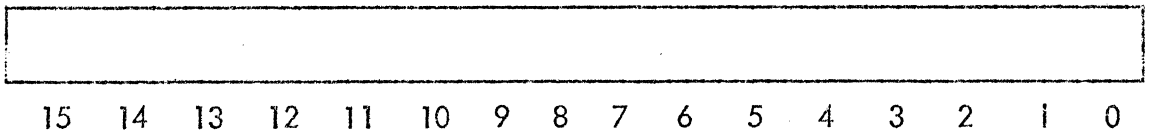
14: DATA ERROR - Identical with bit 14 of RCER register.

This bit is read only and initialized to zero.

15: SPECIAL CONDITION - Set to indicate that the Controller sensed an error condition. It is logical OR of bits 11 - 14 of this register and RCER register.

This bit is read only and initialized to zero.

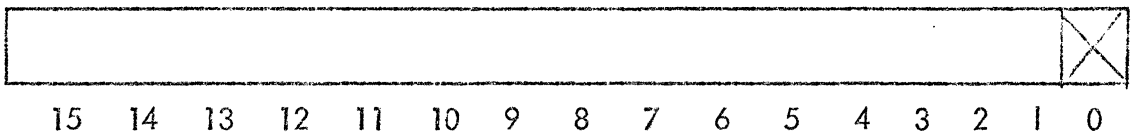
6.5 Word Count Register (RCWC) = 777450



0-15 Word Count -This register is loaded with the 2's complement of the block length and incremememented by one after each transfer. When the content of this register has been incremented to zero an overflow signal will end the operation. By definition the block size is limited to 65.536(2^{16}) words.

This register is read/write

6.6 Current Address Register (RCCA = 777452)



Before initiating any transfer operation the program declares the address of the UNIBUS location with which the controller should start data transaction. All data transfers take place at even address boundaries (no byte capability). After each data transfer this register is incremented by two. When this register overflows, extended memory bits in RCCS are incremented. Bit 0 of this register is always zero, and remaining bits are read/write.

6.7 Address Extension Register (RCEX, = 777454)

This register contains extension addresses of the Disc Address Register (RCDA) and allows up to 256 track selections. Selection of up to four disc devices is accomplished with bits 3 & 4. If the contents of this register are non zero the Extension Register Flag bit (bit 15) of the Disc Address Register (RCDA) is set to 1. This register is read/write, initialized to zero and incremented by the roll-over of RCDA.

15 14 13 12 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit 0 - Track Address Bit 6
1 - Track Address Bit 7
2 - Track Address Bit 8

Bit 3,4 - Unit Select

00 - Unit 1
01 - Unit 2
10 - Unit 3
11 - Unit 4

Bits 5-15 Not Used

7.0 Programming Considerations

This controller is designed to be equivalent to the DEC RC-11 System. The control registers available to the programmer are the same ones implemented in the RC-11 System. There are some additional programming considerations required because the 8400 recording density and transfer rates are so much greater than those encountered in the RC-11 System. In particular, the data are recorded in an interlaced sector mode to allow high density recording without excessive loading of the UNIBUS during transfers. The interlacing factor can be set by the systems user to 1:1, 2:1, 4:1, or 8:1. In general, the greater the interlace factor the lower average transfer rate required to keep up with the disc. The penalty for not keeping up is inefficient transfers and possible detected timing errors requiring transfer retries.

In general the programmer need not consider the interlace factor except in the case where the look ahead register is being used to optimize transfer sequences. The interlace factor will determine the pattern of addresses which appear in sequence in the look ahead register. To properly interpret these addresses, the programmer must be aware of the expected sequence. When, for example, interlace factor of 2:1 is selected it simply means that sequentially number sectors occupy every other physical sector on the disc. This implies that on one revolution of the disc only one half of the total physical sectors on a track can be accessed. Then on the next revolution the alternate physical sectors may be accessed. There is a corresponding pattern with 4:1 and 8:1 interlace factors. The numbering of physically adjacent sectors for 2:1 interlace is 0, 128, 1, 129 . . . . 127,255. This is the sector address sequence which will be seen in the look ahead register. If, for example, the look ahead register contains a sector address of 128, the next available sector is sector 1, not sector 129.

The system is designed around a sector length of 32, 16 bit words. Multiple sector writes are automatically completed on sequentially number sectors.

Transfer status can be monitored in the classic ways. The program may simply test the DONE bit (bit 7 in the Control/Status word) and wait for transfer completion. In interrupt driven systems, setting bit 6 in the control/status register will cause an interrupt when DONE is asserted. The DONE bit is initialized to a logical 1 state upon power up, master clear, etc. This implies that if interrupts are enabled before a transfer is started, an interrupt will be generated. Furthermore, each transition of the interrupt enable bit from off to on will result in another interrupt.

If interrupts are enabled and the Go bit (Bit 1 of the Control/Status register) is set at the same time, no interrupt will be generated because GO rests DONE.

After each transfer, the program should test the SPECIAL CONDITION bit (Bit 15 of the Control/Status register). If an abnormal condition has been detected by the Controller this bit will be set, otherwise a perfect transfer sequence occurred. If bit 15 is found set, the program must check the error status bits to determine the error and make the appropriate response.

8.0 Error Checking

In writing, a 16 bit cyclic check word is written at the end of each sector. In reading each sector, the cyclic code is read and compared against the code which was generated from the previous 16 words.

If they do not match the BCER status flag (Bit 14 of RCER) and the Data Error status flag (Bit 14 of RCCS) are set. The current read operation will not be terminated by the data error. The cyclic code generator uses equation $1 + X^2 + X^{15} + X^{16}$.

9.0 Function Verification Program

A program is supplied to allow verification of proper disc/controller operations.

10.0 Physical Description

The 8020 Disc Memory System consists of the Model 8020-C Controller, a Model 8410 or Model 8430 Disc Memory Unit, and an optional chassis with integral 8020-P Controller Power Supply and the disc to controller interconnecting cable.

The 8020-C Controller consists of two printed circuit cards mounted in a DEC System Unit Block. Optionally the Controller can be supplied in a 19 inch rack mountable chassis containing an integral D.C. Power Supply (Model 8020-P), with a 5 1/4 inch panel height and a 21 inch depth.

The Disc Memory Unit including its self-contained D.C Power Supply is a 19 inch rack mountable assembly 8.75 inches high with a 21.2 inch depth.

The UNIBUS is connected to the controller using standard DEC UNIBUS receptacles. Provision is made to loop the UNIBUS cable through the controller or to terminate the UNIBUS on the controller.

11.0 Power Requirements

The 8400 Series Disc Memory Units operate on 115 VAC, 50 or 60 Hz power. The Disc Memory Unit requires 8.3 amps start current and 2.3 amps operating current. The Model 8010-C Controller will require 6 amps of +5 VDC.

12.0 Environmental Conditions

The 8020 Disc Memory System will meet the same environmental conditions specified for the 8400 Series Disc Memory Unit.