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Mass Storage Subsystem

User's Manual

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PREFACE

This manual provides information on the 6100 Series Mass Storage Subsystem. This subsystem can store 10M bytes of data on a fixed disk drive and 500K bytes on a removable floppy disk drive. It is Multibus† compatible.

Chapter 1 describes the system and its components, and lists pertinent specifications.

Chapter 2 provides initialization and installation instructions. Installation with several different AMC Multibus systems is described.

Chapter 3 includes general operating practices. This manual contains no details on equipment operation. Consult the appropriate software manual for this information (e.g., AMDOS User's Manual).

Appropriate drawings are included to aid in understanding the subsystem and its interface.

For more detailed information, consult the following documents.

AMDOS User's Manual Revision B	AMC	059910425-001
8100 Series Microcomputer Development System, User's Manual	AMC	059910671-001
DTC-86 Host Adapter for Intel Multibus System, Product Specification, May 5, 1981	Data Technology Company	
SA1000 Fixed Disk Drive, OEM Manual	Shugart Associates	39010-1
SA1400 Series Disk Controller, OEM Manual	Shugart Associates	39016-0

†Multibus is a registered trademark of Intel Corporation

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CHAPTER 1

GENERAL INFORMATION

INTRODUCTION

The 6100 Series is a mass storage subsystem for use with Multibus computer systems. It consists of a cabinet containing a Winchester disk drive, an 8-inch flexible disk drive, a controller card, and a power supply; a separate host interface card to place inside the Multibus chassis; control software contained in PROM devices; and interconnection cables. The Winchester disk capacity is 10M bytes (unformatted), and the floppy disk capacity is 512K bytes. This configuration allows easy backup of data from the Winchester disks to removable floppy disks.

PHYSICAL DESCRIPTION

The disk drive cabinet is made of formed steel with a front bezel of heavy-duty plastic. The cabinet holds an 8-inch Winchester-type fixed disk drive with two disks and four heads in a sealed chamber, an 8-inch floppy disk drive, a disk controller card, and a power supply. The controller card is mounted inside the cabinet, and connects to both of the disk drives via the interior wiring harness. Connections between the disk cabinet and the host Multibus chassis are made through the connectors on the rear panel. Four of these are 50-pin connectors, and one is a 20-pin unit. This panel also contains the ac input connector, power switch, fuse, and ventilating fan. Two additional jacks allow connection of two remote power control cables to two other chassis.

Either one or two 50-conductor cables connect the disk cabinet to the Multibus chassis, depending upon the installation configuration. These are flat cables inside a protective insulating sleeve. A separate cable connects to the interface card, which mounts inside the host Multibus chassis. This card is 12 inches by 6.75 inches, and is fully Multibus compatible, both physically and electrically.

Figure 1-1 shows the disk cabinet and the Multibus interface card. Table 1-1 summarizes the physical specifications of the unit.

FUNCTIONAL DESCRIPTION

This unit provides mass storage for a Multibus computer system, such as the AMC 8100 Series. Figure 1-2 identifies the major components of the subsystem. The Winchester disk has four surfaces, each accessed by a separate head. It provides 8.4M bytes of formatted data storage capacity on its sealed and protected surfaces. The floppy disk drive format is either single-sided, double-density, with a 512K byte capacity per disk (compatible with the IBM System 34 soft sector

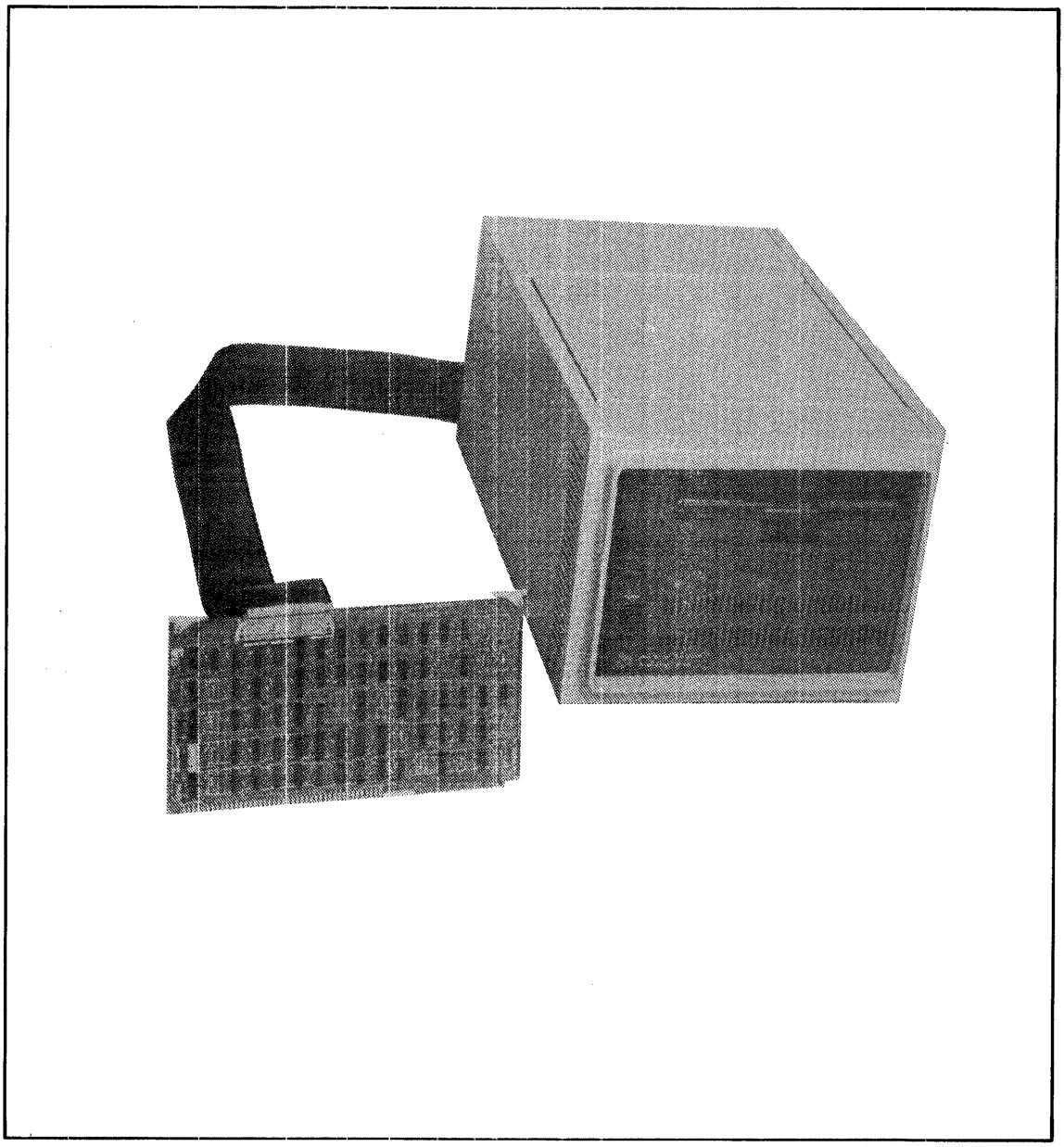


Figure 1-1. 6100 Series Disk Cabinet and Multibus Interface Card

format); or single-sided, single-density, with 256K byte capacity (compatible with the IBM 3740 format). With this arrangement, a large amount of data can be available for quick access from the fixed disk, and it can be easily saved onto floppy disks for backup storage.

All disk operations are overseen by the disk controller card inside the disk cabinet. This card formats and buffers data for transfer between a maximum of four disk drives and the Multibus interface card. It provides appropriate error checking and correcting facilities for all of the drives.

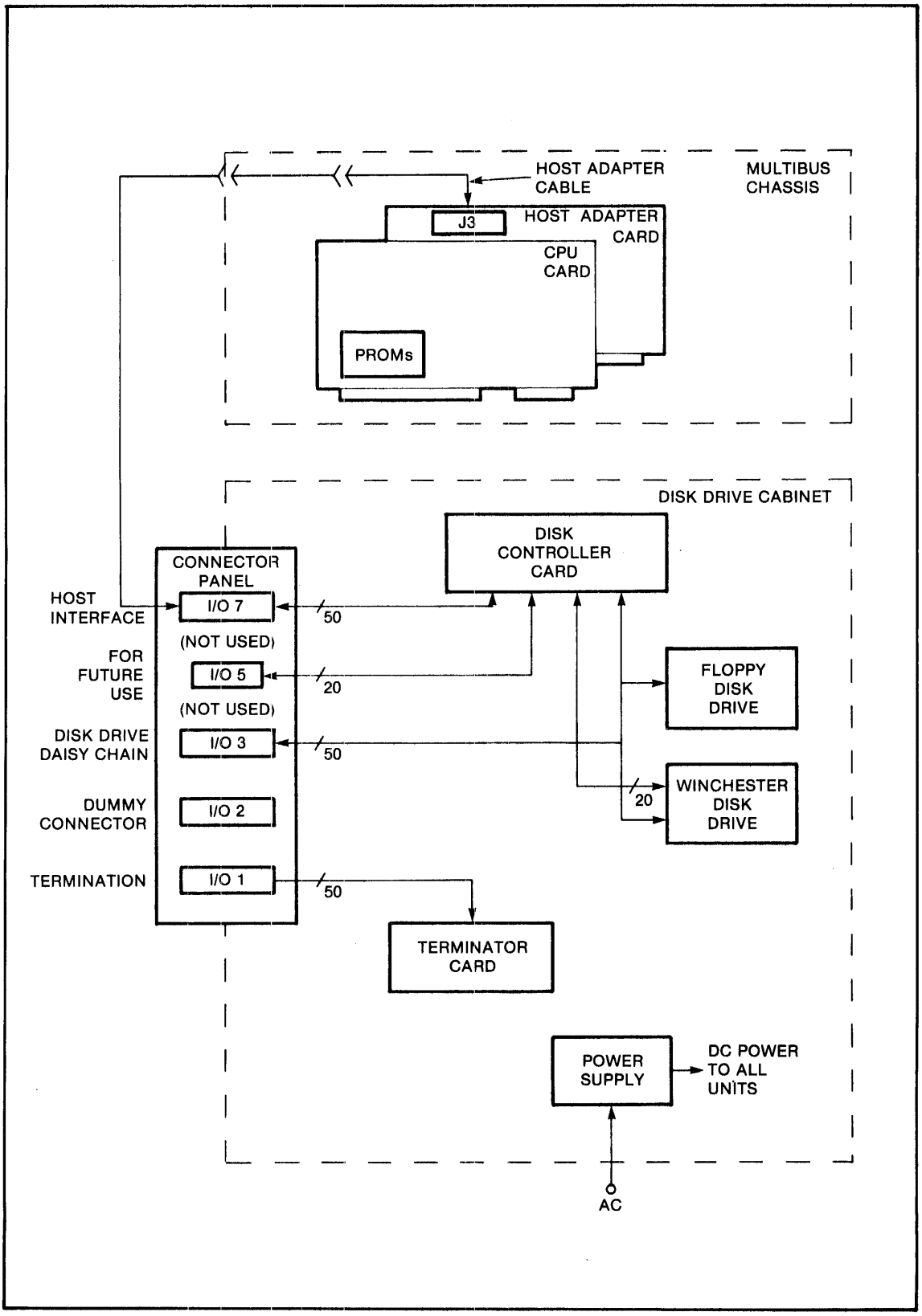


Figure 1-2. Mass Storage Subsystem Components

TABLE 1-1. PHYSICAL SPECIFICATIONS

	OPERATING	STORAGE
Temperature Humidity	10-40°C (50-104°F) 10%-80% (no condensation)	0-75°C (32-167°F) 10%-95% (no condensation)
	DISK CABINET	HOST ADAPTER CARD
Height Width Length Weight	267.0 mm (10.5 in) 330.0 mm (13.0 in) 610.0 mm (24.0 in) 35.4 kg (78 lbs)	12.4 mm (0.50 in) 171.4 mm (6.75 in) 304.8 mm (12.00 in) 0.5 kg (1.10 lbs)
Disk Cabinet Power:		
VOLTAGE (V ac)	FREQUENCY (Hz)	FUSING (Amps)
90-105 108-126 198-231 216-252	50/60 ± 0.5† 60 ± 0.5 50 ± 0.5 50 ± 0.5	6.25 5.00 3.00 3.00
Host Adapter Card Power: +5 VDC at 2.5 A (maximum)		

†The power supply operates at only one frequency; either 50 or 60 Hz is specified at purchase.

A second card, the host adapter card provides a register-buffered interface between the disk controller and the Multibus. Direct memory access is provided by an 8- or 16-bit data path and 16- or 20-bit addressing as specified by the user. Once a disk command is initiated, the host adapter is responsible for arbitrating access to the disk controller bus and data transfers that occur on that bus. On the Multibus side, the host adapter is responsible for bus arbitration and DMA data transfers; it also generates an interrupt when the command terminates. Appendix A contains details on the software interface provided by the host adapter card.

The host adapter card resides inside the Multibus chassis, and requires only +5 volts for power from that bus. All power for the cabinet mounted components of the Mass Storage Subsystem is derived from the internal dc power supply. There is a separate fuse to protect this unit. The remote control cable can be connected between the Multibus chassis and the disk cabinet, allowing both units to be activated from the Multibus power switch.

Table 1-2 summarizes functional specifications of the subsystem.

TABLE 1-2. FUNCTIONAL SPECIFICATIONS

	FLOPPY DISK DRIVE	WINCHESTER DISK DRIVE
Recording Media	One removable disk, 8-inch diameter	Two non-removable disks, 8-inch diameter
Disk Surfaces	1	4
R/W Heads	1	4
Formatting Single Density (SD)	IBM 3740 compatible	N/A
Double Density (DD)	IBM System 34 Soft-Sector compatible, except side 0, track 0 (single density)	Modified IBM System 34 Soft-Sector
Tracks/Surface	77	256
Sectors/Track	26	32
Bytes/Sector	128 (SD) 256 (DD)	256
Data Coding	FM (SD) MFM (DD)	MFM
Capacity Per Drive (Formatted)	250K bytes (SD) 500K bytes (DD)	8.4M bytes
Transfer Rate	250K bits/s (SD) 500K bits/s (DD)	4.34M bits/s
Access Time Track to Track Average	 8ms 260ms	 19ms 70ms
Average Latency	83ms	9.6ms
Rotational Speed	360 rpm	3125 rpm

CHAPTER 2

INITIALIZATION AND INSTALLATION

INTRODUCTION

This section provides instructions for initializing and installing the 6100 subsystem in a Multibus environment. Specific details are included for several different AMC chassis.

UNPACKING AND INSPECTION

Inspect the shipping cartons immediately for evidence of mishandling during transit. When there is evidence of severe damage or water stains, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present and the contents are damaged, retain the carton and all shipping materials for the agent's inspection. Report all shipping damages to the carrier immediately upon detection.

NOTE

If there is evidence of damage to the equipment, do not attempt any servicing. Any attempt at servicing the equipment without the consent and coordination of the Advanced Micro Computer Field Service Manager voids the warranty.

Save salvageable shipping materials in case the product must be shipped in the future.

After all the equipment is removed from the shipping cartons and there is no obvious shipping damage, remove the packing slip and inventory the equipment received against the shipping list. If discrepancies are noted, notify AMC immediately.

INITIALIZATION AND OPTION SELECTION

This section identifies options available to the user and how to select them.

HOST ADAPTER CARD

The host adapter card is installed inside the Multibus chassis. Check the card for proper configuration as described in this section.

I/O Ports: Base Address Selection

The software interface between the Multibus CPU and the disk controller card is provided by registers on the host adapter card. The CPU can read from and write to these I/O ports to start command execution. For 16-bit address systems, six ports are used; for 20-bit address systems, eight ports are required (table 2-1).

The base address of these ports is selected by the DIP switch at location 3N (figure 2-1) as described in table 2-2.

TABLE 2-1. HOST ADAPTER I/O PORTS

MEMORY ADDRESS	I/O PORT
Base + 7	Command Address Top†
Base + 6	Data Address Top†
Base + 5	Command Address High
Base + 4	Command Address Low
Base + 3	Data Address High
Base + 2	Data Address Low
Base + 1	Command Completion Status Register
Base + 0	Channel Status Register

†Required only for 20-bit addressing

TABLE 2-2. I/O PORT BASE ADDRESS DIP SWITCH SETTINGS

SWITCH POSITION	BASE ADDRESS BIT	AMC CONFIGURATION 8100 Series (Addr=A0H)
8	Not Used	Don't Care
7	Not Used	Don't Care
6	Not Used	Don't Care
5	B7 (MSB)	On (Closed)
4	B6	Off (Open)
3	B5	On
2	B4	Off
1	B3	Off
None	B2	0
None	B1	0
None	B0	0

Off = Logical 0
On = Logical 1

Interrupt Line

Select either none or only one interrupt line of the eight available lines by setting the DIP switch at location 5E (figure 2-1). Ensure that only one switch is set ON, otherwise results are inconsistent (table 2-3).

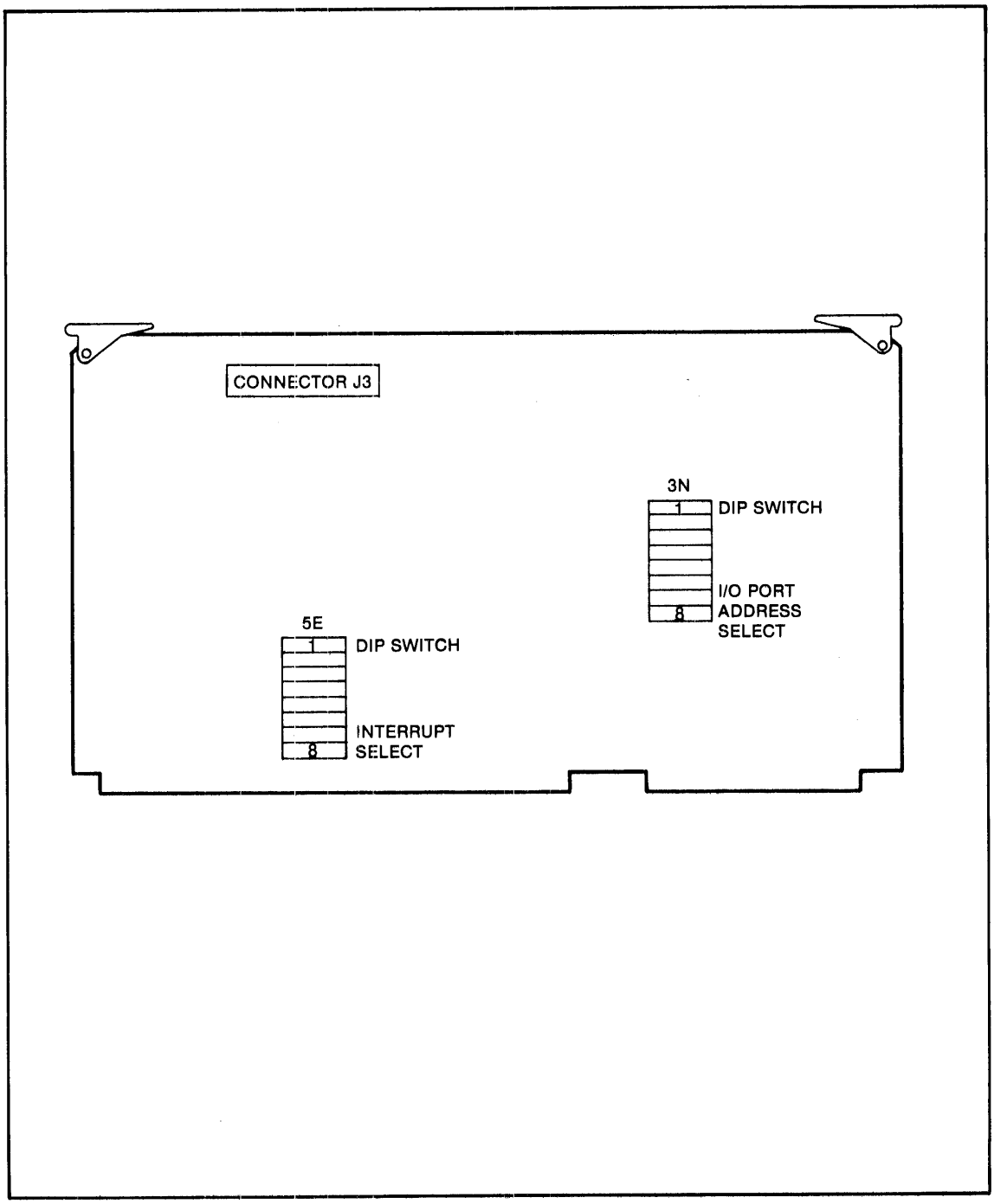


Figure 2-1. Host Adapter Card Layout

TABLE 2-3. INTERRUPT SWITCH SELECTION

SWITCH POSITION	INTERRUPT LINE	AMC CONFIGURATION 8100 SERIES
SW1	INT0	Off (Open)
SW2	INT1	Off (Open)
SW3	INT2	Off (Open)
SW4	INT3	Off (Open)
SW5	INT4	Off (Open)
SW6	INT5	Off (Open)
SW7	INT6	Off (Open)
SW8	INT7	Off (Open)

Multibus Address

The host adapter can be set up to provide either 16-bit or 20-bit addresses (table 2-4). As supplied, either addressing mode can be used. When using less than 20 bits, force the top address bits to zero in the software driver routine (see example in software interface appendix).

Multibus BHEN (Byte High Enable) Signal

Multibus cards which allow 16-bit data transfers use BHEN; cards which do not allow 16-bit data transfers do not use the BHEN signal. For example, the Am95/4005, 4006, and 4010 do not use the BHEN signal. The Am95/4116 does use the BHEN signal. See table 2-4 for implementing this option.

Release Multibus

This option allows the host adapter to retain control of the Multibus either for one DMA cycle or for the whole duration of command execution. In the former case, the host adapter asserts the Multibus BUSY signal for only one DMA cycle and allows other devices to get on the Multibus after completing that cycle. In the latter case, the host adapter removes the BUSY signal only after completion of command execution. This prevents other devices from getting on the Multibus while the controller is executing the command. This mode of DMA transfer is faster because the host adapter does not have to arbitrate control of the Multibus for every DMA cycle.

See table 2-4 for implementing this option. It is initially connected to release the Multibus after every cycle.

TABLE 2-4. JUMPER-SELECTED OPTIONS FOR HOST ADAPTER CARD

FUNCTION	CONNECT	DISCONNECT	AMC CONFIGURATION 8100 SERIES
20-bit Address			
Enable	H-K	H-J	X
Disable	H-J	H-K	
Multibus BHEN (Byte High Enable) Signal			
With BHEN	T-U	T-W	
Without BHEN	T-W	T-U	X
Release Multibus			
Release After One DMA Cycle	X-Y	X-Z	X
Release After One Command Execution	X-Z	X-Y	
Parity on the Disk Controller Host Bus			
Enable Odd Parity	1-2	2-3	X
Disable Parity	2-3	1-2	

Parity on Disk Controller Bus

These jumpers allow the host adapter to enable and disable parity on the controller bus. Verify that the controller and the host adapter have identical parity selections, either both enabled or both disabled. See table 2-4 for setting this option.

DISK CONTROLLER CARD

Figure 2-2 locates jumpers and switches to select options on the disk controller card. This card is mounted inside the disk cabinet, and is accessible only by removing the top assembly of the chassis.

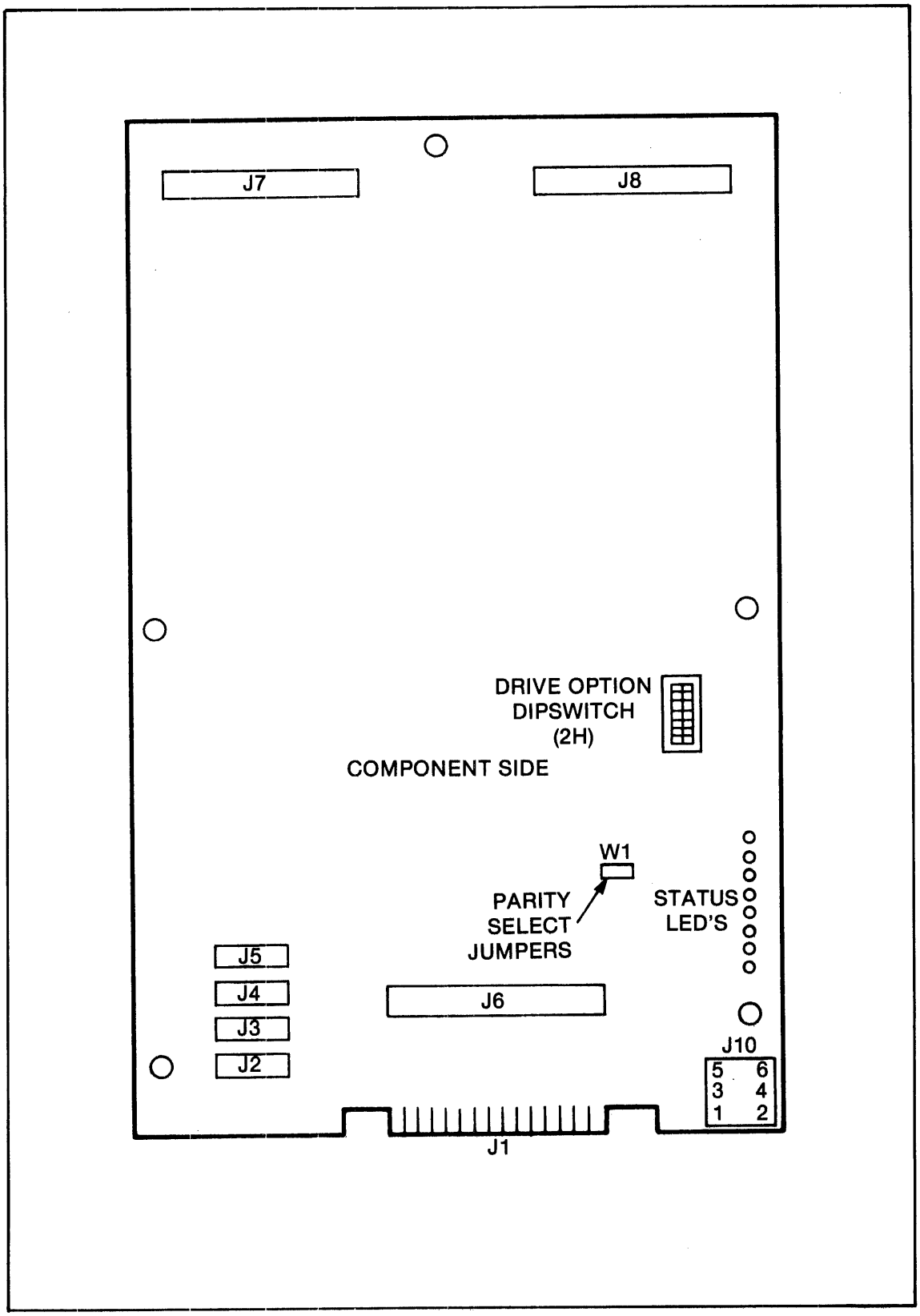


Figure 2-2. Disk Controller Card Locations

Parity Select Jumpers

Odd parity can be used by the host system to verify data integrity. The controller always uses odd parity in communicating with the host system.

Odd parity checking by the disk controller is controlled by connecting a jumper located near the host connector (J6, figure 2-2). With the jumper at position A-B, the controller tests for odd parity on all input data. With the jumper at position B-C, the controller does not test for parity. It is shipped in the A-B position.

Drive Type Selection

Table 2-5 shows the DIP switch settings (location 2H) for various types of drives for the disk controller card. Table 2-6 shows how to select disk drives for each of the four logical units by using the DIP switch. Any type of drive may be designated as any logical unit.

TABLE 2-5. DIP SWITCH SETTINGS FOR VARIOUS DISK DRIVES

DISK DRIVE	SWITCH SETTINGS
SA800	on-off
SA850	off-off
SA1002	on-on
SA1004	off-on

TABLE 2-6. DISK DRIVE SELECTION

Switch Position	1 2	3 4	5 6	7 8
LUN	3	2	1	0
AMC CONFIGURATION 8100 SERIES	on off	off on	on off	on off

DISK DRIVES

The disk drives are properly configured for use inside the 6100 subsystem as shipped. The only configuration changes required relate to the installation with the Multibus system, namely cable termination. This is accomplished by correctly positioning a short 50-conductor jumper cable on the rear connector panel. When this is the only disk unit in the system, the jumper cable connects the termination and drive daisy-chain conectors. When this unit is being added to a system with

other disk units, the jumper cable is removed and does not terminate the line. This process is described in the following Installation Procedure section.

CPU CARD

The Multibus CPU card might have several options which require changes when installing the 6100 subsystem. This section describes the necessary configuration changes for various AMC MonoBoard Computer cards which can utilize the Mass Storage Subsystem.

Am95/4005

A new system bootstrap routine is provided in the 2732 device labelled 002510766-001. Remove any devices from locations U42, U43, U44, and U45. Insert the new PROM into the socket at U42.

If installed, remove these jumpers:

62-64, 62-65, 66-68, 66-69, 74-75, 76-77.

Install only 62-63 and 66-70. Remove the mapping PROM at U39, and replace with the new device labelled 2510802-001.

Am95/4006

A new system bootstrap routine is provided in the 2732 device labelled 002510766-001. Remove any devices from locations U43, U44, U45, and U46. Insert the new PROM into the socket at U43.

If installed, remove these jumpers:

135-136, 136-138, 139-141, 140-141.

Install only 73-74, 133-136, 134-141.

Remove the mapping PROM at U40, and replace with the new device labelled 002510765-001.

Am95/4010

A new system bootstrap routine is provided in the 2732 device labelled 002510766-001. Remove any device from U27. Insert the new PROM into the socket at U27. Also, change these jumpers when replacing a 2716 with a 2732 device:

remove 4-6; 7-8;
insert 5-6.

INSTALLATION PROCEDURE

The following installation instructions assume that the Multibus chassis has already been installed according to the procedure in its manual.

INSTALLATION PREPARATION

Prepare the system for installation of the 6100 subsystem with the following procedure.

1. Move the disk cabinet to the installation site. Remove the spindle lock which secures the Winchester unit. This is a small metal bar with a right angle bend and a mounting slot. It is located on the bottom of the disk drive, under a cover plate mounted to the bottom cover.

    a. Remove the cover plate. Note the instructions on the bottom cover (figure 2-3).

    b. Remove the spindle lock with either a nutdriver or a screwdriver.

    c. Replace the spindle lock in the second slot provided, as shown in figure 2-3. Tighten the lock in place to prevent loss. Replace the cover plate.

    CAUTION

    The spindle lock must be re-attached whenever the disk drive is to be shipped or stored. It must be removed before the unit is activated for use. Ignoring either of these instructions can cause permanent damage to the unit. The unit should always be handled with care, and the lock should be attached whenever a possibility of rough handling exists.

2. Check the configuration of the host adapter card as specified under System Initialization and Options (table 2-2).

3. Remove the top cover from the Multibus chassis. Remove the CPU card and configure it as described under System Initialization and Options. Ensure that the correct PROM devices are inserted in the correct locations.

4. This concludes installation preparation. Complete the installation process by following the instructions contained in the appropriate following subsection.

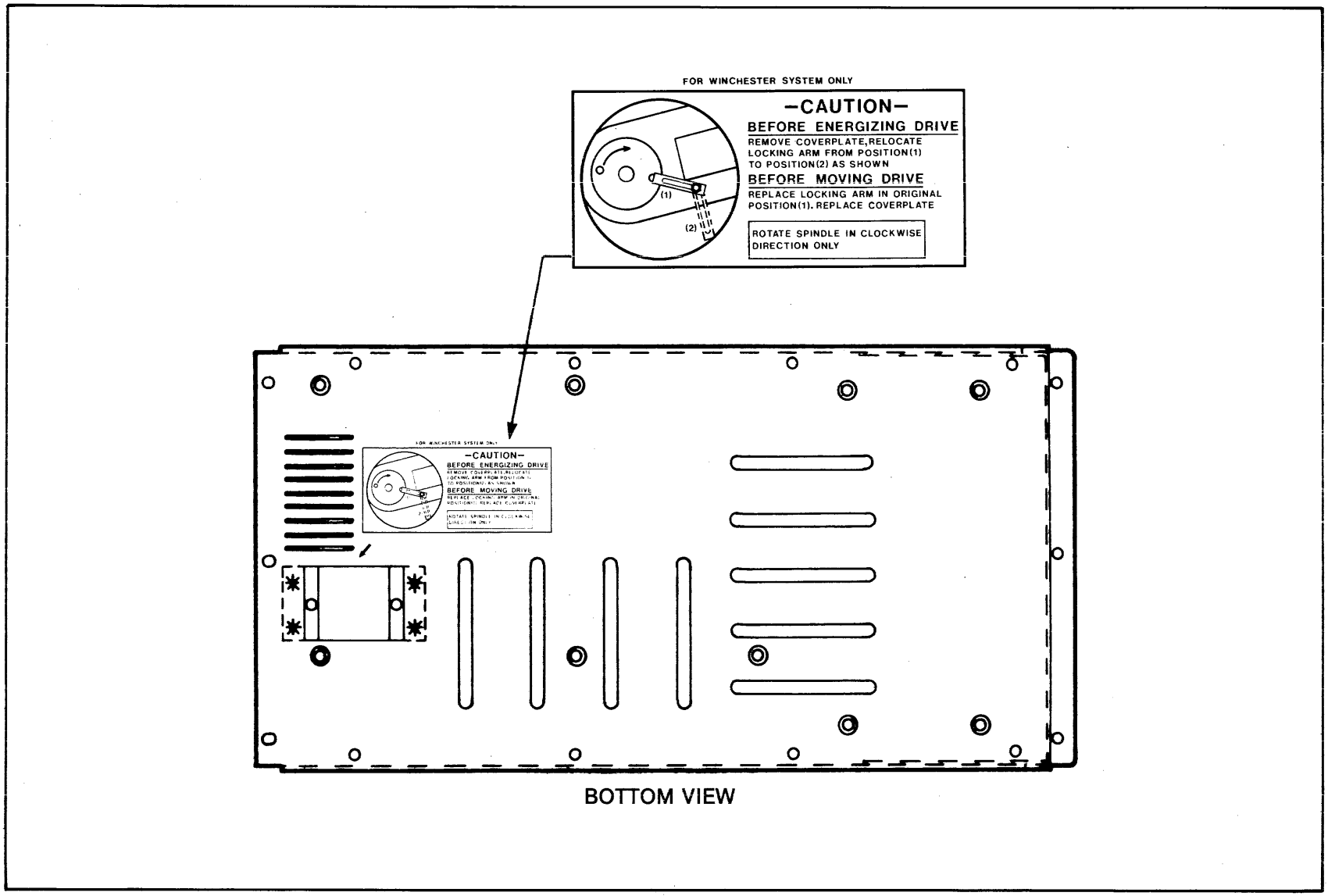


Figure 2-3. Bottom View of Cabinet

INSTALLATION WITH AN 8100 SERIES SYSTEM WITHOUT FLOPPY DISKS

1. Perform the instructions contained in the preceding Installation Preparation section.

2. Insert the CPU card into the Multibus chassis. Insert the host adapter card into a slot near the CPU card (use slot 14 if available).

3. Attach the host adapter interface cable between host adapter connector J3 and the FDC P4 cable (if installed). If the FDC P4 cable is not installed in the chassis, use the CPU J3 cable.

   Match each end of the cable correctly. Proper mating aligns pin 1 to jack 1 on each connector. The red edge markers on all cables should line up when properly installed.

4. Connect all other cables inside the Multibus chassis as previously connected.

5. Connect the two chassis together with a 50-pin jumper cable. Attach one end to the Winchester disk cabinet, connector I/07. Attach the other end either to the Multibus chassis connector DISK: (if cable FDC P4 was used in step 3); or to connector UL1: (if cable CPU J3 was used in step 3. First remove any other cable from connector UL1: if installed). See figure 2-4(a).

6. Connect the short 50-pin jumper cable between I/O 1 and I/O 3 on the back of the disk cabinet. This terminates the disk daisy chain cable inside the disk cabinet.

7. Connect the ac power cable of the disk cabinet to an ac outlet. Using an outlet on the back of the Multibus chassis supplies power to the disk cabinet whenever the Multibus chassis is powered.

8. An alternate method to activate disk cabinet power requires installation of a remote power control cable between the Multibus chassis and the disk cabinet. This cable carries a logic level signal between the two chassis when the Multibus chassis is powered up. This signal activates power switching circuits in the disk cabinet. The ac power cable for the disk cabinet need not be plugged into the Multibus chassis in this configuration.

9. The 6100 subsystem installation is now complete. Return to the installation procedure for the 8100 chassis and proceed.

INSTALLATION WITH AN 8100 SERIES SYSTEM AND A FLOPPY DISK EXTENSION

1. Perform the instructions contained in the preceding Installation Preparation section.

2. Remove the disk controller card from the Multibus chassis.

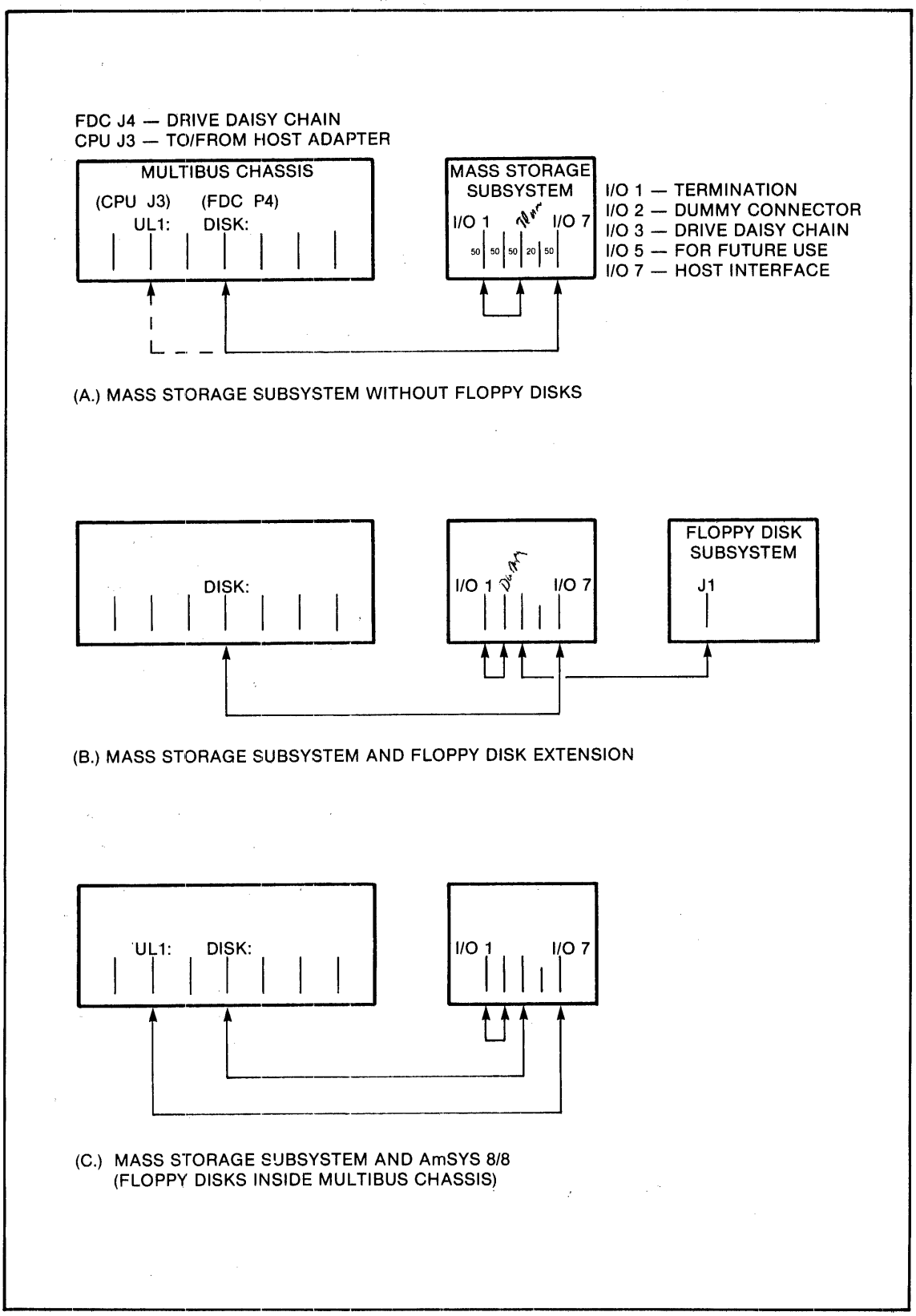


Figure 2-4. Cabinet Interconnections

3. Insert the CPU card into the Multibus chassis. Insert the host adapter card into the slot previously occupied by the disk controller card.

4. Attach the host adapter interface cable between connector J3 on the host adapter card and the FDC P4 cable.

   Match each end of the cable correctly. Proper mating aligns pin 1 to jack 1 on each connector. The red edge markers on all cables should line up when properly installed.

5. Connect all other cables inside the Multibus chassis as previously connected.

6. Connect the Multibus chassis and Winchester disk chassis together with a 50-pin jumper cable. Attach one end to the Winchester disk cabinet, connector I/07. Attach the other end to the Multibus chassis connector DISK:. See figure 2-4(b).

7. To utilize all three floppy disk drives and the Winchester disk drive, connect the two disk cabinets with a 50-pin jumper cable. Attach one end to the Winchester disk cabinet, connector I/03. Attach the other end to either connector on the back of the floppy disk extension chassis.

8. Connect the short 50-pin jumper cable between I/01 and I/02 on the back of the Winchester disk cabinet. This stores the cable out of the way by attaching it to the dummy connector. In this case, the disk daisy chain cable is terminated by the last floppy disk drive in the extension chassis.

9. Connect the ac power cable of the disk cabinet to an ac outlet. Using an outlet on the back of the Multibus chassis supplies power to the disk cabinet whenever the Multibus chassis is powered.

10. An alternate method to activate disk cabinet power requires installation of a remote power control cable between the Multibus chassis and the disk cabinet. This cable carries a logic level signal between the two chassis when the Multibus chassis is power ed up. This signal activates power switching circuits in the disk cabinet. The ac power cable for the disk need not be plugged into the Multibus chassis in this configuration.

    A second remote control cable can be attached between the two disk cabinets, to activate power to all three cabinets from a single switch.

11. The 6100 subsystem installation is now complete. Return to the installation procedure for the 8100 chassis and proceed.

INSTALLATION WITH AN AmSYS 8/8 SYSTEM WITH INTERNAL FLOPPY DISKS

1. Perform the instructions contained in the preceding Installation Preparation section.

2. Remove the disk controller card from the Multibus chassis.

3. Insert the CPU card into the Multibus chassis. Insert the host adapter card into the slot previously occupied by the disk controller.

4. Attach the host adapter interface cable between connector J3 on the host adapter card and the CPU J3 cable.

   Match each end of the cable correctly. Proper mating aligns pin 1 to jack 1 on each connector. The red edge markers on all cables should line up when properly installed.

5. Connect all other cables inside the Multibus chassis as previously connected.

6. Connect the Multibus chassis and the disk chassis together with two 50-pin jumper cables. Attach one cable between the Winchester disk cabinet, connector I/07, and the Multibus chassis, connector UL1: (from connector CPU J3).

   Attach the second cable between Winchester cabinet connector I/O 3 and Multibus connector DISK: (from connector FDC P4). See figure 2-4(c).

7. Connect the short 50-pin jumper cable between I/01 and I/02 on the back of the Winchester disk cabinet. This stores the cable out of the way by attaching it to the dummy connector. In this case, the disk daisy chain cable is terminated by the last floppy disk drive inside the AmSYS 8/8 chassis.

8. Connect the ac power cable of the disk cabinet to an ac outlet. Using an outlet on the back of the Multibus chassis supplies power to the disk cabinet whenever the Multibus chassis is powered.

9. An alternate method to activate disk cabinet power requires installation of a remote power control cable between the Multibus chassis and the disk cabinet. This cable carries a logic level signal between the two chassis when the Multibus chassis is powered up. This signal activates power switching circuits in the disk cabinet. The ac power cable for the disk need not be plugged into the Multibus chassis in this configuration.

10. The 6100 subsystem installation is now complete. Return to the installation procedure for the AmSYS 8/8 chassis and proceed.

INSTALLATION WITH OTHER MULTIBUS SYSTEMS

The installation procedure for other Multibus systems is similar to that described above for the 8100 Series. Ensure that the configurations of the controller card, host adapter card, and CPU card are correct for the system.

CHAPTER 3

OPERATION

INTRODUCTION

This section provides basic instructions for the care and handling of floppy disks and disk drives, and Winchester disk drives. This information is general in nature, and does not include any specific instructions related to disk operating systems. For details on computer operations with the disk, consult the appropriate software manual for the operating system being used.

FLOPPY DISK UNIT

The diskette used with the floppy disk drive is sealed in an 8-inch square cover that is lined to minimize static electricity. When not in use, the diskette should be kept in the storage envelope provided with each diskette.

Store diskettes in normal work areas where temperatures are in the range 50-125 degrees Fahrenheit (27-50 degrees Celsius). Do not expose them to magnetic fields, such as those around large power supply transformers. Do not expose them to direct sunlight for an extended period of time.

Insert the floppy disk into the disk drive opening, with the label up and out and the write protect notch toward the drive (figure 3-1).

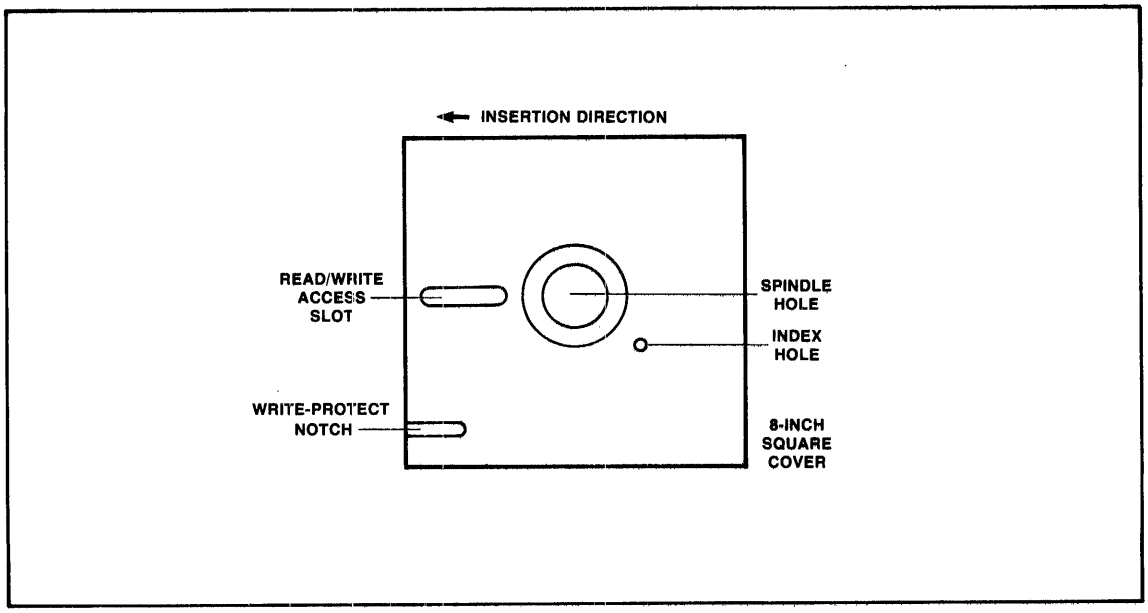


Figure 3-1. Floppy Disk

CAUTION

Exercise care when handling diskettes. Do not touch the recording surface exposed through the openings on the cover. Use only diskettes of comparable quality to those provided with the system. Lower quality diskettes cause excessive wear of the read/ write head.

CAUTION

Information stored on the diskette can be destroyed by static electricity discharge from a person touch ing the equipment. Synthetic carpets, in particu- lar, can cause a build-up of static electricity. Periodic application of Neutro-Stat (or equivalent) antistatic spray can retard the static electricity build-up; however a safer solution is to install the system on an antistatic mat (see Velostat type 1854 -4' x 8' x 1/8" as manufactured by 3M-Static Control Systems, St. Paul, Minn. 55101, or equivalent).

The floppy disk drive engages the diskette when the door is closed. The door is closed by pushing the top of the door down until it latches in a closed position.

CAUTION

Do not replace diskettes while programs or commands are being executed. Do not turn power to the disk drive unit on or off when a diskette is inside. This can destroy a track of data. When drive units must be powered down and a red activity indicator is lighted, open the drive unit door and remove the diskette before powering down.

A diskette can be write-protected by removing the tape strip from the write-protect notch. This prevents data from being recorded on the diskette. Each diskette is shipped with several tape strips.

NOTE

When the write-protect notch is covered with a tape strip, the diskette is write-enabled (data can be recorded on the diskette). Some commands require that the accessed diskette be write-enabled.

Before a blank diskette may be used to record data, it must be formatted. This consists of recording the index address mark and record identification fields and gaps onto the disk. If any of these marks are accidentally erased, the diskette must be formatted again,

which erases all data previously recorded on it. To avoid a potential disaster, maintain thorough back-up copies of all important diskettes and update them frequently. The formatting process is described in the operating system manual. For example, the AMDOS utility program called FORMAT initializes blank diskettes. Diskettes provided by AMC are formatted for single density use.

WINCHESTER DISK

Operation of the Winchester disk unit is very straightforward once installed. The ac power switch and fuse are at the rear of the chassis. Two non-removable 8-inch disks are enclosed inside a sealed compartment. This arrangement allows no user access to the storage media as with the floppy disk drive. The operator can turn the unit on and off.

CAUTION

> Ensure that the spindle lock at the bottom of the drive is in the locked position whenever the unit is transported or stored. Ensure that it is in the unlocked position whenever the unit is to be used. Ignoring either of these cautions can permanently damage the disk subsystem. See chapter 2, Installation Procedure, for details.
>
> Whenever the unit is stored, insert the spindle lock in case it is moved during storage.

All other disk operations are controlled by the operating system software. A good system will be transparent to the user; that is, it will perform all the required functions automatically, with minimal operator intervention.

The Winchester disk recording format is similar to that of the floppy disk. However, additional software features are required due to the use of non-removable storage media. Among these requirements is a convenient method to copy data between the Winchester and floppy disks (both directions) for backup storage. Also, a method to prevent damaged areas of the disk surface from being used by the system is necessary. These and other specific features for Winchester disk operations are covered in the operating system user's manual.

CHAPTER 4
SERVICE INFORMATION

SERVICE AND REPAIR ASSISTANCE

Service and repair assistance can be obtained from Advanced Micro Computers by contacting the AMC Field Service Department in Santa Clara, California at one of the following numbers:

Telephone:	(408) 988-7777	
Toll Free:	(800) 672-3548	California
	(800) 538-9791	U.S.A. (except California)

To return a product to Advanced Micro Computers for service or repair, contact the Field Service Department. A Return Material Authorization number and shipping instructions will be provided. When return is because of damage during shipment from AMC, or when the product is out of warranty, a purchase order is required for the AMC Field Service Department to initiate the repair.

Prepare the product for shipment by repackaging it in the original factory packaging material, if available. When the original packaging is not available, wrap the product in a cushioning material (such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, New Jersey) and enclose it in a heavy-duty corrugated shipping carton. Seal the shipping carton securely, mark it FRAGILE, and ship it to the address specified by the AMC Field Service Department.

SERVICE DIAGRAMS

These diagrams are included for reference and service purposes:

Chassis Wiring Diagram	119110733-001
Host Adapter Card Schematic Diagram	N/A
Disk Controller Card Functional Block Diagram	N/A

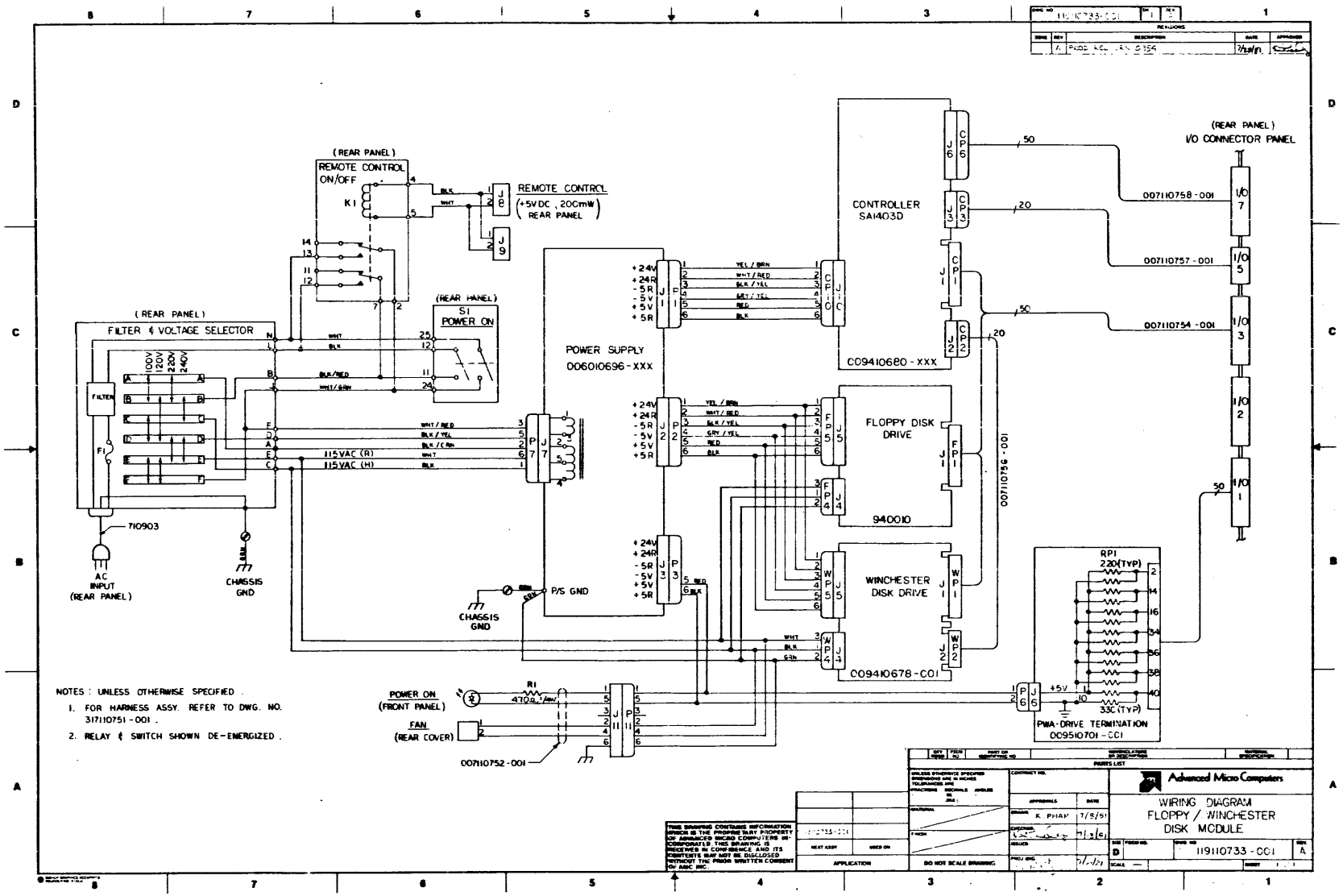


Figure 4-1. Chassis Wiring Diagram

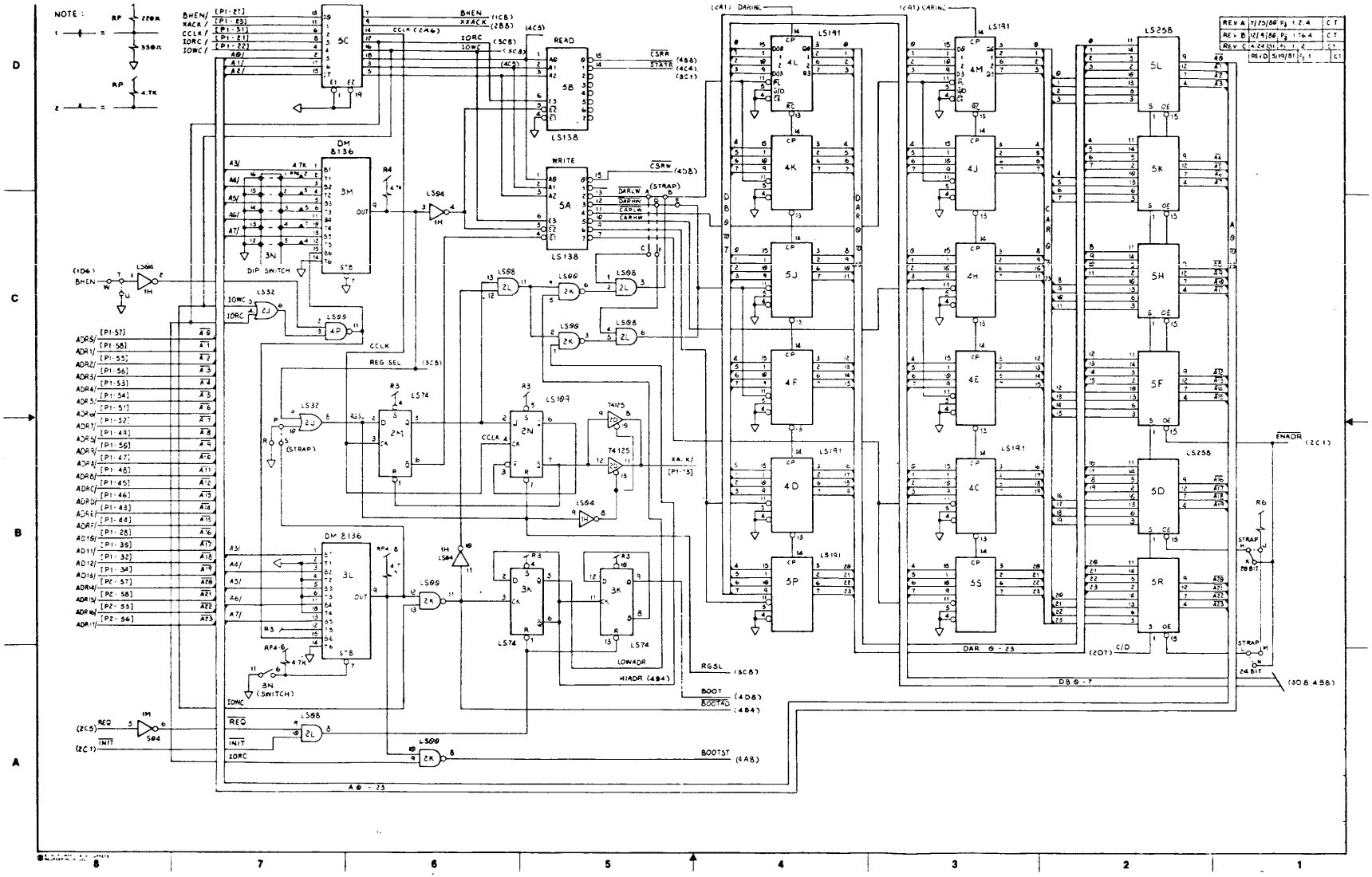


Figure 4-2. Host Adapter Card Schematic Diagram, Sheet 1 of 4

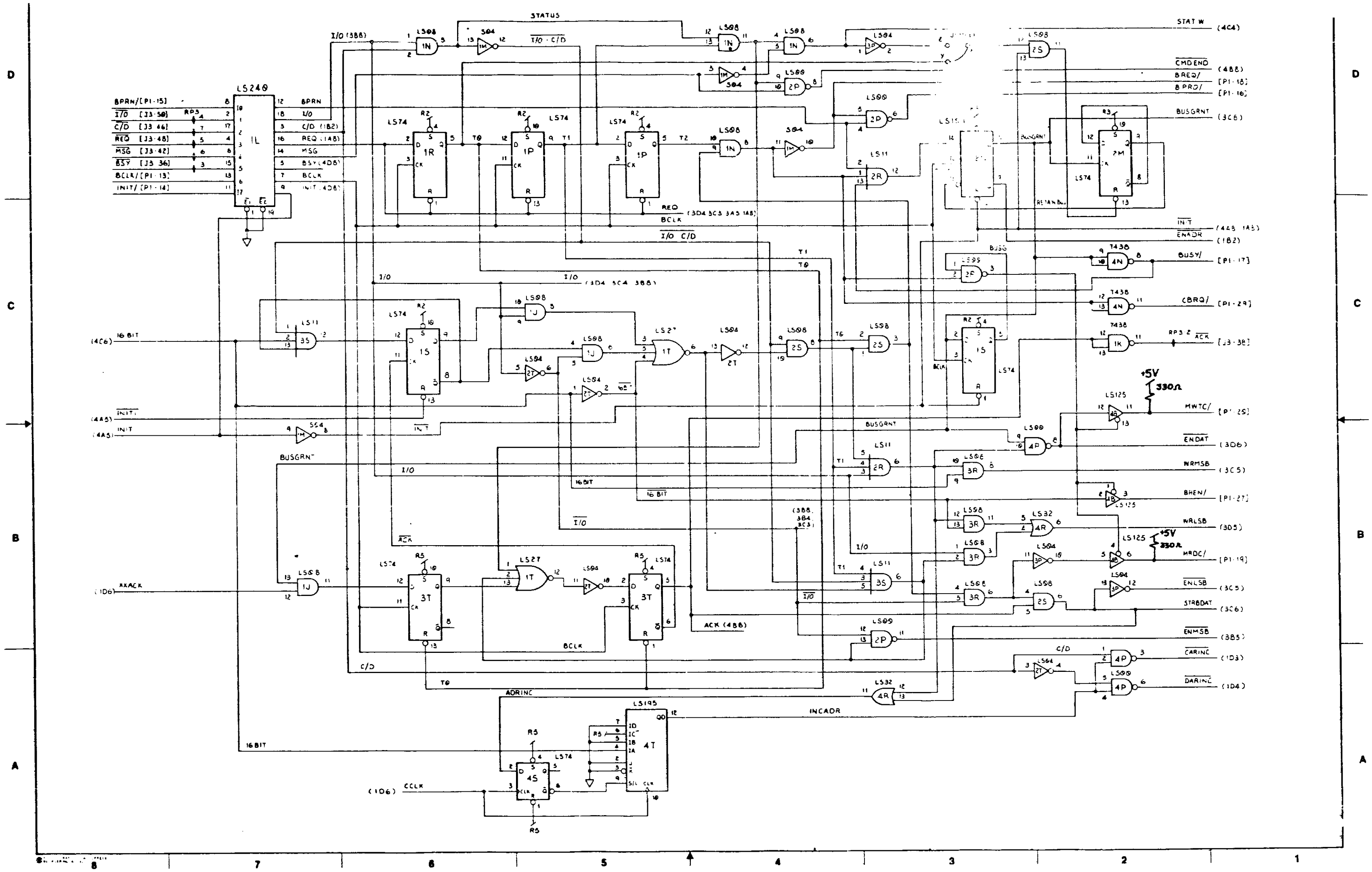


Figure 4-2. Host Adapter Card Schematic Diagram, Sheet 2 of 4

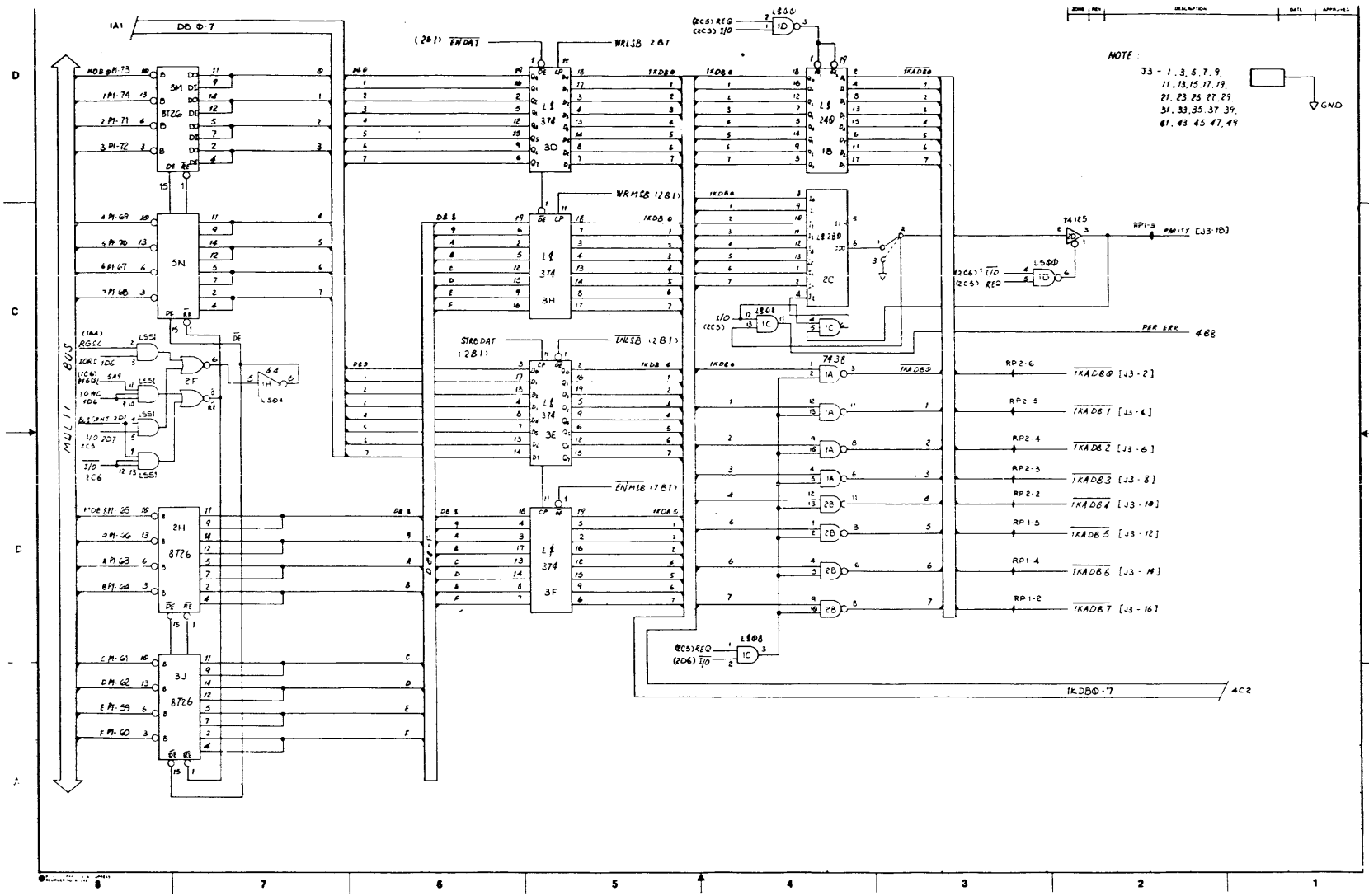


Figure 4-2. Host Adapter Card Schematic Diagram, Sheet 3 of 4

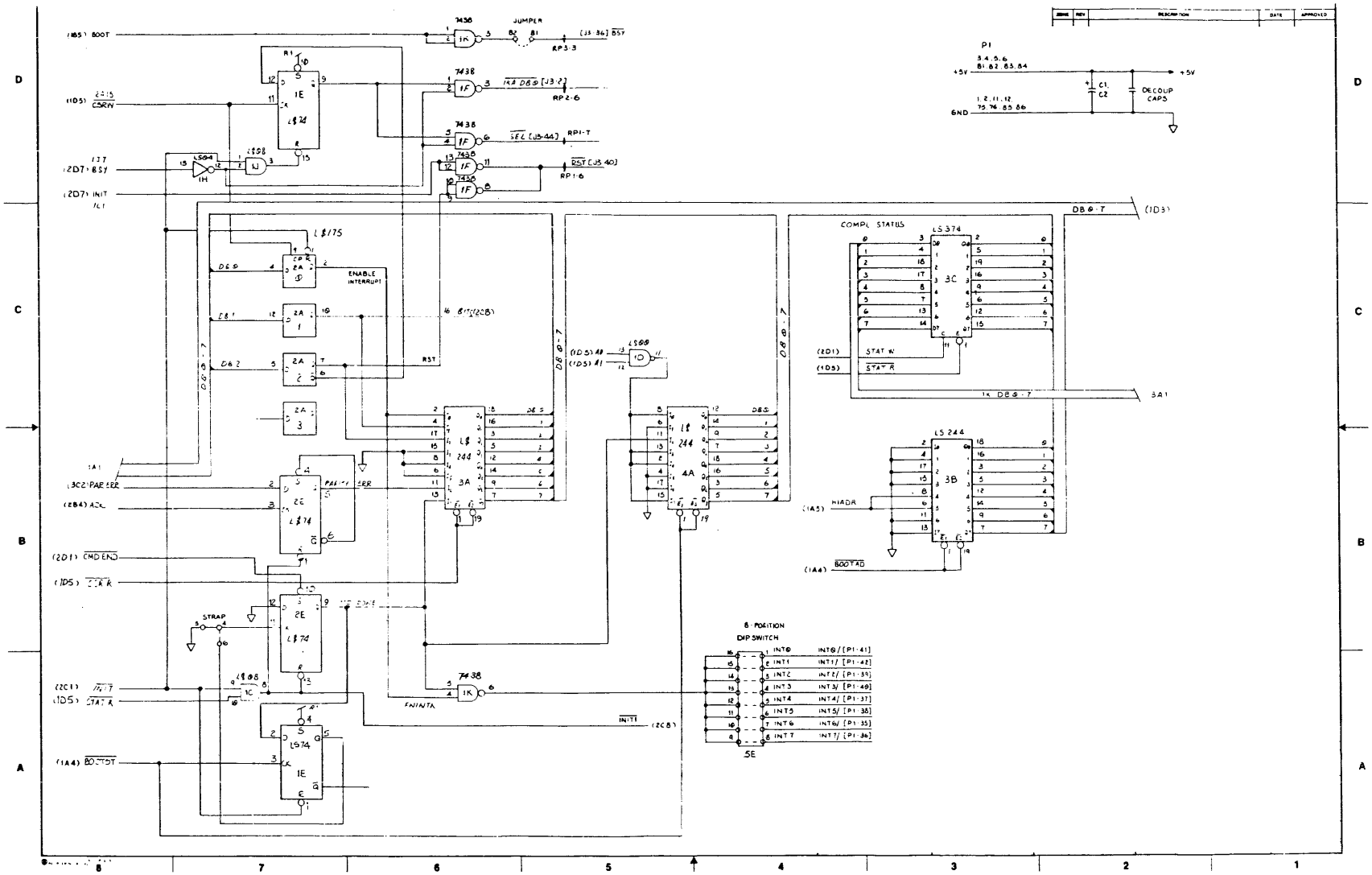


Figure 4-2. Host Adapter Card Schematic Diagram, Sheet 4 of 4

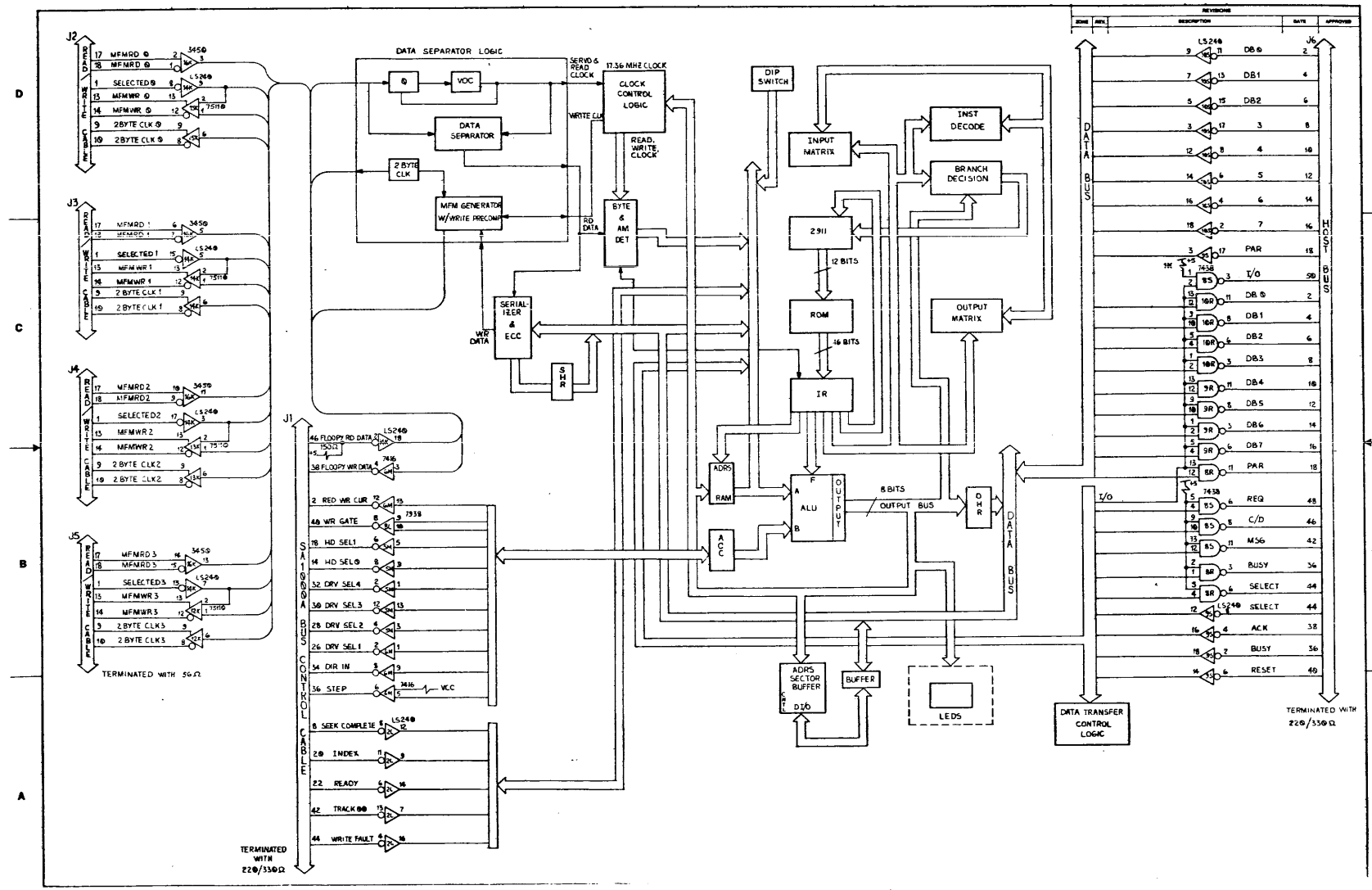


Figure 4-3. Disk Controller Card Functional Block Diagram

APPENDIX A

SOFTWARE INTERFACE

HOST ADAPTER REGISTER DESCRIPTION

The Multibus software interface is provided by registers into which the CPU can read and write to start command execution. The host CPU issues disk I/O commands to the controller by setting up registers in the host adapter. The 16-bit address version of the host adapter communicates with the CPU through six input and output ports:

- Channel status register
- Command completion status register
- Data address register (high/low)
- Command address register (high/low)

The 20-bit address version utilizes two additional output ports, for a total of eight:

- Data address register (top)
- Command address register (top)

CHANNEL STATUS REGISTER (IN/OUT) BASE+0

This register is used to set up the data transfer mode, to start the command execution, and to monitor the status of the command execution. The bit assignments are as follows:

BIT	DESCRIPTION
0	Enable Interrupt
1	16-bit Data Transfer
2	
3	
4	
5	
6	Parity Error
7	Command Done

Writing (OUT) to the channel status register (CSR) with bit 0 set to 1 causes the host adapter to interrupt the CPU when the controller completes the command execution. When bit 0 is reset to 0, no interrupt is generated.

Writing (OUT) to the CSR when bit 1 is set to 1 causes 16 bits of data to be transferred for each DMA cycle. Since the data path between the host adapter and the controller is 8 bits wide, packing and unpacking of the data is done in the host adapter. DAT0/-DAT7/ of the 16-bit word are transferred first, followed by DAT8/-DATF/ to/from the controller. When bit 1 is reset to 0, eight bits of data are transferred at a time. OUT to CSR automatically starts command execution.

Reading (IN) the CSR returns the status of command execution. Bit 6 is set by the host adapter if a parity error is detected while the data is being transferred from the controller. Bit 7 is set by the host adapter when the controller completes command execution. Bit 6 (parity error) and bit 7 (command done) are cleared by the host adapter when an IN instruction to the command completion status register port is executed.

COMMAND COMPLETION STATUS REGISTER (IN) BASE+1

This register must be read (IN) once per command execution to clear the parity error and command done bits in the CSR. The contents of this register are posted by the controller upon normal or error termination. This information includes the logical unit number of the drive, any error encountered during command execution, and any parity error detected while transferring data from the host adapter. The bit assignments for the register are as follows:

BIT	DESCRIPTION
0	Parity Error
1	Error Occurred
2	
3	
4	
5	LUN
6	LUN
7	LUN

Issue a request sense command to the controller to obtain information about the error. The controller returns four bytes to the host system, as described in the AMDOS User's Manual (Revision B), Appendix D.

DATA ADDRESS REGISTER (OUT)

Data address low BASE +2
Data address high BASE +3
Data address top BASE +6†

Data address low, high, and top registers indicate the memory location where the data is to be transferred.

Data address low contains the least significant eight bits (ADR 0-7). Data address high contains the next highest eight bits (ADR 8-15). Data address top contains the top eight bits (ADR 16-23); zero fill bits 20-23 when using 20-bit addressing.

†Not required if 20-bit address option is disabled.

COMMAND ADDRESS REGISTER (OUT)

Command address low	BASE + 4
Command address high	BASE + 5
Command address top	BASE + 7†

Command address low, high, and top registers indicate to the controller the memory location where the command descriptor resides.

Command address low contains the least significant eight bits (ADR 0-7).
Command address high contains the next highest eight bits (ADR 8-15).
Command address top contains the top eight bits (ADR 16-23); zero fill bits 20-23 when using 20-bit addressing.

SOFTWARE OPERATION

The software sets up a command descriptor block in memory, and loads the memory address of the first byte of the command descriptor block in the command address registers. The data address registers are loaded with the memory address where the data is to be transferred (the registers are not loaded unless a data transfer is involved).

The program deposits the data transfer mode bits in the CSR and waits for the command execution to complete, either by polling the command done bit in the CSR, or by waiting for an interrupt to occur (if the interrupt is enabled). The command completion status register is read (IN) to check the completion status and to clear the command done and parity error bits in the CSR.

Figure A-1 lists a sample I/O driver program.

DISK CONTOLLER COMMAND DESCRIPTOR BLOCK

Once the CPU selects a disk operation, the controller requests a command descriptor block (CDB) which is either six or 10 bytes long. The first byte of the CDB contains the command class and the command operation code. The remaining bytes specify the drive logical unit number (LUN), logical sector address, number of sectors to be transferred or a destination device (copy command), and a control field byte. Commands are divided into four classes:

1. Class 0: Utility, data transfer, and status commands.
2. Class 1: Disk copy commands.
3. Classes 2 through 5 and 7: Not used at this time.
4. Class 6: FDD format selection.

†Not required if 20-bit address option is disabled.

```
;EQUATES FOR THE HOST ADAPTER REGISTERS.
;THE BASE PORT ADDRESS IS SET UP FOR A0H
CSR     EQU   00A0H   ;CSR PORT ADDRESS
STAT    EQU   00A1H   ;COMPLETION STATUS REG. PORT ADDRESS
DARL    EQU   00A2H   ;DATA ADDRESS LO REG. PORT ADDRESS
DARH    EQU   00A3H   ;DATA ADDRESS HI REG. PORT ADDRESS
CARL    EQU   00A4H   ;CDB ADDRESS LO REG. PORT ADDRESS
CARH    EQU   00A5H   ;CDB ADDRESS HI REG. PORT ADDRESS
DART*   EQU   00A6H   ;DATA ADDRESS TOP REG. PORT ADDRESS
CART*   EQU   00A7H   ;COMMAND ADDRESS TOP REG. PORT ADDRESS
;THIS ROUTINE SETS UP THE HOST ADAPTER REGISTERS, STARTS THE COMMAND
;EXECUTION AND RETRIEVES THE CHANNEL STATUS AND CONTROLLER COMPLETION
;STATUS. IT ASSUMES THAT THE COMMAND DESCRIPTOR BLOCK IS ALREADY
;SET UP WITH THE COMMAND, BLOCK ADDRESS, NUMBER OF BLOCKS TO TRANSFER
;AND CONTROL FLAGS.
;NOTE - THE CALLING ROUTINE SHOULD CHECK CSREG AND STREG FOR ERROR
;CONDITIONS.
;NOTE - FOR NON DATA TRANSFER COMMAND (SEEK, RECAL...) IT IS NOT
;NECESSARY TO SET UP THE DATA ADDRESS REGISTER BUT IT IS OKAY.
DSKIO:  LXI   H,CDB   ;GET COMMAND DESCRIPTOR BLOCK ADDRESS
        MOV   A,L     ;SETUP THE CDB ADDRESS REGISTERS
        OUT   CARL    ;CDB ADR LO REG
        MOV   A,H
        OUT   CARH    ;CDB ADR HI REG
        MVI   A,0†    ;NOTE THE TOP 8-BIT ADDRESS IS FORCED TO ZERO
        OUT   CART†   ;FOR SIMPLICITY
        LXI   H,BUF   ;GET THE DATA BUFFER MEMORY ADDRESS
        MOV   A,L     ;SETUP THE DATA ADDRESS REGISTERS.
        OUT   DARL    ;DATA ADR LO REG.
        MOV   A,H
        OUT   DARH    ;DATA ADR HI REG.
        MVI   A,0†    ;NOTE THE TOP 8-BIT ADDRESS IS FORCED TO ZERO
        OUT   DART†   ;FOR SIMPLICITY
        MVI   A,0
        OUT   CSR     ;START THE COMMAND EXECUTION.
;WAIT FOR THE COMMAND EXECUTION TO COMPLETE
DSKI00: IN    CSR     ;READ THE CSR
        ANI   80H     ;CHECK IF COMMAND DONE FLAG IS SET
        JZ    DSKI00  ;LOOP IF COMMAND EXECUTION IS NOT COMPLETE
        STA   CSREG   ;SAVE CONTENTS OF CSR FOR TESTING LATER
;COMMAND EXECUTION IS COMPLETE
        IN    STAT    ;GET CONTROLLER COMMAND COMPLETION STATUS
        STA   STREG   ;SAVE IT FOR TESTING LATER
        RET
CDB:    DS    8       ;COMMAND DESCRIPTOR BLOCK (CDB)
BUF:    DS    256     ;DATA BUFFER MEMORY ADDRESS
        END
```

†Required only if 20-bit address option is enabled.

Figure A-1. Sample I/O Driver Program

Command descriptor blocks for class 0 and class 6 commands are 6 bytes in length, and those for class 1 commands are 10 bytes in length (see figure A-2).

The controller checks all incoming command descriptor blocks for validity and also checks (if enabled) all CDB's and data for odd parity. A parity error causes an immediate halt of the command or data transfer, terminating with a status byte transfer. This does not cause incorrect data to be written because the write does not occur until the sector buffer has been filled. An error in the command structure causes a status byte transfer to occur upon completion of the CDB transfer.

COMMAND DESCRIPTION, CLASS 0

The following commands are listed by their respective hexadecimal operation codes:

OPCODE	COMMAND DESCRIPTION
00	Test Drive Read: selects a particular drive and verifies that it is ready. The ready condition is indicated by the status byte. A not ready drive causes bit 1 of the status byte to be set.
01	Recalibrate: positions the head(s) of the selected drive over track 00 and clears any fault conditions.
02	Request Syndrome: returns two bytes of error offset and syndrome to the host system for host error correction cap ability (see figure A-3). The first byte is offset in the data field of the error location. The most significant three bits of the second byte point to the beginning of the error location. The least significant four bits of the second byte are the syndrome which is a data correction mark which is to be exclusive or'ed with the faulty data. This command is only valid when automatic data correction has been disabled in the control field byte (byte 6).
03	Request Sense: following an error, the host might form a request sense command for a more detailed description.
04	Format Drive: formats all cylinders with the identification fields set according to the specified interleave code. Data fields will contain a hexadecimal 6C data pattern.
05	Check Track Format: verifies correct identification fields and data sync marks for all sectors on a single data track. The data track is addressed via the logical sector address which may be any address within the desired track.

MSB LSB

	7	6	5	4	3	2	1	0
BYTE 1	CLASS = 000			OPERATION CODE				
2	0	LUN		LOGICAL SECTOR ADRS 2 (MS)				
3	LOGICAL SECTOR ADRS 1							
4	LOGICAL SECTOR ADRS 0 (LS)							
5	NUMBER OF SECTORS/INTERLEAVE CODE							(NOTE 1)
6	CONTROL FIELD							(NOTE 2)

Note 1: Byte five is number of sectors for read or write commands; byte five is interleave factor for format or check track commands.

Note 2: Defined in figure 2-4(c).

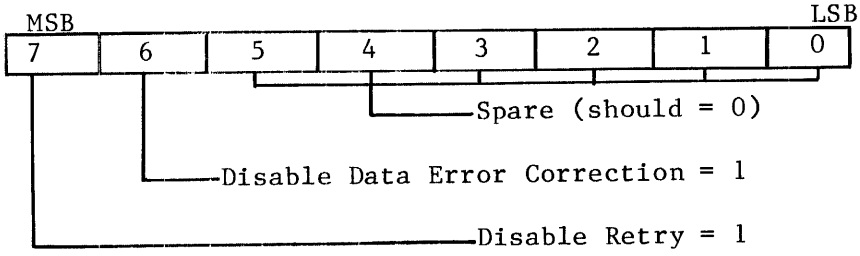
a. Class 0 Command Descriptor Block

	7	6	5	4	3	2	1	0
BYTE 1	CLASS = 001			OPERATION CODE				
2	0	LUN(S)		LOGICAL SECTOR ADRS 2 (S)				
3	LOGICAL SECTOR ADRS 1 (S)							
4	LOGICAL SECTOR ADRS 0 (S) (LS)							
5	NUMBER OF SECTORS							
6	0	LUN (D)		LOGICAL SECTOR ADRS 2 (D)				
7	LOGICAL SECTOR ADRS 1 (D)							
8	LOGICAL SECTOR ADRS 0 (D)							
9	SPARE (SHOULD = 0)							
10	CONTROL FIELD							(NOTE 1)

(S)=SOURCE DEVICE (D)=DESTINATION DEVICE

Note 1: Defined in figure 2-4(c).

b. Class 1 Command Descriptor Block



c. Control Field Byte

Figure A-2. Command Descriptor Block Description

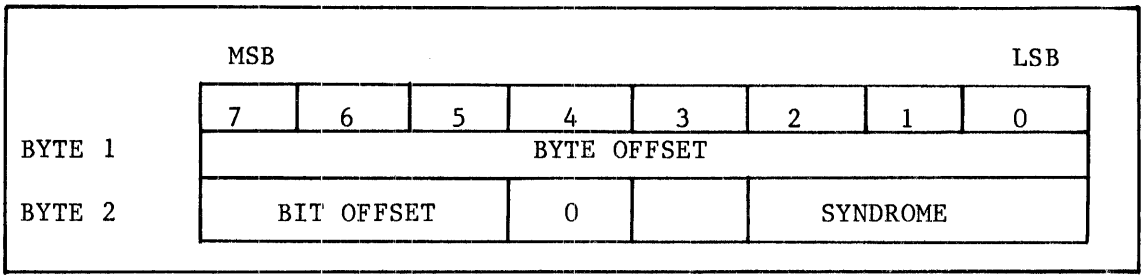


Figure A-3. Request Syndrome Block

OPCODE	COMMAND DESCRIPTION
06	Format Track: same as the Format Drive command except that only one data track is formatted. The data track is addressed via the logical sector address which can be any address within the desired track.
07	Format Bad Track: formats the specified track with the bad track flag set in the identification field(s) (bit 7 of the Head Address Byte set). The track is addressed via the logical sector address which can be any address within the desired track.
08	Read: reads the designated number of sectors from the disk beginning with the logical sector address given in the command descriptor block.
0A	Write: writes the designated number of sectors to the disk beginning with the logical sector address given in the command descriptor block.
0B	Seek: a seek is performed to the logical sector address specified in the command descriptor block.

COMMAND DESCRIPTION, CLASS 1

00	Copy Sector: copies the specified number of sectors from a source LUN to a destination LUN. Number of sectors transferred may be from 1 to 256. The completion status byte will indicate the source LUN. If an error occurs, a REQUEST SENSE command is issued to the source LUN. The sense bytes will indicate type of error for the appropriate LUN.

COMMAND DESCRIPTION, CLASS 6

00	Define Floppy Disk Track Format: the track format code in byte 5 of the CDB defines the track format for the LUN. The track format codes are listed in table A-1.

TABLE A-1. FLOPPY DISK FORMATS

TRACK FORMAT CODE	TRACK FORMAT DESCRIPTION
00	Single-density, single-sided. All tracks FM recording, 128 bytes/sector, 26 sectors per track.
01	Single-density, double-sided. All tracks FM recording, 128 bytes/sector, 26 sectors per track.
02	Double-density, single-sided. Side 0, cylinder 0 FM recording, 128 bytes/sector, 26 sectors per track. All other tracks MFM recording, 256 bytes/sector, 26 sectors per track.
03	Double-density, double-sided. Side 0, cylinder 0 FM recording, 128 bytes/sector, 26 sectors/track. All other tracks MFM recording, 256 bytes/sector, 26 sectors/track.

SECTOR INTERLEAVE CODES

In order to tailor host system data transfer speed to the disk rotational speed, sector interleaving is available. Sixteen interleave codes are offered numbered 1 to 16. Not all interleave codes result in optimum sector interleave; therefore the interleave code should be chosen carefully. In order to maintain IBM floppy disk compatibility, an interleave code of 1 should be used. This results in a non-interleave condition.

The interleave code given during the format command is calculated as follows:

The interleave algorithm is: Sector + Interleave.

Two examples of interleave codes are shown:

Interleave code of 16:

Physical: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Logical: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30

Physical: 16 17 18 19 20 21 22 23 24 25 25 27 28 29 30 31

Logical: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31

Interleave code of 2:

Physical:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Logical:	0	16	1	17	2	18	3	19	4	20	5	21	6	22	7	23

Physical:	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Logical:	8	24	9	25	10	26	11	27	12	28	13	29	14	30	15	31

APPENDIX B
CHASSIS CONNECTORS

This section provides the pinouts for the connectors on the rear panel of the Mass Storage Subsystem.

Connector I/O2 is a 50-pin dummy connector and has no signals.

Positions I/O 4 and I/O 6 are not used.

TABLE B-1. CONNECTOR I/O1: DRIVE TERMINATION CONNECTOR PINOUT

PIN	SIGNAL	PIN	SIGNAL
1	Ground	2	Reduced Write Current
3		4	Not Used
5		6	
7		8	
9		10	
11		12	Not Used
13		14	Head Select 0
15		16	Not Used
17		18	
19		20	
21		22	
23		24	
25		26	
27		28	
29		30	
31		32	Not Used
33		34	Direction In
35		36	Step
37		38	Floppy Write Data
39	Ground	40	Write Gate

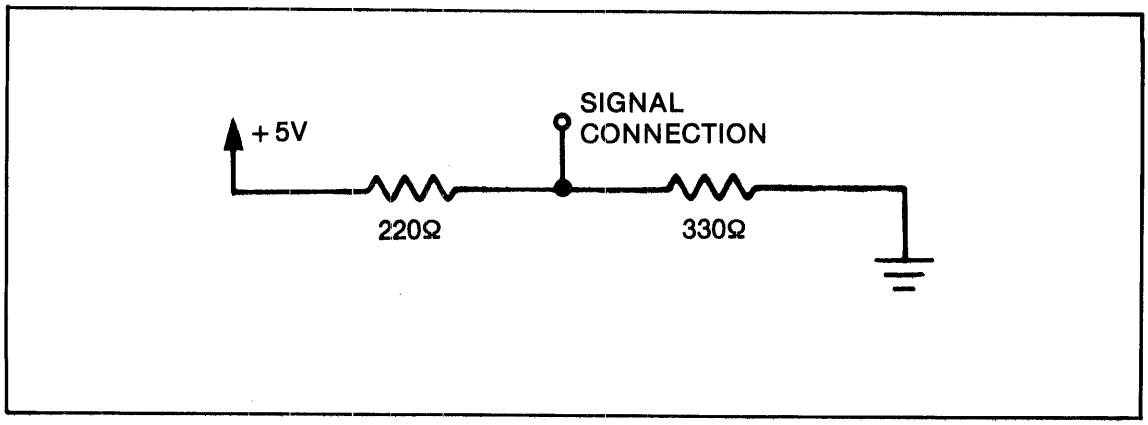


Figure B-1. Typical Drive Termination Circuit

TABLE B-2. CONNECTOR I/O3: DISK DRIVE DAISY CHAIN CONNECTOR PINOUT

PIN	SIGNAL	PIN	SIGNAL		
			SA1000	SA800	SA850
1	Ground	2	IW Switch		IW Switch
3		4			
5		6			
7		8	Seek Complete		
9		10			Two Sided
11		12			
13		14	Head Sel 0		Side Sel
15		16			
17		18	Head Sel 1	Head Load	Head Load
19		20	Index	Index	Index
21		22	Ready	Ready	Ready
23		24			
25		26	Drive Sel 1	Drive Sel 1	Drive Sel 1
27		28	Drive Sel 2	Drive Sel 2	Drive Sel 2
29		30	Drive Sel 3	Drive Sel 3	Drive Sel 3
31		32	Drive Sel 4	Drive Sel 4	Drive Sel 4
33		34	Direction Sel	Direction Sel	Direction Sel
35		36	Step	Step	Step
37		38		Write Data	Write Data
39		40	Write Gate	Write Gate	Write Gate
41		42	Track 000	Track 00	Track 00
43		44	Write Fault	Write Protect	Write Protect
45		46		Read Data	Read Data
47		48			
49	Ground	50			

TABLE B-3. CONNECTOR I/O5: SA1000 DATA CONNECTOR PINOUT (SPARE)

PIN	SIGNAL	PIN	SIGNAL
1	Drive Selected	2	Ground
3		4	
5		6	
7		8	Ground
9	+Timing Clock	10	-Timing Clock
11	Ground	12	Ground
13	+MFM Write Data	14	-MFM Write Data
15	Ground	16	Ground
17	+MFM Read Data	18	-MFM Read Data
19	Ground	20	Ground

TABLE B-4. CONNECTOR I/O7: HOST INTERFACE CONNECTOR PINOUT

PIN	SIGNAL	PIN	SIGNAL	
1	Ground	2	Data Bit 0 (DB0)	
3	↕	4	↕ 1	
5		6	2	
7		8	3	
9		10	4	
11		12	5	
13		14	6	
15		16	Data Bit 7 (DB7)	
17		18	Parity Bit	
19		20	For Future Use	
21		22	↕	
23		24		
25		26		
27		28		
29		30		
31		32		
33		34	For Future Use	
35		36	Busy	(BSY) ---> OUTPUT
37		38	Acknowledge	(ACK) <--- INPUT
39		40	Reset	(RST) <--- INPUT
41		42	Message	(MSG) ---> OUTPUT
43		44	Select	(SEL) <--- INPUT
45		46	Control/Data	(C/D) ---> OUTPUT
47		48	Request	(REQ) ---> OUTPUT
49	Ground	50	Input/Output	(I/O) ---> OUTPUT

Note: All signals are TTL, negative true.

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COMMENT SHEET

Address comments to:

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3340 Scott Boulevard
Santa Clara, CA 95051

TITLE: Mass Storage Subsystem User's Manual
PUBLICATION NO: 059910734-001 Revision A

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