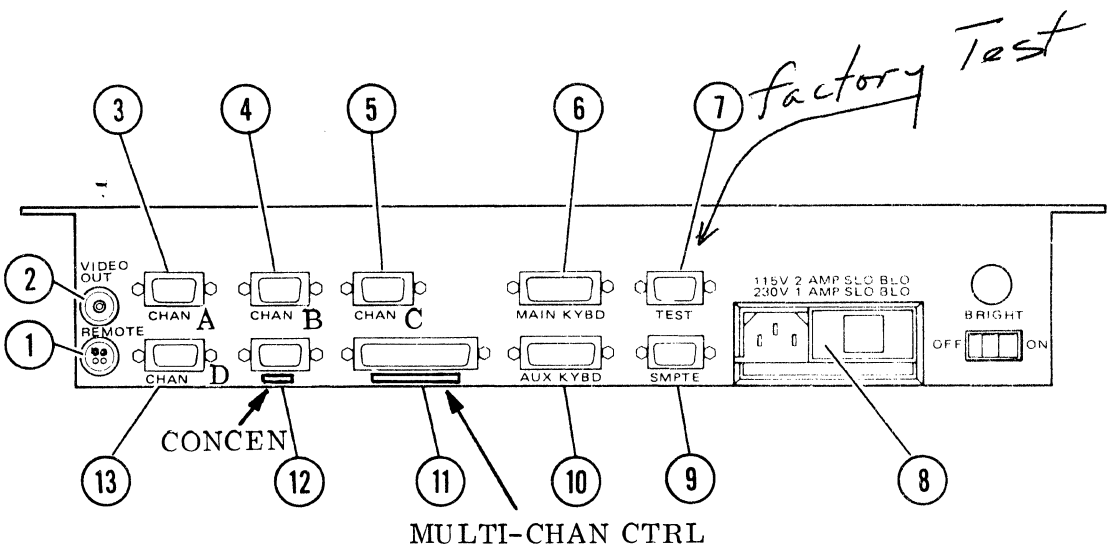
ADO

Training Manual

10021

ADO

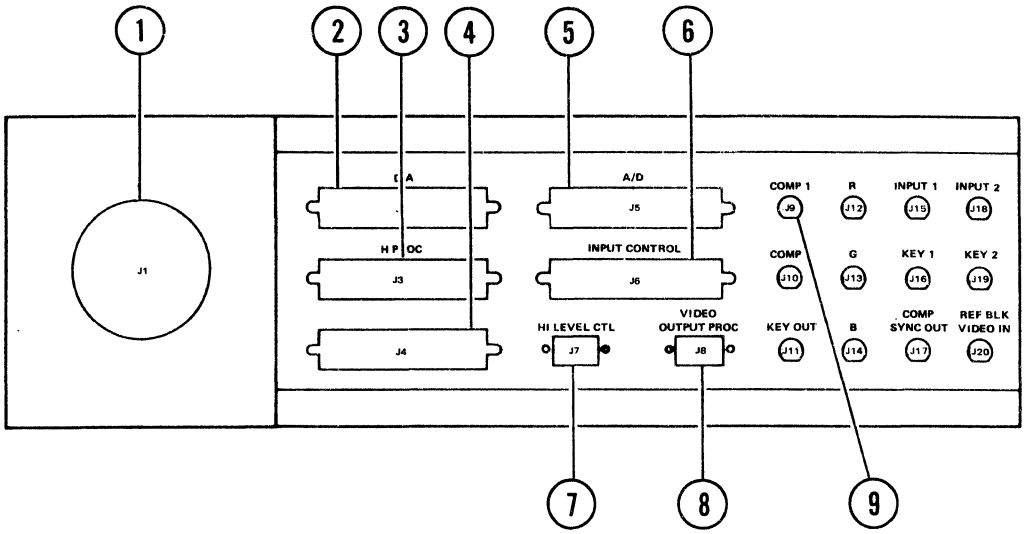
Menu Monitor Connector Panel



Reference No.	Name	Type	Description
1	REMOTE	4-pin	Remote command
2	VID OUT	BNC	CRT monitor display output
3	CHAN 1	9-pin	Signal system chassis No. 1 serial port
4	CHAN 2	9-pin	Signal system chassis No. 2 serial port
5	CHAN 3	9-pin	Signal system chassis No. 3 serial port
6	MAIN KYBD	15-pin	Keyboard port
8	115V 2 AMP SLO BLO 230V 1 AMP SLO BLO	3-wire	115 Vac input connector fuse
9	SMPTE		SMPTE port
10	AUX KYBD	15-pin	Auxiliary keyboard port
11	CHANNEL 1-5	25-pin	Combined signal system ports
12	CHAN 5	9-pin	Signal system chassis No. 5 serial port
13	CHAN 4	9-pin	Signal system chassis No. 4 serial port

Not Active →

Signal System Chassis Connector Panel

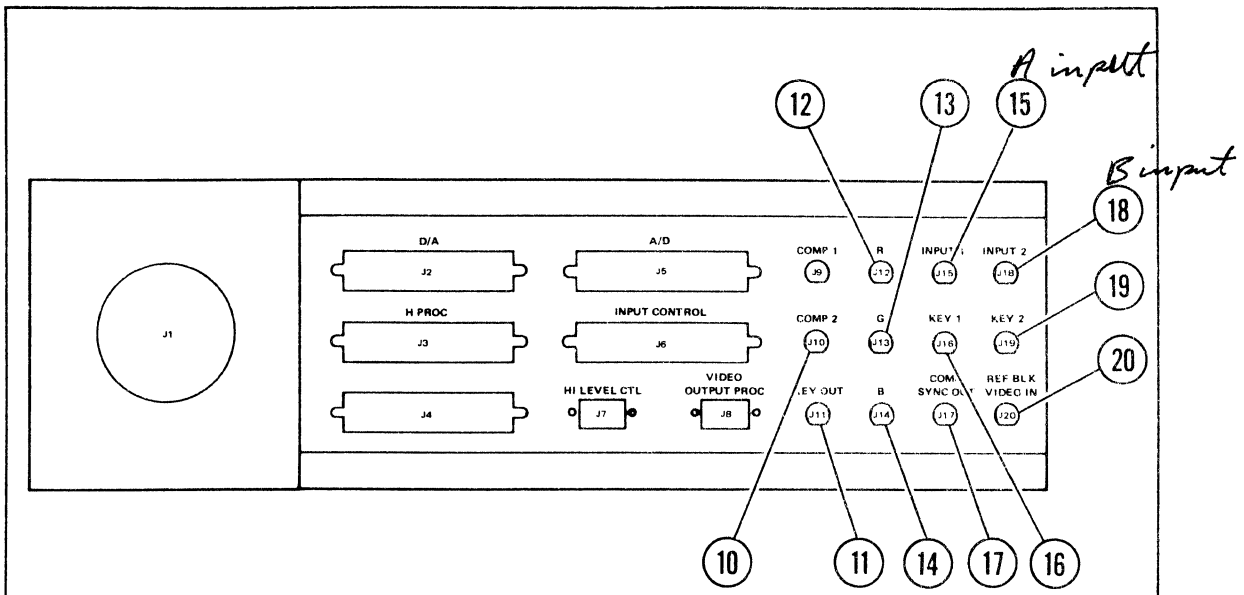


Reference No.	Number	Name	Type	Description
1	J1	115 VAC	Three-prong power	Power input
2	J2	D/A	Ribbon	Digital input to analog section
3	J3	H PROC	Ribbon	Digital processor output
4	J4	-	-	Not used
5	J5	A/D	Ribbon	Digital output from analog section
6	J6	INPUT CONTROL	Ribbon	Digital processor input
7	J7	HI LEVEL CTL	9-Pin, Type D	Serial port to CRT menu monitor
8	J8	VIDEO OUTPUT PROC	9-Pin, Type D	For concentrator option
9	J9	COMP 1	BNC	Composite video output 1

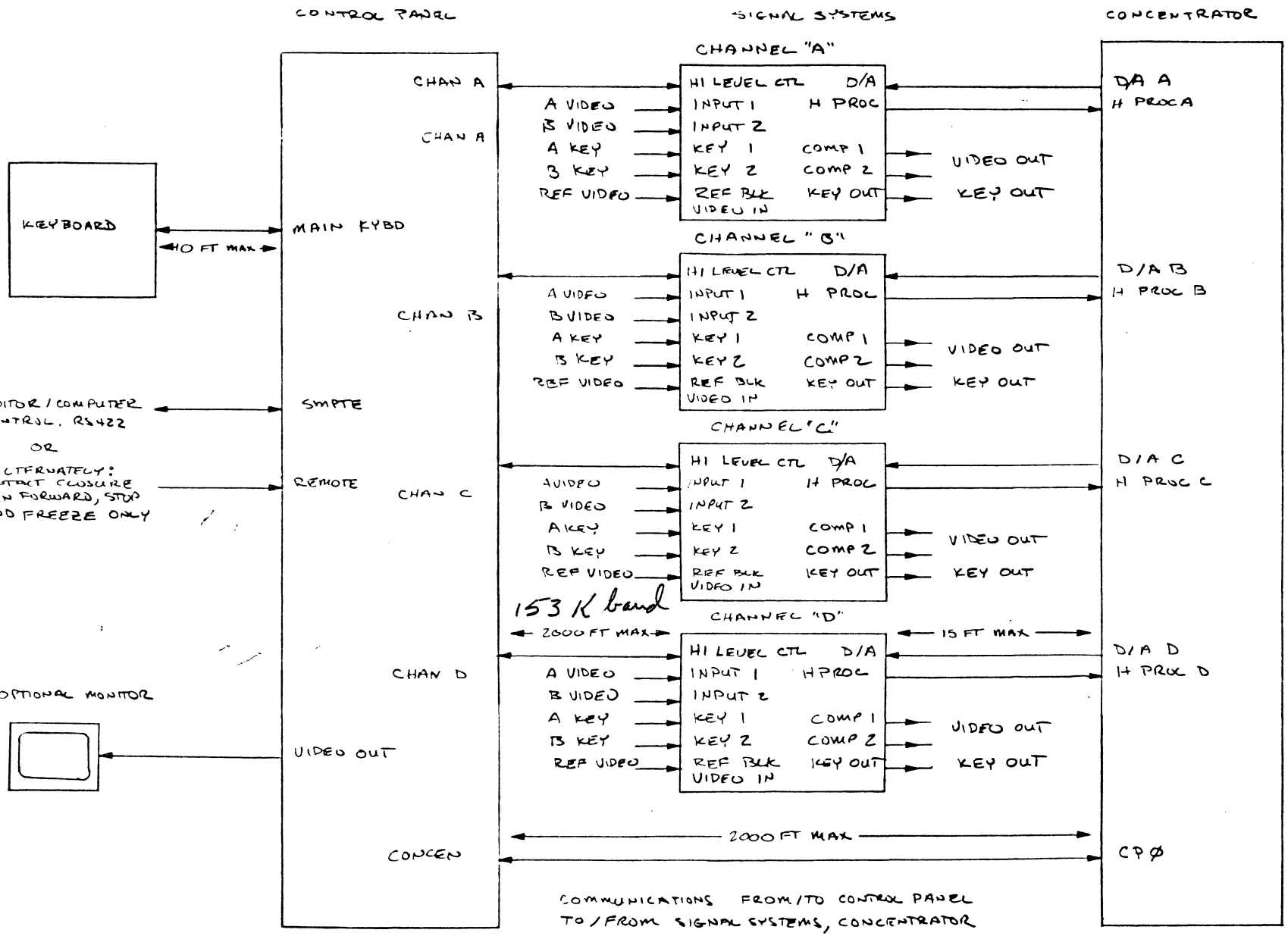
Not Active → 8

(Continued next page)

Signal System Chassis Connector Panel (Continued)

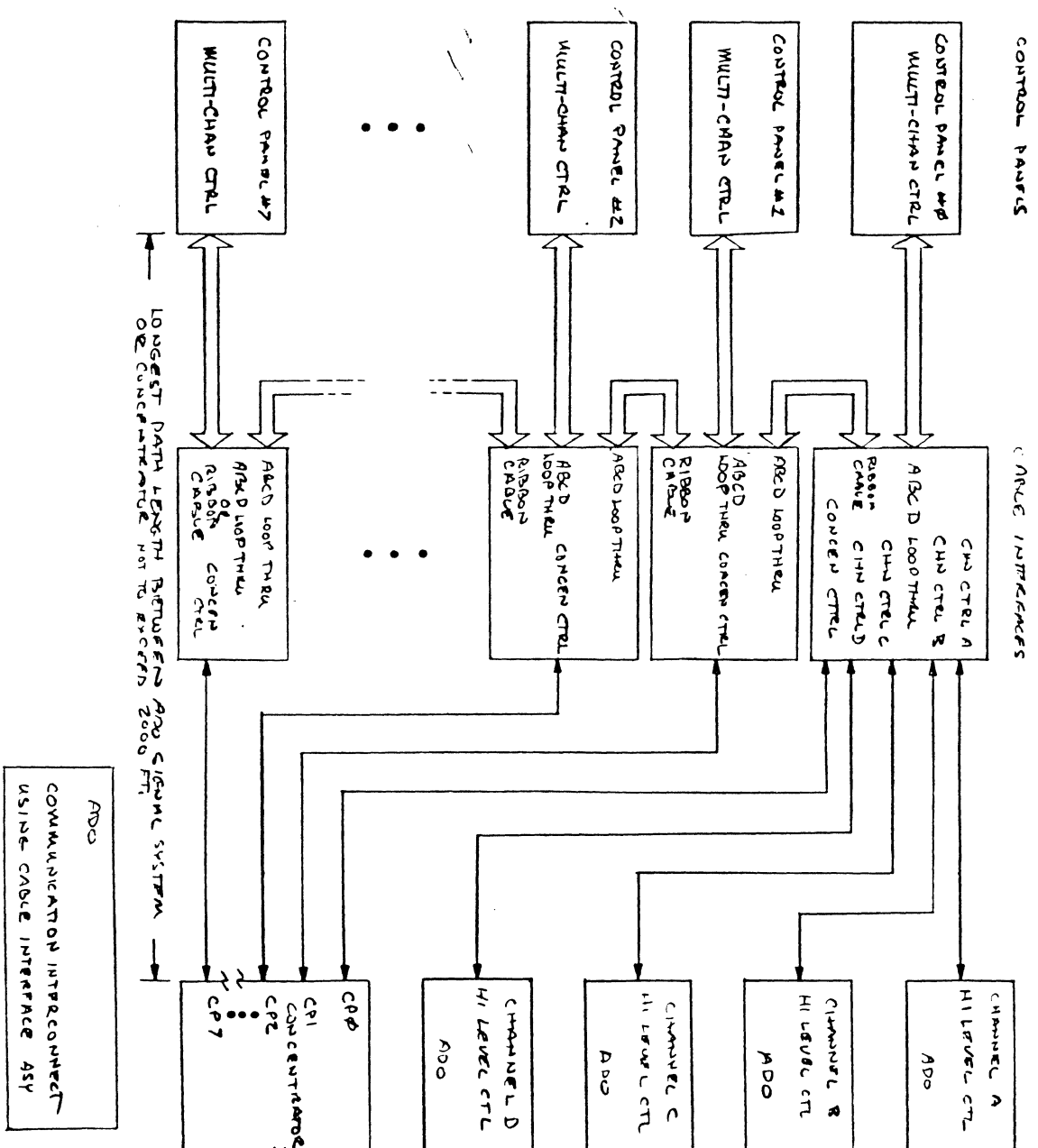


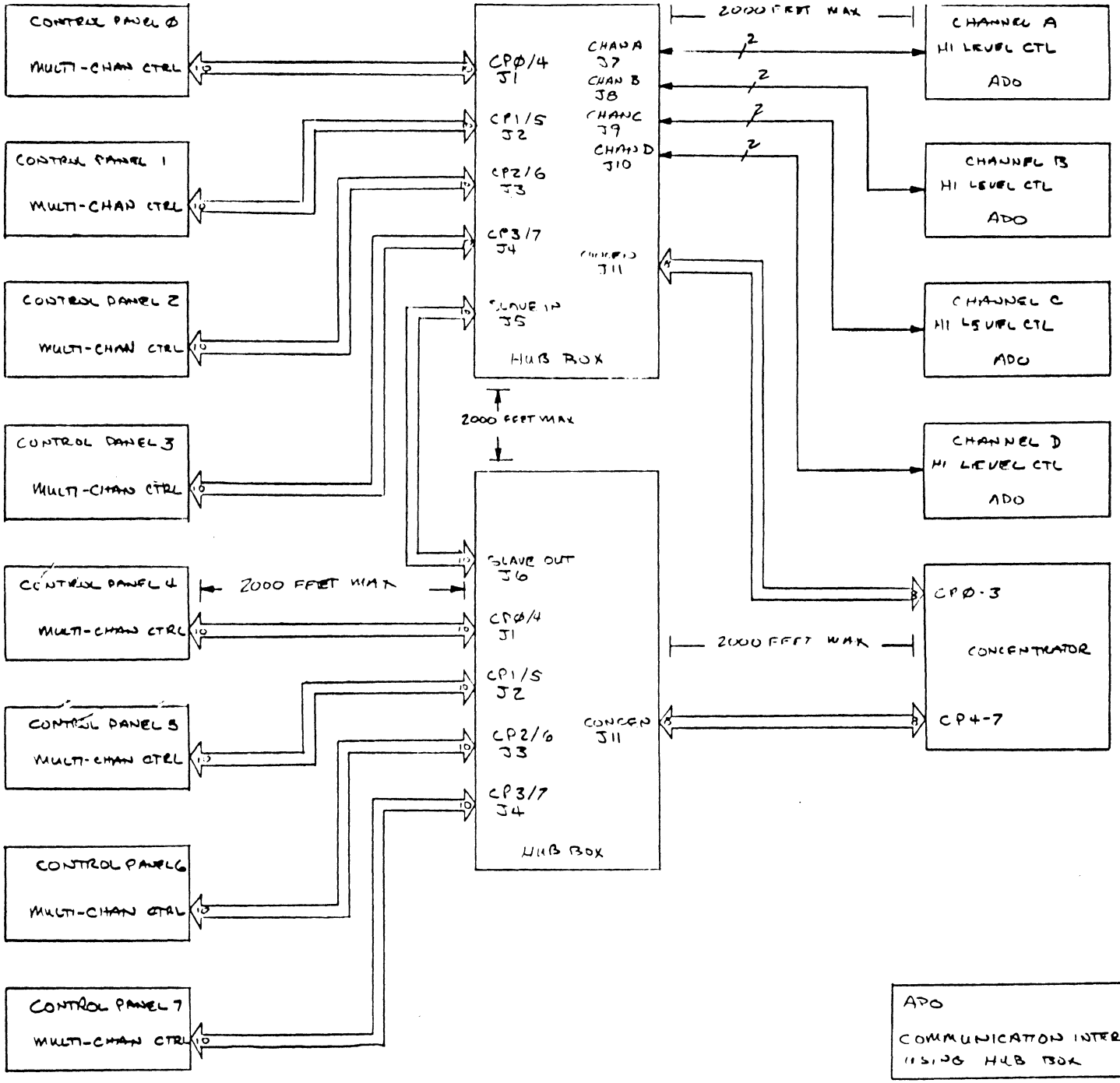
Reference No.	Number	Name	Type	Description
10	J10	COMP 2	BNC	Composite video output 2
11	J11	KEY OUT	BNC	Key output (noncomposite)
12	12	R (Not Active)	BNC	Red output (OPTIONAL)
13	J13	G (Not Active)	BNC	Green output (OPTIONAL)
14	J14	B (Not Active)	BNC	Blue output (OPTIONAL)
15	J15	INPUT 1	BNC	Composite video input 1 Input A)
16	J16	KEY 1	BNC	Key video input 1 (Input A) (OPTIONAL)
17	J17	COMP SYNC OUT OUT (Not Active)	BNC	Composite sync output (OPTIONAL)
18	J18	INPUT 2	BNC	Composite video input 2 (Input B)
19	J19	KEY 2	BNC	Key video input 2 (Input B) (OPTIONAL)
20	J20	REF BLK VIDEO IN	BNC	Station reference black burst video input

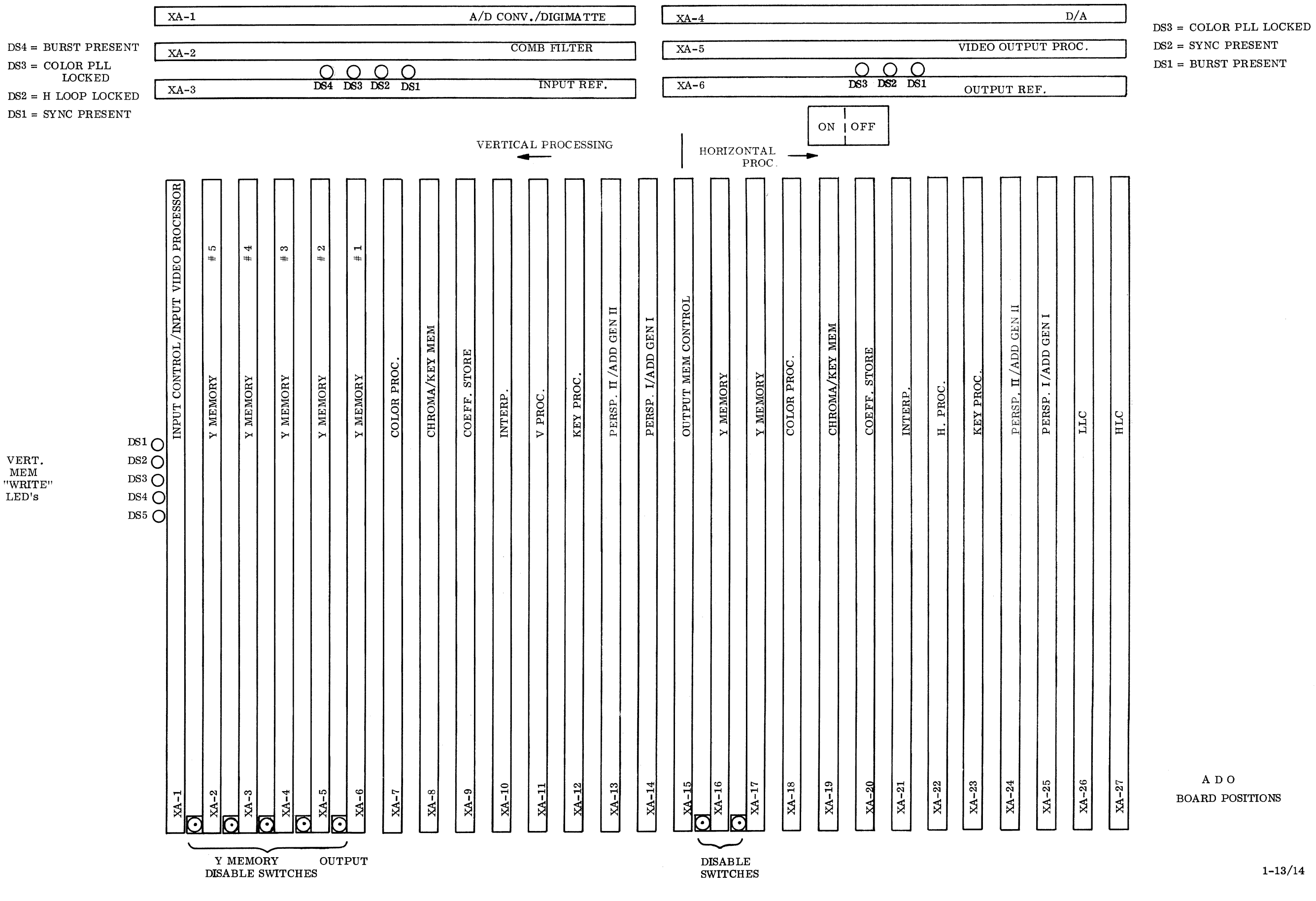


8/7-1

/0021 XX-007

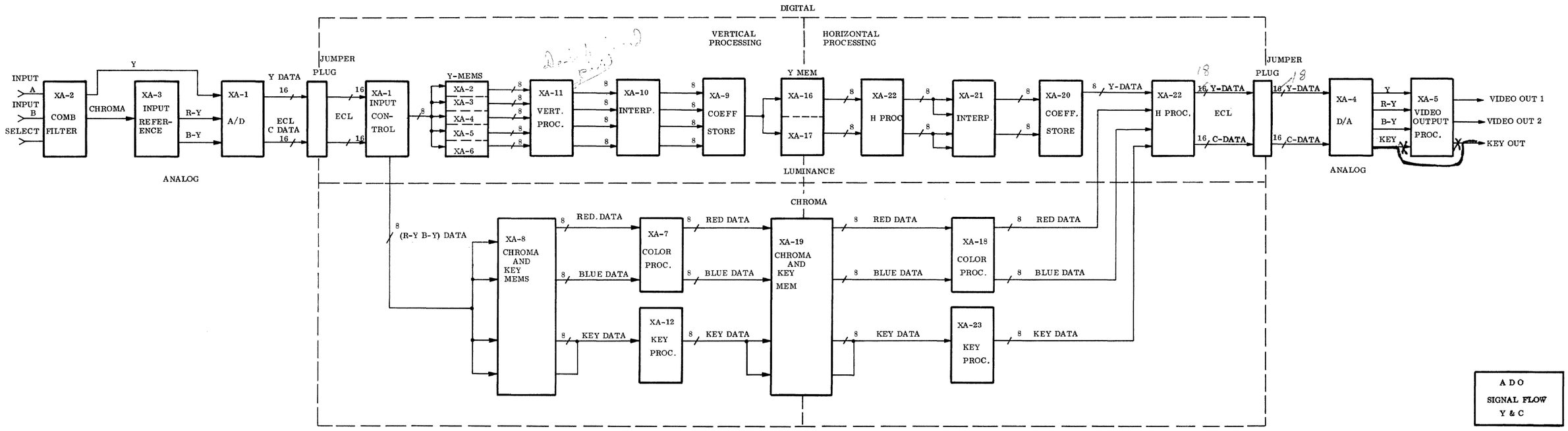

CONTROL PANELS
CONTROL PANEL #0
MULTI-CHAN CTRL
CONTROL PANEL #1
MULTI-CHAN CTRL
CONTROL PANEL #2
MULTI-CHAN CTRL
CONTROL PANEL #7
MULTI-CHAN CTRL
CABLE INTERFACES
CHN CTRL A
CHN CTRL B
A,B,C,D LOOP THRU
CHN CTRL C
CHN CTRL D
CONCEN CTRL
RIBBON CABLE
A,B,C,D LOOP THRU
A,B,C,D LOOP THRU CONCEN CTRL
RIBBON CABLE
A,B,C,D LOOP THRU
A,B,C,D LOOP THRU CONCEN CTRL
RIBBON CABLE
CHANNEL A HI LEVEL CTL ADO
CHANNEL B HI LEVEL CTL ADO
CHANNEL C HI LEVEL CTL ADO
CHANNEL D HI LEVEL CTL ADO
CP0
CP1 CONCENTRATOR
CP2
CP7
LONGEST PATH LENGTH BETWEEN ADO CIRCUIT SYSTEM OR CONCENTRATOR NOT TO EXCEED 2000 FT.
ADO
COMMUNICATION INTERCONNECT USING CABLE INTERFACE ASY



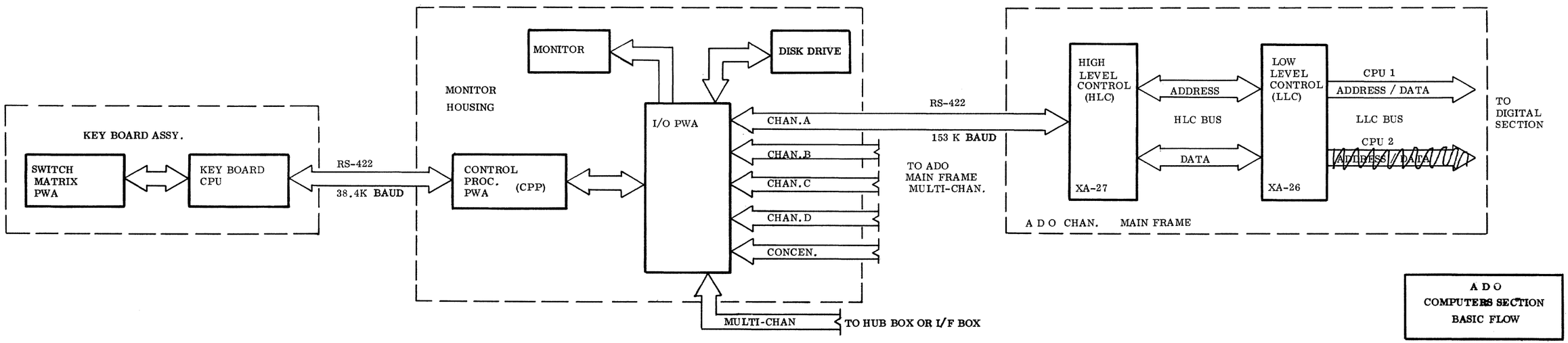


A D O
BOARD POSITIONS

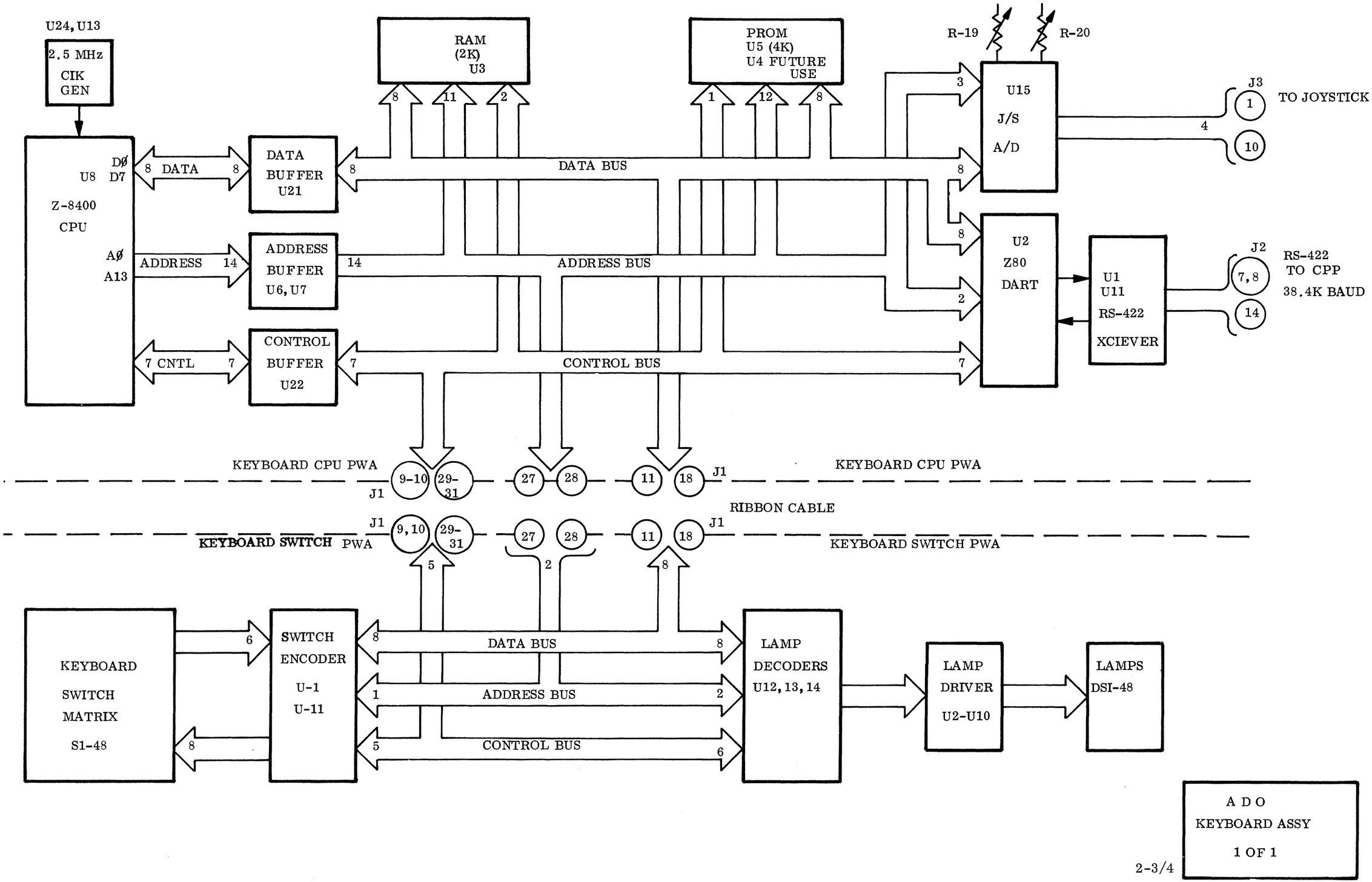
One frame Delay
input -to- output



ADO
SIGNAL FLOW
Y & C



A D O
COMPUTERS SECTION
BASIC FLOW



A D O
KEYBOARD ASSY
1 OF 1

Resets CPU each time!

1465021-02

U4, 5 CS
4K ROM

U3
24K RAM
(STATIC)

A12
G2A
A
B
U19
Y0
Y1
Y3

DATA BUS

U 21
DATA
BUFFER
T/R

Z - 80
CPU

D0
D7
A0
A15
M1
MREQ
IORQ
RD
WR
RESET

U6, 7
ADDRESS
BUFFER

U22
CONTROL
BUFFER

IORQ
M1
RD
U17, 18

ADDRESS BUS
A13
A0
A1

CONTROL BUS
MREQ

U24, 13
Q1
2.5MHz
CLK
Q

2.5 MHz

U9
AD
CLK
Ø

KEY
AD
CLK

RESET
Int

U10
Q
Q

RESET

RS-422
DRIVER/RECEIVER

U2
DART
D0
D7
A0
A1
M1
RD
CLK
IROQ
DTRA
TXDA
RXDA

U11
U1

J2
15
8
14
7
TO CPP

U14
+5V
REG
7

M1 RD Ø
IORQ
A3

RD
WR
U16
13
1
U16
U12, 17

AD CLK
A0
A1
A2
ADD
ALE
IN0
IN1
IN2
OE U15
A/D
+REF
-REF
D0
D7
EOC

6 X AXIS
8 Y AXIS
9 Z AXIS
JOYSTICK

+5V
R19
+5V
R20

DATA BUS
D0
U12, 17
U23

KEY BOARD
C P U

32 7 28 27 12 17 30 34 J1

RIBBON
CABLE

32 7 23 27 12 17 30 34

KEY
A0
A1
AD
CLK

SWITCH
MATRIX
S1 through S48

RL0 - AL6

RL0
RL6
CS
CLK
A0
RES
WR
RD
U11

DATA BUS
CONTROL BUS

P1
P2
P3
RES
WR
RD
CS
LAMP
DECODERS
U12, 13, 14
A0
A1

24
24
24
24
24
24

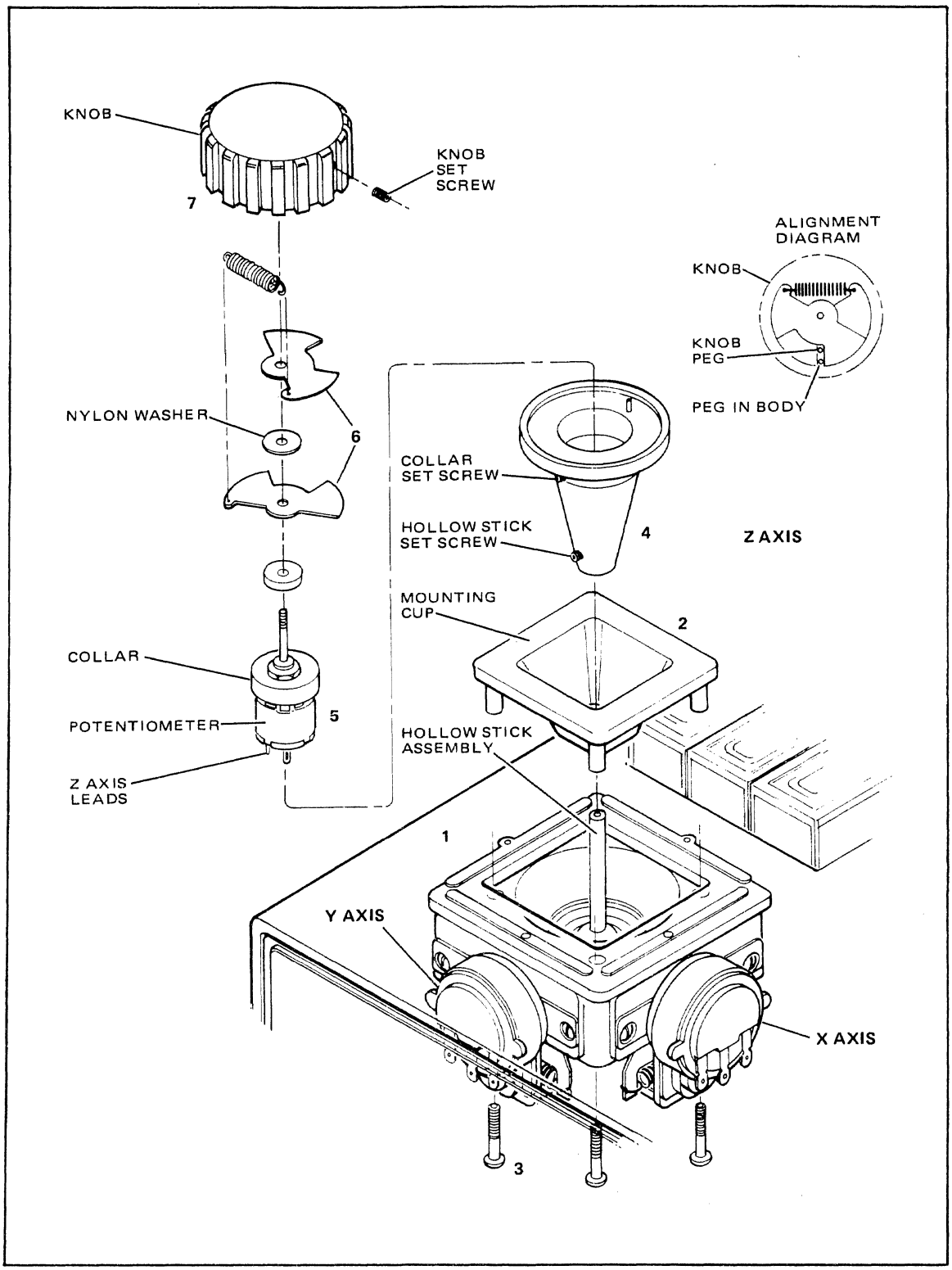
LAMP
DRIVERS
U2-10

LAMPS

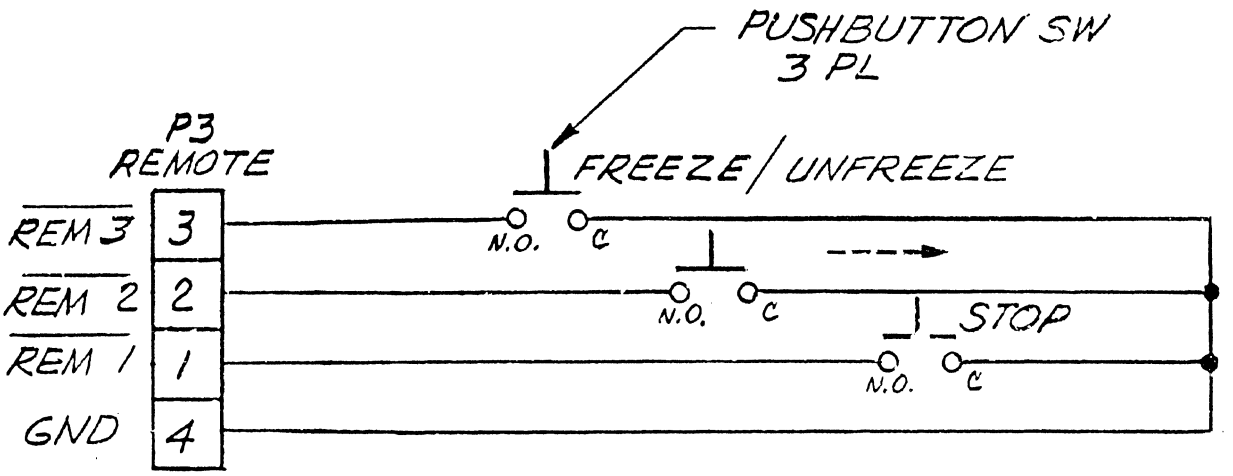
OUT 1
OUT 7
U 1
A
B
C

KEYBOARD SWITCH MOUNTING PWA

A D O
KEYBOARD ASSY
CONTROL FLOW
2-5/6



Joystick Assembly



External Remote Control Cable

Not Active

BAUD CLK 5K, 5L

J5

SMPTE 3,4

5,6

MAIN KYBD 17,18

15,16

AUX KBYD 21,22

23,24

MAINT. 9,10

11,12

4 UART'S 5N, 5P, 5S, 5T

38.4 Kbaud

RS-422 4U, 5V 4W, 5U

CPP TO KEYBOARD — DATA BLOCK TO KEYBOARD IS ACTIVE EVERY FIELD CONTAINS COMMAND FOR KEYBOARD LAMP. 3ms

DATA BITS HAVE 1 START BIT(LOW) FOLLOWED BY SYNC CHAR. 300 NS

KEYBOARD TO CPP — DATA BLOCK CONTAINS X, Y, & Z JOYSTICK INFO. & KEY PRESSED DATA.

DATA BLOCK FROM KEYBOARD TO CPP WILL ONLY COME AFTER BEING PULLED BY CPP.

1 FIELD TIME 17 ns

RAM 64K 3N, 4N, 3P, 4P, 3R, 4R, 4S, 3S, 3M, 4M, 3L, 4L, 3K, 4K, 3L, 4L

EE PROM 2D

000-07E 2716-3 Intel

RAM ADDRESS

PROM 6U, 6N 7U, 7N, 6W, 6M, 7W, 7M 7P, 6P

RAM CONTROL & BUFFERING 3E, 3H, 4G, 4H, 4T, 3T

EE PROM CNTL. 3C, 4B, 5C, 1A

J2 J7

A0 A7 A8 A15

D0 D7 D8 D15

I/O PWA

4 MHz

CLK GEN. 7F & 7E

6 MHz

CLK

Z - 8002 CPU 6E

AD0 AD15

AS

ADDRESS STROBE

16 DATA/ADDRESS

ADDRESS LATCH 7H, & 6 H

DATA BUFFER 6J & 7J DIR

DS

9 CONTROL BUS

CONTROL & STATUS BUFFERS 5D & 5E

MREQ DS R/W N/S B/W ST0 ST3

RESET

MANUAL RESET E4 E5

4D 33 ms OS

RESET

BUFFER, DRIVER 2P, U, R, S, T

SWITCHES 1S-1-8 1T-1-8

REMOTE CMD RECEIVER 2Y, 2W

SEL

J10 P-3

MONITOR HOUSING BACK PANEL CONNECTOR

STOP

FREEZE/ UNFREEZE

REMOTE

CPP SWITCH FUNCTIONS

1S-1 NOT USED

1S-2 ON=PAL OFF=NTSC

CONTROL PANEL 1D

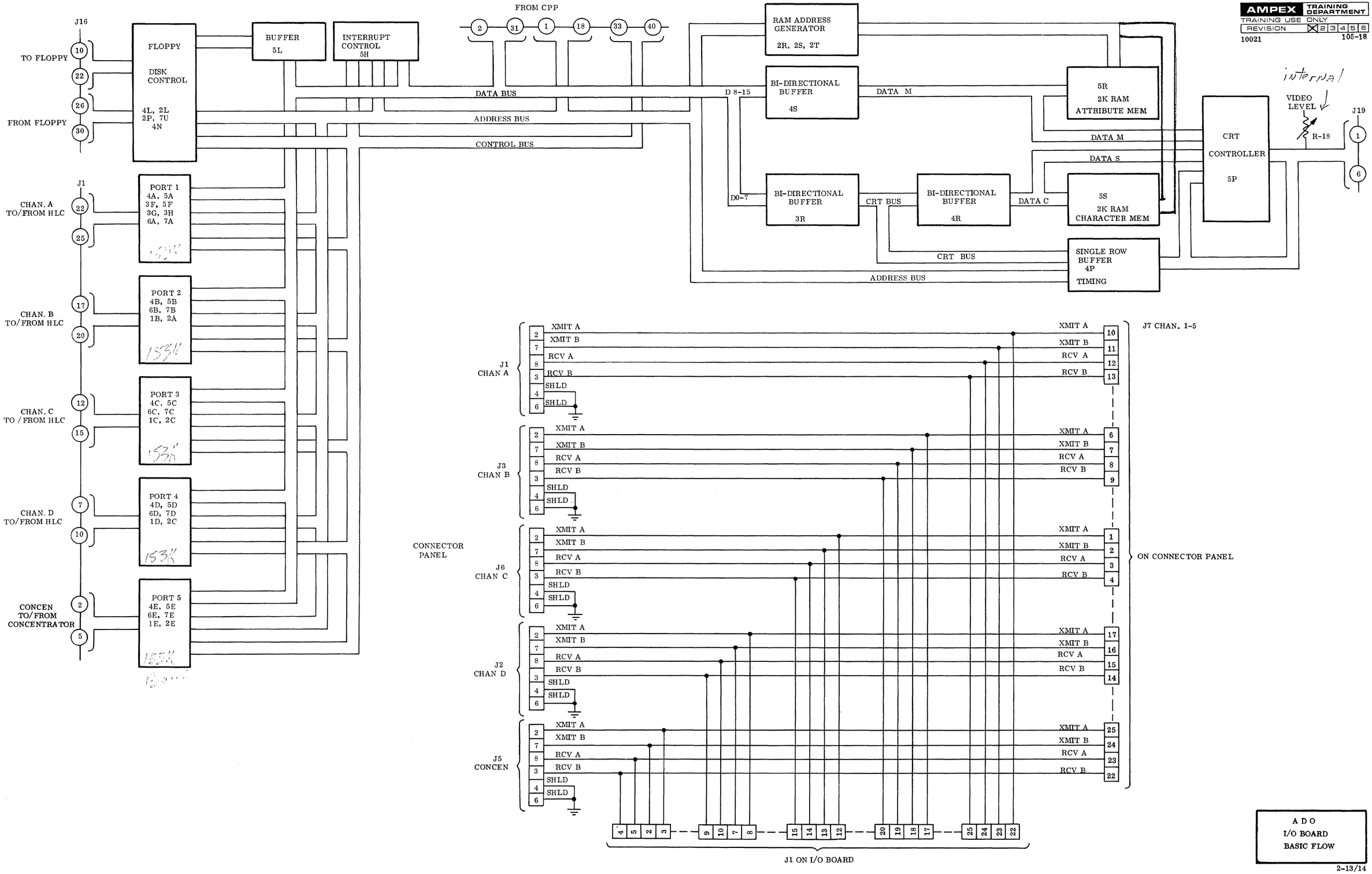
	1S-3	1S-4	1S-5
0	ON	ON	ON
1	OFF	ON	ON
2	ON	OFF	ON
3	OFF	OFF	ON
4	ON	ON	OFF
5	OFF	ON	OFF
6	ON	OFF	OFF
7	OFF	OFF	OFF

1S-6-8 NOT USED

1T-1-8 NOT USED

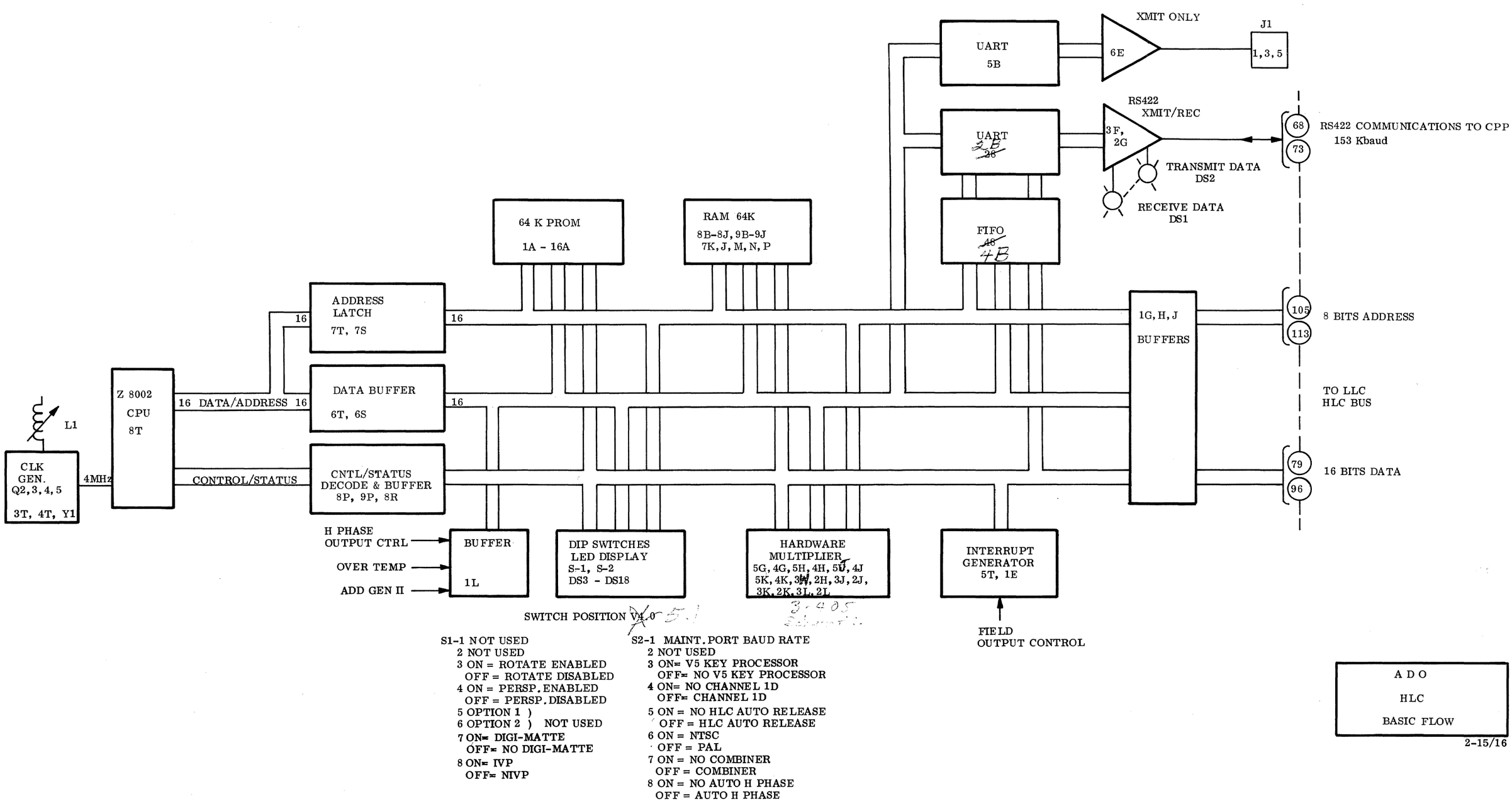
A D O C.P.P.

2-11/12



A D O
I/O BOARD
BASIC FLOW

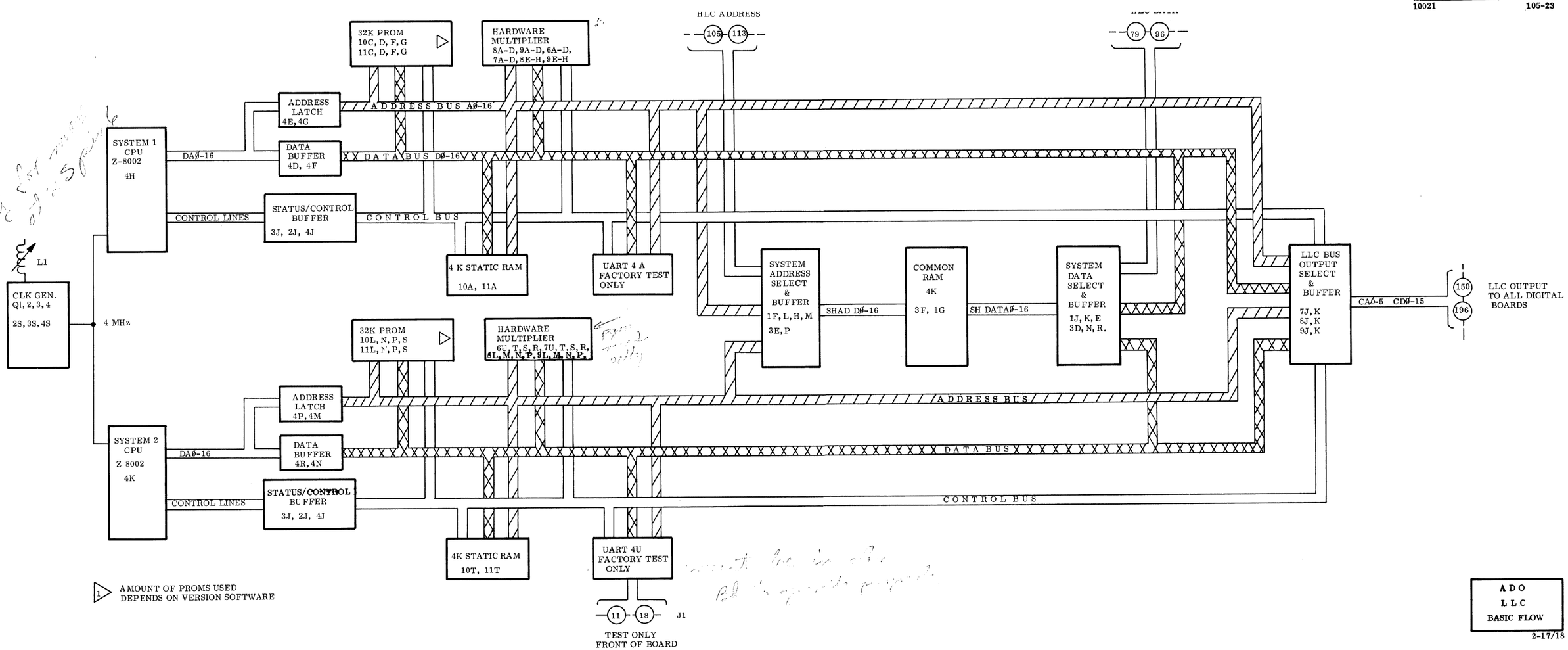
2-13/14



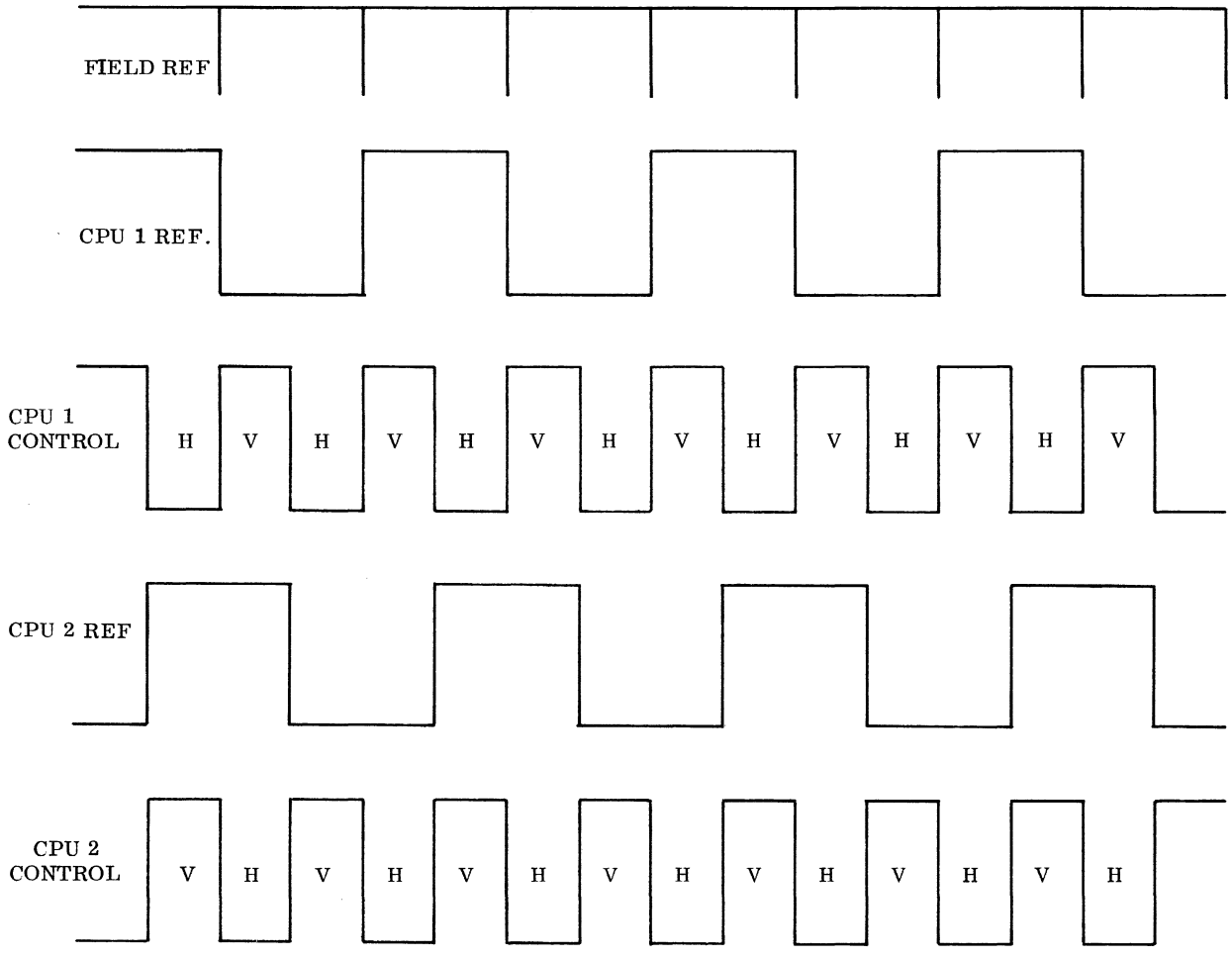
S1-1 NOT USED
2 NOT USED
3 ON = ROTATE ENABLED
OFF = ROTATE DISABLED
4 ON = PERSP. ENABLED
OFF = PERSP. DISABLED
5 OPTION 1)
6 OPTION 2) NOT USED
7 ON= DIGI-MATTE
OFF= NO DIGI-MATTE
8 ON= IVP
OFF= NIVP

S2-1 MAINT. PORT BAUD RATE
2 NOT USED
3 ON= V5 KEY PROCESSOR
OFF= NO V5 KEY PROCESSOR
4 ON= NO CHANNEL 1D
OFF= CHANNEL 1D
5 ON = NO HLC AUTO RELEASE
OFF = HLC AUTO RELEASE
6 ON = NTSC
OFF = PAL
7 ON = NO COMBINER
OFF = COMBINER
8 ON = NO AUTO H PHASE
OFF = AUTO H PHASE

A D O
HLC
BASIC FLOW
2-15/16



ADO
LLC
BASIC FLOW
2-17/18



V = VERTICAL SECTION (INPUT)

H = HORIZONTAL SECTION (OUTPUT)

LOGICAL TIMING DIAGRAM OF LLC COMP. BUS CONTROL OF V & H SECTIONS IN THE ADO.

ADO
LLC
FIELD TIMING

2-19/20

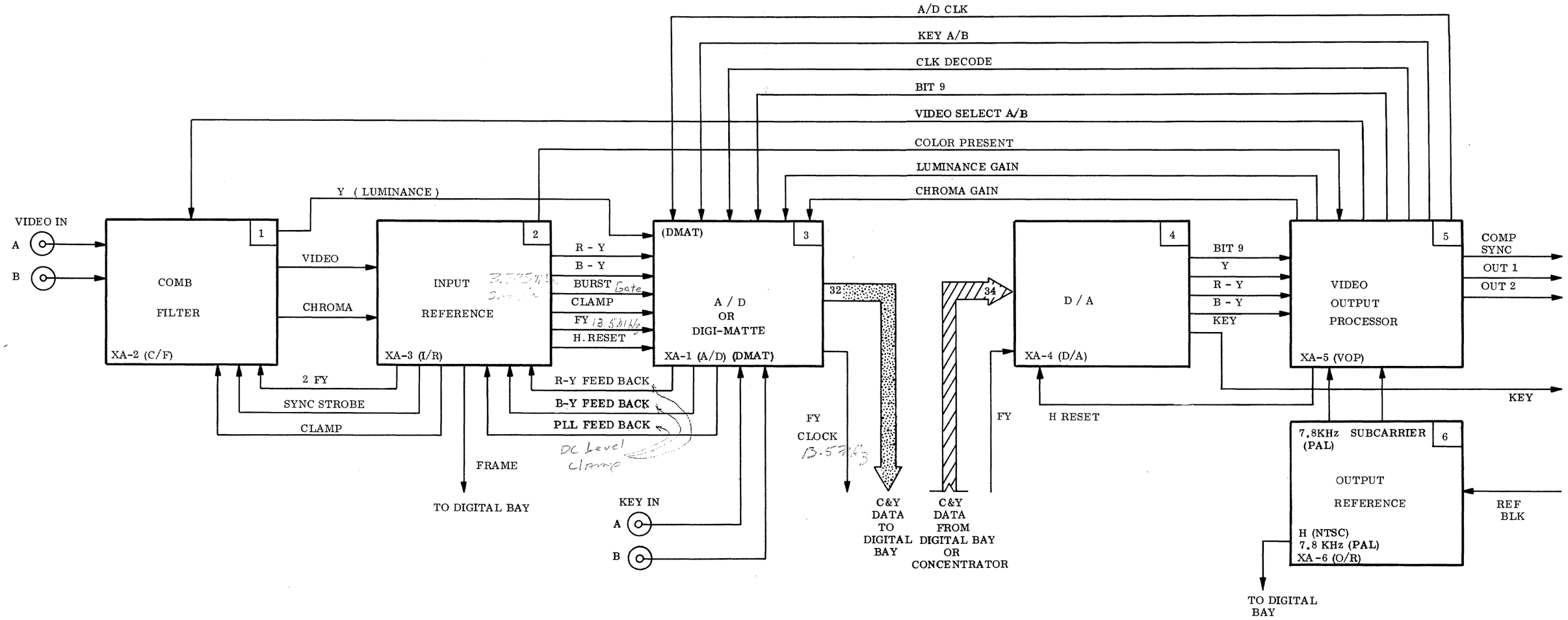
AMPEX TRAINING DEPARTMENT

TRAINING USE ONLY

REVISION 1 2 3 4 5 6

10021-01

105-22



ADO
ANALOG FLOW
(IN/OUT)

3-1/2

COMB FILTER SET UP

Equipment required:

Tektronix 465 Oscilloscope or equivalent. Scope must have a vertical channel output.
Vectorscope, Tektronix 520 or equivalent.
Spectrum Analyzer, HP or equivalent.

1. Select reverse color bars from the signal generator.

2. Connect Channel 1 scope probe to TP13, One Line Delayed Video. Channel 2 to TP14, Two Line Delayed Video. Invert Channel 2 and add Channel 1 and Channel 2. Adjust R315, Y Gain, for a match in the DC levels between TP13 and TP14. The luminance should be canceled at this point.

3. Turn off the B-Y signal from the signal generator. Externally lock the vectorscope. Connect the vertical output from the scope to the vectorscope. Connect Channel 1 of the scope to TP12, Undelayed Video. Note the position of the R-Y vectors. Connect the scope to TP13. Adjust L23, C1 Phase, for maximum amplitude at TP10 and then adjust L23 for a phase difference of 180 degrees between TP12 and TP13.

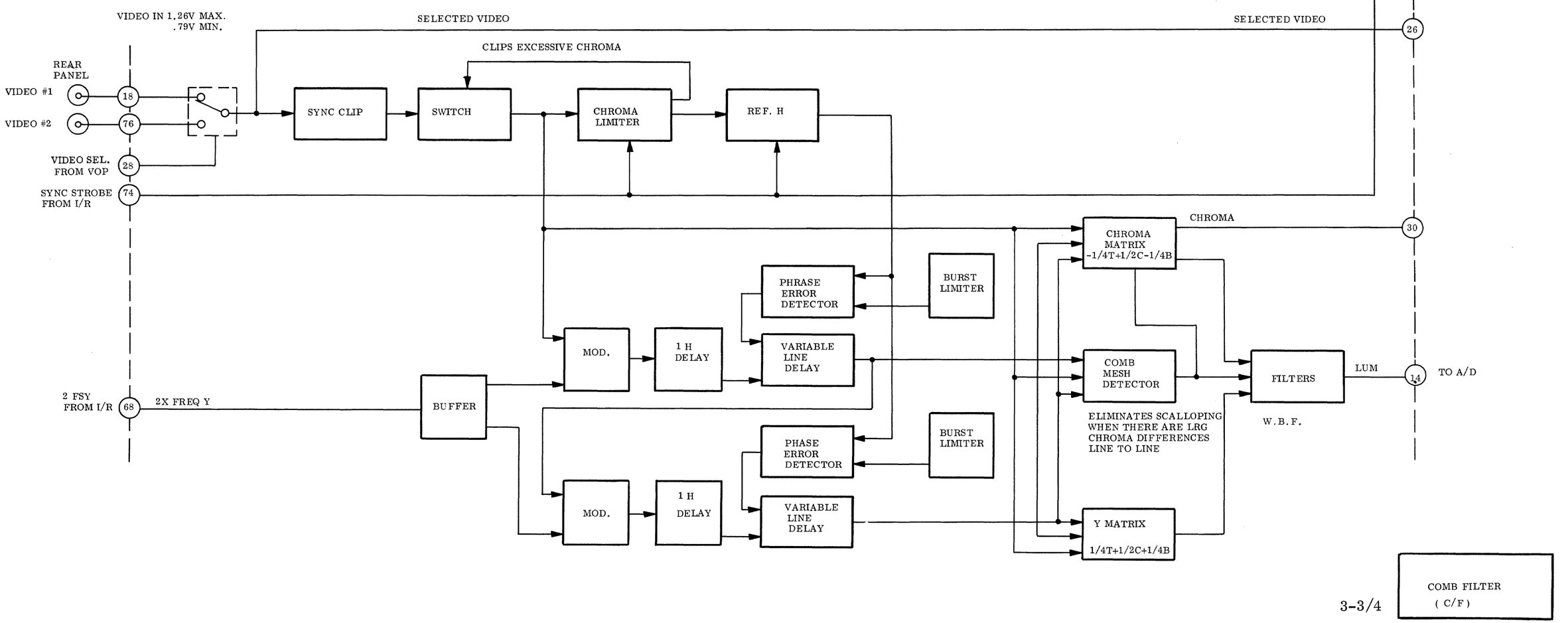
4. Scope probe to TP14. Adjust L42, C2 Phase, for maximum amplitude at TP11 and then adjust L42 for a phase difference of 360 degrees between TP12 and TP14.

5. Channel 2 scope probe to TP3, adjust L47 for maximum amplitude of chroma at TP3. Channel 1 scope probe to TP8 and channel 2 scope probe to Pin 14. Observe the area where the color bars reverse. Adjust R268 for no chroma spikes in the picture and no spikes in the middle of switch pulse at TP8. Check the switch pulse at the beginning and end of the field, re-adjust R268 if necessary.

6. Observe the color bar switch point at Pin 14, Y Out. Adjust R103 for the best match between the adaptive and non adaptive mode video levels. Switch the signal generator to a 1T pulse. Adjust C206 for minimum ringing at the switch point.

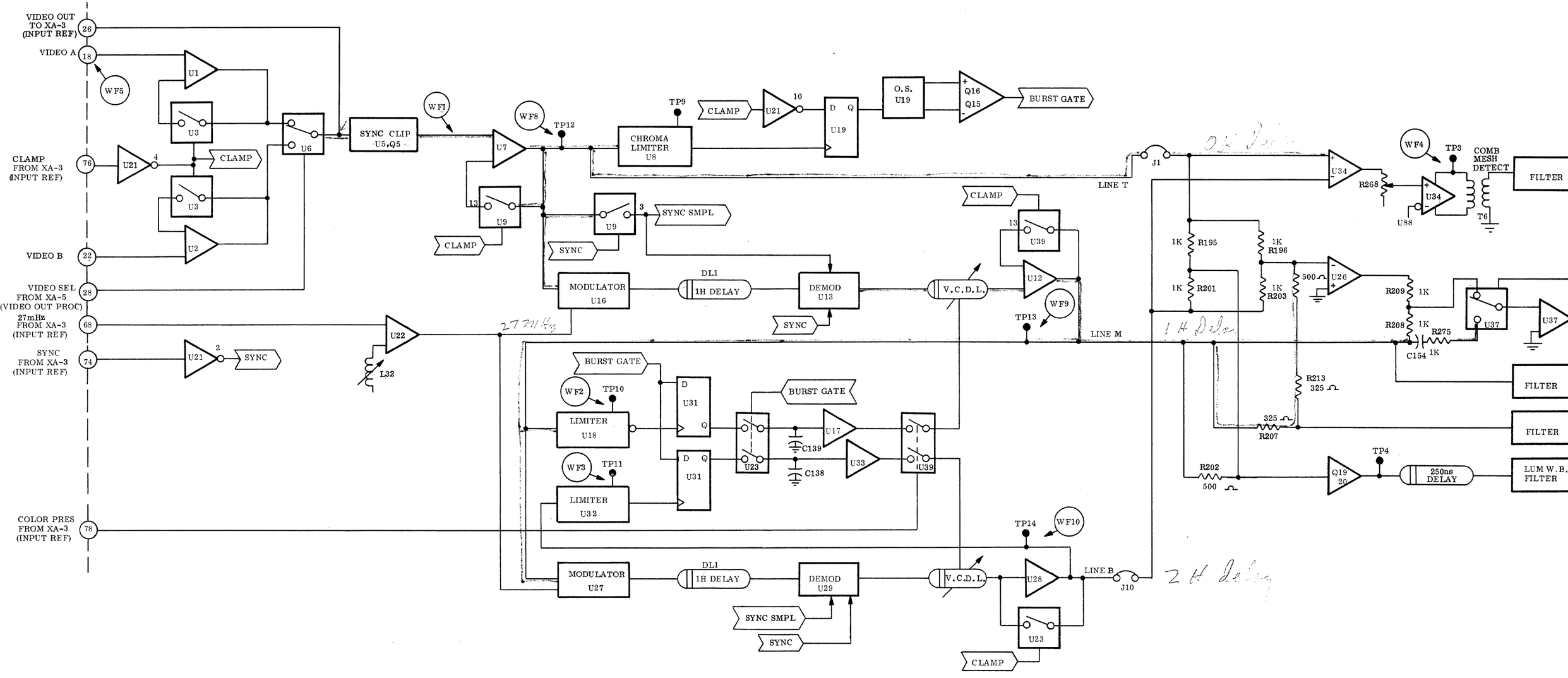
7. Final tweek. Switch the signal generator to reverse color bars. Observe Pin 14 with the spectrum analyzer. The chroma should be more than 40db below that of the luminance. If not, re-adjust L23, L42 and R315 for the chroma to be more than 40db below luminance.

8. Expand the picture and rotate. Look for moire in the picture, there should be none. Moire in the picture indicates a mis-adjustment of the Comb Filter PWA.



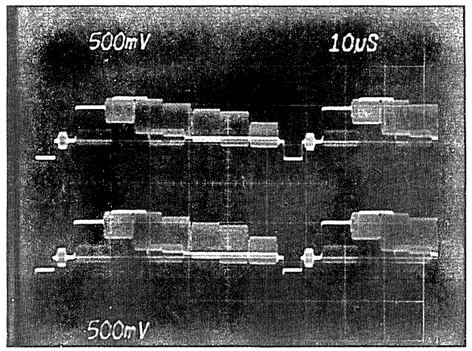
3-3/4

COMB FILTER
(C/F)


VIDEO OUT TO XA-3 (INPUT REF)
26
VIDEO A
18
WF5
U1
U3
U6
CLAMP FROM XA-3 (INPUT REF)
76
U21
4
CLAMP
U3
U2
VIDEO B
22
VIDEO SEL FROM XA-5 (VIDEO OUT PROC)
28
27mHz FROM XA-3 (INPUT REF)
68
SYNC FROM XA-3 (INPUT REF)
74
U21
2
SYNC
COLOR PRES FROM XA-3 (INPUT REF)
78
U22
L32
SYNC CLIP U5,Q5
WF1
U7
WF8
TP12
13
U9
CLAMP
U9
3
SYNC SMPL
SYNC
MODULATOR U16
DL1
1H DELAY
DEMOD U13
SYNC
TP9
CLAMP
U21
10
D Q
U19
O.S. U19
Q16
Q15
BURST GATE
CHROMA LIMITER U8
LINE T
J1
CLAMP
13
U39
U12
WF9
TP13
LINE M
V.C.D.L.
BURST GATE
WF2
TP10
LIMITER U18
D
U31
Q
WF3
TP11
LIMITER U32
D Q
U31
BURST GATE
U23
C139
C138
U17
U33
U39
MODULATOR U27
DL1
1H DELAY
DEMOD U29
SYNC SMPL
SYNC
V.C.D.L.
TP14
WF10
U28
LINE B
J10
U23
CLAMP
J1
U34
R268
WF4
TP3
COMB MESH DETECT
FILTER
U88
T6
1K R195
1K R196
1K R201
1K R203
500
U26
R209 1K
R208 1K
R275
C154 1K
U37
R213 325
325
R207
R202 500
Q19 20
TP4
250ns DELAY
FILTER
FILTER
LUM W.B. FILTER

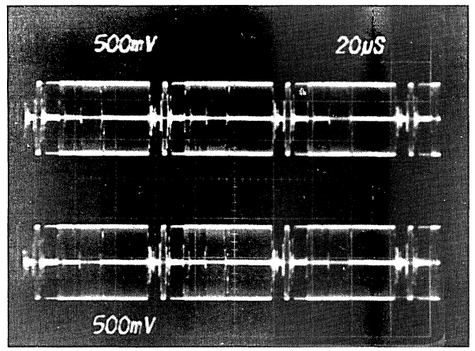
WF1
WF8
TP12
U7
CHROMA LIMITER U8
TP9
CLAMP
U21
10
D Q U19
O.S. U19
Q16 Q15
BURST GATE
J1
LINE T
U34
R268
WF4
TP3
COMB MESH DETECT
U34
U88
T6
FILTER
TP8
13 U9
CLAMP
3 U9
SYNC
SYNC SMPL
DL1
MODULATOR U16
1H DELAY
DEMOD U13
SYNC
V.C.D.L.
CLAMP
13 U39
U12
WF9
TP13
LINE M
1K R195
1K R201
1K R196
1K R203
500
U26
R209 1K
R208 1K
R275
C154 1K
U37
U37
WF6
30
CHROMA OUT TO XA-3 (INPUT REF)
27 MHz
1 H Dly.
BURST GATE
WF2
TP10
LIMITER U18
WF3
TP11
LIMITER U32
D U31 Q
D Q U31
BURST GATE
U23
C139
C138
U17
U33
U39
R213 325
325 R207
FILTER
TP7
R103
TP5
J14
FILTER
1K
1K
U11
U11
WF7
14
Y OUT TO XA-1 (A/D)
R202 500
Q19 20
TP4
250ns DELAY
LUM W.B. FILTER
TP6
U20
TP14
WF10
MODULATOR U27
DL1
1H DELAY
DEMOD U29
SYNC SMPL
SYNC
V.C.D.L.
U28
LINE B
J10
2 H delay
U23
CLAMP

A D O
NTSC
COMB FILTER
3-5/6



VIDEO IN
PIN 18 (TRIGGER) WF5

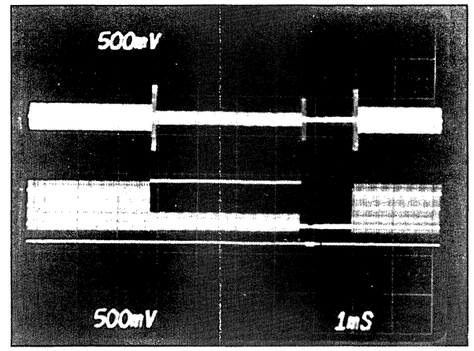
EMITTER Q-5 WF1



LINE 2 CHROMA
AT TP10 WF2

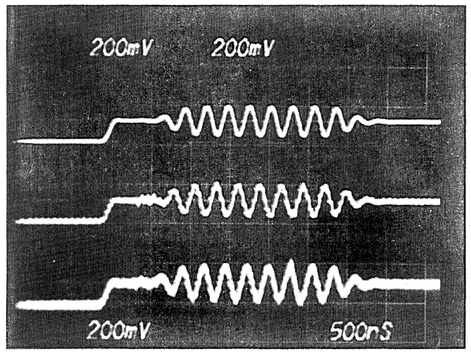
LINE 1 CHROMA
AT TP11 WF3

(TRIGGER VIDEO IN)



CHROMA AT TP3 WF4

VIDEO IN
PIN 18 (TRIGGER) WF5

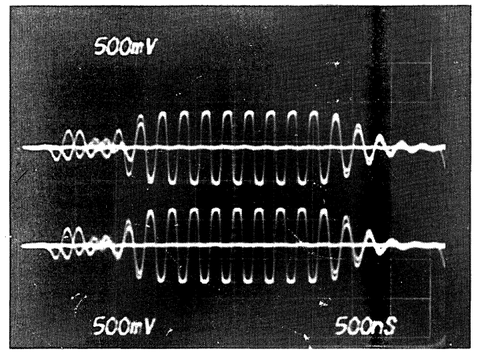


BURST OF LINE T
TP12 WF8

BURST OF LINE M
TP13 WF9

BURST OF LINE B
TP14 WF10

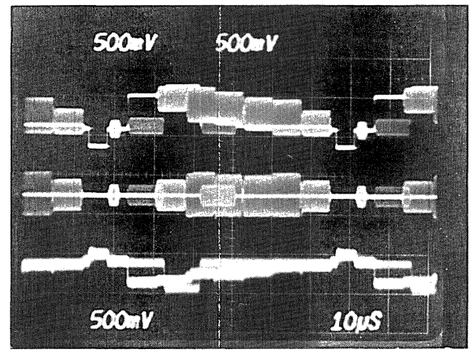
(TRIGGER VIDEO IN)



EXPANDED VIEW
OF TP10 WF2

180°
PHASE DIFFERENCE

EXPANDED VIEW
OF TP11 WF3

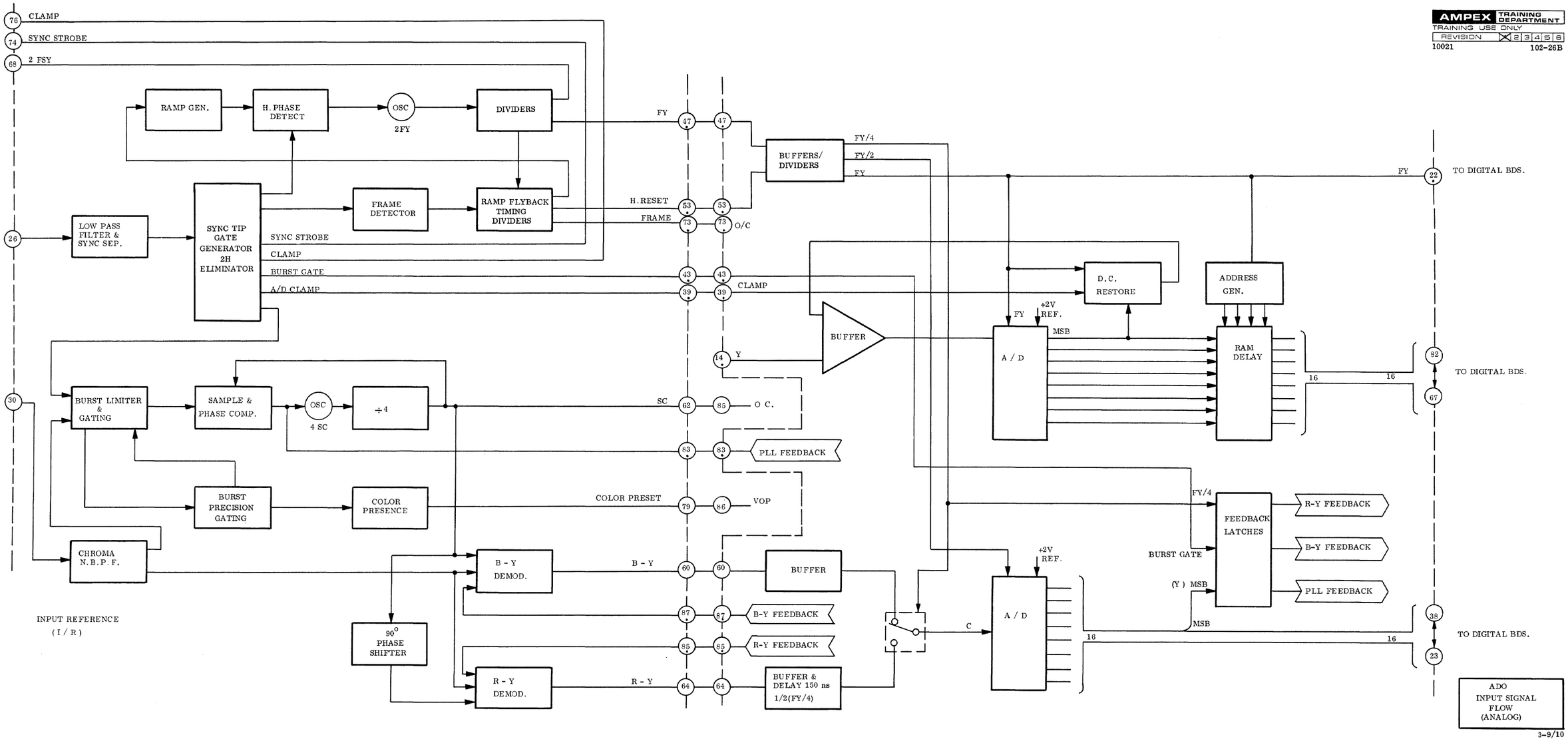


VIDEO IN
PIN 18 (TRIGGER) WF5

CHROMA OUT
PIN 30 WF6

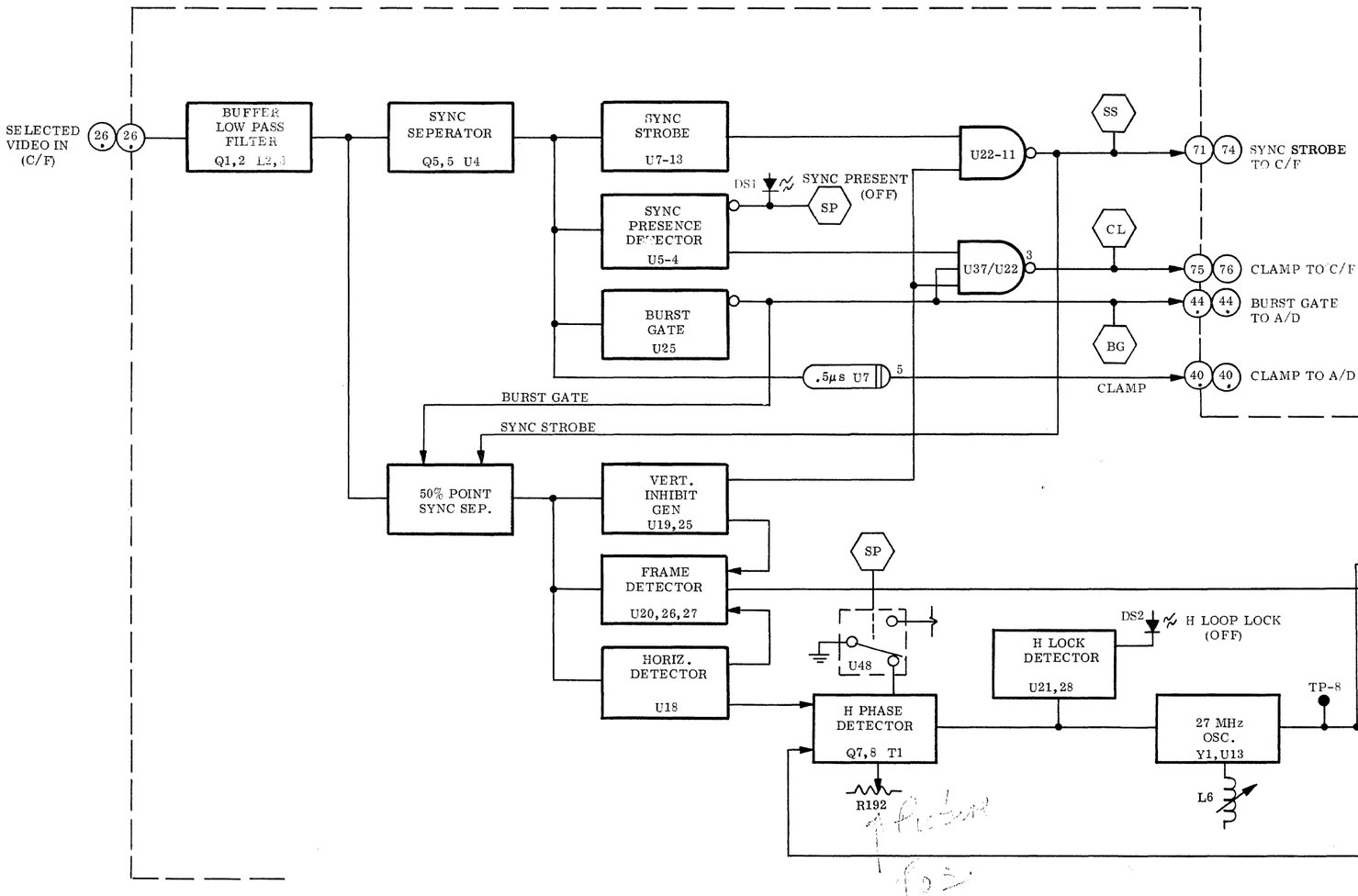
Y OUT
PIN 14 WF7

ADO
COMB FILTER
WAVEFORMS



ADO
INPUT SIGNAL
FLOW
(ANALOG)

3-9/10


SELECTED VIDEO IN (C/F)
26
26
BUFFER LOW PASS FILTER Q1,2 L2,3
SYNC SEPERATOR Q5,5 U4
SYNC STROBE U7-13
SYNC PRESENCE DETECTOR U5-4
BURST GATE U25
.5µs U7
5
DS1
SYNC PRESENT (OFF)
SP
U22-11
U37/U22
3
SS
CL
BG
71
74
SYNC STROBE TO C/F
75
76
CLAMP TO C/F
44
44
BURST GATE TO A/D
40
40
CLAMP TO A/D
CLAMP
BURST GATE
SYNC STROBE
50% POINT SYNC SEP.
VERT. INHIBIT GEN U19,25
FRAME DETECTOR U20,26,27
HORIZ. DETECTOR U18
U48
H PHASE DETECTOR Q7,8 T1
R192
H LOCK DETECTOR U21,28
DS2
H LOOP LOCK (OFF)
27 MHz OSC. Y1,U13
L6
TP-8
÷ 2 U15
2 Fy (27MHz)
Fy (13.5MHz)
÷ 864 PAL ÷ 858 NTSC U9,10,11,24
PULSE FORMER DELAY U24,30,31
÷ 525 U1,2,3
HORIZ.
U13
14
15
67
67
68
68
2Fy TO C/F
2
3
47
47
48
48
Fy TO A/D
54
54
H TO A/D
74
74
FRAME TO O/R
LIMITER U33
BURST PRESENT
DS4
GATE
BURST PRESENT DETECTOR U43-1 CR18
TP7
BG
LATE BURST GATE GENERATOR U39,U37-8
CL
SS
COLOR PRESENT
R78
TP-1
Q16,17
CHROMA FROM C/F
30
30
BAND PASS FILTER, AMPLIFIER Q14/Q15

SS
CL
BG
CLAMP
SYNC STROBE TO C/F
CLAMP TO C/F
BURST GATE TO A/D
CLAMP TO A/D

LIMITER U33
BURST PRESENT DS4
GATE
PHASE COMPARATOR Q24, T5 CR8-11
TP6
L18
FOUR TIMES SUBCARRIER OSCILLATOR Q21, 22, Y2
TP5
FOUR PHASE DIVIDE BY 4 U55
U48
TP7
BURST PRESENT DETECTOR U43-1 CR18
FEED BACK CONTROL Q20
LATE BURST GATE GENERATOR U39, U37-8
7.8KHz DETECTOR
PHASE LOCK DETECTOR U47, U28-13
DS3 (OFF) COLOR PLL LOCKED
DIVIDE BY TWO U42-5
J5/J6
COLOR PLL FEEDBACK FROM A/D
PAL SEQ TO VOP
COLOR PRESENT
TO V.O.P.
TO COMB FILTER
R-Y FEEDBACK
R-Y TO A/D
R156
R-Y DEMODULATOR AND FILTER T6, T8, U41
B-Y DEMODULATOR AND FILTER T4, U34
B-Y FEEDBACK
B-Y TO A/D
R78
BAND PASS FILTER, AMPLIFIER Q14/Q15
TP-1
Q16,17
CHROMA FROM C/F
HORIZ.
2 Fy (27MHz)
U13
2Fy TO C/F
Fy (13.5MHz)
Fy TO A/D
H TO A/D
FRAME TO O/R
DS2 H LOOP LOCK (OFF)
H LOCK DETECTOR U21, 28
27 MHz OSC. Y1, U13
L6
TP-8
÷ 2 U15
÷ 864 PAL ÷ 858 NTSC U9, 10, 11, 24
PULSE FORMER DELAY U24, 30, 31
÷ 525 U1, 2, 3

ADO INPUT REF.
1 OF 1
3-11/12

CHROMA GAIN FROM V.O.P. 42 55

R-Y FROM INPUT REF. 64 64

BUFFER Q-16 U-35

148 ns DELAY

Q10, 11, 13, 14

B-Y FROM INPUT REF. 60 60

Q-5 U-19

Vrb D8 IN U28 CHROMA A/D CONV. D1

LSB

MSB

U25 U30 TTL/ ECL CONV.

R-Y, B-Y DATA ECL

67 145 82 162 R-Y, B-Y DATA TO DIGITAL CHASSIS

FEEDBACK LATCHES

D U26 U27 U34

86 86 R-Y FEED BACK TO I/R

D U26 U31 U34

88 88 B-Y FEED BACK TO I/R

FY FROM INPUT REF. 53 53 13.5 MHz

H RESET FROM I/R 54 54

CLK DEVIDER U24, U29

Fy/4

Fy/2

Fy/4

Fy/4

Fy

MSB SAMPLE

U20 U27 U31 U33

84 84 PLL FEED BACK TO I/R

CLAMP FROM I/R 40 40

BURST GATE FROM I/R 43 43

REF. VOLTAGE GEN. U13, U18 Q4, Q7

-6V TO A/D U28

-6V TO A/D U5

-2V REF TO VOP 44 19 -2V ±.02V

R-30

U-47 U-49

DC RESTORE

ADDERS U4, 16, 15, 22

8 8 SET-UP SWITCHES S1-1, 8

8

5 CYCLE DELAY

BUFFER RAM DELAY U7, 8 U11, 12

DATA

OUTPUT LATCHES ECL OUT U2, 6, 10 U14

23 144 38 130 "Y" DATA TO DIGITAL CHASSIS

"Y" DATA

MSB

CONV. D1 U5 "Y" A/D IN D8 LSB

BUFFER U9 Q1, 2, 3

"Y" FROM C/F 14 14

"Y" GAIN FROM V.O.P. 40 17

-2V ± 1V

A0 A3

U1

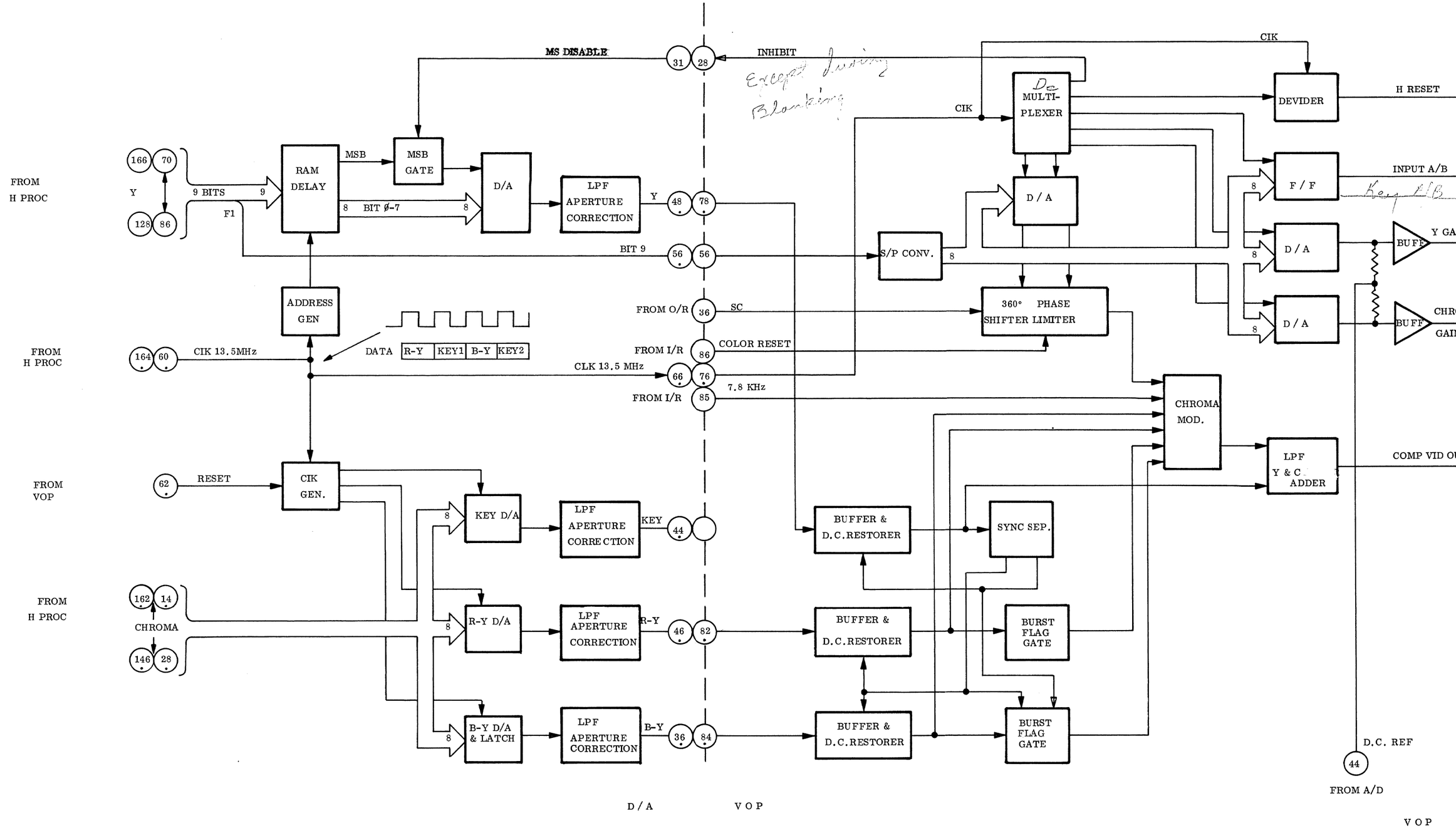
21 163 22 164 FY TO DIGITAL CHASSIS

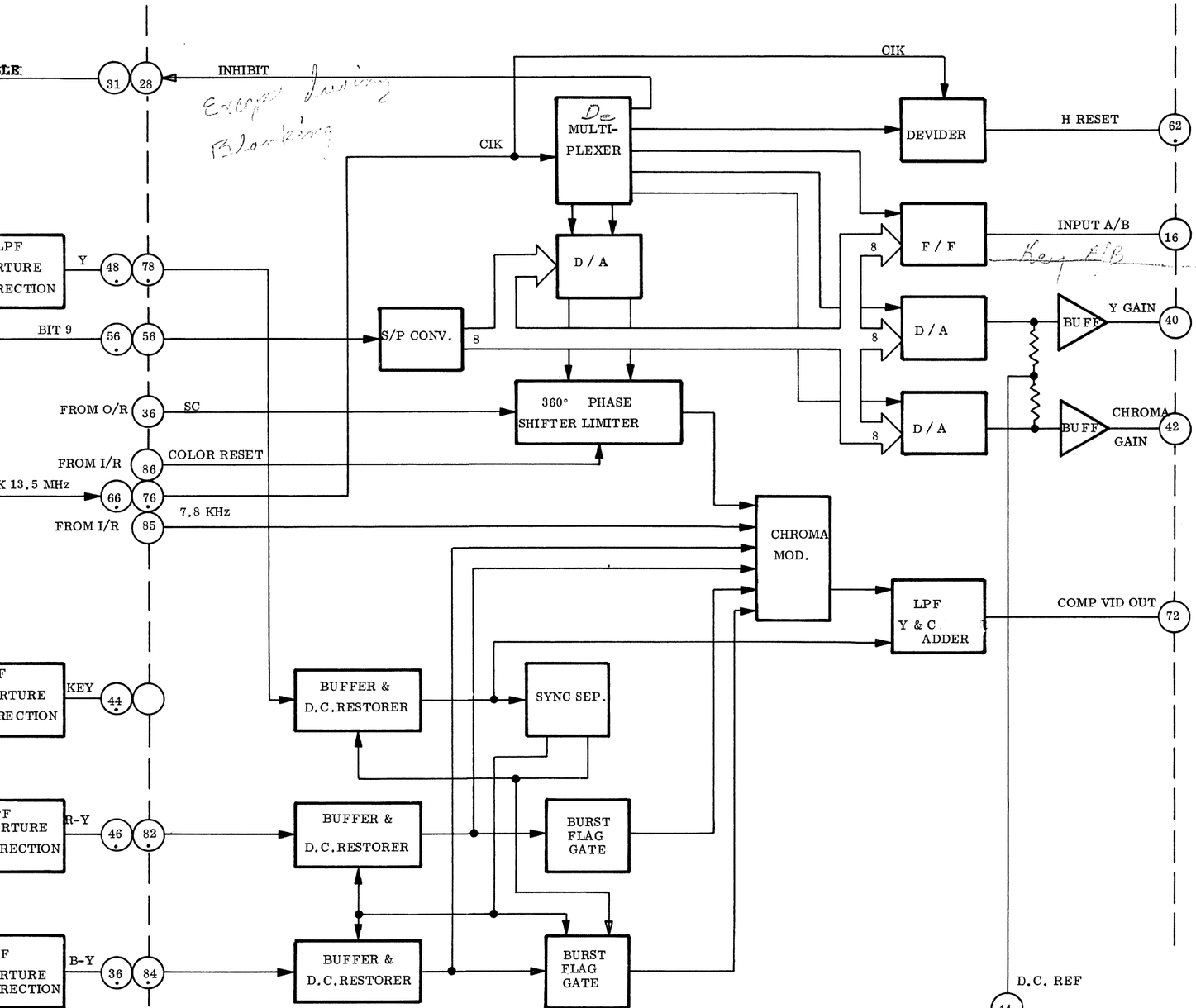
ADD. GEN U3

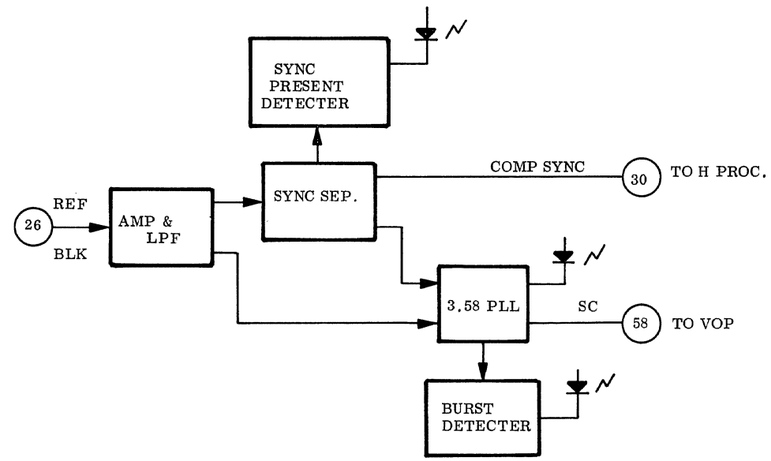
Fy

A D O
A / D P W A

3-13/14


MS DISABLE
31
28
INHIBIT
Except during Blanking
CIK
Do MULTI-PLEXER
DEVIDER
H RESET
FROM H PROC
166
70
Y
128
86
9 BITS
9
F1
RAM DELAY
MSB
MSB GATE
8 BIT Ø-7
8
D/A
LPF APERTURE CORRECTION
Y
48
78
BIT 9
56
56
S/P CONV.
8
D / A
F / F
INPUT A/B
Key A/B
Y GA
BUFF
ADDRESS GEN
FROM O/R
36
SC
360° PHASE SHIFTER LIMITER
FROM H PROC
164
60
CIK 13.5MHz
DATA
R-Y
KEY1
B-Y
KEY2
FROM I/R
86
COLOR RESET
CLK 13.5 MHz
66
76
7.8 KHz
FROM I/R
85
CHROMA MOD.
LPF Y & C ADDER
COMP VID OU
FROM VOP
62
RESET
CIK GEN.
KEY D/A
LPF APERTURE CORRECTION
KEY
44
BUFFER & D.C.RESTORER
SYNC SEP.
FROM H PROC
162
14
CHROMA
146
28
R-Y D/A
LPF APERTURE CORRECTION
R-Y
46
82
BUFFER & D.C.RESTORER
BURST FLAG GATE
B-Y D/A & LATCH
LPF APERTURE CORRECTION
B-Y
36
84
BUFFER & D.C.RESTORER
BURST FLAG GATE
D.C. REF
44
FROM A/D
D / A
V O P
V O P





A D O
ANALOG OUTPUT FLOW

3-15/16

Fy

÷ 858
U5, 10, 16, 39
6, 13, 19

LD

62 62 H RESET TO D/A

BIT 9 FROM D/A 56 56

D S/P CONV. U4
QH
QA

DATA AØ-A7

Fy FROM D/A 66 76

A4 A5 A6

START BIT DECODE
U8/U1

LATCH D/A U13/U19
15, 22
C
$\overline{C}$
TO U25 THIS PAGE

LATCH D/A U12/U18
16 23
B
$\overline{B}$
TO U24 THIS PAGE

COUNTER U2, U3, U19

INHIBIT TO D/A 31 28 SIGN BIT

CMD DECODER
U3/U9/11

30 CLK Decode

LATCH U11
14
16 28 A/B SELECT TO C/F
Z1 Key A-B switch

LATCH D/A U14/U20
24, 28
REF
40 17 Y GAIN TO A/D

-2vREF FROM A/D 19 44

-2vREF

REF
LATCH D/A U15/U21
18, 25
42 55 CHROMA GAIN TO A/D

COLOR PRESENT FROM I/R 80 86

FROM U18 THIS PAGE
B
$\overline{B}$
MOD/ DEMOD U24

SC FROM OUTPUT REF 58 36 56 32

LIMITER U23, T1

TP1

LIMITER U28 T3

90° PHASE SHIFTER L3, C121

L-3

TP2

MOD/ DEMOD U25

FROM U19 THIS PAGE
C
$\overline{C}$

R-Y FROM D/A 40 82

BUFFER D.C. RESTORE Q25, 26, U30

REF. D.C. CLAMP SMPL. HOLD

SMPL

7.8KHz FROM I/R 62 85

J1
A B

PAL PHASE INVERSION U32, Q41 Q42

B-Y FROM D/A 36 84

BUFFER D.C. RESTORE Q46, 47, U36

REF. D.C. CLAMP SMPL. HOLD U33 U34

SMPL

SYNC SEP. PULSE FORMER Q14, 15, 16 U29

CLAMP

LUMA FROM D/A 48 78

BUFFER CLAMP Q50, 51, U37

R-21

7 - situp

62 62 H RESET TO D/A

C TO U25 THIS PAGE

$\overline{C}$

B TO U24 THIS PAGE

$\overline{B}$

16 28 A/B SELECT TO C/F

Z1 Key A-B switch

40 17 Y GAIN TO A/D

42 55 CHROMA GAIN TO A/D

COLOR PRESENT FROM I/R 80 86

SC FROM OUTPUT REF 58 36, 56 32

LIMITER U23, T1

FROM U18 THIS PAGE B, $\overline{B}$

MOD/ DEMOD U24

LIMITER U28 T3

TP1

90° PHASE SHIFTER L3, C121

L-3

TP2

MOD/ DEMOD U25

FROM U19 THIS PAGE C, $\overline{C}$

R-Y FROM D/A 40 82

BUFFER D.C. RESTORE Q25, 26, U30

SMPL

REF. D.C. CLAMP SMPL. HOLD

+12y 87 R-235 R-Y BALANCE -12x

Quad 9 L-4

90° PHASE SHIFTER L4, C76 C101

R-Y MOD. U31

white Bal

7.8KHz FROM I/R 62 85

J1 A B

PAL PHASE INVERSION U32, Q41 Q42

B-Y MOD. U35

Q62 Q63

B-Y FROM D/A 36 84

BUFFER D.C. RESTORE Q46, 47, U36

SMPL

REF. D.C. CLAMP SMPL. HOLD U33 U34

+12V 121 R-237 B-Y BALANCE -12V

SYNC SEP. PULSE FORMER Q14, 15, 16 U29

CLAMP

LUMA FROM D/A 48 78

BUFFER CLAMP Q50, 51, U37

R-81

Y - drive

Y - Quad

R-239 109

106 R-238

CHROMA LEVEL

LOW PASS FILTER AMP. Q43, 44, 45 L5 Q53-58

72 COMP OUT 1

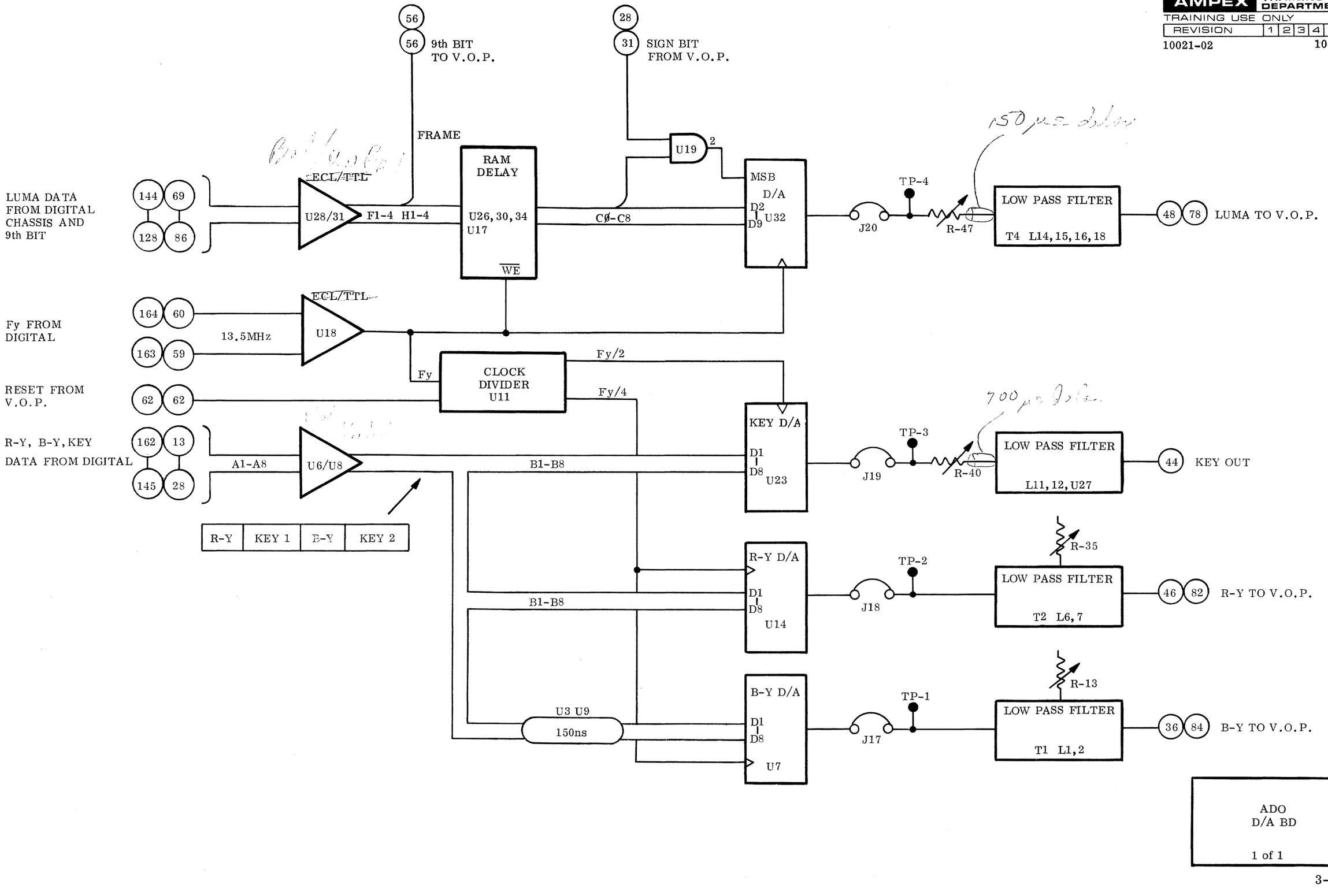
68 COMP OUT 2

TO BACK PNL

ADO
VIDEO OUTPUT PWA

1 of 1

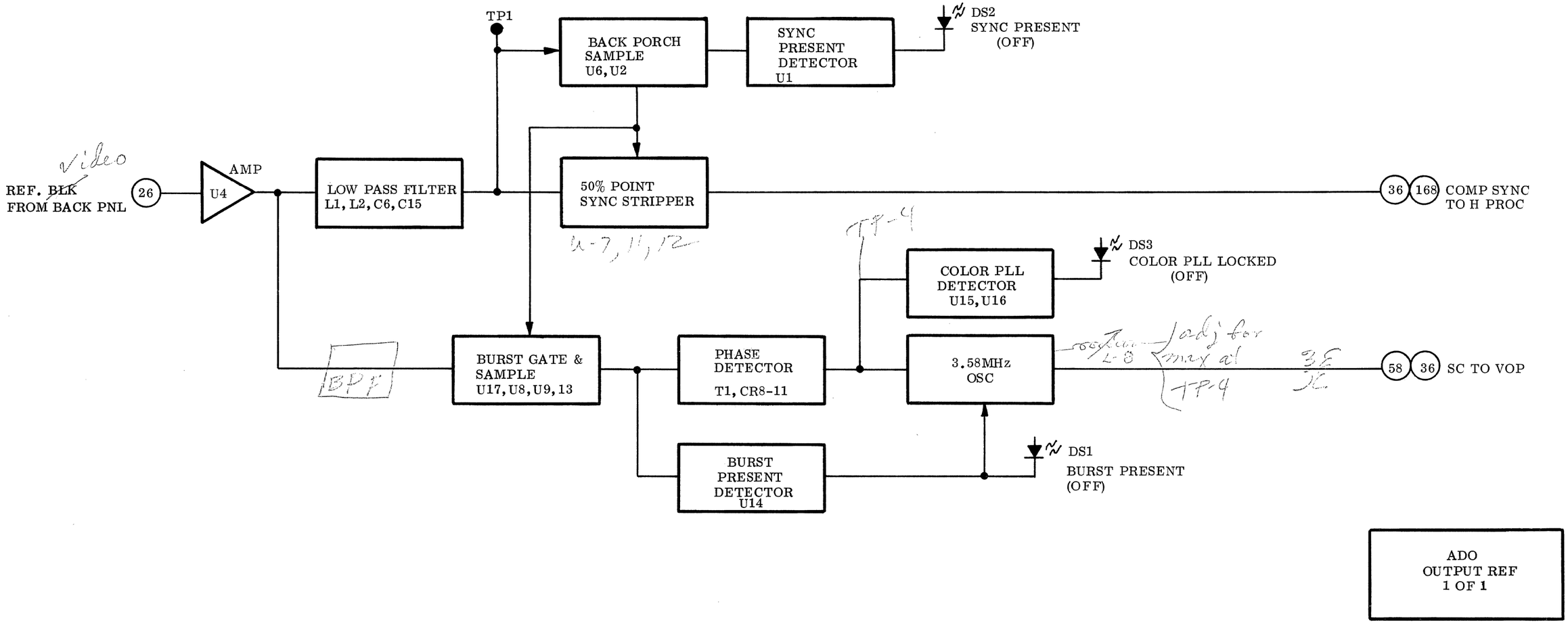
3-17/18



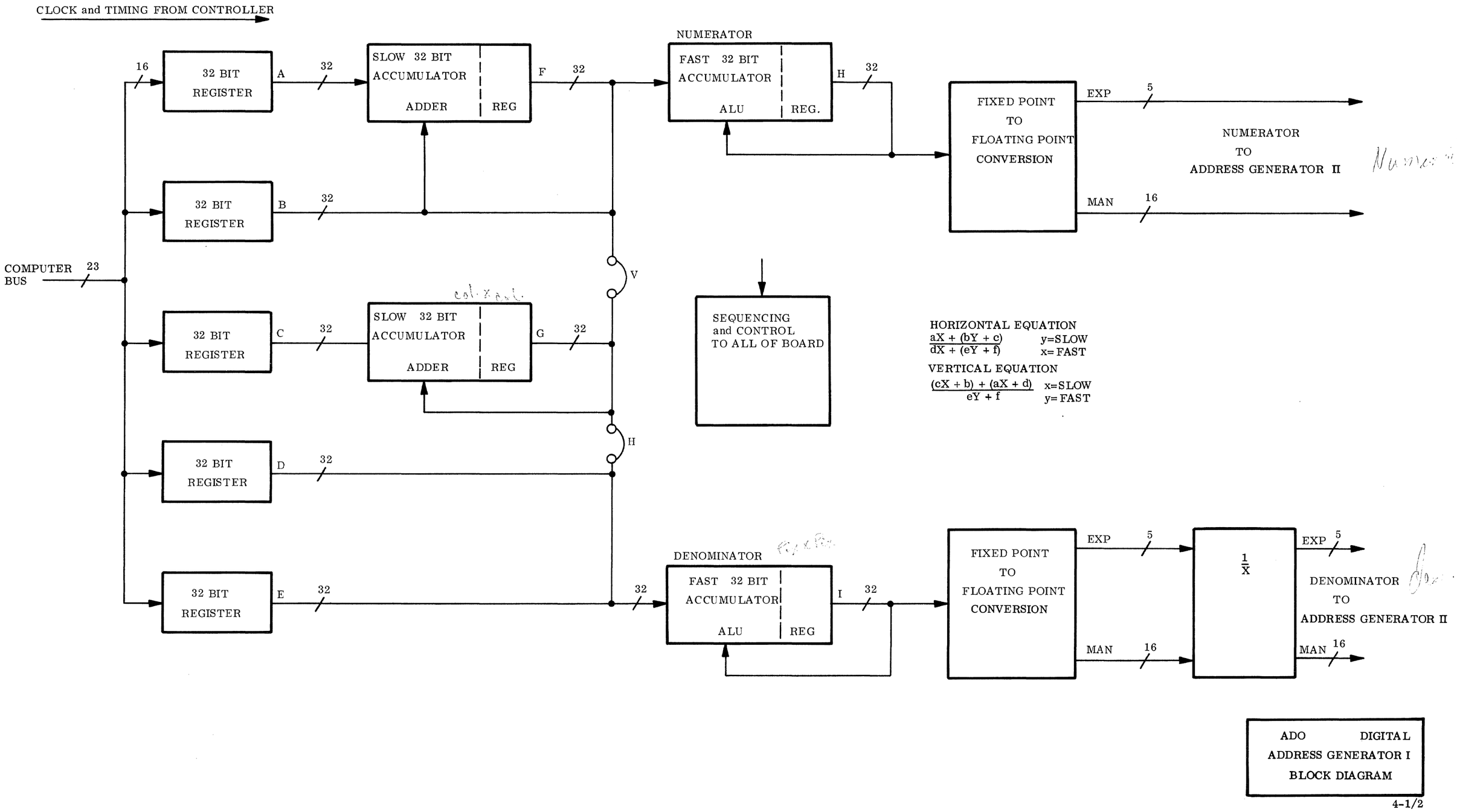
ADO
D/A BD

1 of 1

3-19/20



ADO
OUTPUT REF
1 OF 1



HORIZONTAL EQUATION

$$\frac{aX + (bY + c)}{dX + (eY + f)}$$

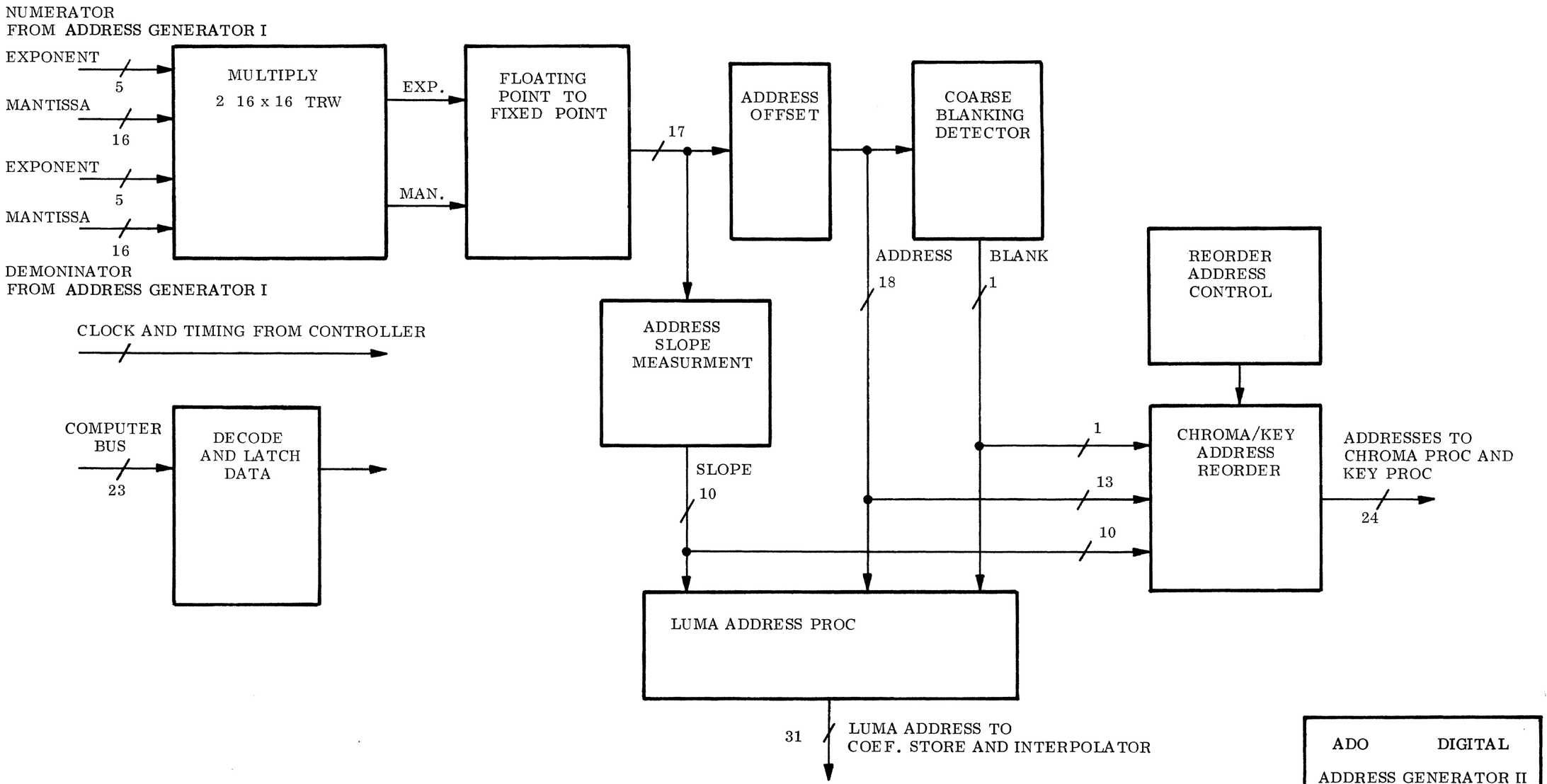
y=SLOW
x= FAST

VERTICAL EQUATION

$$\frac{(cX + b) + (aX + d)}{eY + f}$$

x=SLOW
y= FAST

ADO DIGITAL
ADDRESS GENERATOR I
BLOCK DIAGRAM



ADO DIGITAL

ADDRESS GENERATOR II
BLOCK DIAGRAM

ADO ADDRESS GENERATOR Fig 9

10021 XX-008

O* C* AA* W* } OUTPUT OF ADDRESS GENERATOR I GOES TO ADDRESS GENERATOR II

CHECKS LEADING ZERO'S

CD

SLOW ACCUMULATOR

NUMERATOR

NUMERATOR EXPONENT

F.P. CONVERT

F.P. → LINEAR CONVERT

BLOCK NORMALISE

MULT. MANTISSAE

FAST ACCU.

SLOW ACCU.

FAST ACCU.

DENOMINATOR

DENOMINATOR MANTISSA

DENOMINATOR EXPONENT

INVERTER

ADDRESS

Q ADD FROM LLC (TARGET ADDRESS)

OFFSET

ADDRESS SLOPE

CHROMA SLOPE

COARSE BLANK

SN SH4 - IR SH5

ROTATE 3 COEFFS — COEFF. STORE

PHASE 3L COEFFS — COEFF. STORE

BLOCK OFFSET RAM — INTERPOLATOR ADDERS. (CARRY)

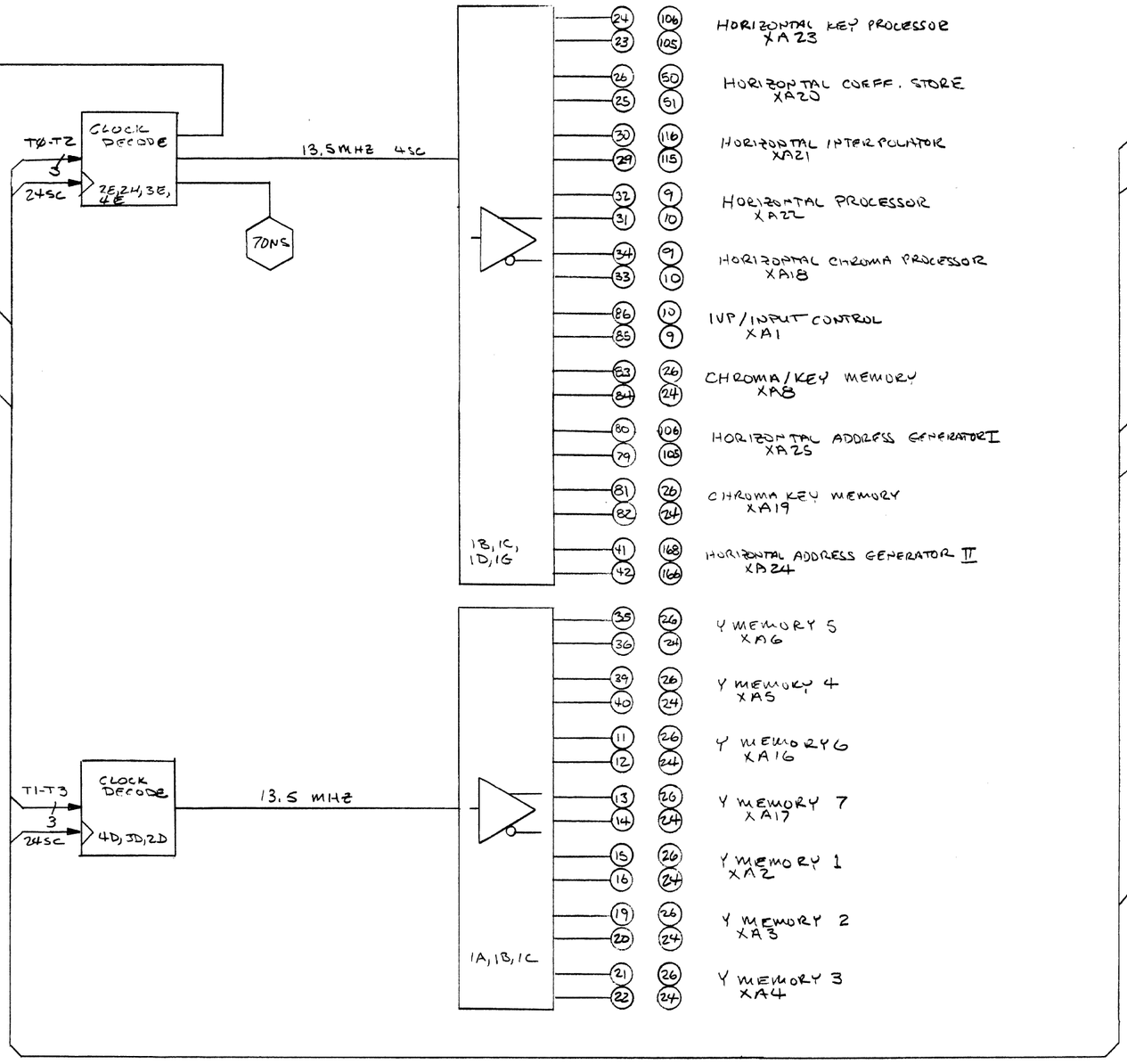
FILTER ADD. SOURCE ADDRESS TO RAM — INTERPOLATOR BASE ADDRESS

MAG FACTOR — COEFF. STORE

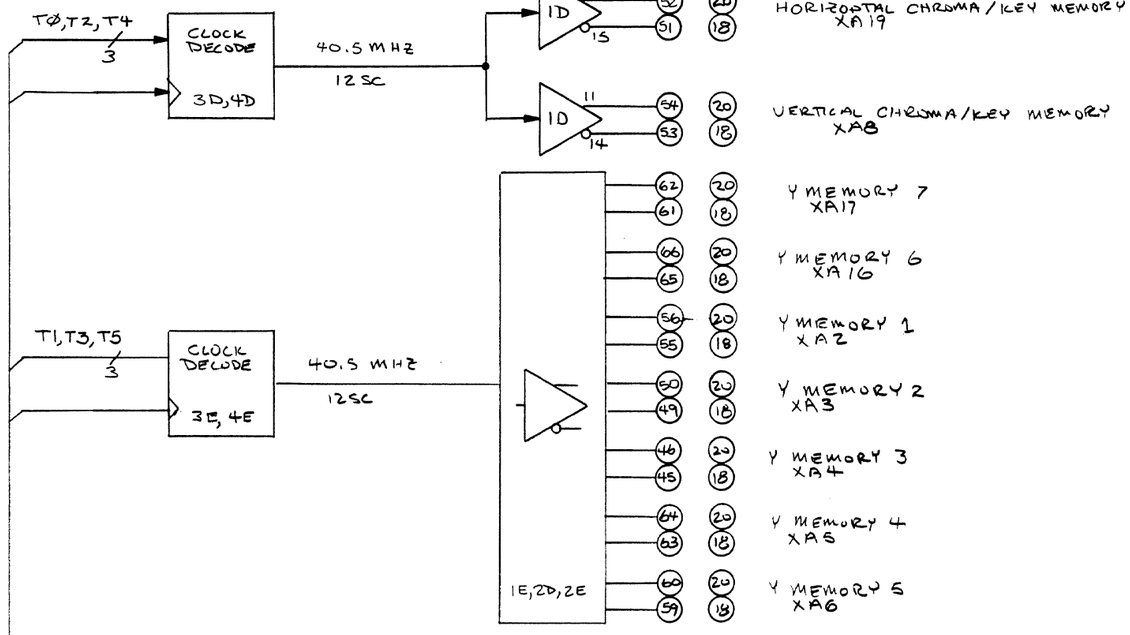
4 - 5/6

XX-008C

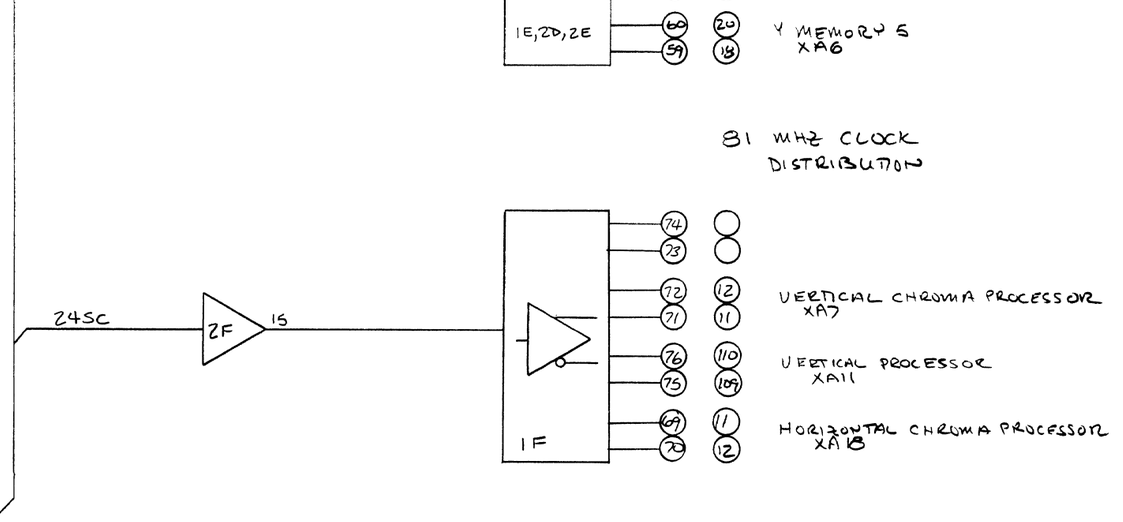
13.5 MHZ CLOCK DISTRIBUTION



40.5MHZ CLOCK DISTRIBUTION

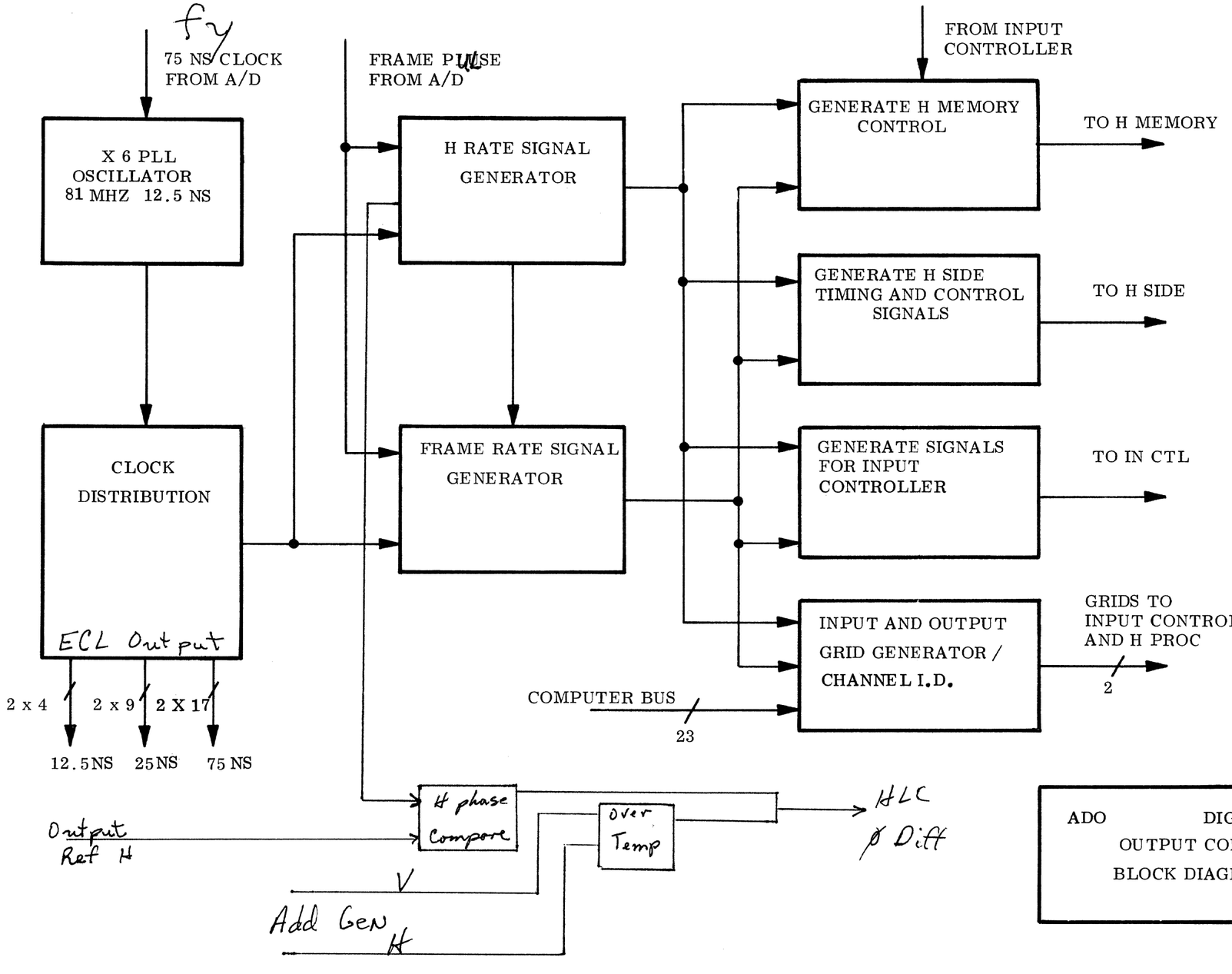


81 MHZ CLOCK DISTRIBUTION



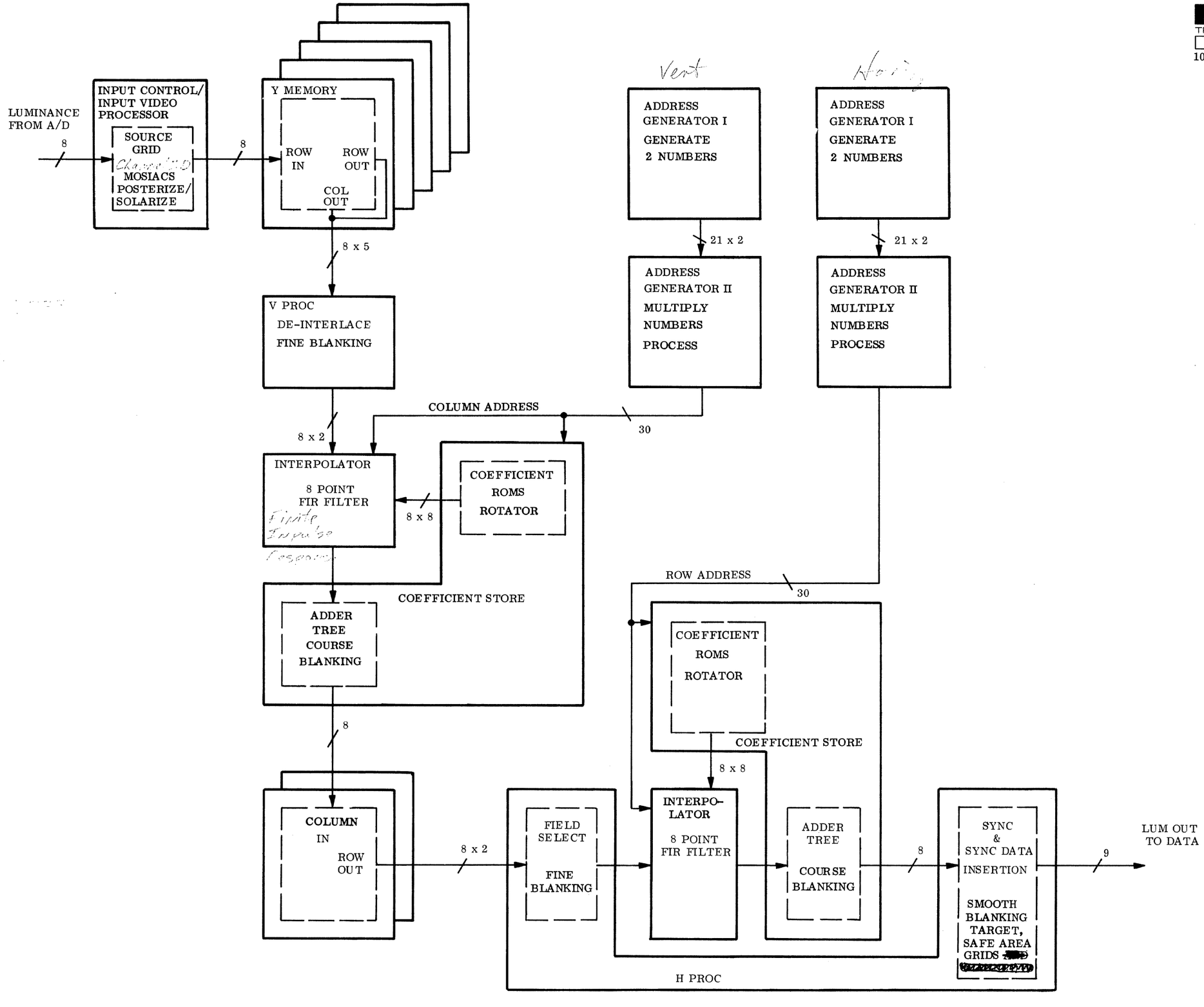
ADO DIGITAL OUTPUT CONTROL CLOCK DISTRIBUTION

4-7/8



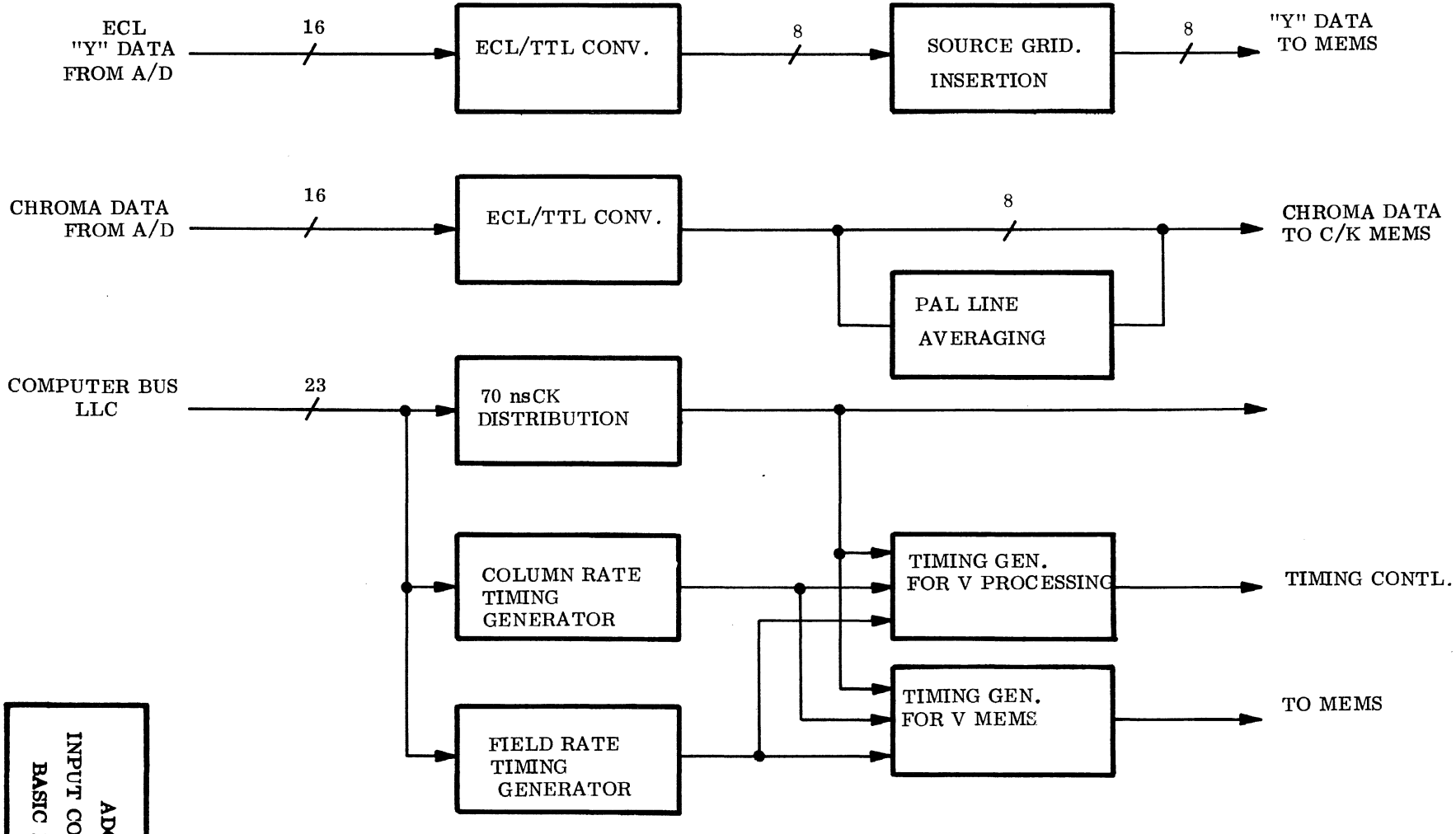
ADO DIGITAL
OUTPUT CONTROL
BLOCK DIAGRAM

4-9/10

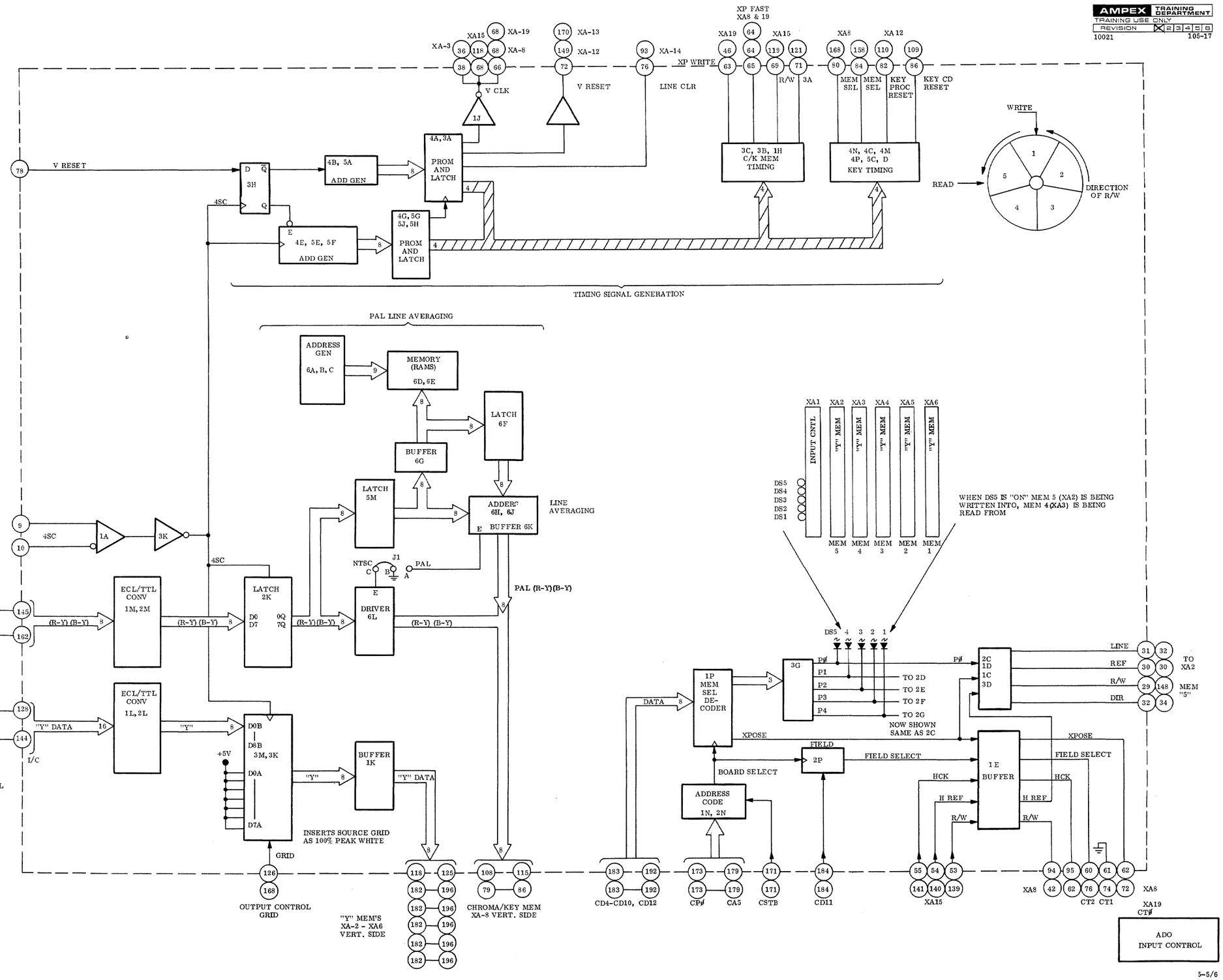


ADO LUMINANCE
DIGITAL SIGNAL FLOW

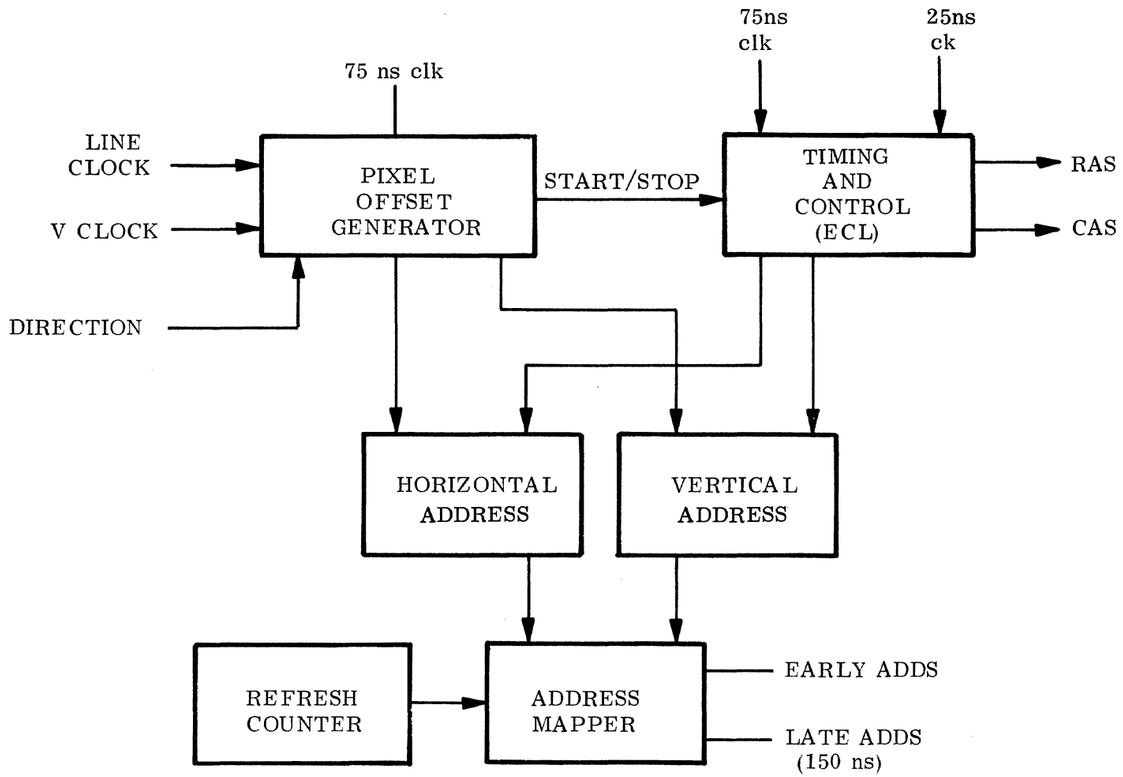
5-1/2



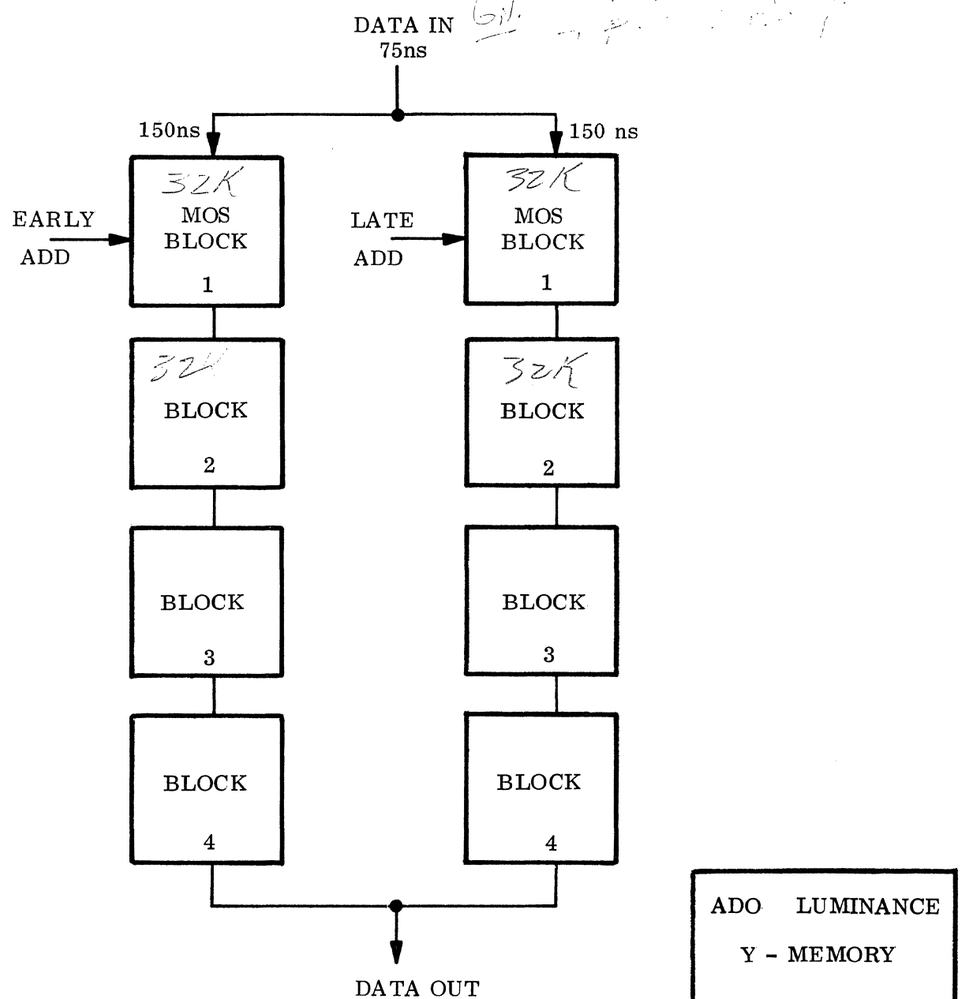
ADO
INPUT CONTROL
BASIC FLOW


XP FAST
XA8 & 19
XA-3
XA15
XA-19
XA-8
XA-13
XA-12
XA-14
XP WRITE
XA19
XA15
XA8
XA12
V CLK
V RESET
LINE CLR
R/W
3A
MEM SEL
MEM SEL
KEY PROC RESET
KEY CD RESET
WRITE
READ
DIRECTION OF R/W
78
V RESET
3H
4SC
4B, 5A
ADD GEN
4A, 3A
PROM AND LATCH
3C, 3B, 1H
C/K MEM TIMING
4N, 4C, 4M
4P, 5C, D
KEY TIMING
4E, 5E, 5F
ADD GEN
4G, 5G
5J, 5H
PROM AND LATCH
TIMING SIGNAL GENERATION
PAL LINE AVERAGING
ADDRESS GEN
6A, B, C
MEMORY (RAMS)
6D, 6E
BUFFER 6G
LATCH 6F
LATCH 5M
ADDER 6H, 6J
BUFFER 6K
LINE AVERAGING
NTSC
PAL
J1
PAL (R-Y)(B-Y)
DRIVER 6L
LATCH 2K
ECL/TTL CONV 1M, 2M
ECL/TTL CONV 1L, 2L
MULTIPLEXED (R-Y) (B-Y) ECL
ECL "Y" DATA TO INPUT CNTL. BD.
A/D
I/C
J5
J6
RIBBON CONNECTOR ON BACK PANEL OF SYSTEM
(R-Y) (B-Y)
"Y" DATA
"Y"
"Y" DATA
+5V
D0B
D8B
3M, 3K
D0A
D7A
INSERTS SOURCE GRID AS 100% PEAK WHITE
GRID
OUTPUT CONTROL GRID
"Y" MEM'S XA-2 - XA6 VERT. SIDE
CHROMA/KEY MEM XA-8 VERT. SIDE
XA1
XA2
XA3
XA4
XA5
XA6
INPUT CNTL
"Y" MEM
DS5
DS4
DS3
DS2
DS1
MEM 5
MEM 4
MEM 3
MEM 2
MEM 1
WHEN DS5 IS "ON" MEM 5 (XA2) IS BEING WRITTEN INTO, MEM 4 (XA3) IS BEING READ FROM
1P MEM SEL DE-CODER
DATA
3G
TO 2D
TO 2E
TO 2F
TO 2G
NOW SHOWN SAME AS 2C
2C
1D
1C
3D
LINE
REF
R/W
DIR
TO XA2
MEM "5"
XPOSE
FIELD
2P
FIELD SELECT
BOARD SELECT
ADDRESS CODE 1N, 2N
1E BUFFER
HCK
H REF
R/W
CD4-CD10, CD12
CP∅
CA5
CSTB
CD11
XA15
XA8
CT2 CT1
XA19 CT∅
ADO INPUT CONTROL

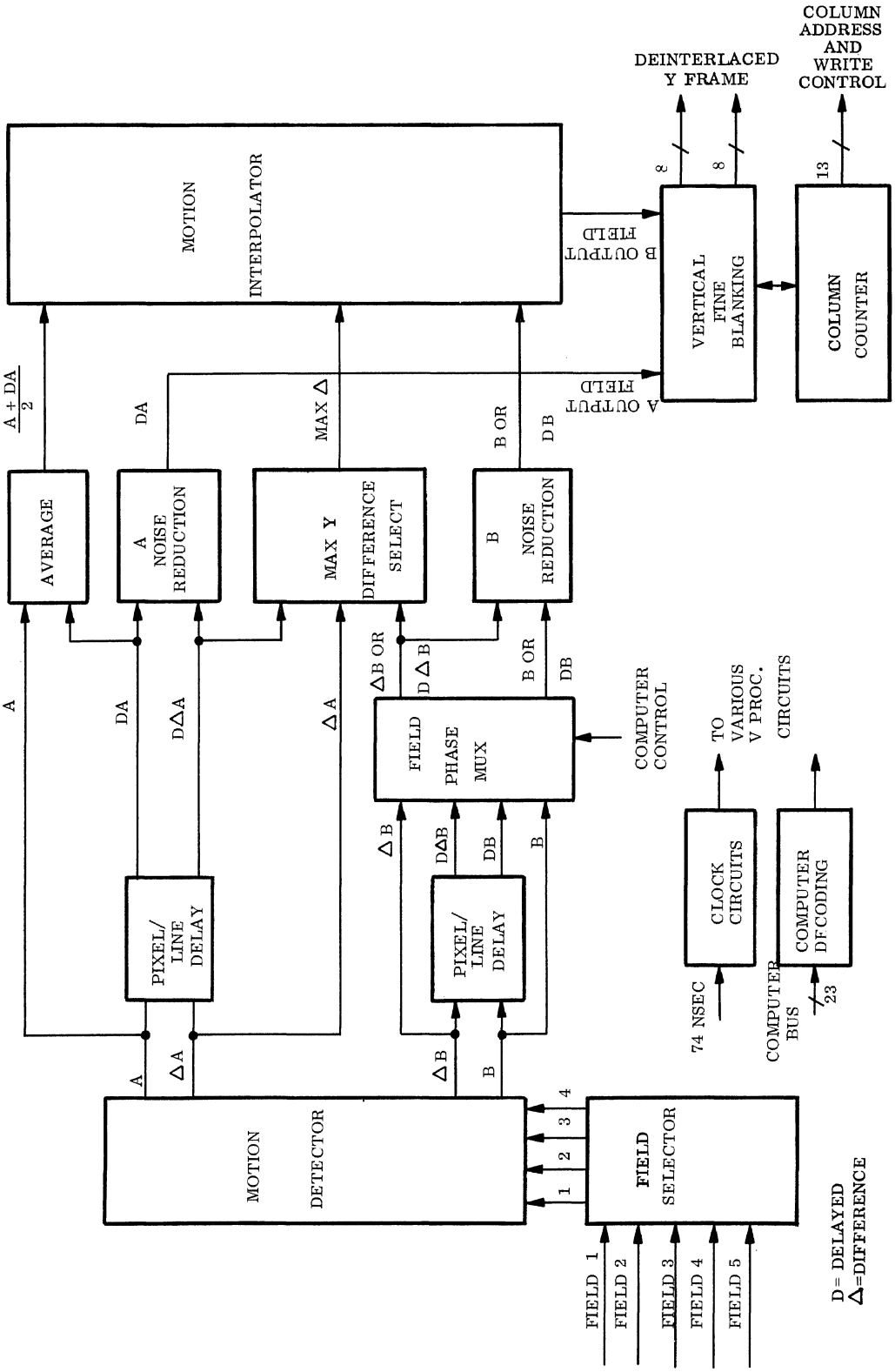
5-5/6



1. MOS BLOCKS cycle at 600 ns.
2. Multiplex of each block in chain gives 150 ns data
3. Each block consists of 32 k Bytes or 16 x MK 4116 RAMs.
4. Test point to disable early or late block at rear of card
5. Card disable button at front of card.



ADO LUMINANCE
Y - MEMORY



A D O
V. PROC
BASIC FLOW

"Y" DATA IN

FROM MEM 5 XA-2 — 152, 10, 166, 90 — MAØ-7 — 8
FROM MEM 4 XA-3 — 152, 9, 166, 88 — MBØ-7 — 8
FROM MEM 3 XA-4 — 152, 16, 166, 96 — MCØ-7 — 8
FROM MEM 2 XA-5 — 152, 14, 166, 94 — MDØ-7 — 8
FROM MEM 1 XA-6 — 152, 12, 166, 92 — MEØ-7 — 8

FIELD SELECT
1A, B, C, D
1E, F, G, H
2A, E, C, G

MOST CURRENT FIELD

AAØ-7 (A)
ABØ-7 (B)
ACØ-7 (C)
ADØ-7 (D)

LATCH
2B, D, F, H

BAØ-7 (A)
BBØ-7 (B)
BCØ-7 (C)
BDØ-7 (D)

MOTION DETECT
3A, C, D
A-C= Δ A

MOTION DETECT
3E, G, H
B-D= Δ B

A-C DIFF. 8
B-D DIFF. 8

PROM & LATCH
4A, C
5A

PROM & LATCH
4G, E
5E

LATCH
3F, 4F

LATCH
3F, 4F

CK2

RAM DELAY
10A-H

RAM DELAY
9A. B 8A, B, C

RAM DELAY
8D-8J

RAM DELAY
10J 9C-J

CAØ-7 (A) → DAØ-7 (DA) → LATCH 10N → EAØ-7 (DA) → LATCH 10P → FDAØ-7 (DA)

(A) → 10M → FAØ-7 (A)

CCØ-5 (ΔA) → DCØ-5 (DΔA) → LATCH 7G → ECØ-5 (DΔA) → LATCH 7F → FDCØ-5 (DΔA)

(ΔA) → LATCH 6A → FCØ-5 (ΔA)

CDØ-5 (ΔB) → DDØ-5 (DΔB) → LATCH 5B → EDØ-5 (DΔB) → MUX 5C, 5D SEL → FDØ-5

SELECT B ON ODD FIELD
DΔB ON EVEN FIELD

(ΔB)

(B)

CBØ-7 (B) → DBØ-7 (DB) → 9N LATCH → EBØ-7 (DB) → MUX 8N, 9M SEL → FBØ-7

SELECT B ON ODD FIELD
DB ON EVEN FIELD

EFLD "I" ON EVEN FIELD
"O" ON ODD FIELD

ISØ IS1 IS2 IS3

FIELD SELECT PROM 3M

HFLD

EFLD

CK2

COMMAND LATCHES
3N

FRC MOT
FRC STILL
NR DIS
XPOSE

RSEL

JØ-J15

TO PAGE 2

DATA FROM L.L.C. CDØ — CD15 — 196, 196, 180, 180

ADDRESS FROM L.L.C. CAØ — CA5 — 179, 179, 173, 173

ADDRESS DECODER
1R, S

Y5
Y6
Y7

4SC 70ns
24SC 12ns

CLOCK DISTRIBUTE
2K, 3K, 3J

4SC
24SC

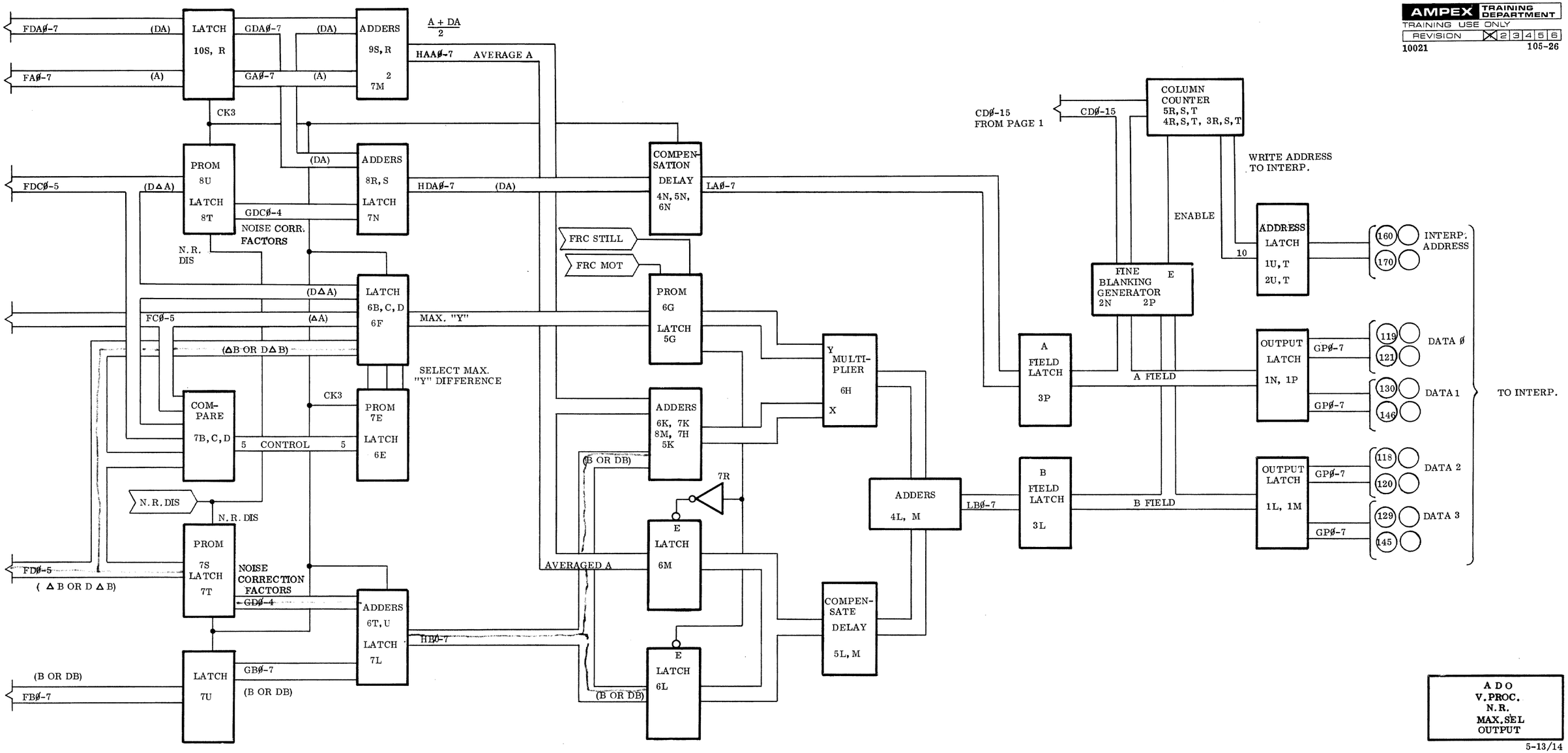
RAM CONTROL
3J, 4J

WEØ
WE1
WE2
CK8

CK3
CK2
CK1
CKØ

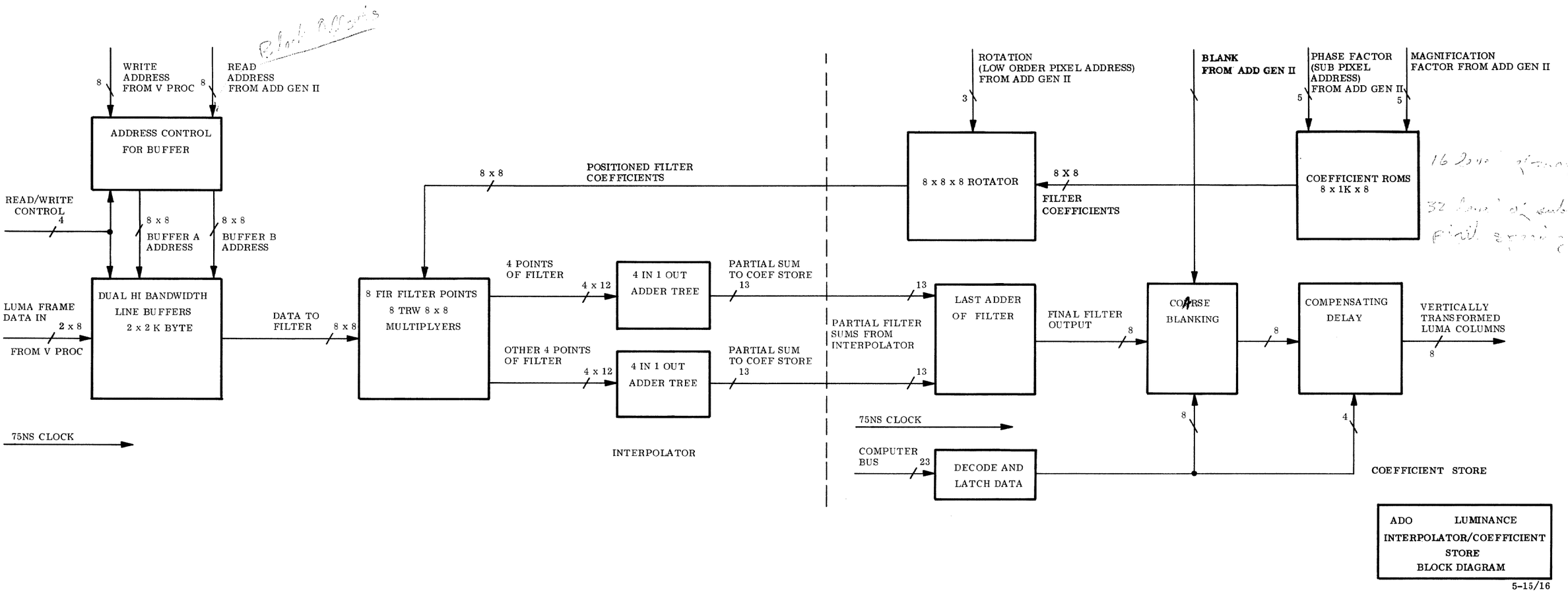
A D O
V. PROC
FIELD SELECT
MOTION DETECT
PHASE MUX

5-11/12



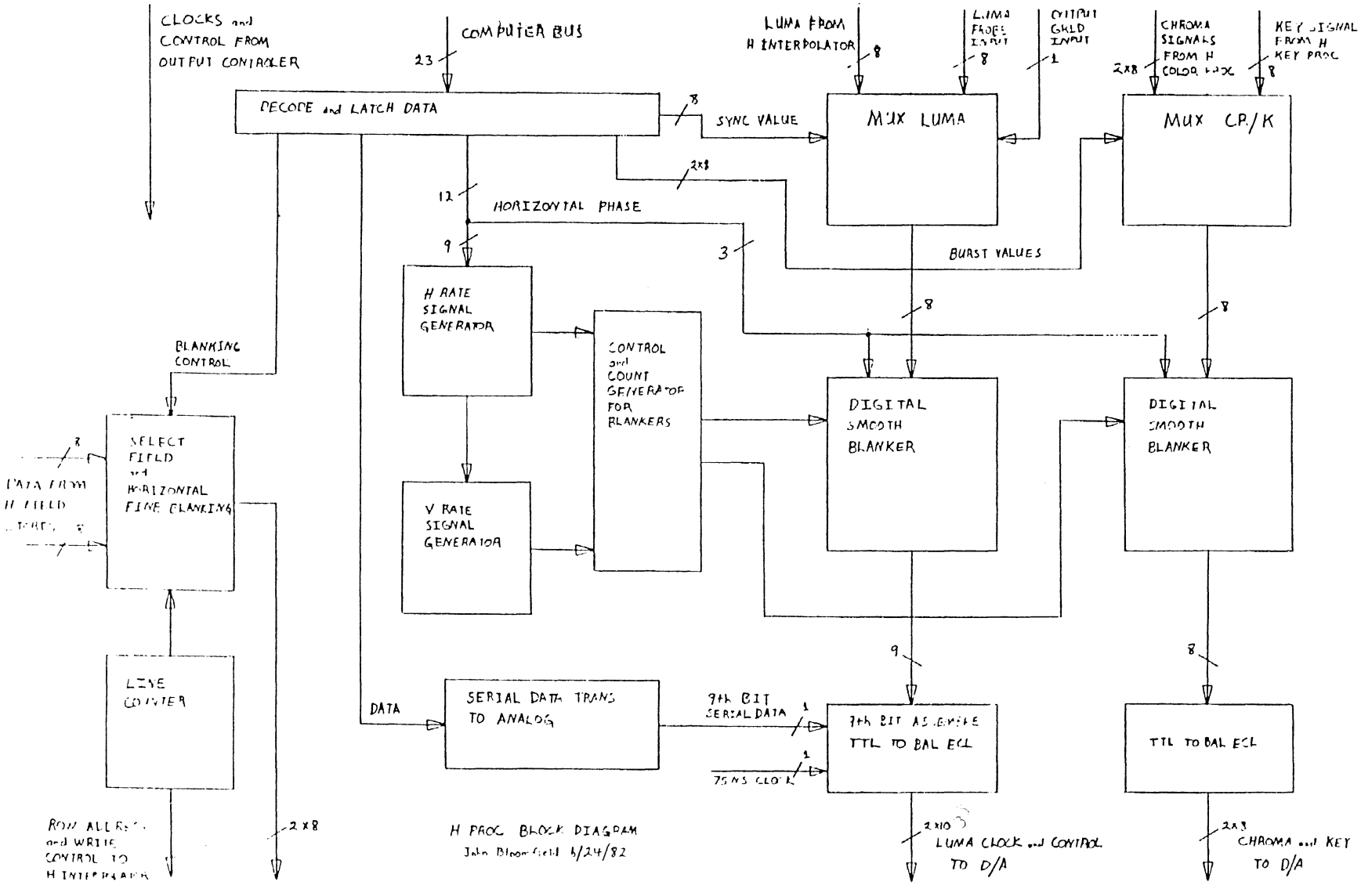
A D O
V. PROC.
N.R.
MAX. SEL
OUTPUT

5-13/14

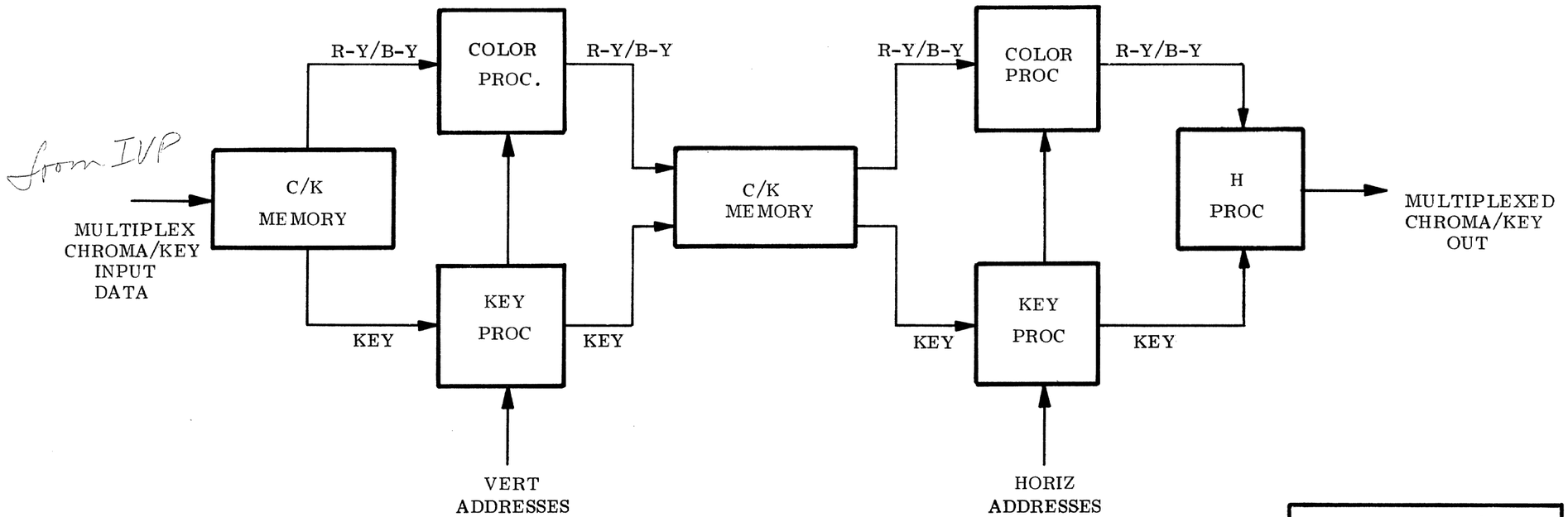


ADO LUMINANCE INTERPOLATOR/COEFFICIENT STORE BLOCK DIAGRAM

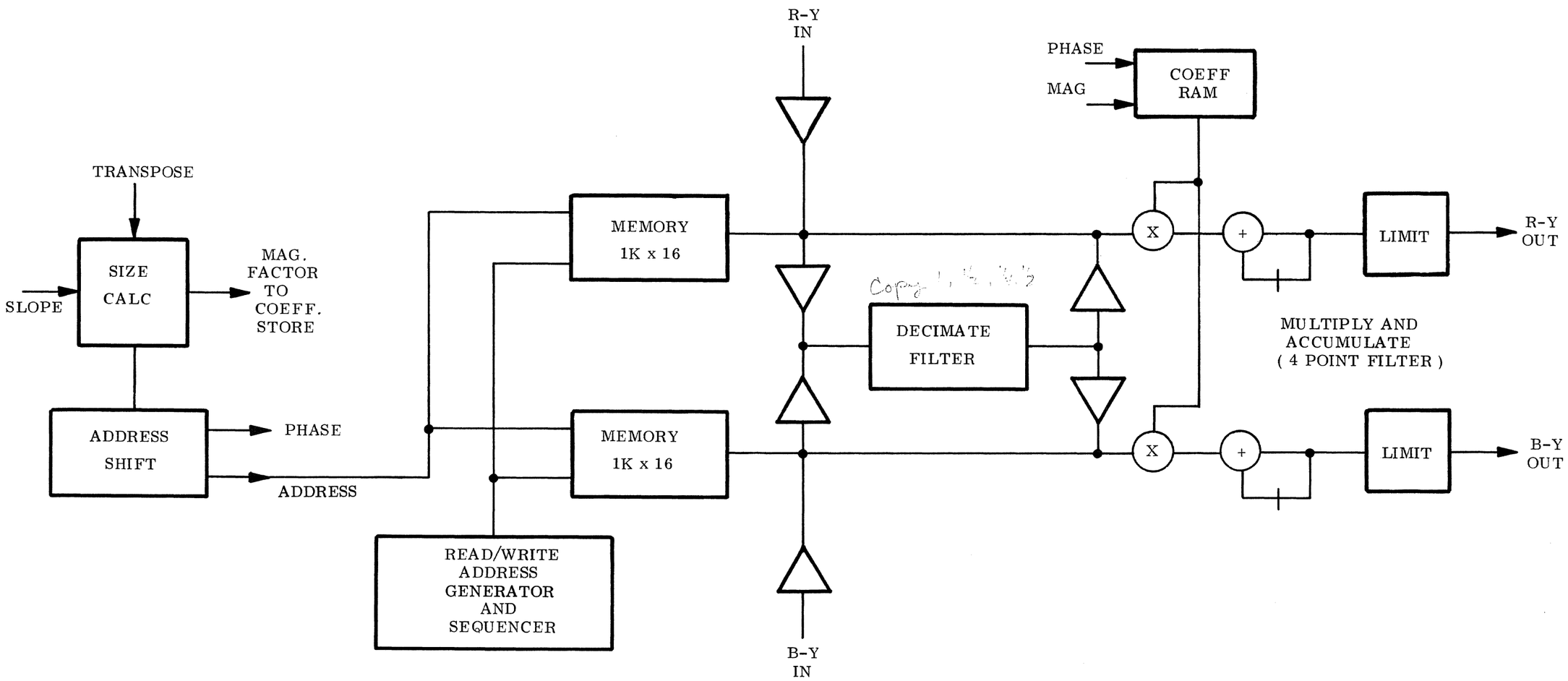
5-15/16



H PROC BLOCK DIAGRAM
John Bloomfield 6/24/82



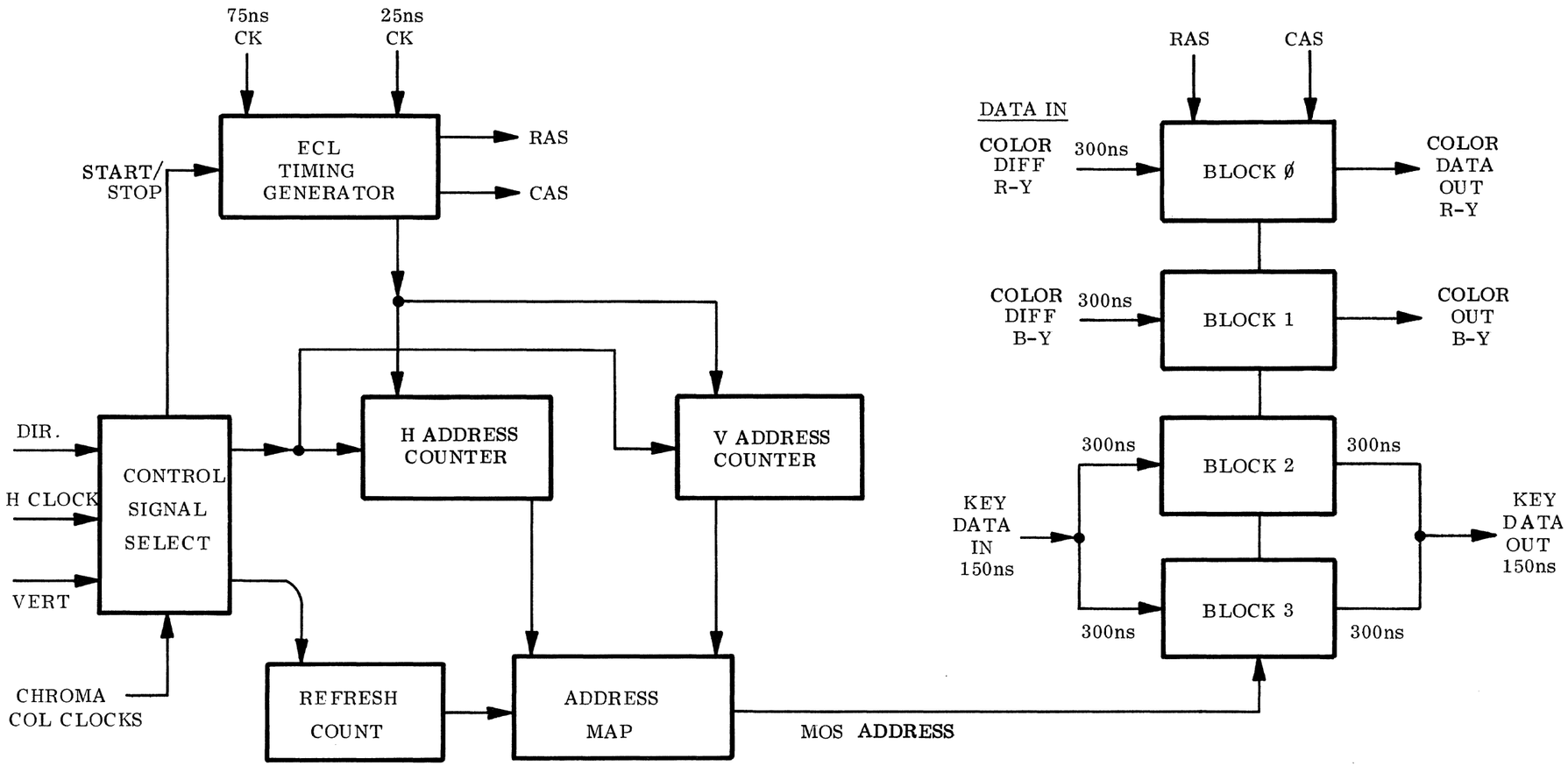
ADO CHROMA/KEY CHROMA AND KEY PROCESSING SYSTEM



ADO CHROMA/KEY

COLOR PROCESSOR

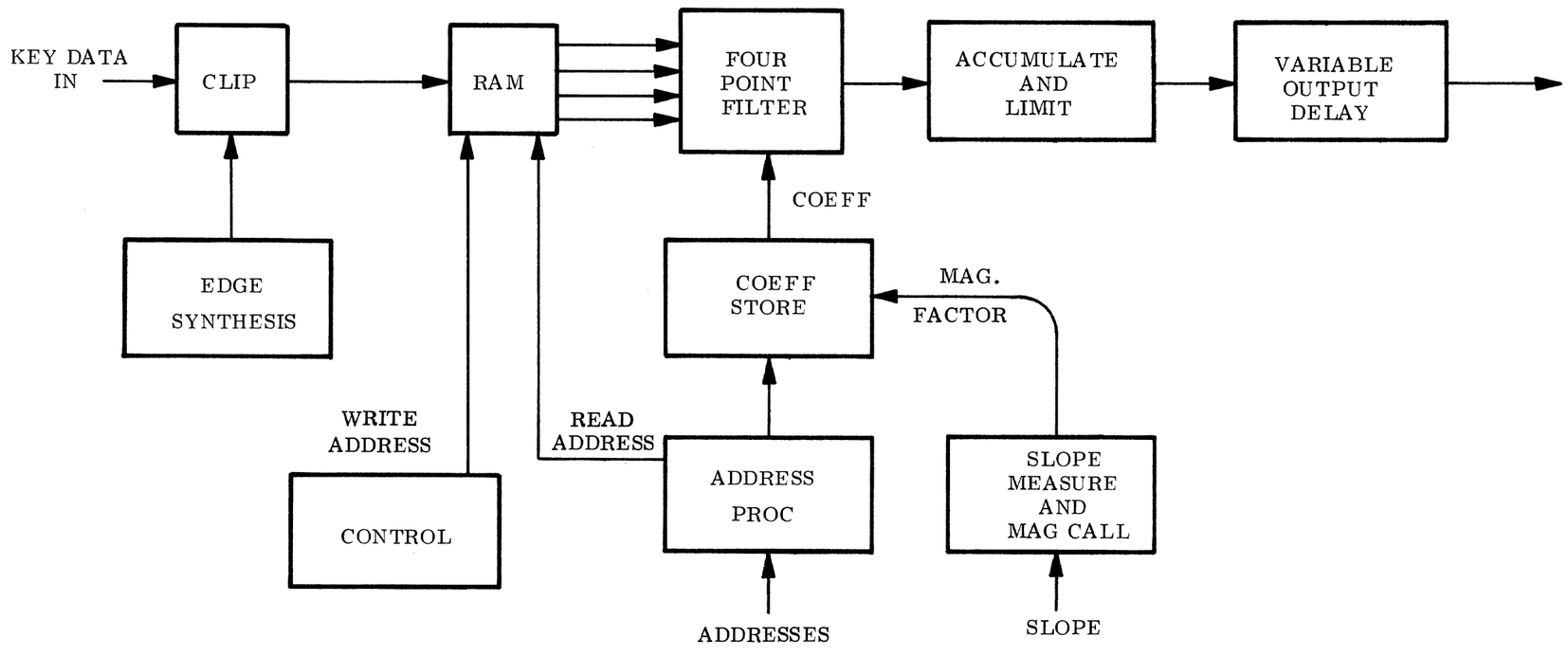
(One Side Shown. - Card has two identical sections)



1. All DATA paths eight bits. The card has four separate eight bit memories
2. Each block is 64 k Bytes (8 x MK 4164 Dynamic RAMs)

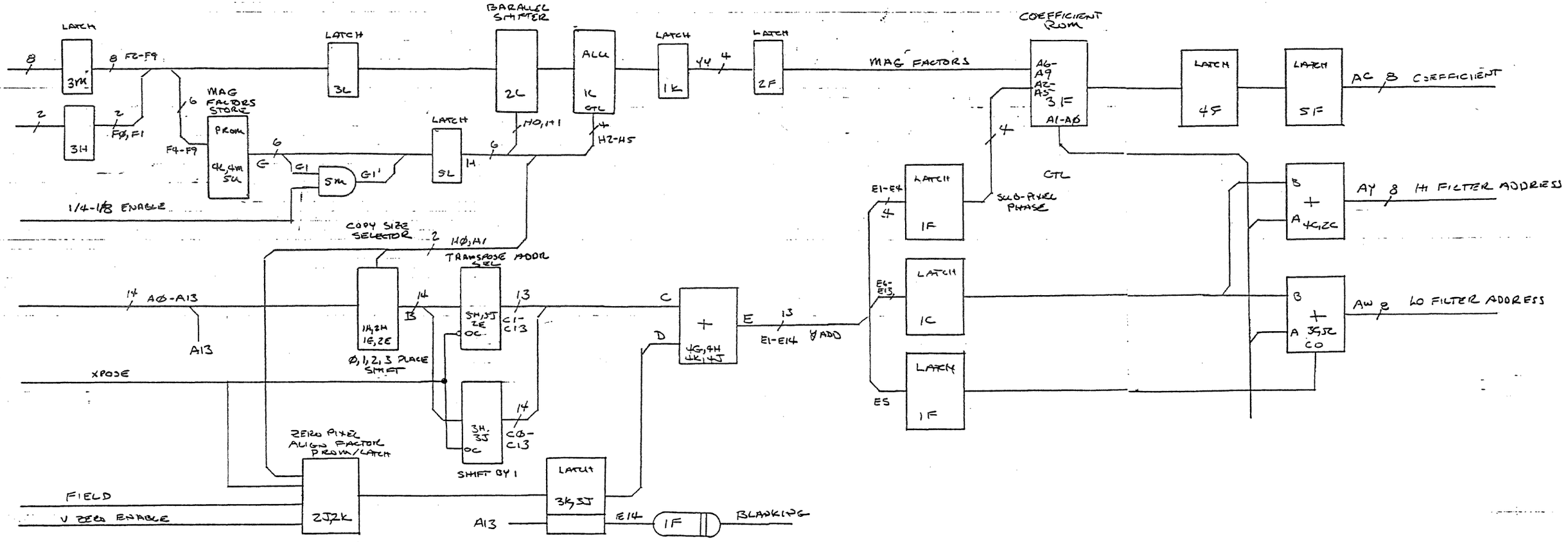
ADO CHROMA/KEY

CHROMA AND KEY MEMORY



ADO CHROMA/KEY

KEY PROCESSOR


LATCH
3M
8
8 F2-F9
3H
2
2
FØ, F1
MAG FACTORS STORE
PROM
4K, 4M SW
F4-F9
6
G
G1
5M
G1'
1/4-1/8 ENABLE
LATCH
3L
LATCH
5L
H
6
PARALLEL SHIFTER
2L
HØ, H1
ALU
1K
CTL
4
H2-H5
LATCH
1K
44
4
LATCH
2F
MAG FACTORS
COEFFICIENT ROM
A6-A9 A2-A5
3 1F
A1-A6
4
CTL
SUB-PIXEL PHASE
LATCH
4F
LATCH
5F
AC 8 COEFFICIENT
COPY SIZE SELECTOR
2
HØ, H1
TRANSPOSE MODE SEL
14
AØ-A13
A13
XPOSE
1H, 2H 1G, 2E
B
14
SH, 5J 2E OC
C1-C13
Ø, 1, 2, 3 PLACE SHIFT
3H, 5J OC
SHIFT BY 1
14
CØ-C13
C
D
+
4G, 4H 1K, 4J
E
13
E1-E14
Y ADD
ZERO PIXEL ALIGN FACTOR PROM/LATCH
2J, 2K
FIELD
V ZERO ENABLE
LATCH
3K, 5J
A13
E14
1F
BLANKING
E1-E4
4
LATCH
1F
E6-E13
LATCH
1C
E5
LATCH
1F
B
+
A 4K, 2C
AY 8 HI FILTER ADDRESS
B
+
A 3G, 2E
CO
AW 8 LO FILTER ADDRESS

COLOR PRINT

LO DATA

I

FINE BLANK DATA

10R

BLUE BORDER

10P

RED BORDER

10K

10L

8 L

COMPUTER DATA IN

188

196

9

AG

J7

L7

8

10J, 10H

8J

INNER TERM ADDER

9

O

X3 MULTPCIER

A

B

B1

+5V

10G, 10F

10E

10

R

LATCH

10D, 10C

T

ADDER/ ROUNDING

10

12

9B, 9C

10B

8

LATCH

8H

K

8

DATA

INTERPOLATED

J

I

J

I7

M7

8

8

9

N

XS MULTPCIER

A

B

B2

B1

+5V

9G, 9F, 9E

12

P

LATCH

9D

10, C

S

12

10M

BLUE BORDER

9K

M 7

10N

RED BORDER

8K

OUTER TRK ADDER

DATA EDGE ADDRESS

ADDRESS COMPARITORS

J

HI DATA

9

3U

4U

ALB

3T, 3S

AGB

4T, 4S

1

1

9

9

9

4R

OC

FINE BLANK SWITCH CMD

AG 8

COMPUTER DATA

CC 9

INPUT WRITE ADDR

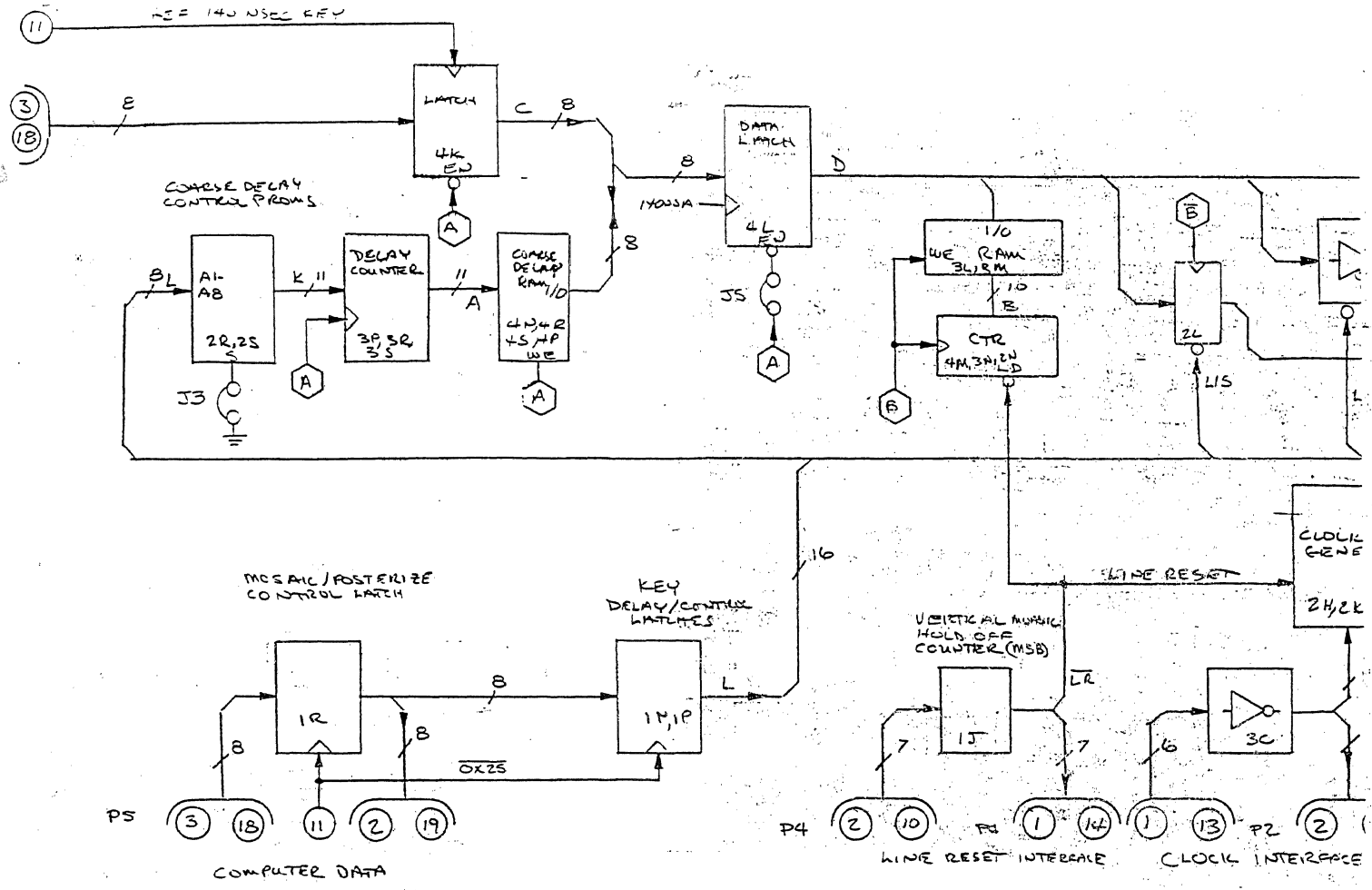
DECIMATOR

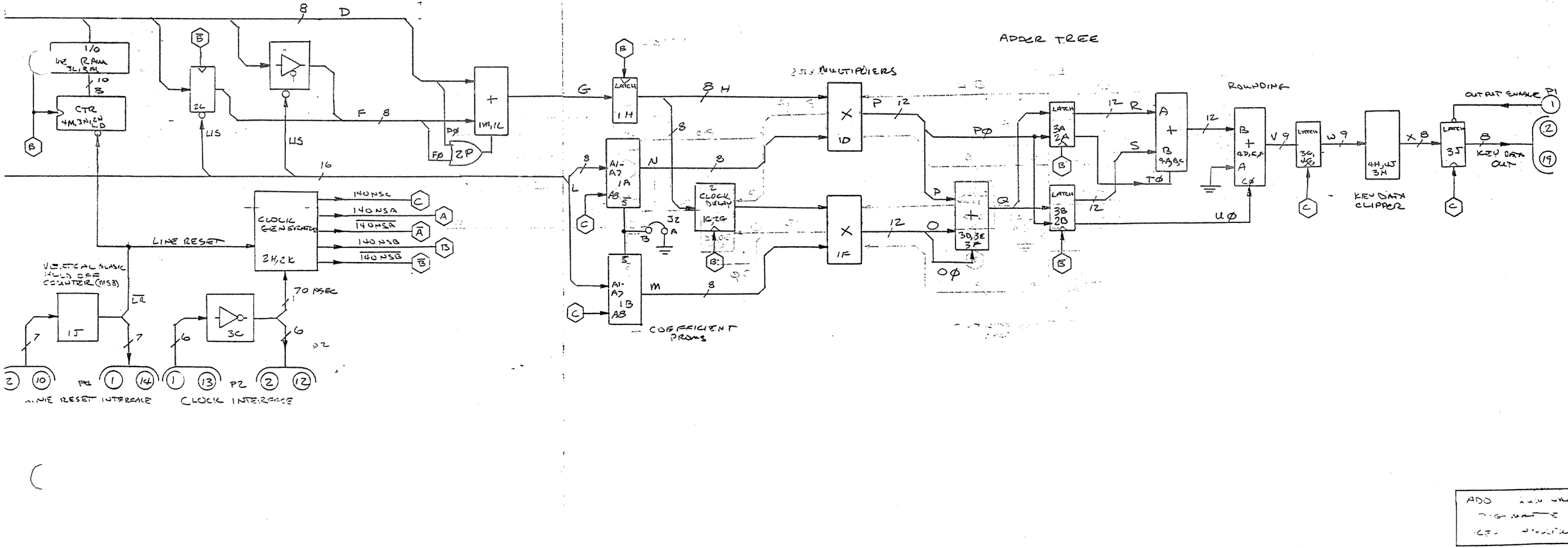
COLOR PROC

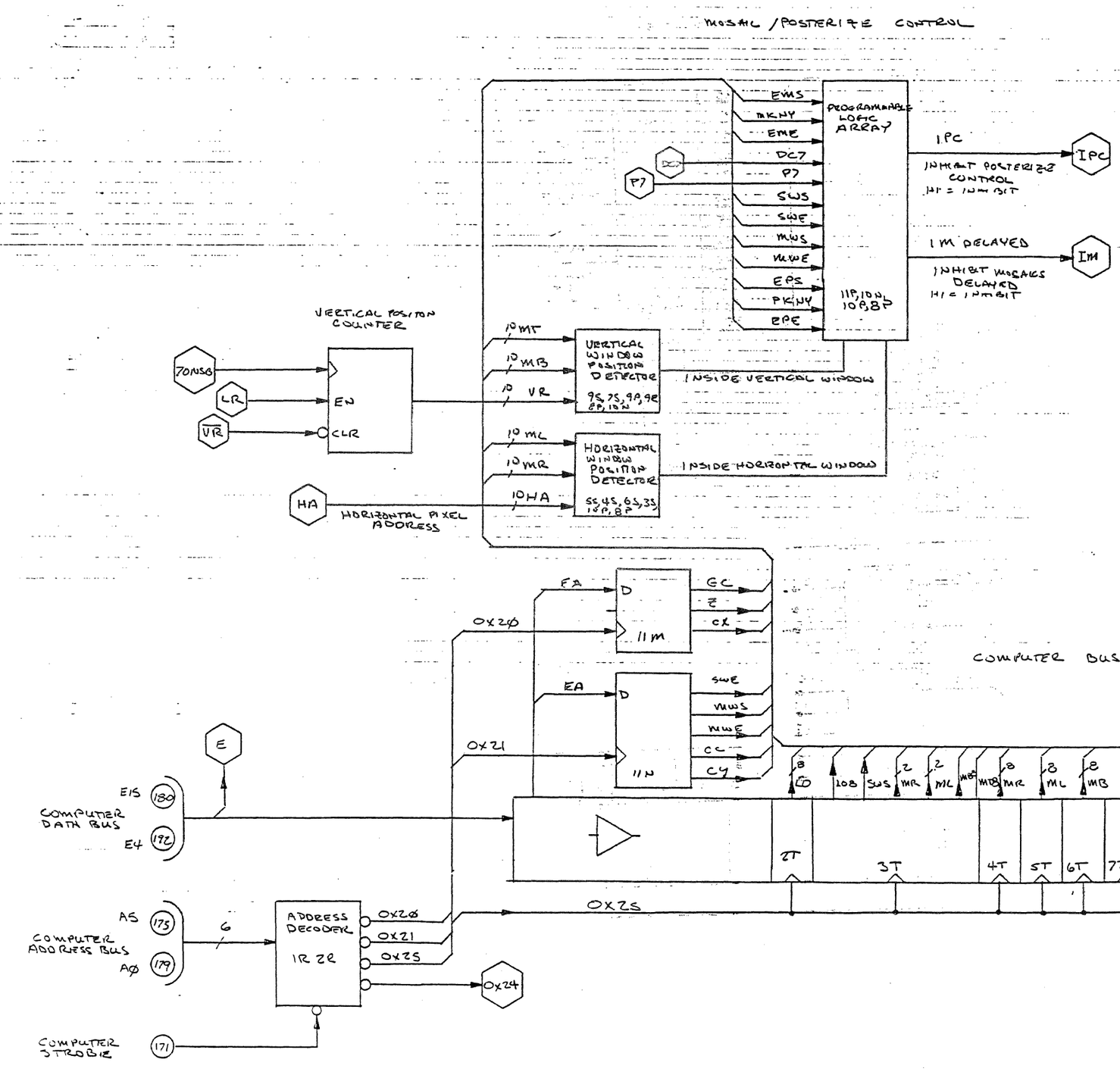
FINE BLANKER

+5V
C
B
A
J1
PAL
NTSC
280 NSEC
U ZERO ENABLE
1K,1D
EDGE AVERAGING
DATA INPUT LATCH
EN
2N
AF
AE
8
RED DATA IN
2M
OC
5N
AG
1N
G
FIPE BLANKING VALUES
3,5,4M +R
AH
LATCH 7M
LATCH 6M
AD
AT
MEMORY INPUT LATCHES
7G
6G
AJ
K DATA
ADDRESS MULTIPLEXER
DECIMATE ADDR
AV
AW
LO FILTER ADD
AY
HI FILTER ADD
7A,7B
6A,6B
Y
R-Y DATA STORE RAMS
7E,7F
6E
7F
LO DATA
HI DATA
DECIMATOR INPUT LATCHES
HI
LO
7J
6J
J
I
HI DATA
LO DATA
TO B-Y DATA STORE RAMS ADDRESS
INTERPOLATOR
LATCH 7L
LATCH 6L
HI
PATA IN
AC
COEFF IN
X 9L
AK
4 POINT ADDER
+ 8A,9A 9T
AL
AL 3 AL11
AN
7A,8T
INTERMEDIATE SUM STORE
12 AL0-AL11
R-Y CHROMA ACCUMULATOR
7T
R-Y CHROMA CLIPPER
5R,5U 5P,5T 6R,6T
COARSE BLANKER
IR,IS
AM
8
145
138
RED DATA OUT
AG
COMPUTER DATA
1L
COARSE BLANKER DATA STORE
TO DECIMATOR

Schematic
SHEET 7OF 7
COLOR PROC


11
KEY 140 NSEC KEY
3
18
E
LATCH
4K
EN
C
8
A
COARSE DELAY CONTROL PROMS
B L
A1-A8
2R,2S
J3
K 11
DELAY COUNTER
3P,3R 3S
A
11
A
COARSE DELAY RAM I/O
4N,4R 4S,4P WE
A
8
8
1Y0,3A
DATA LATCH
4L
EN
D
J5
A
I/O
WE RAM 3L,3M
I/O
B
CTR
4M,3A1,2N LD
B
B
2L
L15
CLOCK GENE
MOSAIC/POSTERIZE CONTROL LATCH
8
1R
8
8
OX25
KEY DELAY/CONTROL LATCHES
16
1N,1P
L
LINE RESET
VERTICAL MNEMONIC HOLD OFF COUNTER (MSB)
LR
7
1J
7
6
3C
P5
3
18
11
2
19
COMPUTER DATA
P4
2
10
P3
1
14
LINE RESET INTERFACE
1
13
P2
2
CLOCK INTERFACE


ADDER TREE
25 MULTIPLIERS
COEFFICIENT PROMS
ROUNDING
KEY DATA CLIPPER
OUTPUT ENABLE
KEY DATA OUT
CLOCK GENERATOR
2H,2L
LINE RESET
140NSC
140NSA
140NSB
70 NSEC
VERTICAL BASIC HOLD OFF COUNTER (MSB)
CLOCK INTERFACE
LINE RESET INTERFACE
ADD



COMPUTER BUS NOMENCLATURE

EMS	EXTERNAL MOSAIC SENSE	HI = INVERT MSB
MKNY	MOSAIC KEY NOT Y	HI = USE KEY MSB
PKNY	POSTER KEY NOT Y	HI = USE KEY MSB
DC7	EXTERNAL KEY MSB	
P7	LUMINANCE MSB	
SWS	SOLAR WINDOW SENSE	HI = INSIDE, LO = OUTSIDE
SWE	SOLAR WINDOW ENABLE	HI = BOUNDED BY WINDOW
MWS	MOSAIC WINDOW SENSE	HI = INSIDE, LO = OUTSIDE
EPS	EXTERNAL POSTER SENSE	HI = INVERT MSB
EPE	EXTERNAL POSTER ENABLE	
MT	RECTANGULAR WINDOW TOP BORDER	
MB	RECTANGULAR WINDOW BOTTOM BORDER	
ML	RECTANGULAR WINDOW LEFT EDGE	
MR	RECTANGULAR WINDOW RIGHT EDGE	
MV	MOSAIC VERTICAL BLOCK SIZE	
MH	MOSAIC HORIZONTAL BLOCK SIZE	
CCS	CHROMA SHIFT	
CY	CHROMA MAPSELECT	
CX	LUMA MAP SELECT	
LO	LUMINANCE OFFSET	
CMVE	CHROMA MOSAIC VERTICAL ENABLE	HI = ENABLE
CMHI	CHROMA MOSAIC HORIZONTAL INHBIT	HI = INHBIT
GC	GRID CONTROL	HI = INVERT LUMA MSB, LO = WHITE GRID
Z	KEY MAP SELECT	
MWE	MOSAIC WINDOW ENABLE	HI = BOUNDED BY WINDOW
EME	EXTERNAL MOSAIC ENABLE	HI = ENABLE EXTERNAL

COMPUTER BUS COMMAND / CONTROL SHIFT REGISTER

ADO 3/3 LUMINANCE INPUT VIDEO PROCESSOR

COMPUTER CONTROL

ECL TO TTL CONVERSION

(128) (144)

1L, 2L

A 8

Y DATA IN FROM A/D CONVERTER

Y DATA LATCH 9F

8 Y DATA

LUMINANCE INVERSION

LUMINANCE OFFSET ADDER

9 LD

LUMINANCE OFFSET VALUE

A Σ S B

E8 E7 DIFF = INVERT

8

P 8

P7 LUMA DATA BIT

LUMINANCE POSTERIZE MAPPING PROM

A0-A7 A8-A10 O0-O7 CS 6E, 6G

XØ-X2 X3 XS

AA 8

70NSB

LUMA MAP SELECT

LLW

PAL CHROMA LINE AVERAGING

(145) (162)

1N, 2N

8

DATA LATCH

C 8

CHROMA/KEY DATA IN FROM A/D CONVERTER

PCLK

COLOR DATA LATCH 4N

D 8

CHROMA MEMORY

5M

E 8

SP, SR 3M VO WE A0-A9

E

10

H

LATCH SN

G 8

CE

A B 3.5K 3L Σ

J 8

OC D Q CK 4K

PCLK

ES4 NTSC ES5 ES3 PAL

G 4L

CK 8

CHROMA DATA

COLOR DATA SHIFTER

CSØ CS1 SHIFT CTL 6K, 6L 6M

2

70NSB

INHIBIT POSTERIZE/COLORIZE

IPC

CHROMA SHIFT CTL

LUMA MAP SELECT CX

CHROMA MAP SELECT CY

10L, 11L, 12L

X 4

Y 3

POSTERIZE/COLORIZE DISABLE SWITCH

CHROMA POSTERIZE MAPPING PROM

A0-A7 A8-A10 O0-O7 7N

3 Y

CHROMA MAP SELECT

70NSB

CLOCK/ ADDRESS GEN

70NSA

10

H/HA

LINE PIXEL ADDRESSES HA → 10

CHROMA AND KEY DATA

3M, 3R, 4P, 4R, 9M

140 NS KEY

COLORCLK1

COLOR EN1

COLORCLK2

COLOR EN2

COLOR EN

LR LINE RESET

CE

YCKE

COLOR/KEY CLOCKS AND ENABLES

MC MAPPING CONTROL

C

A0-A7 A8 A10 9L KEY MAPPING PROM O0-O7

3 KEY MAP SELECT

LUMINANCE INVERSION

LUMINANCE =SET ADDER

DIFF = INVERT

LUMA DATA (BIT)

LUMINANCE POSITIVE MAPPING PROM

LUMA MAP SELECT

LUMA RECLOCK LATCH

LUMA LINE STORE

LUMA LINE WRITE

LUMA PIXEL STORE

XAIS OUTPUT CONTROL PWA

GRID

GRID INSERTION

BIT 7 GRID INVERSION

TO VERTICAL Y MEMORIES XA2 - XA6

CHROMA DATA

COLOR DATA SHIFTER

SHIFT CTL

CHROMA POSTERIZE MAPPING PROM

CHROMA MAP SELECT

CHROMA RECLOCK LATCH

CHROMA LINE STORE

CHROMA LINE WRITE

1 LINE RAM

CHROMA PIXEL STORES / CHROMA AND ICEY RE-MULTIPLIER

COLOR CLK1

CLRENE

CMIHI

COLOR1EN

COLOR2CLK

CLRENE

CMIHI

COLOR2EN

XAB CHROMA/KEY MEMORY

CHROMA AND KEY VIDEO OUT

R-Y/B-Y/KEY OUT

KEY BIT 7 DB7

KEY RAM DELAY 4K X1 BIT

DELAYED KEY BIT 7

KEY RAM DELAY ADDRESS GENERATOR

DIP SWITCH 12F, 12E

POSTERIZE/COLORIZE DISABLE SWITCH

KEY MAP SELECT

KEY RE-MULTIPLEX/ ICEY INTERPOLATOR

NONE KEY

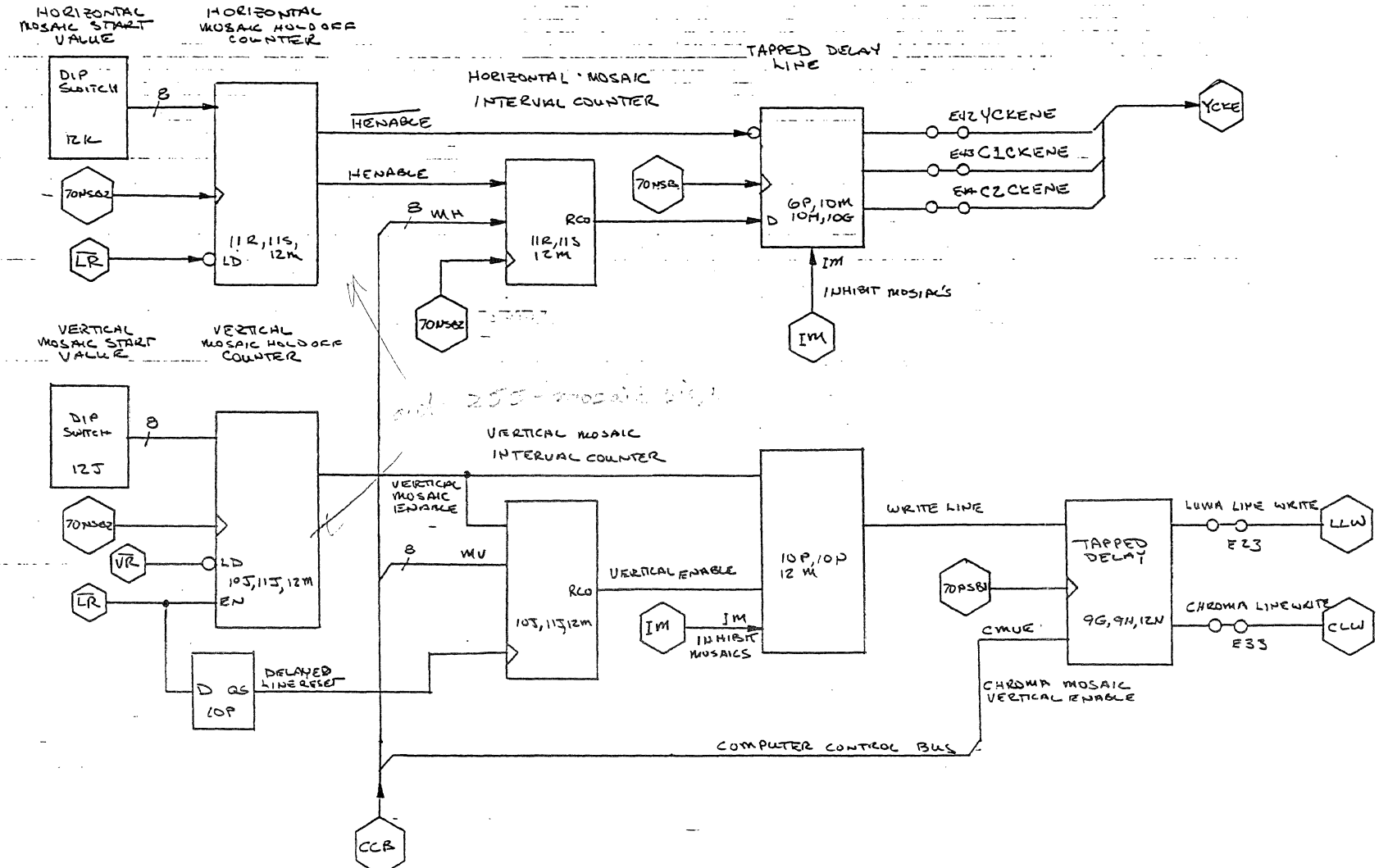
COLOR EN

White = +127
Black = 0
Bk = -128

bit = inside window
not bit = outside window

ADD 1/3 LUMINANCE INPUT VIDEO PROCESSOR

LUMINANCE / CHROMA/ ICEY PROCESSING


HORIZONTAL MOSAIC START VALUE
HORIZONTAL MOSAIC HOLDOFF COUNTER
DIP SWITCH 12K
8
11R,11S, 12M
LD
LR
70NS82
HENABLE
HORIZONTAL MOSAIC INTERVAL COUNTER
TAPPED DELAY LINE
8 MH
RCO
11R,11S 12M
70MSB
6P,10M 10M,10G
D
IM
INHIBIT MOSAICS
E12YCKENE
E13C1CKENE
E14C2CKENE
YCKE
VERTICAL MOSAIC START VALUE
VERTICAL MOSAIC HOLDOFF COUNTER
DIP SWITCH 12J
VERTICAL MOSAIC INTERVAL COUNTER
VERTICAL MOSAIC ENABLE
VR
10J,11J,12M
EN
8 MV
RCO
10J,11J,12M
VERTICAL ENABLE
10P,10P 12M
WRITE LINE
70PSBV
TAPPED DELAY
9G,9H,12N
CMUE
LUMA LINE WRITE
E23
LLW
CHROMA LINEWRITE
E33
CLW
CHROMA MOSAIC VERTICAL ENABLE
D Q5 10P
DELAYED LINE RESET
COMPUTER CONTROL BUS
CCB