Arix Corporation

IOSB Adapter Module (IOSB)

Preliminary Functional Spec.
May 01, 1989

Bruce Elliott (408) 446-2072

INTRODUCTION

Large System 90 configurations will require more than 16 modules. For expansion, several 16 port buses can be connected. One 16 port bus is the CSS bus, the other 16 port buses are I/O system buses (IOSB).

The IO System Bus Adapter (IOSBA), in conjunction with a LINK and an I/O module (IOM), is used to connect an I/O bus to the CSS bus. The IOSBA resides in the highest priority slot of the I/O bus, the IOM resides in a high priority slot of the CSS bus, and the LINK connects the IOSBA and IOM.

The I/O System Bus Adapter Module will be an 8 layer board. The IOSBA will be plugged directly into an I/O expansion chassis. The adapter will connect to the IOSB via a 150 pin female system connector and a 80 pin female arbiter connector.

Two 64 pin connectors will provide for direct connection to an IOM via two 64 pin ribbon cables with lengths of up to 15 feet (I/O LINK).

2 I/O ADAPTER TRANSMISSION CONVENTIONS

Commands originating on an I/O bus that are addressed to a slot on the CSS bus or another I/O bus must be sent to the CSS bus for delivery. Commands originating on an I/O bus that are addressed to a slot on that same I/O bus may also be sent to the CSS bus for delivery. The first read command of an interlocked sequence must also be sent to the CSS bus to obtain system lock.

To send a COMMAND to the CSS bus for delivery, a module on an I/O bus sets ARB.DEST[3:0] equal to BUS.IOSBA.SLOT[3:0] when requesting permission from the I/O bus arbiter to transmit, and asserts BUS.IOX.ACTIVE, to signal that transmission is on the I/O bus. BUS.IOX.ACTIVE indicates that the transmission is for the IOSBA. At this point BUS.DEST[3:0] is the CSS bus slot, not an I/O bus slot. The IOSBA receives the command and forwards it to the CSS bus by way of the LINK and IOM.

COMMANDS addressed to a slot on an I/O bus are delivered first to the IOM that connects to that I/O bus. The CSS bus module sets ARB.DEST[3:0] and BUS.DEST[3:0] equal to BUS.IOM.SLOT[3:0] when requesting permission from the CSS bus arbiter to transmit, and asserts BUS.ACTIVE, to signal that transmission is on the CSS bus. The destination I/O slot is carried in SYSTEM ADDRESS[31:28] (BUS.DATA[47:44]). The IOSBA connected to the IOM will copy these bits to the destination field for transmission of the COMMAND on the I/O bus (I/O bus ARB.DEST[3:0] and BUS.DEST[3:0]). COMMANDS to an IOM and the attached IOSBA are addressed to BUS.DATA[47:44] = F regardless of the location of the IOM on the CSS bus and the IOSBA on the I/O bus.

RESPONSE Transmissions originating on an I/O bus are sent to the I/O bus slot from which the read command was received. If the requester is on another bus, the destination of the response will initially be the slot of the IOSBA (ARB.DEST[3:0] and BUS.DEST[3:0] equal to BUS.IOSBA.SLOT[3:0]). The IOSBA maintains the source slot of each Read Command it transmits on the I/O bus and copies that source slot into the Destination field of the RESPONSE that is returned to it. The response is then forwarded to the connecting IOM via the LINK. Modules always assert BUS.ACTIVE when transmitting RESPONSES.

RESPONSE Transmissions originating on a CSS bus are sent to the CSS bus slot from which the read command was received. If the requester is on

another bus, the destination of the response will initially be the slot of the IOM which requested the Read Command (ARB.DEST[3:0] and BUS.DEST[3:0] equal to the source IOM.SLOT[3:0]). The IOM maintains the I/O bus source slot of each Read Command it transmits on the CSS bus and copies that source slot into the Destination field of the RESPONSE that is returned to it. The RESPONSE is then forwarded to the connecting IOSBA via the LINK.

3 I/O ADAPTER HARDWARE OVERVIEW

Figure 1 is the I/O System Bus Adapter Block Diagram. The IOSBA consists of a Down-link Section, a Up-link Section, and a Local Control/Status section.

3.1 DOWN LINK SECTION

The down-link section consists of a down-link control circuit, down-link response and command FIFOs, and an IOSB output section.

3.1.1 DOWN-LINK CONTROL CIRCUIT

The down-link control circuit monitors all link transmissions and checks them for errors. It latches all error free commands and responses into the down-link FIFOs. Since the link is only 32 bits wide, the control circuit assembles commands and responses into 64 bit quantities which are then stored in the FIFOs. In accordance with the link protocol, a link type field is sent down the link with each 32 bits of data. This link type field is used to assemble the 64 bit quantity and attach an IOSB data type. 32 bit responses and read commands are assembled in both halves of the 64 bit quantity.

The down-link control circuit also strips commands for the local control and status registers, which are not entered into the down-link FIFO. The local control/status section executes them and immediately increments the command counter in the IOM.

3.1.2 DOWN-LINK FIFOs

The down-link contains an 8 deep command FIFO and an 8 deep response FIFO. The down-link FIFOs are loaded synchronous to the link clock and unloaded synchronous to the IOSB clock.

The following information is stored in the down-link response FIFO:

- Response data bytes<63:00>
- Response data parity<7:0>
- Response source<3:0> (not required)
- Response destination<3:0>
- Response type<5:0>
- Response type parity

The following information is stored in the down-link command FIFO:

- Command data bytes<63:00>
- Command data parity<7:0>
- Command source<3:0>
- Command destination<3:0>
- Command destination parity

Command type<5:0>
Command type parity

3.1.3 IOSB OUTPUT SECTION

The output section controls sending commands and responses over the IOSB. Responses are always sent with higher priority than commands. Commands are immediately backed off if a response is entered into the response FIFO. When a command is sent to the IOSB it is unloaded from the down-link command FIFO and a strobe synchronized to the link clock is sent to increment the ready counter on the IOM.

Only one read command can be outstanding on the IOSB at any time. Before a read command is sent on the IOSB, the output control section checks that there is enough space in the up-link response FIFO to hold the expected response. Because one entry can always be unloaded from the up-link response FIFO faster than the IOSB can load four responses, checking the FIFO's full status for less than six entries (3 to 8 empty) will assure that there is enough space for a response of any size. When a read command is sent on the IOSB, a counter is loaded with the size of the expected response and the source of the read command is saved so that it can be appended as the destination field of corresponding IOSB responses.

The IOSB output section will monitor the IOSB for ARB.GRANT timeouts and response timeouts. A timeout will result in error information being latched and a interrupt being sent to the IOM. For grant timeouts, the current request will be removed and the current FIFO output unloaded. For response timeouts, the pending read command will be terminated.

The IOSBA can send commands and responses to the IOSB every 3 IOSB clock cks.

3.1.4 DOWN-LINK SYNCHRONIZATION

The down-link control circuit uses the link clock to load the down-link FIFOs.

The IOSB output section uses the IOSB clock to unload the down-link FIFOs.

The synchronizing stage of the down-link FIFOs will be enabled to provide a READY_A and READY_B output that is synchronous with the IOSB clock.

A ready increment strobe will be generated when a command has been sent on the IOSB. It will be synchronized with the link clock to generate the link signal IOA.RDY.INC.

The up-link FIFOs synchronizing stage will be enabled to provide FULL_A and FULL_B outputs which are synchronized to the IOSB clock.

3.2 UP-LINK SECTION

The up-link section consists of the IOSB Input Section, Command and Response FIFOs, and the Link Control Circuit.

3.2.1 IOSB INPUT SECTION

The IOSB input section monitors all activity on the IOSB bus. This section latches all error free commands sent using the BUS.IOX.ACTIVE strobe and all error free commands sent using the BUS.ACTIVE strobe that matches the IOSBA destination slot number into the up-link command FIFO. It also loads all error free responses matching the IOSBA destination slot number.

The IOSB input section contains a IOSB ready counter which is monitored

by the IOSB arbiter. The ready counter is set to eight on IOSB reset. The ready counter is decremented by the arbiter and incremented by the up-link command FIFO control logic. It can also be incremented by the input section if the ready counter was decremented and no valid command was received.

All commands and responses directed to the IOSBA are checked for source errors, destination errors, type errors, and data errors if DATA.PAR.VALID is asserted. Responses are also checked to make sure that their source match the destination of the last read command. All data parity is regenerated and added to the data before it is loaded into the up-link FIFOs. If an error is detected, a local IOSBA error latch will be loaded with pertinent information and the up-link control circuit directed to send an interrupt to the SPM (send a interrupt write command up the link).

In addition to monitoring commands and responses directed to the IOSBA, the IOSB input section monitors all IOSB bus activity for error conditions. If an error condition is detected, a local IOSBA error latch will be loaded with pertinent information and the up-link control circuit directed to send an interrupt to the SPM (send a interrupt write command up the link).

3.2.2 UP-LINK COMMAND AND RESPONSE FIFOs

The up-link contains an 8 deep command FIFO and an 8 deep response FIFO. The up-link FIFOs are loaded synchronous to the IOSB clock and unloaded synchronous to the link clock.

The following information is stored in the up-link response FIFO:

- Response data bytes<63:00>
- Response data parity<7:0>
- Response destination<3:0>
- Response source<3:0> (required for link error checking)
- Response source parity (required for link error checking)
- Response type<5:0>
- Response type parity

The following information is stored in the up-link command FIFO:

- Command data bytes<63:00>
- Command data parity<7:0>
- Command source<3:0>
- Command destination<3:0>
- Command destination parity
- Command type<5:0>
- Command type parity
- Command sequence number<1:0> (identifies locked sequences)

3.2.3 UP-LINK CONTROL CIRCUIT

The Up-link Control Circuit is synchronous with the link clock. It is in charge of sending command and responses over the link, and controlling locked operations. Since the link is only 32 bits wide, the control circuit must disassemble up-link commands and send them according to

the link protocol. Responses are always sent with higher priority then commands.

Because down-link response FIFOs can always be unloaded faster than the link can load them, read commands are sent up the link without checking if there is space available in the down-link response FIFO.

The up-control circuit is also responsible for sending responses up the link for reads of local IOSBA registers and sending interrupts to the SPM (sending a write command up the link) if a condition occurs which necessitates processor intervention.

For locked operations, the ARB.LOCK* signal from the IOSB is monitored, and the links LNK.RM.SEQ* is controlled. A locked sequence starts when the IOSB input section receives an error free command with ARB.LOCK* asserted. The command is entered into the up-link command FIFO along with an asserted RM.SEQ bit and a RM.SEQN bit. The RM.SEQN bit is from a register that toggles whenever ARB.LOCK* goes from asserted to non-asserted.
As long as the ARB.LOCK* signal stays asserted, all commands will be loaded into the command FIFO along with the RM.SEQ bit asserted and the current RM.SEQN bit.
At the start of a locked sequence, the link signal LNK.RM.SEQ* is asserted when the 1st read command for that locked sequence is sent up the link. LNK.RM.SEQ* will remain asserted until all commands for the current locked sequence have been sent up the link. All commands for the current lock sequence have been sent up the link, when one of the following occurs:

ARB.LOCK* is deasserted and the up-link command FIFO is empty.

RM.SEQN bit of the next up-link command is inverted from that of the last up-link command, indicating a new locked sequence.

RM.SEQ bit of the next up-link command is deasserted, indicating that the next command is not a locked sequence.

After a locked sequence ends, the LNK.RM.SEQ signal will be deasserted for a minimum of one link clock cycle before it is asserted again.

The link control circuit also contains a ready counter for the IOM's command FIFO. This is decremented by the IOSBA when a command is sent to the IOM. The IOM increments the counter whenever it unloads the command from its command FIFO. After reset, the IOM increments this counter to the correct number of command buffers available in the IOM.

3.2.4 UP-LINK SYNCHRONIZATION

The IOSB input section uses the IOSB clock to load the up-link FIFOs.
The up-link control circuit uses the link clock to unload the up-link FIFOs.
The IOSB ready counters will be maintained using the IOSB clock. The up-link control circuit will provide an increment IOSB ready signal when a command has been unloaded from the up-link command FIFO. This signal will be synchronized to the IOSB clock.
The ARB.LOCK signal from the IOSB is synchronized to the IOSB clock. It will be captured and resynchronized to the link clock for use with locked operations.

The up-link FIFOs synchronizing stage will be enabled to provide FULL_A and FULL_B outputs which are synchronized to the IOSB clock for use by the IOSB output section.

3.3 LOCAL CONTROL/STATUS SECTION

The local control/status section consists of a local control circuit and an assortment of control and status registers.

3.3.1 LOCAL CONTROL CIRCUIT

The local control circuit monitors for down-link commands directed to the local control/status register address space. Commands are executed immediately and the the command counter in the IOM incremented. For read commands, the uplink control circuit is informed that read data is available to be sent up the link. The up-link response FIFO is given priority.

The local control logic also monitors the IOSB down-link control circuit, the IOSB output section, the IOSB input section, and timeout error detection circuits for a request to send an interrupt request to the SPM (send an interrupt write command up the link). The local control circuit co-ordinates with the up-link control circuit to send the command data up the link.

The CSS system is permitted to have only one outstanding read command to the IOSBA local address space.

Parity generation is provided for all local/control data sent up the link.

3.3.2 LOCAL CONTROL/STATUS REGISTERS

The IOSBA will have various Control and Status registers in the IOSBA address range of FFFFE000 to FFFFEFFF. Control registers may be read back at the same address as their write address.

ERROR REGISTERS: A bit is set in an error status if its corresponding error condition is detected. Error data is also latched into corresponding error status registers. To clear a bit and re-enable its corresponding error status registers, a 0 must be written to its bit location.

CONTROL REGISTERS: these registers are used to control various test parameters, interrupt control, and error register control.

INTERRUPT REGISTERS: these registers are used to provide interrupt information to the the SPM.

FIFO CONTROL BUS: For test purposes, internal FIFO registers are accessable via an 8 bit FIFO control bus. As per Associative FIFO specification, the FIFO control port is written with the register number for which access is desired. The selected FIFO's register may then be read or written.

3.3.3 LOCAL CONTROL/STATUS SYNCHRONIZATION

The local control/status section uses the link clock for local access.

Status and interrupt requests that are originating from the IOSB are resynchronized using the link clock.

Control registers which are loaded from the link which effect the IOSB bus are resynchronized using the IOSB clock.

4 I/O ADAPTER TESTABILITY HARDWARE OVERVIEW

The local control/status section provides circuits to enable testing of the IOSBA. The following section is a cursory description of the features provided for testability. A detailed description of the actual control bits and status bits is given in the control/status register section.

4.1 LOOPBACK

Test circuits are provided to enable loop-back of read and write commands on the IOSB. A command may be sent down the link to set a bit in a local control register that places the IOSBA into loopback mode.

4.1.1 LOOPBACK OF WRITE COMMANDS

For write commands sent down the link, the destination I/O slot is carried in SYSTEM ADDRESS[31:28] (BUS.DATA[47:44]). The IOSBA will copy these bits to the destination field for transmission of the COMMAND on the I/O bus (I/O bus ARB.DEST[3:0] and BUS.DEST[3:0]). The IOSBA will drive BUS.IOX.ACTIVE which will cause the write command to loop back to the IOSBA and be sent back up the link to the system destination that was specified in BUS.DATA[47:44].

4.1.2 LOOPBACK OF READ COMMANDS AND RESPONSES

For read commands sent down the link, the destination I/O slot is carried in SYSTEM ADDRESS[31:28] (BUS.DATA[47:44]). The IOSBA will copy these bits to the destination field for transmission of the COMMAND on the I/O bus (I/O bus ARB.DEST[3:0] and BUS.DEST[3:0]). The IOSBA will also save the source of the read command, SB.SLOT[3:0] and set the IOSB source to the IOSBA slot. The IOSBA will then drive BUS.IOX.ACTIVE which will cause the read command to loop back to the IOSBA and be sent back up the link to the system destination that was specified in BUS.DATA[47:44]. The IOM will save the source to the up-link read command (IOSBA slot) and issue the system read command. When the IOM receives the response it will attach the IOSBA slot to the destination field and send it down the link. The IOSBA will send the response to the IOSB with the IOSBA slot being the destination. This will cause the read response to be looped back to the IOSBA. The IOSBA will attach the saved source of the read command and send it up the link to the originator of the read command.

4.2 SINGLE STEP

Single step control is provided for down-link and up-link control. Used in conjunction with the FIFO control port, loopback, and each other, all FIFO locations can be tested.

4.2.1 DOWN-LINK SINGLE STEP

A single step mode enable and single step execute bit is provided for down-link command control. When the single step mode bit is set to single step mode, down-link commands will be loaded into the down-link FIFO but will not be sent to the IOSB. Causing the single step execute bit to transition from non-asserted to asserted will cause one FIFO entry to be transmitted on the IOSB.

A single step mode enable and single step execute bit is provided for down-link response control. When the single step mode bit is set to single step mode, down-link responses will be loaded into the down-link response FIFO but will not be sent to the IOSB. Causing the single step execute bit

transition from non-asserted to asserted will cause one FIFO entry to be transmitted on the IOSB.

In order to test response FIFOs, read commands must be issued by the CSS system. In single step mode, the IOSBA and CSS system will detect a response timeout. In order to prevent IOSBA response timeout, the system may set a local control bit that will disable IOSBA timeouts. In order to prevent system timeout, in single step test mode, the system may set a local control bit that will cause the IOSBA to convert down-link write commands to read commands. Thus in loopback mode, the IOSBA response FIFOs can be tested by issuing write commands.

The down-link single step control register is loaded using the link clock. These signals will be resynchronized using the IOSB clock.

4.2.2 UP-LINK SINGLE STEP

A single step mode enable and single step execute bit is provided for up-link command control. When the single step mode bit is set to single step mode, up-link commands will be loaded into the up-link FIFO but will not be sent to the link. Causing the single step execute bit to transition from non-asserted to asserted will cause one FIFO entry to be transmitted on the link.

A single step mode enable and single step execute bit is provided for up-link response control. When the single step mode bit is set to single step mode, up-link responses will be loaded into the up-link response FIFO but will not be sent to the link. Causing the single step execute bit to transition from non-asserted to asserted will cause one FIFO entry to be transmitted on the link.

4.3 ERROR TESTING

4.3.1 DOWN LINK ERROR CHECKING

The down-link control circuit can detect parity errors in data, type ioslot, and sbslot fields. The IOM has control registers which enable parity errors to be generated for IOSLOT and LNK DATA. The IOM will therefore, be used to test the IOSBA downlink error detection of these fields. An IOSBA control register will provide a bit which will cause the sbslot parity to be inverted when received on the down-link. This will provide a means for testing sbslot parity error detection. An IOSBA control register will also provide a bit which will cause the LNK TYPE parity to be inverted when received on the down-link. This will provide a means for testing link type parity error detection.

In order to have access to local address space to turn off these bits once set, parity errors will not be generated for local IOSBA address space accesses.

4.3.2 IOSB ERROR GENERATION AND DETECTION

An IOSBA control register will be provided that will enable independant generation of IOSB data, type, dest, and src errors. With the IOSBA in non loopback mode, this will provide a means of testing the IOSBA bus activity monitor as well as testing error detection for other modules on the IOSB. In loopback mode, this feature will provide a means for testing the IOSBA input section (up-link) error detection.

An IOSBA control register bit will be provided for enabling or disabling response timeouts. In single step mode, this provides a means for testing response timeouts.

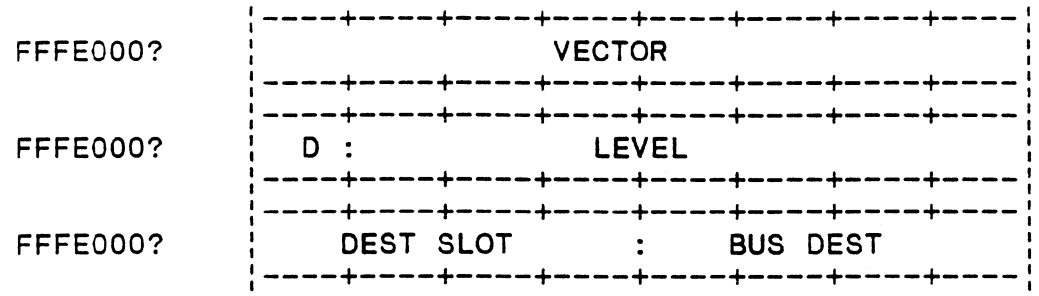
3.3 UP LINK ERROR CHECKING

Up-link error checking is done in the IOM. The IOM provides a means of testing its own error detecting circuits when in loopback mode.

5 IOSBA CONTROL/STATUS REGISTERS

The IOSBA will have various Control/Status registers. The IOSBA register address space is in the address range FFFFE000 to FFFFEFFF. These registers will be accessable from the CSS system bus. The requesting module must set BUS.DEST = IOM.SLOT, ARB.DEST = IOM.SLOT, A31-00 to the correct register address and drive BUS.ACTIVE. A31-28 will be F for IOM/IOSBA address space. These registers will also be accessable from the I/O bus by sending commands to the CSS system bus. The requesting module must set BUS.DEST = IOM.SLOT, ARB.DEST = IOSBA.SLOT, A31-00 to the correct register address and driving BUS.IOX.ACTIVE.

5.1 SB INTERRUPT CONTROL REGISTERS



VECTOR: Programmed by the system.

LEVEL: Programmed by the system.
D: A 1 specifies that this is a directed interrupt.

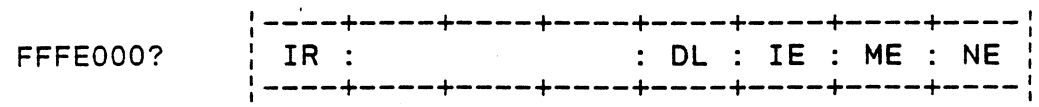
BUS DEST: Programmed by the system.
Sent as bus destination for interrupt commands.

DEST SLOT: Programmed by the system.
Sent as part of 32 bit interrupt command to direct SPM interrupts to a specified slot if the directed bit is set.

Sent as part of 32 bit interrupt command to direct SPM interrupts.

DEFAULT: NONE

5.2 ERROR CONTROL REGISTER



IR: Enables interrupt write commands to be sent up the link.

The following bits are set if its corresponding error condition is detected. Error data is also latched into corresponding error status registers. To clear a bit and re-enable its corresponding error status registers, a 0 must be written to its bit location.

DL: Set by the IOSBA when a down-link error is detected. Down-link error data is latched into the down-link error status registers.

IE: Set by the IOSBA when an error is detected in IOSB data directed to its IOSB input section (up-link). Error data is latched into the IOSB input error status registers.

ME: Set by the IOSBA when it IOSB bus monitor detects an bus error in activity for destinations other than the IOSBA. Error data is latched into the IOSB monitor error status registers. Errors can be caused by bus errors, naks, no acks/naks and IOSBA output section arb timeout.

NE: Set when the IOSBA detects a non-transmission type error. Error data is latched into the IOSB local error status registers. Errors can be caused by a response timeout, up-link buffer overflow or down-link buffer overflow.

DEFAULT: 00000000

5.3 TEST CONTROL REGISTER 1

FFFE000?

DE	SE	TE				LSBE	LTE

DE: Forces IOSB destination error by inverting BUS.DEST*
SE: Forces IOSB source error by inverting BUS.SRC*
TE: Forces IOSB type error by inverting BUS.TYPE.PAR

LTE: Forces down-link type error on non-local accesses by inverting LNK.TYPE.PAR on reception.
LSBE: Forces down-link sbslot error on non-local accesses by inverting LNK.SBSLOT<3:0> on reception.

DEFAULT: 00000000

5.4 TEST CONTROL REGISTER 2

FFFE000?

DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0

DE<7:0>: Forces IOSB data parity error by inverting BUS.DATA.PAR for the specified bits when driven on the IOSB bus.

DEFAULT: 00000000

5.5 TEST CONTROL REGISTER 3

FFFE000?

LR	LE	RX				RDY	FLT

LR: A 1 issues a local IOSBA reset. Self clearing.

LE: Enables IOSB loopback mode.
RX: Enables write commands to be converted to read commands for response loopback testing in single step mode.

RDY: A 1 will turn on the front panel green RDY led.
NORM: A 0 will turn on the front panel red FLT led.

DEFAULT: 00000000

5.6 TEST CONTROL REGISTER 4

FFFE000?

DCE	DCX	DRE	DRX	UCE	UCX	URE	URX

DCE: Sets down-link command mode to single step.
DCX: A 0 to 1 executes a down-link command FIFO single step
DRE: Sets down-link response mode to single step.
DRX: A 0 to 1 executes a down-link response FIFO single step
UCE: Sets up-link command mode to single step.
UCX: A 0 to 1 executes a up-link command FIFO single step
URE: Sets up-link response mode to single step.
URX: A 0 to 1 executes a up-link response FIFO single step

DEFAULT: 00000000

5.7 CARD ID STATUS REGISTER

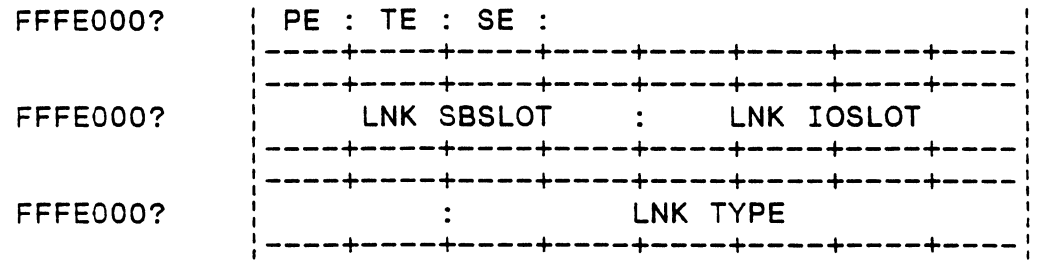
FFFEXXXC

??

CARD ID: The card id is a long word read only register. The IOSBA card id will be XXXXXX??H.

8 IOSB DOWN-LINK ERROR STATUS REGISTER 1

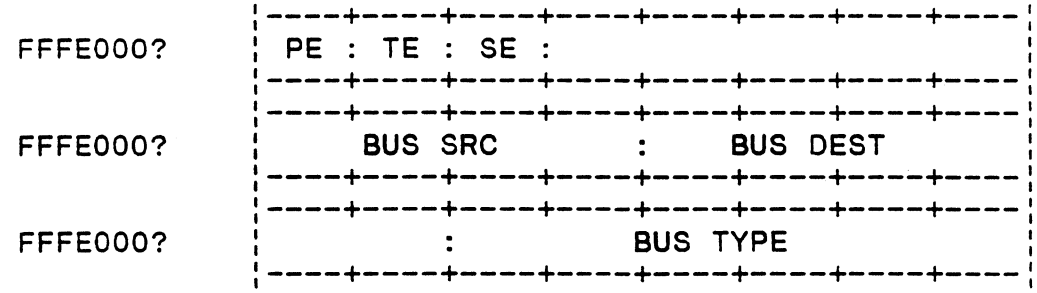
Valid only if the DL error bit is set in the ERROR CONTROL REGISTER.



PE: Data parity error detected
TE: Type error detected
SE: Source error detected
LNK SBSLOT: Received link sbslot field
LNK IOSLOT: Received link ioslot field
LNK TYPE: Received link type field

5.9 IOSB INPUT ERROR STATUS REGISTER 1

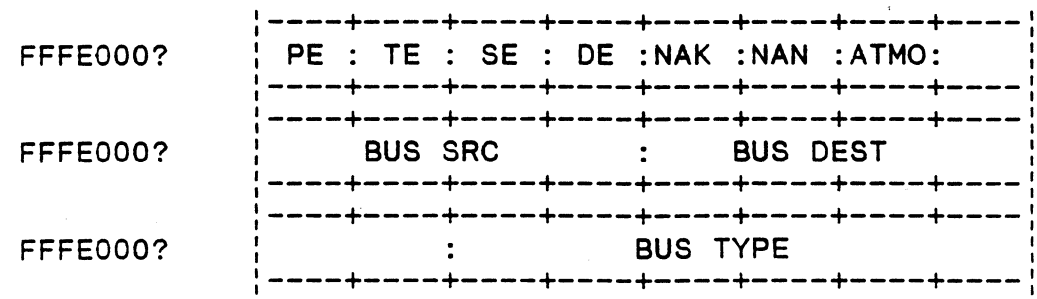
Valid only if the IE error bit is set in the ERROR CONTROL REGISTER.



PE: Data parity error detected
TE: Type error detected
SE: Source error detected
BUS DEST: Received IOSB dest field
BUS SRC: Received IOSB src field
BUS TYPE: Received IOSB type field

5.10 IOSB MONITOR ERROR STATUS REGISTER 1

Valid only if the ME error bit is set in the ERROR CONTROL REGISTER.

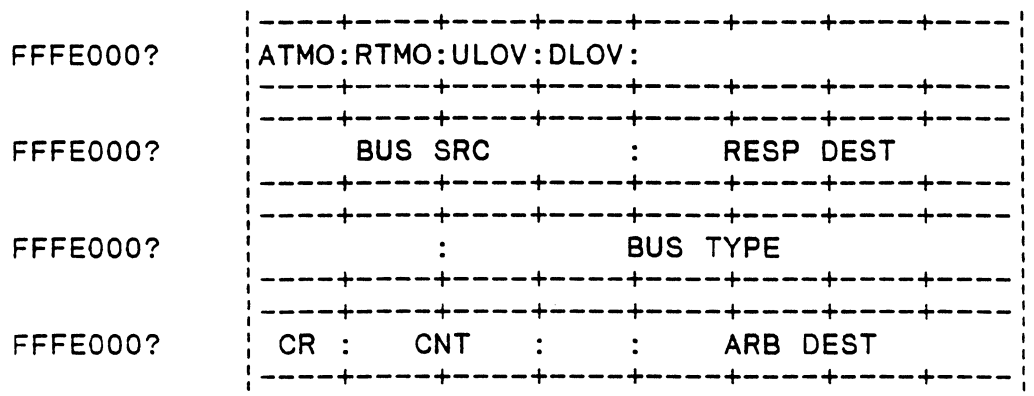


PE: Data parity error detected
TE: Type error detected
SE: Source error detected
DE: Destination error detected
NAK: Bus nak detected

NAN: No bus ack or nak transmitted
BUS DEST: Received IOSB dest field
BUS SRC: Received IOSB src field
BUS TYPE: Received IOSB type field
ARB DEST: requested ARB dest field
CR: 1 if command 0 if response

5.11 IOSB LOCAL ERROR STATUS REGISTER 1

Valid only if the NE error bit is set in the ERROR CONTROL REGISTER.



ATMO: Arbitration timeout
RTMO: Response timeout
ULOV: Up-link overflow
DLOV: Down-link overflow
ARB DEST: Requested ARB dest field
CR: 1 if command 0 if response
CNT: Remaining response count for current read command
RESP DEST: IOSB ARB dest field
BUS DEST: IOSB ARB dest field
BUS SRC: Received IOSB src field
BUS TYPE: Received IOSB type field

5.12 FIFO REGISTER REGISTERS 1

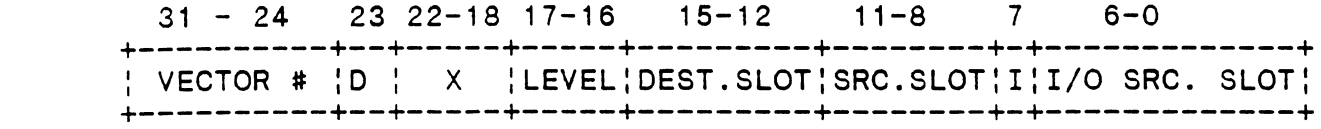
For test purposes, internal FIFO registers are accessable via an 8 bit FIFO control bus. As per Associative FIFO specification, the FIFO control port is written with the register number for which access is desired. The selected FIFO's register may then be read or written. The address space of the FIFOs are as follows:

Up-link	command	FIFO upper:	FFFE000?
Up-link	command	FIFO lower:	FFFE000?
Up-link	response	FIFO upper:	FFFE000?
Up-link	response	FIFO lower:	FFFE000?
Down-link	command	FIFO upper:	FFFE000?
Down-link	command	FIFO lower:	FFFE000?
Down-link	response	FIFO upper:	FFFE000?
Down-link	response	FIFO lower:	FFFE000?

6 INTERRUPTS

The IOSBA will generate CSS interrupts to the CSS bus by sending a 4 byte write command over the LINK to system address FFFFFFA0. The destination slot is programmed in the interrupt destination register described above. The

IOSBA will generate interrupts when enabled, upon detection of an I/O bus error, a UPLINK error, or DOWNLINK error. The IOSBA interrupt status registers as described above provides interrupt status.



I/O SRC. SLOT: I/O bus slot of IOSBA.

I: A 1 specifies that the adapter is on the I/O bus.

SRC.SLOT: IOM bus slot.

DEST.SLOT: The destination slot of a directed interrupt.

LEVEL: Priority Level.

D: A 1 specifies that this is a directed interrupt.

VECTOR: Specifies cause of interrupt vector

BUS TX.DEST.SLOT:
This value is programmed by the system into the IOSBA Interrupt Destination Register

7 CONTROL WRITE COMMANDS

A CSS bus module may issue a control write command to a module on the I/O bus as follows:

Issue a write command with DEST.SLOT = IOM.SLOT
Address = FFFFD00S where S = the slot # of the module to receive the control write command.
Data = type of control write command.
0: deassert module interface enable
1: assert module interface enable
2: deassert module enable
3: assert module enable

8 I/O ADAPTER LED INDICATORS

The IOSBA will have 5 LED's.

NORM	green:	Programmed from the CSS system bus
FLT	red:	Set upon reset and programmed from the CSS system bus
LINK	red:	Indicates LINK access
LFLT	red:	Indicates LINK bus fault. Driven from error control register.
BFLT	red:	Indicates I/O bus fault. Driven from error control register.

9 I/O ADAPTER RESET

The IOSBA will be reset upon receipt of the I/O bus signal BUS.RESET*, programmed card reset as described in the control/status register section, or a LINK IOA.RESET.

10 CLOCK DISTRIBUTION

The IOSBA will use the 20 MHZ BCLK* signal as its source of clock information.This signal will be loaded by six 74AS1804 loads. The 74AS1804 will drive the clock lines on the board.

The IOSBA will also use the 10 MHZ LNK.CLOCK* signal as a source of clock information. This signal will be loaded by four 74AS1804 loads and terminated to ground through a 100 ohm resister. The 74AS1804 will drive the appropriate clock lines on the board.

All clock lines will be routed without stubs.

11 LINK SIGNAL DISTRIBUTION

All signals will be driven, received, and terminated as per link spec.

All bidirectional signals will be terminated at the IOSBA with a 220 ohms to +5V and 220 ohms to ground. All bidirectional signals will be driven at the IOSBA with 74AS760 open collector drivers.

Unidirectional signals from the IOSBA to IOM will be driven with 74AS1804 drivers.

Unidirectional signals received by the IOSBA will be terminated at the IOSBA with 100 ohms to ground and clocked into 74ALS374's using the buffered and inverted link clock.

LNK.SLOT signals will be bypassed at the IOSBA with .1UF to ground.

LNK.A5V.SENSE will be terminated at the IOSBA with .001UF capacitor and 330 ohm resister to ground.

LNK.CONN1PIN1,LNK.CONN1PIN64,LNK.CONN2PIN1, and LNK.CONN1PIN64 will be connected to ground at the IOSBA.

12 CONNECTORS

The IOSBA board has the following 4 connectors.
One 150 pin female system connector
One 80 pin female Arbiter connector.
Two 64 pin female LINK connectors.

For signal description of system bus and Arbiter connectors see the System Bus Specification.

13 POWER CONSUMPTION

The IOSBA will use 5V only. It is estimated that this board will consume 12 A at 5V.

14 PERFORMANCE

The IOSBA uses the 20 MHZ CSS bus clock and the 10 MHZ LINK clock. Since these clocks are asynchronous with respect to each other, the IOSBA control signals are synchronized. This synchronization is overlapped with the bus transfers. Therefore, latency not transfer rate will be affected. The maximum data transfer rate will be 20 MBYTES/SEC when writing to the CSS bus and 35.6 MBYTES/SEC when reading from the CSS bus.

Writes: two 10 MHZ clk ticks for 4 byte write command

Reads: one 10 MHZ clk tick for read command
two 10 MHZ clk ticks for 8 byte response, up to 4 8 byte responses

Response and commands can be sent to the IOSB every IOSB 3 clock ticks.

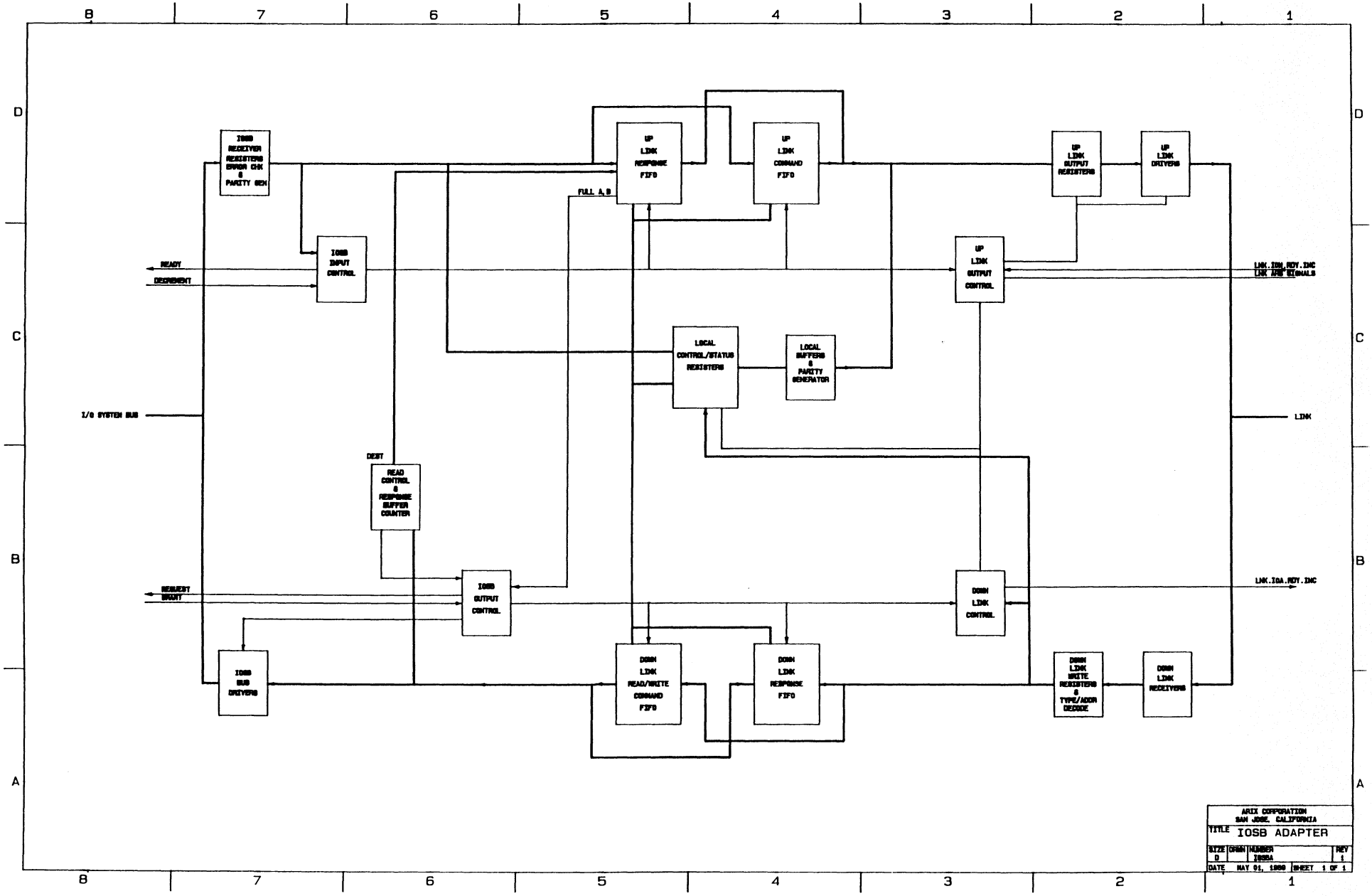
15 IO ADAPTER BOARD ELECTRICAL IMPLEMENTATION DESCRIPTION

The entire design will be implemented using standard MSI, Programmable logic devices, and Arix Associative FIFO gate arrays. The estimated number of IC's per function is as follows:

FUNCTION	NUMBER OF ICS
CSS INTERFACE	100
LINK INTERFACE	25
UPLINK	40
DOWNLINK	40
LOCAL	25
MISCELLANEOUS	50
TOTAL	280

16 BILL OF MATERIALS

Standard IC's (237)	$275
PALs (35)	$ 90
Gate arrays (8)	$144
Miscellaneous	$ 20
PCB,sockets,Mechanical	$280
	$809


IOSB RECEIVER REGISTERS ERROR CHK & PARITY GEN
UP LINK RESPONSE FIFO
UP LINK COMMAND FIFO
UP LINK OUTPUT REGISTERS
UP LINK DRIVERS
FULL A,B
READY
DECREMENT
IOSB INPUT CONTROL
UP LINK OUTPUT CONTROL
LINK.IOA.RDY.INC
LINK IOA SIGNALS
LOCAL CONTROL/STATUS REGISTERS
LOCAL BUFFERS & PARITY GENERATOR
I/O SYSTEM BUS
LINK
DEBT
READ CONTROL & RESPONSE BUFFER COUNTER
REQUEST GRANT
IOSB OUTPUT CONTROL
DOWN LINK CONTROL
LNK.IOA.RDY.INC
IOSB BUS DRIVERS
DOWN LINK READ/WRITE COMMAND FIFO
DOWN LINK RESPONSE FIFO
DOWN LINK WRITE REGISTERS & TYPE/ADDR DECODE
DOWN LINK RECEIVERS
ARIX CORPORATION
SAN JOSE, CALIFORNIA
TITLE IOSB ADAPTER
SIZE D
DRWN
NUMBER 1003A
REV 1
DATE MAY 01, 1990
SHEET 1 OF 1