European Electronic Data Processing—A Report on the Industry and the State-of-the-Art*

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To help assure that the U. S. computer engineer has good visibility on the European scene, I. L. Auerbach was asked to undertake the task of surveying the many computer developments in that part of the world. Engineers will find useful information in this paper, in which several of the most promising technical developments have been identified and described briefly, and the characteristics of most of the computers in operation and in development are summarized.

—*The Guest Editor*

Summary—**Information processing activities in Western Europe are developing at an increasingly rapid pace. Newly created companies and many of the established business machine and electronic firms are entering this burgeoning field. A first-hand tour of major industrial and academic groups in Western Europe reveals important progress in equipment design and manufacturing techniques, as well as significant advanced development work.**

The United States is ahead of Western Europe, due primarily to a greater over-all research and development effort. However, there is no national boundary for creative ideas; European laboratories are developing new techniques and products for the world market, ranging from peripheral equipment to complete information processing systems.

The survey of European activities is presented in three parts: an introduction, details of some important technological developments under way, and a detailed review of the characteristics of European computing systems. The technological developments include fixed high-speed memories, magnetic thin films, random-access memories, pattern recognition, learning machines, hydraulic logic, and problem-oriented languages.

I. Introduction

IN a mere fifteen years the electronic digital computer has risen from a laboratory curiosity to a vital element of present-day civilization. The phenomenal growth of the computer industry in the United States has been the subject of many articles, both technical and popular. But too little attention has been given to the work going on in other countries. Indeed, very basic research and development is being conducted everywhere in the world. It is therefore of inestimable value to keep in focus these activities and recognize the magnitude of the ever-growing field.

While virtually every nation today is engaged in some sort of computer activity, the most significant work being done is found in the United States and Western Europe. Several European countries, notably Great Britain, France, Sweden, The Netherlands and Germany, have been active for many years and have well-established research groups and manufacturing concerns. Other nations entered the field more recently and are aggressively forging ahead in basic research and product development.

In an effort to learn first hand just what the Western Europeans are doing in information processing, the author spent seven weeks touring the continent and Great Britain, visiting virtually every major area of computer activity. Through exhaustive interviews, tours of facilities, and examination of equipment the author has prepared this presentation of the technical state of the art in Western Europe.

II. Technological Developments

All over Western Europe important research is being conducted by both commercial and government organizations in advancing the state of the computer art. Some of the work parallels that being done in the United States and elsewhere, while in other cases European groups are pursuing entirely new ideas. Although not all advanced developments are revealed to an outside observer, the author was fortunate in seeing much original and interesting work in process. The items of particular interest are noted below, categorized by technical subject matter, so that the results of several organizations working in the same area may be grouped together.

Fixed High-Speed Memories

There is very interesting development work in Western Europe in the area of fixed high-speed memories, including both technique developments and application studies. Two techniques are receiving particular attention: wired-core memories, and fixed memories using magnetic rods.

Wired-Core Memories: Wired-core memory techniques, well known but little used in the United States, are extremely popular in Western Europe. Almost every modern European computer uses some form of wired-core storage.

In wired-core storage, a wire is threaded through a core matrix in a pattern which represents stored information. Such memories are characterized by nondestructive readout, with higher speed (under 1 μsec

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switching time is typical) and lower cost than coincident-current memories. Wired-core memories are used to store various fixed or seldom-changed data; *e.g.*, start-up sequences, basic programs for communicating with peripheral equipment, basic subroutines such as standard trigonometric functions, program constants, and, in some cases, entire operating programs. The technique is particularly useful in microprogramming, where the cores control logical gates and the structure of the wired-core matrix defines the logical characteristics of the computer. Industrial control is one of the areas where wired-core techniques have great potential application.

Telefunken in Germany uses E-shaped wired cores in the TR-4, a large-scale, high-speed, solid-state computer. One slot of the E core stores a ONE and the other slot stores a ZERO. A storage capacity of 256 words is achieved with 52 cores and 52 diodes mounted on a single plug-in card threaded with 256 wires. Telefunken claims an access time of 1 μsec with a 30 per cent cost saving over coincident-current systems.

In Holland, N.V. Electrologica uses wired-core storage in the X1 computer. Organized in blocks of 64 words, the storage is used for peripheral equipment subroutines. N.V. Electrologica has automated the assembly of the wired-core matrices with punched paper tape.

Most other European groups are active in wired-core development and application, particularly Elliott Brothers in England who have utilized the technique for both serial and parallel storage in process-control computers.

Fixed Rod Memories: The advantages of wired-core memories are retained and the disadvantage of inflexibility of modification overcome in a new memory development at the University of Manchester in England. Using small magnetic rods inserted in a wire mesh, this 8192-word memory has achieved the highest operating speed of any known memory of equal size being built into a computer anywhere in the world: 0.3 μsec cycle time and 0.15 μsec access time have been achieved in laboratory tests.

The fixed rod memory was developed by Professor T. Kilburn for use in the radically new MUSE computer currently under development. The memory has a capacity of 8192 words of 48 bits each. A smaller version, 256×256, using parts supplied by Manchester, was built at the University of Pisa in Italy and is operating in the C.E.P. computer there.

The fixed rod memory is constructed from a woven mesh of copper wire mounted over a soft plastic. Ferrite rods 1 mm in diameter and 5 mm long are placed in the interstices of the mesh wherever a ONE is to be stored. The woven mesh for a 4096-word memory is 3 feet wide and 8 feet long with $\frac{1}{16}$-inch grid spacing. The mesh, folded in half over the plastic, results in a two-sided frame 3 feet by 4 feet. There are 256×768 loops in the mesh, organized as 256×16 words of 48 bits each.

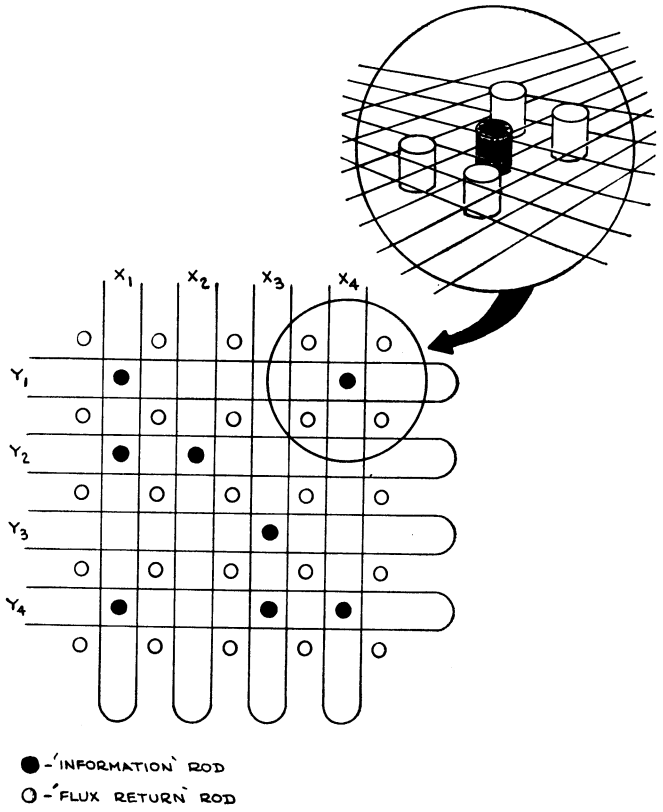

Fig. 1—Kilburn fixed rod memory technique.

The wire mesh is formed into loops (see Fig. 1) by cutting one horizontal and one vertical edge of the mesh. When a ferrite rod is inserted within both a horizontal and vertical loop, it couples these loops and may be detected. To provide a flux return path for the magnetic field and to reduce noise, identical rods are inserted in all of the noncoupled loops.

The memory is organized by switching 48 sense amplifiers to a selected 1-out-of-16 group of 48 loops on the vertical axis. A single driver switched to one of the 256 loops on the horizontal axis provides the interrogation.

Magnetic Thin Films

Research on magnetic thin films is under way in many laboratories throughout Europe. Two of the organizations visited—IBM Zurich, and ICT in England—made some information available about their programs so that a brief review of these programs serves as an indication of the state of the art.

At the IBM Laboratories in Zurich a major program on magnetic thin films is divided between two groups: one engaged in metallurgical methods for depositing and heat-treating ferromagnetic films, and the other concerned with the switching properties of the films and their application in logical devices and memory.

IBM's investigations show that ferromagnetic resonance of a thin film occurs at 1 kMc, which may establish the upper boundary for speed. The possibility of making use of the ferromagnetic resonance in new cir-

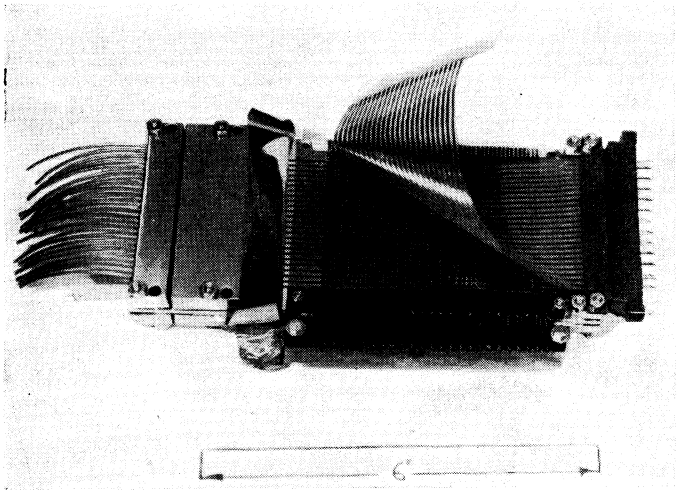

Fig. 2—ICT thin film memory, laboratory model.

cuits is being studied. Experiments have been conducted on nanosecond switching of film 1000 angstroms thick and 1 cm square. Output signals of up to 0.1 volt have been obtained comparable to signal amplitudes derived from small ferrite cores. Memory planes are being tested.

Through microscopic examination of the thin film under polarized light, both the IBM and ICT researchers have been able to observe the domain wall switching and have discovered that the domains "lock up" on impurities.

In England, International Computers and Tabulators Ltd. is active in thin film research. ICT's main emphasis is on improving the reproducibility of the desirable properties of the magnetic thin film, to permit economical manufacture of large-scale memories with cycle times under 100 nanoseconds. Metallurgical research at ICT has produced a new alloy called Gyralloy which is deposited by vacuum evaporation onto an oxidized aluminum substrate. The presence of a conductor so near the film gives a good signal-to-noise ratio and reduces the drive impedance, because magnetic flux cannot penetrate into the conductor in the duration of the selection pulse. ICT claims no harmful damping effect on the magnetic reversal with this arrangement.

An experimental thin film memory assembly built by ICT is shown in Fig. 2. The Gyralloy is deposited on the aluminum substrate in a continuous film—not in spots. An insulating layer is applied over the film; over this are printed circuit copper conductors, which form the read winding. At right angles to the read winding are coils of flat wire, with 10 turns per coil, again at right angles to these coils is a set of conductors embedded in a plastic sheet, for x/y control.

Other European groups engaged in thin film research include Siemens & Halske and the Max Planck Institut fuer Physik in Germany; and Plessey, Mullard Radio Research Laboratory, and the University of Manchester in England.

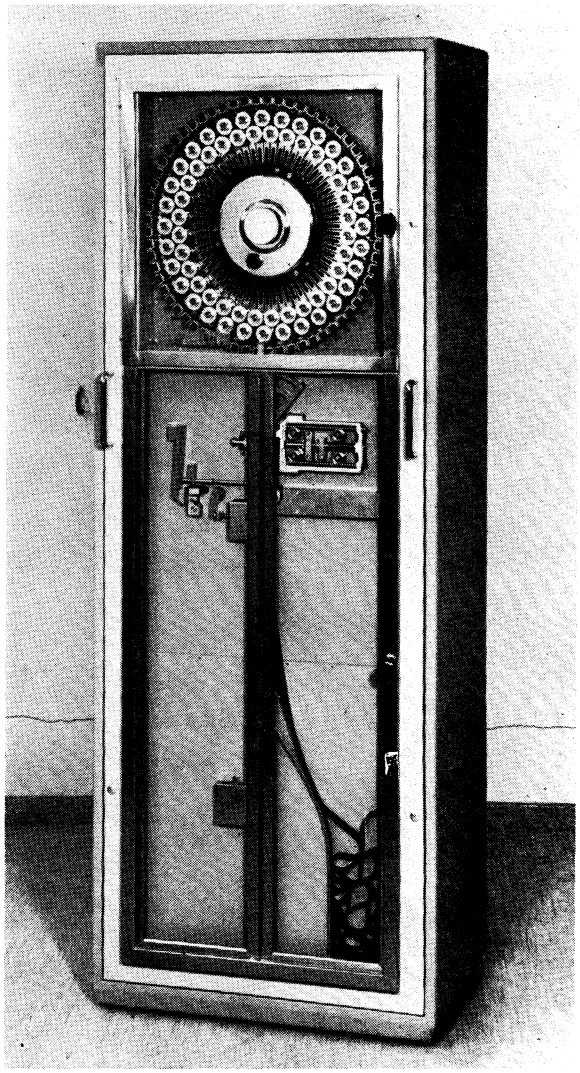

Fig. 3—FACIT ECM 64 Carousel memory.

Random-Access Memories

The problem of providing random access to large quantities of stored data has been attacked many ways in the United States and Europe. Two interesting developments in this area are the Carousel memory developed by Facit in Sweden, and the K-10 memory built by Standard Elektrik Lorenz in Germany.

The Carousel (Fig. 3) permits access to any of over five million stored decimal digits in an average of less than two seconds. It contains 64 small reels of 8-channel magnetic tape mounted in two concentric circles on a wheel. A given reel of tape is read by indexing the wheel so that the selected tape is at the bottom. A weight attached to the end of the tape drops down past an air-gap read/write head to an unwinding bin. Photoelectric sensors control start, stop, and rewind. A fully loaded Carousel wheel can be replaced in about ten seconds.

Standard Elektrik Lorenz' K-10 (Fig. 4) takes a somewhat different approach to the random-access storage problem. It provides a storage capacity equal

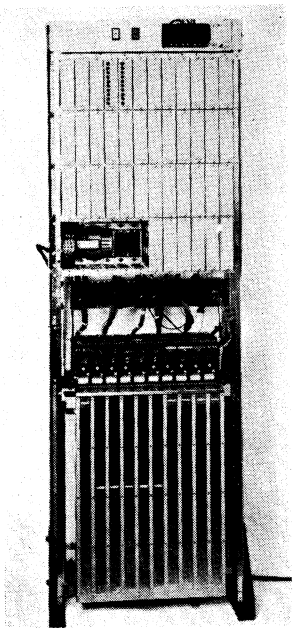

Fig. 4—Standard Elektrik Lorenz K-10 memory.

to that of a standard tape transport with a 1000-meter tape, but with an access time of only 2.5 per cent of a conventional unit. The K-10 has ten bins, each containing 100 meters of tape. Associated with each bin is a read/write head and a drive mechanism. The tapes normally rest with the midpoint over the head, detected photoelectrically. A typical application uses a crossbar switch, four tape control units, and nine K-10's for simultaneous reading or writing on any four of 90 tapes.

Pattern Recognition

The most outstanding development work observed in character recognition in Europe is being conducted at the Technische Hochschule in Karlsruhe, Germany. Solartron in England has produced commercial equipment for character reading. BULL in France, EMI in England, and three German manufacturers are also working in equipment development.

The Karlsruhe approach, sponsored by the German Post Office, is a unique combination of analog and digital techniques. The initial input of a character is straightforward; a flying spot is used to scan the pattern at a rate of 3000 characters per second and the output signal wave is converted to bits indicating black or white areas. The result of a scan is 200 bits (20 vertical by 10 horizontal). A two-dimensional 200-bit shift register stores this image of the original pattern as it develops. The system is currently limited to 14 characters; continued development is expected to increase this number.

The first phase of processing centers the character image. First the character image is transferred from the shift register to an array of 200 flip-flops which in turn feed a resistor matrix. The resistors are so interconnected that there are four output currents: left side, right side, top and bottom. The character is scanned and repeatedly reloaded into the flip-flop array from the shift register with each vertical synchronizing pulse. The character effectively moves from left to right across the array until the left and right currents are equal. This is defined as horizontal centering.

The flip-flops are cross-connected so that vertical shifting of the character image is possible. Then the character is positioned so that the top and bottom currents are equal. This is defined as vertical centering. The horizontal and vertical "centering" places each character image in its unique standard position.

The next phase of processing, which has been thoroughly analyzed but only partially implemented in hardware, is the extraction of salient features from the pattern. Since the currents flowing in the resistors represent the "potential field" (Fig. 5) of the character stored, it is possible to deduce the key shape features of the character from properties of this potential field. For a simple example, a node with a maximum current inflow indicates the end of a line or an isolated point.

An analysis of first and second differentials of current flow at a point indicates the location and curvature of a line. The sign of the first differential indicates whether the character lies to the right or left of the test point. The sign of the second differential indicates whether the line is straight, curved away from or curved towards the test point (see Fig. 6). Note that these currents and differentials are analog, not digital phenomena.

To test the first and second differentials, some novel circuits have been devised. The most novel test uses a differential transformer technique. Leads from adjacent nodes of the resistor matrix are wound around ferrite cores with proper numbers of turns and direction. There are also sense and interrogate windings on the core.

The core is saturated in one direction or the other depending on the sign of the second differential. An interrogate pulse only produces an output for a positive second differential.

The figures to be recognized are described in terms of the location of major straight lines, the direction of curvature in the upper, middle and lower portion of the figure, and the location of line terminals. The present recognition criteria were selected experimentally and wired into the equipment.

Solartron's commercial development is the ERA (Electronic Reading Automation), which converts printed characters to punched cards at the rate of up to 240 characters per second. The accuracy claimed is better than one in 10,000 rejects and one in 1,000,000 errors. Four units represent the necessary equipment for recognition: the scanner, memory, logic, and document handler. The latter provides only for cash register tally rolls, but developments are in process for handling separate documents. One of the Solartron ERA systems

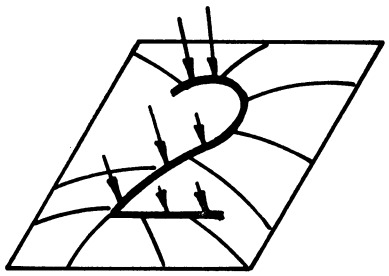

Fig. 5—Two-dimensional potential field for the character "2."

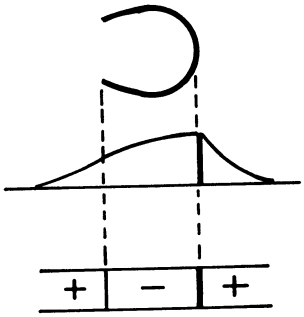

Fig. 6—Determining character shape by analysis of second differential.

was observed undergoing final factory tests in July, 1960.

The ERA is designed to read numerals (0–11), plus some alphabet characters and special signs. (Models are under development for sensing additional characters.) The sensor uses a flying-spot scanner and a photoelectric pickup. Each character is prescanned twice. The first prescan establishes peak white and black levels which are used to clamp the limits to a narrower range than would otherwise be necessary, thus compensating for smudging and other irregularities. The second prescan establishes x-y limits to center the character; then a final scan transfers the character information into ferrite core storage. Each character has its own criteria stored within the machine; both acceptance and exclusion criteria are used for identification.

Three of the larger German computer manufacturers (Telefunken, Siemens, and Standard Elektrik Lorenz) have been also working on character recognition equipment, in an effort to receive contracts for equipment to mechanize the German Post Check system and the German Post Office letter sorting problem. Telefunken has a pilot model reader for American Banking Association characters under test.

Electric and Musical Industries (EMI) in England is developing a character reader named FRED (Figure Reading Electronic Device).

Machine Learning

Exploratory work in learning machines, most of it in the early stages, is being pursued by several European groups, notably the Technische Hochschulen in Vienna, Austria, and Karlsruhe, Germany, and Manchester University and Solartron in England. Unfortunately, little information is available on these activities, other than an indication of the general approach each group is taking.

In Vienna, programs are being developed for the MAILUEFTERL computer to create a new type of conditioned reflex automaton. An improved model of Shannon's maze runner has also been developed, with the ability to detect circle-ways, dissolving them into parts of the solution.

The Karlsruhe group has devoted much study to the philosophy of learning machines and has produced excellent articles summarizing the accomplishments in the field. Their work, like that in Vienna, is concerned primarily with conditioned reflexes and is closely related to their developments in character recognition. One approach to the conditioned reflex problem uses the multistep characteristic of ferrite cores in a matrix, with the sensors connected to one axis and the reactors to the other. By repeatedly exposing the sensors to the situation, a conditioned reflex is built up so that, when the reactors are interrogated, a learning-type reaction is obtained. In addition to character recognition, applications of this technique are seen in information retrieval and automatic speech recognition.

At Manchester University, one problem under investigation involves control of a configuration of water tanks in which some drain into others, some drain into a sink, and some are filled from an external source. All flows are controlled by valves, some of which operate randomly, while others are controlled by a learning machine. The machine is told only which tanks are too full or too empty and must try to maintain the proper levels without knowing how the tanks are interconnected or what the valves control. Such a machine may find application in chemical processing.

Another learning problem under study at Manchester involves the memory organization of the MUSE (ATLAS) computer. To achieve, in effect, a huge fast-access memory, MUSE combines a magnetic core memory and a drum memory such that information is transferred between the memories without direction from the programmer. The computer's task is to keep those data which are frequently requested in the immediate-access core memory, with less used data in the drum. When a given block of information is requested, it is read out immediately if in core storage, or transferred from the drum in exchange for an unused block in the core memory. Learning criteria are being developed so the computer can maintain the best compromise of storage locations at all times.

Solartron's association with Rheem Manufacturing Company in the United States has resulted in the development of EUCRATES, an experimental teaching and learning machine. Learning is accomplished by storing the number of hits in correlating a keyboard and a selected light. As the number of hits is increased, the "pupil" part of EUCRATES "learns" the correlation,

and eventually selects the right key. To simulate human behavior, a "forgettery" control is introduced that requires continuous enhancement. The "pupil" learns under control of the "teacher" part of the equipment, or on a trial-and-error basis without outside assistance.

Solartron has also developed a teaching machine, the SAKI (Solartron Automatic Keyboard Instructor) which trains operators in the use of punch-card equipment. It consists of a keyboard, a power supply, and a control unit. On the latter are two indicators, one corresponding to the location of the keys, and the other a card with rows of random numbers and/or letters. In operation, a light shines behind each of the characters on the card, in sequence. The corresponding keyboard indicator is also illuminated, telling the trainee which key to depress. As the proper buttons are depressed, the keyboard indicators grow dimmer and the rate is increased. If errors are made, the rate is reduced and the indicators gradually come back on again.

Hydraulic Logic

One of the most interesting and unusual developments in Europe is the work being done at IBM's Zurich laboratory on hydraulic logic. This is exploratory work aimed at establishing basic techniques rather than building hardware.

This application of hydraulic techniques is quite different from the conventional usage where high power is used to move heavy external loads. In hydraulic logic there is no external load, thus permitting lower pressures and much smaller elements. Miniaturization also permits higher speed, and hydraulic elements compete favorably with relays in this area of performance. Laboratory models of a free-running multivibrator have been operated at 300 cps, and calculations indicate that, with care, 2000 cps operation can be obtained.

Although hydraulic elements can take many forms, the devices built by IBM Zurich use "spool" valves, shown in both schematic and symbolic form in Fig. 7. In this simple building block, three inputs (A, M, and N) and one output (X) are provided. Logical signals in the form of high and low pressure (corresponding to the voltage no-voltage levels in electronic binary logic) are applied to the inputs. A static medium pressure is applied to m. Thus the pressure at A determines the position of the valve, which in turn defines, together with the input at M or N, the pressure at X. If high pressure is regarded as logical ONE and low pressure as logical ZERO, the performance is described as

$$X = MA' + NA.$$

The logical capability of the hydraulic element is thus greater than that of a single transistor.

By providing a feedback path from X to A, a bistable element is created. These simple configurations—the gate and the bistable device—are the basis for all other hydraulic logic elements. Gating networks, shift registers, counters, matrices, and multivibrators have been built and successfully operated. Fig. 8 shows the logical diagram of a scale-of-two counter and a working model of this unit. Fig. 9 shows two multivibrators, with bores of 5 mm and 1 mm, respectively. The larger models are executed in clear plastic to permit direct visual observation of operation using stroboscopes and high-speed photography.

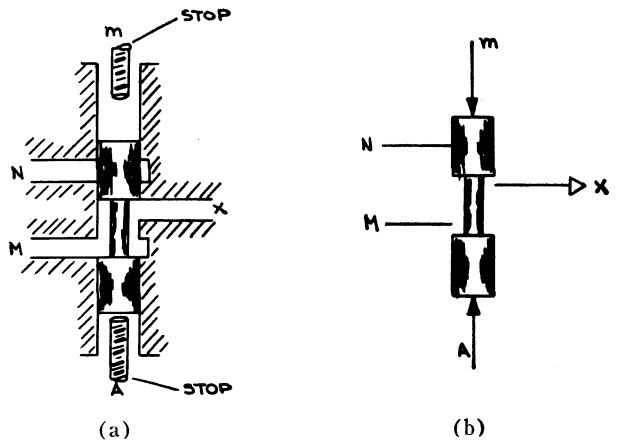

Fig. 7—Basic hydraulic logic element. (a) Schematic, (b) Symbolic.

Hydraulic logic presents many serious design problems. In many respects the elements behave like their electronic counterparts, and problems such as transient peaks when a current in an inductive circuit is suddenly stopped are encountered. In addition, many physical effects relating to fluid flow influence the design. Inertia is especially critical in determining response time, and channel (*i.e.*, conductor) lengths must be equal for two parallel-fed elements to operate synchronously.

Despite these problems, the IBM Zurich group has made an impressive start toward realization of practical control and decisioning equipment using hydraulic elements exclusively. They admit that a hydraulic computer is in the far distant future, but point to more immediate potential applications, such as process control and machine tool control. They feel that the high reliability and long life of hydraulic components make the technique especially attractive in such applications.

Other Developments

In addition to the major development efforts described above, several other interesting programs were observed in both computer applications and hardware techniques. In the former area, the work in problem-oriented computer languages is worthy of special mention.

Development of computer languages for simplifying programming is centered around ALGOL (Algorithmic Programming Language). The idea for ALGOL originated in Germany several years ago and is being developed by a cooperative group representing West German and Swiss technical institutes. A preliminary

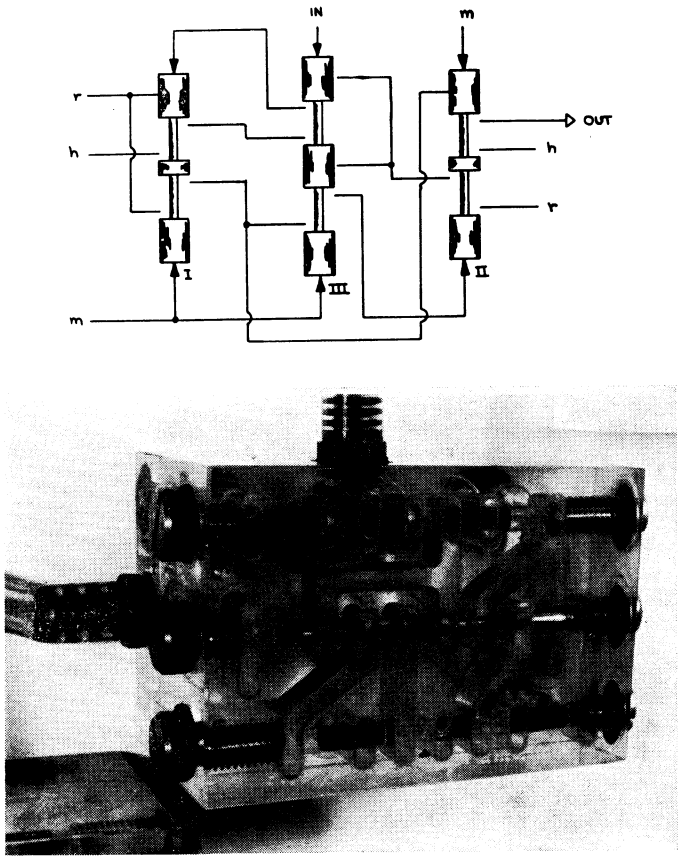

Fig. 8—Hydraulic scale-of-two counter.

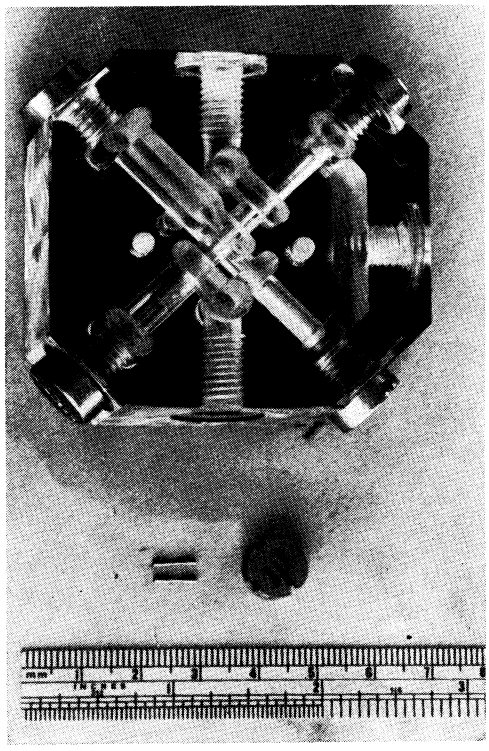

Fig. 9—Hydraulic multivibrators, 1-mm and 5-mm bores.

ALGOL language proposal was approved by GAMM, a German technical society, in 1957. ALGOL conferences in 1958 and 1960 saw the formation of a unified effort to establish a universal computer language. Currently, most computer groups in Europe are working on or have completed ALGOL-60 translators for their computers. Universities are teaching the language and are reporting very good results.

Elliott Brothers have observed an interesting phenomenon that can be used for nondestructive storage with nickel delay lines. A bit of information is stored in a nickel wire by discharging a capacitor through the wire at a fixed point. Bits may be placed every $\frac{1}{2}$ to 1 centimeter along the wire, equivalent to approximately one-microsecond intervals. The discharge applies a permanently stored circular magnetization to the wire. Passing a current pulse through the wire sets up an acoustic wave from each bit stored, so that an acoustic coil transducer mounted on the wire past the current output will receive a sequence of acoustic signals corresponding to the stored discharges in the wire.

III. Computers in Europe

The chart on pages 340–347 presents a comprehensive summary of Western European computers. Included are all current or recent computing systems on which information is available. The chart is mainly devoted to commercially available machines, but a few of the more important one-of-a-kind computers, as well as some systems still in development, are included for reference. The data in the chart were compiled from manufacturers' literature and, in most cases, through direct communication with the manufacturers.

The indexes on which the evaluation of computing systems is based were chosen in the belief that they achieve the most meaningful presentation of information. To clarify the indexes and define the terms used, Table I, on page 339, explains the column headings.

To provide a frame of reference for the computer comparison, the following paragraphs present brief notes on each company and computer represented in the chart.

Great Britain

Computer activity in Great Britain is second only to that in the United States. Several large manufacturers are active in commercial development and production, and British universities continue to play an important role in advanced computer development.

Leo Computers Ltd: Leo Computers Ltd. is a wholly owned subsidiary of J. Lyons and Company Ltd. of London, a pioneer in the application of computers in business. Leo Computers' first effort was LEO I, the oldest computer in the world still in operation. LEO II was introduced in 1957 and was followed by LEO III, an-

nounced in the summer of 1960. This transistorized parallel computer has three distinctive features: basic actions are controlled by microprograms; the computer can be microcoded to operate as a multiradix computer; and two or more different programs can be operated simultaneously under control of a master program.

Ferranti Ltd.: Ferranti Ltd. was one of the earliest companies in Great Britain to enter the computer field, beginning with the MARK I development in collaboration with the University of Manchester in 1951. Since then Ferranti has produced a large family of electronic digital computers, and the company is today at the forefront of technological developments and scientific computation in England.

The ATLAS computer, jointly developed with the University of Manchester, is the most advanced computer being developed in Europe. It features an extremely sophisticated organization and several unusual hardware techniques, including the fixed rod memory described earlier. Ferranti is also building advanced process control computers.

Elliott Brothers: Elliott Brothers, a division of Elliott Automation, entered the general-purpose computer field in the early 1950's, producing several serial scientific machines. The first business data processing machine made by Elliott was the 405 computer, using tube/diode logic, a magnetic tape memory and a 16,000-word magnetic disk memory.

In 1958 Elliott introduced the partly transistorized 802 computer, followed almost immediately by the completely transistorized 803, which is being promoted as a small-scale scientific computer, a small-scale business data processor, or as the computer unit of an on-line industrial data processing system. Elliott recently announced the 503, a large high-speed scientific computer.

EMI Electronics Ltd.: EMI Electronics Ltd., known for its work in analog control systems, entered the general-purpose electronic digital computer field with the EMIDEC 1100, a transistor/magnetic core computer. The 1100 is a two-address binary parallel machine with magnetic core and drum storage.

In 1955 the National Research Development Corporation contracted with EMI Electronics Ltd. to design and develop an advanced data processing system. This system, the EMIDEC 2400, is a very large high-speed data processor comparable to the IBM 7080, with a sophisticated organization of on-line and off-line peripheral equipment. Special features of the 2400 include automatic interunit switching of peripheral units, with an interrupt facility to permit breaking into the normal computing routine for peripheral unit control; elaborate error-checking and time-sharing of computing and input-output functions.

International Computers and Tabulators Ltd. (ICT): ICT was formed in 1959 from the British Tabulating Machine Company, Ltd. (Hollerith) and Powers-Samas Accounting Machines Ltd. Later in 1959, ICT and the General Electric Company Ltd. formed Computer Developments Ltd. as a jointly owned design and coordinating group. The 1301 computer, the first outgrowth of this united effort, is a file processor for medium-size companies. A fully transistor 1 Mc binary-coded-decimal serial-parallel machine, the 1301 has a magnetic core and drum memory.

Standard Telephones and Cables Ltd. (STC): STC's entry into electronic data processing came in 1958, when the first STANTEC ZEBRA was produced, using a logical design developed by the Netherlands Postal and Communications Services. The ZEBRA's unique features include the use of large etched circuit boards for interconnections between the vacuum-tube plug-in modules, extensive use of microprogramming, and the use of all "short" storage registers as instruction modifiers. In addition to the normal machine code, a "simple code" has been designed especially for the unskilled user.

STC is producing the STANTEC COMPUTING SYSTEM, the heart of which is a transistorized and improved version of the STANTEC ZEBRA. In the STANTEC COMPUTING SYSTEM, the magnetic drum is supplemented with ferrite core fast-access storage. Among the peripheral equipment available with the system is the Standard Elektrik Lorenz K-10 Magnetic Tape Unit, described earlier.

English Electric Company Ltd.: In 1947 the National Physical Laboratory at Teddington, England, formed an Electronics Section to undertake the design and construction of an electronic digital computer, designated ACE. In 1952 English Electric Company was given the task of designing an engineered model of the ACE design, with expanded capability. The result was DEUCE (Digital Electronic Universal Computing Engine), a vacuum-tube serial machine with mercury delay storage and magnetic drum back-up storage.

English Electric Company currently has an agreement with RCA to produce a transistorized medium-size data processing system patterned after the RCA 501. The English version, designated the KDP10, is physically and functionally similar to the RCA system and is not included in the chart.

France

Computer activity in France is proceeding at a moderate level, concentrated primarily in a few large, active firms. There is considerable potential for France to continue to be the leading producer of data processing equipment on the Continent, but it is clear that in the future there will be much more serious competition from other countries.

Compagnie des Machines BULL: BULL is the largest data processing manufacturing organization in Europe and ranks among the top four companies in the world. Its most important data processing equipments are the GAMMA 3 and GAMMA 60 computers. The former is a small-scale computer introduced in 1952. When fully equipped, the GAMMA 3 is similar in size to the IBM 650.

The GAMMA 60, BULL's entry into the large-scale solid-state data processing system market, is an advanced machine featuring simultaneous independent processing of several unrelated problems. Its internal structure is based on the concept of autonomous operation of individual elements under control of a central unit which dispatches data and instructions to the elements and serves as a buffer storage for transferred data.

Société D'Electronique et D'Automatisme (SEA): Primarily involved in the design and manufacture of analog computers for the military, SEA expanded into flight simulators and machine tool control. During the past four years the company has produced a series of digital computers for military, scientific and business applications. The computers are used almost entirely within France.

The CAB 500 is a small serial digital scientific computer using magnetic logic elements and transistors, with magnetic drum storage. The SEA 3000 system is a medium-scale data processor designed for scientific and commercial applications. The heart of the system is the SEA 3030 computer, a vacuum-tube, binary computer with ferrite core and drum memory. Successor to the 3000 is the SEA 3900, a fully transistor serial-parallel 2 Mc data processor also intended for general commercial applications. A modified version is available for scientific calculations.

Société Nouvelle D'Electronique (SNE): SNE's parallel binary computer, the KL901, is designed for scientific, statistical, and accounting applications. The vacuum-tube machine uses magnetic-tape and ferrite-core memories. The tape units have 36 tracks, allowing an entire word to be read in parallel.

Italy

The most active computer development work currently being done in Italy is at the University of Pisa and the Olivetti Laboratories near Milan. These two groups are working on both new computers and application problems.

University of Pisa (Centro di Studi sulle Calcolatrici Elettroniche): The University of Pisa's Computer Center is engaged in logical design, computer programming, numerical analysis, and electronic design and construction. The computer development work is among the most advanced observed in Europe. The University's computer, CEP (Calcolatrice Elettronica Pisa), is a 36-bit parallel binary computer with magnetic core and drum memory. The CEP has several interesting and advanced features, including fixed high-speed rod memory for storing microprograms, identical in concept to the fixed memory being built at the University of Manchester (described earlier); and an order structure embodying double address modifiers.

Olivetti: Olivetti is the only major commercial Italian manufacturing company extensively working on data processing equipment. The Olivetti computer product line includes two electronic systems: the ELEA 9003 and the ELEA 6001. The computers are both transistor machines with variable word length. The 9003 is a large system for business applications, while the 6001 is a scientific computer. Both computers operate on a decimal character-by-character basis with memory access time of ten microseconds per character and use threaded-core type microprogramming.

West Germany

The computer industry in Western Germany is quite active on many fronts, despite the country's relatively late start in the field. In the early 1950's the only significant work on computers was being done at the universities and research institutes; not until the past few years did the commercial companies become involved.

Siemens & Halske AG: The SIEMENS 2002 is a transistorized decimal machine, with magnetic-core and drum storage. Input-output equipment includes paper tape, punched card, magnetic tape printer and cathode-ray tube. The machine is designed for both scientific and commercial applications and sales have split evenly between these two uses.

Telefunken: Telefunken specializes in communications, radar, computers and other electronic fields. The Telefunken TR-4, a large-scale transistorized high-speed computer designed for both business and scientific applications, is the fastest computer being built in Germany. It uses two novel fixed memories: a wired ferrite core array, described earlier, and a memory used for microprogramming, consisting of double-sided printed-circuit cards, with diodes inserted wherever connections are desired.

Standard Elektrik Lorenz AG: Standard Elektrik Lorenz is an affiliate of the International Telephone and Telegraph Company. The company's data processing activities include the development of special-purpose systems from elements manufactured by various members of the ITT family. Standard Elektrik Lorenz has developed a transistor general-purpose computer, the ER-56, which uses the K-10 tape unit, described earlier. The ER-56 contains a switching network which can connect the various units in any arrangement desired.

Zuse K.-G.: Zuse started developing computers in 1947 and produced the Z 4, a relay computer, in 1950. An-

TABLE I

DEFINITION OF EUROPEAN COMPUTER CHART TERMINOLOGY

Term	Definition
Manufacturer and Country	This is the actual manufacturing concern. In some cases the agency responsible for the design or sales of the machine, may be shown in parentheses. Intra-company divisions are shown where appropriate. The country is where the computer is actually built.
Computer Name	This is the name the computer is usually called. For numbered computers, the manufacturer's abbreviation is usually shown along with the number.
Availability—Number on Order	This is the total number of machines for which firm orders have been received, but which have not been installed. The figure is current as of September, 1960.
Availability—Number Installed	This, is the number of completed machines actually installed and operating as of September, 1960.
Availability—Date of First Installation	This is the actual (or anticipated) date of first installation.
Technique—Circuits	Transistor, transistor-diode, transistor-core, vacuum tube.
Word Length	The number of bits (including sign) or digits used in a normal add operation. Parity bits are not included in the count. In variable word length machines, this is the number of digits or characters retrieved from memory on each cycle.
Addresses per Instruction/Instructions per Word	The numerator is the number of full addresses in the instruction used to specify operands. In those machines where an address is included in each instruction to specify the location of the next instruction, the form $x+1$ is used for an x address machine.
Number of Operations: Decoded/Possible	The numerator is the number of operation codes with assigned functions. The denominator is the number of combinations possible of the bits (or digits) used to specify the operation code.
Operation Times	All operation times are in microseconds. The times include memory access for the instruction and the operands. "Subroutine" indicates that a single instruction cannot perform the operation.
Storage—Cycle Time	The minimum time between two consecutive accesses to the same storage unit. This involves the read and restore cycle on core memories.
Storage—Access-Time	The average time to retrieve one word. This is the read cycle only on core memories, and half the time of a drum revolution on drum memories.
Storage—Data Unit Accessed	This is the amount of information transferred out on one call to the memory. This is usually a word, but sometimes it is a character (variable word length machines) on a block of many words (back up drum and memories).
On-Line Input-Output—Speed	The speed of various units is rated as follows: Punch card equipment: Cards per minute. Paper tape equipment: Frames per second. Line printers: Lines per minute. Other units: Characters per second.
On-Line Input-Output—Number of Units	This is the maximum number of units which may be attached to a production model computer without modifying the equipment.
Magnetic Tape—Characters per Second	Alphanumeric character or six-bit groups transferred per second. This is the maximum transfer rate within a block.
Magnetic Tape—Bits per Inch/Inches per Second	Bits per inch on each track.
Magnetic Tape—Number of Units Operating/Total Tape Units	The numerator refers to the number of tape drives which may be reading (or writing) data into the central computer simultaneously. Rewinding, searching or other independent operations are not considered.
Special Features	Any important facts about the computer which are not shown elsewhere on the chart.

EUROPEAN COMPUTERS

No.	Manufacturer and Country	Computer Name	Availability: Number On Order	Availability: Number Installed	Availability: Date of First Installation	Technique: Circuits	Technique: Clock Rate	General Machine Features: Word Length	General Machine Features: Addresses per Instruction / Instructions per Word	General Machine Features: Number of Operations Decoded / Possible	General Machine Features: Number of Index Registers	General Machine Features: Indirect Addressing	General Machine Features: Partial and Multiple Word Operations	General Machine Features: Internal Checking	Operation Times (Micro-Seconds) (Including Memory Accesses): Addition (Fixed / Floating)	Multiply (Fixed / Floating)	Control Transfer (Min. / Max.)	Shift Operations (1 Place / Average)
1	Leo Computers Ltd. Great Britain	LEO III	3	0	1961	Transistor Diode	INA	42 Bits	1 / 2	110 / 140	Up to 12	No	Half Word Operations	Parity	44 / 200–450	300–700 / 600–900	30 / 49	56 / 88
2	Ferranti Ltd. Great Britain	PEGASUS	10	28	1956	Vacuum Tube	333 kc	39 Bits	1 / 2	62 / 64	7	No	Double Word	Parity	300 / Subroutine	1900 / Subroutine	300 / 300	425 / 2750
3	Ferranti Ltd. Great Britain	MERCURY	3	19	1957	Vacuum Tube	1000 kc	10-20-40 Bits	1 / 2	70 / 128	7	No	Double Word	Parity	60 / 180	Subroutine / 300	60 / 60	60 / 300
4	Ferranti Ltd. Great Britain	PERSEUS	0	2	1958	Vacuum Tube	333 kc	72 Bits	1 / 3	63 / 64	7	No	Both	Parity and Complete Arithmetic Check	234 / Subroutine	780 / Subroutine	234 / 3744	234 / 4680
5	Ferranti Ltd. Great Britain	SIRIUS	2	1	1959	Transistor Core	500 kc	10 Decimal Digits	1 / 1	60 / 100	9	No	No	Parity	240 / Subroutine	4000–16,000 / Subroutine	240 / 4000	240 / 1200
6	Ferranti Ltd. Great Britain	ARGUS	0	1	1960	Transistor Diode	500 kc	12 Bits	1 / 1	54 / 64	7	No	Double Word	Parity	20 / Subroutine	100 / Subroutine	20 / 20	20 / 20
7	Ferranti Ltd. Great Britain	ORION	9	0	1961	Transistor Core	500 kc	48 Bits	3 / 1	114 / 128	64	Yes	Both	Parity	36–68 / 60–80	64–184 / 140–160	36 / 68	4 / 48
8	Ferranti Ltd. Great Britain	APOLLO	1	0	1961	Transistor Diode	500 kc	24 Bits	1 / 1	80 / 128	3	No	No	Parity	6 / Subroutine	60 / Subroutine	6 / 12	8 / 30
9	Ferranti Ltd. and Manchester University Great Britain	MUSE (ATLAS)	1	0	1961	Transistor Diode	INA	48 Bits	1 / 1	400 Anticipated / 1024	125	No	Both	Parity	1.1 / 1.1	4 / 4	1 / 2	1 / 12
10	Elliott Brothers Great Britain	803	18	5	1959	Transistor	166.5 kc	39 Bits	1 / 2	60 / 64	4096	No	No	Parity	720 / 720	29,560 / 9360	720 / 720	1440 / 15,480
11	Elliott Brothers Great Britain	503	0	0	1962	Transistor	INA	39 Bits	1 / 2	INA / 64	4096	No	INA	Parity	8 / 8–15	18–28 / 15–25	4	INA

No.	Storage: Type of Storage	Storage: Number of Words: Minimum System	Storage: Number of Words: Maximum System	Storage: Number of Words: Module Size	Storage: Word Time μsec.	Storage: Access Time μsec.	Storage: Data Unit Accessed	On-Line Input-Output: Type of Unit	On-Line Input-Output: Manufacturer	On-Line Input-Output: Speed	On-Line Input-Output: Number of Units	Magnetic Tape: Manufacturer	Magnetic Tape: Char. per Second	Magnetic Tape: Bits/Inch / Inches/Sec.	Magnetic Tape: Number Operating / Total Tape Units	Special Features	Computer Name
1	Core	1024	32,768	4096	INA	7	Word or Half Word	Tape Reader	Elliott	1000 FPS	32	Ampex (1")	90,000	300 / 150	3 / 24	The computer will generate output layout automatically. A single instruction will follow a table of addresses and editing controls to a perfect output line.	LEO III
								Tape Punch	Teletype	110 FPS	48						
								Card Reader	ICT	600 CPM	16						
								Card Punch	IBM/ CT	250/100 CPM	32						
								Printer	Analex	850 LPM	16	Ampex (½")	45,000	300 / 150	4 / 32		
									ICT	600 LPM							
									IBM	150 LPM							
2	Nickel Delay Line	55	55	—	126	0	Word	Tape Reader	Ferranti	300 FPS	2	Burroughs or Decca	9,250	123 / 75	2 / 10	7 Accumulators	PEGASUS
								Tape Punch	Teletype	60 FPS	1						
	Drum	7168	7168	—	126	8000	Word or 8 Words	Card Reader	Power Samas	200 CPM	1						
								Card Punch	Power Samas	100 CPM	1						
3	Core	1024	1024	—	10	2	Word	Tape Reader	Ferranti	300 FPS	2	Burroughs	15,000	266 / 60	2 / 8	Division by subroutine only.	MERCURY
								Tape Punch	Creed	33 FPS	1						
	Drum	8192	16,384	4096	20	10,000	32 Words	7 Others Optional									
4	Nickel Delay Line	1024	1024	—	234	234	Word	Tape Reader	Ferranti	200 FPS	2	Burroughs	9,250	123 / 75	4 / 16	Variable radix arithmetic operations	PERSEUS
								Card Reader	Power Samas	300 CPM	1						
								Teleprinter	Creed	10 CPS	1						
5	Nickel Delay Line	1000	10,000	1000	80	4000	Word	Tape Reader	Ferranti	300 FPS	10	Magnetic Tape Available				—	SIRIUS
								Tape Punch	Teletype	60 FPS	10						
6	Core	1024	3072	1024	20	2	Word	Custom Specified (Includes Analog-Digital Converters)				Custom Specified				Process control machine with peg board instructions	ARGUS
	Drum	0	50,000	50,000	4	12,000	Track										
7	Core	4096	16,384	4096	12	6	Word	Card Read	ICT	600 CPM	No Limit	Ampex FR 300	90,000	375 / 120	4 / 16	—	ORION
								Card Punch	ICT	100 CPM							
								Printer	ICT	600 LPM							
									BULL	150 LPM							
									Rank	3000 LPM							
	Drum	16,384	16,777,216	16,384	200	12,000	Variable	Tape Punch	Creed	300 FPS							
								Tape Reader	Ferranti	1000 FPS							
8	Core	8000	32,000	4000	6	2	Word	Custom Specified (Includes Analog-Digital Converters)				Custom Specified				Primarily for air traffic control	APOLLO
9	Core	8192	262,144[a]	4096	2	0.5	Word	Custom Specified			256 Total	Ampex	90,000	375 / 120	8 / 32	Automatic drum-core data transfers. Fixed ferrite slug memory for control operations	MUSE (ATLAS)
	Drum	0	1,048,576[a]	24,576	4	6000	512 Words										
10	Core	4096	8192	4096	INA	INA	Word	Tape Reader	Elliott	140 FPS	1	No Magnetic Tape				Serial Computer	803
								Tape Punch	Creed	25 FPS	1						
								Card Reader	Elliott	300 CPM	1						
								Card Punch	IBM	100 CPM	1						
								35 mm mag. Film	Elliott	1.44 msec per Word	1						
								Analog-Digital Converters									
11	Core	4096	8192	4096	4	INA	Word	Tape Reader	Elliott	1000 FPS	Multiple	Potter	45,000	INA	INA	Programs compatible with 803	503
								Tape Punch	Teletype	100 FPS	Multiple						
								Card Reader	Elliott	400 CPM	Multiple						
								Card Punch	IBM	100 CPM	Multiple						
								Printer	INA	900 LPM	Multiple						

INA—Information not available

[a] *Maximum internal memory addressing capacity is 1,048,576 words.*

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EUROPEAN COMPUTERS (*Cont'd*)

No.	Manufacturer and Country	Computer Name	Availability: Number On Order	Availability: Number Installed	Availability: Date of First Installation	Technique: Circuits	Technique: Clock Rate	General Machine Features: Word Length	General Machine Features: Addresses per Instruction / Instructions per Word	General Machine Features: Number of Operations Decoded / Possible	General Machine Features: Number of Index Registers	General Machine Features: Indirect Addressing	General Machine Features: Partial and Multiple Word Operations	General Machine Features: Internal Checking	Operation Times (Micro-Seconds) (Including Memory Accesses): Addition (Fixed / Floating)	Multiply (Fixed / Floating)	Control Transfer (Min. / Max.)	Shift Operation (1 Place / Average)
12	EMI Electronics Ltd. Great Britain	EMIDEC 1100	15	4	1960	Transistor	100 kc	36 Bits	2 / 1	30 / 32	7	No	Double Word Addition	None	140 / Subroutine	1260 / Subroutine	125 / 225	170 / 340
13	EMI Electronics Ltd. Great Britain	EMIDEC 2400	3	0	1961	Transistor Diode	1000 kc	36 Bits	2 / 1	57 / 64	64	No	Multiword Transfers	Parity	32 / Subroutine	130 / Subroutine	16 / 30	32 / 60
14	ICT Great Britain	ICT 1200 ICT 1201 ICT 1202	21	57	1955	Vacuum Tube	40 kc	40 Bits	1+1 / 1	38 / 64	0	No	Both	No	2500 / Subroutine	20,000 / Subroutine	1250 / 20,000	2500 / 2500
15	Computer Development Ltd. (ICT & GEC) Great Britain	ICT 1301	25	0	1961	Transistor Diode	1000 kc	12 Decimal or Sterling Digits Incl. Sign	1 / 2	51 / 100	0	No	No	2 Parity Bits per Word Check Sum on Drum	27 / Subroutine	2040 / Subroutine	12 / 12	23 / 23
16	Standard Telephones and Cables Great Britain	STAN-TEC ZEBRA	6	32	1957	Vacuum Tube	100 kc	33 Bits	1 / 1	Micro Programmed / 2^{15}	12	No	Multiple Word Operations	Parity	312 / Subroutine	11,000 / Subroutine	INA	INA
17	Standard Telephones and Cables Great Britain	STAN-TEC SYSTEM	10	0	1960	Transistor	128 kc	33 Bits	1 / 1	Micro Programmed / 2^{15}	12	No	Multiple Word Operations	Parity	312 / Subroutine	624 / Subroutine	INA	INA
18	English Electric Great Britain	DEUCE[a]	2	30	1955	Vacuum Tube	1000 kc	32 Bits	2+1 / 1	Not Defined	0	No	Many Double Word Operations	No	64 / Subroutine	2080 / Subroutine	64 / 96	64 / 544
19	English Electric Great Britain	KDF-9	INA	0	1962	Transistor Core Diode	2000 kc	48 Bits	0 or 1 / 2 to 6	292 / INA	16	Yes	Double Word	INA	1 / 7 From Special Working Store	14 / 14	INA	2.5 / 5
20	Compagnie des Machines BULL France	GAMMA 3 ET	25	88	1956	Vacuum Tube-Diode	280 kc	12 Digits (Binary Commands)	1 / 3	INA	0	No	Variable Word Length Up To 12 Digits	INA	850 / Subroutine	11,000 / Subroutine	INA	INA

No.	Storage: Type of Storage	Storage: Number of Words: Minimum System	Storage: Number of Words: Maximum System	Storage: Number of Words: Module Size	Storage: Word Time μsec.	Storage: Access Time μsec.	Storage: Data Unit Accessed	On-Line Input-Output: Type of Unit	On-Line Input-Output: Manufacturer	On-Line Input-Output: Speed	On-Line Input-Output: Number of Units	Magnetic Tape: Manufacturer	Magnetic Tape: Char. per Second	Magnetic Tape: Bits/Inch / Inches/Sec.	Magnetic Tape: Number Operating / Total Tape Units	Special Features	Computer Name
12	Core	1024	4096	—	20	10	Word	Tape Reader	Ferranti	300 FPS	16 Total	Anpex FR 300	20,000	167 / 120	6 / 16	Automatic decimal-binary conversions	EMIDEC 1100
								Tape Punch	Creed	30/300 FPS							
								Card Reader	Elliott	400 CPM							
								Card Punch	ICT	100 CPM							
								Printer	ICT	300 LPM							
	Drum	16,384	65,536	16,384	INA	15,000	4 Words										
13	Core	4096	32,768	4096	10	5	Word	Tape Reader	Elliott	1000 FPS	Multiple	EMI	60,000	300 / 200	5 / 30	Flexible switching of peripheral equipment to on-line or off-line use. Program interrupt.	EMIDEC 2400
								Tape Punch	Creed	300 FPS	Multiple						
								Card Reader	Elliott	400 CPM	Multiple						
	Diode-capacitor	64	64	—	4.5	1.5	Word	Card Punch	ICT	100 CPM	Multiple						
								Printer	ICT / Rank	300 LPM / 3000 LPM	6						
14	Drum	4096	8192	4096	1250	10,000	Word	Card Reader	ICT	100 CPM	1	No Magnetic Tape				Direct transfer from card reader to printer and punch. The same card can be punched in both decimal and binary	ICT 1200 ICT 1201 ICT 1202
								Card Punch	ICT	100 CPM	1						
								Printer	ICT	100 LPM	1						
15	Core	400	2000	400	12	4	Word	Card Reader	ICT	600 CPM	1	Ampex FR 300	90,000	300 / 150	2 / 8	Automatic error correction on tapes	ICT 1301
								Card Punch	ICT	100 CPM	1						
	Drum	12,000	96,000	12,000	52	286	200 Words	Printer	ICT	600 LPM	1	Ampex FR 400	22,500	300 / 75			
16	Drum	8192	8192	—	312	5000	Word	Tape Reader	Ferranti	200 FPS	1–2	No Magnetic Tape				Microprogrammed computer	STAN-TEC ZEBRA
								Tape Punch	Teletype	50 FPS	1–2						
								Teleprinter	Creed	7 CPS	1–2						
17	Core	512	8192	512	INA	INA	Word	Tape Reader	Elliott	800 FPS	1–6	ITT K2S	20,000	200 / 100	1 / 64	Up to 8 blocks of core buffer storage with 32 words each are available.	STAN-TEC SYSTEM
								Tape Punch	Teletype	50 FPS	1–6						
									Creed	300 FPS							
								Card Punch	ICT	150 CPM	1						
	Drum	8192	8192	—	INA	5000	Word	Card Reader	Elliott	340 CPM	1	Ampex	INA	INA	1 / 64		
								Printer	Rank	3000 LPM	Off Line						
								Teleprinter	Creed	10 CPS	1–2						
18	Mercury Delay Line	402	626	—	32	.496	Word or Multi-Word	Tape Reader	INA	850 FPS	1 (Optional)	Decca	8000	80 / 100	1 / 8	Serial binary computer	DEUCE
								Tape Punch	INA	30 FPS	1 (Optional)						
	Drum	8192	8192	—	INA	15	32 Words	Card Reader	ICT	200 CPM	2						
								Card Punch	ICT	100 CPM	2						
19	Core	4096	32,768	4096	Main Storage 6 μs Special Wkg Store .5 μs Read 1 μs Write	Main Storage 3 μs Special Wkg Store .5 μs	Word	Printer	Rank	3000 LPM	As Required	English Electric	33,333	333 / 100	8 to 16 / 64	Use of special working storages. Concurrent operation up to 4 programs running on time sharing basis. Time smoothing advance control.	KDF-9
								Tape Reader	INA	1000 FPS							
								Tape Punch	INA	110/300 FPS							
								Card Reader	English Electric	400 CPM							
								Card Punch	English Electric	150 CPM							
								Printer	English Electric	600/900 LPM							
20	Electro-magnetic Delay Line	71	135	16	172	500	1 Digit	Card Reader	BULL	150 or 300 CPM	1–2	Burroughs	21,500 Digits	200 / 67	1 / 8	—	GAMMA 3 ET
								Card Punch	BULL	150 or 300 CPM	1–2						
	Drum	4096	16,384	4096	172	10,000	16 Words	Printer	BULL	150 or 300 LPM	1–2						

INA—Information not available

[a] *Maximum internal memory addressing capacity is 1,048,576 words.*

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EUROPEAN COMPUTERS (*Cont'd*)

No.	Manufacturer and Country	Computer Name	Availability: Number On Order	Availability: Number Installed	Availability: Date of First Installation	Technique: Circuits	Technique: Clock Rate	General Machine Features: Word Length	Addresses per Instruction / Instructions per Word	Number of Operations Decoded / Possible	Number of Index Registers	Indirect Addressing	Partial and Multiple Word Operations	Internal Checking	Operation Times (Micro-Seconds) (Including Memory Accesses): Addition (Fixed / Floating)	Multiply (Fixed / Floating)	Control Transfer (Min. / Max.)	Shift Operations (1 Place / Average)
21	Compagnie des Machines BULL France	GAMMA 60	13	3	1960	Transistor Diode	2700 kc	6 Digits or 24 Bits	1–3 / Undefined	INA	0	Yes	No	Modulo 7 Check On All Operations	100 / INA	250 / INA	INA	INA
22	SEA France	CAB 3030	INA	3	1958	Vacuum Tube Diode	100 kc	30 Bits	2 / 1	31 / 31	1	No	Double Word	Parity	320 / 9600	640 / 5120	INA	320 / 5120
23	Le Matériel Electrique S-W (SEA) France	CAB 500	20	2	1960	Magnetic Switching (Symmag)	220 kc	32 Bits	2 / 1	46 / 64	1	No	Double Word	Parity	308 / Subroutine	Subroutine / Subroutine	INA	308 / 308
24	SEA France	SEA 3900	20	2	INA	Transistor Diode	2000 kc	Variable (2 Characters Per Memory Access)	3 / Undefined	43 / 128	3 (One For Each Address)	No	Data Controlled Word Length	Parity	216 / Subroutine	5590 / Subroutine [5 Digit Factors]	48	Undefined
25	SEA France	CAB 5000	INA	INA	INA	Transistor Diode	2000 kc	42 Bits	2 / 1	34 / INA	3	No	Double Word	2 Parity Bits Per Word	24 / 48	48 / 48	24 / 24	48 / 48
26	SNE France	KL 901	INA	1	1960	Transistor and Vacuum Tube Diode	200 kc	29 Bits	2 / 1	56 / 64	2	Yes	No	Parity	10 / 20	No Operation / 80	10 / 10	10 / 10
27	University of Pisa Italy	C.E.P.	1	0	1960	Vacuum Tube Germanium Diodes and Transistor	Asynchronous	36 Bits	1 / 1	512 / 512	64	No	Double Word	No	15 / 100	135 / 135	10 / 24	10 / 52
28	Olivetti Italy	ELEA 6001	4	INA	1960	Transistor Diode Core	250 kc	Variable Number of Digits	1–3 / Undefined	116 / 256	16	Yes	Data Controlled Word Length	Parity Bit On Each Digit	364 / 2198	3804 / 3426 [10 Digit Factors]	60	Undefined
29	Olivetti Italy	ELEA 9003	6	1	1960	Transistor Diode	100 kc	Variable Number of Characters	1 / Undefined	91 / 256	40	No	Variable Word Length Controlled By Either Instructions Or Data	Parity Bit On Each Character Modulo 3 Check on Arithmetic	200 / Subroutine	1400 / Subroutine	100	Undefined
30	Siemens Halske A G Germany	SIEMENS 2002	22	8	1958	Transistor Diode	200 kc	12 Decimal Digits and Sign	1 / 1	86 / 1000	3	Yes	INA	Illegal Digit Combinations	90 / 450	1260 / 1350	90 / 90	INA
31	Telefunken Germany	TR-4	4	0	1961	Transistor Diode	2000 kc	48 Bits	1 / 2	208 / 256	256	Yes	Half and Double Word Operations	Modulo 3 Check On All Operations	8.5 / 15	30 / 30	7.5	10.5 / 12

No.	Storage: Type of Storage	Number of Words: Minimum System	Number of Words: Maximum System	Number of Words: Module Size	Word Time μsec.	Access Time μsec.	Data Unit Accessed	On-Line Input-Output: Type of Unit	Manufacturer	Speed	Number of Units	Magnetic Tape: Manufacturer	Char. per Second	Bits/Inch / Inches/Sec.	Number Operating / Total Tape Units	Special Features	Computer Name
21	Core	8192	32,768	4096	10	10	Word	Card Reader	BULL	300 CPM	INA	Burroughs	21,500 Digits	200 / 67	10 / 48	—	GAMMA 60
								Card Punch	BULL	300 CPM	INA						
								Printer	BULL	300 LPM	INA						
	Drum	25,600	No Limit	25,600	100	10,000	Word	Tape Reader	BULL	300 FPS	INA						
								Tape Punch	BULL	25 FPS	INA						
22	Core	1024	16,384	1024	320	6	Word	Tape Reader	Ferranti	200 or 400 FPS	2	Potter	8000	140 / 60	1 / 10	—	CAB 3030
								Tape Punch	SEA	45 FPS	2						
	Drum	16,384	16,384	—	320	20,000	32 or 128 Words	Printer	Shepard	900 LPM	1						
								Microfilm Printer	SEA	2000 Char/sec	1						
23	Drum	16,384	16,384	16,384	160	10	Word	Tape Reader	SEA	80 FPS	1 (Optional)	Magnetic Tape Available				—	CAB 500
								Tape Punch	SEA	45 FPS	1 (Optional)						
	Shift Register	16	16	16	2.5	2.5	Word	Typewriter	Friden	10 CPS	1						
24	Core	2048 Characters	4096 Characters	—	INA	6	Char.	Printer	Shepard	900 LPM	No Limit	C.d.C. (French Licensee of Potter)	9000	300 / 60	2 / No Limit	Double recording on magnetic tape	SEA 3900
								Card Reader	Elliott	400 CPM	No Limit						
	Drum	40,960 Characters	81,920 Characters	—	INA	15,000	160 Char.	Tape Reader	SEA	450 FPS	No Limit						
								Tape Punch	SEA	45 FPS	No Limit						
25	Core	4096	32,768	4096	24	6	Word	Tape Reader	SEA	400 FPS	2	C.d.C. (French Licensee of Potter)	9000	300 / 60	2 / 64	Square root operation	CAB 5000
								Tape Punch	SEA	50 FPS	2						
	Drum	16,384	131,072	16,384	160	10,000	128 Words	Printer	Shepard	900 LPM	1						
26	Core	1024	8192 (Total Including Fixed Memory)	1024	10	5	Word	Tape Reader	SNE	1000 FPS	1	SNE	50,000 (10,000 Words)	200 / 50	2 / 8	Square root operation	KL 901
								Tape Punch	Creed	33 FPS	1						
27	Core	4096	32,768	INA	7	3.5	Word	Tape Reader	Ferranti	300 FPS	2	Ampex	20,000	270 / 75	1 / 8	Fixed ferrite slug memory (256×256 bits) for control. Two index register addresses per instruction. Extra codes.	C.E.P.
								Tape Punch	Teletype	60 FPS	3						
	Drum	16,384	INA	16,384	39	10,000	Variable	Printer	BULL	150 LPM	1						
28	Core	10,000	100,000	10,000	10	6	Digit	Tape Reader	Olivetti	800 FPS	1	Ampex	22,500	300 / 75	1 / 6	Wired in micro subroutines and expandable set of commands.	ELEA 6001
								Tape Punch	Olivetti	50 FPS	1						
								Card Reader	BULL	150 CPM	1						
								Printer	Oliv tti	600 LPM	1						
29	Core	20,000	160,000	20,000	10	10	2 Char.	Tape Reader	Olivetti	800 FPS	10 Total	Ampex	45,000	300 / 150	2 / 20	Three simultaneous program sequences.	ELEA 9003
								Tape Punch	Olivetti	50 FPS							
								Card Reader	BULL	500 CPM							
	Drum	0	360,000	120,000	11	10,000	Up to 1920 Char.	Card Punch	BULL	150 CPM							
								Printer	Olivetti	600 LPM							
30	Core	1000	100,000	—	14	5	Word	Tape Reader	Siemens	200 FPS	1–5	Siemens or Ampex	46,000	200 / 120	INA / 60	Real time input	SIEMENS 2002
								Tape Punch	Siemens	60 FPS	1–5						
								Card Reader	IBM	800 CPM	1–5						
	Drum	10,000	2,000,000 Characters	10,000	INA	19,000	INA	Card Punch	IBM	250 CPM	1–5						
								Printer	IBM	1000 LPM							
									Analex	900 LPM							
31	Core	8192	28,672	4096	6	2	Word	Tape Reader	Elliott	1000 FPS	64 Total	Telefunken	37,500	375 / 100	8 / 64	Operations usually faster than noted due to overlapping memory accesses	TR-4
									FACIT	500 FPS							
								Tape Punch	FACIT	150 FPS							
	Fixed Core	1024	4096	256	1	1	Word	Card Reader	IBM	800 CPM							
									BULL	300 CPM							
								Card Punch	IBM	250 CPM							
									BULL								

INA—Information not available

[a] *Maximum internal memory addressing capacity is 1,048,576 words.*

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EUROPEAN COMPUTERS (*Cont'd*)

No.	Manufacturer and Country	Computer Name	Availability: Number On Order	Availability: Number Installed	Availability: Date of First Installation	Technique: Circuits	Technique: Clock Rate	General Machine Features: Word Length	Addresses per Instruction / Instructions per Word	Number of Operations Decoded / Possible	Number of Index Registers	Indirect Addressing	Partial and Multiple Word Operations	Internal Checking	Operation Times (Micro-Seconds) (Including Memory Accesses): Addition (Fixed / Floating)	Multiply (Fixed / Floating)	Control Transfer (Min. / Max.)	Shift Operation (1 Place / Average)
32	Standard Elektrik Lorenz Germany	ER-56	12	7	1959	Transistor Diode	100 kc	7 Decimal Digits	1 / 1	82 / 100	9	No	Double Word	2 Out of 5 Code	200 / 1000	500 / 1500	150 / 300	150 / 150
33	Standard Elektrik Lorenz Germany	SEL-B7	1	0	INA	Transistor Diode	100 kc	10 Characters	1 / 1	57 / 100	9	Yes	Partial Word Operations	Parity	90–180 / Subroutine	Subroutine / Subroutine	60 / 60	INA
34	Zuse K.-G. Germany	Z-22R	INA	30	1958	Vacuum Tube	140 kc	38 Bits	1 / 1	Micro Programmed / 2^{18}	24	Yes	Double Word	INA	600 / Subroutine	15,000 / Subroutine	300	INA
35	Zuse K.-G. Germany	Z-23	INA	0	1961	Transistor	150 kc	40 Bits	1 / 1	Micro Programmed / 2^{18}	240	Yes	Double Word	INA	300 / 10,000	13,000 / 20,000	300	INA
36	Zuse K.-G. Germany	Z-31	INA	0	INA	Transistor	53 kc	10 Decimal Digits and Sign	1 / 1	42 / INA	10	Yes	Double Word	2 Out of 5 Code	600 / Subroutine	20,000 / Subroutine	INA	INA
37	N. V. Electrologica Netherlands	X1	16	10	1959	Transistor Diode	500 kc	27 Bits	1 / 1	48 / 64	1	No	No	Parity	64 / Subroutine	500 / Subroutine	36 / 64	48 / 144
38	Philips Netherlands	PASCAL / STEVIN	2	0	1960	Vacuum Tube Transistor Diode	660 kc	42 Bits	1 / 2	57 / 64	8	INA	INA	Parity on Half Word Carry Comparison in Adder	10 / 10–60	70 / 55	4.5 / 7.5	11.5 / 42
39	Facit Sweden	EDB 2 / EDB 3	3	5	1957	Vacuum Tube and Transistor	180 kc	40 Bits	1 / 2	95 / 128	0	No	Half Word Operations	No	45 / Subroutine	290 / Subroutine	22 / INA	45 / 157
40	Regnecentralen Dansk Institut for matematik-Maskina Denmark	GIER	1	0	1961	Transistor Diode	500 kc	40 Bits Plus 2 For Word Indicator	1 / 1	37 / 64	12	Yes	No	No	50 / INA	170 / INA	INA	INA

No.	Storage: Type of Storage	Storage: Number of Words: Minimum System	Storage: Number of Words: Maximum System	Storage: Number of Words: Module Size	Storage: Word Time μsec.	Storage: Access Time μsec.	Storage: Data Unit Accessed	On-Line Input-Output: Type of Unit	On-Line Input-Output: Manufacturer	On-Line Input-Output: Speed	On-Line Input-Output: Number of Units	Magnetic Tape: Manufacturer	Magnetic Tape: Char. per Second	Magnetic Tape: Bits/Inch / Inches/Sec.	Magnetic Tape: Number Operating / Total Tape Units	Special Features	Computer Name
32	Core	200	9000	200/1000	30	5	Word	Tape Reader	Ferranti	400 FPS	23 Total	Ampex	52,500 (Digits)	250 / 150	4 / 16	Control unit simultaneously connects any core storage to any input, output or processing unit. Tape bin storage units.	ER-56
								Tape Punch	Lorenz	50 FPS							
									Creed	300 FPS							
	Drum	6000	72,000	6000	INA	10,000	20–200 Words	Card Reader	Elliott	400 CPM		Standard Elektrik	35,000 (Digits)	250 / 100	4 / 16		
								Card Punch	IBM	100 CPM							
								Printer	Shepard	900 LPM							
33	Core	2000	10,000	2000	10	3	Word	Tape Reader	Lorenz	100 FPS	6	Standard Elektrik	25,000	250 / 100	24 / 48	Reservation system computer with real time input-output facilities and large back up memory using tape bins and drum with independent searching facilities	SEL-B7
									Ferranti	300 FPS							
	Drum	9000	180,000	9000	INA	10,000	Word	Tape Punch	Lorenz	50 FPS	6						
								Printer	Shepard	900 LPM	2						
34	Drum	8192	8192	—	300	5000	Word	Tape Reader	Ferranti	200 FPS	1	No Magnetic Tape				—	Z-22 R
								Tape Punch	Creed	25 FPS	1 (Optional)						
								Typewriter	Siemens	10 CPS	1						
35	Core	240	8431	256	300	INA	Word	Tape Reader	Ferranti	300 FPS	1	INA				—	Z-23
								Tape Punch	Creed	50 FPS	1						
	Drum	8192	8192	—	300	5000	Word	Card Reader	INA	300 CPM	INA						
								Card Punch	INA	150 CPM	INA						
								Printer	Maul	80 CPS	1						
36	Core	200	10,000	INA	300	INA	Word	Tape Reader	Ferranti	300 FPS	INA	INA				—	Z-31
								Tape Punch	Creed	50 FPS							
								Card Reader	INA	INA							
								Card Punch	INA	INA							
								Printer	Maul	80 CPS							
37	Core	1216	32,768	512	32	INA	Word	Tape Reader	Ferranti	150 FPS	1+	INA	30,000	200 / 150	2 / 16	Wired core memory for subroutines added in 64 word units. Each 4096 word memory unit has independent input-output connections.	X1
								Tape Punch	Creed	25 FPS	1+						
								Card Reader	BULL	700 CPM	1+						
								Card Punch	BULL	112 CPM	1+						
								Printer	INA	150/600 LPM	1+						
38	Core	2048	2048	1024	6	3	Word	Tape Reader	Philips Lab.	1200 FPS	1	Ampex	45,000	300 / 150	2 / 16	30 interpretive single address instructions initiating subroutines	PASCAL / STEVIN
								Tape Punch	Teletype	60 FPS	1						
								Card Reader	BULL	150/750 CPM	1						
	Drum	16,384	16,384	—	10,000 for Block	0	128 Words	Card Punch	BULL	75/120 CPM	1						
								Printer	BULL	150 LPM	1						
39	Core	2048	65,536	4096	10	2	Word	Tape Reader	FACIT	500 FPS	8	FACIT	40,000	200 / 200	17 / 64	"Carousel" magnetic tape memory	EDB 2 / EDB 3
								Tape Punch	FACIT	150 FPS	8						
	Drum	8192	8192	—	625	10,000	32 Words	Card Reader	INA	700 CPM	8						
								Card Punch	INA	120 CPM	8						
40	Core	1024	1024	—	10	4	Word	Tape Reader	FACIT	500 FPS	1	No Magnetic Tape				The operation times include indexing and counting. Every operation may be conditional.	GIER
	Drum	12,000	12,000	—	500	500 Block Access	40 Words	Tape Punch	FACIT	150 FPS	1						
								Typewriter	Friden	10 CPS	1						

INA—Information not available

[a] *Maximum internal memory addressing capacity is 1,048,576 words.*

other more advanced relay computer, the Z 5, appeared in 1953. In 1958 Zuse introduced a vacuum-tube 8192-word magnetic drum computer, the Z 22. This is a medium-scale wired-core microprogrammed computer with extremely flexible programming.

In 1960 the Z 23 and Z 31 were announced. The Z 23 is a solid-state version of the Z 22, with an additional 240-word magnetic core memory. The Z 31 is a new, small, general-purpose solid-state computer with a basic magnetic core memory of 200 words, expandable to 10,000 words. Like the Z 22, it uses paper tape as its input-output medium and a typewriter for printed output.

The Netherlands

Contributions in the information processing field from The Netherlands have been high for the total computer activity in the country. The general emphasis is on the smaller computer systems.

Mathematisch Centrum: The Mathematisch Centrum was founded in 1946 as a government-sponsored nonprofit organization to work in the fields of pure and applied mathematics, statistics and digital computers. It was engaged in early developments of relay and magnetic drum computers, and built the ARMAC (Automatische Rekenmaschine Mathematisch Centrum), completed in June, 1956, and still in operation.

N.V. Electrologica: In 1958, under sponsorship of the Nillmij Insurance Company of Amsterdam, the transistor magnetic-core X 1 computer was designed by the Mathematisch Centrum. To fulfill the demands for additional X 1 computers Nillmij organized a new company—N.V. Electrologica—to make copies of the X 1 and to expand the computer's input-output capabilities. The engineering and fabrication group from the Mathematisch Centrum was transferred to the new company.

N.V. Philips Gloeilampen Fabrieken: The Philips organization, one of the largest electrical component manufacturing companies in the world, has its main research and development laboratories in The Netherlands. To keep abreast of the new applications of components in computers, the company is building two computers—PASCAL and STEVIN—for its own use. They are identical, except for input-output equipment.

Philips is also engaged in the design and construction of an electronic system for air traffic control. In June, 1960, the gigantic digital data transmission system to be used for the United Airlines reservation system in the United States was nearing completion.

Sweden

Scene of some of Europe's earliest computer activity, Sweden is currently active in research, development and production. The work stems from the government's Swedish Board for Computing Machinery (Matematikmaskinnamnden). The Board was active in early computer development. Its BESK computer, completed in 1953, was used as a pattern for the early machines built by FACIT and SAAB, and by the Dansk Institute for Matematikmaskiner in Copenhagen.

FACIT: FACIT Electronic, a subsidiary of FACIT-Atvidabergs, is one of Sweden's major data processing equipment manufacturers. The FACIT EDB computer is an almost exact copy of the BESK computer developed by the Swedish Board. The first machine produced is installed in the data processing center in Stockholm established and maintained by the company, providing computing service on a rental basis. The current model, the EDB 3, incorporates the new FACIT ECM 64 Carousel memory, described earlier.

SAAB: SAAB, well known for its aircraft and automobile production, is also active in digital computation. The company built a BESK-type computer for its own use and has built a transistorized airborne navigation computer. A solid-state commercial computer is in development.

Denmark

In 1953 the Academy of Sciences in Denmark formed a new institute, Regnecentralen (Dansk Institut for Matematikmaskiner), to work in the field of digital computer development and application. The group patterned its first computer, the DASK, after the BESK computer designed by the Swedish Board for Computing Machinery. The DASK was built and put into around-the-clock operation in early 1958.

In connection with computing and consulting work for the Geodetic Institute of Denmark, Regnecentralen was requested to design and build a new computer for the Institute. This computer, GIER, is a transistor parallel computer with magnetic core and drum storage. The computer was planned for considerable programming flexibility and simplicity.

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