Jan 27 71

M E M O R A N D U M

TO: Minuteman Computer Users Group

FROM: Ken Watkinson, Dan Bergen, & Lloyd Lauffer, Florida State University

DATE: September 14, 1970

During the past year we have been working to make our D17B computer operational again. To date we have applied power to the computer, provided a basic cooling system, constructed a simple control panel, and programmed it with programs of 2 to 10 steps. The purpose of this memo is to relate to you what we have done, how we have done it, and what additional information we have found out. This information, in addition to the manuals specified, should be helpful to those trying to operationalize their computer.

Any comments or criticism pertaining to this memo are welcome along with any additional information you have discovered. Please address all replies to:

MCUG
CAI Center
Florida State University
Tallahassee, Florida 32306

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I. INITIAL SET-UP

A. Disassembly

The D17B computer with its associated power supplies are contained in the toroid structure around the remains of the guidance platform (in the declassified version). We have separated the computer/power supply structure from the base plate and hence the guidance platform in order to get at J7, J8, and J17 located on the bottom of the structure. To do this required removal of the screws around the base on both the outside and inside of the toroid. In order to get at the inside screws, the gyro mounts had to be removed. The disassembly also required taking off the power supply leads from the base and cutting the cooling line in two places--between the heat transfer unit and the memory unit and along the tubing coming from the power supply section. It is at these points that the forced cooling can later be connected.

Once disassembled, the computer/power supply unit was placed upside down on a table. This gives easy access to the various connectors (i.e., J7, J8, and J17 - see Figure 1) and the power supply leads. We have removed all the cover panels from the structure in order to be able to pull cards in checking out the computer.

B. Power Supply

The basic power requirement is 28 volts dc to drive the internal supplies in the power supply half of the toroid. Although all the supplies are not used (i.e., those for the gyro motors, etc.), we have not determined and removed the unnecessary ones. Our unit

draws a steady state current of 17-18 amps with an initial transient of slightly over 24 amps. We have constructed our own 28 volt power supply and the schematic is shown in Appendix A. It has been in operation for over 4 months and there have been no problems.

Power is applied to the leads taken off the base assembly. The positive voltage is connected to the yellow lead. The brown and the large red leads are tied together and connected to the negative side. Figure 2 shows where these leads connect onto the unit. The brown and yellow leads tie to TB5 and TB6 respectively on the power supply side and the large red lead to a tie block below (when the computer is upside-down) the memory unit.

The 40 volts dc overvoltage is only required for starting the gyros and is not needed for computer operations. Therefore, this supply and its associated timing circuitry (the 2 seconds disconnect) may be eliminated.

C. Cooling

With power applied and no means of cooling other than radiation to the room, both the power supply base and the memory get very hot within a few minutes. Therefore, we rigged up a two gallon container to serve as a reservior with a pump to circulate water through the memory and power supplies. For identification and testing, we have found that water (as obtained from the tap) pumped through the existing coolant route at approximately 5 to 10 gallons per minute suffices for about 20 minutes. Power is then turned off to allow the power supplies and the memory to cool while we change the, by now, warm water. (A good rule of thumb is to keep

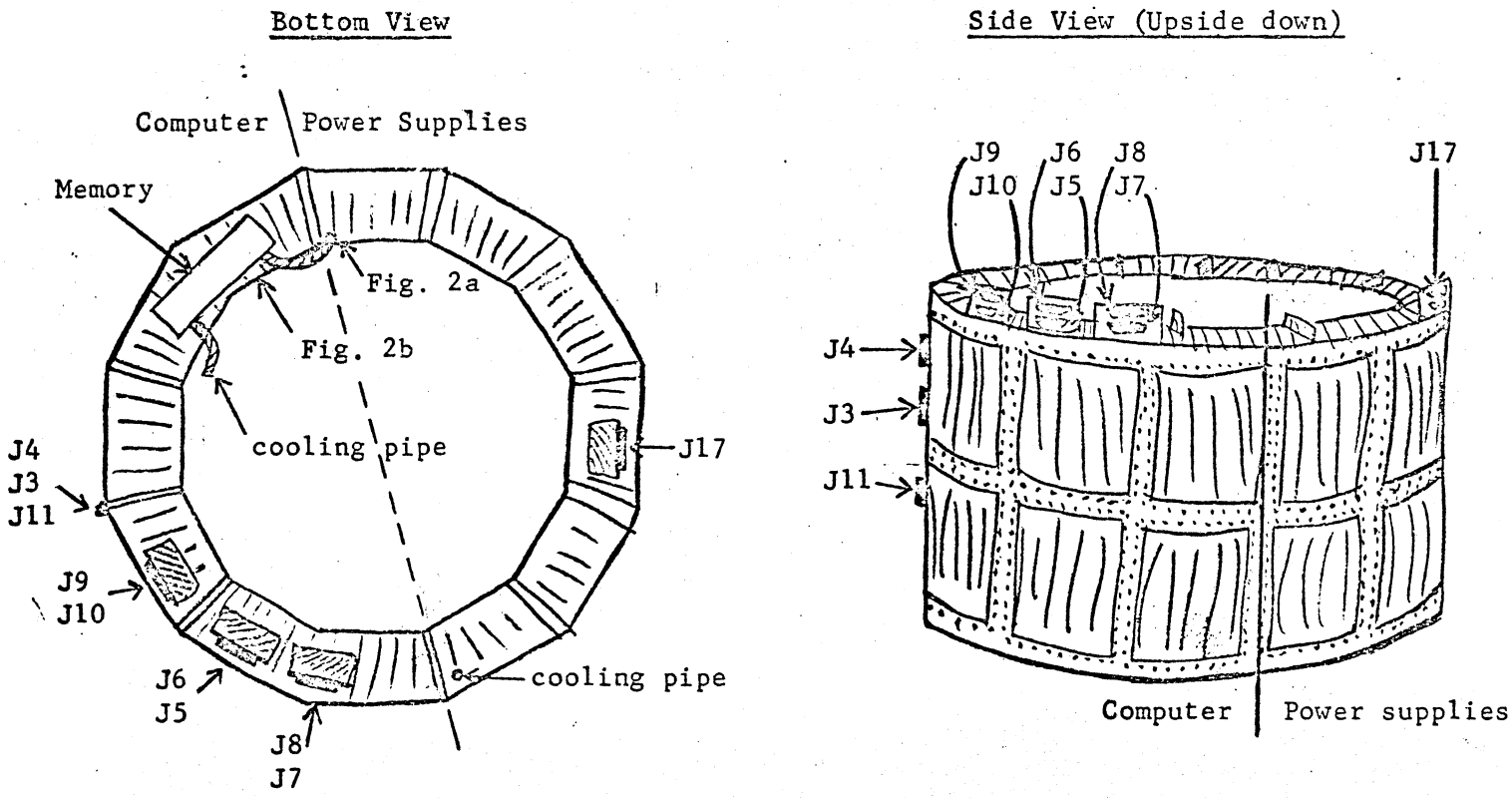


Figure 1 - Connector Locations

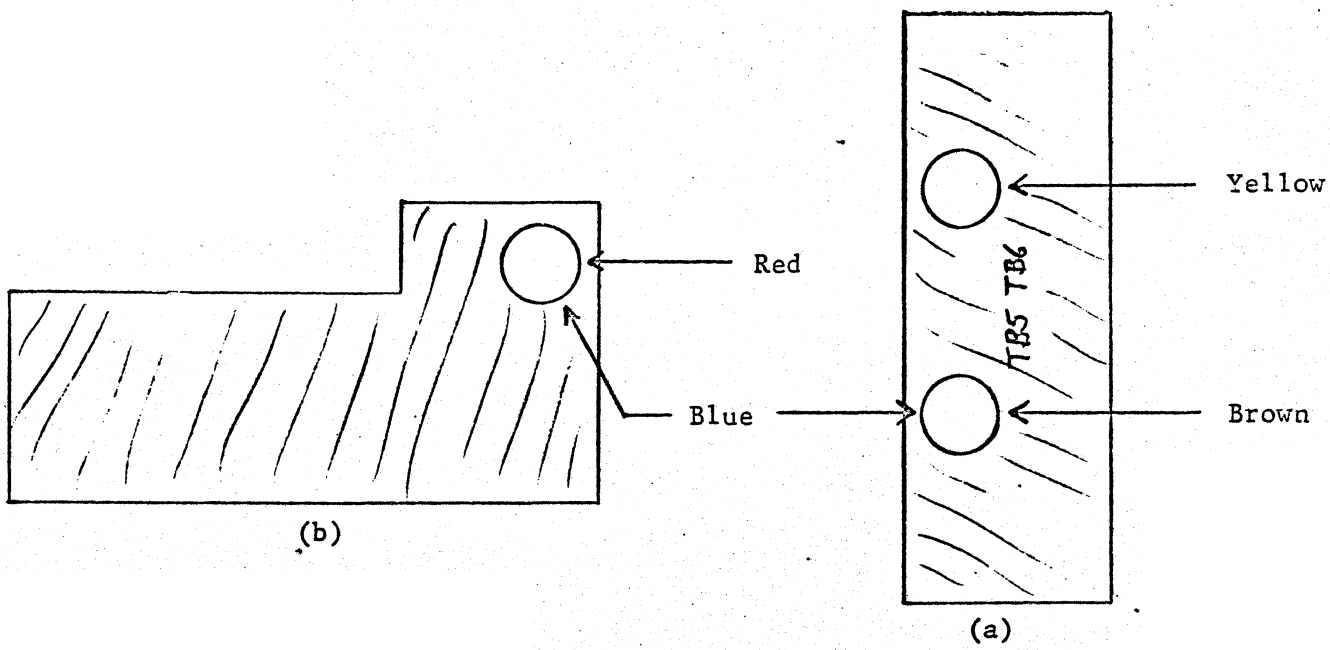


Figure 2 - Power connections

the memory cool enough to touch.) This has been with the card covers removed.

For prolonged operation and/or the covers attached, forced air circulation through the cards may be necessary along with a means of cooling the circulated water. Some thought should be given to a permenant cooling system for long term use.

D. Documentation Needed

The documentation that we found helpful is as follows:

1) Introduction Manual to the D17B.

2) T. O. 11G2-10-5-3-10, Digital Computer Electronic Modules.

3) T. O. 11G2-10-5-3-5, General Purpose Digital Computer (Model D17B).

4) Missile Guidance Set Interconnections Wire Diagram (sheet 9 of 10 and 10 of 10)--enclosed as Appendix B.

5) Listings of functions on some of the internal connectors (J3, J4, and J11). Most of these points go to various control flip-flops and are useful in following the state of the computer. These listings enclosed as Appendix C.

Also of use, particularly to those contemplating acquiring the D17B, is the Preliminary Maintenance Manual of the Minuteman D17A Computer and Associated Test Equipment, Project Office Memorandum No. 71, Part 1, January, 1960, as handed out by Autonetics at the June MCUG meeting. This memorandum contains a good description of the earlier version, the D17A, but most of it applies to the D17B. Included in it are descriptions of the I/O facilities and the programming format.

II. PIN IDENTIFICATION

A. Test Points for Internal Power Supplies

The following pins are test points for the internal power supplies. They are useful for checking the internal supplies when power is first applied.

Connector	Pin No.	Voltage	Tolerance
J17	29	+15 volts	± 2%
	32	-1	± 2
	33	-25	±4
	35	+10	±2
	36	+25	±2
	37	-3	±2
	38	+35	±2
	39	-10	±2
J17	40	-28	(supply voltage)

B. Control Panel Pin Locations

We have constructed a simple control panel for our initial efforts in exercising the computer. This panel consists of switches to provide the necessary inputs to the computer (the schematic is given in Appendix D). Output is by an oscilloscope monitoring the accumulator channel and the other registers.

The pin locations given below were primarily determined by continuity checks between J1 and J2 on the outer shell and J7, J8, and J17 on the computer. The Missile Guidance Set Interconnection Wiring Diagram was also used.

Connector	Pin No.	Function
J7	1	I_1 } Octal Number } Character Input (p. 72-76)*
J7	2	I_2
J7	3	I_3
J7	4	I_4 - Command Bit
J7	5	I_5 - Parity Bit
J7	6	T_c' } Sprocket Timing Input
J8	38	T_c
J7	15	M_{rc} - Master Reset (p. 168)
J7	16	E_{wc} - Enable Write (p. 169)
J7	17	K_{hc} - $\overline{\text{Halt}}$ (p. 14)
J8	15	K_{sc} - $\overline{\text{Single Cycle}}$ (p. 14, 169)
J8	16	K_{rc} - $\overline{\text{Run}}$ (p. 14)
J8	17	I_{mc} - Mode Control Input
J8	24	F_{sc} - Fill Signal - initiates input (p. 12)

C. Character Output (COA) Pin Locations

This COA information was obtained by checking for the corresponding pins between J6 and the outputs of the I/O drivers. (P. 172-174).

Connector	Pin No.	Function
J6	19	S_{C1} } Character Output Bits
↕	20	S_{C2}
	21	S_{C3}
	22	S_{C4}
	23	S_{C5} - Parity
J6	24	S_{CT} - Output Timing

*Page numbers in parenthesis refer to the Introduction Manual.

D. Read Amplifiers

To monitor the various memory channels the following test points were found to be helpful. These points are marked on each read amplifier card and on the "No. 3 Read Amplifier Schematic Diagram" found in pages 5-3 thru 5-6 of Digital Computer Modules. The information in the following table may be found in the "Table of Term Locations for Read Amplifiers" on pages 5-214 and 5-215 of the General Purpose Digital Computer (Model D17B).

Receptacle	Location	Circuit No. 1 Test Point 7	Circuit No. 2 Test Point 8	Circuit No. 3 Test Point 9
J401	A1	M44	M46	M50
J402	A2	M36	M40	M42
J403	A3	M30	M32	M34
J404	A4	Rx	Ux	Vx
J405	A5	Emx	Ex	Ix
J406	A6	S	C	Spare
J407	A7	Nx	Fx	Ax
J408	A8	Lx	Hmx	Hx
J409	A9	M22	M24	M26
J410	A10	M14	M16	M20
J411	A11	M06	M10	M12
J412	A12	M00	M02	M04

E. Multiplexer Output

For telemetry purposes, there is a multiplexer card that can be used to display memory channels 0 thru 50, the contents of the A, L, N, and I registers, or the contents of the E, H, F, U, V, or R loops.

The channel, register, or loop that is transmitted for display is determined by the control settings of the C_{DU0}, C_{DU1}, C_{DU2}, C_{DU3}, and the C_{DL0}, C_{DL1}, ... , C_{DL7}. Thus, with a four position and a eight position switch (see Appendix E) these outputs may be displayed. C_{DC} accesses the I register.

Function	Connector	Pin	Mpx Card Pin
CDL0	J8	1	35
CDL1	J8	2	34
CDL2	J8	3	$\overline{5}$
CDL3	J8	4	8
CDL4	J8	5	9
CDL5	J8	6	11
CDL6	J8	7	22
CDL7	J8	8	18
CDU0	J8	9	1
CDU0	J8	10	$\overline{Y}$
CDU2	J8	11	27
CDU3	J8	12	A
CDC	J8	13	17

Information concerning Mpx was determined from the "Table of Logic Equations," on pages 5-148 to 5-151 in General Purpose Digital Computer (Model D17B) and from Number 126 Logic Network Schematic Diagram page 5-507/5-508 in Digital Computer Electronic Modules.

Codes for Various Mpx Outputs

CDU	CDL	OUTPUT
0	0	M00
	1	M02
	2	M04
	3	M06
	4	M10
	5	M12
	6	M14
	7	M16
1	0	M20
	1	M22
	2	M24
	3	M26
	4	M30
	5	M32
	6	M34
	7	M36
2	0	M40
	1	M42
	2	M44
	3	M46
	4	M50
	5	F_x
	6	H_x
	7	E_x
3	0	U_x
	1	A_x
	2	L_x
	3	N_x
	4	V_x
	5	R_x
	6	H_{mx}
	7	E_{mx}

III. ERRORS

The following items of documentation were found to be either unnecessary or incorrect.

1. The 40 v dc overvoltage supply is not necessary.

2. The 22K resistors shown in series with the T_c and T_c' switches should be no more than 2K and could be eliminated entirely. If the 22K resistors are left in, a solid logic shift is not made. Also, capacitors should be placed across the switch contacts to lessen the effect of switch bounce.*

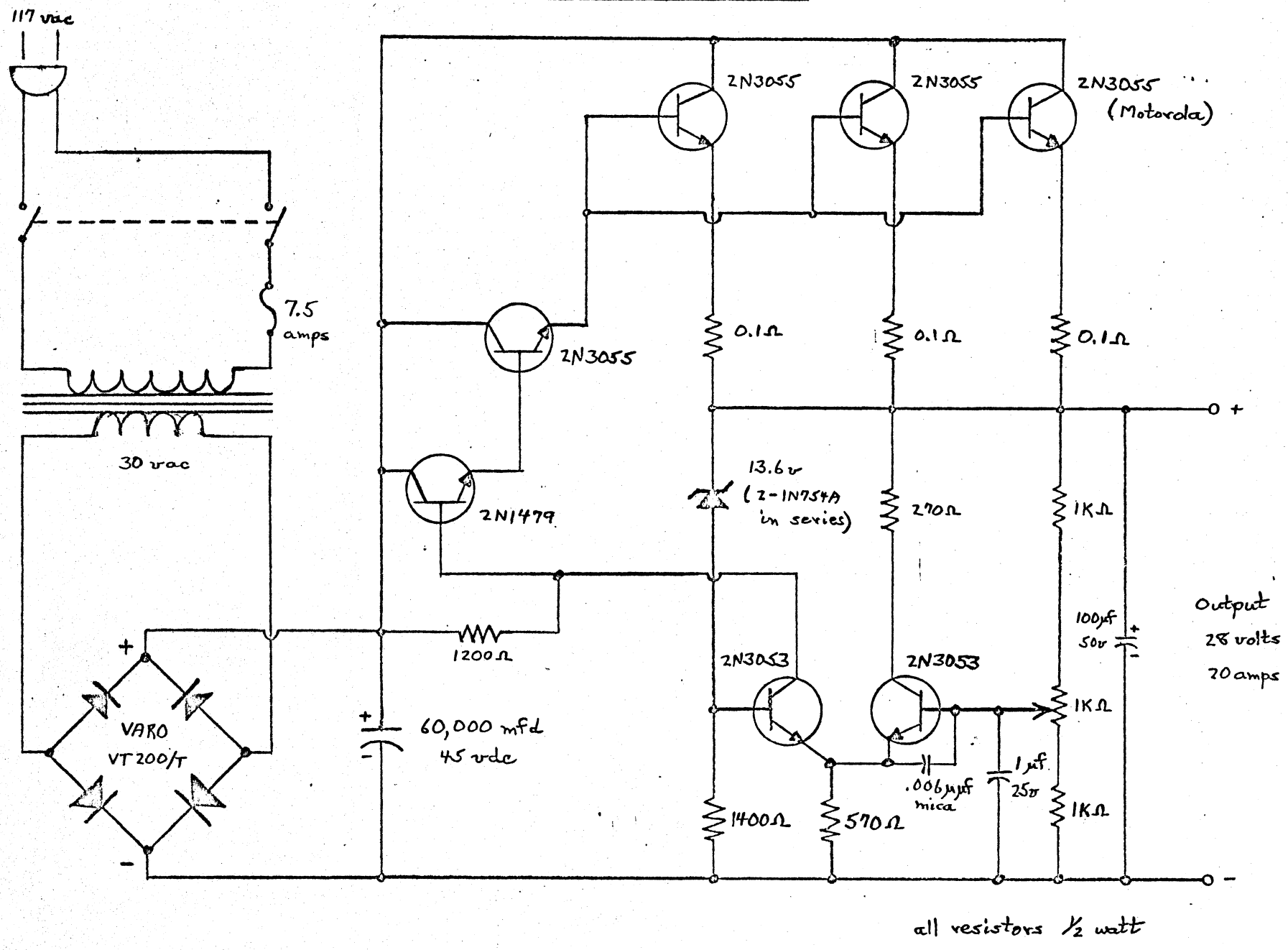
3. The Ewc (enable write, cold memory channels) is shown as a switch to ground. This should be a switch to +25 vdc. This may be clearly seen by referring to the drawing of the "No. 2 Write Electronic Switch Schematic Diagram" on pages 5-73/5-74 of T. O. 11G-10-5-3-10.*

4. The 22K register shown to +25 v in the single step switch (Ksc') should be 2.2K, 1W. An additional 2.2K, 1W, in series with the switch and Ksc' is needed to lower the heat in the resistor.*

*See Appendix D -- Control Panel Schematic

APPENDIX A

POWER SUPPLY SCHEMATIC

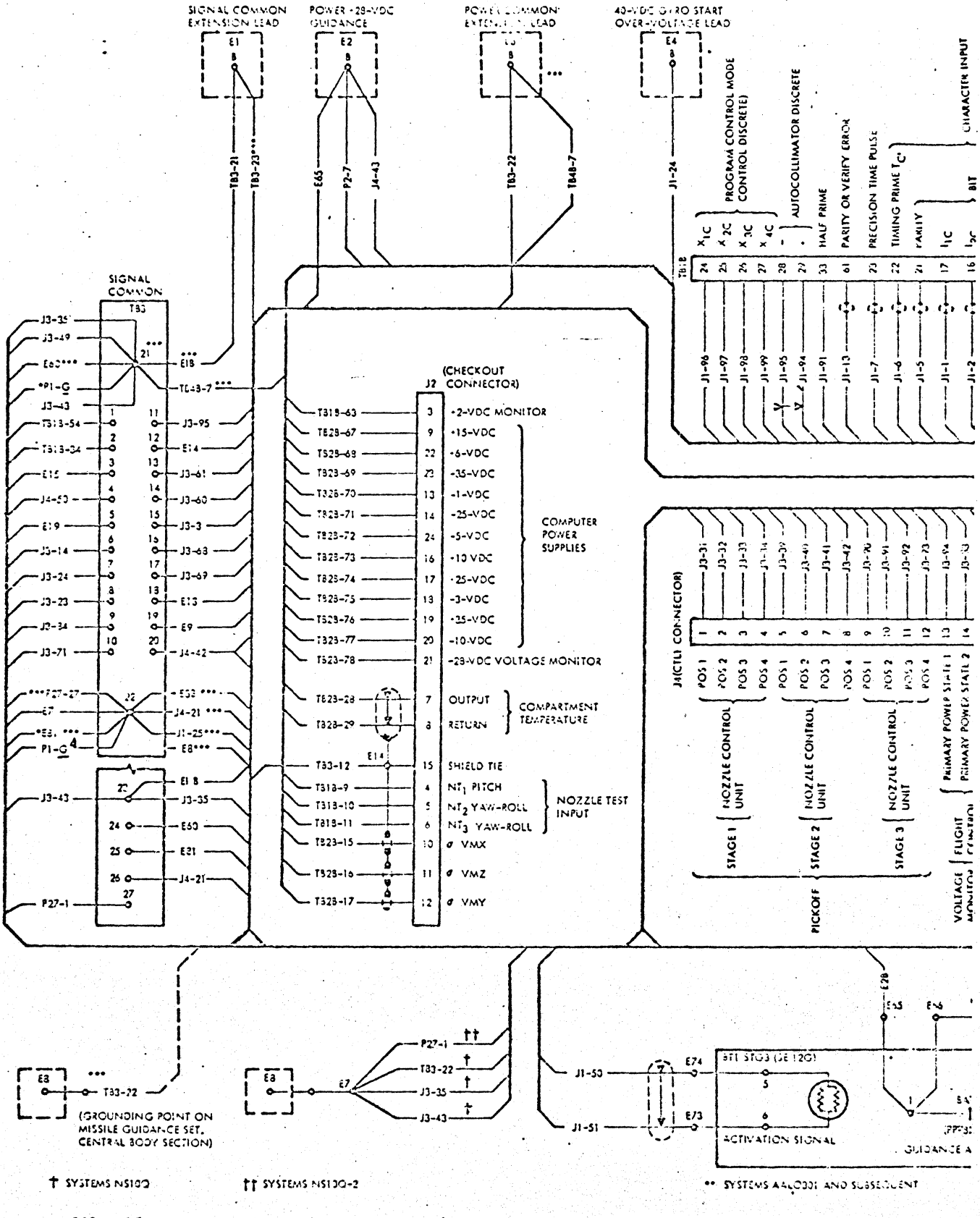


APPENDIX B

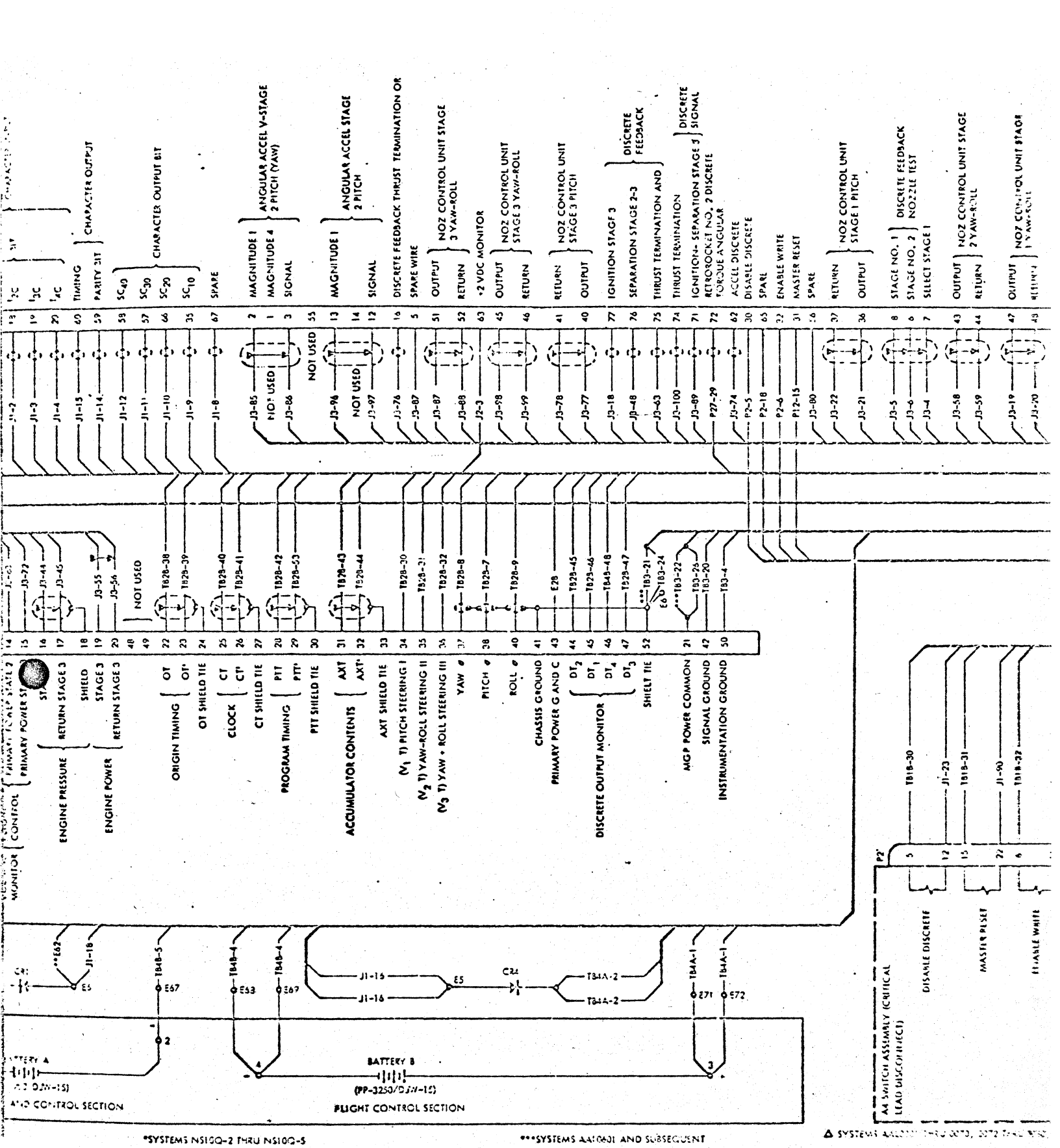
Missile Guidance Set

Interconnection Wiring Diagram

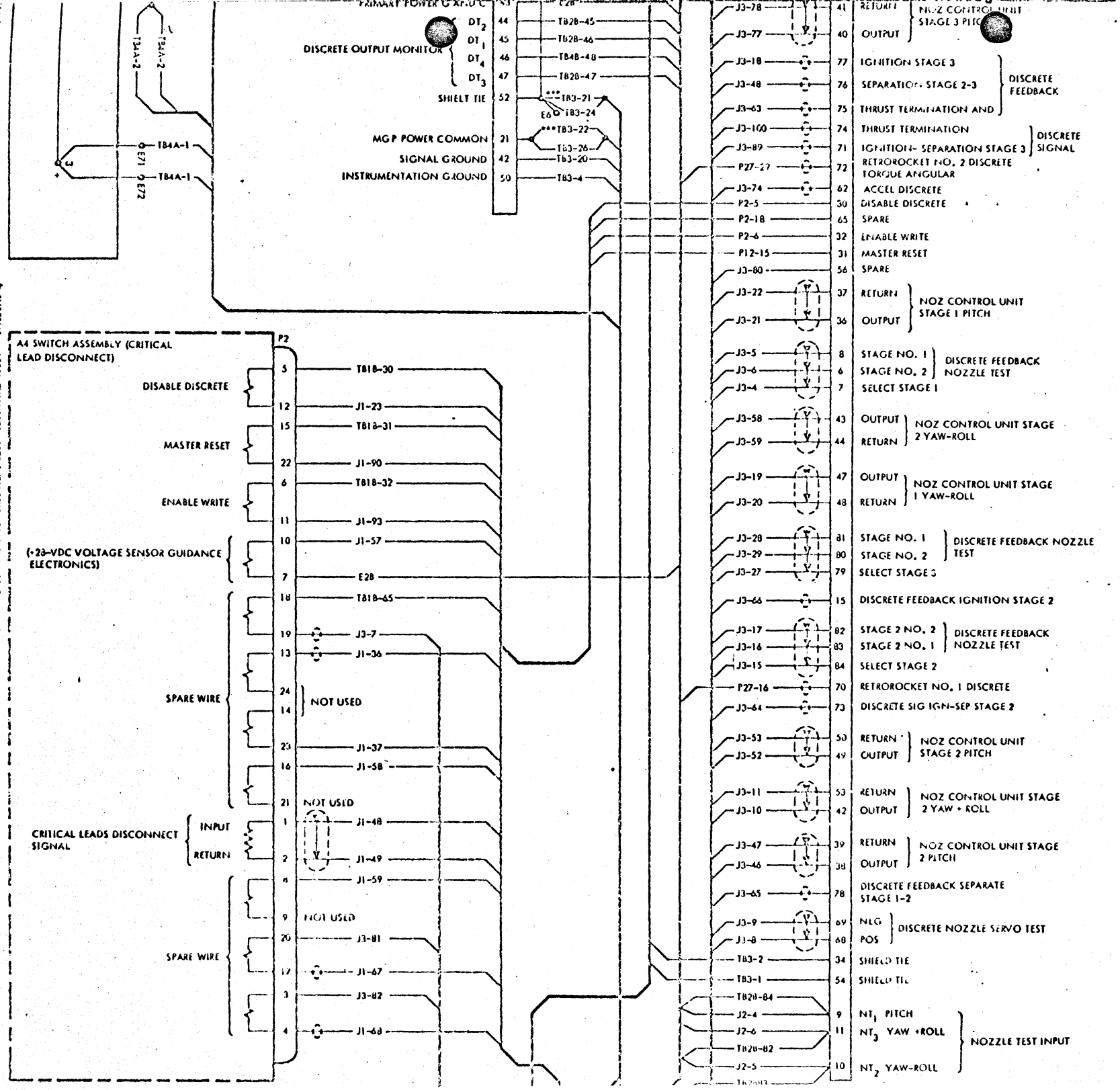
Sheet 9 of 10
and
Sheet 10 of 10



Missile Guidance Set Interconnection Wiring Diagram (Sheet 9 of 10) p. 1



Missile Guidance Set Interconnection Wiring Diagram (Sheet 9 of 10) p. 2


SYSTEMS AAL6401 AND SUBSEQUENT
SYSTEMS AAL6201 THRU 6070, 6072 THRU 6080, 6082 THRU 6087, 6089 THRU 6114, 6117 THRU 6123, 6125, 6127, 6133 THRU 6147, 6153 THRU 6168
A4 SWITCH ASSEMBLY (CRITICAL LEAD DISCONNECT)
P2
DISABLE DISCRETE
MASTER RESET
ENABLE WRITE
(+28-VDC VOLTAGE SENSOR GUIDANCE ELECTRONICS)
SPARE WIRE
CRITICAL LEADS DISCONNECT SIGNAL
INPUT
RETURN
SPARE WIRE
NOT USED
DISCRETE OUTPUT MONITOR
SHIELT TIE
MGP POWER COMMON
SIGNAL GROUND
INSTRUMENTATION GROUND
DISCRETE FEEDBACK
DISCRETE SIGNAL
NOZ CONTROL UNIT STAGE 3 PITCH
NOZ CONTROL UNIT STAGE 1 PITCH
DISCRETE FEEDBACK NOZZLE TEST
NOZ CONTROL UNIT STAGE 2 YAW-ROLL
NOZ CONTROL UNIT STAGE 1 YAW-ROLL
NOZ CONTROL UNIT STAGE 2 PITCH
NOZ CONTROL UNIT STAGE 2 YAW + ROLL
NOZ CONTROL UNIT STAGE 2 PITCH
DISCRETE NOZZLE SERVO TEST
NOZZLE TEST INPUT

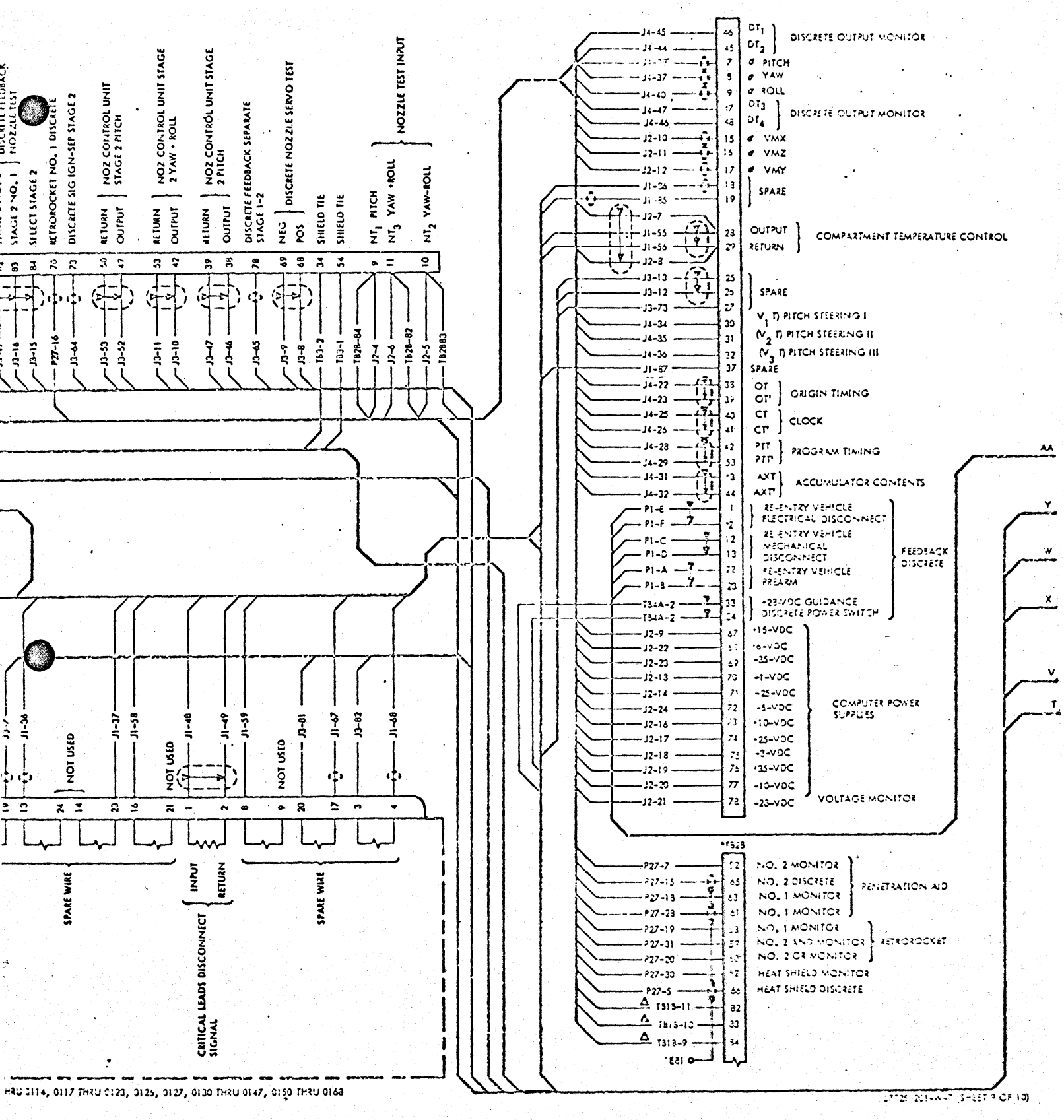
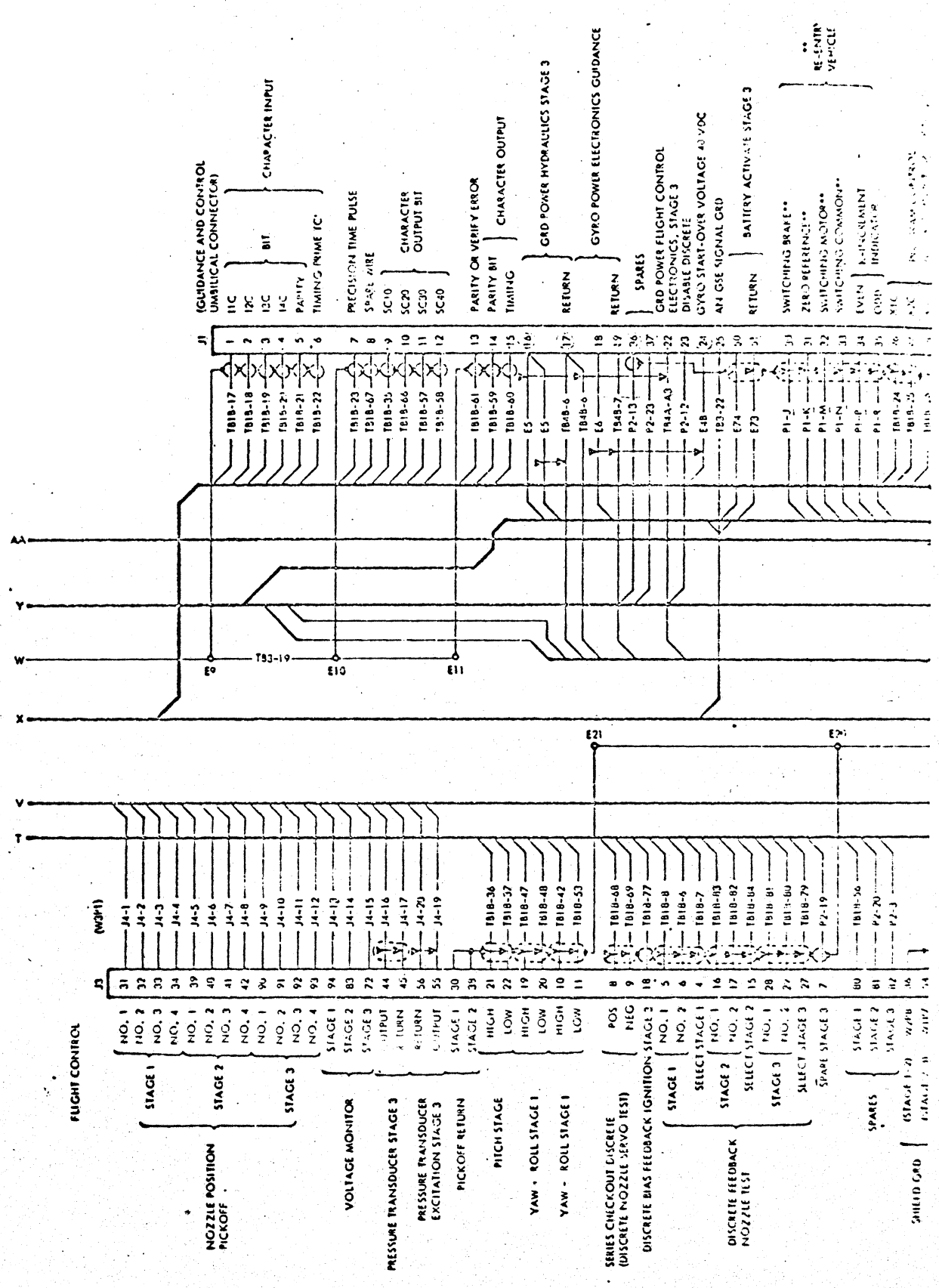
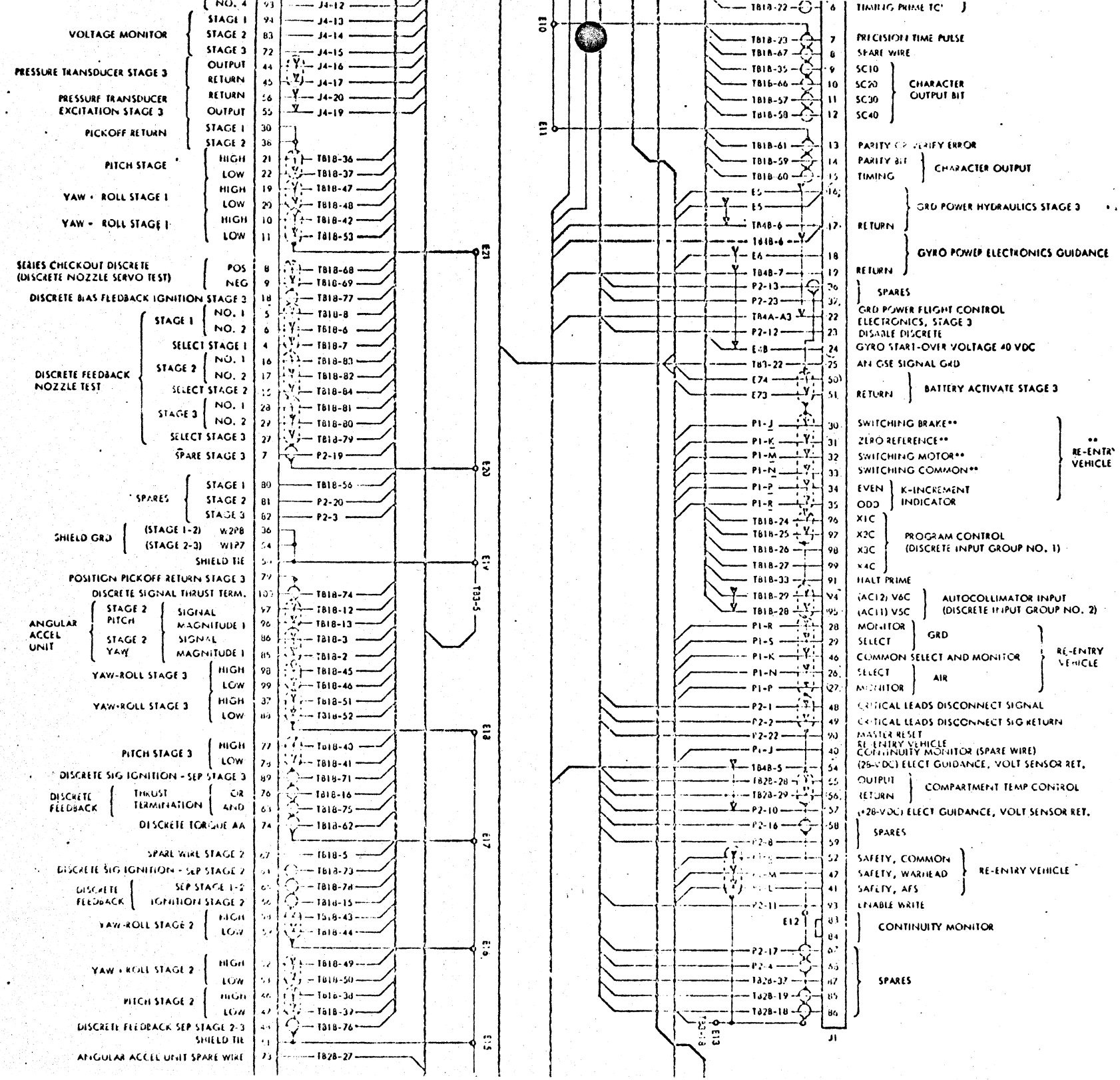


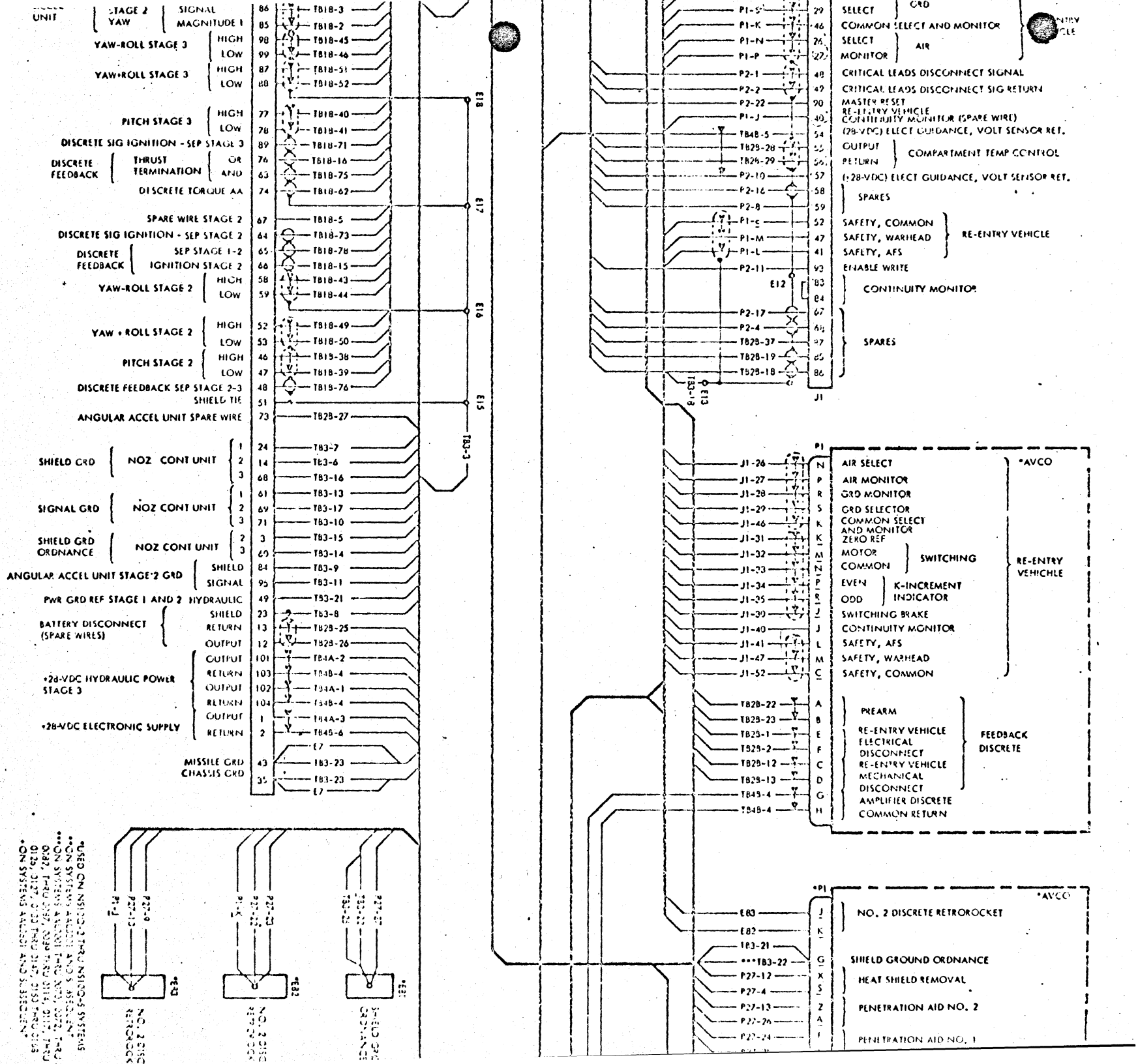
Figure 3-5. Missile Guidance Set Interconnection Wiring Diagram (Sheet 9 of 10)



Missile Guidance Set Interconnection Wiring Diagram (Sheet 10 of 10) p. 1



Missile Guidance Set Interconnection Wiring Diagram (Sheet 10 of 10) P. 2


UNIT
STAGE 2 YAW
SIGNAL MAGNITUDE 1
YAW-ROLL STAGE 3 HIGH
YAW-ROLL STAGE 3 LOW
YAW+ROLL STAGE 3 HIGH
YAW+ROLL STAGE 3 LOW
PITCH STAGE 3 HIGH
PITCH STAGE 3 LOW
DISCRETE SIG IGNITION - SEP STAGE 3
DISCRETE FEEDBACK THRUST TERMINATION OR AND
DISCRETE TORQUE AA
SPARE WIRE STAGE 2
DISCRETE SIG IGNITION - SEP STAGE 2
DISCRETE FEEDBACK SEP STAGE 1-2 IGNITION STAGE 2
YAW-ROLL STAGE 2 HIGH
YAW-ROLL STAGE 2 LOW
YAW + ROLL STAGE 2 HIGH
YAW + ROLL STAGE 2 LOW
PITCH STAGE 2 HIGH
PITCH STAGE 2 LOW
DISCRETE FEEDBACK SEP STAGE 2-3
SHIELD TIE
ANGULAR ACCEL UNIT SPARE WIRE
SHIELD GRD NOZ CONT UNIT
SIGNAL GRD NOZ CONT UNIT
SHIELD GRD ORDNANCE NOZ CONT UNIT
ANGULAR ACCEL UNIT STAGE 2 GRD SHIELD
ANGULAR ACCEL UNIT STAGE 2 GRD SIGNAL
PWR GRD REF STAGE 1 AND 2 HYDRAULIC
BATTERY DISCONNECT (SPARE WIRES) SHIELD
BATTERY DISCONNECT (SPARE WIRES) RETURN
BATTERY DISCONNECT (SPARE WIRES) OUTPUT
+28-VDC HYDRAULIC POWER STAGE 3 OUTPUT
+28-VDC HYDRAULIC POWER STAGE 3 RETURN
+28-VDC HYDRAULIC POWER STAGE 3 OUTPUT
+28-VDC HYDRAULIC POWER STAGE 3 RETURN
+28-VDC ELECTRONIC SUPPLY OUTPUT
+28-VDC ELECTRONIC SUPPLY RETURN
MISSILE GRD
CHASSIS GRD
SELECT
COMMON SELECT AND MONITOR
SELECT
MONITOR
AIR
CRITICAL LEADS DISCONNECT SIGNAL
CRITICAL LEADS DISCONNECT SIG RETURN
MASTER RESET
RE-ENTRY VEHICLE CONTINUITY MONITOR (SPARE WIRE)
(28-VDC) ELECT GUIDANCE, VOLT SENSOR RET.
OUTPUT
RETURN
COMPARTMENT TEMP CONTROL
(+28-VDC) ELECT GUIDANCE, VOLT SENSOR RET.
SPARES
SAFETY, COMMON
SAFETY, WARHEAD
SAFETY, AFS
RE-ENTRY VEHICLE
ENABLE WRITE
CONTINUITY MONITOR
SPARES
AIR SELECT
AIR MONITOR
GRD MONITOR
GRD SELECTOR
COMMON SELECT AND MONITOR
ZERO REF
MOTOR COMMON
SWITCHING
EVEN
ODD
K-INCREMENT INDICATOR
SWITCHING BRAKE
CONTINUITY MONITOR
SAFETY, AFS
SAFETY, WARHEAD
SAFETY, COMMON
*AVCO
RE-ENTRY VEHICHLE
PREARM
RE-ENTRY VEHICLE ELECTRICAL DISCONNECT
RE-ENTRY VEHICLE MECHANICAL DISCONNECT
AMPLIFIER DISCRETE COMMON RETURN
FEEDBACK DISCRETE
NO. 2 DISCRETE RETROROCKET
SHIELD GROUND ORDNANCE
HEAT SHIELD REMOVAL
PENETRATION AID NO. 2
PENETRATION AID NO. 1
*USED ON NSI00-2 THRU NSI00-5 SYSTEMS
**ON SYSTEMS
***ON SYSTEMS

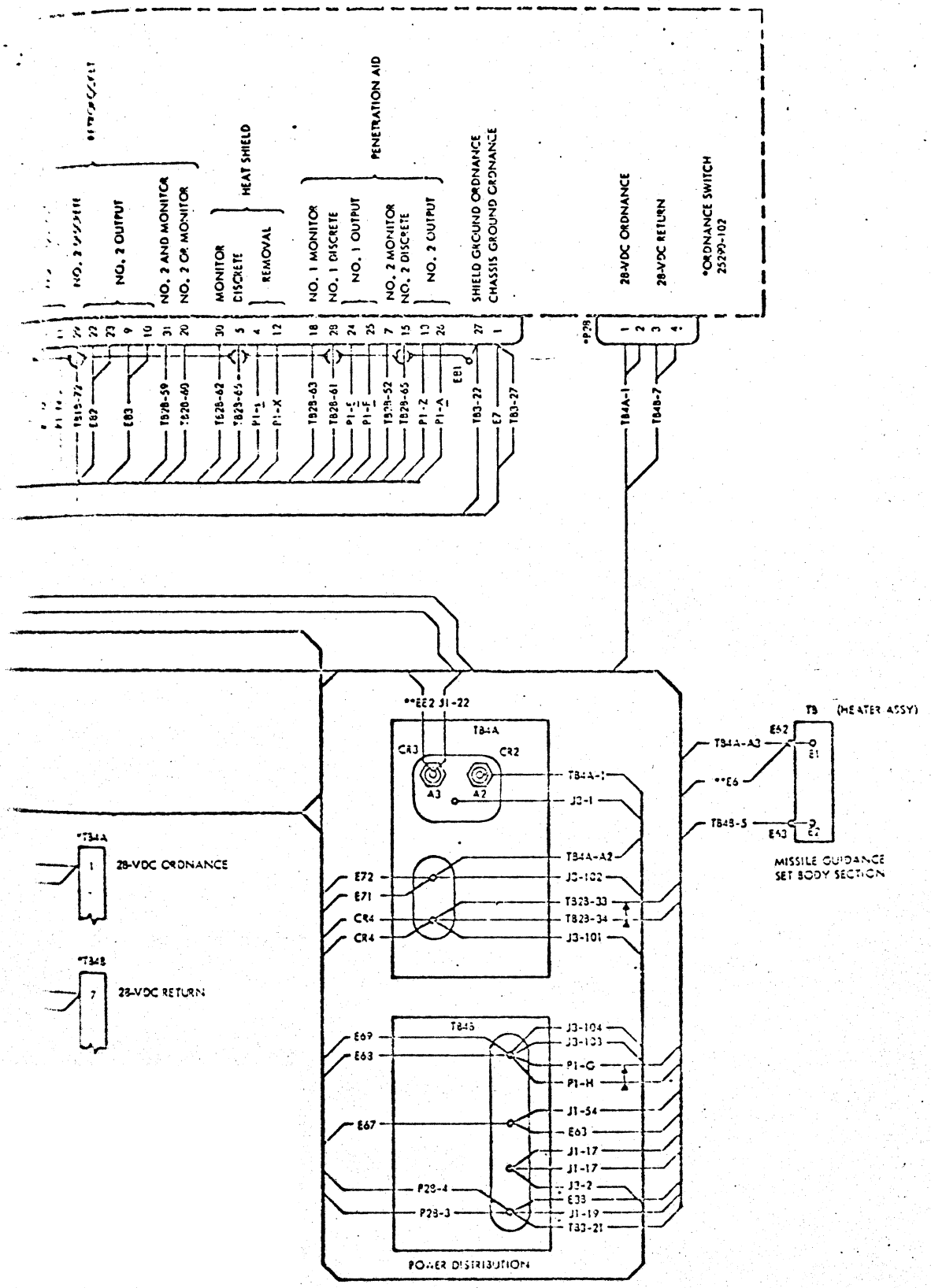


Figure 3-5. Missile Guidance Set Interconnection Wiring Diagram (Sheet 10 of 10)

APPENDIX C

FLIP-FLOP OUTPUTS ON J3, J4, AND J11

Card Slot	Ckt. No.	Pin No.	Name	Receptacle	Pin No.
J422 (A22)	1	1,2	F_C	J3	34
	2	D,E	N_P	J3	40
	3	J,K	I_P	J3	42
	4	11,12	P_2	J4	35
	5	T,U	O_2	J4	12
	6	C,D	O_3	J4	13
	7	30,31	P_3	J4	36
	8	M,N	O_4	J4	14
	9	37,38	O_I	J4	11
	10	V,W	P_1	J4	34
J426 (A26)	1		C_{B4}	J4	4
	2		C_{B3}	J4	3
	3		C_{P5}	J4	22
	4		C_{P4}	J4	21
	5		C_{B5}	J4	5
	6		C_{P2}	J4	19
	7	Same	C_{B2}	J4	2
	8		C_{P3}	J4	20
	9		C_{B1}	J4	1
	10		C_{P1}	J4	18
J428 (A28)	1		B_3	J3	3
	2		T_X	J3	49
	3		T_D	J3	50
	4		B_5	J3	5
	5		B_4	J3	4
	6	as	B_1	J3	1
	7		B_6	J3	6
	8		B_2	J3	2
	9		T_P	J3	48
	10		Q	J3	39
J430 (A30)	1		C_4	J4	9
	2		R_S	J4	38
	3		C_3	J4	8
	4		C_5	J4	10
	5	above	C_1	J4	6
	6		R_T	J4	39
	7		R_K	J4	37
	8		R_C	J3	36
	9		I_C	J3	24
	10		C_2	J4	7

APPENDIX C - continued

Card Slot	Ckt. No.	Pin No.	Name	Receptacle	Pin No.
J434 (A34)	1	1,2	N_D	J4	32
	2	D,E	K	J3	14
	3	J,K	E	J3	38
	4	11,12	A_K	J3	45
	5	T,U	I_D	J3	33
	6	C,D	A_P	J4	41
	7	30,31	D	J3	37
	8	M,N	J	J3	13
	9	37,38	A_{24}	J3	44
	10	V,W	AC	J3	23
J438 (A38)	1		D_5	J11	5
	2		D_R	J4	17
	3		D_C	J4	47
	4		G_1	J11	6
	5		G_3	J11	8
	6		G_2	JI1	7
	7	Same	D_3	J11	3
	8		D_2	J11	2
	9		D_4	J11	4
	10		D_1	J11	1
J440 (A40)	1		V_{11}	J11	9
	2		V_{12}	J11	10
	3		V_{13}	J11	11
	4		V_{23}	J11	20
	5		V_{22}	J11	19
	6	as	V_{21}	J11	18
	7		V_{31}	J11	26
	8		V_{32}	J11	27
	9		V_{33}	J11	28
	10		Spare	J11	
J523 (A58)	1		V_K	J4	40
	2		V_S	J4	41
	3		V_C	J3	35
	4		S_1	J4	23
	5	above	W_B	J4	43
	6		W_A	J4	42
	7		Z_1	J4	44
	8		Z_2	J4	45
	9		S_2	J4	24
	10		S_3	J4	25
J524 (A59)	1		S_{B3}	J4	28
	2		S_{B2}	J4	27
	3		L_X	J3	21
	4		N_C	J3	22
	5		L_C	J3	25
	6		S_{B1}	J4	26
	7		O_{B2}	J4	30
	8		L_P	J3	43
	9		O_{B1}	J4	29
	10		O_{B3}	J4	31

APPENDIX C - continued

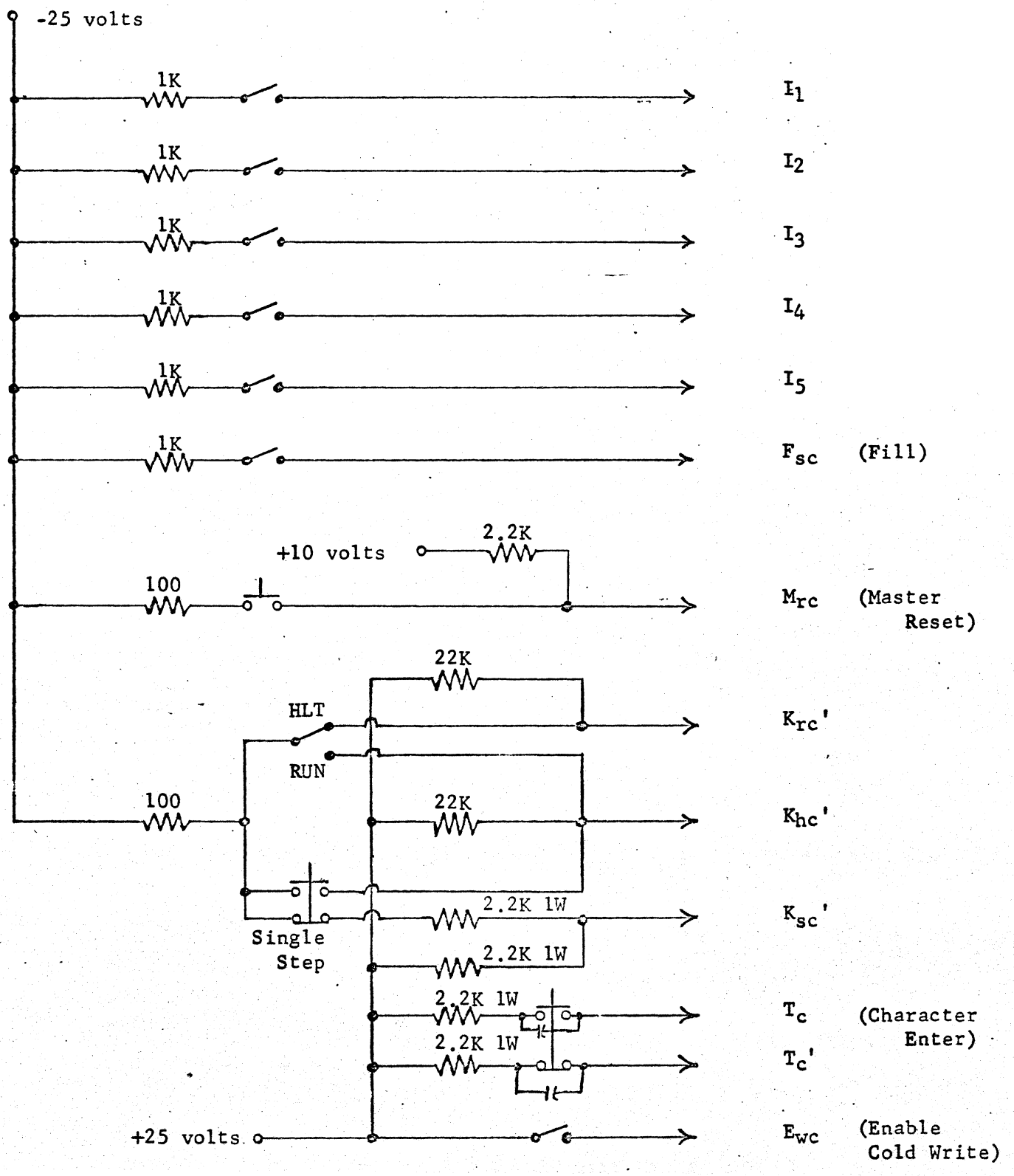
Card Slot	Ckt. No.	Pin No.	Name	Receptacle	Pin No.
J536 (A71)	1	1,2	V_{15}	J11	13
	2	D,E	V_{16}	J11	14
	3	J,K	V_{17}	J11	16
	4	11,12	V_{18}	J11	17
	5	T,U	Spare		
	6	$\overline{C}$,$\overline{D}$	V_{14}	J11	12
	7	30,31	M_{PX}	J3	46
	8	$\overline{M}$,$\overline{N}$	H_S	J3	16
	9	37,38	Spare		
	10	$\overline{V}$,$\overline{W}$	J_T	J4	46
J538 (A73)	1	Same as above	V_{34}	J11	29
	2		V_{35}	J11	30
	3		V_{36}	J11	31
	4		V_{37}	J11	32
	5		V_{25}	J11	22
	6		V_{26}	J11	23
	7		V_{38}	J11	33
	8		V_{27}	J11	24
	9		V_{24}	J11	21
	10		V_{28}	J11	25

The above listing was obtained by referencing the "Table of Term Locations for Flip-flop assemblies (sheet 1 of 2 and sheet 2 of 2)", on pages 5-211 and 5-212 of General Purpose Digital Computer (Model D17B), Technical Manual, continuity checks between the module card terminal and output terminals on J3, J4, and J11 then yielded the pin locations.

By monitoring these flip-flops and following the "Tables of Mode Transition Data" (pages 5-216 to 5-227, T.O. 11G2-10-5-3-5), the state of the computer may be observed.

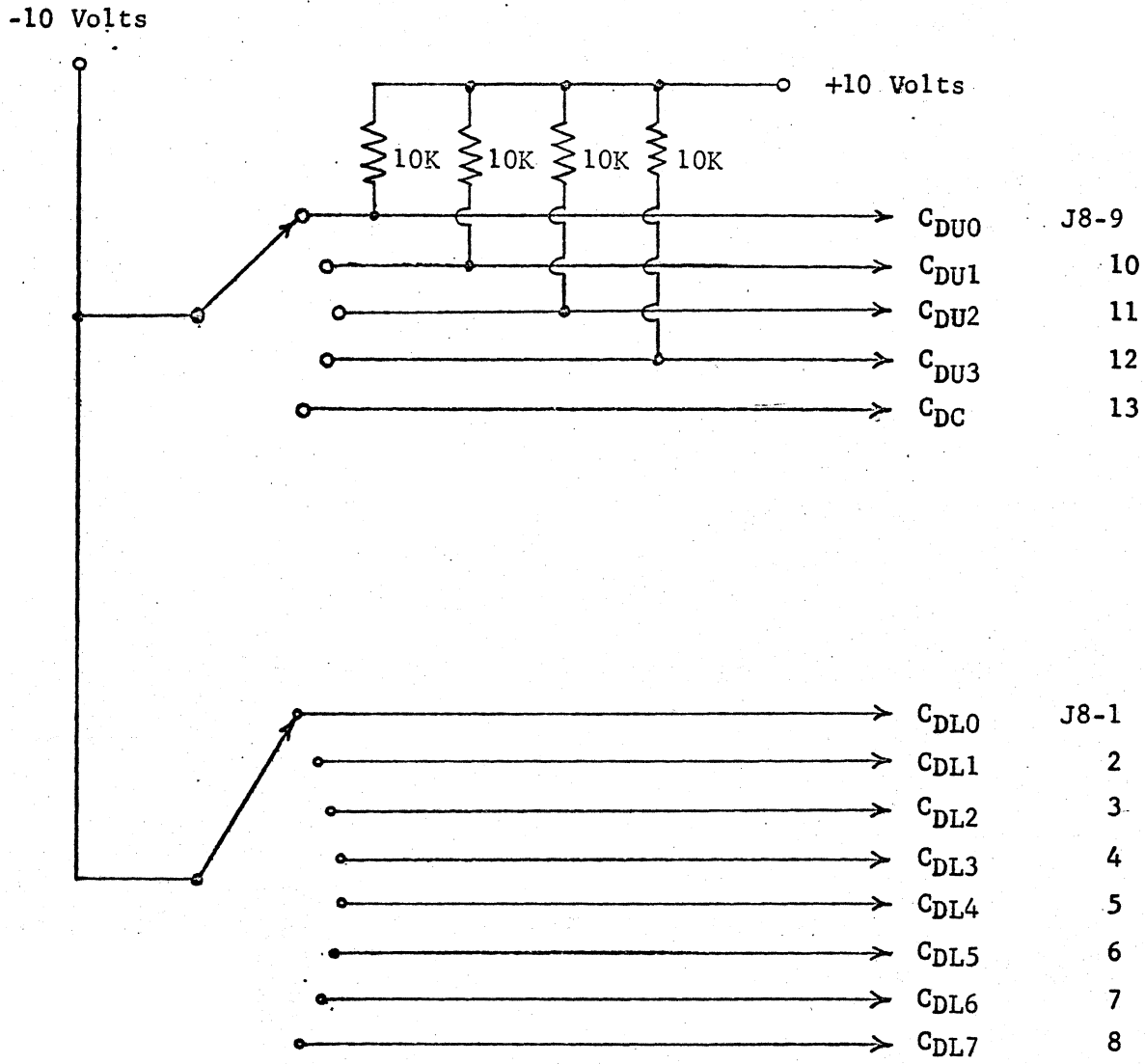
APPENDIX D

CONTROL PANEL SCHEMATIC



APPENDIX E

MULTIPLEXER SWITCHING SCHEMATIC



APPENDIX F

SAMPLE PROGRAM

This program clears the accumulator and then increments it with each disk revolution. The program starts at address 0 when the Master Reset is pressed. Location 0000 is a CLA instruction which clears the A register and adds the contents of location 0201 to the A register. The next instruction is taken from location 0001. This location contains an ADD instruction which adds the contents of location 0202 to the A register. The next instruction is taken from location 0001.

Order of entry is left to right as written here:

$I_3I_2I_1I_3I_2I_1I_3$----------I_2I_1.

LOCATION				CONTENTS							
Channel Number		Sector		Op Code	F	Sp-Next Instr. SF Flag SP		C Chan.		S Sector	
000	000	000	000	100	100	000	001	000	010	000	001
000	000	000	001	110	100	000	001	000	010	000	010
000	010	000	001	000	000	000	000	000	000	000	000
000	010	000	010	000	000	000	000	000	000	000	001

(pp. 48-82 & 107-108)