MINUTEMAN COMPUTER

USERS GROUP

D17B COMPUTER

DOCUMENTATION

Report MCUG-1-71

* Plug-In Assembly Locations
* Wire List
* Logic Equations

April 1971

PREFACE

This publication of the *MINUTEMAN COMPUTER USERS GROUP* contains plug-in assembly locations, a wire list, and logic equations for the D17B computers currently used in the Systems Laboratory at Tulane University. Arrangement of the material is specified by the table of contents on the following page which lists the first page number in each major section.

An attempt has been made to correct errors previously contained in this material. Additional errors and corrections will be distributed to *MCUG* members for the purpose of updating this publication as they are reported. Please send correspondence to the chairman of the *MCUG* at the following address.

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D17B COMPUTER

PLUG-IN ASSEMBLY LOCATIONS

All plug-in assemblies listed in the following section are part of D17B computers located in the Systems Laboratory at Tulane University.

Assembly Number	Receptacle Number	Nomenclature	Part Number
A1	J401	No. 3 Read Amplifier	57673-501
A2	J402	No. 3 Read Amplifier	57673-501
A3	J403	"	"
A4	J404	"	"
A5	J405	"	"
A6	J406	"	"
A7	J407	"	"
A8	J408	"	"
A9	J409	"	"
A10	J410	"	"
A11	J411	"	"
A12	J412	"	"
A13	J413	No. 128 Logic Network	57830-501
A14	J414	Write Amplifier Assembly	57606-501
A15	J415	No. 30 Logic Network	57669-501
A16	J416	No. 2 Write Electronic Switch	57759-501
A17	J417	No. 3 Clock Pulse Trigger Amplifier	57806-501
A18	J418	No. 2 Control Network	57836-501
A19	J419	Write Switch Control Network	57645-501
A20	J420	No. 112 Logic Network	57858-501
A21	J421	No. 113 Logic Network	57860-501
A22	J422	No. 2 Flip-Flop Network	57800-501
A23	J423	No. 114 Logic Network	57862-501
A24	J424	No. 115 Logic Network	57864-501
A25	J425	No. 116 Logic Network	57866-501
A26	J426	No. 2 Flip-Flop Network	57800-501
A27	J427	No. 111 Logic Network	57856-501
A28	J428	No. 2 Flip-Flop Network	57800-501
A29	J429	No. 117 Logic Network	57868-501
A30	J430	No. 2 Flip-Flop Network	57800-501
A31	J431	No. 129 Logic Network	57834-501
A32	J432	No. 119 Logic Network	57808-501
A33	J433	No. 120 Logic Network	57810-501
A34	J434	No. 2 Flip-Flop Network	57800-501
A35	J435	No. 21 Logic Network	57627-501
A36	J436	No. 122 Logic Network	57814-501
A37	J437	No. 123 Logic Network	57816-501
A38	J438	No. 2 Flip-Flop	57800-501
A39	J439	No. 124 Logic Network	57818-501

Assembly Number	Receptacle Number	Nomenclature	Part Number
A40	J440	No. 2 Flip-Flop Network	57800-501
A41	J441	No. 6 Input/Output Network	57765-501
A42	J442	No. 101 Input/Output Network	57826-501
A43	J443	No. 101 Input/Output Network	57826-501
A44	J444	"	"
A45	J445	"	"
A46	J446	"	"
A47	J447	"	"
A48	J448	Cable Electronic Control Amplifier	57820-501
A52	P20-	Magnetic Memory Assembly	55380-304
A53	J518	Write Amplifier Assembly	57606-501
A54	J519	No. 107 Logic Network	57848-501
A55	J520	Write Amplifier Assembly	57606-501
A56	J521	No. 108 Logic Network	57850-501
A57	J522	No. 109 Logic Network	57852-501
A58	J523	No. 2 Flip-Flop Network	57800-501
A59	J524	No. 2 Flip-Flop Network	57800-501
A60	J525	No. 110 Logic Network	57854-501
A61	J526	No. 103 Logic Network	57846-501
A62	J527	No. 2 Logic Driver Electronic Control Amplifier	57824-501
A63	J528	No. 4 Logic Network	57711-501
A64	J529	No. 102 Logic Network	57844-501
A65	J530	No. 2 Logic Driver Electronic Control Amplifier	57824-501
A68	J533	No. 101 Logic Network	57842-501
A69	J534	No. 2 Logic Driver Electronic Control Amplifier	57824-501
A70	J535	No. 126 Logic Network	57822-501
A71	J536	No. 2 Flip-Flop Network	57800-501
A72	J537	No. 127 Logic Network	57828-501
A73	J538	No. 2 Flip-Flop Network	57800-501
A74	J539	No. 3 Digital-to-Analog Converter	57812-501
A75	J540	No. 3 Digital-to-Analog Converter	57812-501
A76	J541	No. 4 Voltage Output D-C Amplifier	57870-501
A77	J542	No. 4 Voltage Output D-C Amplifier	57870-501
A78	J543	"	"
A79	J544	No. 2 Voltage Output Electronic Switch	57840-501
A81	J546	No. 2 Voltage Output Electronic Switch	57840-501
A83	J548	No. 104 Input/Output Network	57832-501

D17B COMPUTER

WIRE LIST

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J1 -30	J518-29	10V
J1 -31	J418- L	10V
J401-/J	J401-30	10V
J401-30	J402-/J	10V
J402-/J	J402-30	10V
J402-30	J403-/J	10V
J403-/J	J403-30	10V
J403-30	J404-/J	10V
J404-/J	J404-30	10V
J404-30	J405-/J	10V
J405-/J	J405-30	10V
J405-30	J406-/J	10V
J406-/J	J406-30	10V
J406-30	J407-/J	10V
J407-/J	J407-30	10V
J407-30	J408-/J	10V
J408-/J	J408-30	10V
J408-30	J409-/J	10V
J409-/J	J409-30	10V
J409-30	J410-/J	10V
J410-/J	J410-30	10V
J410-30	J411-/J	10V
J411-/J	J411-30	10V
J411-30	J412-/J	10V
J412-/J	J412-30	10V
J412-30	J414-/H	10V
J414-/H	J414-29	10V
J414-29	J418- L	10V
J417-39	J418- M	10V
J418- L	J418-10	10V
J418- M	J418-11	10V
J418-10	J518-29	10V
J418-10	J418-11	10V
J418-11	J422- Z	10V
J422- Z	J426- Z	10V
J426- Z	J428- Z	10V
J428- Z	J430- Z	10V
J430- Z	J434- Z	10V
J434- Z	J438- Z	10V
J438- Z	J440- Z	10V
J440- Z	J441-22	10V
J441-21	J441-22	10V
J441-21	J442- 2	10V
J442- 2	J443- 2	10V
J443- 2	J444- 2	10V
J444- 2	J445- 2	10V
J445- 2	J446- 2	10V
J446- 2	J447- 2	10V
J447- 2	J448- C	10V
J448- C	J538- Z	10V
J518-/H	J518-29	10V
J518-/H	J520-29	10V
J520-/H	J520-29	10V
J520-/H	J523- Z	10V
J523- Z	J524- Z	10V
J524- Z	J527- Z	10V
J527- X	J527- Z	10V
J527- X	J530- X	10V
J530- X	J530- Z	10V
J530- Z	J534- Z	10V
J534- X	J534- Z	10V
J534- X	J536- Z	10V
J536- Z	J538- Z	10V
J1 - 9	J518-23	15V
J414- Y	J414- N	15V
J414- Y	J414-/A	15V
J414-/A	J414-/P	15V

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J414-/A	J414-23	15V
J414-/P	J414-/Y	15V
J414-/Y	J417-/V	15V
J414-23	J416- Y	15V
J416- Y	J416-21	15V
J416-21	J518-23	15V
J417-/V	J418-/U	15V
J418-/U	J418-39	15V
J418-39	J419-/E	15V
J518-/A	J518-23	15V
J518-/A	J520-23	15V
J520-/A	J520-23	15V
J520-/A	J544- V	15V
J544- V	J546- V	15V
J1 -10	J419- C	15V
J419- A	J419- 1	15V
J419- A	J419- B	15V
J419- B	J419- C	15V
J419- 1	J419- 2	15V
P201-45	J419- 2	15V
P201-49	J419- 1	15V
P202-45	J419- A	15V
P202-49	J419- B	15V
J1 -16	J417-36	2V
J1 -18	J518-20	2V
J1 -19	J417-36	2V
J1 -20	J523-22	2V
J1 -21	J422-22	2V
J401-/L	J401-32	2V
J401-/L	J417-37	2V
J401-32	J402-/L	2V
J402-/L	J402-32	2V
J402-32	J403-/L	2V
J403-/L	J403-32	2V
J403-32	J404-/L	2V
J404-/L	J404-32	2V
J404-32	J405-/L	2V
J405-/L	J405-32	2V
J405-32	J406-/L	2V
J406-/L	J406-32	2V
J406-32	J407-/L	2V
J407-/L	J407-32	2V
J407-32	J408-/L	2V
J408-/L	J408-32	2V
J408-32	J409-/L	2V
J409-/L	J409-32	2V
J409-32	J410-/L	2V
J410-/L	J410-32	2V
J410-32	J411-/L	2V
J411-/L	J411-32	2V
J411-32	J412-/L	2V
J412-/L	J412-32	2V
J412-32	J414- X	2V
J414- X	J414-20	2V
J414-20	J520- X	2V
J417-36	J417-37	2V
J417-37	J434-23	2V
J422-22	J422-23	2V
J422-23	J426-23	2V
J426-22	J426-23	2V
J426-22	J428-22	2V
J428-22	J428-23	2V
J428-23	J430-23	2V
J430-22	J430-23	2V
J430-22	J434-22	2V
J434-22	J434-23	2V

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J434-23	J440-23	2V
J438-22	J538-22	2V
J438-22	J438-23	2V
J438-23	J440-23	2V
J440-22	J440-23	2V
J518- X	J518-20	2V
J518- X	J520-20	2V
J520- X	J520-20	2V
J523-22	J523-23	2V
J523-23	J524-22	2V
J524-22	J524-23	2V
J524-23	J536-23	2V
J536-22	J536-23	2V
J536-22	J538-23	2V
J538-22	J538-23	2V
J7 -25	J440-22	2V
J1 - 7	J417- B	25V
J416-/H	J416-29	25V
J416-29	J417- 1	25V
J417- B	J417- 1	25V
J417- 1	J418-/P	25V
J418-/P	J418-35	25V
J418-35	J441-20	25V
J441-20	J442- 5	25V
J442- 4	J442- 5	25V
J442- 4	J443- 4	25V
J443- 4	J444- 4	25V
J443- 4	J443- 5	25V
J444- 4	J445- 4	25V
J444- 4	J444- 5	25V
J445- 4	J446- 4	25V
J445- 4	J445- 5	25V
J446- 4	J447- 4	25V
J446- 4	J446- 5	25V
J447- 4	J447- 5	25V
J447- 5	J448-17	25V
J448-17	J548-20	25V
J539- J	J539- 8	25V
J539- J	J540- 8	25V
J540- J	J540- 8	25V
J540- J	J541-/C	25V
J541-/C	J542-/C	25V
J542-/C	J543-/C	25V
J543-/C	J548-21	25V
J548-20	J548-21	25V
J1 - 1	J419- U	35V
J419- U	J419-17	35V
J419-17	J541- Z	35V
J448- A	J543- Z	35V
J541- Z	J542- Z	35V
J542- Z	J543- Z	35V
J2 -20	J539-31	5V P
J2 -22	J539-31	5V P
J539-/K	J540-31	5V P
J539-/K	J539-31	5V P
J540-/K	J540-31	5V P
J1 - 5	J419-/W	6V
J401- U	J401-17	6V
J401-/F	J401-28	6V
J401-17	J402- U	6V
J401-28	J402-/F	6V
J402- U	J402-17	6V
J402-/F	J402-28	6V
J402-17	J403- U	6V
J402-28	J403-/F	6V

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J403- U	J403-17	6V
J403-/F	J403-28	6V
J403-17	J404- U	6V
J403-28	J404-/F	6V
J404- U	J404-17	6V
J404-/F	J404-28	6V
J404-17	J405- U	6V
J404-28	J405-/F	6V
J405- U	J405-17	6V
J405-/F	J405-28	6V
J405-17	J406- U	6V
J405-28	J406-/F	6V
J406- U	J406-17	6V
J406-/F	J406-28	6V
J406-17	J407- U	6V
J406-28	J407-/F	6V
J407- U	J407-17	6V
J407-/F	J407-28	6V
J407-17	J408- U	6V
J407-28	J408-/F	6V
J408- U	J408-17	6V
J408-/F	J408-28	6V
J408-17	J409- U	6V
J408-28	J409-/F	6V
J409- U	J409-17	6V
J409-/F	J409-28	6V
J409-17	J410- U	6V
J409-28	J410-/F	6V
J410- U	J410-17	6V
J410-/F	J410-28	6V
J410-17	J411- U	6V
J410-28	J411-/F	6V
J411- U	J411-17	6V
J411-/F	J411-28	6V
J411-17	J412- U	6V
J411-28	J412-/F	6V
J412- U	J412-17	6V
J412-/F	J412-28	6V
J412-17	J412-28	6V
J412-28	J419-/X	6V
J417-/R	J418-/H	6V
J417-/R	J417-/S	6V
J418-/H	J418-29	6V
J419-/W	J419-/X	6V
J419-/W	J418-29	6V
J419-/X	J541-41	6V
J541-41	J542-41	6V
J542-41	J543-41	6V
J1 -26	J417-/A	-1V
J1 -27	J417-/E	-1V
J417-/A	J417-/B	-1V
J417-/B	J417-/C	-1V
J417-/C	J417-/D	-1V
J417-/D	J417-/E	-1V
J2 - 3	J518-25	-10V
J2 - 4	J414-25	-10V
J2 -42	J544-/A	-10V
J414-/C	J414-25	-10V
J414-25	J416-23	-10V
J416-23	J417-10	-10V
J417-10	J417-11	-10V
J417-11	J418- N	-10V
J418- N	J418-12	-10V
J418-12	J419-/D	-10V
J419-/D	J419-26	-10V
J419-26	J422-25	-10V
J422-24	J422-25	-10V

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J422-25	J426-24	-10V
J426-24	J426-25	-10V
J426-25	J428-24	-10V
J428-24	J428-25	-10V
J428-25	J430-25	-10V
J430-24	J430-25	-10V
J430-25	J431-/D	-10V
J431-/D	J433-/M	-10V
J433-/L	J433-32	-10V
J433-/L	J433-/M	-10V
J433-32	J434-25	-10V
J434-24	J434-25	-10V
J434-24	J438-25	-10V
J438-24	J438-25	-10V
J438-24	J440-24	-10V
J440-24	J440-25	-10V
J440-25	J441-/V	-10V
J441- 1	J441-43	-10V
J441- 1	J548- W	-10V
J441-/V	J441-/W	-10V
J441-/W	J441-43	-10V
J518-/C	J518-25	-10V
J518-/C	J520-25	-10V
J520-/C	J520-25	-10V
J520-/C	J523-24	-10V
J523-24	J523-25	-10V
J523-25	J524-25	-10V
J524-24	J524-25	-10V
J524-24	J526-26	-10V
J526-26	J526-27	-10V
J526-27	J527-/B	-10V
J527-/A	J527-/B	-10V
J527-/A	J528-22	-10V
J528- N	J528-12	-10V
J528- N	J529-11	-10V
J528- P	J528- N	-10V
J528-22	J528- P	-10V
J529- M	J529-11	-10V
J529- M	J530-18	-10V
J530-/A	J530-/B	-10V
J530-/A	J530-18	-10V
J530-/B	J533-12	-10V
J533- N	J533-12	-10V
J533- N	J534-/A	-10V
J534-/A	J534-/B	-10V
J534-/B	J536-25	-10V
J536-24	J536-25	-10V
J536-24	J537-23	-10V
J537-23	J538-24	-10V
J538-24	J538-25	-10V
J538-25	J539-37	-10V
J539-/S	J539-37	-10V
J539-/S	J540-37	-10V
J540-/S	J540-37	-10V
J540-/S	J544-21	-10V
J544-/A	J544-21	-10V
J544-/A	J546-/A	-10V
J544-20	J544-21	-10V
J546-/A	J548-19	-10V
J548- W	J548-19	-10V
J2 - 1	J412-33	-10V 1
J2 - 2	J401-/M	-10V 1
J401-/M	J401-33	-10V 1
J401-33	J402-/M	-10V 1
J402-/M	J402-33	-10V 1
J402-33	J403-/M	-10V 1
J403-/M	J403-33	-10V 1
J403-33	J404-/M	-10V 1
J404-/M	J404-33	-10V 1
J404-33	J405-/M	-10V 1
J405-/M	J405-33	-10V 1
J405-33	J406-/M	-10V 1
J406-/M	J406-33	-10V 1
J406-33	J407-/M	-10V 1
J407-/M	J407-33	-10V 1
J407-33	J408-/M	-10V 1
J408-/M	J408-33	-10V 1
J408-33	J409-/M	-10V 1
J409-/M	J409-33	-10V 1
J409-33	J410-/M	-10V 1
J410-/M	J410-33	-10V 1
J410-33	J411-/M	-10V 1
J411-/M	J411-33	-10V 1
J411-33	J412-/M	-10V 1
J412-/M	J412-33	-10V 1
J2 -24	J444- A	-25V
J2 -25	J435- R	-25V
J2 -26	J537-14	-25V
J2 -27	J519-14	-25V
J2 -28	J413- R	-25V
J413- R	J413-14	-25V
J413-14	J415- R	-25V
J415- R	J415-14	-25V
J415-14	J417-33	-25V
J417-32	J417-33	-25V
J417-32	J418-/A	-25V
J418-/A	J418-23	-25V
J418-23	J419-/B	-25V
J419- Z	J420- R	-25V
J419- Z	J419-/B	-25V
J420- R	J420-14	-25V
J420-14	J421- R	-25V
J421- R	J421-14	-25V
J421-14	J423- R	-25V
J423- R	J423-14	-25V
J423-14	J424- R	-25V
J424- R	J424-14	-25V
J424-14	J425- R	-25V
J425- R	J425-14	-25V
J425-14	J427- R	-25V
J427- R	J427-14	-25V
J427-14	J429- R	-25V
J429- R	J429-14	-25V
J429-14	J431- R	-25V
J431- R	J431-14	-25V
J431-14	J432- R	-25V
J432- R	J432-14	-25V
J432-14	J433- R	-25V
J433- R	J433-14	-25V
J433-14	J443-/Y	-25V
J433-14	J534-20	-25V
J435- R	J435-14	-25V
J435-14	J436- R	-25V
J436- R	J436-14	-25V
J436-14	J437-14	-25V
J437-14	J439- R	-25V
J439- R	J439-14	-25V
J439- 4	J439-14	-25V
J439- 4	J441- A	-25V
J441- A	J441-41	-25V
J441- A	J442- A	-25V
J441-/Y	J441-42	-25V
J441-41	J441-42	-25V
J441-42	J442-/Y	-25V
J442- A	J443- A	-25V
J442-/Y	J443-/Y	-25V
J443-/Y	J447-/U	-25V
J444- A	J444-/Y	-25V

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J444- A	J445- A	-25V
J444-/Y	J445-/Y	-25V
J445- A	J446- A	-25V
J445-/Y	J446-/Y	-25V
J446- A	J447- A	-25V
J446-/Y	J447-/Y	-25V
J447- A	J448- D	-25V
J447-/U	J447-41	-25V
J447-/U	J448- 5	-25V
J447-/Y	J447-41	-25V
J448- D	J448- 4	-25V
J448- 4	J448- 5	-25V
J448- 4	J548- H	-25V
J519- R	J519-14	-25V
J519- R	J521-14	-25V
J521- R	J521-14	-25V
J521- R	J522-14	-25V
J522- R	J522-14	-25V
J522- R	J525-14	-25V
J525- R	J525-14	-25V
J525- R	J526-14	-25V
J526- R	J526-14	-25V
J526- U	J527-20	-25V
J526- U	J526-14	-25V
J527-20	J527-22	-25V
J527-22	J528-14	-25V
J528- R	J528-14	-25V
J528- R	J529-14	-25V
J529- R	J529-14	-25V
J529- R	J530-20	-25V
J529- 6	J533-14	-25V
J529- 6	J529-14	-25V
J530-20	J530-22	-25V
J533- R	J533-14	-25V
J533- R	J534-20	-25V
J534-/F	J534-22	-25V
J534-20	J534-22	-25V
J537- R	J537-14	-25V
J537- R	J539-12	-25V
J537- T	J537- R	-25V
J539- N	J539-12	-25V
J539- N	J540-12	-25V
J540- N	J540-12	-25V
J540- N	J541- X	-25V
J541- X	J542- X	-25V
J542- X	J543- X	-25V
J543- W	J543- X	-25V
J543- X	J543- Y	-25V
J543- Y	J548-24	-25V
J548- H	J548-24	-25V
J1 -13	J416- E	-3V
J414-/B	J414-24	-3V
J414-21	J414-24	-3V
J414-24	J416-/B	-3V
J416- E	J416- 5	-3V
J416- E	J416- K	-3V
J416- K	J416-/B	-3V
J416- K	J416- 9	-3V
J416- 5	J443- 1	-3V
J416- 9	J442- 1	-3V
J416-/B	J416-24	-3V
J416-24	J419-/A	-3V
J419-/A	J419-23	-3V
J442- 1	J443- 1	-3V
J443- 1	J444- 1	-3V
J444- 1	J445- 1	-3V
J445- 1	J446- 1	-3V
J446- 1	J447- 1	-3V

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J447- 1	J448- L	-3V
J448- F	J448- L	-3V
J448- F	J448- 3	-3V
J448- 3	J548-/A	-3V
J518-/B	J518-24	-3V
J518-/B	J520-24	-3V
J520-/B	J520-24	-3V
J520-/B	J527-/X	-3V
J527- C	J527- D	-3V
J527- C	J530- C	-3V
J527-/W	J530-/W	-3V
J527-/W	J527-/X	-3V
J530- C	J534- C	-3V
J530- C	J530- D	-3V
J530-/W	J534-/W	-3V
J530-/W	J530-/X	-3V
J534- C	J534- D	-3V
J534- D	J534-/W	-3V
J534-/W	J534-/X	-3V
J534-/X	J548-34	-3V
J548-/A	J548-22	-3V
J548-22	J548-34	-3V
J1 - 3	J442- Z	-35V
J442- Z	J443- Z	-35V
J443- Z	J444- Z	-35V
J444- Z	J445- Z	-35V
J445- Z	J446- Z	-35V
J446- Z	J447- Z	-35V
J1 -34	J416-19	-5V
J1 -35	J430- Y	-5V
J1 -36	J438- Y	-5V
J1 -37	J536-21	-5V
J416-19	J416-20	-5V
J416-20	J426-21	-5V
J426- Y	J426-21	-5V
J426-21	J428- Y	-5V
J428- Y	J428-21	-5V
J428-21	J434- Y	-5V
J430- Y	J430-21	-5V
J430-21	J434- Y	-5V
J434- Y	J434-21	-5V
J434-21	J448- H	-5V
J438- Y	J438-21	-5V
J438-21	J440- Y	-5V
J440- Y	J440-21	-5V
J440-21	J448- H	-5V
J448- H	J538- Y	-5V
J536- Y	J536-21	-5V
J536- Y	J538-21	-5V
J538- Y	J538-21	-5V
J2 - 9	J539- 1	-5V P
J2 -11	J539- 1	-5V P
J539- A	J539- 1	-5V P
J539- A	J540- 1	-5V P
J540- A	J540- 1	-5V P
J1 -38	J417-/W	-5V
J1 -39	J523-21	-5V
J417-/W	J419-30	-5V
J419-30	J422-21	-5V
J422- Y	J422-21	-5V
J422-21	J524- Y	-5V
J523- Y	J523-21	-5V
J523- Y	J524-21	-5V
J524- Y	J524-21	-5V

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J3 -23	J526-34	AC
J433-40	J434-/V	AC
J433-40	J533- J	AC
J434-/V	J434-/W	AC
J437- N	J533- J	AC
J526-34	J533- J	AC
J413- N	J437-/A	AC/
J433-28	J434-/X	AC/
J433-28	J437-/A	AC/
J434-/X	J434-/Y	AC/
J3 -45	J434-12	AK
J413- W	J424-19	AK
J423-37	J424-19	AK
J423-37	J433-43	AK
J433-43	J434-11	AK
J434-11	J533- V	AK
J434-11	J434-12	AK
J434-12	J437-16	AK
J533- V	J537- M	AK
J413-/C	J423-/M	AK/
J423-/M	J424-/B	AK/
J424-/B	J433-/T	AK/
J433-/T	J434- S	AK/
J434- R	J434- S	AK/
J434- S	J437-23	AK/
J437-23	J537- X	AK/
J3 -41	J525-13	AP
J425- E	J437- A	AP
J425- E	J525-13	AP
J433-/S	J434-/D	AP
J434-/C	J437- A	AP
J434-/C	J434-/D	AP
J434-/D	J439-34	AP
J437- A	J537-/S	AP
J425-/R	J433-41	AP/
J433-41	J434-/H	AP/
J434-/F	J437- B	AP/
J434-/F	J434-/H	AP/
J434-/H	J439-30	AP/
J437- B	J537-/R	AP/
P200- 9	J407- E	AR
J3 -19	J525- B	AX
J407-38	J413-23	AX
J413-23	J420-23	AX
J420-23	J423-/F	AX
J420-23	J519- C	AX
J448- J	J526- 5	AX
J519- C	J521-/P	AX
J519- C	J525- B	AX
J521-/P	J522-/L	AX
J525- B	J526- 5	AX
J407-39	J413- P	AX/
J413- P	J421-/F	AX/
J421-/F	J424-/F	AX/
J424-/F	J525- J	AX/
J519-22	J525- J	AX/
J519-22	J521-/S	AX/
J521-/S	J522-38	AX/
J522-38	J526-/P	AX/
J429- 3	J433-10	AX/A--
J431-/E	J433-10	AX/A--
J433-10	J437- F	AX/A--
J437- F	J537- L	AX/A--
J527-42	J527-43	AX/A--
J527-42	J535-43	AX/A--
J535-43	J537- L	AX/A--
J526-/T	J527-/T	AX/A--D
J429- H	J527- F	AXA--
J429- H	J433- L	AXA--
J431-/F	J435- W	AXA--
J431-/F	J437-38	AXA--
J433- L	J435- W	AXA--
J433- L	J535- C	AXA--
J527- F	J527- H	AXA--
J535- C	J537- 6	AXA--
J526- 1	J527- 1	AXA--D
J413-/V	J519- H	AXP/-
J519- H	J526-39	AXP/-
J5 - 7	J448- 8	AXT
J5 - 8	J448- K	AXT/
P201-15	J414- F	A23W
P201-14	J414- C	A23W/
J3 -44	J424-35	A24
J413- 1	J425- J	A24
J424-35	J425- J	A24
J425- J	J432-23	A24
J432-23	J434-37	A24
J432-23	J537- 3	A24
J434-37	J434-38	A24
J434-37	J435-36	A24
J413- L	J425-/T	A24/
J425-/T	J434-/U	A24/
J434-/T	J434-/U	A24/
J434-/T	J435-/L	A24/
J435-/L	J436-/M	A24/
J436-/M	J537- 4	A24/
J427- P	J529- X	BLU3-
J427- P	J525- N	BLU3-
J432-37	J435- L	BLU3-
J435- L	J529- X	BLU3-
J529-40	J530- K	BLU5--
J530- J	J530- K	BLU5--
J529- K	J530- 8	BLU5--D
J525-26	J530- 6	BLU7--
J529-36	J530- 6	BLU7--
J530- 5	J530- 6	BLU7--
J529- J	J530- 7	BLU7--D
J427-25	J530-27	BLO--
J529-39	J530-28	BLO--
J530-27	J530-28	BLO--
J529-/E	J530-29	BLO--D

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J432-/T	J530-36	BL1--
J525-37	J530-37	BL1--
J529-42	J530-37	BL1--
J530-36	J530-37	BL1--
J529-/N	J530-38	BL1--D
J427- D	J435- M	BL2--
J427- D	J528- 1	BL2--
J528- 1	J530-/L	BL2--
J529-35	J530-/M	BL2--
J530-/L	J530-/M	BL2--
J529-/H	J530-34	BL2--D
J529-38	J530-15	BM3--
J529-38	J533-/T	BM3--
J530-14	J530-15	BM3--
J529-20	J530-17	BM3--D
J432-41	J529- 9	BSU0--
J529- 9	J530-39	BSU0--
J530-39	J530-40	BSU0--
J529-/P	J530-41	BSU0--D
J529-34	J533-/H	BU03--
J530- V	J530- W	BU03--
J530- W	J533-/H	BU03--
J529- Y	J530-19	BU03--D
J3 - 1	J424-27	B1
J424-27	J428-/C	B1
J427- K	J428-/C	B1
J427- K	J433- D	B1
J428-/C	J428-/D	B1
J428-/D	J432-38	B1
J433- D	J435-13	B1
J433- D	J529-37	B1
J3 - 7	J427-23	B1/
J423-33	J428-/H	B1/
J427-23	J428-/F	B1/
J427-23	J429-18	B1/
J428-/F	J428-/H	B1/
J429-18	J433- 8	B1/
J433- 8	J529-19	B1/
J3 - 2	J529-18	B2
J413- 6	J529-18	B2
J428-/M	J431- 7	B2
J428-/M	J428-/N	B2
J428-/M	J432-40	B2
J431- 7	J529-18	B2
J3 - 8	J525- L	B2/
J427- 6	J431- K	B2/
J427- 6	J525- L	B2/
J427- 6	J529-30	B2/
J428-/P	J428-/R	B2/
J428-/P	J432-24	B2/
J431- K	J435- K	B2/
J431- K	J432-24	B2/
J3 - 3	J428- 1	B3
J425-/X	J431-/L	B3
J428- 1	J528- 2	B3
J428- 1	J428- 2	B3

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J428- 2	J431-/L	B3
J431-/L	J432-/U	B3
J432-/U	J437-41	B3
J521-/J	J529- W	B3
J528- 2	J529- W	B3
J3 - 9	J525- 8	B3/
J425-35	J431-18	B3/
J428- B	J428- C	B3/
J428- B	J525- 8	B3/
J428- B	J529- C	B3/
J428- C	J431-18	B3/
J3 - 4	J525-/T	B4
J428- T	J428- U	B4
J428- T	J529- 8	B4
J525-/T	J533-/P	B4
J529- 8	J533-/P	B4
J533-/P	J537-42	B4
J3 -10	J428- X	B4/
J428- W	J428- X	B4/
J428- W	J529- V	B4/
J528-/M	J529- V	B4/
J3 - 5	J428-12	B5
J428-11	J528- 3	B5
J428-11	J428-12	B5
J428-12	J432-/V	B5
J436- 8	J529- D	B5
J528- 3	J529- D	B5
J3 -11	J428- R	B5/
J421-38	J431-/S	B5/
J428- R	J428- S	B5/
J428- R	J529-26	B5/
J428- S	J431-/S	B5/
J431-/S	J437- V	B5/
J3 - 6	J428-31	B6
J428-30	J428-31	B6
J428-30	J529- A	B6
J529- A	J537-20	B6
J3 -12	J427-26	B6/
J427-26	J428-/K	B6/
J427-26	J431-19	B6/
J428-/K	J428-/L	B6/
J431-19	J529-27	B6/
J529-27	J537-21	B6/
J423-34	J435- V	B6M1--
J435- V	J530- A	B6M1--
J525-/S	J529-43	B6M1--
J529-43	J530- B	B6M1--
J530- A	J530- B	B6M1--
J529- H	J530- E	B6M1--D
J406-15	J417-/X	CAC
J425- C	J529- N	CBLT-
J425- C	J425-32	CBLT-
J425- T	J429- K	CBL0-
J429- K	J528-/H	CBL0-
J425- D	J529-29	CBST-
J425- D	J425-/J	CBST-

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J4 - 1	J425-28	CB1
J425-28	J426-37	CB1
J426-37	J426-38	CB1
J426-37	J427-/S	CB1
J427-/S	J429-13	CB1
J427-/S	J431-/X	CB1
J429-13	J522- Y	CB1
J431-/X	J437-/S	CB1
J425-/N	J426-/T	CB1/
J425-/N	J522-40	CB1/
J426-/T	J426-/U	CB1/
J426-/T	J427-36	CB1/
J427-36	J429-/Y	CB1/
J427-36	J528-/A	CB1/
J4 - 2	J522-21	CB2
J425- K	J425-36	CB2
J425- K	J432- A	CB2
J425- K	J522-21	CB2
J425-36	J426-31	CB2
J425-36	J427-40	CB2
J426-30	J426-31	CB2
J432- A	J436-16	CB2
J425-/D	J426-/K	CB2/
J425-/D	J522- 2	CB2/
J426-/K	J426-/L	CB2/
J426-/L	J427-35	CB2/
J427-35	J429-34	CB2/
J429-34	J431-41	CB2/
J431-41	J436- F	CB2/
J522- 2	J528-/B	CB2/
J425-16	J429-40	CB21/-
J425-16	J521-22	CB21/-
J521-22	J528- U	CB21/-
J4 - 3	J528-25	CB3
J425- 9	J426- E	CB3
J426- D	J426- E	CB3
J426- D	J528-25	CB3
J426- E	J427-/X	CB3
J427-/X	J432- W	CB3
J432- W	J436- S	CB3
J436- S	J437-32	CB3
J425-/W	J427-/M	CB3/
J426- F	J432- 5	CB3/
J426- F	J426- H	CB3/
J426- H	J427-/M	CB3/
J432- 5	J436- A	CB3/
J436- A	J528-24	CB3/
J4 - 4	J521-/B	CB4
J425- 3	J426- 2	CB4
J425- 3	J521-/B	CB4
J426- 1	J429- M	CB4
J426- 1	J426- 2	CB4
J427-/H	J429- M	CB4
J427-/H	J431-42	CB4
J429- M	J436-12	CB4
J436-12	J437- K	CB4
J425- N	J426- C	CB4/
J425- N	J522- 3	CB4/
J426- B	J426- C	CB4/
J426- C	J429- 4	CB4/
J427- W	J429- 4	CB4/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J429- 4	J436- 3	CB4/
J4 - 5	J528-/D	CB5
J413- K	J425- 2	CB5
J425- 2	J426- T	CB5
J425- 2	J528-/D	CB5
J426- T	J426- U	CB5
J426- U	J427-/C	CB5
J427-/C	J429-42	CB5
J429-42	J436- T	CB5
J425- 8	J426- W	CB5/
J426- W	J426- X	CB5/
J426- X	J427-22	CB5/
J427-22	J429- N	CB5/
J429- N	J436- 6	CB5/
J431-/M	J528-29	CB53-
J521-32	J522- 4	CB53-
J521-32	J528-29	CB53-
J8 -13	J535-17	CDC
J8 - 1	J535-35	CDL0
J8 - 2	J535-34	CDL1
J8 - 3	J535-/S	CDL2
J8 - 4	J535- 8	CDL3
J8 - 5	J535- 9	CDL4
J8 - 6	J535-11	CDL5
J8 - 7	J535-22	CDL6
J8 - 8	J535-18	CDL7
J8 - 9	J535- 1	CDU0
J8 -10	J535-/Y	CDU1
J8 -11	J535-27	CDU2
J8 -12	J535- A	CDU3
J8 -22	J448- 2	CK
J8 -23	J448- E	CK/
J3 -47	J524-20	CLOCK
J414- S	J414-15	CLOCK
J414-15	J417- 2	CLOCK
J417- 2	J417- 3	CLOCK
J417- 3	J419- 4	CLOCK
J417- 3	J417-13	CLOCK
J417-13	J417-14	CLOCK
J417-14	J417-22	CLOCK
J417-21	J417-22	CLOCK
J417-21	J422-20	CLOCK
J419- 4	J520-15	CLOCK
J422-20	J426-20	CLOCK
J426-20	J428-20	CLOCK
J428-20	J430-20	CLOCK
J430-20	J434-20	CLOCK
J434-20	J438-20	CLOCK
J438-20	J440-20	CLOCK
J440-20	J448- P	CLOCK
J448- B	J448- P	CLOCK

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J518- S	J518-15	CLOCK
J518- S	J520-15	CLOCK
J520- S	J520-15	CLOCK
J520- S	J523-20	CLOCK
J523-20	J524-20	CLOCK
J524-20	J536-20	CLOCK
J536-20	J538-20	CLOCK
J415-/D	J420-17	CL0--
J420-17	J421- C	CL0--
J421- C	J534- 6	CL0--
J437-19	J534- 5	CL0--
J534- 5	J534- 6	CL0--
J533- 4	J534- 7	CL0--D
J415-/C	J420-22	CL1--
J420-22	J421- D	CL1--
J421- D	J433- 3	CL1--
J433- 3	J435-/P	CL1--
J433- 3	J534- A	CL1--
J534- A	J534- B	CL1--
J533- B	J534- E	CL1--D
J415- W	J420-24	CL2--
J420-24	J421- F	CL2--
J421- F	J429- 8	CL2--
J429- 8	J534- 9	CL2--
J534- 9	J534-10	CL2--
J533- 9	J534-11	CL2--D
J415- Y	J420-20	CL3--
J420-20	J421-17	CL3--
J421-17	J433- 4	CL3--
J433- 4	J437-/M	CL3--
J433- 4	J534- P	CL3--
J534- P	J534- R	CL3--
J533-10	J534-13	CL3--D
J415-/B	J420-28	CL4--
J420-28	J432-/W	CL4--
J420-28	J421-20	CL4--
J421-20	J534- F	CL4--
J533-/R	J534- H	CL4--
J534- F	J534- H	CL4--
J533- 2	J534- 1	CL4--D
J415-/A	J420-/Y	CL5--
J420-/Y	J421-22	CL5--
J421-22	J432-/J	CL5--
J432-/J	J534- 2	CL5--
J533-/U	J534- 3	CL5--
J534- 2	J534- 3	CL5--
J533- D	J534- 4	CL5--D
J415- Z	J420-/B	CL6--
J420-/B	J421-25	CL6--
J420-/B	J534- J	CL6--
J533-33	J534- K	CL6--
J534- J	J534- K	CL6--
J533- K	J534- 8	CL6--D
J415-22	J420- U	CL7--
J420- U	J421- S	CL7--
J421- S	J534- M	CL7--
J534- M	J534- N	CL7--
J533- L	J534-12	CL7--D
J427- Y	J528-16	CPIR-
J423- N	J424- 1	CPL0-
J424- 1	J522- C	CPL0-
J522- C	J528-13	CPL0-
J423- C	J424- 3	CPL1-
J424- 3	J429-/N	CPL1-
J424- 3	J528-31	CPL1-
J423- J	J424- J	CPL2-
J424- J	J528- S	CPL2-
J423- F	J424- 7	CPL3-
J424- 7	J528-15	CPL3-
J423- K	J424- 9	CPL4-
J424- 9	J436-40	CPL4-
J424- 9	J522- 9	CPL4-
J522- 9	J528-/K	CPL4-
J423- H	J424-11	CPL5-
J423- H	J528-30	CPL5-
J424-11	J436-19	CPL5-
J436-19	J437-36	CPL5-
J423- D	J424- 5	CPL6-
J424- 5	J436-/T	CPL6-
J424- 5	J522- T	CPL6-
J522- T	J528- T	CPL6-
J423- E	J424- F	CPL7-
J424- F	J528-/J	CPL7-
J4 -18	J525-/E	CP1
J426-/V	J426-/W	CP1
J426-/V	J427-/D	CP1
J427-/D	J525-/E	CP1
J522-33	J525-/E	CP1
J525-/E	J528-19	CP1
J426-/X	J426-/Y	CP1/
J426-/X	J427-21	CP1/
J427-21	J528- W	CP1/
J522-43	J525-/J	CP1/
J525-/J	J528- W	CP1/
J4 -19	J528- X	CP2
J426-/C	J426-/D	CP2
J426-/C	J528- X	CP2
J426-/D	J427-38	CP2
J426-/F	J426-/H	CP2/
J426-/F	J528-18	CP2/
J426-/H	J427-37	CP2/
J4 -20	J528-20	CP3
J426-/M	J528-20	CP3
J426-/M	J426-/N	CP3
J426-/N	J427-/N	CP3
J427-/N	J436-/H	CP3
J426-/P	J426-/R	CP3/
J426-/P	J427-34	CP3/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J427-34	J436-42	CP3/
J427-34	J528- V	CP3/
J4 -21	J526-/M	CP4
J423-28	J424-43	CP4
J424-43	J427-/V	CP4
J426-11	J426-12	CP4
J426-11	J526-/M	CP4
J426-12	J427-/V	CP4
J423- P	J426- R	CP4/
J423- P	J522-15	CP4/
J424-40	J427-41	CP4/
J426- R	J426- S	CP4/
J426- S	J427-41	CP4/
J427-41	J436-41	CP4/
J4 -22	J526-/L	CP5
J423- V	J424-39	CP5
J423- V	J426- K	CP5
J424-39	J435-/R	CP5
J426- J	J426- K	CP5
J426- J	J522- E	CP5
J522- E	J528-23	CP5
J526-/L	J528-23	CP5
J423-13	J426- M	CP5/
J424-41	J427-/A	CP5/
J424-41	J436-43	CP5/
J426- L	J426- M	CP5/
J426- L	J525-/C	CP5/
J426- M	J427-/A	CP5/
P200-16	J406- 5	CR
J5 -13	J448- R	CT
J5 -14	J448-15	CT/
J414-16	J431-20	CTP1-3
J414-31	J431- D	CTP1-4
J415-21	J420- 2	CU0--
J420- 2	J421- A	CU0--
J421- A	J534-27	CU0--
J437-29	J534-27	CU0--
J533-/X	J534-28	CU0--
J534-27	J534-28	CU0--
J533-29	J534-29	CU0--D
J415-23	J420-12	CU1--
J420-12	J435-/N	CU1--
J420-12	J421- B	CU1--
J435-/N	J437- X	CU1--
J437- X	J534-/C	CU1--
J534-/C	J534-/D	CU1--
J533-28	J534-26	CU1--D
J415-/P	J420- T	CU2--
J420- T	J421-13	CU2--
J421-13	J534-14	CU2--
J533-/N	J534-15	CU2--
J534-14	J534-15	CU2--
J533- P	J534-17	CU2--D
J420- 6	J533- S	CU3-

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J4 - 6	J533- 8	C1
J421-/P	J429-/A	C1
J429-/A	J432-/D	C1
J429-/A	J430- U	C1
J430- T	J430- U	C1
J430- T	J533- 8	C1
J432-/D	J437-30	C1
J432-/D	J433-23	C1
J433-23	J435-17	C1
J437-30	J439-/J	C1
J421-/N	J429-25	C1/
J429-25	J430- X	C1/
J430- W	J430- X	C1/
J430- X	J433-22	C1/
J432-/H	J433-22	C1/
J432-/H	J439-29	C1/
J433-22	J435-15	C1/
J435-15	J533- 6	C1/
J437-/U	J439-29	C1/
J4 - 7	J533- 5	C2
J421-/R	J430-/V	C2
J429-16	J430-/V	C2
J429-16	J533- 5	C2
J430-/V	J430-/W	C2
J433- F	J437-15	C2
J433- F	J533- 5	C2
J437-15	J439-33	C2
J421-/L	J429-29	C2/
J429-29	J433- H	C2/
J429-29	J430-/X	C2/
J430-/X	J430-/Y	C2/
J430-/X	J437-33	C2/
J433- H	J533- F	C2/
J4 - 8	J533-/J	C3
J413- 9	J430- J	C3
J429-17	J430- K	C3
J429-17	J432-/E	C3
J430- J	J433- J	C3
J430- J	J430- K	C3
J432-/E	J437- Z	C3
J433- J	J533-/J	C3
J437- Z	J439-31	C3
J533-/J	J537-/E	C3
J429-36	J432-29	C3/
J430- L	J430- M	C3/
J430- L	J533- 7	C3/
J430- M	J433- V	C3/
J432-29	J439-36	C3/
J432-29	J433- V	C3/
J4 - 9	J533-/F	C4
J430- 1	J430- 2	C4
J430- 1	J533-/F	C4
J430- 2	J432- X	C4
J432- X	J437- P	C4
J437- P	J439-/K	C4
J413- C	J432- 6	C4/
J429-26	J432- 6	C4/
J429-26	J437-34	C4/
J430- B	J430- C	C4/
J430- B	J533-/B	C4/
J430- C	J432- 6	C4/
J533-/B	J537-25	C4/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J4 -10	J526-15	C5
J413- V	J430-12	C5
J430-11	J430-12	C5
J430-11	J437- E	C5
J430-11	J526-15	C5
J526-15	J533-/E	C5
J533-/E	J537- S	C5
J429- 6	J430- R	C5/
J429- 6	J533-/A	C5/
J430- R	J430- S	C5/
J430- S	J433- W	C5/
J433- W	J437-17	C5/
J533-/A	J537- 2	C5/
J413-/B	J430- S	C5/
J3 -37	J525-/N	D
J413- D	J525-/N	D
J429-/X	J434-31	D
J434-30	J434-31	D
J434-30	J436-23	D
J436-23	J529-25	D
J525-/N	J529-25	D
J413-33	J425-/S	D/
J425-/S	J434-/L	D/
J432-/C	J433-34	D/
J432-/C	J436- 2	D/
J433-34	J434-/K	D/
J434-/K	J434-/L	D/
J436- 2	J437- 2	D/
J436- 2	J525-/P	D/
J525-/P	J529- T	D/
J528-41	J529- T	D/
J442-/F	J448-30	DA1
J443-/F	J448-18	DA2
J444-/F	J448-32	DA3
J445-/F	J448-42	DA4
J442-/N	J448- 9	DB1
J443-/N	J448-21	DB2 *
J444-/N	J448-20	DB3
J445-/N	J448- 6	DB4
J4 -47	J529-28	DC
J438- J	J438- K	DC
J438- K	J529-28	DC
J444-39	J448-31	DC3 *
J445-39	J448-/Y	DC4 *
J438- L	J438- M	DC/
J438- L	J533-34	DC/
J438- M	J441-/F	DC/
J441-31	J534-30	DC/A--
J534-30	J534-31	DC/A--
J533-32	J534-32	DC/A--D
J442-39	J448-43	DC1
J443-39	J448- 7	DC2
J10 -33	J548-/N	DDC
J3 -17	J442- L	DDC
J442- L	J443- L	DDC
J442-/V	J443-/V	DDC
J443- L	J444- L	DDC

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J443-/V	J444-/V	DDC
J444- L	J445- L	DDC
J444-/V	J445-/V	DDC
J445- L	J448-12	DDC
J445- L	J445-/V	DDC
J448-12	J548-/N	DDC
J7 -14	J548-/N	DDC
J8 -43	J520-21	DG13
J8 -44	J525-24	DG14
J8 -46	J423- W	DG16
J8 -47	J425- S	DG17
J8 -48	J529- L	DG18
J8 -49	J441-/X	DG19
J8 -50	J544-18	DG20
J11 -34	J526- 7	DG21
J11 -35	J526-33	DG22
J11 -36	J528-17	DG23
J11 -37	J528-27	DG24
J11 -38	J528-28	DG25
J11 -39	J528-42	DG26
J11 -40	J528- Z	DG27
J11 -41	J528-/C	DG28
J11 -42	J528-/E	DG29
J11 -43	J528-/F	DG30
J11 -44	J534-33	DG31
J11 -45	J530-33	DG32
J11 -46	J530-/R	DG33
J11 -47	J527-18	DG34
J11 -48	J527-/E	DG35
J11 -49	J527-/J	DG36
J11 -50	J527-/R	DG37
J7 -23	J443-12	DG39
J7 -24	J443-18	DG40
J7 -34	J443-36	DG41
J7 -21	J443-/U	DG42
J7 -36	J443-41	DG43 *
J7 -32	J443-27	DG44 *
J7 -19	J443-06	DG45
J7 -33	J444-31	DG46 *
J7 -20	J443-08	DG47 *
J4 -17	J432- 9	DR
J432- 9	J438- D	DR
J438- D	J438- E	DR
J438- F	J438- H	DR/
J438- H	J441-/L	DR/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J436-10	J437-/F	DS-
J436-10	J529-/C	DS-
J437-/F	J439-43	DS-
J413-35	J424-28	DTP/--
J424-28	J429-38	DTP/--
J429-38	J437-/W	DTP/--
J435-25	J436-36	DTP/--
J435-25	J530- M	DTP/--
J436-36	J437-/W	DTP/--
J522-37	J528-/N	DTP/--
J528-/N	J533-24	DTP/--
J530- M	J530- N	DTP/--
J530- N	J533-24	DTP/--
J533-24	J537-/K	DTP/--
J529-13	J530-12	DTP/--D
J530-/C	J530-/D	DTP--
J530-/D	J533- Y	DTP--
J529-24	J530-26	DTP--D
J5 - 1	J448- 1	DT1
J5 - 2	J448-10	DT2
J5 - 3	J448-22	DT3
J5 - 4	J448-34	DT4
J441-/A	J442- B	D01
J10 - 5	J442- D	D01C
J441-/M	J442- J	D02
J10 - 6	J442-10	D02C
J441-16	J442- R	D03
J10 - 7	J442-16	D03C
J441-/N	J442- X	D04
J10 - 8	J442-22	D04C
J441- P	J443- B	D08
J6 - 1	J443- D	D08C
J441- Z	J443- J	D09
J6 - 2	J443-10	D09C
J11 - 1	J438-/V	D1
J438-/V	J438-/W	D1
J438-/W	J441-29	D1
J438-/X	J438-/Y	D1/
J438-/Y	J441-30	D1/
J441-/K	J442-/D	D10
J10 -31	J442-28	D10C
J441- S	J442-/L	D11
J6 - 6	J442-34	D11C
J441- M	J443-/D	D12

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J6 - 3	J443-28	D12C
J441- Y	J444-/D	D13
J435-27	J528-39	D13/-
J6 - 4	J444-28	D13C
J441-/H	J442-/T	D14
J6 - 5	J442-40	D14C
J441-15	J445-/L	D15
J10 -30	J445-34	D15C
J441- K	J444-/L	D16
J6 - 7	J444-34	D16C
J441- X	J443-/T	D17
J10 -29	J443-40	D17C
J441-27	J444-/T	D18
J9 -25	J444-40	D18C
J441- N	J443-/L	D19
J9 -26	J443-34	D19C
J11 - 2	J438-/N	D2
J438-/M	J441-28	D2
J438-/M	J438-/N	D2
J438-/N	J439-37	D2
J438-/P	J441-/J	D2/
J438-/P	J438-/R	D2/
J438-/R	J439-38	D2/
J441- H	J445-/T	D20**
J441- H		D20*
J9 -23	J445-40	D20C**
J9 -23	J445- D	D20C *
J441- U	J445-/D	D21
J10 -32	J445-28	D21C
J441-/E	J443- R	D22
J9 -28	J443-16	D22C
J441- L	J443- X	D23
J9 -29	J443-22	D23C
J441- B	J444- B	D24
J6 -26	J444- D	D24C
J441- T	J444- J	D25
J9 -30	J444-10	D25C
J441-26	J444- R	D26
J9 -31	J444-16	D26C

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J441- F	J444- X	D27
J9 -32	J444-22	D27C
J441- C	J445- B	D28**
J441- C	J445-/T	D28 *
J9 -33	J445- D	D28C**
J9 -33	J445-40	D28C *
J441- R	J445- J	D29
J9 -34	J445-10	D29C
J11 - 3	J438-31	D3
J438-30	J438-31	D3
J438-30	J441-32	D3
J438-31	J439-42	D3
J438-/K	J438-/L	D3/
J438-/L	J439-/L	D3/
J439-/L	J441-/P	D3/
J441-/B	J445- R	D30
J9 -35	J445-16	D30C
J441- J	J445- X	D31
J9 -36	J445-22	D31C
J11 - 4	J436-11	D4
J436-11	J438-37	D4
J438-37	J441-35	D4
J438-37	J438-38	D4
J438-/T	J441-34	D4/
J438-/T	J438-/U	D4/
J438-/U	J439-40	D4/
J11 - 5	J436- 9	D5
J436- 9	J438- 2	D5
J438- 1	J438- 2	D5
J438- 2	J441-/R	D5
J438- B	J438- C	D5/
J438- C	J441-33	D5/
J439-39	J441-33	D5/
J3 -38	J525- 2	E
J429-/M	J436-33	E
J434- J	J434- K	E
J434- J	J437- 5	E
J434- J	J533- Z	E
J436-33	J437- 5	E
J525- 2	J526- 3	E
J525- 2	J528-/R	E
J528-/R	J533- Z	E
J429-37	J436-24	E/
J434- L	J434- M	E/
J434- L	J522- Z	E/
J434- M	J436-24	E/
J429-33	J432-16	EFB--
J432-16	J522- P	EFB--
J522- P	J534-23	EFB--
J533-/V	J534-24	EFB--
J534-23	J534-24	EFB--
J533-25	J534-25	EFB--D
P203- 7	J405- N	EMR
J3 -29	J423-26	EMX
J405-41	J420-/F	EMX
J420-/F	J423-26	EMX
J423-26	J535-19	EMX
J405-/W	J421- W	EMX/
J421- W	J424-/D	EMX/
J424-/D	J535-26	EMX/
P202-15	J518- T	EP
P202-14	J518- Y	EP/
P203- 9	J405- 5	ER
J423-/Y	J429-/W	ETP-
J423-/Y	J424-/C	ETP-
J429-/W	J436- F	ETP-
J436- F	J533-/C	ETP-
J416-/C	J416-/D	EW
J416-/D	J548- S	EW
J7 -16	J548- R	EWC
J3 -28	J423-19	EX
J405-40	J420- V	EX
J420- V	J423-19	EX
J420- V	J519-26	EX
J519-26	J535- Z	EX
J405-/V	J421- T	EX/
J421- T	J424- U	EX/
J421- T	J519- T	EX/
J519- T	J535-/B	EX/
J425- H	J429-/J	EOP-
J429-/J	J436-25	EOP-
J436-25	J533-/D	EOP-
J441-14	J447-/T	E1
J7 -22	J447-40	E10
J441-13	J447- B	E2
J6 -27	J447- D	E20
J441-10	J447- J	E3
J7 -35	J447-10	E30
J3 -34	J422- 1	FC
J422- 1	J519- V	FC
J422- 1	J422- 2	FC
J422- 2	J423-/R	FC
J423-/R	J435-33	FC
J435-33	J437-/K	FC
J422- B	J521- Y	FC/
J422- B	J422- C	FC/
J422- C	J425-18	FC/
J425-18	J432- V	FC/
J519-/U	J521- Y	FC/
J401-/X	J401-/Y	FFR
J401-/Y	J401-43	FFR
J401-43	J402-/X	FFR
J402-/X	J402-/Y	FFR
J402-/Y	J402-43	FFR
J402-43	J403-/X	FFR
J403-/X	J403-/Y	FFR
J403-/Y	J403-43	FFR
J403-43	J412-43	FFR

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J409-/X	J409-/Y	FFR
J409-/Y	J409-43	FFR
J409-43	J410-/X	FFR
J410-/X	J410-/Y	FFR
J410-/Y	J410-43	FFR
J410-43	J411-/X	FFR
J411-/X	J411-/Y	FFR
J411-/Y	J411-43	FFR
J411-43	J412-/X	FFR
J412-/X	J412-/Y	FFR
J412-/Y	J412-43	FFR
J412-43	J413-15	FFR
J413-10	J413-15	FFR
J413-10	J441-/D	FFR
J413-15	J413-/L	FFR
J441-/C	J441-/D	FFR
J8 -25	J548-26	FK
P201-47	J518- H	FP
P201-46	J518- N	FP/
P200- 3	J407- 5	FR
J442-/A	J521-/E	FS
J8 -24	J442-23	FSC
J3 -27	J423-22	FX
J407-40	J420-16	FX
J420-16	J423-22	FX
J420-16	J519-/W	FX
J519-/W	J535- V	FX
J407-/V	J421-23	FX/
J421-23	J424-18	FX/
J421-23	J519-/J	FX/
J519-/J	J535-/D	FX/
E70 -043		GRD †
J1 - 2	E70 -002	GRD
J1 - 4	E70 -003	GRD
J1 - 6	E70 -004	GRD
J1 - 8	E70 -005	GRD
J1 -11	E70 -006	GRD
J1 -12	E70 -007	GRD
J1 -14	E70 -008	GRD
J1 -15	J417-43	GRD
J1 -17		GRD †
J1 -22	E70 -009	GRD
J1 -23	E70 -010	GRD
J1 -24	E70 -011	GRD
J1 -25	E70 -012	GRD
J1 -28	E70 -013	GRD
J1 -29	E70 -014	GRD
J1 -32	E70 -015	GRD
J1 -33	E70 -016	GRD
J1 -40	E70 -017	GRD
J1 -41	E70 -018	GRD
J1 -42	E70 -019	GRD
J1 -43	E70 -020	GRD
J1 -44	E70 -021	GRD
J1 -45	E70 -022	GRD
J10 -18	E70 -047	GRD
J10 -25		GRD †
J10 -26	J544- 3	GRD
J10 -27	J544- 3	GRD
J10 -28	J544- 9	GRD
J11 -15	E70 -110	GRD
J2 - 5	E70 -023	GRD

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J2 - 6	E70 -024	GRD
J2 - 7	E70 -025	GRD
J2 - 8	E70 -026	GRD
J2 -10	E70 -027	GRD
J2 -12	J539- 4	GRD
J2 -13		GRD †
J2 -18	E70 -028	GRD
J2 -21	E70 -029	GRD
J2 -23	J539-/N	GRD
J2 -29	E70 -030	GRD
J2 -30	E70 -031	GRD
J2 -31	E70 -032	GRD
J2 -32	E70 -033	GRD
J2 -33	E70 -034	GRD
J2 -38		GRD †
J2 -50	E70 -035	GRD
J3 -15	E70 -042	GRD
J4 -16	E70 -048	GRD
J401- F	J401- P	GRD
J401- F	J401- 6	GRD
J401- 6	E70 -039	GRD
J401-/S	J401-37	GRD
J401-37	J402-/S	GRD
J402- F	J402- P	GRD
J402- F	J402- 6	GRD
J402- 6	E70 -038	GRD
J402-/S	J402-37	GRD
J402-37	J403-/S	GRD
J403- F	J403- P	GRD
J403- F	J403- 6	GRD
J403- 6	E70 -044	GRD
J403-/S	J403-37	GRD
J403-37	J404-/S	GRD
J404- F	J404- P	GRD
J404- F	J404- 6	GRD
J404- 6	E70 -045	GRD
J404-/S	J404-37	GRD
J404-/X	J404-/Y	GRD
J404-/Y	J404-43	GRD
J404-37	J405-/S	GRD
J404-37	J404-43	GRD
J405- F	J405- P	GRD
J405- F	J405- 6	GRD
J405- 6	E70 -046	GRD
J405-/S	J405-37	GRD
J405-/X	J405-/Y	GRD
J405-/Y	J405-43	GRD
J405-37	J406-/S	GRD
J405-37	J405-43	GRD
J406- E	J406- F	GRD
J406- F	J406- P	GRD
J406- F	J406- 6	GRD
J406- 6	E70 -050	GRD
J406- 6	J406-13	GRD
J406-/S	J406-37	GRD
J406-/V	J406-40	GRD
J406-/X	J406-/Y	GRD
J406-/Y	J406-43	GRD
J406-37	J407-/S	GRD
J406-37	J406-38	GRD
J406-37	J406-43	GRD
J406-38	J406-39	GRD
J406-39	J406-40	GRD
J407- F	J407- P	GRD
J407- F	J407- 6	GRD
J407- 6	E70 -051	GRD
J407-/S	J407-37	GRD
J407-/X	J407-/Y	GRD
J407-/Y	J407-43	GRD

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J407-37	E70 -052	GRD
J407-37	J407-43	GRD
J408- F	J408- P	GRD
J408- F	J408- 6	GRD
J408- 6	E70 -056	GRD
J408-/S	J408-37	GRD
J408-/X	J408-/Y	GRD
J408-/Y	J408-43	GRD
J408-37	J409-/S	GRD
J408-37	J408-43	GRD
J409- F	J409- P	GRD
J409- F	J409- 6	GRD
J409- 6	E70 -057	GRD
J409-/S	J409-37	GRD
J409-37	J410-/S	GRD
J410- F	J410- P	GRD
J410- F	J410- 6	GRD
J410- 6	E70 -058	GRD
J410-/S	J410-37	GRD
J410-37	J411-/S	GRD
J411- F	J411- P	GRD
J411- F	J411- 6	GRD
J411- 6	E70 -062	GRD
J411-/S	J411-37	GRD
J411-37	J412-/S	GRD
J412- F	J412- P	GRD
J412- F	J412- 6	GRD
J412- 6	E70 -063	GRD
J412-/S	J412-37	GRD
J412-37	E70 -064	GRD
J414-/E	E70 -068	GRD
J414-/E	J414-/F	GRD
J414-/E	J414-27	GRD
J414-27	J414-28	GRD
J416- Z	E70 -069	GRD #
J416- Z	E70 -070	GRD
J416- Z	J416-22	GRD
J417- H	E70 -109	GRD
J417- H	J539- 2	GRD
J417- 8	E70 -108	GRD #
J417- 8	J417- 9	GRD
J417- 9	E70 -107	GRD
J417- 9	J417-24	GRD
J417-24	J417-25	GRD
J417-25	J417-43	GRD
J417-42	E70 -104	GRD #
J417-42	J417-43	GRD
J417-43	E70 -103	GRD
J418- A	E70 -102	GRD
J418- A	J418- 1	GRD
J418- 4	E70 -101	GRD
J419- X	J419-/T	GRD
J419- X	E70 -098	GRD
J419-33	E70 -097	GRD
J419-33	J419-34	GRD
J419-34	J419-35	GRD
J419-35	J419-36	GRD
J419-36	J419-37	GRD
J419-37	J419-38	GRD
J419-38	J419-39	GRD
J419-39	J419-40	GRD
J419-40	J419-41	GRD
J422-/E	E70 -096	GRD
J422-/E	J422-28	GRD
J426-/E	E70 -093	GRD
J426-/E	J426-28	GRD
J428-/E	E70 -091	GRD #
J428-/E	E70 -092	GRD
J428-/E	J428-28	GRD

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J430-/E	E70 -087	GRD
J430-/E	E70 -088	GRD #
J430-/E	J430-28	GRD
J434-/E	E70 -086	GRD #
J434-/E	J434-28	GRD
J434-28	E70 -082	GRD
J438-/E	E70 -081	GRD
J438-/E	J438-28	GRD
J438-28	E70 -080	GRD #
J440-/E	E70 -076	GRD
J440-/E	J440-28	GRD
J440-28	E70 -075	GRD #
J441-23	E70 -074	GRD
J441-23	J441-24	GRD
J442- P	E70 -106	GRD #
J442- P	J442-13	GRD
J442-/C	J442-25	GRD
J442-/C	J442-/S	GRD
J442-/S	J442-37	GRD
J442-13	J443- P	GRD
J442-25	J443-/C	GRD
J442-37	J443-/S	GRD
J443- P	J443-13	GRD
J443-/C	J443-25	GRD
J443-/S	J443-37	GRD
J443-13	J444- P	GRD
J443-25	J444-/C	GRD
J443-37	J444-/S	GRD
J444- P	J444-13	GRD
J444-/C	J444-25	GRD
J444-/S	J444-37	GRD
J444-13	J444-25	GRD
J444-25	E70 -094	GRD
J444-37	E70 -095	GRD #
J445- P	E70 -100	GRD #
J445- P	J445-13	GRD
J445-/C	J445-25	GRD
J445-/C	J445-/S	GRD
J445-/S	J445-37	GRD
J445-13	J446- P	GRD
J445-25	J446-/C	GRD
J445-37	J446-/S	GRD
J446- P	J446-13	GRD
J446-/C	J446-25	GRD
J446-/S	J446-37	GRD
J446-13	J447- P	GRD
J446-25	J447-/C	GRD
J446-37	J447-/S	GRD
J447- P	J447-13	GRD
J447-/C	J447-25	GRD
J447-/S	J447-37	GRD
J447-13	J447-25	GRD
J447-25	E70 -099	GRD
J447-37	E70 -105	GRD #
J5 -18	E70 -090	GRD
J518-/E	J518-/F	GRD
J518-/F	J518-28	GRD
J518-27	E70 -089	GRD
J518-27	J518-28	GRD
J520-/E	J520-/F	GRD
J520-/F	J520-28	GRD
J520-27	E70 -085	GRD
J520-27	J520-28	GRD
J523-/E	E70 -084	GRD
J523-/E	J523-28	GRD
J524-/E	E70 -083	GRD #
J524-/E	E70 -079	GRD
J524-/E	J524-28	GRD
J527- L	E70 -078	GRD

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J527- L	J527- S	GRD
J527- S	J527- U	GRD
J527- U	J527-/H	GRD
J527-/H	J527-/K	GRD
J527-/K	J527-/S	GRD
J530- L	E70 -077	GRD
J530- L	J530- S	GRD
J530- S	J530- U	GRD
J530- U	J530-/H	GRD
J530-/H	J530-/K	GRD
J530-/K	J530-/S	GRD
J534- L	E70 -073	GRD
J534- L	J534- S	GRD
J534- S	J534- U	GRD
J534- U	J534-/H	GRD
J534-/H	J534-/K	GRD
J534-/K	J534-/S	GRD
J536-/E	E70 -072	GRD
J536-/E	J536-28	GRD
J536-28	E70 -071	GRD #
J538-/E	E70 -067	GRD #
J538-/E	J538-28	GRD
J538-28	E70 -066	GRD
J539- D	J539- 4	GRD
J539- D	J540- 4	GRD
J539- 2	J539-33	GRD
J539-/N	J540- D	GRD
J539-/N	J541-42	GRD
J540- D	E70 -065	GRD
J540- D	J540- 4	GRD
J541-/X	J541-/Y	GRD
J541-/X	J541-42	GRD
J541-/X	J542-42	GRD
J541-42	J541-43	GRD
J542-/X	J542-42	GRD
J542-/X	J542-/Y	GRD
J542-/X	J543-42	GRD
J542-42	J542-43	GRD
J543-/X	J543-42	GRD
J543-/X	J543-/Y	GRD
J543-/X	J544-40	GRD
J543-42	J543-43	GRD
J544- B	J544- 3	GRD
J544- 3	J544- 9	GRD
J544- 9	J544-22	GRD
J544-/V	J544-40	GRD
J544-/V	J544-/X	GRD
J544-/V	J546-40	GRD
J544-22	J544-27	GRD
J544-23	E70 -061	GRD
J544-27	J544-40	GRD
J546- B	J546- 3	GRD
J546- 3	J546- 9	GRD
J546- 9	J546-22	GRD
J546-/V	J546-40	GRD
J546-/V	J546-/X	GRD
J546-22	J546-27	GRD
J546-27	J546-40	GRD
J548- T	E70 -060	GRD #
J548- T	E70 -059	GRD
J548- T	J548-17	GRD
J548-17	J548-35	GRD
J6 -18	E70 -055	GRD
J6 -32		GRD †
J6 -33	J546-27	GRD
J6 -35	J544-/X	GRD
J6 -37	J546- 3	GRD
J6 -39	J546-/X	GRD
J6 -41	J544-22	GRD
J6 -43	J546- B	GRD
J6 -45	J546-22	GRD
J6 -47	J544-27	GRD
J6 -49	J546- 9	GRD
J7 -18	E70 -054	GRD
J8 -18	E70 -053	GRD
J8 -39	J419-37	GRD
J8 -40	J419-38	GRD
J8 -41	J419-39	GRD
J8 -42	J419-40	GRD
J8 -45	J419-41	GRD
J9 -18	E70 -049	GRD
P200- 2	J407- P	GRD
P200- 4	J407- 6	GRD
P200- 6	J405- F	GRD
P200- 8	J408- P	GRD
P200-10	J407- F	GRD
P200-12	J408- 6	GRD
P200-14	J408- F	GRD
P200-17	J406- 6	GRD
P200-19	J412- 6	GRD
P200-21	J411- P	GRD
P200-23	J411- F	GRD
P200-25	J410- 6	GRD
P200-27	J409- P	GRD
P200-35	J412- P	GRD
P200-37	J412- F	GRD
P200-39	J411- 6	GRD
P200-41	J410- P	GRD
P200-43	J410- F	GRD
P200-45	J409- 6	GRD
P203- 2	J404- F	GRD
P203- 4	J404- 6	GRD
P203- 6	J404- P	GRD
P203- 8	J405- P	GRD
P203-10	J405- 6	GRD
P203-17	J406- P	GRD
P203-19	J403- P	GRD
P203-21	J403- F	GRD
P203-23	J402- 6	GRD
P203-25	J401- P	GRD
P203-27	J401- F	GRD
P203-35	J409- F	GRD
P203-37	J403- 6	GRD
P203-39	J402- P	GRD
P203-41	J402- F	GRD
P203-43	J401- 6	GRD
P204- 1	E70 -036	GRD ##
P204- 2	E70 -037	GRD
J11 - 6	J438-11	G1
J438-11	J438-12	G1
J438-12	J548-43	G1
J432-/F	J438- S	G1/
J438- R	J438- S	G1/
J438- R	J548-/X	G1/
J10 -12	J548-41	G10C
J10 -13	J548-/Y	G11C
J11 - 7	J438-/C	G2
J438-/C	J438-/D	G2
J438-/D	J548-39	G2
J432-30	J438-/H	G2/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J438-/F	J438-/H	G2/
J438-/F	J548-42	G2/
J10 -14	J548-/U	G20C
J10 -15	J548-40	G21C
J11 - 8	J438- T	G3
J438- T	J438- U	G3
J438- U	J548-/T	G3
J432-28	J438- X	G3/
J438- W	J438- X	G3/
J438- X	J548-38	G3/
J10 -16	J548-/W	G30C
J10 -17	J548-/V	G31C
P200-11	J408- 5	HMR
J3 -31	J423-27	HMX
J408-40	J420-19	HMX
J420-19	J423-27	HMX
J423-27	J535-23	HMX
J408-/V	J421- X	HMX/
J421- X	J424-/E	HMX/
J424-/E	J535-/A	HMX/
P201-13	J518- F	HP
P201-12	J518- C	HP/
P200-13	J408- E	HR
J3 -16	J536-/N	HS
J536-/P	J537-/J	HS/
J536-/P	J536-/R	HS/
J3 -30	J420- X	HX
J408-38	J420- X	HX
J420- X	J423-24	HX
J423-24	J519-42	HX
J519-42	J535- W	HX
J408-39	J421-24	HX/
J421-24	J424- S	HX/
J424- S	J519-15	HX/
J519-15	J535-/C	HX/
J437- 6	J447- V	IB
J10 -22	J447-19	IBC
J3 -24	J528- 7	IC
J423-/L	J430-37	IC
J423-/L	J424-23	IC
J424-23	J435-19	IC
J430-37	J430-38	IC
J435-19	J528- 7	IC
J423-/W	J430-/U	IC/
J423-/W	J424- Z	IC/
J424- Z	J528- E	IC/
J430-/T	J430-/U	IC/
J423-38	J436-35	ICX/-

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J423-38	J424-/A	ICX/-
J424-/A	J528- A	ICX/-
J4 -33	J434- U	ID
J434- T	J434- U	ID
J429-/T	J431- H	ID/
J431- H	J434- W	ID/
J434- W	J434- X	ID/
J434- X	J436-22	ID/
J424-/K	J443-/A	IM
J8 -17	J443-23	IMC
J3 -42	J422- J	IP
J422- J	J525-38	IP
J422- J	J422- K	IP
J422- K	J425-/H	IP
J424-38	J425-/H	IP
J521-41	J525-38	IP
J422- L	J525-/U	IP/
J422- L	J422- M	IP/
J422- M	J425-25	IP/
J424-34	J425-25	IP/
J425-25	J429-/F	IP/
J429-/F	J436- J	IP/
J521-42	J525-/U	IP/
J525-/U	J528-35	IP/
P200- 5	J405- E	IR
J3 -20	J528-37	IX
J405-38	J423-/X	IX
J423-/X	J424-22	IX
J424-22	J425-27	IX
J425-27	J437-/H	IX
J437-/H	J535-24	IX
J528-37	J535-24	IX
J405-39	J423-42	IX/
J423-42	J425- Y	IX/
J425- Y	J528- 5	IX/
J437- 9	J535-25	IX/
J528- 5	J535-25	IX/
J435-20	J528-40	IXE-
J427-/R	J442-/W	I1
J442- E	J521- N	I1A
J10 -39	J442- 6	I1AC
J5 -22	J442- 6	I1AC
J442- F	J521- D	I1B
J10 -40	J442- 7	I1BC
J5 -23	J442- 7	I1BC
J7 - 1	J442-42	I1C
J431- E	J443-/B	I1N
J7 -31	J443-26	I1NC
J431- L	J443-/H	I11**

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J7 -32	J443-29	I11C**
J431- W	J443-/J	I14**
J7 -33	J443-32	I14C**
J427-39	J442-/X	I2
J442- M	J521- M	I2A
J10 -41	J442-11	I2AC
J5 -24	J442-11	I2AC
J442- N	J521- E	I2B
J10 -42	J442-14	I2BC
J5 -25	J442-14	I2BC
J7 - 2	J442-43	I2C
P201-30	J520-/T	I24W
P201-29	J520-/Y	I24W/
J427-42	J443- E	I3
J442- U	J521- L	I3A
J10 -43	J442-17	I3AC
J5 -26	J442-17	I3AC
J442- V	J521- H	I3B
J10 -44	J442-19	I3BC
J5 -27	J442-19	I3BC
J7 - 3	J443- 6	I3C
J431- B	J443-/X	I3N
J7 -37	J443-43	I3NC
J431- N	J444- E	I31**
J7 -19	J444- 6	I31C**
J431-/A	J444- F	I34**
J7 -20	J444- 7	I34C**
J427-/E	J443- F	I4
J431- 2	J442-/B	I4A
J10 -45	J442-26	I4AC
J5 -28	J442-26	I4AC
J431-10	J442-/H	I4B
J10 -46	J442-29	I4BC
J5 -29	J442-29	I4BC
J7 - 4	J443- 7	I4C
J443- M	J525- K	I5
J431- 1	J442-/J	I5A
J10 -47	J442-32	I5AC
J5 -30	J442-32	I5AC

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J436-/U	J446-/B	I5B
J10 -48	J446-26	I5BC
J5 -31	J446-26	I5BC
J7 - 5	J443-11	I5C
J431- 4	J442-/P	I6A
J10 -49	J442-35	I6AC
J5 -32	J442-35	I6AC
J436-37	J446-/H	I6B
J10 -50	J446-29	I6BC
J5 -33	J446-29	I6BC
J431-24	J442-/R	I7
J7 - 7	J442-38	I7C
J3 -13	J429- 2	J
J420-/P	J421-37	J
J421-37	J431-34	J
J429- 2	J432- 4	J
J429- 2	J526- 8	J
J431-34	J434-/M	J
J432- 4	J433- 6	J
J433- 6	J437- M	J
J434-/M	J434-/N	J
J434-/M	J435-/C	J
J435-/C	J437- M	J
J437- M	J537- J	J
J525-25	J526- 8	J
J433- K	J437- D	J/
J433- K	J435- X	J/
J433- K	J525- 4	J/
J434-/P	J434-/R	J/
J434-/P	J439-32	J/
J434-/P	J435- X	J/
J437- D	J537- K	J/
J522- F	J525- 4	J/
J525- 4	J526-21	J/
J4 -46	J528-/L	JT
J528-/L	J536-/V	JT
J536-/V	J536-/W	JT
J536-/X	J536-/Y	JT/
J3 -14	J526- 2	K
J423-/V	J429-/K	K
J423-/V	J424- W	K
J429-/K	J431-/N	K
J431-/N	J433-33	K
J433-33	J436- K	K
J434- D	J434- E	K
J434- D	J526- 2	K
J434- D	J533-23	K
J434- E	J436- K	K
J436- K	J448-/D	K
J448-/D	J548- 6	K
J521-/C	J522-/S	K
J521-/C	J526- 2	K
J413- B	J525- D	K/
J423-39	J424- Y	K/
J424- Y	J433- Z	K/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J433- Z	J437-/B	K/
J434- F	J434- H	K/
J434- F	J525- D	K/
J434- H	J436- X	K/
J436- X	J437-/B	K/
J522-35	J528-32	K/
J525- D	J526-23	K/
J526-23	J528-32	K/
J527- 2	J527- 3	KA--
J527- 3	J528- J	KA--
J526- A	J527- 4	KA--D
J433-/P	J525-27	KD/-
J420-31	J421-/W	KDP-
J420-31	J423-/B	KDP-
J421-/W	J424-37	KDP-
J423-/B	J435- 8	KDP-
J435- 8	J533-27	KDP-
J425- Z	J433-24	KE--
J425- Z	J526-10	KE--
J433-24	J436-/X	KE--
J526-10	J527-30	KE--
J527-30	J527-31	KE--
J527-31	J533-/W	KE--
J526-/F	J527-32	KE--D
J436-31	J522- S	KFB-
J522- S	J533-42	KFB-
J420-41	J424-/M	KH/
J424-/M	J548- 1	KH/
J7 -17	J548-14	KH/C
J423-18	J424-42	KIC-
J424-42	J528- C	KIC-
J8 -30	J548- 5	KK
J435-/F	J548- C	KR/
J8 -16	J548- 2	KR/K
J436-/C	J548- L	KS/
J8 -15	J548-12	KS/K
J431-40	J522- 7	KTP-
J522- 7	J533-26	KTP-
J3 -25	J522-34	LC
J427-/U	J524- T	LC
J522-34	J524- U	LC
J524- T	J524- U	LC
J427-/W	J524- W	LC/
J522-/P	J524- X	LC/
J524- W	J524- X	LC/
J3 -43	J525- F	LP
J429- E	J525- F	LP
J522-29	J524-/M	LP
J524-/M	J524-/N	LP
J524-/M	J525- F	LP

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J429- B	J525- 9	LP/
J522-22	J525- 9	LP/
J522-22	J524-/P	LP/
J524-/P	J524-/R	LP/
P200- 7	J408- N	LR
J3 -21	J524- J	LX
J420-/L	J423-/J	LX
J423-/J	J427-/T	LX
J427-/T	J429- D	LX
J429- D	J433- C	LX
J429- D	J524- J	LX
J433- C	J535- K	LX
J522-/N	J524- K	LX
J524- J	J524- K	LX
J420-/T	J421-/E	LX/
J421-/E	J424-25	LX/
J424-25	J427-/P	LX/
J427-/P	J429-11	LX/
J429-11	J433- 9	LX/
J429-11	J524- L	LX/
J522-39	J524- M	LX/
J524- L	J524- M	LX/
J524- M	J535-/R	LX/
J4 -50	J522-/E	LO
J408-41	J522-/E	LO
J408-/W	J522-25	LO/
P201-32	J520- H	L24W
P201-31	J520- N	L24W/
J413- Y	J533- A	MC-
J533- A	J537-/M	MC-
J3 -46	J536-31	MPX
J448- S	J536-30	MPX
J536-30	J536-31	MPX
J536-/K	J536-/L	MPX/
J8 -32	J448- U	MPXK
J8 -33	J448- T	MPXK/
J4 -49	J522- 8	MR
J431-36	J435-23	MR
J431-36	J522- 8	MR
J435-23	J548- V	MR
J7 -15	J548-23	MRC
J412-41	J420- H	M00
J420- H	J423- M	M00
J423- M	J535- E	M00
J412-/W	J421- 3	M00/
J421- 3	J424- 2	M00/
J424- 2	J535-/W	M00/
P200-34	J412- N	M00R
P201-34	J415-15	M00W
P201- 1	J415-/T	M00W/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
P201-18	J416- V	M00WC
J412-40	J420- F	M02
J420- F	J423- A	M02
J423- A	J535- 6	M02
J412-/V	J421- 4	M02/
J421- 4	J424- 4	M02/
J424- 4	J535-37	M02/
P200-18	J412- 5	M02R
P201-35	J415- P	M02W
P201- 2	J415-39	M02W/
P201-19	J416- R	M02WC
J412-38	J420- E	M04
J420- E	J423- 8	M04
J423- 8	J535- D	M04
J412-39	J421- E	M04/
J421- E	J424- 6	M04/
J424- 6	J535-38	M04/
P200-36	J412- E	M04R
P201-36	J415-13	M04W
P201- 3	J415-/U	M04W/
P201-20	J416- T	M04WC
J411-41	J420- D	M06
J420- D	J423-10	M06
J423-10	J535- L	M06
J411-/W	J421- H	M06/
J421- H	J424- 8	M06/
J424- 8	J535-/P	M06/
P200-20	J411- N	M06R
P201-37	J415- N	M06W
P201- 4	J415-40	M06W/
P201-21	J416- L	M06WC
J411-40	J420- B	M10
J420- B	J423- 7	M10
J423- 7	J535- 5	M10
J411-/V	J421- J	M10/
J421- J	J424-10	M10/
J424-10	J535-39	M10/
P200-38	J411- 5	M10R
P201-38	J415-12	M10W
P201- 5	J415-/V	M10W/
P201-22	J416- J	M10WC
J411-38	J420- 4	M12
J420- 4	J423- 9	M12
J423- 9	J535- 4	M12

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J411-39	J421- K	M12/
J421- K	J424-12	M12/
J424-12	J535-40	M12/
P200-22	J411- E	M12R
P201-39	J415- M	M12W
P201- 6	J415-41	M12W/
P201-23	J416- N	M12WC
J410-41	J420- C	M14
J420- C	J423-12	M14
J423-12	J535- 3	M14
J410-/W	J421- L	M14/
J421- L	J424- E	M14/
J424- E	J535-41	M14/
P200-40	J410- N	M14R
P201-40	J415- L	M14W
P201- 7	J415-/W	M14W/
P201-24	J416- D	M14WC
J410-40	J420- 3	M16
J420- 3	J423-11	M16
J423-11	J535- 2	M16
J410-/V	J421- M	M16/
J421- M	J424- H	M16/
J424- H	J535-42	M16/
P200-24	J410- 5	M16R
P201-41	J415- K	M16W
P201- 8	J415-42	M16W/
P201-25	J416- F	M16WC
J410-38	J420- 7	M20
J420- 7	J423- L	M20
J423- L	J535- N	M20
J410-39	J421-11	M20/
J421-11	J424- D	M20/
J424- D	J535-/M	M20/
P200-42	J410- E	M20R
P201-42	J415-10	M20W
P201- 9	J415-/X	M20W/
P201-26	J416- X	M20WC
J409-41	J420- 8	M22
J420- 8	J423- B	M22
J423- B	J535-12	M22
J409-/W	J421-10	M22/
J421-10	J424- C	M22/
J424- C	J535-/L	M22/
P200-26	J409- N	M22R

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
P201-43	J415- 9	M22W
P201-10	J415-43	M22W/
P201-27	J416-/E	M22WC
J409-40	J420- J	M24
J420- J	J423- 5	M24
J423- 5	J535- M	M24
J409-/V	J421- 9	M24/
J421- 9	J424- M	M24/
J424- M	J535-/N	M24/
P200-44	J409- 5	M24R
P201-44	J415- E	M24W
P201-11	J415-/H	M24W/
P201-28	J416-/F	M24WC
J409-38	J420- L	M26
J420- L	J423- 3	M26
J423- 3	J535- P	M26
J409-39	J421- 5	M26/
J421- 5	J424- L	M26/
J424- L	J535-/K	M26/
P203-34	J409- E	M26R
P202-34	J415- 5	M26W
P202- 1	J415-30	M26W/
P202-18	J416-/L	M26WC
J403-41	J420-11	M30
J420-11	J423- 6	M30
J423- 6	J535- R	M30
J403-/W	J421- 6	M30/
J421- 6	J424- K	M30/
J424- K	J535-/J	M30/
P203-18	J403- N	M30R
P202-35	J415- D	M30W
P202- 2	J415-/J	M30W/
P202-19	J416-/J	M30WC
J403-40	J420-10	M32
J420-10	J423- 4	M32
J423- 4	J535- F	M32
J403-/V	J421- 8	M32/
J421- 8	J424-13	M32/
J424-13	J535-/V	M32/
P203-36	J403- 5	M32R
P202-36	J415- 4	M32W
P202- 3	J415-31	M32W/
P202-20	J416-/S	M32WC

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J403-38	J420- M	M34
J420- M	J423- 1	M34
J423- 1	J535- H	M34
J403-39	J421- 7	M34/
J421- 7	J424- B	M34/
J424- B	J535-/U	M34/
P203-20	J403- E	M34R
P202-37	J415- C	M34W
P202- 4	J415-/K	M34W/
P202-21	J416-/N	M34WC
J402-41	J420- N	M36
J420- N	J423- 2	M36
J423- 2	J535- J	M36
J402-/W	J421- P	M36/
J421- P	J424- A	M36/
J424- A	J535-/T	M36/
P203-38	J402- N	M36R
P202-38	J415- 3	M36W
P202- 5	J415-32	M36W/
P202-22	J416-/U	M36WC
J402-40	J420-18	M40
J420-18	J423-21	M40
J423-21	J535- T	M40
J402-/V	J421- U	M40/
J421- U	J424- N	M40/
J424- N	J535-/F	M40/
P203-22	J402- 5	M40R
P202-39	J415- B	M40W
P202- 6	J415-/L	M40W/
P202-23	J416- B	M40WC
J402-38	J420- Z	M42
J420- Z	J423-25	M42
J423-25	J535-16	M42
J402-39	J421-15	M42/
J421-15	J424- P	M42/
J424- P	J535-28	M42/
P203-40	J402- E	M42R
P202-40	J415- 2	M42W
P202- 7	J415-33	M42W/
P202-24	J416- A	M42WC
J401-41	J420- Y	M44
J420- Y	J423- Z	M44
J423- Z	J535- U	M44
J401-/W	J421-16	M44/
J421-16	J424-17	M44/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J424-17	J535-/E	M44/
P203-24	J401- N	M44R
P202-41	J415- A	M44W
P202- 8	J415-/M	M44W/
P202-25	J416-/W	M44WC
J401-40	J420-/A	M46
J420-/A	J423-23	M46
J423-23	J535- S	M46
J401-/V	J421-18	M46/
J421-18	J424-15	M46/
J424-15	J535-/H	M46/
P203-42	J401- 5	M46R
P202-42	J415- 1	M46W
P202- 9	J415-34	M46W/
P202-26	J416-/X	M46WC
J401-38	J420- W	M50
J420- W	J423- Y	M50
J423- Y	J535-15	M50
J401-39	J421-19	M50/
J421-19	J424- V	M50/
J424- V	J535-29	M50/
P203-26	J401- E	M50R
P202-43	J415- J	M50W
P202-10	J415-/N	M50W/
P202-27	J416-/Y	M50WC
J3 -22	J524-11	NC
J420- S	J421- 2	NC
J421- 2	J524-11	NC
J524-11	J524-12	NC
J524-12	J526-/J	NC
J524-12	J533- T	NC
J420-29	J421-33	NC/
J420-29	J524- R	NC/
J421-33	J437-39	NC/
J524- R	J524- S	NC/
J420-/K	J421-/H	NCU3-
J421-/H	J533-13	NCU3-
J4 -32	J533- W	ND
J429- L	J434- 2	ND
J434- 1	J434- 2	ND
J434- 1	J533- W	ND
J434- 2	J436-27	ND
J429-/U	J436-/P	ND/
J432-20	J436-/P	ND/
J432-20	J434- C	ND/
J434- B	J434- C	ND/
J434- B	J533-21	ND/
J529-33	J533-21	ND/
J429-/L	J525-21	NENT-
J525-21	J526-/X	NENT-

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J420-33	J424-/N	NJ/--
J424-/N	J527-23	NJ/--
J526-/K	J527-24	NJ/--
J526-/K	J548-30	NJ/--
J527-23	J527-24	NJ/--
J526-17	J527-25	NJ/--D
J436-/N	J528-/U	NJT-
J421-/U	J435-/J	NL/-
J435-/J	J436- 1	NL/-
J436- 1	J526-25	NL/-
J522-/C	J526-25	NL/-
J423-/K	J424-24	NL--
J424-24	J427-27	NL--
J427-27	J429-39	NL--
J427-27	J526- K	NL--
J429-39	J431-43	NL--
J431-43	J436-34	NL--
J435-11	J436-34	NL--
J435-11	J437-10	NL--
J437-10	J548-/K	NL--
J526- K	J527-/N	NL--
J527-/N	J527-/P	NL--
J526-31	J527-35	NL--D
J424-/X	J435-/S	NLRC/-
J424-/X	J522- H	NLRC/-
J522- H	J526- E	NLRC/-
J420-36	J424-/T	NMH--
J420-36	J521- T	NMH--
J424-/T	J435-26	NMH--
J435-26	J436- Z	NMH--
J436- Z	J441- 2	NMH--
J441- 2	J548- M	NMH--
J521- T	J527- V	NMH--
J521- T	J525- 6	NMH--
J527- V	J527- W	NMH--
J526-16	J527-19	NMH--D
J8 -26	J548- A	NMHK
J3 -40	J525-41	NP
J422- D	J422- E	NP
J422- E	J425-23	NP
J425-23	J429- V	NP
J429- V	J433-38	NP
J433-38	J437- 3	NP
J437- 3	J537-41	NP
J525-41	J537-41	NP
J422- F	J422- H	NP/
J422- F	J425- F	NP/
J425- F	J429-/B	NP/
J429-/B	J433-42	NP/
J433-42	J437- R	NP/
J437- R	J537-39	NP/
J525-34	J537-39	NP/
J423-/E	J429-31	NPC-
J423-/E	J522- J	NPC-
J429-31	J437-35	NPC-
J436-17	J437-35	NPC-
J522- J	J526-43	NPC-

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
P200- 1	J407- N	NR
J420- A	J421-/M	NRS--
J420- A	J527- 9	NRS--
J421-/M	J423-36	NRS--
J423-36	J424-26	NRS--
J429-43	J431-33	NRS--
J431-33	J435-/D	NRS--
J435-/D	J437- 7	NRS--
J435-/D	J439-41	NRS--
J437- 7	J527-10	NRS--
J527- 9	J527-10	NRS--
J526-12	J527-11	NRS--D
J427-/B	J525-/A	NSC-
J525-/A	J526-/Y	NSC-
J427-33	J525-/D	NST-
J525-/D	J526- B	NST-
J7 -28	J541- E	NT1
J7 -29	J542- E	NT2
J7 -30	J543- E	NT3
J424-32	J427-19	NW-
J427-19	J526- C	NW-
J522- 6	J526- C	NW-
J522- 6	J525-22	NW-
J3 -18	J429- U	NX
J407-41	J420-27	NX
J420-27	J421-29	NX
J421-29	J429- U	NX
J429- U	J525- H	NX
J525- H	J535-14	NX
J407-/W	J421-/D	NX/
J420-/R	J421-/D	NX/
J421-/D	J429-/C	NX/
J429-/C	J525- C	NX/
J525- C	J535-30	NX/
P202-30	J520- F	N24W
P202-29	J520- C	N24W/
J433-/R	J433-/V	OA-
J433-/R	J526-/E	OA-
J433-/V	J437-42	OA-
J425- W	J528-/V	OBSM-
J4 -29	J524-38	OB1
J421-/Y	J425-42	OB1
J425-42	J436- D	OB1
J436- D	J524-37	OB1
J524-37	J524-38	OB1
J421-/X	J436- M	OB1/
J436- M	J524-/T	OB1/
J524-/T	J524-/U	OB1/
J4 -30	J524-30	OB2
J420-32	J427-/F	OB2
J427-/F	J436- 4	OB2
J436- 4	J528-34	OB2

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J524-30	J524-31	OB2
J524-31	J528-34	OB2
J420-/S	J427- Z	OB2/
J427- Z	J524-/K	OB2/
J524-/K	J524-/L	OB2/
J4 -31	J524-/V	OB3
J423-/A	J436- 5	OB3
J436- 5	J528-/P	OB3
J524-/V	J524-/W	OB3
J524-/W	J525- S	OB3
J525- S	J528-/P	OB3
J423-/D	J436- L	OB3/
J436- L	J525-42	OB3/
J524-/X	J524-/Y	OB3/
J524-/X	J525-42	OB3/
J424-36	J436-/W	OCX-
J432-22	J436-/W	OCX-
J432-22	J528- D	OCX-
J433-37	J437-37	OF-
J437-37	J526- M	OF-
J425-26	J435-28	OL--
J435-28	J436-26	OL--
J436-26	J437- L	OL--
J437- L	J527- M	OL--
J526-35	J527- N	OL--
J527- M	J527- N	OL--
J526- P	J527-12	OL--D
J433-/U	J526-/U	OLC-
J425- 4	J526-29	OLF-
J425- 4	J425-/K	OLF-
J425-21	J435-/B	OM-
J425-21	J522-12	OM-
J435-/B	J437-13	OM-
J522-12	J526-/D	OM-
J413- 4	J425-29	OMF--
J413- 4	J522-/A	OMF--
J425-29	J437-/R	OMF--
J522-/A	J525- 3	OMF--
J522-/A	J526-32	OMF--
J526-32	J527-39	OMF--
J527-39	J527-40	OMF--
J526-42	J527-41	OMF--D
J425- 6	J425-41	OMFP-
J425- 6	J526-28	OMFP-
J425-41	J433-39	OMFP-
J429- 5	J433-39	OMFP-
J413- 8	J420-/N	OMO--
J420-/N	J429-/P	OMO--
J429-/P	J432- 3	OMO--
J432- 3	J527- A	OMO--
J432- 3	J537-/L	OMO--
J522-/M	J525-10	OMO--
J525-10	J527- A	OMO--
J526-/N	J527- B	OMO--
J527- A	J527- R	OMO--

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J526- F	J527- E	OMO--D
J429-/R	J526-/C	OMO1/-
J413-34	J431-/P	OP-
J431-/P	J526- N	OP-
J521-23	J526- N	OP-
J521-23	J522-42	OP-
J8 -31	J418- 3	OR
J5 - 5	J448-/J	OT
J5 - 6	J448-/H	OT/
J432-19	J527-14	OU--
J526-38	J527-15	OU--
J527-14	J527-15	OU--
J526- T	J527-17	OU--D
J427-32	J526-/V	OUO-
J420- 5	J425-/U	OX--
J420- 5	J527- P	OX--
J425-/U	J435-/K	OX--
J433-/A	J435-/K	OX--
J435-/K	J437-18	OX--
J527- P	J527- R	OX--
J527- R	J533-/Y	OX--
J526- S	J527-13	OX--D
J421-35	J423-/H	OXPR-
J423-/H	J533-30	OXPR-
J432-27	J437-26	OXUO-
J432-27	J433- A	OXUO-
J433- A	J533-43	OXUO-
J437-26	J439-28	OXUO-
J429-15	J433- 7	OXU2-
J429-15	J432-/X	OXU2-
J432-/X	J437-/P	OXU2-
J433- 7	J533-/M	OXU2-
J435-12	J437-/P	OXU2-
J429- J	J433- X	OY--
J433- X	J437-/T	OY--
J435- T	J437-/T	OY--
J435- T	J533- H	OY--
J526-19	J533- H	OY--
J526-19	J527-/L	OY--
J527-/L	J527-/M	OY--
J526-/H	J527-34	OY--D
J433- B	J437-24	OYAC-
J437-24	J533-11	OYAC-
J433-25	J533- 1	OYRS-
J429-35	J432- Z	OYST-
J432- Z	J433-27	OYST-
J432- Z	J533- M	OYST-
J4 -11	J526- J	01
J413- 3	J420-37	01
J413- 3	J425- 1	01
J420-37	J422-37	01

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J420-37	J421-41	01
J421-41	J431-/R	01
J422-37	J422-38	01
J425- 1	J526- J	01
J431-/R	J433-35	01
J521-33	J522-/B	01
J522-/B	J526- J	01
J413- J	J421-/S	01/
J421-/S	J422-/T	01/
J422-/T	J422-/U	01/
J422-/U	J424-/U	01/
J424-/U	J425-/L	01/
J424-/U	J429-23	01/
J425- 7	J425-/L	01/
J425- 7	J526-/A	01/
J429-23	J435-/A	01/
J435-/A	J437- U	01/
J437- U	J437-/X	01/
J522-24	J526-/A	01/
J526-/A	J533-18	01/
J533-18	J537-/C	01/
J4 -12	J526-13	02
J420-38	J424-/S	02
J420-38	J422- U	02
J422- T	J422- U	02
J424-/S	J436-29	02
J436-29	J437- C	02
J437- C	J528-10	02
J521-/D	J526-13	02
J526-13	J528-10	02
J420-34	J436-/B	02/
J420-34	J422- X	02/
J422- W	J422- X	02/
J436-/B	J437- H	02/
J437- H	J533- U	02/
J521- Z	J526- W	02/
J526- W	J533- U	02/
J4 -13	J525- E	03
J422-/C	J422-/D	03
J422-/C	J525- F	03
J422-/D	J433-26	03
J525- E	J526-18	03
J526-18	J548-/L	03
J413- M	J422-/F	03/
J422-/F	J422-/H	03/
J422-/H	J436-30	03/
J436-30	J437-/D	03/
J437-/D	J533-17	03/
J522-/T	J526- 9	03/
J526- 9	J533-17	03/
J533-17	J548-/H	03/
J527-/C	J527-/D	031/--
J527-/C	J528- K	031/--
J527-/D	J529-32	031/--
J526- V	J527-26	031/--D
J4 -14	J525-/B	04
J413- A	J522- V	04
J420-35	J422-/N	04
J422-/M	J436-32	04
J422-/M	J422-/N	04
J436-32	J437-/C	04

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J437-/C	J533-16	O4
J521-/F	J522- V	O4
J521-/F	J526-/B	O4
J525-/B	J526-/B	O4
J526-/B	J533-16	O4
J420-39	J421-/T	O4/
J421-/T	J422-/R	O4/
J422-/P	J422-/R	O4/
J422-/P	J528- 8	O4/
J422-/R	J433-36	O4/
J526-41	J528- 8	O4/
J8 -29	J548-/M	PHK
J8 -34	J548- 7	PK
J5 - 9	J448-/W	PTK
J5 -10	J448-/X	PTK/
J5 -11	J448-/T	PTT
J5 -12	J448-/U	PTT/
J441- 3	J446- X	PVE
J6 -25	J446-22	PVEC
J8 -35	J548-18	PVK
J4 -34	J422-/V	P1
J422-/V	J422-/W	P1
J422-/W	J425-/P	P1
J425-/P	J435-30	P1
J435-30	J441- 9	P1
J441- 9	J548- Z	P1
J422-/X	J422-/Y	P1/
J422-/X	J441- 7	P1/
J441- 7	J548- 4	P1/
J4 -35	J431- V	P2
J422-11	J422-12	P2
J422-12	J425-39	P2
J425-39	J431- V	P2
J431- V	J432- 7	P2
J432- 7	J441-11	P2
J441-11	J548-/C	P2
J422- R	J422- S	P2/
J422- S	J432- S	P2/
J432- S	J441-12	P2/
J441-12	J548- 3	P2/
J4 -36	J432- 8	P3
J422-30	J422-31	P3
J422-30	J425-19	P3
J425-19	J432- 8	P3
J425-19	J519-17	P3
J519-17	J548- B	P3
J422-/K	J422-/L	P3/
J422-/K	J519-19	P3/
J3 -39	J526- H	Q
J428-/V	J428-/W	Q
J428-/W	J526- H	Q

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J428-/X	J428-/Y	Q/
J428-/X	J437-31	Q/
J435- U	J437-31	Q/
J435- U	J528-26	Q/
J522-/K	J528-26	Q/
J401- X	J401-20	RAR
J401-20	J402- X	RAR
J402- X	J402-20	RAR
J402-20	J403- X	RAR
J403- X	J403-20	RAR
J403-20	J409- X	RAR
J409- X	J409-20	RAR
J409-20	J410- X	RAR
J410- X	J410-20	RAR
J410-20	J411- X	RAR
J411- X	J411-20	RAR
J411-20	J412- X	RAR
J412- X	J412-20	RAR
J412-20	J419-/V	RAR
J404- X	J404-20	RAR 1
J404-20	J405- X	RAR 1
J405- X	J405-20	RAR 1
J405-20	J406- X	RAR 1
J406- X	J406-20	RAR 1
J406-20	J407- X	RAR 1
J407- X	J407-20	RAR 1
J407-20	J408- X	RAR 1
J408- X	J408-20	RAR 1
J408-20	J418-30	RAR 1
J3 -36	J526- Z	RC
J430-/M	J430-/N	RC
J430-/M	J431-27	RC
J431-27	J435-10	RC
J435-10	J526- Z	RC
J521-/R	J526- Z	RC
J430-/P	J430-/R	RC/
J430-/P	J431-30	RC/
J430-/R	J526- Y	RC/
J431-30	J435-/H	RC/
J521-38	J526- Y	RC/
J526- Y	J548-28	RC/
J4 -37	J430-31	RK
J420-/W	J421-/K	RK
J421-/K	J430-31	RK
J421-/K	J521-37	RK
J430-30	J430-31	RK
J430-31	J431-32	RK
J420-/H	J421- Z	RK/
J421- Z	J430-/K	RK/
J421- Z	J521-/T	RK/
J430-/K	J430-/L	RK/
J430-/L	J431- J	RK/
P202-13	J520-/K	RP
P202-12	J520-/P	RP/
P203- 5	J404- N	RR
J4 -38	J431-29	RS
J430- D	J430- E	RS
J430- D	J521-/L	RS
J430- E	J431-29	RS

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J430- F	J430- H	RS/
J430- F	J521-/V	RS/
J430- H	J431-28	RS/
J4 -39	J430-/C	RT
J430-/C	J430-/D	RT
J430-/D	J521-35	RT
J430-/F	J430-/H	RT/
J430-/H	J521-/K	RT/
J3 -33	J431-/J	RX
J404-41	J420-/E	RX
J420-/E	J421-/J	RX
J421-/J	J431-/J	RX
J431-/J	J535-13	RX
J521-/N	J535-13	RX
J404-/W	J420-/X	RX/
J420-/X	J421-/A	RX/
J420-/X	J431-/C	RX/
J421-/A	J521-36	RX/
J521-36	J535-31	RX/
J4 -48	J525-39	S
J406-41	J421-40	S
J421-40	J424-/R	S
J424-/R	J431-35	S
J431-35	J448-/F	S
J448- X	J448-/E	S
J448- X	J537-38	S
J525-39	J537-38	S
J406-/W	J525-40	S/
J525-40	J537-40	S/
J4 -26	J524-/C	SB1
J425-38	J522- M	SB1
J522- M	J524-/D	SB1
J524-/C	J524-/D	SB1
J522-41	J524-/F	SB1/
J524-/F	J524-/H	SB1/
J4 -27	J524- D	SB2
J424-33	J429- F	SB2
J429- F	J433-/K	SB2
J429- F	J524- D	SB2
J433-/K	J433-/X	SB2
J433-/K	J548-16	SB2
J522- 5	J524- E	SB2
J524- D	J524- E	SB2
J420-40	J424-/L	SB2/
J424-/L	J522- K	SB2/
J429- C	J524- F	SB2/
J522- K	J524- H	SB2/
J524- F	J524- H	SB2/
J4 -28	J525-28	SB3
J433-/Y	J524- 1	SB3
J522- N	J525-28	SB3
J522- N	J524- 1	SB3
J524- 1	J524- 2	SB3
J525-28	J548-15	SB3
J522- A	J524- B	SB3/
J524- B	J524- C	SB3/
J524- C	J525-23	SB3/
J525-23	J548- K	SB3/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J433-/N	J441- D	SB41
J439-24	J446- R	SCT
J6 -24	J446-16	SCTO
J439-25	J446-/D	SC1
J6 -19	J446-28	SC10
J439-/F	J446-/L	SC2
J6 -20	J446-34	SC20
J439-26	J446-/T	SC3
J413-37	J528- B	SC3-
J6 -21	J446-40	SC30
J439-27	J446- B	SC4
J6 -22	J446- D	SC40
J439-/E	J446- J	SC5
J6 -23	J446-10	SC50
J439-/H	J527- 5	SC6--
J527- 5	J527- 6	SC6--
J526- 6	J527- 7	SC6--D
J418-14	J448- V	SD **
J8 -36	J418- P	SI
J8 -20	J448-/C	SK
J8 -21	J448- Y	SK/
P203-16	J406- N	SR
J417-/T	J418-/M	ST
J401-/B	J401-24	STROBE
J401-24	J402-/B	STROBE
J402-/B	J402-24	STROBE
J402-24	J403-/B	STROBE
J403-/B	J403-24	STROBE
J403-24	J404-/B	STROBE
J404-/B	J404-24	STROBE
J404-24	J405-/B	STROBE
J405-/B	J405-24	STROBE
J405-24	J406-/B	STROBE
J406-/B	J406-24	STROBE
J406-24	J407-/B	STROBE
J407-/B	J407-24	STROBE
J407-24	J408-/B	STROBE
J408-/B	J408-24	STROBE
J408-24	J409-/B	STROBE
J409-/B	J409-24	STROBE
J409-24	J410-/B	STROBE
J410-/B	J410-24	STROBE
J410-24	J411-/B	STROBE
J411-/B	J411-24	STROBE
J411-24	J412-/B	STROBE
J412-/B	J412-24	STROBE
J412-24	J418-42	STROBE
P204- 5	J418-/L	SOL
J415-16	J416-18	SOO

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J415- S	J416-14	S02
J415-17	J416-16	S04
J415- T	J416-10	S06
J4 -23	J528- L	S1
J519- 4	J523-12	S1
J523-11	J523-12	S1
J523-11	J528- L	S1
J448-/L	J448-41	S1/
J448-/L	J519- 3	S1/
J519- 3	J523- R	S1/
J523- R	J523- S	S1/
J415-18	J416- 8	S10
J415- U	J416-12	S12
J415-19	J416- 4	S14
J415- V	J416- 6	S16
J4 -24	J523-38	S2
J448-33	J448-40	S2
J448-33	J528- 6	S2
J519- D	J523-38	S2
J523-37	J528- 6	S2
J523-37	J523-38	S2
J519- 5	J523-/T	S2/
J523-/T	J523-/U	S2/
J415-/F	J416- W	S20
J415-/E	J416-27	S22
J415-24	J416-28	S24
J415-25	J416-32	S26
J4 -25	J523-/W	S3
J519- E	J523-/V	S3
J523-/V	J523-/W	S3
J448-/M	J448-/V	S3/
J448-/M	J528- F	S3/
J519- 6	J528- F	S3/
J519- 6	J523-/X	S3/
J523-/X	J523-/Y	S3/
J415-26	J416-30	S30
J415-27	J416-37	S32
J415-28	J416-34	S34
J415-29	J416-39	S36
J415- 7	J416- 2	S40
J415- H	J416- 1	S42
J415-38	J416-41	S44
J415-/S	J416-42	S46
J415-35	J416-43	S50
J415-/Y	J548- Y	S50W

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J431-/Y	J548- E	T
J420-26	J431-37	T/
J431-37	J548-10	T/
J7 - 6	J548- N	T/C
J8 -38	J548- D	TC
J519-37	J521-13	TCD-
J521-13	J529- P	TCD-
J421-39	J431-/T	TEH-
J431-/T	J529- 4	TEH-
J521-/W	J525-/M	TEH-
J525-/M	J529- 4	TEH-
J3 -48	J526-36	TP
J413-21	J423-/P	TP
J423-/P	J428-37	TP
J427- 5	J428-37	TP
J427- 5	J529- 2	TP
J427- 5	J526-36	TP
J428-37	J428-38	TP
J427- 8	J529- 1	TP/
J428-/T	J428-/U	TP/
J428-/T	J431-31	TP/
J431-31	J529- 1	TP/
J519-16	J525- 7	TP/
J522-/R	J526-/R	TP/
J525- 7	J528- H	TP/
J525- 7	J526-/R	TP/
J526-/R	J533-35	TP/
J528- H	J529- 1	TP/
J519- B	J519-/S	TPA--
J519- B	J522- D	TPA--
J521- J	J522- D	TPA--
J522- D	J530- 9	TPA--
J530- 9	J537-37	TPA--
J530- 9	J530-10	TPA--
J529-12	J530-11	TPA--D
J429- Z	J431-23	TPB--
J431-23	J432-25	TPB--
J431-23	J530- 2	TPB--
J432-25	J435-/E	TPB--
J435-/E	J436-18	TPB--
J435-/E	J439-35	TPB--
J439-35	J448-/F	TPB--
J530- 2	J530- 3	TPB--
J530- 3	J533-22	TPB--
J529- 7	J530- 4	TPB--D
J534-36	J534-37	TPX0/--
J4 -15	J525- 1	TPX0/--
J413-22	J423-/N	TPX0/--
J423-/N	J424-21	TPX0/--
J424-21	J427-24	TPX0/--
J424-21	J525- 1	TPX0/--
J427-24	J435-/M	TPX0/--
J435-/M	J437-/N	TPX0/--
J435-/M	J534-36	TPX0/--
J519- W	J521- W	TPX0/--
J521- W	J525- 1	TPX0/--
J533-38	J534-38	TPX0/--D

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J3 -49	J428- D	TX
J413-/T	J419-25	TX
J419-25	J420-30	TX
J420-30	J421-30	TX
J421-30	J424-31	TX
J424-31	J425-34	TX
J424-31	J429- P	TX
J427- E	J428- E	TX
J427- E	J519- 7	TX
J428- D	J428- E	TX
J428- E	J429- P	TX
J519- U	J519- 7	TX
J519- U	J529-31	TX
J529-31	J533-19	TX
J529-31	J537-36	TX
J419-24	J420-/M	TX/
J420-/M	J433-29	TX/
J420-/M	J421-28	TX/
J421-28	J427- F	TX/
J427- F	J428- F	TX/
J427- F	J522- W	TX/
J428- F	J428- H	TX/
J519-43	J522- W	TX/
J522- W	J533-36	TX/
J431-17	J432-18	TXA--
J431-17	J433- 2	TXA--
J432-18	J437- W	TXA--
J433- 2	J528- 9	TXA--
J435-29	J436-28	TXA--
J436-28	J437- W	TXA--
J521-25	J522-26	TXA--
J522-26	J525-35	TXA--
J525-35	J530-/N	TXA--
J528- 9	J530-/P	TXA--
J530-/N	J530-/P	TXA--
J529-/M	J530-35	TXA--D
J8 -28	J419-31	TXK
J8 -27	J419-32	TXK/
J3 -50	J525- P	TO
J413-36	J423-43	TO
J423-43	J424-/V	TO
J424-/V	J521- 1	TO
J428- J	J428- K	TO
J428- J	J525- P	TO
J428- J	J521- 1	TO
J428- K	J429- 9	TO
J519-/A	J525- Z	TO
J521- 1	J522-11	TO
J522-11	J525- Z	TO
J525- Z	J529-41	TO
J428- L	J428- M	TO/
J428- L	J522-27	TO/
J428- M	J431-16	TO/
J431-16	J433-16	TO/
J433-16	J437-11	TO/
J437-11	J441-17	TO/
J519-/V	J522-27	TO/
J519-/V	J533-37	TO/
J431- M	J432- 2	TOA--
J432- 2	J433- 1	TOA--
J432- 2	J530-42	TOA--
J433- 1	J435- E	TOA--

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J435- E	J436-20	TOA--
J435- E	J437- 4	TOA--
J526-37	J530-42	TOA--
J530-42	J530-43	TOA--
J529-/S	J530-/T	TOA--D
J413- 5	J427- 9	T1-
J425-22	J427- 9	T1-
J425-22	J432-43	T1-
J427- 9	J529-21	T1-
J529-21	J537-/F	T1-
J431-11	J435- 2	T10-
J435- 2	J529-22	T10-
J425- 5	J429-28	T11--
J427- 4	J429-28	T11--
J427- 4	J530- P	T11--
J429-28	J431-/V	T11--
J431-/V	J432-/P	T11--
J431-/V	J436-39	T11--
J436-39	J437-/V	T11--
J530- P	J530- R	T11--
J529- S	J530-13	T11--D
J427- J	J429- Y	T12-
J427- J	J437-12	T12-
J427- J	J529-16	T12-
J435-/U	J437-12	T12-
J521-39	J529-16	T12-
J425- L	J522-23	T13--
J425- L	J425-/V	T13--
J425-/V	J429-30	T13--
J427- H	J431- P	T13--
J429-30	J431- P	T13--
J431- P	J432- N	T13--
J432- N	J530- F	T13--
J435- Z	J436- C	T13--
J435- Z	J437-40	T13--
J436- C	J530- F	T13--
J522-23	J528-43	T13--
J530- F	J530- H	T13--
J529- 3	J530- 1	T13--D
J413- F	J425-37	T14-
J425-37	J435-/X	T14-
J435-/X	J529-/K	T14-
J429-21	J431-22	T15-
J431-22	J432-17	T15-
J432-17	J529-/A	T15-
J529-/A	J537-/B	T15-
J427- L	J432- T	T16-
J432- T	J529-/J	T16-
J432- T	J437-25	T16-
J435-39	J436-/R	T16-
J436-/R	J437-25	T16-
J432-11	J436-/S	T17-
J432-11	J525-/F	T17-
J525-/F	J529-/T	T17-
J435-42	J525- V	T18-
J525- V	J529-/W	T18-

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J432- L	J525- 5	T19-
J525- 5	J529-/R	T19-
J413- E	J429-22	T2-
J429-22	J431- X	T2-
J431- X	J432- U	T2-
J432- U	J435- B	T2-
J435- B	J529-/L	T2-
J424-/W	J427- M	T20-
J424-/W	J435-34	T20-
J427- M	J525-12	T20-
J525-12	J529-/U	T20-
J432- K	J529-/X	T21-
J525-36	J529-/X	T21-
J435-31	J436-/Y	T22-
J435-31	J529-/Y	T22-
J525-/R	J529-/Y	T22-
J432- J	J435- 9	T23-
J432- J	J529-/F	T23-
J525- Y	J529-/F	T23-
J420-42	J424-/P	T24--
J424-/P	J429-24	T24--
J427-10	J429-24	T24--
J427-10	J521-10	T24--
J429-24	J431-/U	T24--
J431-/U	J437-20	T24--
J436-13	J437-20	T24--
J521-10	J522-36	T24--
J522-36	J525-33	T24--
J525-33	J530-24	T24--
J530-23	J530-24	T24--
J529-23	J530-25	T24--D
J435- 5	J437-22	T4-
J435- 5	J529-/B	T4-
J525-/H	J529-/B	T4-
J427- 7	J432-34	T5-
J427- 7	J525- W	T5-
J525- W	J529- Z	T5-
J436-/A	J528- 4	T816-
P202-32	J518-/K	UP
P202-31	J518-/P	UP/
P203- 3	J404- 5	UR
J3 -26	J423-35	UX
J404-40	J420-21	UX
J420-21	J423-35	UX
J420-21	J519-21	UX
J423-35	J437-/L	UX
J437-/L	J535- B	UX
J404-/V	J421- V	UX/
J421- V	J424-/H	UX/
J421- V	J519- Y	UX/
J423-/S	J424-/H	UX/
J519- Y	J535-/X	UX/
J519-/R	J521-16	VA0-
J521-16	J526-/W	VA0-

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J519-39	J521-15	VA1-
J521-15	J526-40	VA1-
J519-35	J521-19	VA2-
J521-19	J526-30	VA2-
J519-/P	J521-21	VA3-
J521-21	J526- L	VA3-
J3 -35	J523- J	VC
J523- J	J523- K	VC
J523- K	J526-/S	VC
J523- L	J523- M	VC/
J523- M	J526-22	VC/
J526-22	J528-33	VC/
J528-33	J548-/F	VC/
J414-/D	J414-26	VCC
J414-26	J518-26	VCC
J414-26	J422-/A	VCC
J422-/A	J422-/B	VCC
J422-/B	J426-/B	VCC
J426-/A	J426-/B	VCC
J426-/A	J428-/A	VCC
J428-/A	J428-/B	VCC
J428-/B	J430-/B	VCC
J430-/A	J430-/B	VCC
J430-/A	J434-/A	VCC
J434-/A	J434-/B	VCC
J434-/B	J438-/B	VCC
J438-/A	J438-/B	VCC
J438-/A	J440-/A	VCC
J440-/A	J440-/B	VCC
J518-/D	J518-26	VCC
J518-/D	J520-26	VCC
J520-/D	J520-26	VCC
J520-/D	J523-/A	VCC
J523-/A	J523-/B	VCC
J523-/B	J524-/B	VCC
J524-/A	J524-/B	VCC
J524-/A	J536-/A	VCC
J536-/A	J536-/B	VCC
J536-/B	J538-/B	VCC
J538-/A	J538-/B	VCC
J4 -40	J523- 2	VK
J420-/U	J421-32	VK
J421-32	J523- 1	VK
J519-/T	J523- 2	VK
J523- 1	J523- 2	VK
J420-/D	J421-/B	VK/
J421-/B	J523- B	VK/
J519-23	J521-12	VK/
J521-12	J523- C	VK/
J523- B	J523- C	VK/
P202-47	J518-/T	VP
P202-46	J518-/Y	VP/
P203- 1	J404- E	VR
J8 -37	J548-/D	VRK
J4 -41	J523- E	VS
J423-/U	J523- D	VS
J519-38	J521-18	VS

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J521-18	J523- E	VS
J523- D	J523- E	VS
J423-/T	J523- F	VS/
J519-36	J521-24	VS/
J521-24	J523- F	VS/
J523- F	J523- H	VS/
J544- X	J548- F	VS0
J544-/B	J548-/B	VS1
J546- X	J548-33	VS2
J546-/B	J548- U	VS3
J533-/S	J534- V	VT--
J534- V	J534- W	VT--
J533-15	J534-19	VT-
J3 -32	J526-24	VX
J404-38	J420-/C	VX
J420-/C	J421-31	VX
J420-/C	J519-18	VX
J421-31	J423-32	VX
J519-/M	J519-18	VX
J519-18	J521- P	VX
J521- P	J526-24	VX
J526-24	J535-10	VX
J404-39	J421-/C	VX/
J420-/V	J421-/C	VX/
J420-/V	J423-41	VX/
J421-/C	J519- Z	VX/
J519- Z	J519-40	VX/
J519- Z	J521-17	VX/
J519-40	J535-33	VX/
J521-17	J526-11	VX/
J539-/E	J541- D	V1
J541- A	J541- 1	V1A
J541- A	J544-/Y	V1A
J544-/Y	J546-/Y	V1A
J533-/K	J537- 5	V1P-
J439- A	J537-18	V1S-
J533-40	J537-18	V1S-
J5 -19	J541- 7	V1T
J10 - 9	J544- 2	V10 0
J11 - 9	J440- 1	V11
J440- 1	J440- 2	V11
J6 -34	J544-42	V11 0
J440- B	J440- C	V11/
J440- B	J539- B	V11/
J11 -10	J439- 1	V12
J439- 1	J440- D	V12
J440- D	J440- E	V12
J6 -36	J546- 2	V12 0
J439- D	J440- F	V12/
J440- F	J440- H	V12/
J440- F	J539- E	V12/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J11 -11	J440- K	V13
J439- 3	J440- J	V13
J440- J	J440- K	V13
J6 -38	J546-42	V13 0
J439- C	J440- L	V13/
J440- L	J440- M	V13/
J440- L	J539- K	V13/
J11 -12	J439- 2	V14
J439- 2	J536-/C	V14
J536-/C	J536-/D	V14
J439- B	J536-/F	V14/
J536-/F	J536-/H	V14/
J536-/F	J539- P	V14/
J11 -13	J536- 1	V15
J536- 1	J536- 2	V15
J536- B	J536- C	V15/
J536- B	J539- T	V15/
J11 -14	J536- D	V16
J536- D	J536- E	V16
J536- F	J536- H	V16/
J536- F	J539- X	V16/
J11 -16	J536- J	V17
J536- J	J536- K	V17
J536- L	J536- M	V17/
J536- L	J539-/B	V17/
J11 -17	J536-11	V18
J536-11	J536-12	V18
J536-12	J539-/F	V18
J536- R	J536- S	V18/
J540-/U	J542- D	V2
J542- A	J542- 1	V2A
J542- A	J544- C	V2A
J544- C	J546- C	V2A
J539-/X	J540-/P	V2M
J533-41	J537- H	V2P-
J439-15	J537-/A	V2S-
J533-39	J537-/A	V2S-
J5 -20	J542- 7	V2T
J10 -10	J544- A	V20 0
J11 -18	J440-/C	V21
J440-/C	J440-/D	V21
J6 -40	J544- Z	V21 0
J440-/F	J440-/H	V21/
J440-/F	J539-/L	V21/
J11 -19	J439- S	V22
J439- S	J440- T	V22
J440- T	J440- U	V22

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J6 -42	J546- A	V22 0
J439- P	J440- W	V22/
J440- W	J440- X	V22/
J440- W	J539-/R	V22/
J11 -20	J439-18	V23
J439-18	J440-12	V23
J440-11	J440-12	V23
J6 -44	J546- Z	V23 0
J439- M	J440- R	V23/
J440- R	J440- S	V23/
J440- R	J539-/V	V23/
J11 -21	J439-10	V24
J439-10	J538-37	V24
J538-37	J538-38	V24
J439- J	J538-/T	V24/
J538-/T	J538-/U	V24/
J538-/T	J539-/Y	V24/
J11 -22	J538- T	V25
J538- T	J538- U	V25
J538- W	J538- X	V25/
J538- W	J540-/L	V25/
J11 -23	J538-/C	V26
J538-/C	J538-/D	V26
J538-/F	J538-/H	V26/
J538-/F	J540-/R	V26/
J11 -24	J538-/M	V27
J538-/M	J538-/N	V27
J538-/P	J538-/R	V27/
J538-/P	J540-/V	V27/
J11 -25	J538-/W	V28
J538-/W	J540-/Y	V28
J538-/X	J538-/Y	V28/
J540-/E	J543- D	V3
J543- A	J543- 1	V3A
J543- A	J544- N	V3A
J544- N	J546- N	V3A
J533-/L	J537-/P	V3P-
J439- U	J537- Z	V3S-
J533-31	J537- Z	V3S-
J5 -21	J543- 7	V3T
J10 -11	J544- K	V30 0
J11 -26	J440-30	V31
J440-30	J440-31	V31
J6 -46	J544-/E	V31 0
J440-/K	J440-/L	V31/
J440-/K	J540- B	V31/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J11 -27	J439-19	V32
J439-19	J440-/M	V32
J440-/M	J440-/N	V32
J6 -48	J546- K	V32 0
J439- W	J440-/P	V32/
J440-/P	J440-/R	V32/
J440-/P	J540- E	V32/
J11 -28	J440-38	V33
J439- V	J440-37	V33
J440-37	J440-38	V33
J6 -50	J546-/E	V33 0
J439-17	J440-/T	V33/
J440-/T	J440-/U	V33/
J440-/T	J540- K	V33/
J11 -29	J439-16	V34
J439-16	J538- 1	V34
J538- 1	J538- 2	V34
J439- T	J538- B	V34/
J538- B	J538- C	V34/
J538- B	J540- P	V34/
J11 -30	J538- D	V35
J538- D	J538- E	V35
J538- F	J538- H	V35/
J538- F	J540- T	V35/
J11 -31	J538- J	V36
J538- J	J538- K	V36
J538- L	J538- M	V36/
J538- L	J540- X	V36/
J11 -32	J538-11	V37
J538-11	J538-12	V37
J538- R	J538- S	V37/
J538- R	J540-/B	V37/
J11 -33	J538-30	V38
J538-30	J538-31	V38
J538-31	J540-/F	V38
J538-/K	J538-/L	V38/
J4 -42	J528-/S	WA
J436-/V	J521- 3	WA
J521- 3	J523-/C	WA
J523-/C	J523-/D	WA
J523-/D	J528-/S	WA
J431-13	J436-38	WA/
J431-13	J441- 8	WA/
J431-13	J521- 2	WA/
J521- 2	J523-/F	WA/
J523-/F	J523-/H	WA/
J523-/H	J528-/T	WA/
J4 -43	J528-36	WB
J431- 5	J441- E	WB
J431- 5	J529-10	WB
J523- T	J523- U	WB
J523- T	J529-10	WB

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J528-36	J529-10	WB
J431-12	J523- W	WB/
J521-40	J523- X	WB/
J521-40	J528-38	WB/
J523- W	J523- X	WB/
J431-/H	J529-15	WBB3/-
J521-/M	J529-15	WBB3/-
J414-/T	J415-/R	WC0
J415-/R	J419-27	WC0
J414-/K	J419-29	WC1
J414-/K	J431- F	WC1
J415-11	J419-28	WC1X
J414- H	J419-22	WH0
J415-36	J419-22	WH0
J414- T	J419-20	WH1
J419-20	J431- S	WH1
J415- 8	J419-21	WH1X
J431-25	J528-/Y	W0-
J431- T	J521- F	W1-
J521- F	J528-/X	W1-
J441- 6	J447-/D	W21
J6 -30	J447-28	W21C
J431- 6	J521-11	W3-
J521-11	J528-/W	W3-
J435- D	J446-/J	X1
J7 - 8	J446-32	X1C
J432-/K	J444-/J	X10
J9 - 5	J444-32	X10C
J435- 1	J447- E	X11
J10 -19	J447- 6	X11C
J432-36	J444-/P	X12
J6 - 8	J444-35	X12C
J435-/V	J447- F	X13
J10 -20	J447- 7	X13C
J432- M	J444-/R	X14
J6 - 9	J444-38	X14C
J435-/Y	J447- M	X15
J6 -10	J447-11	X15C
J432-12	J444-/W	X16
J6 -11	J444-42	X16C
J435-40	J447- N	X17
J6 -12	J447-14	X17C
J432-10	J444-/X	X18
J10 -21	J444-43	X18C
J435-43	J447- U	X19
J9 -10	J447-17	X19C
J6 -13	J446-17	X193
J432-/L	J445-/B	X2
J7 - 9	J445-26	X2C
J435- A	J446-/P	X3
J7 -10	J446-35	X3C
J432-32	J445-/H	X4
J7 -11	J445-29	X4C
J435- 4	J446-/R	X5
J9 - 7	J446-38	X5C
J432-/N	J444-/B	X6
J10 -23	J444-26	X6C
J435- S	J446-/W	X7
J9 - 2	J446-42	X7C
J432-/M	J444-/H	X8
J9 - 3	J444-29	X8C
J435- P	J446-/X	X9
J9 - 4	J446-43	X9C
J435- 7	J445-/J	Y1
J10 - 1	J445-32	Y1C
J432-/S	J445- U	Y10
J9 -13	J445-17	Y10C
J435- 3	J446- E	Y11
J9 -14	J446- 6	Y11C
J432-/R	J445- V	Y12
J9 -15	J445-19	Y12C
J435-/T	J446- F	Y13
J9 -16	J446- 7	Y13C
J432- B	J445-/A	Y14
J9 -17	J445-23	Y14C
J435-/W	J446- M	Y15
J9 -44	J446-11	Y15C

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J432- C	J444- M	Y16
J9 -45	J444-11	Y16C
J435-38	J446- N	Y17
J9 -46	J446-14	Y17C
J432- P	J444- N	Y18
J9 - 9	J444-14	Y18C
J435-41	J446- U	Y19
J6 -13	J446-17	Y19C
J432-42	J445- E	Y2
J10 - 2	J445- 6	Y2C
J432- E	J444- U	Y20
J6 -14	J444-17	Y20C
J435-35	J446- V	Y21
J6 -15	J446-19	Y21C
J432- F	J444- V	Y22
J6 -16	J444-19	Y22C
J435-32	J446-/A	Y23
J6 -17	J446-23	Y23C
J432- H	J444-/A	Y24
J7 -27	J444-23	Y24C
J435- C	J445-/P	Y3
J10 - 3	J445-35	Y3C
J432-39	J445- F	Y4
J10 - 4	J445- 7	Y4C
J435- H	J445-/R	Y5
J7 -12	J445-38	Y5C
J432-35	J445- M	Y6
J7 -13	J445-11	Y6C
J435- J	J445-/W	Y7
J7 -26	J445-42	Y7C
J432-33	J445- N	Y8
J9 -11	J445-14	Y8C
J435- N	J445-/X	Y9
J9 -12	J445-43	Y9C
J4 -44	J523-31	Z1
J521- 6	J523-30	Z1
J523-30	J523-31	Z1
J521- 5	J523-/K	Z1/
J523-/K	J523-/L	Z1/

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J4 -45	J523-/N	Z2
J521- 7	J523-/M	Z2
J523-/M	J523-/N	Z2
J521- 8	J523-/P	Z2/
J523-/P	J523-/R	Z2/
J434-43	J437-43	0AC
J434-15	J437- T	0AK
J433-15	J434-29	0AP
J413-13	J414- E	0A23
J433-/J	J434-40	0A24
J434-40	J537-/N	0A24
J427-16	J428-29	0B1
J427- B	J428-36	0B2
J427- C	J428- 4	0B3
J427-11	J428-19	0B4
J427-13	J428-15	0B5
J427-17	J428-33	0B6
J425-31	J426-40	0CB1
J425-/M	J426-33	0CB2
J425-/M	J425-40	0CB2
J425-15	J426- 7	0CB3
J425- A	J426- 4	0CB4
J425-24	J426-19	0CB5
J426-43	J427-43	0CP1
J426-29	J427-29	0CP2
J426-36	J427-30	0CP3
J426-15	J427- V	0CP4
J426-10	J427- U	0CP5
J429-32	J430-19	0C1
J429-/D	J430-43	0C2
J430-10	J432- 1	0C3
J429- A	J430- 4	0C4
J429-27	J430-15	0C5
J434-33	J436-/L	0D
J436- W	J438-10	0DC
J437-/J	J438- 7	0DR
J438-43	J439-/X	0D1
J438-36	J439-/T	0D2
J438-33	J439-/V	0D3

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J438-40	J439-/W	0D4
J437- S	J438- 4	0D5
J434-10	J436-15	0E
J518- Z	J519-12	0EP
J420- 1	J422- 4	0FC
J518- R	J519- N	0FP
J519- N	J519-/K	0FP
J438-15	J439-/D	0G1
J438-29	J439-/B	0G2
J438-19	J439-/C	0G3
J518- E	J519- M	0HP
J536-36	J537-/H	0HS
J430-40	J432-31	0IC
J432-15	J434-19	0ID
J422-10	J424-30	0IP
J520-/X	J521-/X	0I24
J434-36	J435-22	0J
J536-43	J537-35	0JT
J434- 7	J435-16	0K
J522-32	J524-19	0LC
J522-/V	J524-36	0LP
J522-16	J524-10	0LX
J520- R	J522-17	0L24
J535-36	J536-33	0MPX
J522-31	J524-15	0NC
J434- 4	J436- P	0ND
J421- 1	J422- 7	0NP
J520- E	J525-/L	0N24W
J524-40	J525-/K	00B1
J524-33	J525-/V	00B2
J524-43	J525-32	00B3
J421-/V	J422-40	001
J420-43	J422-19	002
J422-29	J423-29	003
J422-36	J424-29	004
J421-43	J422-43	0P1
J421-26	J422-15	0P2

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J422-33	J423-31	0P3
J428-43	J429-/H	0Q
J430-36	J431-39	0RC
J430-33	J431-/K	0RK
J520-/S	J521-43	0RP
J430- 7	J431-15	0RS
J430-29	J431-26	0RT
J524-29	J525-31	0SB1
J524- 7	J525-15	0SB2
J524- 4	J525-30	0SB3
J522-/W	J523-15	0S1
J522-/X	J523-40	0S2
J522-/Y	J523-43	0S3
J427-18	J428-40	0TP
J427- 2	J428- 7	0TX
J428-10	J429- 1	0T0
J518-/S	J519-28	0UP
J522- B	J523-10	0VC
J521- V	J523- 4	0VK
J518-/X	J519-/L	0VP
J521- 4	J523- 7	0VS
J439- 5	J440- 4	0V11
J439- 6	J440- 7	0V12
J439- H	J440-10	0V13
J536-29	J537-26	0V14
J536- 4	J537- 9	0V15
J536- 7	J537-10	0V16
J536-10	J537- B	0V17
J536-15	J537- A	0V18
J439- N	J440-29	0V21
J439-11	J440-19	0V22
J439- 8	J440-15	0V23
J537-27	J538-40	0V24
J537- 8	J536-19	0V25
J537- 7	J538-29	0V26
J537-34	J538-36	0V27

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J537-33	J538-43	0V28
J439-20	J440-33	0V31
J439-22	J440-36	0V32
J439-/A	J440-40	0V33
J537-28	J538- 4	0V34
J537-32	J538- 7	0V35
J537-31	J538-10	0V36
J537-29	J538-15	0V37
J537-30	J538-33	0V38
J523-29	J525- T	0WA
J523-19	J525-18	0WB
J413-/J	J414-/X	0WC0
J413-42	J414-/S	0WC1
J413- S	J414- R	0WH0
J413-/K	J414- Z	0WH1
J521-29	J523-33	0Z1
J521-31	J523-36	0Z2
J434-41	J437-/Y	1AC
J434- N	J437-27	1AK
J433-/F	J434-26	1AP
J413- 2	J414- A	1A23
J433-/W	J434-/S	1A24
J427- S	J428-26	1B1
J427-/K	J428-34	1B2
J427- A	J428- A	1B3
J427- T	J428-16	1B4
J427- 1	J428- N	1B5
J427-15	J428-/J	1B6
J425-/Y	J425-33	1CB1
J425-33	J426-/S	1CB1
J425- P	J426-/J	1CB2
J425- P	J425-43	1CB2
J425- B	J426- 5	1CB3
J425- M	J426- A	1CB4
J425-30	J426-16	1CB5
J426-41	J427-/Y	1CP1
J426-26	J427-28	1CP2
J426-34	J427-31	1CP3
J426- N	J427-/L	1CP4
J426- 8	J427-/J	1CP5
J429-12	J430-16	1C1
J430-41	J432-/Y	1C2
J430- 8	J432-/A	1C3
J429- S	J430- A	1C4
J429- T	J430- N	1C5
J434-/J	J436-/E	1D
J437-28	J438- 8	1DC
J437- 1	J438- 5	1DR
J438-41	J439-/Y	1D1
J438-34	J439-/U	1D2
J436- U	J438-/J	1D3
J436- V	J438-/S	1D4
J437-/E	J438- A	1D5
J434- 8	J436-/D	1E
J518- W	J519- A	1EP
J519- A	J519-27	1EP
J420-15	J422- A	1FC
J518- L	J519- 2	1FP
J519- 2	J519-/X	1FP
J438- N	J439-/P	1G1
J438-26	J439-/S	1G2
J438-16	J439-/R	1G3
J518- A	J519- 1	1HP
J519- 1	J519-41	1HP
J534-34	J537-/D	1HS
J429-/S	J430-/S	1IC
J434-16	J436-/F	1ID
J422- 8	J423-16	1IP
J520-/U	J521-/Y	1I24
J434-34	J435-37	1J
J536-41	J537-43	1JT
J434- 5	J435-24	1K
J522- U	J524-16	1LC
J522-/J	J524-34	1LP
J522-/D	J524- 8	1LX

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J520- L	J522-30	1L24
J535- 7	J536-/J	1MPX
J522-13	J524- N	1NC
J434- A	J436- B	1ND
J420-/J	J422- 5	1NP
J520- A	J525-/W	1N24W
J524-/S	J525- U	1OB1
J524-/J	J525-29	1OB2
J524-41	J525-/Y	1OB3
J421-36	J422-/S	1O1
J420-25	J422-16	1O2
J422-26	J423-30	1O3
J422-34	J424-/Y	1O4
J421-42	J422-41	1P1
J421-27	J422- N	1P2
J422-/J	J423-40	1P3
J428-41	J429-/V	1Q
J430-34	J431-/W	1RC
J430-/J	J431- U	1RK
J520-/L	J521-34	1RP
J430- 5	J431- A	1RS
J430-26	J431-/B	1RT
J524-26	J525-17	1SB1
J524- 5	J525- A	1SB2
J524- A	J525-16	1SB3
J522- 1	J523- N	1S1
J522-18	J523-/S	1S2
J522-19	J523-41	1S3
J428-/S	J431-38	1TP
J427- 3	J428- 5	1TX
J428- 8	J429-10	1TO
J518-/L	J519- S	1UP
J519- S	J519-25	1UP
J521-/A	J523- 8	1VC
J521- A	J523- A	1VK
J518-/U	J519-/Y	1VP
J521- S	J523- 5	1VS

From Receptacle and Terminal No.	To Receptacle and Terminal No.	Function
J439- E	J440- A	1V11
J439- F	J440- 5	1V12
J439- 7	J440- 8	1V13
J536-26	J537-17	1V14
J536- A	J537- D	1V15
J536- 5	J537- C	1V16
J536- 8	J537-11	1V17
J536- N	J537-13	1V18
J439-13	J440-26	1V21
J439-12	J440-16	1V22
J439- L	J440- N	1V23
J537-16	J538-/S	1V24
J537- E	J538-16	1V25
J537- F	J538-26	1V26
J537-/I	J538-34	1V27
J537-/U	J538-41	1V28
J439- X	J440-/J	1V31
J439- Z	J440-34	1V32
J439-23	J440-/S	1V33
J537-15	J538- A	1V34
J537-/V	J538- 5	1V35
J537-/W	J538- 8	1V36
J537-/Y	J538- N	1V37
J537-/X	J538-/J	1V38
J523-26	J525-43	1WA
J523-16	J525-/X	1WB
J413-43	J414-/U	1WC0
J413-41	J414-/L	1WC1
J413-/F	J414- L	1WH0
J413-/X	J414- W	1WH1
J521-26	J523-/J	1Z1
J521-30	J523-34	1Z2
J2 -19	J541-/B	20VAC
J541-/B	J542-/B	20VAC
J542-/B	J543-/B	20VAC
P204- 4	J2 -44	28VAC A
J2 -35	J418- 2	28VAC A_S

D17B COMPUTER

LOGIC EQUATIONS

Term	Equation	Receptacle	Pin No.	Definition
$_1A_C$ =		J437	$\overline{Y}$	A_C controls recirculation of A register. Any time A register is to be modified, A_C is one-set.
	$C_2' [T_O^{T_{OA}}]$		33 4	Full word or right-half word shift
	$+ C_1 [T_O^{T_{OA}}]$		30 4	Right-half word shift only
	$[K E O_4' O_3' O_2' O_1'^{O_Y}] [C_5' C_4'^{C_{UO}}]$		$\overline{T}$ 29	
	$+ C_1'' [B_6 B_3' T_P'^{T_{13}}]$		$\overline{U}$ 40	Left-half word shift only
	$[K E O_4 O_3' O_2' O_1'^{O_X}] C_4' C_2'$		18 34 33	Discrete Input A (DIA) or Discrete Input B (DIB)
	$+ C_{B3} [K E O_4' O_3' O_1'^{O_L}] N_C'$		32 L 39	Word 2 of Execute during Split Compare and Limit (SCI) when right half of A register exceeds limit
	$+ C_5 Q' [K E O_4' O_3' O_2' O_1'^{O_Y}]$		E 31 $\overline{T}$	Word 1 of Execute during Character Output A (COA) is used to extend A register by four bits
	$+ ([K' J'^{N_{PC}}] V_C R_C' C_{P5} C_{P4}) (C_{P3} C_{P2}' C_{P1}^{C_{PL5}})$		35 36	Enters Process mode when Enter code is activated during Load
	$+ \{ [K E O_4 O_3' O_2' O_1'^{O_F}] \}^{T_{OA}}[T_O]$		4	
	$+ ([K E] O_4 O_3' O_2' O_1^{O_F})$		37	Clear and Add (CLA)
	$+ [K N_C O_4' O_3^{O_{MF}}]$		$\overline{R}$	Word 1 of Execute during Multiply is used to interrupt recirculation
	$+ ([K E] O_4 O_3^{O_A}) B_3$		42 41	Full/split word of Add or Subtract

Term	Equation	Receptacle	Pin No.	Definition
$_1A_C$	(CONT)	J437	$\overline{Y}$	
	$+\left([K\,E\,O_4O_3{}'O_2{}'O_1{}']\,[C_5\,C_4{}']\right)\,[C_3{}'C_2C_1]\,[A_X]\,[T_P{}'T_X{}'T_O{}']$		$\overline{P}\,\overline{M}\,38\,\overline{N}$	Complement A register when the first one appears
	$+C_{B1}\,[K\,E\,O_4{}'O_3{}'O_1]\,N_C{}'\,[B_6B_3{}'T_P{}']$		$\overline{S}$ L 39 40	Word 2 of Execute during SCL when left-half word of A register exceeds limit
$_0A_C$ *			43	Zero-sets A_C after modifying A register
	$[D_{TP}{}']$		$\overline{W}$	True at last bit time of Execute
	$+\left\{\begin{matrix}C_2\\ \\ +C_1{}'\end{matrix}\right\}\,[K\,E\,O_4{}'O_3{}'O_2{}'O_1{}']\,C_5{}'\,[B_5B_4{}'B_3B_2]$		15	Right-half word shift only
			$\overline{T}$ 17 $\overline{V}$	
			$\overline{U}$	Both halves word shift
	$+\left([K\,E]\,O_4O_3\right)O_1{}'\,\left(B_3{}'B_2\right)$		42 $\overline{X}$ 12	Split Add or Subtract
	$+[K\,E\,O_4{}'O_3{}'O_1]\,\left(B_3{}'B_2\right)$		L 12	Effective during SCL if right-half word was replaced
	$+[K\,E\,O_4{}'O_3{}'O_2{}'O_1{}']\,[B_5{}'B_4{}'B_2B_1{}']$		$\overline{T}$ 20	Starts recirculation during Y special
$_1A_K$ *			27	A_K is carry/borrow for Add/Subtract, extension of A register for shifts, increase I register for Enter, indicates polarity of A register during SCL, and indicates left-half or right-half word for voltage outputs.

Term	Equation	Receptacle	Pin No.	Definition
$_1A_K$	(CONT)	J-437	27	
	$\left\{\begin{matrix} O_2' A_P \\ \\ \\ + O_2 A_P' \end{matrix}\right\} ([K E] \overset{O_A}{O_4 O_3}) A_C N_P$		H A	Initiates a carry during Add
			42 N 3	
			C B	Initiates a borrow during Subtract
	$+ [K E O_4' O_3' O_1] C_{B4} [\overset{O_L}{\underset{T_{OA}}{T_O}}]$		L K 4	One-sets A_K when right-half word of A is negative during SCL
	$+ [K E O_4' O_3' O_1] J (B_6 B_3' \overset{O_L}{\underset{T_{13}}{T_P}}]$		L M 40	One-sets A_K when left-half word of A is negative during SCL
	$+ \left([K E O_4 O_3' O_2' O_1'] [C_5' C_4']\right) \left(\overset{O_{XUO}}{\underset{T_{16}}{[B_6 B_5 B_4]}} [B_2 B_1']\right)$		26 25	One-sets A_K during Binary Output A (BOA), Binary Output B (BOB), or Binary output C (BOC) to Add to or Subtract from A
	$+ \left([K E O_4' O_3' O_2' O_1'] A_C\right) [\overset{O_{YAC}}{\underset{A_{XA}}{A_X}}]$		24 38	Left shifts when A_K extends A register by one bit
	$+ [K' V_C] E.D' [\overset{N_L}{\underset{T_{OA}}{T_O}}]$		10 5 2 4	Augments I register by one when Enter code is activated during Load
	$+ \left\{\begin{matrix} \overset{T_4}{I_X ([B_6' B_5'] [B_2 B_1'])} \\ \\ \\ \\ + A_K' [B_6 B_3' \overset{T_{13}}{T_P'}] \end{matrix}\right\} [K E O_4 O_3' O_2' O_1'] \overset{O_X}{\underset{C_{UI}}{[C_5' C_4]}} C_3$		$\overline{H}$ 22	Copies right-half word (eight most significant bits) into voltage output register
			18 X Z	
			23 40	Copies left-half word (eight most significant bits) into voltage output register

Term	Equation	Receptacle	Pin No.	Definition
$_1A_K$	(CONT)	J437	27	
	$\left\{\begin{matrix} A_{XA} \\ [A_X]\ C_5\ O_2' \end{matrix}\right\} \overset{O_M}{([K\ E]\ O_4'O_3)}\ C_4J'$		38 E H	Initiates a carry during addition time of Multiply
	$+\left\{\begin{matrix} A_{XA}' \\ +[A_X']\ C_5O_2 \end{matrix}\right\}$		13 P D	
			F E C	Initiates a borrow during subtraction time of Multiply
$_0A_K$	=		T	A_K is carry/borrow for Add/Subtract, extension of A register for shifts, increase I register for Enter, indicates polarity of A register during SCL, and indicates left-half or right-half word for voltage outputs.
	$\left\{\begin{matrix} O_2'\ A_P' \\ \\ \\ +\ O_2\ A_P \end{matrix}\right\} \overset{O_A}{([K\ E]\ O_4\ O_3)}\ A_C N_P'$		H B	Turns off carry during addition
			42 N R	
			C A	Turns off borrow during subtraction
	$\left\{\begin{matrix} K' \\ +\ O_4 \\ \\ \\ +\ O_3' \end{matrix}\right\} \overset{T_{XA}}{[T_X]}$		$\overline{B}$	Effective during Noncompute; initializes A_K
			$\overline{C}$	Effective during execution of most one-word instructions; initializes A_K
			W	
			$\overline{D}$	Initiates a zero into least significant bit of left shifts
	$\overset{O_L}{\rightarrow} [K\ E\ O_4'O_3'O_1]\ \overset{T_{12}}{(B_3'B_2)}$		L 12	Zero-sets A_K if right-half word of A register is negative during SCL

Term	Equation	Receptacle	Pin No.	Definition
$_0A_K$	(CONT)	J437	T	
	$\left\{\begin{matrix} A_{XA}' \\ C_2' [A_X'] \\ \\ \\ + C_2 [A_X] \end{matrix}\right\} \overset{O_{XUO}}{([K E O_4 O_3' O_2' O_1'] [C_5' C_4'])} B_5'$		33 F	Turns off A_K during binary outputs when first zero appears while adding
			26 V	
			15 38	Turns off A_K during binary outputs when first one appears while subtracting
	$+ \left([K E O_4' O_3' O_2' O_1'] \overset{O_{YAC}}{A_C}\right) A_{XA}' [A_X']$		24 F	Left shifts when A_K extends A register by one bit
	$+ [K' \overset{N_L}{V_C}] L_X' T_O'$		10 9 11	Turns off A_K when first zero appears from L_X when augmenting I register by one during Load mode
	$\left\{\begin{matrix} A_{XA}' \\ [A_X'] C_5' O_2' \\ \\ \\ + [A_X] C_5' O_2 \end{matrix}\right\} \overset{O_M}{([K E] O_4' O_3)} C_4$		F 17 H	Turns off the carry during addition time at Multiply
			13 P	
			38 17 C	Turns off the borrow during subtraction time of Multiply
	$\left\{\begin{matrix} \overset{O_A}{([K E] O_4 O_3)} \\ \\ + [K E O_4 O_3' O_2' O_1'] \overset{O_X}{[C_5' C_4]} \overset{C_{UI}}{C_3} A_K \\ \\ \\ + \\ \\ \\ + [K E O_4' O_3' O_2' O_1'] \overset{O_Y}{C_5'} A_C' \end{matrix}\right\} O_1' [B_6 B_3' \overset{T_{13}}{T_P'}]$		42	Ensures that no carry is present at beginning of Split Add/ Subtract for left-half words
			18 X Z 16	Turns A_K off, if A_K was on for right-half word during Voltage Output A (VOA), Voltage Output B (VOB), or Voltage Output C (VOC)
			U 40	
			$\overline{T}$ 17 $\overline{A}$	Inserts a zero into left-half word of left shifts

Term	Equation	Receptacle	Pin No.	Definition
$_0A_K$	(CONT)	J437	T	
	$+ J\left([K\,E]\ O_4'O_3\right)^{O_M}$		M 13	Initializes carry/borrow during multiplication (T_1 and/or T_{14})
$_1A_P$ =		J433	$\bar{F}$	A_P is delay flip-flop of A register and input buffer for inserting new values into A register
	$\left([K\,E\,O_4'O_3'O_2'O_1']\ A_C\right) A_K\,C_5'C_3'^{O_{YAC}}$		B 43 W V	Left shifts only of A register. A_K is inserted into A register
	$+ [T_O]^{T_{OA}}$		1	Automatic Gain Control (AGC)
	$+ K'\,A_C\,L_X$		Z 40 C	Copies L register into A register when Enter Code is activated
	$+\left\{\begin{array}{l} A_{XA}' \\ [A_X']\ A_K \\ \\ A_{XA} \\ + [A_X]\ A_K' \end{array}\right\}\left([K\,E\,O_4O_3'O_2'O_1'][C_5'C_4']\right)\ T_X'^{O_{XUO}}$		10 43	Copies A_X inversely until first zero appears (Add) or first one appears (Subtract) from A_X during BOA, BOB, or BOC
			A 29	
			L $\bar{T}$	Directs copy during BOA, BOB, or BOC
	$+\left\{\begin{array}{l} C_{L1}\quad A_{XA} \\ [C_3'C_2'C_1]\ [A_X]\ L_X \\ C_{L3}\quad A_{XA} \\ + [C_3'\ C_2C_1]\ [A_X]\ A_C \\ \\ + C_3\,B_1\,J \\ + C_3\,B_1'\,C_2 \end{array}\right\}\left([K\,E\,O_4\,O_3'\,O_2'\,O_1'][C_5\,C_4']\right)\ T_X'^{O_{XU2}}$		3 L C	Logical AND. If a one is in L and A registers, put a one into A register
			4 10 40	Copies A_X inversely during Complement (COM) after first one appears
			7 29	
			J D 6	Inserts the state of odd-numbered discrete input lines into A register
			J 8 F	Inserts the state of even-numbered discrete input lines into A register

Term	Equation	Receptacle	Pin No.	Definition
$_1A_P$	(CONT)	J433	$\overline{F}$	
	$\left\{ \begin{array}{l} A_C \\ \overset{K_E}{+ [K\,E]\, O_3} \\ + \left\{ \begin{array}{l} \\ \overset{O_{YRS}}{+ \left([K\,E\,O_4'\,O_3'\,O_2'\,O_1']\, C_5'\, C_3\right)} \end{array} \right. \end{array} \right\} \overset{A_{XA}}{[A_X]}\ T_X'$		28	Normal recirculation
			24 26	Copies A_X into A_P during Add or Subtract
			L 29	
			25	Right shifts so sign of A register may be spread
	$+ \left([K\,E\,O_4'\,O_3'\,O_2'\,O_1']\, C_5\, A_C\right) \overset{O_{YST}}{C_1}$		27 23	COA, C_4, C_3, C_2, and C_1 extend A register by four bits during word 1 of Execute
$_0A_P$ =			15	Same as definition for $_1A_P$
	$\left([K\,E\,O_4'\,O_3'\,O_2'\,O_1']\, A_C\right) A_K'\, C_5'\, C_3' \overset{O_{YAC}}{}$		B $\overline{T}$ W V	Left shifts only of A register when A_K is inserted into A register
	$+ [T_X] \overset{T_{XA}}{}$		2	AGC
	$+ K'\, A_C\, L_X'$		2 40 9	Copies L register into A register when Enter code is activated
	$\left\{ \begin{array}{l} A_{XA}' \\ [A_X']\, A_K' \\ \\ \\ \overset{A_{XA}}{+ [A_X]\, A_K} \end{array} \right\} \left([K\,E\,O_4\,O_3'\,O_2'\,O_1']\, [C_5'\, C_4']\right) \overset{O_{XUO}}{T_O'}$		10 $\overline{T}$	Copies A_X inversely until first zero appears (Add) or first one appears (Subtract) during BOA, BOB, and BOC
			A 16	
			L 43	Directs copy during BOA, BOB, or BOC

Term	Equation	Receptacle	Pin No.	Definition
0^{A_P}	(CONT)	J433	15	
	$\{ [C_3' C_2' C_1^{C_{L1}}] [A_X'^{A_{XA}}]$		3 10	Logical AND. If a zero is in A register, put zero into A register
	$+ [C_3' C_2' C_1^{C_{L1}}] L_X'$		3 9	Logical AND. If a zero is in I register, put zero into A register
	$+ [C_3' C_2 C_1^{C_{L3}}] [A_X^{A_{XA}}] A_C$		4 L 40	Copies A_X inversely during COM after first one appears
	$+ ([K E O_4 O_3' O_2' O_1'] [C_5 C_4'])^{O_{XU2}} T_O' \}$		7 16	
	$+ C_3 B_1 J'$		J D K	Inserts the state of odd-numbered discrete input lines into A register
	$+ C_3 B_1' C_2'$		J 8 H	Inserts the state of even-numbered discrete input lines into A register
	$\{ A_C'$		28	Normal recirculation
	$+ [K E]^{K_E} O_3$		24 26	Copies A_X into A_P during Add or Subtract
	$+ ([K E O_4' O_3' O_2' O_1'] C_5' C_3)^{O_{YRS}} \}$		10 16	
	$[A_X'^{A_{XA}}] T_O'$		25	Right shifts so sign may be spread
	$+ ([K E O_4' O_3' O_2' O_1'] C_5 A)^{O_{YST}} C_1'$		27 22	COA, C_4, C_3, C_2, and C_1 extend A register by four bits during word 1 of Execute

Term	Equation	Receptacle	Pin No.	Definition
$1^{A_{24}}$ =		J433	W	A_{24} is delay flip-flop for A, sum flip-flop for Add/Subtract, and input buffer for inserting new values into A register
	$A_P' N_P' A_K'$		41 42 43	Add/Subtract a zero and zero with a carry/borrow
	$+ A_P' N_P A_K'$		41 38 $\overline{T}$	Add/Subtract a zero and one without a carry/borrow
	$\left.\begin{array}{l} \\ \\ \end{array}\right\} \left([K E] O_4 O_3\right)^{O_A} A_C$		$\overline{V}$ 40	Add/Subtract
	$+ A_P N_P' A_K'$		$\overline{S}$ 42 $\overline{T}$	Add/Subtract a one and zero without a carry/borrow
	$+ A_P N_P A_K$		$\overline{S}$ 38 43	Add/Subtract a one and one with a carry/borrow
	K'		Z	Recirculation during Noncompute
	$+ A_C'$		28	Recirculation
	$+ [K E O_4 O_3' O_2' O_1']^{O_X}$		$\overline{A}$	Copies A_P into A_{24} during X specials
+	$\left.\begin{array}{l} \\ \\ \end{array}\right\} A_P$		$\overline{S}$	
	$+ [K E O_4' O_3' O_2' O_1'] C_5' C_3'^{O_Y}$		X W V	Copies A_P into A_{24} during left shifts
	$+ \left([K E O_4' O_3' O_2' O_1'] C_5 A_C\right)^{O_{YST}}$		27	Copies A_P into A_{24} during COA, word 1, of Execute
	$+ \left([K E] O_4 O_3' O_2' O_1\right)^{O_F} N_P$		37 38	Copies N_P into A register during CLA
	$+ \left([K E O_4' O_3' O_1] A_C\right)^{O_{LC}} N_P A_K'$		$\overline{U}$ 38 $\overline{T}$	During SCL copies N_P into A register, if A register was positive and exceeded the limit
	$+ \left([K E O_4' O_3' O_1] A_C\right)^{O_{LC}} N_P' A_K$		$\overline{U}$ 42 43	During SCL, copies N_P into A register inversely, if A register was negative and exceeded the limit

Term	Equation	Receptacle	Pin No.	Definition
$_1A_{24}$	(CONT)	J433	$\overline{W}$	
	$+ \left([K N_C O_4' O_3] T_P\right) A_P' N_P \left(S_{B3}\right)$		39 41 38 $\overline{Y}$	Multiply is used to determine the sign of the product, ie: -x+ or +x- = minus product
	$+ \left([K N_C O_4' O_3] T_P\right) A_P N_P' \left(S_{B2}\right)$		39 $\overline{S}$ 42 $\overline{X}$	
	$+ \left([K E O_4' O_3' O_2' O_1'] C_5' C_3\right) A_C [A_X]$		25 40 L	Right shifts A_X into A_{24} deleting A_P from recirculation loop
$_0A_{24}$ =			$\overline{J}$	A_{24} is delay flip-flop for A, sum flip-flop for Add/Subtract, and input buffer for inserting new values into A register
	$\left\{ A_P' N_P' A_K' + A_P' N_P A_K + A_P N_P' A_K + A_P N_P A_K' \right\} \left([K E] O_4 O_3\right) A_C$		41 42 $\overline{T}$	Add/Subtract a zero and zero without a carry/borrow
			41 38 43	Add/Subtract a zero and one with a carry/borrow
			$\overline{V}$ 40	
			$\overline{S}$ 42 43	Add/Subtract a one and zero with a carry/borrow
			$\overline{S}$ 38 $\overline{T}$	Add/Subtract a one and one without a carry/borrow
	$+ \left\{ K' + A_C' + [K E O_4 O_3' O_2' O_1'] + [K E O_4' O_3' O_2' O_1'] C_5' C_3' + [K E O_4' O_3' O_2' O_1'] C_5 A_C \right\} A_P'$		Z	Recirculation during Noncompute
			28	Recirculation
			$\overline{A}$	Copies A_P into A_{24} during X specials
			41	
			X W V	Copies A_P into A_{24} during left shift
			27	Copies A_P into A_{24} during COA during word 1 of Execute

Term	Equation	Receptacle	Pin No.	Definition
$0^{A_{24}}$	(CONT)	J433	$\overline{J}$	
	$+ \left([K E] O_4 O_3' O_2' O_1\right) N_P'$ (O_F)		37 42	Copies N_P into A register during CLA
	$+ \left([K E O_4' O_3' O_1] A_C\right) N_P' A_K'$ (O_{LC})		$\overline{U}$ 42 $\overline{T}$	Copies N_P into A register during SCL, if A register was positive and exceeded the limit
	$+ \left([K E O_4' O_3' O_1] A_C\right) N_P A_K$ (O_{LC})		$\overline{U}$ 38 43	Copies N_P into A register inversely during SCL, if A register was negative and exceeded the limit
	$+ \left([K E O_4' O_3' O_2' O_1'] C_5' C_3\right) A_C[A_X']$ (O_{YRS}, A_{XA}')		25 40 10	Right shifts A_X into A_{24}, deleting A_P from recirculation loop
	$+\{ C_5'[A_X'] A_K'$ (A_{XA}')	J537	$\overline{N}$	
			2 L X	H_S' indicates product of previous bits is 0. This insures the product is +0.
	$+ C_5'[A_X] A_K$ (A_{XA})		2 6 M	
	$+ C_5[A_X'] A_K$ (A_{XA}')		S L M	Used during last word of Multiply
	$+ C_5[A_X] A_K'$ (A_{XA})		$\overline{L}\,\overline{K}\,\overline{J}$	
	$+ C_4'[A_X']\}$ (A_{XA}') $[K Q O_4' O_3][D' T_P] H_S'$ (O_{MC}, D_{TP}')		S 6 X	
			25 L	
$1^{A_{23}}$ =		J413	2	A_{23} is write amplifier for A register, product flip-flop for Multiply, and inserts round-off pulses.
	$\{ A_C' + O_4 + O_3' + K' \} A_{24}$		N	Compute
			A	One word instructions
			1	Copies A_{24} into A_{23}
			M	One word instructions and Y specials
			B	Noncompute

Term	Equation	Receptacle	Pin No.	Definition
$_1A_{23}$	(CONT)	J413	2	
	$+\left\{\begin{matrix} C_4' C_3 \\ + C_{B5} D \end{matrix}\right\} {}^{O_{MO}}[K Q O_4' O_3] A_X$		C 9	Rules 1 and 5 during words 2 through 13 of Execute
			8 23	Multiply
			K D	T_X, T_O, and T_1 during word 2 of Execute for recirculation of round-off pulses
	$+\left\{\begin{matrix} C_5' A_X' A_K \\ + C_5' A_X A_K' \\ + C_5 A_X' A_K' \\ + C_5 A_X A_K \end{matrix}\right\} {}^{O_{MO}}[K Q O_4' O_3] {}^{M_C}(C_4 C_3 A_C)$		$\bar{B}$ P W	Add/Subtract logic for rules 1, 2, 4, 5, 6, and 8
			$\bar{B}$ 23 $\bar{C}$	Add/Subtract logic for rules 1, 2, 4, 5, 6, and 8
			8 Y	Multiplication during words 2 through 13 of Execute
			V P $\bar{C}$	Add/Subtract logic for rules 1, 2, 4, 5, 6, and 8
			V 23 W	Add/Subtract logic for rules 1, 2, 4, 5, 6, and 8
	$+\left\{\begin{matrix} {}^{T_1}O_1 ([B_6' B_5' B_3] B_4') \\ + O_1' {}^{T_2}([B_6' B_5' B_3] [B_2' B_1']) \\ + O_1' {}^{T_{14}}([B_6 B_5 B_4] B_2') \end{matrix}\right\} {}^{O_{MF}}[K N_C O_4' O_3]$		3 5	Inserts full word round-off pulse
			J E	Inserts right-half split word round-off pulse
			4	Multiply
			J F	Inserts left-half split word round-off pulse
$_0A_{23}$ =			13	A_{23} is write amplifier for A register, product flip-flop for Multiply, and inserts round-off pulses.
	$\left\{\begin{matrix} A_C' \\ + O_4 \\ + O_3' \\ + K' \end{matrix}\right\} A_{24}'$		N	Compute
			A	One word instructions
			L	Copies A_{24} into A_{23}
			M	One word instructions and Y specials
			B	Noncompute

Term	Equation	Receptacle	Pin No.	Definition
$_0A_{23}$	(CONT)	J413	13	
	$+\left\{\begin{matrix} C_4' C_3 \\ \\ + C_{B5} D \end{matrix}\right\} {}^{O_{MO}}[K Q O_4' O_3] A_X'$		C 9	Rules 1 and 5 during words 2 through 13 of Execute
			8 P	Multiply
			K D	T_X, T_O, and T_1 during word 2 of Execute for recirculation of round-off pulses
	$+\left\{\begin{matrix} C_5' A_X' A_K' \\ + C_5' A_X A_K \\ \\ + C_5 A_X' A_K \\ + C_5 A_X A_K' \end{matrix}\right\} {}^{O_{MO}}[K Q O_4' O_3] \; {}^{M_C} C_4 C_3 A_C$		$\overline{B}$ P $\overline{C}$	Add/Subtract logic for rules 1, 2, 4, 5, 6, and 8
			$\overline{B}$ 23 W	Add/Subtract logic for rules 1, 2, 4, 5, 6, and 8
			8 Y	Multiply
			V P W	Add/Subtract logic for rules 1, 2, 4, 5, 6, and 8
			V 23 $\overline{C}$	Add/Subtract logic for rules 1, 2, 4, 5, 6, and 8
			13	
	$+\left\{\begin{matrix} {}^{T_2} O_1 \left([B_6' B_5' B_3] [B_2' B_1']\right) \\ + B_2 \\ \\ + O_1' \left([B_6' B_5' B_3] B_4'\right) \end{matrix}\right\} {}^{O_{MF}}[K N_C O_4' O_3]$		3 E	Zeros A register after insertion of round-off pulse for full word
			6	Zeros A register after insertion of round-off pulse for both split words
			4	Multiply
			J 5	Zeros A register before inserting round-off pulse for right-half split word
$_1B_6$ =		J427	15	
	$^{T_{12}}(B_3' B_2) \; T_P'$		J 8	Bit counter logic
$_0B_6$ =			17	
	T_P		5	Zero-sets B_6 during normal operation and during synchronization

Term	Equation	Receptacle	Pin No.	Definition
$_1B_5$ =		J427	1	B_5 is used as a bit counter flip-flop
	$\left([B_6' B_5'] B_4 [B_2' B_1]\right)^{T_5} T_P'$		7 8	Bit counter logic
$_0B_5$ =			13	B_5 is used as a bit counter flip-flop
	$\left([B_6 B_5 B_4] [B_2 B_1']\right)^{T_{16}}$		L	Bit counter logic
	$+ T_P$		5	Zero-sets bit counters (B flip-flops) during synchronization
$_1B_4$ =			T	B_4 is used as a bit counter flip-flop
	$\left([B_6' B_5' B_3] B_4'\right)^{T_1} T_P'$		9 8	Bit counter logic
	$+ [B_6 B_3' T_P']^{T_{13}}$		H	Bit counter logic
$_0B_4$ =			11	B_4 is used as a bit counter flip-flop
	$\left(B_6' B_5 B_4\right)^{B_{LU3}} [B_2 B_1']^{B_{L2}}$		P D	Bit counter logic for T_8
	$+ \left([B_6 B_5' B_4] [B_2 B_1']\right)^{T_{20}}$		M	Bit counter logic
	$+ T_P$		5	Zero-sets B flip-flops during synchronization
$_1B_3$ =			A	B_3 is used as a bit counter flip-flop
	$B_2' T_P' T_X'$		6 8 F	Effective at T_0 and T_{13}

Term	Equation	Receptacle	Pin No.	Definition
$_0B_3$ =		J427	C	B_3 is used as a bit counter flip-flop
	T_{11} $[B_5 B_4' B_3 B_2]$		4	Bit counter logic
	+ $[B_5' B_4' B_2 B_1']$ T_{24}		10	Bit counter logic
	+ T_P		5	Zero-sets B flip-flops during synchronization
$_1B_2$ =			$\bar{K}$	B_2 is used as a bit counter flip-flop
	$[B_2' B_1']$ B_{LO} $[T_P' T_X' T_O']$ T_{PXO}'		25 24	T_2, T_6, T_{10}, T_{14}, T_{18}, T_{22}
$_0B_2$ =			B	B_2 is used as a bit counter flip-flop
	$[B_2 B_1']$ B_{L2}		D	T_4, T_8, T_{12}, T_{16}, T_{20}, T_{24}
	+ T_P		5	Zero-sets B flip-flops during synchronization
$_1B_1$ =			S	B_1 is used as a bit counter flip-flop
	B_1'		23	Even bit times
$_0B_1$ =			16	B_1 is used as a bit counter flip-flop
	$B_1 T_P'$		K 8	Odd bit times
$_1C_{B5}$ =		J425	30	C_{B5} is an operand channel buffer flip-flop and a word counter for multiword instructions
	$I_P (D' B_5 B_4')$ C_{BLT}		$\bar{H}$ C	Loads new operand channel information into C_B flip-flops at T_9 through T_{13} of D' mode

Term	Equation	Receptacle	Pin No.	Definition
$_1C_{B5}$	(CONT)	J425	30	
	$+\left([O_3' O_1'] D N_D' [B_6' B_5' B_3]\right) L_X^{C_{BST}}$		D 27	Loads counter in I register into C_B flip-flops for multiword instructions and word 1 of Execute during T_1 through T_5
	$+\left([K N_C O_4' O_3] T_P\right)^{O_{MFP}}$		6	During word 1 of Multiply for recirculation of round-off pulses, (See A_{23} logic)
$_0C_{B5}$ *			24	C_{B5} is an operand channel buffer flip-flop and a word counter for multiword instructions
	$I_P' \left(D' B_5 B_4'\right)^{C_{BLT}}$		25 C	Loads new operand channel information into C_B flip-flops
	$+\left([K E] O_4' O_3\right)^{O_M} \left([B_6' B_5' B_3] B_4'\right)^{T_1}$		21 22	Zero-sets C_{B5} after round-off pulses (Multiply) are recirculated
	$+\left([O_3' O_1'] D N_D' [B_6' B_5' B_3]\right) L_X'^{C_{BST}}$		D Y	Loads counter in I register into C_B flip-flops during T_1 through T_5
	$+C_{B4}' \left(C_{B3}' C_{B2}' C_{B1}'\right)^{C_{BLO}} \left(N_D [D T_P]\right)^{E_{OP}}$		N T H	Countdown logic for multiword instructions
$_1C_{B4}$ *			M	C_{B4} is an operand channel buffer flip-flop word counter for multiword instructions, and holds sign of right-half word of A register during SCL
	$C_{B5} \left(D' B_5 B_4'\right)^{C_{BLT}}$		2 C	Loads new operand channel information into C_B flip-flops at T_9 through T_{13} of D' mode
	$+\left\{ O_{B1} \left([B_6 B_5 B_4] B_2'\right)^{T_{14}} C_{B3} \cdot \right.$		42 37 9	Eight-word disagreement
	$\left. + C_{B11}' S_{B1} \left([B_6 B_5 B_4] B_2'\right)^{T_{14}} C_{B3} \right\} D' C_{B4}' C_{B2}$		$\overline{S}$ N K	Eight-word disagreement; changes operand channel from 54 to 74 (16 words) or 56 to 76 (8 words)
			$\overline{N}$ 38 37 9	Sixteen-word disagreement

Term	Equation	Receptacle	Pin No.	Definition
$_1C_{B4}$	(CONT)	J425	M	
	$+ \left([O_3' O_1'] D N_D' [B_6' B_5' B_3']\right) C_{BST} C_{B5}$		D 2	Loads counter into C_B flip-flops for multiword instructions during word 1 of Execute during T_1 through T_5
	$+ C_{B4}' \left(C_{B3}' C_{B2}' C_{B1}'\right) \left(N_D [D T_P]\right) C_{BLO} E_{OP}$		N T H	Countdown logic for multiword instructions
	$+ \left([K E O_4' O_3' O_1] N_C\right) A_{24} [B_6 B_3' T_P'] O_{LF} T_{13}$		4 J L	Monitors A register during SCL, word 1, for polarity of right-half word
	$+ \left([K N_C O_4' O_3] T_P\right) O_1 O_{MFP}$		6 1	During Multiply, inserts the number (14_8) into C_B flip-flops during word 1 of Execute
$_0C_{B4}$ =			A	C_{B4} is an operand channel buffer flip-flop word counter for multiword instructions, and holds sign of right-half word of A register during SCL
	$C_{B5}' \left(D' B_5 B_4'\right) C_{BLT}$		8 C	Loads new operand channel information into C_B flip-flops at T_9 through T_{13} during D' mode
	$+ \left([O_3' O_1'] D N_D' [B_6' B_5' B_3']\right) C_{BST} C_{B5}'$		D 8	Loads counter into C_B flip-flops for multiword instructions during word 1 of Execute
	$+ C_{B4} \left(C_{B3}' C_{B2}' C_{B1}'\right) \left(N_D [D T_P]\right) C_{BLO} E_{OP}$		3 T H	Countdown logic for multiword instructions
	$+ \left([K E O_4' O_3' O_1] N_C\right) [B_5 B_4' B_3 B_2] O_{LF} T_{11}$		4 5	Initializes C_{B4} prior to check of the sign of right-half word during SCL, word 1
	$+ \left([K N_C O_4 O_3] T_P\right) O_1' O_{MFP}$		6 7	Inserts count of 6_8 into C_B flip-flops for Split Multiply (SMP) during word 1 of Execute

Term	Equation	Receptacle	Pin No.	Definition
$_1C_{B3}$ =		J425	B	C_{B3} is an operand channel buffer flip-flop word counter for multiword instructions and indicates if right-half word of A register exceeds memory contents
	$C_{B4}\,(D'\,B_5\,B_4')^{C_{BLT}}$		3 C	Loads new operand channel information into C_B flip-flops at T_9 through T_{13} during D' mode
	$+\,([K]_A IP'\,O_{B3}\,O_{B2}[D'\,T_P])^{O_{BSM}}\,C_{B3}'\,P_3\,F_C'$		W $\bar{W}$ 19 18	Modifies operand channel address as per phase register for Multiply modified (full or split)
	$+\,([O_3'\,O_1']\,D\,N_D'[B_6'\,B_5'\,B_3])^{C_{BST}}\,C_{B4}$		D 3	Loads counter into C_B flip-flops for multiword instructions during word 1 of Execute
	$+\,(C_{B3}'\,C_{B2}'\,C_{B1})^{C_{BLO}}\,(N_D[D\,T_P])^{E_{OP}}$		T H	Countdown logic for multiword instructions
	$+\,([K\,E\,O_4'\,O_3'\,O_1]\,N_C)^{O_{LF}}\,C_{B2}\,C_{B1}[B_6\,B_3'\,T_P']^{T_{13}}$		4 K 28 L	During SCL, right-half word of A register exceeds memory contents
	$+\,([K\,N_C\,O_4'\,O_3]\,T_P)^{O_{MFP}}$		6	Inserts third bit of counter into C_B flip-flops for Multiply (14_8 = 01100) or for SMP (6_8 = 00110_2)
$_0C_{B3}$ =			15	C_{B3} is an operand channel buffer flip-flop word counter for multiword instructions and indicates if right-half word of A register exceeds memory contents
	$C_{B4}'\,(D'\,B_5\,B_4')^{C_{BLT}}$		N C	Loads new operand channel information into C_B flip-flops at T_9 through T_{13} during D' mode
	$+\,([K]_A I_P'\,O_{B3}\,O_{B2}[D'\,T_P])^{O_{BSM}}\,C_{B3}\,P_3\,F_C'$		W 9 19 18	Modifies operand channel address as per phase register for Multiply modified (full or split)
	$+\,([O_3'\,O_1']\,D\,N_D'[B_6'\,B_5'\,B_3])^{C_{BST}}\,C_{B4}'$		D N	Loads counter into C_B flip-flops for multiword instructions during word 1 of Execute

Term	Equation	Receptacle	Pin No.	Definition
$_0C_{B3}$	(CONT)	J425	15	
	$+ C_{B3}(C_{B2}' C_{B1})(N_D[D\ T_P])^{C_{B21}'\ E_{OP}\ KE}[K\ E]$		9 16 H Z	Countdown logic for multiword instructions
	$+ ([K\ E\ O_4' O_3' O_1] N_C)^{O_{LF}\ T_{11}}[B_5 B_4' B_3 B_2]$		4 5	During SCL, initializes C_{B3} to zero state prior to T_{13} during word 1 of Execute
$_1C_{B2}$ =			P, 43	C_{B2} is an operand channel buffer flip-flop, word counter for multiword instructions, and compares A register and memory with C_{B1} for magnitude during SCL.
	$C_{B3}(D' B_5 B_4')^{C_{BLT}}$		9 C	Loads new operand channel information into C_B flip-flops at T_9 through T_{13} during D' mode
	$+ ([K]_A I_P' O_{B3} O_{B2}[D' T_P])^{O_{BSM}} P_2 C_{B2}'$		W 39 $\bar{D}$	Modifies operand channel address as per phase register for Multiply modified (full or split)
	$+ ([O_3' O_1'] D N_D'[B_6' B_5' B_3])^{C_{BST}} C_{B3}$		D 9	Loads counter into C_B flip-flops for multiword instructions during word 1 of Execute
	$+ (C_{B2}' C_{B1}')(N_D[D\ T_P])^{C_{B21}'\ E_{OP}\ K_E}[K\ E]$		16 H Z	Countdown logic for multiword instructions
	$+ ([K\ E\ O_4' O_3' O_1] N_C)^{O_{LF}} N_P' A_P$		4 F E	During SCL, used in conjunction with C_{B1} to determine if A register is greater than memory during word 1 of Execute
	$+ ([K\ N_C O_4' O_3] T_P)^{O_{MFP}} O_1'$		6 7	During SMP, inserts second least significant bit of the number ($6_8 = 00110_2$) into C_{B2} during word 1 of Execute
$_0C_{B2}$ =			40, $\overline{M}$	C_{B2} is an operand channel buffer flip-flop, word counter for multiword instructions, and compares A register and memory with C_{B1} for magnitude during SCL.
	$C_{B3}'(D' B_5 B_4')^{C_{BLT}}$		$\overline{W}$ C	Loads new operand channel information into C_B flip-flops at T_9 through T_{13} of D' mode

Term	Equation	Receptacle	Pin No.	Definition
$_0C_{B2}$	(CONT)	J425	40, $\overline{M}$	
	$+ \left([K]_A I_P' O_{B3} O_{B2} [D' T_P]\right) P_2 C_{B2}$ (O_{BSM})		W 39 K	Modifies operand channel address as per phase register for Multiply modified (full or split)
	$+ \left([O_3' O_1'] D N_D' [B_6' B_5' B_3]\right) C_{B3}'$ (C_{BST})		D $\overline{W}$	Loads counter into C_B flip-flops for multiword instructions during word 1 of Execute
	$+ C_{B2} C_{B1}' \left(N_D [D T_P]\right)$ (E_{OP})		K $\overline{N}$ H	Countdown logic for multiword instructions
	$+ \left([K E O_4' O_3' O_1] N_C\right) N_P A_P'$ (O_{LF})		4 23 $\overline{R}$	During SCL, is used in conjunction with C_{B1} to determine if A register is greater than memory during word 1 of Execute
	$+ \left([K N_C O_4' O_3] T_P\right) O_1$ (O_{MFP})		41 1	During multiply, inserts second least significant bit of the number ($14_8 = 01100_2$) into C_{B2} during word 1 of Execute
$_1C_{B1}$ =			33, Y	C_{B1} is an operand channel buffer flip-flop, word counter for multiword instructions, and compares A register and memory with C_{B2} for magnitude.
	$C_{B2} D' [B_6 B_3' T_P']$ (T_{13})		K $\overline{S}$ L	Loads new operand channel information into C_B flip-flops
	$+ \left([K]_A I_P' O_{B3} O_{B2} [D' T_P]\right) P_1 C_{B1}'$ (O_{BSM})		W $\overline{P}$ $\overline{N}$	Modifies operand channel address as per phase register for Multiply modified (full or split)
	$+ \left([O_3' O_1'] D N_D' [B_6' B_5' B_3]\right) C_{B2}$ (C_{BST})		D K	Loads counter into C_B flip-flops for multiword instructions during word 1 of Execute
	$+ C_{B1}' \left(N_D [D T_P]\right) [K E]$ (E_{OP} K_E)		$\overline{N}$ H Z	Countdown logic for multiword instructions
	$+ [K N_C O_4' O_3] O_1' B_3$ (O_{MF})		29 7 $\overline{X}$	During SMP, one sets C_{B1} to allow L_{24} to copy L_P on word 1 of Multiply; L_P, in turn, copies A_X

Term	Equation	Receptacle	Pin No.	Definition
$_1C_{B1}$	(CONT)	J425	33, Y	
	$+\left(\left[K\,E\,O_4'\,O_3'\,O_1\right]N_C\right)N_P'\,A_P'$		4 F $\bar{R}$	Used during SCL with C_{B2} to determine if A register is greater than memory during word 1 of Execute
	$+\left[K\,E\,O_4\,O_3'\,O_2'\,O_1'\right]A_{24}'\,T_X$		$\bar{U}$ $\bar{T}$ 34	During Minus Magnitude (MIM), if A register is positive, changes Operation code to COM
$_0C_{B1}$ =			31	C_{B1} is an operand channel buffer flip-flop, word counter for multiword instructions, and compares A register and memory with C_{B2} for magnitude.
	$C_{B2}'\,D'\left[B_6\,B_3'\,T_P'\right]$		$\bar{D}$ $\bar{S}$ L	Loads new operand channel information into C_B flip-flops
	$+\left(\left[K\right]_A I_P'\,O_{B3}\,O_{B2}\left[D'\,T_P\right]\right)P_1\,C_{B1}$		W $\bar{P}$ 28	Modifies operand channel address per phase register for Multiply modified (full or split)
	$+\left(\left[O_3'\,O_1'\right]D\,N_D'\left[B_6'\,B_5'\,B_3\right]\right)C_{B2}'$		D $\bar{D}$	Loads counter into C_B flip-flops for multiword instructions during word 1 of Execute
	$+C_{B1}\left(N_D\left[D\,T_P\right]\right)$		28 H	Countdown logic for multiword instructions
	$+\left[K\,N_C\,O_4'\,O_3\right]B_3'$		29 35	During SMP, resets C_{B1} for bit times not in split word during word 1 of Execute
	$+\left(\left[K\,E\,O_4'\,O_3'\,O_1\right]N_C\right)N_P\,A_P$		4 23 E	Use during SCL with C_{B2} to determine if A register is greater than memory during word 1 of Execute
	$+\left[K\,E\,O_4'\,O_3'\,O_1\right]C_{B2}'\,T_X$		26 $\bar{D}$ 34	During SCL, if left-half word of A register is less than left-half word of memory, zero-sets C_{B1} at T_X of word 2 of SCL

Term	Equation	Receptacle	Pin No.	Definition
$_1C_{P5}$ =		J427	$\bar{J}$	C_P5 is channel program flip-flop during Compute and controls flip-flop during Load.
	$C_{B5}([K\,O_4\,O_3'\,O_2\,O_1'][T_O]_A^{O_{UO}})$		$\bar{C}$ 32	Loads C_P flip-flops with new program Channel code
	$+[K'\,V_C]\,B_6'^{N_L}$		27 26	During Noncompute Load mode, one-sets C_{P5} for Process code. C_{P5} is used as a control factor for O_4
$_0C_{P5}$ =			U	C_{P5} is channel program flip-flop during Compute and controls flip-flop during Load
	$C_{B5}'([K\,O_4\,O_3'\,O_2\,O_1'][T_O]_A^{O_{UO}})$		22 32	Loads C_P flip-flops with new program Channel code
	$+([K'\,J'\,]\,V_C\,R_C)^{N_{SC}}$		$\bar{B}$	Sample Code mode of Noncompute Load mode
$_1C_{P4}$ =			$\bar{L}$	C_{P4} is channel program flip-flop during Compute and receives character input information
	$C_{B4}([K\,O_4\,O_3'\,O_2\,O_1'][T_O]_A^{O_{UO}})$		$\bar{H}$ 32	Loads C_P flip-flops with new program Channel code during unconditional Transfer
	$+([K]_A\,C_{PIR}\,C_{P5}\,C_{P3}\,C_{P2})\,O_{B2}[B_5'\,B_4'\,B_2\,B_1']^{T_{24}}$		Y $\bar{F}$ 10	Modifies program channel if 8- or 16-word disagreement occurs when program is in E loop (8 words) or H loops (16 words)
	$+([K'\,J'\,]\,V_C\,R_C)\,I_4^{*N_{SC}}$		$\bar{B}\,\bar{E}$	Inserts information into computer from an external source; (N_{SC}) = Sample mode of Noncompute during Load
	$+C_{FI}([K'\,V_C]\,O_4)\,C_{P5}'^{N_{ST}}$		$\bar{D}$ 33 $\bar{A}$	Checks parity during Load
$_0C_{P4}$ =			V	C_{P4} is channel program flip-flop during Compute and receives character input information
	$C_{B4}'([K\,O_4\,O_3'\,O_2\,O_1'][T_O]_A^{O_{UO}})$		W 32	Loads C_P flip-flops with new program Channel code during unconditional Transfer

Term	Equation	Receptacle	Pin No.	Definition
${}_0C_{P4}$ =	(CONT)	J427	V	
	$+ \left([K]_A C_{P5} C_{P3} C_{P2}\right) O_{B2}' [B_5' B_4' B_2 B_1']$		Y Z 10	Modifies program channel if 8- or 16-word agreement occurs when program is in E loop (8 words) or H loops (16 words)
	$+ \left([K' V_C] J^{N_W} R_C'\right)$		19	During Wait submode of Load mode, is used to initialize C_P register prior to sampling input lines
	$+ C_{P1}' \left([K' V_C] O_4\right)^{N_{ST}} C_{P5}'$		21 33 $\bar{A}$	Checks parity during Load
${}_1C_{P3}$ =			31	C_{P3} is channel program flop-flop during Compute and receives character input information during Load
	$C_{B3} \left([K O_4 O_3' O_2 O_1'] [T_O]_A\right)^{O_{UO}}$		$\bar{X}$ 32	Loads C_P flip-flops with new program Channel code during unconditional Transfer
	$+ \left([K' J'] V_C R_C\right)^{N_{SC}} I_3^*$		$\bar{B}$ 42	Inserts new information into computer from an external source during Sample code mode of Load
	$+ \left([K' V_C] O_4\right)^{N_{ST}} L_C' C_{P4}$		33 $\bar{W}$ $\bar{V}$	Checks parity of Load mode
	$+ \left([K' V_C] O_4\right)^{N_{ST}} L_C L_X$		33 $\bar{U}$ $\bar{T}$	Extends L register by three bits during Load mode to put new octal number into L register
${}_0C_{P3}$ =			30	C_{P3} is channel program flip-flop during Compute and receives character input information during Load
	$C_{B3}' \left([K O_4 O_3' O_2 O_1'] [T_O]_A\right)^{O_{UO}}$		$\bar{M}$ 32	Loads C_P flip-flops with new program Channel code during unconditional Transfer
	$+ \left([K' V_C] O_4\right)^{N_{ST}} L_C' C_{P4}'$		33 $\bar{W}$ 41	Checks parity of Load mode; initializes C_{P3} during Wait submode of Load mode
	$+ \left([K' V_C] O_4\right)^{N_{ST}} L_C L_X'$		33 $\bar{U}$ $\bar{P}$	Extends L register by three bits during Load mode to put new octal number into L register

Term	Equation	Receptacle	Pin No.	Definition
$_1C_{P2}$ =		J427	28	C_{P2} is a channel program flip-flop during Compute and receives character input information during Load.
	$C_{B2}([K\,O_4O_3{}'O_2O_1{}'][T_O]_A^{O_{UO}})$		40 32	Loads C_P flip-flops with new program Channel code during unconditional Transfer
	$+ [K'\,J'] V_C R_C I_2^{*N_{SC}}$		$\overline{B}$ 39	Inserts new information into computer from an external source during Sample code mode of Load
	$+ C_{P3}([K' V_C] O_4^{N_{ST}})$		$\overline{N}$ 33	Checks parity of Load mode
$_0C_{P2}$ =			29	C_{P2} is a channel program flip-flop during Compute and receives character input information during Load.
	$C_{B2}'([K\,O_4O_3{}'O_2O_1{}'][T_O]_A^{O_{UO}})$		35 32	Loads C_P flip-flops with new program Channel code during unconditional Transfer
	$+ C_{P3}'([K' V_C] O_4^{N_{ST}})$		34 33	Checks parity of Load mode; initializes C_{P2} during Wait submode of Load mode
$_1C_{P1}$ =			$\overline{Y}$	C_{P1} is channel program flip-flop during Compute and receives character input information during Load.
	$C_{B1}([K\,O_4O_3{}'O_2O_1{}'][T_O]_A^{O_{UO}})$		$\overline{S}$ 32	Load C_P flip-flops with new program Channel code during unconditional Transfer
	$+ ([K'\,J'] V_C R_C) I_1^{*N_{SC}}$		$\overline{B}$ $\overline{R}$	Inserts new information into computer from an external source during Sample code mode of Load
	$+ C_{P2}([K' V_C] O_4^{N_{ST}})$		38 33	Checks parity of Load
$_0C_{P1}$ =			43	C_{P1} is channel program flip-flop during Compute and receives character input information during Load.
	$+ C_{B1}''([K\,O_4O_3{}'O_2O_1{}'][T_O]_A^{O_{UO}})$		36 32	Loads C_P flip-flops with new program Channel code during unconditional Transfer

Term	Equation	Receptacle	Pin No.	Definition
$_0C_{P1}$	(CONT)	J427	43	
	$+ C_{P2}' ([K' V_C] O_4^{N_{ST}})$		37 33	Checks parity of Load mode; initializes C_{P1} during Wait submode of Load mode
$_1C_5$ =		J429	T	C_5 holds present operand channel information and is used as control factor during words 2 through 13 of Multiply.
	$C_{B5} [E N_D' T_X^{E_{FB}}]$		42 33	Loads C_5 with new operand information at first bit of Execute
	$+\left\{\begin{matrix} C_1' N_X \\ + C_1 N_P \end{matrix}\right\} [K Q O_4' O_3]^{O_{MO}} C_2$		25 U	Rules 1, 2, 4, 5, 6, and 8
			$\bar{P}$ 16	Multiply
			$\bar{A}$ V	Causes a one-bit shift before addition or subtraction during rules 3 and 7
$_0C_5$ =			27	C_5 holds present operand channel information and is used as control factor during words 2 through 13 of Multiply.
	$C_{B5}' [E N_D' T_X^{E_{FB}}]$		N 33	Loads C_5 with new operand information at first bit of Execute
	$+\left\{\begin{matrix} C_1' N_X' \\ + C_1 N_P' \end{matrix}\right\} [K Q O_4' O_3]^{O_{MO}} C_2$		25 $\bar{C}$	Rules 1, 2, 4, 5, 6, and 8
			$\bar{P}$ 16	Multiply
			$\bar{A}$ $\bar{B}$	Causes a one-bit shift before addition or subtraction during rules 3 and 7
	$+ [K Q O_4' O_3]^{O_{MO}} C_4' [B_6 B_3' T_P']^{T_{13}}$		$\bar{P}$ 26 30	Prevents addition or subtraction at T_{14} for SMP
$_1C_4$ =			S	C_4 holds present operand channel information, is used as output register during COA, and control factor for shift and Multiply
	$C_{B4} [E N_D' T_X^{E_{FB}}]$		M 33	Loads new operand channel information into C_4 at first bit of Execute

Term	Equation	Receptacle	Pin No.	Definition
$_1C_4$	(CONT)	J429	S	
	$+\left([K E O_4' O_3' O_2' O_1'] C_5 A_C^{O_{YST}}\right)[A_X^{A_{XA}}]$		35 H	During COA, causes four-bit left shift of A register during word 1 of COA; leaves T_{24} information in C_4 at completion of word 1
	$+[K E O_4' O_3' O_2' O_1'] C_{B5}' C_{B4}' \left(C_{B3}' C_{B2}' C_{B1}'\right) N_D T_X^{O_Y\ C_{BLO}}$		J N 4 K L P	Prevents shifting if a zero shift is coded
	$+\left\{\begin{array}{l} T_O \\ + C_1\left([B_6' B_5' B_3'] [B_2' B_1']\right)^{T_2} \\ \\ \\ + O_1' [B_6 B_3' T_P']^{T_{13}} \\ + C_1\left([B_6 B_5 B_4'] B_1\right)^{T_{15}} \end{array}\right\}[K Q O_4' O_3]^{O_{MO}}$		9	Turns on C_4, was off from the last word
			$\bar{A}$ 22	Rules 3 and 7 apply to full word and right-half word of SMP
			$\bar{P}$	During Multiply, C_4 acts as carry control
			23 30	Turns on C_4, if C_4 was off from right-half word
			$\bar{A}$ 21	Rules 3 and 7 apply to left-half word of SMP
$_0C_4$ =			A	C_4 holds present operand channel information, is used as output register during COA, and control factor for shift and Multiply
	$C_{B4}' [E N_D' T_X]^{E_{FB}}$		4 33	Loads C_4 with new operand channel information during first bit of Execute
	$+\left([K N_C O_4' O_3] T_P\right)^{O_{MFP}}$		5	During first word of Multiply, initializes C_4 prior to actual multiplication
	$+[K E O_4' O_3' O_2' O_1'] [T_P]^{T_{PB}} C_5'$		J Z 6	Initiates shift time
	$+\left\{\begin{array}{l} L_P' S_{B2}' \\ \\ \\ + L_P S_{B2} \end{array}\right\}[K Q O_4' O_3]^{O_{MO}} J$		B C	
			$\bar{P}$ 2	During Multiply, stop-carry control for rules 1, 3, 5 and 7. C_4 will be turned on again for rules 3 and 7.
			E F	

Term	Equation	Receptacle	Pin No.	Definition
$_0C_4$	(CONT)	J429	A	
	$+\left([K E O_4' O_3' O_2' O_1'] C_5 A_C\right)^{O_{YST}} [A_X']^{A_{XA}'}$		35 3	During COA, causes a four-bit left shift of A register; leaves most significant bit in C_4 at completion of word 1
$_1C_3$ =		J432	$\bar{A}$	C_3 holds present operand channel information and is used as an output register during COA and control factor during words 2 through 13 of Multiply.
	$C_{B3}[E N_D' T_X]^{E_{FB}}$		W 16	Loads new operand channel information into C_3 at first bit of Execute
	$+\left([K E O_4' O_3' O_2' O_1'] C_5 A_C\right)^{O_{YST}} C_4$		Z X	During COA, causes a four-bit left shift of A register during word 1 of Execute; leaves T_{23} information in C_3 at completion
	$+\left\{\begin{array}{l}\left([B_6 B_5 B_4] [B_2 B_1']\right)^{T_{16}} \\ +\left([B_6' B_5' B_3] [B_2' B_1']\right)^{T_2} \\ \\ +D'\left([B_6 B_5 B_4] B_1\right)^{T_{15}}\end{array}\right\} [K Q O_4' O_3]^{O_{MO}}$		T	Starts addition/subtraction for left half
			U	Starts addition/subtraction
			3	Multiply
			$\bar{C}$ 17	Starts addition/subtraction for left half of last word of Execute
$_0C_3$ =			1	C_3 holds present operand channel information and is used as an output register during COA and control factor during words 2 through 13 of Multiply.
	$C_{B3}'[E N_D' T_X]^{E_{FB}}$		5 16	Loads new operand channel information into C_3 at first bit of Execute
	$+\left([K E O_4' O_3' O_2' O_1'] C_5 A_C\right)^{O_{YST}} C_4'$		Z 6	During COA, causes a four-bit left shift of A register during word 1 of Execute; leaves T_{23} information in C_3 at completion
	$+[K Q O_4' O_3]^{O_{MO}} [T_O]^{T_{OA}}$		3 2	During Multiply, stops addition/subtraction

Term	Equation	Receptacle	Pin No.	Definition
$_0C_3$	(CONT)	J432	1	
	$+[K\,Q\,O_4'\,O_3]^{O_{MO}}\,J$		3 4	During Multiply, J is true at T_1 for full Multiply and SMP, and at T_{14} for SMP only; stops addition and addition/subtraction
$_1C_2$ =			$\overline{Y}$	C_2 holds present operand channel information, is used as an Add/Subtract indicator for binary outputs, samples discrete inputs, is an output register for COA, and is a control factor for Multiply during words 2 through 13.
$\left\{\begin{array}{l} C_1'\,G_1' \\ +C_3\,C_1\,G_2' \\ \\ \\ +C_3'\,G_3' \end{array}\right\}$	$\left([K\,E\,O_4\,O_3'\,O_2'\,O_1']\,[C_5'\,C_4']\right)^{O_{XUO}}\,[T_O]^{T_{OA}}$		$\overline{H}\,\overline{F}$	During BOA when G_1 is zero, subtracts one from A register
			$\overline{E}\,\overline{D}$ 30	During BOB when G_2 is zero, subtracts one from A register
			27 2	During binary output, C_2 acts as addition/subtraction indicator for A register
			29 28	During BOC when G_3 is zero, subtracts one from A
$+\left\{\begin{array}{l} \left([B_6'\,B_5'\,B_3]\,B_4'\right)X_2^{*\,T_1} \\ +[B_6'\,B_5']\,B_2\,B_1\,X_4^{*\,B_{SUO}} \\ +\left([B_6'\,B_5']\,B_4\,[B_2'\,B_1]\right)X_6^{*\,T_5} \\ \\ +\left(B_6'\,B_5\,B_4\right)B_1\,X_8^{*\,B_{LU3}} \\ +B_5\,B_3\,[B_2'\,B_1]\,X_{10}^{*\,B_{L1}} \\ +[B_5'\,B_4'\,B_3\,B_2]\,X_{12}^{*\,T_{11}} \end{array}\right\}$	$\left([K\,E\,O_4\,O_3'\,O_2'\,O_1'][C_5\,C_4']\right)^{O_{XU2}}\,[C_3\,C_2'\,C_1]^{C_{L5}}$		$\overline{L}$	The even-numbered DIA lines are sampled into C_2, then put into A register
			41 40 38 32	
			$\overline{N}$ 34	
			$\overline{X}\,\overline{J}$	$\left(O_4\,O_3'\,O_2'\,O_1 = 40;\ [C_5\,C_4']\ C_3 = 5;\ C_2'\,C_1' = 2\right)$ = DIA
			$\overline{M}$ 37 38	
			$\overline{V}\,\overline{U}\,\overline{T}\,\overline{K}$	
			$\overline{P}$ 36	

Term	Equation	Receptacle	Pin No.	Definition
$_1C_2$	(CONT)	J432	$\overline{Y}$	
	$\{ [B_6 B_3' T_P'] X_{14}^{T_{13}}$		N M	
	$+ ([B_6 B_5 B_4] B_1) X_{16}^{T_{15}}$		17 12	
	$+ ([B_6 B_5' B_4] [B_2' B_1]) X_{18}^{T_{17}}$		11 10	
	$+ ([K E O_4 O_3' O_2' O_1'] [C_5' C_4']) [C_3 C_2' C_1]$ O_{XU2} C_{L5}		$\overline{X}$ $\overline{J}$	$(O_4 O_3' O_2' O_1' = 40; [C_5 C_4'] C_3 = 5; C_2' C_1 = 2)$ = DIA
	$+ ([B_6 B_5' B_4] B_2 B_1) D_R^{T_{19}}$		L 9	Inserts state of D_R into A register during DIA
	$+ ([B_6 B_4' B_3] [B_2' B_1]) P_3 F_C'^{T_{21}}$		K 8 V	Inserts state of P_3 into A register during DIA
	$+ ([B_4' B_3 B_2] B_5' B_1) P_2^{T_{23}} \}$		J 7	Inserts state of P_2 into A register during DIA
	$\{ (B_6' B_5' B_3] B_4') Y_2^{*T_1}$		43 42	Inserts state of even-numbered DIB lines into C_2, then into A register
	$+ [B_6' B_5'] B_2 B_1 Y_4^{*B_{SUO}}$		41 40 38 39	
	$+ ([B_6' B_5'] B_4 [B_2' B_1]) Y_6^{*T_5}$		34 35	
	$+ ([K E O_4 O_3' O_2' O_1'] [C_5 C_4']) [C_3 C_2' C_1']$ O_{XU2} C_{L4}		$\overline{X}$ $\overline{W}$	$(O_{XU2}' = 40; [C_5 C_4'] C_3 = 5; C_2' C_1' = 0)$ = DIB
	$+ (B_6' B_5 B_4) B_1 Y_8^{*B_{LU3}}$		37 38 33	
	$+ B_5 B_3 [B_2' B_1] Y_{10}^{*B_{L1}}$		$\overline{V}$ $\overline{U}$ $\overline{T}$ $\overline{S}$	
	$+ [B_5 B_4' B_3 B_2] Y_{12}^{*T_{11}} \}$		$\overline{P}$ $\overline{R}$	

Term	Equation	Receptacle	Pin No.	Definition
$_1C_2$	(CONT)	J432	$\overline{Y}$	
	$\{ [B_6 B_6' T_P'] Y_{14}^{T_{13}}$		N B	$\}$ Inserts state of even-numbered DIB lines into C_2, then into A register
	$+ ([B_6 B_5 B_4] B_1) Y_{16}^{T_{15}}$		17 C	
	$+ ([B_6 B_5' B_4] [B_2' B_1]) Y_{18}^{T_{17}}$		11 D	
	$+ ([B_6 B_5' B_4] B_2 B_1) Y_{20}^{T_{19}}$		L E	
	$+ ([B_6 B_4' B_3] [B_2' B_1]) Y_{22}^{T_{23}}$		K F	
	$+ ([B_4' B_3 B_2] B_5' B_1) Y_{24}^{T_{23}} \}$		J H	
	$\cdot ([K E O_4 O_3' O_2' O_1'] [C_5 C_4'])^{O_{XU2}} [C_3 C_2' C_1']^{C_{L4}}$		$\overline{X}$ $\overline{W}$	$\}$ $(O_{XU2} = 40; [C_5 C_4'] C_3 = 5; C_2' C_1' = 0)$ = DIB
	$+ ([K E O_4' O_3' O_2' O_1'] C_5 A_C)^{O_{YST}} C_3$		Z $\overline{E}$	During COA, causes four-bit left shift of A register during word 1 of Execute; leaves T_{22} information in C_2
	$+ [K Q O_4' O_3]^{O_{MO}} [T_O]^{T_{OA}}$		3 Z	During Multiply, controls timing for copying N_X or N_P into C_5
	$+ [K Q O_4' O_3]^{O_{MO}} [B_6 B_3' T_P']^{T_{13}}$		3 N	During Multiply, controls timing for copying N_X or N_P into C_5
	$+ C_{B2} [E N_D' T_X]^{E_{FB}}$		A 16	Loads C_2 with new operand channel information at first bit of Execute

Term	Equation	Receptacle	Pin No.	Definition
$_0C_2$ =		J429	$\bar{D}$	C_2 holds present operand channel information, is used as an Add/Subtract indicator for binary outputs, samples discrete inputs, is an output register for COA, and is a control factor for Multiply during words 2 through 13.
	$C_{B2}' [E N_D' T_X]^{E_{FB}}$		34 33	Loads C_2 with new operand channel information at first bit of Execute
	$+ ([K E O_4 O_3' O_2' O_1'] [C_5 C_4']) C_3 B_1'^{O_{XU2}}$		15 17 18	Zero-sets C_2 to zero at even-numbered bit times for DIA and DIB in preparation for sampling lines
	$+ ([K E O_4' O_3' O_2' O_1'] C_5 \wedge_C) C_3'^{O_{YST}}$		35 36	During COA, causes a four-bit left shift of A register during word 1 of Execute; leaves T_{22} information in C_2 at completion
	$+ \left\{ \begin{array}{l} C_1' [B_5' B_4' B_2 B_1']^{T_{24}} \\ + [T_P]^{T_{PB}} \\ + O_1' C_1' [B_5 B_4' B_3 B_2]^{T_{11}} \\ + O_1' (B_3' B_2)^{T_{12}} \end{array} \right\} [K Q O_4' O_3]^{O_{MO}}$		25 24 Z $\bar{P}$ 23 25 28 23 Y	Rules 1, 2, 4, 5, 6, and 8 during full word Rules 3 and 7 During Multiply, C_2 determines the time C_5 will copy N_X or N_P Rules 1, 2, 4, 5, 6, and 8 during split word Rules 3 and 7 during split word
$_1C_1$ =			12	C_1 holds present operand channel information, is an output register for COA, and control factor for Multiply during words 2 through 13.
	$C_{B1} [E N_D' T_X]^{E_{FB}}$		13 33	Loads new operand channel information into C_1 at first bit of Execute
	$+ ([K E O_4 O_3' O_2' O_1'] [C_5 C_4']) [C_3' C_2 C_1'] C_{B1} T_O^{O_{XU2}\ C_{L2}}$		15 8 13 9	Modifies instruction from MIM to COM if A register is positive. (Refer to $_1C_{B1}$.)

Term	Equation	Receptacle	Pin No.	Definition
$_1C_1$	(CONT)	J429	12	
	$+\left([K E O_4' O_3' O_2' O_1'] C_5 A_C\right) C_2^{O_{YST}}$		35 16	During COA, causes four-bit left shift of A register during word 1 of Execute; leaves T_{21} information in C_1 at completion of Execute
	$+\left\{\begin{matrix} L_X L_P' S_{B2}' \\ + L_X' L_P S_{B2} \end{matrix}\right\}[K Q O_4' O_3] J^{O_{MO}}$		D B C	Rule 3
			$\overline{P}$ 2	During Multiply at T_{14} and/or T_1, O_{MO} enables C_5 to copy N_P for rules 3 and 7
			11 E F	Rule 7
$_0C_1$ =			32	C_1 holds present operand channel information, is an output register for COA, and control factor for Multiply during words 2 through 13.
	$C_{B1}' [E N_D' T_X]^{E_{FB}}$		$\overline{Y}$ 33	Loads new operand channel information into C_1 at first bit of Execute
	$+\left([K E O_4' O_3' O_2' O_1'] C_5 A_C\right) C_2'^{O_{YST}}$		35 29	During COA, causes a four-bit left shift of A register during word 1 of Execute; leaves T_{21} information in C_1 at completion of Execute
	$+[K Q O_4' O_3] T_O^{O_{MO}}$		$\overline{P}$ 9	Full word. Initializes C_1 prior to determination of rules for Multiply
	$+\left([K Q O_4' O_3] O_1'\right)[B_6 B_3' T_P']^{O_{MOI}\ T_{13}}$		$\overline{R}$ 30	Split word. Initializes C_1 prior to determination of rules for Multiply
$_1D_C$ =		J437	28	D_C is a control for loading discrete register
	$[K E O_4 O_3' O_2' O_1'] [C_5' C_4] [C_3' C_2 C_1] [T_O]^{O_X\ C_{UI}\ C_{L3}\ T_{OA}}$		18 X $\overline{M}$ 4	(O_X = 40; C_{UI} C_{L3} = 26) = DOA; During Discrete Output A (DOA), controls loading (D_C) and enables discrete output lines (D_C)

Term	Equation	Receptacle	Pin No.	Definition
$_0D_C$ =		J436	W	D_C is a control for loading discrete register.
	B_5		8	T_6 through T_{16}
$_1D_R$ =		J437	1	D_R indicates trouble in external equipment.
	I_B*		6	Input line from external equipment
$_0D_R$ =			$\overline{J}$	D_R indicates trouble in external equipment
	$[K E O_4 O_3' O_2' O_1'^{O_X}] [C_5' C_4^{C_{UI}}] [C_3' C_2' C_1'^{C_{LO}}] [T_O^{T_{OA}}]$		18 X 19 4	(O_X = 40; C_{UI} C_{LO} = 20); reset Detector
$_1D_5$ =			$\overline{E}$	D_5 is most significant of discrete output register.
	$I_X (D_C^{D_S} [B_6' B_5'])$		$\overline{H}$ $\overline{F}$	Copies T_1 through T_5 information from I register into D register during Execute
	$+ F_C U_X^{T_{Z4}} [B_5' B_4' B_2 B_1']$		$\overline{K}$ $\overline{L}$ 20	When U goes negative and computer is in Fine Countdown, set D_5 to one.
$_0D_5$ =			S	D_5 is most significant of discrete output register.
	$I_X' (D_C^{D_S} [B_6' B_5'])$		9 $\overline{F}$	Copies T_1 through T_5 information of I register into D register during Execute
	$+ [K' V_C' R_C^{N_{RS}}]$		7	Initializes D register during synchronization
$_1D_4$ =		J436	V	D_4 is second most significant bit of discrete output register.
	$D_5 (D_C^{D_S} [B_6' B_5'])$		9 10	Copies T_1 through T_5 information of I register serially into D register during Execute

Term	Equation	Receptacle	Pin No.	Definition
$_0D_4$ =		J439	$\overline{W}$	D_4 is second most significant bit of discrete output register.
	D_S $D_5' (D_C [B_6' B_5'])$		39 43	Copies T_1 through T_5 information of I register serially into D register during Execute
	N_{RS} $+[K' V_C' R_C]$		41	Initializes D register during synchronization
$_1D_3$ =		J436	U	D_3 is third most significant of discrete output register.
	D_S $D_4 (D_C [B_6' B_5'])$		11 10	Copies T_1 through T_5 information of I register serially into D register during Execute
$_0D_3$ =		J439	$\overline{V}$	D_3 is third most significant of discrete output register.
	D_S $D_4' (D_C [B_6' B_5'])$		40 43	Copies T_1 through T_5 information of I register serially into D register during Execute
	N_{RS} $+[K' V_C' R_C]$		41	Initializes D register during synchronization
$_1D_2$ =			$\overline{U}$	D_2 is fourth most significant of discrete output register.
	D_S $D_3 (D_C [B_6' B_5'])$		42 43	Copies T_1 through T_5 information of I register serially into D register during Execute
$_0D_2$ =			$\overline{T}$	D_2 is fourth most significant of discrete output register.
	D_S $D_3' (D_C [B_6' B_5'])$		$\overline{L}$ 43	Copies T_1 through T_5 information of I register serially into D register during Execute
	N_{RS} $+[K' V_C' R_C]$		41	Initializes D register during synchronization

Term	Equation	Receptacle	Pin No.	Definition
$_1D_1$ =		J439	$\bar{Y}$	D_1 is least significant of discrete output register.
	$D_2 \left(D_C^{D_S} [B_6' B_5']\right)$		37 43	Copies T_1 through T_5 information of I register serially into D register during Execute
$_0D_1$ =			$\bar{X}$	D_1 is least significant of discrete output register.
	$D_2' \left(D_C^{D_S} [B_6' B_5']\right)$		38 43	Copies T_1 through T_5 information of I register serially into D register during Execute
	$+ [K' V_C' R_C]^{N_{RS}}$		41	Initializes D register during synchronization
$_1D$ =		J436	$\bar{E}$	D is a mode control flip-flop.
	$[K E] [D' T_P]^{K_E D_{TP}'} (I_C' I_X')^{I_{CX}'}$		$\bar{X}$ 36 35	Initiates Instruction Search mode during K from last word of Execute
	$+ E [D' T_P]^{D_{TP}'} [K' V_C]^{N_L}$		33 36 34	Initiates Wait mode of K' from last word of Execute
	$+ E' D' \left([K]_A O_4' O_2 [O_3' O_1'] [T_X]_A\right)^{O_{CX}} A_{24}'$		24 2 $\bar{W}$ $\bar{M}$	Initiates Instruction Search mode while in Instruction Read mode and A register is positive and instruction is Transfer on Minus (TMI)
	$+ N_D' [D' T_P]^{D_{TP}'}$		$\bar{P}$ 36	Initiates first word of Execute when number agreement is obtained between S and I_P
	$+ \left(K' V_C' J_T B_4'\right)^{N_{JT}}$		$\bar{N}$	Prevents K mode being initiated until N_P and S agree while in Halt mode
$_0D$ =			$\bar{L}$	D is a mode control flip-flop.
	$O_4 \left([K E] [E N_D' T_X]\right)^{K_{FB}}$		32 31	Initiates last word of Execute for one-word instructions

Term	Equation	Receptacle	Pin No.	Definition
$_0D$	(CONT)	J436	$\overline{L}$	
	$+O_3' O_2 ([K E] [E N_D' T_X])$		30 29 31	Initiates last word of Execute for one-word instructions
	$+[K E] C_{B5}' C_{B4}' C_{B3}' C_{B2}' N_D [T_X]$		$\overline{X}$ 6 3 A E 27 28	Initiates last word of Execute for multiword instructions
	$+K E' D I_D' [T_O]$		K 24 23 22 20	Initiates Instruction Read mode
	$+([K' J'] V_C R_C' C_{P5} C_{P4}) (C_{P3} C_{P2}' C_{P1}) [T_P]$		F7 19 18	Initiates Operand Search mode when Enter code is activated during Load
	$+K' E (N_D [D T_P])$		X 33 25	Initiates last word of Execute during Load
	$+[K' V_C' R_C' J] O_2' (B_5 B_3 [B_2 B_1']) K_S'^*$		Z $\overline{B}$ $\overline{A}$ $\overline{C}$	Initiates K mode for single-cycle operations
	$+[K E O_4' O_3' O_1] N_D [T_X]$		26 27 28	Initiates last word of Execute for SCL
$_1E$ =			$\overline{D}$	E is a mode control flip-flop.
	$E' N_D' [D' T_P]$		24 $\overline{P}$ 36	Initiates Execute mode when number agreement is found between I_P and S during T_2 through T_8
$_0E$ =			15	E is a mode control flip-flop.
	$\{ I_{CX}' \}$		35	Used when a new instruction was not read into I register during Execute
	$\{ (I_C' I_X') \}$		27	Used when there is number disagreement
	$\{ +N_D \}$		33 36	Halt Execute
	$\{ +K' \} E [D' T_P]$		X	Used when COMPUTE switch is placed at HALT

Term	Equation	Receptacle	Pin No.	Definition
$_0E$	(CONT)	J436	15	
	$+(K' V_C' N_L')$		1	Ensures that E is zero state when in Halt mode
$_1E_P$ =		J519	27, A	E_P is an E loop write amplifier.
	$S_3 S_2' A_X$		E 5 C	Copies A register into E loop when storing or flagging to E loop
	$+\left\{\begin{matrix} S_3' \\ +S_2 \end{matrix}\right\} E_X T_X'$		6 26 43 D	Recirculation
	$+[T_P] T_{PA}$		B	AGC information
$_0E_P$ =			12	E_P is an E loop write amplifier.
	$S_3 S_2' (A_X' T_P') A_{XP}'$		E 5 H	Copies A register into E loop when storing or flagging to E loop
	$+\left\{\begin{matrix} S_3' \\ +S_2 \end{matrix}\right\} E_X' T_P'$		6 T 16 D	Recirculation
	$+T_X$		7	AGC information
$_1F_C$ =	$[K E O_4 O_3' O_2' O_1' E] (C_5 C_4)[C_3' C_2' C_1'] [B_5' B_4' B_2 B_1'] O_X C_{U3} C_{LI} T_{24}$	J420	15 5 6 22 42	F_C is a fine countdown indicator. (O_X = 40; C_{U3} C_{LI} = 62) = Enter Fine Countdown
$_0F_C$ =	$[K E O_4 O_3' O_2' O_1'] (C_5 C_4)[C_3' C_2' C_1'][B_5' B_4' B_2 B_1'] O_X C_{U3} C_{LO} T_{24}$		1 5 6 17 42	F_C is a fine countdown indicator. (O_X = 40; C_{U3} C_{LO} = 60) = Halt Fine Countdown
	$+[K' V_C' R_C] N_{RS}$		A	Initializes F_C during synchronization

Term	Equation	Receptacle	Pin No.	Definition
$_1F_P$ =		J519	$\overline{X}$, 2	F_P is F loop write amplifier
	$S_2' S_1 A_X$		5 4 C	Copies A register into F loop when storing or flagging into F loop
	$+\left\{\begin{matrix} S_2 \\ \\ +S_1' \end{matrix}\right\} F_X T_X'$		D	
			$\overline{W}$ 43	Recirculation
			3	
	$+[T_P]^{T_{PA}}$		B	AGC information
$_0F_P$ =			$\overline{K}$, N	F_P is F loop write amplifier
	$S_2' S_1 (A_X' T_P')^{A_{XP}'}$		5 4 H	Copies A register into F loop when storing or flagging into F loop
	$+\left\{\begin{matrix} S_2 \\ \\ +S_1' \end{matrix}\right\} F_X' T_P'$		D	
			$\overline{J}$ 16	Recirculation
			3	
	$+T_X$		7	AGC information
$_1G_3$ =		J439	$\overline{R}$	G_3 is a binary output C flip-flop
	$([K E O_4 O_3' O_2' O_1'] [C_5' C_4']) C_3' A_P [T_P]^{T_{PB}}$		28 36 34 35	(O_{XUO} = 40; $[C_5' C_4'] C_3'$ = 02) = BOC; Loads sign of A register into G_3
$_0G_3$ =			$\overline{C}$	G_3 is a binary output C flip-flop
	$([K E O_4 O_3' O_2' O_1'] [C_5' C_4']) C_3' A_P' [T_P]^{T_{PB}}$		28 36 30 35	(O_{XUO} = 40; $[C_5' C_4'] C_3'$ = 02) = BOC; Loads sign of A register into G_3

Term	Equation	Receptacle	Pin No.	Definition
$_1G_2$ =		J439	$\bar{S}$	G_2 is a binary output B flip-flop
	$([K E O_4 O_3' O_2' O_1'] [C_5' C_4']) C_3 C_1 A_P [T_P]^{O_{XUO}}_{T_{PB}}$		28 31 $\bar{J}$ 34 35	(O_{XUO} = 40; $[C_5' C_4']$ C_3 C_1 = 12) = BOB; Loads sign of A register into G_2
$_0G_2$ =			$\bar{B}$	G_2 is a binary output B flip-flop
	$([K E O_4 O_3' O_2' O_1'] [C_5' C_4']) C_3 C_1 A_P' [T_P]^{O_{XUO}}_{T_{PB}}$		28 31 $\bar{J}$ 30 35	(O_{XUO} = 40; $[C_5' C_4']$ C_3 C_1 = 12) = BOB; Loads sign of A register into G_2
$_1G_1$ =			$\bar{P}$	G_1 is a binary output A flip-flop
	$([K E O_4 O_3' O_2' O_1'] [C_5' C_4']) C_1' A_P [T_P]^{O_{XUO}}_{T_{PB}}$		28 29 34 35	(O_{XUO} = 40; $[C_5' C_4']$ C_1' = 10) = BOA; Loads sign of A register into G_1
$_0G_1$ =			$\bar{D}$	G_1 is a binary output A flip-flop
	$([K E O_4 O_3' O_2' O_1'] [C_5' C_4']) C_1' A_P' [T_P]^{O_{XUO}}_{T_{PB}}$		28 29 30 35	(O_{XUO} = 40; $[C_5' C_4']$ C_1' = 10) = BOA; Loads sign of A register into G_1
$_1H_P$ =		J519	41, 1	H_P is H loop write amplifier
	$S_3 S_2 S_1' A_X$		E D 3 C	Copies A register into H loop when storing or flagging to H loop
	$+\left\{\begin{matrix} S_3' \\ +S_2' \\ +S_1 \end{matrix}\right\} H_X T_X'$		6 5 42 43 4	Recirculation
	$+ [T_P]^{T_{PA}}$		B	AGC information

Term	Equation	Receptacle	Pin No.	Definition
$_0H_P$ =		J519	M	H_P is H loop write amplifier
	$S_3\ S_2\ S_1'\ (A_X'\ T_P')^{A_{XP}'}$		E D 3 H	Copies A register into H loop when storing or flagging to H loop
	$+\left\{\begin{matrix} S_3' \\ +S_2' \\ +S_1 \end{matrix}\right\} H_X'\ T_P'$		6	
			15 16	Recirculation
			5	
			4	
	$+\ T_X$		7	AGC information
$_1H_S$ =	$\left\{\begin{matrix} C_5'\ [A_X']\ A_K^{A_{XA}'} \\ +C_5'\ [A_X]\ A_K'^{A_{XA}} \\ +C_5\ [A_X']\ A_K'^{A_{XA}'} \\ +C_5\ [A_X]\ A_K^{A_{XA}} \end{matrix}\right\} (C_4\ C_3\ A_C)^{M_C}$	J537	$\bar{D}$	H_S determines sign of product of multiplication
			2 L M	
			2 6 X	
			$\bar{M}$	Multiply
			S L X	Monitors multiplicand and multiplier to determine if product will be zero
			S 6 M	
	$+\ C_4'\ C_3\ [A_X]^{A_{XA}}$		25 $\bar{E}$ 6	
$_0H_S$ =			$\bar{H}$	H_S determines sign of product of multiplication
	$([B_6'\ B_5'\ B_3]\ B_4')^{T_1}$		$\bar{F}$	Initializes H_S prior to monitoring multiplicand and multiplier

Term	Equation	Receptacle	Pin No.	Definition
$_0H_S$	(CONT)	J537	$\overline{H}$	
	$+ O_1' \left([B_6 B_5 B_4] B_1 \right)^{T_{15}}$		$\overline{C}\,\overline{B}$	Initializes H_S prior to monitoring multiplicand and multiplier
$_1I_C$ =		J429	$\overline{S}$	I_C is an I register interrupt control flip-flop
	$\left\{ \begin{matrix} E' D \\ + E I_P' \end{matrix} \right\} K I_D' T_O$		37 $\overline{X}$	Used in Instruction Search mode
			$\overline{K}\,\overline{T}$ 9	Used when instruction agreement is found
			$\overline{M}\,\overline{F}$	Used in the Execute mode if there is no anti-repeat one
	$+ \left([K' J'] V_C R_C' C_{P5} C_{P4} \right)^{N_{PC}} \left(C_{P3}' C_{P2}' C_{P1} \right)^{C_{PL1}} T_O$		31 $\overline{N}$ 9	One-sets I_C when Locate code is activated during Load
	$+ [K' V_C' R_C]^{N_{RS}} T_O$		43 9	One-sets I_C during synchronization to enable unconditional Transfer command to be put into I register
$_0I_C$ =	$[T_P]^{T_{PB}}$	J432	31	I_C is an I register interrupt control flip-flop
			25	Resets I_C each T_P time
$_1I_D$ =		J436	$\overline{F}$	I_D indicates instruction agreement with various word length channels
	$\left\{ \begin{matrix} \left([B_6 B_5 B_4] [B_2 B_1'] \right)^{T_{16}} \\ + \left(C_{P3} C_{P2} C_{P1}' \right)^{C_{PL6}} \left([B_6 B_5' B_4] [B_2' B_1] \right)^{T_{17}} \end{matrix} \right\} O_{B3} C_{P3}$		$\overline{R}$	F loop and E loop four-word disagreement
			5 $\overline{H}$	
			$\overline{T}\,\overline{S}$	H loop eight-word disagreement
	$+ \left\{ \begin{matrix} C_{P5}' \\ + C_{P4}' C_{P3}' \\ + C_{P4}' \left(C_{P3} C_{P2} C_{P1}' \right)^{C_{PL4}} \end{matrix} \right\} O_{B1} \left([B_6 B_4' B_3] [B_2' B_1'] \right)^{T_{22}}$		43	Channels 00 through 36
			41 42	Channels 40 through 46
			D $\overline{Y}$	128-word disagreement
			41 40	Channel 50

Term	Equation	Receptacle	Pin No.	Definition
$_1I_D$	(CONT)	J436	$\overline{F}$	
	$+ W_A [B_5 B_4' B_3 B_2] I_{5B}^{T_{11}}$		$\overline{V}$ 39 $\overline{U}$	I_D is used as input buffer for resolver line I_{5B}* at word 3 (module four counter)
	$+ W_A' [B_5 B_4' B_3 B_2] I_{6B}^{T_{11}}$		38 39 37	I_D is used as input buffer for resolver line I_{6B}* at word 2 (module four counter)
$_0I_D$ =		J432	15	I_D indicates instruction agreement with various word length channels
	$N_D' [K O_4 O_3' O_2 O_1'] [T_X]^{O_U \quad T_{XA}}$		20 19 18	Used to force instruction agreement when number agreement is found and instruction is 50 (Transfer)
	$+ N_D' ([K]_A O_4' O_2 [O_3' O_1'] [T_X]_A)^{O_{CX}} A_{24}$		20 22 23	Used to force instruction agreement when number agreement is found, A register is negative, and instruction is 10 (TMI)
	$+ B_5 B_2'$		$\overline{V}$ 24	T_6, T_9, T_{10}, T_{13}, and T_{14} initialize I_D prior to Instruction Search (T_{14} through T_{20}); used for buffering in resolver lines I_{5B} and I_{6B}
$_1I_P$ =		J423	16	I_P is delay flip-flop for I register, Loads new instructions into I register from memory, inserts anti-repeat one, and inserts Transfer (TRA) into I register during synchronization

Term	Equation	Receptacle	Pin No.	Definition
$_1I_P$	(CONT)	J423	16	
	$\left\{ \begin{array}{l} C_{PL0} \\ (C_{P3}' C_{P2}' C_{P1}') M_{00} \\ C_{PL1} \\ + (C_{P3}' C_{P2}' C_{P1}) M_{02} \\ C_{PL2} \\ + (C_{P3}' C_{P2} C_{P1}') M_{04} \\ C_{PL3} \\ + (C_{P3}' C_{P2} C_{P1}) M_{06} \\ C_{PL4} \\ + (C_{P3} C_{P2}' C_{P1}') M_{10} \\ C_{PL5} \\ + (C_{P3} C_{P2}' C_{P1}) M_{12} \\ C_{PL6} \\ + (C_{P3} C_{P2} C_{P1}') M_{14} \\ C_{PL7} \\ + (C_{P3} C_{P2} C_{P1}) M_{16} \end{array} \right\} K_{IC} (K I_C T_P') C_{P5}' C_{P4}'$		N M C A J 8 F 10 18 13 P K 7 H 9 D 12 E 11	Used to read a new instruction into I register when instruction agreement is found. Channel is designated by setting C_P flip-flops

Term	Equation	Receptacle	Pin No.	Definition
I_P	(CONT)	J423	16	
	$\left\{ \begin{array}{l} C_{PL0} \\ \left(C_{P3}' C_{P2}' C_{P1}'\right) M_{20} \\ + \left(C_{P3}' C_{P2}' C_{P1}\right) M_{22} \\ + \left(C_{P3}' C_{P2} C_{P1}'\right) M_{24} \\ + \left(C_{P3}' C_{P2} C_{P1}\right) M_{26} \\ + \left(C_{P3} C_{P2}' C_{P1}'\right) M_{30} \\ + \left(C_{P3} C_{P2}' C_{P1}\right) M_{32} \\ + \left(C_{P3} C_{P2} C_{P1}'\right) M_{34} \\ + \left(C_{P3} C_{P2} C_{P1}\right) M_{36} \end{array} \right\}$	N L		
		C B		
		J 5		
		F 3		
	$+ \left(K I_C T_P'\right) C_{P5}' C_{P4}$	18 13 28		Used to read a new instruction into I register when instruction agreement is found. Channel is designated by setting C_P flip-flops
		K 6		
		H 4		
		D 1		
		E 2		

Term	Equation	Receptacle	Pin No.	Definition
$_1I_P$	(CONT)	J423	16	
	$\left\{ \begin{array}{l} C_{PL0} \\ (C_{P3}' C_{P2}' C_{P1}') M_{40} \\ C_{PL1} \\ + (C_{P3}' C_{P2}' C_{P1}) M_{42} \\ C_{PL2} \\ + (C_{P3}' C_{P2} C_{P1}') M_{44} \\ C_{PL3} \\ + (C_{P3}' C_{P2} C_{P1}) M_{46} \\ + \left\{ \begin{array}{l} C_{PL4} \\ + (C_{P3} C_{P2}' C_{P1}') M_{50} \\ C_{PL5} \\ + (C_{P3} C_{P2}' C_{P1}) F_X \\ C_{PL6} \\ + (C_{P3} C_{P2} C_{P1}') H_X \\ C_{PL7} \\ + (C_{P3} C_{P2} C_{P1}) E_X \end{array} \right. \end{array} \right\} K_{IC} ([K]_A I_C T_P') C_{P5} C_{P4}'$		N 21 C 25 J Z F 23 18 V P K Y H 22 D 24 E 19	Used to read a new instruction into I register when instruction agreement is found. Channel is designated by setting C_P flip-flops
	$\left\{ \begin{array}{l} C_{PL0} \\ + (C_{P3}' C_{P2}' C_{P1}') U_X \\ C_{PL1} \\ + (C_{P3}' C_{P2}' C_{P1}) A_X \\ C_{PL6} \\ + (C_{P3} C_{P2} C_{P1}') H_{MX} \\ C_{PL7} \\ + (C_{P3} C_{P2} C_{P1}) E_{MX} \end{array} \right\} K_{IC} ([K]_A I_C T_P') C_{P5} C_{P4}$		N 35 C $\overline{F}$ 18 V 28 D 27 E 26	Used to read a new instruction into I register when instruction agreement is found. Channel is designated by setting C_P flip-flops

Term	Equation	Receptacle	Pin No.	Definition
I_P	(CONT)	J423	16	
	$I_C \left(E \left[D \overset{E_{TP}}{T_P}\right]\right)$		$\overline{L}\ \overline{Y}$	Inserts the anti-repeat one into I register when an instruction is in Execute and another is read into I register
	$+ I_X \left(E\left[D \overset{E_{TP}}{T_P}\right]\right)$		$\overline{X}\ \overline{Y}$	Recirculates the anti-repeat one
	$+ K I_C' I_X \left[T_P' T_X' \overset{T_{PXO}}{T_O}'\right]$		$\overline{V}\ \overline{W}\ \overline{X}\ \overline{N}$	Recirculation during Compute
	$+ I_X' T_O$		42 43	Inversion type AGC information
	$+ B_1' \left[K' V_C' \overset{N_{RS}}{R_C}\right] \left[B_6 B_4' \overset{B_{6MI}}{B_3}\right]$		33 36 34	Insert instruction 50 into I register during synchronization
	$+ A_K' I_X K' I_C' \left[T_P' T_X' \overset{T_{PXO}}{T_O}'\right]$		$\overline{M}\ \overline{X}$ 39 $\overline{W}\ \overline{N}$	Recirculation during Noncompute mode
	$+ A_K \left(I_C' \overset{I_{CX}}{I_X}'\right) K' \left[T_P' T_X' \overset{T_{PXO}}{T_O}'\right]$		$\overline{37}\ \overline{38}\ \overline{39}\ \overline{N}$	Copies I_X inversely into I_P when Enter code is activated to increase I register by one
	$+ L_X \left[K' \overset{N_L}{V_C}\right] I_C$		$\overline{J}\ \overline{K}\ \overline{L}$	Inserts contents of L register into I register when Locate code is activated during Load

Term	Equation	Receptacle	Pin No.	Definition
0^{I}_{P} =	$\left\{ \begin{array}{l} C_{PLO} \\ (C_{P3}' C_{P2}' C_{P1}') M_{00}' \\ C_{PL1} \\ + (C_{P3}' C_{P2}' C_{P1}) M_{02}' \\ C_{PL2} \\ + (C_{P3}' C_{P2} C_{P1}') M_{04}' \\ C_{PL3} \\ + (C_{P3}' C_{P2} C_{P1}) M_{06}' \\ C_{PL4} \\ + (C_{P3} C_{P2}' C_{P1}') M_{10}' \\ C_{PL5} \\ + (C_{P3} C_{P2}' C_{P1}) M_{12}' \\ C_{PL6} \\ + (C_{P3} C_{P2} C_{P1}') M_{14}' \\ C_{PL7} \\ + (C_{P3} C_{P2} C_{P1}) M_{16}' \end{array} \right\} \begin{array}{l} K_{IC} \\ ([K]_A I_C T_P') C_{P5}' C_{P4}' \end{array}$	J424	30 1 2 3 4 J 6 7 8 42 41 40 9 10 11 12 5 E F H	I_P is delay flip-flop for I register, Loads new instructions into I register from memory, inserts anti-repeat one, and inserts Transfer (TRA) into I register during synchronization Used to read a new instruction into I register when instruction agreement is found. Channel is designated by setting C_P flip-flops

Term	Equation	Receptacle	Pin No.	Definition
0^{I}_{P}	(CONT)	J424	30	
	$\left\{ \begin{array}{l} {}^{C_{PL0}}(C_{P3}' C_{P2}' C_{P1}') M_{20}' \\ + {}^{C_{PL1}}(C_{P3}' C_{P2}' C_{P1}) M_{22}' \\ + {}^{C_{PL2}}(C_{P3}' C_{P2} C_{P1}') M_{24}' \\ + {}^{C_{PL3}}(C_{P3}' C_{P2} C_{P1}) M_{26}' \\ + {}^{C_{PL4}}(C_{P3} C_{P2}' C_{P1}') M_{30}' \\ + {}^{C_{PL5}}(C_{P3} C_{P2}' C_{P1}) M_{32}' \\ + {}^{C_{PL6}}(C_{P3} C_{P2} C_{P1}') M_{34}' \\ + {}^{C_{PL7}}(C_{P3} C_{P2} C_{P1}) M_{36}' \end{array} \right\} \left([K]_{A}\, {}^{K_{IC}} I_{C}\, T_{P}' \right) C_{P5}' C_{P4}$		1 D 3 C J M 7 L 42 41 43 9 K 11 13 5 B F A	Used to read a new instruction into I register when instruction agreement is found. Channel is designated by setting C_P flip-flops

Term	Equation	Receptacle	Pin No.	Definition
$_0I_P$	(CONT)	J424	30	
	$+\left\{\begin{array}{l} C_{PL0} \\ (C_{P3}' C_{P2}' C_{P1}') M_{40}' \\ C_{PL1} \\ + (C_{P3}' C_{P2}' C_{P1}) M_{42}' \\ C_{PL2} \\ + (C_{P3}' C_{P2} C_{P1}') M_{44}' \\ C_{PL3} \\ + (C_{P3}' C_{P2} C_{P1}) M_{46}' \\ C_{PL4} \\ + (C_{P3} C_{P2}' C_{P1}) M_{50}' \\ C_{PL5} \\ + (C_{P3} C_{P2}' C_{P1}) F_X' \\ C_{PL6} \\ + (C_{P3} C_{P2} C_{P1}') H_X' \\ C_{PL7} \\ + (C_{P3} C_{P2} C_{P1}) E_X' \end{array}\right\} \overset{K_{IC}}{([K]_A I_C T_P')} C_{P5} C_{P4}'$		1 N 3 P J 17 7 15 42 39 40 9 V 11 18 5 S F U	Used to read a new instruction into I register when instruction agreement is found. Channel is designated by setting C_P flip-flops

Term	Equation	Receptacle	Pin No.	Definition
0^{I}_{P}	(CONT)	J424	30	
	$\left\{ \begin{array}{l} C_{PL0} \\ (C_{P3}' C_{P2}' C_{P1}') U_X' \\ + (C_{P3}' C_{P2}' C_{P1}) A_X' \\ + (C_{P3} C_{P2} C_{P1}') H_{MX}' \\ + (C_{P3} C_{P2} C_{P1}) E_{MX}' \end{array} \right\} ([K]_A I_C T_P') C_{P5} C_{P4}$		1 $\overline{H}$ 3 $\overline{F}$ 42 39 43 5 $\overline{E}$ F $\overline{D}$	Used to read a new instruction into I register when instruction agreement is found. Channel is designated by setting C_P flip-flops
	$+ [D' T_P]^{D_{TP}'}$		28	Destroys the anti-repeat one if present
	$+ (I_C' I_X')^{I_{CX}'} (E[D T_P])^{E_{TP}}$		$\overline{A}$ $\overline{C}$	Recirculates zeros in the anti-repeat position if a one has not been written
	$+ K (I_C' I_X')^{I_{CX}'} [T_P' T_X' T_O']^{T_{PXO}'}$		W $\overline{A}$ 21	Recirculation during Compute
	$+ I_X T_O$		22 $\overline{V}$	Inversion type AGC information
	$+ B_1 [K' V_C' R_C]^{N_{RS}}$		27 26	Inserts instruction 50 into I register during synchronization
	$+ A_K' (I_C' I_X')^{I_{CX}'} K' [T_P' T_X' T_O']^{T_{PXO}'}$		$\overline{B}$ $\overline{A}$ Y 21	Recirculation during Noncompute mode
	$+ A_K I_X K' I_C' [T_P' T_X' T_O']^{T_{PXO}'}$		19 22 Y Z 2	Copies I_X inversely when Entercode is activated so I register will be increased by one
	$+ L_X' [K' V_C]^{N_L} I_C$		25 24 23	Copies L register into I register when Locate code is activated

Term	Equation	Receptacle	Pin No.	Definition
$_1I_{24W}$ =		J521	$\overline{Y}$	I_{24W} is an I register write amplifier
	I_P		41	Puts contents of I_P into I_{24}
$_0I_{24W}$ =			$\overline{X}$	I_{24W} is an I register write amplifier
	I_P'		42	Puts contents of I_P into I_{24}
$_1J_T$ =		J537	43	J_T compares N_P and S for entering Compute mode
	$N_P S' B_4$		41 40 42	Compares N and S for agreement
	$+ N_P' S B_4$		39 38 42	
	$+ [T_P]^{T_{PA}}$		37	Sets J_T to one to enable J_T to one-set D
$_0J_T$ =			35	J_T compares N_P and S for entering Compute mode
	T_X		36	Initializes prior to agreement check
$_1J$ =		J435	37	J samples discrete inputs during Compute mode, used as parity bit for COA, transfers most significant bit of voltage output in V register, holds sign of left-half word of A register during SCL, decodes flip-flop for Multiply, and used as mode control during Noncompute mode.
	$C_1 ([KEO_4O_3'O_2'O_1'][C_5 C_4'])^{O_{XU2}} \{ [T_O]^{T_{OA}} X_1^* + ([B_6' B_5' B_3][B_2' B_1'])^{T_2} X_3^* + ([B_6' B_5'][B_2 B_1'])^{T_4} X_5^* + (B_6' B_5 B_4)^{B_{LU3}} B_2' X_7^* + (B_6' B_5 B_4)^{B_{LU3}} [B_2 B_1']^{B_{L2}} X_9^* + (B_5 B_4' B_3 B_1')^{T_{10}} X_{11}^* \}$		E D	($C_1 = 2$; $O_{XU2} = 40$; $[C_5 C_4'] = 5$) = 40XX5200 = DIA
			B A	
			5 4	
			17 12	
			L K S	
			L M P	Puts state of odd-numbered X lines into J and, in turn, into A register
			2 1	

Term	Equation	Receptacle	Pin No.	Definition
$_1J$	(CONT)	J435	37	
	$\{(B_3' B_2) X_{13}^{T_{12}}$		$\overline{U}\ \overline{V}$	Puts state of odd-numbered X lines into J and, in turn, into A register
	$+([B_6 B_5 B_4]\ B_2') X_{15}^{T_{14}}$		$\overline{X}\ \overline{Y}$	
	$+([B_6 B_5 B_4]\ [B_2 B_1']) X_{17}^{T_{16}}$		39 40	
	$+([B_6 B_5' B_4]\ [B_2 B_1']) X_{19}^{T_{18}}$		42 43	
	$+([B_6 B_5' B_4]\ [B_2 B_1']) F_C^{T_{20}}$		34 33	
	$+([B_6 B_4' B_3]\ [B_2' B_1']) P_1^{T_{22}}\}$		31 30	
	$C_1([R E O_4 O_3' O_2' O_1'']\ [C_5 C_4''])^{O_{XU2}}$		17 12	$(C_1 = 2; O_{XU2} = 40; [C_5 C_4'] = 5) = 40XX5200 = DLA$
	$+([K' V_C]\ R_C'\ [T_P])C_{P5}^{N_{LRC}' T_{PB}}$		$\overline{S}\ \overline{E}\ \overline{R}$	One-sets J at T_P time of Process code during Load to initiate Wait mode

Term	Equation	Receptacle	Pin No.	Definition
$_1J$	(CONT)	J435	37	
	T_{OA}			
	$[T_O]\ Y_1^*$		E 7	
	$+\left([B_6'B_5'B_3]^{T_2}[B_2'B_1']\right)Y_3^*$		B C	Puts state of odd-numbered Y lines into J and, in turn, into A register
	$+\left([B_6'B_5']^{T_4}[B_2B_1']\right)Y_5^*$		5 H	
+	$C_1'\left([KEO_4O_3'O_2'O_1']^{O_{XU2}}[C_5C_4']\right)$		15 12	$(C_1' = 0; O_{XU2} = 40; [C_5C_4'] = 5) = 40XX5000 = DIB$
	$+\left(B_6'B_5B_4\right)^{B_{LU3}}B_2'Y_7^*$		L K J	
	$+\left(B_6'B_5B_4\right)^{B_{LU3}}[B_2B_1']^{B_{L2}}Y_9^*$		L M N	
	$+\left(B_5B_4'B_3B_1'\right)^{T_{10}}Y_{11}^*$		2 3	

Term	Equation	Receptacle	Pin No.	Definition
$_1J$	(CONT)	J435	37	
	$\left\{ \begin{array}{l} (B_3' B_2)\, Y_{13}^{T_{12}} \\ + ([B_6 B_5 B_4]\, B_2')\, Y_{15}^{T_{14}} \\ + ([B_6 B_5 B_4]\, [B_2 B_1'])\, Y_{17}^{T_{16}} \\ + \\ + ([B_6 B_5' B_4]\, [B_2' B_1'])\, Y_{19}^{T_{18}} \\ + ([B_6 B_5' B_4]\, [B_2 B_1'])\, Y_{21}^{T_{20}} \\ + ([B_6 B_4' B_3]\, [B_2' B_1'])\, Y_{23}^{T_{22}} \end{array} \right\} C_1' ([K E O_4 O_3' O_2' O_1']\, [C_5 C_4'])^{O_{XU2}}$		$\overline{U}\ \overline{T}$	Puts state of odd-numbered Y lines into J and, in turn, into A register
			$\overline{X}\ \overline{W}$	
			39 38	
			15 12	$(C_1' = 0;\ O_{XU2} = 40;\ [C_5 C_4'] = 5) = 40XX5000$ = DIB
			42 41	
			34 35	
			31 32	
	$+ [K' V_C' R_C]\, [T_P]^{N_{RS}\ T_{PB}}$		$\overline{D}\ \overline{E}$	Initiates Sync Bit Counter 1 mode
	$+ (K' V_C')\, R_C' K_R'^{*}\, [T_P]^{N_L'\ T_{PB}}$		$\overline{J}\ \overline{H}\ \overline{F}\ \overline{E}$	Ensures mode to be manual Halt when COMPUTE switch is at HALT
	$+ [K E O_4' O_3' O_2' O_1']\, Q'\, [B_6 B_4' B_3]^{B_{6M1}}\, [A_X]^{A_{XA}}\, J'^{O_Y}$		T U V W X	Counts the ones from A_X during COA at T_1 through T_{24}. J serves as parity bit.
	$+ ([K E]\, O_4^{*} O_3)\, [T_O]^{O_M\ T_{OA}}$		$\overline{B}\ E$	Used during Multiply. J is a decoding flip-flop. Decoding time is T_1 for full word and T_1 and T_{14} for split word.

Term	Equation	Receptacle	Pin No.	Definition
1^J	(CONT)	J435	37	
	$+[K E O_4 O_3' O_2' O_1'] [C_5' C_4] A_{24} [T_P' T_X' T_O']^{O_X\ C_{U1}\ T_{PXO}'}$		$\overline{K}\,\overline{N}$ 36 $\overline{M}$	Used during voltage output. J holds fourth most significant bit at T_{11} or T_{24} which is put into Vi5, i = 1, 2, or 3
	$+[K E O_4' O_3' O_1] A_{24} [T_X]^{O_L\ T_{XA}}$		28 36 29	Used during SCL. Puts sign of left-half word of A register into J to determine polarity of A register
	$+([K E] O_4' O_3) O_1' [B_6 B_3' T_P']^{O_M\ T_{13}}$		$\overline{B}\,\overline{A}$ Z	Used during Multiply. J is a decoding flip-flop. Decoding time is T_1 for full word and T_1 and T_{14} for split word.
0^J *			22	J samples discrete inputs during Compute mode, used as parity bit for COA, transfers most significant bit of voltage output in V register, holds sign of left-half word of A register during SCL, decodes flip-flop for Multiply, and used as mode control during Noncompute mode.
	$B_1 ([K E O_4 O_3' O_2' O_1'] [C_5 C_4'])^{O_{XU2}}$		13 12	Initializes J at odd-numbered bit times in preparation for monitoring discrete input lines at even bit times
	$+[K' V_C] R_C' ([B_4' B_3 B_2] B_5' B_1)^{N_L\ T_{23}}$		11 10 9	Advances from Prepare-to-Sample mode to Sample mode to Load
	$+M_R$ *		23	Master reset
	$+(K [D' T_P])^{K_{DP}}$		8	Initializes J at last bit of operand search or Execute mode during Compute (K)
	$+[K E O_4' O_3' O_2' O_1'] Q' [B_6 B_4' B_3] [A_X] J^{O_Y\ B_{6M1}}$		T U V W $\overline{C}$	Counts the ones from A_X at T_{21} through T_{24} during COA. J serves as parity bit.
	$+([K E] O_4' O_3) J^{O_M}$		$\overline{B}\,\overline{C}$	Resets J during Multiply. (Refer to $O_M\ T_{OA}$ logic for 1^J.)
	$+[K E O_4 O_3' O_2' O_1'] [C_5' C_4] A_{24}'^{O_X\ C_{U1}}$		$\overline{K}\,\overline{N}\,\overline{L}$	Copies A during voltage output. (Refer to $O_X\ C_{UI}\ A_{24}\ T_{PXO}'$ logic for 1^J.)

Term	Equation	Receptacle	Pin No.	Definition
$_1K$ =		J435	24	K is a mode control.
	$[K' V_C' R_C' J] (D' [B_6 B_3' T_P'])^{N_{MH}\ D_{13}'}$		26 27	Enters Compute mode (K) when N and S agree. (Refer to J_T and D logic.)
$_0K$ =			16	K is a mode control.
	$\left\{ I_C \right\}^{D_{TP}'} [D' T_P] K_R'^*$		19	K is a mode control.
	$\left\{ + (I_X F_1)^{I_{XE}} \right\}$		25 $\overline{F}$	Halts Compute mode when COMPUTE switch is at HALT and when executing a new instruction which has already been read into I register
			20	
	$+[K E O_4 O_3' O_2' O_1'] [C_5' C_4] [C_3' C_2' C_1] [T_P]^{O_X\ C_{U1}\ C_{L1}\ T_{PB}}$		$\overline{K}\,\overline{N}\,\overline{P}\,\overline{E}$	$(O_X = 40; [C_5' C_4] C_3' = 2; C_2' C_1 = 2)$ = 40XX2200 = HPR. Forces the computer into Program Halt mode at T_P of that word.
	$+M_R^*$		23	Initializes K to zero state
$_1L_C$ =		J522	U	L_C is an L register interrupt control flip-flop.
	$([K E] O_4' O_3) [E N_D' T_X]^{O_M\ E_{FB}}$		12 P	Used during Multiply to one-set L_C so multiplier in A register may be put into L register
	$+ S_{B3} S_{B2}' S_{B1} ([K E] [E N_D' T_X])^{K_{FB}}$		N K M S	One-sets L_C by Flag code which allows L register to copy A register.
	$+ ([K J'] V_C R_C' C_{P5} C_{P4}) (C_{P3} C_{P2} C_{P1}')^{N_{PC}\ C_{PL6}} T_O$		J T 11	One-sets L_C when Clear code is activated and at Process mode of Load
	$+ ([K' V_C] R_C') J' C_{P5} C_{P4}'^{N_{LRC}'} T_O$		H F E 15 11	One-sets L_C when an octal number code is activated and at Process mode of Load

Term	Equation	Receptacle	Pin No.	Definition
$_0L_C$ =		J522	32	L_C is an L register interrupt control flip-flop.
	D_{TP}'			
	$[D' T_P]$		37	Initializes L_C at each D' T_P during operand search or last word of Execute during Compute
	T_{24}			
	$+ K' [B_5' B_4' B_2 B_1']$		35 36	Zero-sets L_C when not in Compute
	T_{PA}			
	$+ O_3' [T_P]$		$\overline{T}$ D	Resets L_C if A register was flagged to L register during Y specials and SCL.
$_1L_P$ =			$\overline{J}$	L_P is L register delay flip-flop, receives new information from A register during Compute, and character input during Noncompute
	$L_X L_C' T_P'$		$\overline{N}$ $\overline{P}$ $\overline{R}$	Recirculation
	$+ K A_X L_C Q' T_P'$		$\overline{S}$ $\overline{L}$ 34 $\overline{K}$ $\overline{R}$	During Compute, copies A register into L register for flag during word 1 of Execute and during word 1 of SMP
	$+ K' L_C C_{P1}$		35 34 33	Inserts new information into L register from C_P flip-flops during Load mode
	T_{PA}			
	$+ L_X' [T_P]$		39 D	Inversion type AGC information
	O_{MO}			
	$+ [K Q O_4' O_3] L_X$		$\overline{M}$ $\overline{N}$	L_P copies L_X during Multiply. L_P and L_X contain multiplier bits at T_1 for full word and at T_1 and T_{14} for split word
$_0L_P$ =			$\overline{V}$	L_P is L register delay flip-flop, receives new information from A register during Compute, and character input during Noncompute
	$L_X' L_C' T_P'$		39 $\overline{P}$ $\overline{R}$	Recirculation
	$+ K A_X' L_C Q' T_P'$		$\overline{S}$ 38 34 $\overline{K}$ $\overline{R}$	During Compute, copies A register into L register for flag during word 1 of Execute and during word 1 of SMP
	$+ K' L_C C_{P1}'$		35 34 43	Inserts new information into L register from C_P flip-flops during Load mode

Term	Equation	Receptacle	Pin No.	Definition
$_0L_P$	(CONT)	J522	$\overline{V}$	
	$+[T_P]^{T_{PA}} L_X$		D $\overline{N}$	Inversion type AGC information
	$+[K Q O_4' O_3]^{O_{MO}} L_X'$		$\overline{M}$ 39	L_P copies L_X during Multiply. L_P and L_X contain multiplier bits at T_1 for full word and at T_1 and T_{14} for split word
$_1L_X$ =			$\overline{D}$	L_X is an L register delay flip-flop.
	L_O		$\overline{E}$	Direct copy during recirculation
$_0L_X$ =			16	L_X is an L register delay flip-flop.
	L_O'		25	Direct copy during recirculation
$_1L_{24}$ =			30	L_{24} is an L register delay flip-flop and copies A register into L register during Multiply.
	$[K N_C O_4' O_3]^{O_{MF}} O_1 A_X T_O'$		$\overline{A}$ $\overline{B}$ $\overline{L}$ 27	Multiplies full word. Inserts A register into L register with one bit right shift
	$+([K E] O_4' O_3) Q' [T_X]^{O_M\ T_{XA}}$		12 $\overline{K}$ 26	Inserts AGC at word 1 of Multiply
	$+[K Q O_4' O_3]^{O_{MO}} L_O$		$\overline{M}$ $\overline{E}$	During words 2 through 13 of Multiply, L register is 25-bit register.
	$\left.\begin{array}{l} L_C' \\ + C_{B1}[K N_C O_4' O_3]^{O_{MF}} T_O' \\ + O_4 \\ + O_3' \end{array}\right\} L_P$		$\overline{P}$	Normal recirculation
			Y $\overline{A}$ 27	Copies L_P for word 1 of SMP
			29	Recirculation
			V	Used during all instructions 40 and above during K and when L_C is one during Load mode
			$\overline{T}$	Used during all instructions 10 and below during K

Term	Equation	Receptacle	Pin No.	Definition
$_0L_{24}$ =		J522	17	L_{24} is an L register delay flip-flop and copies A register into L register during Multiply.
	$\left\{\begin{array}{l} O_1 A_X' \\ + O_1' [B_6 B_3' T_P']^{T_{13}} \\ + T_O \end{array}\right\} [K N_C O_4' O_3]^{O_{MF}}$		$\overline{B}$ 38	Copies A register into L register for full word with a one-bit right shift
			24 23	Zero next to least significant bit for SMP
			$\overline{A}$	Word 1 of Multiply
			11	AGC and zero next to least significant bit for full word and right-half word of SMP
	$+ [K Q O_4' O_3] L_O'^{O_{MO}}$		$\overline{M}$ 25	During words 2 through 13 of Multiply, L register is a 25-bit register
	$+ \left\{\begin{array}{l} L_C' T_X' \\ + C_{B1} [K N_C O_4' O_3]^{O_{MF}} \\ + O_4 \\ + O_3' \\ + E' \end{array}\right\} L_P'$		$\overline{P}$ W	Normal recirculation
			Y $\overline{A}$	Word 1 of SMP
			22	Recirculation
			V	Used for instructions 40 and above during K and when L_C is one during Load
			$\overline{T}$	Used for instructions 10 and below during K
			Z	Nonexecute during Load mode for Clear code

Term	Equation	Receptacle	Pin No.	Definition
$_1M_{PX}$ =		J535	7	M_{PX} is a multiplex flip-flop and copies desired channel for display purposes.
	$\{C_{DL0}^{*} M_{00}$		35 E	
	$+ C_{DL1}^{*} M_{02}$		34 6	
	$+ C_{DL2}^{*} M_{04}$		$\overline{S}$ D	
	$+ C_{DL3}^{*} M_{06}\}C_{DU0}^{*}$		8 L	
			1	M_{PX} copies desired channel as determined by switch settings on control panel. M_{PX} will then telemeter the desired channel to control panel or external equipment for display purposes.
	$+ C_{DL4}^{*} M_{10}$		9 5	
	$+ C_{DL5}^{*} M_{12}$		11 4	
	$+ C_{DL6}^{*} M_{14}$		22 3	
	$+ C_{DL7}^{*} M_{16}\}$		18 2	
	$+\{C_{DL0}^{*} M_{20}$		35 N	
	$+ C_{DL1}^{*} M_{22}$		34 12	
	$+ C_{DL2}^{*} M_{24}$		$\overline{S}$ M	
	$+ C_{DL3}^{*} M_{26}\}C_{DU1}^{*}$		8 P	
			$\overline{Y}$	M_{PX} copies desired channel as determined by switch settings on control panel. M_{PX} will then telemeter desired channel to control panel or external equipment for display purposes.
	$+ C_{DL4}^{*} M_{30}$		9 R	
	$+ C_{DL5}^{*} M_{32}$		11 F	
	$+ C_{DL6}^{*} M_{34}$		22 H	
	$+ C_{DL7}^{*} M_{36}$		18 J	

Term	Equation	Receptacle	Pin No.	Definition
$_1M_{PX}$	(CONT)	J535	7	
	$\left\{ \begin{array}{l} C_{DL0}^{*}\ M_{40} \\ +C_{DL1}^{*}\ M_{42} \\ +C_{DL2}^{*}\ M_{44} \\ +C_{DL3}^{*}\ M_{46} \\ +C_{DL4}^{*}\ M_{50} \\ +C_{DL5}^{*}\ F_X \\ +C_{DL6}^{*}\ H_X \\ +C_{DL7}^{*}\ E_X \end{array} \right\} C_{DU2}^{*}$		35 T 34 16 $\overline{S}$ U 8 S 27 9 15 11 V 22 W 18 Z	M_{PX} copies desired channel as determined by switch settings on control panel. M_{PX} will then telemeter desired channel to control panel or external equipment for display purposes.
	$\left\{ \begin{array}{l} C_{DL0}^{*}\ U_X \\ C_{DL1}^{*}\ \begin{matrix} A_{XA} \\ [A_X] \end{matrix} \\ +C_{DL2}^{*}\ L_X \\ +C_{DL3}^{*}\ N_X \\ +C_{DL4}^{*}\ V_X \\ +C_{DL5}^{*}\ R_X \\ +C_{DL6}^{*}\ H_{MX} \\ +C_{DL7}^{*}\ E_{MX} \end{array} \right\} C_{DU3}^{*}$		35 B 34 C $\overline{S}$ K 8 14 A 9 10 11 13 22 23 18 19	M_{PX} copies desired channel as determined by switch settings on control panel. M_{PX} will then telemeter desired channel to control panel or external equipment for display purposes.
	$+C_{DC}^{*}\ I_X$		17 24	

Term	Equation	Receptacle	Pin No.	Definition
$_0M_{PX}$ =		J535	36	M_{PX} is a multiplex flip-flop and copies desired channel for display purposes.
	$\left\{ \begin{array}{l} C_{DL0}{}^{*} M_{0\,0}{}' \\ +C_{DL1}{}^{*} M_{0\,2}{}' \\ +C_{DL2}{}^{*} M_{0\,4}{}' \\ +C_{DL3}{}^{*} M_{0\,6}{}' \end{array} \right\} C_{DU0}{}^{*}$		35 $\overline{W}$	
			34 37	
			$\overline{S}$ 38	
			8 $\overline{P}$	
			1	M_{PX} copies desired channel as determined by switch settings on control panel. M_{PX} will then telemeter desired channel to control panel or external equipment for display purposes.
	$\left\{ \begin{array}{l} +C_{DL4}{}^{*} M_{10}{}' \\ +C_{DL5}{}^{*} M_{12}{}' \\ +C_{DL6}{}^{*} M_{14}{}' \\ +C_{DL7}{}^{*} M_{16}{}' \end{array} \right\} C_{DU0}{}^{*}$		9 39	
			11 40	
			22 41	
			18 42	
	$+\left\{ \begin{array}{l} C_{DL0}{}^{*} M_{20}{}' \\ +C_{DL1}{}^{*} M_{22}{}' \\ +C_{DL2}{}^{*} M_{24}{}' \\ +C_{DL3}{}^{*} M_{26}{}' \end{array} \right\} C_{DU1}{}^{*}$		35 $\overline{M}$	
			34 $\overline{L}$	
			$\overline{S}$ $\overline{N}$	
			8 $\overline{K}$	
			$\overline{Y}$	M_{PX} is a multiplex flip-flop and copies desired channel for display purposes.
	$+\left\{ \begin{array}{l} +C_{DL4}{}^{*} M_{30}{}' \\ +C_{DL5}{}^{*} M_{32}{}' \\ +C_{DL6}{}^{*} M_{34}{}' \\ +C_{DL7}{}^{*} M_{36}{}' \end{array} \right\} C_{DU1}{}^{*}$		9 $\overline{J}$	
			11 $\overline{V}$	
			22 $\overline{U}$	
			18 $\overline{T}$	

Term	Equation	Receptacle	Pin No.	Definition
$_0M_{PX}$	(CONT)	J535	36	
	$\left\{ C_{DL0}^{*} M_{40}' \right.$		35 $\overline{F}$	
	$+ C_{DL1}^{*} M_{42}'$		34 28	
	$+ C_{DL2}^{*} M_{44}'$		$\overline{S}$ $\overline{E}$	
	$+ C_{DL3}^{*} M_{46}' \left. \right\} C_{DU2}^{*}$		8 $\overline{H}$	
	$+ C_{DL4}^{*} M_{50}'$		27	M_{PX} copies desired channel as determined by switch settings on control panel. M_{PX} will then telemeter desired channel to control panel or external equipment for display purposes.
	$+ C_{DL5}^{*} F_X'$		9 29	
	$+ C_{DL6}^{*} H_X'$		11 $\overline{D}$	
	$+ C_{DL7}^{*} E_X' \left. \right\}$		22 $\overline{C}$	
	$\left\{ C_{DL0}^{*} U_X' \right.$		18 $\overline{B}$	
	$+ C_{DL1}^{*} [A_X^{A_{XA}}]'$		35 $\overline{X}$	
	$+ C_{DL2}^{*} L_X'$		34 43	
	$+ C_{DL3}^{*} N_X' \left. \right\} C_{DU3}^{*}$		$\overline{S}$ $\overline{R}$	
	$+ C_{DL4}^{*} V_X'$		8 30	
	$+ C_{DL5}^{*} R_X'$		A	M_{PX} copies desired channel as determined by switch settings on control panel. M_{PX} will then telemeter desired channel to control panel or external equipment for display purposes.
	$+ C_{DL6}^{*} H_{MX}'$		9 33	
	$+ C_{DL7}^{*} E_{MX}'$		11 31	
	$+ C_{DC}^{*} I_X'$		22 $\overline{A}$	
			18 26	
			17 25	

Term	Equation	Receptacle	Pin No.	Definition
$_1N_C$ =		J522	13	N_C is N register control flip-flop and breaks recirculation of N register when N_C is true.
	E_{FB} $[E\ N_D'\ T_X]$		P	One-sets N_C at first bit of Execute
$_0N_C$ =			31	N_C is N register control flip-flop and breaks recirculation of N register when N_C is true.
	T_{PA} $[T_P]$		D	Initializes N_C flip-flop
	$+ (K'\ V_C')^{N_L'}$		$\overline{C}$	Used during Noncompute and Nonload modes
$_1N_D$ =		J436	B	N_D checks for number agreement for operand sector with respect to word length of channel.
	$\left\{ \begin{array}{l} C_{B4}\ O_{B2} \\ + C_{B5}'\ C_{B2}'\ O_{B1} \\ + O_{B3}\ I_P' \\ \\ + O_{B3}\ C_{B5}'\ C_{B4}' \\ + O_{B3}\ C_{B5}'\ C_{B3}'\ C_{B2}' \end{array} \right\} D'\ [B_6\ B_3'\ T_P']^{T_{13}}$		12 4	Four-word disagreement (E, F, V, and R loops)
			6 E D	Eight-word disagreement (H loop)
			5 J	Channels 00 through 36
			2 C	Checks for number disagreement
			5 6 3	Channels 40 through 46
			5 6 A E	Channels 40 and 50
	$+ (E\ [D\ T_P])^{E_{TP}}$		F	One-sets N_D at T_P time during execution of multiword instructions
	$+ I_P'\ D'\ O_{B3}\ O_{B1}\ C_{B5}\ C_{B4}\ C_{B3}\ C_{B2}\ [B_5'\ B_4'\ B_2\ B_1']^{T_{24}'}$		J 2 5 D T 12 S 16 13	Used to force number disagreement when instruction is store and operand channel is 74 or 76

Term	Equation	Receptacle	Pin No.	Definition
$_0N_D$ =		J436	P	N_D checks for number agreement for operand sector with respect to word length of channel.
	$K I_P' D' O_{B3}' O_{B1}' [B_5' B_4' B_2 B_1']^{T_{24}}$		K J 2 L M 13	Used to force number agreement for X and specials
	$+ D' [B_5 B_4' B_3 B_2]^{T_{11}}$		2 39	Initializes prior to number agreement check
$_1N_P$ =		J420	$\overline{J}$	N_P inserts information from desired operand channel into N register and is used in A register. (Refer to A_{24} logic.)
	$[C_3' C_2' C_1'] M_{00}^{C_{L0}}$		17 H	
	$+ [C_3' C_2' C_1] M_{02}^{C_{L1}}$		22 F	
	$+ [C_3' C_2 C_1'] M_{04}^{C_{L2}}$		24 E	
	$+ [C_3' C_2 C_1] M_{06}^{C_{L3}}$		20 D	
	$N_C [C_5' C_4']^{C_{UO}}$		S 2	Copies information from desired channel as indicated by setting of C flip-flops and sector when N_C is one-set
	$+ [C_3 C_2' C_1'] M_{10}^{C_{L4}}$		28 B	
	$+ [C_3 C_2' C_1] M_{12}^{C_{L5}}$		$\overline{Y}$ 4	
	$+ [C_3 C_2 C_1'] M_{14}^{C_{L6}}$		$\overline{B}$ C	
	$+ [C_3 C_2 C_1] M_{16}^{C_{L7}}$		U 3	

Term	Equation	Receptacle	Pin No.	Definition
$_1N_P$	(CONT)	J420	$\overline{J}$	
	$+\left\{\begin{array}{l} C_{L0}\,[C_3'\,C_2'\,C_1']\,M_{20} \\ +\,C_{L1}\,[C_3'\,C_2'\,C_1]\,M_{22} \\ +\,C_{L2}\,[C_3'\,C_2\,C_1']\,M_{24} \\ +\,C_{L3}\,[C_3'\,C_2\,C_1]\,M_{26} \\ +\,C_{L4}\,[C_3\,C_2'\,C_1']\,M_{30} \\ +\,C_{L5}\,[C_3\,C_2'\,C_1]\,M_{32} \\ +\,C_{L6}\,[C_3\,C_2\,C_1']\,M_{34} \\ +\,C_{L7}\,[C_3\,C_2\,C_1]\,M_{36} \end{array}\right\} N_C\,C_{UI}\,[C_5'\,C_4]$		17 7	
			22 8	
			24 J	
			20 L	
			S 12	Copies information from desired channel as indicated by setting of C flip-flops and sector when N_C is one-set
			28 11	
			$\overline{Y}$ 10	
			$\overline{B}$ M	
			U N	

Term	Equation	Receptacle	Pin No.	Definition
$_1N_P$	(CONT)	J420	$\overline{J}$	
	C_{L0} $[C_3' C_2' C_1'] M_{40}$		17 18	
	$+ C_{L1}$ $[C_3' C_2' C_1] M_{42}$		22 Z	
	$+ C_{L2}$ $[C_3' C_2 C_1'] M_{44}$		24 Y	
	$+ C_{L3}$ $[C_3' C_2 C_1] M_{46}$		20 $\overline{A}$	
	$+ N_C [C_5 C_4'] C_{U2}$		S T	Copies information from desired channel as indicated by setting of C flip-flops and sector when N_C is one-set
	$+ C_{L4}$ $[C_3 C_2' C_1'] M_{50}$		28 W	
	$+ C_{L5}$ $[C_3 C_2' C_1] F_X$		$\overline{Y}$ 16	
	$+ C_{L6}$ $[C_3 C_2 C_1'] H_X$		$\overline{B}$ X	
	$+ C_{L7}$ $[C_3 C_2 C_1] E_X$		U V	

Term	Equation	Receptacle	Pin No.	Definition
$_1N_P$	(CONT)	J420	$\overline{J}$	
	$\left\{ \begin{array}{l} C_{L0} \\ [C_3' C_2' C_1'] U_X \\ C_{L1} \\ +[C_3' C_2' C_1] A_X \\ C_{L2} \\ +[C_3' C_2 C_1'] L_X \\ C_{L3} \\ +[C_3' C_2 C_1] N_X \\ \\ \\ \\ C_{L4} \\ +[C_3 C_2' C_1'] V_X V_K' \\ C_{L5} \\ +[C_3 C_2' C_1] R_X R_K' \\ C_{L6} \\ +[C_3 C_2 C_1'] H_{MX} \\ C_{L7} \\ +[C_3 C_2 C_1] E_{MX} \end{array} \right\} (N_C C_5 C_4)^{N_{CU3}}$		17 21	
			22 23	
			24 $\overline{L}$	
			20 27	
			$\overline{K}$	Copies information from desired channel as indicated by setting of C flip-flops and sector when N_C is one-set
			28 $\overline{C}$ $\overline{D}$	
			$\overline{Y}$ $\overline{E}$ $\overline{H}$	
			$\overline{B}$ 19	
			U $\overline{F}$	
	$+(N_C C_5 C_4)^{N_{CU3}} [C_3 C_2' C_1'] V_X' V_K^{C_{L4}}$		$\overline{K}$ 28 $\overline{V}$ $\overline{U}$	Copies V or R loops inversely into N_P when V_K or R_K is one-set
	$+(N_C C_5 C_4)^{N_{CU3}} [C_3 C_2' C_1] R_X' R_K^{C_{L5}}$		$\overline{K}$ $\overline{Y}$ $\overline{X}$ $\overline{W}$	

Term	Equation	Receptacle	Pin No.	Definition
$_1N_P$	(CONT)	J420	$\overline{J}$	
	$+N_C' N_X T_X'$		29 27 $\overline{M}$	Recirculation
	$+N_X' T_X$		$\overline{R}$ 30	Inversion type AGC information
$_0N_P$ =		J421	I	N_P inserts information from desired operand channel into N register and is used in A register. (Refer to A_{24} logic.)
	$\left\{ \begin{array}{l} C_{L0} \\ [C_3' C_2' C_1'] M_{00}' \end{array} \right.$		C 3	
	$\left. \begin{array}{l} C_{L1} \\ +[C_3' C_2' C_1] M_{02}' \end{array} \right.$		D 4	
	$\left. \begin{array}{l} C_{L2} \\ +[C_3' C_2 C_1'] M_{04}' \end{array} \right.$		F E	
	$\left. \begin{array}{l} C_{L3} \\ +[C_3' C_2 C_1] M_{06}' \end{array} \right.$		17 H	
	$\left. \begin{array}{l} \\ \end{array} \right\} N_C [C_5' C_4']^{C_{U0}}$		2 A	Copies information from desired channel as indicated by setting of C flip-flops and sector when N_C is one-set
	$\left. \begin{array}{l} C_{L4} \\ +[C_3 C_2' C_1'] M_{10}' \end{array} \right.$		20 J	
	$\left. \begin{array}{l} C_{L5} \\ +[C_3 C_2' C_1] M_{12}' \end{array} \right.$		22 K	
	$\left. \begin{array}{l} C_{L6} \\ +[C_3 C_2 C_1'] M_{14}' \end{array} \right.$		25 L	
	$\left. \begin{array}{l} C_{L7} \\ +[C_3 C_2 C_1] M_{16}' \end{array} \right\}$		S M	

Term	Equation	Receptacle	Pin No.	Definition
$_0N_P$	(CONT)	J421	1	
	$\left\{ \begin{array}{l} C_{L0} \\ [C_3' C_2' C_1'] M_{20}' \end{array} \right.$		C 11	
	$\begin{array}{l} C_{L1} \\ +[C_3' C_2' C_1] M_{22}' \end{array}$		D 10	
	$\begin{array}{l} C_{L2} \\ +[C_3' C_2 C_1'] M_{24}' \end{array}$		F 9	
	$\begin{array}{l} C_{L3} \\ +[C_3' C_2 C_1] M_{26}' \end{array}$		17 5	
	$+ \left\{ \begin{array}{l} \\ \end{array} \right\} N_C \overset{C_{U1}}{[C_5' C_4]}$		2 B	Copies information from desired channel as indicated by setting of C flip-flops and sector when N_C is one-set
	$\begin{array}{l} C_{L4} \\ +[C_3 C_2' C_1'] M_{30}' \end{array}$		20 6	
	$\begin{array}{l} C_{L5} \\ +[C_3 C_2' C_1] M_{32}' \end{array}$		22 8	
	$\begin{array}{l} C_{L6} \\ +[C_3 C_2 C_1'] M_{34}' \end{array}$		25 7	
	$\begin{array}{l} C_{L7} \\ +[C_3 C_2 C_1] M_{36}' \end{array} \right\}$		S P	

Term	Equation	Receptacle	Pin No.	Definition
$_0N_P$	(CONT)	J421	1	
	$\left\{ \begin{array}{l} C_{L0} \\ [C_3' C_2' C_1'] M_{40}' \\ C_{L1} \\ +[C_3' C_2' C_1] M_{42}' \\ C_{L2} \\ +[C_3' C_2 C_1'] M_{44}' \\ C_{L3} \\ +[C_3' C_2 C_1] M_{46}' \\ \\ \\ C_{L4} \\ +[C_3 C_2' C_1'] M_{50}' \\ C_{L5} \\ +[C_3 C_2' C_1] F_X' \\ C_{L6} \\ +[C_3 C_2 C_1'] H_X' \\ C_{L7} \\ +[C_3 C_2 C_1] E_X' \end{array} \right\} \cdot \begin{array}{l} C_{U2} \\ N_C [C_5 C_4'] \end{array}$		C U	
			D 15	
			F 16	
			17 18	
			2 13	Copies information from desired channel as indicated by setting of C flip-flops and sector when N_C is one-set.
			20 19	
			22 23	
			25 24	
			S T	

Term	Equation	Receptacle	Pin No.	Definition
0^{N_P}	(CONT)	J421	1	
	$\left\{ \begin{array}{l} [C_3' C_2' C_1'] U_X' \\ + [C_3' C_2' C_1] A_X' \\ + [C_3' C_2 C_1'] L_X' \\ + [C_3' C_2 C_1] N_X'' \\ + \\ + [C_3 C_2' C_1'] V_X' V_K' \\ + [C_3 C_2' C_1] R_X' R_K' \\ + [C_3 C_2 C_1'] H_{MX}' \\ + [C_3 C_2 C_1] E_{MX}' \end{array} \right\} \begin{array}{l} C_{L0} \\ C_{L1} \\ C_{L2} \\ C_{L33} \\ \\ C_{L4} \\ C_{L5} \\ C_{L6} \\ C_{L7} \end{array} \left(N_C C_5 C_4\right)^{N_{CU3}}$		C V D $\overline{F}$ F $\overline{E}$ 17 $\overline{D}$ $\overline{H}$ 20 $\overline{C}$ $\overline{B}$ 22 $\overline{A}$ Z 25 X S W	Copies information from desired channel as indicated by setting of C flip-flops and sector when N_C is one-set
	$+ \left(N_C C_5 C_4\right)^{N_{CU3}} [C_3 C_2' C_1'] V_X V_K^{C_{L4}}$		$\overline{H}$ 20 31 32	Copies V or R loop inversely into N_P when V_K is one-set
	$+ \left(N_C C_5 C_4\right)^{N_{CU3}} [C_3 C_2' C_1] R_X R_K^{C_{L5}}$		$\overline{H}$ 22 $\overline{J}$ $\overline{K}$	
	$+ N_C'' N_{XX}'' T_X''$		33 $\overline{D}$ 28	Recirculation
	$+ N_X T_X$		29 30	Inversion type AGC information

Term	Equation	Receptacle	Pin No.	Definition
$1^{N_{24W}}$ =		J525	$\overline{W}$	N_{24W} is a N register write amplifier.
	$N_P D$		41 $\overline{N}$	Recirculates during D mode
	$+ S D'$		39 $\overline{P}$	Copies sector during D mode
$0^{N_{24W}}$ =			$\overline{L}$	N_{24W} is a N register write amplifier.
	$N_P' D$		34 $\overline{N}$	Recirculates during D mode
	$+ S' D'$		40 $\overline{P}$	Copies sector during D' mode
$1^{O_{B3}}$ =			$\overline{Y}$	O_{B3} is an operation buffer flip-flop and checks agreement of I_P and S during operand sector and sector of next instruction.
	$B_4 I_P S'$		$\overline{T}$ 38 40	Comparison for sector agreement
	$+ B_4 I_P' S$		$\overline{T}\,\overline{U}$ 39	Comparison for sector agreement
	$+ I_P [B_6 B_4' B_3]^{B_{6MI}}$		38 $\overline{S}$	Loads Operation code during T_{21} through T_{24}
$0^{O_{B3}}$ =			32	O_{B3} is an operation buffer flip-flop and checks agreement of I_P and S during operand sector and sector of next instruction.
	$I_P' [B_6 B_4' B_3]^{B_{6MI}}$		$\overline{U}\,\overline{S}$	Loads Operation code during T_{21} through T_{24}
	$+ (B_6 B_3')^{T_{EH}}$		$\overline{M}$	T_P and T_{13}

Term	Equation	Receptacle	Pin No.	Definition
1^{O}_{B2} =		J525	29	O_{B2} is an operation buffer flip-flop and instruction and numbe agreement flip-flop.
	$\left\{ \begin{array}{l} \overset{T_4}{([B_6' B_5][B_2 B_1'])} \\ + C_{P1} \overset{T_{17}}{([B_6 B_5' B_4][B_2' B_1])} \\ \\ C_{P1}' \overset{T_{18}}{([B_6 B_5' B_4][B_2' B_1'])} \\ + \overset{T_{24}}{[B_5' B_4' B_2 B_1']} \end{array} \right\} O_{B3}$		$\overline{H}$	Four-word disagreement for operand sector
			$\overline{E}\,\overline{F}$	Eight-word disagreement for sector of next instruction
			S	
			$\overline{J}\,V$	Sixteen-word disagreement for sector of next instruction
			33	Loads Operation code
0^{O}_{B2} =			$\overline{V}$	O_{B2} is an operation buffer flip-flop and instruction and number agreement flip-flop.
	$O_{B3}' \overset{T_{24}}{[B_5' B_4' B_2 B_1']}$		42 33	Loads Operation code
	$+ \overset{T_{EH}}{(B_6 B_3')}$		$\overline{M}$	T_P and T_{13}
1^{O}_{B1} =			U	O_{B1} is an operation buffer flip-flop, and instruction and number agreement flip-flop.

Term	Equation	Receptacle	Pin No.	Definition
$_1O_{B1}$	(CONT)	J525		
	$\left\{ \begin{array}{l} \overset{T_5}{([B_6' B_5'] B_4 [B_2' B_1])} \\ + \overset{T_{18}}{([B_6 B_5' B_4] [B_2' B_1'])} \\ \\ + \overset{T_{23}}{([B_4' B_3 B_2] B_5' B_1)} \\ + \overset{T_{21}}{I_P' ([B_6 B_4' B_3] [B_2' B_1])} \end{array} \right\} O_{B3}$		W	Eight-word disagreement for operand number agreement
			V	Sixteen-word disagreement for cold storage when instruction is flagged
			S	
			Y	Operation code loading.
			$\overline{U}$ 36	When instruction is not flagged, 128-word disagreement for cold storage
$_0O_{B1}$ =			$\overline{K}$	O_{B1} is an operation buffer flip-flop, and instruction and number agreement flip-flop.
	$\overset{T_{XA}}{[T_X]}$		35	Initializes prior to operand number agreement check
	$+ \overset{B_{LU7}}{[B_6 B_5 B_4]}$		26	T_{14}, T_{15}, and T_{16}
	$+ \overset{T_{22}}{([B_6 B_4' B_3] [B_2' B_1'])}$		$\overline{R}$	Initializes prior to Operation code Loading
$_1O_4$ =		J424	$\overline{Y}$	O_4 is an Operation code flip-flop during Compute and mode control during Noncompute.
	$I_P \overset{K_{DP}}{([K]_A [D' T_P])}$		38 37	Loads new Operation code at last bit of Execute or last bit of Operand Search

Term	Equation	Receptacle	Pin No.	Definition
$_1O_4$	(CONT)	J424	$\overline{Y}$	
	$\left\{ \begin{array}{l} C_{P5}' \left([B_6\ B_5'\ B_4]\ [B_2\ B_1'] \right)^{T_{20}} \\ + C_{P5}\ C_{P4}'\ T_O \end{array} \right\} \left([K'\ V_C]\ R_C' \right)^{N_{LRC}'}$		41 $\overline{W}$	Initiates actual parity check time
			$\overline{X}$	Used during Noncompute Load mode
			39 40 $\overline{V}$	Turns O_4 on to control shifting of C_P flip-flops
	$+ \left([K]_A\ O_4'\ O_2\ [O_3'\ O_1']\ [T_X]_A \right)^{O_{CX}}\ A_{24}$		36 35	Modifies Operation code from TMI to TRA if A register is negative
	$+ [K'\ V_C'\ R_C'\ J]\ O_1'\ O_2\ S\ [B_5'\ B_4'\ B_2\ B_1']^{N_{MH}\ T_{24}}$		$\overline{T}\ \overline{U}\ \overline{S}\ \overline{R}\ \overline{P}$	Turns on O_4 every other revolution at sector 176
$_0O_4$ =			29	O_4 is an Operation code flip-flop during Compute and mode control during Noncompute
	$I_P' \left([K]_A\ [D'\ T_P] \right)^{K_{DP}}$		34 37	Loads new Operation code at last bit of Execute or last bit of Operand Search
	$+ [K'\ J']\ [B_5'\ B_4'\ B_2\ B_1']^{N_J'\ T_{24}}$		$\overline{N}\ \overline{P}$	Noncompute in Sample mode or Parity mode, Process of Load mode, or Program Halt of Nonload
	$+ \left\{ \begin{array}{l} I_M^* \\ + S_{B2}'\ K_H'^* \end{array} \right\} [K'\ V_C'\ R_C'\ J]^{N_{MH}}\ O_2\ T_O$		$\overline{K}$	Resets O_4
			$\overline{T}\ \overline{S}\ \overline{V}$	
			$\overline{L}\ \overline{M}$	Enters Compute mode if COMPUTE switch is not at HALT and a parity or verify error does not exist
	$+ \left([K'\ V_C]\ J\ R_C' \right)^{N_W}\ S_{B2}\ T_X$		32 33 31	Parity error has been detected during parity check which produces manual Halt mode

Term	Equation	Receptacle	Pin No.	Definition
$_1O_3$ =		J423	30	O_3 is an Operation code flip-flop during Compute mode and mode control during Noncompute mode.
	$O_{B3}\ \left([K]_A [D' T_P]\right)^{K_{DP}}$		$\bar{A}\ \bar{B}$	Loads new Operation code at last bit of Execute or last bit of Operand Search
	$+ \left([K' J'] V_C R_C' C_{P5} C_{P4}\right)^{N_{PC}} \left(C_{P3}' C_{P2} C_{P1}\right)^{C_{PL3}}{}' T_P$		$\bar{E}\ F\ \bar{P}$	Initiates Verify code at T_P time of Process code
$_0O_3$ =			29	O_3 is an Operation code flip-flop during Compute mode and mode control during Noncompute mode.
	$O_{B3}'\ \left([K]_A [D' T_P]\right)^{K_{DP}}$		$\bar{D}\ \bar{B}$	Loads new Operation code at last bit of Execute or last bit of Operand Search
	$+ \left([K' J'] V_C R_C' C_{P5} C_{P4}\right)^{N_{PC}} \left(C_{P3}' C_{P2} C_{P1}'\right)^{C_{PL2}} T_P$		$\bar{E}\ J\ \bar{P}$	Fills code at T_P time of Process code
$_1O_2$ =		J420	25	O_2 is an Operation code flip-flop during Compute; Add/Subtract indicator during words 2 through 13 of Multiply, and mode control during Noncompute mode.
	$O_{B2}\ \left([K]_A [D' T_P]\right)^{K_{DP}}$		32 31	Loads new Operation code at last bit of Execute or last bit of Operand Search
	$+ [K Q O_4' O_3]\ J\ L_X^{O_{MO}}$		$\bar{N}\ \bar{P}\ \bar{L}$	During Multiply, makes decision to Subtract
	$+ [K' J']^{N_J'}$		33	Ensures that proper mode is entered going from Program Halt to manual Halt mode
	$+ [K' V_C' R_C' J]\ O_4 O_2' T'^{N_{MH}}$ *		36 35 34 26	Submode control during manual Halt mode; causes transiton from prepare to Load to interlock

Term	Equation	Receptacle	Pin No.	Definition
$_0O_2$ =		J420	43	O_2 is an Operation code flip-flop during Compute; Add/Subtract indicator during words 2 through 13 of Multiply, and mode control during Noncompute mode.
	$O_{B2}' \left([K]_A [D' T_P]\right)$		$\bar{S}$ 31	Loads new Operation code at last bit of Execute or last bit of Operand Search
	$+ [K Q O_4' O_3] J L_X'$		$\bar{N} \bar{P} \bar{T}$	During Multiply, makes decision to Add
	$+ \left\{ \begin{matrix} O_4' S_{B2}' K_H' * \\ + O_4 O_2 O_1 \end{matrix} \right\} [K' V_C' R_C' J] [B_5' B_4' B_2 B_1']$		39 40 41	Submode control during manual Halt mode; causes transition from either Idle 1 or Idle 2 to prepare to Compute.
			36 42	
			35 38 37	Submode control during manual Halt mode; causes transition from interlock to prepare to Load to interlock
$_1O_1$ =		J421	36	O_1 is an Operation code flip-flop during Compute mode, and mode control during Noncompute mode.
	$O_{B1} \left([K]_A [D' T_P]\right)$		$\bar{Y} \bar{W}$	Loads new Operation code at last bit of Execute or last bit of Operand Search mode
	$+ (K' V_C') J O_1' S (B_6 B_3') B_5'$		$\bar{U}$ 37 $\bar{S}$ 40 39 38	Provides a 10-millisecond delay to allow M_R* to drop off during synchronization. Also is effective during manual Halt mode.
$_0O_1$ =			$\bar{V}$	O_1 is an Operation code flip-flop during Compute mode, and mode control during Noncompute mode.
	$O_{B1}' \left([K]_A [D' T_P]\right)$		$\bar{X} \bar{W}$	Loads new Operation code at last bit of Execute or last bit of Operand Search modes
	$+ (K' V_C') O_4' O_1 S (B_6 B_3') B_5'$		$\bar{U} \bar{T}$ 41 40 39 38	Provides a 10-millisecond delay to allow M_R* to drop off during synchronization. Also is effective during manual Halt mode

Term	Equation	Receptacle	Pin No.	Definition
$_1P_3$ =		J423	40	P_3 is a phase register flip-flop and carry/borrow flip-flop during Fine Countdown mode.
	$\left([K E O_4 O_3' O_2' O_1'] [B_6' B_5' B_3] C_5 C_4 C_3\right) I_X^{O_{XPR}}$		$\bar{H}\,\bar{X}$	$(O_4 O_3' O_2' O_1' = 40; [B_6' B_5' B_3'] = T_1$ through T_5; $C_5 C_4 C_3 = 7$; $I_X = 2) = 40XX7020$ = LPR; copies the state of I_X at T_5 into P_3
	$+\left\{\begin{matrix} V_S' U_X \\ \\ + V_S U_X' \end{matrix}\right\} V_X F_C [T_P' T_X' T_O']^{T_{PXO}'}$		$\bar{T}$ 35	One-sets P_3 adding a one to one
			32 $\bar{R}\,\bar{N}$	P_3 acts as carry/borrow during Fine Countdown mode for integration of V with U loops.
			$\bar{U}\,\bar{S}$	One-sets P_3; subtracts a one from a zero
$_0P_3$ =			31	P_3 is a phase register flip-flop and carry/borrow flip-flop during Fine Countdown mode.
	$\left([K E O_4 O_3' O_2' O_1'] [B_6' B_5' B_3] C_5 C_4 C_3\right) I_X'^{O_{XPR}}$		$\bar{H}$ 42	$(O_4 O_3' O_2' O_1' = 40; [B_6' B_5' B_3'] = T_1$ through T_5; $C_5 C_4 C_3 = 7; I_X' = 0) = 40XX7000$ - LPR; copies state of I_X at T_5 into P_3
	$+\left\{\begin{matrix} V_S' U_X' \\ \\ V_S U_X \end{matrix}\right\} V_X' F_C$		$\bar{T}\,\bar{S}$	Turns off P_3 if on. Adds a zero to zero
			41 $\bar{R}$	P_3 acts as carry/borrow during Fine Countdown mode for integration of V with U loops.
			$\bar{U}$ 35	Turns off P_3 if on. Subtracts a zero from one
	$+ F_C T_P$		$\bar{R}\,\bar{P}$	Initializes P_3 prior to integration of V to U loops
	$+ [K' V_C' R_C]^{N_{RS}}$		36	Initializes phase register during synchronization

Term	Equation	Receptacle	Pin No.	Definition
$_1P_2$ =		J421	27	P_2 is a phase register flip-flop.
	O_{XPR} $([K E O_4 O_3' O_2' O_1'] [B_6' B_5' B_3] C_5 C_4 C_3) C_2$		35 $\overline{R}$	$(O_4 O_3' O_2' O_1' = 40; [B_6' B_5' B_3] = T_1$ through T_5; $C_5 C_4 C_3 = 7; C_2 = 4) = 40XX7400 =$ LPR; copies state of C_2 into P_2. C_2 contains T_9 information of the instruction.
$_0P_2$ =			26	P_2 is a phase register flip-flop.
	O_{XPR} $([K E O_4 O_3' O_2' O_1'] [B_6' B_5' B_3] C_5 C_4 C_3) C_2'$		35 $\overline{L}$	$(O_4 O_3' O_2' O_1' = 40; [B_6' B_5' B_3] = T_1$ through T_5; $C_5 C_4 C_3 = 7; C_2 = 0) = 40XX7000 =$ LPR; copies state of C_2 into P_2. C_2 contains T_9 information of the instruction.
	N_{RS} + $[K' V_C' R_C]$		$\overline{M}$	Initializes phase register during synchronization
$_1P_1$ =			42	P_1 is a phase register flip-flop.
	O_{XPR} $([K E O_4 O_3' O_2' O_1'] [B_6' B_5' B_3] C_5 C_4 C_3) C_1$		35 $\overline{P}$	$(O_4 O_3' O_2' O_1' = 40; [B_6' B_5' B_3] = T_1$ through T_5; $C_5 C_4 C_3 = 7; C_1 = 2) = 40XX7200 =$ LPR; copies state of C_1 into P_1. C_1 contains T_8 information of the instruction.
$_0P_1$ =			43	P_1 is a phase register flip-flop.
	O_{XPR} $([K E O_4 O_3' O_2' O_1'] [B_6' B_5' B_3] C_5 C_4 C_3) C_1'$		35 $\overline{N}$	$(O_4 O_3' O_2' O_1' = 40; [B_6 B_5' B_3] = T_1$ through T_5; $C_5 C_4 C_3 = 7; C_1' = 0) = 40XX7000 =$ LPR; copies state of C_1 into P_1. C_1 contains T_8 information of the instruction.
	N_{RS} + $[K' V_C' R_C]$		$\overline{M}$	Initializes phase register during synchronization

Term	Equation	Receptacle	Pin No.	Definition
$_1Q$ =		J429	$\bar{V}$	Q is a control flip-flop for multiword executions.
	$(E [D T_P]) N_D^{E_{TP}}$		$\bar{W}\ \bar{U}$	One-sets Q at T_P of first word of Execute
	$+ [K' V_C] (C_{B2}' C_{B1}') N_D' [D' T_P] E'^{N_L\ C_{B21}'\ D_{TP}'}$		39 40 $\bar{U}$ 38 37	One-sets Q to provide a two-word delay for writing into channel 50
$_0Q$ =			$\bar{H}$	Q is a control flip-flop for multiword executions.
	$E [D' T_P]^{D_{TP}'}$		$\bar{M}$ 38	Zero-sets Q at last bit of Execute
	$+ [K' V_C] (C_{B2}' C_{B1}') (N_D [D T_P])^{N_L\ C_{B21}'\ E_{OP}}$		39 40 $\bar{J}$	Zero-sets Q after two words so writing may take place into channel 50
	$+ ([K' J'] V_C')^{N_{ENT}}$		$\bar{L}$	Initializes Q during synchronization
$_1R_C$ =		J431	$\bar{W}$	R_C is R register interrupt control flip-flop and mode control during Noncompute mode.
	$(O_3' O_2 O_1 E) K (Q' C_{B5} C_{B3} [T_X]_A) C_{B4} C_{B2}'^{*} C_{B1}^{O_P\ C_{B53}}$		$\bar{P}\ \bar{N}\ \bar{M}$ 42 41 $\bar{X}$	Stores A register into R loop
	$+ [K' V_C] J T^{*} [B_5 B_4' B_3 B_2]^{N_L\ T_{11}}$		43 34 $\bar{Y}$ $\bar{V}$	Initiates Prepare to Sample submode of Load mode. T indicates a character is available. T may be always true on a photo reader.
	$+ M_R^{*}$		36	Master reset
$_0R_C$ =			39	R_C is R register interrupt control flip-flop and mode control during Noncompute mode.
	$([K]_A [T_P]_B)^{K_{TP}}$		40	Resets R_C to zero each T_P of Compute

Term	Equation	Receptacle	Pin No.	Definition
$_0R_C$	(CONT)	J431	39	
	$+ [K' V_C] T'^{N_L} * [B_6 B_3' T_P']^{T_{13}}$		43 37 P	Initiates the Wait mode. T' indicates a character is not available.
	$+ [K' V_C' R_C] J S (B_6 B_3')^{N_{RS}} B_5' O_1^{T_{EH}}$		33 34 35 $\overline{T}$ $\overline{S}$ $\overline{R}$	Initiates manual Halt mode from Sync Bit Counter 2 submode
$_1R_K$ =	(For D17B Part No. 58599-501-11, -41, -61, and -81 only)		U	R_K samples resolver inputs into R loop coarse time pulse and is used for resolver decoding as a change indicator.
	$I_{4B}^{W_3} * (W_B W_A)^{T_{PB}} [T_P]$		10 6 23	Samples I_{4B} at T_P of sectors 2, 6, 12, 16, etc. for phase B of resolver inputs
	$+ \{ I_{11}^{T_{OA}} * [T_O] + I_{14}^{T_2} * ([B_6' B_5' B_3'] [B_2' B_1']) \}^{W_1} (W_B' W_A)$		L M W X	Variable incremental inputs of ±1 or ±4 for right-half word of sector 1 or R loop
	$+ \{ I_{31}^{T_{13}} * [B_6' B_3' T_P'] + I_{34}^{T_{15}} * ([B_6 B_5 B_4] B_1) \}^{W_1} (W_B' W_A)$		T	T_{23} of sector 0 through T_{20} of sector 1, etc.
			N P $\overline{A}$ 22	Variable incremental inputs of ±1 or ±4 for left-half word of sector 1 of R loop
	$+ \{ R_S' R_X \}^{W_{BB3}'} T_P' (W_B B_3')$		28 $\overline{J}$	During resolver decoding, if R_S and R_X do not agree, there is a change. One-sets R_K.
			31 $\overline{H}$	T_X, T_O, and T_{12}, T_{13} of sectors 2 and 3, 6 and 7, etc.
	$+ \{ R_S R_X \}^{W_{BB3}'} T_P' (W_B B_3')$		29 $\overline{C}$	During resolver decoding, if R_S and R_X do not agree, there is a change. One-sets R_K.

Term	Equation	Receptacle	Pin No.	Definition
1^{R_K}	(CONT)	J431	U	
	$+ I_7^* \left(W_B' W_A'\right)^{W_O} [T_P]^{T_{PB}}$		24 25 23	L_7 is coarse time pulse sampled at T_P of sectors 177, 3, 7, or 13, etc.
	$+ R_X \left(W_B' W_A'\right)^{W_O} B_6' B_3' T_O'$		$\overline{J}$ 25 19 18 16	$(W_O B_6' B_3' T_O') = T_X$ and T_{12} of sectors 0, 4, 10, 14, etc. Used for initiating a change into coarse time counter and/or fine time counter.
R_K	= (For D17B, Part No. 56599-501-21, -101, and -111 only'		U	R_K samples resolver inputs into R loop coarse time pulse and is used for resolver decoding as a change indicator.
	$I_{4B}^* \left(W_B W_A\right)^{W_3} [T_P]^{T_{PB}}$		10 6 23	Samples I_{4B} at T_P of sectors 2, 6, 12, 16, etc. for phase B of resolver inputs
	$+ \left\{ \begin{matrix} [T_O] \\ T_{13} \\ [B_6 B_3' T_P'] \end{matrix} \right\}^{T_{OA}} \left(W_B' W_A\right)^{W_1}$		M	Variable incremental input of ±1 or ±4 for right-half word of sector 1 or R loop
			T	T_{23} of sector 0 through T_{20} of sector 1, etc.
			P	Variable incremental input of ±1 or ±4 for left-half word of sector 1 of R loop
	$+ \left\{ \begin{matrix} R_S' R_X \\ \\ \\ R_S R_X' \end{matrix} \right\} T_P' \left(W_B B_3'\right)^{W_{BB3}}$		28 $\overline{J}$	During resolver decoding, if R_S and R_X do not agree, there is a change. One-sets R_K.
			31 $\overline{H}$	T_X, T_O, and T_{12}, T_{13} of sectors 2 and 3, 6 and 7, etc.
			29 $\overline{C}$	During resolver decoding, if R_S and R_X do not agree, there is a change. One-sets R_K.
	$+ I_7^* \left(W_B' W_A'\right)^{W_O} [T_P]^{T_{PB}}$		24 25 23	L_7 is coarse time pulse sampled at T_P of sectors 177, 3, 7, or 13, etc.
	$+ R_X \left(W_B' W_A'\right)^{W_O} B_6' B_3' T_O'$		$\overline{J}$ 25 19 18 16	$(W_O B_6' B_3' T_O') = T_X$ and T_{12} of sectors 0, 4, 10, 14, etc. Used for initiating a change into coarse time counter and/or fine time counter.

Term	Equation	Receptacle	Pin No.	Definition
0^{R_K} =			$\overline{K}$	R_K samples resolver inputs into R loop coarse time pulse and is used for resolver decoding as a change indicator.
	$\{R_C' R_X' R_S'$		30 $\overline{C}$ 28	During addition, turns off carry for resolver inputs
	$+ R_C' R_X R_S$		30 $\overline{J}$ 29	During subtraction, turns off borrow for resolver inputs
	$\}B_3 R_K$		$\overline{L}$ 32	
	$+ R_C [A_X^{A_X' A}] R_S'$		27 $\overline{E}$ 28	Same as previous equation for O^{R_K} except at this time, A register is being stored into R loop.
	$+ R_C [A_X^{A_{XA}}] R_S$		27 $\overline{F}$ 29	
	$+ [B_5' B_4' B_3 B_2]^{T_{11}}$		$\overline{V}$	Initializes prior to sampling inputs
	$+ [B_5' B_4' B_2 B_1']^{T_{24}}$		$\overline{U}$	Initializes prior to sampling inputs
	$+\{R_S' R_X'\}^{W_{BB3}'} T_P' (W_B B_3')$		28 $\overline{C}$	During resolver decoding, R_S and R_X agree; no change; then zero-set R_K
			31 $\overline{H}$	T_X, T_O, and T_{12}, T_{13} of sectors 2 and 3, 6 and 7, etc.
	$+ R_S R_X\}$		29 $\overline{J}$	During resolver decoding, R_S and R_X agree; no change; then zero-set R_K

Term	Equation	Receptacle	Pin No.	Definition
$_0R_K$	(CONT)	J431	$\overline{K}$	
	$+ R_X' (W_B' W_A') B_6' B_3' T_O'^{W_O}$		$\overline{C}$ 25 19 18 16	$(W_O B_6' B_3' T_O') = T_X$ and T_{12} of sectors 0, 4, 10, 14, etc. No change for coarse time counter and/or fine time counter
$_1R_P$ =		J521	34	R_P is R loop write amplifier and Add/Subtract for resolver inputs.
	$\{R_C' R_X R_K'$		38 $\overline{N}$ $\overline{T}$	Addition/subtraction logic for resolver inputs
	$+ R_C' R_X' R_K\}B_3 R_T'$		38 36 37	
			$\overline{J}$ $\overline{K}$	
	$+ R_C A_X R_K'$		$\overline{R}$ $\overline{P}$ $\overline{T}$	Addition/subtraction logic for resolver inputs during execution of storing A register into R loop (R_C)
	$+ R_C A_X' R_K$		$\overline{R}$ $\overline{S}$ 37	
	$+ R_S (W_B B_3)'^{W_{BB3}'}$		$\overline{L}$ $\overline{M}$	Copies present resolver inputs into memory for use four words later
	$+ R_X' W_B' (B_3' B_2)^{T_{12}}$		36 40 39	Copies R_X inversely into R_P to provide a reference for fine time counter so it will count only one each eight words
	$+ R_K R_X' W_B' [T_X]^{T_{XA}}$		37 36 40 25	Provides a reference for coarse time counter so pulse can be sampled only once every eight words
	$+ R_T [B_5' B_4' B_2 B_1']^{T_{24}}$		35 10	Forces maximum negative number into left-half word of sector 0 of R loop (4000/1) when a coarse time pulse is accepted into computer

Term	Equation	Receptacle	Pin No.	Definition
$_0R_P$ =		J521	43	R_P is R loop write amplifier and Add/Subtract for resolver inputs.
	$\left\{ \begin{array}{l} R_C' R_X' R_K' \\ + R_C' R_X R_K \\ \\ \\ + R_C A_X' R_K' \\ + R_C A_X R_K \end{array} \right\} B_3 R_T'$		38 36 $\overline{T}$ 38 $\overline{11}$ 37 $\overline{J}$ $\overline{K}$ $\overline{R}$ $\overline{S}$ $\overline{T}$ $\overline{R}$ $\overline{P}$ 37	Addition/subtraction logic for resolver inputs Addition/subtraction logic for resolver inputs during execution of storing A register into R loop (R_C)
	$+ R_S' \left(W_{BB3}' W_B B_3' \right)$		$\overline{V.M}$	Copies present resolver inputs into memory for use four words later
	$+ R_X W_B' \left(B_3' B_2 \right)^{T_{12}}$		$\overline{N}$ 40 39	Copies R_X inversely into R_P to provide a reference for fine time counter so it will count only one each eight words
	$+ W_B' \left(B_6 B_3' \right)^{T_{EH}}$		40 $\overline{W}$	$(W_B' T_{EH}) = T_P$ of sectors 177, 03, 07, etc.; T_{13} and T_P of sectors 00, 04, 10, etc.; T_{13} of sectors 01, 05, 11, etc. Puts 4000/1 into left-half word of sector 0 of R loop when coarse time pulse is present
$_1R_S$ =		J431	A	R_S samples resolver inputs and indicates polarity of change.
	$I_{4A}^* \left(W_B W_A \right)^{W_3} [T_P]^{T_{PB}}$		2 6 23	R_S samples I_{4A} at T_P of sectors 2, 6, 12, 16, etc.
	$+ I_{5A}^* \left(W_B W_A \right)^{W_3} [B_5 B_4' B_3 B_2]^{T_{11}}$		1 6 $\overline{V}$	R_S samples I_{5A}^* at T_{11} of sectors 3, 7, 13, 17, etc.
	$+ I_{6A}^* W_B W_A' [B_5 B_4' B_3 B_2]^{T_{11}}$		4 5 13 $\overline{V}$	R_S samples I_{6A} at T_{11} of sectors 2, 6, 12, 16, etc.

Term	Equation	Receptacle	Pin No.	Definition
$_1R_S$	(CONT)	J431	A	
	$\left\{ \begin{array}{l} I_D \cdot B_2 \\ \\ \\ + R_K \cdot B_2 \cdot T_P \end{array} \right\} R_S \cdot (W_B B_3)^{W_{BB3}}$		H7	I_D holds state of I_{6B} and I_{5B} at T_{12} of sectors 2 and 3, respectively.
			28 $\bar{H}$	$W_B B_3 = T_{23}$ of sector 1 through T_{20} of sector 3
			J K 31	R_K holds state of I_{4B} at T_X of sector 3 and phase A and B the same at T_{13} of sectors 2 and 3, and at T_O of sector 3.
	$+ R_X \cdot (W_B \cdot W_A)^{W_O} [T_X]^{T_{XA}}$		$\bar{C}$ 25 17	R_X at T_X of sector 0 indicate a coarse-time pulse was not sampled four words earlier. R_S = one at T_{11} of sector 0 prevents R_T from being one-set.
	$\left\{ \begin{array}{l} I_{1N} [T_O]^{T_{OA}} \\ \\ \\ + I_{3N} [B_6 B_3 T_P]^{T_{13}} \end{array} \right\} (W_B \cdot W_A)^{W_1}$		E M T B P	$W_1 = T_{23}$ of sector 000 to T_{20} of sectors 01 and 04; 05 and 10; and 11, etc. I_{1N} and I_{3N} are input lines into R register. These lines determine whether to Add (R_S = 0) the state of I_{11} and I_{14} to or Subtract (R_S = 1) the state of I_{11} and I_{14} from right-half word of R. I_{1N} and I_{3N} determine whether to Add or Subtract I_{31} and I_{34} from left-half word.
$_0R_S$	$W_B (B_5 B_4 \cdot B_3 B_1)^{T_{10}}$		15	R_S samples resolver inputs and indicates polarity of change.
			5 11	Zero-sets R_S at sectors 2 and 3 prior to sampling resolver input lines
	$+ W_B \cdot [B_5 B_4 \cdot B_3 B_2]^{T_{11}}$		12 $\bar{V}$	Zero-sets R_S at sectors 0 and 1, at sector 0 so fine time counter may be increased by one, and at sector 1 prior to sampling variable incremental inputs
	$+ [B_5 \cdot B_4 \cdot B_2 B_1]^{T_{24}}$		$\bar{U}$	Initialize

Term	Equation	Receptacle	Pin No.	Definition
$_0R_S$	(CONT)	J431	15	
	$+\left\{\begin{matrix} I_D' B_2 \\ \\ \\ + R_K' B_2' T_P' \end{matrix}\right\} R_S \left(W_B B_3\right)^{W_{BB3}'}$		H 7	Determines if there is a change in resolver inputs I_{5B} and I_{6B}
			29 $\overline{H}$	
			J K 31	Determines if there is a change in resolver input I_{4B}; determines decoding of I_4, I_5 and I_6
$_1R_T$ =			$\overline{B}$	R_T resets fine time counter when a coarse time pulse is received.
	$R_S' \left(W_B' W_A'\right)^{W_{QI}} [B_5 B_4' B_3 B_2]^{T_{LD}}$		28 25 $\overline{V}$	One-sets R_T so fine time counter may be set to 4000/1 when a coarse time pulse is sampled
$_0R_T$ =			26	R_T resets fine time counter when a coarse time pulse is received.
	$[T_P]^{T_{PB}}$		23	Initialize
$_1S_{B3}$ =		J525	16	S_{B3} is Flag code buffer flip-flop, receives character input information during Noncompute mode, checks parity of character, and serves as an input control during word 1 of Multiply.
	$\left(K_D'\right)^{K_D'} I_P \left([B_6 B_5' B_4] [B_2 B_1']\right)^{T_{20}}$		27 38 12	Loads most significant bit of Flag code from I_P
	$+ \left([K' J'] V_C R_C\right)^{N_{SC}} I_5^*$		$\overline{A}$ K	S_{B3} receives I_5 (parity bit) during Sample code of Load mode
	$+ S_{B3}' C_{P1} \left([K' V_C] O_4\right)^{N_{ST}} C_{P5}'$		23 $\overline{E}$ $\overline{D}$ $\overline{C}$	S_{B3} counts number of ones from C_{P1} during parity check of Load mode
	$+ \left([K' J'] N_C'\right)^{N_{ENT}}$		21	Ensures that S_{B3} is one when entering manual Halt mode from program Halt mode
	$\left(+ [K N_C O_4' O_3] J' A_P\right)^{O_{MF}}$		3 4 13	One-sets S_{B3} for word 1 of Execute so sign of left-half or full word may be determined in A_{24} for Multiply

Term	Equation	Receptacle	Pin No.	Definition
$0^{S_{B3}} =$		J525	30	S_{B3} is Flag code buffer flip-flop, receives character input information during Noncompute mode, checks parity of character, and serves as an input control during word 1 of Multiply
	$(K D')\ I_P'\ ([B_6\ B_4'\ B_3]\ [B_2'\ B_1])^{K_D'\ T_{21}}$		27 $\bar{U}$ 36	Zero-sets S_{B3} if the instruction is not flagged
	$+ (K D')\ ([B_6\ B_5'\ B_4]\ B_2\ B_1)^{K_D'\ T_{19}}$		27 5	Initializes S_{B3} prior to loading of Flag code bit at T_{20}
	$+ ([K' J']\ V_C\ R_C)\ O_4^{N_{SC}}$		$\bar{A}\ \bar{B}$	Initializes S_{B3} prior to sampling character input lines during Sample code of Load mode
	$+ S_{B3}\ C_{P1}\ ([K'\ V_C]\ O_4)\ C_{P5}^{N_{ST}}$		28 $\bar{E}\ \bar{D}\ \bar{C}$	S_{B3} counts the number of ones from C_{P1} during parity check of Load mode
	$(+ [K N_C O_4'\ O_3]\ J)^{O_{MF}}$		3 25	Initializes S_{B3} prior to checking for sign of product of Multiply, true at T_1 or T_1 and T_{14} of Multiply
$1^{S_{B2}} =$			A	S_{B2} is Flag code buffer flip-flop, verify indicator for verify error, phase indicator during Multiply, and control during word 1 of Multiply.
	$(K D')\ I_P\ ([B_6\ B_5'\ B_4]\ B_2\ B_1)^{K_D'\ T_{19}}$		27 38 5	Leads center bit of Flag code from I_P
	$+\left\{\begin{array}{l} A_X\ N_X'\ K'\ O_3 \\ \\ \\ + A_X'\ N_X\ K'\ O_3 \end{array}\right\} E D' [T_P'\ T_X'\ T_O']^{T_{PXO}'}$		B C D E	
			2 $\bar{P}$ 1	Verifies Load mode; compares new information in A register with information from memory
			J H D E	
	$+ [K'\ V_C'\ R_C'\ J]\ S_{B3}'^{N_{MH}}$		6 23	One-sets S_{B2} when a parity error is detected. This prevents K mode from being initiated.

Term	Equation	Receptacle	Pin No.	Definition
1^{S}_{B2}	(CONT)	J525	A	
	$+ [K Q O_4' O_3] L_P B_3' T_P'^{O_{MO}}$		10 F 8 7	S_{B2} holds present phase of Multiply at T_1 or T_1 and T_{14}.
	$(+ [K N_C O_4' O_3] J' N_P)^{O_{MF}}$		3 4 41	One-sets S_{B2} for word 1 of Execute so sign of left-half or full word may be determined in A_{24} for Multiply
0^{S}_{B2} =			15	S_{B2} is Flag code buffer flip-flop, verify indicator for verify error, phase indicator during Multiply, and control during word 1 of Multiply.
	$(K D)^{K_D'} I_P' ([B_6 B_4' B_3] [B_2' B_1])^{T_{21}}$		27 $\bar{U}$ 36	Zero-sets S_{B2} if instruction is not flagged
	$+ (K D)^{K_D'} [B_6 B_5 B_4]^{B_{LU7}}$		27 26	Initializes S_{B2} at T_{14}, T_{15}, and T_{16} before sampling of Flag code bit at T_{19}
	$+ ([K' V_C] J R_C') T_O^{N_W}$		22 Z	Initializes S_{B2} during Wait mode prior to comparison of A and N of verify
	$+ ([K' J'] V_C')^{N_{ENT}}$		21	Ensures that S_{B2} is zero when entering manual Halt mode
	$+ [K Q O_4' O_3] L_P' B_3' T_P'^{O_{MO}}$		10 9 8 7	S_{B2} holds present phase of Multiply at T_1 or T_1 and T_{14}.
	$(+ [K N_C O_4' O_3] J)^{O_{MF}}$		3 25	Initializes S_{B2} prior to checking for sign of product of Multiply. True at T_1 or T_1 and T_{14} of word 1 Multiply.

Term	Equation	Receptacle	Pin No.	Definition
$_1S_{B1}$ =		J525	17	S_{B1} indicates 16-word disagreement and is used as Flag code buffer flip-flop.
	$O_{B3}\ (B_6'\ B_5\ B_4)^{B_{LU3}}\ B_2'$		S N L	Copies contents of O_{B3} into S_{B1} for number agreement. O_{B3} holds 16-word disagreement at T_6.
	$+ I_P\ ([B_6\ B_5'\ B_4]\ [B_2'\ B_1'])^{T_{18}}$		38 V	Loads least significant bit of Flag code from I_P
$_0S_{B1}$ =			31	S_{B1} indicates 16-word disagreement and is used as Flag code buffer flip-flop.
	$I_P'\ ([B_6\ B_4'\ B_3]\ [B_2'\ B_1])^{T_{21}}$		$\overline{U}$ 36	Initializes S_{B1} if instruction is not flagged
	$+ B_4\ [B_2'\ B_1]^{B_{L1}}$		$\overline{T}$ 37	Initializes at T_2, T_6, T_{14}, and T_{18}
$_1S_3$ =		J522	19	S_3 is a control flip-flop for writing into channel 50 and E, F, H, and U loops.
	$\left\{ \begin{matrix} S_{B1}' \\ \\ \\ + S_{B2} \end{matrix} \right\} \cdot ([K\ E]\ [E\ N_D'\ T_X])^{K_{FB}} S_{B3}$		41 S N 5	Loads state of S_{B3} into S_3 except when Flag code is 12
	$+ (O_3'\ O_2\ O_1\ E)\ (Q'\ C_{B5}\ C_{B3}\ [T_X]\ A)^{O_P}\ C_{B4}'\ C_{B2}^{C_{B53}}$		42 4 3 21	Stores A register into channel 54 or 56
$_0S_3$ =			$\overline{Y}$	S_3 is a control flip-flop for writing into channel 50 and E, F, H, and U loops.
	$[T_P]^{T_{PA}}$		D	Initialization

Term	Equation	Receptacle	Pin No.	Definition
$_1S_2$ =		J522	18	S_2 is a control flip-flop for writing into channel 50 and E, F, H, and U loops.
	K_{FB} $([K\,E]\,[E\,N_D{}'\,T_X])\,S_{B2}$		S 5	Loads Flag code contained in S_{B2} into S_3
	+ $(O_3{}'\,O_2\,O_1\,E)\,(Q'\,C_{B5}\,C_{B3}\,[T_X]_A)\,C_{B4}{}'\,C_{B1}{}'$		42 4 3 40	Stores A register into channel 50 or 54
$_0S_2$ =			$\overline{X}$	S_2 is a control flip-flop for writing into channel 50 and E, F, H, and U loops.
	T_{PA} $[T_P]$		D'	Initialization
$_1S_1$ =			1	S_1 is a control flip-flop for writing into channel 50 and E, F, H, and U loops.
	$\left\{ S_{B3}{}' \right\}$ K_{FB} $([K\,E]\,[E\,N_D{}'\,T_X])\,S_{B1}$		A	
	$\left\{ + S_{B2} \right\}$		S M	Loads Flag code contained in S_{B1} into S_1 except when Flag code is 12
			5	
	+ $(O_3{}'\,O_2\,O_1\,E)\,(Q'\,C_{B5}\,C_{B3}\,[T_X]_A)\,C_{B4}{}'\,C_{B2}{}'$		42 4 3 2	
$_0S_1$ =			$\overline{W}$	S_1 is a control flip-flop for writing into channel 50 and E, F, H, and U loops.
	T_{PA} $[T_P]$		D	Initialization
S_{00} =	C_{U0} C_{L0} $[C_5{}'\,C_4{}']\,[C_3{}'\,C_2{}'\,C_1{}']$	J415	16 21 $\overline{D}$	AND gates for control of write switches

Term	Equation	Receptacle	Pin No.	Definition
S_{02}	$= [C_5' C_4'] [C_3' C_2' C_1]^{C_{U0}\ C_{L1}}$	J415	S 21 $\overline{C}$	AND gates for control of write switches
S_{04}	$= [C_5' C_4'] [C_3' C_2 C_1']^{C_{U0}\ C_{L2}}$		17 21 W	
S_{06}	$= [C_5' C_4'] [C_3' C_2 C_1]^{C_{U0}\ C_{L3}}$		T 21 Y	
S_{10}	$= [C_5' C_4'] [C_3 C_2' C_1']^{C_{U0}\ C_{L4}}$		18 21 $\overline{B}$	
S_{12}	$= [C_5' C_4'] [C_3 C_2' C_1]^{C_{U0}\ C_{L5}}$		U 21 $\overline{A}$	
S_{14}	$= [C_5' C_4'] [C_3 C_2 C_1']^{C_{U0}\ C_{L6}}$		19 21 Z	
S_{16}	$= [C_5' C_4'] [C_3 C_2 C_1]^{C_{U0}\ C_{L7}}$		V 21 22	
S_{20}	$= [C_5' C_4] [C_3' C_2' C_1']^{C_{U1}\ C_{L0}}$		$\overline{F}$ 23 $\overline{D}$	
S_{22}	$= [C_5' C_4] [C_3' C_2' C_1]^{C_{U1}\ C_{L1}}$		$\overline{E}$ 23 $\overline{C}$	
S_{24}	$= [C_5' C_4] [C_3' C_2 C_1']^{C_{U1}\ C_{L2}}$		24 23 W	
S_{26}	$= [C_5' C_4] [C_3' C_2 C_1]^{C_{U1}\ C_{L3}}$		25 23 Y	
S_{30}	$= [C_5' C_4] [C_3 C_2' C_1']^{C_{U1}\ C_{L4}}$		26 23 $\overline{B}$	

Term	Equation	Receptacle	Pin No.	Definition
S_{32}	$= [C_5' C_4] [C_3 C_2' C_1]^{C_{U1} \quad C_{L5}}$	J415	27 23 $\overline{A}$	AND gates for control of write switches
S_{34}	$= [C_5' C_4] [C_3 C_2 C_1']^{C_{U1} \quad C_{L6}}$		28 23 Z	
S_{36}	$= [C_5' C_4] [C_3 C_2 C_1]^{C_{U1} \quad C_{L7}}$		29 23 22	
S_{40}	$= [C_5 C_4'] [C_3' C_2' C_1']^{C_{U2} \quad C_{L0}}$		7 $\overline{P}$ $\overline{D}$	
S_{42}	$= [C_5 C_4'] [C_3' C_2' C_1]^{C_{U2} \quad C_{L1}}$		H $\overline{P}$ $\overline{C}$	
S_{44}	$= [C_5 C_4'] [C_3' C_2 C_1']^{C_{U2} \quad C_{L2}}$		38 $\overline{P}$ W	
S_{46}	$= [C_5 C_4'] [C_3' C_2 C_1]^{C_{U2} \quad C_{L3}}$		$\overline{S}$ $\overline{P}$ Y	
S_{50}	$= D_{DW}^*$		35 $\overline{Y}$	
${}_1T_O$	$= T_X$	J429	10	
			P	Bit counter logic
${}_0T_O$	$= T_O$		1	
			9	Bit counter logic

Term	Equation	Receptacle	Pin No.	Definition
$_1T_P$ =		J431	38	
	$[K' V_C' R_C]^{N_{RS}} S T_P'$		33 35 31	One-sets T_P each time a one appears in S and computer is in Synchronization mode
	$+ [B_5' B_4' B_2 B_1']^{T_{24}}$		$\overline{U}$	Bit counter logic
$_0T_P$ =		J427	18	
	T_P		5	Bit counter logic
$_1T_X$ =			3	
	T_P		5	Bit counter logic
$_0T_X$ =			2	
	T_X		E	Bit counter logic
$_1U_P$ =		J519	25, S	U_P is U loop write amplifier and sum flip-flop for Add/Subtract during Fine Countdown when integrating.
	$\left\{ U_X' V_X' P_3 \right.$		Y Z 17	Add/Subtracts a zero and zero with a carry/borrow
	$+ U_X' V_X P_3'$		Y 18 19	Add/Subtracts a zero and one without a carry/borrow
	$\left. \right\} F_C V_K T_O'$		$V \overline{T} \overline{V}$	Integration of P_3 determines carry/borrow
	$+ U_X V_X' P_3'$		21 Z 19	Add/Subtracts a one and zero without a carry/borrow
	$+ U_X V_X P_3$		21 18 17	Add/Subtracts a one and one with a carry/borrow
	$+ F_C [T_P' T_X' T_O']^{T_{PXO}'} V_K' U_X$		V W 23 21	Recirculation in Fine Countdown and integration is not being performed (V_K')

Term	Equation	Receptacle	Pin No.	Definition
$_1U_P$	(CONT)	J519	25, S	
	$\left\{\begin{matrix} U_X S_3' \\ + U_X S_1' \\ + S_3 S_1 A_X \end{matrix}\right\} F_C' [T_P' T_X' T_O']^{T_{PXO}'}$		21 6 21 3	} Normal recirculation
			$\bar{U}$ W	During T_1 through T_{24} and not in Fine Countdown
			E 4 C	Flag A register into U loop
	$+ T_{XX}$		UJ	AGC information
$_0U_P' =$			28	Recirculation in Fine Countdown and integration is not being performed (V_K')
	$\left\{\begin{matrix} U_X' V_X' P_3' \\ + U_X' V_X P_3 \\ + U_X V_X' P_3 \\ + U_X V_X P_3' \end{matrix}\right\} F_C V_K T_X'$		Y Z 19	Add/Subtracts a zero and zero without a carry/borrow
			Y 18 17	Add/Subtracts a zero and one with a carry/borrow
			V $\bar{T}$ 43	Integration
			21 Z 17	Add/Subtracts a one and zero with a carry/borrow
			21 18 19	Add/Subtracts a one and one without a carry/borrow
	$+ F_C [T_P' T_X' T_O'] V_K' U_X'^{T_{PXO}}$		V W 23 Y	Recirculation in Fine Countdown and integration is not being performed (V_K)
	$\left\{\begin{matrix} U_X' S_3' \\ + U_X' S_1' \\ + S_3 S_1 A_X' \end{matrix}\right\} F_C' [T_P' T_X' T_O']^{T_{PXO}'}$		Y 6 Y 3	} Normal recirculation
			$\bar{U}$ W	During T_{11} through T_{24} and not in Fine Countdown
			E 4 22	Flag A register into U loop
	$+ T_O$		$\bar{A}$	AGC information

Term	Equation	Receptacle	Pin No.	Definition
$_1V_C$ =		J521	$\bar{A}$	V_C is V loop control flip-flop and mode control during Non-compute mode.
	$K(O_3' O_2 O_1 E)\ (Q' C_{B5} C_{B3} [T_X]_A) C_{B4} (C_{B2}' C_{B1})$		$\bar{C}$ 23 32 $\bar{B}$ 22	One-sets V_C during store. The instruction is Store Accumulator (STO) into V loop.
	$+ \{ \dot{O}_1 O_2 F_S^* \}\ [K' V_C' R_C' J]^{N_{MH}}\ [T_X]^{T_{XA}}$		33 $\bar{D}$ $\bar{E}$	One-sets V_C when FILL switch is ON at which initiate Fill mode
			T 25	Manual Halt mode
	$+ O_4 O_2'$		$\bar{F}$ Z	One-sets V_C when T' is false. (Refer to $_1O_2$ logic.)
$_0V_C$ =		J522	B	V_C is V loop control flip-flop and mode control during Non-compute mode.
	$([K]_A [T_P]_B)^{K_{TP}}$		7	Initialization when in Compute mode
	$+ M_R^*$		8	Initialization during synchronization
	$+ ([K' J'] V_C R_C' C_{P5} C_{P4})^{N_{PC}}\ (C_{P3} C_{P2}' C_{P1}')^{C_{PL4}}\ [T_P]^{T_{PA}}$		J 9 D	Process submode of Load mode if Compute code was activated
	$+ ([K' J'] V_C R_C' C_{P5} C_{P4})^{N_{PC}}\ (C_{P3}' C_{P2}' C_{P1})^{C_{PLO}}\ [B_6 B_3' T_P']^{T_{13}}$		J C 23	Process submode of Load mode if Halt code was activated
	$+ ([K' V_C] R_C')^{N_{LRC}'} J' C_{P5} S_{B3}'\ [T_P]^{T_{PA}}$		H F E A D	A parity error was detected during parity check of Load mode
	$+ ([K' V_C] J R_C')^{N_W}\ S_{B2}\ [T_X]^{T_{XA}}$		6 5 26	A verify error was detected during Verify submode of Load mode

Term	Equation	Receptacle	Pin No.	Definition
$_1V_K$ =		J521	A	V_K samples resolver inputs, and decodes resolver change during carry/borrow.
	$I_{1B} * W_A' [T_P]^{T_{PA}}$		D 2 J	Samples phase B of resolver input I_1 at T_P of sectors 177, 01, 03, 05, 07, etc.
	$I_{2B} * (W_B' W_A) [T_P]^{W_1 \; T_{PA}}$		E F J	Samples phase B of resolver input I_2 at T_P of sectors 00, 04, 10, 14, etc.
	$+ I_{3B} * (W_B W_A) [T_P]^{W_3 \; T_{PA}}$		H 11 J	Samples phase B of resolver input I_3 at T_P of sectors 02, 06 12, 16, etc.
	$+ \left\{ \begin{matrix} V_S' V_X \\ + V_S V_X' \end{matrix} \right\} W_A ([B_6' B_5'] B_3')^{T_{CD}}$		24 P 3 13 18 17	Decodes resolver lines I_2 and I_3. If either phase A or B has changed in respect to four words earlier, V_K is one-set. $B_6' B_5' B_3' = T_X$ and T_O
	$+ \left\{ \begin{matrix} V_S' Z_1 \\ + V_S Z_1' \end{matrix} \right\} W_A' [T_X]^{T_{XA}}$		24 6 2 25 18 5	Decodes resolver line I_1. If phase A has changed, V_K is one-set.
	$+ \left\{ \begin{matrix} V_S' Z_2 \\ + V_S Z_2' \end{matrix} \right\} W_A' T_O$		24 7 2 1 18 8	Decodes resolver line I_1. If phase B has changed, V_K is one-set.
$_0V_K$ =			V	V_K samples resolver inputs, and decodes resolver change during carry/borrow.
	$[B_5' B_4' B_2 B_1']^{T_{24}}$		10	Initialization

Term	Equation	Receptacle	Pin No.	Definition
$_0V_K$	(CONT)	J521	10	
	$\left\{ \begin{array}{l} V_{AO} \\ (V_C\ V_X)\ V_S \\ V_{A1} \\ +(V_C\ V_X)\ V_S \\ \\ \\ V_{A2} \\ +(V_C\ A_X)\ V_S \\ V_{A3} \\ +(V_C\ A_X)\ V_S \end{array} \right\} T_{PXO}\ F_C\ [T_P\ T_X\ T_O]$		16 24	Turns V_K off during adding when first zero appears from V_X
			15 18	Turns V_K off during subtracting when first one appears from V_X
			Y W	V_K is carry/borrow for resolver inputs during T_1 through T_{24}
			19 24	Same as V_{A0} and V_{A1} above except this equation is effective when storing A register into V loop
			21 18	
	$+\left\{ \begin{array}{l} V_S\ V_X \\ \\ \\ +V_S\ V_X \end{array} \right\} T_{XA}\ W_A\ [T_X]$		24 17	If Phase A is zero and was zero four words earlier, V_K is zero-set.
			3 25	Resolver decoding I_2 and I_3
			18 P	If phase A is one now and was one four words earlier, V_K is zero-set.
	$+\left\{ \begin{array}{l} V_S\ Z_1 \\ \\ \\ +V_S\ Z_1 \end{array} \right\} T_{XA}\ W_A\ [T_X]$		24 5	If phase A is zero now and was zero two words earlier, V_K is zero-set.
			2 25	Resolver decoding I_1
			18 6	If phase A is one now and was one two words earlier, V_K is zero-set.
$_1V_P$ =		J519	$\overline{Y}$	V_P is V loop write amplifier and sum flip-flop for Add/Subtract of resolver inputs.

Term	Equation	Receptacle	Pin No.	Definition
$_1V_P$	(CONT)	J519	$\overline{Y}$	
	$\left\{ \begin{array}{l} V_{A1} \\ (V_C' V_X) V_K' \\ V_{A0} \\ +(V_C' V_X') V_K \\ V_{A3} \\ +(V_C A_X) V_K' \\ V_{A2} \\ +(V_C A_X') V_K \end{array} \right\} F_C' [T_P' T_X' T_O']^{T_{PXO}'}$		39 23	No change in resolver inputs therefore recirculate directly.
			$\overline{R}$ $\overline{T}$	Change in resolver inputs therefore recirculate inversely
			$\overline{U}$ W	Resolver input Add/Subtract
			$\overline{P}$ 23	Same as V_{A1} and V_{A0} above except this equation is effective when storing A register into V loop
			35 $\overline{T}$	
	$+\left\{ \begin{array}{l} V_{A1} \\ (V_C' V_X) \\ \\ V_{A3} \\ +(V_C A_X) \end{array} \right\} F_C [T_P' T_X' T_O']^{T_{PXO}'}$		39	Recirculation during Fine Countdown
			V W	
			$\overline{P}$	Stores A register into V loop during Fine Countdown
	$+ V_S ([B_6' B_5'] B_3')^{T_{CD}}$		38 37	Copies V_S into V_P during T_X and T_O. V_S contains phase A at T_X and phase A and B alike or different at T_O
	$+ V_X' [T_P]^{T_{PA}}$		40 $\overline{S}$	Inversion type AGC information
$_0V_P$ =		J519	$\overline{L}$	V_P is V loop write amplifier and sum flip-flop for Add/Subtract of resolver inputs

Term	Equation	Receptacle	Pin No.	Definition
$_0V_P$	(CONT)	J519	$\overline{L}$	
	$\left\{ \begin{matrix} V_{AO} \\ (V_C\ V_X)\ V_K \end{matrix} \right.$		$\overline{R}$ 23	No change in resolver inputs therefore recirculate directly
	$\left. \begin{matrix} V_{A1} \\ + (V_C\ V_X)\ V_K \end{matrix} \right\} F_C\,[T_P\ T_X\ T_O]^{T_{PXO}}$		39 $\overline{T}$	Change in resolver inputs therefore recirculate inversely
			$\overline{U}$ W	Resolver input Add/Subtract
	$+ (V_C\ A_X)\ V_K$		35 23	Same as V_{A1} and V_{A0} above except this equation is effective when storing A register into V loop
	$+ (V_C\ A_X)\ V_K$		$\overline{P}$ $\overline{T}$	
	$+ \left\{ \begin{matrix} V_{AO} \\ (V_C\ V_X) \end{matrix} \right.$		$\overline{R}$	Recirculation during Fine Countdown
	$\left. \begin{matrix} \\ \\ V_{A2} \\ (V_C\ A_X) \end{matrix} \right\} F_C\,[T_P\ T_X\ T_O]^{T_{PXO}}$		V W	
			35	Stores A register into V loop during Fine Countdown
	$+ V_S\ ([B_6\ B_5]\ B_3)^{T_{CD}}$		36 37	Copies V_S into V_P during T_X and T_O. V_S contains phase A at T_X and phase A and B alike or different at T_O
	$+ V_X\,[T_P]^{T_{PA}}$		$\overline{M}$ $\overline{S}$	Inversion type AGC information
$_1V_S$ =		J521	S	V_S samples resolver inputs and decodes resolver change during Add/Subtract
	$I_{1A} * W_A\,[T_P]^{T_{PA}}$		N 2 J	Identical to $_1V_K$ logic except this is phase A

Term	Equation	Receptacle	Pin No.	Definition
$_1V_S$	(CONT)	J521	S	
	$+ I_{2A}^{*} \left(W_B^{W_1} W_A\right) [T_P]^{T_{PA}}$		M F J	Identical to $_1V_K$ logic except this is phase A
	$+ I_{3A}^{*} \left(W_B^{W_3} W_A\right) [T_P]^{T_{PA}}$		L 11 J	Identical to $_1V_K$ logic except this is phase A
	$+ V_S' V_K' \left([B_6' B_5'] B_3'\right)^{T_{CD}}$		24 12 13	Resolver decoding at T_X and T_O when polarity of change is negative
$_0V_S$ =			4	V_S samples resolver inputs and decodes resolver change during Add/Subtract
	$[B_5' B_4' B_2 B_1']^{T_{24}}$		10	Initialization
	$+ V_S V_K' \left([B_6' B_5'] B_3'\right)^{T_{CD}}$		18 12 13	Resolver decoding at T_X and T_O when polarity of change is positive
$_1V_{38}$ =		J537	$\overline{X}$	V_{38} is a voltage output C register
	$[A_X] \left([V_T] [B_4' B_3 B_2] [C_{L6}]\right)^{A_{XA}\ V_{3P}}$		6 $\overline{P}$	$[V_T]$ = T_5 through T_{13} or T_{14} through T_X. During VOC, copies state of A_X into V_{38} at T_{11} or T_{23} and T_{24}
$_0V_{38}$ =			30	
	$[A_X'] \left([V_T] [B_4' B_3 B_2] [C_{L6}]\right)^{A_{XA}\ V_{3P}}$		L $\overline{P}$	Refer to $_1V_{38}$ logic
$_1V_{37}$ =			$\overline{Y}$	V_{37} is a voltage output C register
	$A_P \left([V_T] [B_4' B_3 B_2] [C_{L6}]\right)^{V_{3P}}$		$\overline{S}$ $\overline{P}$	During VOC, copies A_P into V_{37} at T_{11} or T_{23} and T_{24}

Term	Equation	Receptacle	Pin No.	Definition
$_0V_{37}$ =		J537	29	
	$A_P' \left([V_T]\ [B_4' B_3 B_2]\ [C_{L6}]\right)^{V_{3P}}$		$\bar{R}\,\bar{P}$	Refer to $_1V_{37}$ logic
$_1V_{36}$ =			$\bar{W}$	V_{36} is a voltage output C register
	$A_{24} \left([V_T]\ [B_4' B_3 B_2]\ [C_{L6}]\right)^{V_{3P}}$		3 $\bar{P}$	During VOC, copies state of A_{24} into V_{36} at T_{11} or T_{23} and T_{24}
$_0V_{36}$ =			31	
	$A_{24}' \left([V_T]\ [B_4' B_3 B_2]\ [C_{L6}]\right)^{V_{3P}}$		4 $\bar{P}$	Refer to $_1V_{36}$ logic
$_1V_{35}$ =			$\bar{V}$	V_{35} is a voltage output C register
	$J \left([V_T]\ [B_4' B_3 B_2]\ [C_{L6}]\right)^{V_{3P}}$		J $\bar{P}$	During VOC, copies state of J into V_{35} at T_{11} or T_{23} and T_{24}
$_0V_{35}$ =			32	
	$J' \left([V_T]\ [B_4' B_3 B_2]\ [C_{L6}]\right)^{V_{3P}}$		K $\bar{P}$	Refer to $_1V_{35}$ logic
$_1V_{34}$ =			15	V_{34} is a voltage output C register
	$A_P \left([V_T]\ B_4\ [C_{L6}]\right)^{V_{3S}}\ B_6'$		$\bar{S}$ Z 21	During VOC, copies A_P into V_{34} at T_5 through T_8
	$+ [A_X]\ \left([V_T]\ B_4\ [C_{L6}]\right)^{V_{3S}}\ B_6$		6 Z 20	During VOC, copies A_X into V_{34} at T_{14} through T_{20}

Term	Equation	Receptacle	Pin No.	Definition
$_0V_{34}$ =		J537	28	
	$A_P' \left([V_T]\ B_4\ (C_{L6}|)\right)^{V_{3S}}\ B_6'$		R Z 21	Refer to $_1V_{34}$ logic
	$+ [A_X']\ \left([V_T]\ B_4\ [C_{L6}]\right)^{A_{XA}'\ V_{3S}}\ B_6$		L Z 20	
$_1V_{33}$ =		J439	23	V_{33} is a voltage output C register
	$V_{34}\ \left([V_T]\ B_4\ [C_{L6}]\right)^{V_{3S}}$		16 U	During VOC, copies V_{34} into V_{33} at T_5 through T_8 or T_{14} through T_{20}
$_0V_{33}$ =			$\bar{A}$	
	$V_{34}'\ \left([V_T]\ B_4\ [C_{L6}]\right)^{V_{3S}}$		TU	Refer to $_1V_{33}$ logic
$_1V_{32}$ =			Z	V_{32} is a voltage output C register
	$V_{33}\ \left([V_T]\ B_4\ [C_{L6}]\right)^{V_{3S}}$		V U	During VOC, copies V_{33} into V_{32} at T_5 through T_8 or T_{14} through T_{20}
$_0V_{32}$ =			22	
	$V_{33}'\ \left([V_T]\ B_4\ [C_{L6}]\right)^{V_{3S}}$		17 U	Refer to $_1V_{32}$ logic
$_1V_{31}$ =			X	V_{31} is a voltage output C register
	$V_{32}\ \left([V_T]\ B_4\ [C_{L6}]\right)^{V_{3S}}$		19 U	During VOC, copies V_{32} into V_{31} at T_5 through T_8 or T_{14} through T_{20}
$_0V_{31}$ =			20	
	$V_{32}'\ \left([V_T]\ B_4\ [C_{L6}]\right)^{V_{3S}}$		W U	Refer to $_1V_{31}$ logic

Term	Equation	Receptacle	Pin No.	Definition
$^{1}V_{28}$ =		J537	$\bar{U}$	V_{26} is a voltage output B register
	$[A_X]([V_T][B_4' B_3 B_2][C_{L5}])^{A_{XA} V_{2P}}$		6 H	During VOB, copies state of A_X into V_{28} at T_{11} or T_{23} and T_{24}
$^{0}V_{28}$ =			33	
	$[A_X'][([V_T][B_4' B_3 B_2][C_{L5}])^{A_{XA} V_{2P}}$		L H	Refer to $^{1}V_{28}$ logic
$^{1}V_{27}$ =			$\bar{T}$	V_{27} is a voltage output B register
	$A_P([V_T][B_4' B_3 B_2][C_{L5}])^{V_{2P}}$		$\bar{S}$ H	During VOB, copies A_P into V_{27} at T_{11} or T_{23} and T_{24}
$^{0}V_{27}$ =			34	
	$A_P'([V_T][B_4' B_3 B_2][C_{L5}])^{V_{2P}}$		$\bar{R}$ H	Refer to $^{1}V_{27}$ logic
$^{1}V_{26}$ =			F	V_{26} is a voltage output B register
	$A_{24}([V_T][B_4' B_3 B_2][C_{L5}])^{V_{2P}}$		3 H	During VOB, copies A_{24} into V_{26} at T_{11} or T_{23} and T_{24}
$^{0}V_{26}$ =			7	
	$A_{24}'([V_T][B_4' B_3 B_2][C_{L5}])^{V_{2P}}$		4 H	Refer to $^{1}V_{26}$ logic
$^{1}V_{25}$ =			E	V_{25} is a voltage output B register
	$J([V_T][B_4' B_3 B_2][C_{L5}])^{V_{2P}}$		J H	During VOB, copies J into V_{25} at T_{11} or T_{23} and T_{24}
$^{0}V_{25}$ =			8	
	$J'([V_T][B_4' B_3 B_2][C_{L5}])^{V_{2P}}$		K H	Refer to $^{1}V_{25}$ logic

Term	Equation	Receptacle	Pin No.	Definition
$1^{V_{24}}$ =		J537	16	V_{24} is a voltage output B register
	$A_P \left([V_T]\ B_4\ [C_{L5}]\right)^{V_{2S}}\ B_6'$		$\bar{S}\,\bar{A}$ 21	During VOB, copies A_P into V_{24} at T_5 through T_8
	$+\ [A_X]\ \left([V_T]\ B_4\ [C_{L5}]\right)^{A_{XA}}\ B_6$		6 $\bar{A}$ 20	During VOB, copies A_X into V_{24} at T_{14} through T_{20}
$0^{V_{24}}$ =			27	
	$A_P' \left([V_T]\ B_4\ [C_{L5}]\right)^{V_{2S}}\ B_6'$		R $\bar{A}$ 21	Refer to $1^{V_{24}}$ logic
	$+\ [A_X']\ \left([V_T]\ B_4\ [C_{L5}]\right)^{A_{XA}''}\ B_6$		L $\bar{A}$ 20	Refer to $1^{V_{24}}$ logic
$1^{V_{23}}$ =		J439	L	V_{23} is a voltage output B register
	$V_{24} \left([V_T]\ B_4\ [C_{L5}]\right)^{V_{2S}}$		10 15	During VOB, copies V_{24} into V_{23} at T_5 through T_8 or T_{14} through T_{20}
$0^{V_{23}}$ =			8	
	$V_{24}' \left([V_T]\ B_4\ [C_{L5}]\right)^{V_{2S}}$		J 15	Refer to $1^{V_{23}}$ logic
$1^{V_{22}}$ =			12	V_{22} is a voltage output B register
	$V_{23} \left([V_T]\ B_4\ [C_{L5}]\right)^{V_{2S}}$		18 15	During VOB, copies V_{23} into V_{22} at T_5 through T_8 or T_{14} through T_{20}
$0^{V_{22}}$ =			11	
	$V_{23}' \left([V_T]\ B_4\ [C_{L5}]\right)^{V_{2S}}$		M 15	Refer to $1^{V_{22}}$ logic

Term	Equation	Receptacle	Pin No.	Definition
$1^{V_{21}}$ =		J439	13	V_{21} is a voltage output B register
	V_{2S} $V_{22}\,([V_T]\ B_4\ [C_{L5}])$		S 15	During VOB, copies V_{22} into V_{21} at T_5 through T_8 or T_{14} through T_{20}
$0^{V_{21}}$ =			N	
	V_{2S} $V_{22}'\,([V_T]\ B_4\ [C_{L5}])$		P 15	Refer to $1^{V_{21}}$ logic
$1^{V_{18}}$ =		J537	13	V_{18} is a voltage output A register
	A_{XA} V_{1P} $[A_X]\,([V_T]\,[B_4'\ B_3\ B_2]\,[C_{L4}])$		6 5	During VOA, copies A_X into V_{18} at T_{11} or T_{23} and T_{24}
$0^{V_{18}}$ =			A	
	A_{XA}' V_{1P} $[A_X']\,([V_T]\,[B_4'\ B_3\ B_2]\,[C_{L4}])$		L 5	Refer to $1^{V_{18}}$ logic
$1^{V_{17}}$ =			11	V_{17} is a voltage output A register
	V_{1P} $A_P\,([V_T]\,[B_4'\ B_3\ B_2]\,[C_{L4}])$		$\bar{S}$ 5	During VOA, copies A_P into V_{17} at T_{11} or T_{23} and T_{24}
$0^{V_{17}}$ =			B	
	V_{1P} $A_P'\,([V_T]\,[B_4'\ B_3\ B_2]\,[C_{L4}])$		$\bar{R}$ 5	Refer to $1^{V_{17}}$ logic
$1^{V_{16}}$ =			C	V_{16} is a voltage output A register
	V_{1P} $A_{24}\,([V_T][B_4'\ B_3\ B_2]\,[C_{L4}])$		3 5	During VOA, copies A_{24} into V_{16} at T_{11} or T_{23} and T_{24}

Term	Equation	Receptacle	Pin No.	Definition
$_0V_{16}$ =		J537	10	
	$A_{24}' \left([V_T]\ [B_4'\ B_3\ B_2]\ [C_{L4}]\right)^{V_{1P}}$		4 5	Refer to $_1V_{16}$ logic
$_1V_{15}$ =			D	V_{15} is a voltage output A register
	$J \left([V_T]\ [B_4'\ B_3\ B_2]\ [C_{L4}]\right)^{V_{1P}}$		J 5	During VOA, copies J into V_{15} at T_{11} or T_{23} and T_{24}
$_0V_{15}$ =			9	
	$\overline{J} \left([V_T]\ [B_4'\ B_3\ B_2]\ [C_{L4}]\right)^{V_{1P}}$		K 5	Refer to $_1V_{15}$ logic
$_1V_{14}$ =			17	V_{14} is a voltage output A register
	$A_P \left([V_T]\ B_4\ [C_{L4}]\right)^{V_{1S}} B_6'$		$\overline{S}$ 18 21	During VOA, copies A_P into V_{14} at T_5 through T_8
	$+ [A_X] \left([V_T]\ B_4\ [C_{L4}]\right)^{A_{XA}\ V_{1S}} B_6$		6 18 20	During VOA, copies A_X into V_{14} at T_{14} through T_{20}
$_0V_{14}$ =			26	
	$A_P' \left([V_T]\ B_4\ [C_{L4}]\right)^{V_{1S}} B_6'$		$\overline{R}$ 18 21	Refer to $_1V_{14}$ logic
	$+ [A_X'] \left([V_T]\ B_4\ [C_{L4}]\right)^{A_{XA}'\ V_{1S}} B_6$		L 18 20	Refer to $_1V_{14}$ logic
$_1V_{13}$ =		J439	7	V_{13} is a voltage output A register
	$W_{I4} \left([V_T]\ B_4\ [C_{L4}]\right)^{V_{1S}}$		2 A	During VOA, copies V_{14} into W_{I3} at T_5 through T_8 or T_{I4} through T_{20}

Term	Equation	Receptacle	Pin No.	Definition
$_0V_{13}$ =		J439	H	
	V_{1S} $V_{14}' ([V_T]\ B_4\ [C_{L4}])$		B A	Refer to $_1V_{13}$ logic
$_1V_{12}$ =			F	V_{12} is a voltage output A register
	V_{1S} $V_{13} ([V_T]\ B_4\ [C_{L4}])$		3 A	During VOA, copies V_{13} into V_{12} at T_5 through T_8 or T_{14} through T_{20}
$_0V_{12}$ =			6	
	V_{1S} $V_{13}' ([V_T]\ B_4\ [C_{L4}])$		C A	Refer to $_1V_{12}$ logic
$_1V_{11}$ =			E	V_{11} is a voltage output A register
	V_{1S} $V_{12} ([V_T]\ B_4\ [C_{L4}])$		1 A	During VOA, copies V_{12} into V_{11} at T_5 through T_8 or T_{14} through T_{20}
$_0V_{11}$ =			5	
	V_{1S} $V_{12}' ([V_T]\ B_4\ [C_{L4}])$		D A	Refer to $_1V_{11}$ logic
$_1W_A$ =		J525	43	W_A and W_B are module four counter for V and R loops
	T_{21} $S ([B_6\ B_4'\ B_3]\ [B_2'\ B_1])$		39 36	One-sets W_A when a one appears on sector track at T_{21}
$_0W_A$ =			T	W_A and W_B are module four counter for V and R loops
	T_{20} $([B_6\ B_5'\ B_4]\ [B_2\ B_1'])$		12	Initialization
$_1W_B$ =			$\bar{X}$	
	T_{22} $S ([B_6\ B_4'\ B_3]\ [B_2'\ B_1'])$		39 $\bar{R}$	One-sets W_B when a one appears on sector track at T_{22}

Term	Equation	Receptacle	Pin No.	Definition
$_0W_B$ =		J525	18	
	$([B_6\ B_5\ B_4]\ [B_2\ B_1]')^{T_{20}}$		12	Initialization
$_1W_{C1}$ =		J413	41	W_{C1} writes ones into cold storage
	$(O_3'\ O_2\ O_1\ E)\ D'\ A_X\ [T_P'\ T_X'\ T_O']^{O_P\ \ T_{PXO}'}$		34 33 23 22	One-sets W_{C1} when instruction is STO and a one is in A_X; (O_P = STO; T_{PXO}' = T_1 through T_{24})
	$+ (O_3'\ O_2\ O_1\ E)\ [D'\ T_P]^{O_P\ \ D_{TP}'}$		34 35	Writes a one at T_P time for AGC; O_P = STO
$_0W_{C1}$ =			42	W_{C1} writes ones into cold storage
	$(A_X'\ T_P')^{A_{XP}'}$		$\bar{V}$	Zero-sets W_{C1} when a zero is in A_X
	$+ T_X$		$\bar{T}$	Initialization
$_1W_{C0}$ =	$\left\{ A_X'\ [T_P'\ T_X'\ T_O']^{T_{PXO}'} \right\}\ (O_3'\ O_2\ O_1\ E)\ D'^{O_P}$		43	W_{C0} writes zeros into cold storage
			P 22	One-sets W_{C0} when a zero is in A_X
			34 33	Stores instruction
	$+ T_O$		36	Writes a zero at T_O for AGC
$_0W_{C0}$ =			$\bar{J}$	W_{C0} writes zeros into cold storage
	$A_X\ [T_P'\ T_X'\ T_O']^{T_{PXO}'}$		23 22	Zero-sets W_{C0} when a one is in A_X
	$+ T_P$		21	Initialization

Term	Equation	Receptacle	Pin No.	Definition
$_1W_{H1}$ =		J413	$\overline{X}$	W_{H1} writes ones into channel 50
	$(S_3' S_2 S_1)^{S_{C3}} A_X [T_P' T_X' T_O']^{T_{PXO}'}$		37 23 22	One-sets W_{H1} when instruction is STO as flag A register into channel 50 and a one is in A_X
	$+ (S_3' S_2 S_1)^{S_{C3}} T_P$		37 21	Writes a one at T_P for AGC when instruction is STO into channel 50
$_0W_{H1}$ =			$\overline{K}$	W_{H1} writes ones into channel 50
	$(A_X' T_P')^{A_{XP}'}$		$\overline{V}$	Zero-sets W_{H1} when a zero is in A_X
	$+ T_X$		$\overline{T}$	Initialization
$_1W_{H0}$ =			$\overline{F}$	W_{H0} writes zeros into channel 50
	$(S_3' S_2 S_1)^{S_{C3}} (A_X' T_P')^{A_{XP}'}$		37 $\overline{V}$	One-sets W_{H0} when instruction is store STO or flag A register into channel 50 and zero is in A_X
	$+ (S_3' S_2 S_1)^{S_{C3}} T_O$		37 36	Writes a zero at T_O for AGC when instruction is STO into channel 50
$_0W_{H0}$ =			S	W_{H0} writes zeros into channel 50
	$A_X [T_P' T_X' T_O']^{T_{PXO}'}$		23 22	Zero-sets W_{H0} when a one is in A_X
	$+ T_P$		21	Initialization
$_1Z_2$ =		J521	30	Z_2 indicates phase A and B alike or different
	$V_S W_A' T_O$		18 2 1	One-sets Z_2 when resolver lines I_{1A} and I_{1B} are alike
$_0Z_2$ =			31	Z_2 indicates phase A and B alike or different
	$V_S' W_A' T_O$		24 2 1	Zero-sets Z_2 when resolver lines I_{1A} and I_{1B} are different

Term	Equation	Receptacle	Pin No.	Definition
$_1Z_1$ =		J521	26	Z_2 indicates phase A and B alike or different
	$V_S\ W_A\ [T_X]^{T_{XA}}$		18 2 25	One-sets Z_1 when resolver line I_{1A} is true
$_0Z_1$ =			29	Z_1 indicates phase A is one or zero
	$V_S\ W_A\ [T_X]^{T_{XA}}$		24 2 25	Zero-sets Z_1 when resolver line I_{1A} is false
	PRIMARY AND GATES			
(A_{XP}') =	$(A_X\ T_P')$		526 39 $\overline{P}$ $\overline{R}$	
(B_{LU3}) =	$(B_6'\ B_5\ B_4)$		529 X 27 D 8	
(C_{U3}) =	$(C_5\ C_4)$		533 S $\overline{E}$ $\overline{F}$	
(C_{BLO}) =	$(C_{B3}'\ C_{B2}'\ C_{B1}')$		528 $\overline{H}$ 24 $\overline{B}$ $\overline{A}$	
(C_{BLT}) =	$(D'\ B_5\ B_4')$		529 N T D V	
(C_{BST}) =	$([O_3'\ O_1']^{O_{31}}\ D\ N_D'\ [B_6'\ B_5'\ B_3]^{B_{UO3}})$		529 29 32 25 33 34	
(C_{B21}') =	$(C_{B2}'\ C_{B1}')$		528 U $\overline{B}$ $\overline{A}$	
(C_{B53}) =	$(Q'\ C_{B5}\ C_{B3}\ [T_{X\,A}])$		528 29 26 $\overline{D}$ 25 9	
(C_{PIR}) =	$([K_A]\ C_{P5}\ C_{P3}\ C_{P2})$		528 16 J 23 20 X	
(C_{PL0}) =	$(C_{P3}'\ C_{P2}'\ C_{P1}')$		528 13 V 18 W	
(C_{PL1}) =	$(C_{P3}'\ C_{P2}'\ C_{P1})$		528 31 V 18 19	
(C_{PL2}) =	$(C_{P3}'\ C_{P2}\ C_{P1}')$		528 S V X W	
(C_{PL3}) =	$(C_{P3}'\ C_{P2}\ C_{P1})$		528 15 V X 19	
(C_{PL4}) =	$(C_{P3}\ C_{P2}'\ C_{P1}')$		528 $\overline{K}$ 20 18 W	

Term	Equation	Receptacle	Pin No.	Definition
(C_{PL5})	$= (C_{P3}\, C_{P2}'\, C_{P1})$		528 30 20 18 19	
(C_{PL6})	$= (C_{P3}\, C_{P2}\, C_{P1}')$		528 T 20 X W	
(C_{PL7})	$= (C_{P3}\, C_{P2}\, C_{P1})$		528 $\overline{J}$ 20 X 19	
(D_S)	$= (D_C\, [B_6'\, B_5']^{B_{SUO}})$		529 $\overline{C}$ 28 9	
(D_{13}')	$= (D'\, [B_6\, B_3'\, T_P']^{T_{13}})$		528 39 41 43	
(E_{OP})	$= (N_D\, [D\, T_P]^{D_{TP}})$		533 $\overline{D}$ W Y	
(E_{TP})	$= (E\, [D\, T_P]^{D_{TP}})$		533 $\overline{C}$ Z Y	
(I_{CX}')	$= (I_C'\, I_X')$		528 A E 5	
(I_{XE})	$= (I_X\, E)$		528 40 37 $\overline{R}$	
(K_{DP})	$= ([K_A]\, [D'\, T_P]^{D_{TP}'})$		533 27 23 24	
(K_D')	$= (K\, D')$		433 $\overline{P}$ 33 34	
(K_{FB})	$= ([K\, E]\, [E\, N_D'\, T_X]^{E_{FB}})$		533 42 $\overline{W}$ $\overline{V}$	
(K_{IC})	$= ([K_A]\, I_C\, T_P')$		528 G J 7 H	
(K_{TP})	$= ([K_A]\, [T_P\, B]^{N_L})$		533 26 23 22	
(M_C)	$= (C_4\, C_3\, A_C)$		533 A $\overline{F}$ $\overline{J}$ J	
(N_L')	$= (K'\, V_C')$		526 25 23 22	
(N_W)	$= ([K'\, V_C]^{N_L}\, J\, R_C')$		526 C K 8 Y	

Term	Equation	Receptacle	Pin No.	Definition
(T_{10})	$= (B_5\ B_4'\ B_3\ B_1')$		529 22 D V W 19	
(T_{12})	$= (B_3'\ B_2)$		529 16 C 18	
(T_{14})	$= ([B_6\ B_5\ B_4]^{B_{LU7}}\ B_2')$		529 $\overline{K}$ 36 30	
(T_{15})	$= ([B_6\ B_5\ B_4]^{B_{LU7}}\ B_1)$		529 $\overline{A}$ 36 37	
(T_{16})	$= ([B_6\ B_5\ B_4]^{B_{LU7}}\ [B_2\ B_1']^{B_{L2}})$		529 $\overline{J}$ 36 35	
(T_{17})	$= ([B_6\ B_5'\ B_4]^{B_{LU5}}\ [B_2'\ B_1]^{B_{L1}})$		529 $\overline{T}$ 40 42	
(T_{18})	$= ([B_6\ B_5'\ B_4]^{B_{LU5}}\ [B_2'\ B_1']^{B_{L0}})$		529 $\overline{W}$ 40 39	
(T_{19})	$= ([B_6\ B_5'\ B_4]^{B_{LU5}}\ B_2\ B_1)$		529 $\overline{R}$ 40 18 37	
(T_{20})	$= ([B_6\ B_5'\ B_4]^{B_{LU5}}\ [B_2\ B_1']^{B_{L2}})$		529 $\overline{U}$ 40 35	
(T_{21})	$= ([B_6\ B_4'\ B_3]^{B_{6MI}}\ [B_2'\ B_1]^{B_{L1}})$		529 $\overline{X}$ 43 42	
(T_{22})	$= ([B_6\ B_4'\ B_3]^{B_{6MI}}\ [B_2'\ B_1']^{B_{L0}})$		529 $\overline{Y}$ 43 39	
(T_{23})	$= ([B_4\ B_3\ B_2]^{B_{M3}}\ B_5'\ B_1)$		529 $\overline{F}$ 38 26 37	
(T_{816})	$= (B_5\ B_3\ [B_2\ B_1']^{B_{L2}})$		528 4 3 2 1	
(V_{AO})	$= (V_C'\ V_X^*)$		526 $\overline{W}$ 22 11	

Term	Equation	Receptacle	Pin No.	Definition
(O_{MOI}')	$= ([K Q O_4' O_3]^{O_{MO}} O_1')$		526 $\bar{C}$ $\bar{N}$ $\bar{A}$	
(O_{YAC})	$= ([K E O_4' O_3' O_2' O_1']^{O_Y} A_C)$		533 11 H J	
(O_{YRS})	$= ([K E O_4' O_3' O_2' O_1']^{O_Y} C_5' C_3)$		533 1 H $\bar{A}$ $\bar{J}$	
(O_{YST})	$= ([K E O_4' O_3' O_2' O_1']^{O_Y} C_5 A_C)$		533 M H $\bar{E}$ $\bar{J}$	
(O_{XPR})	$= ([K E O_4 O_3' O_2' O_2' O_1']^{O_X} [B_6' B_5' B_3]^{B_{UO3}} C_5 C_4 C_3)$		533 30 $\bar{Y}$ $\bar{H}$ $\bar{E}$ $\bar{F}$ $\bar{J}$	
(O_{XUO})	$= ([K E O_4 O_3' O_2' O_1']^{O_X} [C_5' C_4']^{C_{UO}})$		533 43 $\bar{Y}$ $\bar{X}$	
(O_{XU2})	$= ([K E O_4 O_3' O_2' O_1']^{O_X} [C_5 C_4']^{C_{U2}})$		533 $\bar{M}$ $\bar{Y}$ $\bar{N}$	
(S_{C3})	$= (S_3' S_2 S_1)$		528 B F 6 L	
(T_{CD})	$= ([B_6' B_5']^{B_{SUO}} B_3')$		529 P 9 C	
(T_{EH})	$= (B_6 B_3')$		529 4 A C	
(T_1)	$= ([B_6' B_5' B_3]^{B_{UO3}} B_4')$		529 21 34 V	
(T_2)	$= ([B_6' B_5' B_3]^{B_{UO3}} [B_2' B_1']^{B_{L0}})$		529 $\bar{L}$ 34 39	
(T_4)	$= ([B_6' B_5']^{B_{SUO}} [B_2 B_1']^{B_{L2}})$		529 $\bar{B}$ 9 35	
(T_5)	$= ([B_6' B_5']^{B_{SUO}} B_4 [B_2' B_1]^{B_{L1}})$		529 Z 9 8 42	

Term	Equation	Receptacle	Pin No.	Definition
(N_{JT})	$= (K' V_C' J_T B_4')$		528 $\bar{U}$ 32 33 $\bar{L}$ $\bar{M}$	
(N_{PC})	$= ([K' J']_{N_J'} V_C R_C' G_{P5} C_{P4})$		526 43 $\bar{K}$ $\bar{S}$ Y $\bar{L}$ $\bar{M}$	
(N_{SC})	$= '([K' J']_{N_L} V_C R_C)$		526 $\bar{Y}$ $\bar{K}$ $\bar{S}$ Z	
(N_{ST})	$= ([K' V_C] O_4)$		526 B K $\bar{B}$	
(N_{CU3})	$= (N_C C_5 C_4)$		533 13 T $\bar{E}$ $\bar{F}$	
(N_{ENT})	$= ([K' J']_{N_J'} V_C')$		526 $\bar{X}$ $\bar{K}$ 22	
(N_{LRC}')	$= ([K' V_C]_{N_L} R_C')$		526 E K Y	
(O_A)	$= ([K E] O_4 O_3)$		526 $\bar{E}$ 10 $\bar{B}$ 18	
(O_F)	$= ([K E] O_4 O_3' O_2' O_1)$		526 M 10 $\bar{B}$ 9 W J	
(O_M)	$= ([K E] O_4' O_3)$		526 $\bar{D}$ 10 41 18	
(O_P)	$= (O_3' O_2 O_1 E)$		526 N 9 13 J 3	
(O_{CX})	$= ([K_A] O_4' O_2 [O_3' O_1']_{O_{31}'} [T_X A])$		528 D J 8 10 K 9	
(O_{LC})	$= ([K E O_4' O_3' O_1]_{O_L} A_C)$		526 $\bar{U}$ 35 34	
(O_{LF})	$= ([K E O_4' O_3' O_1]_{O_L} N_C)$		526 29 35 $\bar{J}$	
(O_{UO})	$= ([K O_4 O_3' O_2 O_1']_{O_U} [T_O A])$		526 $\bar{V}$ 38 37	
(O_{BSM})	$= ([K_A] [L_P' O_{B3} O_{B2} [D_{TP}']])$		528 $\bar{V}$ J 35 $\bar{P}$ 34 $\bar{N}$	
(O_{MFP})	$= ([K N_C O_4' O_3]_{O_{MF}} T_P)$		526 28 32 36	

Term	Equation	Receptacle	Pin No.	Definition
(V_{A1})	$= (V_C\ V_X)$		526 40 22 24	
(V_{A2})	$= (V_C\ A_X')$		526 30 $\overline{S}$ $\overline{P}$	
(V_{A3})	$= (V_C\ A_X)$		526 L $\overline{S}$ 5	
(V_{1P})	$= ([K\ E\ O_4\ O_3'\ O_2'\ O_1'\ C_5'\ C_4\ A_K]\ [C_3\ C_2'\ C_1']\{B_4'\ B_3\ B_2])$		533 $\overline{K}$ $\overline{S}$ $\overline{R}$ $\overline{T}$	
(V_{2P})	$= ([K\ E\ O_4\ O_3'\ O_2'\ O_1'\ C_5'\ C_4\ A_K][C_3\ C_2'\ C_1][B_4'\ B_3\ B_2])$		533 41 $\overline{S}$ $\overline{U}$ $\overline{T}$	
(V_{3P})	$= ([K\ E\ O_4\ O_3'\ O_2'\ O_1'\ C_5'\ C_4\ A_K]\ [C_3\ C_2\ C_1']\ [B_4'\ B_3\ B_2])$		533 $\overline{L}$ $\overline{S}$ 33 $\overline{T}$	
(V_{1S})	$= ([K\ E\ O_4\ O_3'\ O_2'\ O_1'\ C_5'\ C_4\ A_K]\ [C_3\ C_2'\ C_1']\ B_4)$		533 40 $\overline{S}$ $\overline{R}$ $\overline{P}$	
(V_{2S})	$= ([K\ E\ O_4\ O_3'\ O_2'\ O_1'\ C_5'\ C_4\ A_K]\ [C_3\ C_2'\ C_1']\ B_4)$		533 39 $\overline{S}$ $\overline{U}$ $\overline{P}$	
(V_{3S})	$= ([K\ E\ O_4\ O_3'\ O_2'\ O_1'\ C_5'\ C_4\ A_K]\ [C_3\ C_2\ C_1']\ B_4)$		533 31 $\overline{S}$ 33 $\overline{P}$	
(W_0)	$= (W_B'\ W_A')$		528 $\overline{Y}$ 38 $\overline{T}$	
(W_1)	$= (W_B'\ W_A)$		528 $\overline{X}$ 38 $\overline{S}$	
(W_3)	$= (W_B\ W_A)$		528 $\overline{W}$ 36 $\overline{S}$	
(W_{BB3}')	$= W_B\ B_3'$		529 15 10 C	
	LOGIC DRIVERS PRIMARY AND GATES			
$[A_X]_A$	$= [A_X]$		526 1 5	
$[A_X']_{A'}$	$= [A_X']$		526 $\overline{T}$ $\overline{P}$	
$[B_{L0}]$	$= [B_2'\ B_1']$		529 $\overline{E}$ 30 19	
$[B_{L1}]$	$= [B_2'\ B_1]$		529 $\overline{N}$ 30 37	
$[B_{L2}]$	$= [B_2\ B_1']$		529 $\overline{H}$ 18 19	

Term	Equation	Receptacle	Pin No.	Definition
$[B_{M3}]$	$= [B_4' B_3 B_2]$		529 20 V W 18	
$[B_{LU5}]$	$= [B_6 B_5' B_4]$		529 K A 26 8	
$[B_{LU7}]$	$= [B_6 B_5 B_4]$		529 J A D 8	
$[B_{SUO}]$	$= [B_6' B_5']$		529 $\bar{P}$ 27 26	
$[B_{UO3}]$	$= [B_6' B_5' B_3]$		529 Y 27 26 W	
$[B_{6M1}]$	$= [B_6 B_4' B_3]$		529 H A V W	
$[C_{L0}]$	$= [C_3' C_2' C_1']$		533 4 7 F 6	
$[C_{L1}]$	$= [C_3' C_2' C_1]$		533 B 7 F 8	
$[C_{L2}]$	$= [C_3 C_2 C_1']$		533 9 7 5 6	
$[C_{L3}]$	$= [C_3' C_2 C_1]$		533 10 7 5 8	
$[C_{L4}]$	$= [C_3 C_2' C_1']$		533 2 $\bar{J}$ F 6	
$[C_{L5}]$	$= [C_3 C_2' C_1]$		533 D $\bar{J}$ F 8	
$[C_{L6}]$	$= [C_3 C_2 C_1']$		533 K $\bar{J}$ 5 6	
$[C_{L7}]$	$= [C_3 C_2 C_1]$		533 L $\bar{J}$ 5 8	
$[C_{U0}]$	$= [C_5' C_4']$		533 29 $\bar{A}$ $\bar{B}$	
$[C_{U1}]$	$= [C_5' C_4]$		533 28 $\bar{A}$ $\bar{F}$	
$[C_{U2}]$	$= [C_5 C_4']$		533 P $\bar{E}$ $\bar{B}$	
$[D_{C A}']$	$= [D_C']$		533 32 34	
$[D_{TP}]$	$= [D T_P]$		529 24 25 2	
$[D_{TP}']$	$= [D' T_P]$		529 13 T 2	
$[E_{FB}]$	$= [E N_D' T_X]$		533 25 Z 21 19	

Term	Equation	Receptacle	Pin No.	Definition
$[K_A]$	= $[K]$		526 A 2	
$[K_E]$	= $[K\ E]$		526 $\overline{F}$ 2 3	
$[N_J']$	= $[K'\ J']$		526 17 23 21	
$[N_L]$	= $[K'\ V_C]$		526 31 23 $\overline{S}$	
$[N_{MH}]$	= $[K'\ V_C'\ R_C'\ J]$		526 16 23 22 Y 8	
$[N_{RS}]$	= $[K'\ V_C'\ R_C]$		526 12 23 22 Z	
$[O_L]$	= $[K\ E\ O_4'\ O_3'\ O_1]$		526 P 2 3 41 9 J	
$[O_U]$	= $[K\ O_4\ O_3'\ O_2\ O_1']$		526 T 2 $\overline{B}$ 9 13 $\overline{A}$	
$[O_X]$	= $[K\ E\ O_4\ O_3'\ O_2'\ O_1']$		526 S 2 3 $\overline{B}$ 9 W $\overline{A}$	
$[O_Y]$	= $[K\ E\ O_4'\ O_3'\ O_2'\ O_1']$		526 $\overline{H}$ 2 3 41 9 W $\overline{A}$	
$[O_{MF}]$	= $[K\ N_C\ O_4'\ O_3]$		526 42 2 $\overline{J}$ 41 18	
$[O_{MO}]$	= $[K\ Q\ O_4'\ O_3]$		526 F 2 H 41 18	
$[O_{31}']$	= $[O_3'\ O_1']$		526 V 9 $\overline{A}$	
$[S_{C6}]$	= $\left[[O_Y]\ C_5\ Q\right]$		526 6 19 15 H	
$[T_{OA}]$	= $[T_O]$		529 $\overline{S}$ 41	
$[T_{P\ A}]$	= $[T_P]$		529 12 2	
$[T_{P\ B}]$	= $[T_P]$		529 7 2	
$[T_{11}]$	= $[B_5\ B_4'\ B_3\ B_2]$		529 S D V W 18	
$[T_{13}]$	= $[B_6\ B_3'\ T_P']$		529 3 A C 1	
$[T_{24}]$	= $[B_5'\ B_4'\ B_2\ B_1']$		529 23 26 V 18 19	
$[T_{X\ A}]$	= $[T_X]$		529 $\overline{M}$ 31	
$[T_{PXO}']$	= $[T_P'\ T_X'\ T_O']$		533 38 35 36 37	
$[V_T]$	= $[K\ E\ O_4\ O_3'\ O_2'\ O_1'\ C_5'\ C_4\ A_K]$		533 15 23 Z 16 17 U 18 $\overline{A}$ $\overline{F}$ V	