

LOGIC DIAGRAMS
for
MODEL 1200
CENTRAL PROCESSING UNIT

September 1, 1972

Revised: August 10, 1973


basic / four corporation

A Subsidiary of Management Assistance Inc. (MAI)
1335 South Claudina Street, Anaheim, California 92805

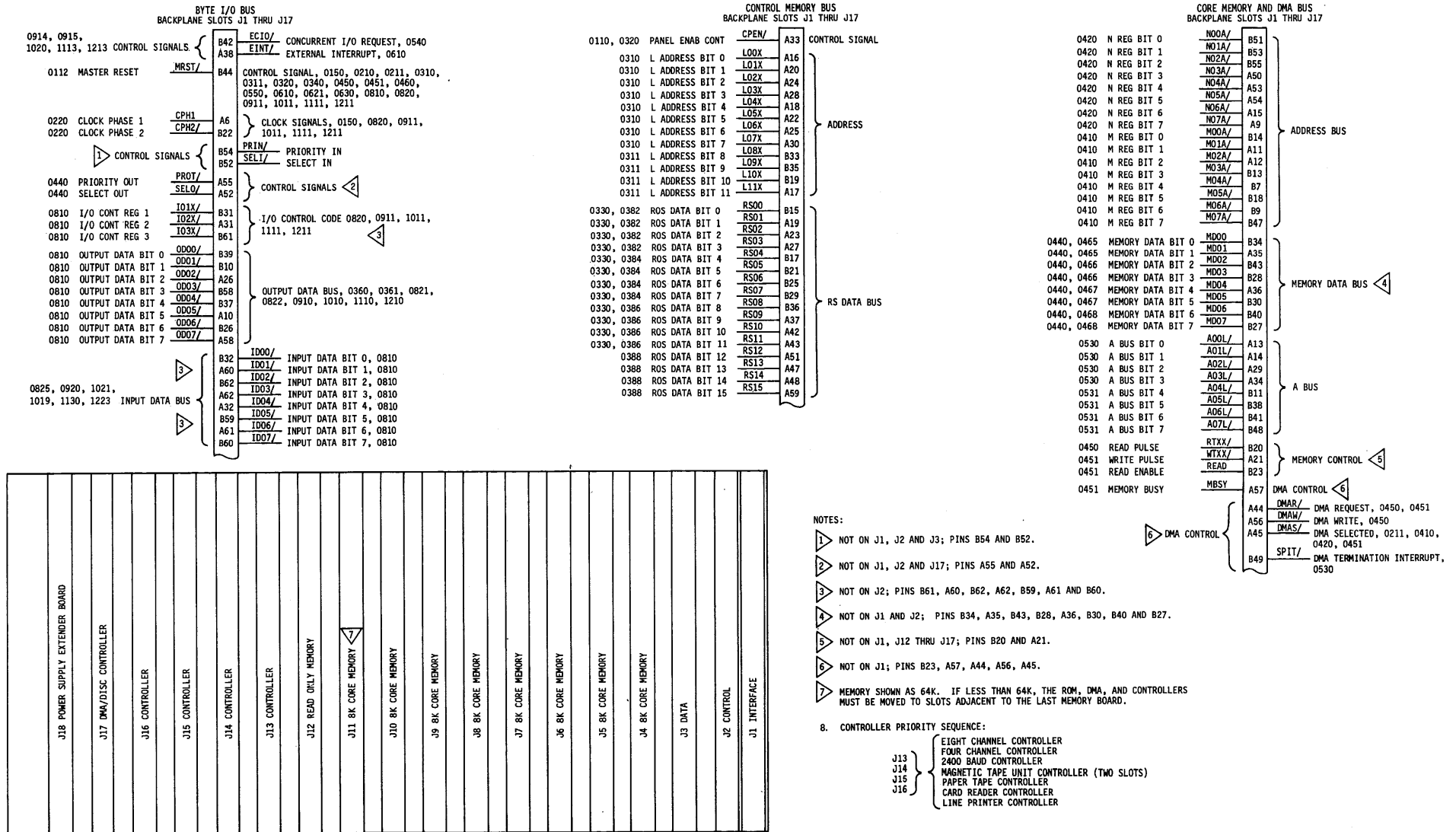


PROPRIETARY INFORMATION

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INTERCONNECTION DIAGRAM



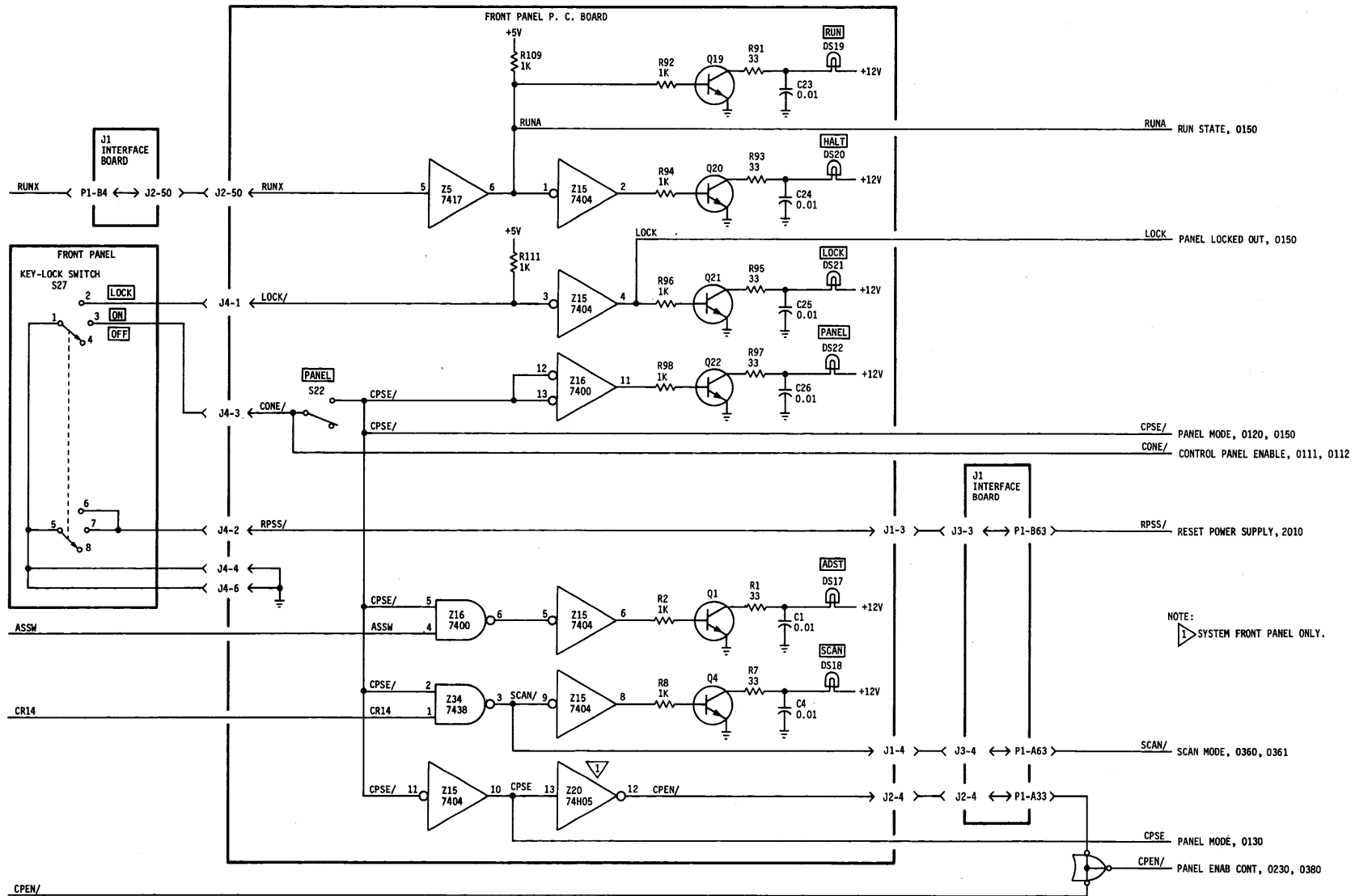
0211 RUN STATE

0150 ADDRESS STOP MODE

0130 DATA SWITCH 14

0320 PANEL ENAB CONT

LD 1010
CENTRAL PROCESSING UNIT



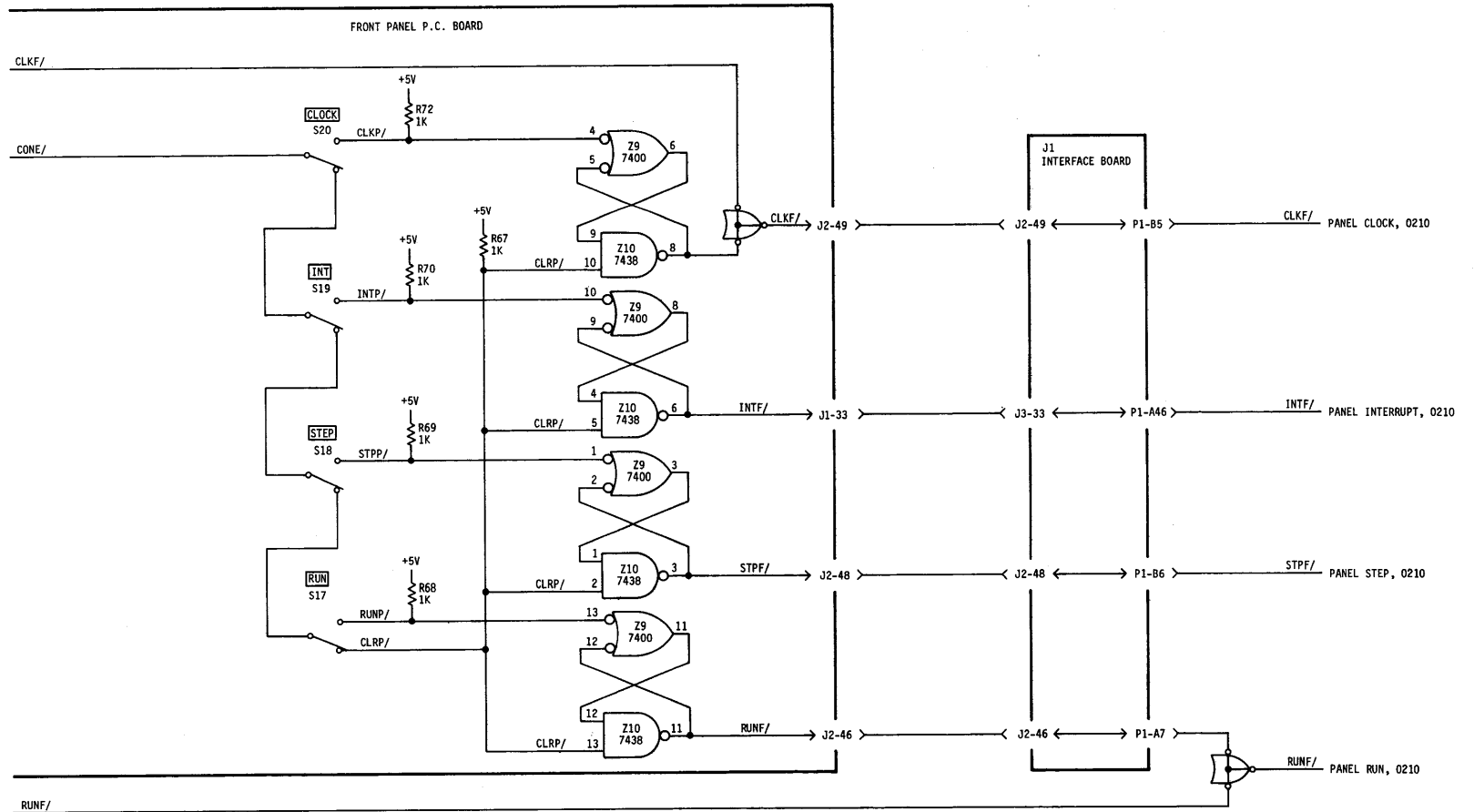
FRONT PANEL CONTROL INDICATORS

FRONT PANEL P.C. BOARD
AND J1 INTERFACE BOARD
0110

FRONT PANEL CONTROL SWITCHES

0150 PANEL CLOCK

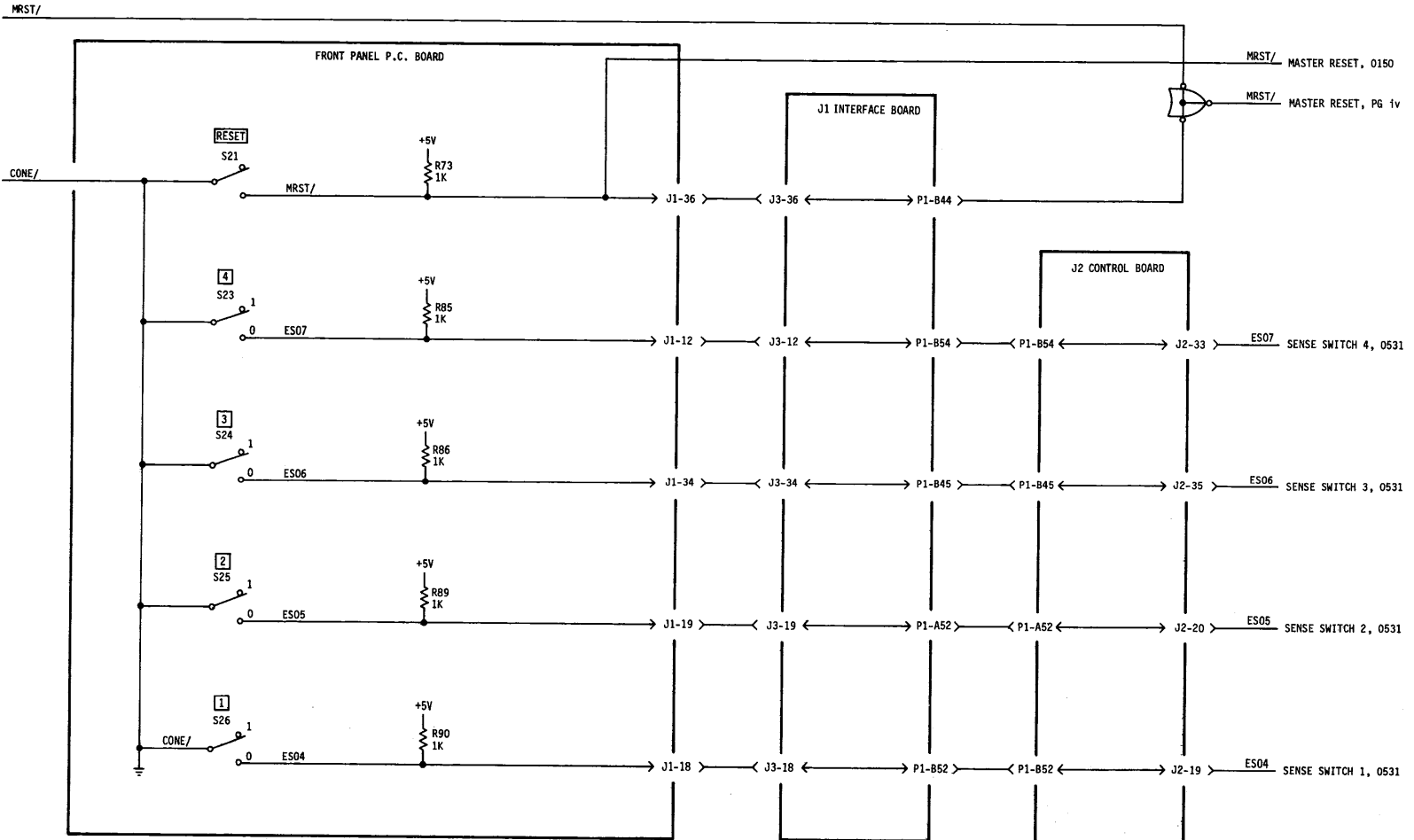
0110 CONTROL PANEL ENABLE



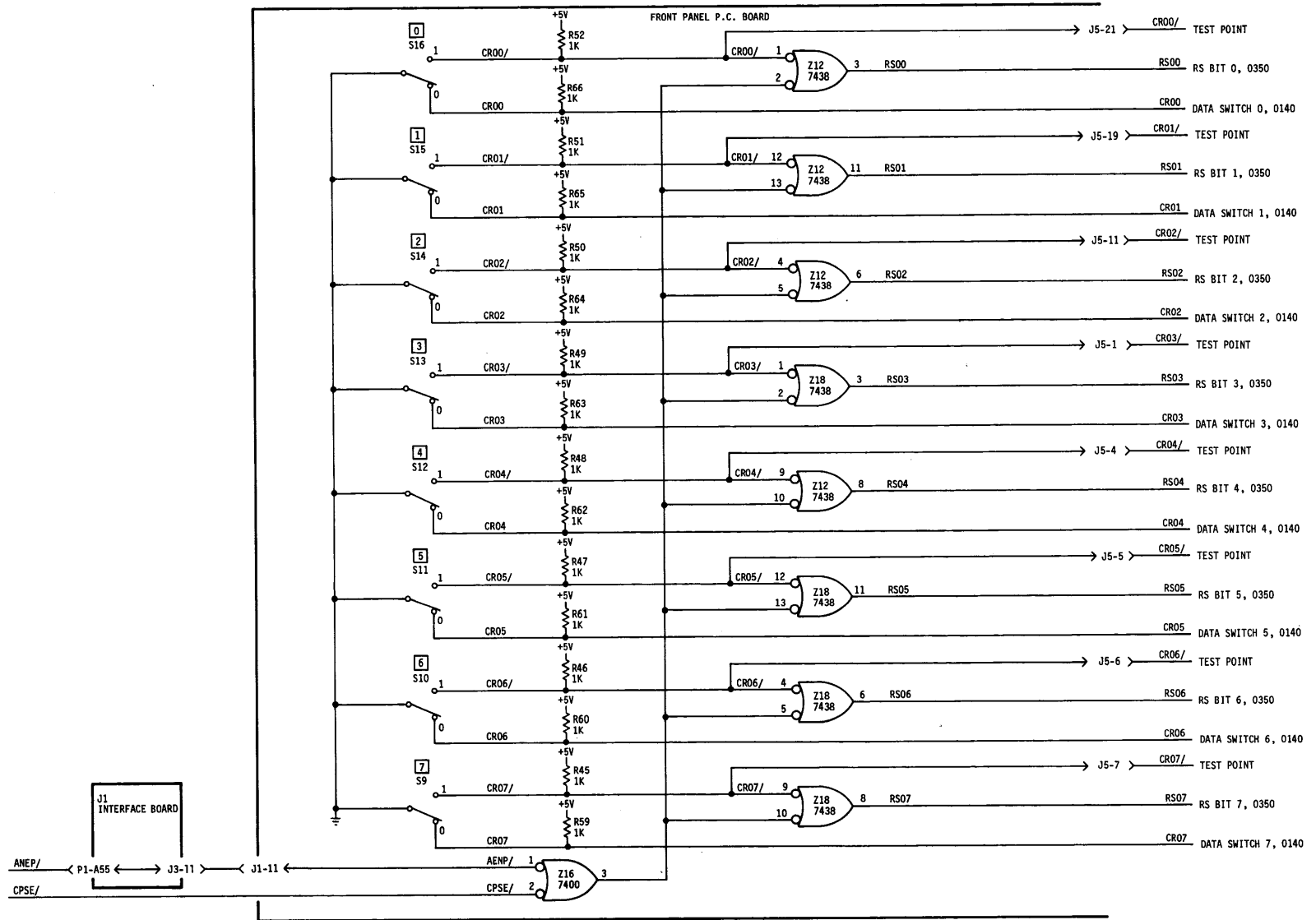
0621 PANEL RUN

0621 MASTER RESET

0110 CONTROL PANEL ENABLE

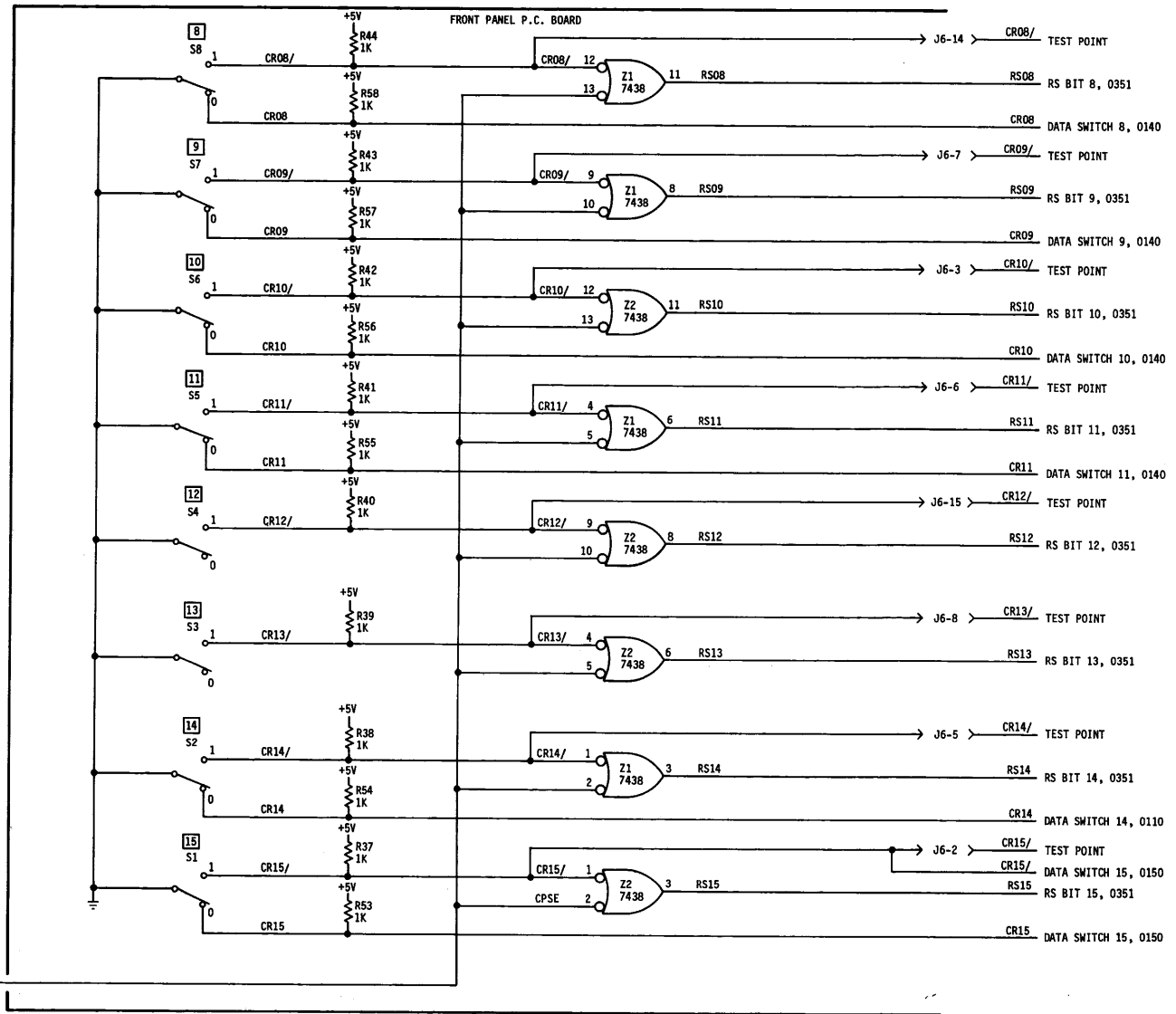


LOWER DATA SWITCHES



0373 ENTER CONSOLE SWITCHES

0110 PANEL MODE



0110 PANEL MODE

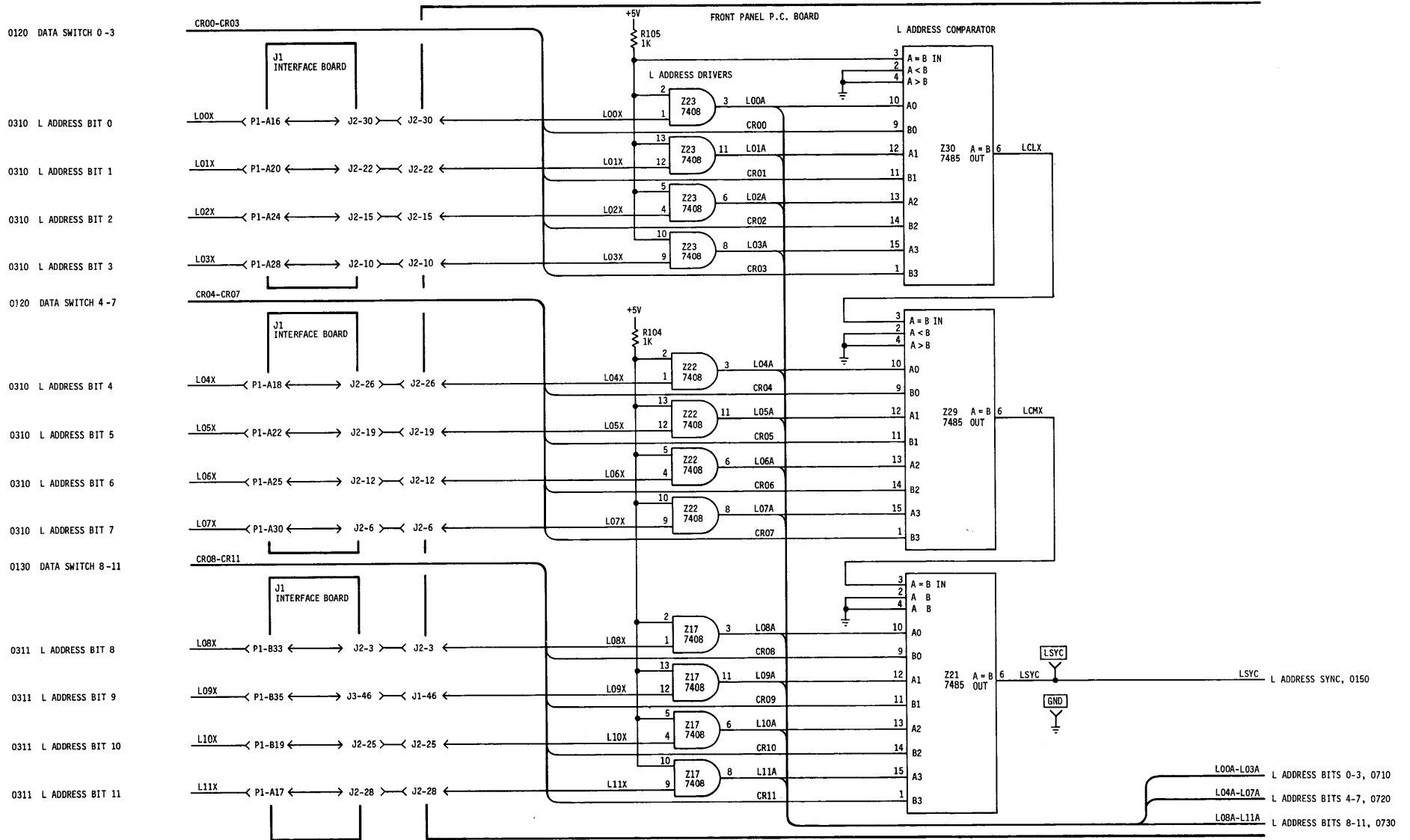
CPSE

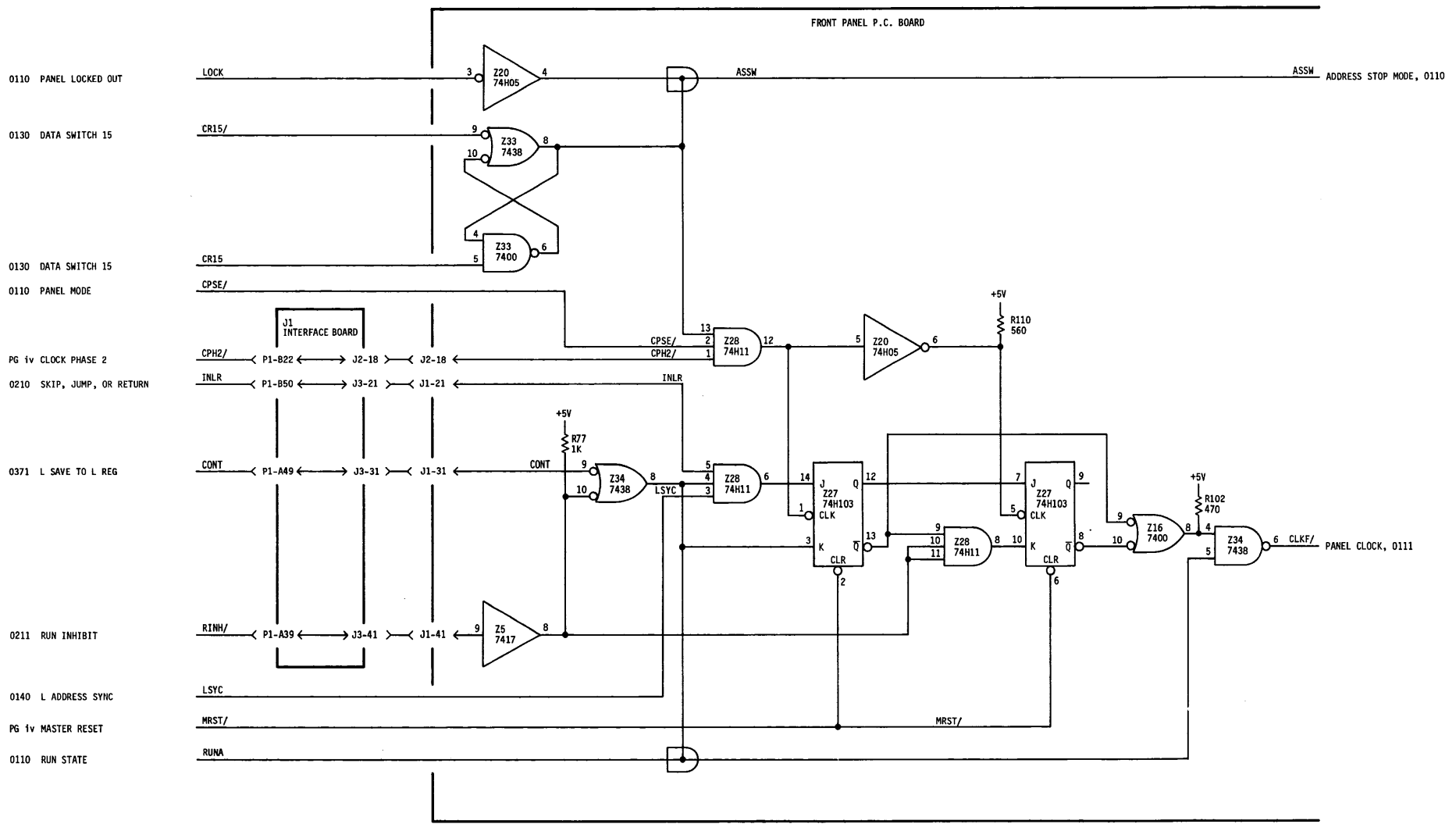
LD 1010
CENTRAL PROCESSING UNIT

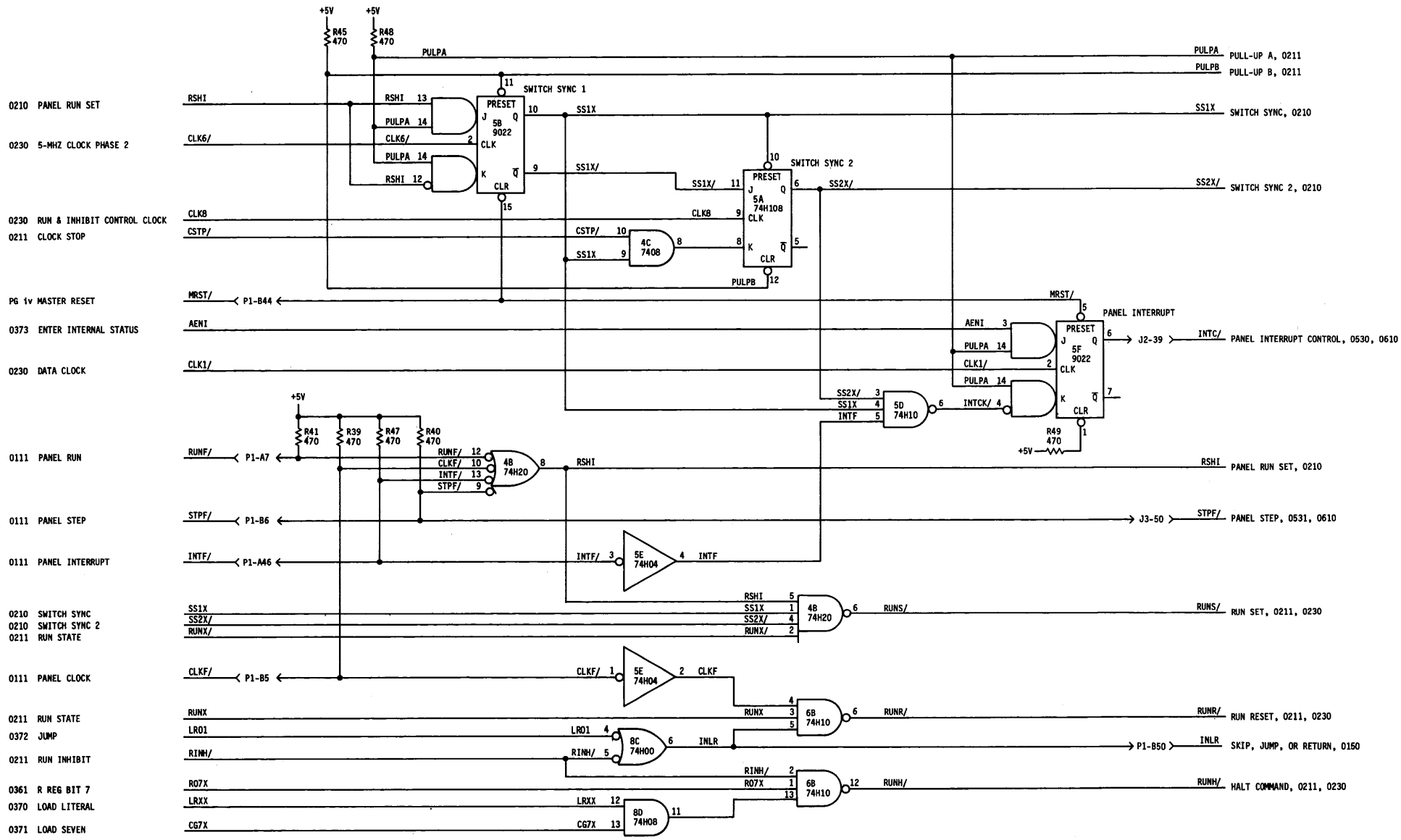
UPPER DATA SWITCHES

FRONT PANEL P.C. BOARD
0130

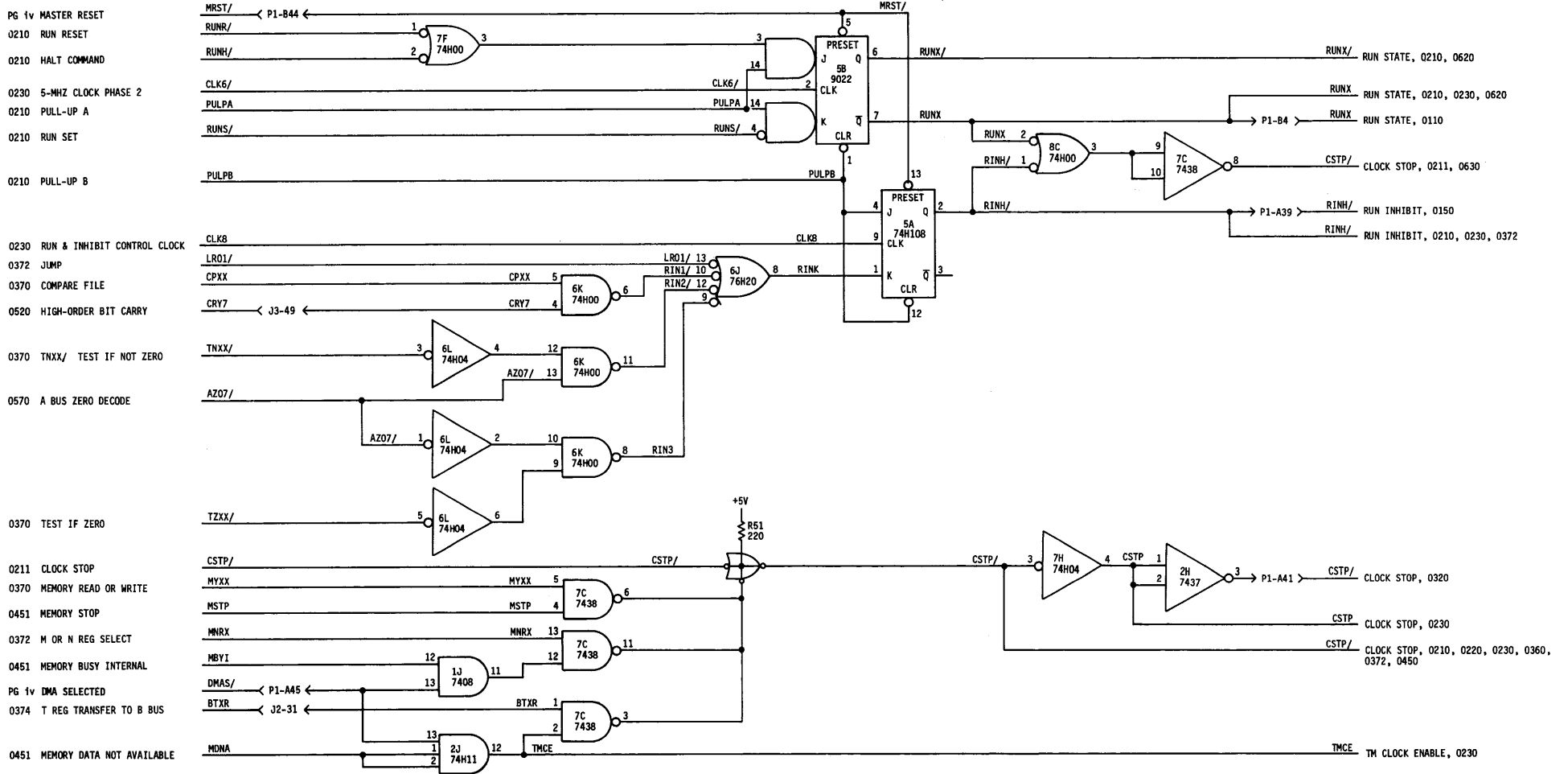
L ADDRESS DRIVERS AND COMPARATOR



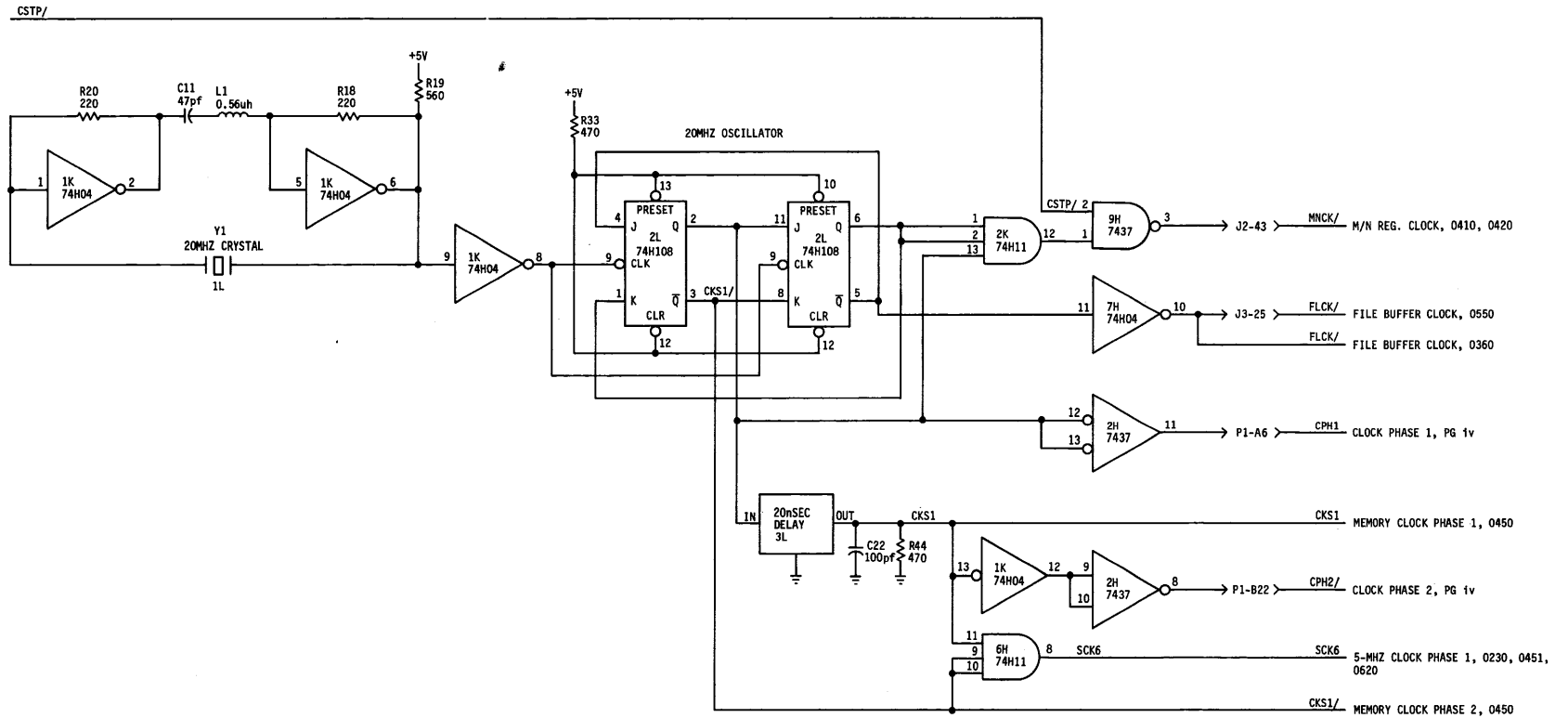




RUN AND INHIBIT CONTROL 1



0211 CLOCK STOP



- 0110 PANEL ENAB CONT
- 0210 RUN RESET
- 0210 HALT COMMAND
- 0372 JUMP
- 0211 CLOCK STOP
- 0210 RUN SET

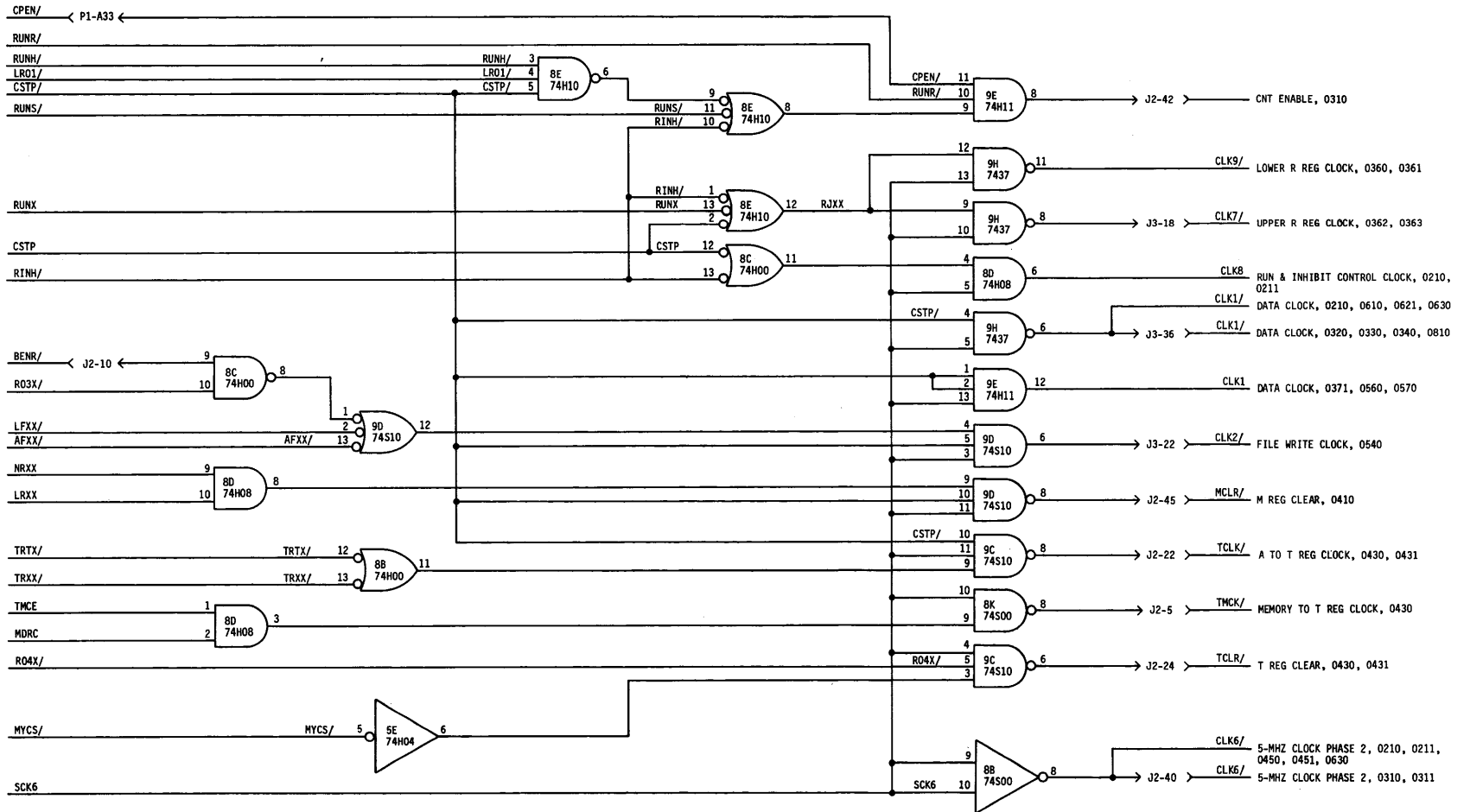
- 0211 RUN STATE
- 0211 CLOCK STOP
- 0211 RUN INHIBIT

- 0374 R REG TO B BUS
- 0360 R REG BIT 3

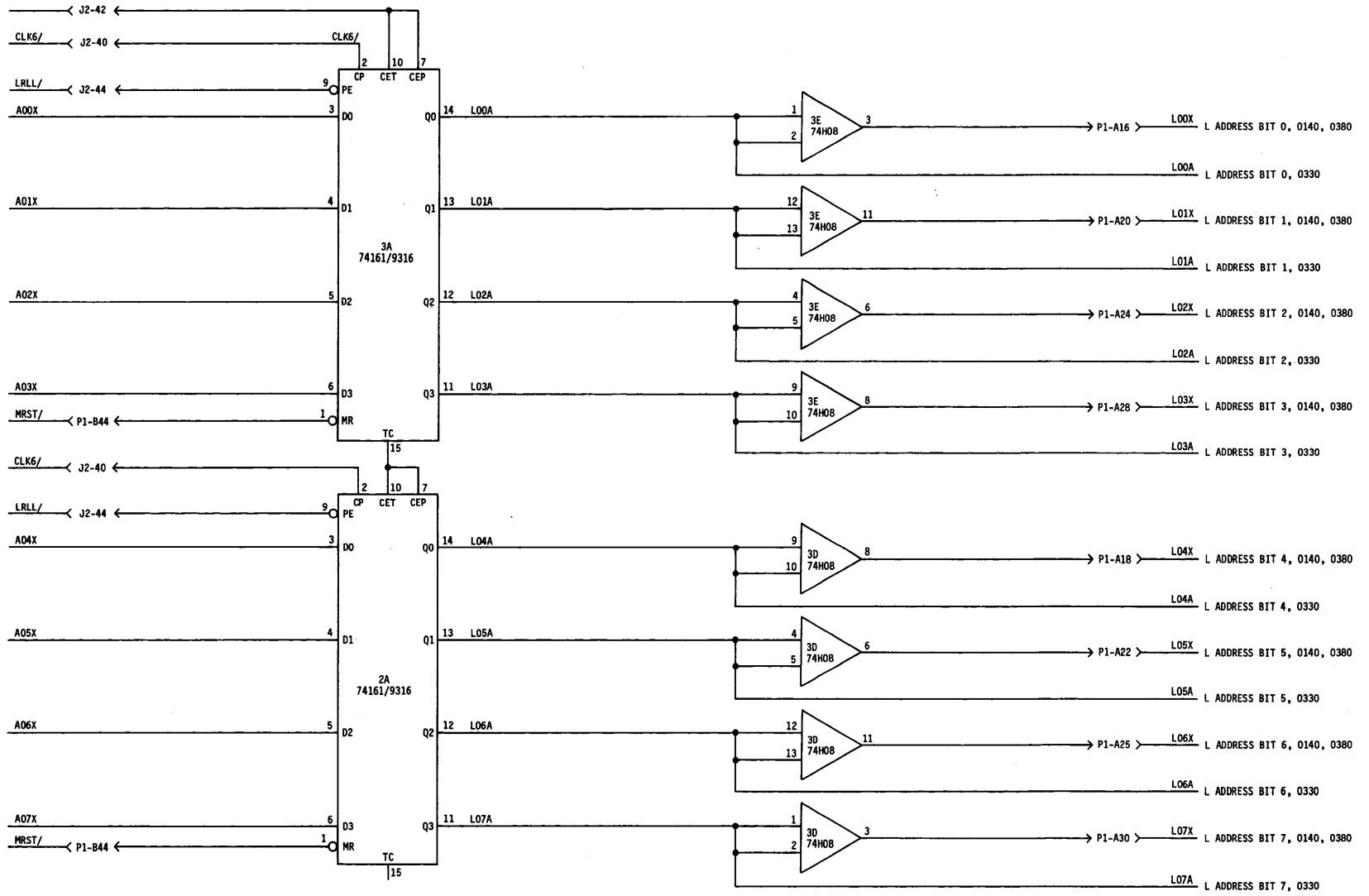
- 0370 LOAD FILE
- 0370 ADD FILE
- 0371 LOAD N
- 0370 LOAD LITERAL

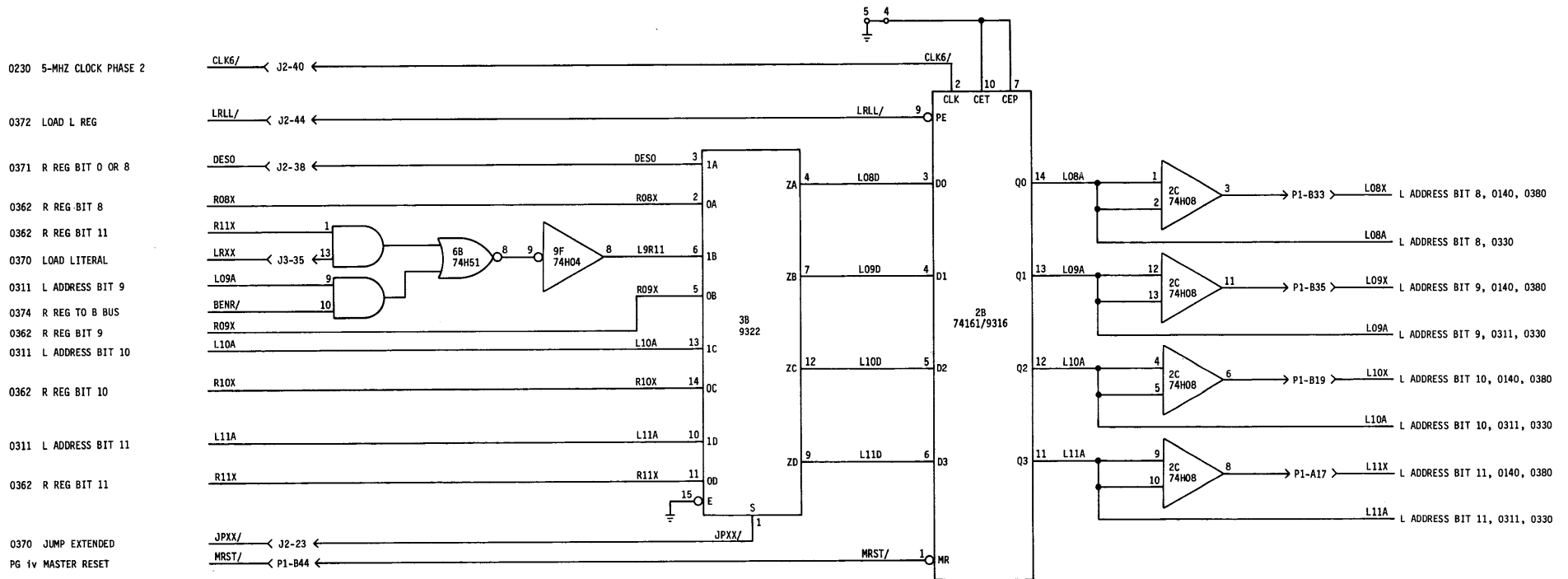
- 0371 RETURN, LOAD T
- 0371 LOAD T
- 0211 TM CLOCK ENABLE
- 0451 READ MEMORY DATA
- 0361 R REG BIT 4

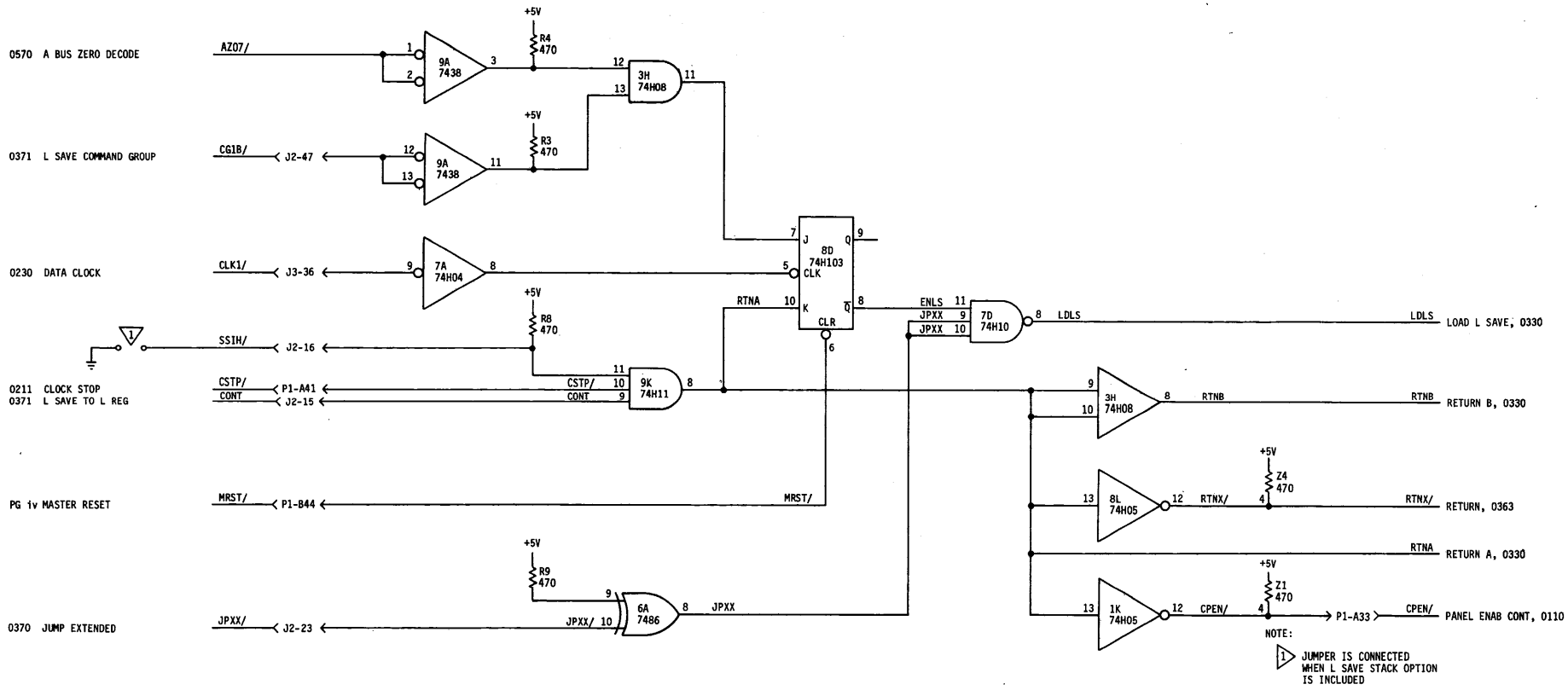
- 0450 MEMORY CYCLE START
- 0220 5-MHZ CLOCK PHASE 1



0230 CNT ENABLE
 0230 5-MHZ CLOCK PHASE 2
 0372 LOAD L REG
 0530 A BUS BIT 0
 0530 A BUS BIT 1
 0530 A BUS BIT 2
 0530 A BUS BIT 3
 PG 1v MASTER RESET
 0230 5-MHZ CLOCK PHASE 2
 0372 LOAD L REG
 0531 A BUS BIT 4
 0531 A BUS BIT 5
 0531 A BUS BIT 6
 0531 A BUS BIT 7
 PG 1v MASTER RESET







CENTRAL PROCESSING UNIT
LD 1010

L SAVE REGISTER

0320 RETURN B

0310 L ADDRESS BIT 0

0310 L ADDRESS BIT 1

0310 L ADDRESS BIT 2

0310 L ADDRESS BIT 3

0230 DATA CLOCK

0320 LOAD L SAVE

0550 PULL-UP 1

0310 L ADDRESS BIT 4

0310 L ADDRESS BIT 5

0310 L ADDRESS BIT 6

0310 L ADDRESS BIT 7

0230 DATA CLOCK

0320 LOAD L SAVE

0550 PULL-UP 1

0311 L ADDRESS BIT 8

0311 L ADDRESS BIT 9

0311 L ADDRESS BIT 10

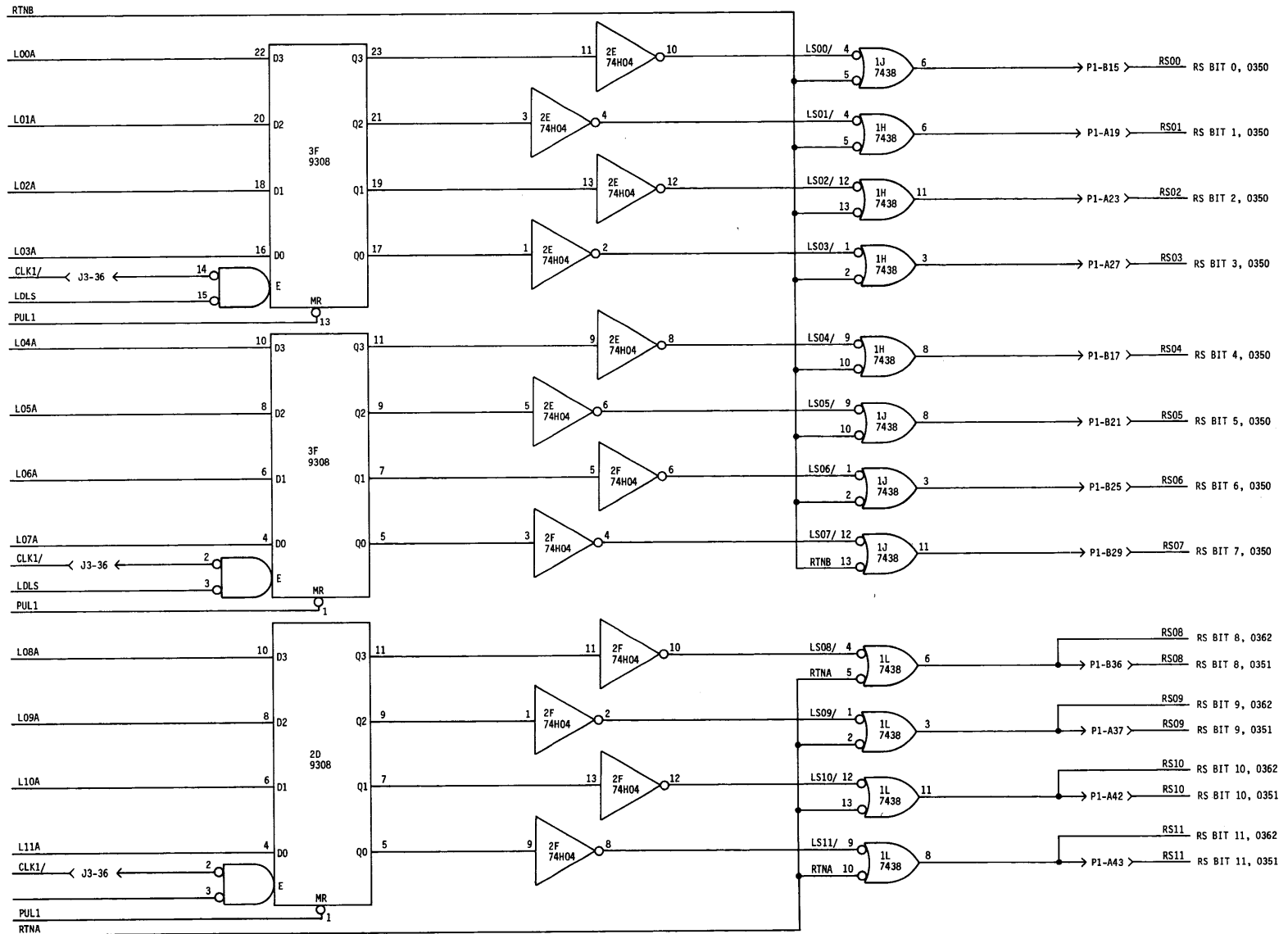
0311 L ADDRESS BIT 11

0230 DATA CLOCK

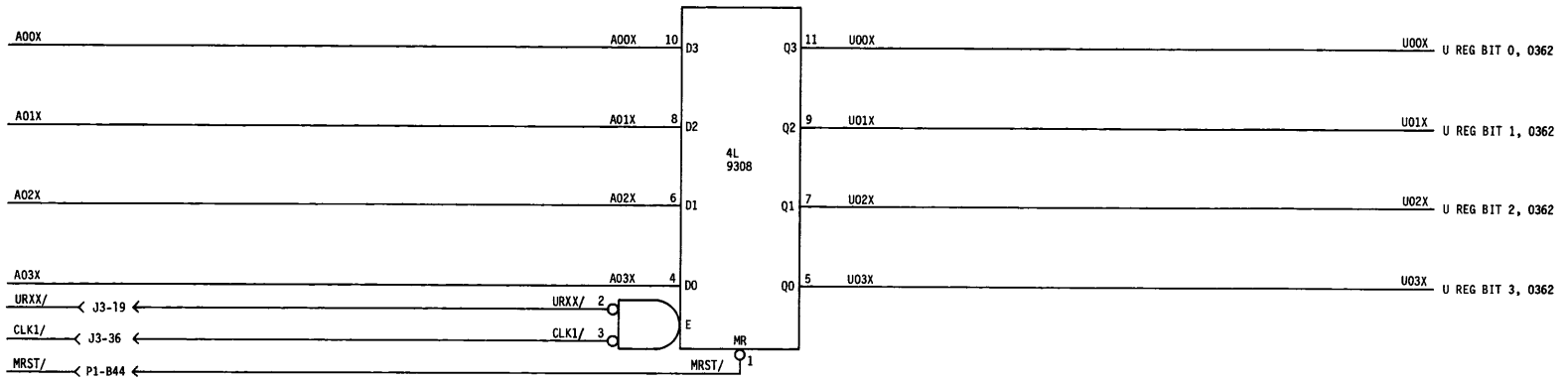
0320 LOAD L SAVE

0550 PULL-UP 1

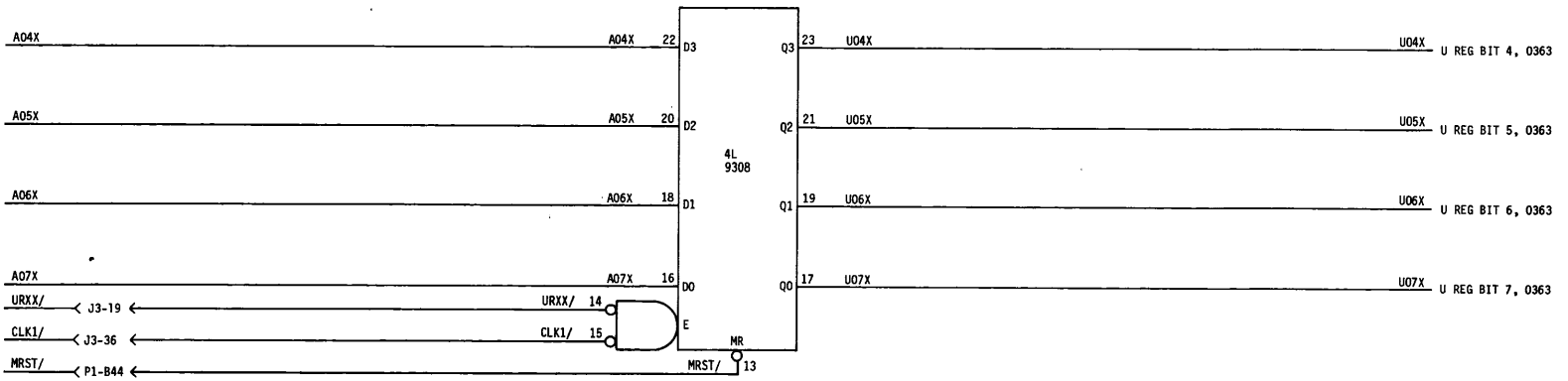
0320 RETURN A

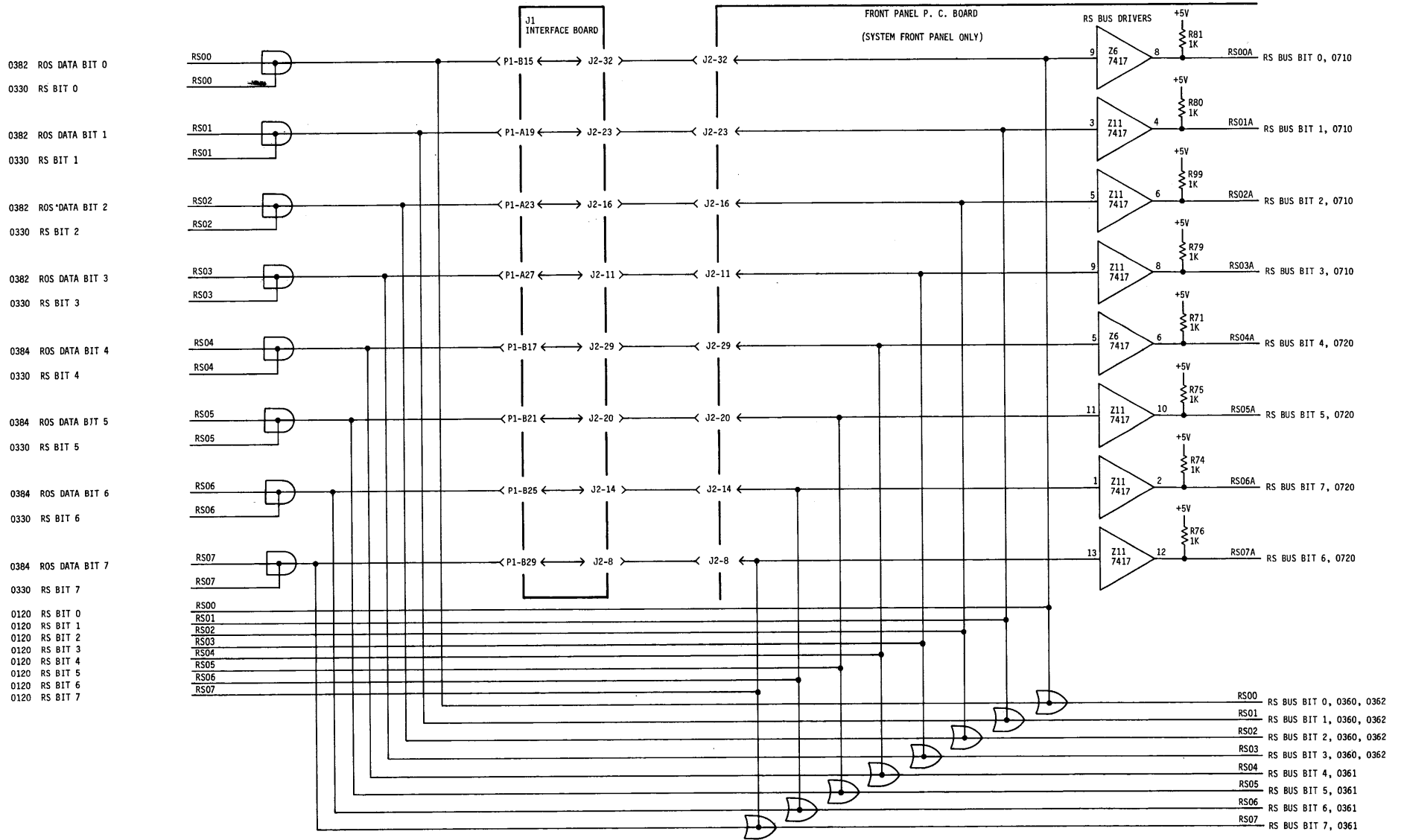


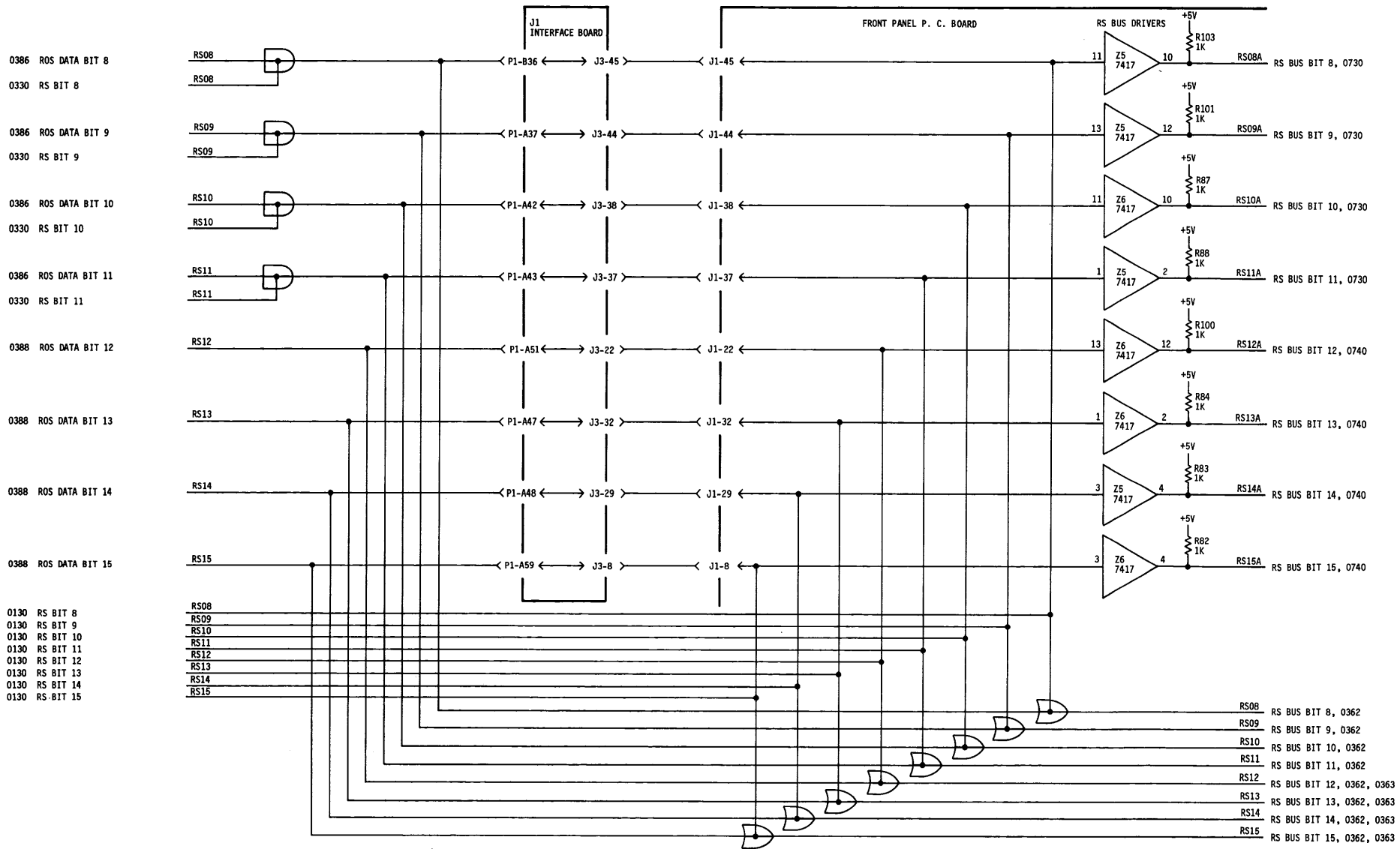
0530 A BUS BIT 0
 0530 A BUS BIT 1
 0530 A BUS BIT 2
 0530 A BUS BIT 3
 0371 LOAD U
 0230 DATA CLOCK
 PG iv MASTER RESET



0531 A BUS BIT 4
 0531 A BUS BIT 5
 0531 A BUS BIT 6
 0531 A BUS BIT 7
 0371 LOAD U
 0230 DATA CLOCK
 PG iv MASTER RESET







LOWER R REGISTER BITS 0-3

0220 FILE BUFFER CLOCK
0211 CLOCK STOP

0371 MODIFY LOWER COMMAND

PG 1v OUTPUT DATA BIT 0

0350 RS BUS BIT 0

PG 1v OUTPUT DATA BIT 1

0350 RS BUS BIT 1

PG 1v OUTPUT DATA BIT 2

0350 RS BUS BIT 2

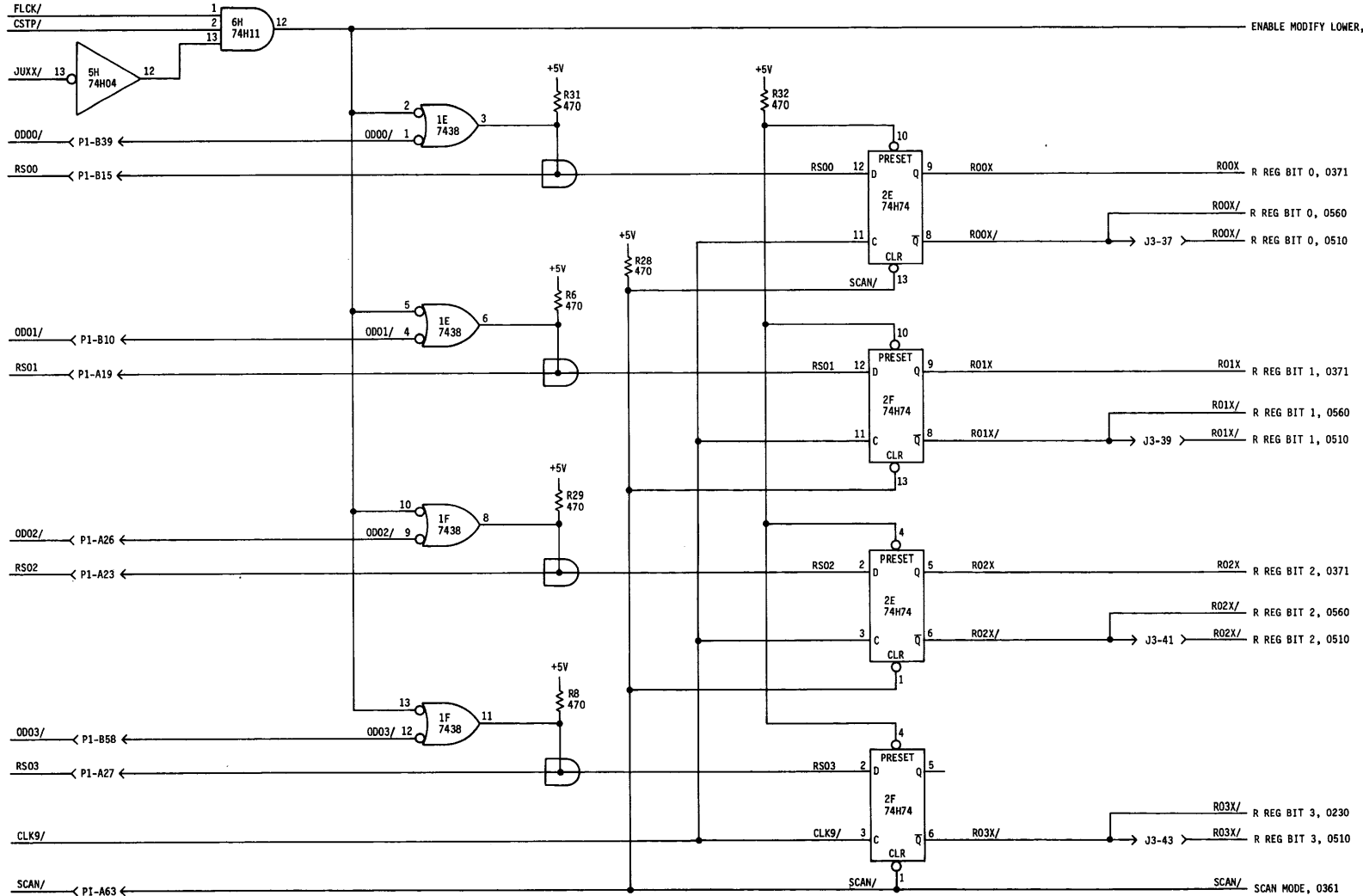
PG 1v OUTPUT DATA BIT 3

0350 RS BUS BIT 3

0230 LOWER R REG CLOCK

0110 SCAN MODE

ENABLE MODIFY LOWER, 0361



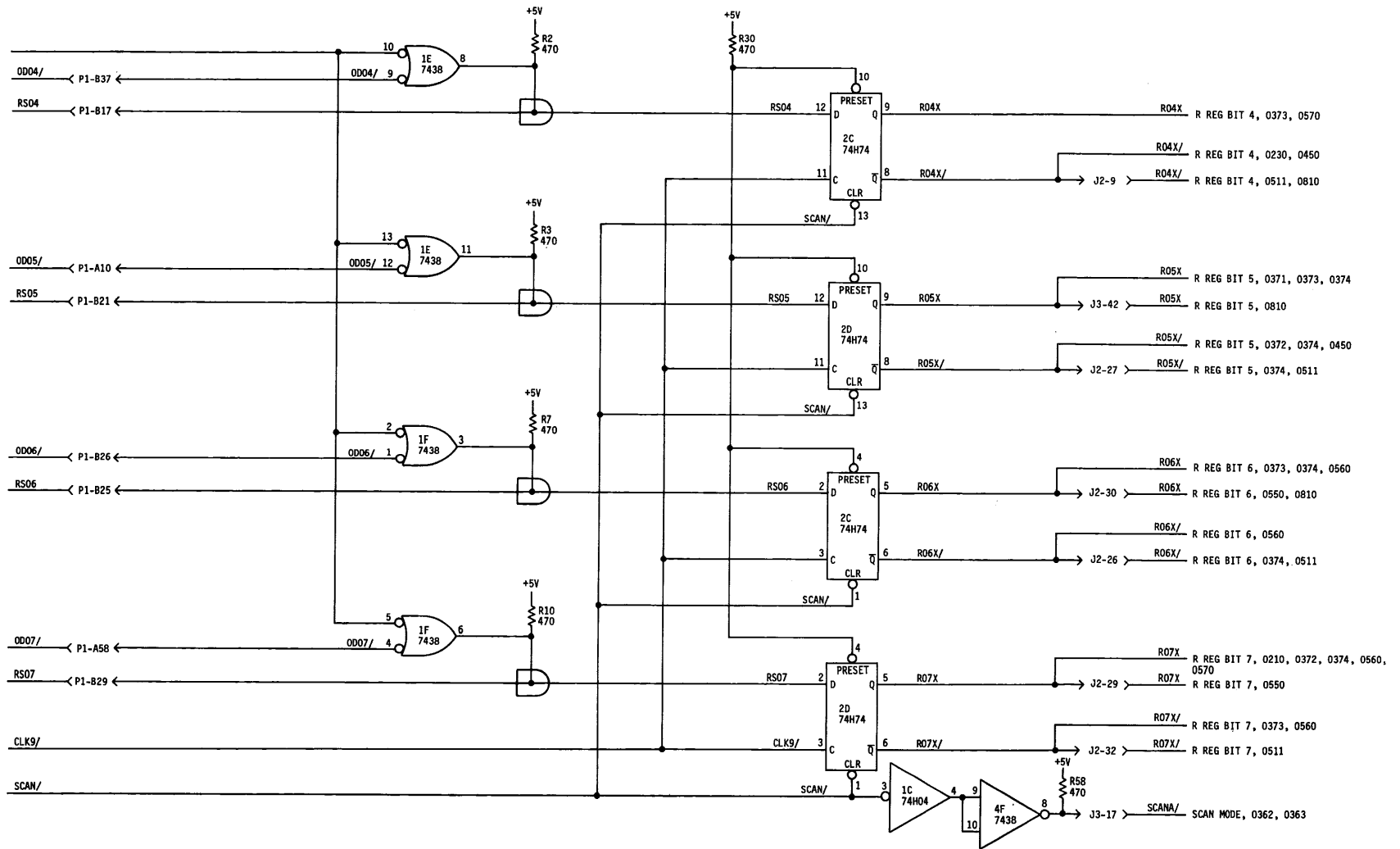
0360 ENABLE MODIFY LOWER
 PG 1v OUTPUT DATA BIT 4
 0350 RS BUS BIT 4

0360 ENABLE MODIFY LOWER
 PG 1v OUTPUT DATA BIT 5
 0350 RS BUS BIT 5

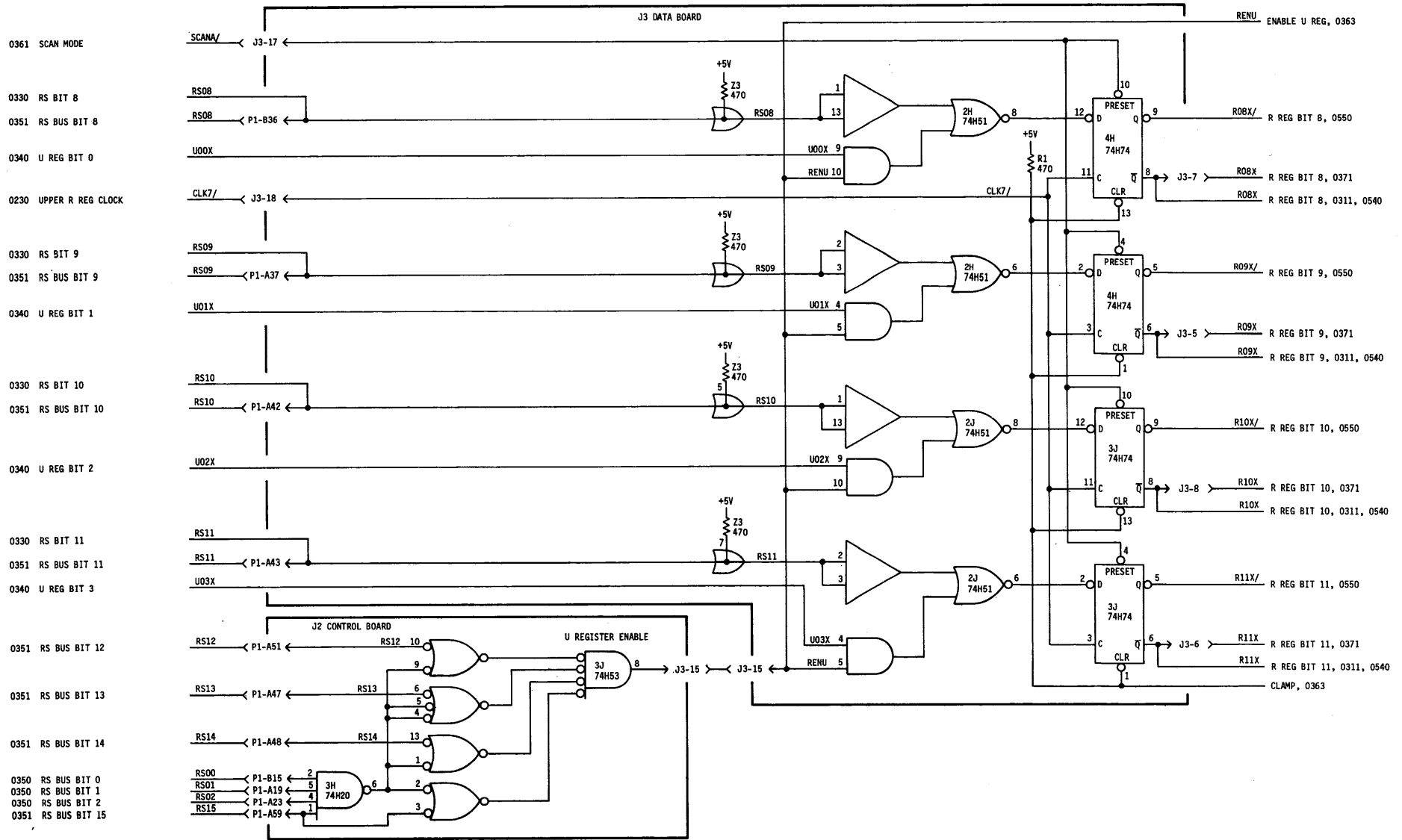
0360 ENABLE MODIFY LOWER
 PG 1v OUTPUT DATA BIT 6
 0350 RS BUS BIT 6

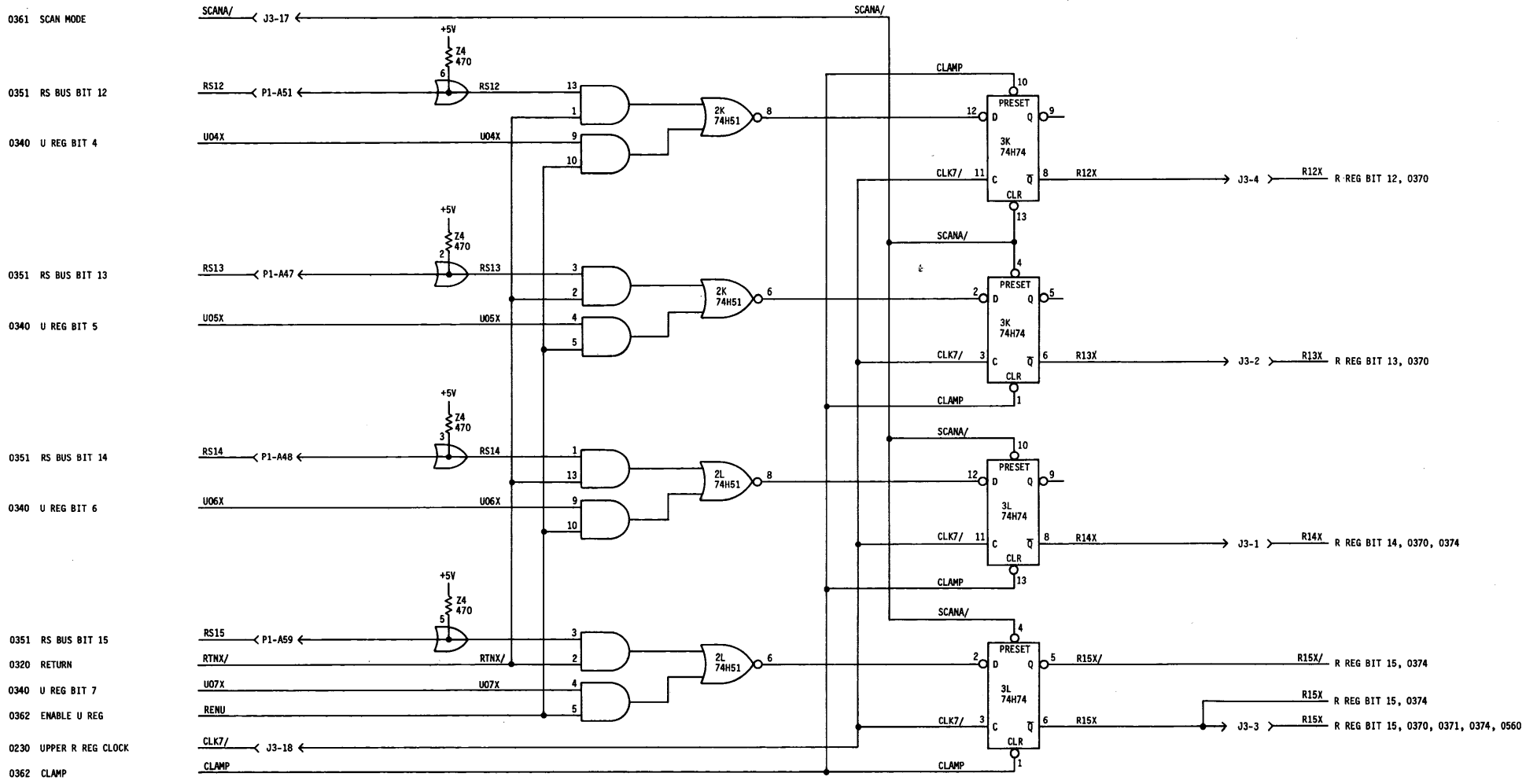
0360 ENABLE MODIFY LOWER
 PG 1v OUTPUT DATA BIT 7
 0350 RS BUS BIT 7

0230 LOWER R REG CLOCK
 0360 SCAN MODE

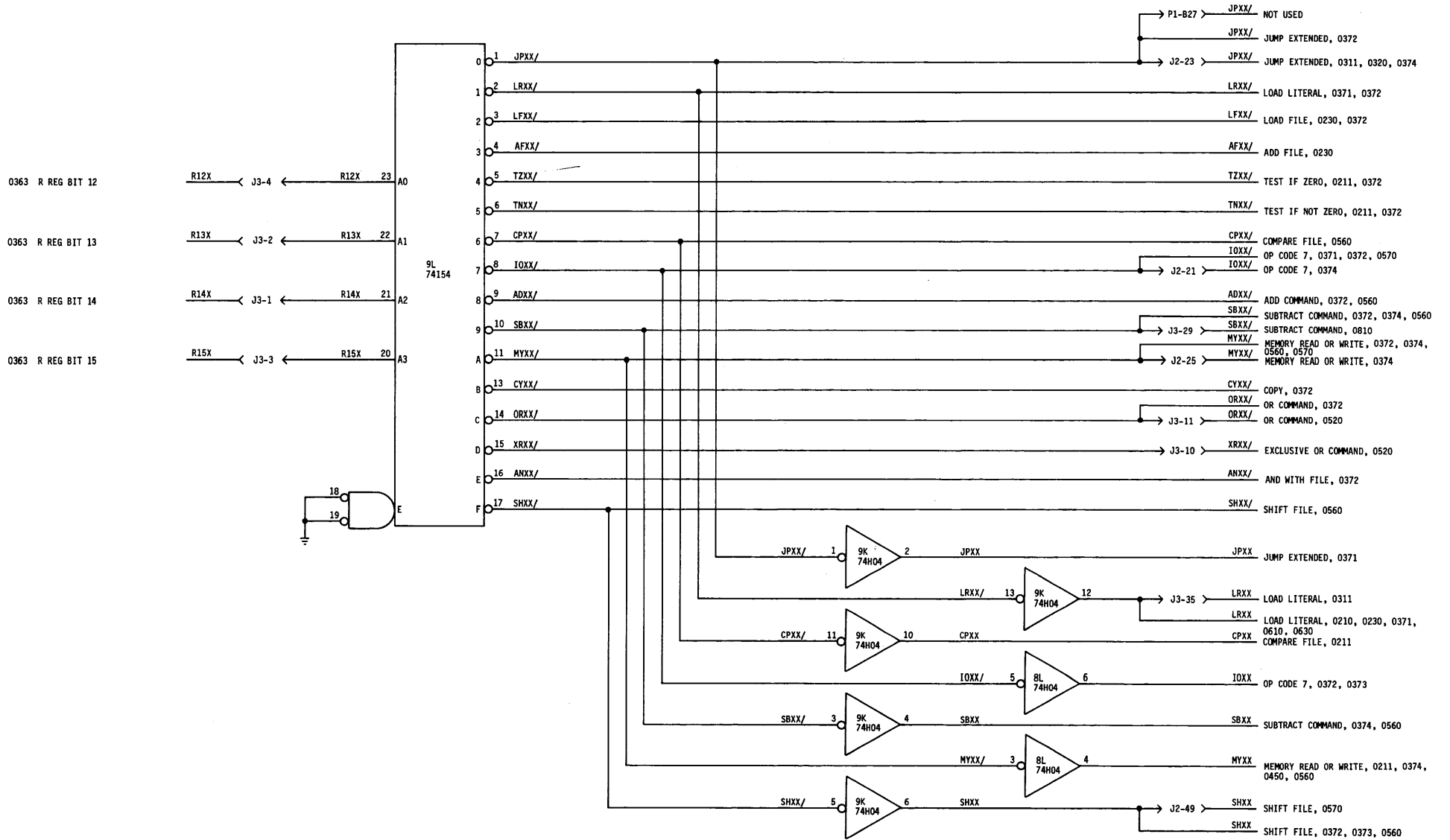


UPPER R REGISTER BITS 8-11

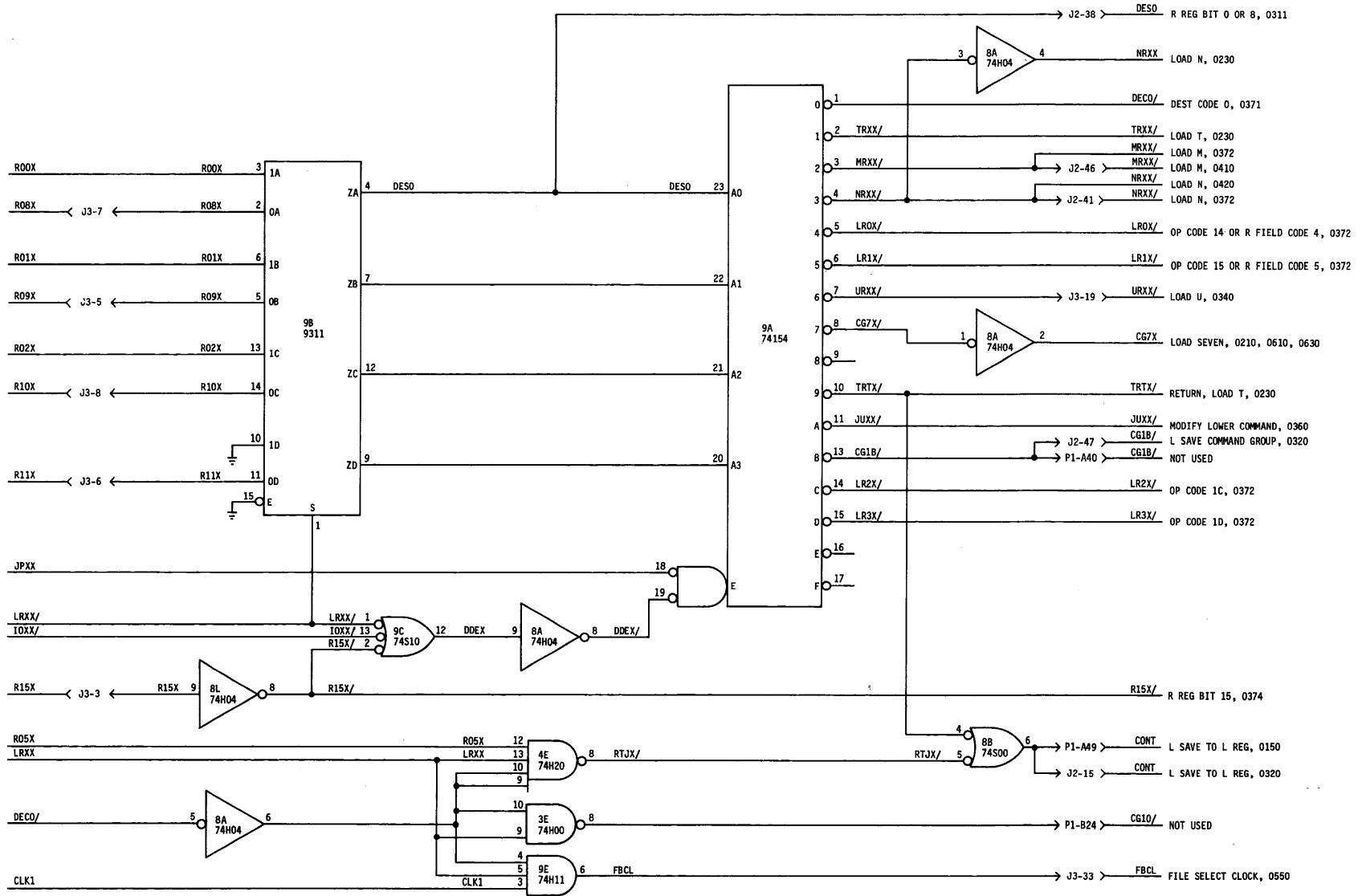




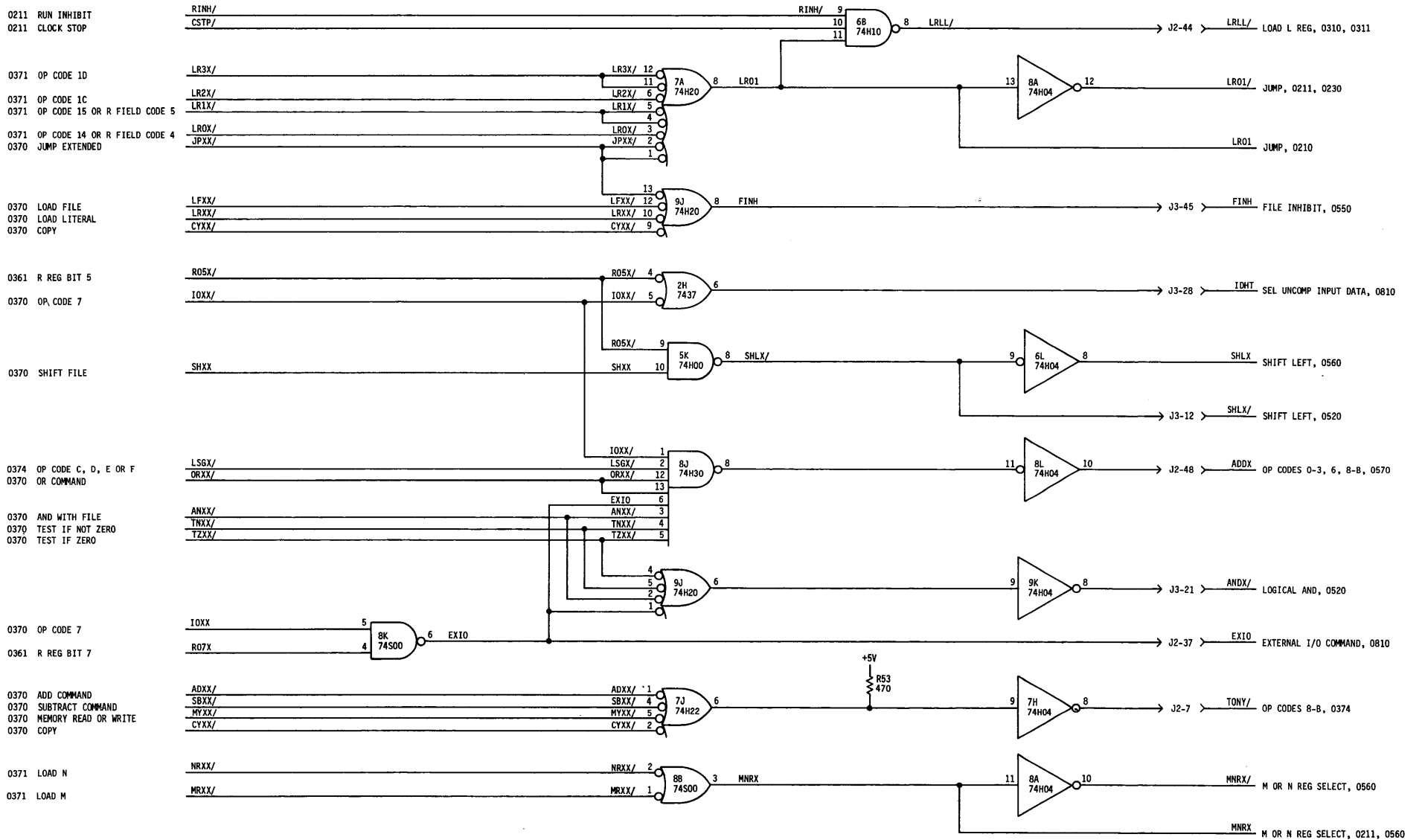
OP CODE DECODER



0360 R REG BIT 0
 0362 R REG BIT 8
 0360 R REG BIT 1
 0362 R REG BIT 9
 0360 R REG BIT 2
 0362 R REG BIT 10
 0362 R REG BIT 11
 0370 JUMP EXTENDED
 0370 LOAD LITERAL
 0370 OP CODE 7
 0363 R REG BIT 15
 0361 R REG BIT 5
 0370 LOAD LITERAL
 0371 DEST CODE 0
 0230 DATA CLOCK



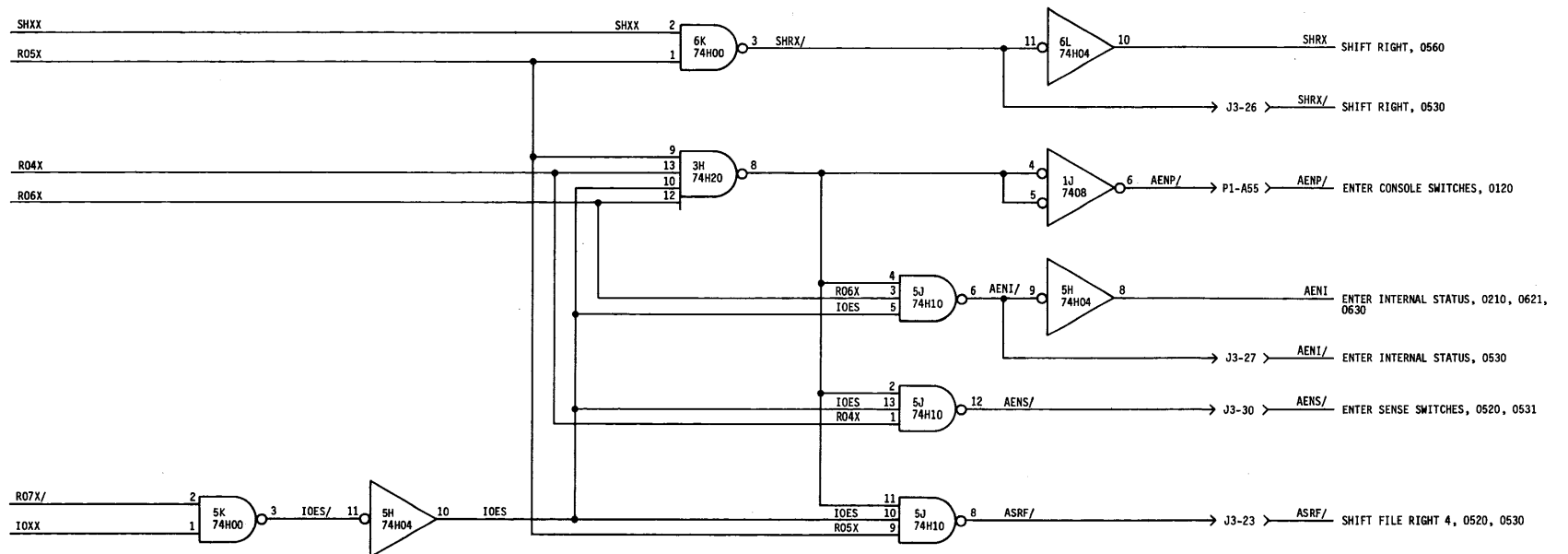
DESTINATION DECODER



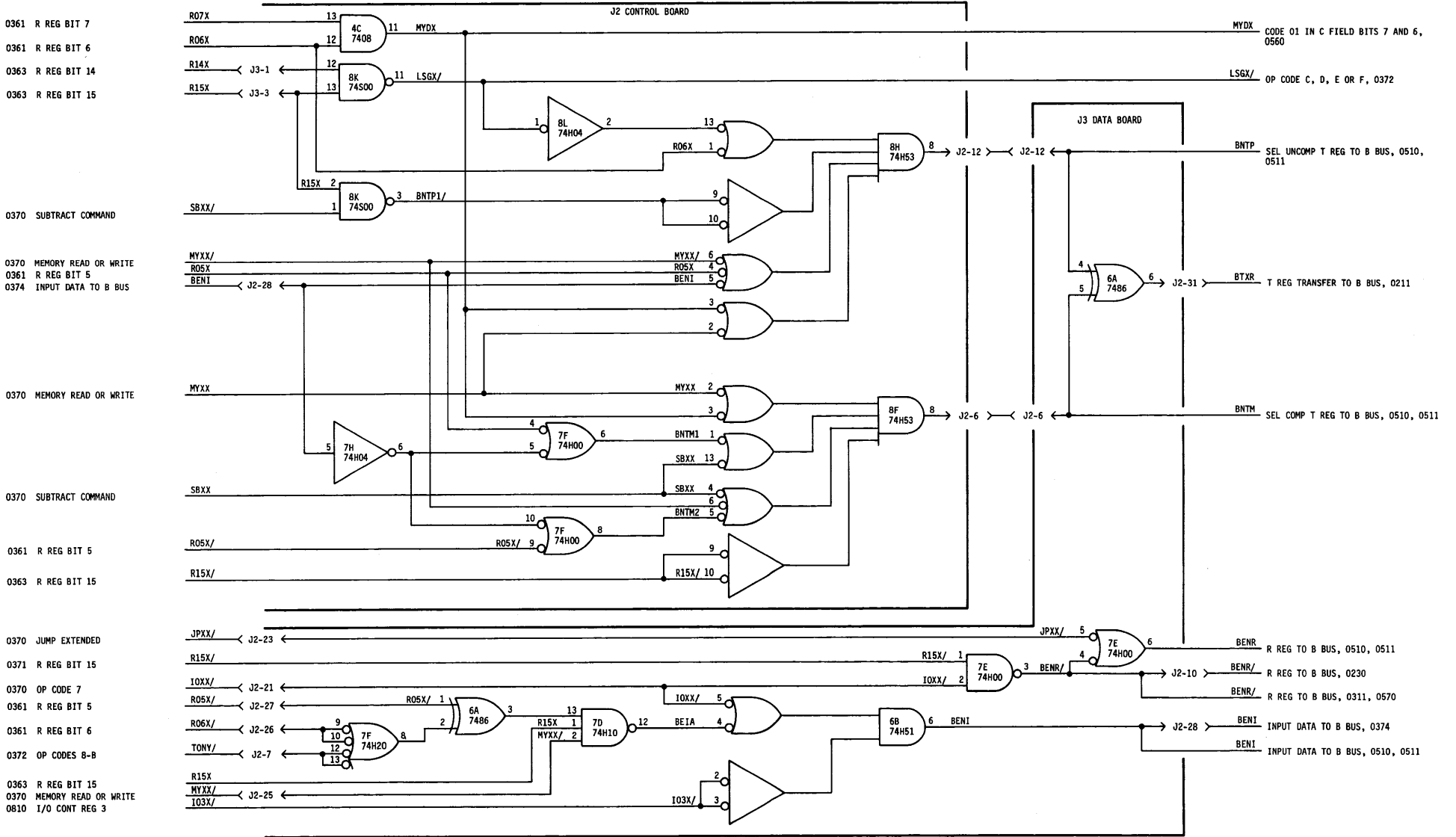
0370 SHIFT FILE
0361 R REG BIT 5

0361 R REG BIT 4
0361 R REG BIT 6

0361 R REG BIT 7
0370 OP CODE 7



B BUS DATA SELECT DECODES



0361 R REG BIT 7
0361 R REG BIT 6
0363 R REG BIT 14
0363 R REG BIT 15

0370 SUBTRACT COMMAND

0370 MEMORY READ OR WRITE
0361 R REG BIT 5
0374 INPUT DATA TO B BUS

0370 MEMORY READ OR WRITE

0370 SUBTRACT COMMAND

0361 R REG BIT 5

0363 R REG BIT 15

0370 JUMP EXTENDED

0371 R REG BIT 15

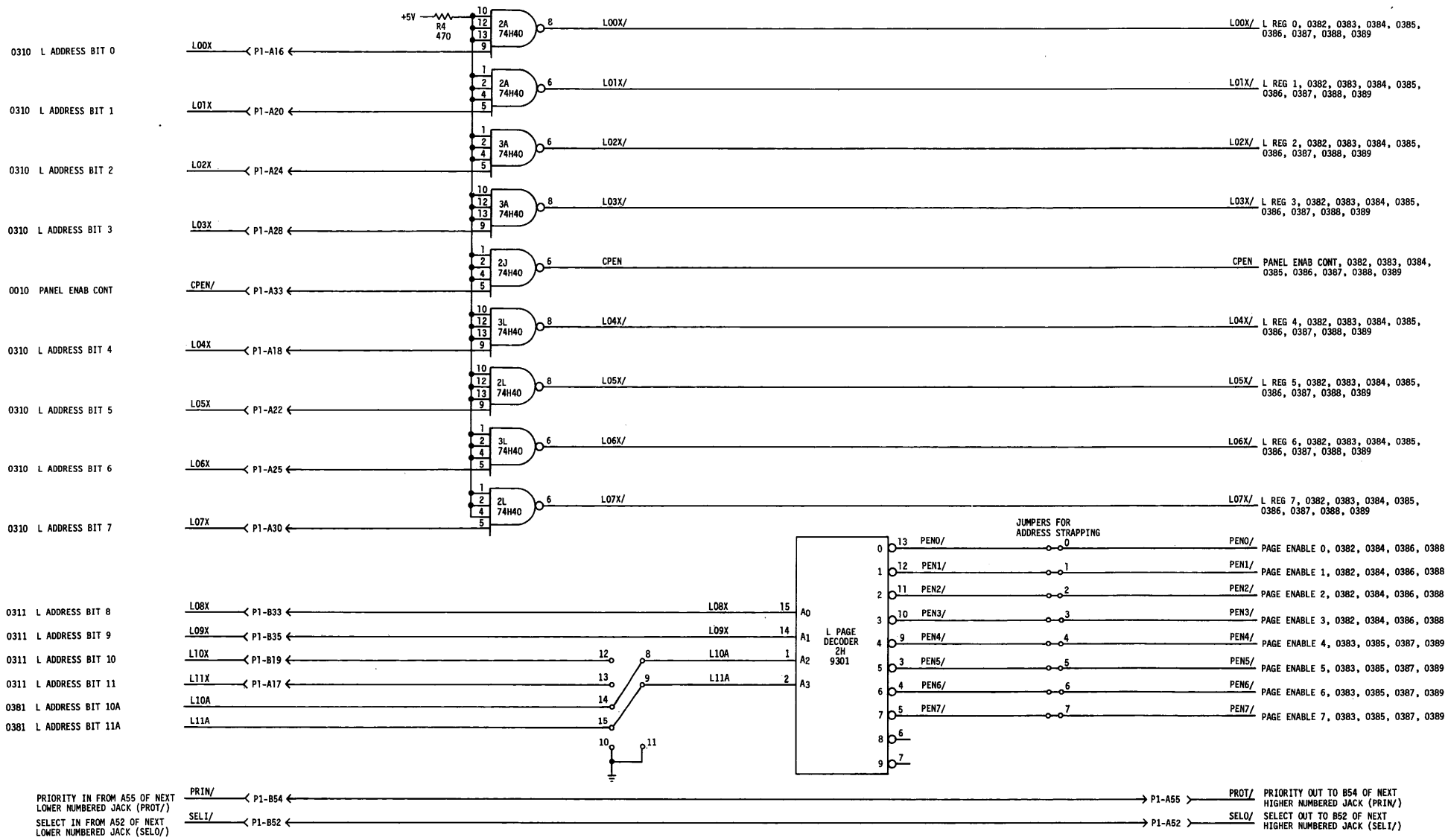
0370 OP CODE 7

0361 R REG BIT 5

0361 R REG BIT 6

0372 OP CODES 8-B

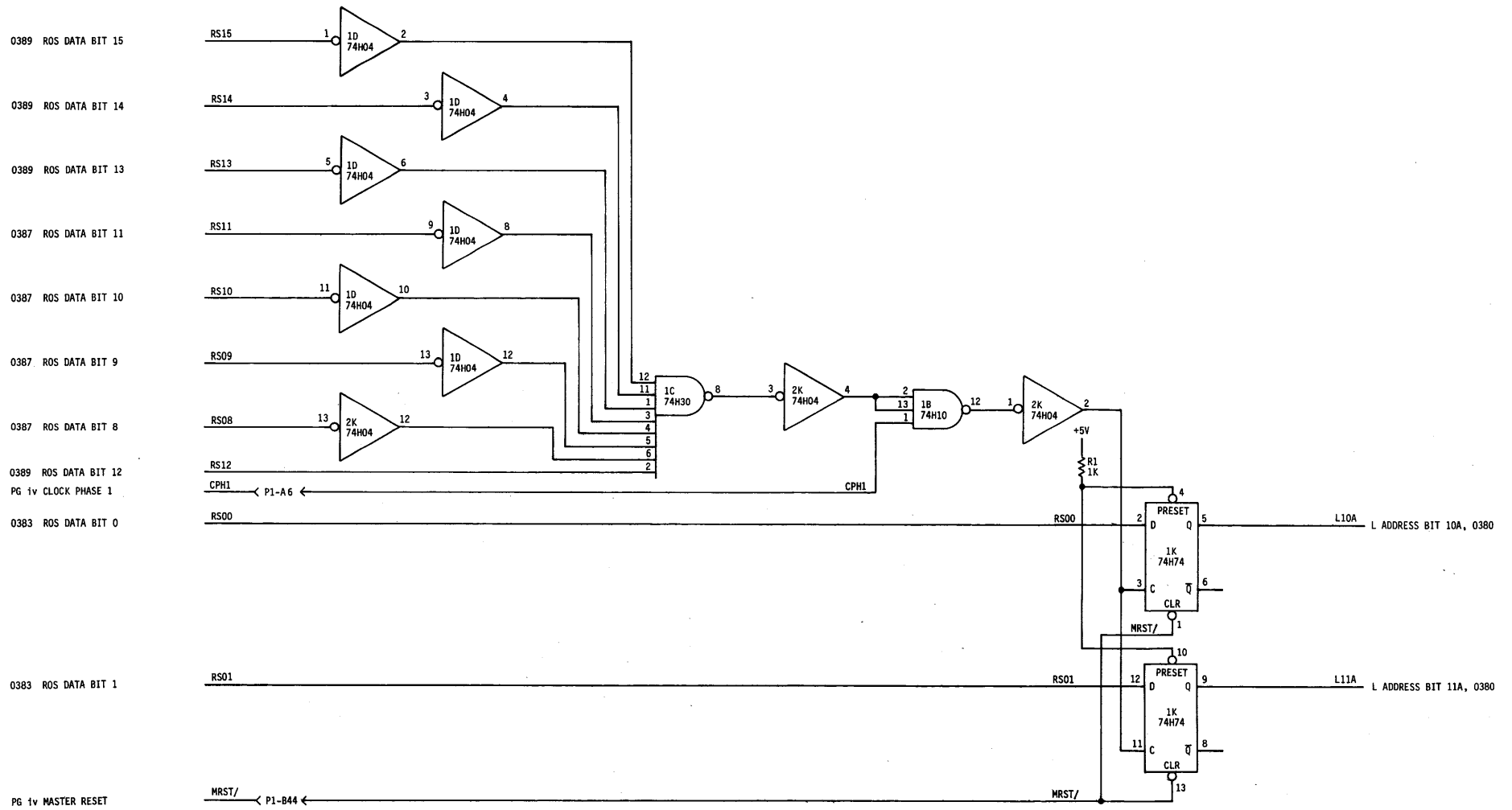
0363 R REG BIT 15
0370 MEMORY READ OR WRITE
0810 I/O CONT REG 3



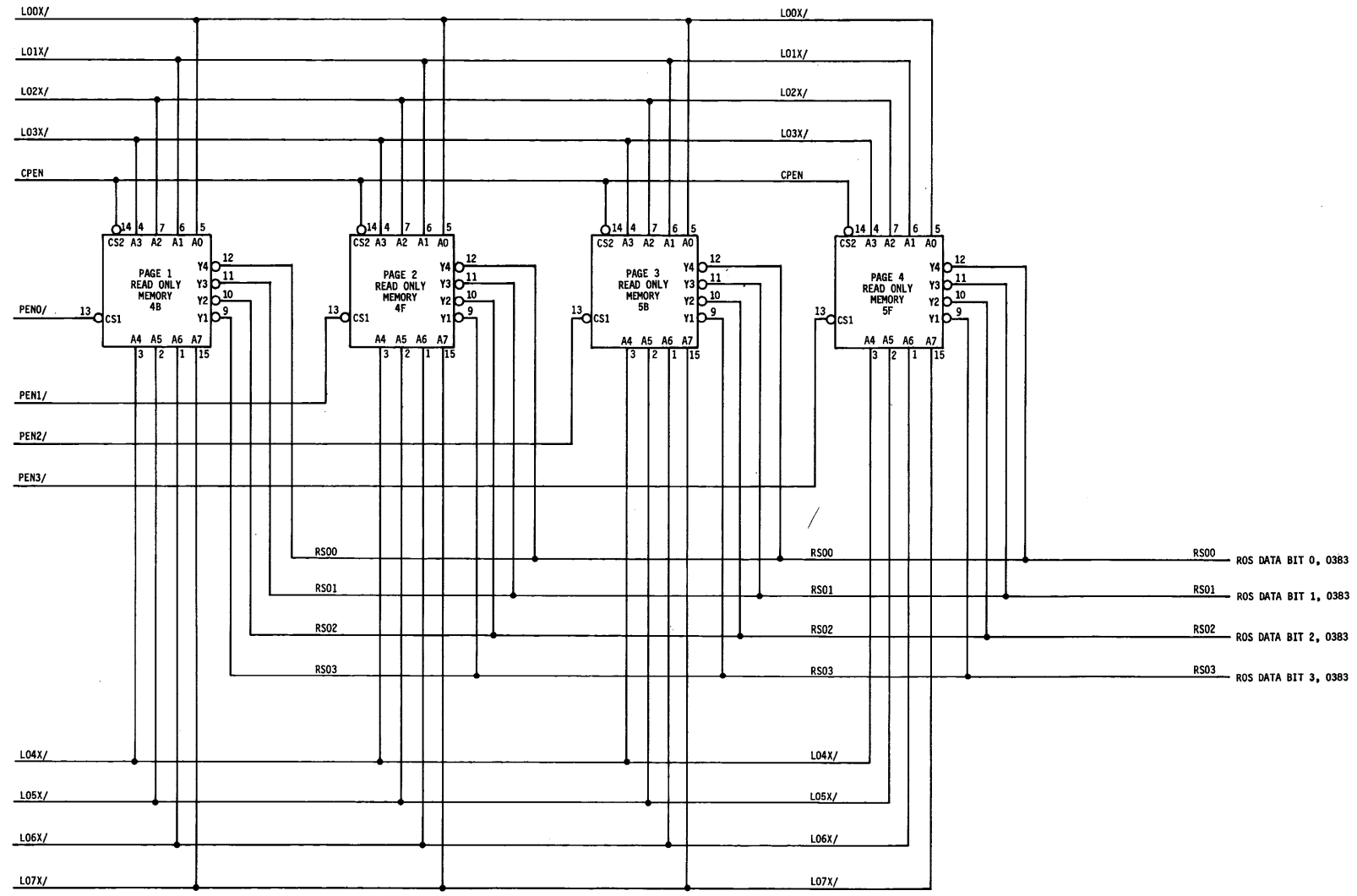
REV. FEB. 21, 1973
LD 1010
CENTRAL PROCESSING UNIT

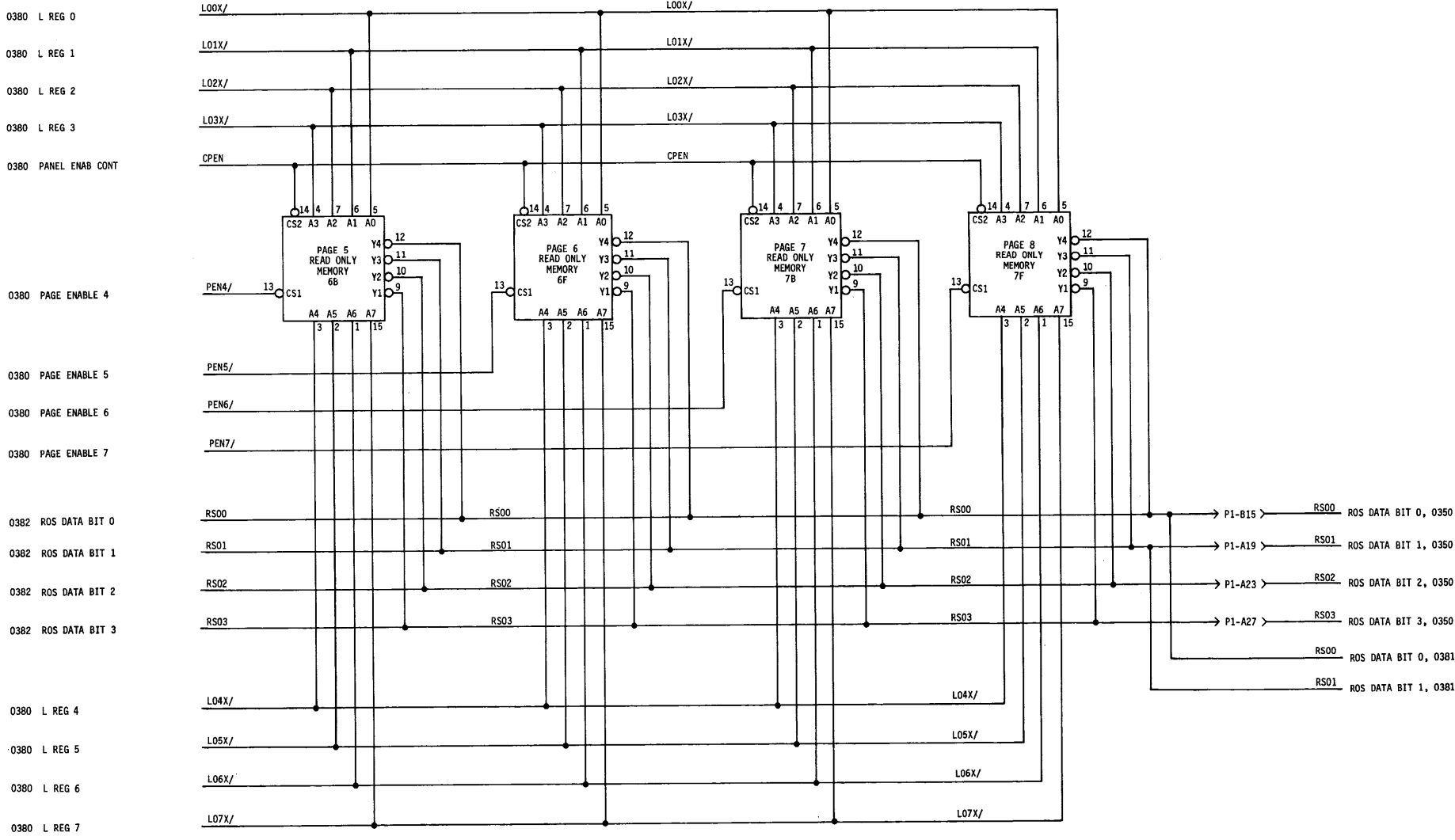
READ ONLY MEMORY CONTROL AND ADDRESS DECODER

READ ONLY MEMORY BOARD
0380

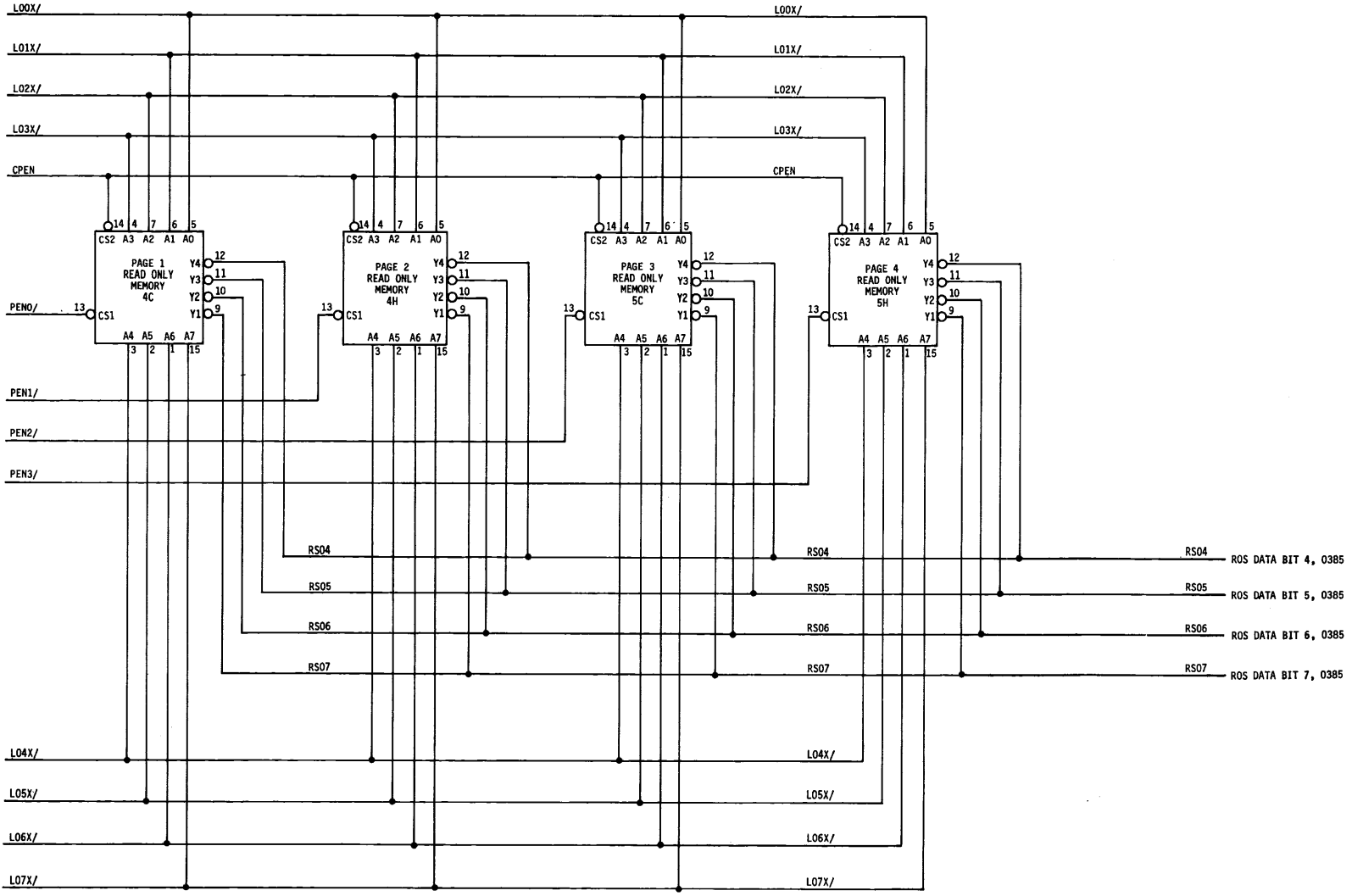


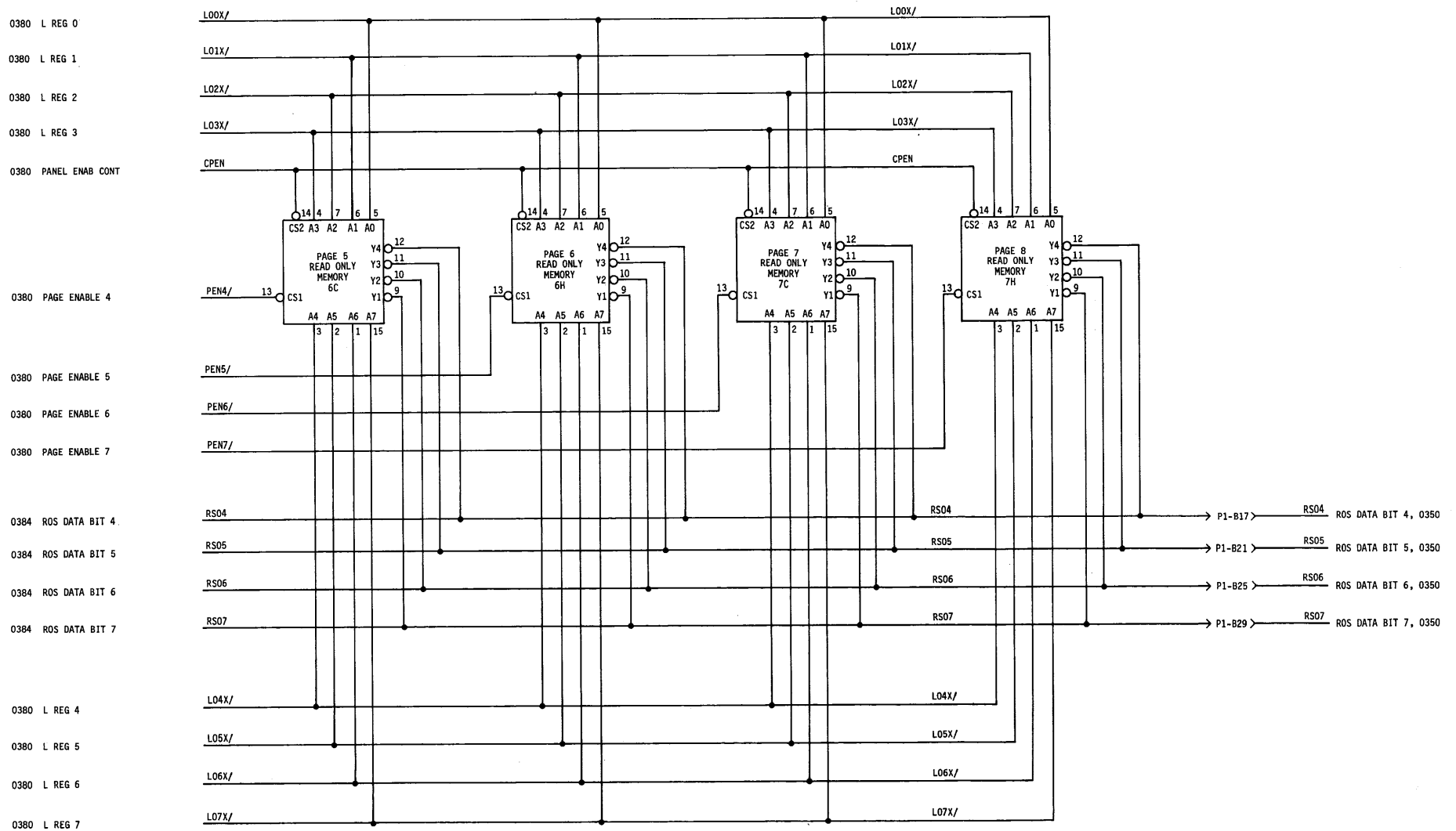
0380 L REG 0
 0380 L REG 1
 0380 L REG 2
 0380 L REG 3
 0380 PANEL ENAB CONT
 0380 PAGE ENABLE 0
 0380 PAGE ENABLE 1
 0380 PAGE ENABLE 2
 0380 PAGE ENABLE 3
 0380 L REG 4
 0380 L REG 5
 0380 L REG 6
 0380 L REG 7



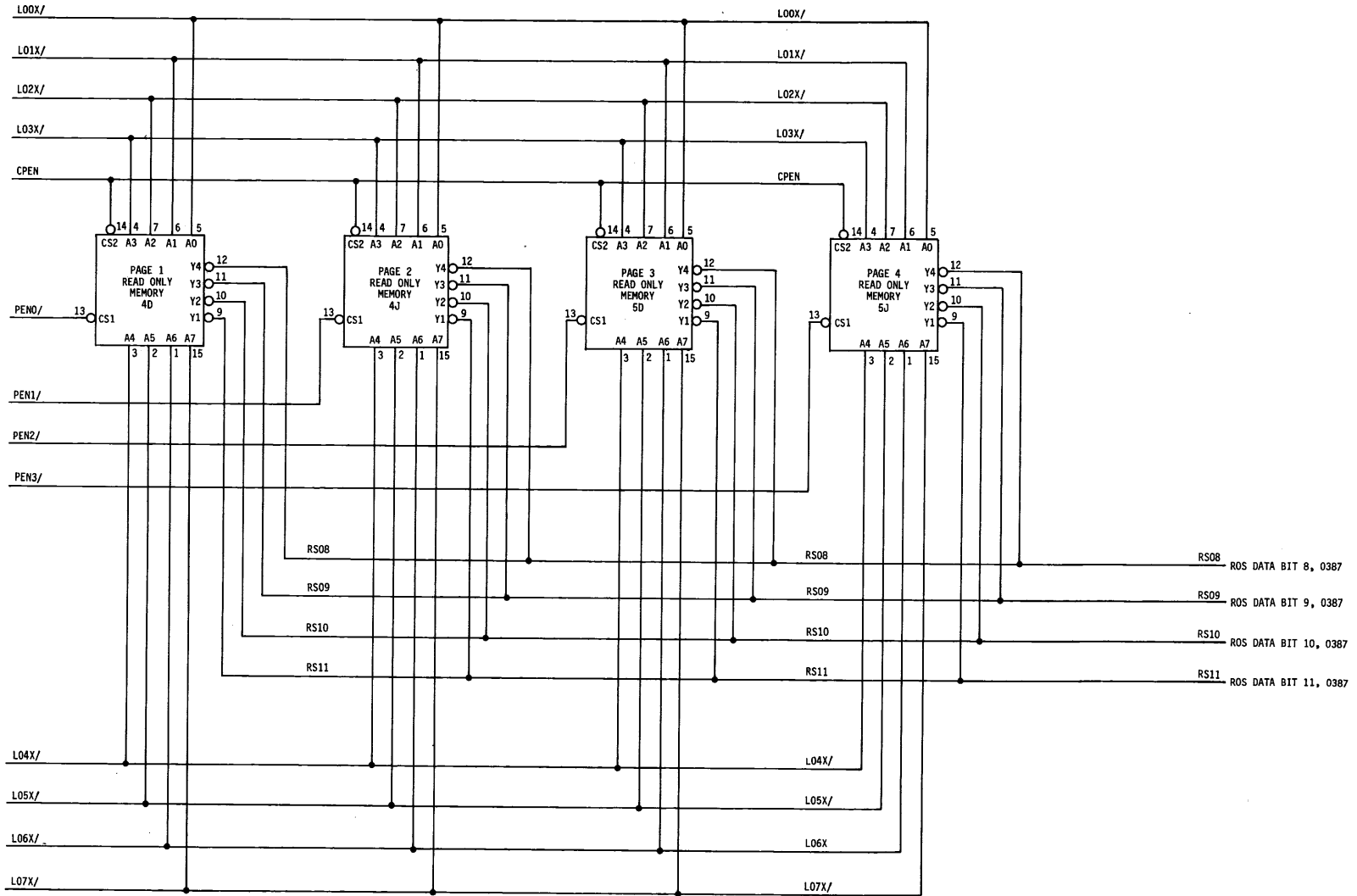


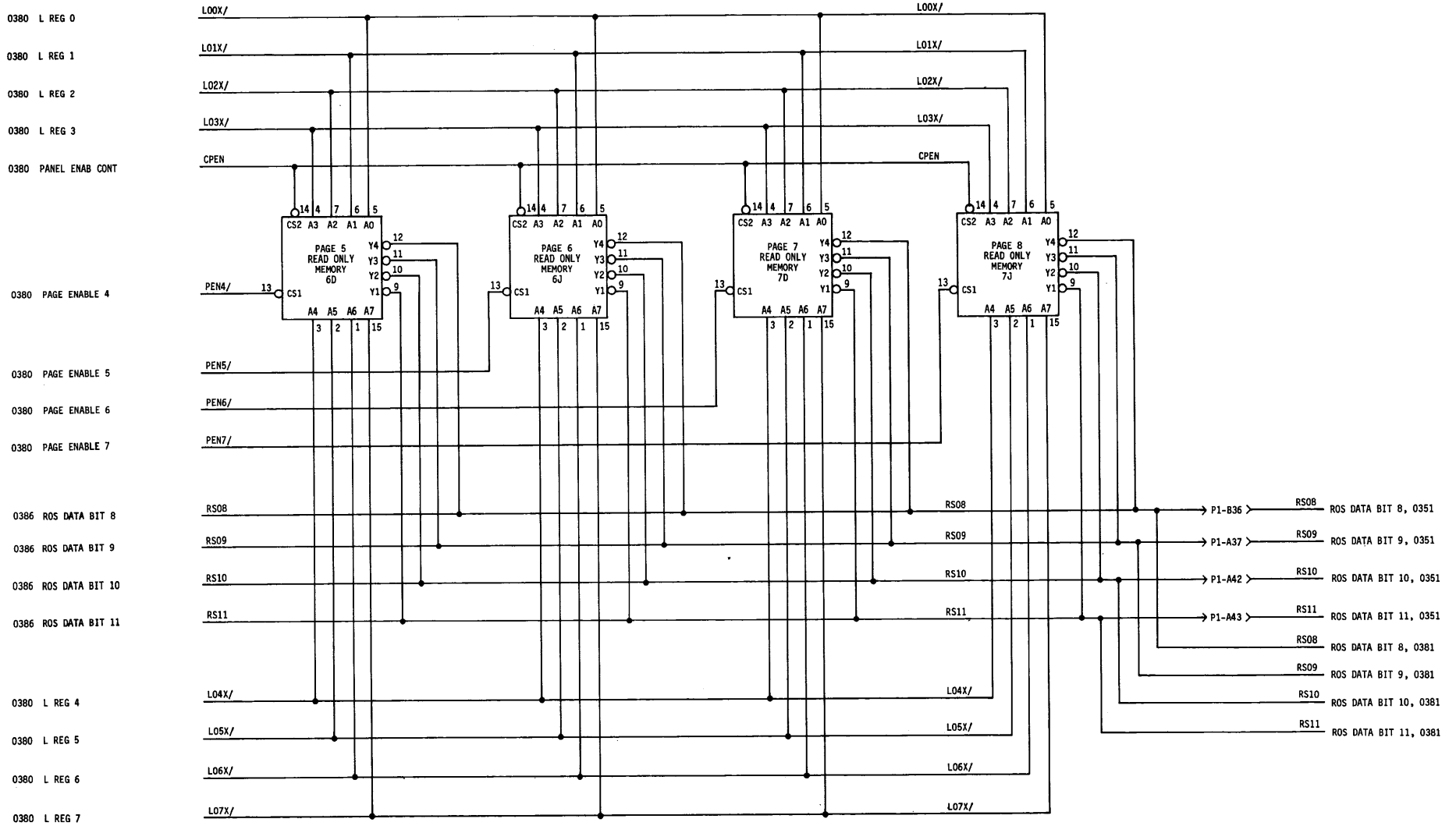
0380 L REG 0
 0380 L REG 1
 0380 L REG 2
 0380 L REG 3
 0380 PANEL ENAB CONT
 0380 PAGE ENABLE 0
 0380 PAGE ENABLE 1
 0380 PAGE ENABLE 2
 0380 PAGE ENABLE 3
 0380 L REG 4
 0380 L REG 5
 0380 L REG 6
 0380 L REG 7



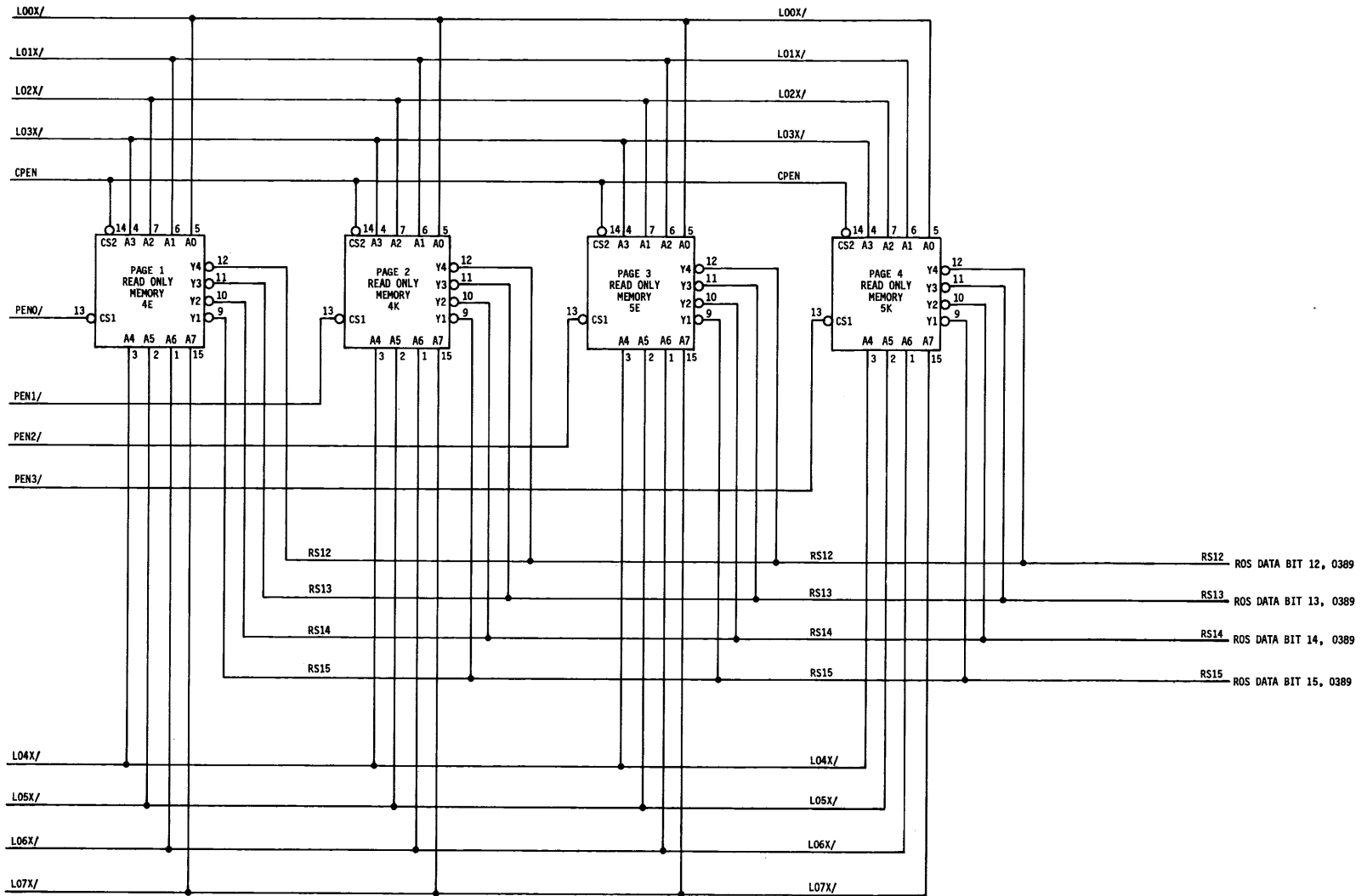


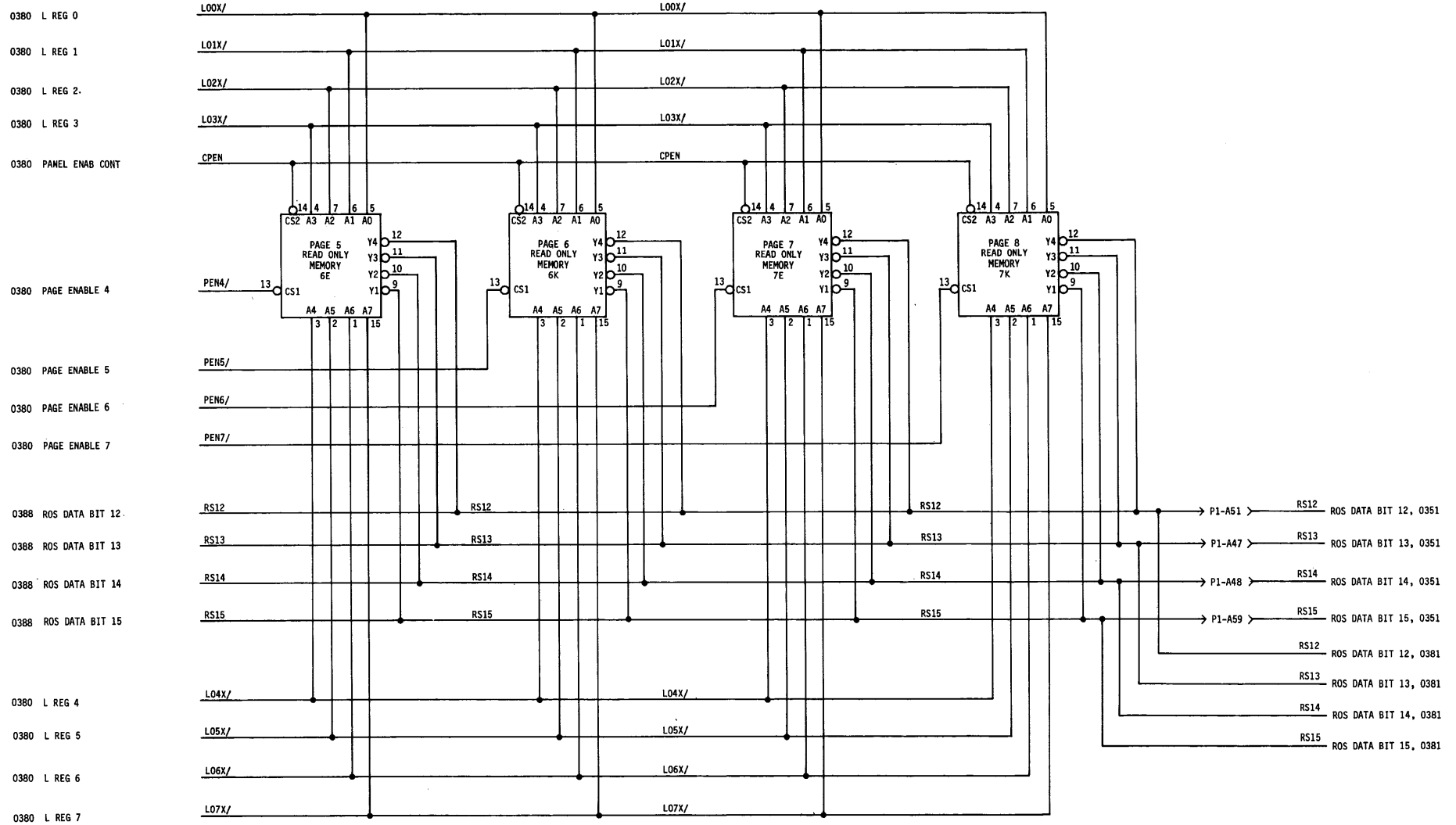
0380 L REG 0
 0380 L REG 1
 0380 L REG 2
 0380 L REG 3
 0380 PANEL ENAB CONT
 0380 PAGE ENABLE 0
 0380 PAGE ENABLE 1
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 0380 PAGE ENABLE 3
 0380 L REG 4
 0380 L REG 5
 0380 L REG 6
 0380 L REG 7

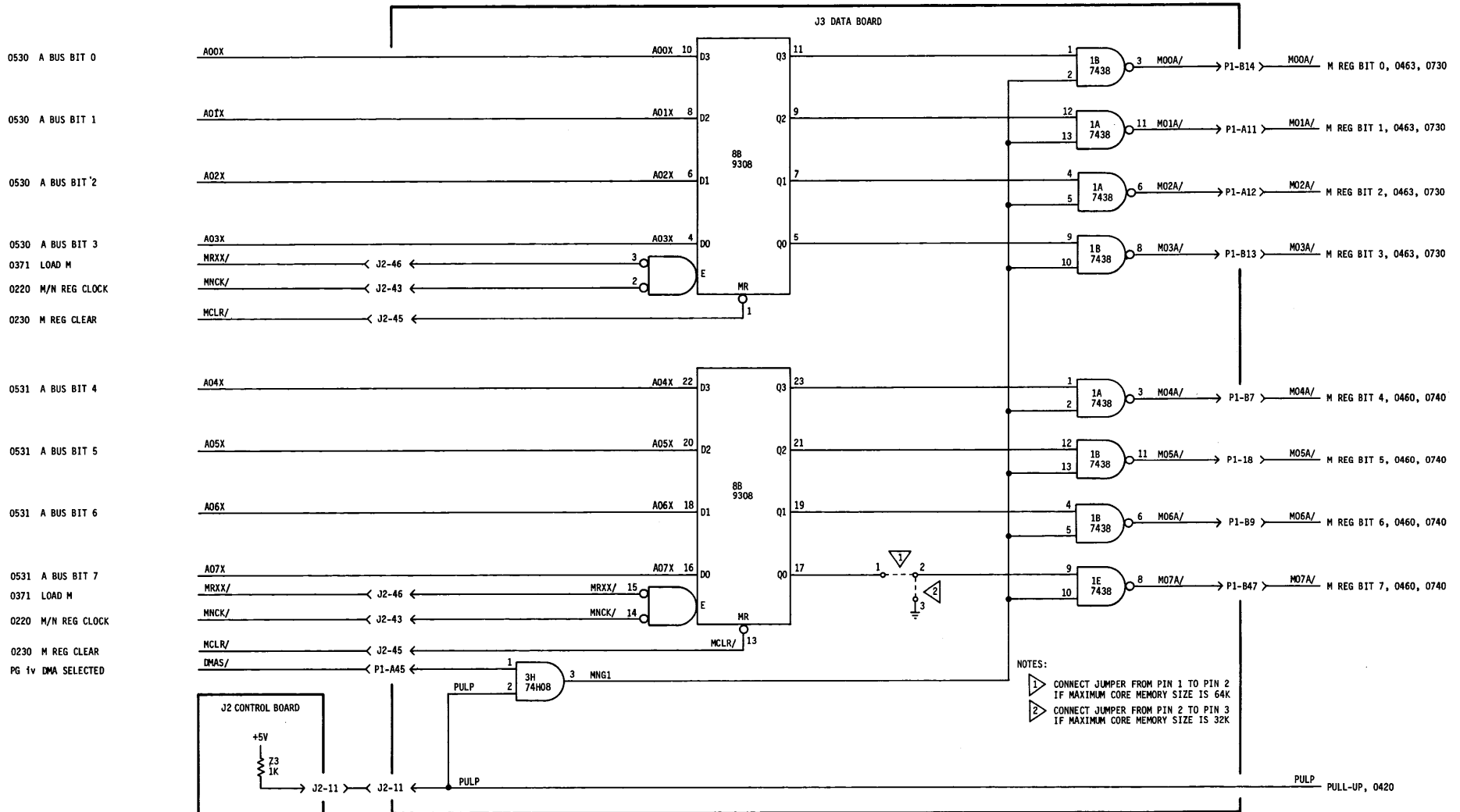




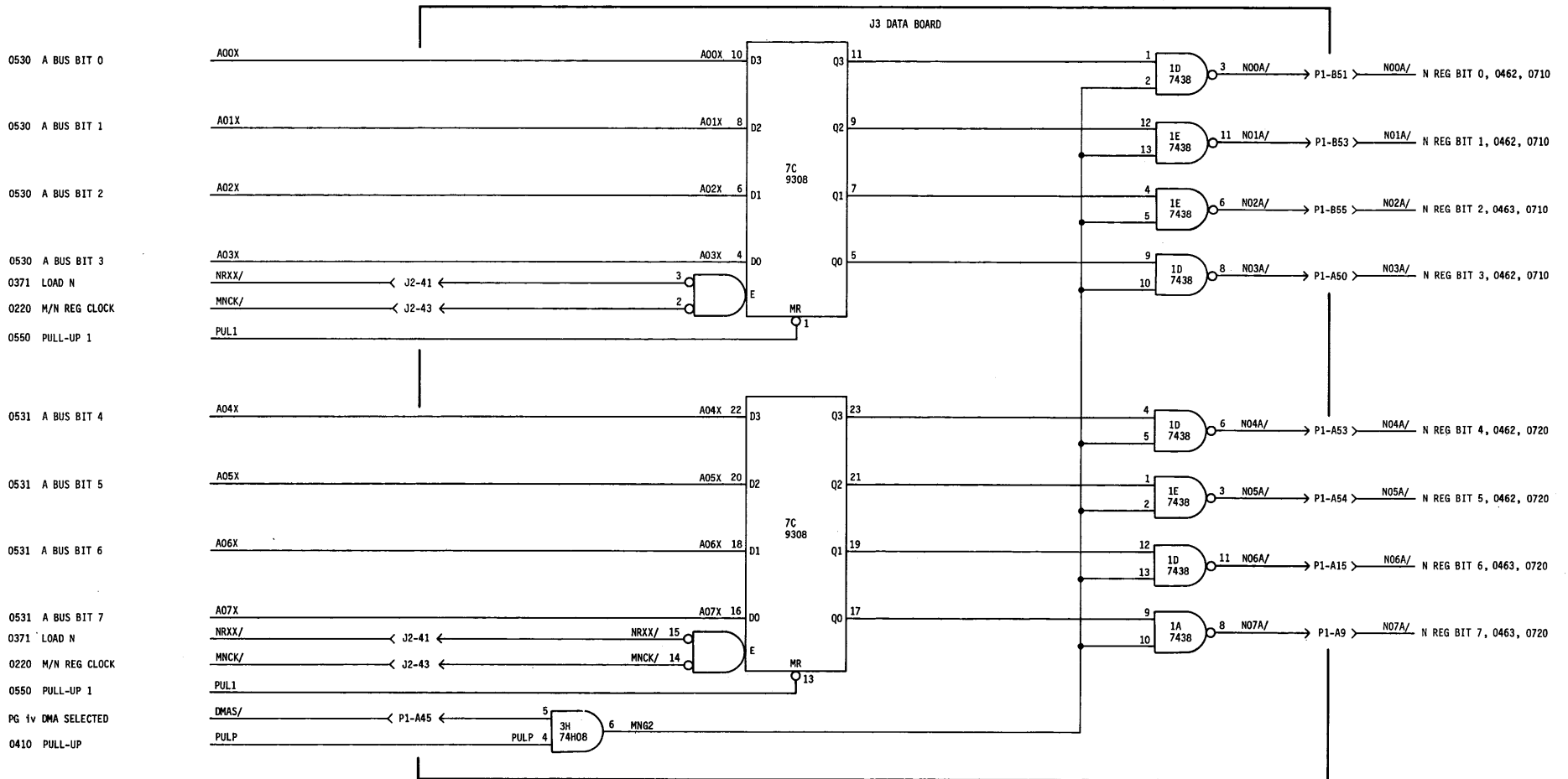
0380 L REG 0
 0380 L REG 1
 0380 L REG 2
 0380 L REG 3
 0380 PANEL ENAB CONT
 0380 PAGE ENABLE 0
 0380 PAGE ENABLE 1
 0380 PAGE ENABLE 2
 0380 PAGE ENABLE 3
 0380 L REG 4
 0380 L REG 5
 0380 L REG 6
 0380 L REG 7

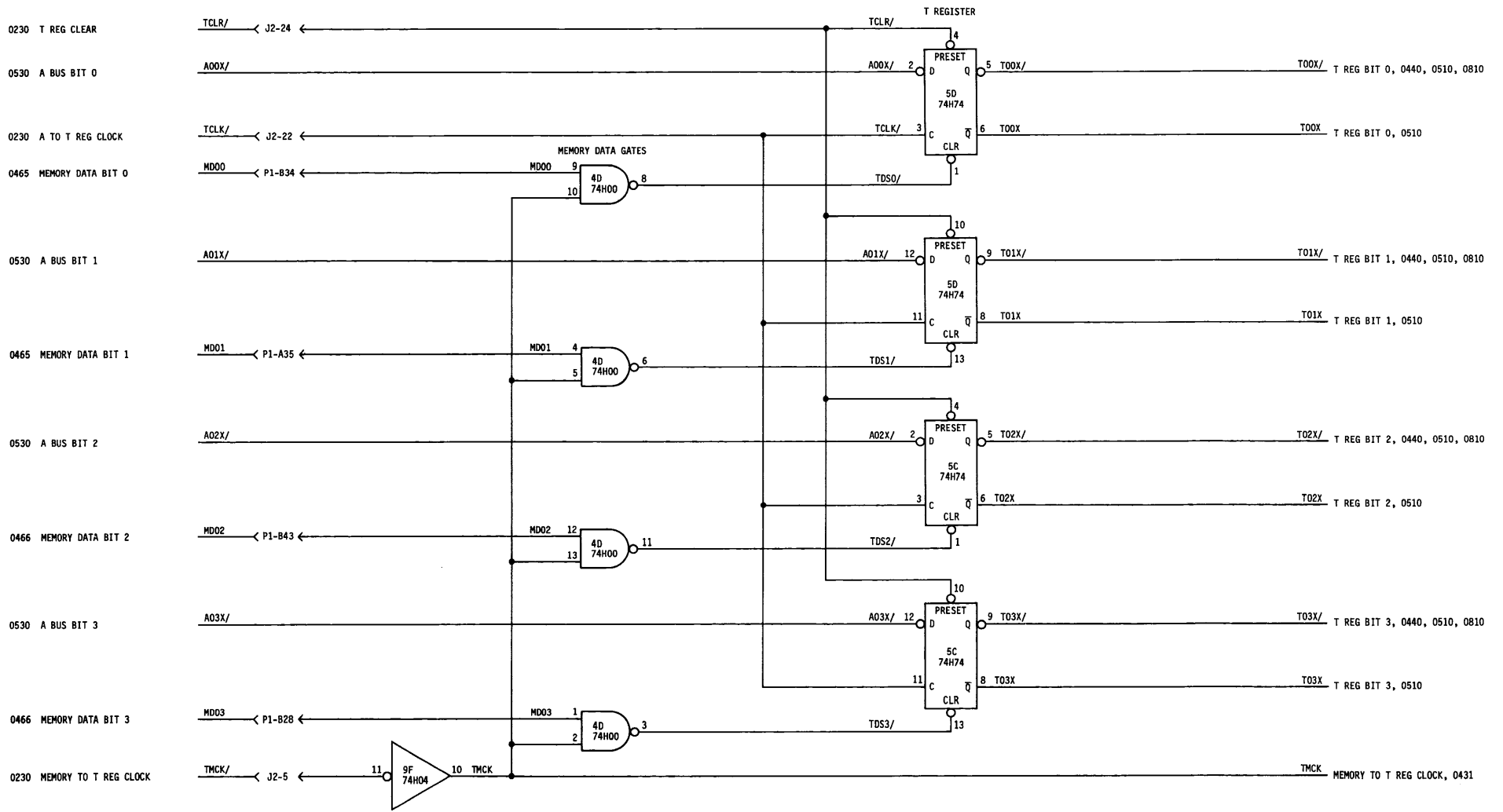


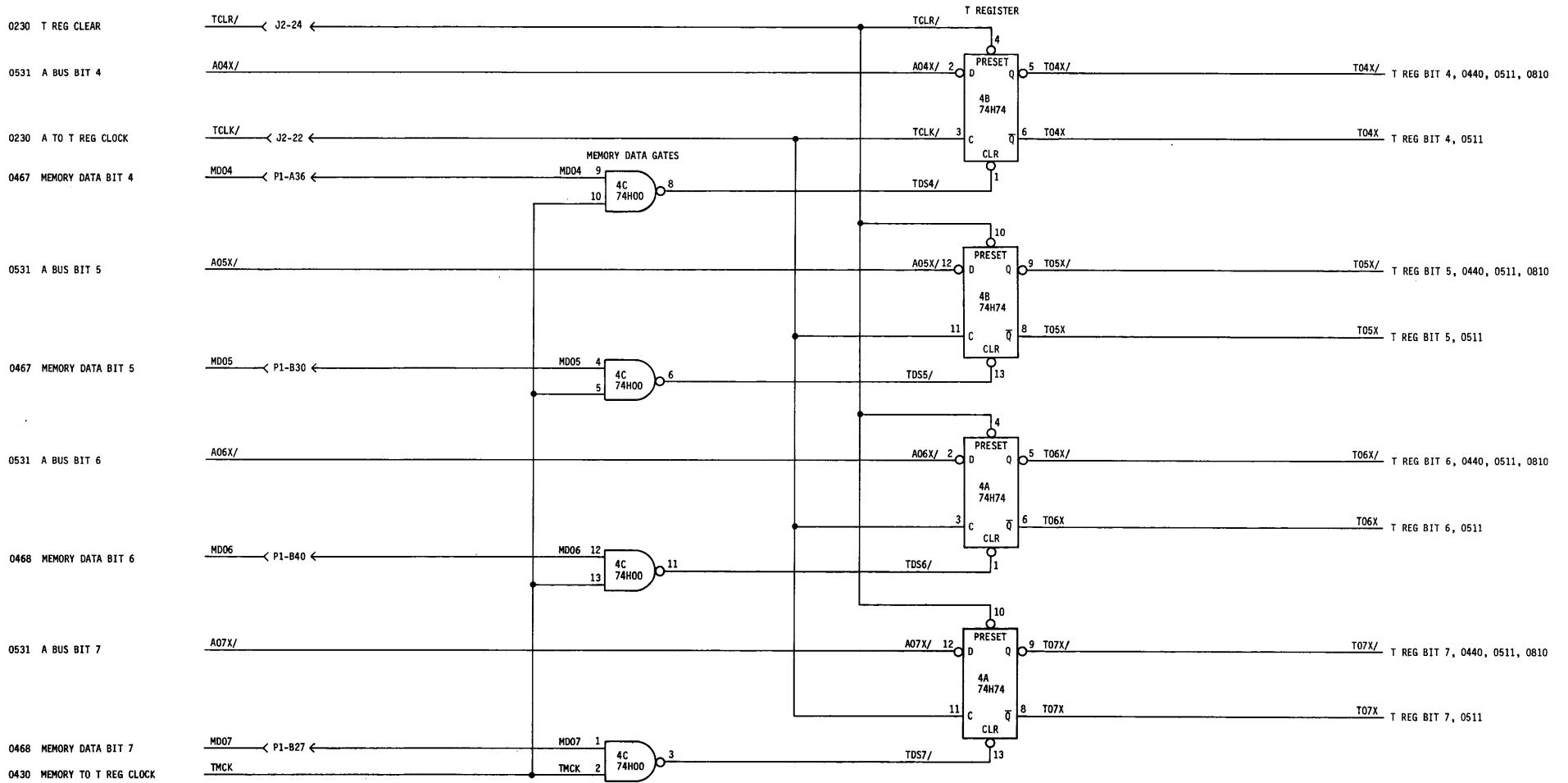


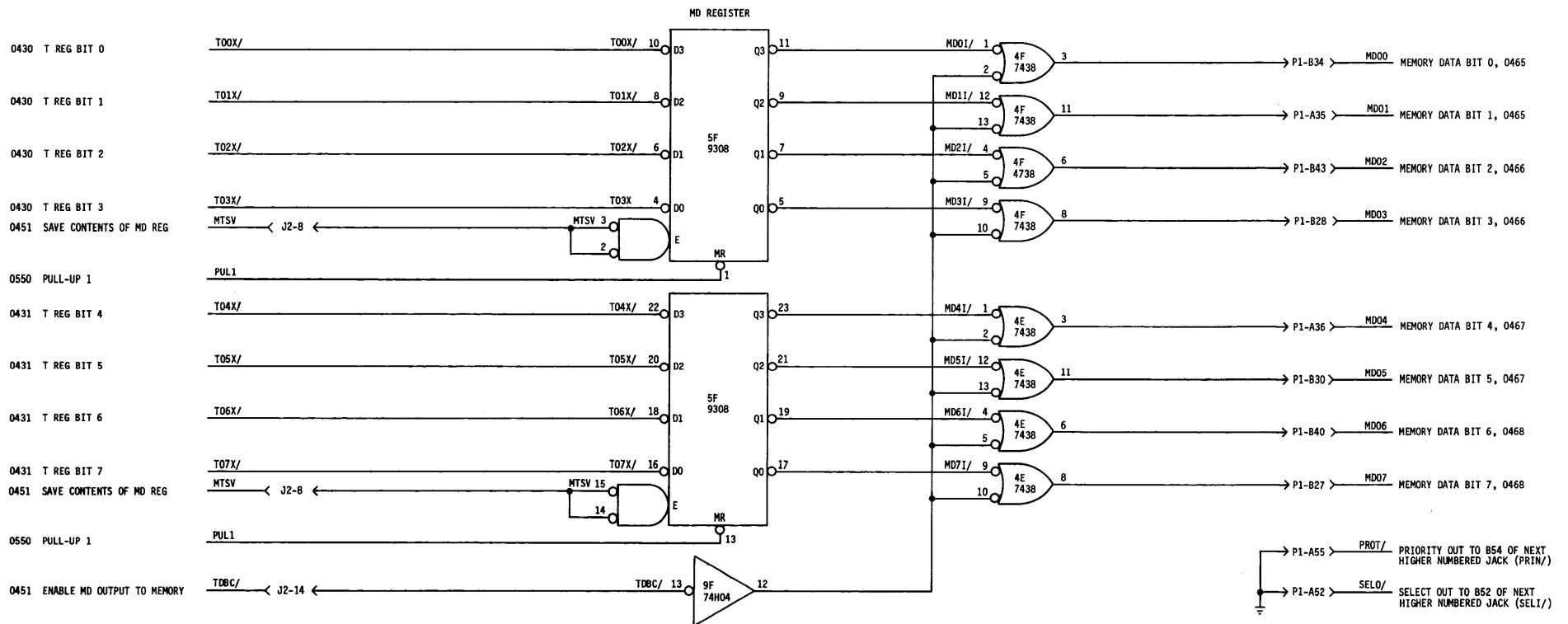


N REGISTER









PG iv MASTER RESET

0220 MEMORY CLOCK PHASE 1
0220 MEMORY CLOCK PHASE 2
0451 WRITE INHIBIT 0 S

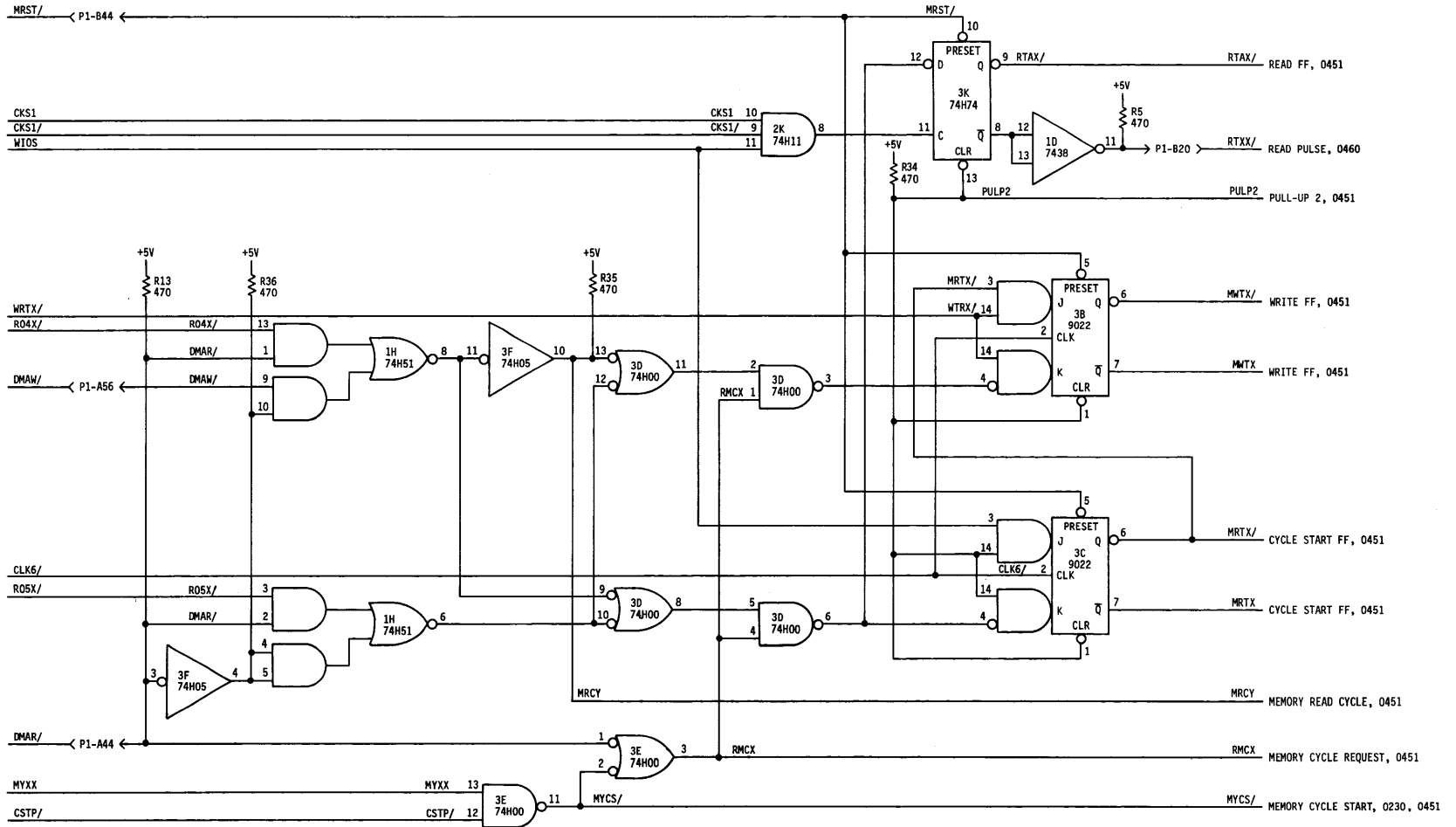
0451 WRITE PULSE INTERNAL
0361 R REG BIT 4

PG iv DMA WRITE

0230 5-MHZ CLOCK PHASE 2
0361 R REG BIT 5

PG iv DMA REQUEST

0370 MEMORY READ OR WRITE
0211 CLOCK STOP



0450 WRITE FF

0450 CYCLE START FF

PG 1v MASTER RESET

0450 PULL-UP 2

0230 5-MHZ CLOCK PULSE

0450 MEMORY CYCLE REQUEST

0450 MEMORY READ CYCLE

0450 MEMORY CYCLE START

0220 5-MHZ CLOCK PHASE 1

0451 WRITE PULSE INTERNAL

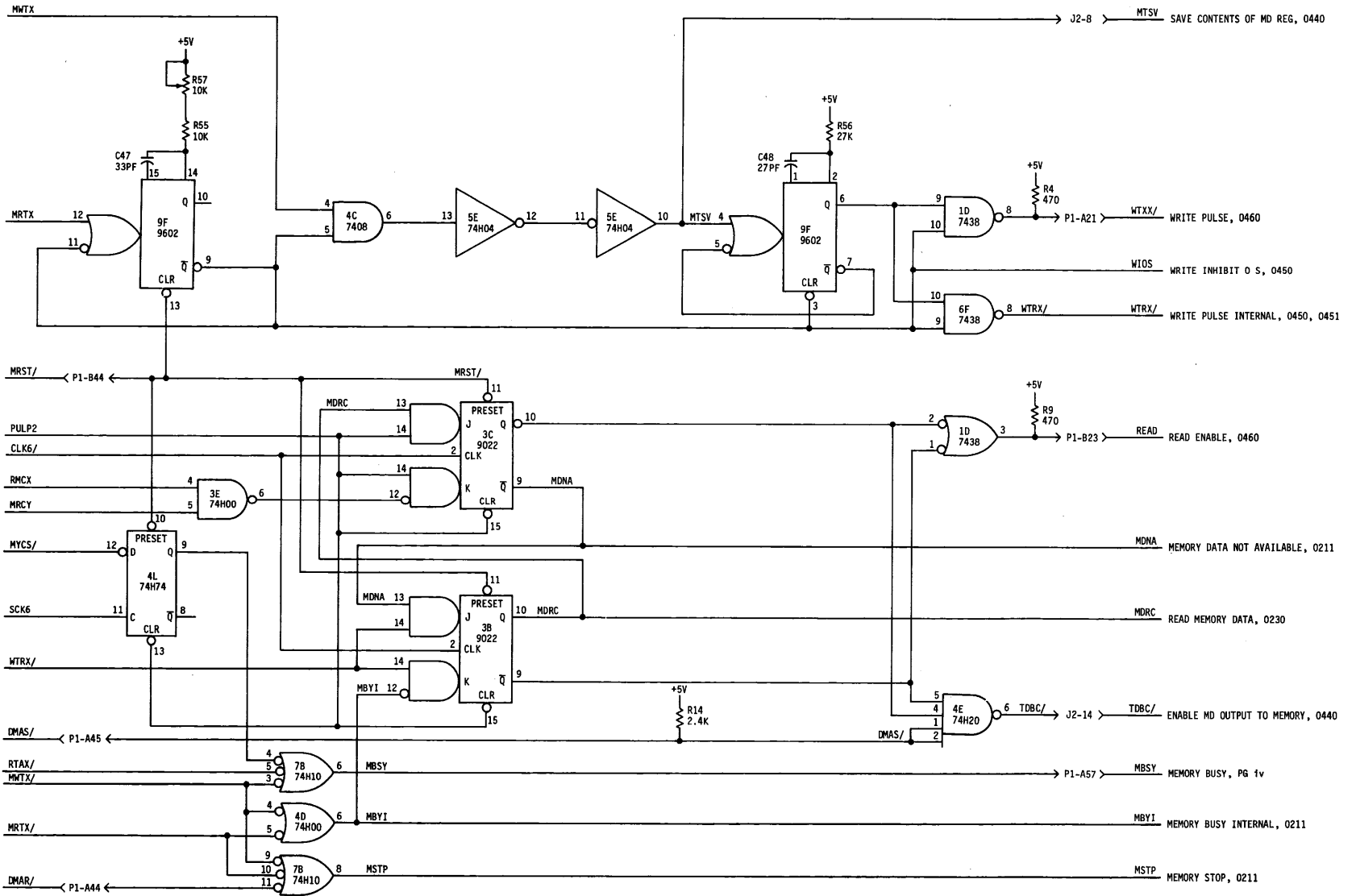
PG 1v DMA SELECTED

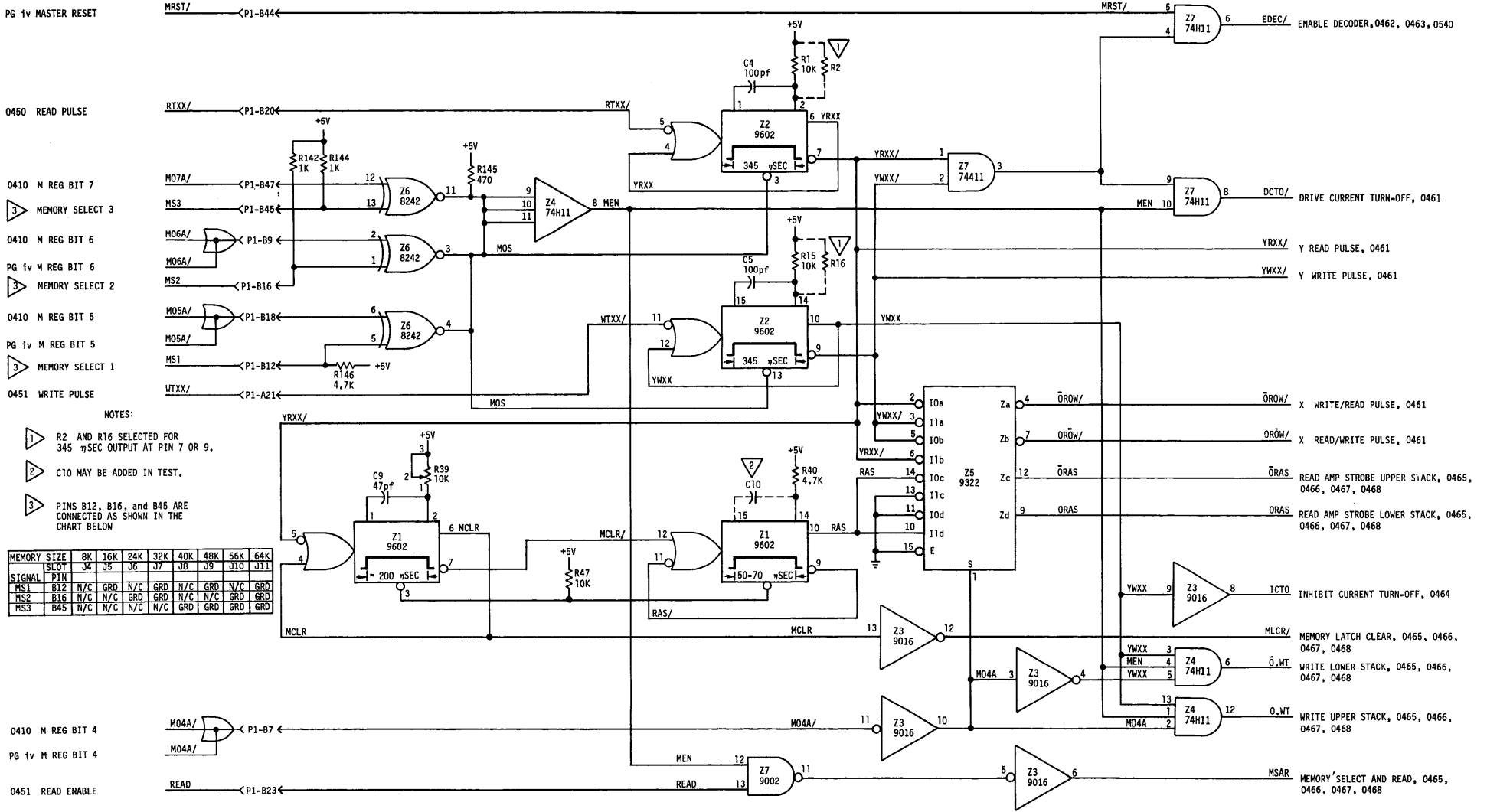
0450 READ FF

0450 WRITE FF

0450 CYCLE START FF

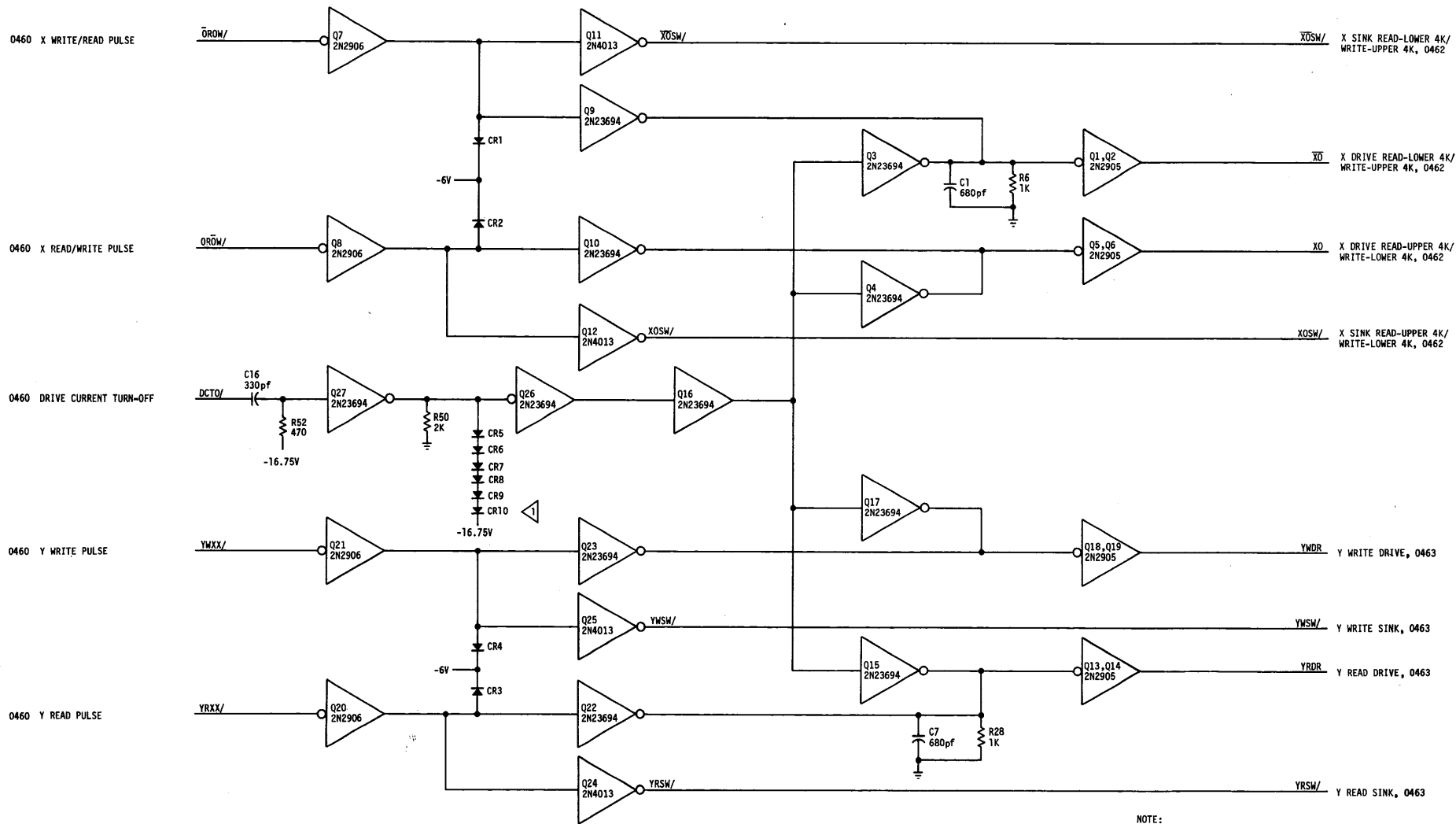
PG 1v DMA REQUEST





- NOTES:
- 1 R2 AND R16 SELECTED FOR 345 nSEC OUTPUT AT PIN 7 OR 9.
 - 2 C10 MAY BE ADDED IN TEST.
 - 3 PINS B12, B16, and B45 ARE CONNECTED AS SHOWN IN THE CHART BELOW

MEMORY SIZE	8K	16K	24K	32K	40K	48K	56K	64K
SIGNAL	PIN							
MS1	B12	N/C	GRD	N/C	GRD	N/C	GRD	GRD
MS2	B16	N/C	GRD	N/C	GRD	N/C	GRD	GRD
MS3	B45	N/C	GRD	N/C	GRD	N/C	GRD	GRD



CENTRAL PROCESSING UNIT
LD 1010

0461 X DRIVE READ-UPPER 4K/
WRITE-LOWER 4K

0420 N REG BIT 0
PG 1v N REG BIT 0

0420 N REG BIT 1
PG 1v N REG BIT 1

0420 N REG BIT 2
PG 1v N REG BIT 2

0460 ENABLE DECODER

0461 X SINK READ-LOWER 4K/
WRITE-UPPER 4K
0461 X SINK READ-UPPER 4K/
WRITE-LOWER 4K

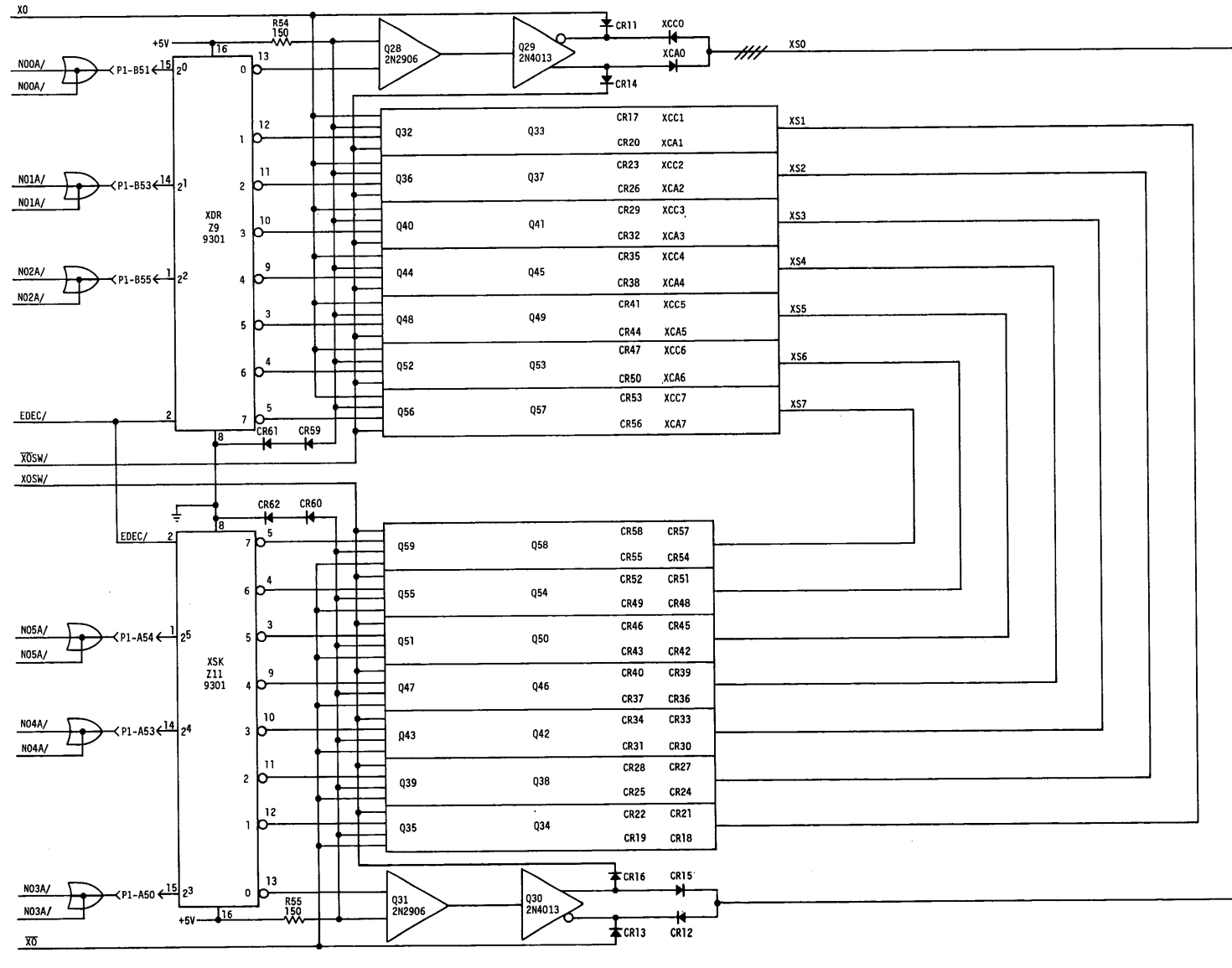
0420 N REG BIT 5
PG 1v N REG BIT 5

0420 N REG BIT 4
PG 1v N REG BIT 4

0420 N REG BIT 3
PG 1v N REG BIT 3

0461 X DRIVE READ-LOWER 4K/
WRITE-UPPER 4K

X SELECT BITS 0-7



0461 Y WRITE DRIVE

0420 N REG BIT 6
PG 1v N REG BIT 6

0420 N REG BIT 7
PG 1v N REG BIT 7

0410 M REG BIT 0
PG 1v M REG BIT 0

0460 ENABLE DECODER

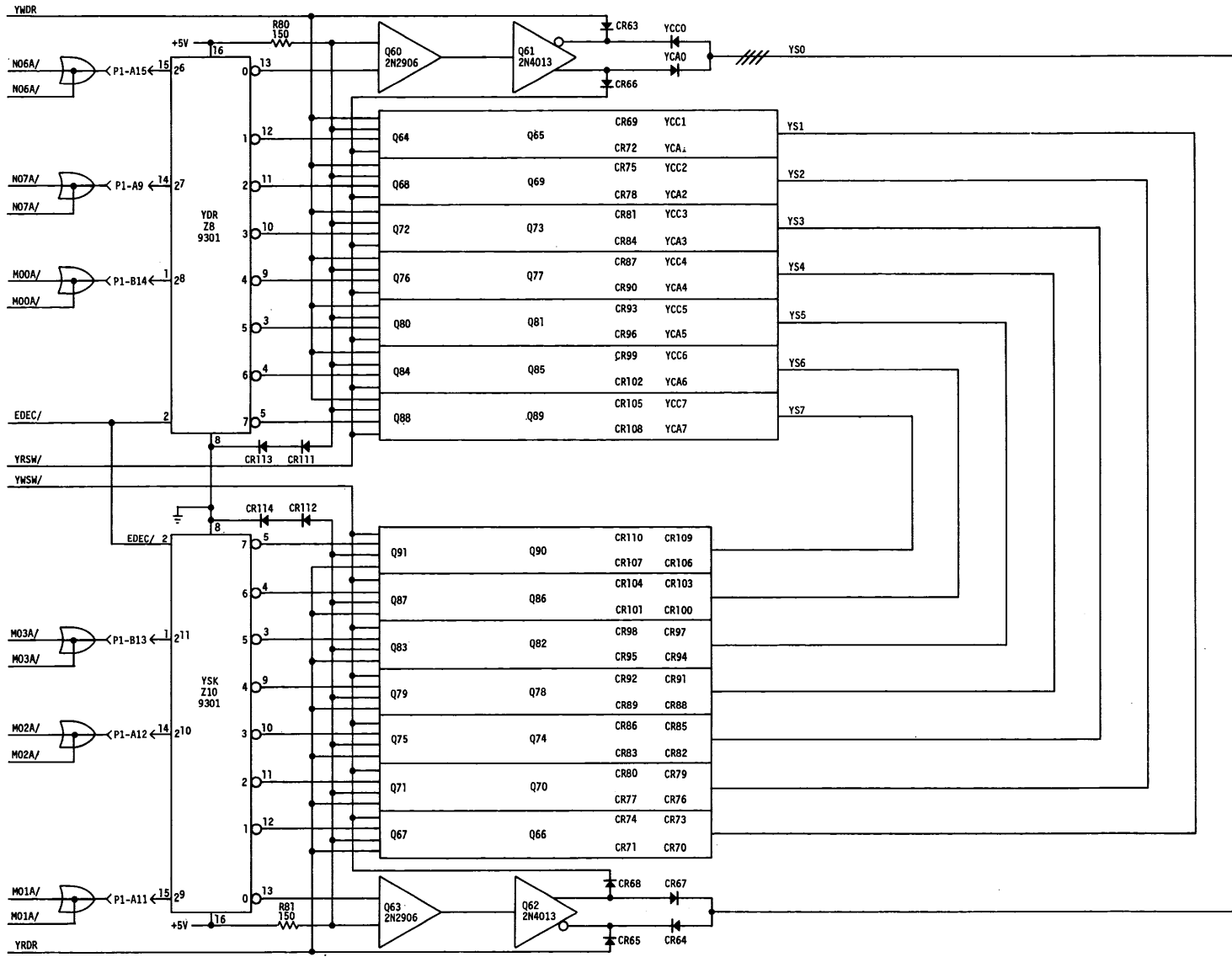
0461 Y READ SINK
0461 Y WRITE SINK

0410 M REG BIT 3
PG 1v M REG BIT 3

0410 M REG BIT 2
PG 1v M REG BIT 2

0410 M REG BIT 1
PG 1v M REG BIT 1

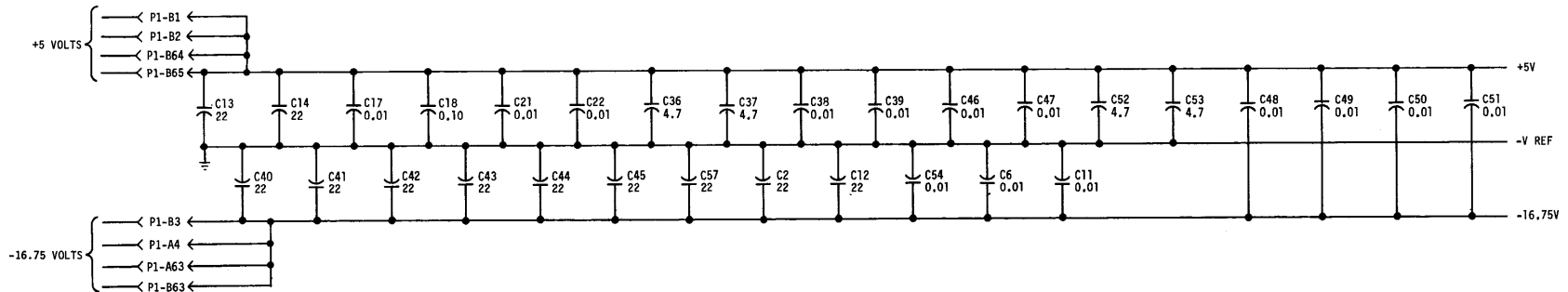
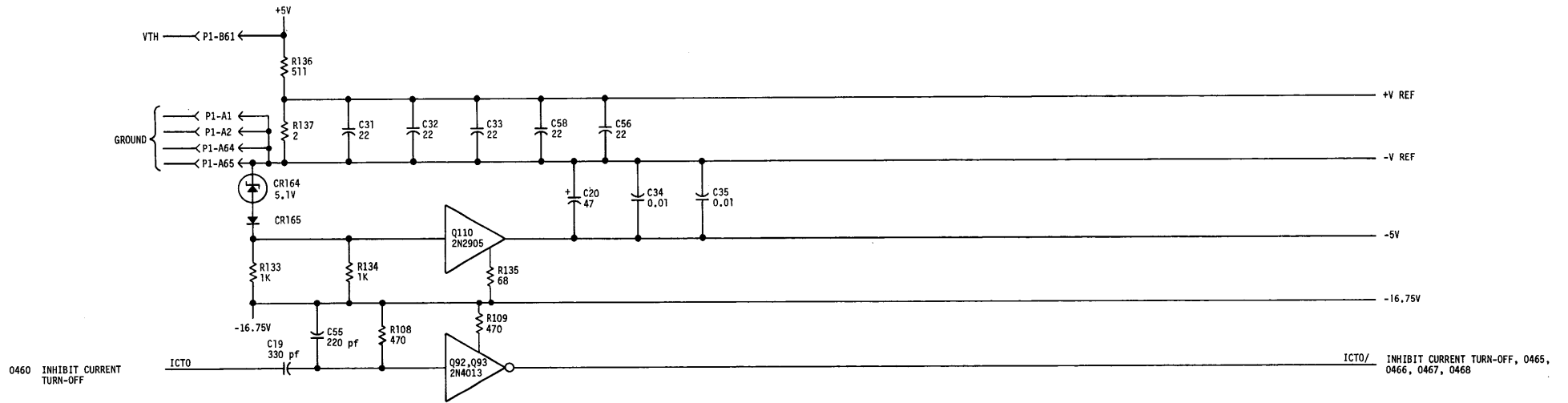
0461 Y READ DRIVE

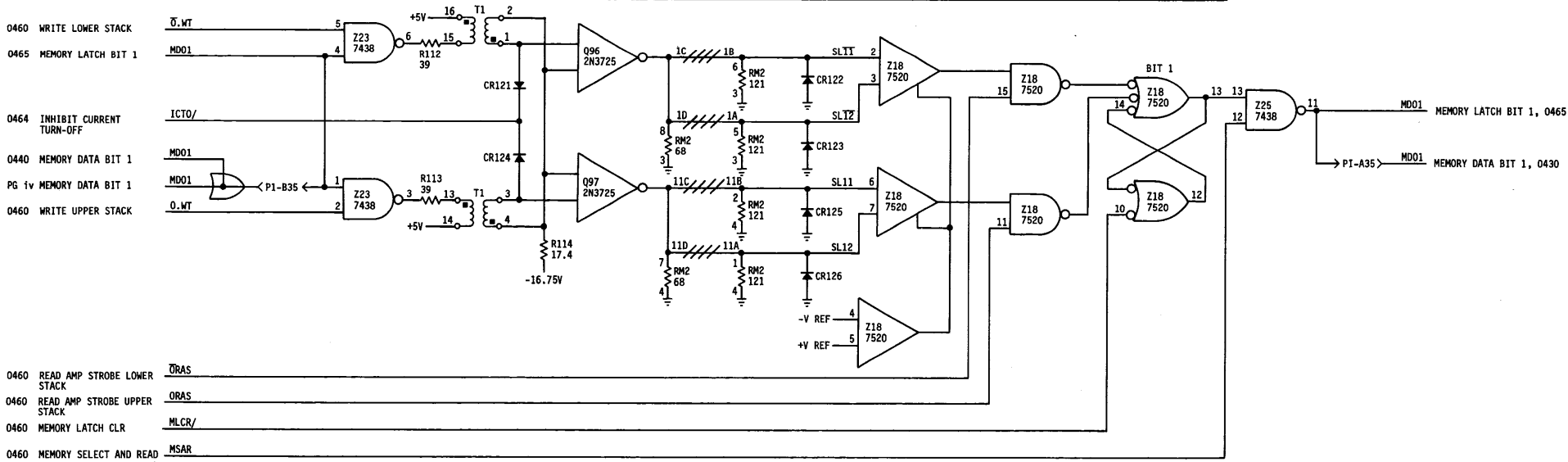
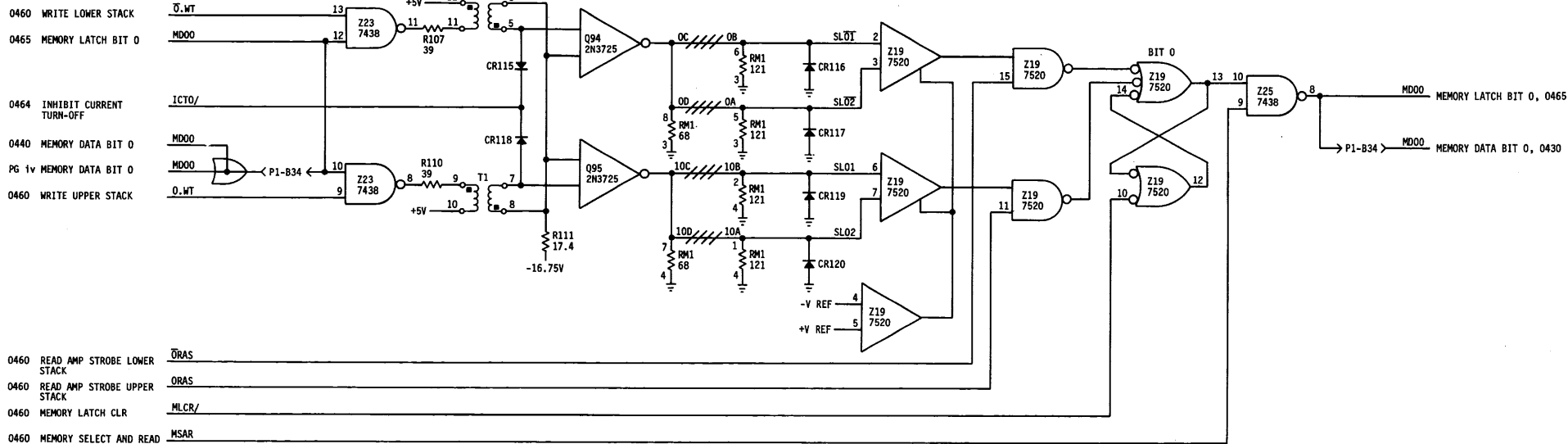


Y SELECT BITS 0-7

PRIORITY IN FROM A55 OF NEXT LOWER NUMBERED JACK (PRIN/) ← P1-B54 → P1-A55 → PROT/ PRIORITY OUT TO B54 OF NEXT HIGHER NUMBERED JACK (PRIN/)

SELECT IN FROM A52 OF NEXT LOWER NUMBERED JACK (SELO/) ← P1-B52 → P1-A52 → SELO/ SELECT OUT TO B52 OF NEXT HIGHER NUMBERED JACK (SELO/)

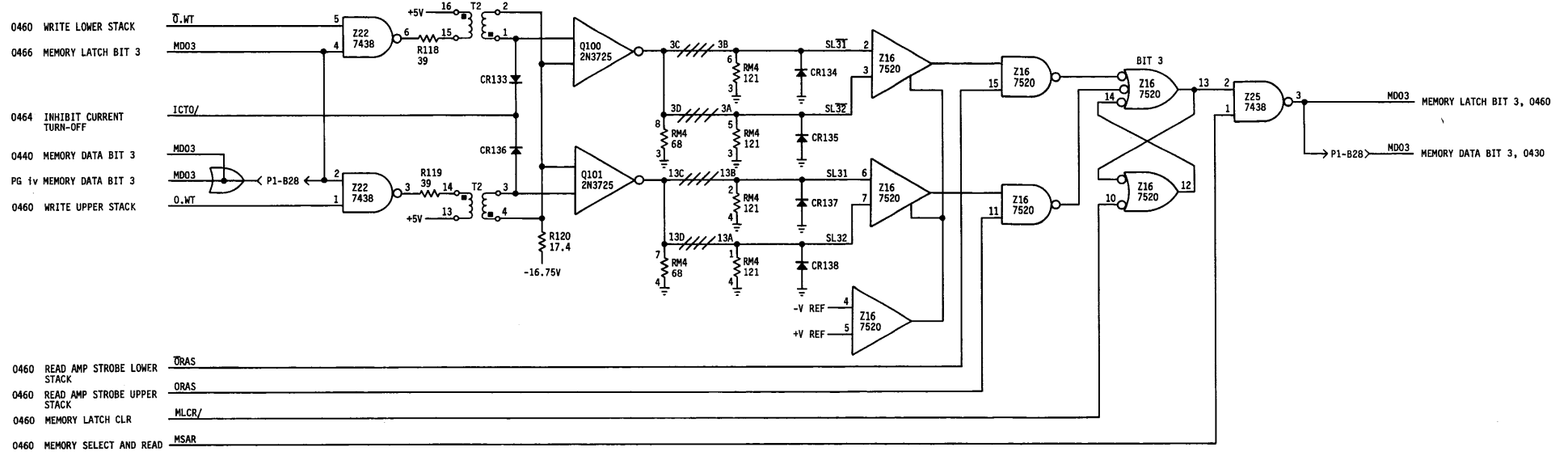
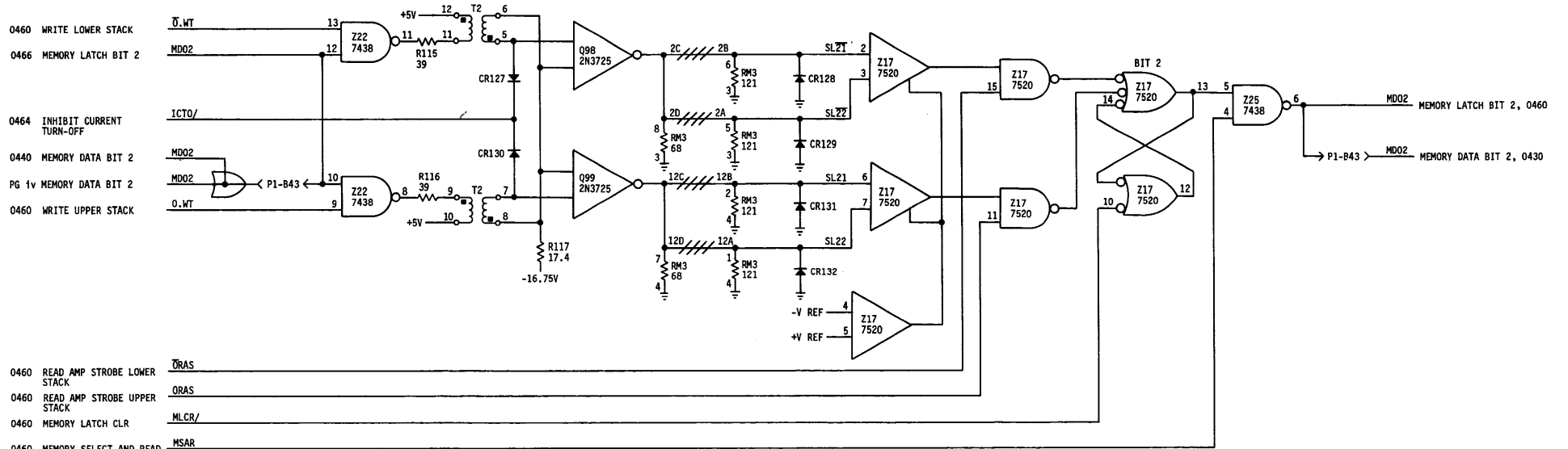


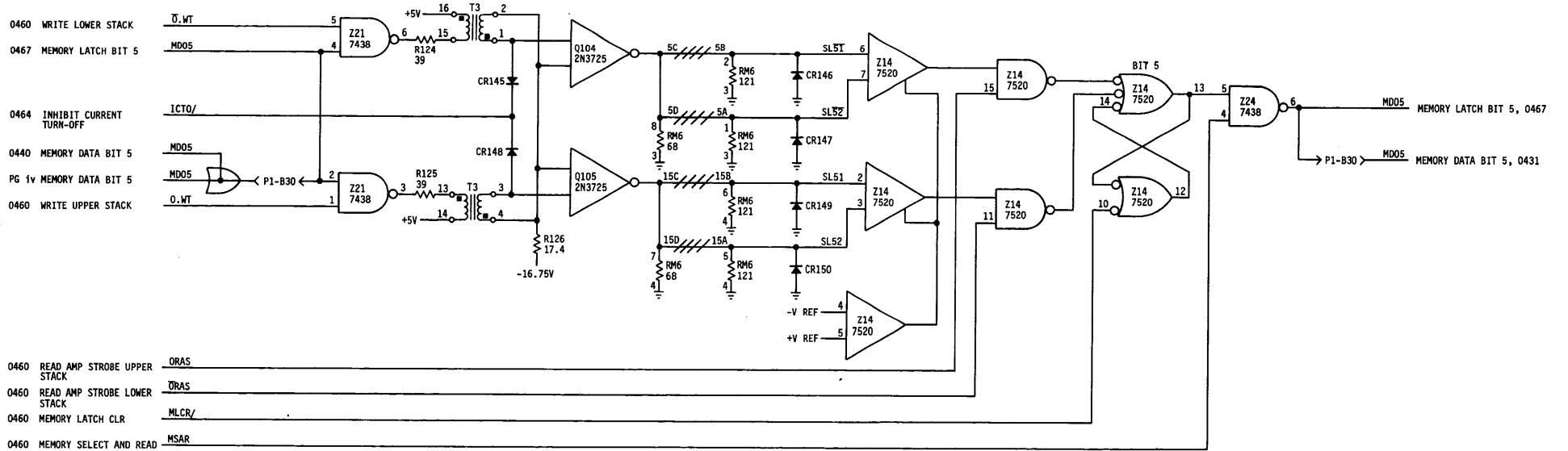
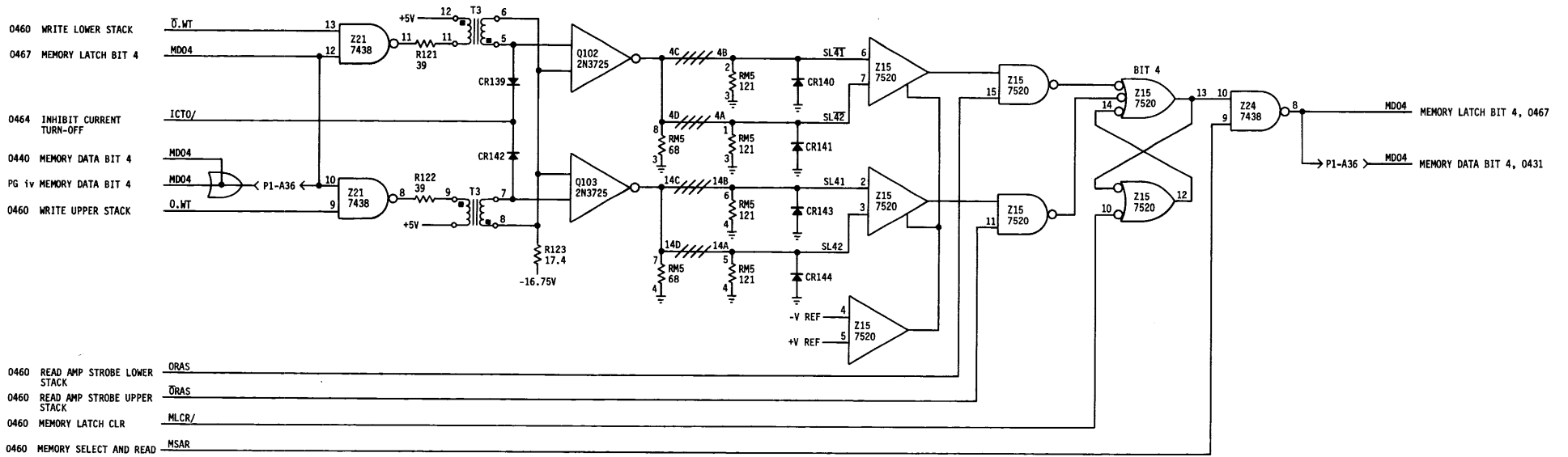


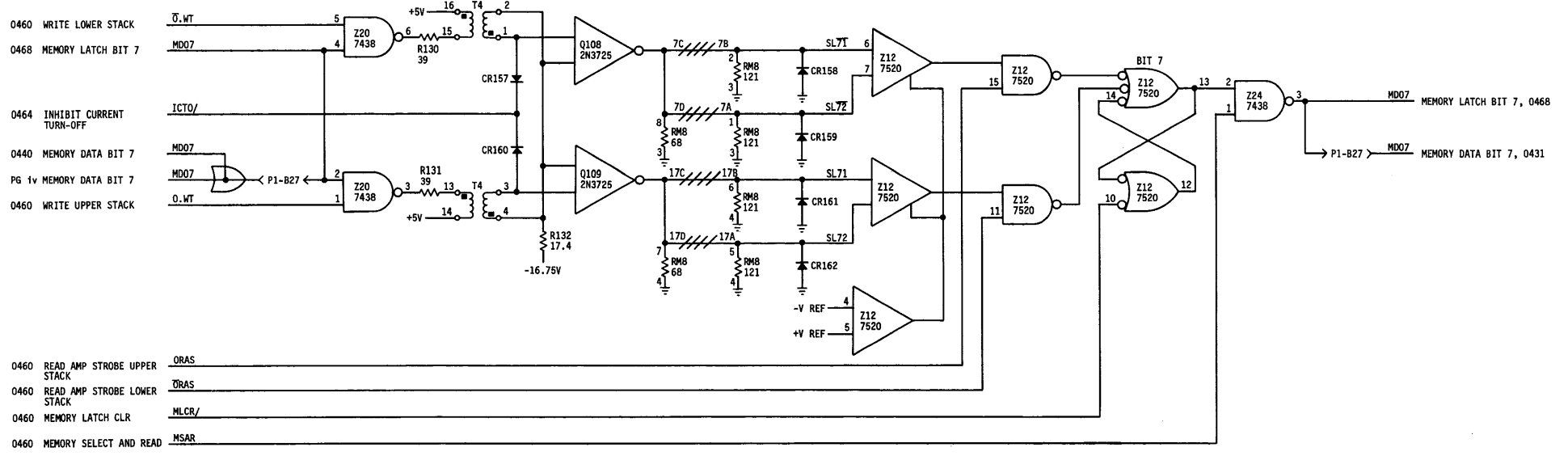
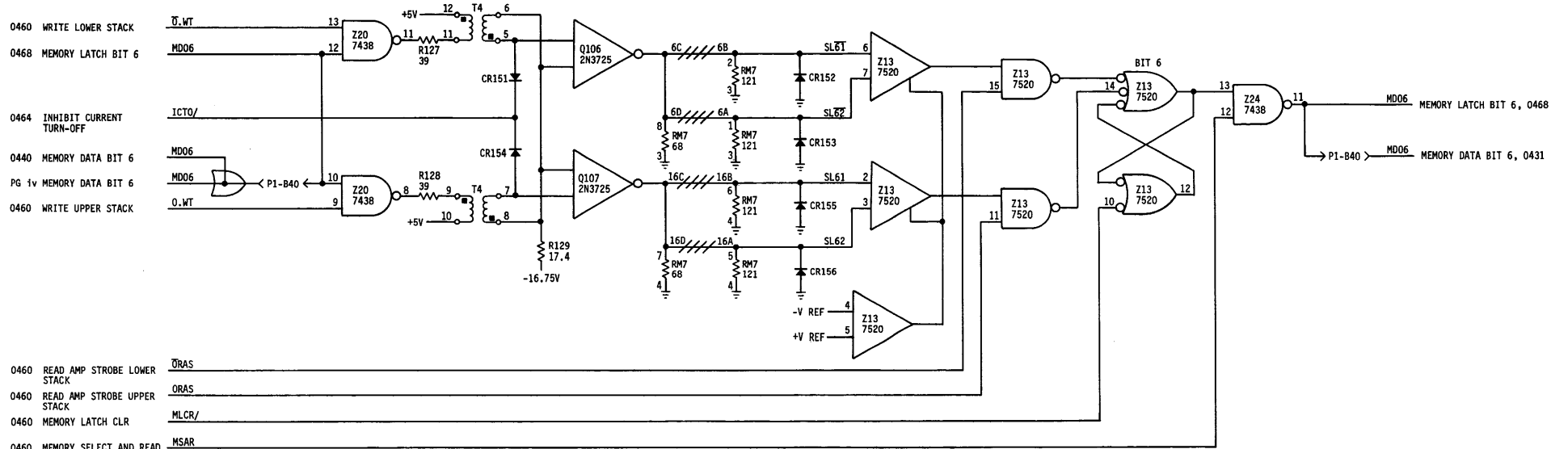
REV. AUG. 10, 1973
LD 1010
CENTRAL PROCESSING UNIT

MEMORY READ/WRITE BITS 0 AND 1

CORE MEMORY
0465





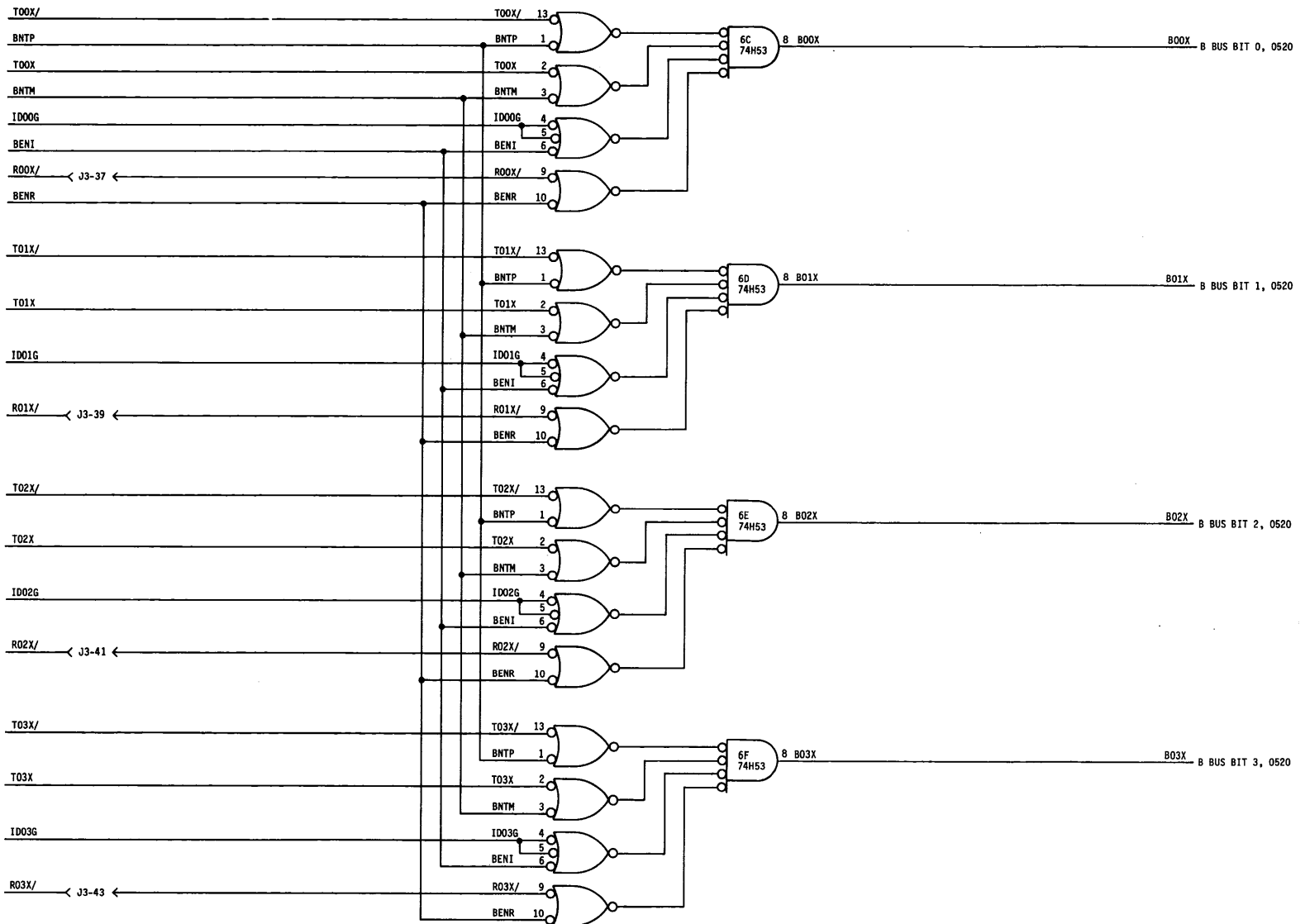


0430 T REG BIT 0
 0374 SEL UNCOMP T REG TO B BUS
 0430 T REG BIT 0
 0374 SEL COMP T REG TO B BUS
 0810 INPUT DATA BIT 0
 0374 INPUT DATA TO B BUS
 0360 R REG BIT 0
 0374 R REG TO B BUS

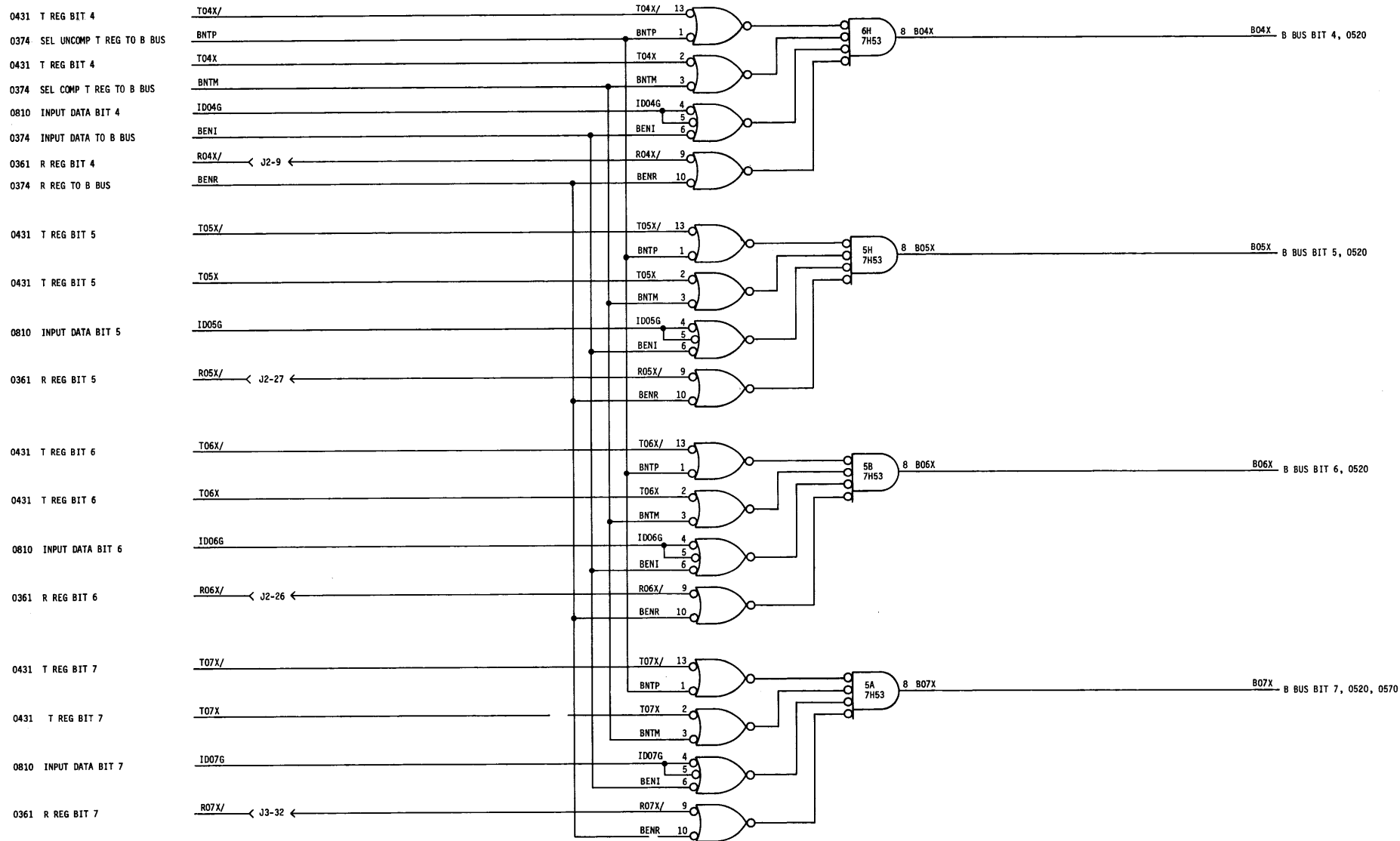
0430 T REG BIT 1
 0430 T REG BIT 1
 0810 INPUT DATA BIT 1
 0360 R REG BIT 1

0430 T REG BIT 2
 0430 T REG BIT 2
 0810 INPUT DATA BIT 2
 0360 R REG BIT 2

0430 T REG BIT 3
 0430 T REG BIT 3
 0810 INPUT DATA BIT 3
 0360 R REG BIT 3



B BUS MULTIPLEXER BITS 4-7



0560 INITIAL CARRY

0550 FILE BIT 0

0510 B BUS BIT 0

0550 FILE BIT 1

0510 B BUS BIT 1

0550 FILE BIT 2

0510 B BUS BIT 2

0550 FILE BIT 3

0510 B BUS BIT 3

0550 FILE BIT 4

0511 B BUS BIT 4

0550 FILE BIT 5

0511 B BUS BIT 5

0550 FILE BIT 6

0511 B BUS BIT 6

0550 FILE BIT 7

0511 B BUS BIT 7

0370 OR COMMAND

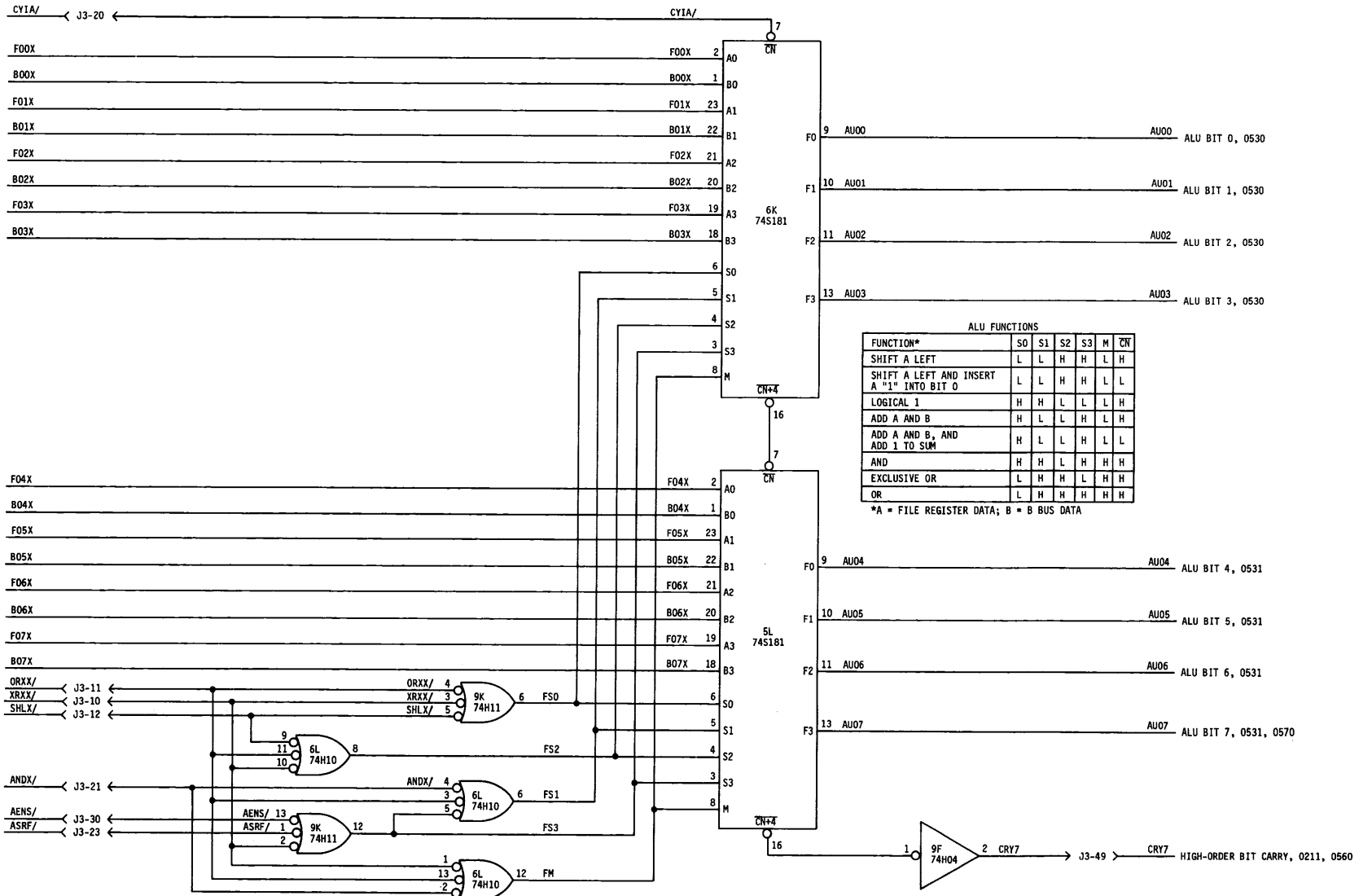
0370 EXCLUSIVE OR COMMAND

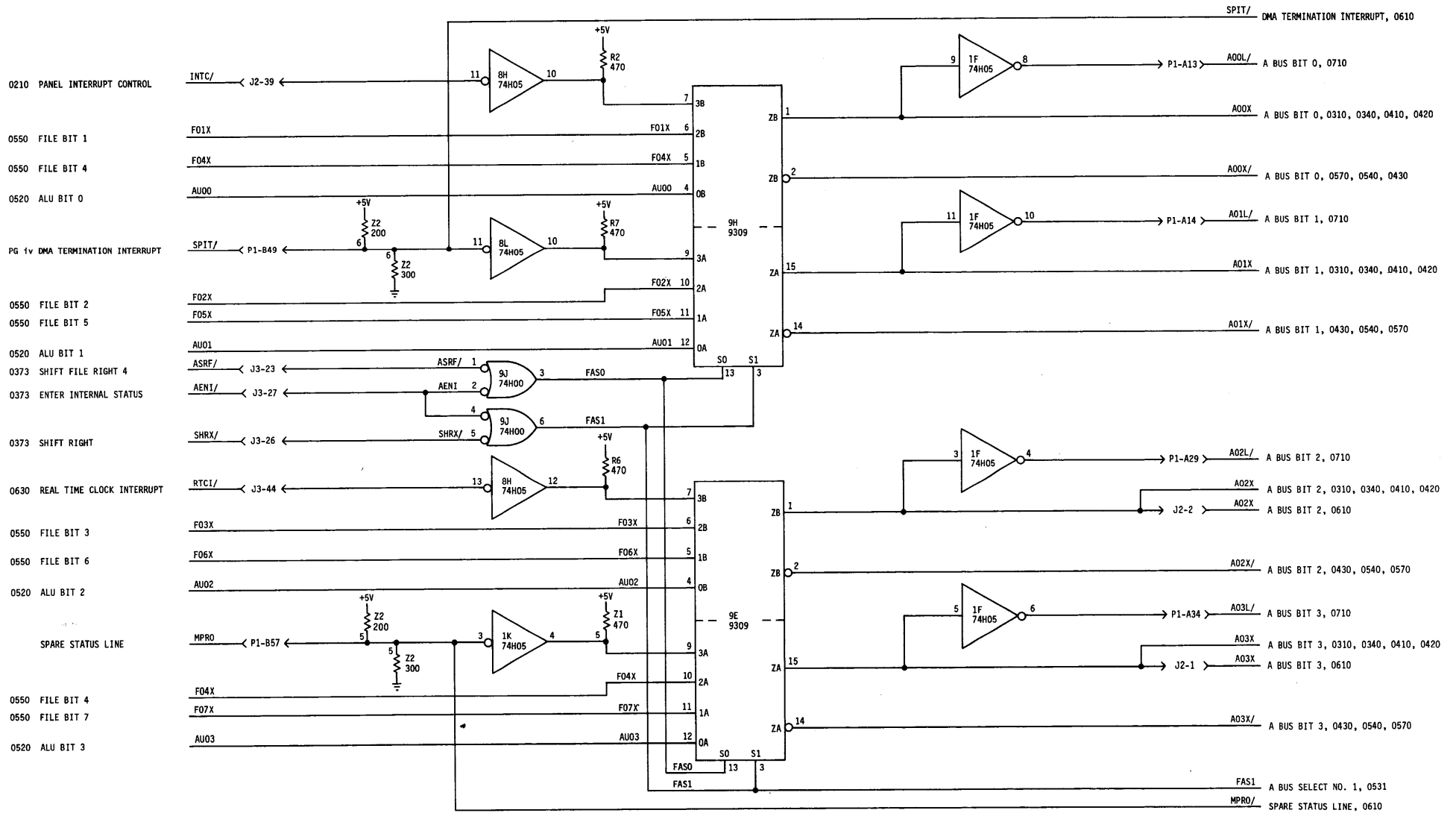
0372 SHIFT LEFT

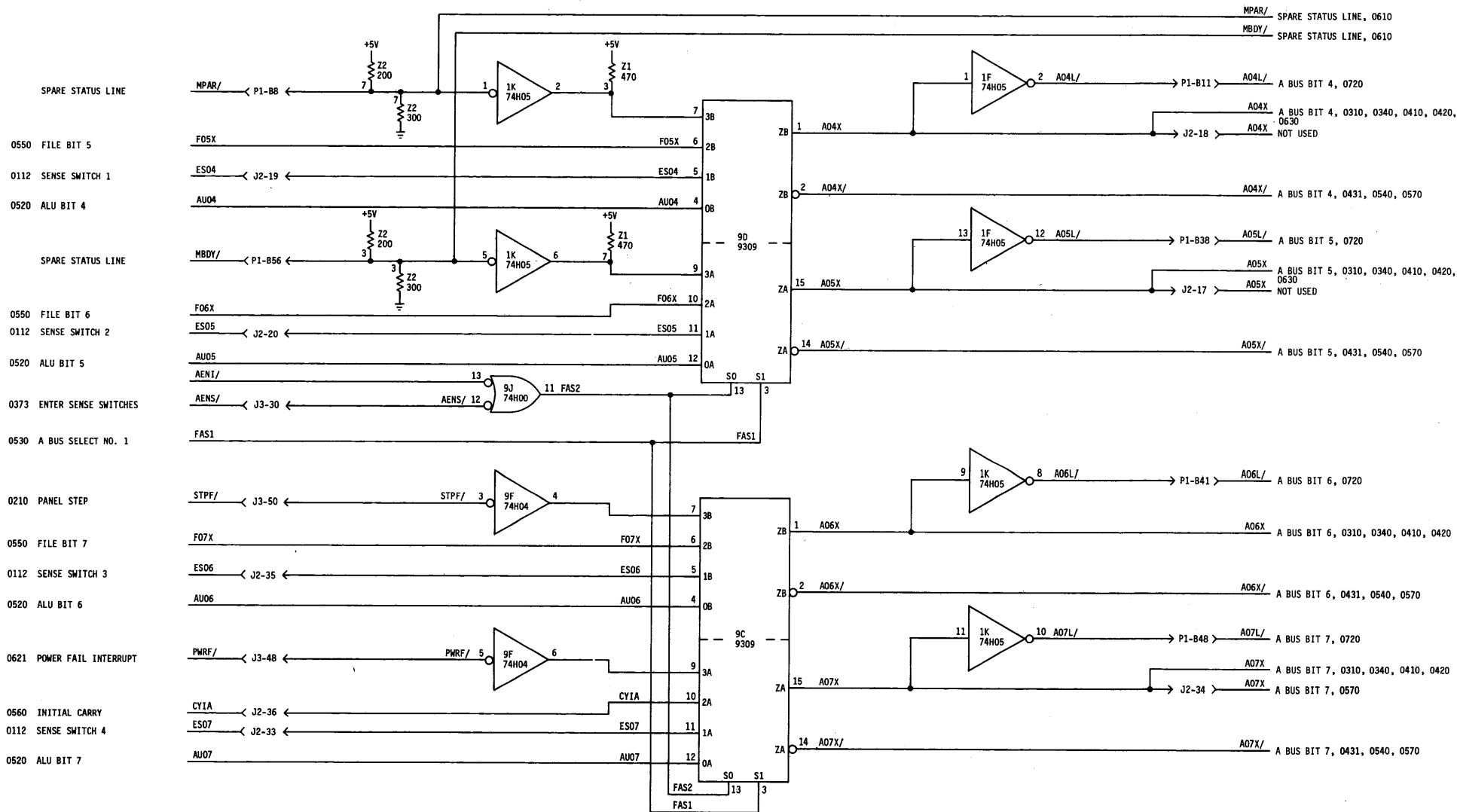
0372 LOGICAL AND

0373 ENTER SENSE SWITCHES

0373 SHIFT FILE RIGHT 4







0550 SELECT SECONDARY FILE
0362 R REG BIT 8-11
0530 A BUS BIT 0-3
0531 A BUS BIT 4-7

0550 SELECT PRIMARY FILE
0230 FILE WRITE CLOCK

0570 OVERFLOW CONDITION

0570 NEGATIVE CONDITION

0570 ZERO CONDITION

PG 1v CONCURRENT I/O REQUEST

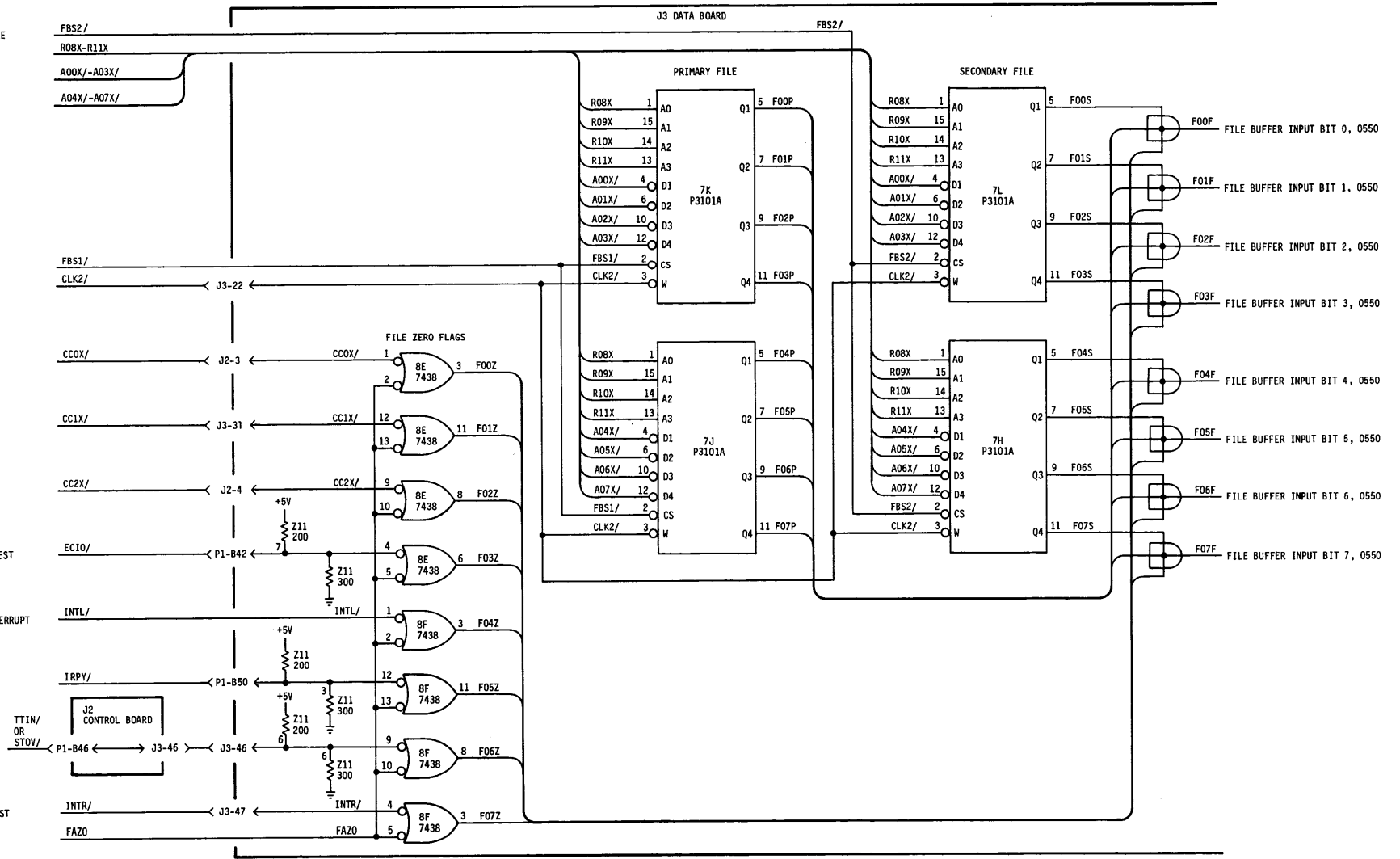
0610 INTERNAL STATUS INTERRUPT

0912 SPARE STATUS LINE

NOT USED

0610 EXT INTERRUPT REQUEST

0550 SELECT FILE ZERO



0372 FILE INHIBIT

0540 FILE BUFFER INPUT BIT 0
0540 FILE BUFFER INPUT BIT 1
0540 FILE BUFFER INPUT BIT 2
0540 FILE BUFFER INPUT BIT 3

0540 FILE BUFFER INPUT BIT 4
0540 FILE BUFFER INPUT BIT 5
0540 FILE BUFFER INPUT BIT 6
0540 FILE BUFFER INPUT BIT 7

0220 FILE BUFFER CLOCK

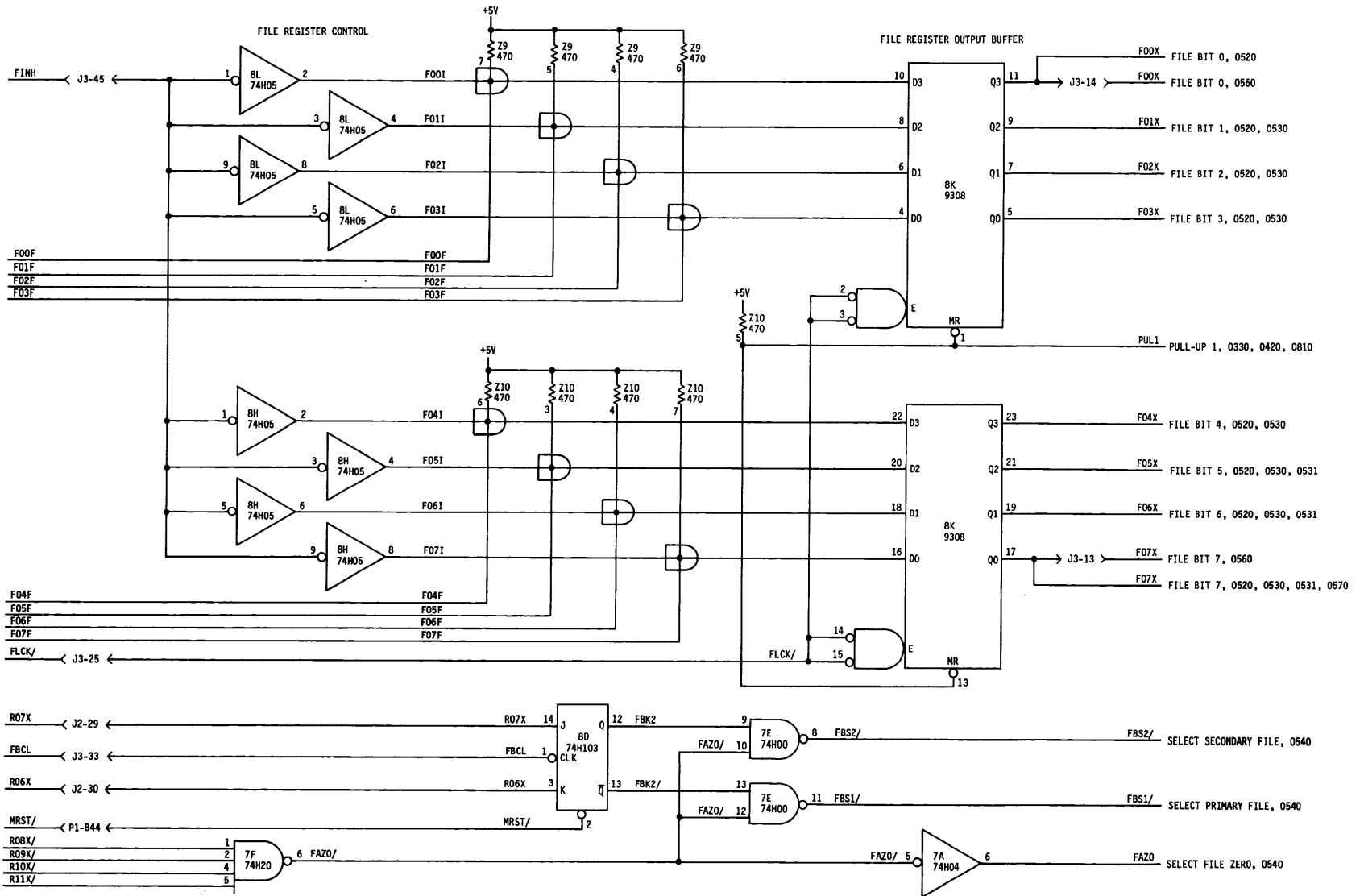
0361 R REG BIT 7

0371 FILE SELECT CLOCK

0361 R REG BIT 6

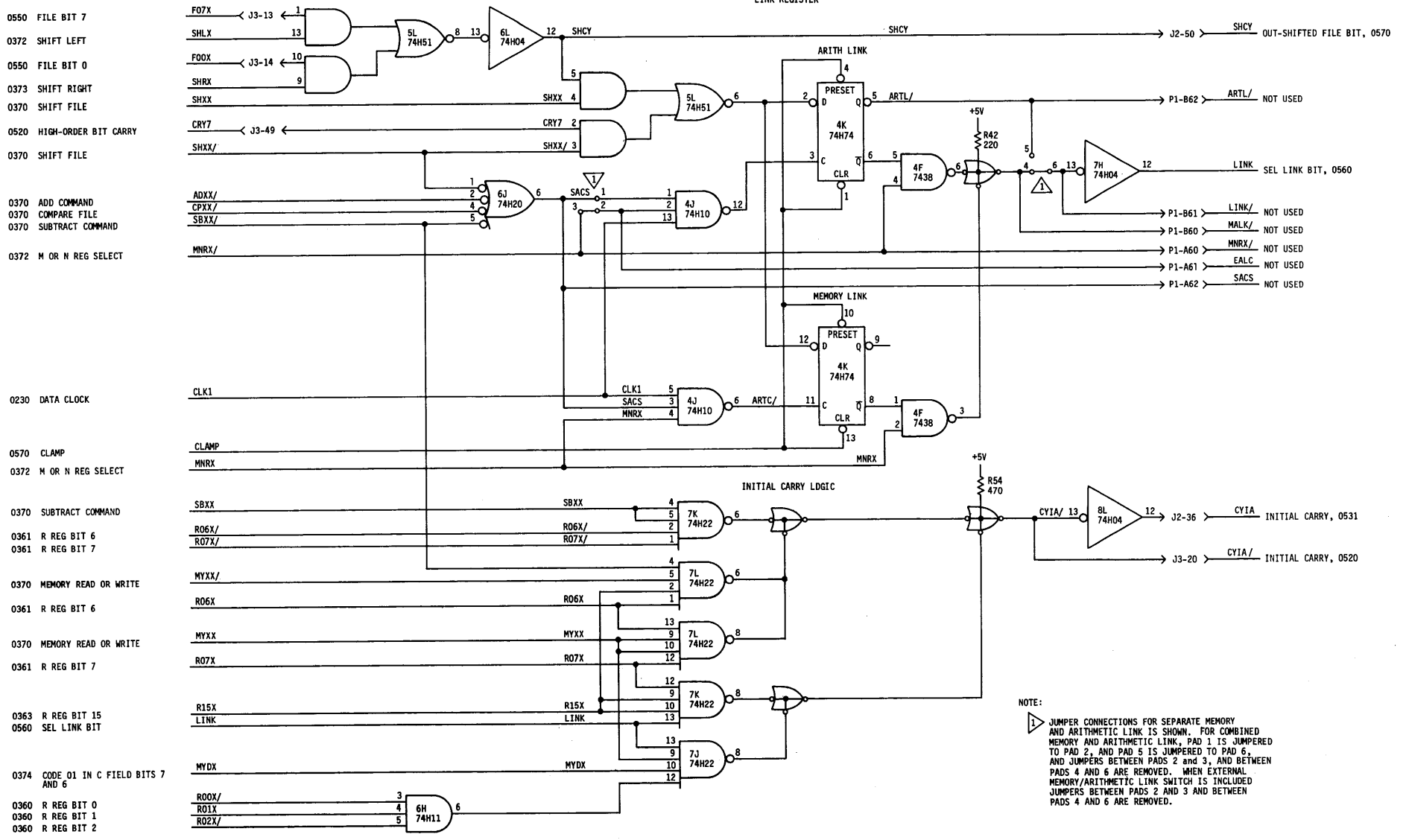
PG 1v MASTER RESET

0362 R REG BIT 8
0362 R REG BIT 9
0362 R REG BIT 10
0362 R REG BIT 11



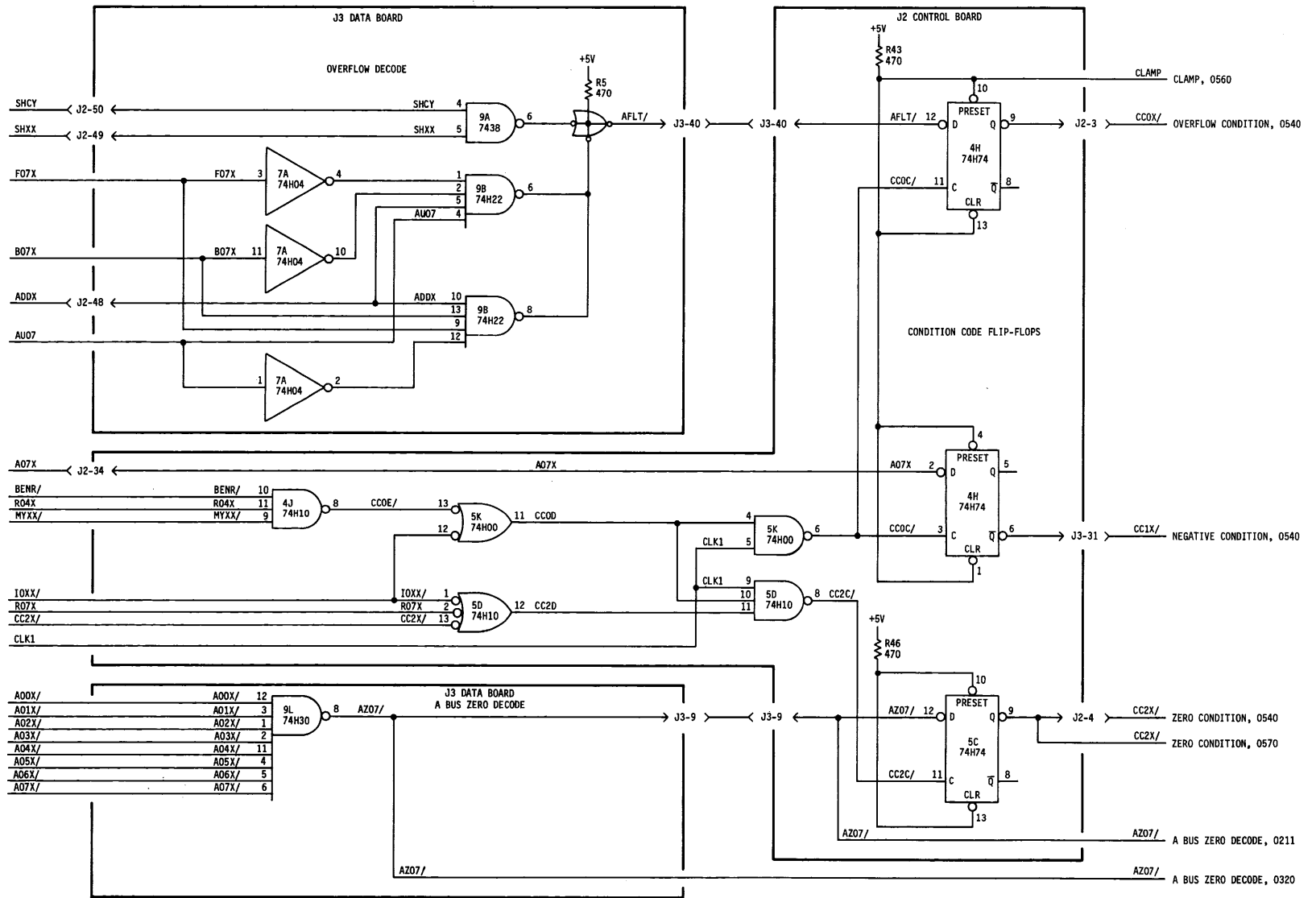
FILE REGISTER CONTROL AND FILE REGISTER OUTPUT BUFFER

LINK REGISTER AND INITIAL CARRY LOGIC



- 0550 FILE BIT 7
- 0372 SHIFT LEFT
- 0550 FILE BIT 0
- 0373 SHIFT RIGHT
- 0370 SHIFT FILE
- 0520 HIGH-ORDER BIT CARRY
- 0370 SHIFT FILE
- 0370 ADD COMMAND
- 0370 COMPARE FILE
- 0370 SUBTRACT COMMAND
- 0372 M OR N REG SELECT
- 0230 DATA CLOCK
- 0570 CLAMP
- 0372 M OR N REG SELECT
- 0370 SUBTRACT COMMAND
- 0361 R REG BIT 6
- 0361 R REG BIT 7
- 0370 MEMORY READ OR WRITE
- 0361 R REG BIT 6
- 0370 MEMORY READ OR WRITE
- 0361 R REG BIT 7
- 0363 R REG BIT 15
- 0560 SEL LINK BIT
- 0374 CODE 01 IN C FIELD BITS 7 AND 6
- 0360 R REG BIT 0
- 0360 R REG BIT 1
- 0360 R REG BIT 2

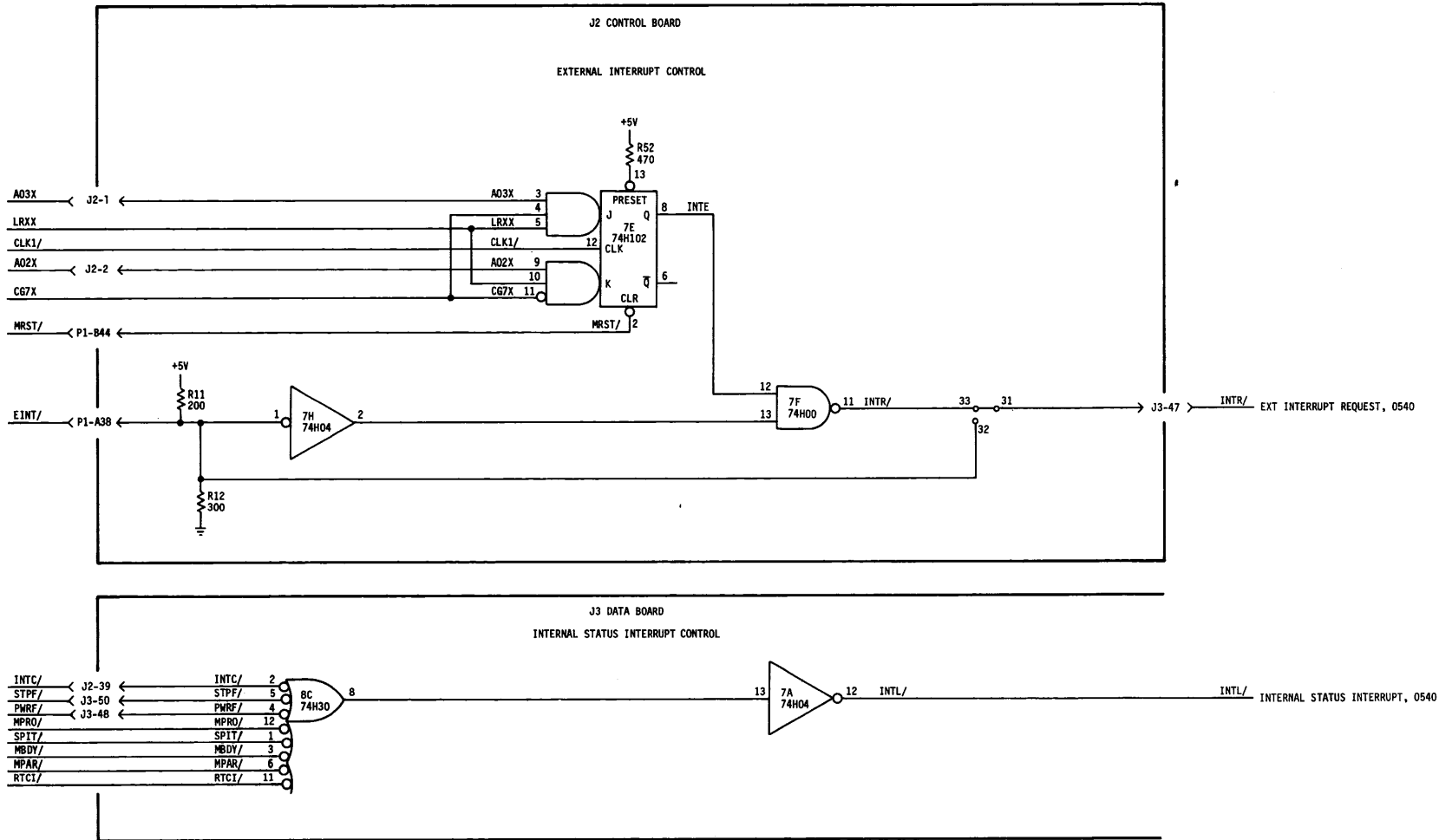
- 0560 OUT-SHIFTED FILE BIT
- 0370 SHIFT FILE
- 0550 FILE BIT 7
- 0511 B BUS BIT 7
- 0372 OP CODES 0-3, 6, 8-BB
- 0520 ALU BIT 7
- 0531 A BUS BIT 7
- 0374 R REG TO B BUS
- 0361 R REG BIT 4
- 0370 MEMORY READ OR WRITE
- 0370 OP CODE 7
- 0361 R REG BIT 7
- 0570 ZERO CONDITION
- 0230 DATA CLOCK
- 0530 A BUS BIT 0
- 0530 A BUS BIT 1
- 0530 A BUS BIT 2
- 0530 A BUS BIT 3
- 0531 A BUS BIT 4
- 0531 A BUS BIT 5
- 0531 A BUS BIT 6
- 0531 A BUS BIT 7



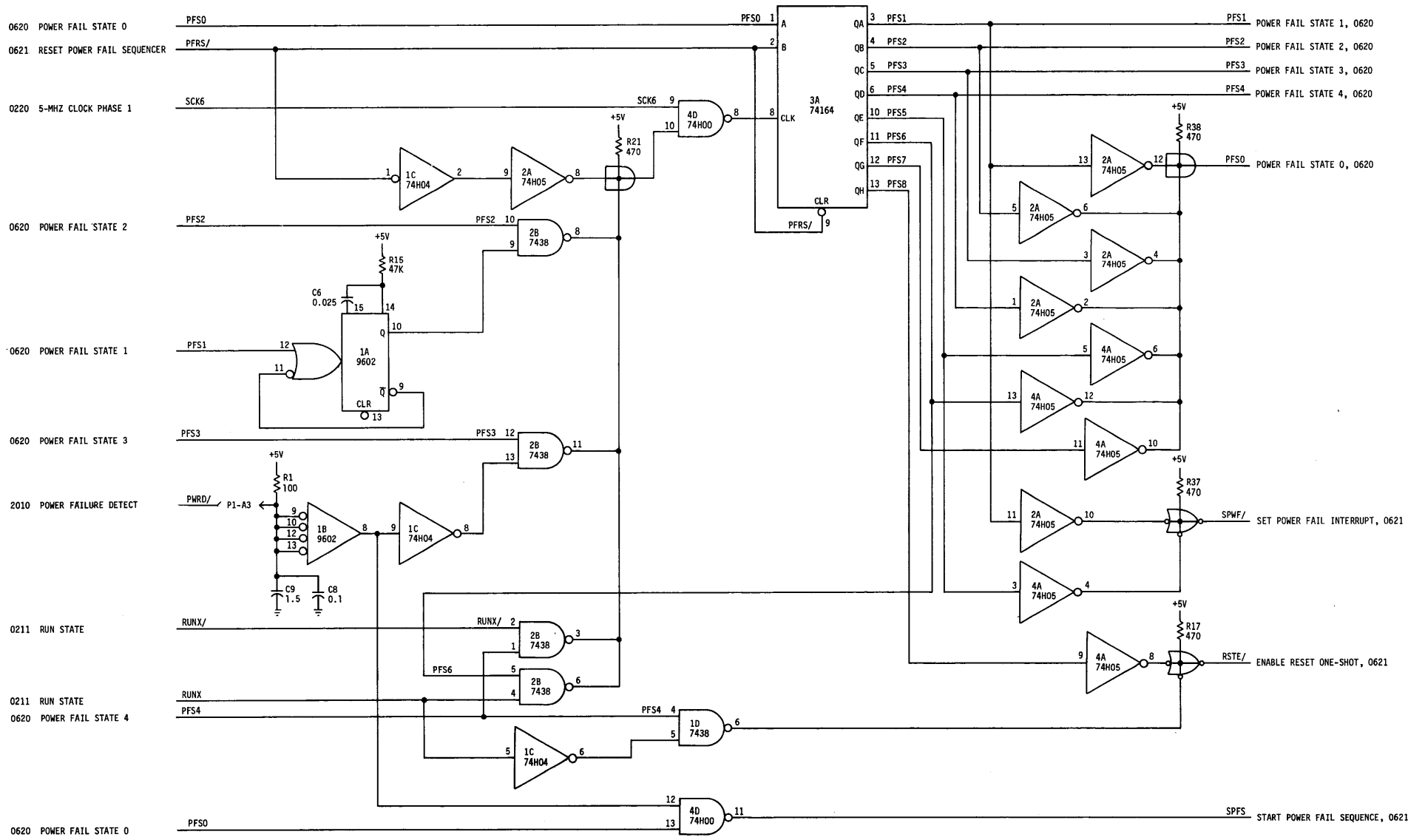
0530 A BUS BIT 3
 0370 LOAD LITERAL
 0230 DATA CLOCK
 0530 A BUS BIT 2
 0371 LOAD SEVEN
 PG 1v MASTER RESET

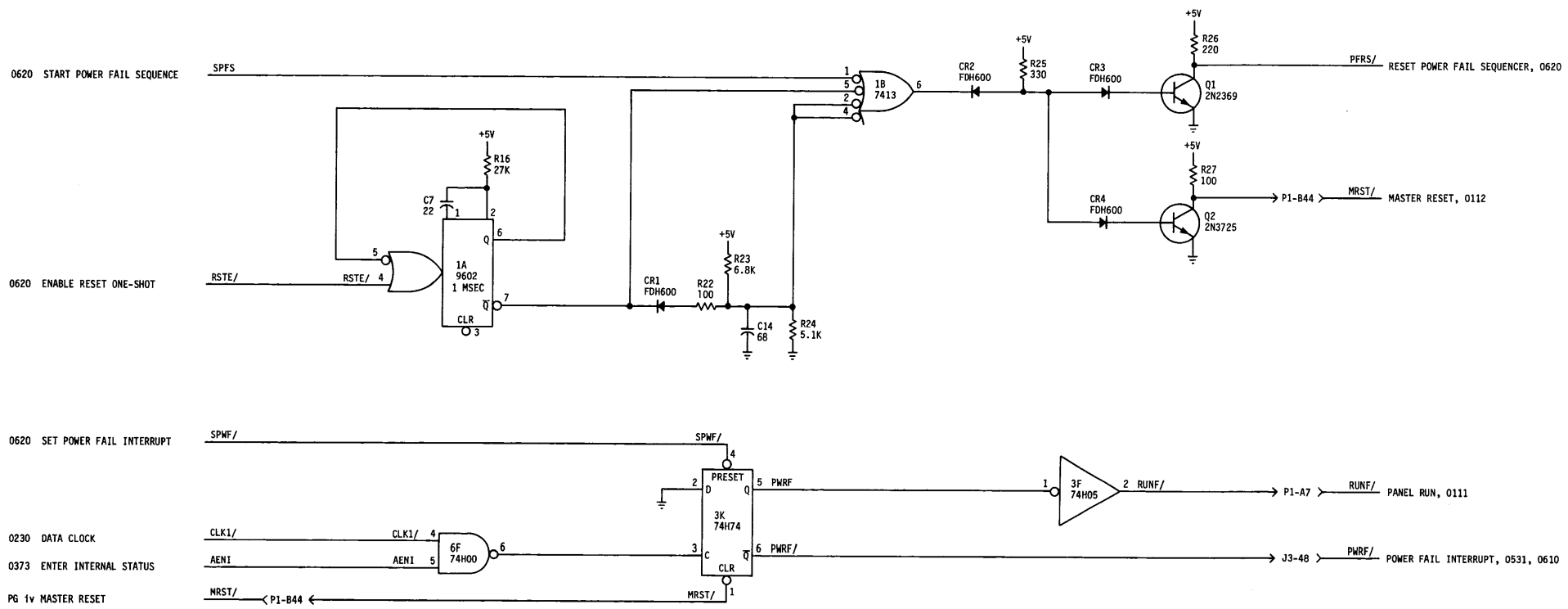
PG 1v EXTERNAL INTERRUPT

0210 PANEL INTERRUPT CONTROL
 0210 PANEL STEP
 0621 POWER FAIL INTERRUPT
 0530 SPARE STATUS LINE
 0530 DMA TERMINATION INTERRUPT
 0531 SPARE STATUS LINE
 0531 SPARE STATUS LINE
 0630 REAL TIME CLOCK INTERRUPT



POWER FAIL 1





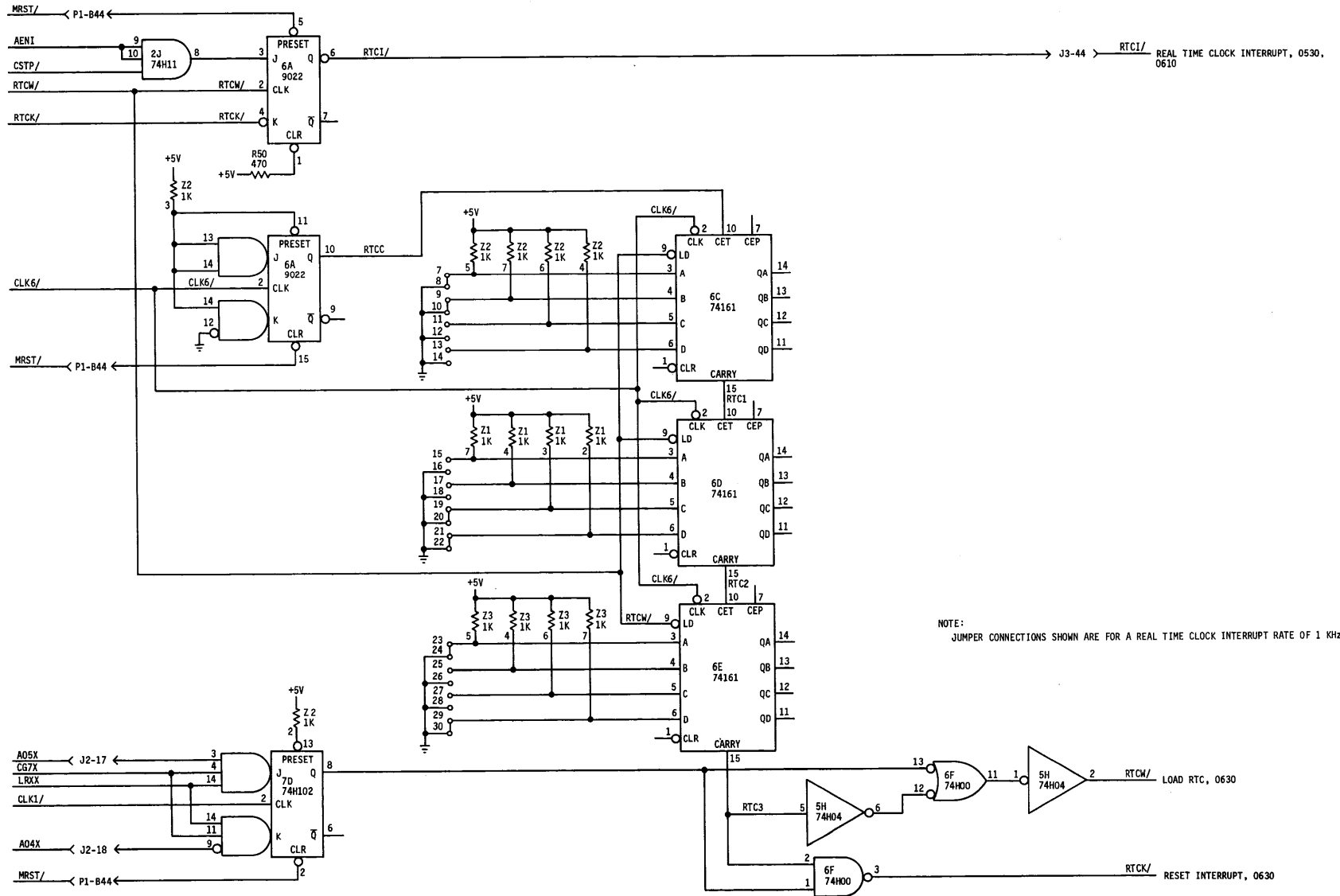
PG 1v MASTER RESET
0373 ENTER INTERNAL STATUS
0211 CLOCK STOP
0630 LOAD RTC
0630 RESET INTERRUPT

0230 5-MHZ CLOCK PHASE 2

PG 1v MASTER RESET

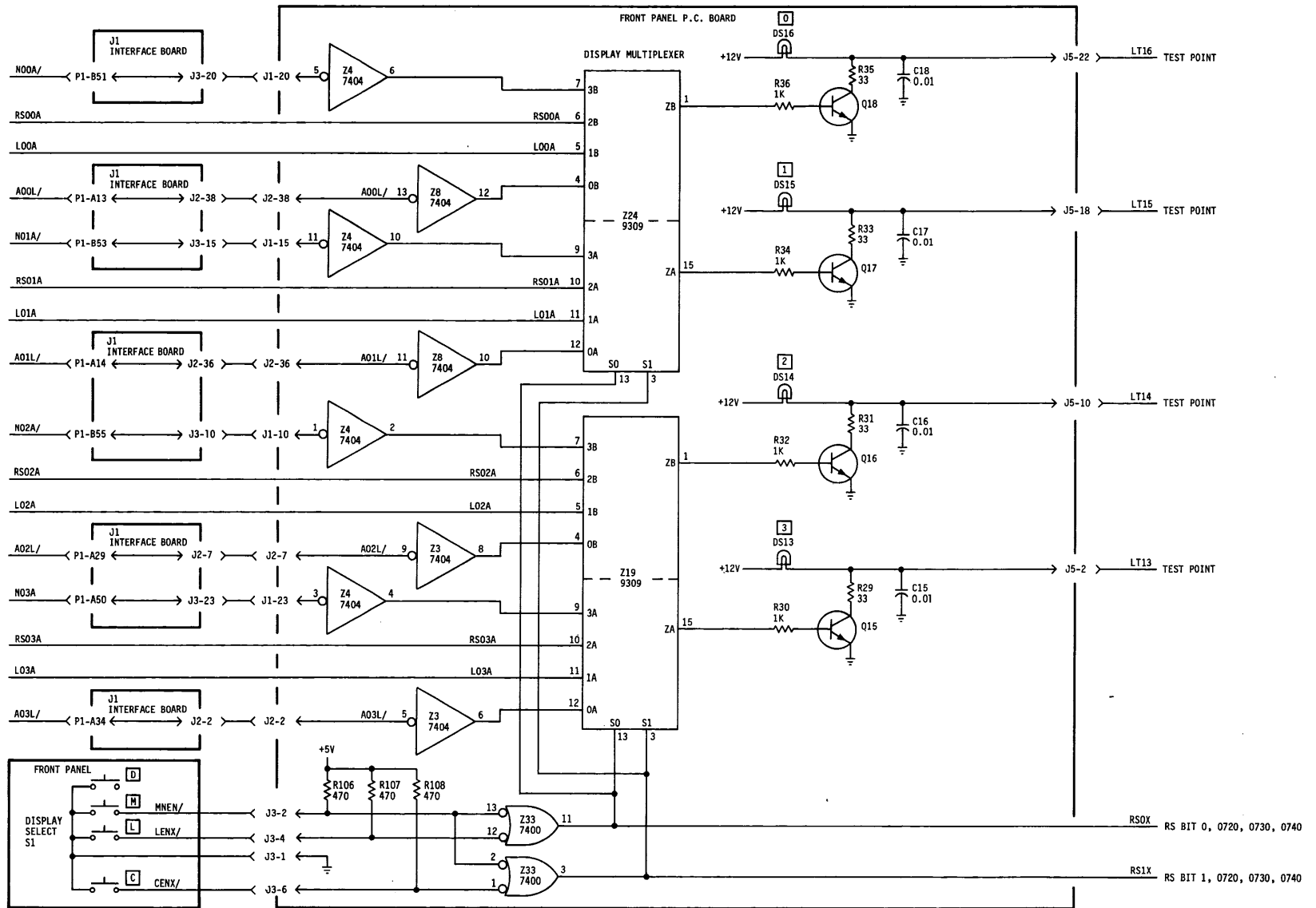
0531 A BUS BIT 5
0371 LOAD SEVEN
0370 LOAD LITERAL
0230 DATA CLOCK

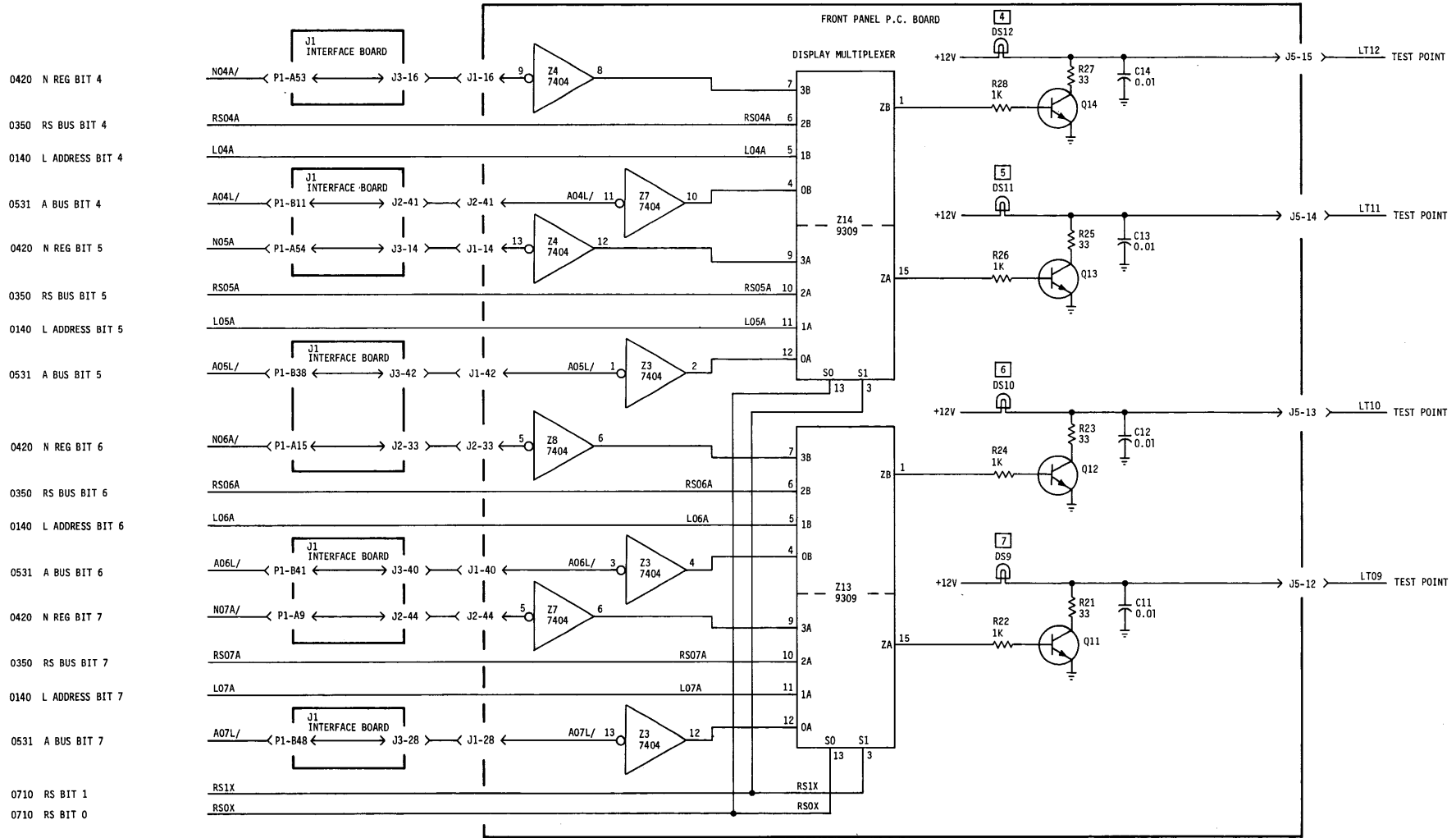
0531 A BUS BIT 4
PG 1v MASTER RESET

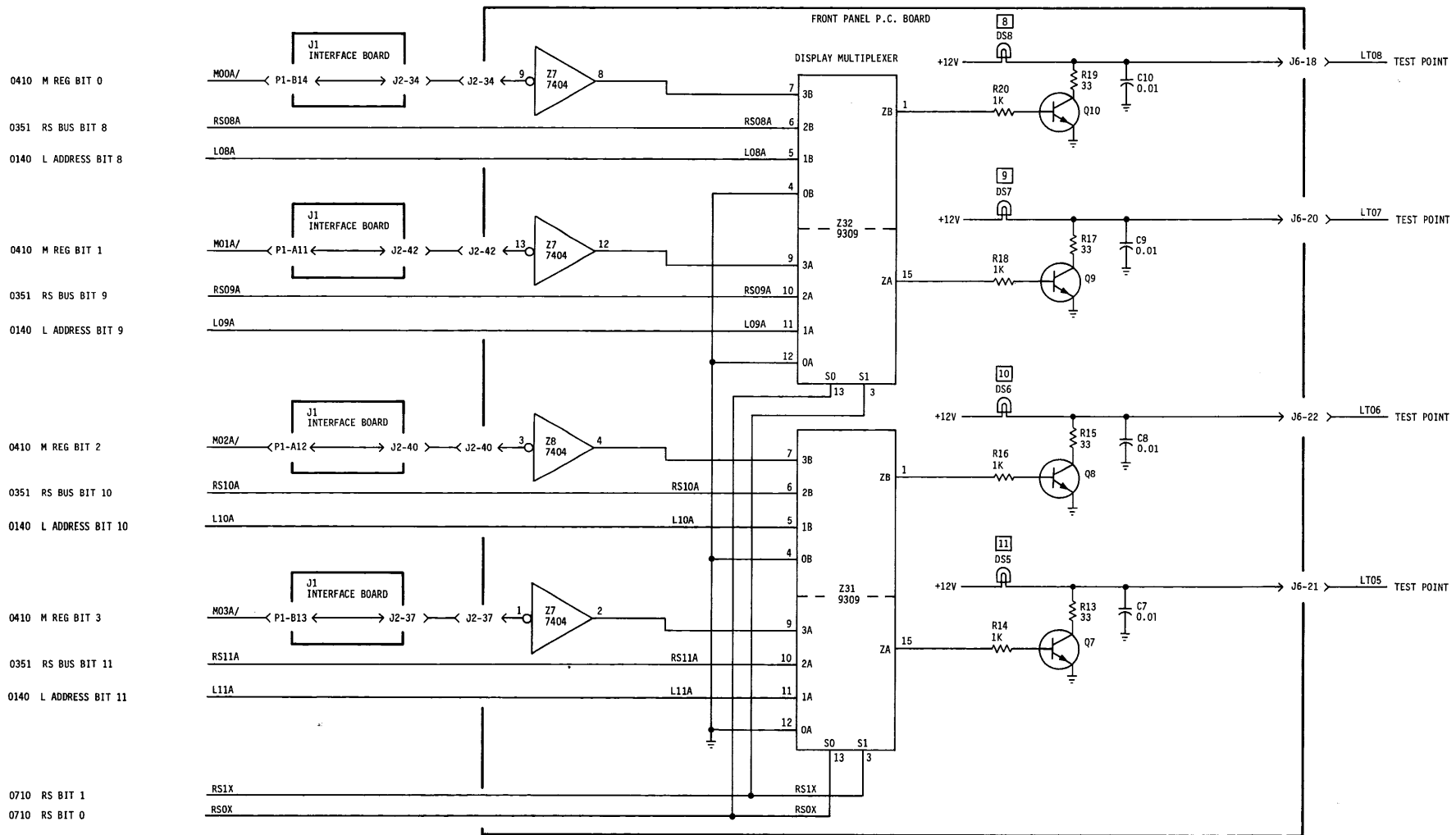


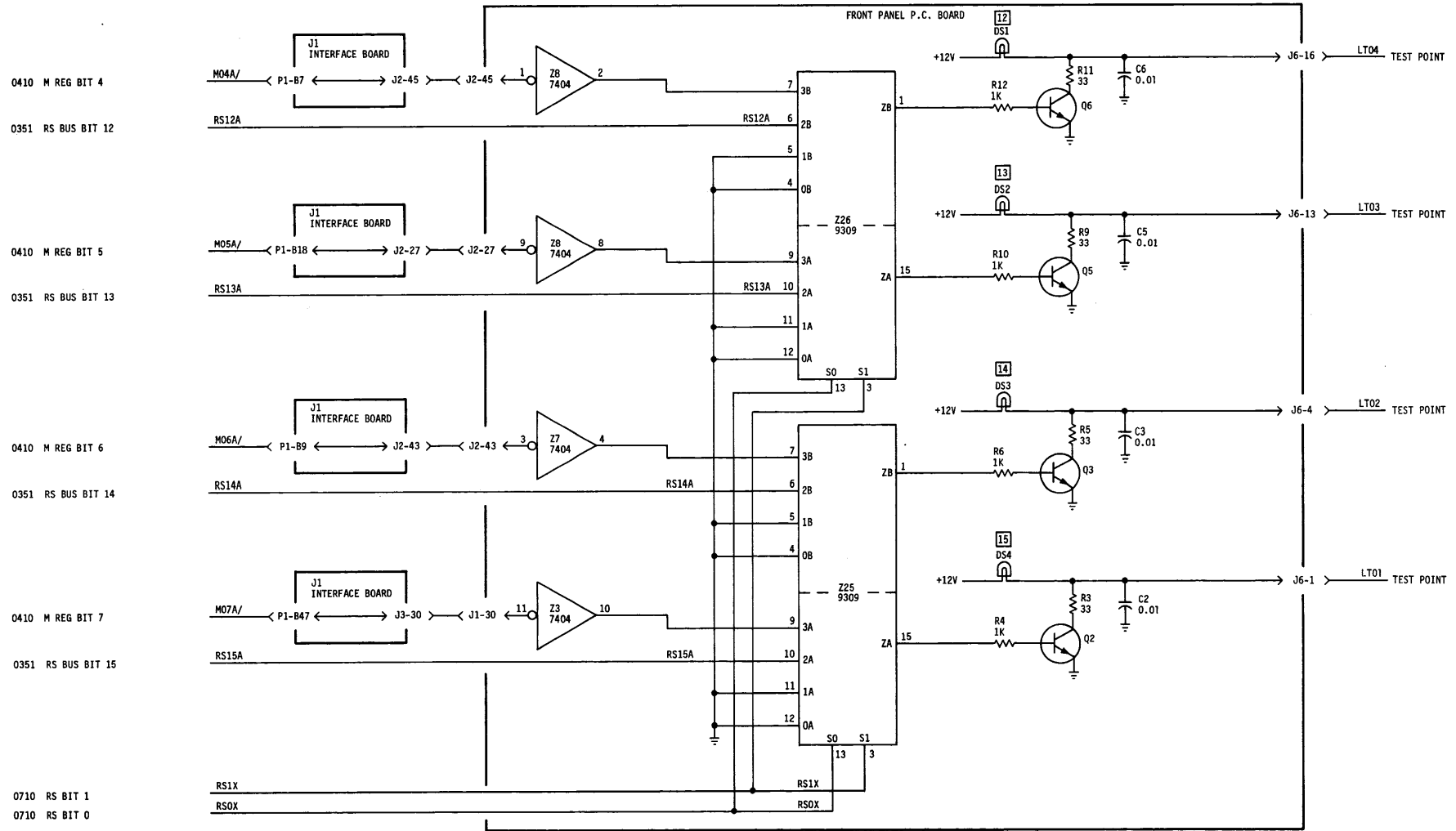
NOTE:
JUMPER CONNECTIONS SHOWN ARE FOR A REAL TIME CLOCK INTERRUPT RATE OF 1 KHz

0420 N REG BIT 0
 0350 RS BUS BIT 0
 0140 L ADDRESS BIT 0
 0530 A BUS BIT 0
 0420 N REG BIT 1
 0350 RS BUS BIT 1
 0140 L ADDRESS BIT 1
 0530 A BUS BIT 1
 0420 N REG BIT 2
 0350 RS BUS BIT 2
 0140 L ADDRESS BIT 2
 0530 A BUS BIT 2
 0420 N REG BIT 3
 0350 RS BUS BIT 3
 0140 L ADDRESS BIT 3
 0530 A BUS BIT 3

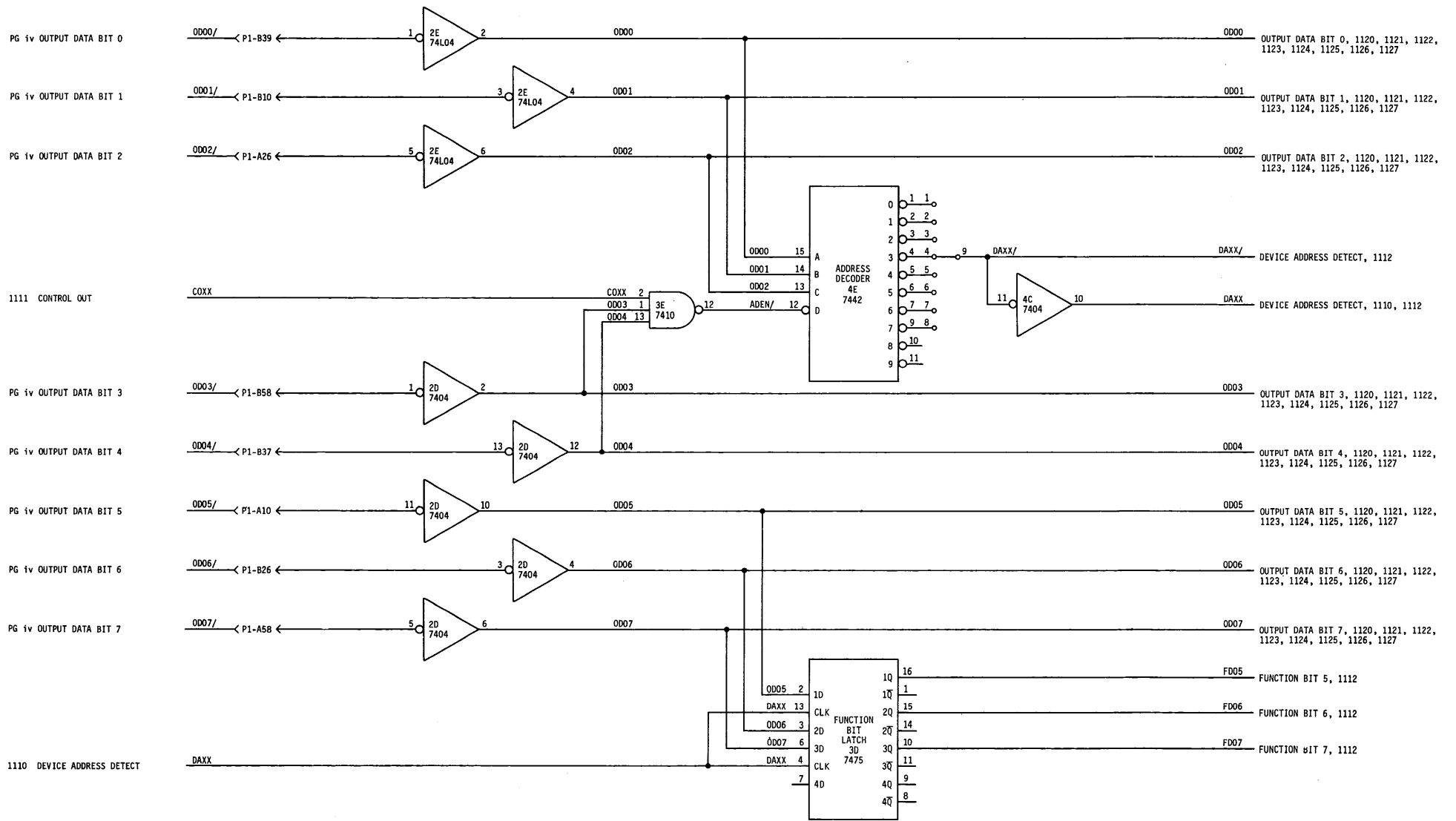


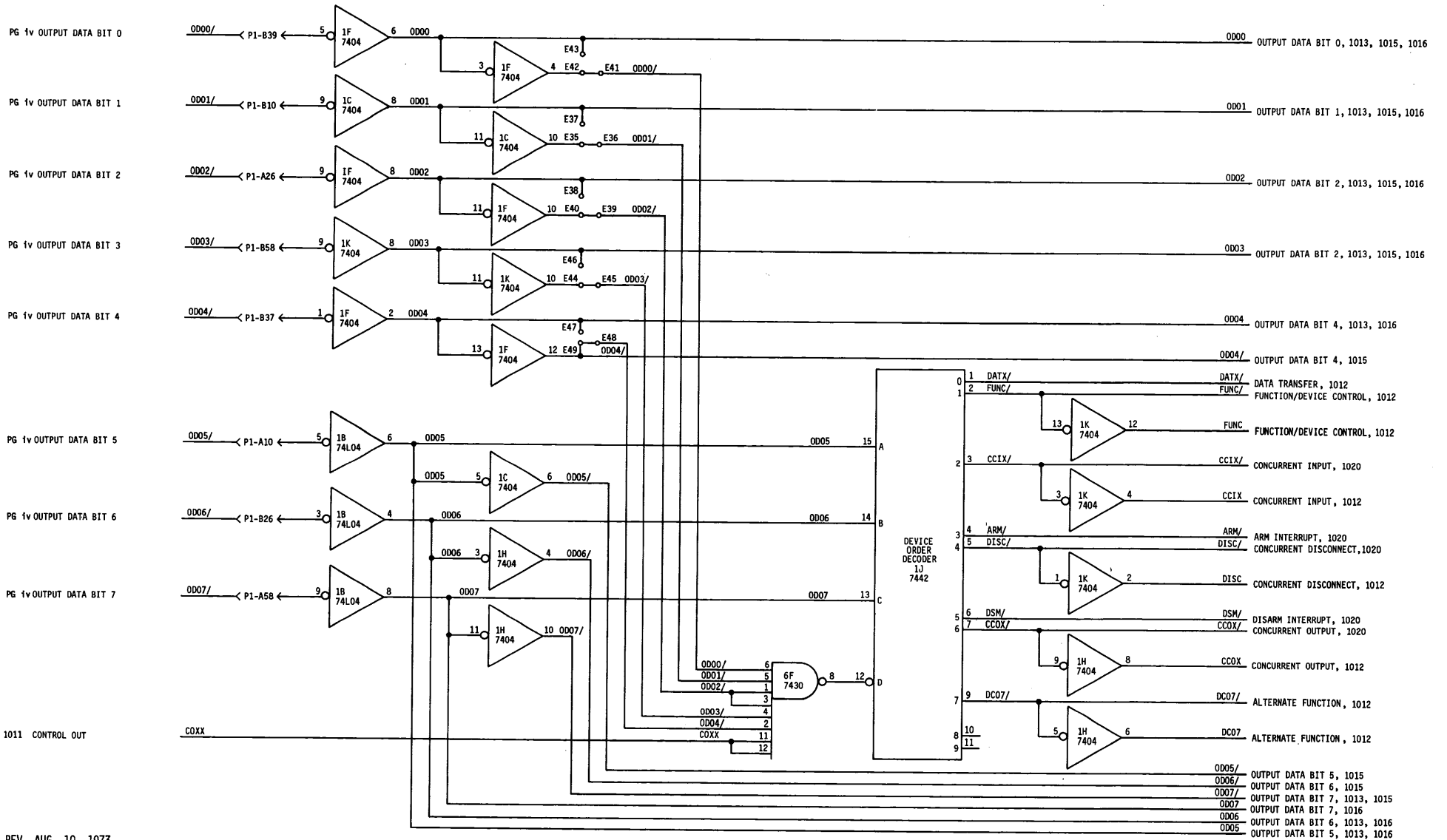




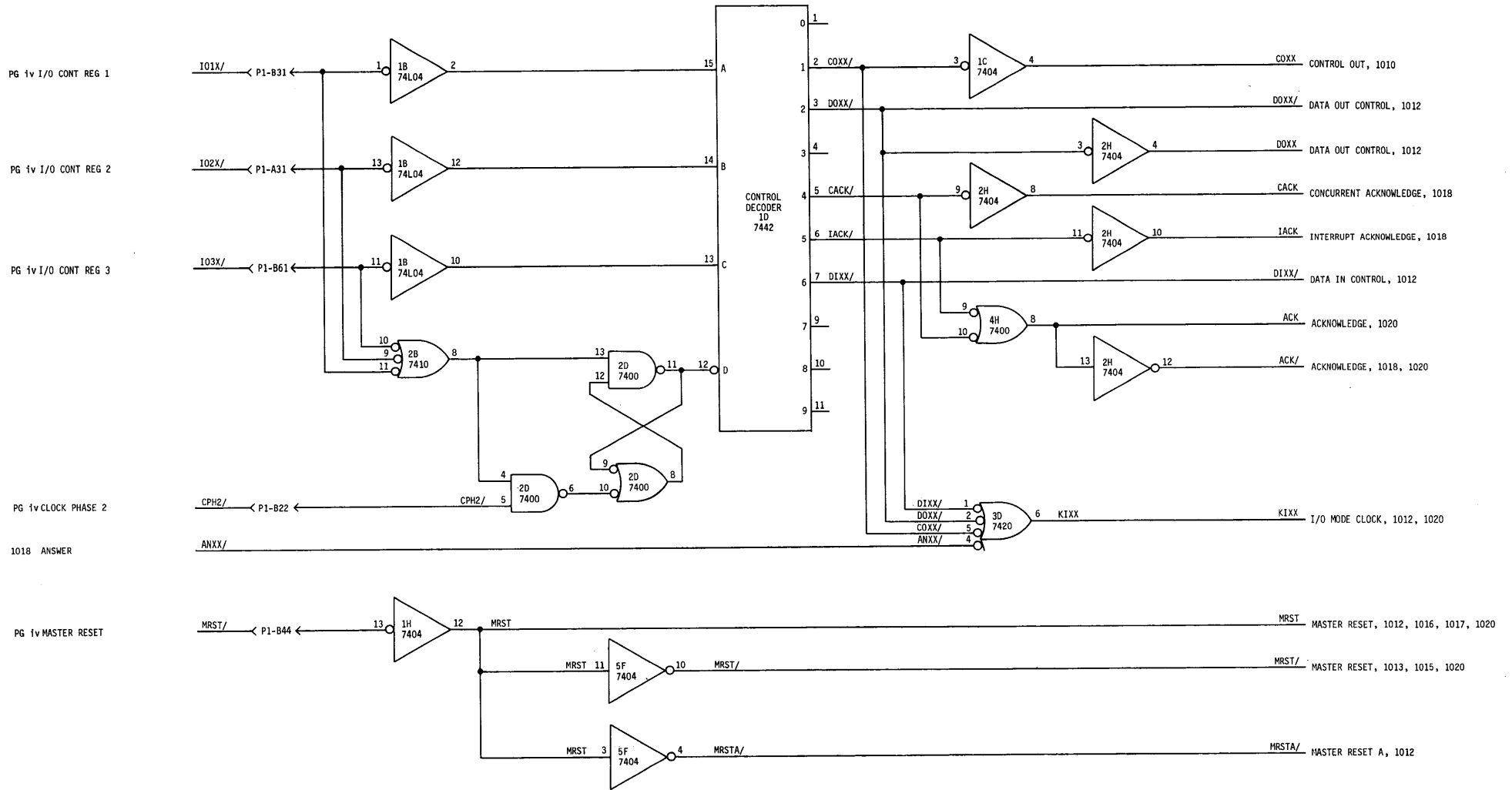


0710 RS BIT 1
0710 RS BIT 0

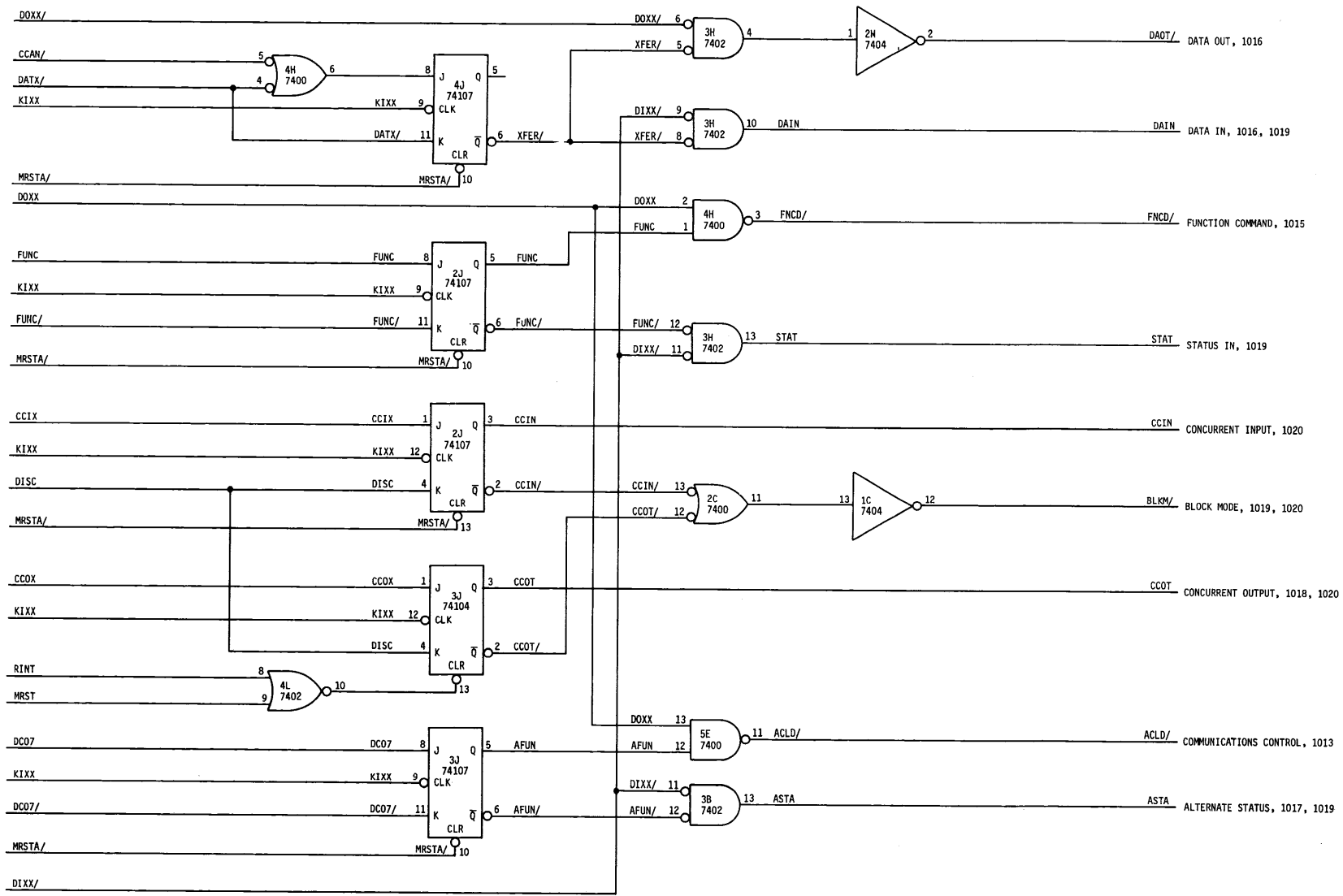




MASTER RESET AND CONTROL DECODER



1011 DATA OUT CONTROL
 1020 CONCURRENT ANSWER
 1010 DATA TRANSFER
 1011 I/O MODE CLOCK
 1011 MASTER RESET A
 1011 DATA OUT CONTROL
 1010 FUNCTION/DEVICE CONTROL
 1011 I/O MODE CLOCK
 1010 FUNCTION/DEVICE CONTROL
 1011 MASTER RESET A
 1010 CONCURRENT INPUT
 1011 I/O MODE CLOCK
 1010 CONCURRENT DISCONNECT
 1011 MASTER RESET A
 1010 CONCURRENT OUTPUT
 1011 I/O MODE CLOCK
 1020 RESET CONCURRENT OUTPUT
 1011 MASTER RESET
 1010 ALTERNATE FUNCTION
 1011 I/O MODE CLOCK
 1010 ALTERNATE FUNCTION
 1011 MASTER RESET A
 1011 DATA IN CONTROL



FUNCTION STORAGE REGISTERS

COMMUNICATIONS CONTROL BYTE STORAGE REGISTER

LOCAL/REMOTE SINGLE CHANNEL CONTROLLER

1012 COMMUNICATIONS CONTROL

1010 OUTPUT DATA BIT 0

1010 OUTPUT DATA BIT 1

1010 OUTPUT DATA BIT 2

1010 OUTPUT DATA BIT 3

1011 MASTER RESET

1012 COMMUNICATIONS CONTROL

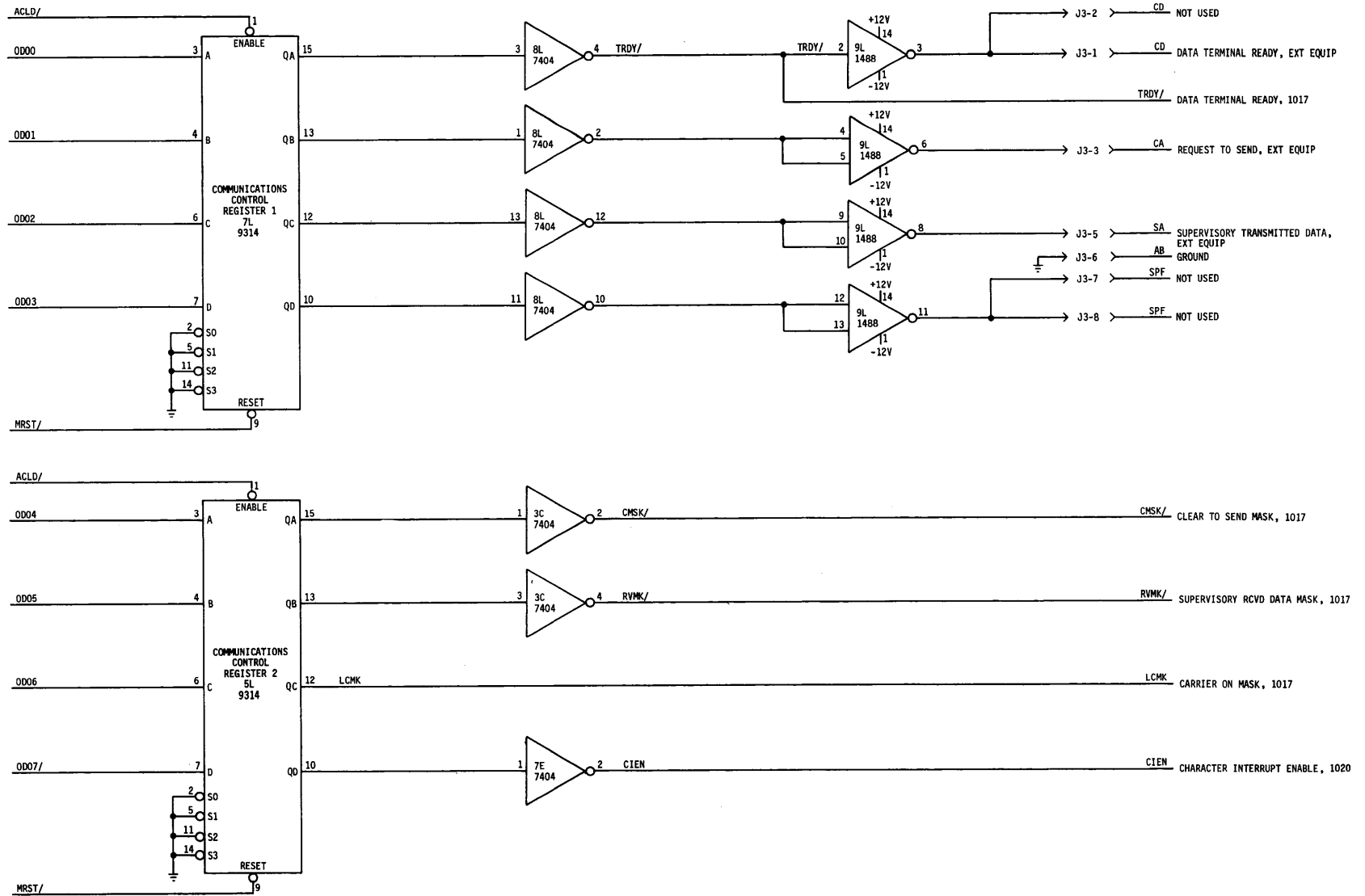
1010 OUTPUT DATA BIT 4

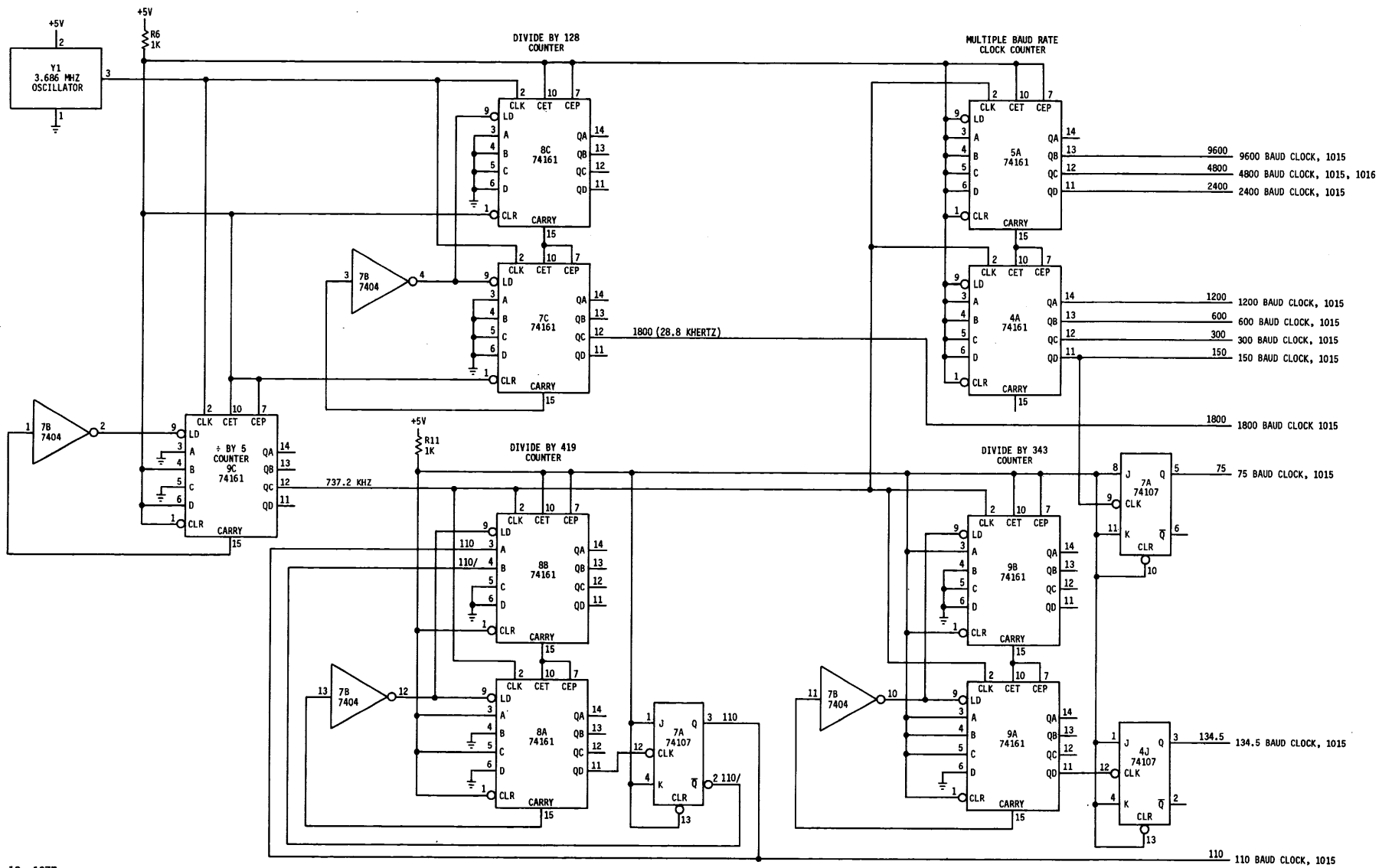
1010 OUTPUT DATA BIT 5

1010 OUTPUT DATA BIT 6

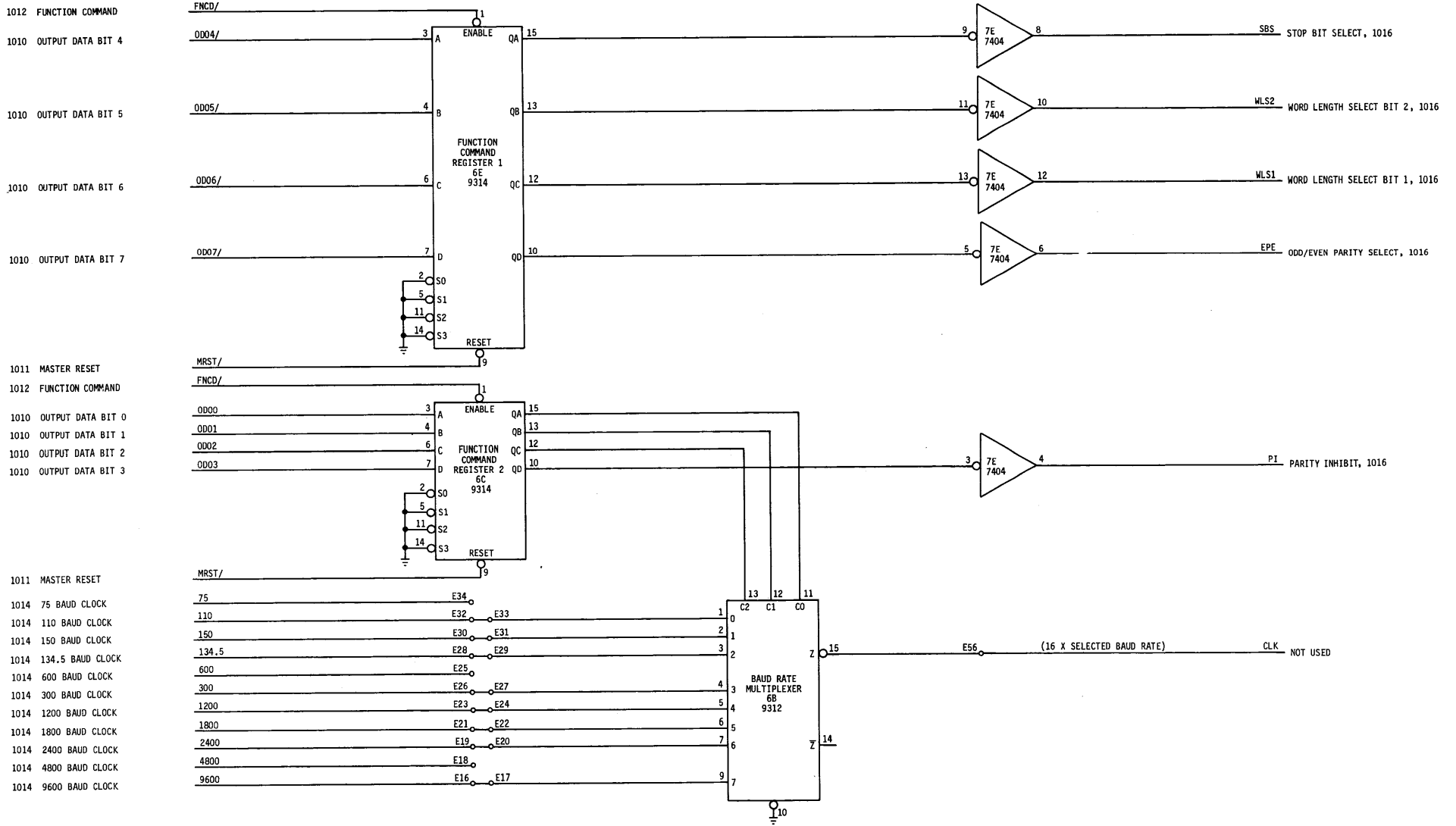
1010 OUTPUT DATA BIT 7

1011 MASTER RESET





FUNCTION COMMAND BYTE STORAGE REGISTER AND BAUD RATE SELECTOR



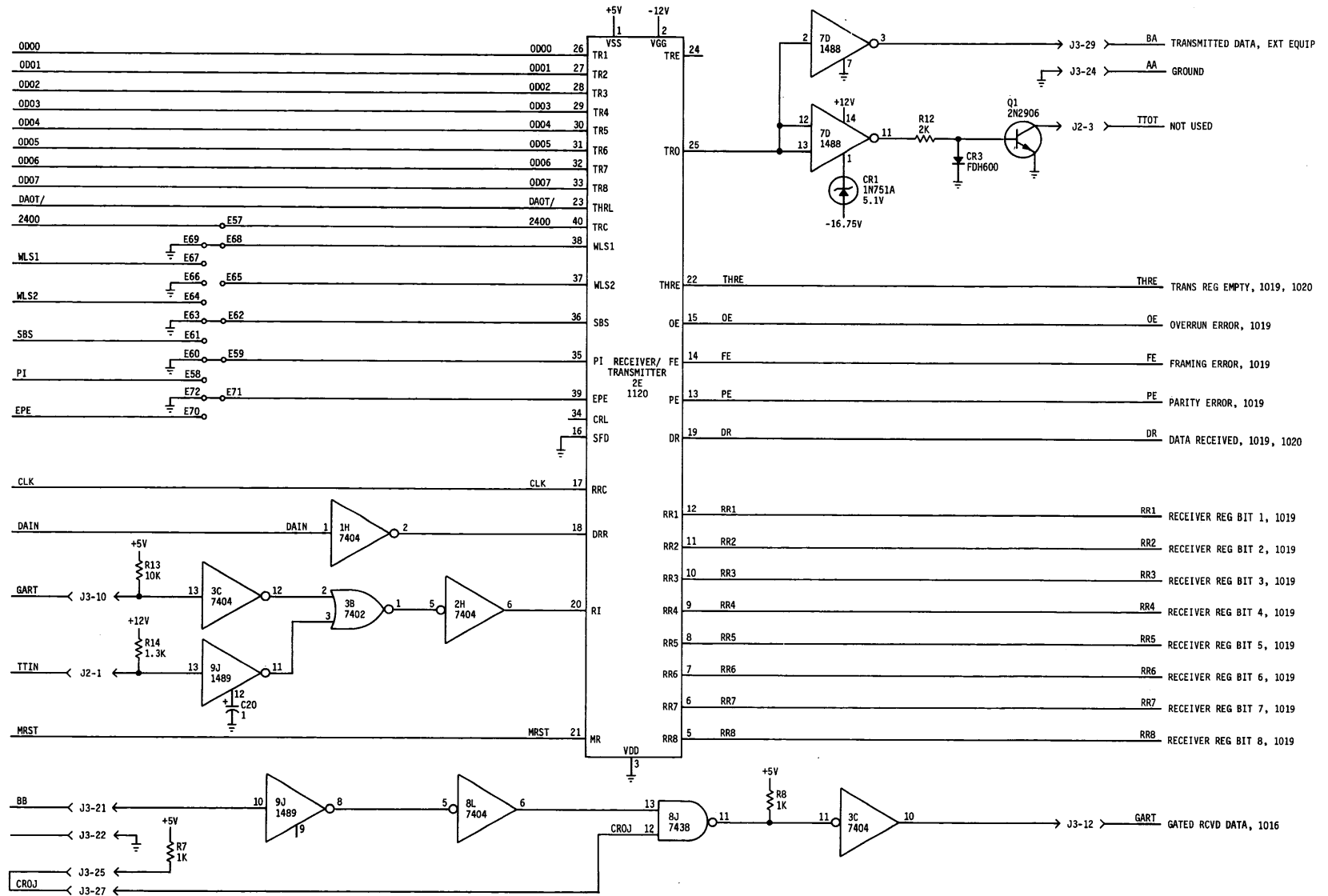
- 1012 FUNCTION COMMAND
- 1010 OUTPUT DATA BIT 4
- 1010 OUTPUT DATA BIT 5
- 1010 OUTPUT DATA BIT 6
- 1010 OUTPUT DATA BIT 7
- 1011 MASTER RESET
- 1012 FUNCTION COMMAND
- 1010 OUTPUT DATA BIT 0
- 1010 OUTPUT DATA BIT 1
- 1010 OUTPUT DATA BIT 2
- 1010 OUTPUT DATA BIT 3
- 1011 MASTER RESET
- 1014 75 BAUD CLOCK
- 1014 110 BAUD CLOCK
- 1014 150 BAUD CLOCK
- 1014 134.5 BAUD CLOCK
- 1014 600 BAUD CLOCK
- 1014 300 BAUD CLOCK
- 1014 1200 BAUD CLOCK
- 1014 1800 BAUD CLOCK
- 1014 2400 BAUD CLOCK
- 1014 4800 BAUD CLOCK
- 1014 9600 BAUD CLOCK

- 1010 OUTPUT DATA BIT 0
- 1010 OUTPUT DATA BIT 1
- 1010 OUTPUT DATA BIT 2
- 1010 OUTPUT DATA BIT 3
- 1010 OUTPUT DATA BIT 4
- 1010 OUTPUT DATA BIT 5
- 1010 OUTPUT DATA BIT 6
- 1010 OUTPUT DATA BIT 7
- 1012 DATA OUT
- 1014 2400 BAUD CLOCK

- 1015 WORD LENGTH SELECT BIT 1
- 1015 WORD LENGTH SELECT BIT 2
- 1015 STOP BIT SELECT
- 1015 PARITY INHIBIT
- 1015 ODD/EVEN PARITY SELECT

- 1015 SELECTED BAUD CLOCK
- 1012 DATA IN
- 1016 GATED RCVD DATA (JUMPERED)
- NOT USED
- 1011 MASTER RESET

- EXT RECEIVED DATA EQUIP
- GROUND
- CROJ

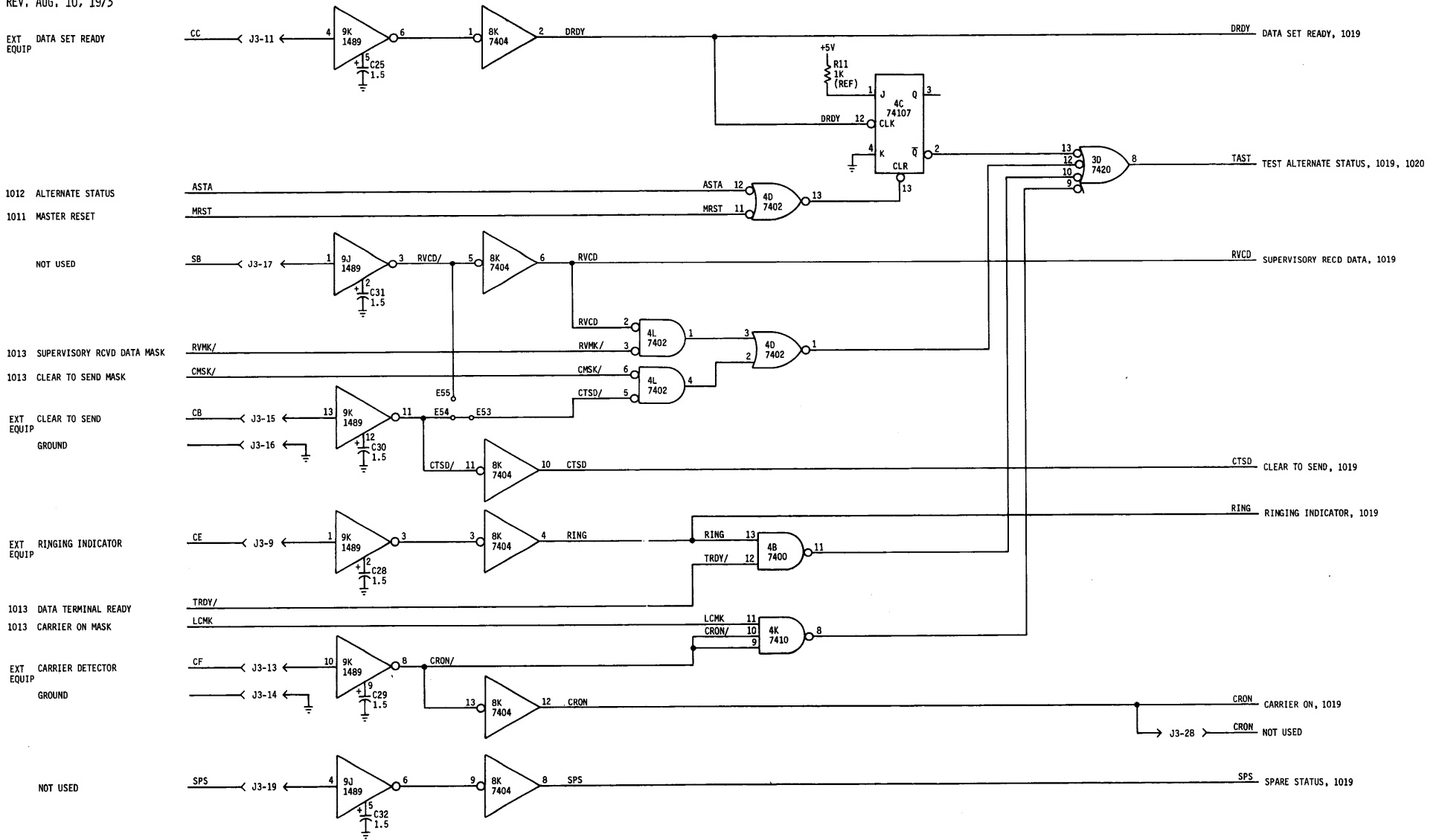


REV. AUG. 10, 1973
LD 1010
CENTRAL PROCESSING UNIT

RECEIVER/TRANSMITTER CIRCUIT

LOCAL/REMOTE SINGLE CHANNEL CONTROLLER
1C16

TEST ALTERNATE STATUS LOGIC



1011 ACKNOWLEDGE

SELECT IN FROM A52 OF NEXT LOWER NUMBERED JACK (SELO/)

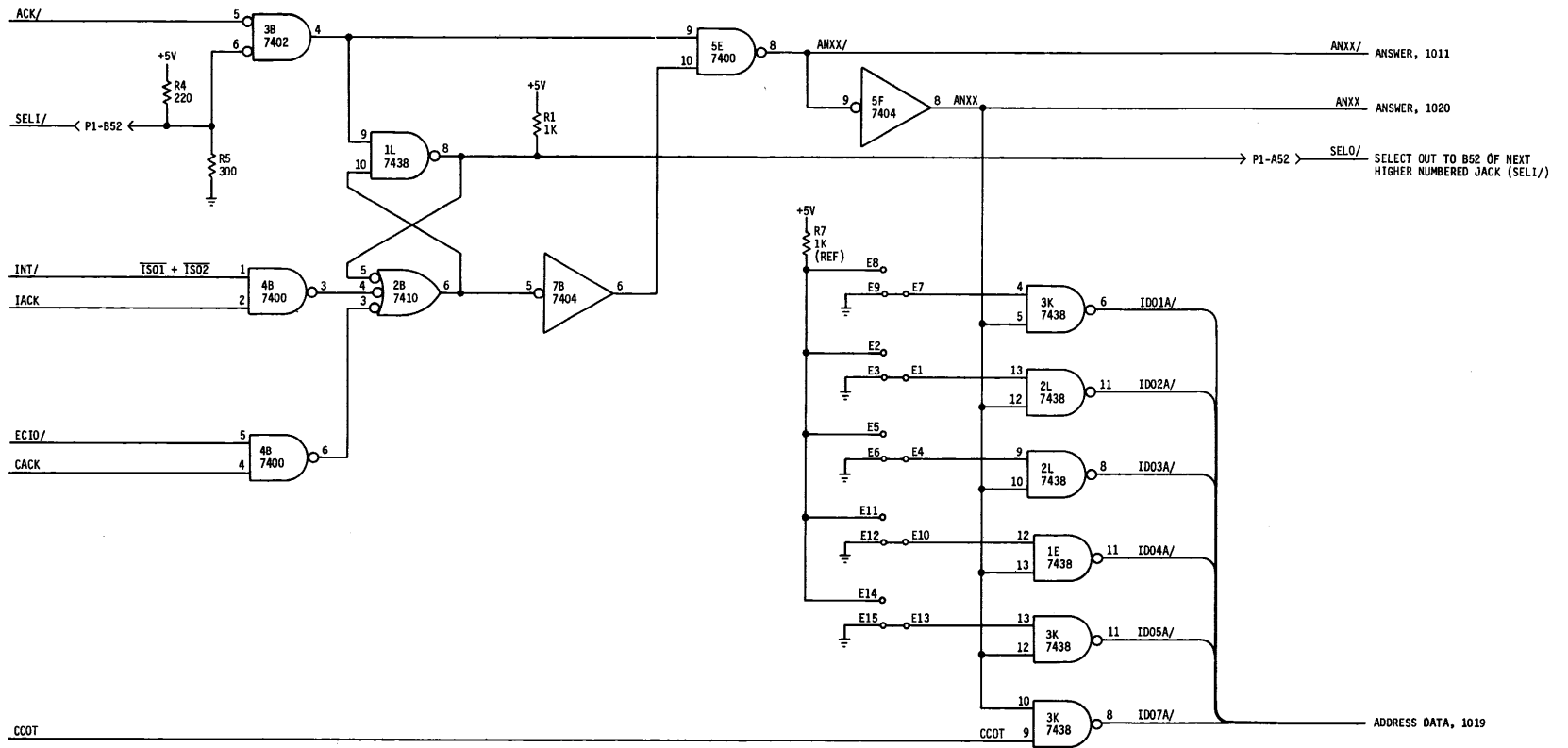
1020 NOT INTERRUPT

1011 INTERRUPT ACKNOWLEDGE

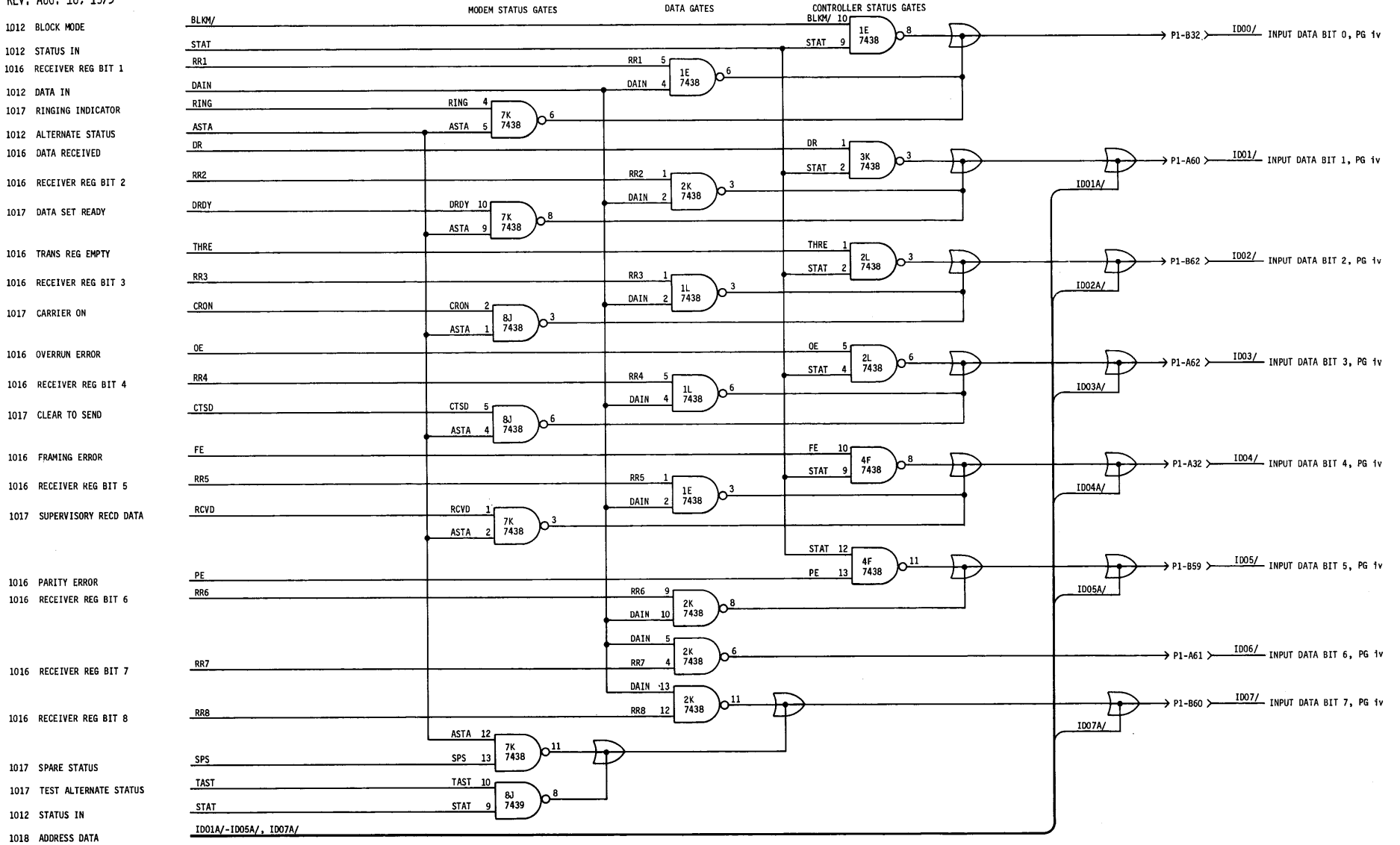
1020 CONCURRENT I/O REQUEST

1011 CONCURRENT ACKNOWLEDGE

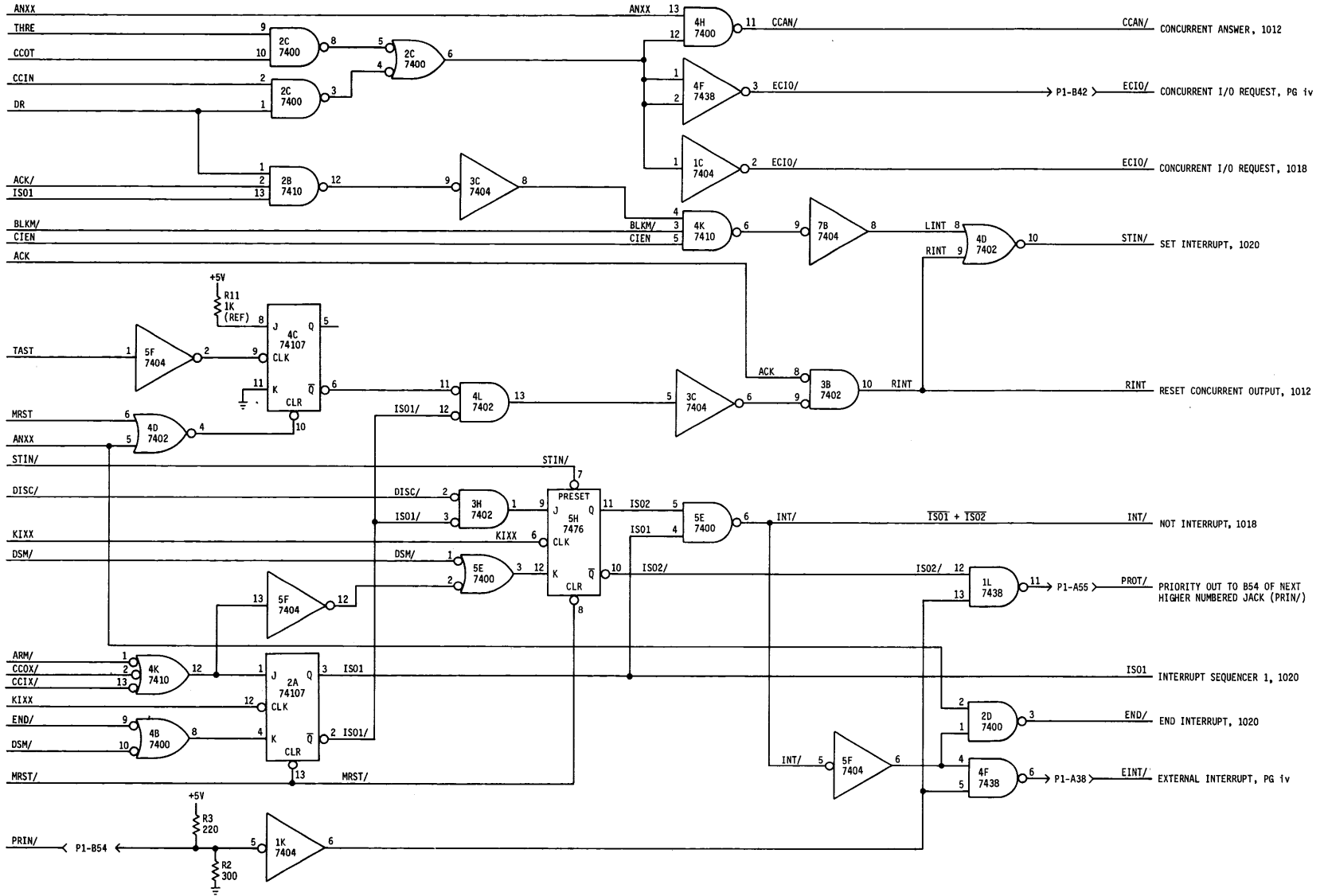
1012 CONCURRENT OUTPUT



COMPUTER INPUT DATA GATING



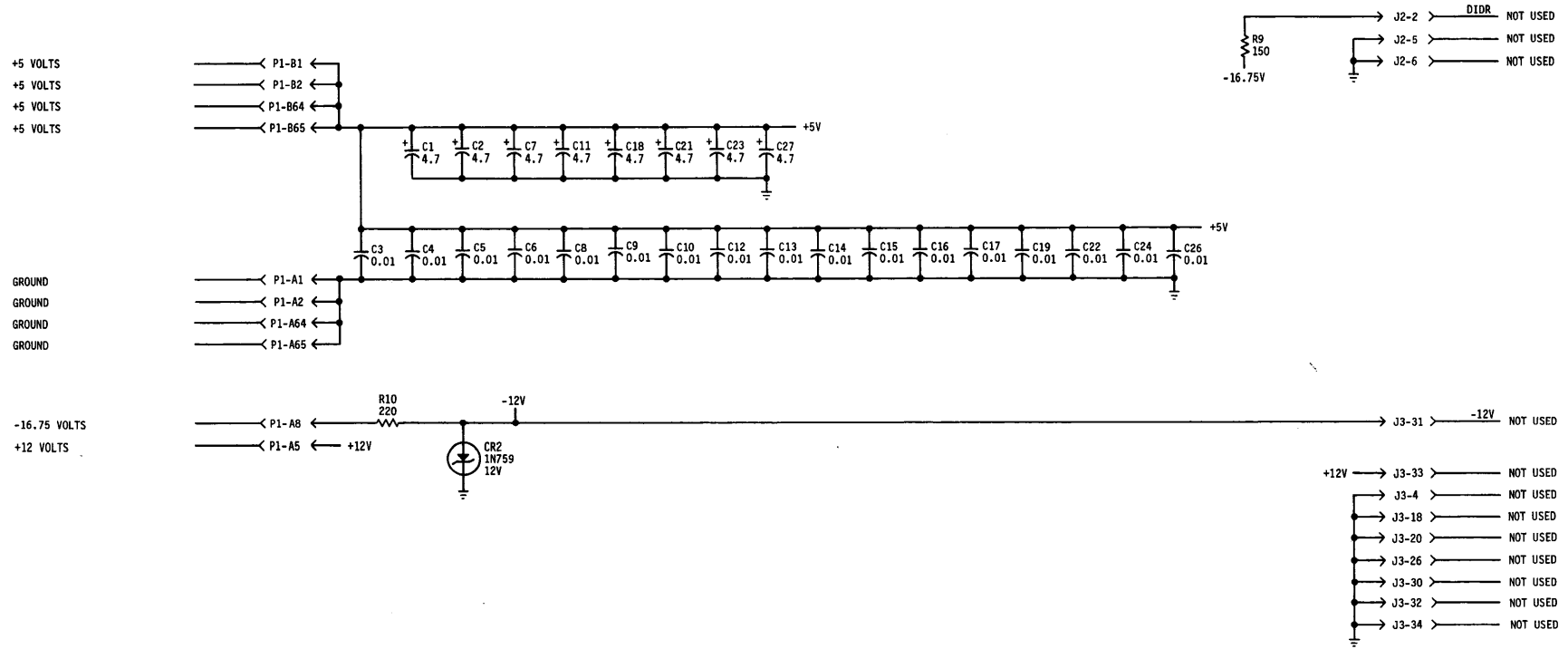
1018 ANSWER
 1016 TRANS REG EMPTY
 1012 CONCURRENT OUTPUT
 1012 CONCURRENT INPUT
 1016 DATA RECEIVED
 1011 ACKNOWLEDGE
 1020 INTERRUPT SEQUENCER 1
 1012 BLOCK MODE
 1013 CHARACTER INTERRUPT ENABLE
 1011 ACKNOWLEDGE
 1017 TEST ALTERNATE STATUS
 1011 MASTER RESET
 1018 ANSWER
 1020 SET INTERRUPT
 1010 CONCURRENT DISCONNECT
 1011 I/O MODE CLOCK
 1010 DISARM INTERRUPT
 1010 ARM INTERRUPT
 1010 CONCURRENT OUTPUT
 1010 CONCURRENT INPUT
 1011 I/O MODE CLOCK
 1020 END INTERRUPT
 1010 DISARM INTERRUPT
 1011 MASTER RESET

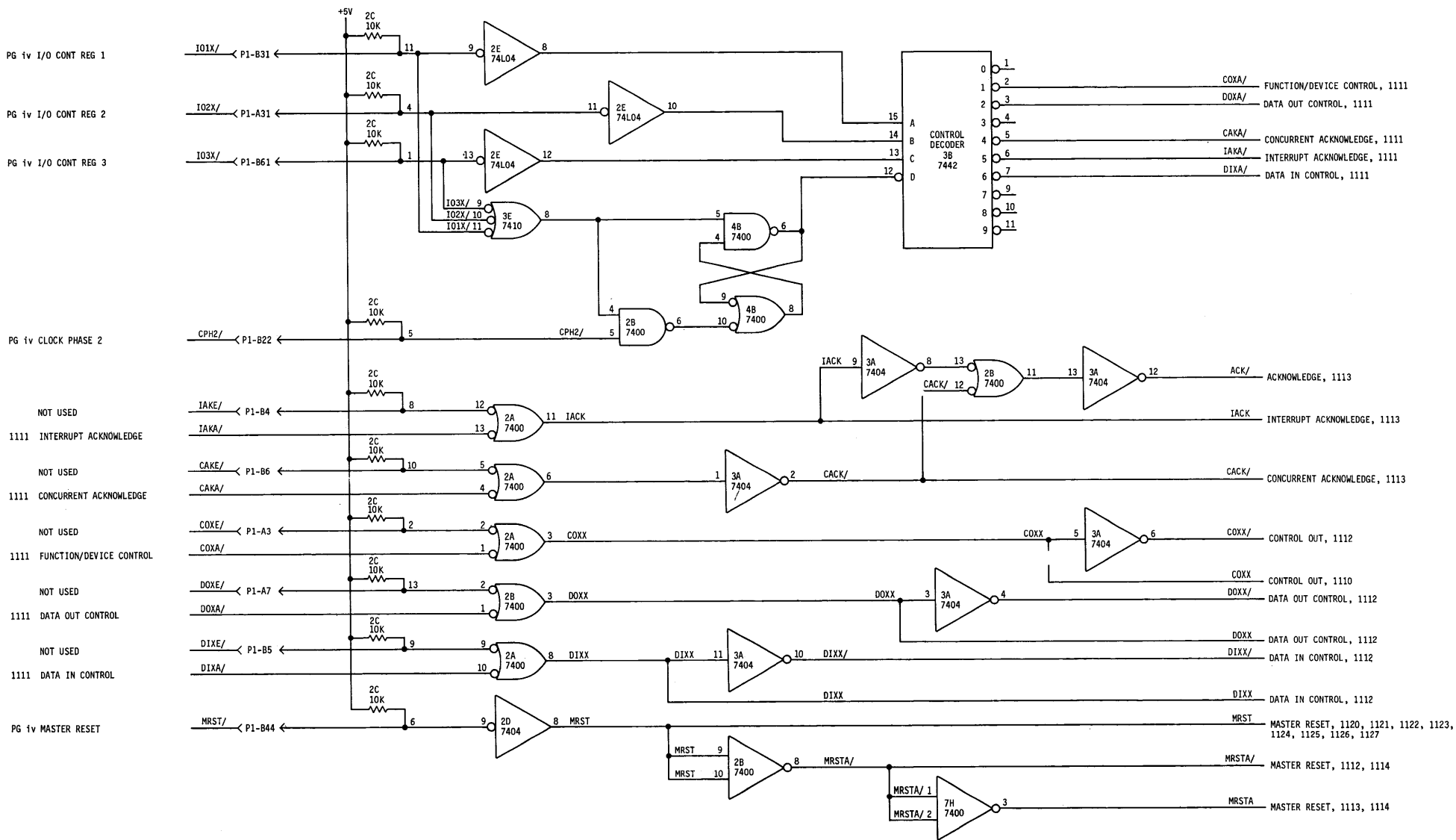


REV. AUG. 10, 1973
 LD 1010
 CENTRAL PROCESSING UNIT

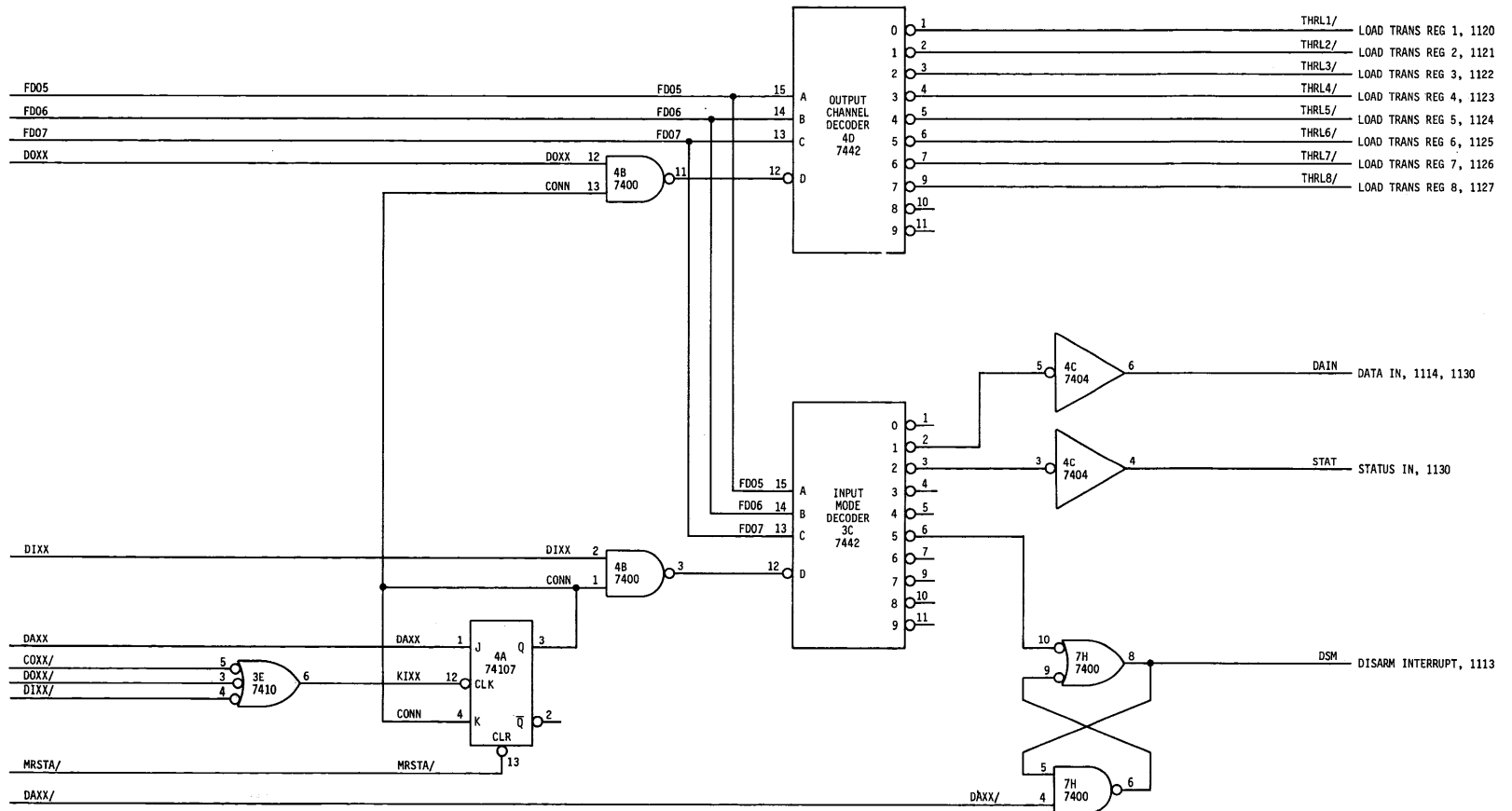
REQUEST CONTROL LOGIC

LOCAL/REMOTE SINGLE CHANNEL CONTROLLER
 1020





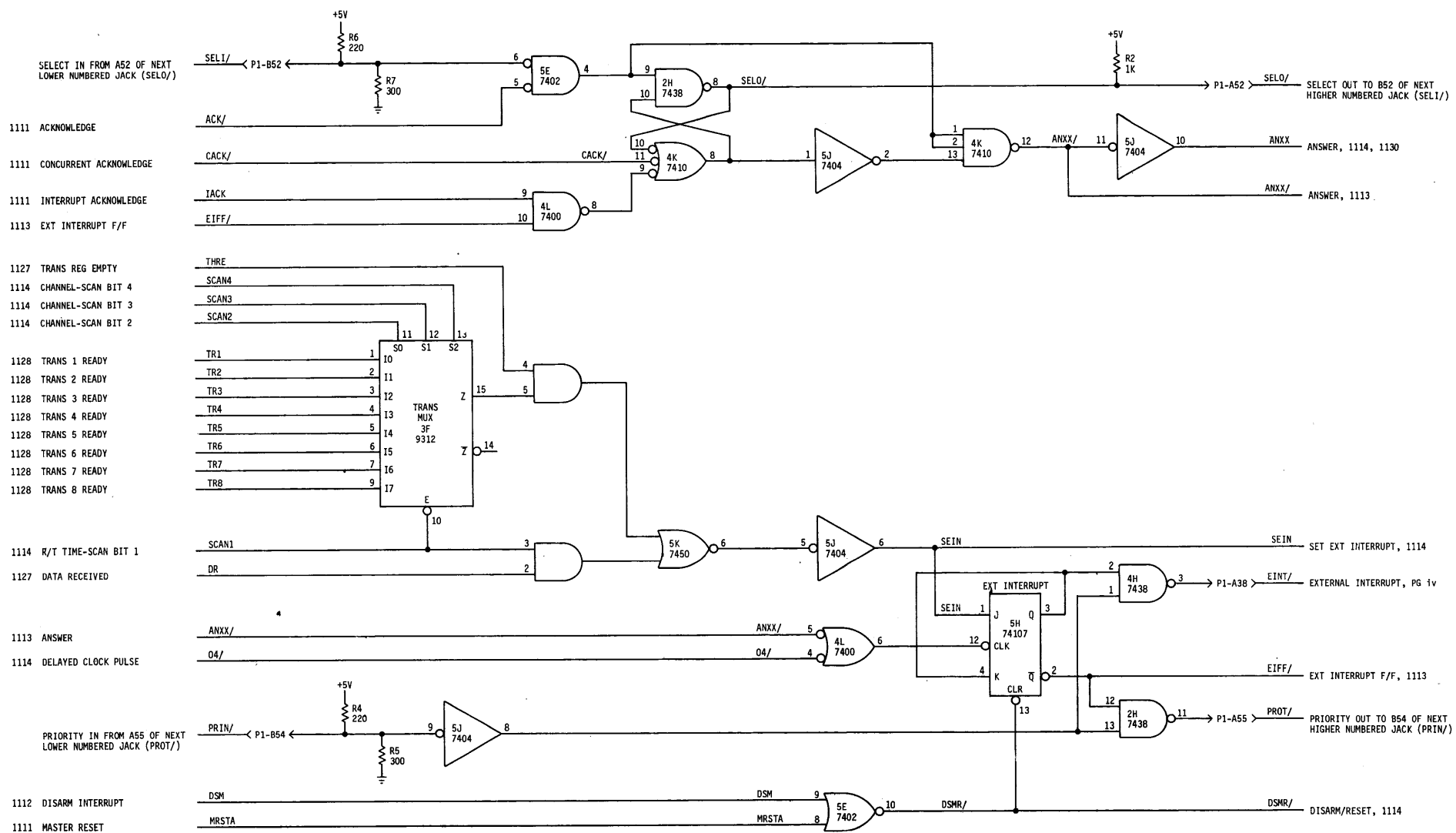
1110 FUNCTION BIT 5
 1110 FUNCTION BIT 6
 1110 FUNCTION BIT 7
 1111 DATA OUT CONTROL



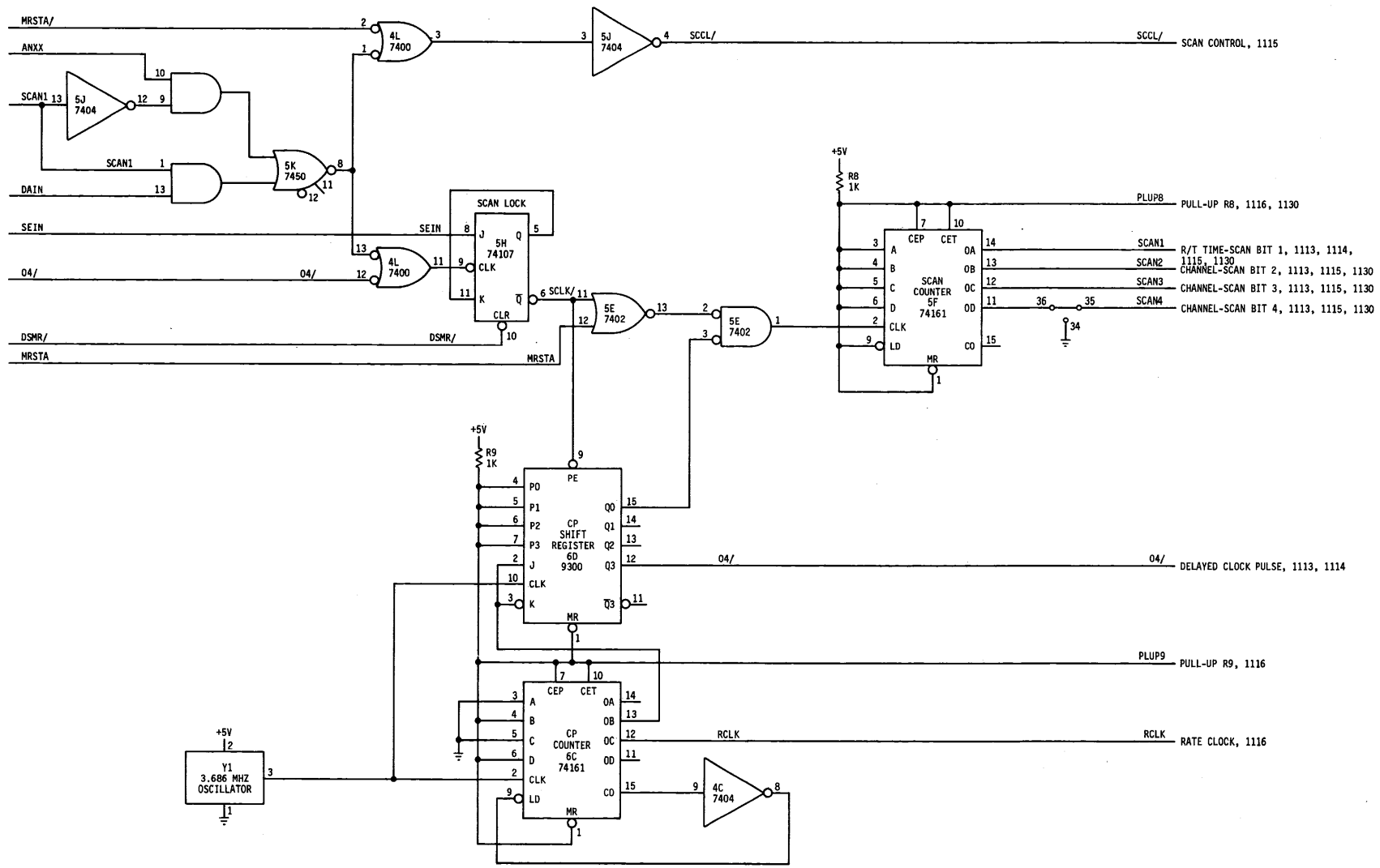
1111 DATA IN CONTROL

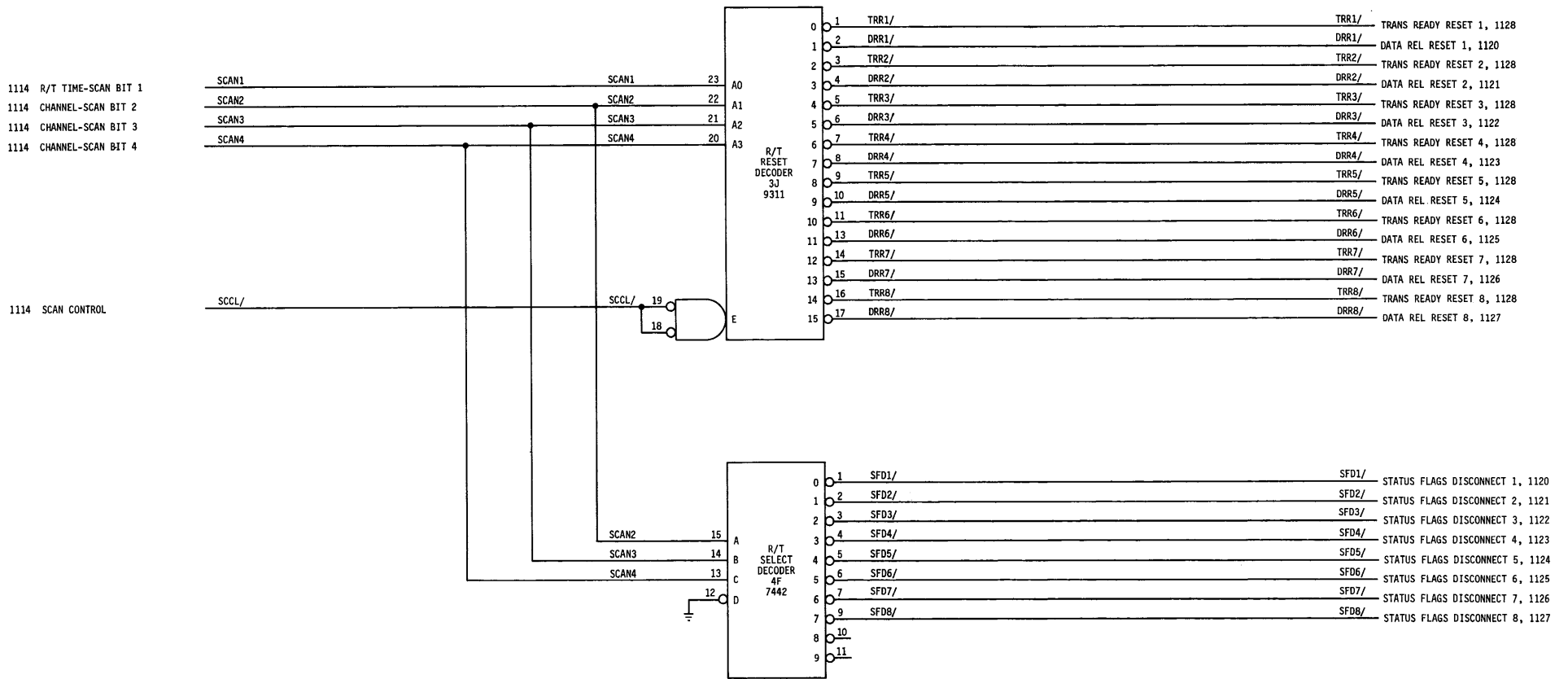
1110 DEVICE ADDRESS DETECT
 .111 CONTROL OUT
 1111 DATA OUT CONTROL
 1111 DATA IN CONTROL

1111 MASTER RESET
 1110 DEVICE ADDRESS DETECT



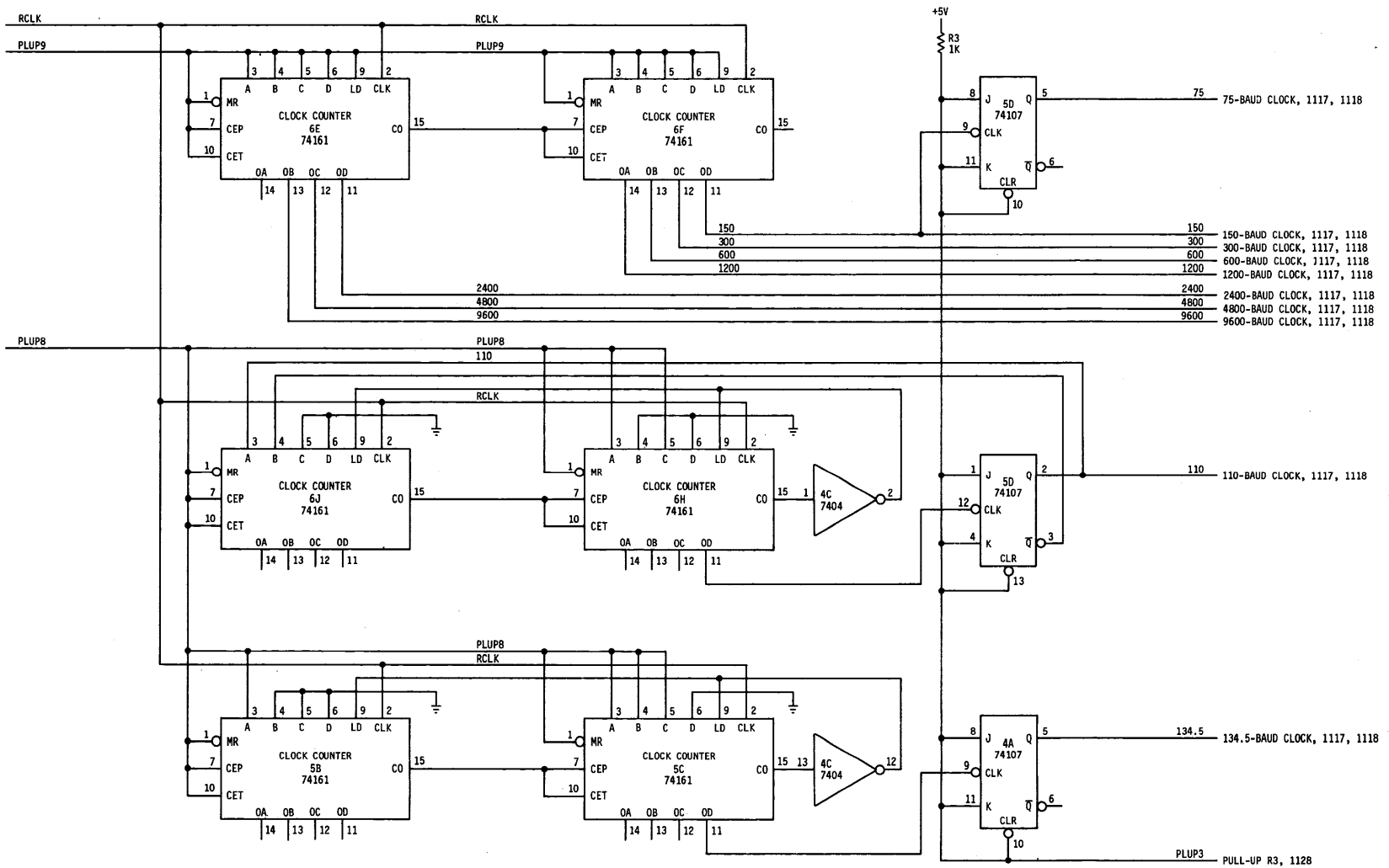
1111 MASTER RESET
 1113 ANSWER
 1114 RIT TIME-SCAN BIT 1
 1112 DATA IN
 1113 SET EXT INTERRUPT
 1114 DELAYED CLOCK PULSE
 1113 DISARM/RESET
 1111 MASTER RESET



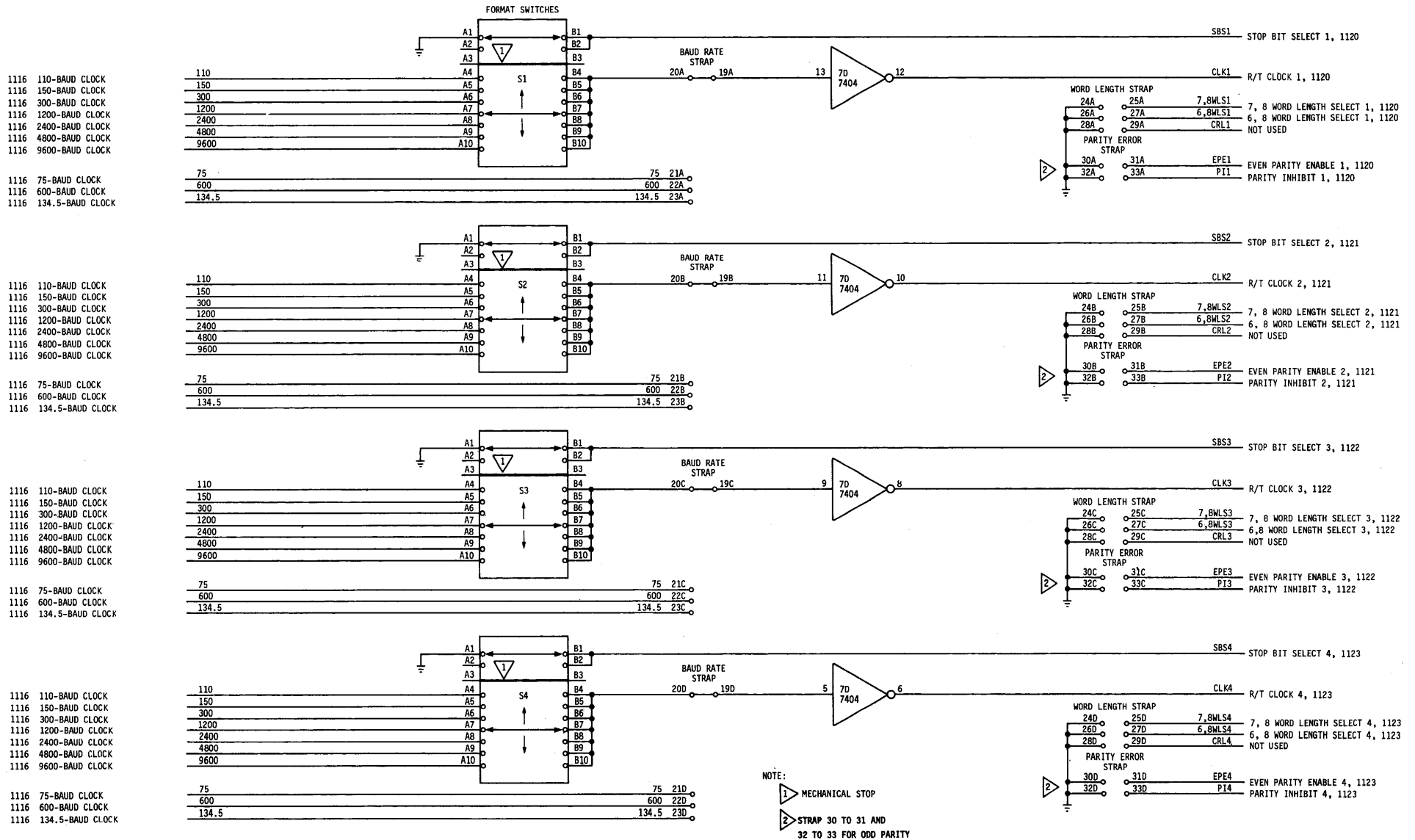


1114 RATE CLOCK
1114 PULL-UP R9

1114 PULL-UP R8



EXTERNAL DEVICE BAUD RATE SELECT CHANNELS 1-4



1116 110-BAUD CLOCK
1116 150-BAUD CLOCK
1116 300-BAUD CLOCK
1116 1200-BAUD CLOCK
1116 2400-BAUD CLOCK
1116 4800-BAUD CLOCK
1116 9600-BAUD CLOCK

1116 75-BAUD CLOCK
1116 600-BAUD CLOCK
1116 134.5-BAUD CLOCK

1116 110-BAUD CLOCK
1116 150-BAUD CLOCK
1116 300-BAUD CLOCK
1116 1200-BAUD CLOCK
1116 2400-BAUD CLOCK
1116 4800-BAUD CLOCK
1116 9600-BAUD CLOCK

1116 75-BAUD CLOCK
1116 600-BAUD CLOCK
1116 134.5-BAUD CLOCK

1116 110-BAUD CLOCK
1116 150-BAUD CLOCK
1116 300-BAUD CLOCK
1116 1200-BAUD CLOCK
1116 2400-BAUD CLOCK
1116 4800-BAUD CLOCK
1116 9600-BAUD CLOCK

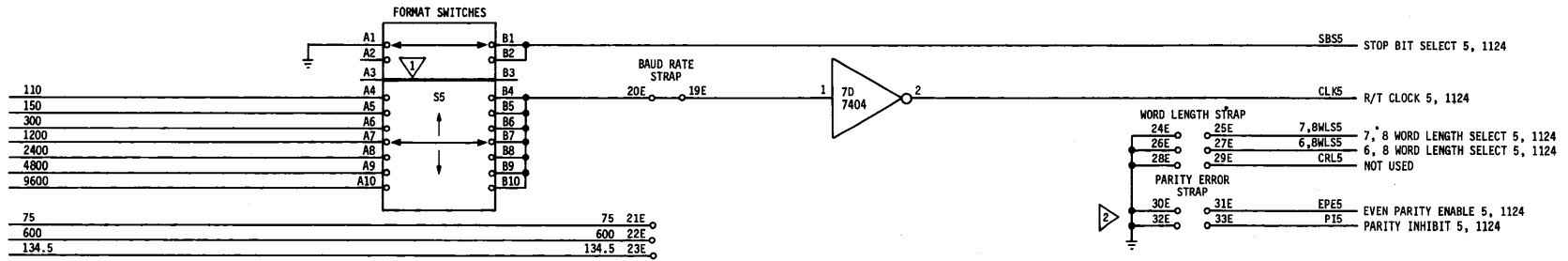
1116 75-BAUD CLOCK
1116 600-BAUD CLOCK
1116 134.5-BAUD CLOCK

1116 110-BAUD CLOCK
1116 150-BAUD CLOCK
1116 300-BAUD CLOCK
1116 1200-BAUD CLOCK
1116 2400-BAUD CLOCK
1116 4800-BAUD CLOCK
1116 9600-BAUD CLOCK

1116 75-BAUD CLOCK
1116 600-BAUD CLOCK
1116 134.5-BAUD CLOCK

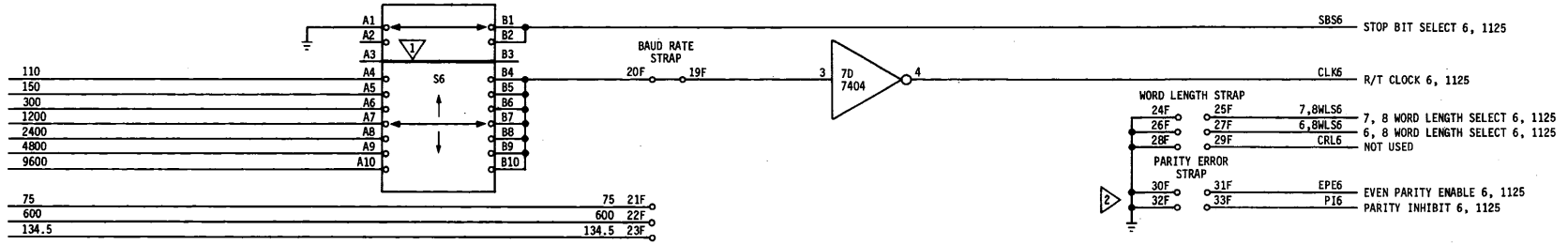
- 1116 110-BAUD CLOCK
- 1116 150-BAUD CLOCK
- 1116 300-BAUD CLOCK
- 1116 1200-BAUD CLOCK
- 1116 2400-BAUD CLOCK
- 1116 4800-BAUD CLOCK
- 1116 9600-BAUD CLOCK

- 1116 75-BAUD CLOCK
- 1116 600-BAUD CLOCK
- 1116 134.5-BAUD CLOCK



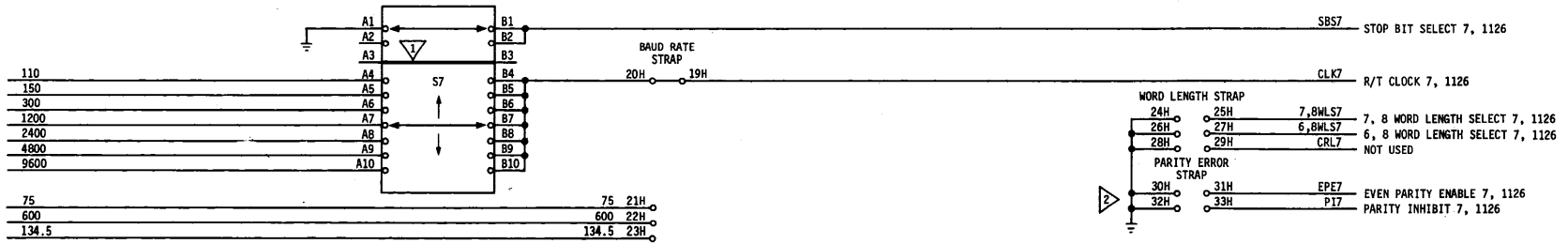
- 1116 110-BAUD CLOCK
- 1116 150-BAUD CLOCK
- 1116 300-BAUD CLOCK
- 1116 1200-BAUD CLOCK
- 1116 2400-BAUD CLOCK
- 1116 4800-BAUD CLOCK
- 1116 9600-BAUD CLOCK

- 1116 75-BAUD CLOCK
- 1116 600-BAUD CLOCK
- 1116 134.5-BAUD CLOCK



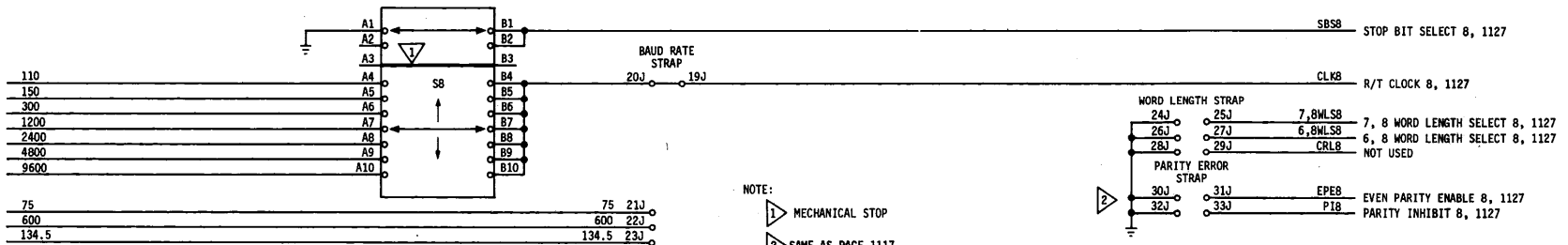
- 1116 110-BAUD CLOCK
- 1116 150-BAUD CLOCK
- 1116 300-BAUD CLOCK
- 1116 1200-BAUD CLOCK
- 1116 2400-BAUD CLOCK
- 1116 4800-BAUD CLOCK
- 1116 9600-BAUD CLOCK

- 1116 75-BAUD CLOCK
- 1116 600-BAUD CLOCK
- 1116 134.5-BAUD CLOCK



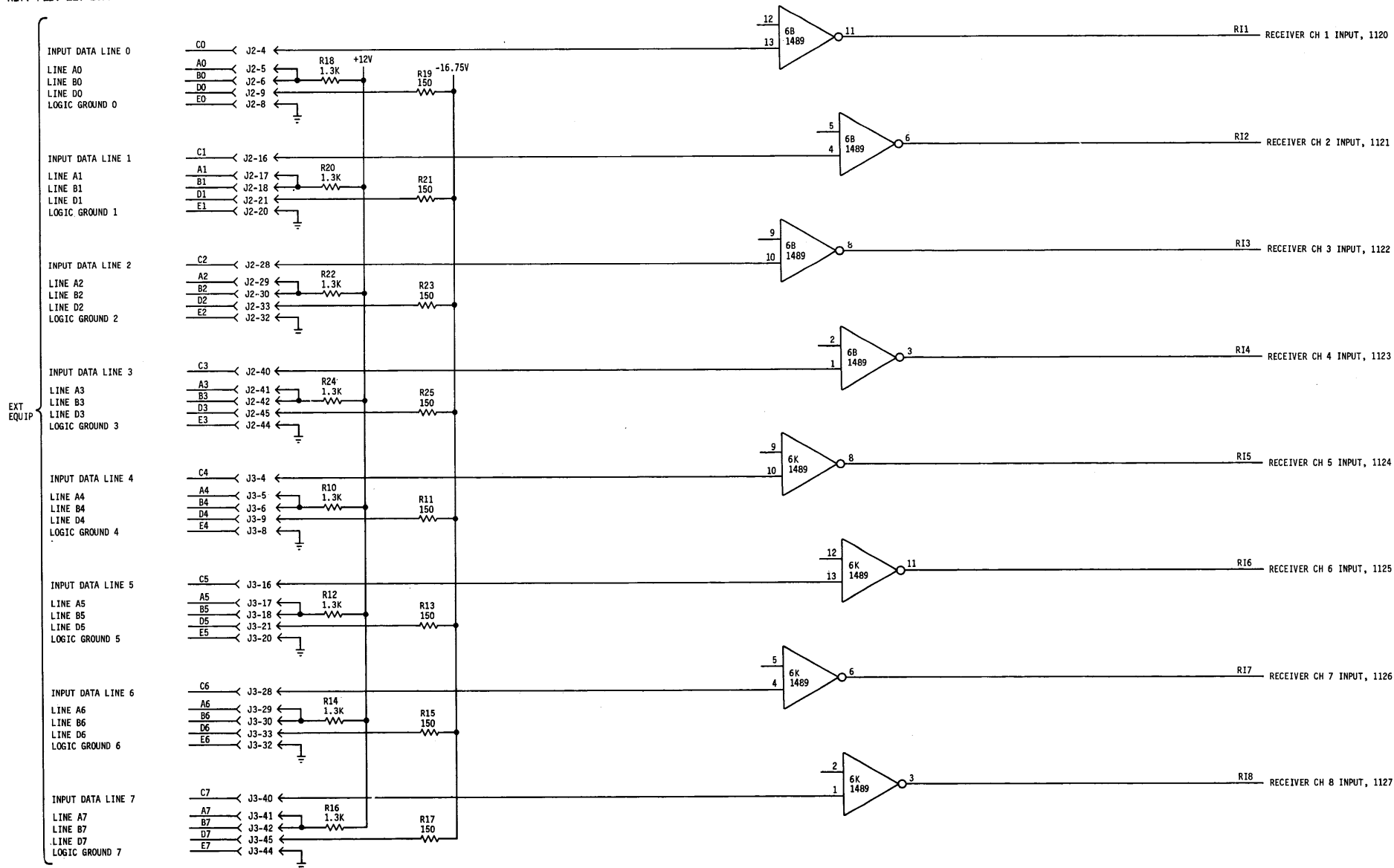
- 1116 110-BAUD CLOCK
- 1116 150-BAUD CLOCK
- 1116 300-BAUD CLOCK
- 1116 1200-BAUD CLOCK
- 1116 2400-BAUD CLOCK
- 1116 4800-BAUD CLOCK
- 1116 9600-BAUD CLOCK

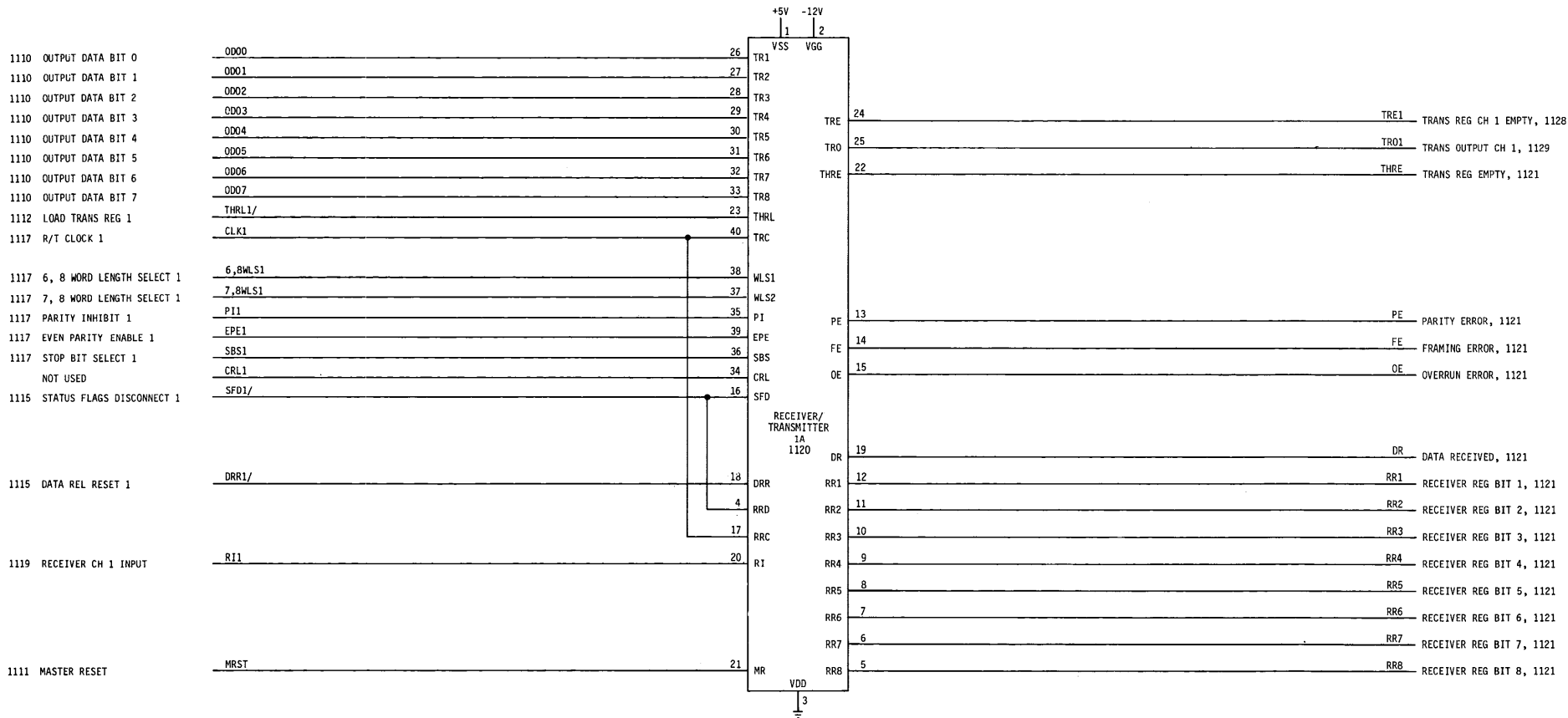
- 1116 75-BAUD CLOCK
- 1116 600-BAUD CLOCK
- 1116 134.5-BAUD CLOCK



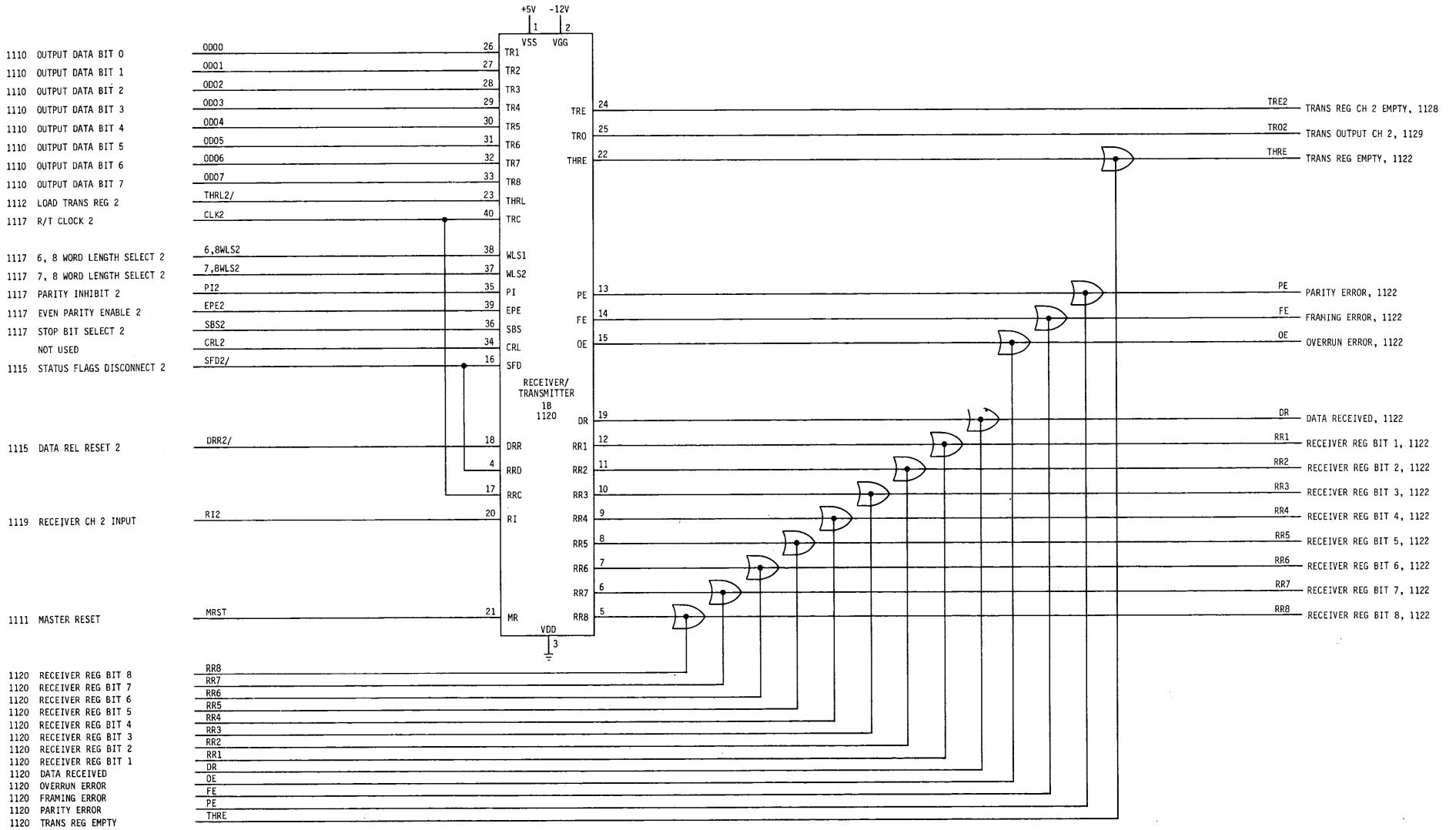
NOTE:
 MECHANICAL STOP
 SAME AS PAGE 1117

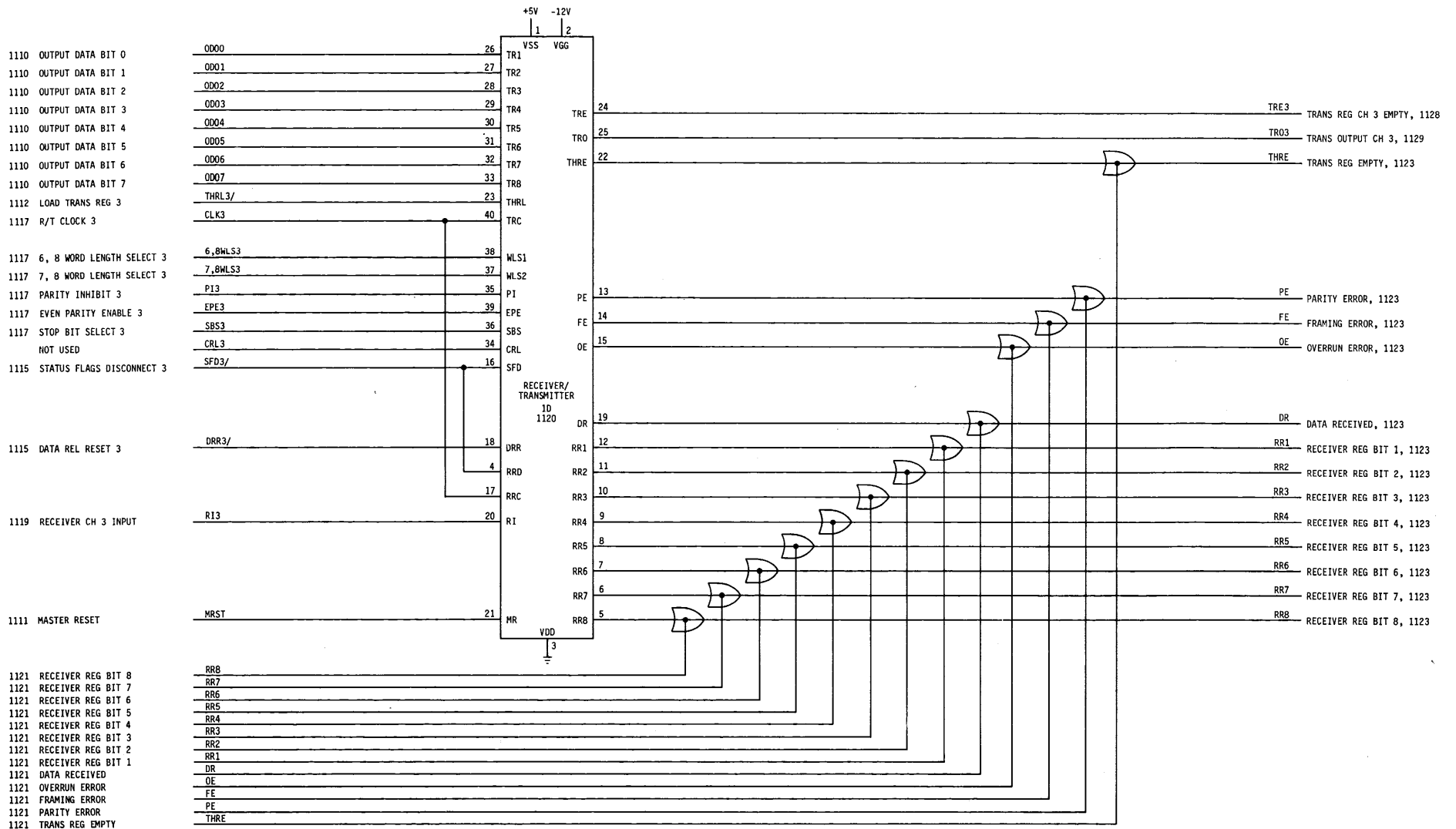
EXTERNAL DEVICE BAUD RATE SELECT CHANNELS 5 - 8

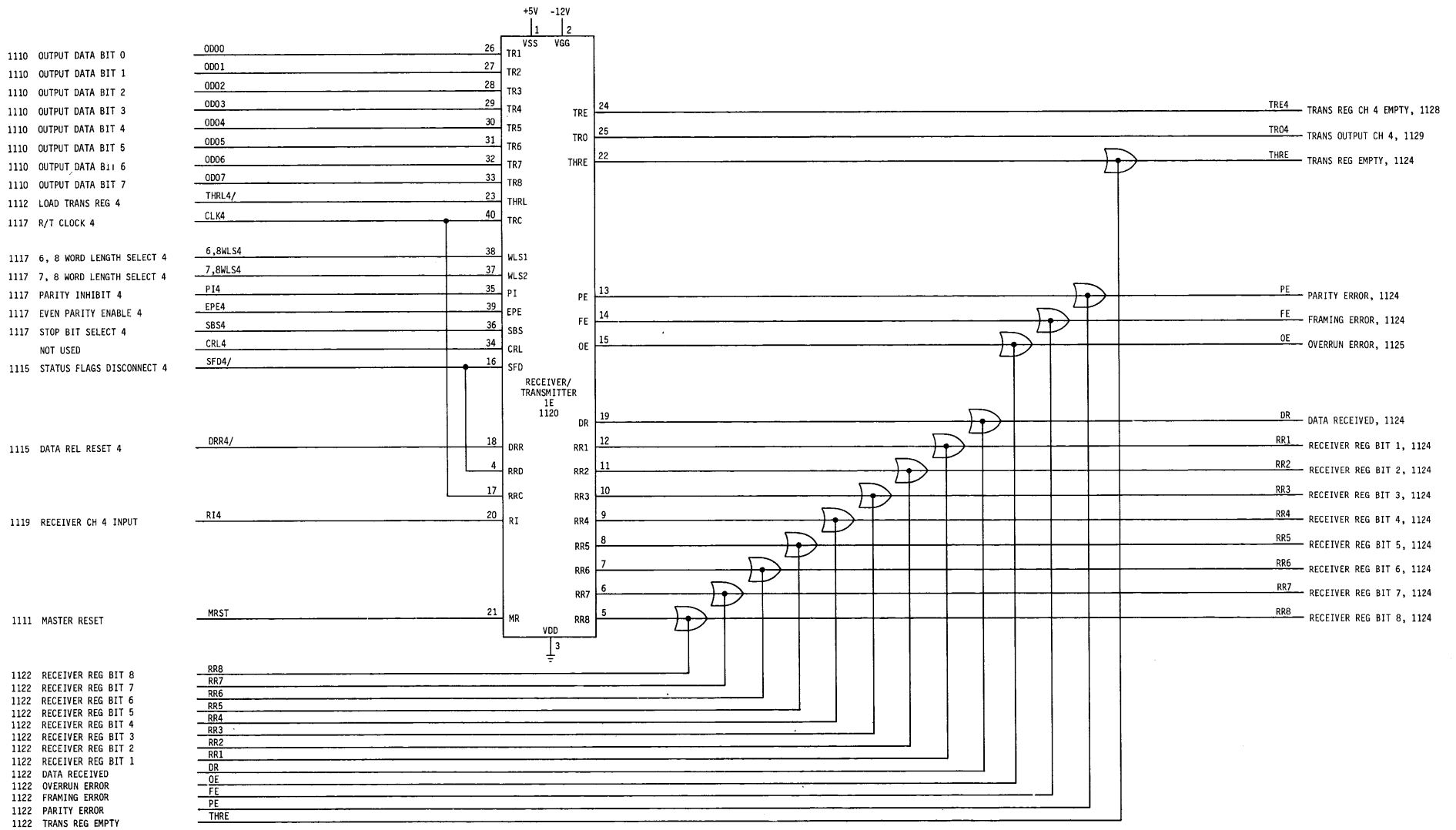


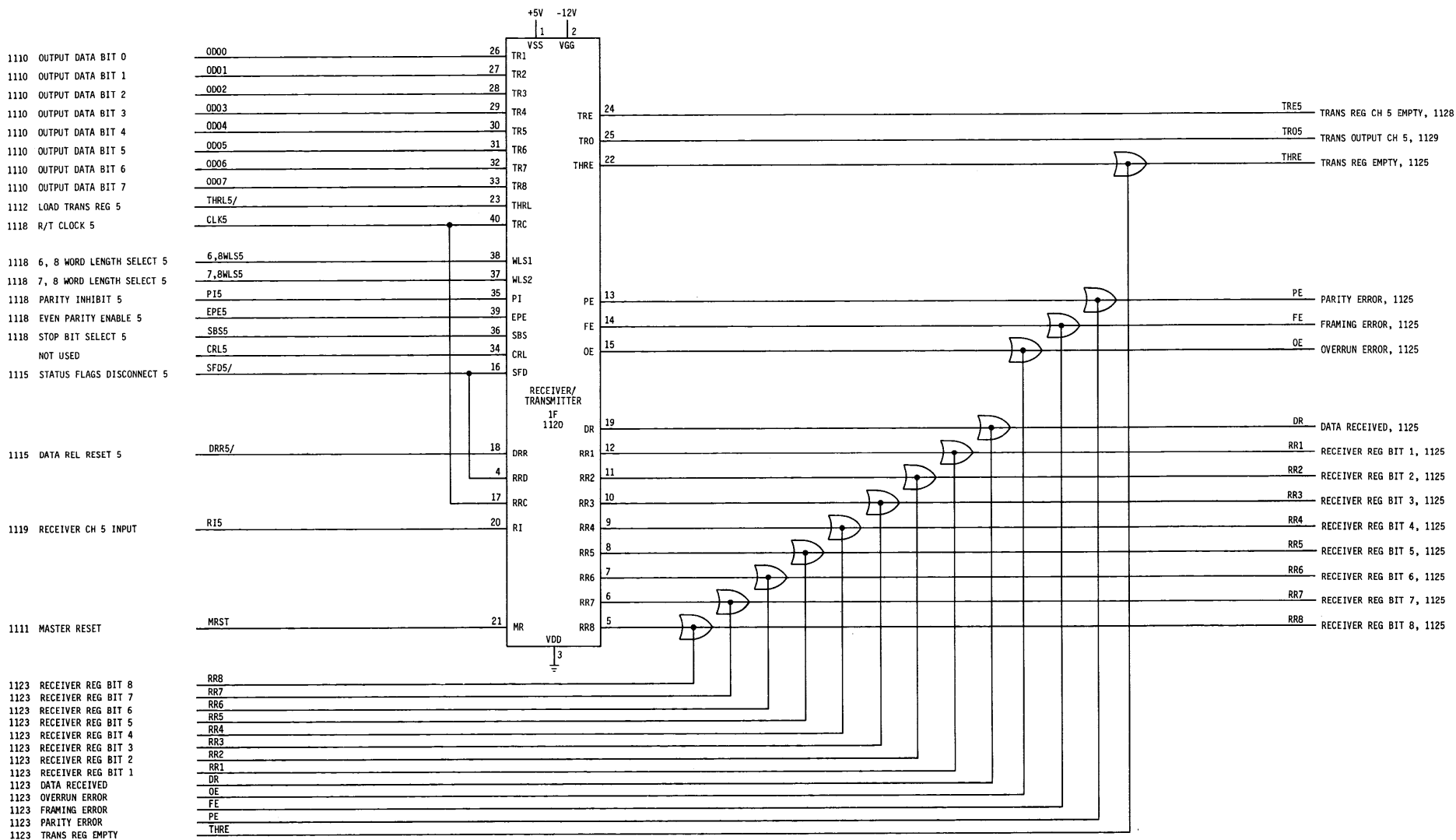


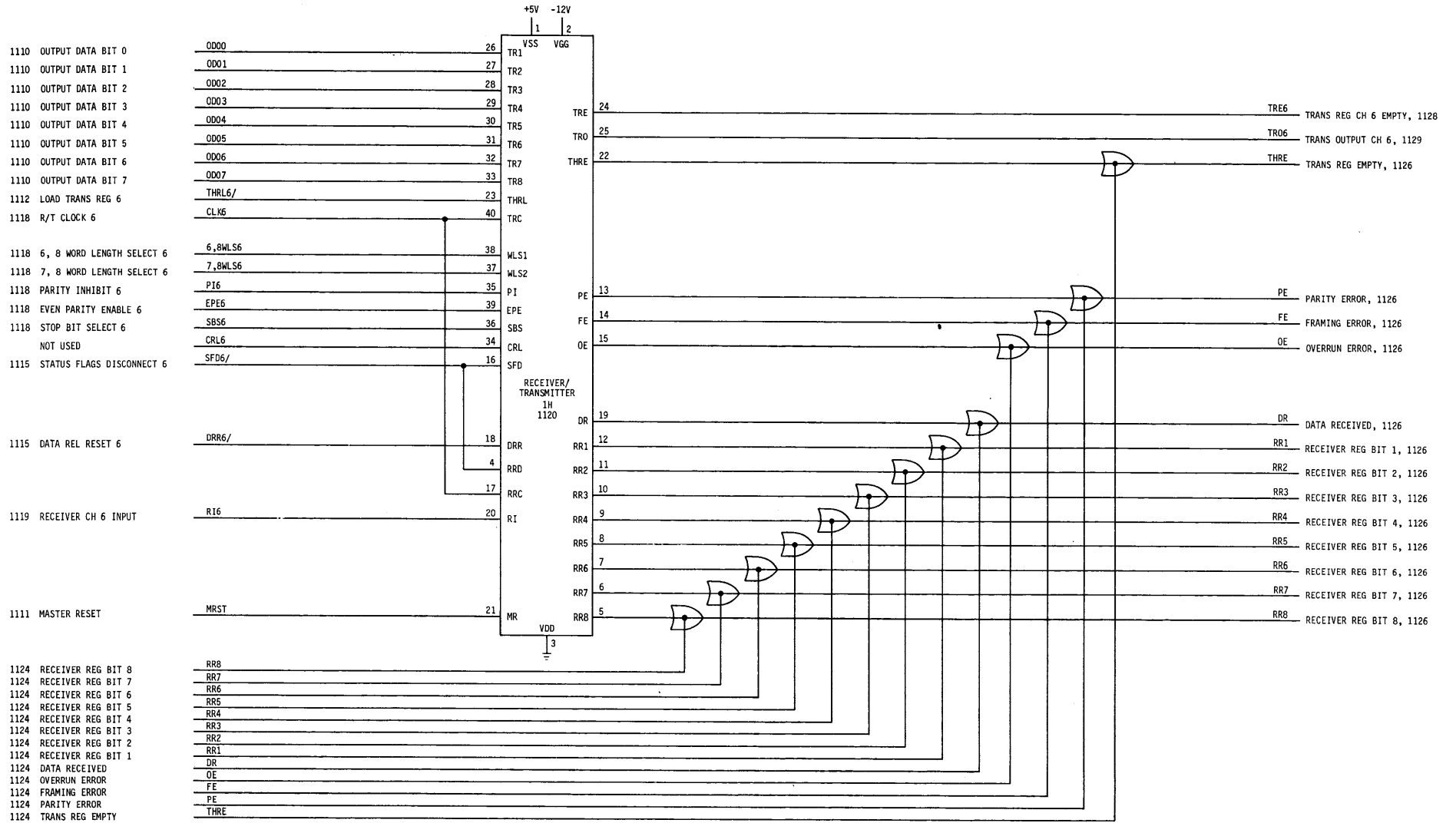
CHANNEL 2 RECEIVER/TRANSMITTER CIRCUIT

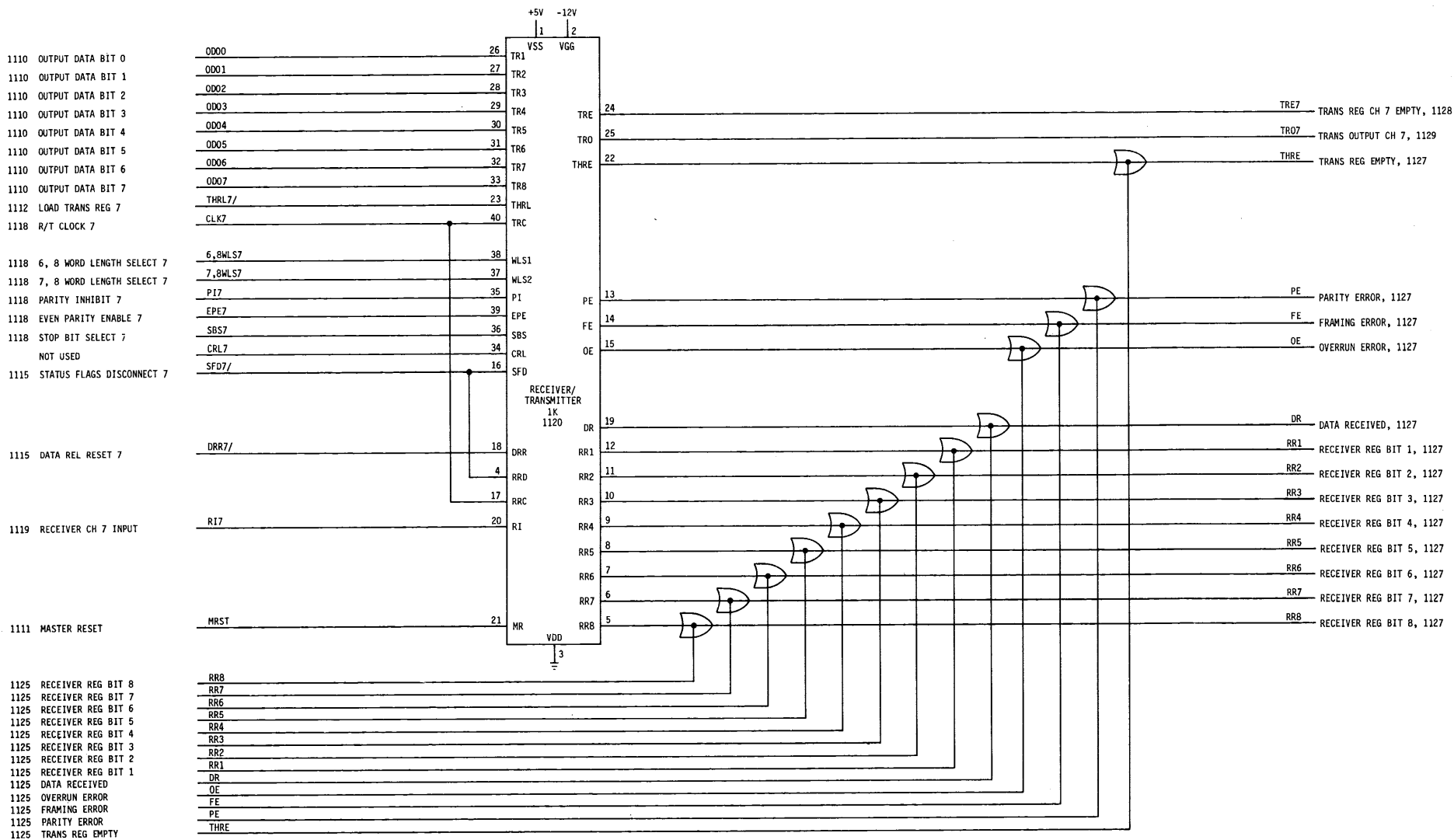




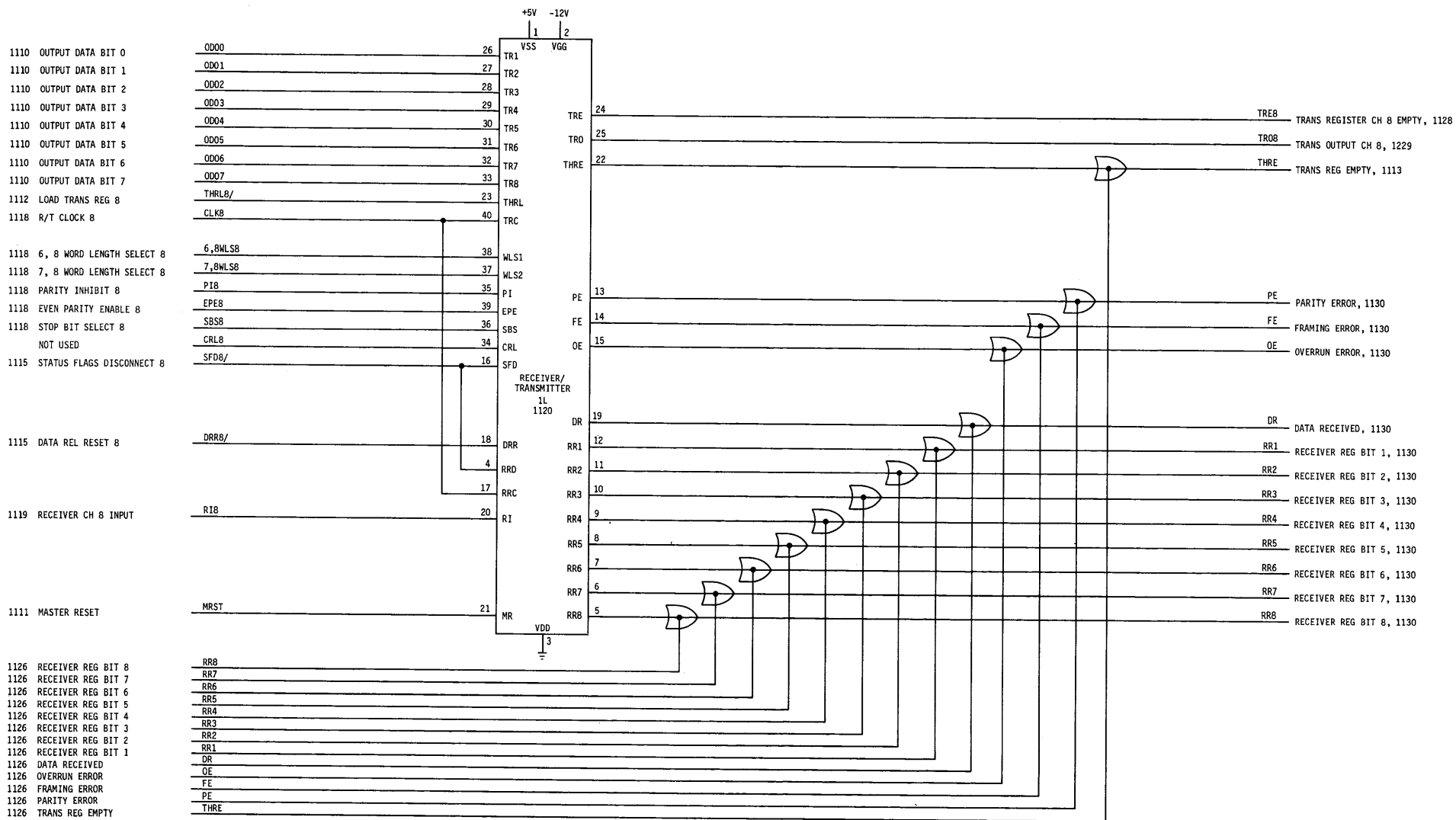




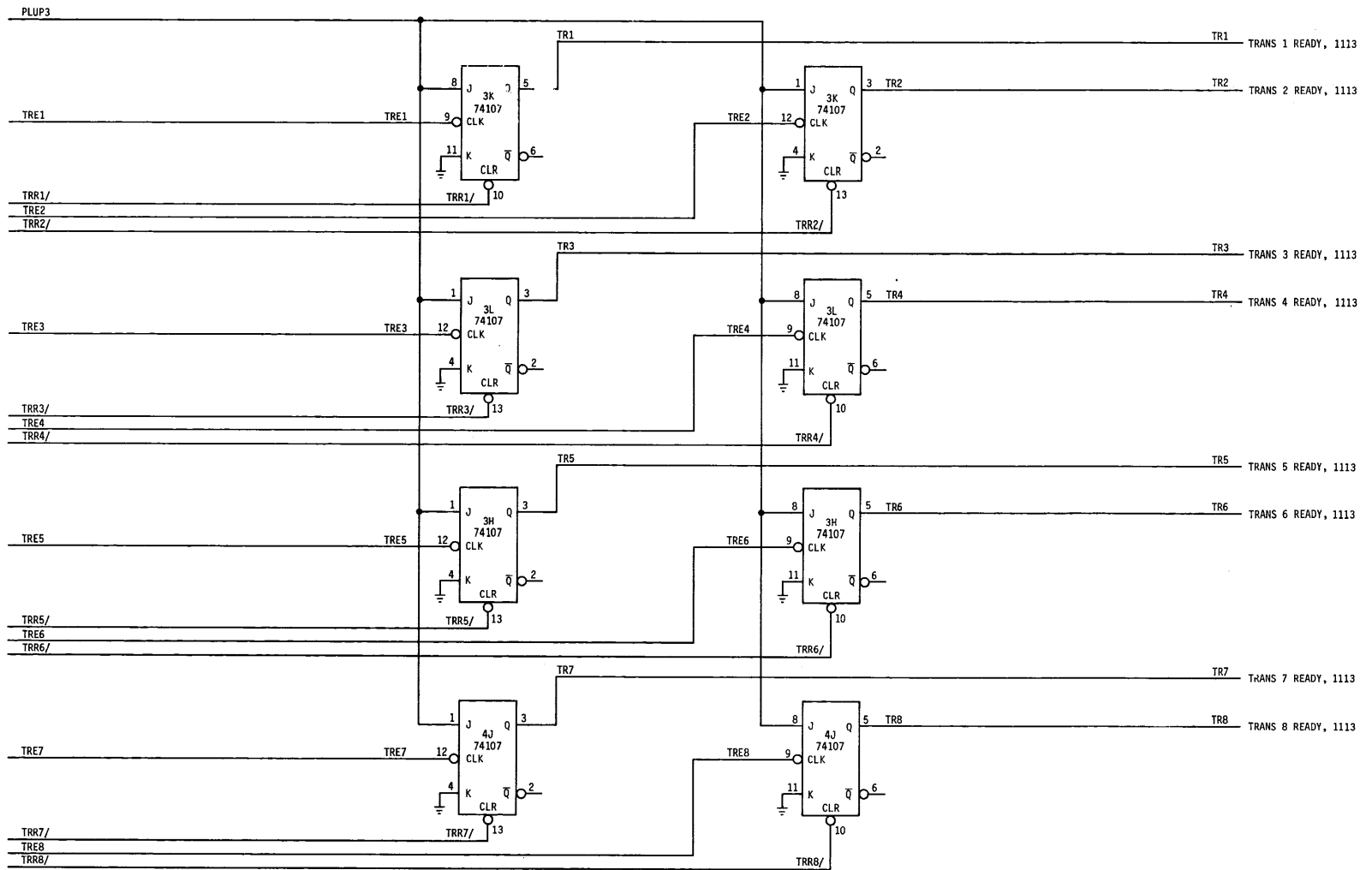




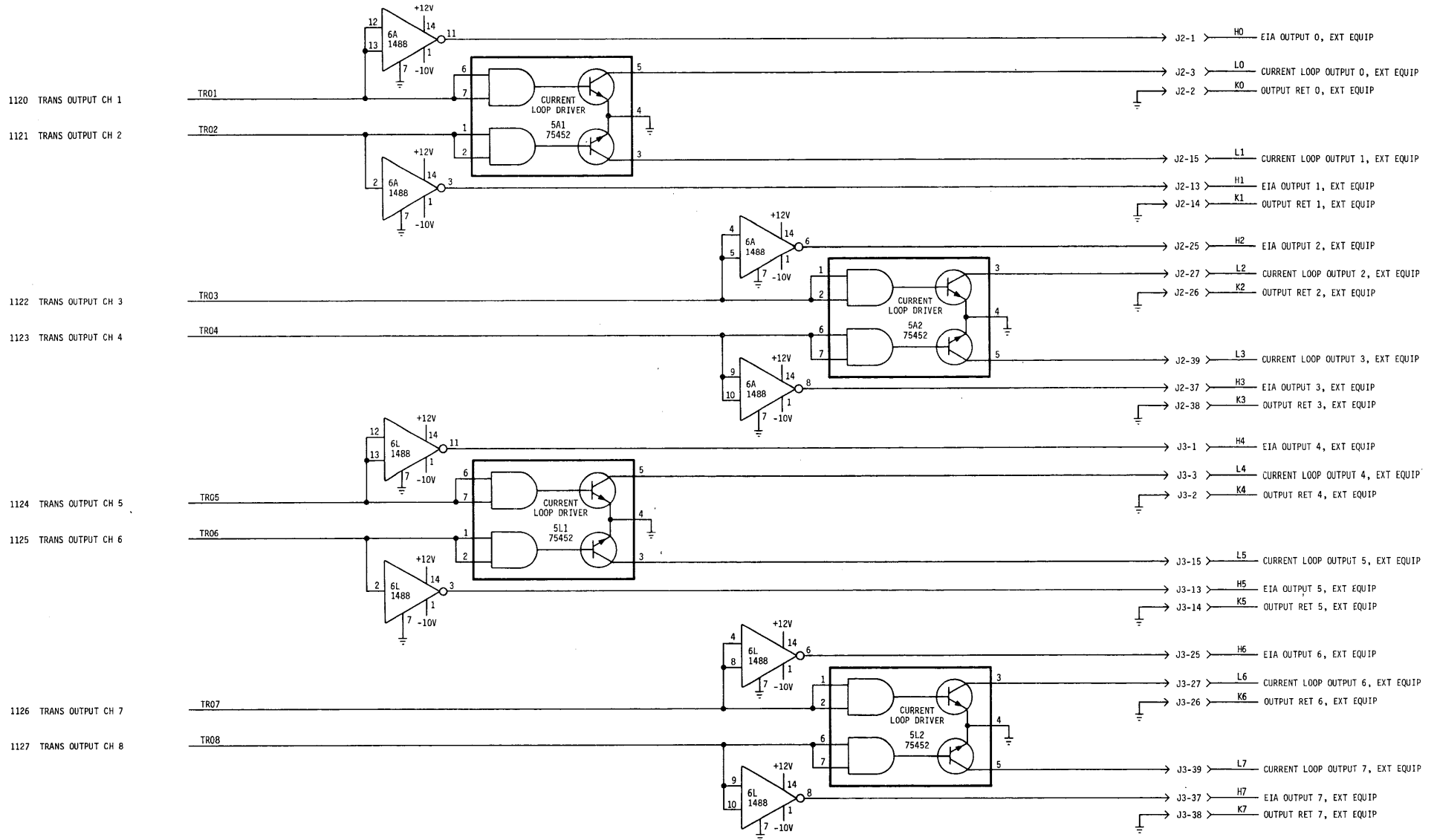
CHANNEL 8 RECEIVER/TRANSMITTER CIRCUIT



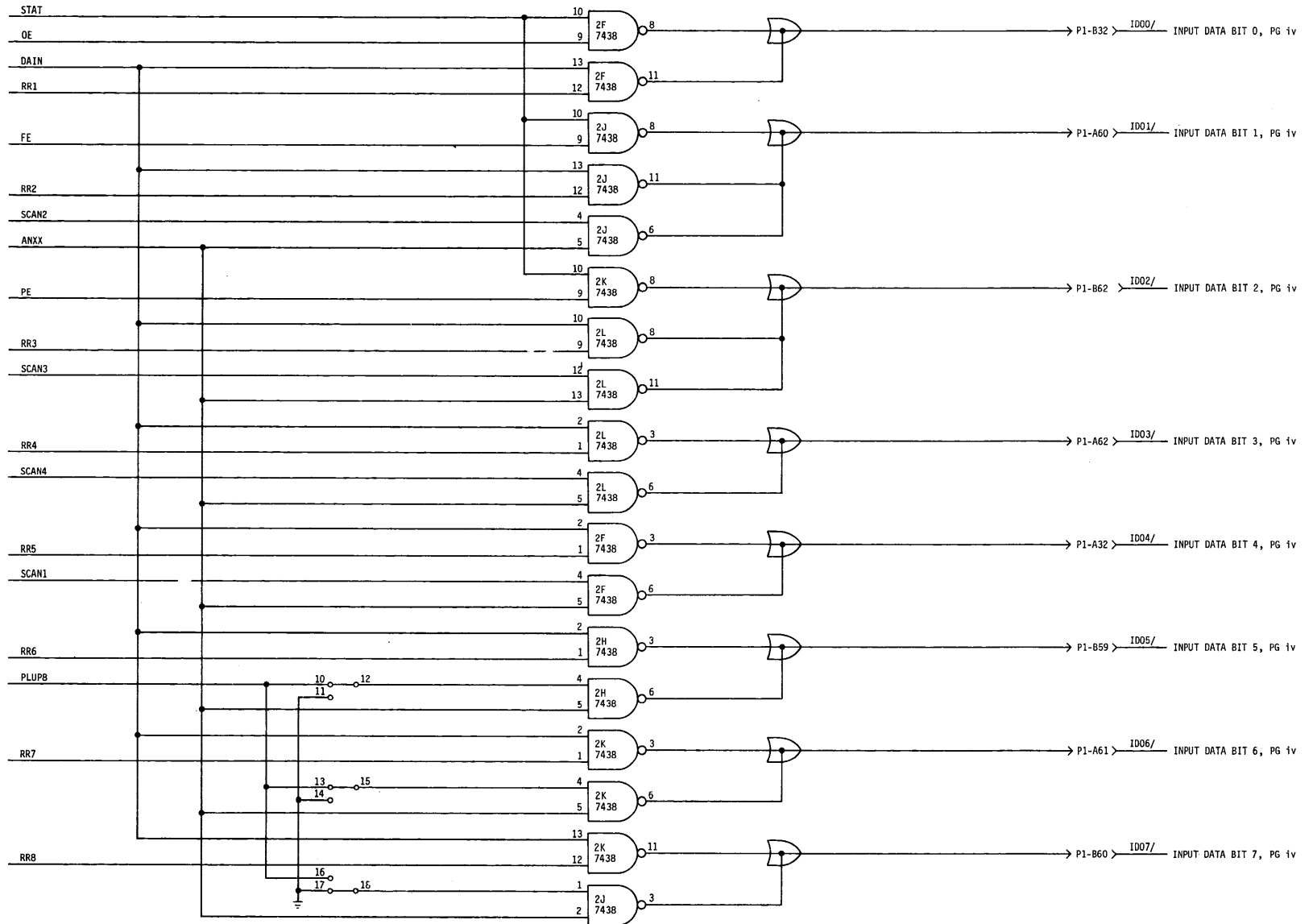
1116 PULL-UP R3
 1120 TRANS REG CH 1 EMPTY
 1115 TRANS READY RESET 1
 1121 TRANS REG CH 2 EMPTY
 1115 TRANS READY RESET 2
 1122 TRANS REG CH 3 EMPTY
 1115 TRANS READY RESET 3
 1123 TRANS REG CH 4 EMPTY
 1115 TRANS READY RESET 4
 1124 TRANS REG CH 5 EMPTY
 1115 TRANS READY RESET 5
 1125 TRANS REG CH 6 EMPTY
 1115 TRANS READY RESET 6
 1126 TRANS REG CH 7 EMPTY
 1115 TRANS READY RESET 7
 1127 TRANS REG CH 8 EMPTY
 1115 TRANS READY RESET 8

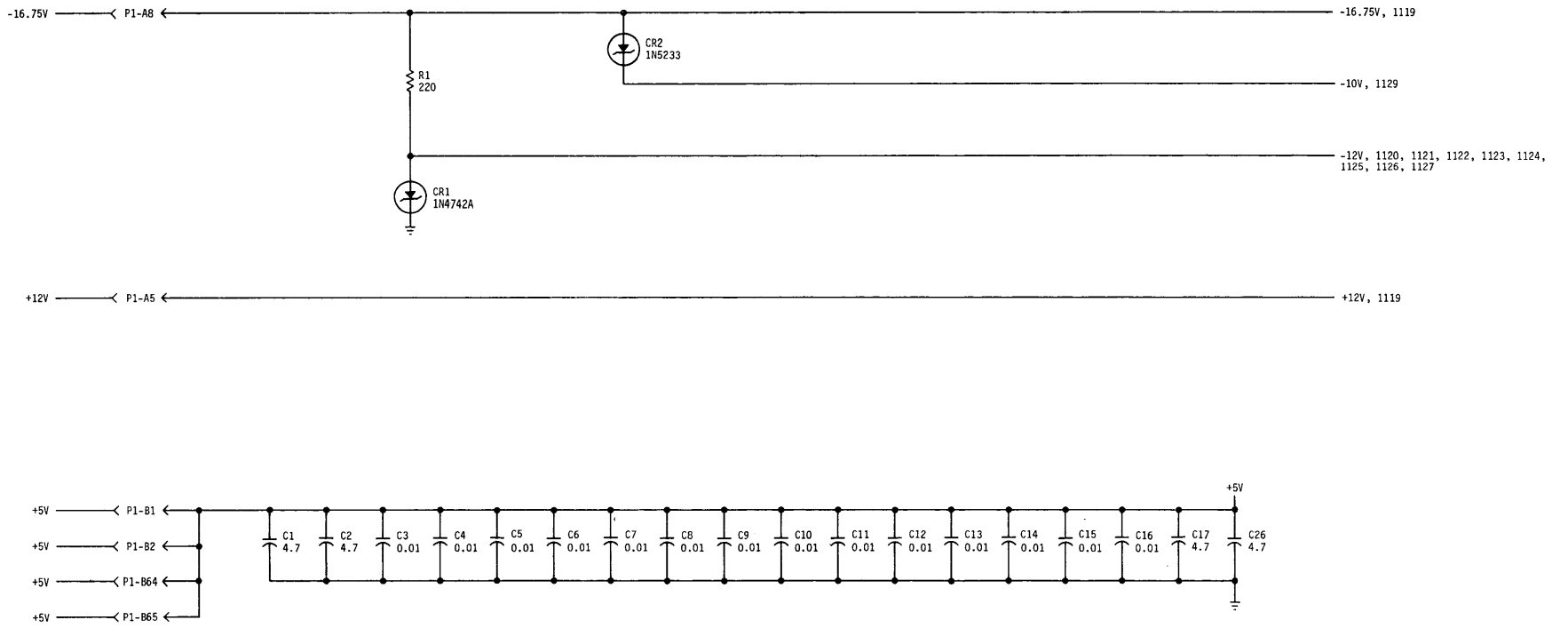


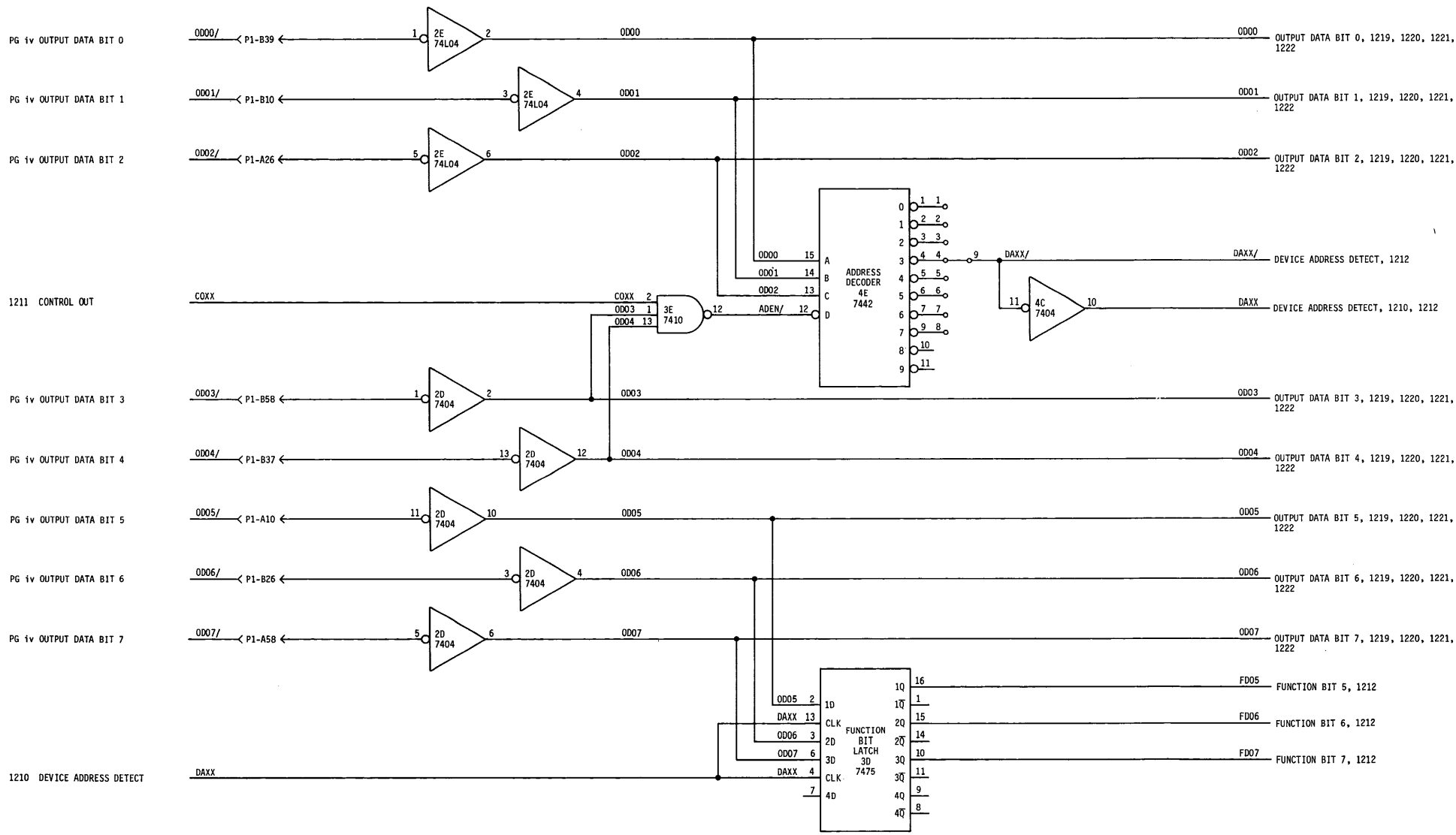
EXTERNAL DEVICE OUTPUT LINE DRIVERS

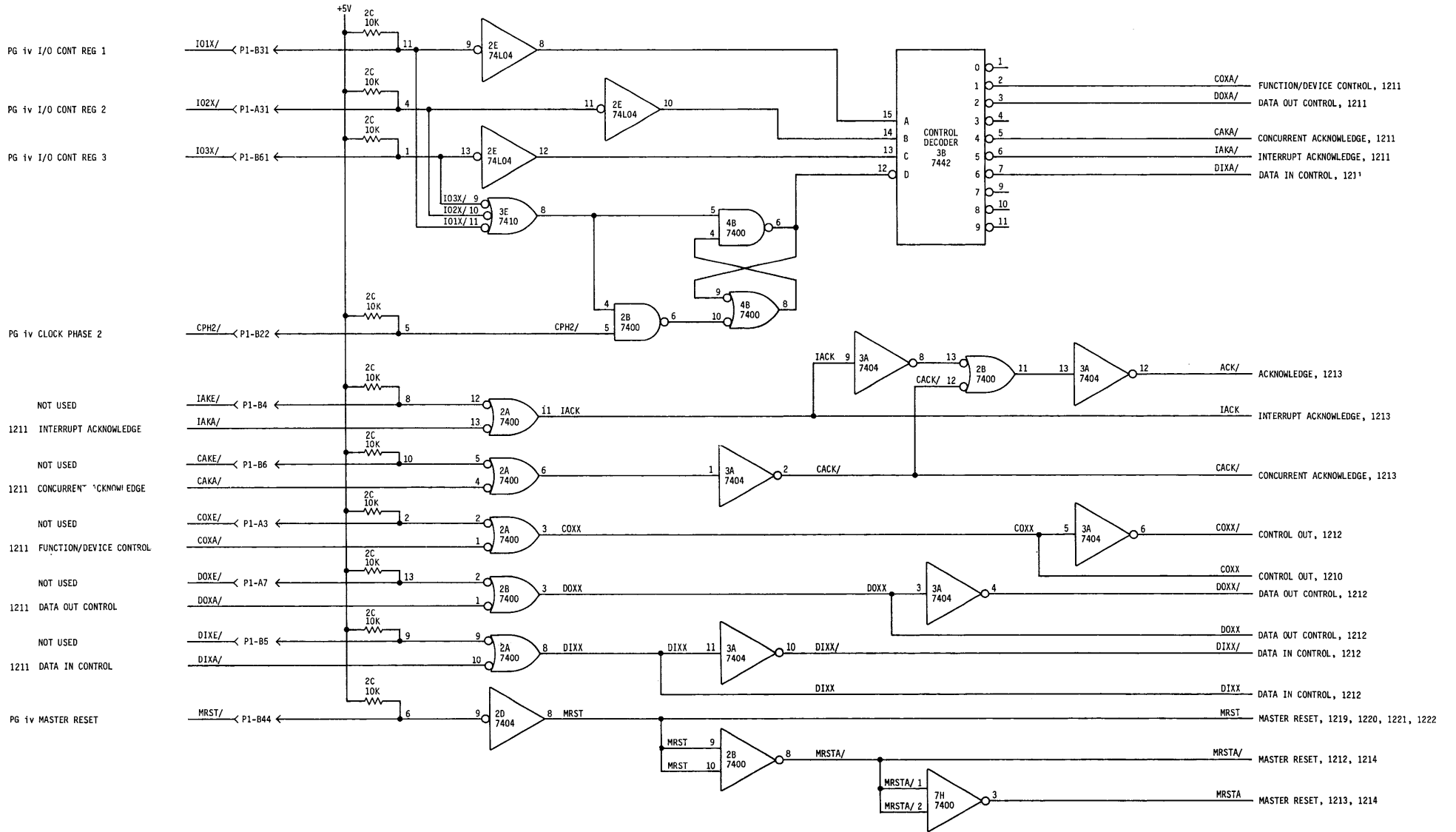


1112 STATUS IN
 1127 OVERRUN ERROR
 1112 DATA IN
 1127 RECEIVER REG BIT 1
 1127 FRAMING ERROR
 1127 RECEIVER REG BIT 2
 1114 CHANNEL-SCAN BIT 2
 1113 ANSWER
 1127 PARITY ERROR
 1127 RECEIVER REG BIT 3
 1114 CHANNEL-SCAN BIT 3
 1127 RECEIVER REG BIT 4
 1114 CHANNEL-SCAN BIT 4
 1127 RECEIVER REG BIT 5
 1114 R/T TIME-SCAN BIT 1
 1127 RECEIVER REG BIT 6
 1114 PULL-UP R8
 1127 RECEIVER REG BIT 7
 1127 RECEIVER REG BIT 8









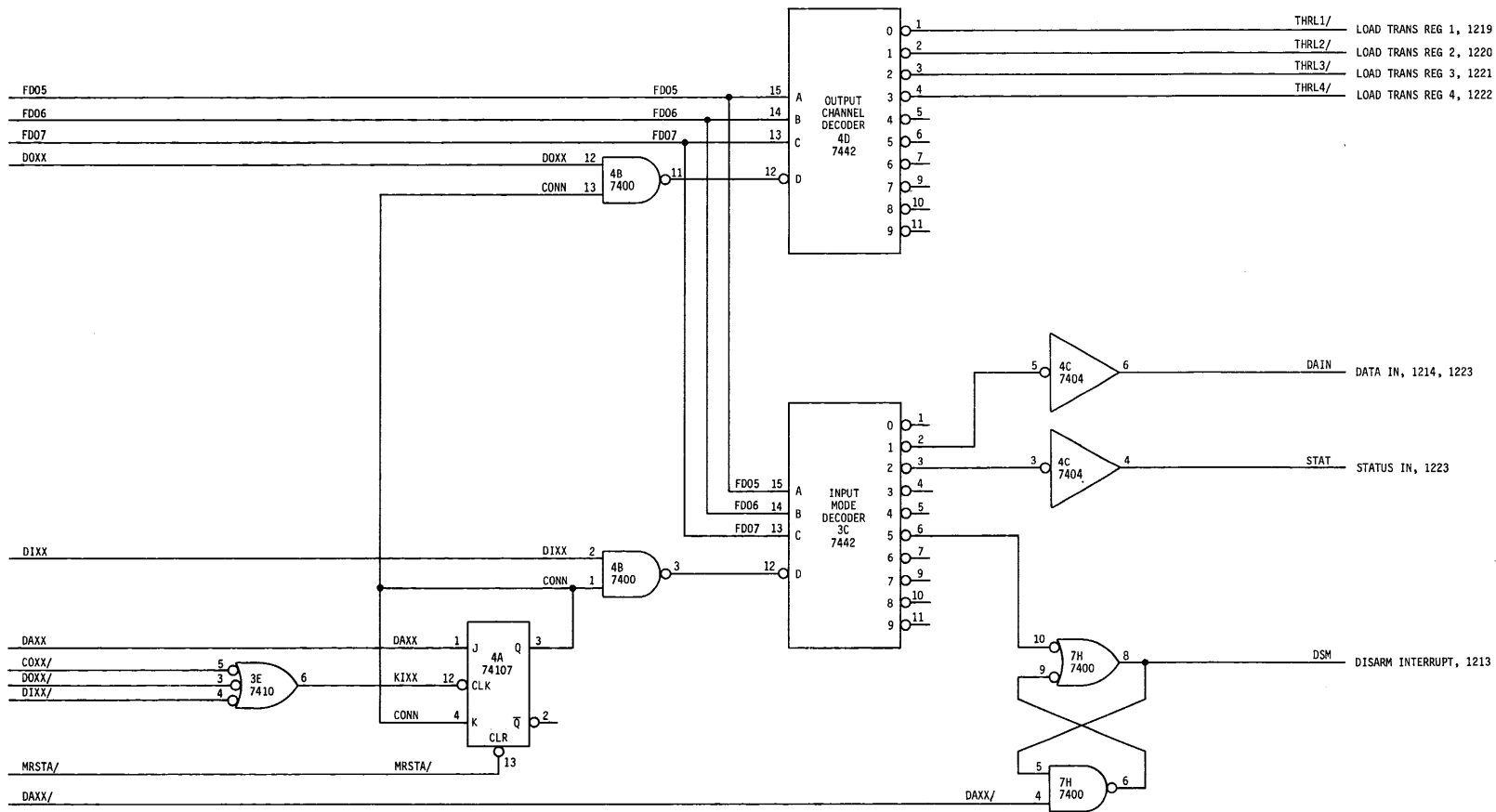
1210 FUNCTION BIT 5
 1210 FUNCTION BIT 6
 1210 FUNCTION BIT 7
 1211 DATA OUT CONTROL

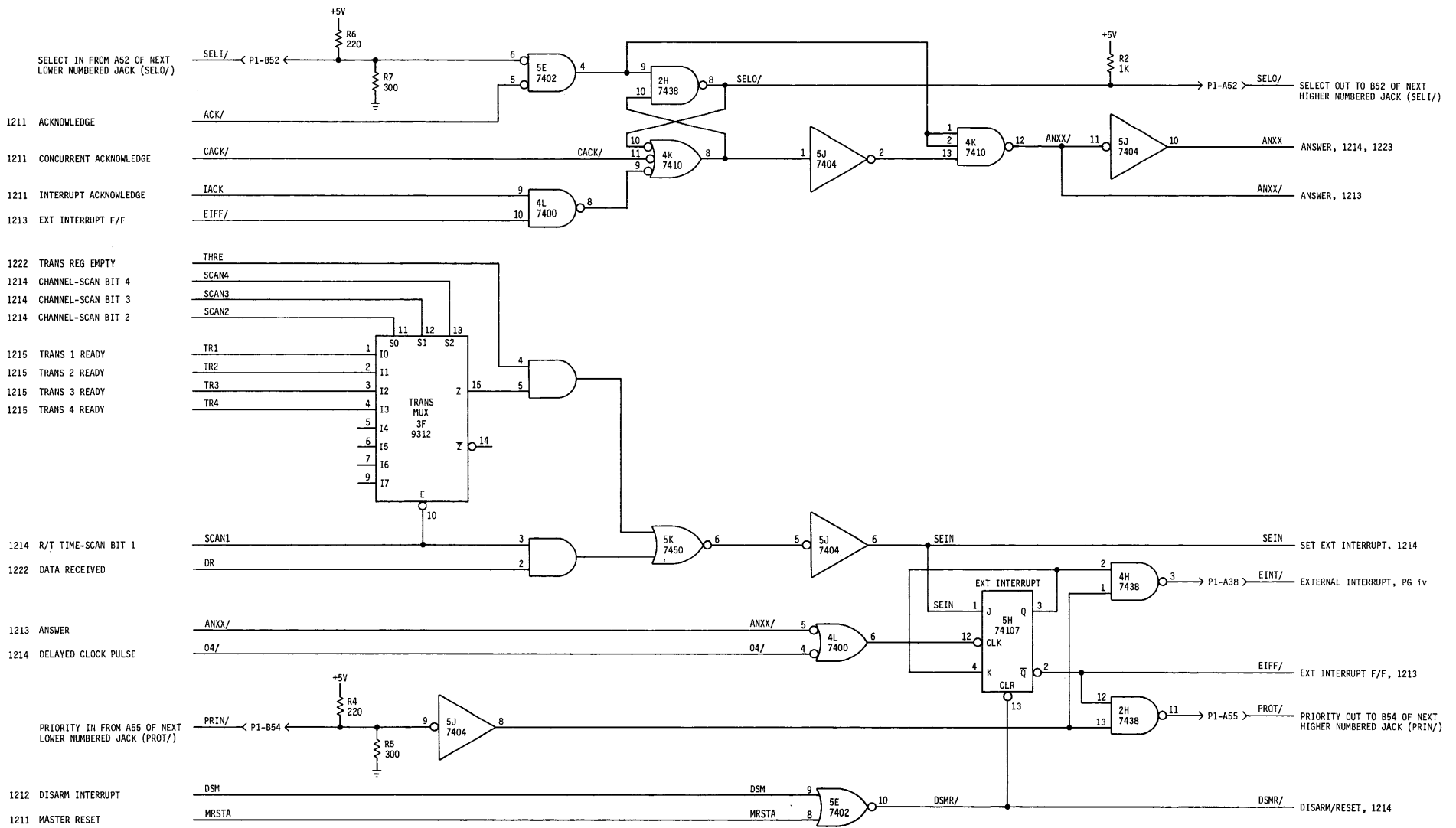
1211 DATA IN CONTROL

1210 DEVICE ADDRESS DETECT
 1211 CONTROL OUT
 1211 DATA OUT CONTROL
 1211 DATA IN CONTROL

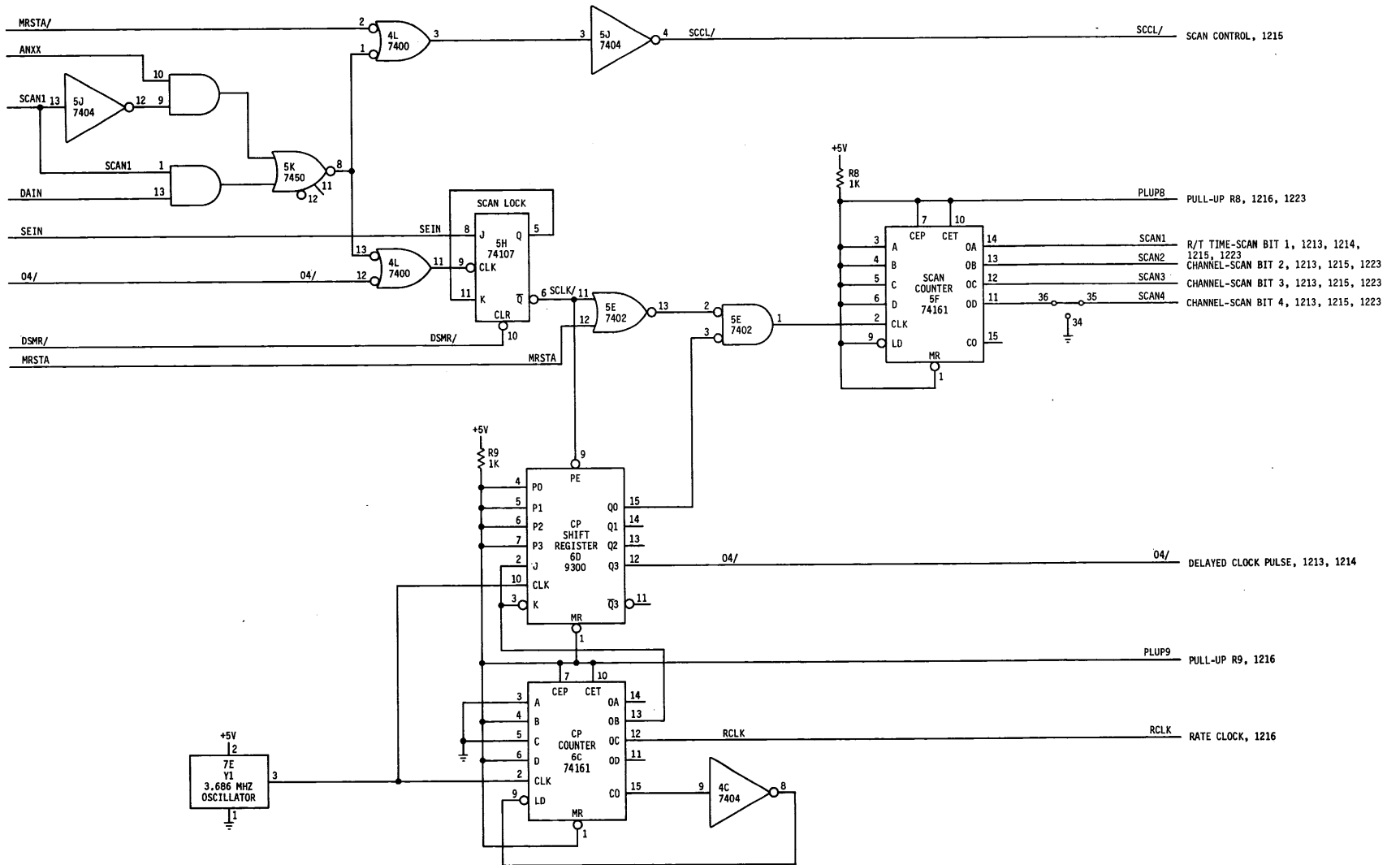
1211 MASTER RESET

1210 DEVICE ADDRESS DETECT





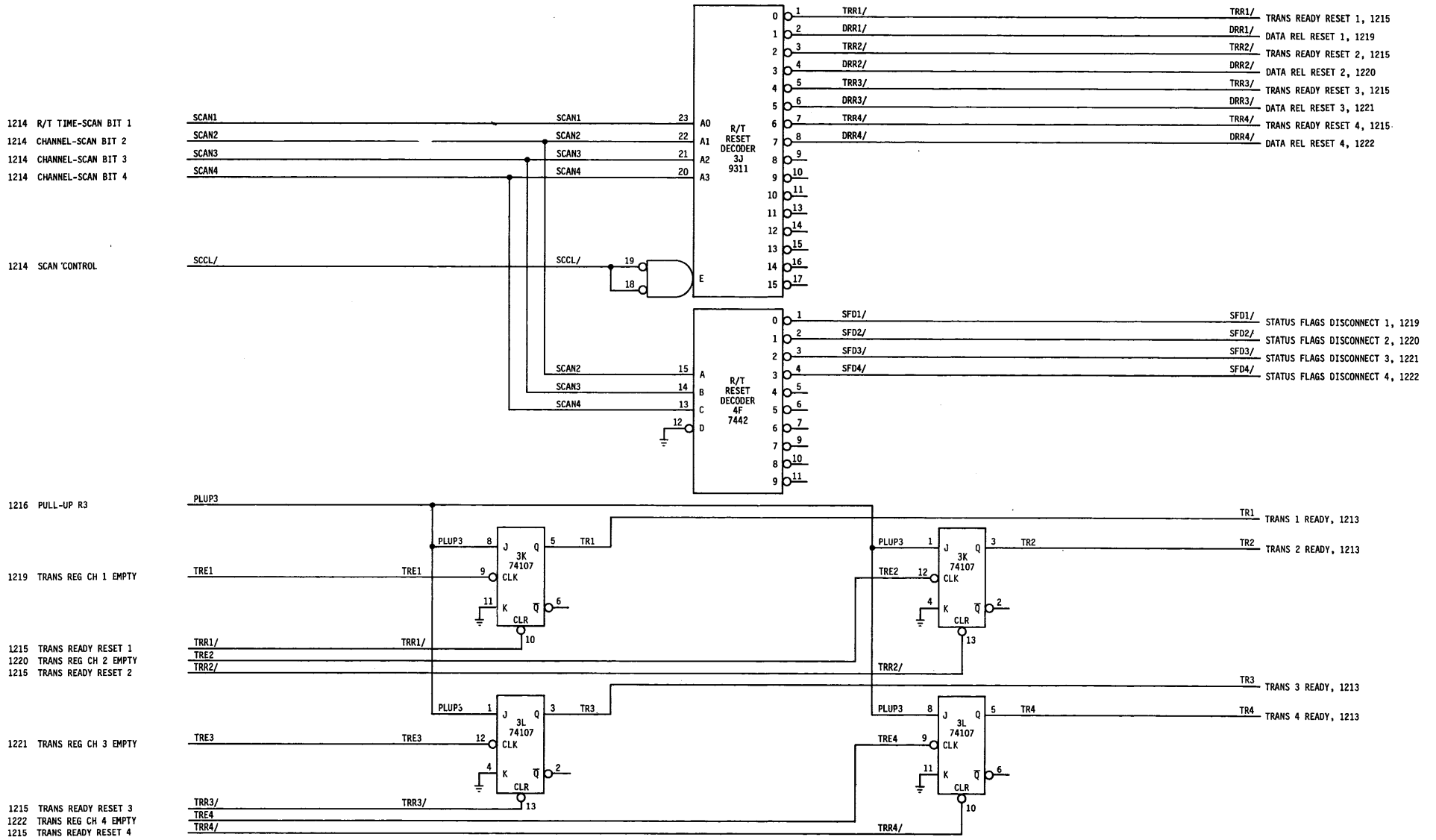
- 1211 MASTER RESET
- 1213 ANSWER
- 1214 RIT TIME-SCAN BIT 1
- 1212 DATA IN
- 1213 SET EXT INTERRUPT
- 1214 DELAYED CLOCK PULSE
- 1213 DISARM/RESET
- 1211 MASTER RESET



TIMING GENERATOR

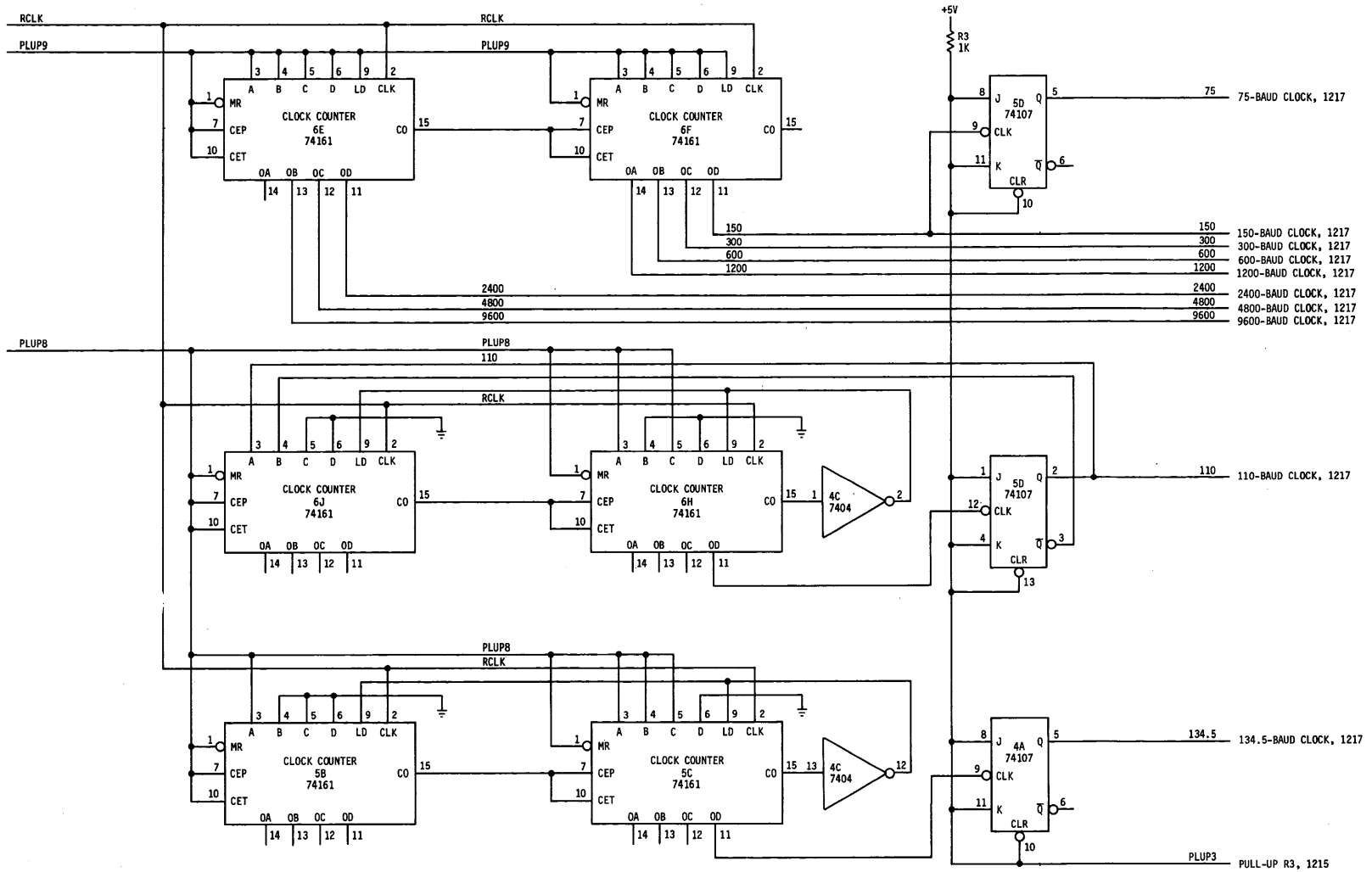
SWITCH SELECTABLE BAUD RATE
FOUR CHANNEL CONTROLLER
1214

RECEIVER/TRANSMITTER SEQUENCER AND TRANSMITTER STATUS REGISTER



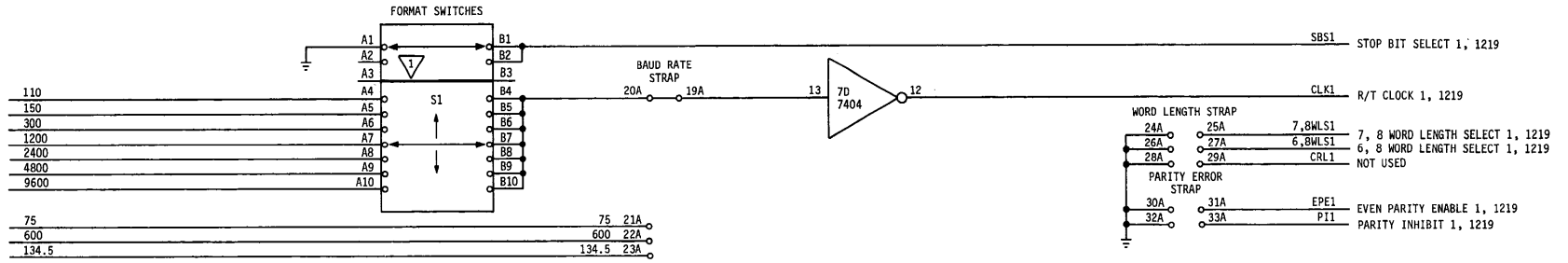
1214 RATE CLOCK
1214 PULL-UP R9

1214 PULL-UP R8



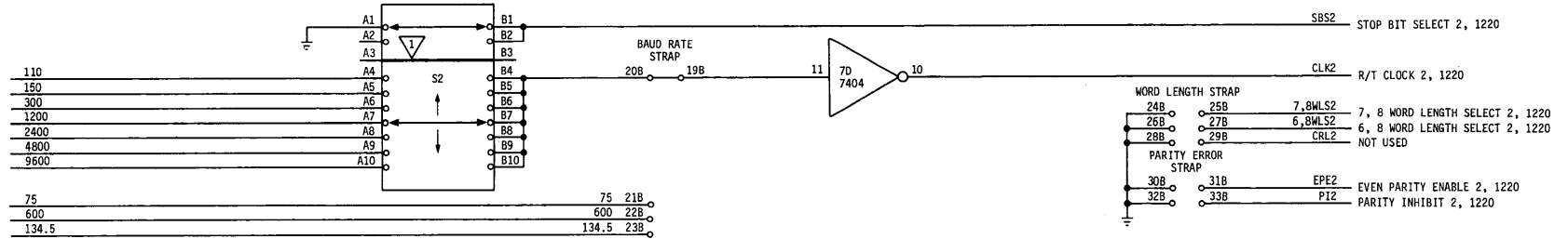
- 1216 110-BAUD CLOCK
- 1216 150-BAUD CLOCK
- 1216 300-BAUD CLOCK
- 1216 1200-BAUD CLOCK
- 1216 2400-BAUD CLOCK
- 1216 4800-BAUD CLOCK
- 1216 9600-BAUD CLOCK

- 1216 75-BAUD CLOCK
- 1216 600-BAUD CLOCK
- 1216 134.5-BAUD CLOCK



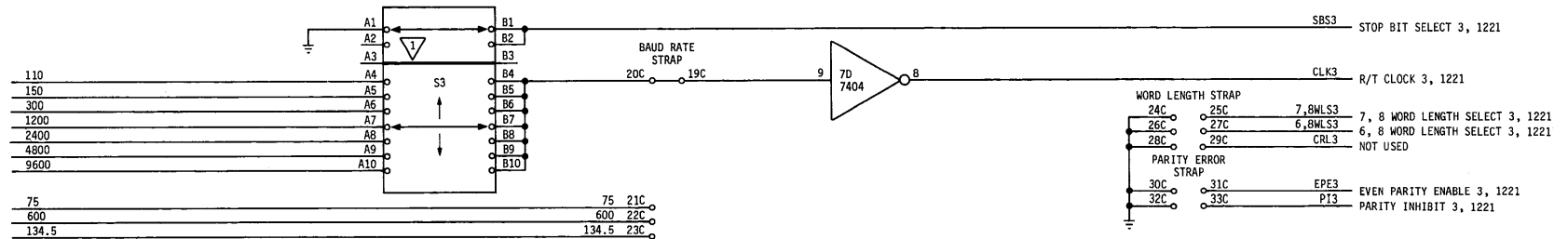
- 1216 110-BAUD CLOCK
- 1216 150-BAUD CLOCK
- 1216 300-BAUD CLOCK
- 1216 1200-BAUD CLOCK
- 1216 2400-BAUD CLOCK
- 1216 4800-BAUD CLOCK
- 1216 9600-BAUD CLOCK

- 1216 75-BAUD CLOCK
- 1216 600-BAUD CLOCK
- 1216 134.5-BAUD CLOCK



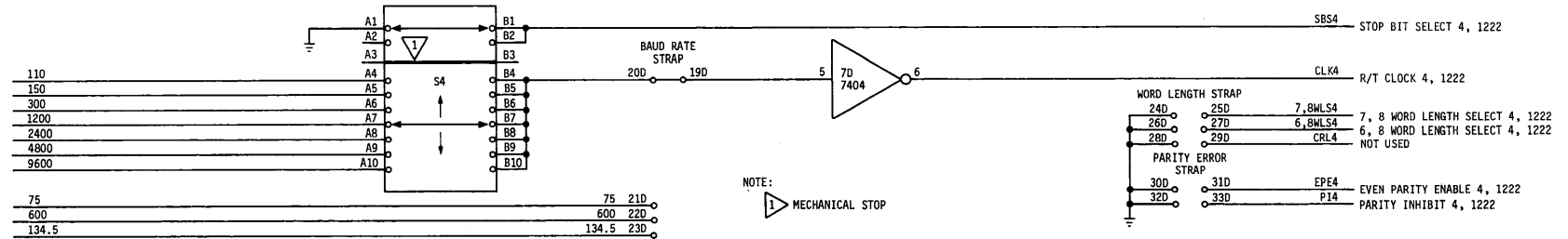
- 1216 110-BAUD CLOCK
- 1216 150-BAUD CLOCK
- 1216 300-BAUD CLOCK
- 1216 1200-BAUD CLOCK
- 1216 2400-BAUD CLOCK
- 1216 4800-BAUD CLOCK
- 1216 9600-BAUD CLOCK

- 1216 75-BAUD CLOCK
- 1216 600-BAUD CLOCK
- 1216 134.5-BAUD CLOCK

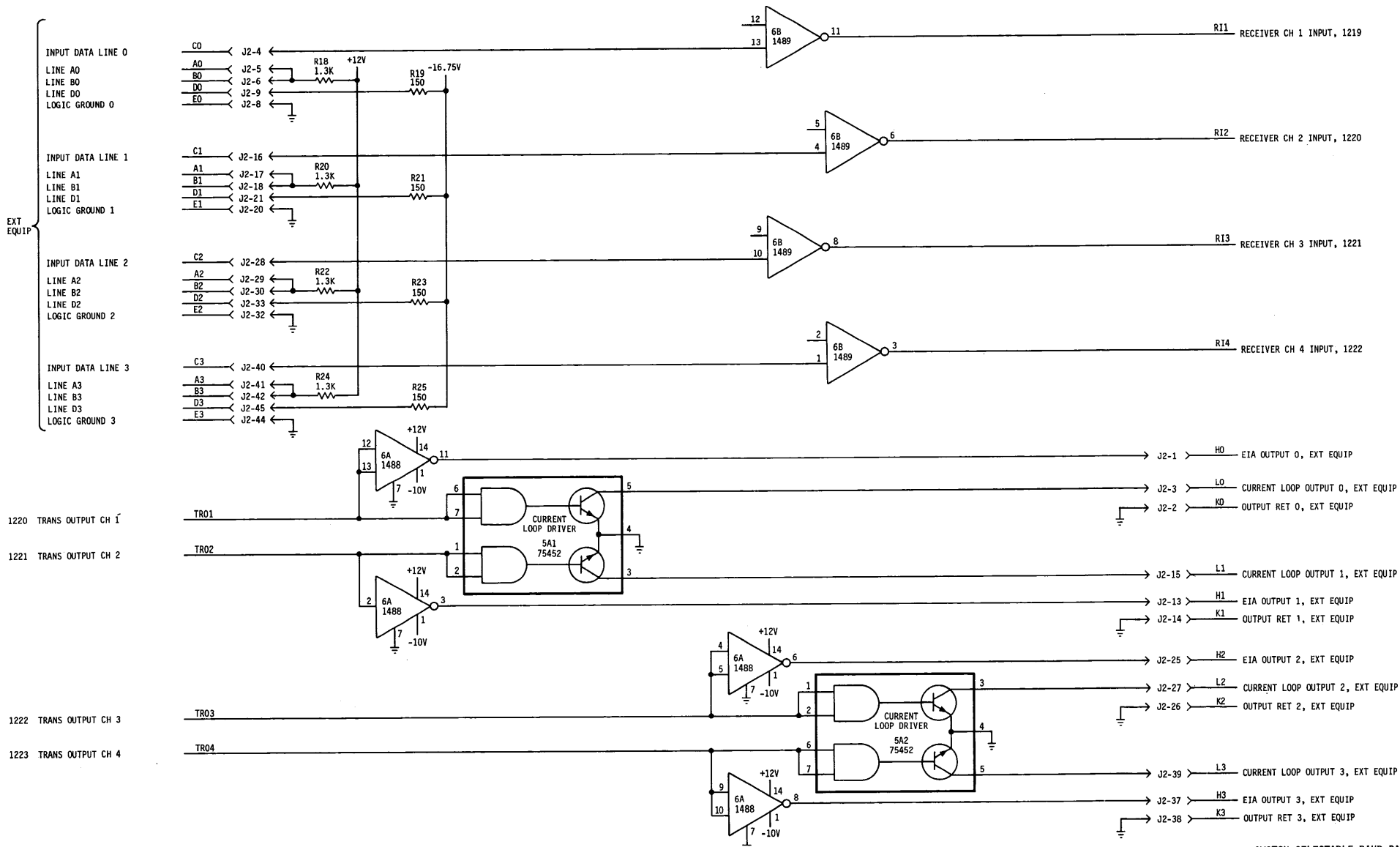


- 1216 110-BAUD CLOCK
- 1216 150-BAUD CLOCK
- 1216 300-BAUD CLOCK
- 1216 1200-BAUD CLOCK
- 1216 2400-BAUD CLOCK
- 1216 4800-BAUD CLOCK
- 1216 9600-BAUD CLOCK

- 1216 75-BAUD CLOCK
- 1216 600-BAUD CLOCK
- 1216 134.5-BAUD CLOCK



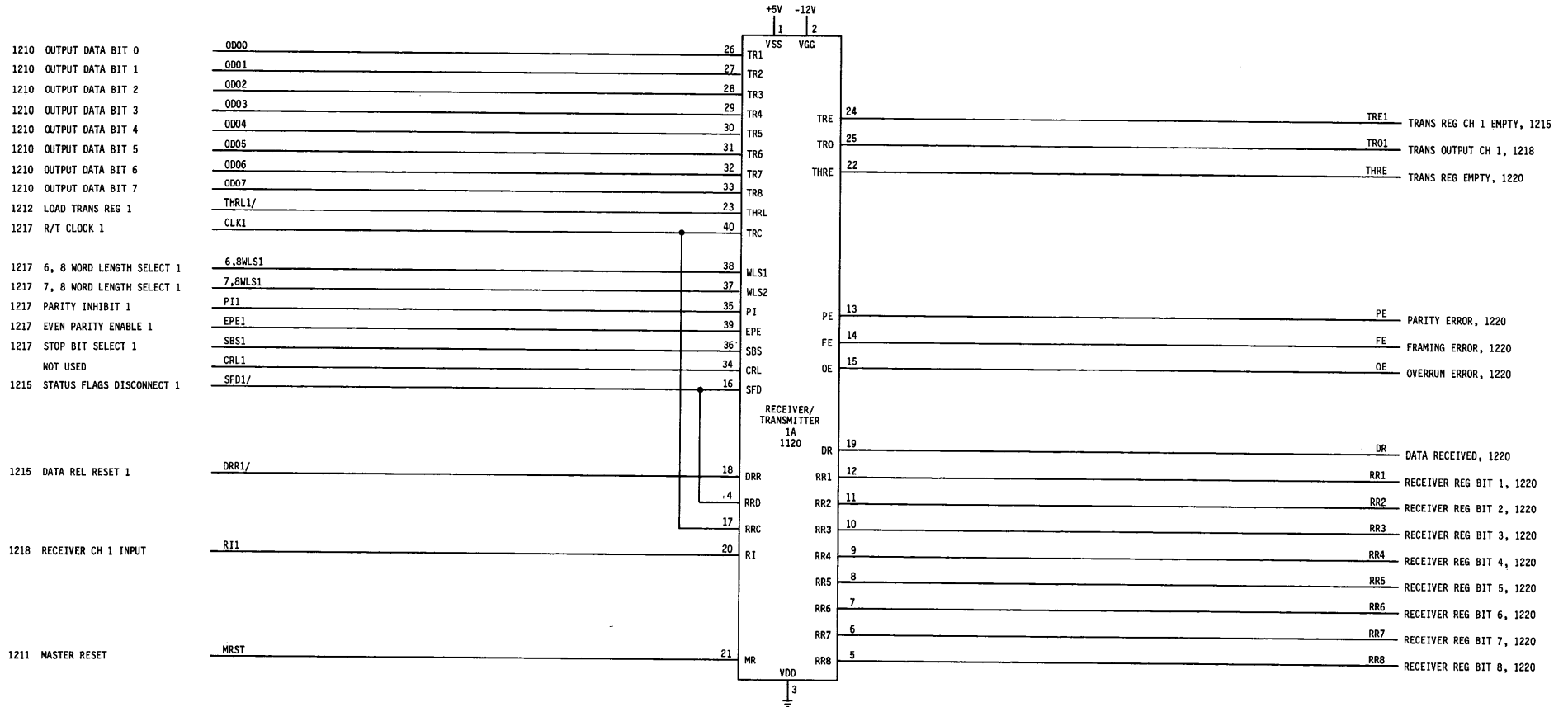
NOTE:
MECHANICAL STOP

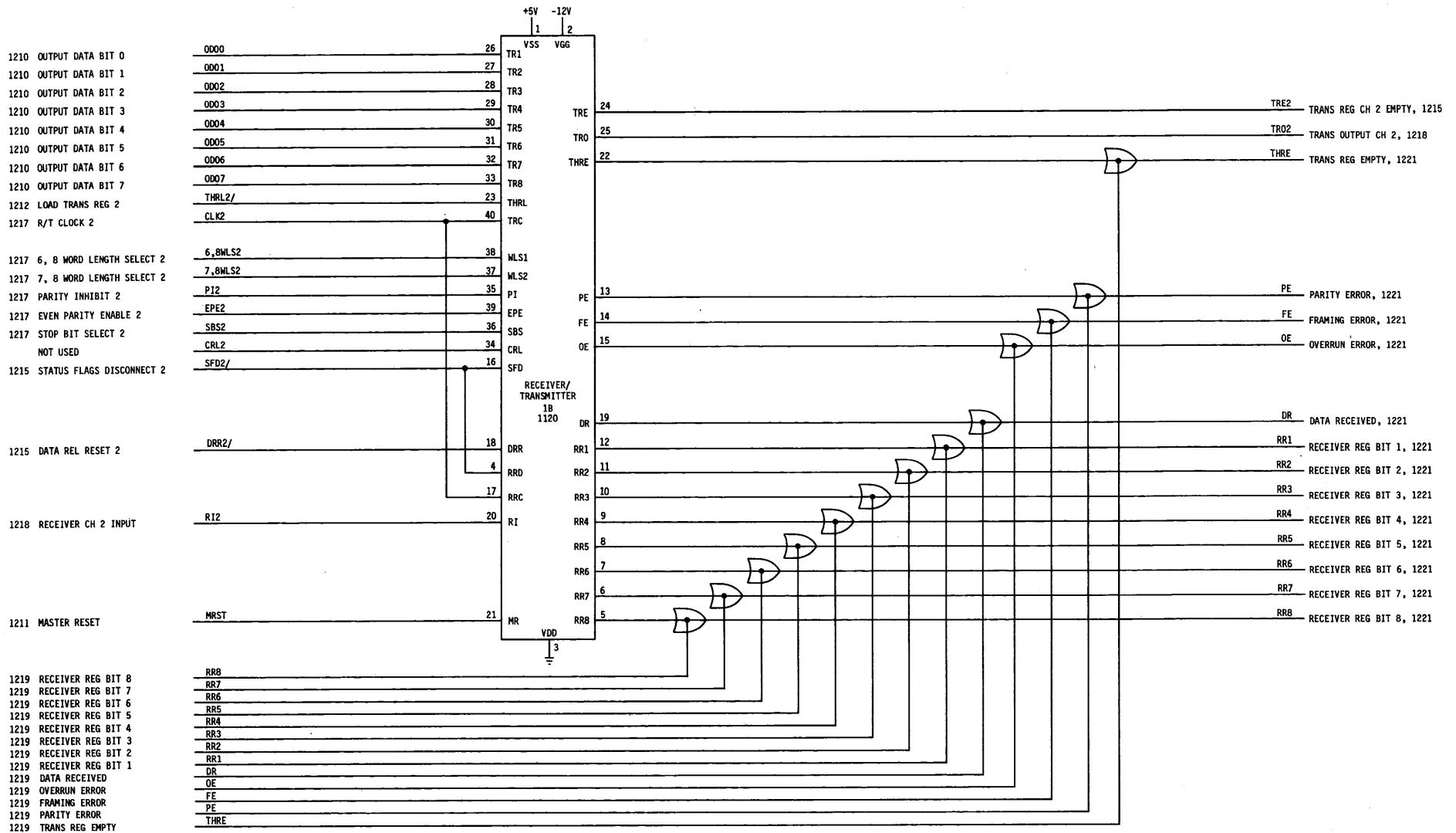


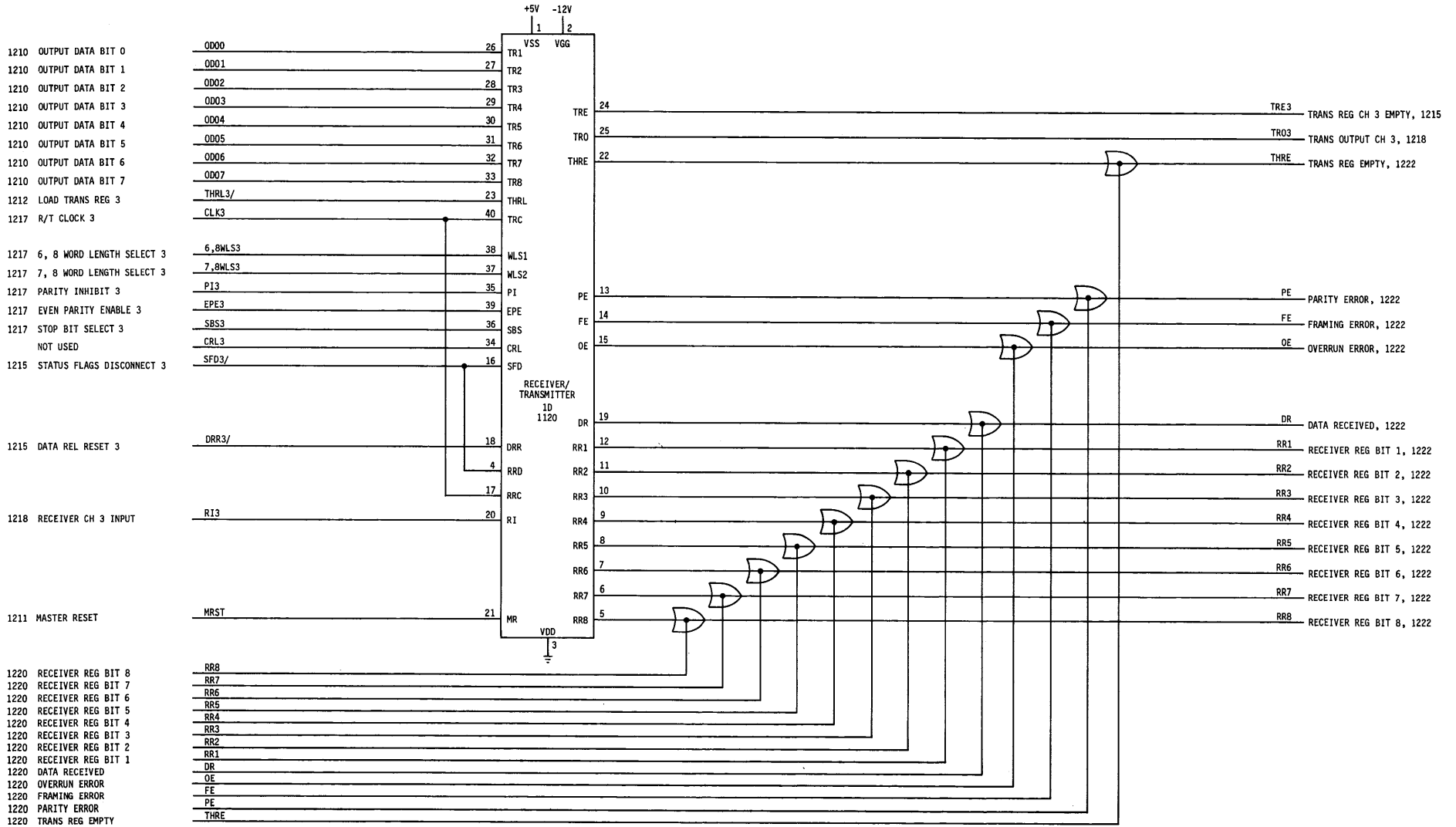
EXTERNAL DEVICE INPUT/OUTPUT LINE RECEIVERS

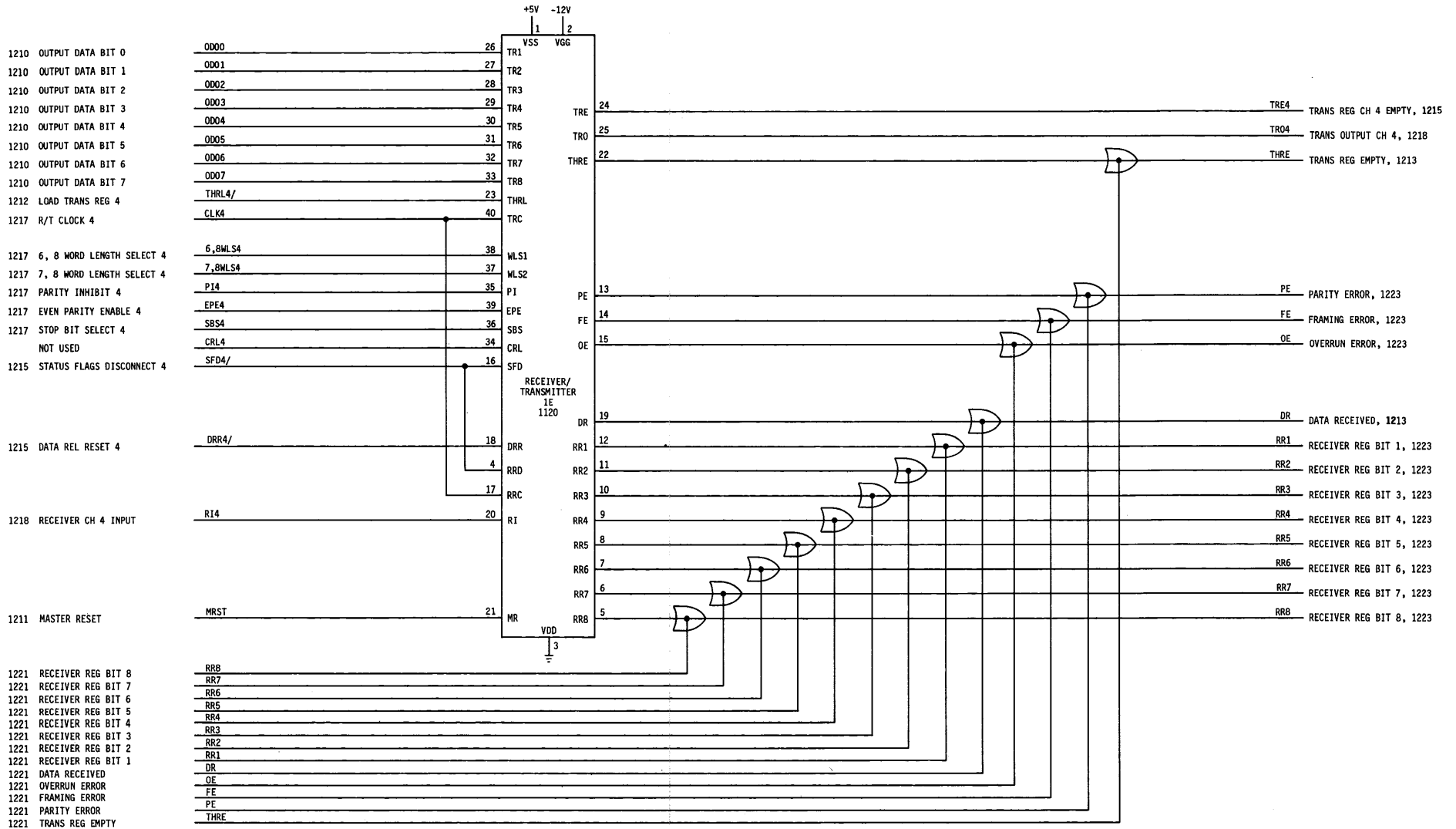
SWITCH SELECTABLE BAUD RATE
FOUR CHANNEL CONTROLLER
1218

CHANNEL 1 RECEIVER/TRANSMITTER CIRCUIT







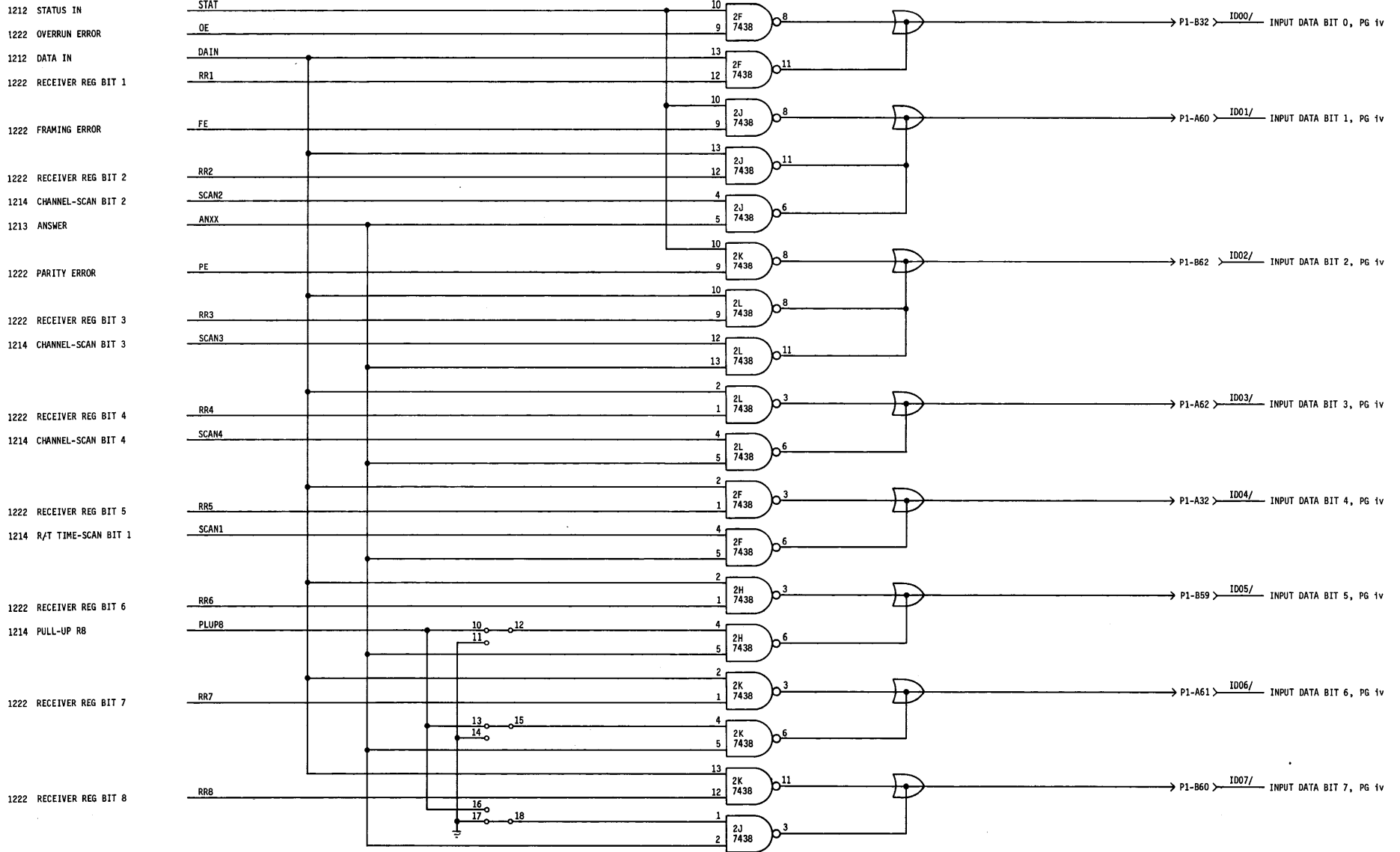


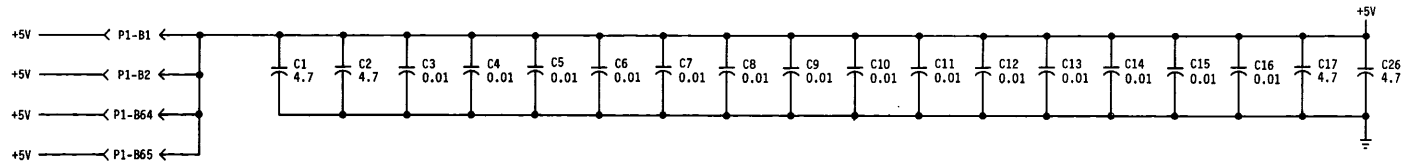
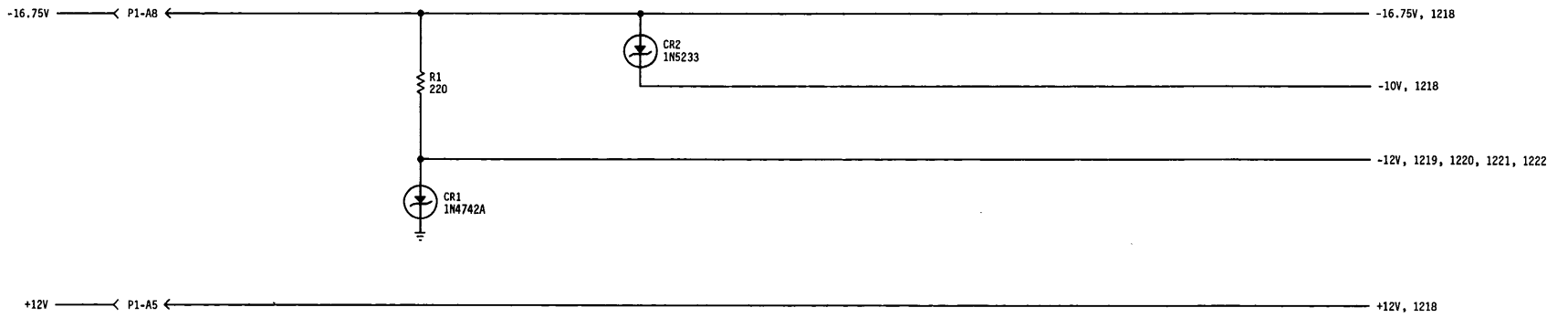
REV. AUG. 10, 1973
LD 1010
CENTRAL PROCESSING UNIT

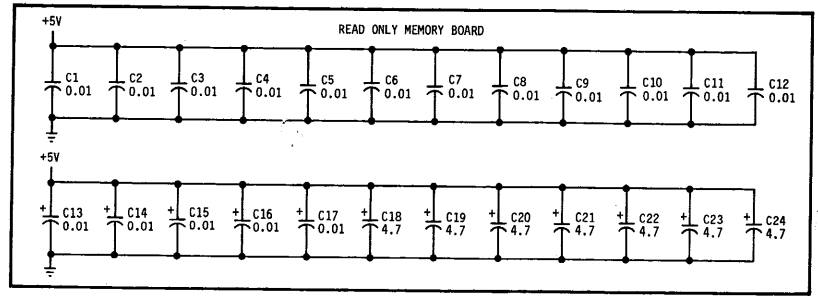
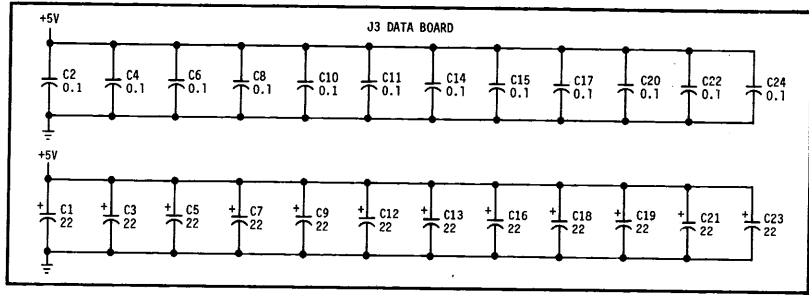
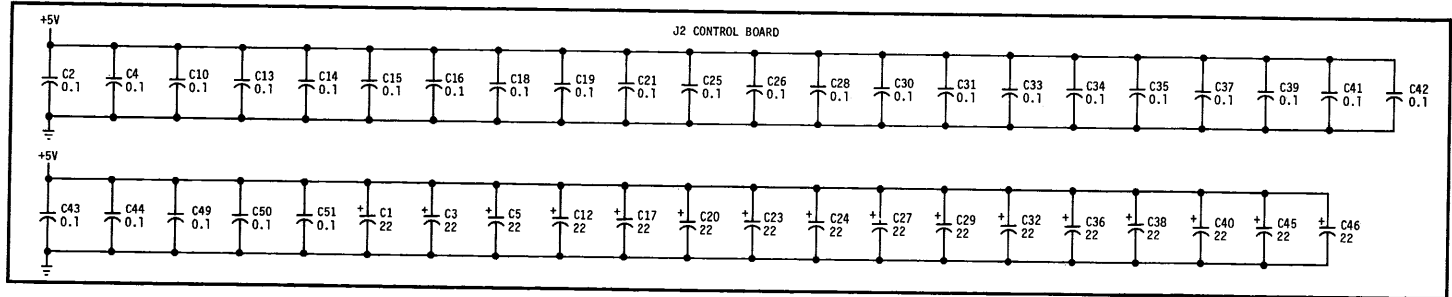
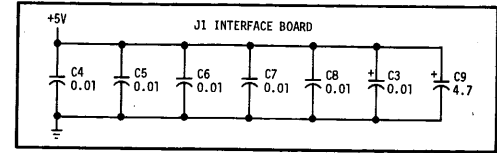
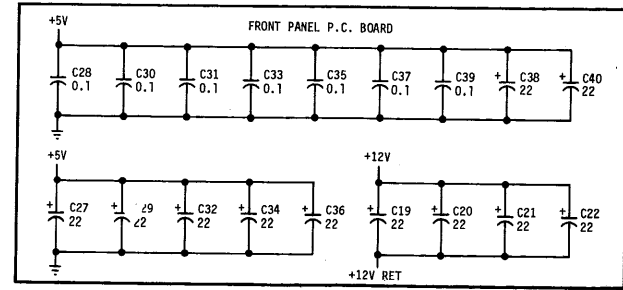
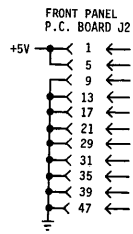
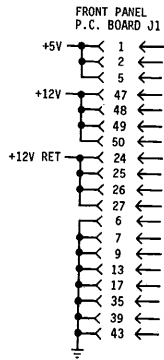
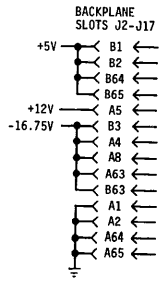
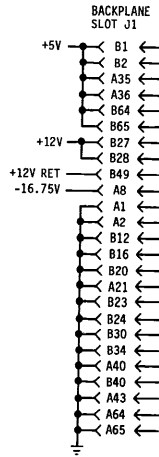
CHANNEL 4 RECEIVER/TRANSMITTER CIRCUIT

SWITCH SELECTABLE BAUD RATE
FOUR CHANNEL CONTROLLER
1222

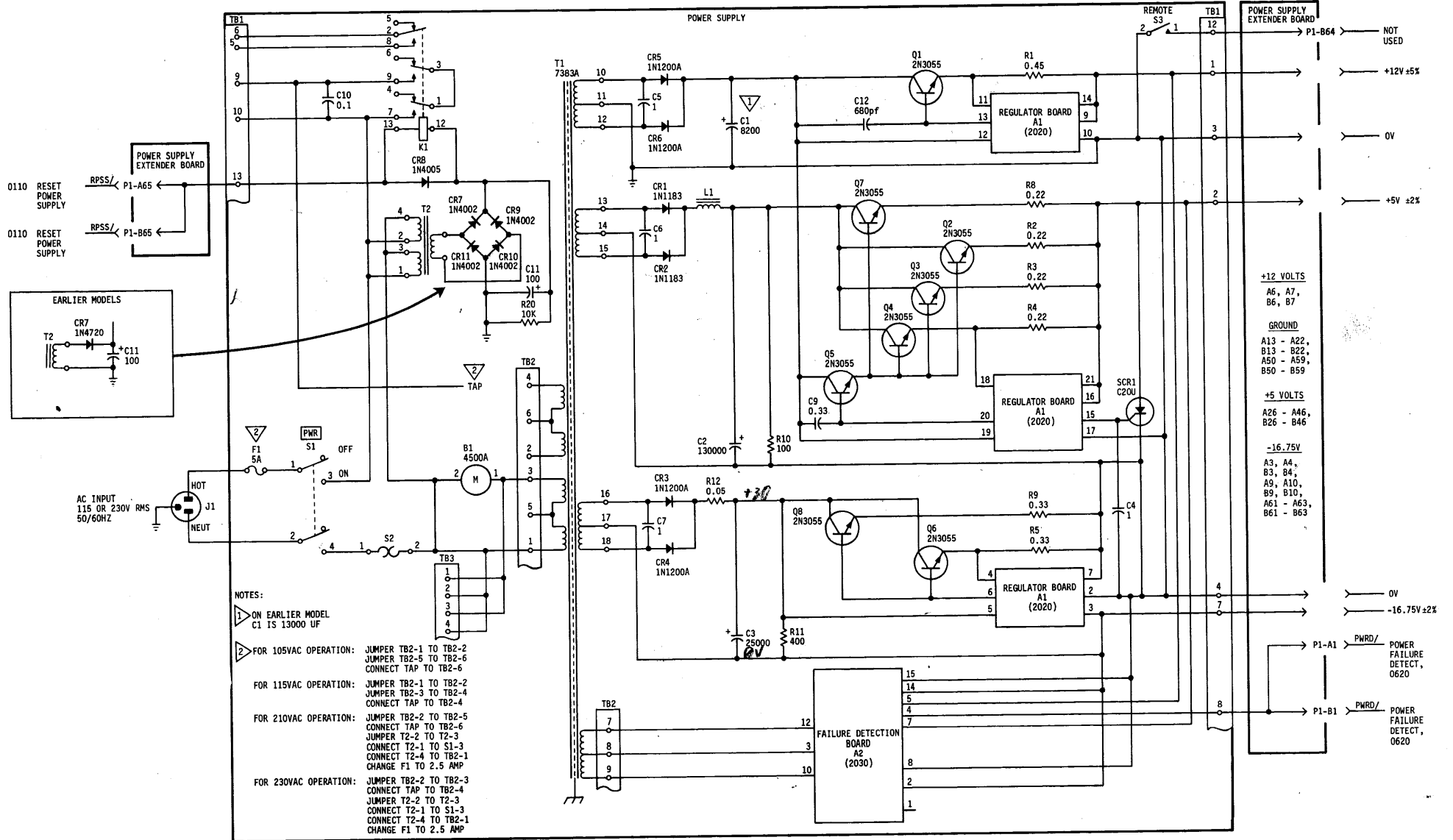
INPUT DATA MULTIPLEXER

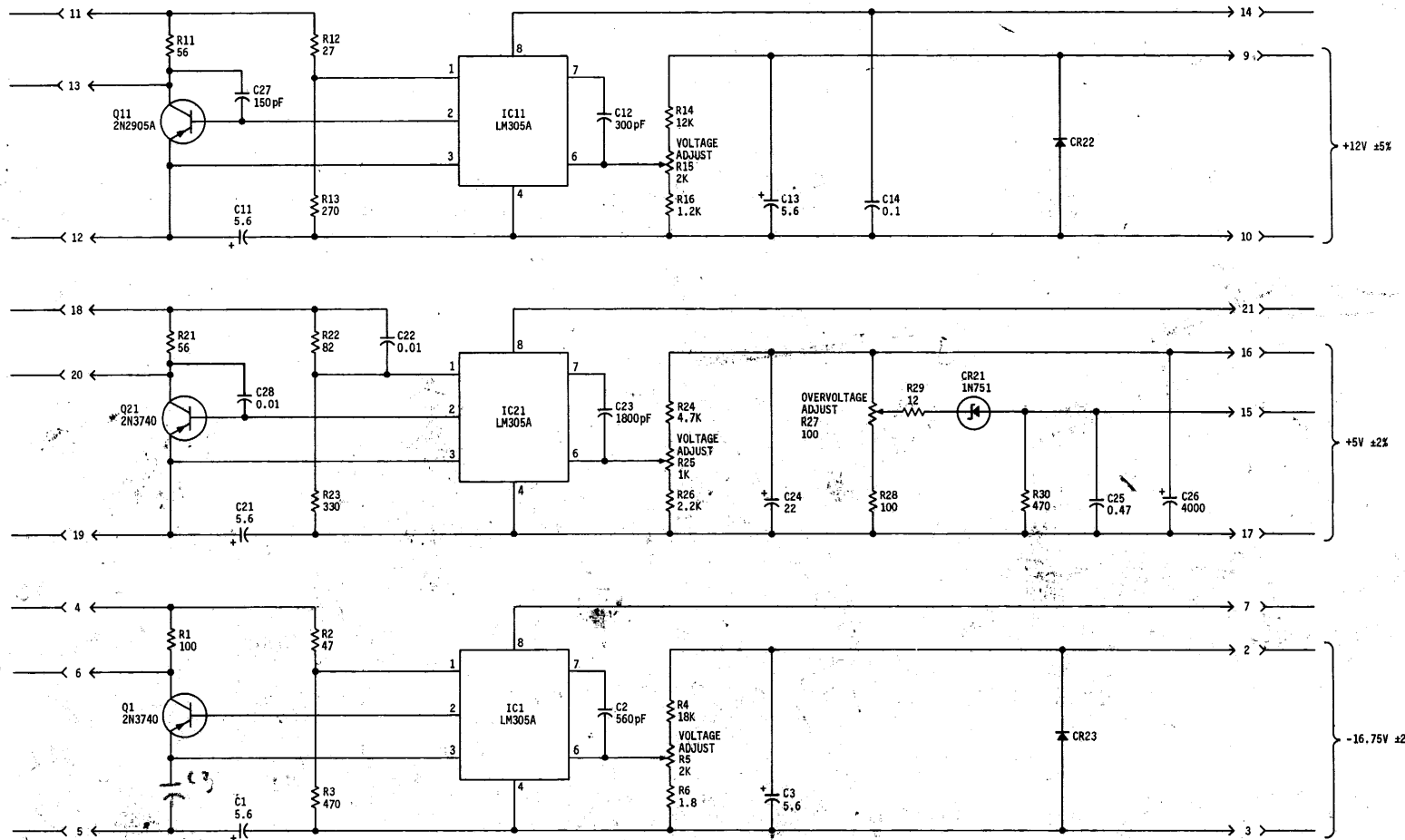


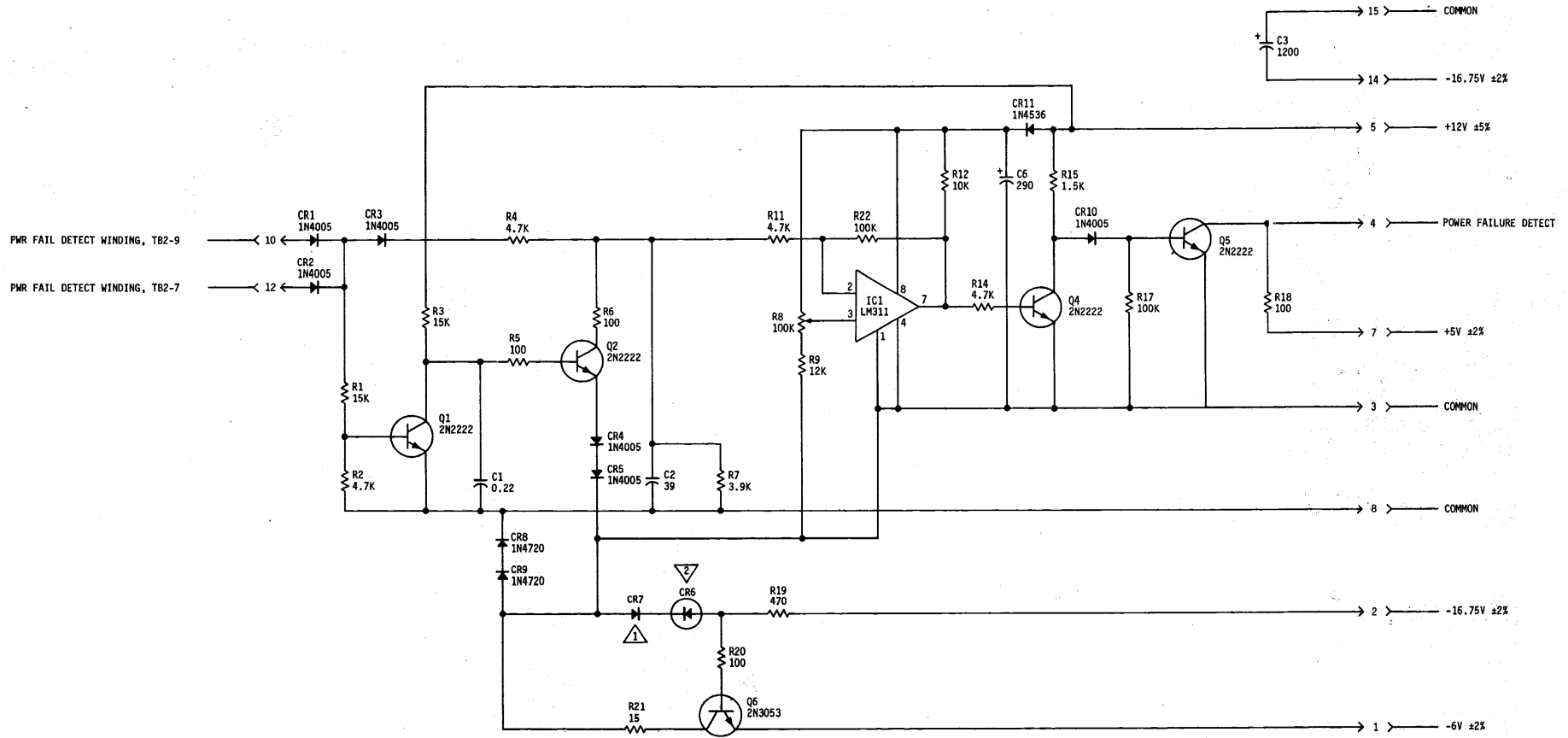




POWER SUPPLY CIRCUIT







NOTES:
 ▲ CR7 SELECTED IN TEST.
 ▲ CR6 IS 1N751A OR 1N4733A.