LD 2003

LOGIC DIAGRAMS
for
DMA/DISC STORAGE UNIT CONTROLLER

July 15, 1976

basic / four corporation
an MAI company

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LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

Title	Unit	Page	Revision Date
CPU Output Data Bus	Disc Control Logic Board	0010	Original
CPU I/O Control Bus	Disc Control Logic Board	0020	Original
Function Decoding	Disc Control Logic Board	0030	Original
Mode Register	Disc Control Logic Board	0040	Original
Drive and Cylinder Address	Disc Control Logic Board	0050	Original
Cylinder Address and Seek	Disc Control Logic Board	0060	Original
Fixed Disc Sector Address	Disc Control Logic Board	0070	Original
Removable Disc Sector Address	Disc Control Logic Board	0080	Original
Disc Select	Disc Control Logic Board	0090	Original
Address Compare and Head Selection	Disc Control Logic Board	0100	Original
Synchronizing	Disc Control Logic Board	0110	Original
Preamble Control	Disc Control Logic Board	0120	Original
Data Block Control	Disc Control Logic Board	0130	Original
Postamble Control	Disc Control Logic Board	0140	Original
Read Byte Control	Disc Control Logic Board	0150	Original
Read Byte Register	Disc Control Logic Board	0160	Original
Byte Ready	Disc Control Logic Board	0170	Original
D Bus Bits 0 and 1	Disc Control Logic Board	0180	Original
D Bus Bits 2 and 3	Disc Control Logic Board	0190	Original
D Bus Bits 4 and 5	Disc Control Logic Board	0200	Original
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Power Distribution	Disc Control Logic Board	0230	Original
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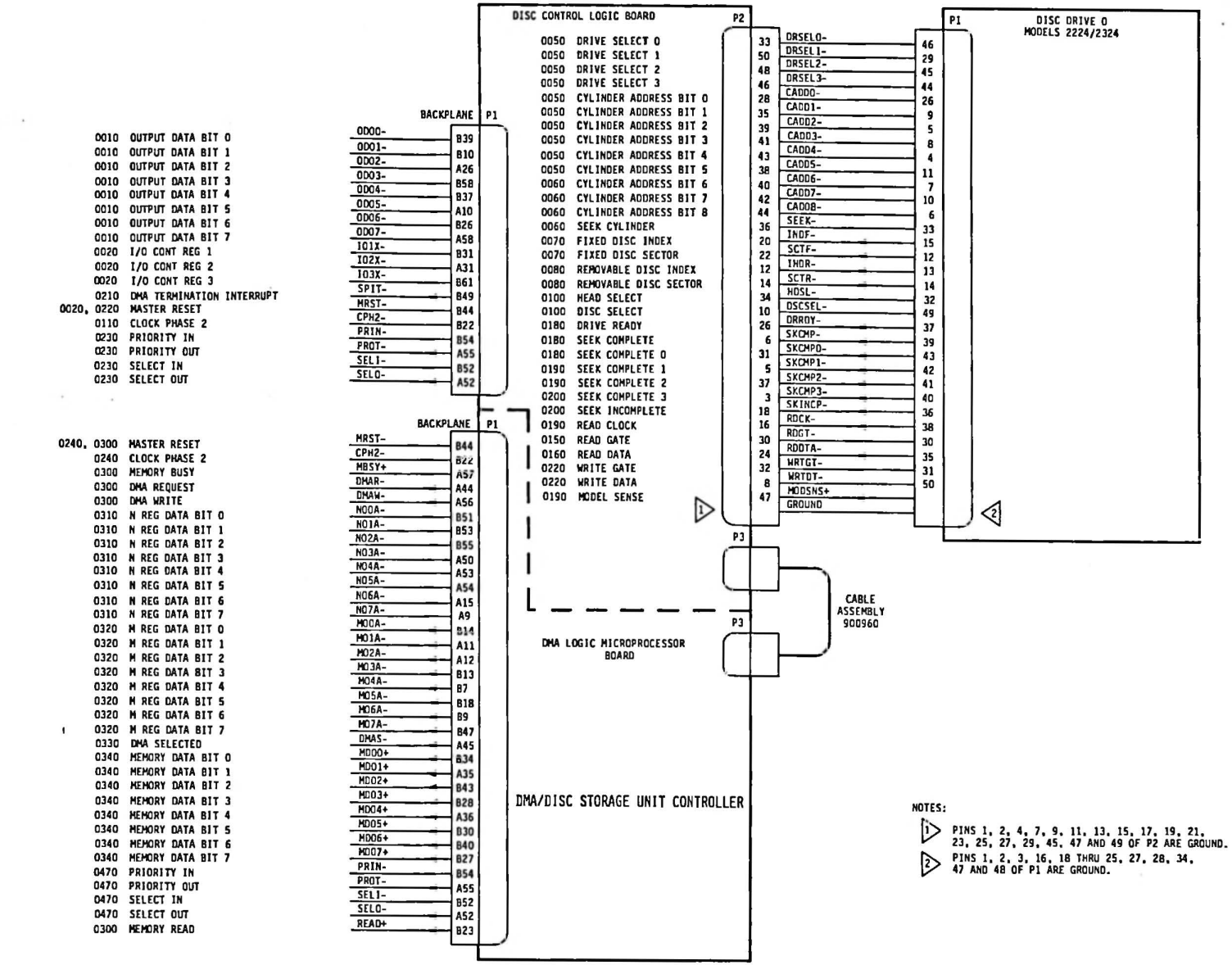
G Register	DMA Logic Microprocessor Board	0350	Original
A Bus Register	DMA Logic Microprocessor Board	0360	Original
B Bus Register	DMA Logic Microprocessor Board	0370	Original
Arithmetic Logic Unit and Scratch Pad Memory, Sheet 1	DMA Logic Microprocessor Board	0380	Original
Arithmetic Logic Unit and Scratch Pad Memory, Sheet 2	DMA Logic Microprocessor Board	0390	Original
KB0 Register	DMA Logic Microprocessor Board	0400	Original
KB1 Register and KB Mux	DMA Logic Microprocessor Board	0410	Original
DA Bus Low Order Byte	DMA Logic Microprocessor Board	0420	Original
DA Bus High Order Byte and Disc Serial Write	DMA Logic Microprocessor Board	0430	Original
KC Register	DMA Logic Microprocessor Board	0440	Original
KD/KC Compare	DMA Logic Microprocessor Board	0450	Original
KD/KB Compare	DMA Logic Microprocessor Board	0460	Original
Power Distribution	DMA Logic Microprocessor Board	0470	Original

INTERCONNECTION DIAGRAM

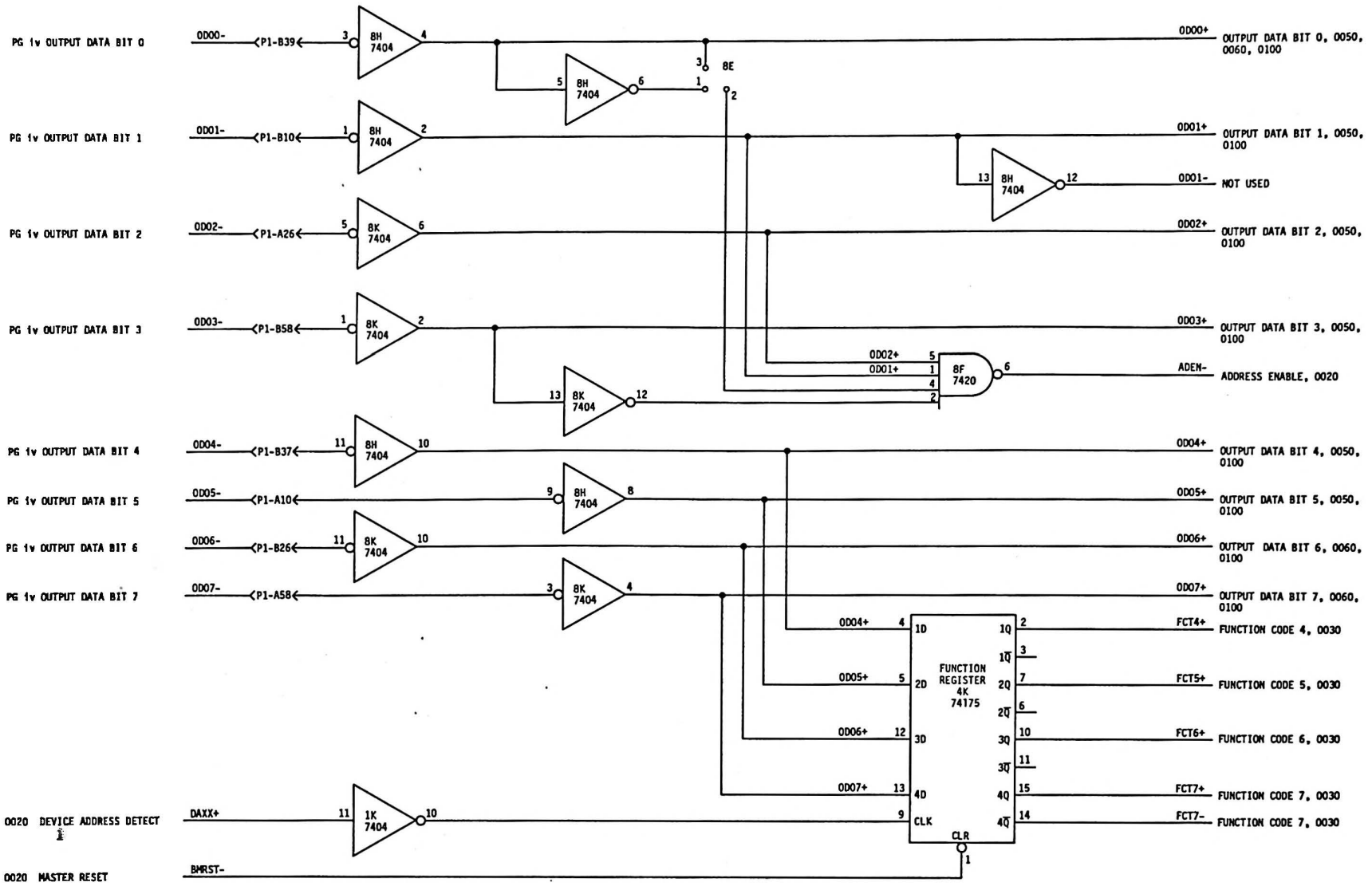


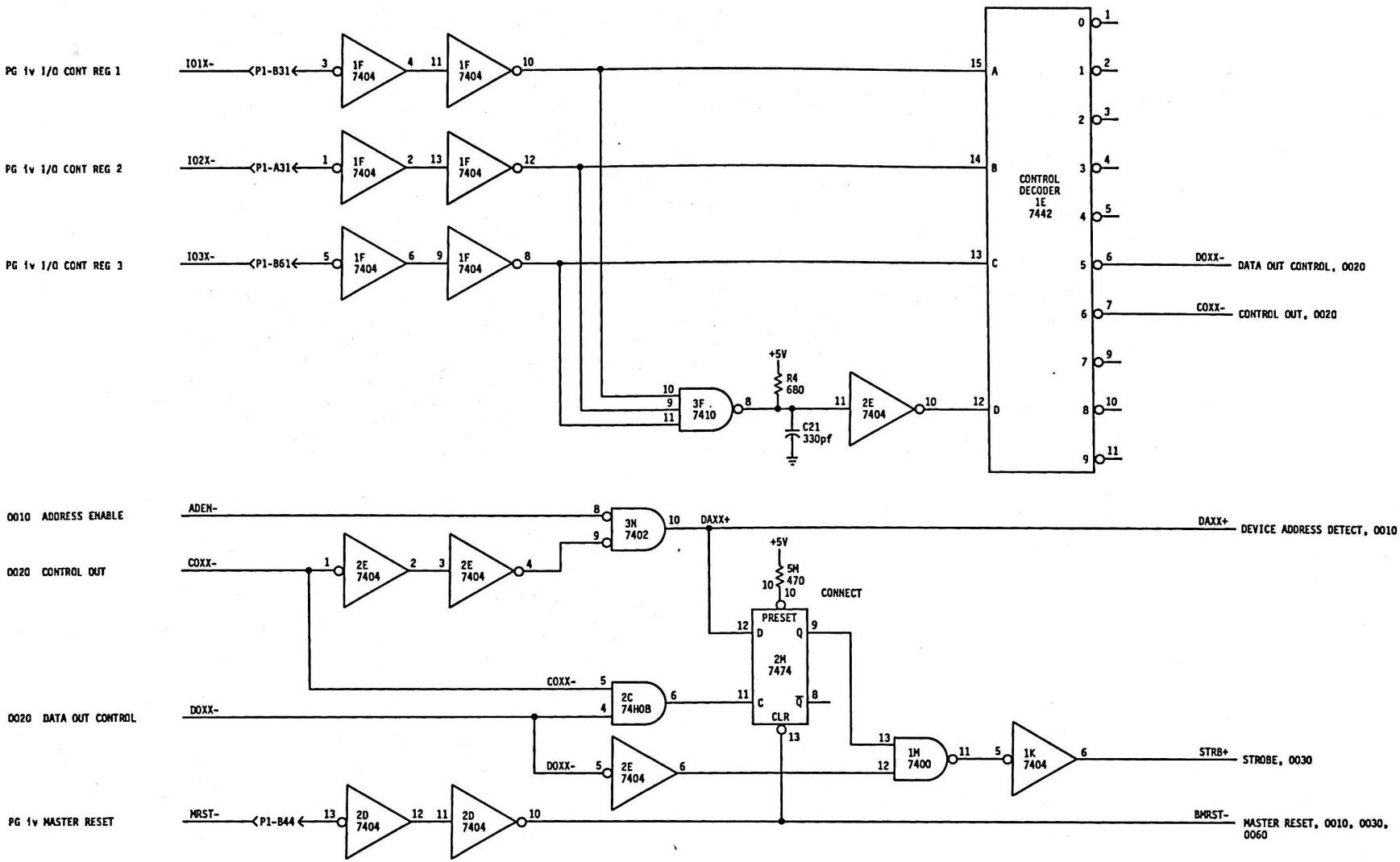
0010 OUTPUT DATA BIT 0
0010 OUTPUT DATA BIT 1
0010 OUTPUT DATA BIT 2
0010 OUTPUT DATA BIT 3
0010 OUTPUT DATA BIT 4
0010 OUTPUT DATA BIT 5
0010 OUTPUT DATA BIT 6
0010 OUTPUT DATA BIT 7
0020 I/O CONT REG 1
0020 I/O CONT REG 2
0020 I/O CONT REG 3
0210 DMA TERMINATION INTERRUPT
0020, 0220 MASTER RESET
0110 CLOCK PHASE 2
0230 PRIORITY IN
0230 PRIORITY OUT
0230 SELECT IN
0230 SELECT OUT

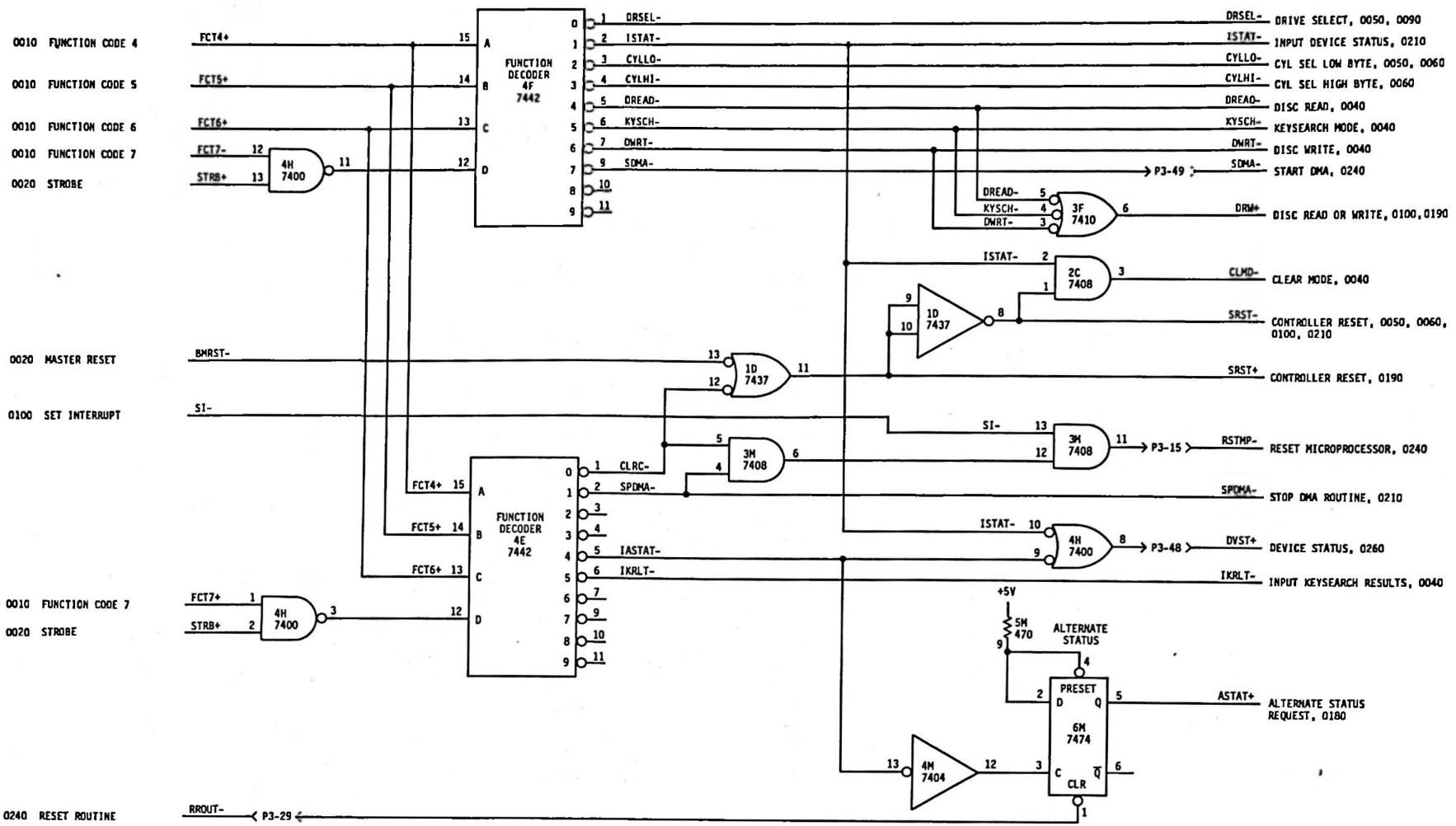
0240, 0300 MASTER RESET
0240 CLOCK PHASE 2
0300 MEMORY BUSY
0300 DMA REQUEST
0300 DMA WRITE
0310 N REG DATA BIT 0
0310 N REG DATA BIT 1
0310 N REG DATA BIT 2
0310 N REG DATA BIT 3
0310 N REG DATA BIT 4
0310 N REG DATA BIT 5
0310 N REG DATA BIT 6
0310 N REG DATA BIT 7
0320 M REG DATA BIT 0
0320 M REG DATA BIT 1
0320 M REG DATA BIT 2
0320 M REG DATA BIT 3
0320 M REG DATA BIT 4
0320 M REG DATA BIT 5
0320 M REG DATA BIT 6
0320 M REG DATA BIT 7
0330 DMA SELECTED
0340 MEMORY DATA BIT 0
0340 MEMORY DATA BIT 1
0340 MEMORY DATA BIT 2
0340 MEMORY DATA BIT 3
0340 MEMORY DATA BIT 4
0340 MEMORY DATA BIT 5
0340 MEMORY DATA BIT 6
0340 MEMORY DATA BIT 7
0470 PRIORITY IN
0470 PRIORITY OUT
0470 SELECT IN
0470 SELECT OUT
0300 MEMORY READ

NOTES:

1. PINS 1, 2, 4, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 45, 47 AND 49 OF P2 ARE GROUND.
2. PINS 1, 2, 3, 16, 18 THRU 25, 27, 28, 34, 47 AND 48 OF P1 ARE GROUND.


PG 1v OUTPUT DATA BIT 0
PG 1v OUTPUT DATA BIT 1
PG 1v OUTPUT DATA BIT 2
PG 1v OUTPUT DATA BIT 3
PG 1v OUTPUT DATA BIT 4
PG 1v OUTPUT DATA BIT 5
PG 1v OUTPUT DATA BIT 6
PG 1v OUTPUT DATA BIT 7
0020 DEVICE ADDRESS DETECT
0020 MASTER RESET
OD00-
OD01-
OD02-
OD03-
OD04-
OD05-
OD06-
OD07-
P1-B39
P1-B10
P1-A26
P1-B58
P1-B37
P1-A10
P1-B26
P1-A58
DAXX+
BMRST-
8H 7404
8K 7404
1K 7404
8E
8F 7420
FUNCTION REGISTER 4K 74175
OD00+
OD01+
OD02+
OD03+
OD04+
OD05+
OD06+
OD07+
OUTPUT DATA BIT 0, 0050, 0060, 0100
OUTPUT DATA BIT 1, 0050, 0100
NOT USED
OUTPUT DATA BIT 2, 0050, 0100
OUTPUT DATA BIT 3, 0050, 0100
ADEN-
ADDRESS ENABLE, 0020
OUTPUT DATA BIT 4, 0050, 0100
OUTPUT DATA BIT 5, 0050, 0100
OUTPUT DATA BIT 6, 0060, 0100
OUTPUT DATA BIT 7, 0060, 0100
FCT4+
FCT5+
FCT6+
FCT7+
FCT7-
FUNCTION CODE 4, 0030
FUNCTION CODE 5, 0030
FUNCTION CODE 6, 0030
FUNCTION CODE 7, 0030
FUNCTION CODE 7, 0030
CLR

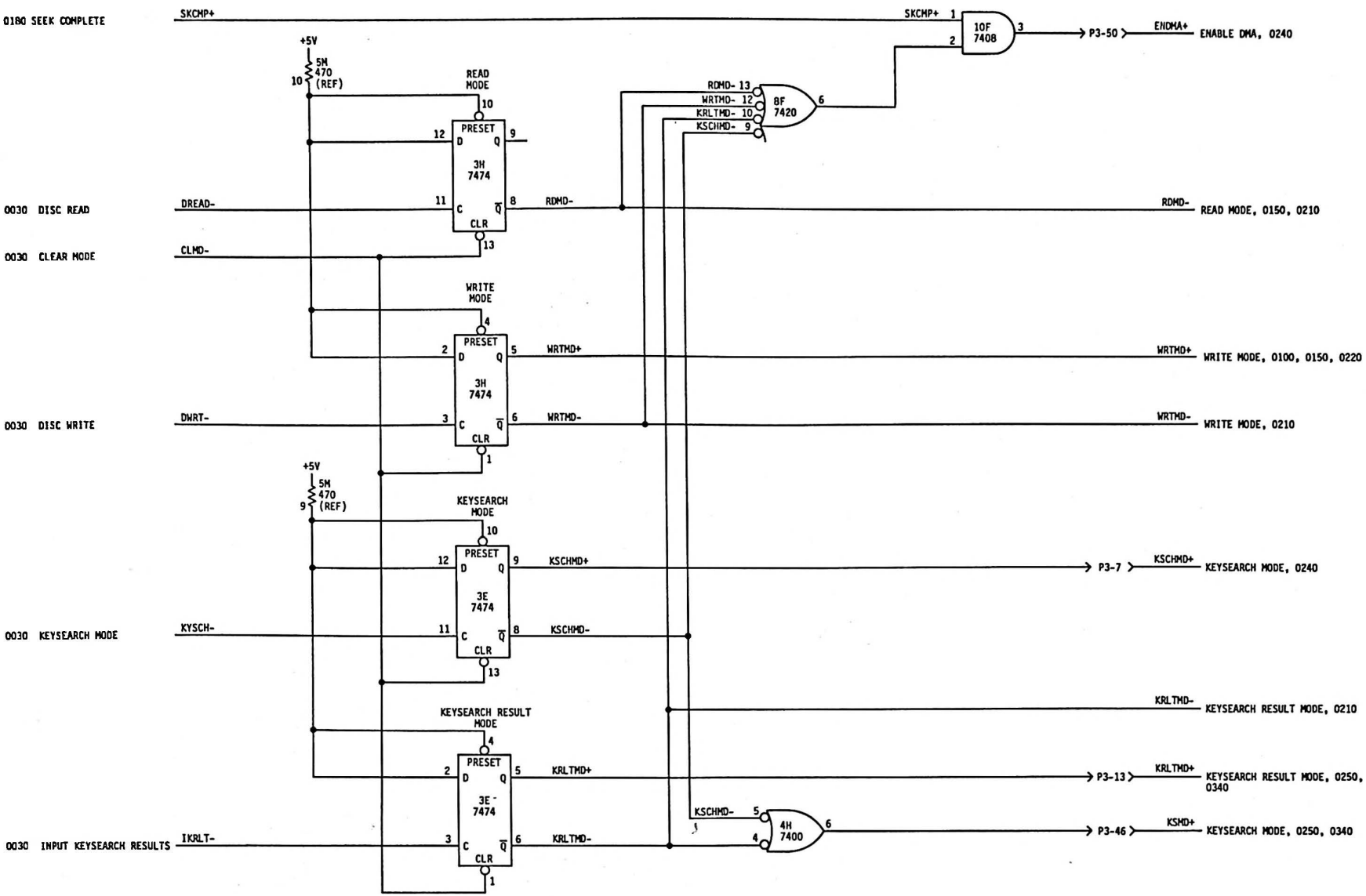

PG 1v I/O CONT REG 1
PG 1v I/O CONT REG 2
PG 1v I/O CONT REG 3
IO1X-
IO2X-
IO3X-
P1-B31
P1-A31
P1-B61
1F 7404
3F 7410
CONTROL DECODER 1E 7442
+5V
R4 680
C21 330pf
2E 7404
DOXX-
DATA OUT CONTROL, 0020
COXX-
CONTROL OUT, 0020
0010 ADDRESS ENABLE
0020 CONTROL OUT
0020 DATA OUT CONTROL
PG 1v MASTER RESET
ADEN-
COXX-
DOXX-
MRST-
P1-B44
3N 7402
2C 74H08
2D 7404
DAXX+
DEVICE ADDRESS DETECT, 0010
5M 470
CONNECT
PRESET
2M 7474
CLR
1M 7400
1K 7404
STRB+
STROBE, 0030
BMRST-
MASTER RESET, 0010, 0030, 0060

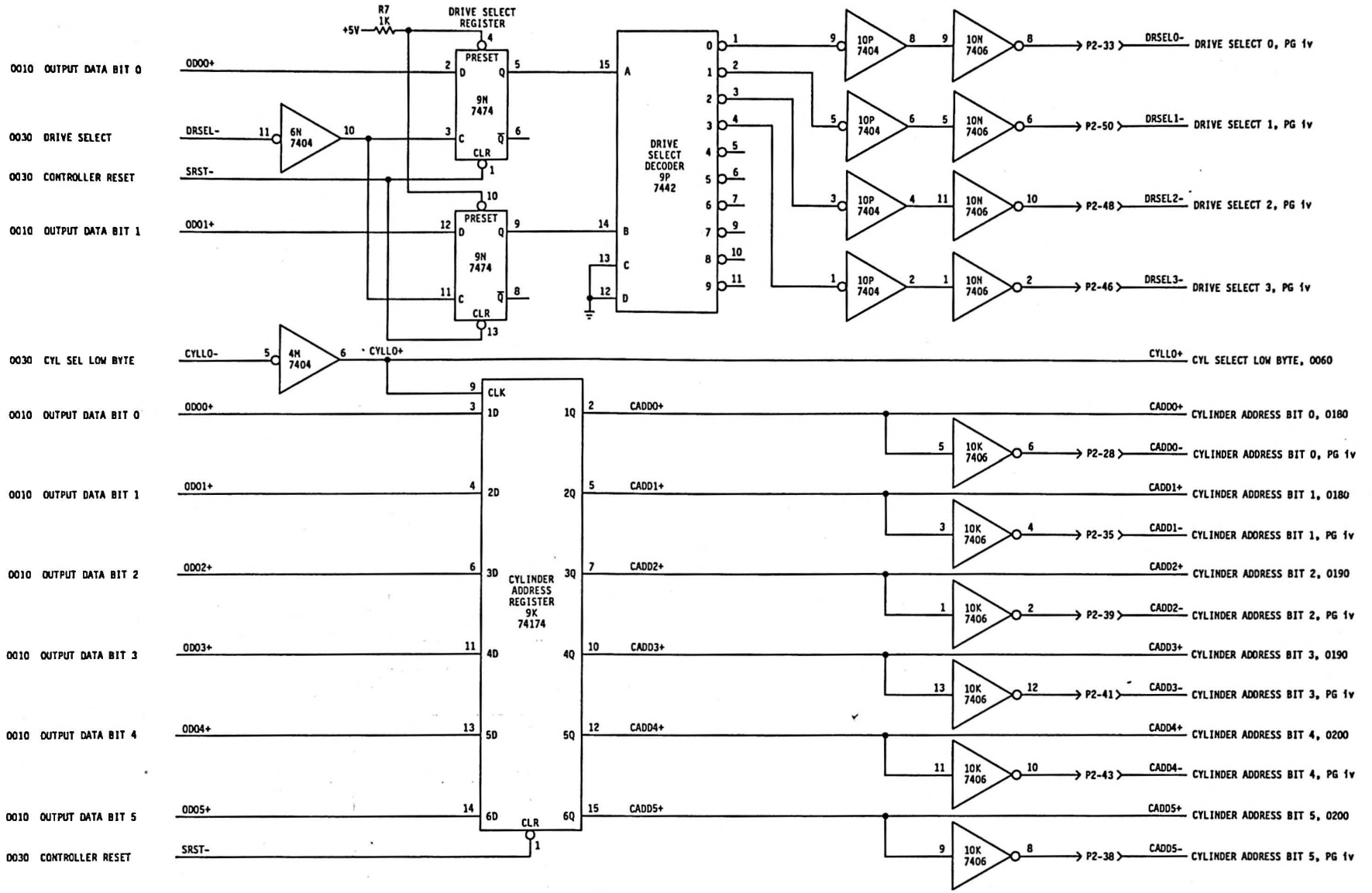


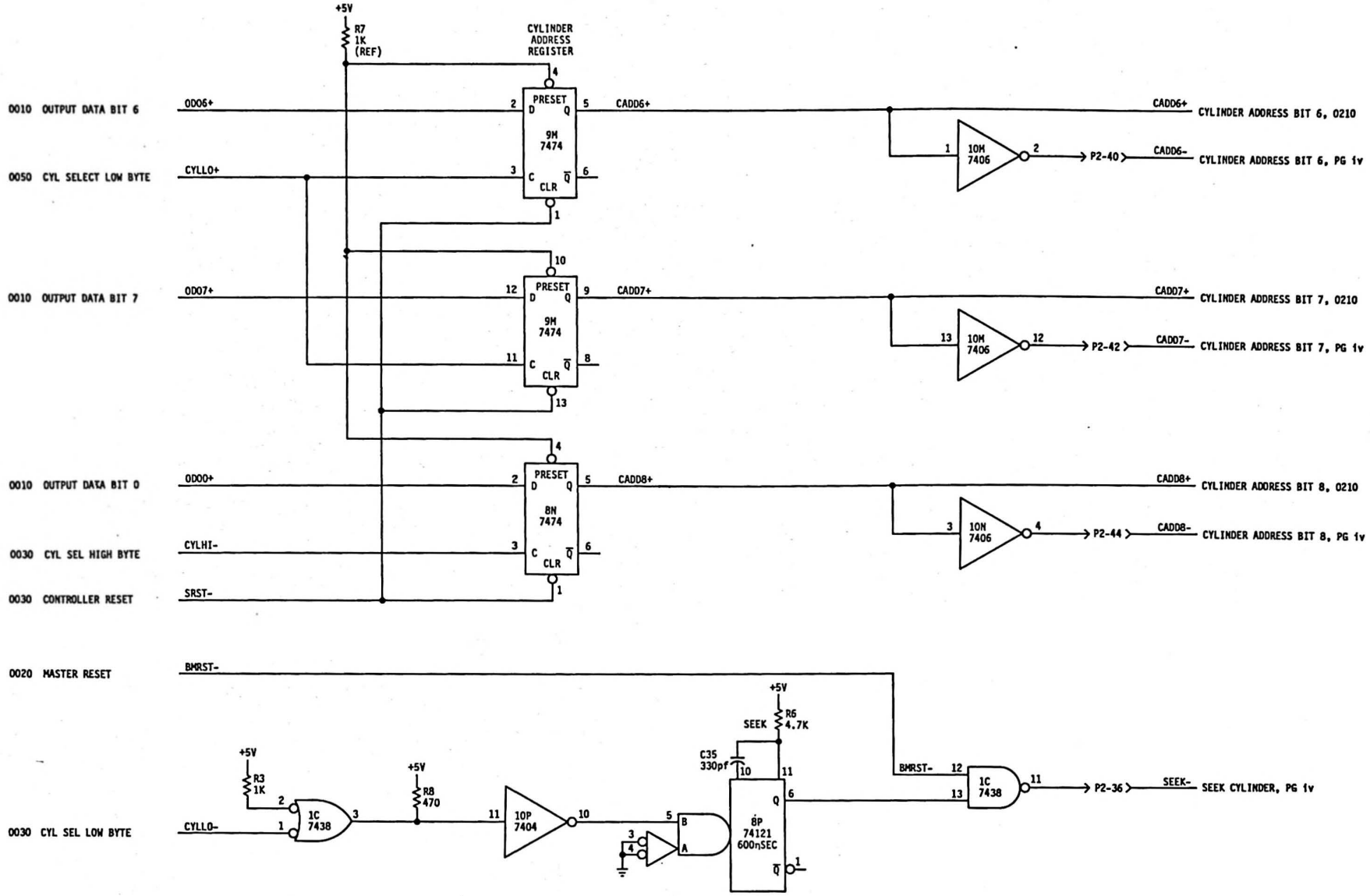
LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

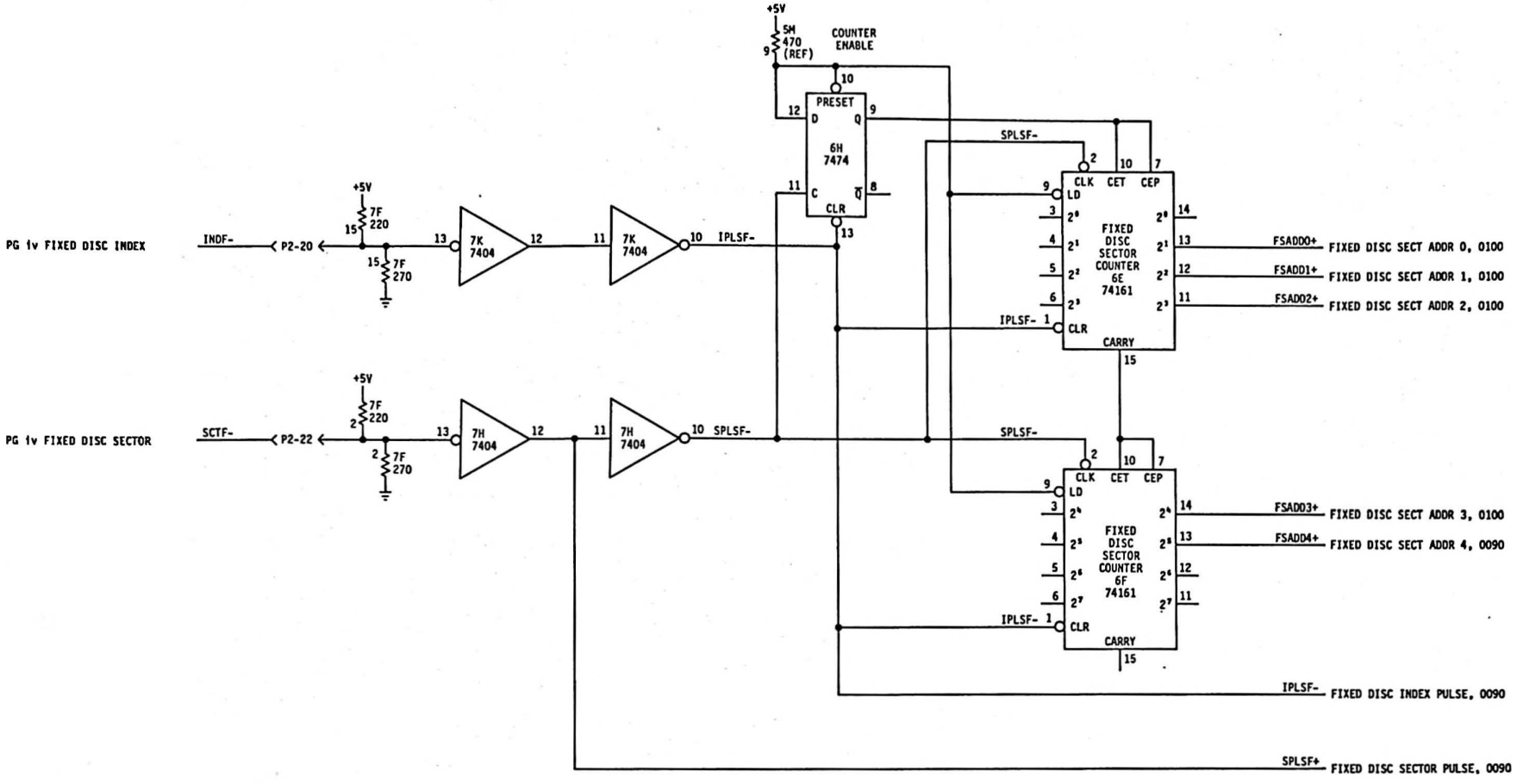
FUNCTION DECODING

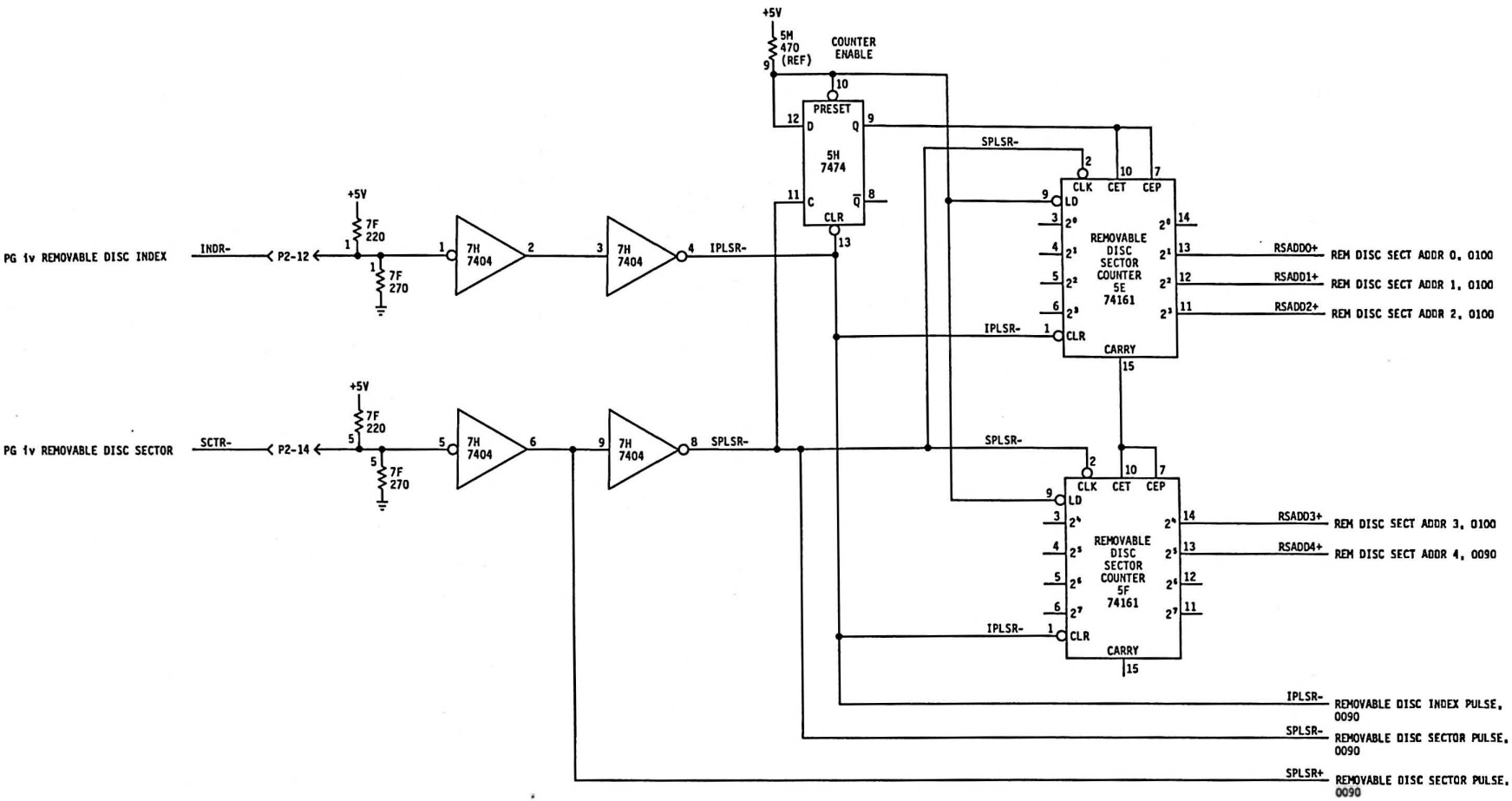
DISC CONTROL LOGIC BOARD
0030

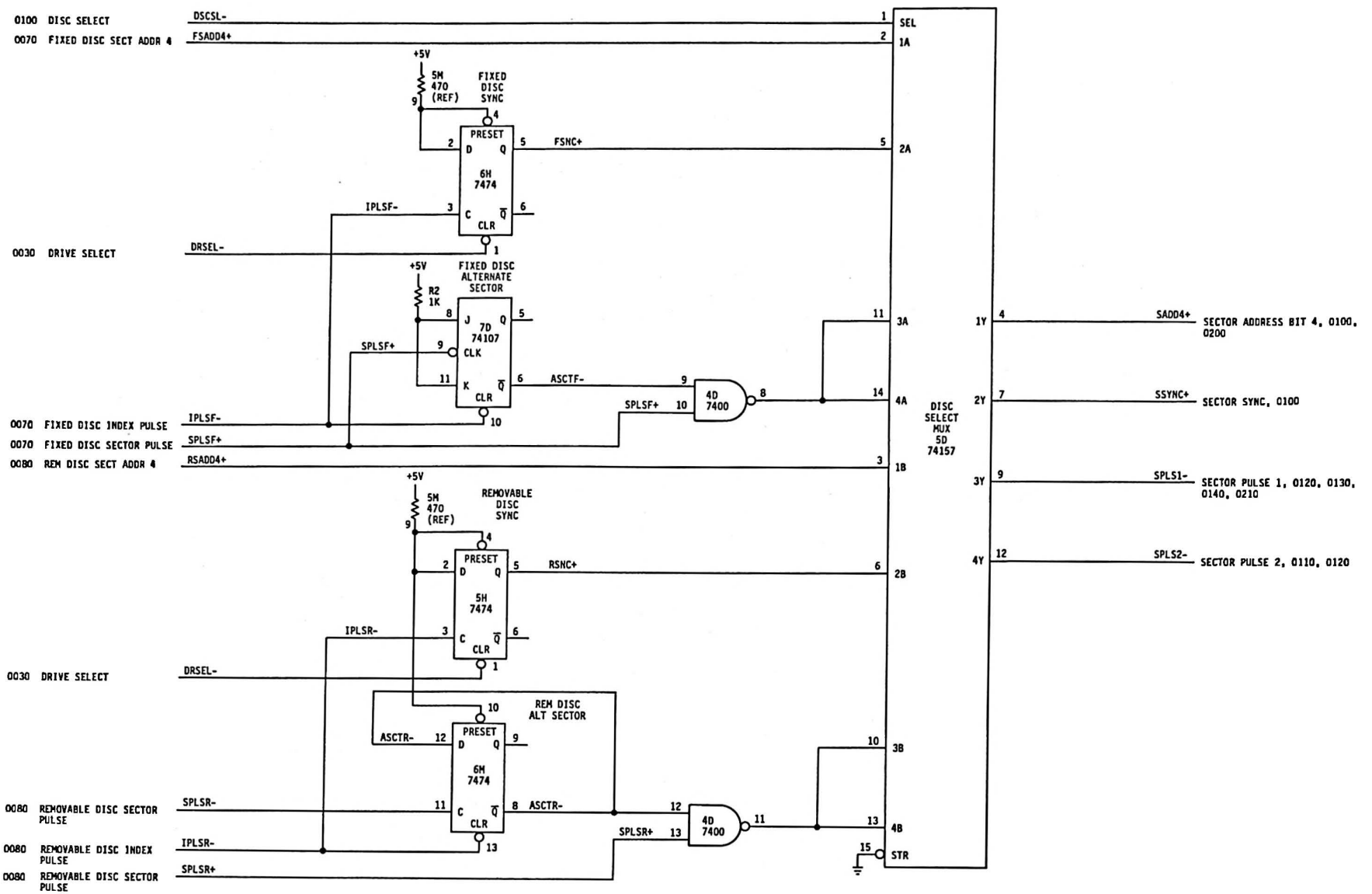

0180 SEEK COMPLETE
SKCMP+
SKCMP+ 1
2
10F 7408
3
P3-50
ENDMA+
ENABLE DMA, 0240
+5V
5M 470 (REF)
10
READ MODE
10
PRESET
12 D Q 9
3H 7474
11 C Q 8
CLR
13
RDMD- 13
WRTMD- 12
KRLTMD- 10
KSCHMD- 9
8F 7420
6
0030 DISC READ
DREAD-
RDMD-
RDMD-
READ MODE, 0150, 0210
0030 CLEAR MODE
CLMD-
WRITE MODE
4
PRESET
2 D Q 5
3H 7474
WRTMD+
WRTMD+
WRITE MODE, 0100, 0150, 0220
0030 DISC WRITE
DWRT-
3 C Q 6
WRTMD-
WRTMD-
WRITE MODE, 0210
CLR
1
+5V
5M 470 (REF)
9
KEYSEARCH MODE
10
PRESET
12 D Q 9
3E 7474
KSCHMD+
P3-7
KSCHMD+
KEYSEARCH MODE, 0240
0030 KEYSEARCH MODE
KYSCH-
11 C Q 8
KSCHMD-
CLR
13
KRLTMD-
KEYSEARCH RESULT MODE, 0210
KEYSEARCH RESULT MODE
4
PRESET
2 D Q 5
3E 7474
KRLTMD+
P3-13
KRLTMD+
KEYSEARCH RESULT MODE, 0250, 0340
KSCHMD- 5
4H 7400
6
P3-46
KSMD+
KEYSEARCH MODE, 0250, 0340
0030 INPUT KEYSEARCH RESULTS
IKRLT-
3 C Q 6
KRLTMD-
CLR
1


0010 OUTPUT DATA BIT 0
0030 DRIVE SELECT
0030 CONTROLLER RESET
0010 OUTPUT DATA BIT 1
0030 CYL SEL LOW BYTE
0010 OUTPUT DATA BIT 0
0010 OUTPUT DATA BIT 1
0010 OUTPUT DATA BIT 2
0010 OUTPUT DATA BIT 3
0010 OUTPUT DATA BIT 4
0010 OUTPUT DATA BIT 5
0030 CONTROLLER RESET
R7 1K
+5V
DRIVE SELECT REGISTER
PRESET
9N 7474
CLR
6N 7404
4M 7404
DRIVE SELECT DECODER 9P 7442
10P 7404
10N 7406
10K 7406
CLK
CYLINDER ADDRESS REGISTER 9K 74174
ODD0+
DRSEL-
SRST-
ODD1+
CYLLO-
CYLLO+
ODD2+
ODD3+
ODD4+
ODD5+
CADD0+
CADD1+
CADD2+
CADD3+
CADD4+
CADD5+
DRSEL0-
DRSEL1-
DRSEL2-
DRSEL3-
P2-33
P2-50
P2-48
P2-46
P2-28
P2-35
P2-39
P2-41
P2-43
P2-38
DRIVE SELECT 0, PG 1v
DRIVE SELECT 1, PG 1v
DRIVE SELECT 2, PG 1v
DRIVE SELECT 3, PG 1v
CYL SELECT LOW BYTE, 0060
CYLINDER ADDRESS BIT 0, 0180
CYLINDER ADDRESS BIT 0, PG 1v
CYLINDER ADDRESS BIT 1, 0180
CYLINDER ADDRESS BIT 1, PG 1v
CYLINDER ADDRESS BIT 2, 0190
CYLINDER ADDRESS BIT 2, PG 1v
CYLINDER ADDRESS BIT 3, 0190
CYLINDER ADDRESS BIT 3, PG 1v
CYLINDER ADDRESS BIT 4, 0200
CYLINDER ADDRESS BIT 4, PG 1v
CYLINDER ADDRESS BIT 5, 0200
CYLINDER ADDRESS BIT 5, PG 1v


+5V
R7
1K
(REF)
CYLINDER ADDRESS REGISTER
0010 OUTPUT DATA BIT 6
ODO6+
PRESET
D Q
9M
7474
C CLR
CLR
CADD6+
CADD6+
CYLINDER ADDRESS BIT 6, 0210
10M
7406
P2-40
CADD6-
CYLINDER ADDRESS BIT 6, PG 1v
0050 CYL SELECT LOW BYTE
CYLLO+
0010 OUTPUT DATA BIT 7
ODO7+
CADD7+
CADD7+
CYLINDER ADDRESS BIT 7, 0210
10M
7406
P2-42
CADD7-
CYLINDER ADDRESS BIT 7, PG 1v
0010 OUTPUT DATA BIT 0
ODO0+
8N
7474
CADD8+
CADD8+
CYLINDER ADDRESS BIT 8, 0210
10N
7406
P2-44
CADD8-
CYLINDER ADDRESS BIT 8, PG 1v
0030 CYL SEL HIGH BYTE
CYLHI-
0030 CONTROLLER RESET
SRST-
0020 MASTER RESET
BMRST-
+5V
R6
4.7K
SEEK
C35
330pf
+5V
R3
1K
+5V
R8
470
0030 CYL SEL LOW BYTE
CYLLO-
1C
7438
10P
7404
8P
74121
600nSEC
BMRST-
1C
7438
P2-36
SEEK-
SEEK CYLINDER, PG 1v


+5V
5M
470
(REF)
COUNTER
ENABLE
PRESET
6H
7474
SPLSF-
FIXED
DISC
SECTOR
COUNTER
6E
74161
FIXED
DISC
SECTOR
COUNTER
6F
74161
CLK
CET
CEP
LD
CLR
CARRY
PG fv FIXED DISC INDEX
INDF-
P2-20
7F
220
7F
270
7K
7404
IPLSF-
PG fv FIXED DISC SECTOR
SCTF-
P2-22
7H
7404
SPLSF-
FSADD0+
FIXED DISC SECT ADDR 0, 0100
FSADD1+
FIXED DISC SECT ADDR 1, 0100
FSADD2+
FIXED DISC SECT ADDR 2, 0100
FSADD3+
FIXED DISC SECT ADDR 3, 0100
FSADD4+
FIXED DISC SECT ADDR 4, 0090
IPLSF-
FIXED DISC INDEX PULSE, 0090
SPLSF+
FIXED DISC SECTOR PULSE, 0090


+5V
5M
470
(REF)
COUNTER
ENABLE
PRESET
5H
7474
SPLSR-
REMOVABLE
DISC
SECTOR
COUNTER
5E
74161
IPLSR-
CARRY
RSADD0+
REM DISC SECT ADDR 0, 0100
RSADD1+
REM DISC SECT ADDR 1, 0100
RSADD2+
REM DISC SECT ADDR 2, 0100
PG 1v REMOVABLE DISC INDEX
INDR-
P2-12
7F
220
7F
270
7H
7404
IPLSR-
PG 1v REMOVABLE DISC SECTOR
SCTR-
P2-14
SPLSR-
REMOVABLE
DISC
SECTOR
COUNTER
5F
74161
RSADD3+
REM DISC SECT ADDR 3, 0100
RSADD4+
REM DISC SECT ADDR 4, 0090
IPLSR-
REMOVABLE DISC INDEX PULSE, 0090
SPLSR-
REMOVABLE DISC SECTOR PULSE, 0090
SPLSR+
REMOVABLE DISC SECTOR PULSE, 0090



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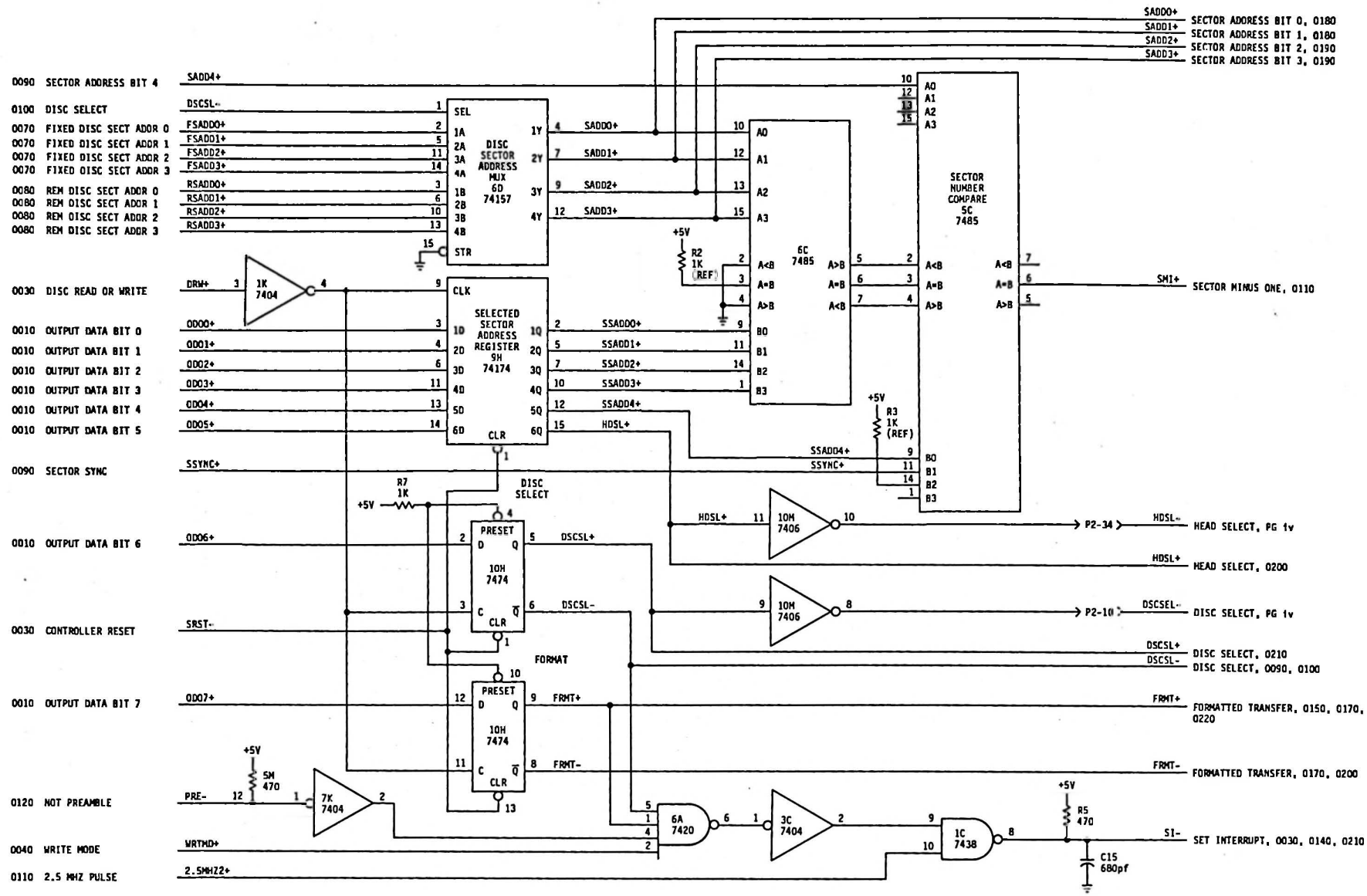
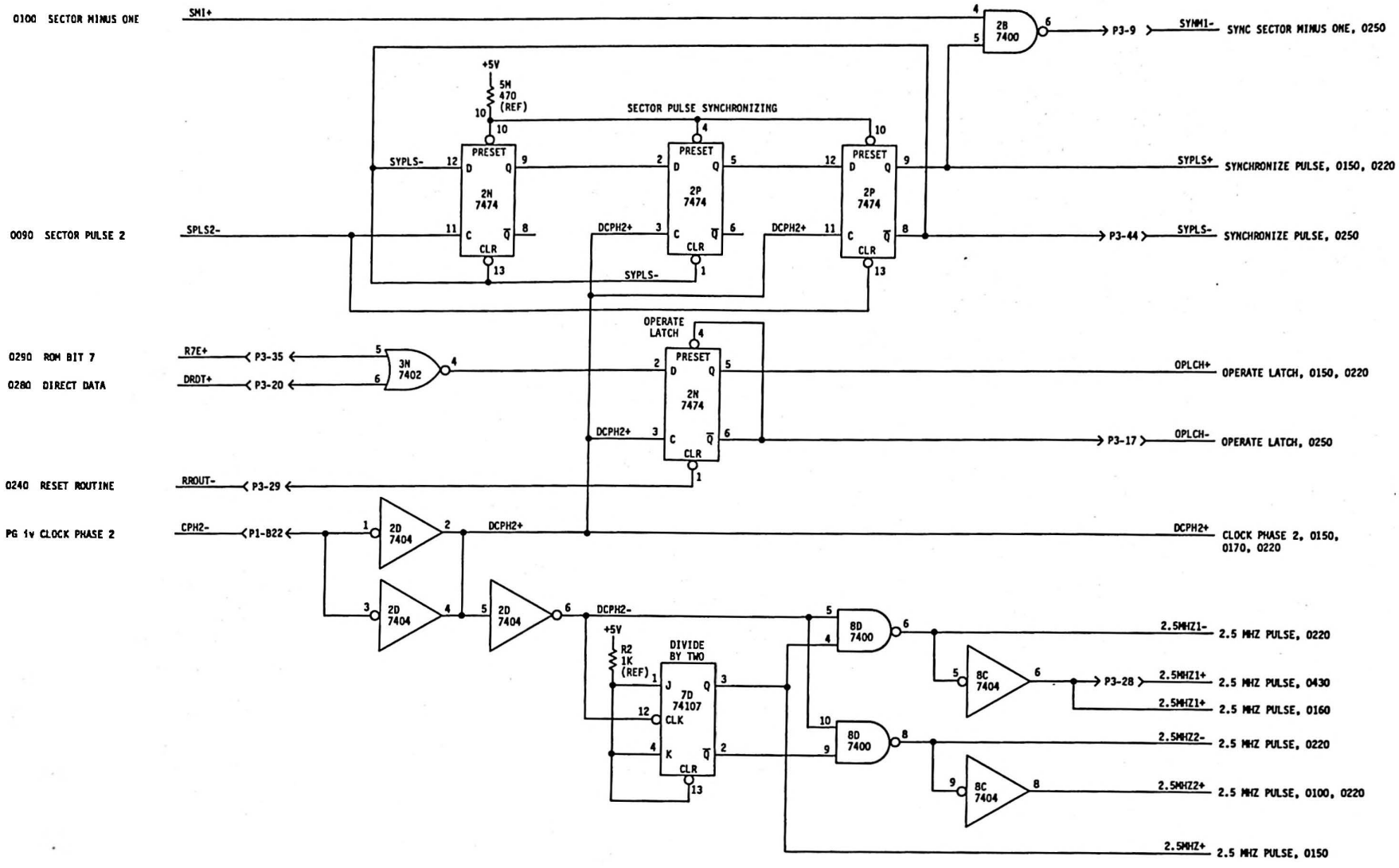
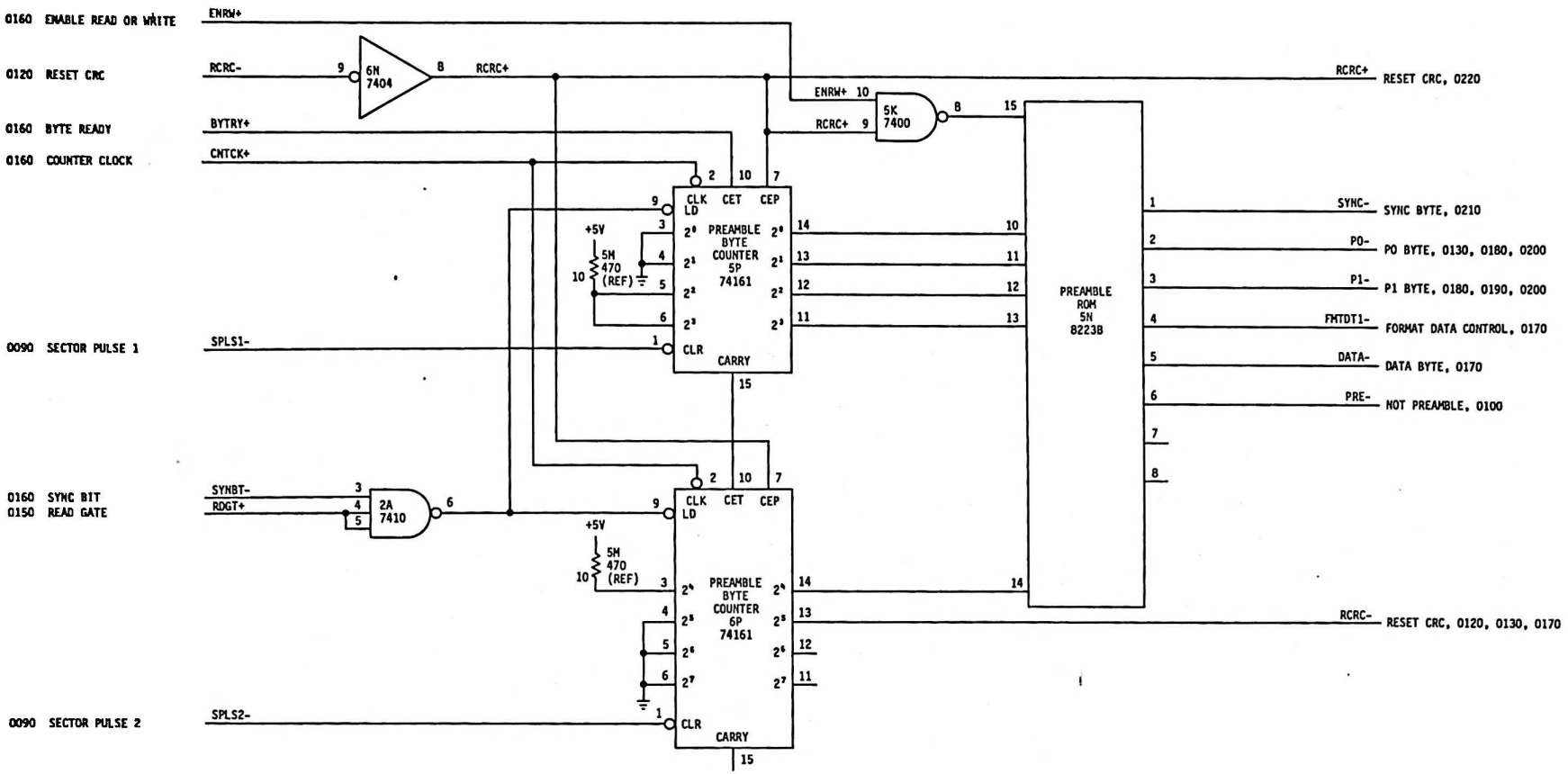
DMA/DISC STORAGE UNIT CONTROLLER

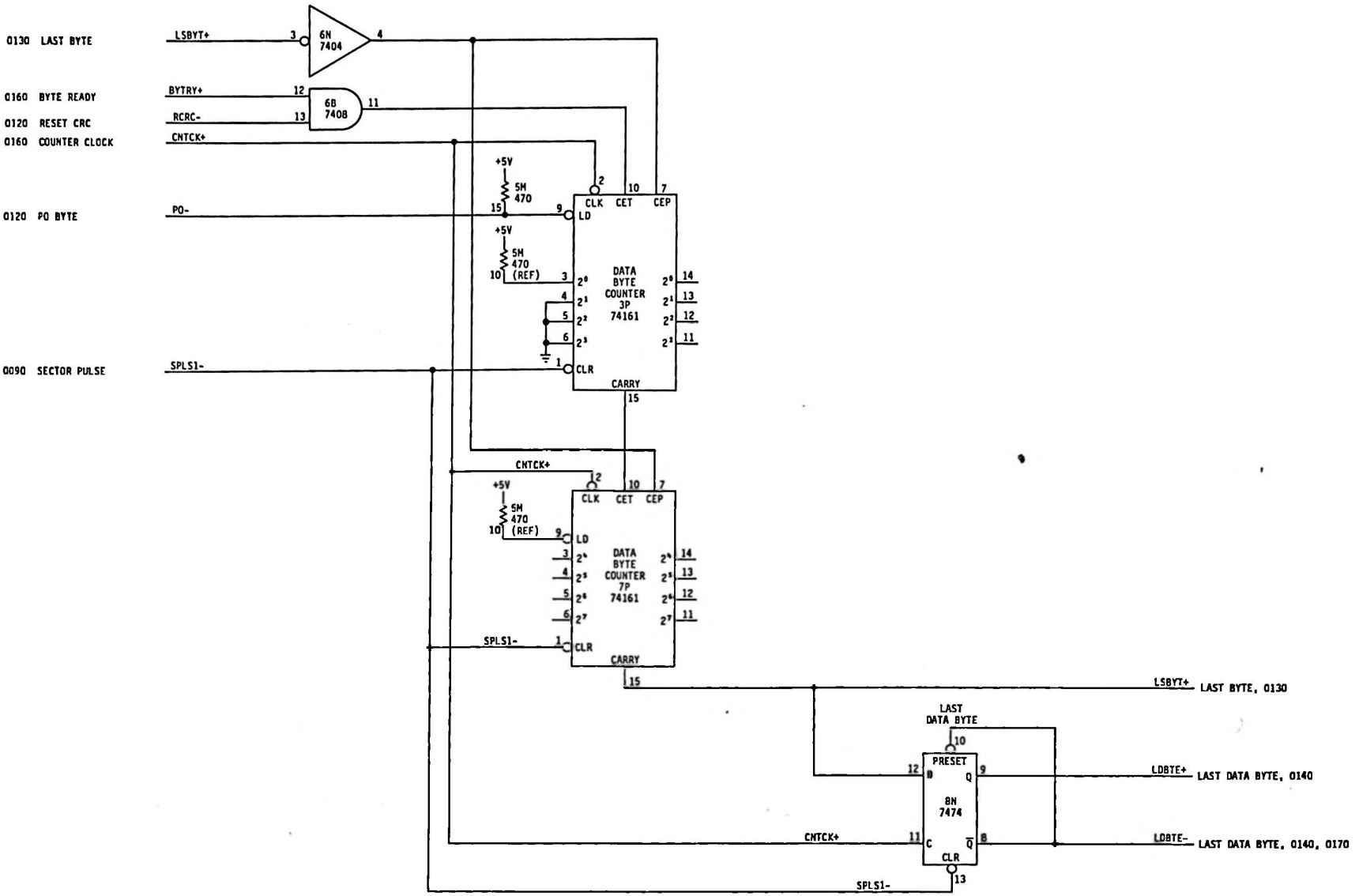
DISC SELECT

DISC CONTROL LOGIC BOARD
0090


SADD0+ SECTOR ADDRESS BIT 0, 0180
SADD1+ SECTOR ADDRESS BIT 1, 0180
SADD2+ SECTOR ADDRESS BIT 2, 0190
SADD3+ SECTOR ADDRESS BIT 3, 0190
0090 SECTOR ADDRESS BIT 4
SADD4+
0100 DISC SELECT
DSCSL-
0070 FIXED DISC SECT ADDR 0
FSADD0+
0070 FIXED DISC SECT ADDR 1
FSADD1+
0070 FIXED DISC SECT ADDR 2
FSADD2+
0070 FIXED DISC SECT ADDR 3
FSADD3+
0080 REM DISC SECT ADDR 0
RSADD0+
0080 REM DISC SECT ADDR 1
RSADD1+
0080 REM DISC SECT ADDR 2
RSADD2+
0080 REM DISC SECT ADDR 3
RSADD3+
DISC SECTOR ADDRESS MUX 6D 74157
SEL
1A
2A
3A
4A
1B
2B
3B
4B
STR
1Y
2Y
3Y
4Y
SADD0+
SADD1+
SADD2+
SADD3+
SECTOR NUMBER COMPARE 5C 7485
A0
A1
A2
A3
A<B
A=B
A>B
6C 7485
B0
B1
B2
B3
+5V
R2 1K (REF)
R3 1K (REF)
0030 DISC READ OR WRITE
DRW+
1K 7404
SELECTED SECTOR ADDRESS REGISTER 9H 74174
CLK
CLR
1D
2D
3D
4D
5D
6D
1Q
2Q
3Q
4Q
5Q
6Q
SSADD0+
SSADD1+
SSADD2+
SSADD3+
SSADD4+
HDSL+
SMI+ SECTOR MINUS ONE, 0110
0010 OUTPUT DATA BIT 0
OD00+
0010 OUTPUT DATA BIT 1
OD01+
0010 OUTPUT DATA BIT 2
OD02+
0010 OUTPUT DATA BIT 3
OD03+
0010 OUTPUT DATA BIT 4
OD04+
0010 OUTPUT DATA BIT 5
OD05+
0090 SECTOR SYNC
SSYNC+
R7 1K
DISC SELECT
0010 OUTPUT DATA BIT 6
OD06+
PRESET
D
Q
C
10H 7474
HDSL+ 11 10H 7406 10 P2-34 HDSL- HEAD SELECT, PG 1v
HDSL+ HEAD SELECT, 0200
DSCSL+
DSCSL-
9 10H 7406 8 P2-10 DSCSEL- DISC SELECT, PG 1v
0030 CONTROLLER RESET
SRST-
DSCSL+ DISC SELECT, 0210
DSCSL- DISC SELECT, 0090, 0100
FORMAT
0010 OUTPUT DATA BIT 7
OD07+
FRMT+
FRMT+ FORMATTED TRANSFER, 0150, 0170, 0220
FRMT-
FRMT- FORMATTED TRANSFER, 0170, 0200
5M 470
0120 NOT PREAMBLE
PRE-
7K 7404
0040 WRITE MODE
WRTMD+
0110 2.5 MHZ PULSE
2.5MHZ2+
6A 7420
3C 7404
1C 7438
R5 470
SI- SET INTERRUPT, 0030, 0140, 0210
C15 680pf


0100 SECTOR MINUS ONE
SMI+
2B 7400
P3-9
SYMM1-
SYNC SECTOR MINUS ONE, 0250
+5V
5M 470 (REF)
SECTOR PULSE SYNCHRONIZING
PRESET
2N 7474
2P 7474
SYPLS-
SYPLS+
SYNCHRONIZE PULSE, 0150, 0220
0090 SECTOR PULSE 2
SPLS2-
DCPH2+
P3-44
SYPLS-
SYNCHRONIZE PULSE, 0250
OPERATE LATCH
0290 ROM BIT 7
0280 DIRECT DATA
R7E+
DRDT+
P3-35
P3-20
3M 7402
OPLCH+
OPERATE LATCH, 0150, 0220
P3-17
OPLCH-
OPERATE LATCH, 0250
0240 RESET ROUTINE
RROUT-
P3-29
PG 1v CLOCK PHASE 2
CPH2-
P1-B22
2D 7404
DCPH2+
CLOCK PHASE 2, 0150, 0170, 0220
DCPH2-
DIVIDE BY TWO
R2 1K (REF)
7D 74107
CLK
8D 7400
8C 7404
2.5MHZ1-
2.5 MHZ PULSE, 0220
P3-28
2.5MHZ1+
2.5 MHZ PULSE, 0430
2.5 MHZ PULSE, 0160
2.5MHZ2-
2.5 MHZ PULSE, 0220
2.5MHZ2+
2.5 MHZ PULSE, 0100, 0220
2.5MHZ+
2.5 MHZ PULSE, 0150

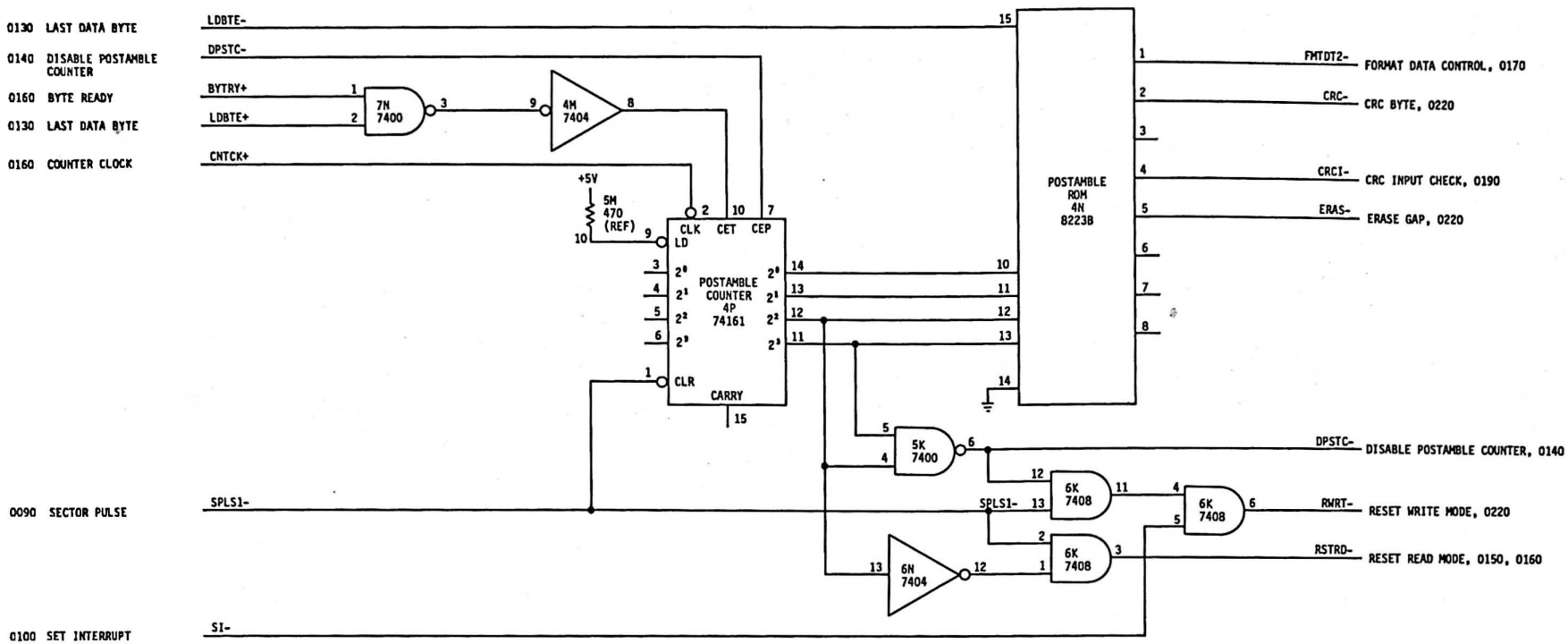

0160 ENABLE READ OR WRITE
ENRW+
0120 RESET CRC
RCRC-
9
6N
7404
8
RCRC+
0160 BYTE READY
BYTRY+
0160 COUNTER CLOCK
CNTCK+
ENRW+ 10
RCRC+ 9
5K
7400
8
15
RCRC+
RESET CRC, 0220
2
10
7
CLK
CET
CEP
LD
9
+5V
3
4
5
6
10
5M
470
(REF)
PREAMBLE
BYTE
COUNTER
5P
74161
14
13
12
11
10
11
12
13
1
CLR
CARRY
15
0090 SECTOR PULSE 1
SPLS1-
PREAMBLE
ROM
5N
8223B
1
SYNC-
SYNC BYTE, 0210
2
PO-
PO BYTE, 0130, 0180, 0200
3
P1-
P1 BYTE, 0180, 0190, 0200
4
FMTDT1-
FORMAT DATA CONTROL, 0170
5
DATA-
DATA BYTE, 0170
6
PRE-
NOT PREAMBLE, 0100
7
8
0160 SYNC BIT
0150 READ GATE
SYNBT-
RDGT+
3
4
5
2A
7410
6
2
10
7
CLK
CET
CEP
LD
9
+5V
5M
470
(REF)
10
PREAMBLE
BYTE
COUNTER
6P
74161
3
4
5
6
14
13
12
11
14
RCRC-
RESET CRC, 0120, 0130, 0170
1
CLR
CARRY
15
0090 SECTOR PULSE 2
SPLS2-

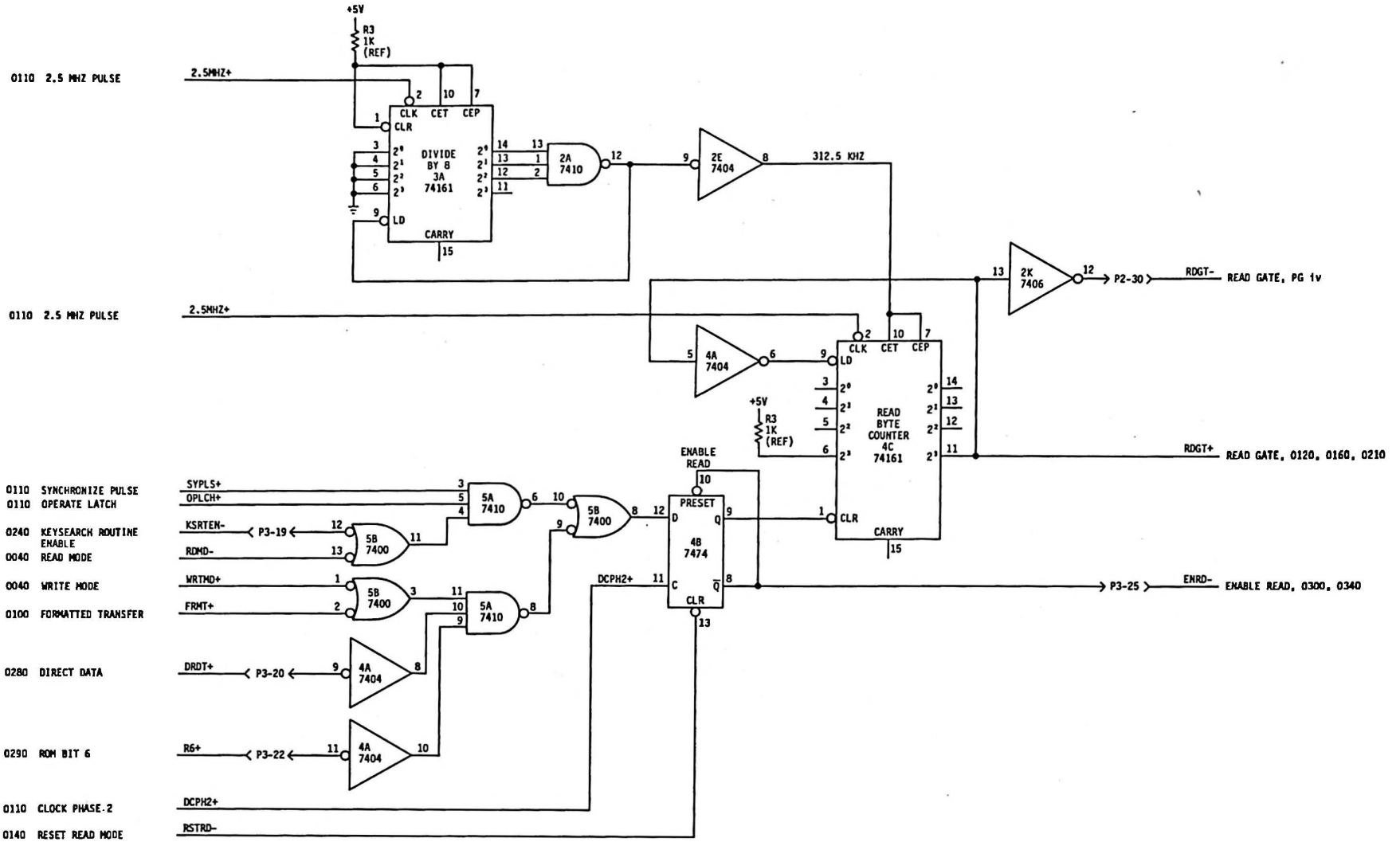


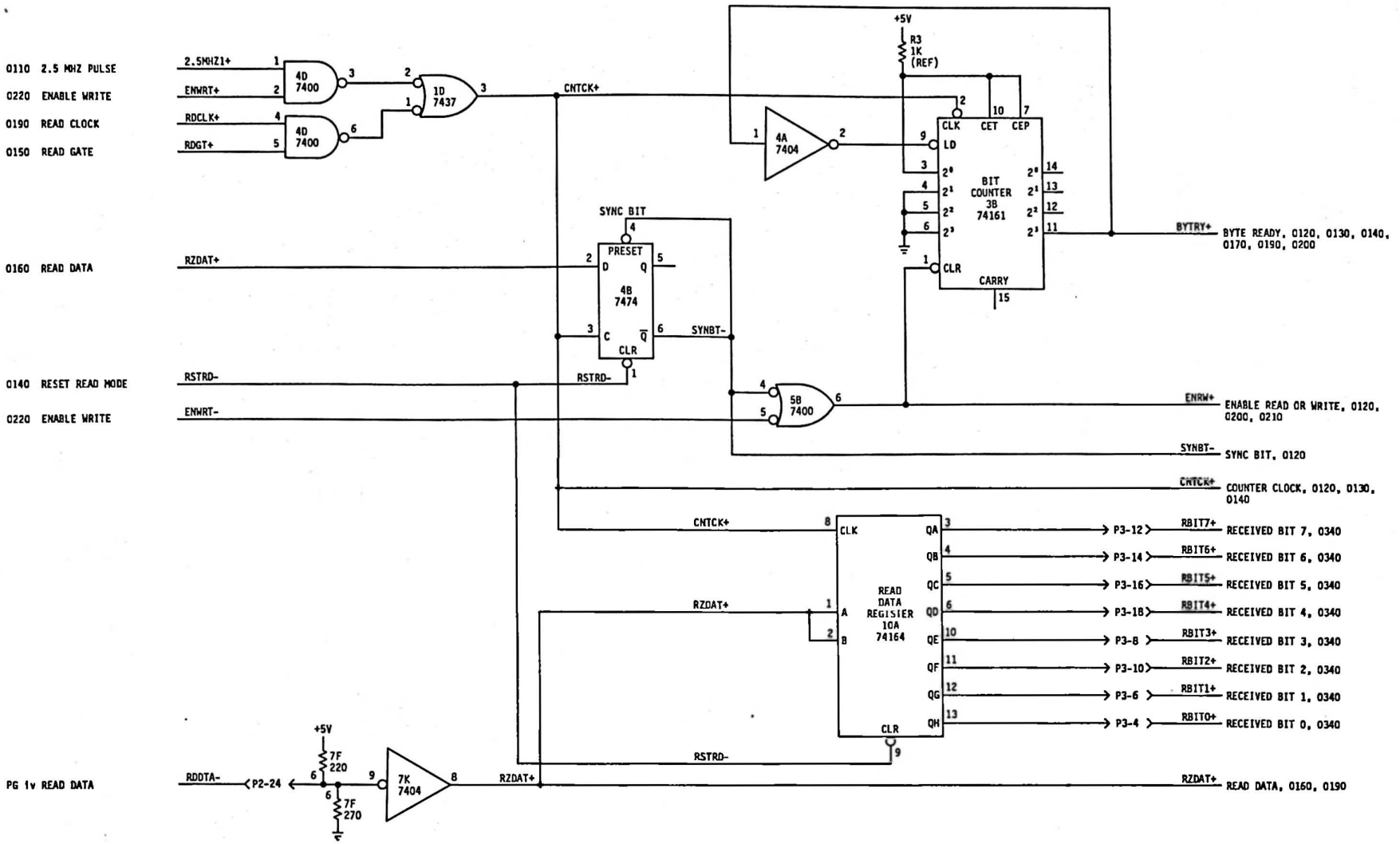
LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

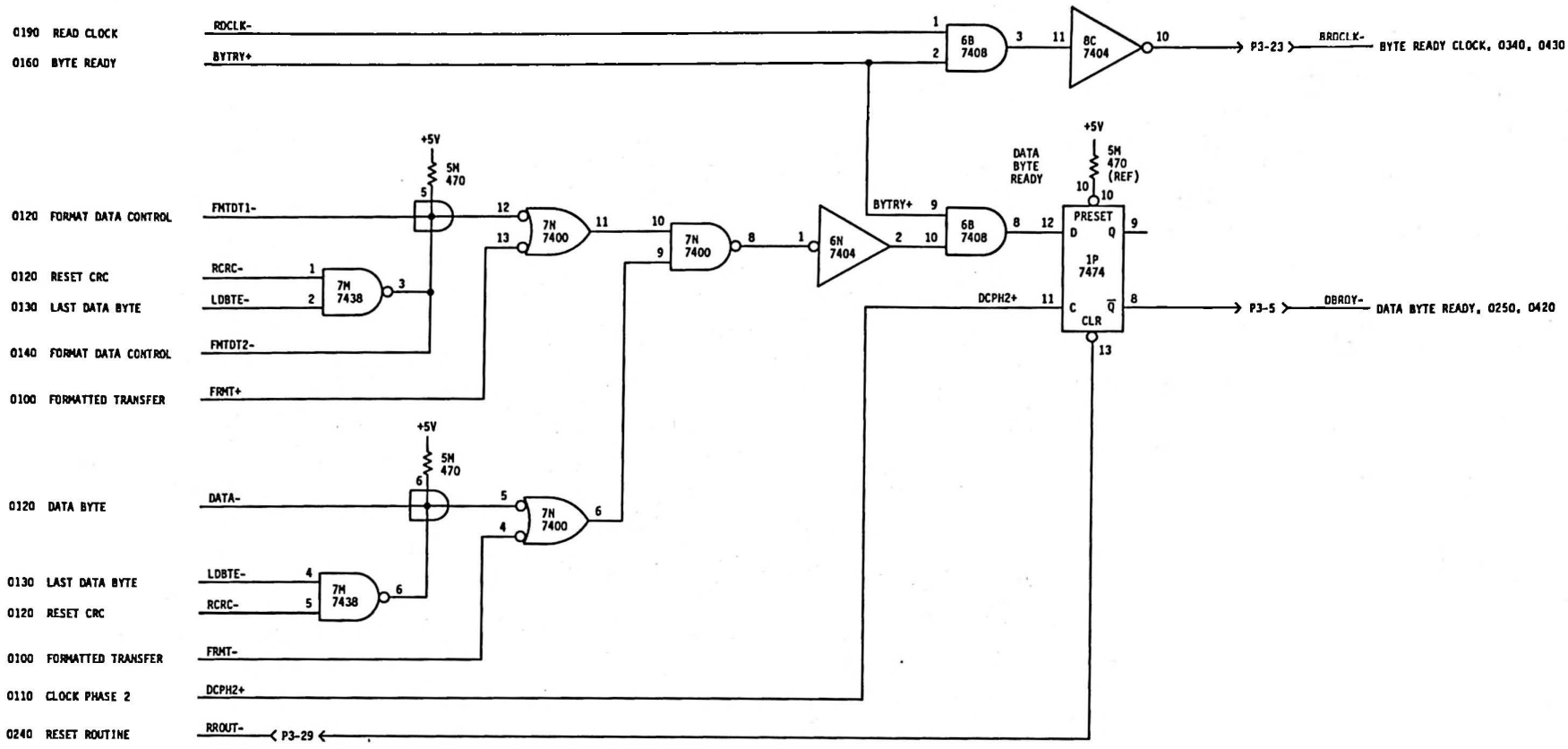
DATA BLOCK CONTROL

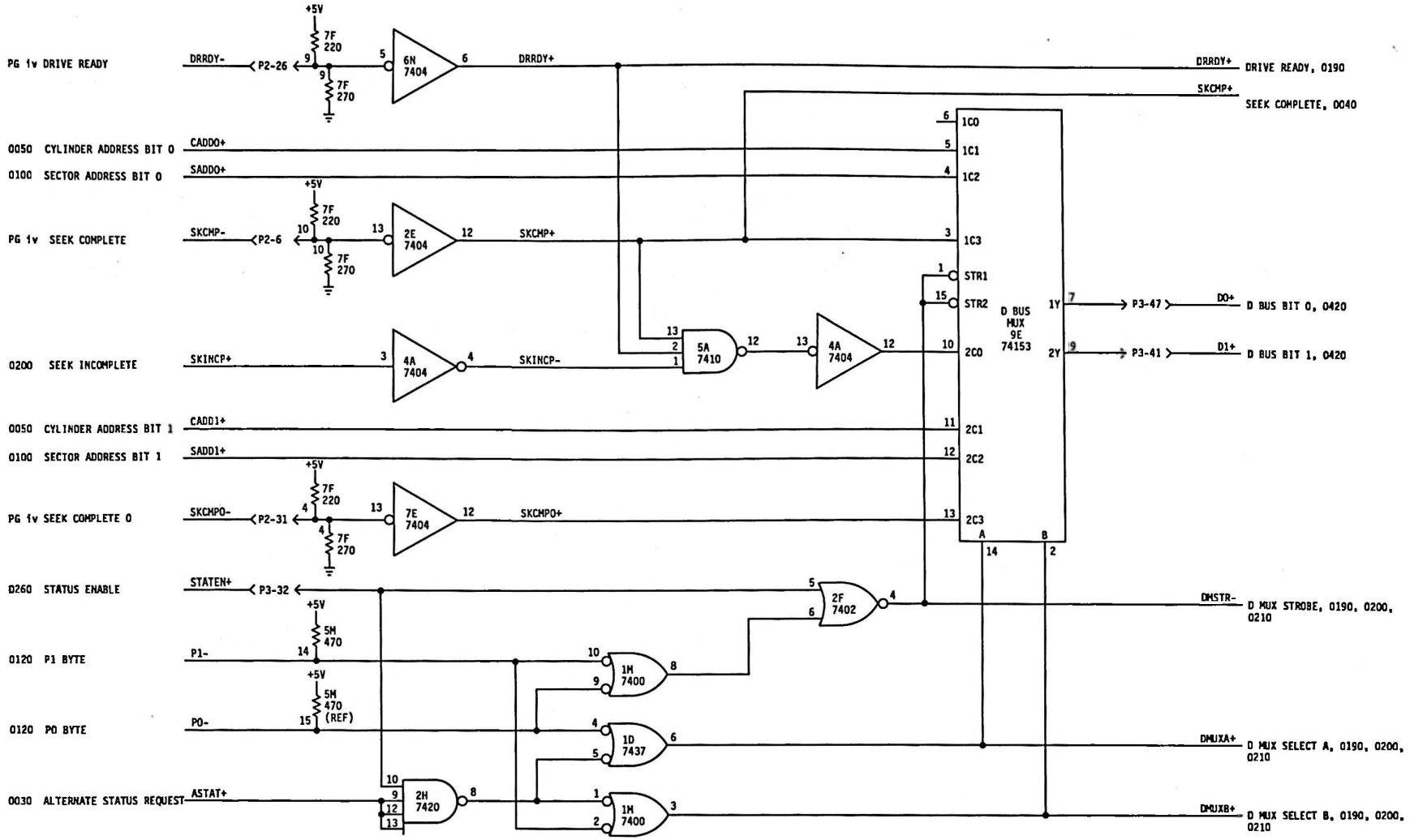
DISC CONTROL LOGIC BOARD
0130

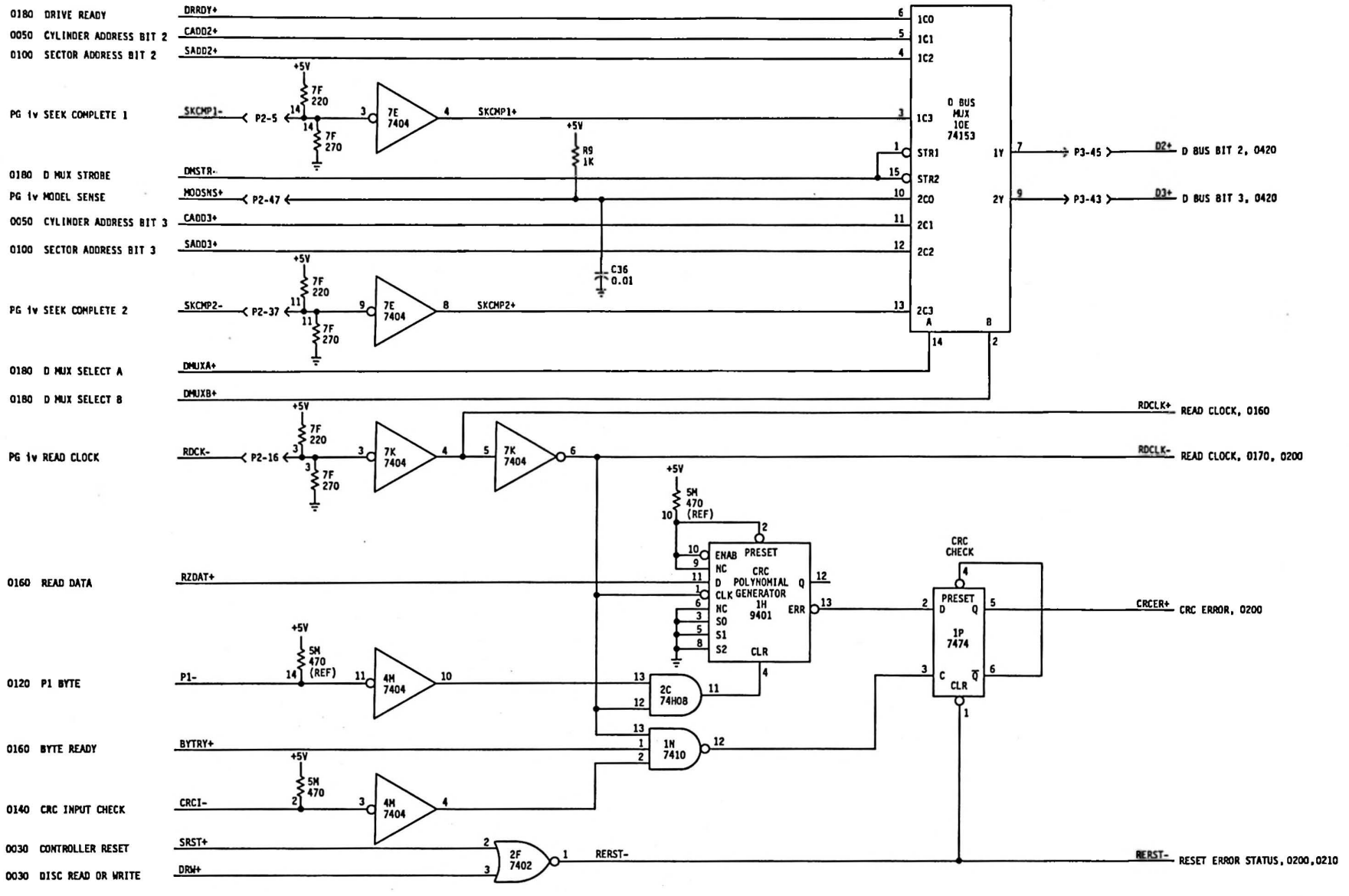

0130 LAST DATA BYTE
0140 DISABLE POSTAMBLE COUNTER
0160 BYTE READY
0130 LAST DATA BYTE
0160 COUNTER CLOCK
0090 SECTOR PULSE
0100 SET INTERRUPT
LDBTE-
DPSTC-
BYTRY+
LDBTE+
CNTCK+
SPLS1-
SI-
7N 7400
4M 7404
+5V
5M 470 (REF)
CLK CET CEP
LD
CLR
CARRY
POSTAMBLE COUNTER 4P 74161
POSTAMBLE ROM 4N 8223B
5K 7400
6K 7408
6K 7408
6K 7408
6N 7404
FMTDT2-
FORMAT DATA CONTROL, 0170
CRC-
CRC BYTE, 0220
CRCI-
CRC INPUT CHECK, 0190
ERAS-
ERASE GAP, 0220
DPSTC-
DISABLE POSTAMBLE COUNTER, 0140
RWRT-
RESET WRITE MODE, 0220
RSTRD-
RESET READ MODE, 0150, 0160


0110 2.5 MHZ PULSE
2.5MHZ+
+5V
R3
1K
(REF)
DIVIDE BY 8
3A
74161
CLK
CET
CEP
CLR
LD
CARRY
2A
7410
2E
7404
312.5 KHZ
2K
7406
P2-30
RDGT-
READ GATE, PG 1v
0110 2.5 MHZ PULSE
2.5MHZ+
4A
7404
READ BYTE COUNTER 4C
74161
RDGT+
READ GATE, 0120, 0160, 0210
ENABLE READ
PRESET
4B
7474
CLR
0110 SYNCHRONIZE PULSE
0110 OPERATE LATCH
SYPLS+
OPLCH+
5A
7410
5B
7400
0240 KEYSEARCH ROUTINE ENABLE
KSRTEN-
P3-19
0040 READ MODE
RDMD-
0040 WRITE MODE
WRTMD+
0100 FORMATTED TRANSFER
FRMT+
DCPH2+
P3-25
ENRD-
ENABLE READ, 0300, 0340
0280 DIRECT DATA
DRDT+
P3-20
0290 ROM BIT 6
R6+
P3-22
0110 CLOCK PHASE.2
DCPH2+
0140 RESET READ MODE
RSTRD-


0110 2.5 MHZ PULSE
0220 ENABLE WRITE
0190 READ CLOCK
0150 READ GATE
2.5MHZ1+
ENWRT+
RDCLK+
RDGT+
4D 7400
1D 7437
CNTCK+
+5V
R3 1K (REF)
4A 7404
BIT COUNTER 3B 74161
CLK
CET
CEP
LD
CLR
CARRY
BYTRY+
BYTE READY, 0120, 0130, 0140, 0170, 0190, 0200
0160 READ DATA
RZDAT+
SYNC BIT
PRESET
4B 7474
SYNBT-
0140 RESET READ MODE
0220 ENABLE WRITE
RSTRD-
ENWRT-
5B 7400
ENRW+
ENABLE READ OR WRITE, 0120, 0200, 0210
SYNC BIT, 0120
COUNTER CLOCK, 0120, 0130, 0140
READ DATA REGISTER 10A 74164
RBIT7+
RBIT6+
RBIT5+
RBIT4+
RBIT3+
RBIT2+
RBIT1+
RBIT0+
P3-12
P3-14
P3-16
P3-18
P3-8
P3-10
P3-6
P3-4
RECEIVED BIT 7, 0340
RECEIVED BIT 6, 0340
RECEIVED BIT 5, 0340
RECEIVED BIT 4, 0340
RECEIVED BIT 3, 0340
RECEIVED BIT 2, 0340
RECEIVED BIT 1, 0340
RECEIVED BIT 0, 0340
PG 1v READ DATA
RDDTA-
P2-24
7F 220
7F 270
7K 7404
RZDAT+
READ DATA, 0160, 0190


0190 READ CLOCK
0160 BYTE READY
RDCLK-
BYTRY+
6B 7408
8C 7404
P3-23
BRDCLK-
BYTE READY CLOCK, 0340, 0430
+5V
5M 470
0120 FORMAT DATA CONTROL
FMTDT1-
7N 7400
0120 RESET CRC
0130 LAST DATA BYTE
RCRC-
LDBTE-
7M 7438
0140 FORMAT DATA CONTROL
FMTDT2-
0100 FORMATTED TRANSFER
FRMT+
6N 7404
DATA BYTE READY
5M 470 (REF)
PRESET
1P 7474
CLR
DCPH2+
P3-5
DBRDY-
DATA BYTE READY, 0250, 0420
0120 DATA BYTE
DATA-
0130 LAST DATA BYTE
0120 RESET CRC
FRMT-
0100 FORMATTED TRANSFER
0110 CLOCK PHASE 2
0240 RESET ROUTINE
RROUT-
P3-29

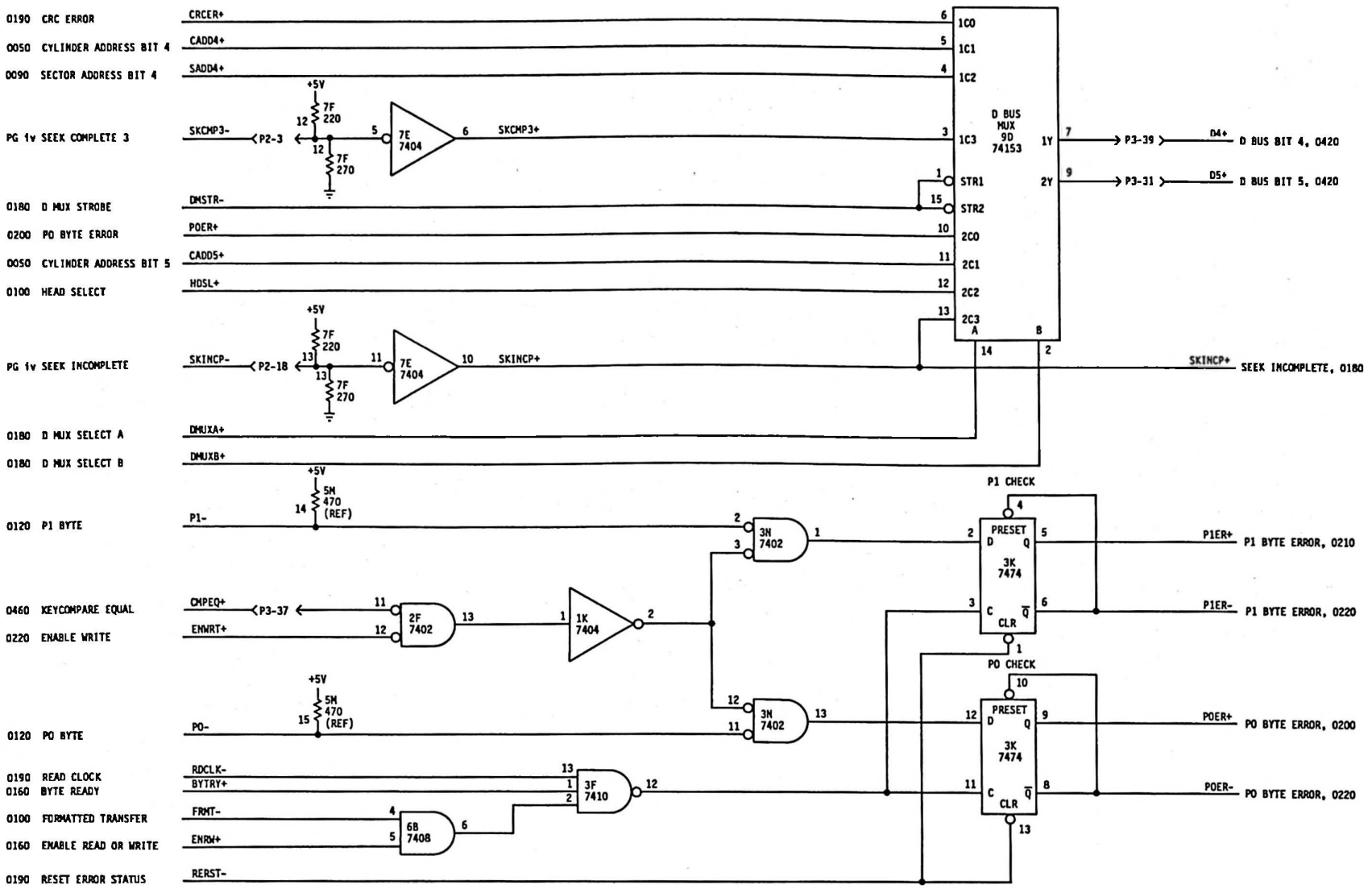

PG 1v DRIVE READY
DRRDY-
P2-26
+5V
7F 220
7F 270
6N 7404
DRRDY+
DRRDY+
DRIVE READY, 0190
SKCMP+
SEEK COMPLETE, 0040
0050 CYLINDER ADDRESS BIT 0
CADDO+
0100 SECTOR ADDRESS BIT 0
SADDO+
PG 1v SEEK COMPLETE
SKCMP-
P2-6
2E 7404
SKCMP+
0200 SEEK INCOMPLETE
SKINCP+
4A 7404
SKINCP-
5A 7410
4A 7404
0050 CYLINDER ADDRESS BIT 1
CADD1+
0100 SECTOR ADDRESS BIT 1
SADD1+
PG 1v SEEK COMPLETE 0
SKCMPO-
P2-31
7E 7404
SKCMPO+
1C0
1C1
1C2
1C3
STR1
STR2
2C0
2C1
2C2
2C3
D BUS MUX 9E 74153
1Y
2Y
P3-47
P3-41
DO+
D1+
D BUS BIT 0, 0420
D BUS BIT 1, 0420
D260 STATUS ENABLE
STATEN+
P3-32
2F 7402
DMSTR-
D MUX STROBE, 0190, 0200, 0210
0120 P1 BYTE
P1-
5M 470
1M 7400
0120 P0 BYTE
P0-
5M 470 (REF)
1D 7437
DMUXA+
D MUX SELECT A, 0190, 0200, 0210
0030 ALTERNATE STATUS REQUEST
ASTAT+
2H 7420
1M 7400
DMUXB+
D MUX SELECT B, 0190, 0200, 0210

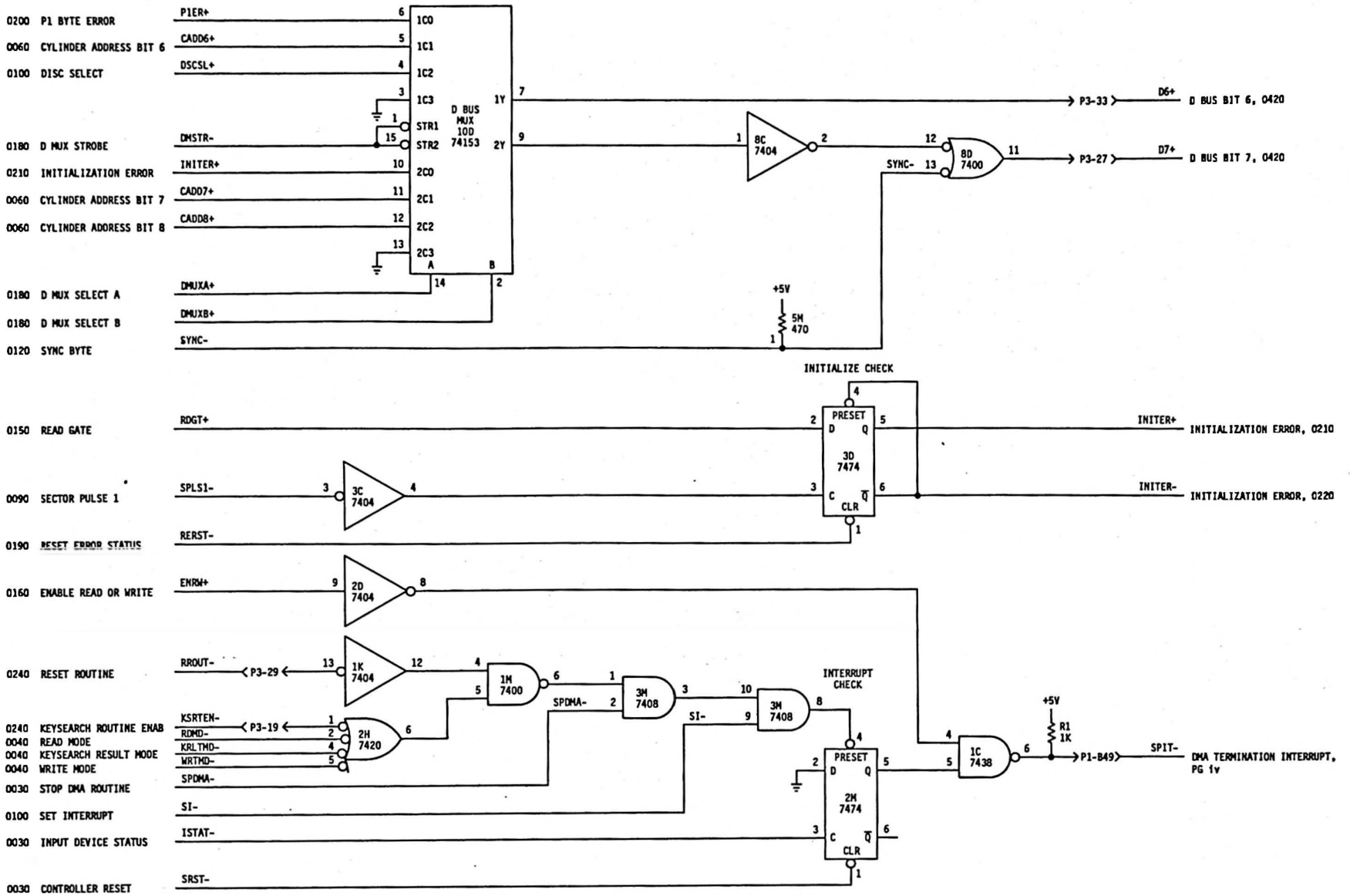


LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

D BUS BITS 2 AND 3

DISC CONTROL LOGIC BOARD
0190

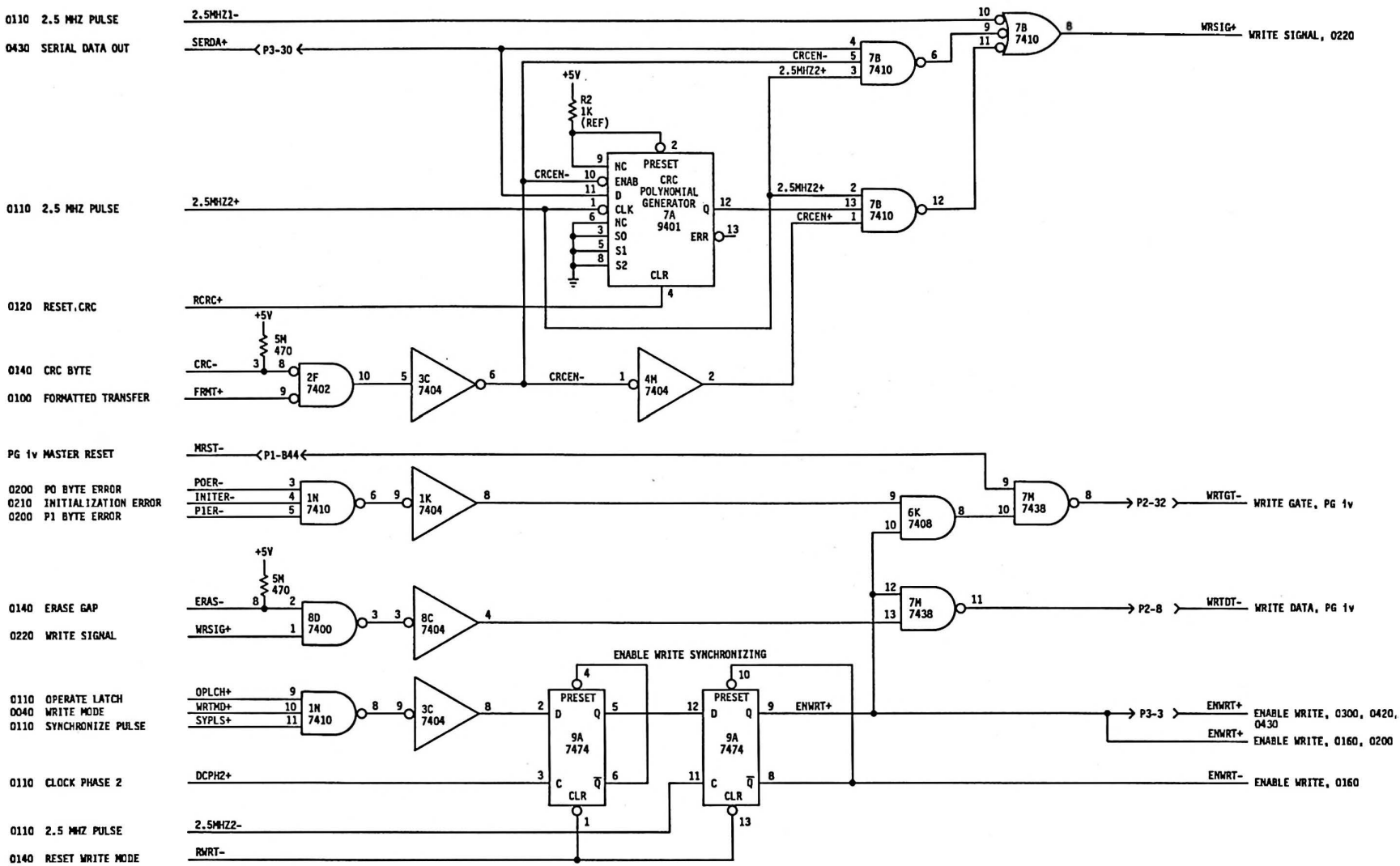

0190 CRC ERROR
CRCER+
0050 CYLINDER ADDRESS BIT 4
CADD4+
0090 SECTOR ADDRESS BIT 4
SADD4+
+5V
7F 220
7F 270
PG 1v SEEK COMPLETE 3
SKCMP3-
P2-3
7E 7404
SKCMP3+
D BUS MUX 9D 74153
1C0
1C1
1C2
1C3
STR1
STR2
2C0
2C1
2C2
2C3
1Y
2Y
P3-39
D4+
D BUS BIT 4, 0420
P3-31
D5+
D BUS BIT 5, 0420
0180 D MUX STROBE
DMSTR-
0200 PO BYTE ERROR
POER+
0050 CYLINDER ADDRESS BIT 5
CADD5+
0100 HEAD SELECT
HDSL+
PG 1v SEEK INCOMPLETE
SKINCP-
P2-18
SKINCP+
SEEK INCOMPLETE, 0180
0180 D MUX SELECT A
DMUXA+
0180 D MUX SELECT B
DMUXB+
0120 P1 BYTE
P1-
5M 470 (REF)
3N 7402
P1 CHECK
PRESET
3K 7474
CLR
P1ER+
P1 BYTE ERROR, 0210
P1ER-
P1 BYTE ERROR, 0220
0460 KEYCOMPARE EQUAL
CMPEQ+
P3-37
0220 ENABLE WRITE
ENWRT+
2F 7402
1K 7404
PO CHECK
0120 PO BYTE
PO-
POER+
PO BYTE ERROR, 0200
POER-
PO BYTE ERROR, 0220
0190 READ CLOCK
RDCLK-
0160 BYTE READY
BYTRY+
3F 7410
0100 FORMATTED TRANSFER
FRMT-
0160 ENABLE READ OR WRITE
ENRW+
6B 7408
0190 RESET ERROR STATUS
RERST-

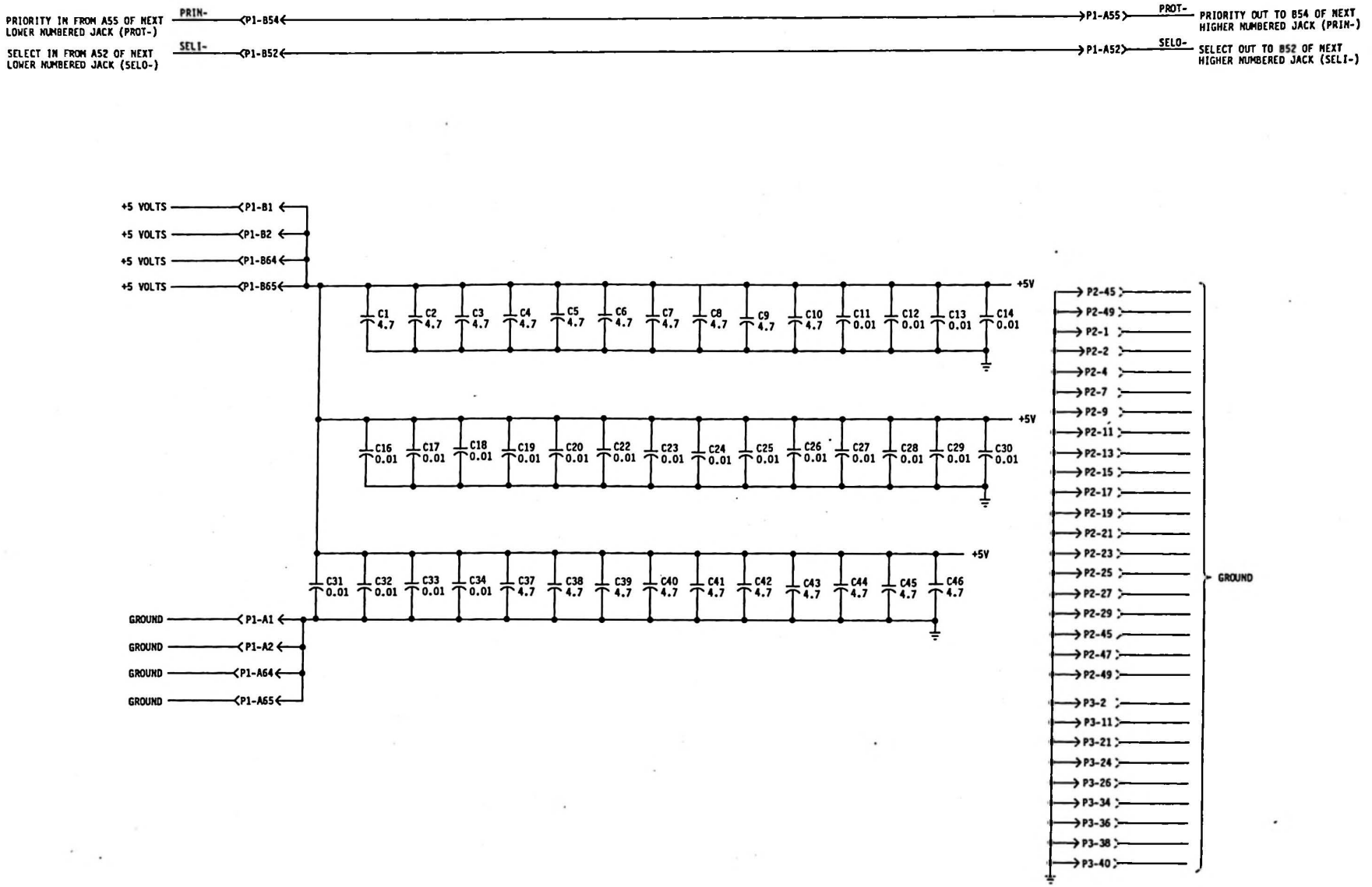


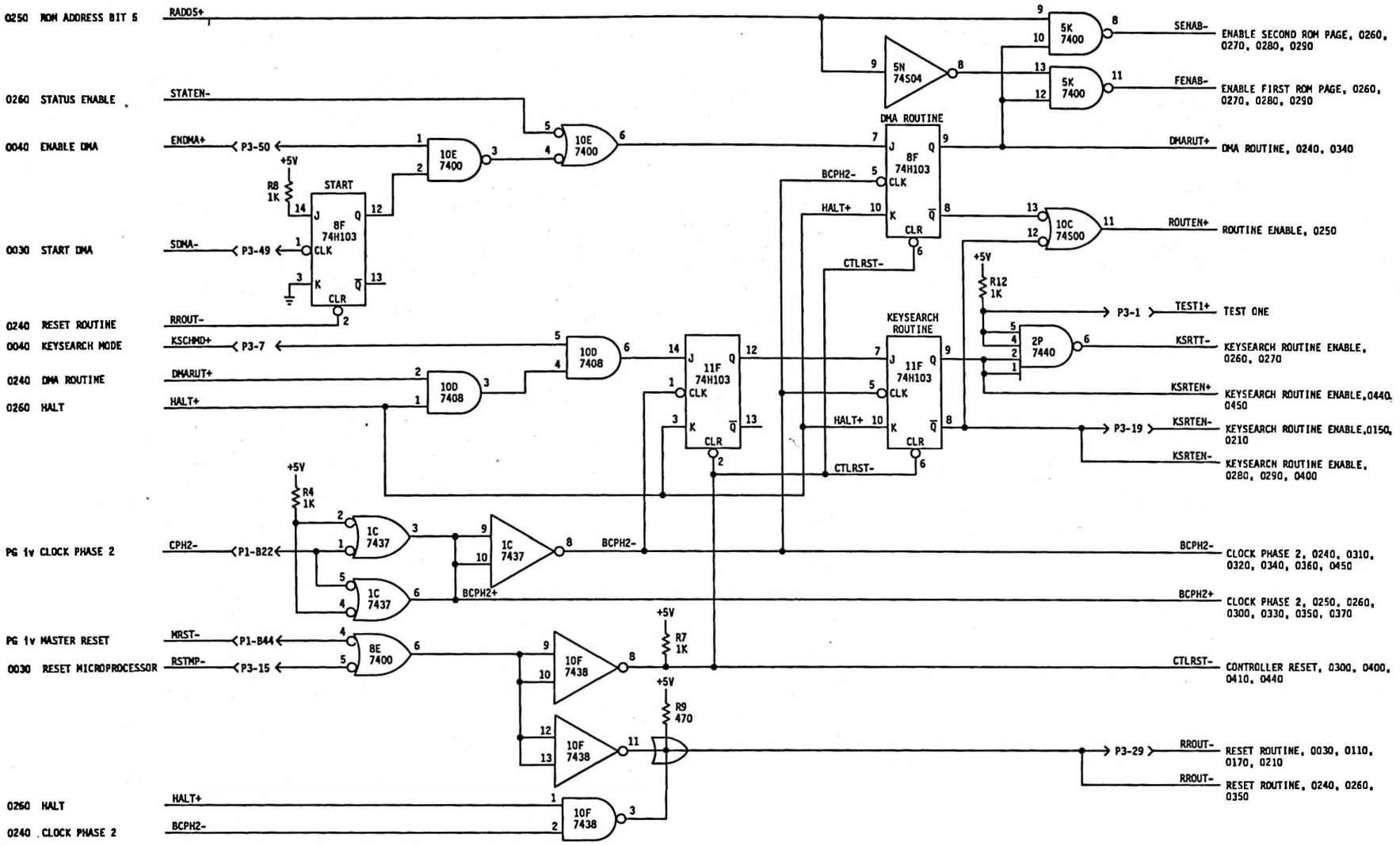
LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

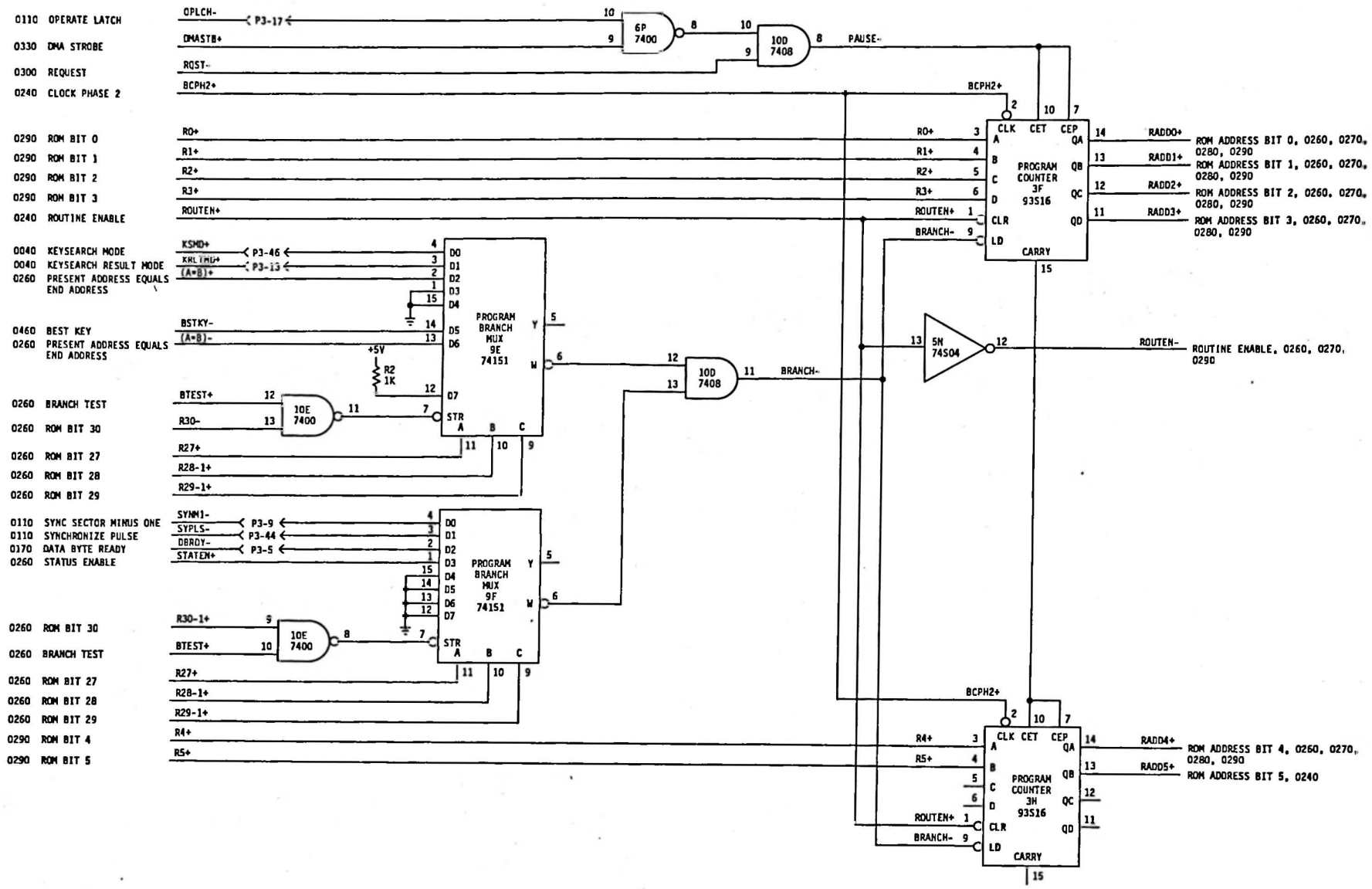
D BUS BITS 6 AND 7 AND INTERRUPT

DISC CONTROL LOGIC BOARD
0210


0110 2.5 MHZ PULSE
2.5MHZ1-
0430 SERIAL DATA OUT
SERDA+
P3-30
7B 7410
WRSIG+
WRITE SIGNAL, 0220
CRCEN-
2.5MHZ2+
+5V
R2 1K (REF)
NC PRESET
ENAB CRC POLYNOMIAL GENERATOR 7A 9401
D
CLK
NC
S0
S1
S2
Q
ERR
CLR
0110 2.5 MHZ PULSE
2.5MHZ2+
CRCEN+
0120 RESET,CRC
RCRC+
5M 470
0140 CRC BYTE
CRC-
0100 FORMATTED TRANSFER
FRMT+
2F 7402
3C 7404
4M 7404
PG 1v MASTER RESET
MRST-
P1-B44
0200 PO BYTE ERROR
0210 INITIALIZATION ERROR
0200 P1 BYTE ERROR
POER-
INITER-
P1ER-
1M 7410
1K 7404
6K 7408
7M 7438
P2-32
WRTGT-
WRITE GATE, PG 1v
0140 ERASE GAP
0220 WRITE SIGNAL
ERAS-
WRSIG+
8D 7400
8C 7404
P2-8
WRTDT-
WRITE DATA, PG 1v
ENABLE WRITE SYNCHRONIZING
0110 OPERATE LATCH
0040 WRITE MODE
0110 SYNCHRONIZE PULSE
OPLCH+
WRTMD+
SYPLS+
PRESET
D Q
9A 7474
C Q CLR
ENWRT+
P3-3
ENWRT+
ENABLE WRITE, 0300, 0420, 0430
ENWRT+
ENABLE WRITE, 0160, 0200
0110 CLOCK PHASE 2
DCPH2+
ENWRT-
ENABLE WRITE, 0160
0110 2.5 MHZ PULSE
2.5MHZ2-
0140 RESET WRITE MODE
RWRT-


PRIORITY IN FROM A55 OF NEXT LOWER NUMBERED JACK (PROT-)
PRIN-
P1-B54
P1-A55
PROT-
PRIORITY OUT TO B54 OF NEXT HIGHER NUMBERED JACK (PRIN-)
SELECT IN FROM A52 OF NEXT LOWER NUMBERED JACK (SELO-)
SELI-
P1-B52
P1-A52
SELO-
SELECT OUT TO B52 OF NEXT HIGHER NUMBERED JACK (SELI-)
+5 VOLTS
P1-B1
+5 VOLTS
P1-B2
+5 VOLTS
P1-B64
+5 VOLTS
P1-B65
C1 4.7
C2 4.7
C3 4.7
C4 4.7
C5 4.7
C6 4.7
C7 4.7
C8 4.7
C9 4.7
C10 4.7
C11 0.01
C12 0.01
C13 0.01
C14 0.01
+5V
C16 0.01
C17 0.01
C18 0.01
C19 0.01
C20 0.01
C22 0.01
C23 0.01
C24 0.01
C25 0.01
C26 0.01
C27 0.01
C28 0.01
C29 0.01
C30 0.01
+5V
C31 0.01
C32 0.01
C33 0.01
C34 0.01
C37 4.7
C38 4.7
C39 4.7
C40 4.7
C41 4.7
C42 4.7
C43 4.7
C44 4.7
C45 4.7
C46 4.7
+5V
GROUND
P1-A1
GROUND
P1-A2
GROUND
P1-A64
GROUND
P1-A65
P2-45
P2-49
P2-1
P2-2
P2-4
P2-7
P2-9
P2-11
P2-13
P2-15
P2-17
P2-19
P2-21
P2-23
P2-25
P2-27
P2-29
P2-45
P2-47
P2-49
P3-2
P3-11
P3-21
P3-24
P3-26
P3-34
P3-36
P3-38
P3-40
GROUND

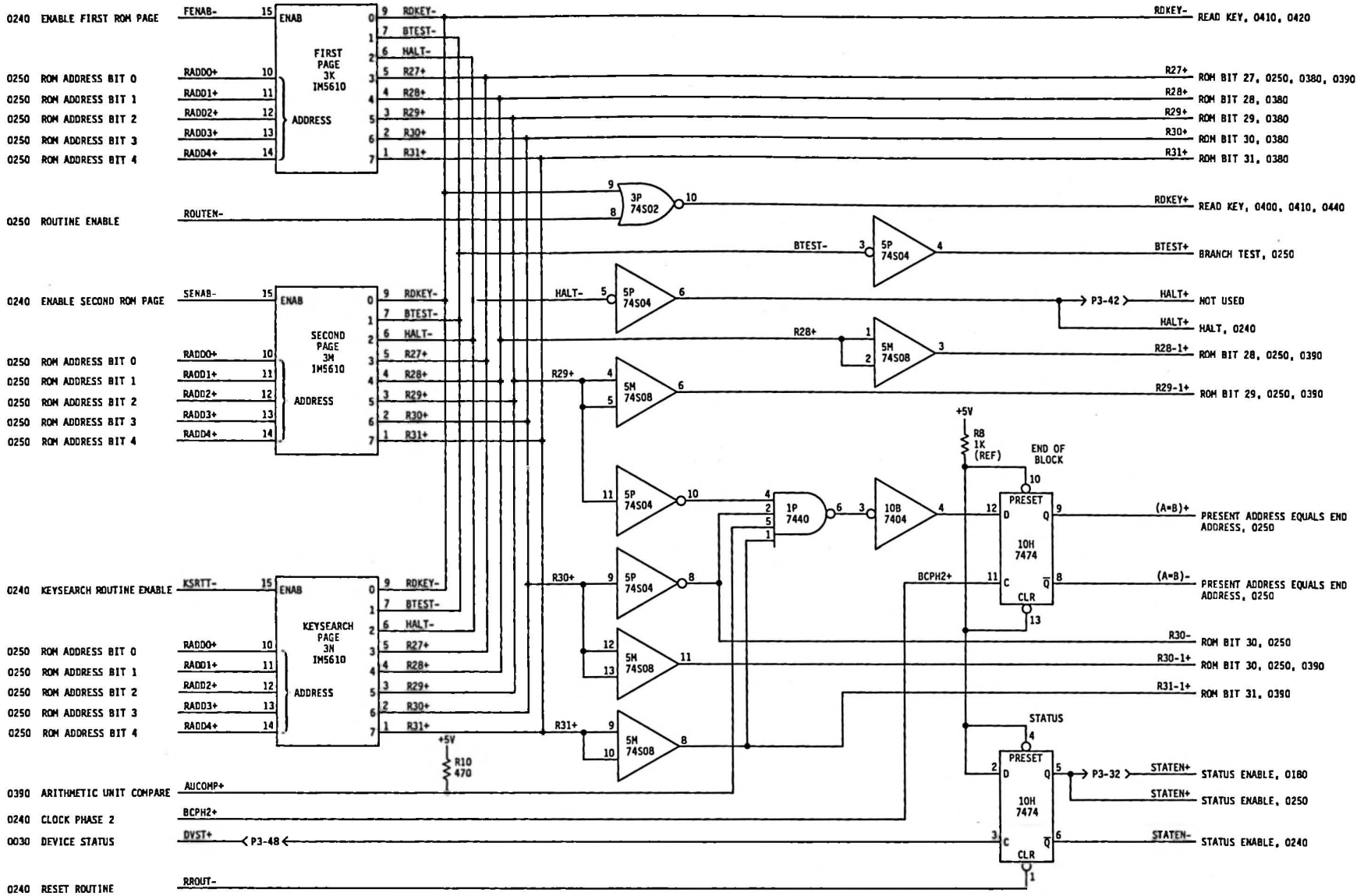

0250 ROM ADDRESS BIT 5
RAD05+
0260 STATUS ENABLE
STATEN-
0040 ENABLE DMA
ENDMA+
P3-50
0030 START DMA
SDMA-
P3-49
0240 RESET ROUTINE
RROUT-
0040 KEYSEARCH MODE
KSCHMD+
P3-7
0240 DMA ROUTINE
DMARUT+
0260 HALT
HALT+
PG iv CLOCK PHASE 2
CPH2-
P1-B22
PG iv MASTER RESET
MRST-
P1-B44
0030 RESET MICROPROCESSOR
RSTMP-
P3-15
0260 HALT
HALT+
0240 CLOCK PHASE 2
BCPH2-
+5V
R8 1K
R4 1K
R7 1K
R9 470
R12 1K
START
8F 74H103
10E 7400
10D 7408
11F 74H103
1C 7437
8E 7400
10F 7438
5N 74S04
5K 7400
8F 74H103
DMA ROUTINE
10C 74S00
KEYSEARCH ROUTINE
2P 7440
BCPH2+
CTLRST-
SENAB-
ENABLE SECOND ROM PAGE, 0260, 0270, 0280, 0290
FENAB-
ENABLE FIRST ROM PAGE, 0260, 0270, 0280, 0290
DMARUT+
DMA ROUTINE, 0240, 0340
ROUTEN+
ROUTINE ENABLE, 0250
TESTI+
TEST ONE
KSRTT-
KEYSEARCH ROUTINE ENABLE, 0260, 0270
KSRTEN+
KEYSEARCH ROUTINE ENABLE, 0440, 0450
KSRTEN-
KEYSEARCH ROUTINE ENABLE, 0150, 0210
KSRTEN-
KEYSEARCH ROUTINE ENABLE, 0280, 0290, 0400
BCPH2-
CLOCK PHASE 2, 0240, 0310, 0320, 0340, 0360, 0450
BCPH2+
CLOCK PHASE 2, 0250, 0260, 0300, 0330, 0350, 0370
CTLRST-
CONTROLLER RESET, 0300, 0400, 0410, 0440
RROUT-
RESET ROUTINE, 0030, 0110, 0170, 0210
RROUT-
RESET ROUTINE, 0240, 0260, 0350

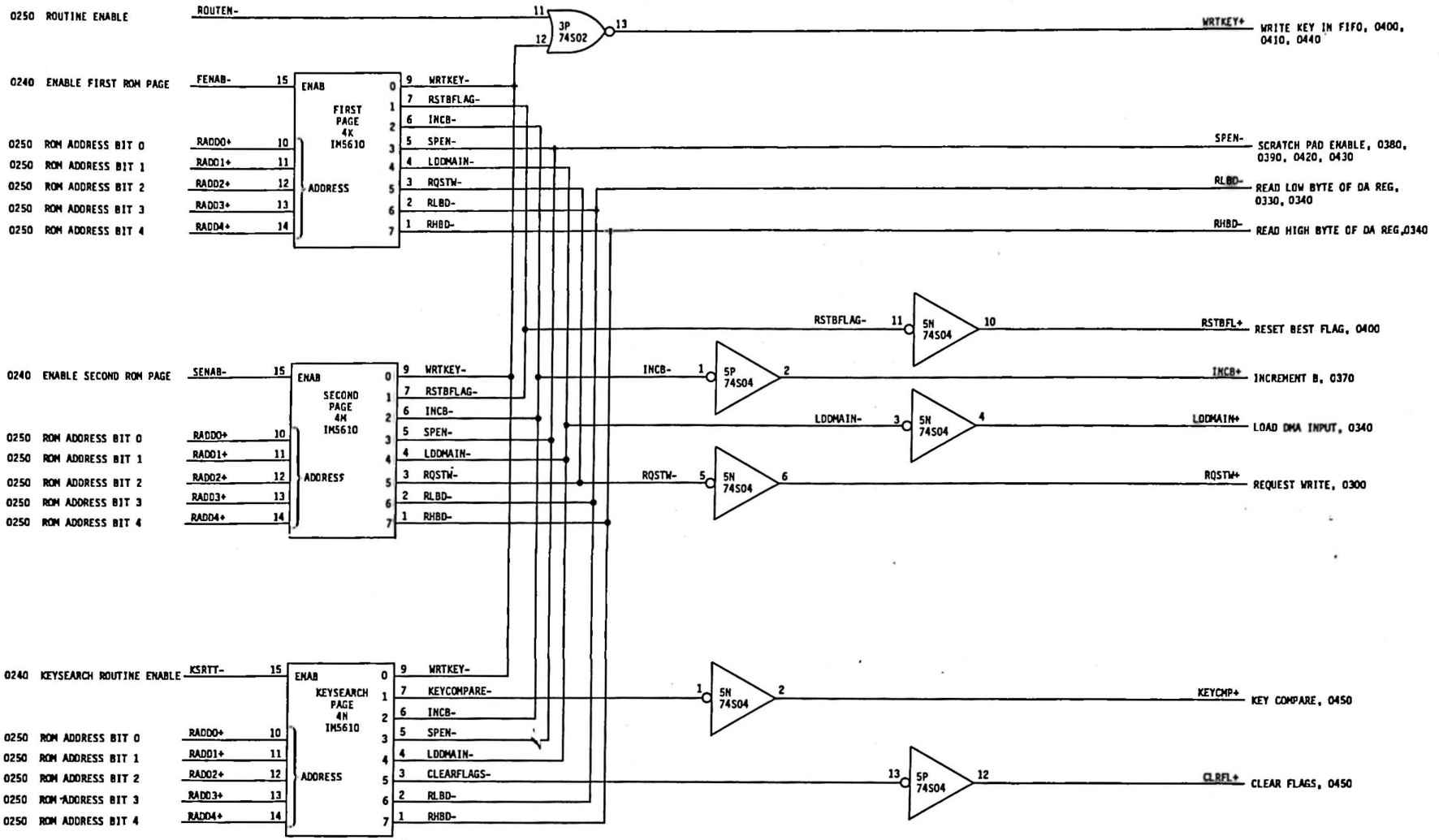


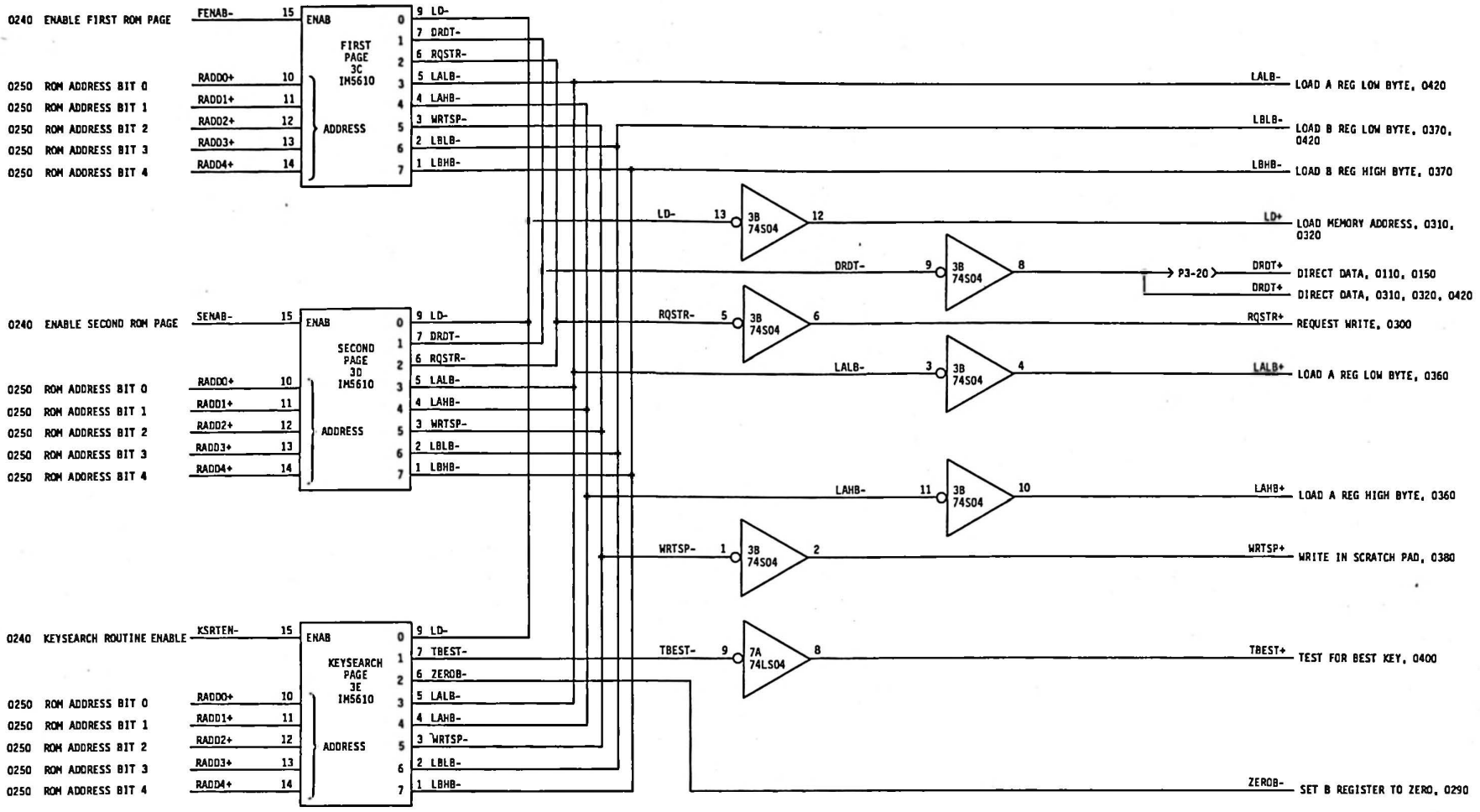
LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

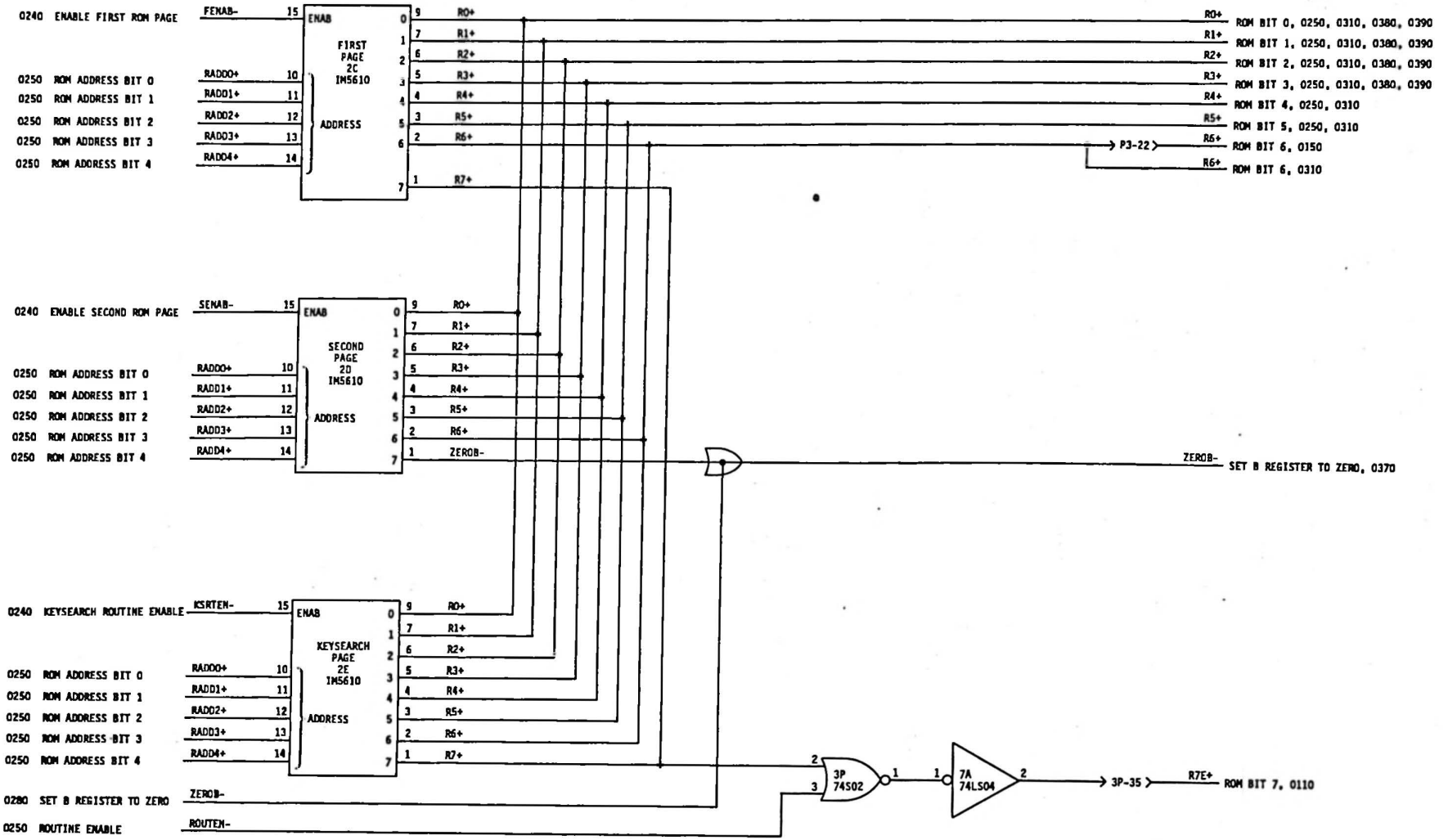
PROGRAM COUNTER

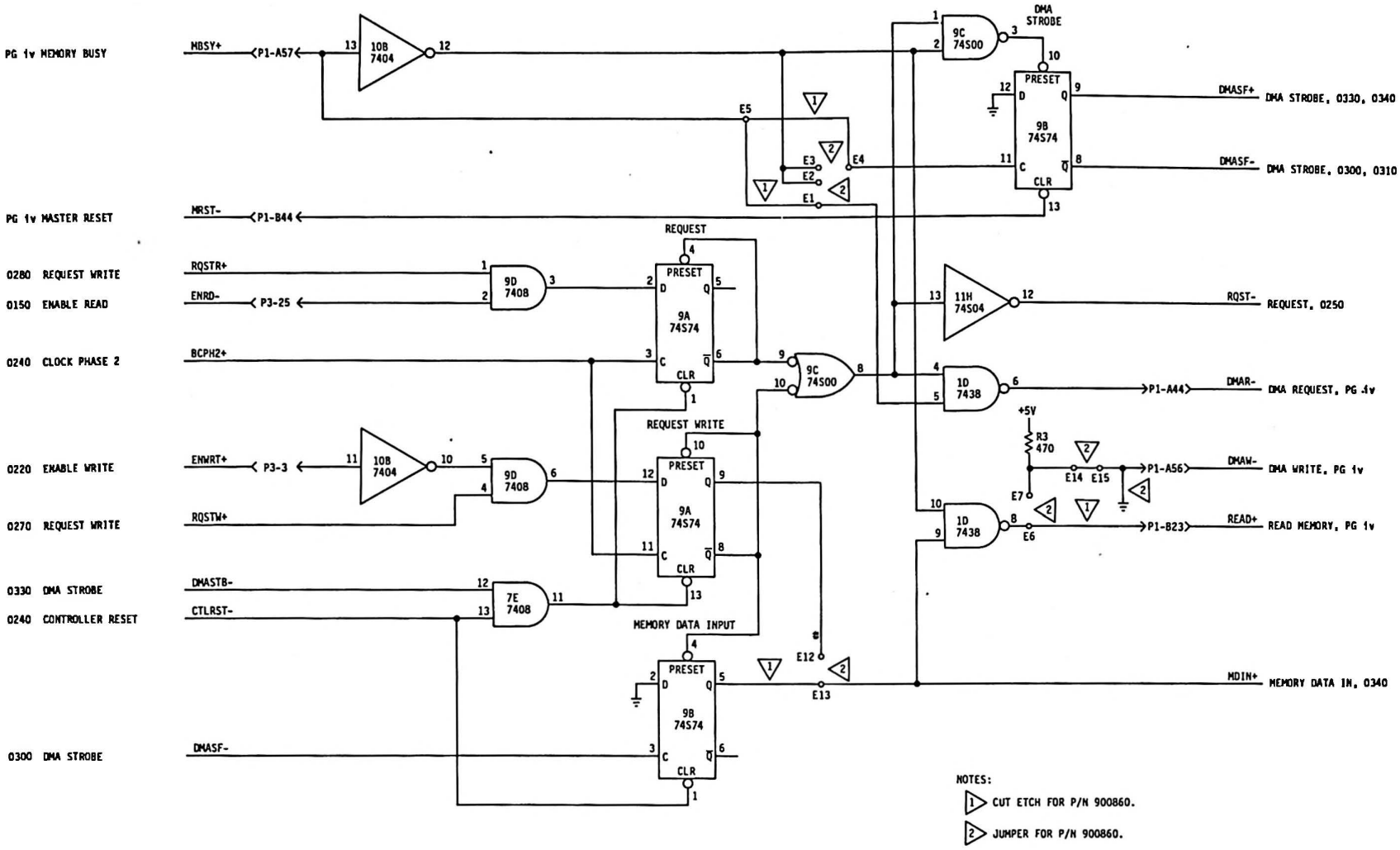
DMA LOGIC MICROPROCESSOR BOARD
0250

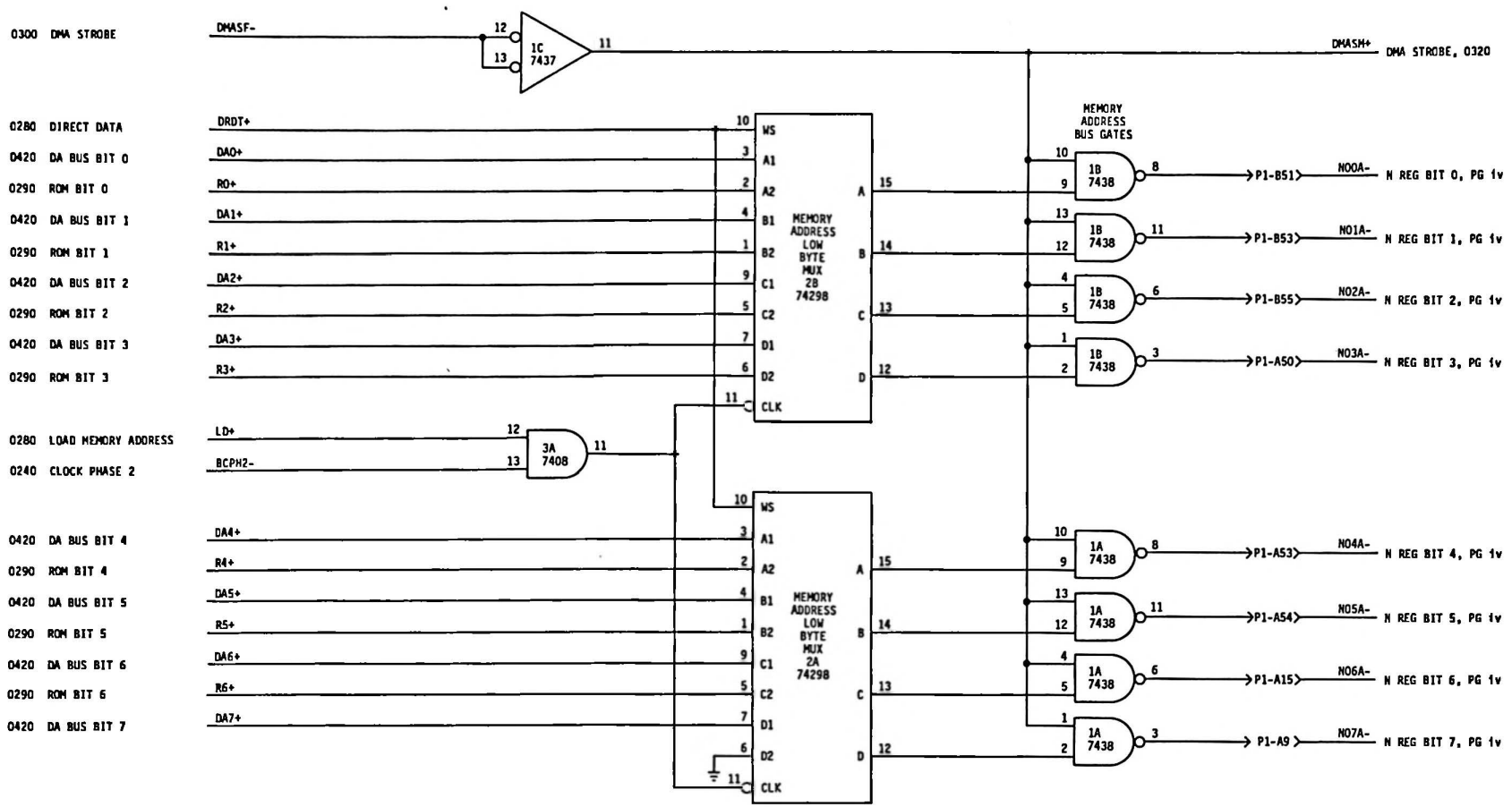

0240 ENABLE FIRST ROM PAGE
FENAB-
FIRST PAGE 3K IM5610
ADDRESS
0250 ROM ADDRESS BIT 0
0250 ROM ADDRESS BIT 1
0250 ROM ADDRESS BIT 2
0250 ROM ADDRESS BIT 3
0250 ROM ADDRESS BIT 4
RADD0+
RADD1+
RADD2+
RADD3+
RADD4+
RDKEY-
BTEST-
HALT-
R27+
R28+
R29+
R30+
R31+
0250 ROUTINE ENABLE
ROUTEN-
3P 74S02
RDKEY+ READ KEY, 0400, 0410, 0440
BTEST-
5P 74S04
BTEST+ BRANCH TEST, 0250
0240 ENABLE SECOND ROM PAGE
SENAB-
SECOND PAGE 3M IM5610
HALT-
P3-42
HALT+ NOT USED
HALT+ HALT, 0240
R28+
5M 74S08
R28-1+ ROM BIT 28, 0250, 0390
R29+
R29-1+ ROM BIT 29, 0250, 0390
+5V
R8 1K (REF)
END OF BLOCK
PRESET
10H 7474
CLR
1P 7440
10B 7404
(A=B)+ PRESENT ADDRESS EQUALS END ADDRESS, 0250
(A=B)- PRESENT ADDRESS EQUALS END ADDRESS, 0250
BCPH2+
0240 KEYSEARCH ROUTINE ENABLE
KSRTT-
KEYSEARCH PAGE 3N IM5610
R30+
R30-
R30-1+ ROM BIT 30, 0250, 0390
R31+
R31-1+ ROM BIT 31, 0390
STATUS
R10 470
0390 ARITHMETIC UNIT COMPARE
AUCOMP+
0240 CLOCK PHASE 2
BCPH2+
0030 DEVICE STATUS
DVST+
P3-48
P3-32
STATEN+ STATUS ENABLE, 0180
STATEN+ STATUS ENABLE, 0250
STATEN- STATUS ENABLE, 0240
0240 RESET ROUTINE
RROUT-

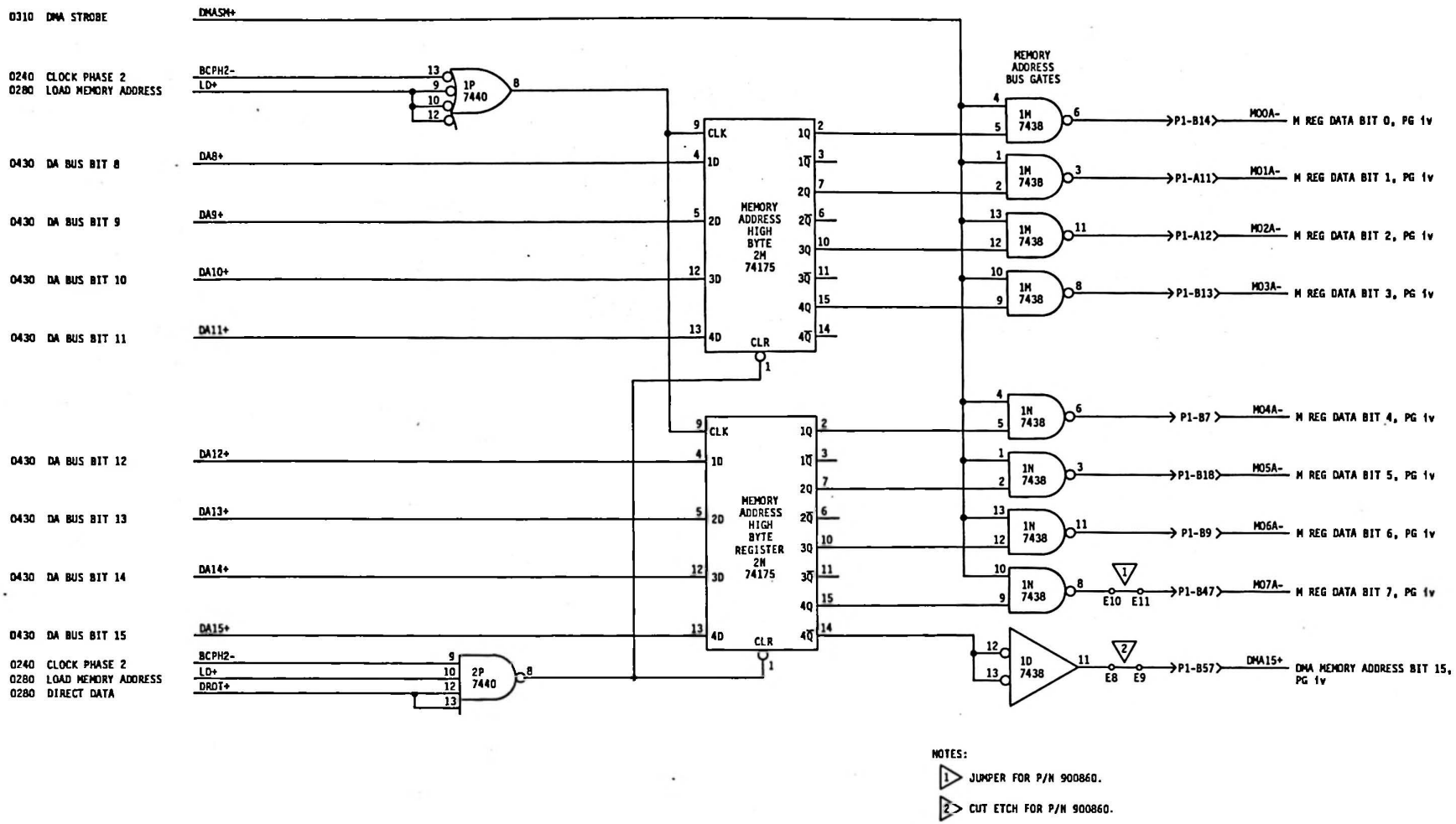

0250 ROUTINE ENABLE
ROUTEN-
3P 74S02
WRTKEY+
WRITE KEY IN FIFO, 0400, 0410, 0440
0240 ENABLE FIRST ROM PAGE
FENAB-
FIRST PAGE 4K IM5610
ENAB
ADDRESS
0250 ROM ADDRESS BIT 0
0250 ROM ADDRESS BIT 1
0250 ROM ADDRESS BIT 2
0250 ROM ADDRESS BIT 3
0250 ROM ADDRESS BIT 4
RADD0+
RADD1+
RADD2+
RADD3+
RADD4+
WRTKEY-
RSTBFLAG-
INCB-
SPEN-
LDDMAIN-
RQSTW-
RLBD-
RHBD-
SPEN-
SCRATCH PAD ENABLE, 0380, 0390, 0420, 0430
RLBD-
READ LOW BYTE OF DA REG, 0330, 0340
RHBD-
READ HIGH BYTE OF DA REG,0340
RSTBFLAG-
5N 74S04
RSTBFL+
RESET BEST FLAG, 0400
0240 ENABLE SECOND ROM PAGE
SENAB-
SECOND PAGE 4M IM5610
INCB-
5P 74S04
INCB+
INCREMENT B, 0370
LDDMAIN-
LOAD DMA INPUT, 0340
RQSTW-
REQUEST WRITE, 0300
0240 KEYSEARCH ROUTINE ENABLE
KSRTT-
KEYSEARCH PAGE 4M IM5610
KEYCOMPARE-
KEYCMP+
KEY COMPARE, 0450
CLEARFLAGS-
CLRFL+
CLEAR FLAGS, 0450


0240 ENABLE FIRST ROM PAGE
FENAB- 15
FIRST PAGE 3C IM5610
ENAB
ADDRESS
0250 ROM ADDRESS BIT 0
0250 ROM ADDRESS BIT 1
0250 ROM ADDRESS BIT 2
0250 ROM ADDRESS BIT 3
0250 ROM ADDRESS BIT 4
RADD0+ 10
RADD1+ 11
RADD2+ 12
RADD3+ 13
RADD4+ 14
9 LD-
7 DRDT-
6 RQSTR-
5 LALB-
4 LAHB-
3 WRTSP-
2 LBLB-
1 LBHB-
0240 ENABLE SECOND ROM PAGE
SENAB- 15
SECOND PAGE 3D IM5610
0240 KEYSEARCH ROUTINE ENABLE
KSRTEN- 15
KEYSEARCH PAGE 3E IM5610
7 TBEST-
6 ZEROB-
LD- 13
3B 74S04 12
LD+
LOAD MEMORY ADDRESS, 0310, 0320
DRDT- 9
3B 74S04 8
P3-20
DRDT+
DIRECT DATA, 0110, 0150
DRDT+
DIRECT DATA, 0310, 0320, 0420
RQSTR- 5
3B 74S04 6
RQSTR+
REQUEST WRITE, 0300
LALB- 3
3B 74S04 4
LALB+
LOAD A REG LOW BYTE, 0360
LAHB- 11
3B 74S04 10
LAHB+
LOAD A REG HIGH BYTE, 0360
WRTSP- 1
3B 74S04 2
WRTSP+
WRITE IN SCRATCH PAD, 0380
TBEST- 9
7A 74LS04 8
TBEST+
TEST FOR BEST KEY, 0400
LALB-
LOAD A REG LOW BYTE, 0420
LBLB-
LOAD B REG LOW BYTE, 0370, 0420
LBHB-
LOAD B REG HIGH BYTE, 0370
ZEROB-
SET B REGISTER TO ZERO, 0290


0240 ENABLE FIRST ROM PAGE
FENAB-
15
ENAB
FIRST PAGE 2C IM5610
ADDRESS
0250 ROM ADDRESS BIT 0
0250 ROM ADDRESS BIT 1
0250 ROM ADDRESS BIT 2
0250 ROM ADDRESS BIT 3
0250 ROM ADDRESS BIT 4
RADD0+
RADD1+
RADD2+
RADD3+
RADD4+
10
11
12
13
14
0
1
2
3
4
5
6
7
9
7
6
5
4
3
2
1
R0+
R1+
R2+
R3+
R4+
R5+
R6+
R7+
R0+ ROM BIT 0, 0250, 0310, 0380, 0390
R1+ ROM BIT 1, 0250, 0310, 0380, 0390
R2+ ROM BIT 2, 0250, 0310, 0380, 0390
R3+ ROM BIT 3, 0250, 0310, 0380, 0390
R4+ ROM BIT 4, 0250, 0310
R5+ ROM BIT 5, 0250, 0310
R6+ ROM BIT 6, 0150
P3-22
R6+ ROM BIT 6, 0310
0240 ENABLE SECOND ROM PAGE
SENAB-
SECOND PAGE 2D IM5610
0250 ROM ADDRESS BIT 0
0250 ROM ADDRESS BIT 1
0250 ROM ADDRESS BIT 2
0250 ROM ADDRESS BIT 3
0250 ROM ADDRESS BIT 4
ZEROB-
ZEROB- SET B REGISTER TO ZERO, 0370
0240 KEYSEARCH ROUTINE ENABLE
KSRTEN-
KEYSEARCH PAGE 2E IM5610
0280 SET B REGISTER TO ZERO
0250 ROUTINE ENABLE
ROUTEN-
3P 74S02
7A 74LS04
3P-35
R7E+
R7E+ ROM BIT 7, 0110

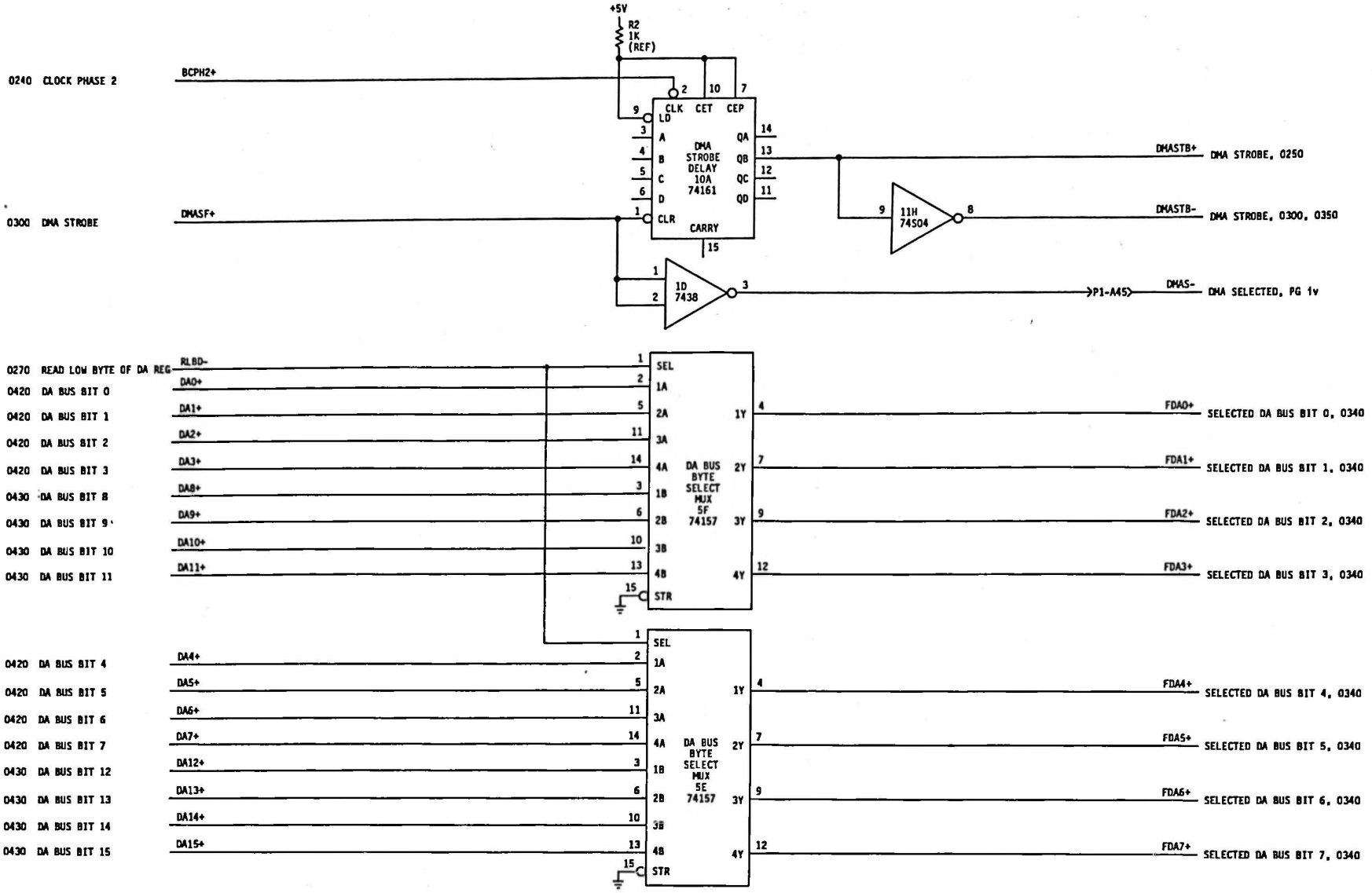

PG 1v MEMORY BUSY
MBSY+
P1-A57
10B 7404
DMA STROBE
9C 74S00
PRESET
9B 74S74
CLR
DMASF+
DMA STROBE, 0330, 0340
DMASF-
DMA STROBE, 0300, 0310
E1
E2
E3
E4
E5
PG 1v MASTER RESET
MRST-
P1-B44
REQUEST
0280 REQUEST WRITE
RQSTR+
0150 ENABLE READ
ENRD-
P3-25
9D 7408
9A 74S74
11H 74S04
RQST-
REQUEST, 0250
0240 CLOCK PHASE 2
BCPH2+
1D 7438
DMAR-
DMA REQUEST, PG 1v
P1-A44
REQUEST WRITE
+5V
R3 470
0220 ENABLE WRITE
ENWRT+
P3-3
DMAW-
DMA WRITE, PG 1v
P1-A56
E14
E15
E7
0270 REQUEST WRITE
RQSTW+
READ+
READ MEMORY, PG 1v
P1-B23
E6
0330 DMA STROBE
DMASTB-
0240 CONTROLLER RESET
CTLRST-
7E 7408
MEMORY DATA INPUT
E12
E13
MDIN+
MEMORY DATA IN, 0340
0300 DMA STROBE
DMASF-
NOTES:
1 CUT ETCH FOR P/N 900860.
2 JUMPER FOR P/N 900860.


0300 DMA STROBE
DMASF-
1C 7437
DMASH+
DMA STROBE, 0320
0280 DIRECT DATA
0420 DA BUS BIT 0
0290 ROM BIT 0
0420 DA BUS BIT 1
0290 ROM BIT 1
0420 DA BUS BIT 2
0290 ROM BIT 2
0420 DA BUS BIT 3
0290 ROM BIT 3
DRDT+
DA0+
R0+
DA1+
R1+
DA2+
R2+
DA3+
R3+
MEMORY ADDRESS LOW BYTE MUX 2B 74298
WS
A1
A2
B1
B2
C1
C2
D1
D2
CLK
A
B
C
D
0280 LOAD MEMORY ADDRESS
0240 CLOCK PHASE 2
LD+
BCPH2-
3A 7408
0420 DA BUS BIT 4
0290 ROM BIT 4
0420 DA BUS BIT 5
0290 ROM BIT 5
0420 DA BUS BIT 6
0290 ROM BIT 6
0420 DA BUS BIT 7
DA4+
R4+
DA5+
R5+
DA6+
R6+
DA7+
MEMORY ADDRESS LOW BYTE MUX 2A 74298
MEMORY ADDRESS BUS GATES
1B 7438
1A 7438
P1-B51
P1-B53
P1-B55
P1-A50
P1-A53
P1-A54
P1-A15
P1-A9
N00A-
N01A-
N02A-
N03A-
N04A-
N05A-
N06A-
N07A-
N REG BIT 0, PG 1v
N REG BIT 1, PG 1v
N REG BIT 2, PG 1v
N REG BIT 3, PG 1v
N REG BIT 4, PG 1v
N REG BIT 5, PG 1v
N REG BIT 6, PG 1v
N REG BIT 7, PG 1v



NOTES:

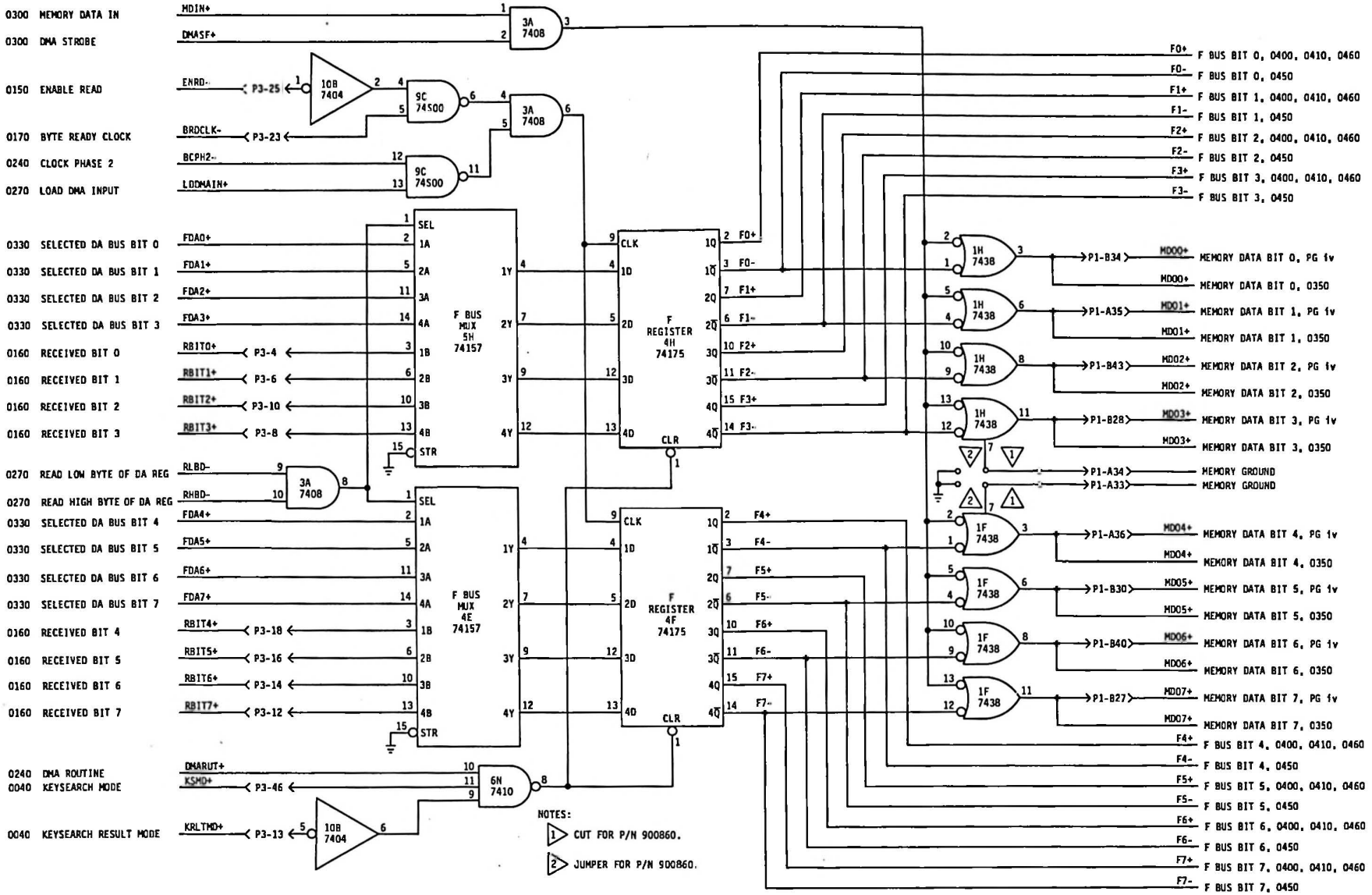
1. JUMPER FOR P/N 900860.
2. CUT ETCH FOR P/N 900860.

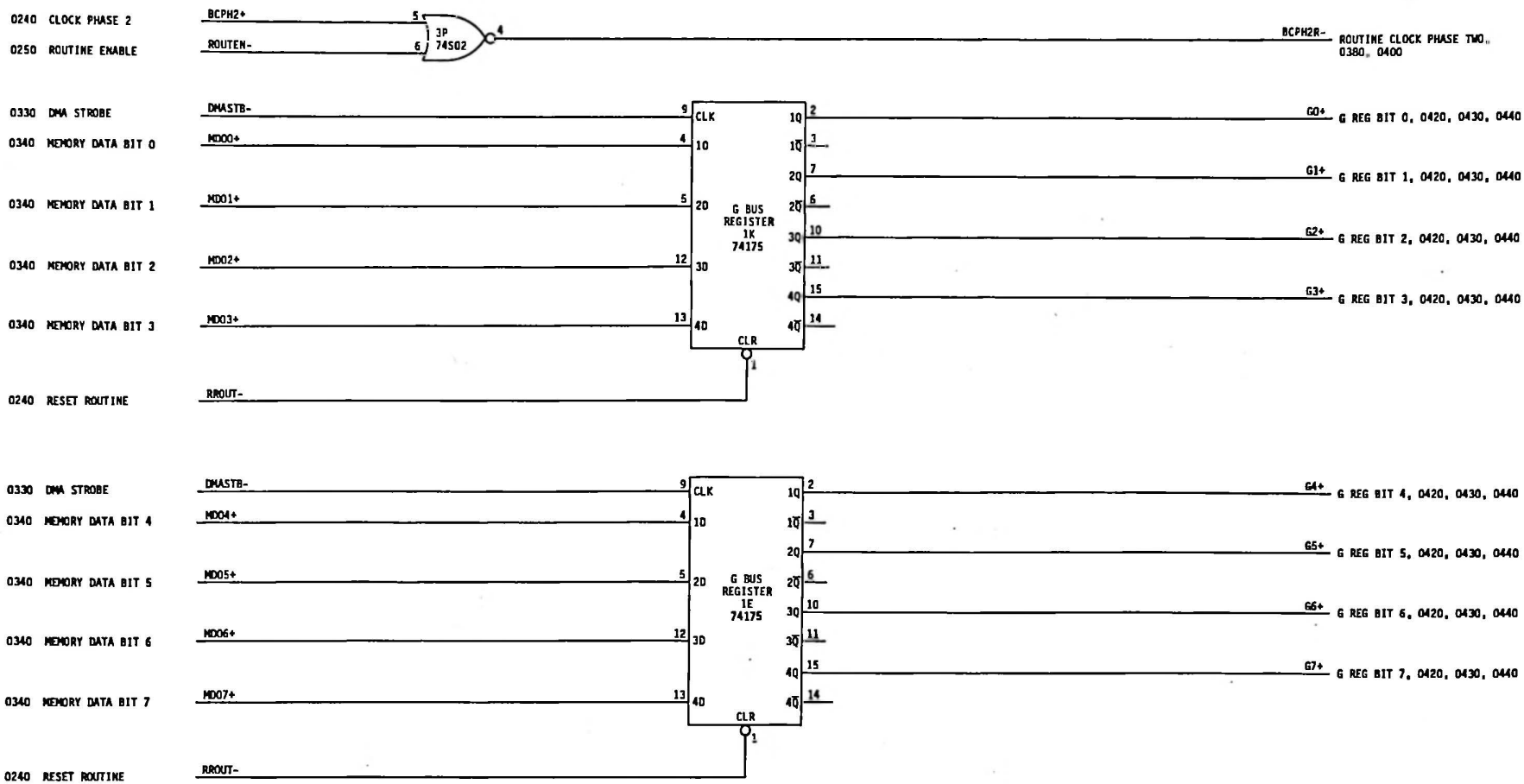


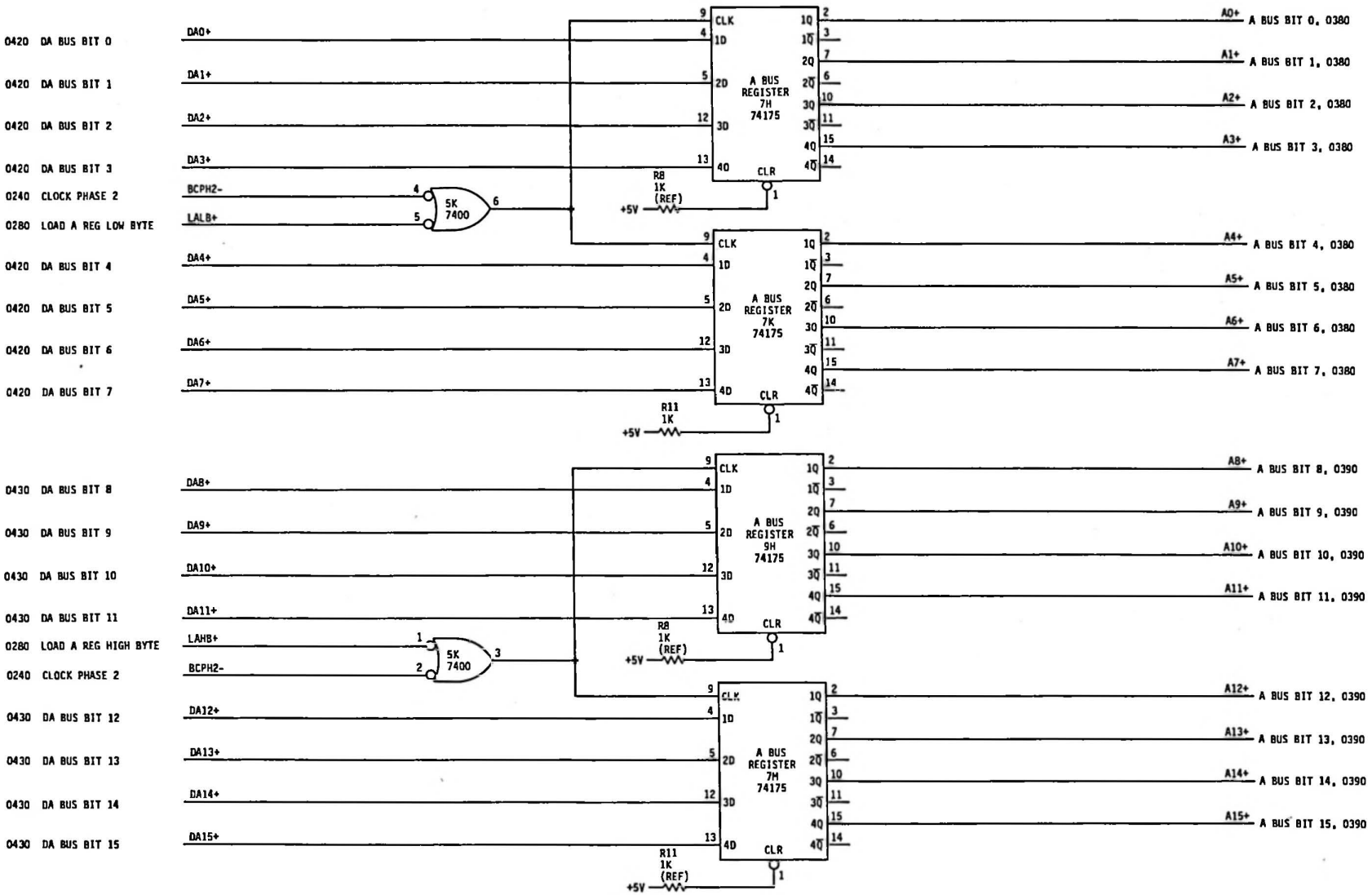
LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

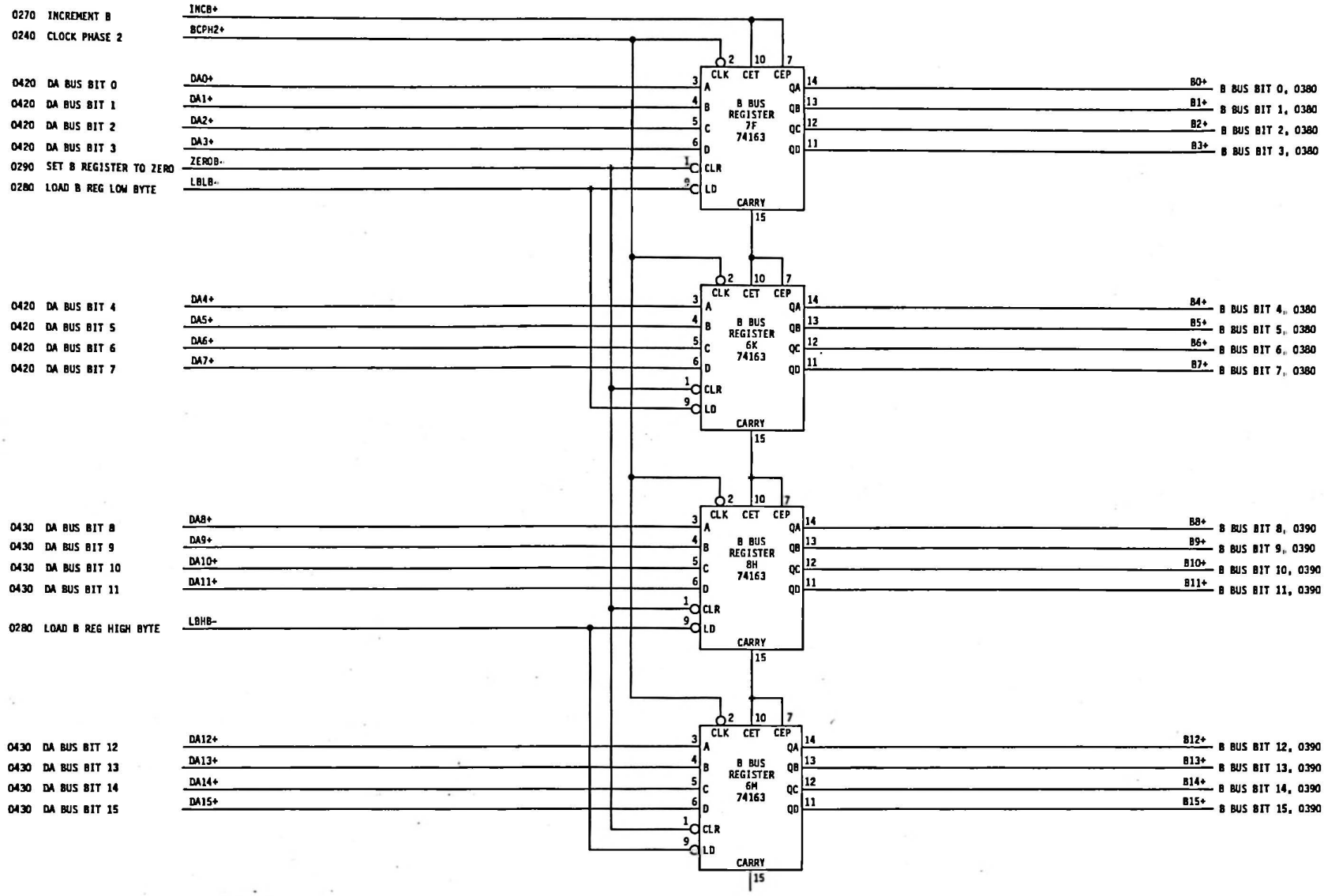
DMA STROBE AND DA BUS BYTE SELECT CIRCUITS

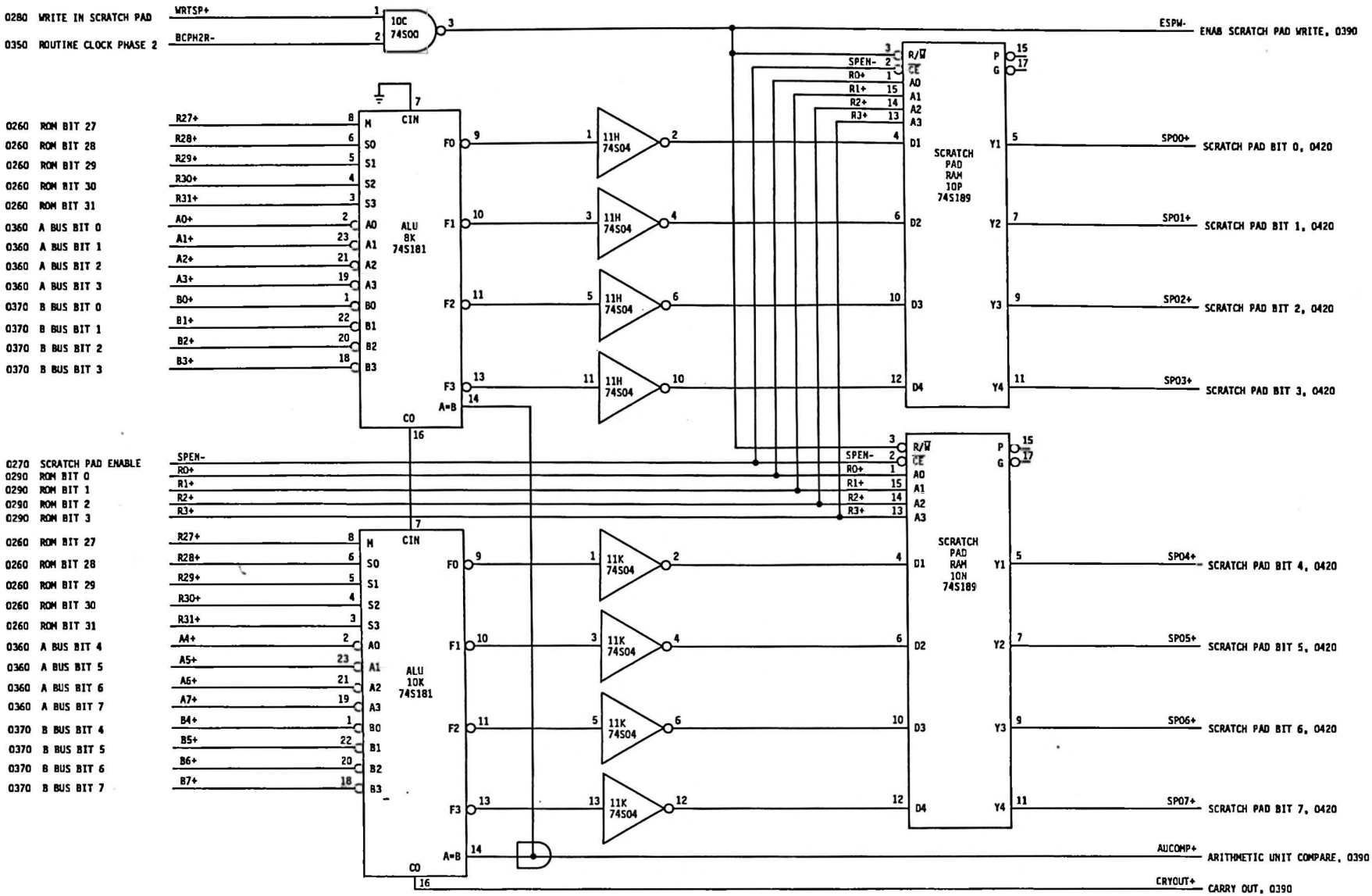
DMA LOGIC MICROPROCESSOR BOARD
0330

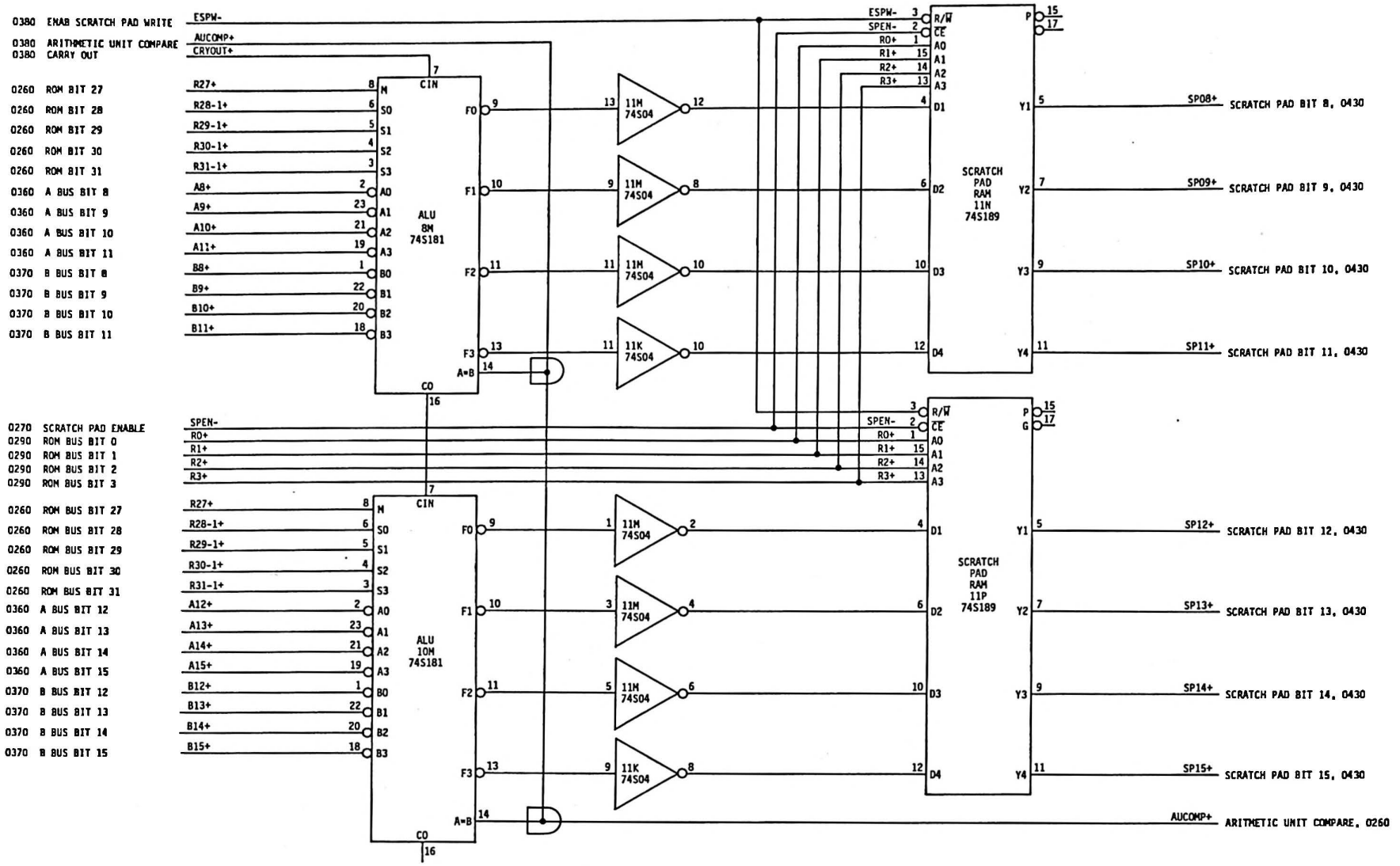

0300 MEMORY DATA IN
0300 DMA STROBE
0150 ENABLE READ
0170 BYTE READY CLOCK
0240 CLOCK PHASE 2
0270 LOAD DMA INPUT
MDIN+
DMASF+
ENRD-
P3-25
BRDCLK-
P3-23
BCPH2-
LDDMAIN+
3A 7408
10B 7404
9C 74S00
0330 SELECTED DA BUS BIT 0
0330 SELECTED DA BUS BIT 1
0330 SELECTED DA BUS BIT 2
0330 SELECTED DA BUS BIT 3
0160 RECEIVED BIT 0
0160 RECEIVED BIT 1
0160 RECEIVED BIT 2
0160 RECEIVED BIT 3
FDA0+
FDA1+
FDA2+
FDA3+
RBIT0+
RBIT1+
RBIT2+
RBIT3+
P3-4
P3-6
P3-10
P3-8
F BUS MUX 5H 74157
SEL
STR
0270 READ LOW BYTE OF DA REG
0270 READ HIGH BYTE OF DA REG
RLBD-
RHBD-
0330 SELECTED DA BUS BIT 4
0330 SELECTED DA BUS BIT 5
0330 SELECTED DA BUS BIT 6
0330 SELECTED DA BUS BIT 7
0160 RECEIVED BIT 4
0160 RECEIVED BIT 5
0160 RECEIVED BIT 6
0160 RECEIVED BIT 7
FDA4+
FDA5+
FDA6+
FDA7+
RBIT4+
RBIT5+
RBIT6+
RBIT7+
P3-18
P3-16
P3-14
P3-12
F BUS MUX 4E 74157
F REGISTER 4H 74175
F REGISTER 4F 74175
CLK
CLR
0240 DMA ROUTINE
0040 KEYSEARCH MODE
DMARUT+
KSMD+
P3-46
6N 7410
0040 KEYSEARCH RESULT MODE
KRLTMD+
P3-13
NOTES:
1 CUT FOR P/N 900860.
2 JUMPER FOR P/N 900860.
F0+ F BUS BIT 0, 0400, 0410, 0460
F0- F BUS BIT 0, 0450
F1+ F BUS BIT 1, 0400, 0410, 0460
F1- F BUS BIT 1, 0450
F2+ F BUS BIT 2, 0400, 0410, 0460
F2- F BUS BIT 2, 0450
F3+ F BUS BIT 3, 0400, 0410, 0460
F3- F BUS BIT 3, 0450
F4+ F BUS BIT 4, 0400, 0410, 0460
F4- F BUS BIT 4, 0450
F5+ F BUS BIT 5, 0400, 0410, 0460
F5- F BUS BIT 5, 0450
F6+ F BUS BIT 6, 0400, 0410, 0460
F6- F BUS BIT 6, 0450
F7+ F BUS BIT 7, 0400, 0410, 0460
F7- F BUS BIT 7, 0450
1H 7438
1F 7438
P1-B34
P1-A35
P1-B43
P1-B28
P1-A34
P1-A33
P1-A36
P1-B30
P1-B40
P1-B27
MD00+ MEMORY DATA BIT 0, PG 1v
MD00+ MEMORY DATA BIT 0, 0350
MD01+ MEMORY DATA BIT 1, PG 1v
MD01+ MEMORY DATA BIT 1, 0350
MD02+ MEMORY DATA BIT 2, PG 1v
MD02+ MEMORY DATA BIT 2, 0350
MD03+ MEMORY DATA BIT 3, PG 1v
MD03+ MEMORY DATA BIT 3, 0350
MEMORY GROUND
MEMORY GROUND
MD04+ MEMORY DATA BIT 4, PG 1v
MD04+ MEMORY DATA BIT 4, 0350
MD05+ MEMORY DATA BIT 5, PG 1v
MD05+ MEMORY DATA BIT 5, 0350
MD06+ MEMORY DATA BIT 6, PG 1v
MD06+ MEMORY DATA BIT 6, 0350
MD07+ MEMORY DATA BIT 7, PG 1v
MD07+ MEMORY DATA BIT 7, 0350

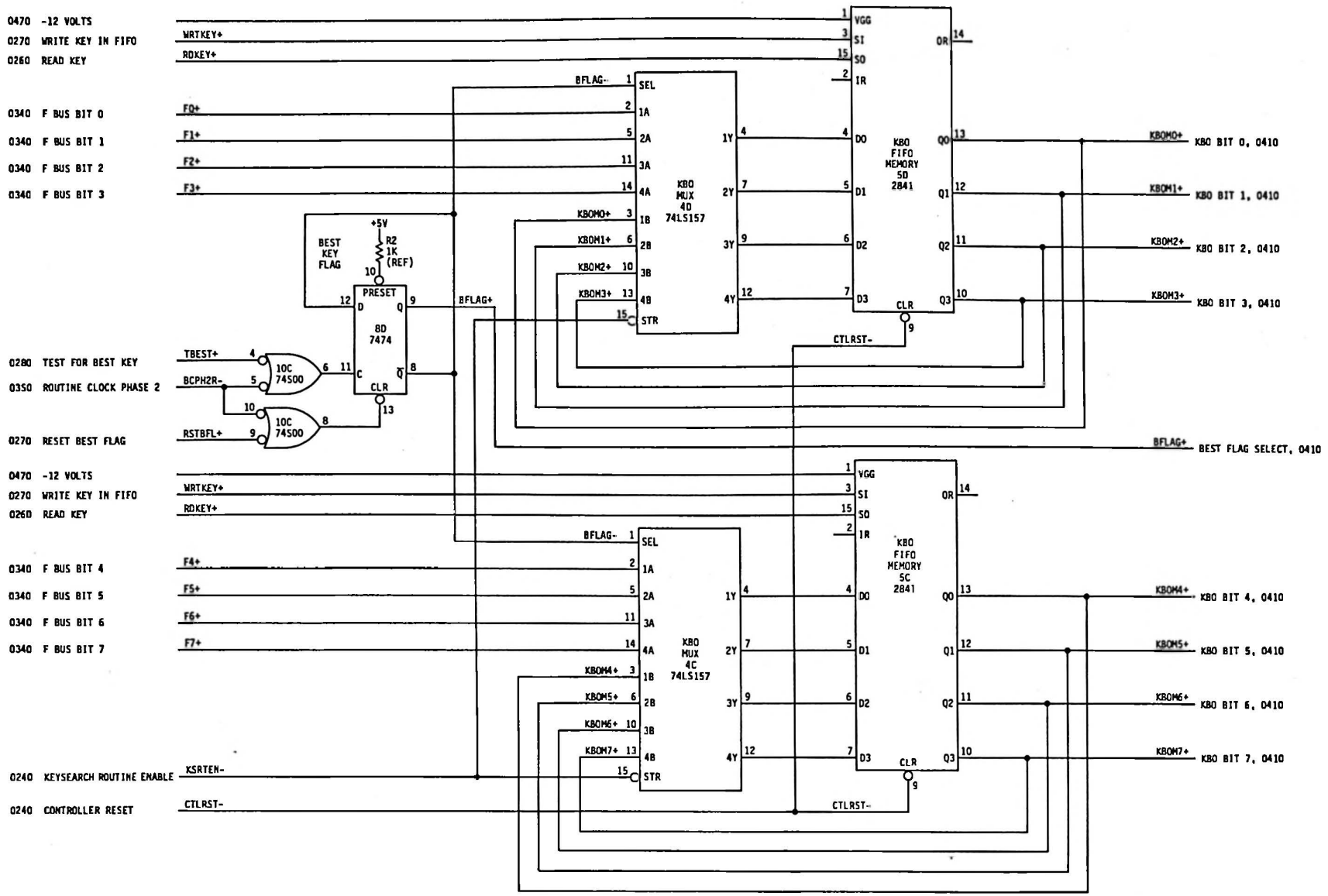

0240 CLOCK PHASE 2
0250 ROUTINE ENABLE
BCPH2+
ROUTEN-
3P 74S02
BCPH2R-
ROUTINE CLOCK PHASE TWO, 0380, 0400
0330 DMA STROBE
0340 MEMORY DATA BIT 0
0340 MEMORY DATA BIT 1
0340 MEMORY DATA BIT 2
0340 MEMORY DATA BIT 3
0240 RESET ROUTINE
DMASTB-
MD00+
MD01+
MD02+
MD03+
RROUT-
CLK
CLR
G BUS REGISTER 1K 74175
G0+
G1+
G2+
G3+
G REG BIT 0, 0420, 0430, 0440
G REG BIT 1, 0420, 0430, 0440
G REG BIT 2, 0420, 0430, 0440
G REG BIT 3, 0420, 0430, 0440
0330 DMA STROBE
0340 MEMORY DATA BIT 4
0340 MEMORY DATA BIT 5
0340 MEMORY DATA BIT 6
0340 MEMORY DATA BIT 7
0240 RESET ROUTINE
DMASTB-
MD04+
MD05+
MD06+
MD07+
RROUT-
CLK
CLR
G BUS REGISTER 1E 74175
G4+
G5+
G6+
G7+
G REG BIT 4, 0420, 0430, 0440
G REG BIT 5, 0420, 0430, 0440
G REG BIT 6, 0420, 0430, 0440
G REG BIT 7, 0420, 0430, 0440

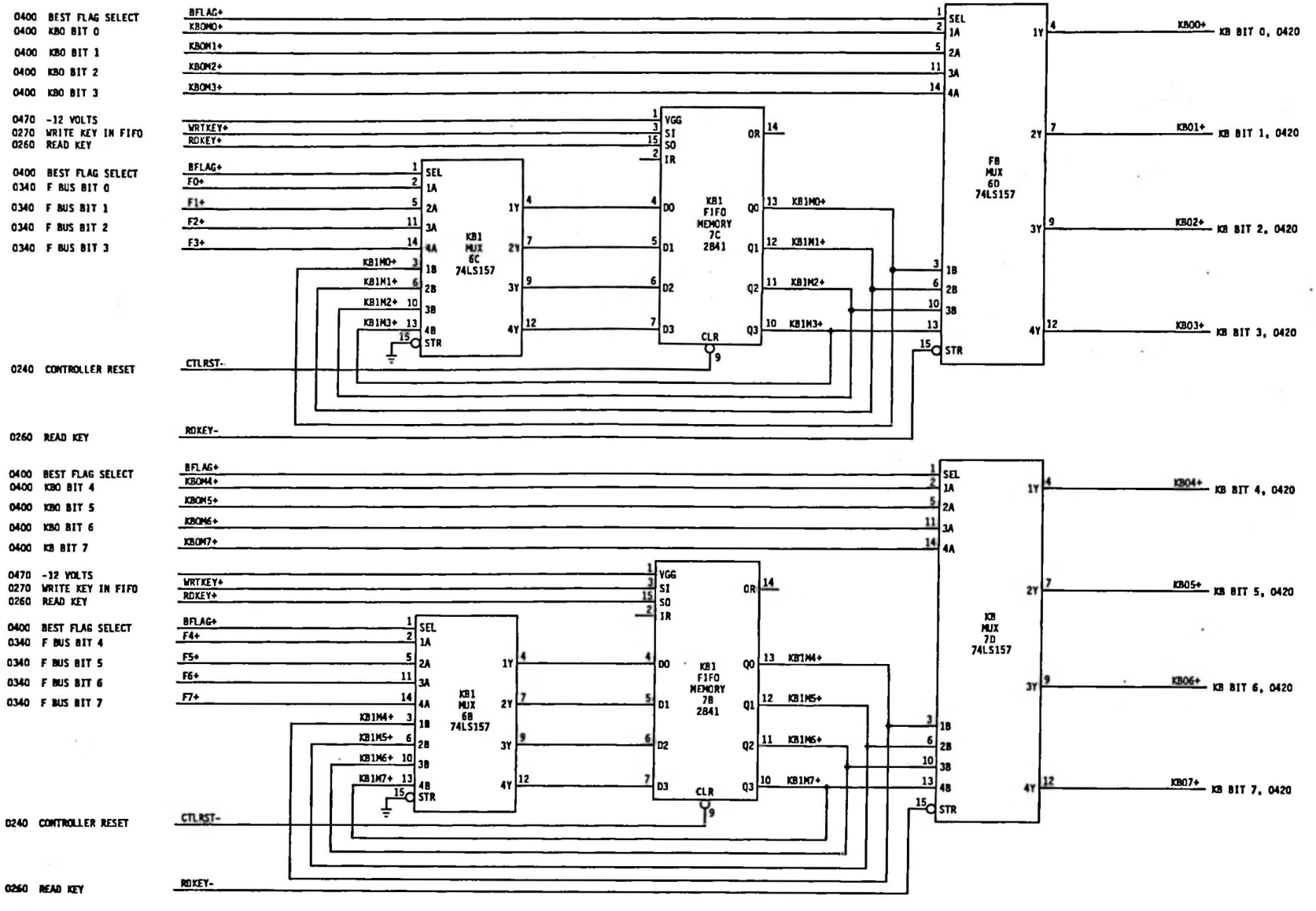

0420 DA BUS BIT 0
0420 DA BUS BIT 1
0420 DA BUS BIT 2
0420 DA BUS BIT 3
0240 CLOCK PHASE 2
0280 LOAD A REG LOW BYTE
0420 DA BUS BIT 4
0420 DA BUS BIT 5
0420 DA BUS BIT 6
0420 DA BUS BIT 7
DA0+
DA1+
DA2+
DA3+
BCPH2-
LALB+
DA4+
DA5+
DA6+
DA7+
5K 7400
A BUS REGISTER 7H 74175
A BUS REGISTER 7K 74175
R8 1K (REF)
R11 1K
+5V
CLK
CLR
A0+ A BUS BIT 0, 0380
A1+ A BUS BIT 1, 0380
A2+ A BUS BIT 2, 0380
A3+ A BUS BIT 3, 0380
A4+ A BUS BIT 4, 0380
A5+ A BUS BIT 5, 0380
A6+ A BUS BIT 6, 0380
A7+ A BUS BIT 7, 0380
0430 DA BUS BIT 8
0430 DA BUS BIT 9
0430 DA BUS BIT 10
0430 DA BUS BIT 11
0280 LOAD A REG HIGH BYTE
0240 CLOCK PHASE 2
0430 DA BUS BIT 12
0430 DA BUS BIT 13
0430 DA BUS BIT 14
0430 DA BUS BIT 15
DA8+
DA9+
DA10+
DA11+
LAHB+
BCPH2-
DA12+
DA13+
DA14+
DA15+
5K 7400
A BUS REGISTER 9H 74175
A BUS REGISTER 7M 74175
R8 1K (REF)
R11 1K (REF)
+5V
CLK
CLR
A8+ A BUS BIT 8, 0390
A9+ A BUS BIT 9, 0390
A10+ A BUS BIT 10, 0390
A11+ A BUS BIT 11, 0390
A12+ A BUS BIT 12, 0390
A13+ A BUS BIT 13, 0390
A14+ A BUS BIT 14, 0390
A15+ A BUS BIT 15, 0390


0270 INCREMENT B
0240 CLOCK PHASE 2
0420 DA BUS BIT 0
0420 DA BUS BIT 1
0420 DA BUS BIT 2
0420 DA BUS BIT 3
0290 SET B REGISTER TO ZERO
0280 LOAD B REG LOW BYTE
INCB+
BCPH2+
DA0+
DA1+
DA2+
DA3+
ZEROB-
LBLB-
CLK CET CEP
A
B
C
D
CLR
LD
B BUS REGISTER 7F 74163
QA QB QC QD
CARRY
15
B0+ B BUS BIT 0, 0380
B1+ B BUS BIT 1, 0380
B2+ B BUS BIT 2, 0380
B3+ B BUS BIT 3, 0380
0420 DA BUS BIT 4
0420 DA BUS BIT 5
0420 DA BUS BIT 6
0420 DA BUS BIT 7
DA4+
DA5+
DA6+
DA7+
B BUS REGISTER 6K 74163
B4+ B BUS BIT 4, 0380
B5+ B BUS BIT 5, 0380
B6+ B BUS BIT 6, 0380
B7+ B BUS BIT 7, 0380
0430 DA BUS BIT 8
0430 DA BUS BIT 9
0430 DA BUS BIT 10
0430 DA BUS BIT 11
0280 LOAD B REG HIGH BYTE
DA8+
DA9+
DA10+
DA11+
LBHB-
B BUS REGISTER 8H 74163
B8+ B BUS BIT 8, 0390
B9+ B BUS BIT 9, 0390
B10+ B BUS BIT 10, 0390
B11+ B BUS BIT 11, 0390
0430 DA BUS BIT 12
0430 DA BUS BIT 13
0430 DA BUS BIT 14
0430 DA BUS BIT 15
DA12+
DA13+
DA14+
DA15+
B BUS REGISTER 6M 74163
B12+ B BUS BIT 12, 0390
B13+ B BUS BIT 13, 0390
B14+ B BUS BIT 14, 0390
B15+ B BUS BIT 15, 0390


0280 WRITE IN SCRATCH PAD
0350 ROUTINE CLOCK PHASE 2
WRTSP+
BCPH2R-
10C 74S00
ESPW-
ENAB SCRATCH PAD WRITE, 0390
0260 ROM BIT 27
0260 ROM BIT 28
0260 ROM BIT 29
0260 ROM BIT 30
0260 ROM BIT 31
0360 A BUS BIT 0
0360 A BUS BIT 1
0360 A BUS BIT 2
0360 A BUS BIT 3
0370 B BUS BIT 0
0370 B BUS BIT 1
0370 B BUS BIT 2
0370 B BUS BIT 3
R27+
R28+
R29+
R30+
R31+
A0+
A1+
A2+
A3+
B0+
B1+
B2+
B3+
ALU 8K 74S181
CIN
M
S0
S1
S2
S3
A0
A1
A2
A3
B0
B1
B2
B3
F0
F1
F2
F3
A=B
CO
11H 74S04
SCRATCH PAD RAM 10P 74S189
R/W
CE
P
G
D1
D2
D3
D4
Y1
Y2
Y3
Y4
SPEN-
RO+
R1+
R2+
R3+
SP00+
SP01+
SP02+
SP03+
SCRATCH PAD BIT 0, 0420
SCRATCH PAD BIT 1, 0420
SCRATCH PAD BIT 2, 0420
SCRATCH PAD BIT 3, 0420
0270 SCRATCH PAD ENABLE
0290 ROM BIT 0
0290 ROM BIT 1
0290 ROM BIT 2
0290 ROM BIT 3
0260 ROM BIT 27
0260 ROM BIT 28
0260 ROM BIT 29
0260 ROM BIT 30
0260 ROM BIT 31
0360 A BUS BIT 4
0360 A BUS BIT 5
0360 A BUS BIT 6
0360 A BUS BIT 7
0370 B BUS BIT 4
0370 B BUS BIT 5
0370 B BUS BIT 6
0370 B BUS BIT 7
A4+
A5+
A6+
A7+
B4+
B5+
B6+
B7+
ALU 10K 74S181
11K 74S04
SCRATCH PAD RAM 10N 74S189
SP04+
SP05+
SP06+
SP07+
SCRATCH PAD BIT 4, 0420
SCRATCH PAD BIT 5, 0420
SCRATCH PAD BIT 6, 0420
SCRATCH PAD BIT 7, 0420
AUCOMP+
ARITHMETIC UNIT COMPARE, 0390
CRYOUT+
CARRY OUT, 0390


0380 ENAB SCRATCH PAD WRITE
ESPW-
0380 ARITHMETIC UNIT COMPARE
AUCOMP+
0380 CARRY OUT
CRYOUT+
0260 ROM BIT 27
0260 ROM BIT 28
0260 ROM BIT 29
0260 ROM BIT 30
0260 ROM BIT 31
0360 A BUS BIT 8
0360 A BUS BIT 9
0360 A BUS BIT 10
0360 A BUS BIT 11
0370 B BUS BIT 8
0370 B BUS BIT 9
0370 B BUS BIT 10
0370 B BUS BIT 11
R27+
R28-1+
R29-1+
R30-1+
R31-1+
A8+
A9+
A10+
A11+
B8+
B9+
B10+
B11+
ALU 8M 74S181
CIN
CO
A=B
11M 74S04
11K 74S04
SCRATCH PAD RAM 11N 74S189
R/W
CE
SP08+ SCRATCH PAD BIT 8, 0430
SP09+ SCRATCH PAD BIT 9, 0430
SP10+ SCRATCH PAD BIT 10, 0430
SP11+ SCRATCH PAD BIT 11, 0430
0270 SCRATCH PAD ENABLE
SPEN-
0290 ROM BUS BIT 0
0290 ROM BUS BIT 1
0290 ROM BUS BIT 2
0290 ROM BUS BIT 3
R0+
R1+
R2+
R3+
0260 ROM BUS BIT 27
0260 ROM BUS BIT 28
0260 ROM BUS BIT 29
0260 ROM BUS BIT 30
0260 ROM BUS BIT 31
0360 A BUS BIT 12
0360 A BUS BIT 13
0360 A BUS BIT 14
0360 A BUS BIT 15
0370 B BUS BIT 12
0370 B BUS BIT 13
0370 B BUS BIT 14
0370 B BUS BIT 15
R27+
R28-1+
R29-1+
R30-1+
R31-1+
A12+
A13+
A14+
A15+
B12+
B13+
B14+
B15+
ALU 10M 74S181
SCRATCH PAD RAM 11P 74S189
SP12+ SCRATCH PAD BIT 12, 0430
SP13+ SCRATCH PAD BIT 13, 0430
SP14+ SCRATCH PAD BIT 14, 0430
SP15+ SCRATCH PAD BIT 15, 0430
AUCOMP+ ARITMETIC UNIT COMPARE, 0260

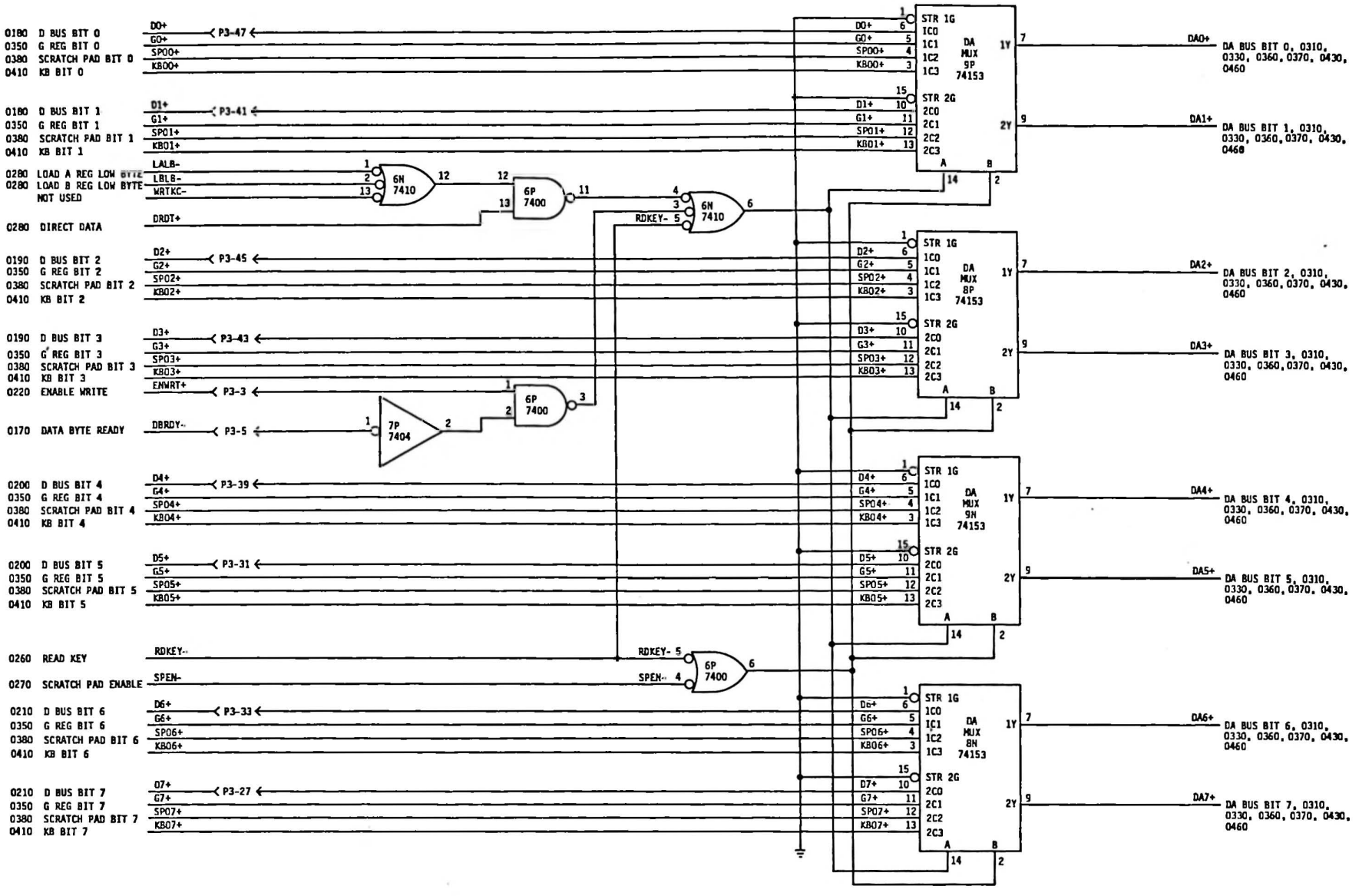

0470 -12 VOLTS
0270 WRITE KEY IN FIFO
0260 READ KEY
0340 F BUS BIT 0
0340 F BUS BIT 1
0340 F BUS BIT 2
0340 F BUS BIT 3
0280 TEST FOR BEST KEY
0350 ROUTINE CLOCK PHASE 2
0270 RESET BEST FLAG
0470 -12 VOLTS
0270 WRITE KEY IN FIFO
0260 READ KEY
0340 F BUS BIT 4
0340 F BUS BIT 5
0340 F BUS BIT 6
0340 F BUS BIT 7
0240 KEYSEARCH ROUTINE ENABLE
0240 CONTROLLER RESET
WRTKEY+
RDKEY+
F0+
F1+
F2+
F3+
F4+
F5+
F6+
F7+
TBEST+
BCPH2R-
RSTBFL+
KSRTEN-
CTLRST-
BFLAG+
BFLAG-
BEST KEY FLAG
+5V
R2 1K (REF)
PRESET
8D 7474
10C 74S00
10C 74S00
KBO MUX 4D 74LS157
KBO MUX 4C 74LS157
KBO FIFO MEMORY 5D 2841
KBO FIFO MEMORY 5C 2841
KBOM0+
KBOM1+
KBOM2+
KBOM3+
KBOM4+
KBOM5+
KBOM6+
KBOM7+
KBO BIT 0, 0410
KBO BIT 1, 0410
KBO BIT 2, 0410
KBO BIT 3, 0410
KBO BIT 4, 0410
KBO BIT 5, 0410
KBO BIT 6, 0410
KBO BIT 7, 0410
BEST FLAG SELECT, 0410

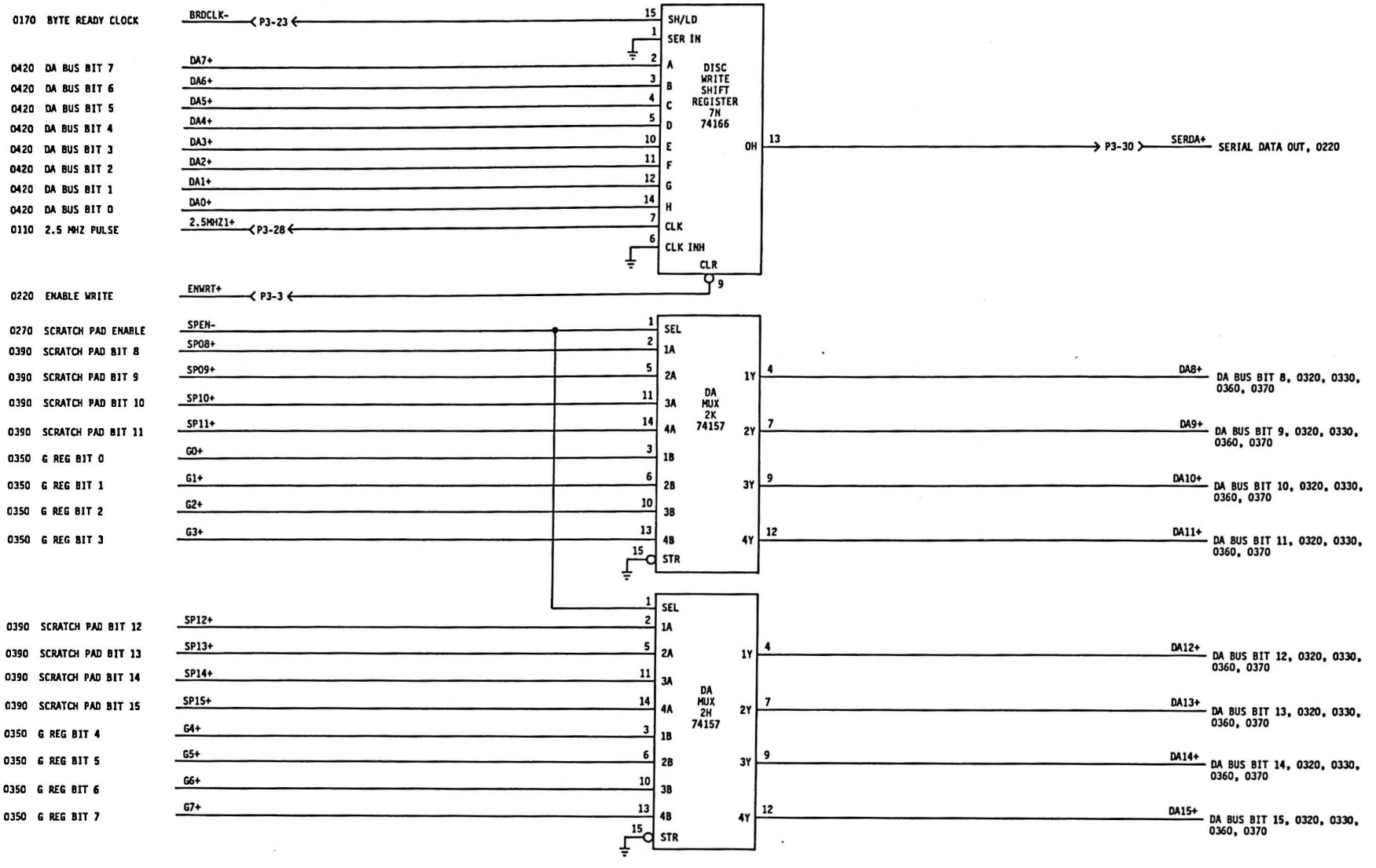


LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

KB1 REGISTER AND KB MUX

DMA LOGIC MICROPROCESSOR BOARD
0410

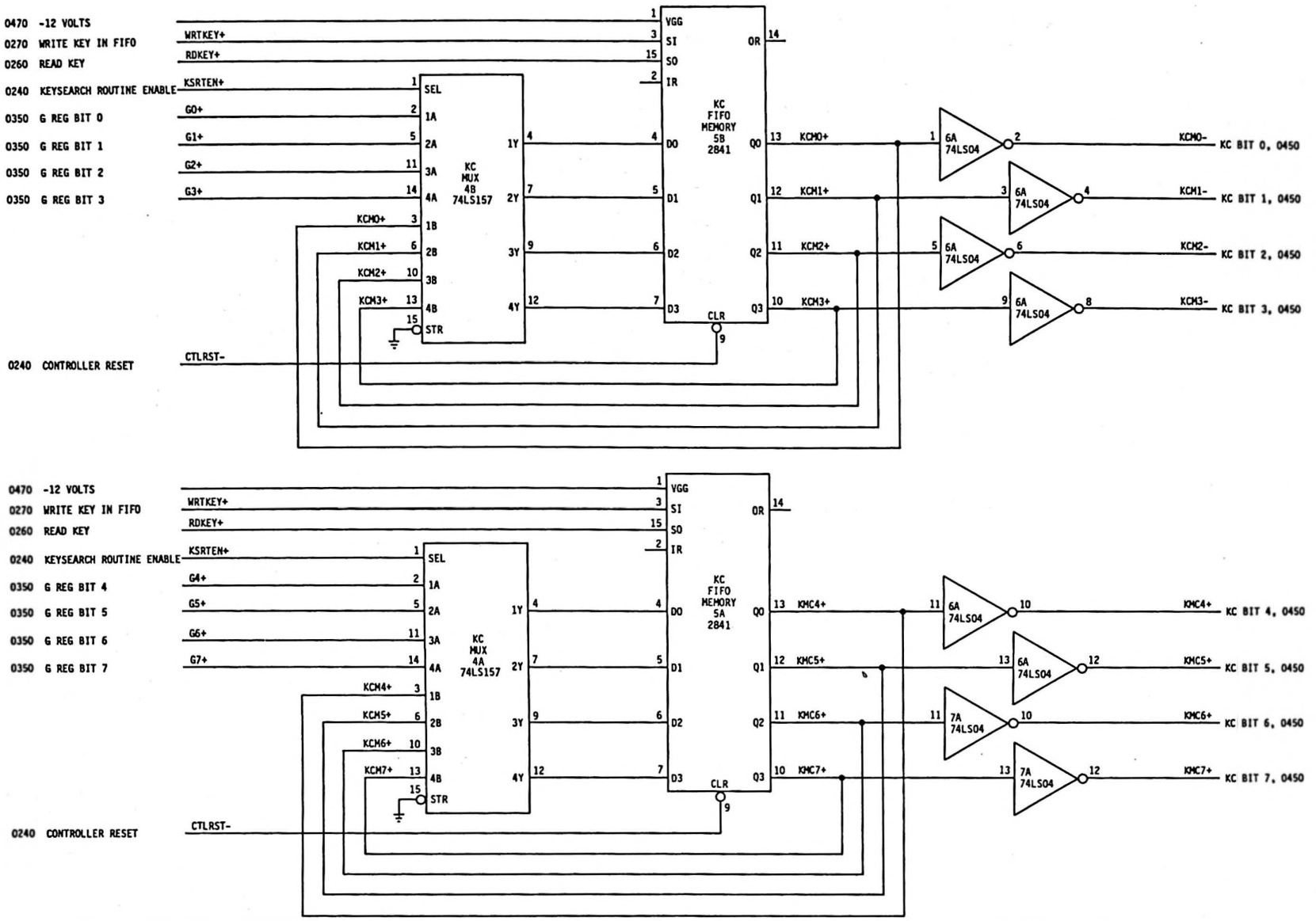

0180 D BUS BIT 0
0350 G REG BIT 0
0380 SCRATCH PAD BIT 0
0410 KB BIT 0
D0+
G0+
SP00+
KB00+
P3-47
0180 D BUS BIT 1
0350 G REG BIT 1
0380 SCRATCH PAD BIT 1
0410 KB BIT 1
D1+
G1+
SP01+
KB01+
P3-41
0280 LOAD A REG LOW BYTE
0280 LOAD B REG LOW BYTE
NOT USED
LALB-
LBLB-
WRTKC-
6N 7410
6P 7400
0280 DIRECT DATA
DRDT+
0190 D BUS BIT 2
0350 G REG BIT 2
0380 SCRATCH PAD BIT 2
0410 KB BIT 2
D2+
G2+
SP02+
KB02+
P3-45
0190 D BUS BIT 3
0350 G REG BIT 3
0380 SCRATCH PAD BIT 3
0410 KB BIT 3
0220 ENABLE WRITE
D3+
G3+
SP03+
KB03+
ENWRT+
P3-43
P3-3
0170 DATA BYTE READY
DBRDY-
P3-5
7P 7404
0200 D BUS BIT 4
0350 G REG BIT 4
0380 SCRATCH PAD BIT 4
0410 KB BIT 4
D4+
G4+
SP04+
KB04+
P3-39
0200 D BUS BIT 5
0350 G REG BIT 5
0380 SCRATCH PAD BIT 5
0410 KB BIT 5
D5+
G5+
SP05+
KB05+
P3-31
0260 READ KEY
0270 SCRATCH PAD ENABLE
RDKEY-
SPEN-
RDKEY- 5
SPEN- 4
0210 D BUS BIT 6
0350 G REG BIT 6
0380 SCRATCH PAD BIT 6
0410 KB BIT 6
D6+
G6+
SP06+
KB06+
P3-33
0210 D BUS BIT 7
0350 G REG BIT 7
0380 SCRATCH PAD BIT 7
0410 KB BIT 7
D7+
G7+
SP07+
KB07+
P3-27
STR 1G
1C0
1C1
1C2
1C3
DA MUX 9P 74153
STR 2G
2C0
2C1
2C2
2C3
1Y
2Y
A
B
DA0+
DA BUS BIT 0, 0310, 0330, 0360, 0370, 0430, 0460
DA1+
DA BUS BIT 1, 0310, 0330, 0360, 0370, 0430, 0460
DA2+
DA BUS BIT 2, 0310, 0330, 0360, 0370, 0430, 0460
DA3+
DA BUS BIT 3, 0310, 0330, 0360, 0370, 0430, 0460
DA4+
DA BUS BIT 4, 0310, 0330, 0360, 0370, 0430, 0460
DA5+
DA BUS BIT 5, 0310, 0330, 0360, 0370, 0430, 0460
DA6+
DA BUS BIT 6, 0310, 0330, 0360, 0370, 0430, 0460
DA7+
DA BUS BIT 7, 0310, 0330, 0360, 0370, 0430, 0460

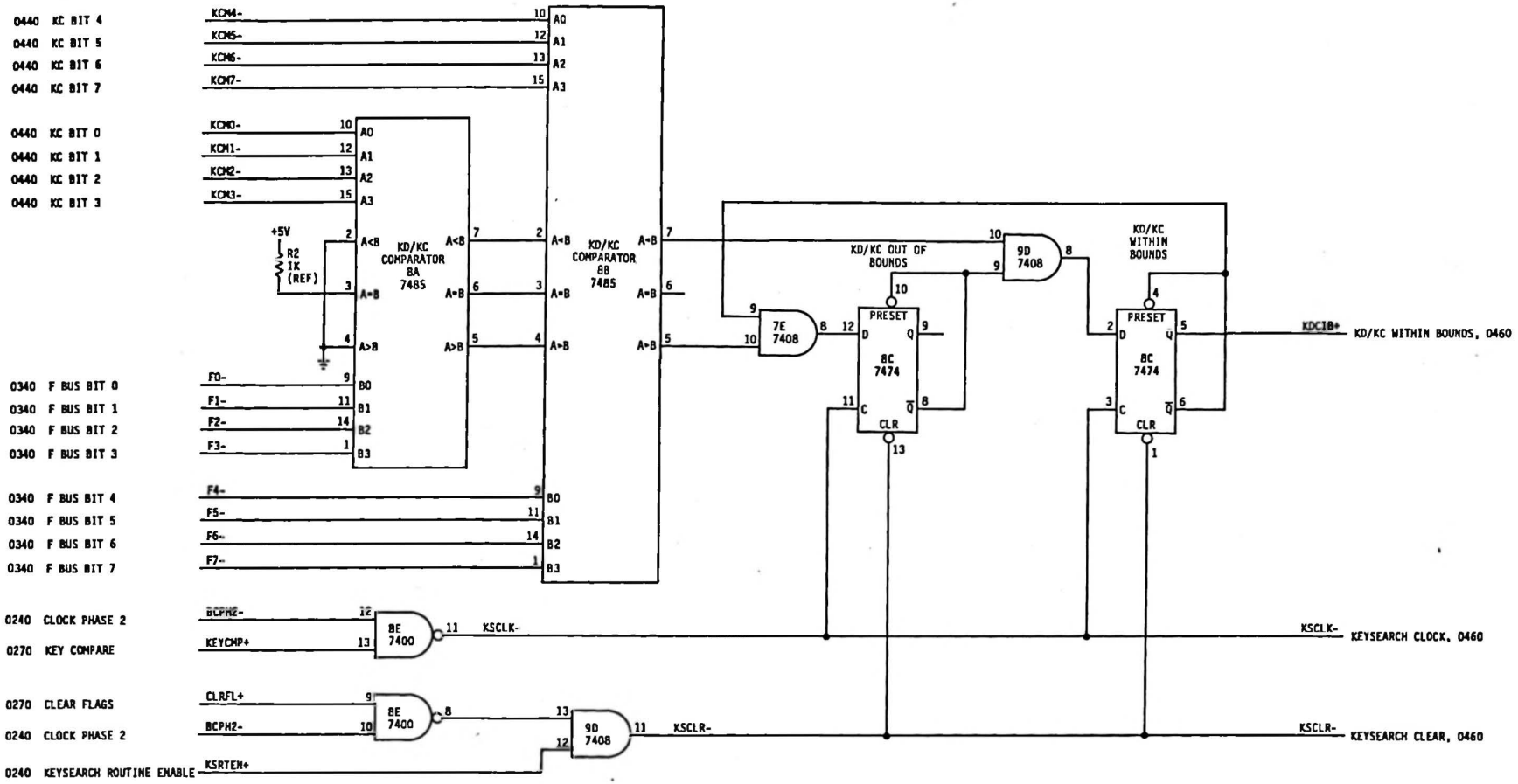


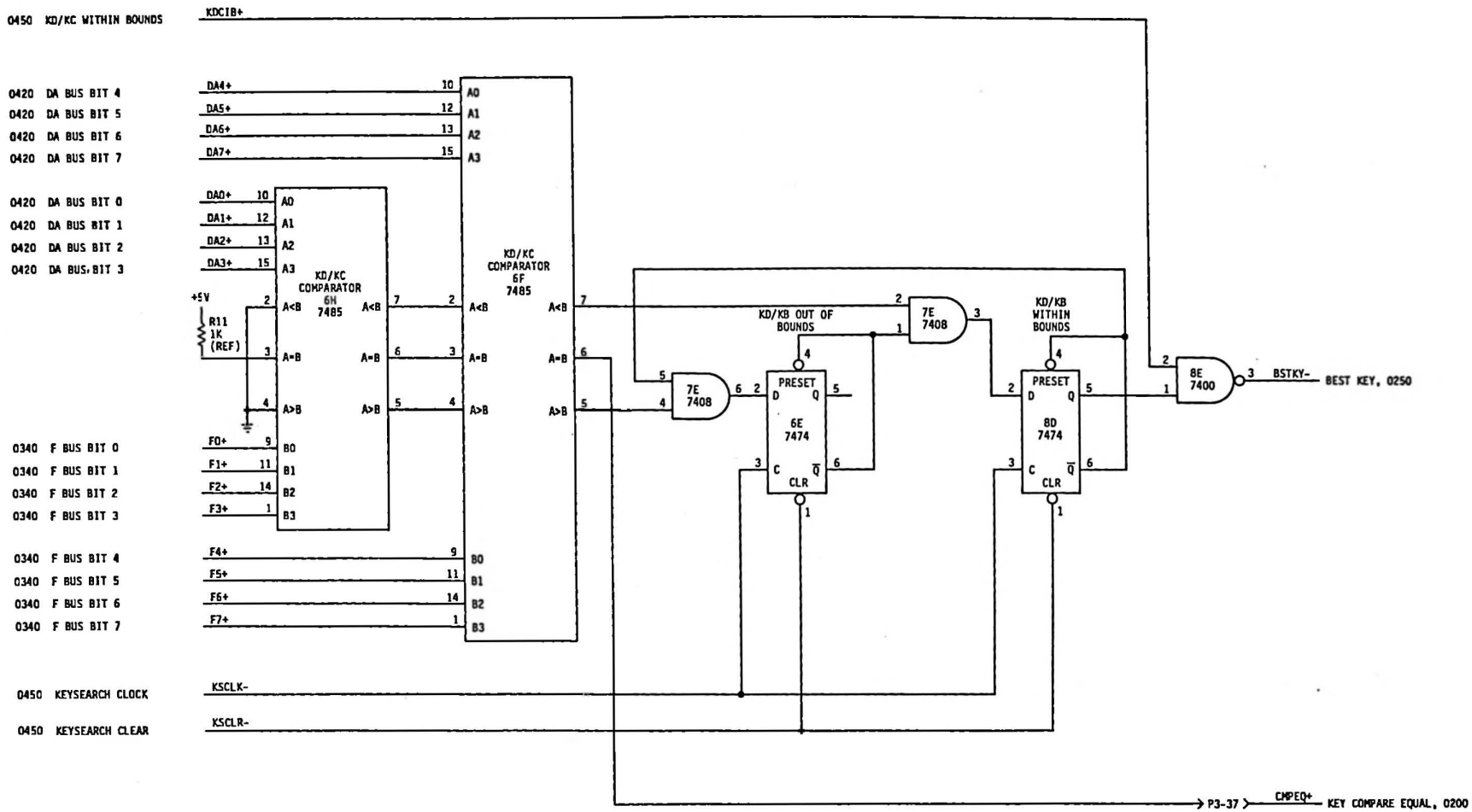
LD 2003
DMA/DISC STORAGE UNIT CONTROLLER

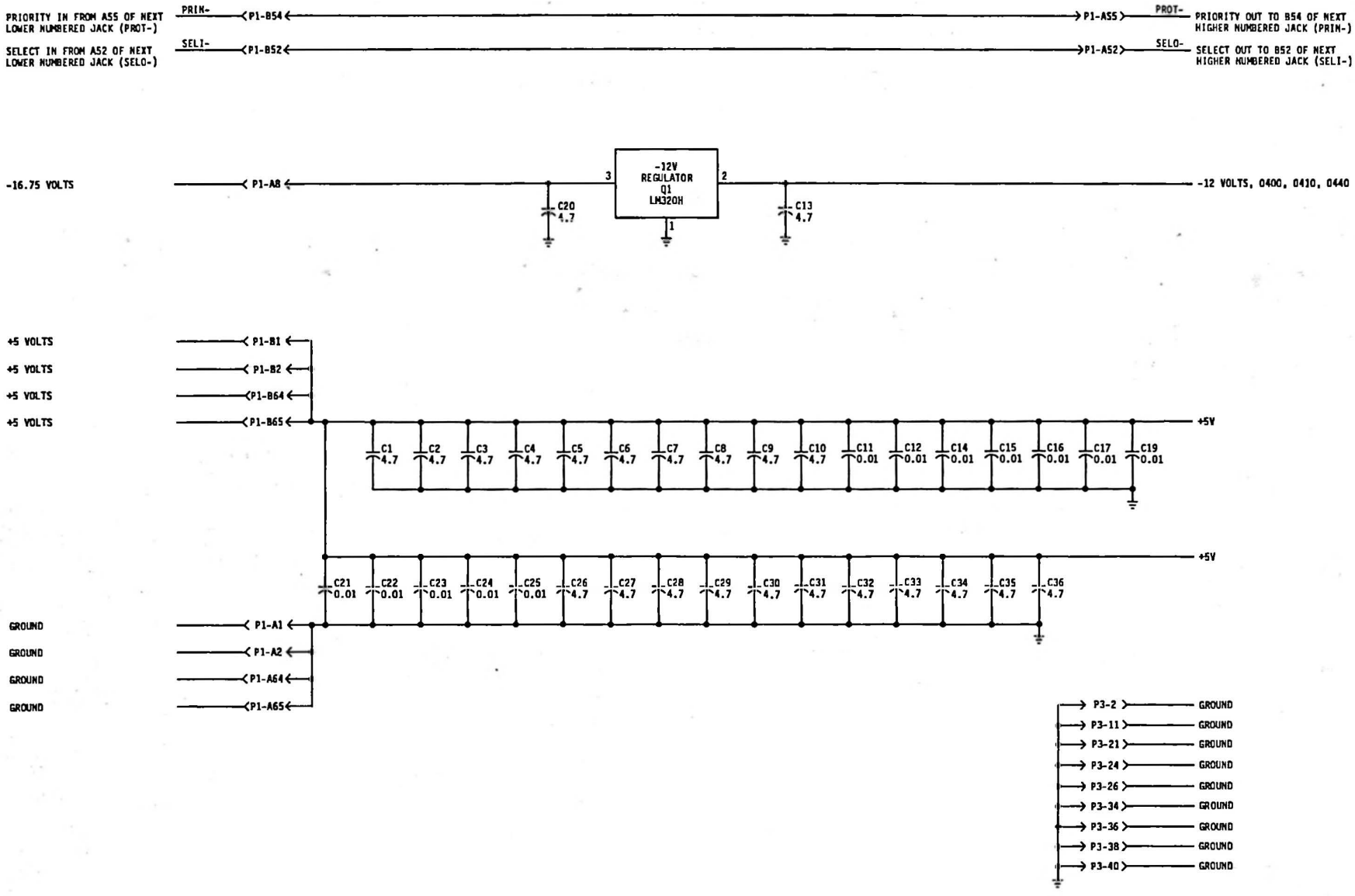
DA BUS HIGH ORDER BYTE AND DISC SERIAL WRITE

DMA LOGIC MICROPROCESSOR BOARD
0430


0470 -12 VOLTS
0270 WRITE KEY IN FIFO
0260 READ KEY
0240 KEYSEARCH ROUTINE ENABLE
0350 G REG BIT 0
0350 G REG BIT 1
0350 G REG BIT 2
0350 G REG BIT 3
0240 CONTROLLER RESET
WRTKEY+
RDKEY+
KSRTEN+
G0+
G1+
G2+
G3+
CTLRST-
KC MUX 4B 74LS157
KC FIFO MEMORY 5B 2841
KCM0+
KCM1+
KCM2+
KCM3+
KCM0-
KCM1-
KCM2-
KCM3-
6A 74LS04
KC BIT 0, 0450
KC BIT 1, 0450
KC BIT 2, 0450
KC BIT 3, 0450
0470 -12 VOLTS
0270 WRITE KEY IN FIFO
0260 READ KEY
0240 KEYSEARCH ROUTINE ENABLE
0350 G REG BIT 4
0350 G REG BIT 5
0350 G REG BIT 6
0350 G REG BIT 7
0240 CONTROLLER RESET
WRTKEY+
RDKEY+
KSRTEN+
G4+
G5+
G6+
G7+
CTLRST-
KC MUX 4A 74LS157
KC FIFO MEMORY 5A 2841
KCM4+
KCM5+
KCM6+
KCM7+
KMC4+
KMC5+
KMC6+
KMC7+
6A 74LS04
7A 74LS04
KC BIT 4, 0450
KC BIT 5, 0450
KC BIT 6, 0450
KC BIT 7, 0450


0440 KC BIT 4
0440 KC BIT 5
0440 KC BIT 6
0440 KC BIT 7
0440 KC BIT 0
0440 KC BIT 1
0440 KC BIT 2
0440 KC BIT 3
KCM4-
KCM5-
KCM6-
KCM7-
KCM0-
KCM1-
KCM2-
KCM3-
+5V
R2
1K
(REF)
KD/KC COMPARATOR 8A 7485
KD/KC COMPARATOR 8B 7485
A<B
A=B
A>B
A0
A1
A2
A3
B0
B1
B2
B3
0340 F BUS BIT 0
0340 F BUS BIT 1
0340 F BUS BIT 2
0340 F BUS BIT 3
0340 F BUS BIT 4
0340 F BUS BIT 5
0340 F BUS BIT 6
0340 F BUS BIT 7
F0-
F1-
F2-
F3-
F4-
F5-
F6-
F7-
7E 7408
KD/KC OUT OF BOUNDS
9D 7408
KD/KC WITHIN BOUNDS
PRESET
8C 7474
CLR
KDC1B+
KD/KC WITHIN BOUNDS, 0460
0240 CLOCK PHASE 2
0270 KEY COMPARE
BCPH2-
KEYCMP+
8E 7400
KSCLK-
KSCLK-
KEYSEARCH CLOCK, 0460
0270 CLEAR FLAGS
0240 CLOCK PHASE 2
CLRFL+
BCPH2-
KSCLR-
KSCLR-
KEYSEARCH CLEAR, 0460
0240 KEYSEARCH ROUTINE ENABLE
KSRTEN+


0450 KD/KC WITHIN BOUNDS
KDCIB+
0420 DA BUS BIT 4
0420 DA BUS BIT 5
0420 DA BUS BIT 6
0420 DA BUS BIT 7
DA4+
DA5+
DA6+
DA7+
A0
A1
A2
A3
0420 DA BUS BIT 0
0420 DA BUS BIT 1
0420 DA BUS BIT 2
0420 DA BUS BIT 3
DA0+
DA1+
DA2+
DA3+
KD/KC COMPARATOR 6H 7485
KD/KC COMPARATOR 6F 7485
A<B
A=B
A>B
+5V
R11 1K (REF)
0340 F BUS BIT 0
0340 F BUS BIT 1
0340 F BUS BIT 2
0340 F BUS BIT 3
F0+
F1+
F2+
F3+
B0
B1
B2
B3
0340 F BUS BIT 4
0340 F BUS BIT 5
0340 F BUS BIT 6
0340 F BUS BIT 7
F4+
F5+
F6+
F7+
0450 KEYSEARCH CLOCK
KSCLK-
0450 KEYSEARCH CLEAR
KSCLR-
KD/KB OUT OF BOUNDS
7E 7408
KD/KB WITHIN BOUNDS
PRESET
6E 7474
8D 7474
CLR
8E 7400
BSTKY-
BEST KEY, 0250
P3-37
CMPEQ+
KEY COMPARE EQUAL, 0200



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DMA/DISC STORAGE UNIT CONTROLLER

POWER DISTRIBUTION

DMA LOGIC MICROPROCESSOR BOARD
0470