TM 2002

TECHNICAL MANUAL
for
DISC STORAGE UNIT
CONTROLLER
Part No. 900280

November 1, 1974

basic / four corporation
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4-1 thru 4-15	Original
5-1 thru 5-4	Original

TABLE OF CONTENTS

SECTION 3. THEORY OF OPERATION (continued)

LIST OF TABLES

LIST OF ILLUSTRATIONS

Section 1

GENERAL DESCRIPTION

1.1 SCOPE

This manual contains general description, installation procedures, theory of operation, and maintenance data for the DMA Disc Storage Unit Controller, Part Number 900280, manufactured by the Basic/Four Corporation, 18552 Mac Arthur Boulevard, Santa Ana, California 92707. The DMA/Disc Storage Unit Controller (called the DMA/disc drive controller) is an integral part of the BASIC/FOUR® data processing systems. The logic diagrams for the DMA/Disc Storage Unit Controller are in LD 2002.

1.2 PURPOSE AND FUNCTIONAL DESCRIPTION (figures 1-1 and 1-2)

The DMA/disc drive controller serves as the communications link between the Central Processing Unit (CPU) and up to four Disc Storage Units. Each of the Disc Storage Units (called disc drives) connected to a controller must be functionally identical. The direct memory access (DMA) channel included in the controller is used for communicating with the CPU. The DMA channel is a high-speed port that connects the core memory of the CPU to the disc drive controller, permitting transfer of a block of data bytes between memory and the disc drives. The DMA channel requires minimum attention from the CPU program during a data transfer. Program instructions are used to set up the channel for a block transfer, but, thereafter, all data transfers occur automatically without program intervention.

During a single block transfer operation (to or from the CPU), up to 5,280 eight-bit data bytes can be transferred. To initiate a block transfer, the CPU first initializes the DMA channel, and issues the appropriate device orders to the DMA/disc drive controller, followed by information bytes specifying the disc drive unit and cylinder (track) number address involved in the data transfer. The controller returns disc drive status information to the CPU. After checking status, the CPU issues a read or write device order, followed by a sector address information byte that specifies the disc (fixed or removable), and disc head (upper or lower) to be used for the read or write operation, and also specifying the starting sector of the previously designated cylinder. The controller again returns status information.

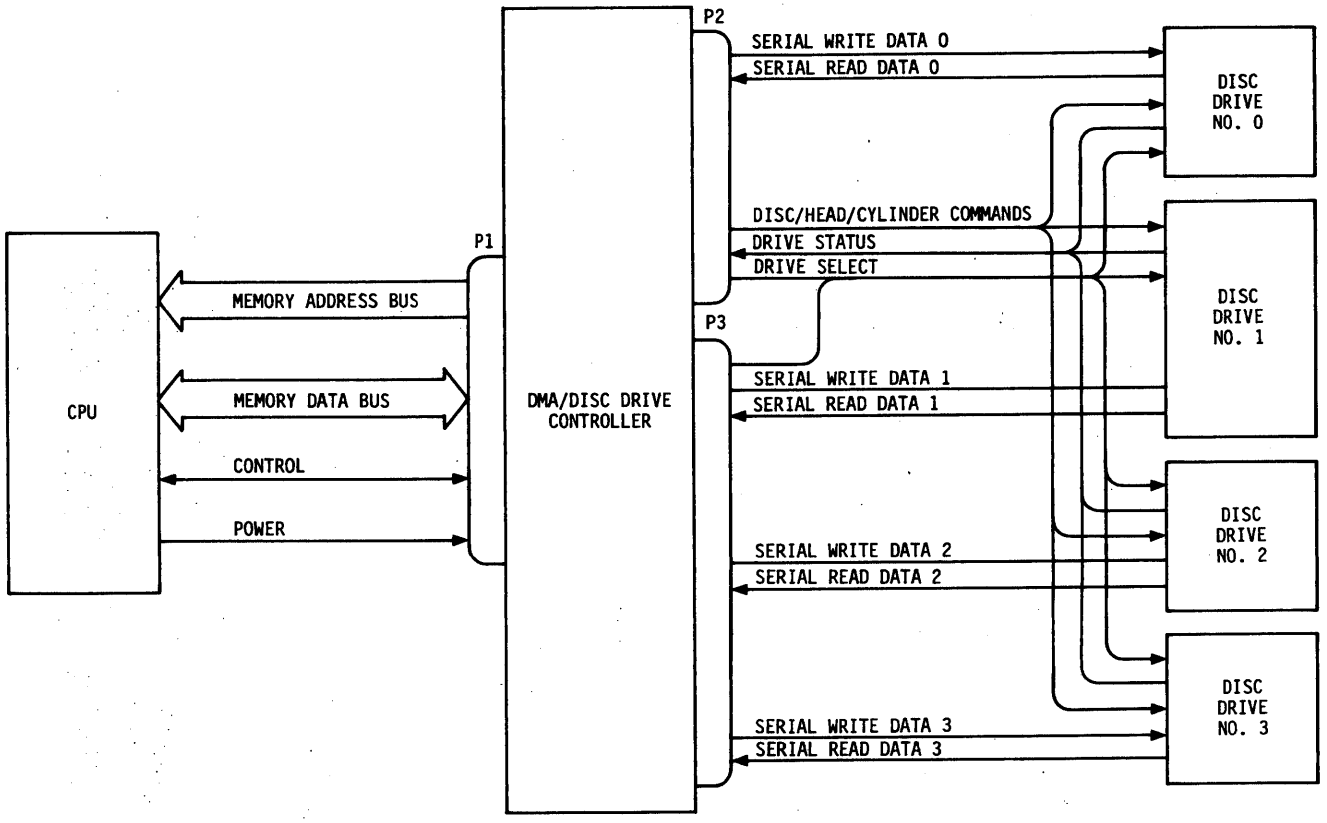


Figure 1-1. DMA/Disc Drive Controller, Simplified Block Diagram

If status is correct, the controller executes the data transfer operation, during which data is transferred from memory to the controller for writing on the disc, or data is read from the disc and supplied to the controller for transfer to CPU memory. At the completion of the data transfer, the controller issues an interrupt to the CPU, and the CPU program responds by again checking status. After status is checked, the CPU issues a reset status command to the controller, resetting the disc drive controller and the disc drive.

Figure 1-2 shows the relationship to the two prime functions of the DMA/Disc Drive Controller. The DMA channel contains all of the logic interface circuits for communication with the CPU except for output from the Disc Drive Controller to the CPU memory. The Disc Drive Controller contains all of the logic interface circuits for communication with the disc drive units. The four digit numbers on the signal flow lines indicate the page number of the logic diagram in LD 2002 where the signal is shown as an input/output. The blocks representing the DMA channel and the Disc Drive Controller reference block diagrams in Section 3 that expand signal flow in greater detail.

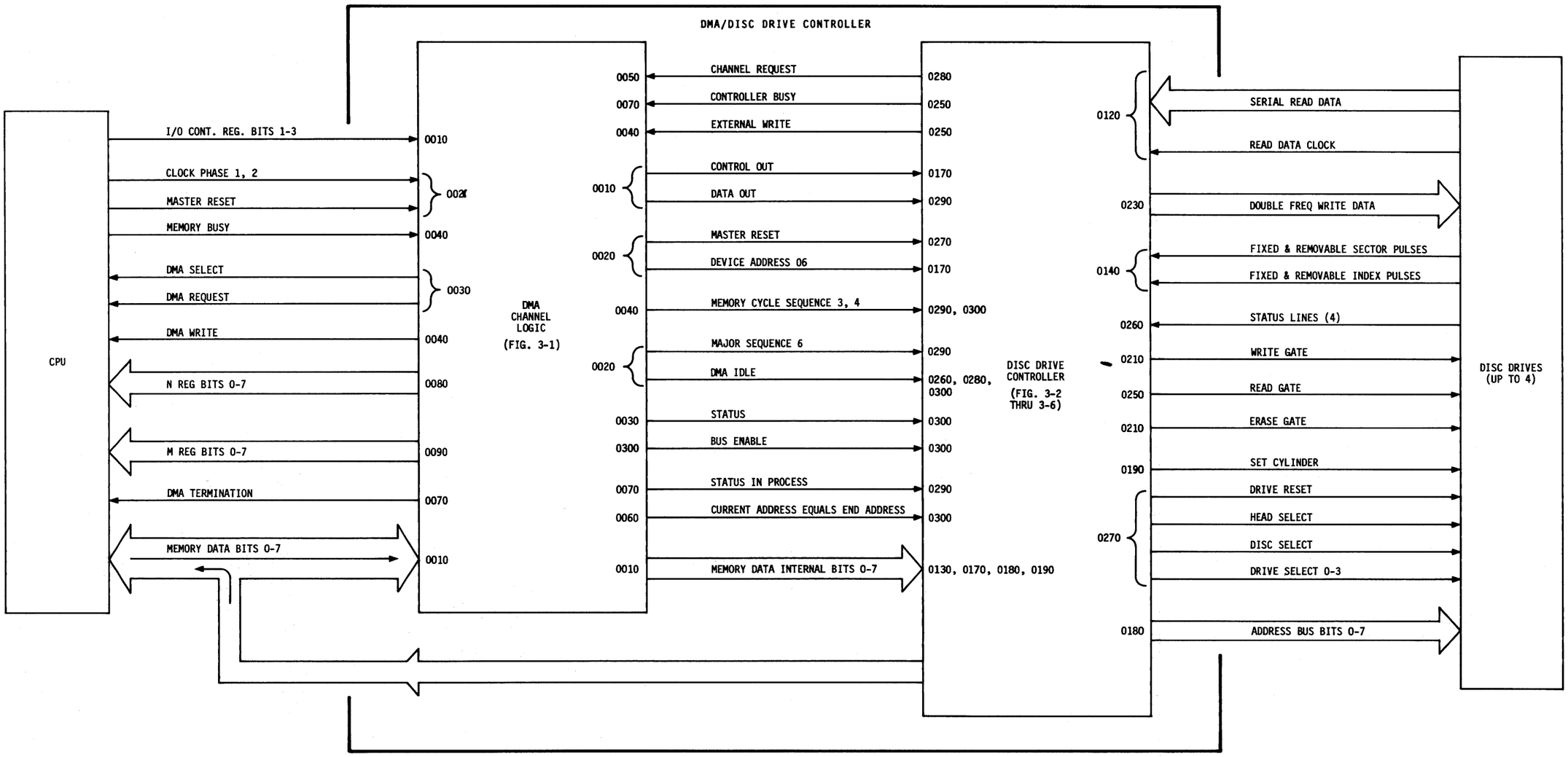


Figure 1-2. Overall Block Diagram

1.3 ELECTRICAL CHARACTERISTICS AND PERFORMANCE DATA

Table 1-1 lists the pertinent electrical characteristics and performance data for the DMA/disc drive controller.

Table 1-1. Electrical Characteristics and Performance Data

Parameter	Characteristic
Input Power Requirements	+5vdc, 3 amperes from CPU (supplied via connector P1 on circuit board)
Environmental:	
Ambient Temperature Range	0 to 50° C.
Relative Humidity	Up to 90% without condensation
Circuit Types	TTL and DTL integrated circuits (IC) used throughout
Internal Logic Levels	Logical 1 = +5vdc (nominal) logical 0 = 0vdc (nominal)
Logic Levels for CPU and Disc Drive Interfaces	Logical 1 = 0vdc (nominal) logical 0 = +3 to 5 vdc
Number of Types of Disc Drives	Up to four Model 2100 or Model 2200 Disc Storage Units can be handled by one controller.
Disc Recording Technology:	
Recording Format	Double-frequency write data (manchester coding)
Data Clock Frequency	6.24 MHz
Bit Density	2200 bits per inch
Bit Cell Time (nominal)	640 nanoseconds
Byte Size	8 bits
Data Transfer Rate	195 kilobytes/second
Disc Rotational Speed	1500 rpm
Number of Discs per Disc Drive	Two - one fixed disc and one removable disc, either of which can be accessed by the controller.
Track Density	100 tracks per inch or 200 tracks per inch.
Number of Tracks per Disc (both sides)	200, 400, or 800 depending on Model number.

Table 1-1. Electrical Characteristics and Performance Data (continued)

Parameter	Characteristic
Disc Recording Technology (continued)	
Number of Bit Cells per Track (nominal)	72,000
Number of Sectors per Track	48
Number of Data Bytes per Sector	110
Number of Data Bytes per Track	5,280
Number of Data Bytes per Disc	1,056,000 (200 tracks per disc), 2,112,000 (400 tracks per disc), or 4,224,000 (800 tracks per disc)
Number of Data Bytes per Disc Drive (two discs)	2,112,000 (200 tracks per disc), 4,224,000 (400 tracks per disc), or 8,448,000 (800 tracks per disc)
Access Times:	
Average Random Move	35 to 150 milliseconds
Average Rotational Delay	20 milliseconds
Average Latency Time	20 milliseconds

1.4 PHYSICAL DESCRIPTION

The DMA/disc drive controller is an 8.575 X 16.5-inch printed circuit board assembly containing integrated circuit (IC) elements. Each IC element is soldered into the board. The reference designation for each IC element consists of the row-column grid coordinates shown in figure 5-1. The reference designation consists of a combination of the column letter and the row number; for example, reference designator 4B is the fourth row location in column B. The numbers in each element box shown in figure 5-1 are the reference designation and the IC type number.

External connections are made to three connectors that are an integral part of the circuit board. Connector P1, which is installed in a mating receptacle in the CPU mainframe, connects the controller to the CPU. A cable assembly from the disc drive units is connected to connectors P2 and P3.

1.5 DATA FORMATS

This paragraph describes the data formats for the various types of data exchanged between the CPU and the controller, and also describes the format of the data written on the magnetic discs.

1.5.1 CPU OUTPUT DATA FORMATS (figure 1-3)

Figure 1-3 shows the various types of output data formats that can be present on the bi-directional MEMORY DATA bus from the CPU to the controller. Bit MEMORY DATA BIT 7 is the most significant bit (MSB), and bit MEMORY DATA BIT 0 is the least significant bit (LSB). As shown in figure 1-3, six types of output data bytes are sent to the controller.

The device order byte is accompanied by the CONTROL OUT code (001_2) in I/O CONTROL REG BITS 3-1 from the CPU. The presence of the CONTROL OUT code notifies the controller that a device order byte is on the MEMORY DATA lines. Although the device order byte is placed on the MEMORY DATA lines, it does not originate in the CPU memory, and a memory cycle is not performed to place the byte on the lines.

	BYTE TYPE	MEMORY DATA BIT 7	6	5	4	3	2	1	0
	DEVICE ORDER	DEVICE ORDER CODE			← DEVICE ADDRESS →				
INFORMATION BYTES	DRIVE SELECT	← NOT USED →						DRIVE SELECT CODE	
	CYLINDER ADDRESS	2^7 (128)	2^6 (64)	2^5 (32)	2^4 (16)	2^3 (8)	2^2 (4)	2^1 (2)	2^0 (1)
	DISC/ HEAD/ SECTOR	DISC SELECT 1 = FIXED 0 = REMOVABLE	HEAD SELECT 1 = LOWER 0 = UPPER	SECTOR ADDRESS 2^5 (32)	2^4 (16)	2^3 (8)	2^2 (4)	2^1 (2)	2^0 (1)
	WRITE DATA	← DATA →							
	BLOCK CONTROL	← STARTING OR ENDING ADDRESS →							

Figure 1-3. CPU Output Data Formats

The three types of information bytes (Drive Select, Cylinder Address, and Disc/Head/Sector) also originate outside of CPU memory. An information byte is accompanied by the DATA OUT code (010_2) in I/O CONTROL REG BITS 1-3 from the CPU. The presence of DATA OUT notifies the controller that an information byte is on the MEMORY DATA lines.

The Write Data and Block Control bytes are contained in CPU memory. The DMA channel must specify the memory address location of the byte to be accessed by sending a 16-bit memory address to the CPU. Then the DMA channel issues a memory cycle request to the CPU. The CPU responds (if the memory is not otherwise busy) by executing a memory read cycle, during which the byte in the addressed memory location is placed on the MEMORY DATA lines to the controller.

The succeeding subparagraphs describe each of the six output data byte types from the CPU.

1.5.1.1 Device Order Byte. This byte contains a device address in MEMORY DATA BITS 4 through 0, and contains a device order in MEMORY DATA BITS 7 through 5. Device orders for the DMA channel section contain device address 16_{hex}. Device orders for disc drive controller section contain device address 06_{hex}. The device order codes are explained in table 1-2.

Table 1-2. Device Order Codes

Device Address*	Memory Data Bit			Definition
	7	6	5	
16_{hex}	0	0	0	Status In. This device order causes the DMA channel section to place memory address 0058_{hex} on the memory address bus to the CPU, and causes the controller to place a status byte on the MEMORY DATA lines to the CPU. The DMA channel executes a status transfer sequence that causes the CPU to perform a memory write cycle, during which the status byte is stored in the addressed memory location.
06_{hex}	0	0	0	Drive Select. Notifies the controller that a drive select information byte is coming.
06_{hex}	0	0	1	Cylinder Select. Notifies the controller that a cylinder address information byte is coming.

Table 1-2. Device Order Codes (continued)

Device Address*	Memory Data Bit			Definition
	7	6	5	
06_{hex}	0	1	0	Select Read. Sets up the controller for a read operation.
06_{hex}	0	1	1	Select Write. Sets up the controller for a normal write operation.
16_{hex}	0	1	1	Initialize Channel. Commands the DMA channel to execute an initialization sequence during which start of block and end of block addresses are fetched from CPU memory and stored in the DMA channel in preparation for a block transfer operation.
16_{hex}	1	0	0	DMA Disconnect. Unconditionally disconnects the DMA channel from the CPU, and resets the DMA channel.
06_{hex}	1	0	0	Select Initial Write. Used to write positional information on a new disc. Identical to the normal write operation, with the exception that positional checking is not performed, and the write operation is limited to a single sector.
06_{hex}	1	0	1	Reset Status. Initiates reset action in the disc drive controller and the disc drives.
06_{hex}	1	1	0	Alternate Status Function. Commands the controller to return controller status information, rather than drive status information, to the CPU.
06_{hex}	1	1	1	Not used.

* Device address 16_{hex} is the DMA channel section; device address 06_{hex} is the disc drive controller section.

1.5.1.2 Drive Select Byte. Following the occurrence of a drive select device order, a DATA OUT control code from the CPU notifies the controller that a drive select byte is on the output bus. The drive select byte contains a two-bit code in bits MEMORY DATA BIT 1 through 0 that selects one of the four disc drive units connected to the controller. The section codes are as follows:

MEMORY DATA BIT 1	0	Selected Disc Drive
0	0	0
0	1	1
1	0	2
1	1	3

1.5.1.3 Cylinder Address Byte. Following the occurrence of a cylinder select device order, a DATA OUT control code from the CPU notifies the controller that a cylinder address byte is on the output bus. The cylinder address byte contains an eight-bit binary code designating one of the 203 cylinders on each side of the disc.

1.5.1.4 Disc/Head/Sector Byte. Following the occurrence of a select read, select write, or select initial write device order, a DATA OUT control code from the CPU notifies the controller that a disc/head/sector byte is on the output bus. Bit MEMORY DATA BIT 7 contains the disc select code; a 1 in bit 7 selects the fixed disc and a 0 in bit 7 selects the removable disc.

Bit MEMORY DATA BIT 6 contains the head select code that designates the side of the disc on which the operation is to be performed; a 1 in this bit selects the lower head and a 0 in bit 6 selects the upper head.

Bits MEMORY DATA BIT 5 through 0 contain a six-bit binary code designating one of the 48 sectors on the cylinder selected by the cylinder address byte.

1.5.1.5 Write Data Byte. When the controller and disc drive are ready to execute a block data transfer to write data on the disc, the controller issues a CHANNEL REQUEST to the DMA channel for each byte to be written on the disc. The DMA channel responds by issuing low DMA SELECT and DMA REQUEST signals, and a high DMA WRITE signal to the CPU. Also, the next address is placed on the memory address lines to the CPU. The CPU responds by executing a memory read cycle, during which the byte in the addressed location is read from memory and placed on the MEMORY DATA lines. The controller accepts the byte and serially transmits it to the disc drive for writing on the disc in the selected sector of the addressed cylinder.

1.5.1.6 Block Control Byte. During initialization of the DMA channel, the DMA channel requests four 8-bit block control bytes from the CPU. To request each byte, the DMA channel issues low DMA SELECT and DMA REQUEST signals, and a high DMA WRITE signal to the CPU. Also, the address (0060_{hex}, 0061_{hex}, 0062_{hex}, or 0063_{hex}) of the block control byte is placed on the memory address bus to the CPU. Address locations 0060 and 0061 contain the start of block memory address, and locations 0062 and 0063 contain the end of block memory address. During the initialization sequence, these four bytes are fetched from CPU memory and stored in the DMA channel.

1.5.2 CPU READ DATA

Eight-bit data bytes read from the disc are presented to the CPU on the MEMORY DATA bus. For each byte to be transferred to the CPU, the controller issues a CHANNEL REQUEST to the DMA channel. The DMA channel responds by issuing low DMA REQUEST, DMA SELECT, and DMA WRITE signals to the CPU. Also, the next address is placed on the memory address bus to the CPU. The CPU responds by executing a memory write cycle, during which the byte on the MEMORY DATA bus is written into the addressed memory location.

1.5.3 STATUS BYTE FORMATS (tables 1-3 and 1-4)

A status byte is placed on the MEMORY DATA bus to the CPU in response to a Status In device order (see table 1-2). The content of the status byte depends on whether or not an Alternate Status Function device order (see table 1-3) preceded the Status In device order. When no Alternate Status Function device order was received, the status byte contains drive status information, as described in table 1-3. When an Alternate Status Function device order was received, the status byte contains controller status information, as described in table 1-4. The DMA channel responds to the Status In device order by placing code 0058_{hex} on the memory address lines. Then the DMA channel issues low DMA REQUEST, DMA SELECT, and DMA WRITE signals to the CPU. The CPU responds by performing a memory write cycle, during which the status byte on the MEMORY DATA bus is written into memory location 0058_{hex}.

Table 1-3. Drive Status Byte Format

Device Status Bit No.	Description
0	DMA Idle. This bit is a 1 when the DMA channel logic is in major activity sequence state 0.
1	Ready to Seek, Read or Write. This bit is a 1 when all of the following status conditions exist: a. The controller is not busy. b. The DRIVE READY status signal from the disc drive is active. c. The ACCESS READY status signal from the disc drive is active. d. The SEEK INCOMPLETE and WRITE UNSAFE status signals from the disc drive are both inactive.
2	Read Error. This bit is a 1 when a CRC or address error is detected at the end of a read operation. During a write operation, a 1 in this bit indicates that a read error was detected in the sector preceding the sector in which data is to be written. This bit is also a 1 when an overrun condition is detected.
3	Access Not Ready. This bit is a 1 when the ACCESS READY status signal from the disc drive is inactive, indicating that a command to move the heads to another cylinder is being executed.
4	Seek Incomplete. This bit is a 1 when the SEEK INCOMPLETE status signal from the disc drive is active, indicating that a seek operation was not completed due to a malfunction.
5	Write Unsafe. This bit is a 1 when the WRITE UNSAFE status signal from the disc drive is active, indicating that an abnormal condition exists in the disc drive or the external power supplies, and writing of records may not be possible.
6	Disc Drive Ready. This bit is a 1 when the DRIVE READY status signal from the disc drive is active, indicating that: a. The drive is properly supplied with power. b. The drive is loaded with a disc cartridge. c. The load/unload switch is in the load position. d. The green ready light is not on.
7	End of Block. This bit is a 1 when the DMA detects an end of block condition.

Table 1-4. Controller Status Byte Format

Device Status Bit No.	Description
0	DMA Idle. This bit is a 1 when the DMA channel logic is in major activity sequence state 0.
1	Ready to Seek, Read or Write. Same as bit 1 of drive status byte.
2	*Read Error. Same as bit 2 of drive status byte.
3	Access Not Ready. Same as bit 3 of drive status byte.
4	*CRC Error. This bit is a 1 when a CRC error is detected during a read operation.
5	*Cylinder Address Error. This bit is a 1 when a discrepancy exists between the cylinder address read from the disc and the cylinder address received from the CPU.
6	*Sector Address Error. This bit is a 1 when a discrepancy exists between the disc/head/sector data read from the disc and the disc/head/sector data received from the CPU.
7	End of Block. This bit is a 1 when the DMA channel logic detects an end of block condition.

* For a write operation, these bits indicate error status for the sector preceding the sector in which a write operation is to be performed.

1.5.4 DISC RECORDING FORMAT (figure 1-4)

Bits are recorded serially on the disc in a manchester coding form. A binary 0 bit is represented by a clock at the beginning of a bit cell, with no subsequent flux reversals in the remainder of the bit cell. A binary 1 bit contains a clock at the beginning of the bit cell, followed by a second flux reversal (data clock) in the center of the bit cell. One recording byte contains eight serial bit cells, written on one of the 406 tracks of the disc. Each track is divided into 48 sectors containing 1,200 bit cells (150 bytes). Of these 150 bytes, one is spare, and the other 149 are shown in figure 1-4. Each sector contains all of the elements shown, broken down as follows, starting at the beginning of the sector:

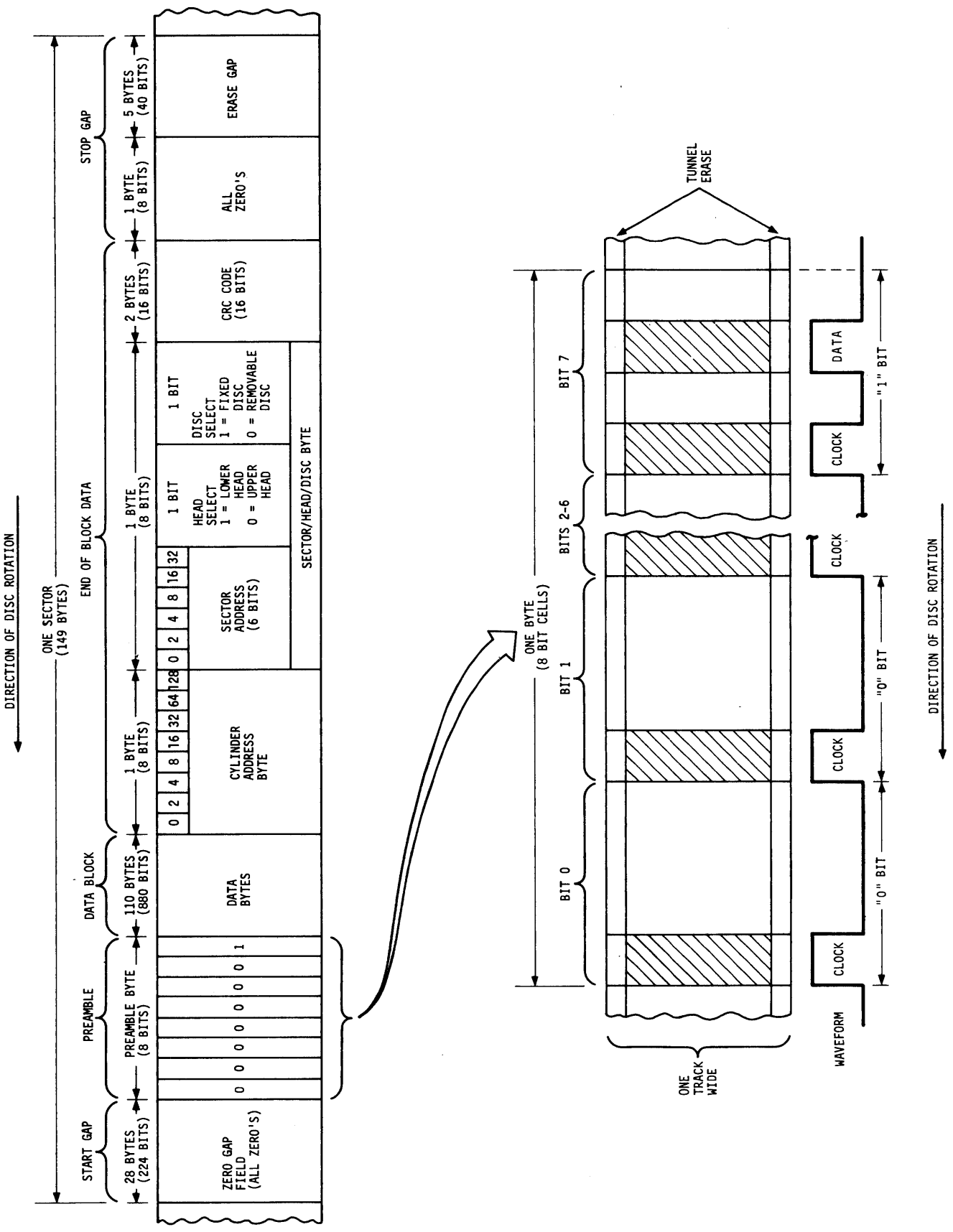


Figure 1-4. Disc Recording Format

a. Start Gap. This portion contains 28 bytes in which all 0's are written (zero gap field).

b. Preamble Byte. This byte contains a 1 in the least significant bit position, and 0's in the remaining seven bit positions.

c. Data Bytes. This section contains 110 data bytes received from the CPU.

d. End of Block Data. This section contains four bytes. The first byte contains the eight-bit cylinder address code (the number of the cylinder in which the sector is located). The second byte contains the six-bit sector address code (the number of the sector), followed by one-bit codes indicating the selected head (upper or lower) and selected disc (fixed or removable). The final two bytes contain the 16-bit cyclic redundancy check (CRC) character used to check for the presence of data errors during a read operation.

e. Stop Gap. Following the CRC character, all 0's are written for one byte. Then for the next five bytes, an erase gap is written (no flux reversals).

1.6 TYPICAL SEQUENCE OF OPERATION

This paragraph describes a typical sequence of events for performing a read or write operation on a single sector (110 data bytes). Interface signals between the CPU and the controller that are mentioned in this discussion are shown in figure 2-1. As noted in the discussion that follows, all of these events are not necessarily required for each read or write operation. The sequence of events is as follows:

a. DMA Initialization. The CPU issues the initialize channel device order to the DMA channel, which responds by fetching and storing the memory addresses for the start and end of the data block to be transferred. At the end of the initialization sequence, the DMA channel is ready for a block data transfer. When a single sector is being read or written, the end of block address is equal to the start of block address plus 109.

b. Drive Select. This operation is only required immediately after power on, or when the previous operation was on a different disc drive. After initializing the DMA channel, the CPU issues CONTROL OUT and places the drive select device order on the MEMORY DATA bus. The controller accepts and stores the device order. Next, the CPU places the drive select byte on the MEMORY DATA bus, and issues DATA OUT. The controller accepts, stores, and decodes the drive select code, and activates the DRIVE SELECT line to the designated disc drive. Status signals from the selected disc drive are returned to the controller, which supplies a drive status byte to the CPU in response to a status in device order. Bit 1 of the status byte (ready to seek, read or write) must be a 1 for the sequence to continue.

c. Cylinder Select. This operation is required only when the previous operation was on a different cylinder. The CPU issues CONTROL OUT and places the cylinder select device order on the MEMORY DATA bus. The controller accepts and stores the device order. Then the CPU places the cylinder address byte on the MEMORY DATA bus, and issues DATA OUT. The controller accepts and stores the cylinder address byte, and supplies the code and a SET CYLINDER command to the previously selected disc drive. The disc drive responds by slewing the head/arm assembly to the designated cylinder of the disc. Bit 3 (access not ready) of the status byte must be a 0 for the sequence to continued.

d. Initiate Read or Write. The CPU issues CONTROL OUT and places the select read, select write, or select initial write device order on the MEMORY DATA bus. The controller accepts and stores the device order. Then the CPU places the disc/head/sector byte on the MEMORY DATA bus, and issues DATA OUT. The controller accepts and stores the disc/head/sector byte, and sends disc and head select commands to the previously selected disc drive. If a select write device order was issued, the controller initiates a read operation in the sector preceding the sector in which the write operation is to be performed. The end of block data (positional information) in this sector is checked. The status byte indicates whether a positional (read) error was detected. If the positional information is correct, a write operation is initiated in the next sector. If the device order was select read or select initial write, no positional checking is performed and the operation commences when the heads are at the beginning of the designated sector.

e. Transfer Data. During this operation, 110 data bytes are transferred from the CPU to the controller for writing on the disc (write operation), or 110 data bytes are read from the disc and transferred (via the controller) to the CPU (read operation). A CHANNEL REQUEST to the DMA channel precedes each byte transfer. The state of the DMA WRITE line to the CPU indicates whether the transfer is to (DMA WRITE low) or from (DMA WRITE high) the CPU. The CPU returns the write data bytes (write operation), or accepts the read data bytes (read operation).

f. Process End of Block Data. Following the transfer of the 110 data bytes, the end of block data is processed. In a write operation, the end of block data (see figure 1-4) is written on the disc. In a read operation, the end of block data is read from the disc and checked for the presence of errors. If errors are detected, the appropriate error latches in the controller are set.

g. End of Block Interrupt. When the DMA channel detects that the current memory address equals the end of block address, the DMA termination line to the CPU goes low, indicating that the operation is completed.

h. Alternate Status Function. The CPU responds to the DMA termination interrupt by issuing CONTROL OUT and placing the alternate status function device order on the output bus. The controller accepts and stores the device order, and returns the controller status byte to the CPU, in response to a status in device order.

i. Disconnect. After status is checked, the CPU issues CONTROL OUT and places the reset status device order on the output bus. The controller accepts and stores the device order. Then the CPU issues DATA OUT. After a fixed delay, the controller and disc drive are both reset.

1.7 DISC FILE ACCESSING TECHNIQUES

As mentioned previously, each disc has either 200 (Model 2100) or 400 (Model 2200) tracks, each divided into 48 sectors. Each sector is capable of storing 110 eight-bit data bytes. Mechanical pickups on the rotating disc turntable produce index and sector pulses as the disc rotates. An index pulse occurs once every disc revolution to indicate the starting (0) sector. At the beginning of each sector, a sector pulse is produced.

The sector and index pulses from the disc drive are supplied to the disc drive controller, where they control the operation of sector counters. Each time the index pulse occurs, the sector counters are reset to 0. Then, as the disc rotates, the sector counters tally the sector pulses to provide an indication of the positional location (sector number) of the disc head.

The CPU specifies the disc (fixed or removable), and the side of the disc (upper or lower) for each read or write operation, by issuing appropriate select codes (disc and head select) to the controller for transmittal to the disc drive. To access a particular data block on the designated side of the selected disc, the CPU issues cylinder and sector address codes to the controller. The cylinder address code is transmitted to the disc drive, and the disc drive responds by slewing the head/arm assembly to the cylinder specified by the address. Once the cylinder is accessed, the sector address from the CPU (stored in the controller) is compared with the sector count from the sector counters until the sector count matches the stored sector address. At this time, the heads are in the correct position for reading or writing the data block, and the data transfer commences.

1.8 ERROR CHECKING (figure 1-4)

During a read operation (performed in response to a select read device order, and also performed on the sector preceding the sector to be written when a select write device order is received), the DMA/disc drive controller checks the end of block data for the presence of errors. The presence of errors is indicated in the status bytes.

Each time a write operation is performed in response to a select write or select initial write device order, end of block data (see paragraph 1.5.4) is written in each sector of the disc. Included in the end of block data is positional information (cylinder and sector addresses and disc and head select codes) and a 16-bit cyclic redundancy check (CRC) character. The positional information is derived from the cylinder address, head select, and disc select codes received from the CPU, and from the sector count contained in the sector counters. The CRC character is derived by shifting each bit written in the sector (all data preceding the CRC character) into a CRC generator in the controller. The CRC generator produces a 16-bit character whose bit pattern is a unique function of the states of all of the data bits written in the sector.

An overrun error may occur if the trailer of a sector is magnetically destroyed. When this coniditon exists it is detected by the controller and the CPU is notified that there has been a read error.

During a read operation, the positional information in the end of block data is read from the disc and compared with the cylinder, disc, head, and sector information currently contained in the controller. A compare mismatch indicates a positional error. Starting at the beginning of the sector, each data bit read from the disc is shifted into the CRC generator. At the time that the CRC character is read from the disc, the reconstructed CRC character in the CRC generator should be identical to the CRC character read from the disc. A compare mismatch indicates that a data error occurred. The data error can be the result of any of the following:

a. The record was incorrectly written on the disc.
b. The record was incorrectly read from the disc.
c. A data error occurred in the controller.

Section 2

INSTALLATION

2.1 SCOPE

This section contains instructions and data required for installing the DMA/Disc Storage Unit Controller in the CPU, and making connections to the disc storage units.

2.2 INSTALLATION IN THE CPU

The DMA/Disc Storage Unit Controller is installed in the last slot in the CPU (slot 17). Connector P1 of the circuit board inserts into the slot in the CPU mainframe. The signal interface between the circuit and the CPU are shown in the figure on page iv of LD 2002.

The DMA/Disc Storage Unit Controller has a pre-wired address of 16_{hex} for the DMA and an address of 06_{hex} for the disc storage unit controller. If another address is assigned, wiring changes must be made.

2.3 CONNECTIONS TO THE DISC STORAGE UNITS

As shown on page iv of LD 2002, up to four disc storage units are connected by a cable to connectors P2 and P3 of the circuit board. Connector P3 is used only when more than one disc storage unit is connected to the controller. With the exception of the DRIVE SELECT, SERIAL READ DATA, READ DATA CLOCK and DOUBLE FREQ WRITE DATA lines, all signals between the controller and the disc storage units are on a common bus to each disc storage unit. Each of the four DRIVE SELECT lines must be connected so that the assigned number of each disc storage unit corresponds to the function assigned in the CPU program.

Section 3

THEORY OF OPERATION

3.1 GENERAL

This section contains detailed theory of operation for the DMA/Disc Storage Unit Control (DMA disc drive controller). Logic signal names (all capital letters) mentioned in the descriptions that follow are as they appear on the logic diagrams in Logic Diagrams Manual LD 2002. Following the logic signal name, a negation symbol (-) is added if the signal is a logical 0 (false) when the active state of the signal exists (indicated by a minus sign suffixed to the mnemonic in LD 2002). If no negation symbol is indicated, the signal is a logical 1 (true) when the active state of the signal exists (indicated by a plus sign suffixed to the mnemonic in LD 2002). Unless otherwise specified, a true (1) logic level is +5v, and a false (0) level is 0v.

3.2 BLOCK DIAGRAM DESCRIPTIONS

The following paragraphs describe the functioning of the DMA/Disc Drive Controller. Each description references a block diagram which illustrates signal flow and references specific pages in LD 2002. The descriptions are divided into the two groups illustrated in figre 1-2; DMA channel and Disc Drive Controller.

3.2.1 DMA CHANNEL LOGIC (figure 3-1)

The DMA channel logic communicates with the CPU to initiate and control block data transfers between the CPU and the disc drive controller. In response to a channel initialization device order from the CPU, start of block and end of block addresses are fetched from the CPU memory and stored in address registers in the DMA channel logic. After initialization, the DMA channel logic is ready to service the disc drive controller for a read or write block transfer operation. Starting with the start of block address, data bytes are written into, or fetched from, the CPU memory.

Each time a data byte transfer is completed, a current address register in the DMA channel logic is incremented. The data transfers continue until the current address equals the end of block address that was stored in the DMA channel logic during the initialization sequence. When the end of block condition is detected, the DMA channel logic initiates a DMA termination interrupt to the CPU.

Normally, the CPU responds to a DMA termination interrupt by issuing a status input device order addressed to the DMA channel logic. The DMA channel logic responds by placing a status byte memory address code (0058_{hex}) on the memory address lines to the CPU, and commanding the disc drive controller to place a device status byte on the MEMORY DATA lines to the CPU. The CPU responds by storing the status byte in the memory address location specified by the DMA channel logic.

Included in the DMA channel logic are the MEMORY DATA line receivers, which distribute the MEMORY DATA bits (from the CPU) throughout the DMA/disc drive controller. The MEMORY DATA bus between the CPU and the DMA disc drive controller is bi-directional. That is, write data block control words, information bytes, or device orders are supplied over the MEMORY DATA bus to the DMA/disc drive controller, and read data or status bytes from the DMA/disc drive controller are supplied over the bus to the CPU. The direction of data flow depends upon the operation being performed.

3.2.1.1 Interface Logic. The interface logic includes the data receivers for the MEMORY DATA inputs from the CPU, the I/O control decoder that decodes the three-bit I/O control codes from the CPU, the receivers for the clock and master reset signals received from the CPU, and the device address decoder that detects the presence of device address code 06_{hex} (disc drive controller address) or 16_{hex} (DMA address) in device orders received from the CPU.

3.2.1.2 Control Logic. The control logic controls the initialization, data transfer, and status transfer sequences performed by the DMA channel logic. The initialization sequence is performed in response to an initialization device order addressed to the DMA. The data transfer sequence is performed following initialization in response to channel requests from the disc drive controller, and continues until either an end of block condition is detected (DMA termination interrupt), or until a DMA disconnect device order is received from the CPU. The status transfer sequence is performed in response to a status input device order from the CPU.

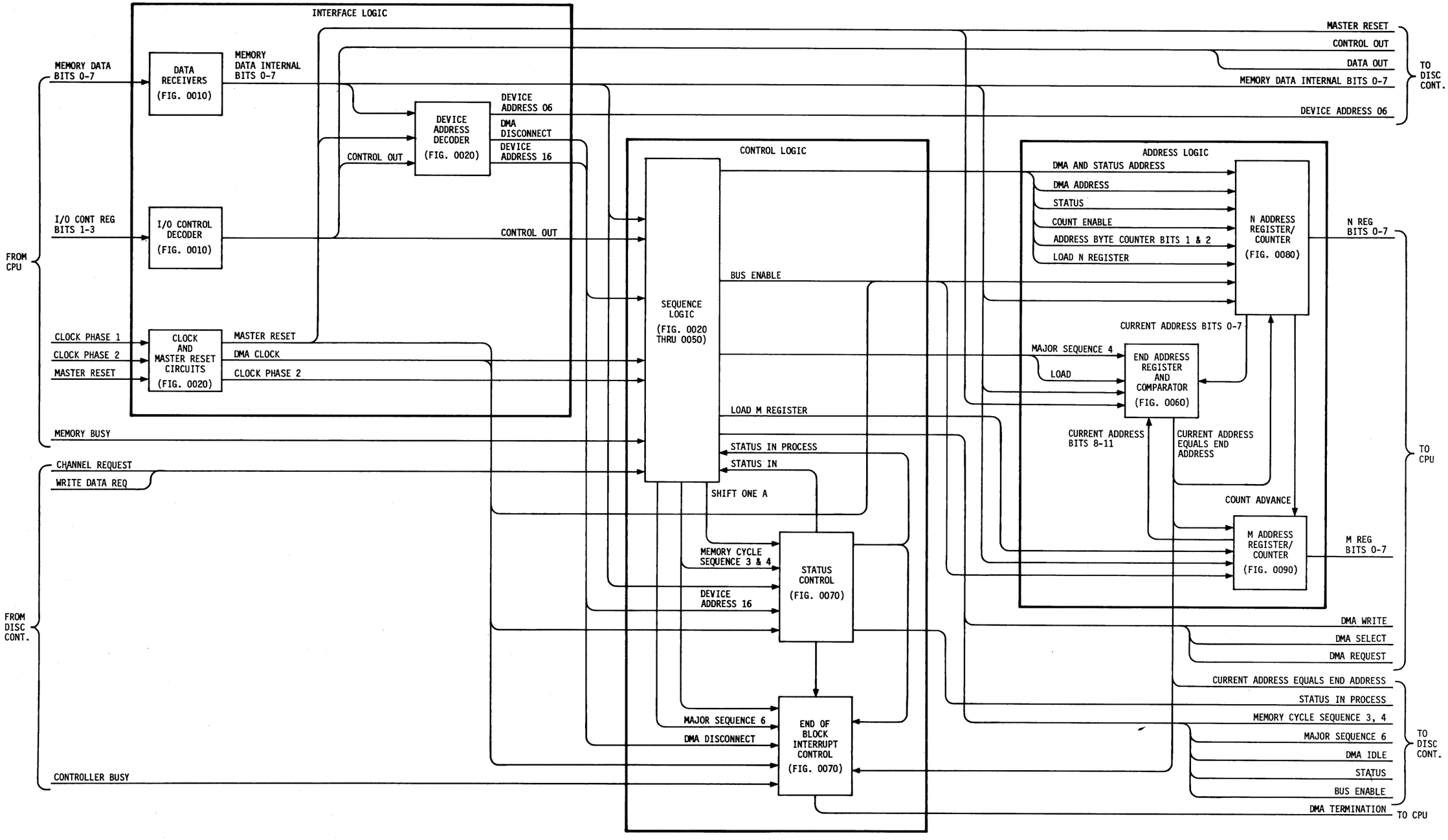


Figure 3-1. DMA Channel Logic, Block Diagram

3.2.1.3 Address Logic. The address logic includes an end address register and comparator, and a current address register/counter (M and N registers). Gating included as part of the M and N registers permits either the contents of the M and N registers or a fixed address (0058_{hex}, 0060_{hex}, 0061_{hex}, 0062_{hex}, or 0063_{hex}) to be gated onto the memory address bus to the CPU. The fixed addresses are used during initialization (addresses 0060 through 0063), or during a status transfer (address 0058).

During initialization, the end address register is loaded with the end of block addresses, and the M and N registers are loaded with the start of block address. During a data transfer sequence, the M and N registers are incremented one count each time a data transfer is completed, setting up the memory address for the next data transfer. The end address comparator compares the contents of the end address register with the contents of the M and N registers. When a match exists, an end of block condition is detected and the data transfer sequence is terminated.

3.2.2 DISC DRIVE CONTROLLER

The disc drive controller is divided into six functional sections. Each of the functional sections is described in the following paragraphs and the signal flow illustrated by block diagrams. All of the four digit numbers are page references to LD 2002. In general, the data flow in the disc drive controller is from the DMA channel to CPU/DMA interface logic and the read/write control logic and then to the read, write, and address logic. Communication between the controller and the disc drive units is also through the read, write, and address logic sections. The data registers provide temporary storage for the disc drive controller.

3.2.2.1 CPU/DMA Interface Logic (figure 3-2). This functional section includes the logic circuits that interface with the DMA channel logic and the CPU. Included is the status logic, the interface control logic, the error logic, the output data logic, the disc drive status receivers, and the request logic. The figure numbers referenced within each block and on all input and output signals refer to the appropriate logic diagrams.

The output data logic produces the read data byte output to the CPU (read operation), or the status byte that is supplied to the CPU in response to a status in device order. The output data logic formulates the appropriate eight-bit byte for transmittal to the CPU.

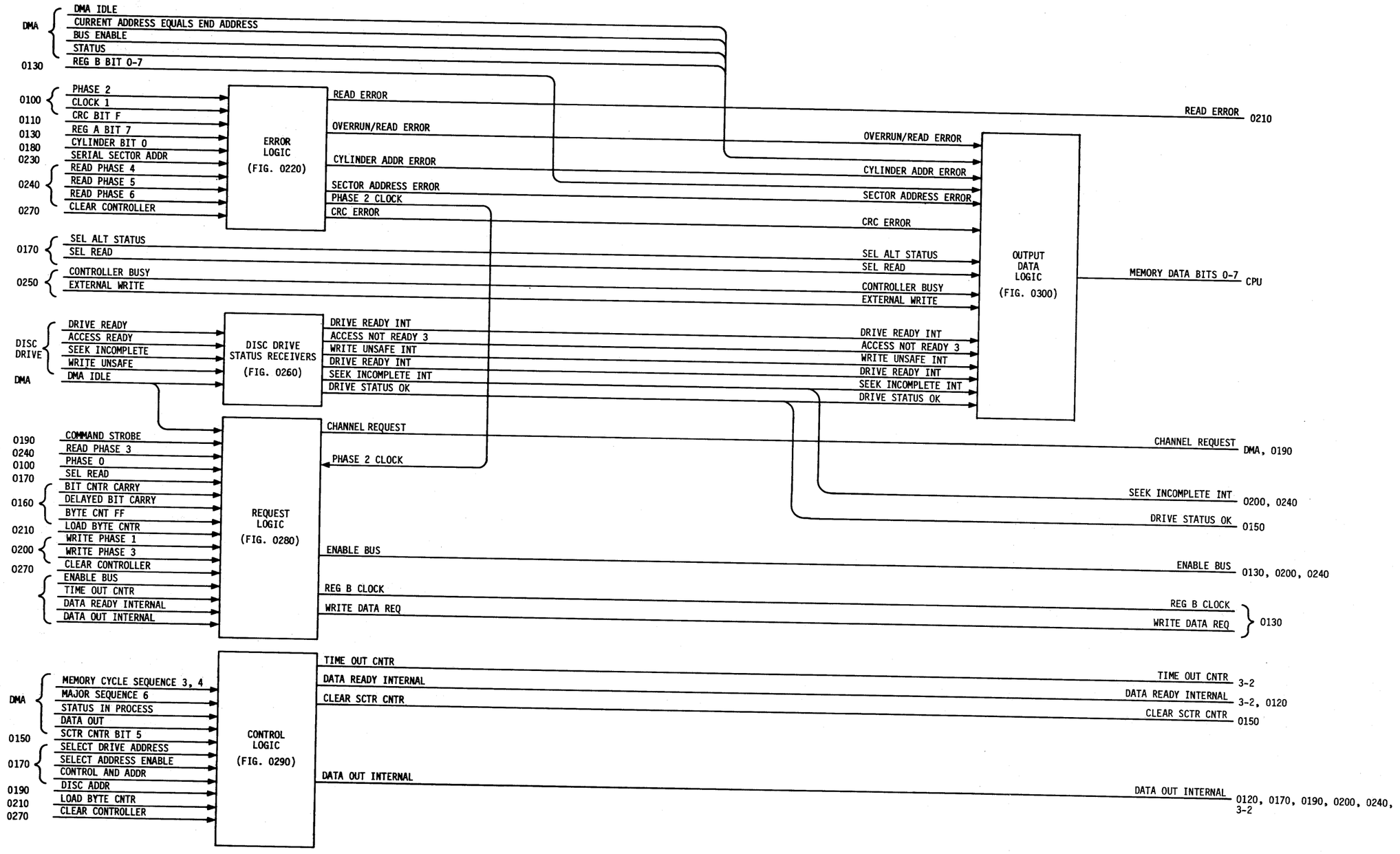


Figure 3-2. CPU/DMA Interface Logic, Block Diagram

The control and request logic processes control signals received from the DMA channel logic.

The error logic circuits develop the four error signals: read error, cylinder address error, sector address error, and CRC error.

The disc drive status receivers receive the status information from the disc drives.

3.2.2.2 Read/Write Control Logic (figure 3-3). This functional section includes logic associated with both the read and write operations of the controller. Included are the function decoder, the clock generator and phase sequencer, the CRC generator, the sector logic, and the bit and byte counters. The figure numbers referenced within each block and on all input and output signals refer to the appropriate logic diagrams.

The function decoder processes device order bytes from the CPU (via the DMA channel logic) to produce function commands used throughout the controller.

The clock generator and phase sequencer generates the basic timing signals used to control the sequence of read/write operations.

The CRC generator is used during the write operation to generate the CRC character written at the end of each sector. During a read operation, the CRC generator reconstructs the CRC character that was previously written on the disc.

The sector logic processes the index and sector pulses received from the disc drive in order to produce a count identifying the disc sector being accessed. By comparing the sector count with the sector address received from the CPU (via the DMA channel logic), the sector logic determines when a read or write operation in a designated sector is ready to be commenced.

The bit and byte counters tally the bits and bytes respectively that have been read or written within a sector, thereby determining the positional location of the disc heads within the sector.

3.2.2.3 Data Registers (figure 0130). The data registers serve as the temporary storage location for all data and sector address bytes received from, or sent to, the CPU. During a write operation, each eight-bit data byte received from the CPU (via the DMA channel logic) is stored in the data registers and converted to serial

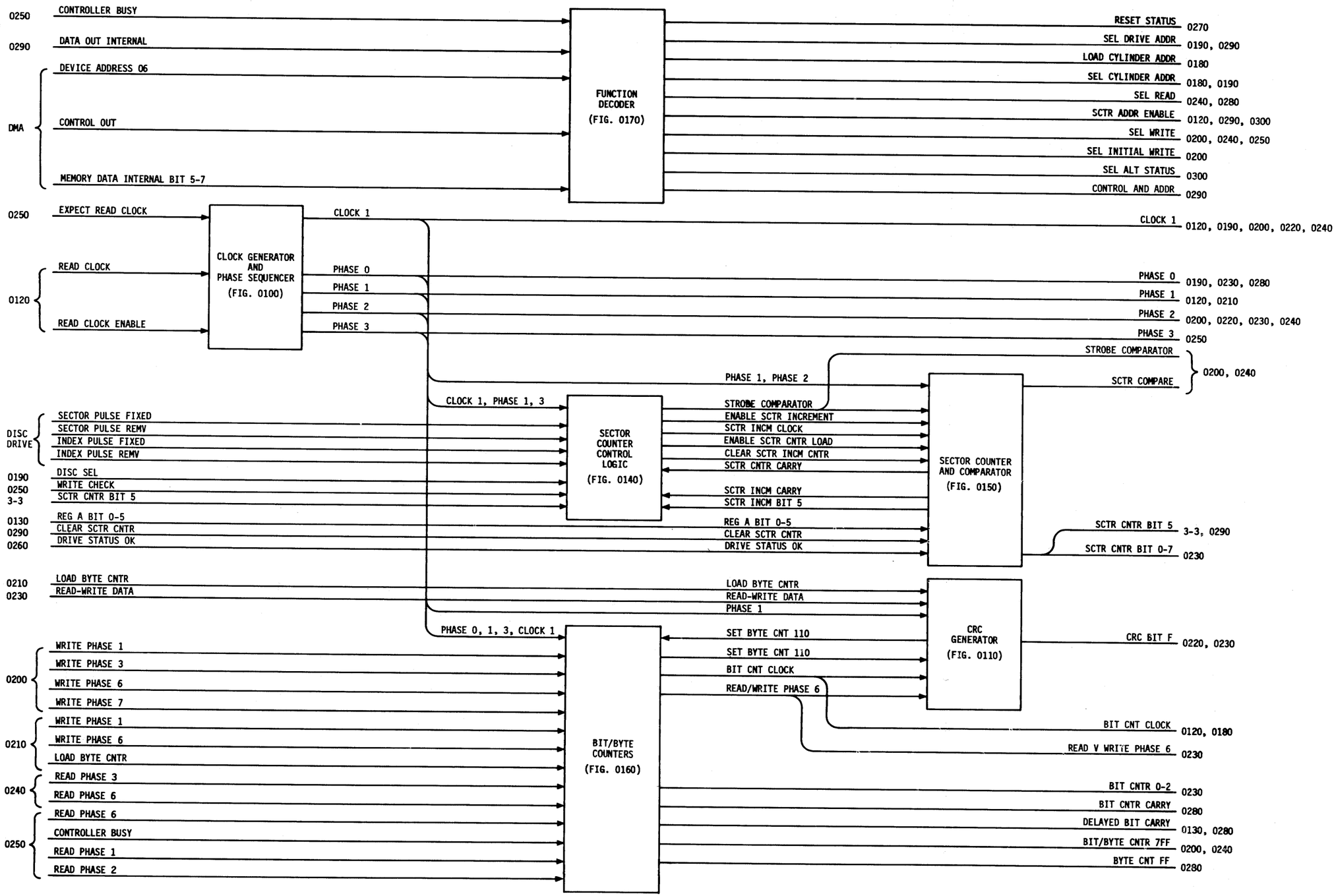


Figure 3-3. Read/Write Control Logic, Block Diagram

form for writing on the disc. During a read operation, the serial read data from the disc is shifted into the data registers, and a serial-to-parallel conversion produces the eight-bit data input bytes supplied to the CPU.

3.2.2.4 Address Logic (figure 3-4). The address logic receives and stores the cylinder address, drive select, disc select, and head select codes from the CPU (via the DMA channel logic). This data is used to form cylinder select, drive select, disc select, and head select commands for the disc drive.

3.2.2.5 Write Logic (figure 3-5). The write logic includes the write sequencer and the write data logic. The write sequencer controls the sequence of actions during a write operation. The write data logic produces the serial write data stream supplied to the disc drive for writing on the disc.

3.2.2.6 Read Logic (figure 3-6). The read logic includes the read sequencer and the read data logic. The read sequencer controls the sequence of actions during a read operation. The read data logic processes the serial read data and read clock received from the disc drive.

3.3 DATA FLOW DESCRIPTION

The following paragraphs describe the data flow for each of the controller functions. The functions are represented by four major data paths: the write data path, the function/address data path, the read data path, and the status data path. The supporting illustrations are block diagrams arranged in data flow sequence. The illustrations reference pages in LD 2002.

3.3.1 WRITE DATA PATH (figure 3-7)

The serial DOUBLE FREQ WRITE DATA to the disc drive is produced by the write data logic. During the initial portion of a write operation, the write data logic produces the 28-byte zero gap field, followed by the preamble byte. Then the CPU transfers 110 consecutive data bytes to the DMA/disc drive controller. Each byte from the CPU is supplied (via the data receivers in the DMA channel logic) to register A, and is then parallel-loaded into register B. Register B operates in the serial shift mode to shift out the bits of each byte to the write data logic

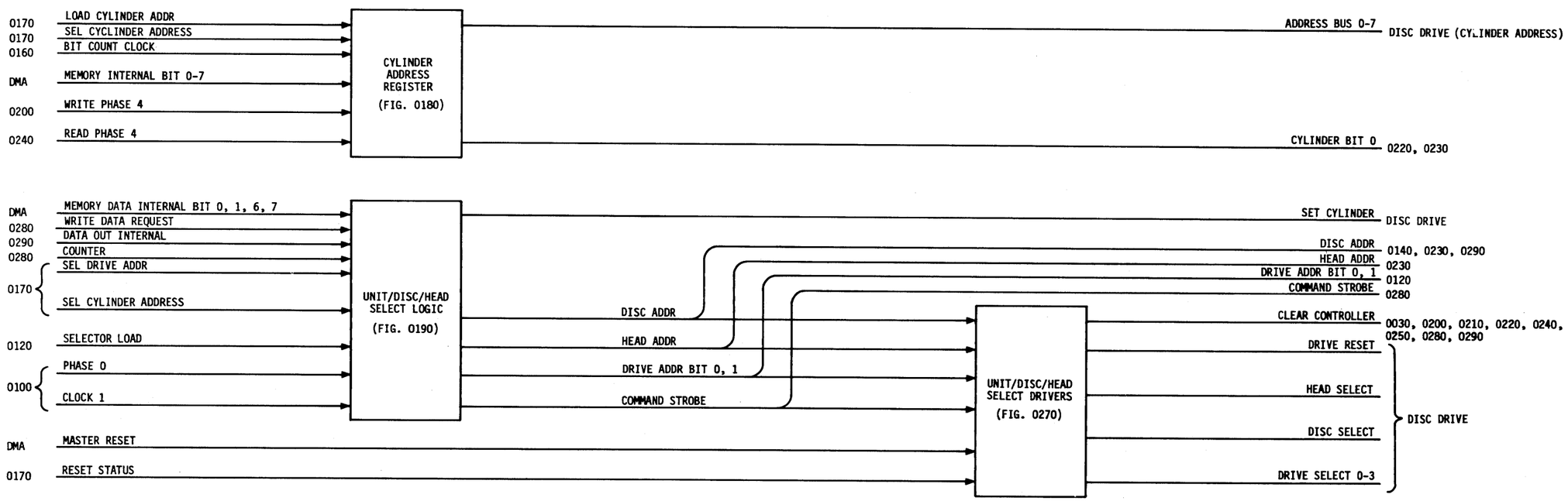


Figure 3-4. Address Logic, Block Diagram

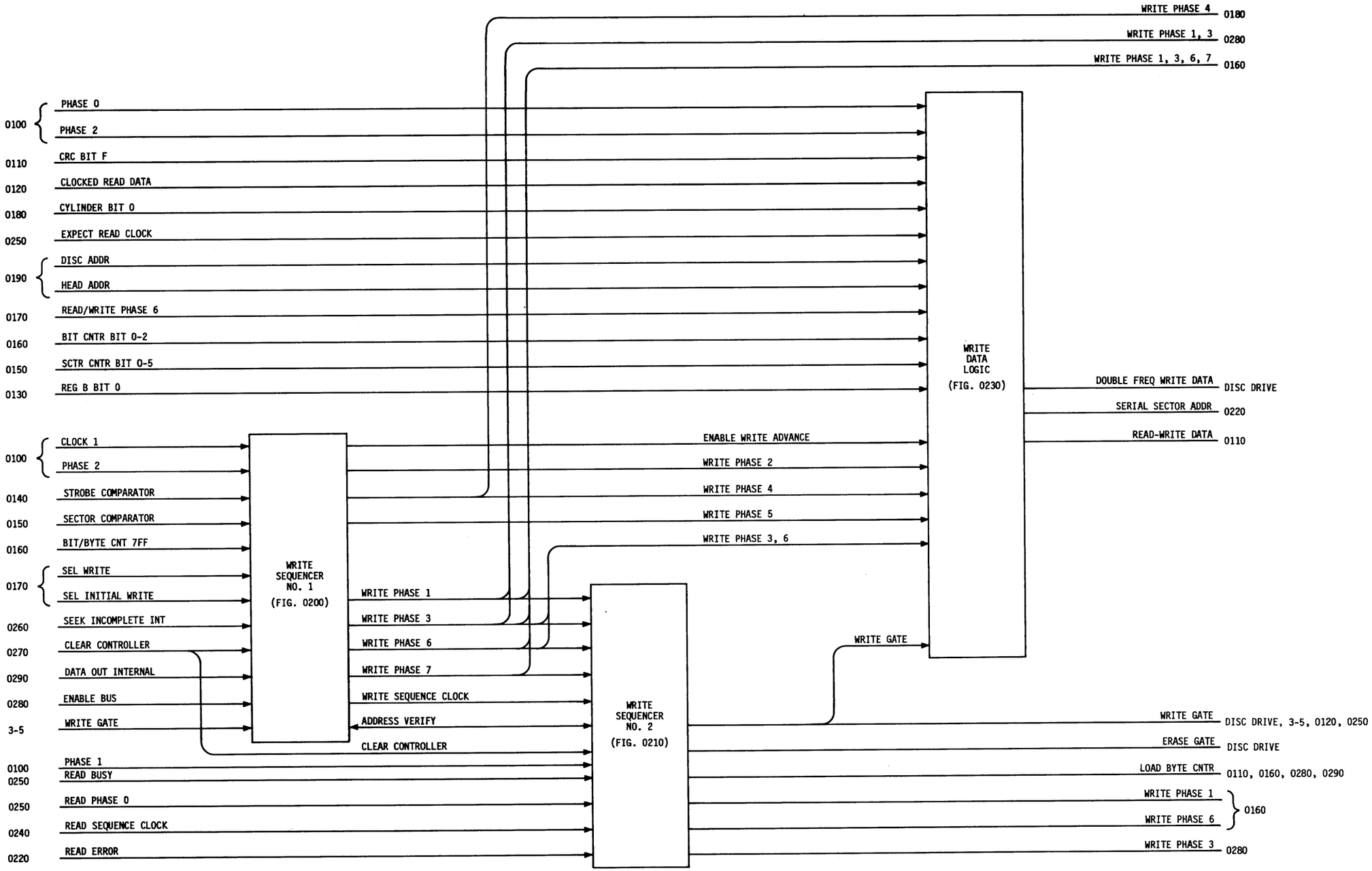


Figure 3-5. Write Logic, Block Diagram

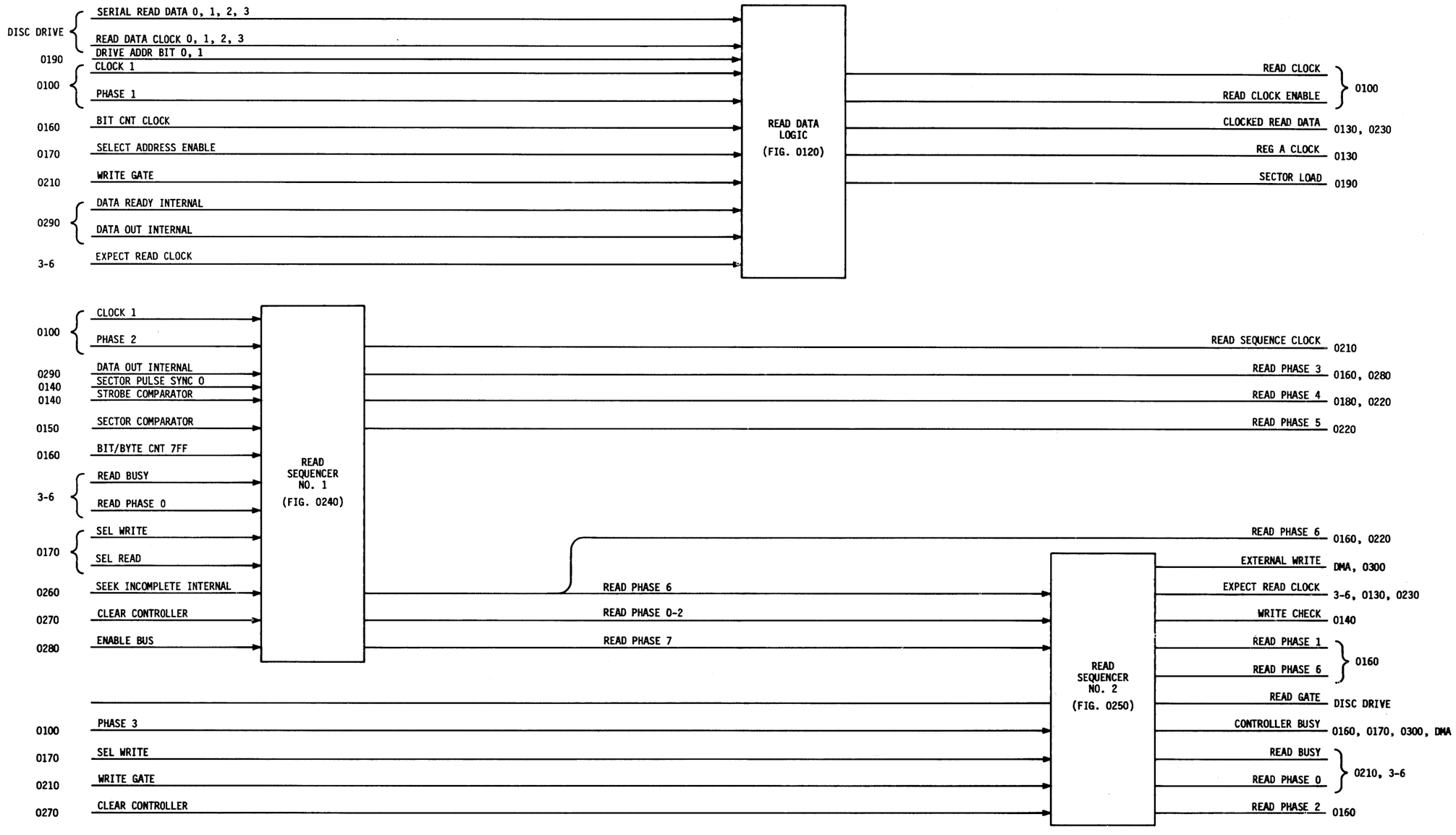


Figure 3-6. Read Logic, Block Diagram

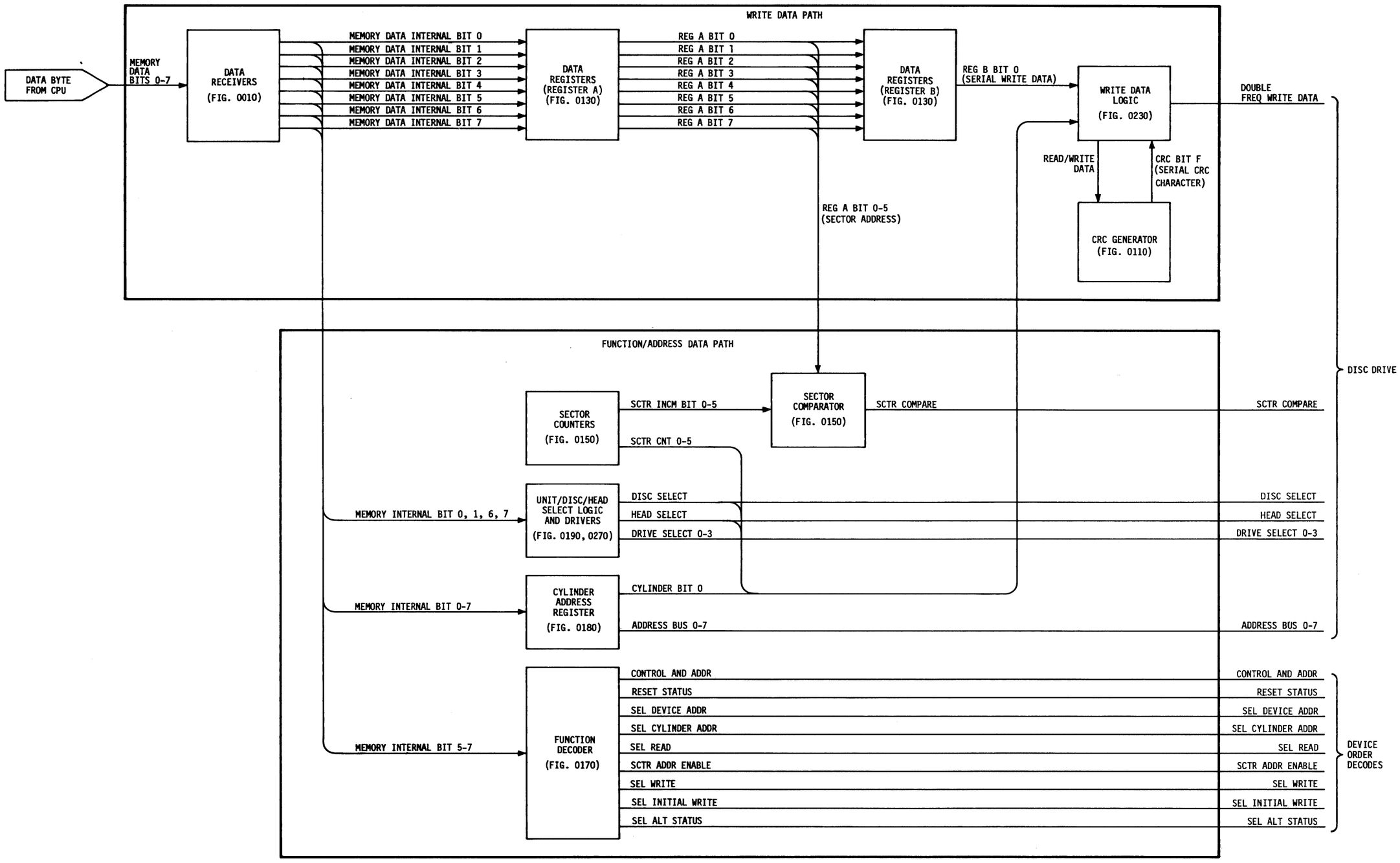


Figure 3-7. CPU-to-Disc Drive Data Flow

is also supplied as READ-WRITE DATA to the CRC generator. During each bit time, the state of the bit shifted into the CRC generator is determined by the state of the READ-WRITE DATA line, in conjunction with the CRC pattern already stored in the generator.

After the 110 data bytes have been transferred to the disc drive, the stored cylinder address (8 bits) is serially shifted (CYLINDER BIT 0) into the write data logic and out to the disc drive. Next, the sector count (SCTR CNT 0-5), head select code (HEAD ADDR), and disc select code (DISC ADDR) are supplied to the write data logic, where a multiplexer converts this data to serial form for output to the disc drive. Finally the contents (16 bits) of the CRC generator are shifted out serially (CRC BIT F) to the write data logic and supplied to the disc drive.

3.3.2 FUNCTION/ADDRESS DATA PATH (figure 3-7)

This path processes the following types of information bytes from the CPU:

a. Device Order Byte. Device order bytes are supplied via the data receivers in the DMA channel logic to the function decoder. If the address section of the device order byte contains the address (06_{hex}) of the disc drive controller, DEVICE ADDRESS 06 = 1 exists, and the function decoder decodes the device order section (bits 5 through 7) to produce a function command that sets up the controller for the specified response.

b. Disc/Head/Sector Address Byte. This byte is supplied via the data receivers to register A, and to the unit/head/disc select logic. The stored sector address portion (REG A BIT 0-5) is supplied to the sector comparator, where it is compared with the sector count (SCTR INCM BIT 0-5) from the sector counters. When the code in REG A BIT 0-5 matches the code in SCTR INCM BIT 0-5, the SCTR COMPARE signal is made true, indicating that the disc heads are positioned at the beginning of the designated sector. The disc and head select data (bits 6 and 7) is supplied (via the data receivers) to the unit/disc/head select logic. Here, the select codes are decoded to produce the HEAD SELECT and DISC SELECT commands to the disc drive.

c. Cylinder Address Byte. Cylinder address bytes are supplied via the data receivers to the cylinder address register. The stored cylinder address code is supplied to the disc drive as bits ADDRESS BUS 0-7.

d. Unit Select Byte. This byte is supplied (via the data receivers) to the unit/disc/head select logic. Here, the code in bits 0 and 1 is decoded to produce the DRIVE SELECT 0-3 commands to the disc drives.

3.3.3 READ DATA PATH (figure 3-8)

Serial read data from the disc drive is supplied to the read data latch. The CLOCKED READ DATA output of the read data latch is supplied to register A, which operates in the shift mode. When eight bits have been shifted into register A, the contents of register A are parallel-loaded into register B, which supplies the recovered read byte to the CPU via the output data logic.

The CLOCKED READ DATA is also supplied via the read-write data gate to the CRC generator. During each bit time, the state of the bit shifted into the CRC generator is determined by the state of the READ-WRITE DATA line, in conjunction with the CRC pattern already stored in the generator.

3.3.4 STATUS DATA PATH (figure 3-8)

Status data supplied to the CPU is derived from the DMA channel logic, the error logic, and disc drive status signals received via disc drive status receivers. The format of the status byte is determined by whether or not an alternate status function command is decoded by the function decoder.

The error logic is used to check the end of block data in each sector to verify that no CRC error is present, and that the disc, head, cylinder, and sector information received from the CPU matches the disc, head, cylinder, and sector information read from the disc. During error checking, the serial read data shifted into register A of the read path is supplied as REG A BIT 7 to the CRC and address checkers. When the address portion of the end of block data is being read, the address checker compares the state of REG A BIT 7 in each bit time with the serial cylinder address (CYLINDER BIT 0) from the cylinder address register, or the SERIAL SECTOR ADDR bit from the address bit multiplexer. The address bit multiplexer, controlled by the bit count from the bit counter, selects one bit from the sector counter or the unit/head/disc select logic while this portion of the end of block data is being read from the disc. When the address checker detects a mismatch between the state of REG A BIT 7 and the selected address data bit, the appropriate error signal is made true.

When the CRC portion of the end of block data is being read, the CRC checker compares the state of REG A BIT 7 in each bit time with the serially shifted output (CRC BIT F) of the CRC generator. When the CRC checker detects a mismatch between the state of REG A BIT 7 and CRC BIT F, the CRC ERROR signal is made true.

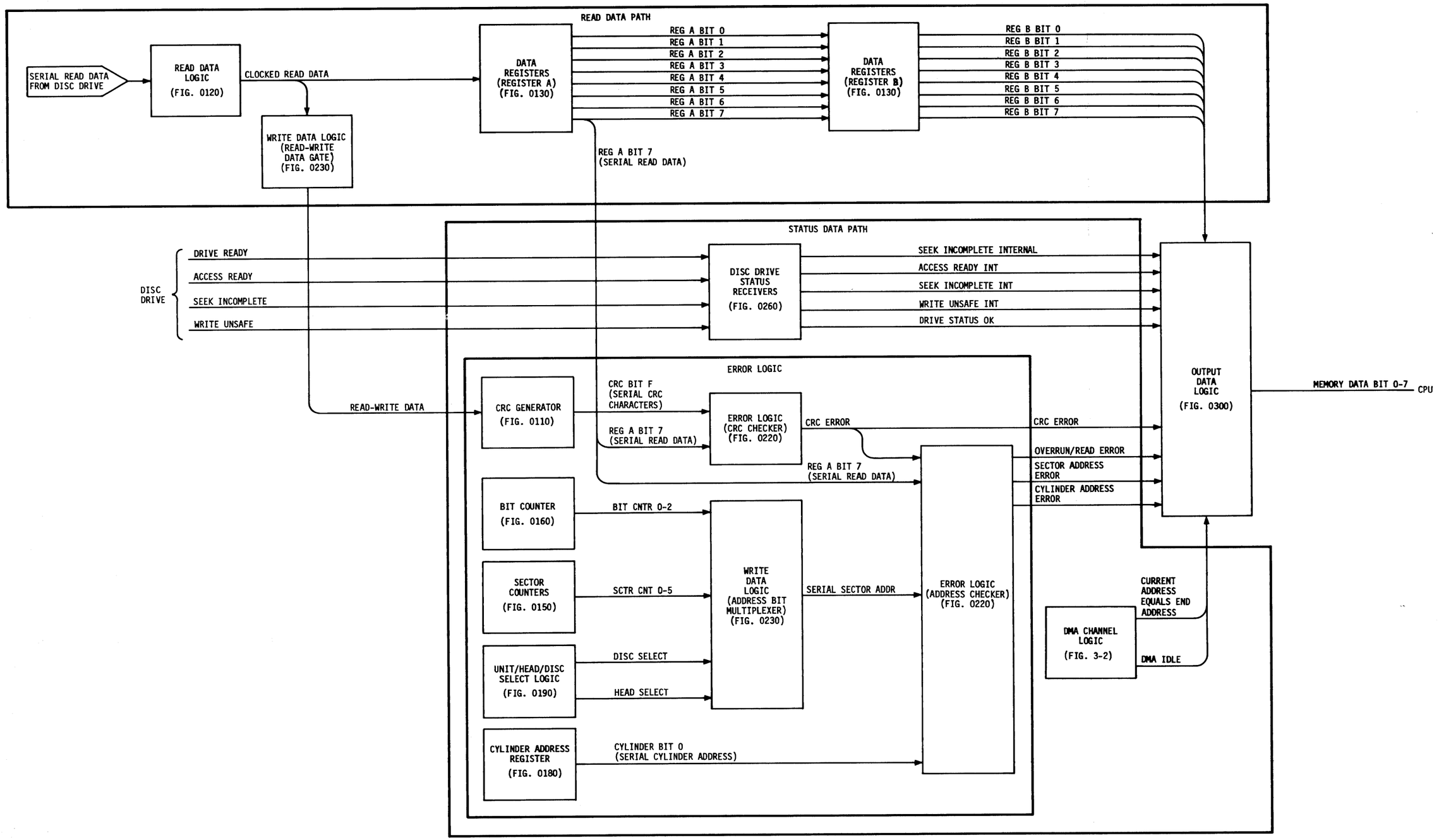


Figure 3-8. Disc Drive-to-CPU Data Flow

The output data logic processes the error and disc drive status signals to formulate the appropriate status byte for the CPU. The status byte is made available to the CPU each time STATUS is true.

3.4 DMA SEQUENCES

Figures 3-9 and 3-10 depict the three sequences performed by the DMA channel logic. In a typical block operation, these three sequences are performed in the following order:

a. Initialization Sequence
b. Data Transfer Sequence
c. Status Transfer Sequence.

These sequences are always performed to completion unless a DMA disconnect device order (96_{hex}) is received from the CPU. When the DMA disconnect device order is received, all sequences are terminated, and the DMA channel logic is reset, as follows:

a. The INHIBIT COUNT ENABLE flip-flop (figure 0020) is reset.
b. The DMA SELECT flip-flop (figure 0030) is reset.
c. The major activity sequencer (figure 0050) is reset.
d. The REQUEST flip-flop (figure 0050) is reset.
e. The DMA termination interrupt flip-flop (figure 0070) is reset.
f. The STATUS IN flip-flop (figure 0070) is reset.

The succeeding paragraphs describe the three sequences shown in figures 3-9 and 3-10.

3.4.1 INITIALIZATION SEQUENCE (figure 3-9)

Upon receipt of an initialization device order (76_{hex}) while the DMA is in major activity sequence state 0 (idle), the DMA advances to major activity sequence states 1, 2, 3, 4 and 6. Sequence states 1, 2, 3 and 4 each exist for 1.2 microseconds if the CPU memory is not otherwise busy. Memory read cycles are performed in sequence states 1, 2, 3 and 4 to fetch the start of block and end of block addresses from the CPU memory. The memory read cycles are initiated by the CPU in response to the issuance of DMA REQUEST = 1, DMA SELECT = 1, and DMA WRITE = 0 from the DMA channel logic. As soon as the memory read cycle commences, DMA REQUEST = 0 occurs. Signal DMA SELECT = 1 continues for an additional 0.8 microseconds, and returns to the 0 state during the final 0.2 microseconds of each memory read cycle.

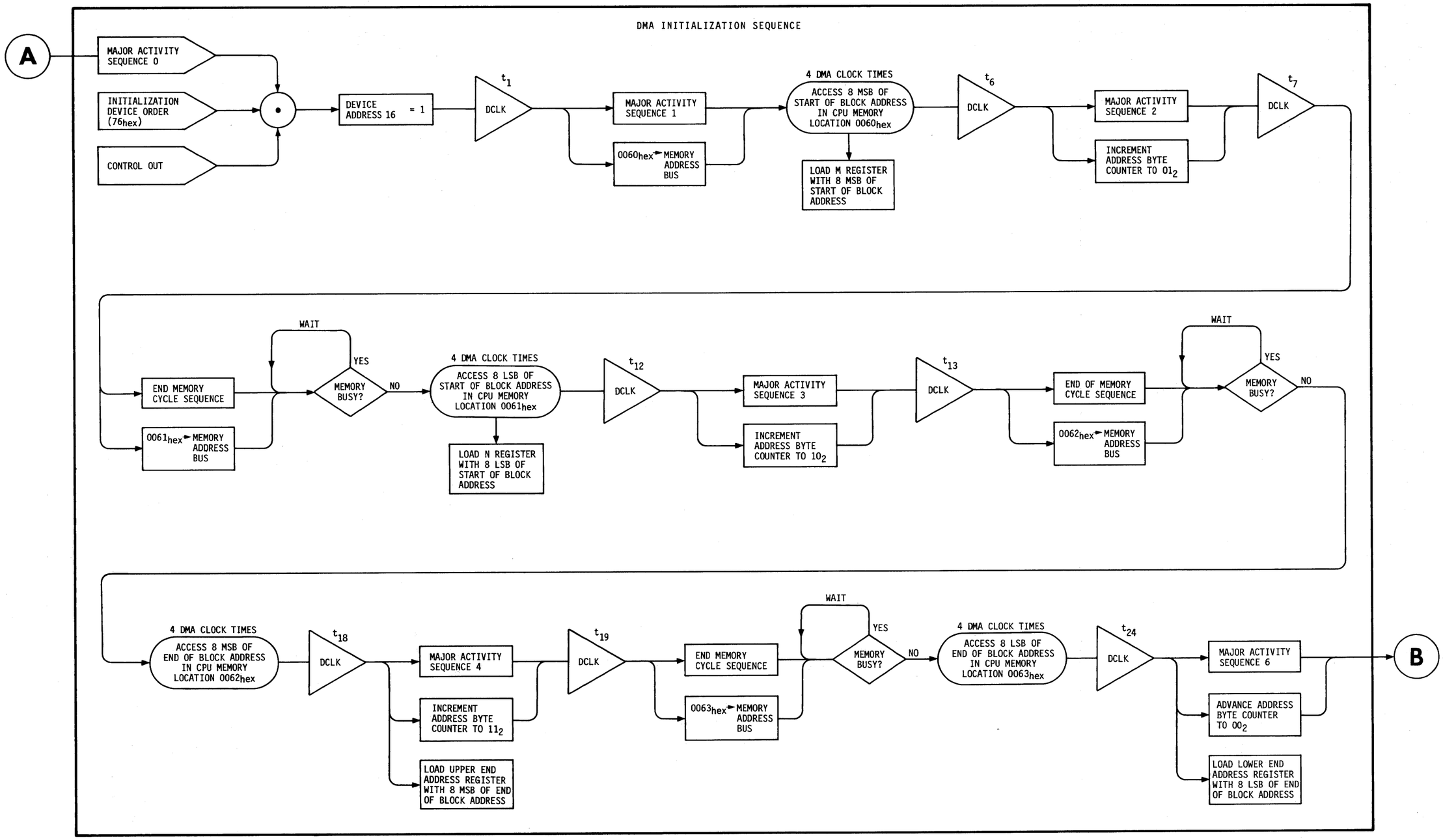


Figure 3-9. DMA Initialization Sequence Diagram

The actions performed during each major activity sequence state are as follows:

3.4.1.1 Major Activity Sequence State 1. Memory address 0060_{hex} is placed on the address bus to the CPU. During the memory read cycle, the byte contained in this location (8 MSB of start of block address) is read from memory. At DMA clock time t_6, the following actions occur:

a. The address byte read from memory is stored in the M register of the DMA channel logic.

b. The address byte counter is advanced to count 01_2, setting up memory address 0061_{hex} for major activity sequence state 2.

c. The DMA channel logic advances to major activity sequence state 2.

3.4.1.2 Major Activity Sequence State 2. Memory address 0061_{hex} is placed on the address bus to the CPU. During the memory read cycle, the byte contained in this location (8 LSB of start of block address) is read from memory. At DMA clock time t_{12}, the following actions occur:

a. The address byte read from memory is stored in the N register of the DMA channel logic.

b. The address byte counter is advanced to count 10_2, setting up memory address 0062_{hex} for major activity sequence state 3.

c. The DMA channel logic advances to major activity sequence state 3.

3.4.1.3 Major Activity Sequence State 3. Memory address 0062_{hex} is placed on the address bus to the CPU. During the memory read cycle, the byte contained in this location (8 MSB of end of block address) is read from memory. At DMA clock time t_{18}, the following actions occur:

a. The address byte read from memory is stored in the 8 MSB positions of the end address register of the DMA channel logic.

b. The address byte counter is advanced to 11_2, setting up memory address 0063_{hex} for major activity sequence state 4.

c. The DMA channel logic advances to major activity sequence state 4.

3.4.1.4 Major Activity Sequence State 4. Memory address 0063_{hex} is placed on the address bus to the CPU. During the memory read cycle, the byte contained in this location (8 LSB of end of block address) is read from memory. At DMA clock time t_{24}, the following actions occur:

a. The address byte read from memory is stored in the 8 LSB positions of the end address register of the DMA channel logic.

b. The address byte counter is advanced to 00_2.

c. The DMA channel logic advances to major activity sequence state 6, enabling the data transfer sequence.

3.4.2 DATA TRANSFER SEQUENCE (figure 3-10)

At the completion of the initialization sequence, the DMA channel logic is in major activity sequence state 6, and remains in this state until either a DMA disconnect device order is received, or until an end of block condition is detected. If the memory is not busy, the DMA channel logic initiates a memory read or write cycle each time CHANNEL REQUEST = 1 is received from the disc drive controller. When CHANNEL REQUEST = 1 occurs, either a memory read cycle or a memory write cycle is initiated by the occurrence of DMA SELECT = 1, DMA REQUEST = 1, and either DMA WRITE = 1 (memory write cycle) or DMA WRITE = 0 (memory read cycle). As soon as the memory cycle sequence commences, DMA REQUEST = 0 occurs. Signal DMA SELECT = 1 continues for an additional 0.8 microsecond, and returns to the 0 state during the final 0.2 microsecond of the memory cycle sequence. The memory location accessed during the memory read or write cycle is determined by the contents (current address) of the M and N registers in the DMA channel logic. If a memory write cycle is being performed, an 8-bit data byte is read from the disc drive and supplied from the disc drive controller to the CPU for entry into the addressed memory location. If a memory read operation is being performed, the 8-bit data or block control byte read from the addressed memory location is supplied (via the data receivers in the DMA channel logic) to the disc drive controller.

The actions occurring at clock time t_6 of the data transfer sequence depend upon whether an end of block condition exists. If the current address in the M and N registers matches the end address in the end address register, an end of block condition exists, and the following actions occur at clock time t_6:

a. The end of block interrupt is set. If the disc drive controller is not busy, a DMA termination interrupt is sent to the CPU.

b. The DMA channel logic returns to major activity sequence state 0 to await another initialization device order from the CPU.

If an end of block condition is not present at clock time t_6, the current address (in the M and N registers) is incremented one count, and the DMA channel logic

remains in major activity sequence state 6 to await the next occurrent of CHANNEL REQUEST = 1 from the disc drive controller. When CHANNEL REQUEST = 1 occurs, the data transfer sequence is repeated.

3.4.3 STATUS TRANSFER SEQUENCE (figure 3-10)

The CPU may initiate a status transfer sequence at any time, but the sequence is also normally performed immediately following the receipt of a DMA termination interrupt. The sequence is initiated upon receipt of a status in device order (16_{hex}) from the CPU. Upon receipt of this command (accompanied by CONTROL OUT), STATUS IN = 1 occurs, and, at clock time t_1, the following actions are produced:

a. The STATUS IN PROCESS flip-flop is set.

b. Code 0058_{hex} is placed on the memory address bus to the CPU.

c. The end of block interrupt is reset.

d. The status byte from the disc drive controller is placed on the MEMORY DATA lines to the CPU.

e. DMA SELECT = 1, DMA REQUEST = 1, and DMA WRITE = 1 all occur, initiating a memory write cycle during which the status byte on the MEMORY DATA lines is written into CPU memory location 0058_{hex}.

During the memory write cycle, STATUS IN is reset. At clock time t_6, the STATUS IN PROCESS flip-flop is reset. Finally, at clock time t_7, the sequence terminates. The action that occurs following the termination of the status transfer sequence depends upon the major activity sequence state that existed when the status transfer sequence was commenced.

3.5 DISC DRIVE CONTROLLER SEQUENCES

Figure 3-11 is a flow diagram depicting the sequence of actions during a write operation, and figure 3-12 depicts the sequence of actions during a read operation. These sequences are performed in response to the following device order commands from the CPU:

a. Select Initial Write. When this device order is received, the controller executes one complete write sequence to write positional information in the designated sector of a new disc.

b. Select Write. When this device order is received, the controller executes the read sequence for the sector that precedes the sector in which

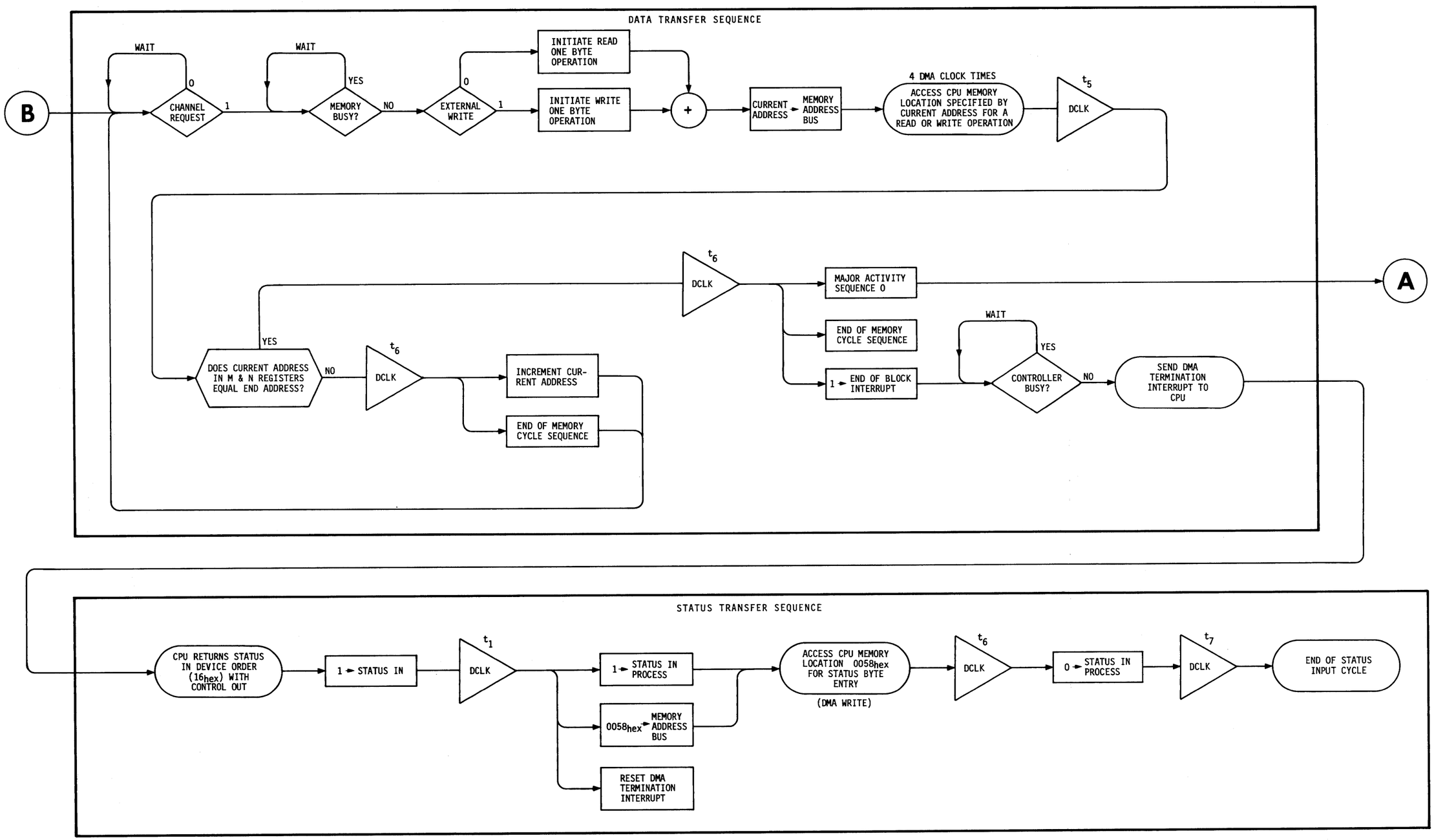


Figure 3-10. DMA Data and Status Transfer Sequences Diagram

the write operation is to be performed. The cylinder address, head select and disc select information read from the disc is compared with the data received from the CPU. Also, the sector address read from the disc is compared with the sector count stored in the controller. When a match exists, indicating that the disc head is at the start of the sector designated for the write operation, the write sequence is executed. If the write operation requires more than one sector, the write sequence is performed repetitively until the operation is completed.

c. Select Read. When this device order is received, a read sequence is initiated when the disc head is at the start of the sector designated for the read operation. If the read operation involves more than one sector, the read sequence is performed repetitively until the operation is completed.

The succeeding paragraphs describe the write and read sequences.

3.5.1 WRITE SEQUENCE (figure 3-11)

The actions occurring at the beginning of the write sequence are determined by whether the sequence was initiated by a select write or select initial write device order. When a select initial write device order is received (SEL INITIAL WRITE = 1), the write sequencer advances from WRITE PHASE 0 to WRITE PHASE 1 when the sector addressed by the CPU is being accessed by the disc drive (SCTR COMPARE = 1). When a select write device order is received (SEL WRITE = 1), the receipt of DATA OUT from the CPU initiates the read sequence (see figure 3-12) which continues until ADDRESS VERIFY goes true, indicating that the end of block data in the sector just preceding the sector to be written matches the incremented sector count, and also matches the cylinder address, head select, and disc select data received from the CPU. When ADDRESS VERIFY = 1 occurs, the next occurrence of a sector pulse (STROBE COMPARATOR = 1) causes the write sequencer to advance from WRITE PHASE 0 to WRITE PHASE 1 if both the DMA and the disc drive are ready (DMA AND DRIVE READY = 1).

In WRITE PHASE 1, the following actions occur:

a. The ERASE GATE and WRITE GATE outputs to the disc drive become active.

b. A zero gap field (28 bytes containing all 0's) is written.

After the 28-byte zero gap field is written (BIT/BYTE CNT 7FF = 1), the write sequencer advances to WRITE PHASE 2, during which the preamble byte is written. The preamble byte contains zero's in the first seven bit positions, and a one in the last bit position.

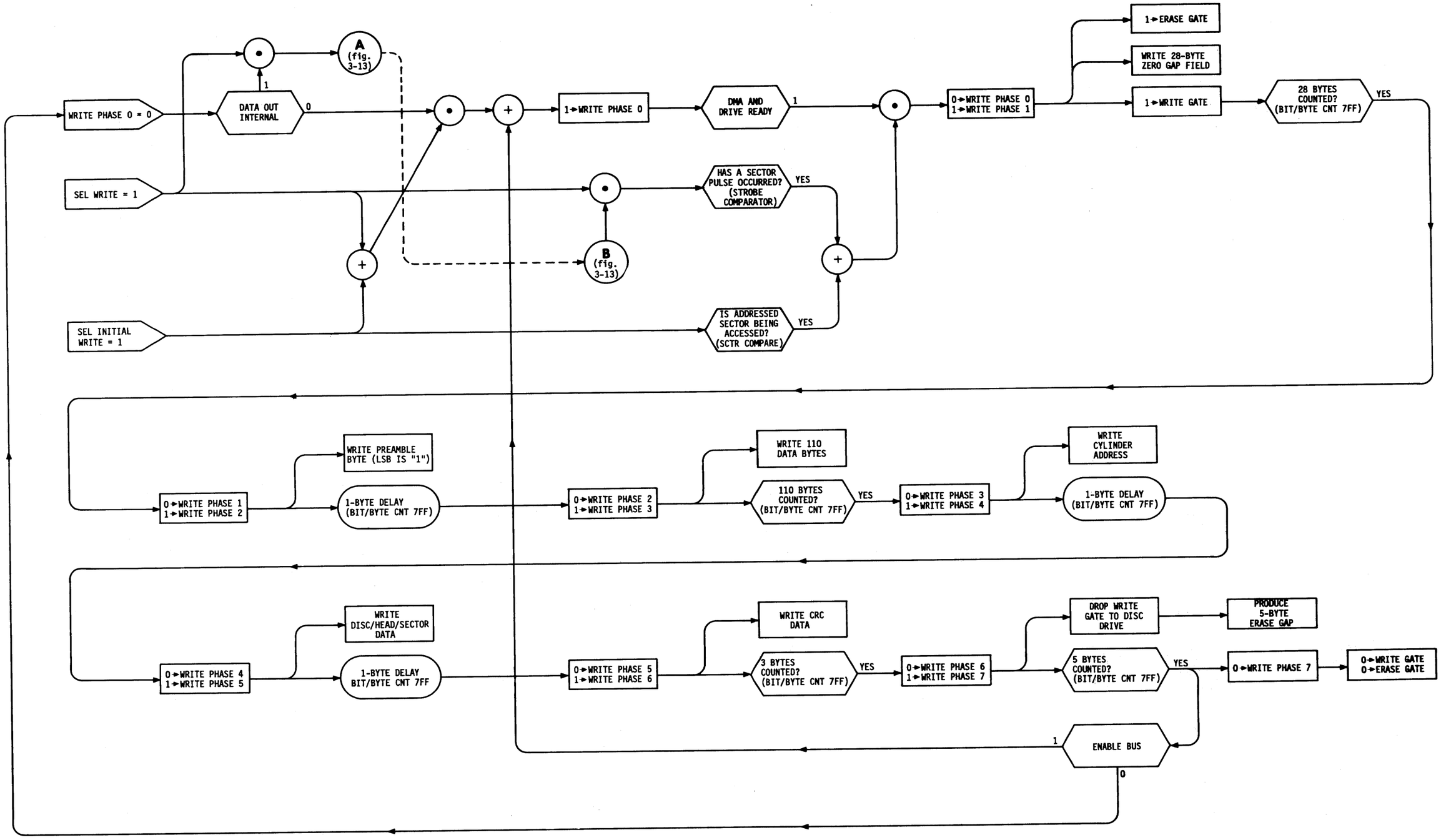


Figure 3-11. Write Sequence, Flow Diagram

At the completion of the preamble byte (BIT/BYTE CNT 7FF = 1), the write sequencer advances to WRITE PHASE 3, during which 110 data bytes are received from the CPU and written on the disc. After the 110 data bytes are written (BIT/BYTE CNT 7FF = 1), the write sequencer advances to WRITE PHASE 4, during which the cylinder address (stored in the cylinder address register) is shifted out and written. After the cylinder address byte is written, the occurrence of BIT/BYTE CNT 7FF = 1 advances the write sequencer to WRITE PHASE 5, during which the stored disc, head, and sector data is shifted out and written on the disc. The occurrence of BIT/BYTE CNT 7FF = 1 then causes the write sequencer to advance to WRITE PHASE 6.

During WRITE PHASE 6, the 16-bit CRC character (stored in the CRC generator) is shifted out and written on the disc. One byte after the completion of the CRC character BIT/BYTE CNT 7FF = 1 again occurs, causing the write sequencer to advance to WRITE PHASE 7. At the start of WRITE PHASE 7, the WRITE GATE output to the disc drive is dropped, but the ERASE GATE output is held on, causing an erase gap to be written. After the five byte erase gap is written, BIT/BYTE CNT 7FF = 1 again occurs, resetting the WRITE GATE and ERASE GATE latches, and terminating WRITE PHASE 7. If the write operation is to be continued (ENABLE BUS true), the write sequencer then returns to WRITE PHASE 0, and the write sequence is repeated.

3.5.2 READ SEQUENCE (figure 3-12)

The read sequence is initiated at the beginning of a write operation (see paragraph 3.5.1), and is also initiated when SEL READ = 1 and DATA OUT both occur. In either case, the read sequencer advances to READ PHASE 0. If the read sequence was initiated by SEL WRITE = 1, the sector incrementer contains a count that is one count higher than the sector counter to allow a sector compare one sector early. The read sequencer remains in READ PHASE 0 until both of the following events occur:

a. The DMA and disc drive are both ready (DMA AND DRIVE READY = 1).

b. The stored sector address supplied by the CPU matches the count in the sector incrementer following the occurrence of a sector pulse (SCTR COMPARE = 1).

When these two events occur, the read sequencer advances to READ PHASE 1, producing READ BUSY = 1. After the mid-point (14 bytes) in the zero gap field has been reached, BIT/BYTE CNT 7FF = 1 advances the read sequencer to READ PHASE 2.

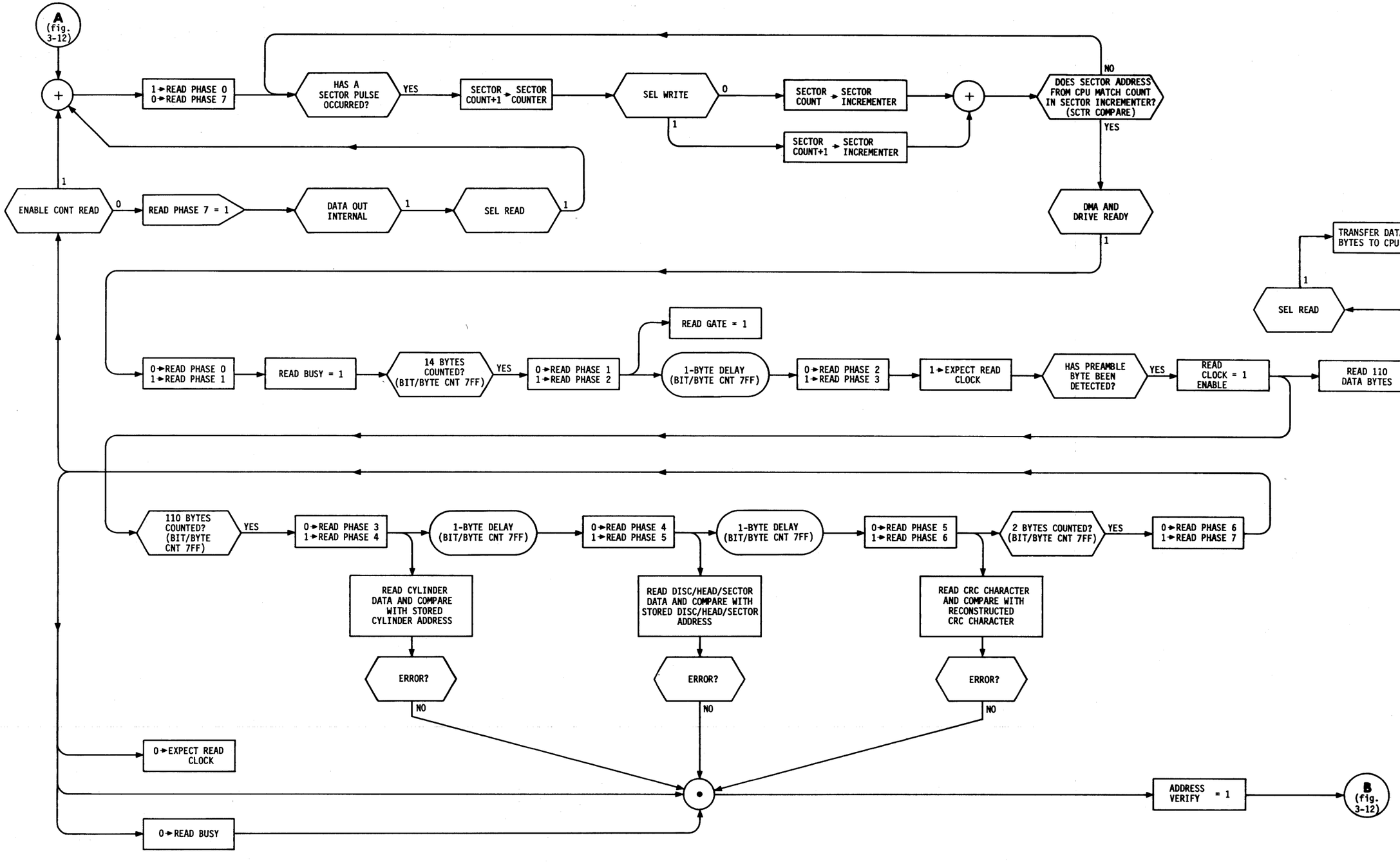


Figure 3-12. Read Sequence, Flow Diagram

In READ PHASE 2, the READ GATE to the disc drive is made true, enabling read operations. After a one-byte delay, BIT/BYTE CNT 7FF = 1 again occurs, the read sequencer advances to READ PHASE 3, and EXPECT READ CLOCK = 1 occurs, enabling the detection of the "1" bit in the preamble byte. Upon detection of the "1" bit in the preamble byte, READ CLOCK ENABLE = 1 occurs, and bit/byte counting of the data bytes read from the disc commences. After 110 data bytes have been read from the disc (and transferred to the CPU if SEL READ is true), BIT/BYTE CNT 7FF = 1 again occurs, and the read sequencer advances to READ PHASE 4.

In READ PHASE 4, the cylinder address data is read from the disc and compared with the stored cylinder address data to check for the presence of a cylinder address error. After the cylinder address has been read and checked, BIT/BYTE CNT 7FF = 1 advances the read sequencer to READ PHASE 5, during which the disc, head, and sector data is read from the disc. This data is compared with the stored disc, and head select data, and the sector count, to check for the presence of a sector address error.

After the disc, head, and sector data has been read and checked, BIT/BYTE CNT 7FF = 1 advances the read sequencer to READ PHASE 6, during which the 16-bit CRC character is read from the disc and compared with the reconstructed CRC character contained in the CRC generator. If a CRC error is detected, the CRC ERROR signal is made true.

After the CRC data is read and checked, BIT/BYTE CNT 7FF = 1 occurs again, and the read sequencer advances to READ PHASE 7. At this time, READ BUSY and EXPECT READ CLOCK are both made false, and ADDRESS VERIFY is made true if no address or CRC error exists. The read sequencer remains in READ PHASE 7 to terminate the read sequence, except when ENABLE CONT READ is true, enabling repetitive read sequences. In this case, the read sequencer immediately advances from READ PHASE 7 to READ PHASE 0 to initiate a new read sequence.

3.6 DMA CHANNEL LOGIC DETAILED LOGIC DESCRIPTION (figure 3-1)

3.6.1 DATA RECEIVERS (figure 0010)

Figure 0010 contains the receivers for the MEMORY DATA BIT 0-7 lines from the CPU. A relatively high (1) input from the CPU produces a high (1) output from the receiver. The MEMORY DATA INTERNAL BIT 0-7 outputs from the receivers are distributed throughout the DMA channel logic and the disc drive controller.

3.6.2 I/O CONTROL DECODER (figure 0010)

Inputs I/O CONT REG BIT 1-3 from the CPU are supplied to receivers that convert the relatively low (1) input from the CPU to a high (1) output. The receiver outputs are supplied to a decoder that produces the CONTROL OUT (code 001_2 in bits 3 to 1) and DATA OUT (code 010_2 in bits 3 to 1) outputs.

3.6.3 CLOCK AND MASTER RESET CIRCUITS (figure 0020)

The MASTER RESET input from the CPU is supplied to a receiver/driver that produces a low output when the input is low (1).

The DMA CLOCK goes positive when the CLOCK PHASE 1 and CLOCK PHASE 2 inputs from the CPU are both high. The negative-going trailing edge of the DMA clock occurs when the CLOCK PHASE 2 input goes low.

3.6.4 DEVICE ADDRESS DECODER (figure 0020)

When CONTROL OUT = 1 exists, the device address decoder is enabled. If the device order that accompanies CONTROL OUT contains code 06_{hex} (address disc drive controller) in MEMORY DATA INTERNAL BITS 4-0, DEVICE ADDRESS 06 = 1 is produced. If the code in MEMORY DATA INTERNAL BITS 4-0 is 16_{hex} (address DMA), DEVICE ADDRESS 16 = 1 is produced. When MASTER RESET = 1 exists, or when DEVICE ADDRESS 16 = 1 exists and MEMORY DATA INTERNAL BIT 7 = 1 (DMA disconnect device order), DMA DISCONNECT = 1 is produced.

3.6.5 SEQUENCE LOGIC (figures 0020 through 0050)

The major elements of the sequence logic are a major activity sequencer, a memory cycle sequencer, and an address byte counter. The remaining sequence logic elements are decodes of the various sequence states.

3.6.5.1 Major Activity Sequencer (figure 0050). The major activity sequencer operates during the initialization sequence (see paragraph 3.4.1). The major activity sequencer consists of a 4-bit parallel-access serial shift register and associated gating logic. All shift register bits are set to zero (state 0), producing DMA IDLE = 1, when either of the following conditions occur:

a. DMA DISCONNECT = 1 exists, clearing the shift register.

b. END OF BLOCK = 1 exists. In this case, the shift register is parallel-loaded with all 0's at the next DMA CLOCK.

Sequencing action begins during the initialization sequence when all of the following conditions exist:

a. DMA IDLE = 1 exists.
b. DEVICE ADDRESS 16 = 1 exists (DMA is being addressed for a device order).
c. MEMORY DATA INTERNAL BIT 5 = 1 exists (initialization device order).

When these conditions exist, the shift register is parallel-loaded with code 0001_2 at the next DMA CLOCK, placing the sequencer in state 1. For the remainder of the initialization sequence, the shift register operates in the shift mode. Each time INCREMENT ADDRESS BYTE COUNTER = 1 occurs, either a 1 or a 0 is shifted into the shift register at the next DMA CLOCK. When INCREMENT ADDRESS BYTE COUNTER = 1 occurs for the first time (during state 1), a 1 is shifted in, producing state 2. A 1 is also shifted in at states 2 and 3. Consequently, when state 4 occurs, the shift register contains 1111_2. At the next occurrence of INCREMENT ADDRESS BYTE COUNTER = 1 (during state 4), a 0 is shifted in, producing code 1110_2 in the shift register. This code corresponds to state 6, which initiates the data transfer sequence (see paragraph 3.4.2).

3.6.5.2 Memory Cycle Sequencer (figure 0040). The memory cycle sequencer times the memory read and write cycles initiated in the CPU. The memory cycle sequencer is a 4-bit serial shift register that always operates in the shift mode. In the idle state (no memory cycle in progress), the shift register contains all 0's (MEMORY CYCLE SEQUENCE 0 = 1 and MEMORY CYCLE SEQUENCE 04 = 1 both exist). A memory cycle sequence is initiated when SHIFT ONE = 1 occurs, producing the shift register states shown in table 3-1 at successive occurrences of the DMA CLOCK.

Signal SHIFT ONE = 1 occurs, initiating a memory cycle sequence, when either of the following conditions exist:

a. CONTROL OUT = 0, DATA OUT = 0, MEMORY CYCLE SEQUENCE 0 = 1, STATUS IN PROCESS = 0, MEMORY BUSY = 0, and no end of block condition is present, and either of the following conditions are present:

    1. The major activity sequencer is in state 1, 2, 3 or 4.

    2. The major activity sequencer is in state 6 and REQUEST = 1 exists (channel request received from disc drive controller).

b. STATUS IN PROCESS = 1 exists.

Table 3-1. Memory Cycle Sequence States

Memory Cycle State	Shift Register States				MEMORY CYCLE SEQUENCE Gates	
	Bit 1 (LSB)	Bit 2	Bit 3	Bit 4 (MSB)	MCS0	MCS04
1	1	0	0	0	0	1
2	1	1	0	0	0	0
3	0	1	1	0	0	0
4	0	0	1	1	0	0
5	0	0	0	1	1	1
6 (idle)	0	0	0	0	1	1

3.6.5.3 Address Byte Counter (figure 0050). The address byte counter is a two-bit binary counter that counts from 00_2 to 11_2 during the initialization sequence. In major activity state 0 or 6, the counter contains 00_2. In major activity states 1 through 4, the counter advances one count at each occurrence of INCREMENT ADDRESS BYTE COUNTER = 1. The counter output is supplied to the N register to establish the states of N REG BITS 0 and 1 during the initialization sequence.

3.6.5.4 Address Logic Control (figure 0020 and 0030). The COUNT ENABLE, END OF BLOCK, LOAD, LOAD M REG., and LOAD M REG. terms on figure 0020, and the COMMAND ADDRESS, COMMAND OR STATUS ADDRESS, STATUS and BUS ENABLE terms on figure 0030 control the operation of the address logic.

During major activity sequencer states 1 through 4, LOAD = 1 occurs for one DMA CLOCK interval during memory cycle sequencer state 3. When LOAD = 1 occurs during major activity sequencer state 1, LOAD M REG. = 1 occurs and LOAD N REG. = 1 both occur. When LOAD = 1 occurs during major activity sequencer state 2, LOAD N REG. = 1 occurs.

While the major activity sequencer is in state 6, and if the INHIBIT COUNT ENABLE flip-flop has not been set by SHIFT ONE A = 1 (status transfer being initiated), COUNT ENABLE = 1 occurs for one DMA CLOCK time when the memory cycle sequencer is in state 5 (see table 3-1). If, when COUNT ENABLE = 1 occurs, CURRENT ADDRESS EQUALS END ADDRESS = 1 exists, END OF BLOCK = 1 is produced.

While the major activity sequencer is in states 1, 2, 3 and 4, COMMAND ADDRESS = 1 and COMMAND OR STATUS ADDRESS = 1 both exist. When a status transfer sequence is in process, COMMAND OR STATUS ADDRESS = 1 and STATUS = 1 both exist. These terms control the code in the address bytes sent during the initialization and status transfer sequences.

During major activity sequence state 6, while DMA SELECT = 1 exists, BUS ENABLE = 1 is produced, provided that a status transfer sequence is not in progress.

3.6.5.5 Memory Cycle Control (figures 0030 and 0040). Signals DMA REQUEST, DMA SELECT, and DMA WRITE are sent to the CPU to initiate memory read or write cycles. Signals DMA SELECT = 1 and DMA REQUEST = 1 both occur, provided that the memory is not busy (MEMORY BUSY = 0), when SHIFT ONE = 1 occurs, indicating that a memory cycle sequence is being initiated. When the CPU initiates the memory cycle, MEMORY BUSY = 1 produces DMA REQUEST = 0. The DMA SELECT flip-flop and MEMORY CYCLE SEQUENCE 0 = 1 hold DMA SELECT in the low (1) state until the memory cycle sequencer advances to state 5 (see table 3-1).

Signal DMA WRITE determines whether a memory read cycle or a memory write cycle is initiated by the CPU in response to the DMA REQUEST and DMA SELECT signals. Signal DMA WRITE = 1 occurs, initiating a memory write cycle, when either of the following two conditions exist:

a. STATUS IN PROCESS = 1 occurs, producing DMA WRITE = 1 for one clock time while MEMORY CYCLE SEQUENCE 0 = 1 exists.

b. A memory cycle sequence is being initiated in major activity state 6, and EXTERNAL WRITE = 1 exists.

3.6.6 STATUS CONTROL (figure 0070)

When the CPU issues the status in device order (16_{hex}), the STATUS IN flip-flop is set on the negative-going trailing edge of DEVICE ADDRESS 16. The occurrence of STATUS IN = 1 produces SHIFT ONE A = 1 (figure 0040), which sets the STATUS IN PROCESS flip-flop at the next DMA CLOCK. The occurrence of STATUS IN PROCESS = 1 resets the STATUS IN flip-flop. At the DMA CLOCK in state 4 of the memory cycle during the status transfer sequence, the STATUS IN PROCESS flip-flop is reset.

3.6.7 END OF BLOCK INTERRUPT CONTROL (figure 0070).

If a status transfer is not in process (STATUS IN PROCESS = 0 exists) while the major activity sequencer is in state 6 (data transfer sequence in process), the occurrence of CURRENT ADDRESS EQUALS END ADDRESS = 1 sets the DMA termination interrupt flip-flop at the DMA CLOCK in state 4 of the memory cycle sequence. Then, if CONTROLLER BUSY = 0 exists, DMA TERMINATION = 1 is sent to the CPU to notify the CPU that a DMA termination interrupt has occurred. At the DMA CLOCK that follows the next occurrence of STATUS IN = 1, the DMA termination interrupt flip-flop is reset.

3.6.8 CURRENT ADDRESS LOGIC (figures 0080, 0090)

The current address logic consists of the M and N register/counters, and associated gating logic. At time t_6 of the initialization sequence (see paragraph 3.4.1), LOAD M REG = 1 occurs, causing the data on the MEMORY DATA INTERNAL bus to be parallel-loaded into the M register (figure 0090) at the next DMA CLOCK. At time t_{12} of the initialization sequence, LOAD N REG = 1 occurs, causing the data on the MEMORY DATA INTERNAL bus to be parallel-loaded into the N register (figure 0080).

After the M and N registers have been loaded during initialization, the two registers function as a 16-bit binary counter. If CURRENT ADDRESS EQUALS END ADDRESS = 0 exists, each occurrence of COUNT ENABLE = 1 causes the counter to be incremented by the DMA CLOCK.

During a data transfer sequence, when BUS ENABLE = 1 occurs, the contents of the M and N registers are gated onto the memory address bus to the CPU. During the initialization or status transfer sequences, BUS ENABLE = 0 exists, and the code on the memory address bus is determined by the states of the COMMAND OR STATUS ADDRESS, COMMAND ADDRESS, and STATUS terms, plus the states of ADDRESS BYTE COUNTER BITS 1 and 2. The M REG BITS (0-7) are always 0 during the initialization or status transfer sequences. During initialization, N REG BITS 0 and 1 assume the states of ADDRESS BYTE COUNTER BITS 0 and 1 respectively, N REG BITS 5 and 6 are in the 1 state, and N REG BITS 2, 3, 4 and 7 are in the 0 state. During the status transfer sequence, N REG BITS 0, 1, 2, 5 and 7 are in the 0 state, and N REG BITS 3, 4 and 5 are in the 1 state.

3.6.9 END ADDRESS LOGIC (figure 0060)

The end address logic consists of the 16-bit end address register, and the end address comparator. On the trailing edge of each occurrence of the LOAD pulse, either the upper or lower eight bits of the end address register are loaded with the data on the MEMORY DATA INTERNAL bus. At time t_{18} of the initialization sequence (see paragraph 3.4.1), the upper eight bits of the end address register are loaded with the eight MSB of the end of block address. At time t_{24} of the initialization sequence, the lower eight bits of the end address register are loaded with the eight LSB of the end of block address.

The end address comparator compares the contents of the end address register with the current address from the M and N registers. If a match exists between the two addresses, CURRENT ADDRESS EQUALS END ADDRESS = 1 occurs.

3.7 DISC DRIVE CONTROLLER DETAILED LOGIC DESCRIPTION

3.7.1 CPU INTERFACE LOGIC (figure 3-2)

3.7.1.1 Error Logic (figure 0220). The error logic compares the data read from the end of block section of each sector with the corresponding data stored in the controller. The comparisons occur between READ PHASE 4 and READ PHASE 6 of the read sequence. The data selected by each read phase is compared (in an exclusive OR gate) to the serial read data (REG A BIT 7) in each bit time. If REG A BIT 7 and the selected data bit are in opposite states, an error exists, and the appropriate error latch is set. The error checking sequence is as follows:

1. When READ PHASE 4 = 1 occurs, the serial read data is compared with the 8-bit serial cylinder address data (CYLINDER BIT 0) from the cylinder address register. If an error is detected, the CYLINDER ADDR ERROR latch is set.

2. When READ PHASE 5 = 1 occurs, the serial read data is compared with the 8-bit SERIAL SECTOR ADDR data from the address bit multiplexer. This data consists of the 6-bit sector address code, followed by the head select and disc select codes (one bit each). If an error is detected, the SECTOR ADDR ERROR latch is set.

3. When READ PHASE 6 = 1 occurs, the serial read data is compared with the 16-bit serial CRC BIT F output of the CRC generator. If an error is detected, the CRC ERROR latch is set.

4. When any of the error conditions checked (1, 2, and 3 above) exist, or when there is a counter overflow, the overrun/read error latch is set generating ORDER.

The states of the error latches are supplied to the status logic. The error latches remain set until CLEAR CONTROLLER (-) = 0 occurs.

3.7.1.2 Disc Drive Status Receivers (figure 0260). One receiver is provided for each of the four status signals supplied by the disc drive. The relatively low state is the active (true) state for the status signal inputs, and produces a true (+5v) output from the receivers. The receiver outputs are supplied to the status logic. The following status signal state combination produces DRIVE STATUS OK = 1: DRIVE READY active, ACCESS READY active, SEEK INCOMPLETE inactive, WRITE UNSAFE inactive.

When DRIVE STATUS OK = 1 exists, DMA AND DRIVE READY is also made true if the DMA channel logic is in major activity sequence state 0.

3.7.1.3 Output Data Logic (figure 0300). The output data logic supplies read data bytes or status bytes to the CPU. When a read operation is in progress, the occurrence of BUS ENABLE = 1 (from the DMA channel logic) and EXTERNAL WRITE = 1 gates the contents of the B register onto the MEMORY DATA bus. During a status transfer operation, STATUS = 1 (from the DMA channel logic) gates a status byte onto the MEMORY DATA bus. The MEMORY DATA BIT 0 line assumes the state of the DMA IDLE line from the DMA channel logic, and the MEMORY DATA BIT 2 line assumes the state of the READ ERROR line from the read error logic. The states of MEMORY DATA BIT lines 1 and 3 through 7 are determined by the state of SEL ALT STATUS from the function decoder. When SEL ALT STATUS = 0 exists, the format shown in table 1-3 is selected. When SEL ALT STATUS = 1 exists, the format shown in table 1-4 is selected.

3.7.1.4 Control Logic (figure 0290). The control logic generates the DATA OUT INTERNAL, DATA READY INTERNAL, CLEAR SCTR CNTR, and TIME OUT CNTR terms.

Signal DATA READY INTERNAL = 1 is produced when the DMA is executing a data transfer sequence and the memory cycle sequencer is in state 3, provided that a status transfer is not in process.

When the CPU outputs a device order byte addressed to the controller, CONTROL AND ADDR = 1 occurs, setting the CONN FOR SERVICE flip-flop. Then, when the CPU produces DATA OUT, DATA OUT INTERNAL = 1 is produced. Also, the CONN FOR SERVICE flip-flop is reset.

Each time the trailing edge of DATA OUT INTERNAL occurs, the DISC ADDR flip-flop stores the state of the DISC ADDR signal from the unit/disc/head select logic. While DATA OUT INTERNAL is still true, the state of the DISC ADDR flip-flop is compared with the newly received state of the DISC ADDR signal to determine whether consecutive operations involve different discs (fixed and removable). If different discs are involved in consecutive operations, the CLEAR SCTR CNTR signal goes false while DATA OUT INTERNAL is true, clearing the sector counter. The occurrence of SEL DEVICE ADDR = 1 from the function decoder also produces a false CLEAR SCTR CNTR pulse output that resets the sector counter.

The time-out counter detects an abnormal end of operation condition. Counting in the time-out counter is enabled when either a select write, select initial write, or select read device order is received, decoded, and stored, producing SCTR ADDR ENABLE = 1. When counting is enabled, the time-out counter is advanced one count each time a positive-to-negative transition occurs in SCTR CNTR BIT 5. The positive-to-negative transition will occur once every revolution of the disc. When operation is normal, the LOAD BYTE CNTR and CONTROL AND ADDR signals will both go true, clearing the time-out counter, before a count of eight is reached. If no clear occurs, the count of eight is reached after eight disc revolutions, producing TIME OUT CNTR = 1, which is supplied to the request logic.

3.7.1.5 Request Logic (figure 0280). The request logic generates the CHANNEL REQUEST and WRITE DATA REQ requests, the ENABLE BUS term, and the REG B CLOCK for data register B. A negative-going REG B CLOCK is produced when either of the following conditions exists:

a. When the write sequencer is in WRITE PHASE 3 (write data bytes), a REG B CLOCK is produced each time PHASE 0 = 1 occurs, to shift the data out of register B to the write data logic.

b. When the read sequencer is in READ PHASE 3 (read data bytes) and SEL READ is true, the REG B CLOCK is produced each time a bit count of 8 is reached (BIT CNTR CARRY = 1) and PHASE 2 = 1 exists, to parallel-load register B with the contents of register A.

A true WRITE DATA REQ output is supplied to the data registers to clear register A when either of the following conditions exist:

a. The write sequencer is in WRITE PHASE 1, the byte counter is being loaded (LOAD BYTE CNTR = 1), and PHASE 0 = 1 exists. This occurrence of WRITE DATA REQ clears the sector address data from register A.

b. The write sequencer is in WRITE PHASE 3 (write data bytes), a bit count of 8 is reached (DELAYED BIT CARRY = 1), the end of the data block has not been reached (BYTE CNT FF = 0), and PHASE 2 CLOCK = 1 exists.

The CHANNEL REQUEST latch is set, supplying a true CHANNEL REQUEST output to the DMA channel logic, when any of the following conditions exist:

a. The read sequencer is in READ PHASE 3 (read data bytes), SEL READ is true, a bit count of 8 is reached (BIT CNTR CARRY = 1), and PHASE 2 CLOCK = 1 exists.

b. WRITE DATA REQ is true.

c. When TIME OUT CNTR = 1 exists (see paragraph 3.7.1.4), the pseudo-write request latch is set, and a CHANNEL REQUEST is generated each time COMMAND STROBE = 1 occurs. The pseudo-write request latch remains set until ENABLE BUS goes false (channel ready or drive status reset received from CPU).

Each time the CHANNEL REQUEST latch is set, it remains set until CLEAR CONTROLLER = 1 occurs, or until DATA READY INTERNAL = 1 and ENABLE BUS = 0 are both present.

The ENABLE BUS flip-flop is set when DATA OUT INTERNAL = 1 occurs. The flip-flop is reset when DMA IDLE = 1 occurs, or when CLEAR CONTROLLER = 1 occurs.

3.7.2 READ/WRITE CONTROL LOGIC (figure 3-13)

3.7.2.1 Function Decoder (figure 0170). If the controller is not busy (CONTROLLER BUSY = 0), the occurrence of CONTROL OUT = 1 enables processing of the device order byte (MEMORY DATA INTERNAL BIT 0-7) from the CPU. When DEVICE ADDRESS 06 = 1 exists, CONTROL AND ADDR = 1 occurs. Then on the trailing edge of CONTROL OUT, CONTROL AND ADDR goes false, loading the three-bit device order code (MEMORY INTERNAL BITS 5-7) into the function storage register. The function storage register contents are decoded by the decade decoder, producing the function commands listed in table 3-2.

3.7.2.2 Clock Generator and Phase Sequencer (figure 0100). The clock generator consists of a 6.24-MHz crystal oscillator and driver circuit that produces square-wave clock CLOCK 1. This clock is used throughout the controller, and is also supplied as the shift clock to the phase sequencer, consisting of a four-bit shift register and associated control logic. The phase sequencer executes one complete four-shift cycle (PHASE 0 through PHASE 3) during each read or write bit time. During a read operation, the phase sequencer is synchronized to each READ CLOCK input from the disc drive. In READ PHASE 3 of a read operation, the phase sequencer stops until the preamble byte is detected (READ CLOCK ENABLE = 1).

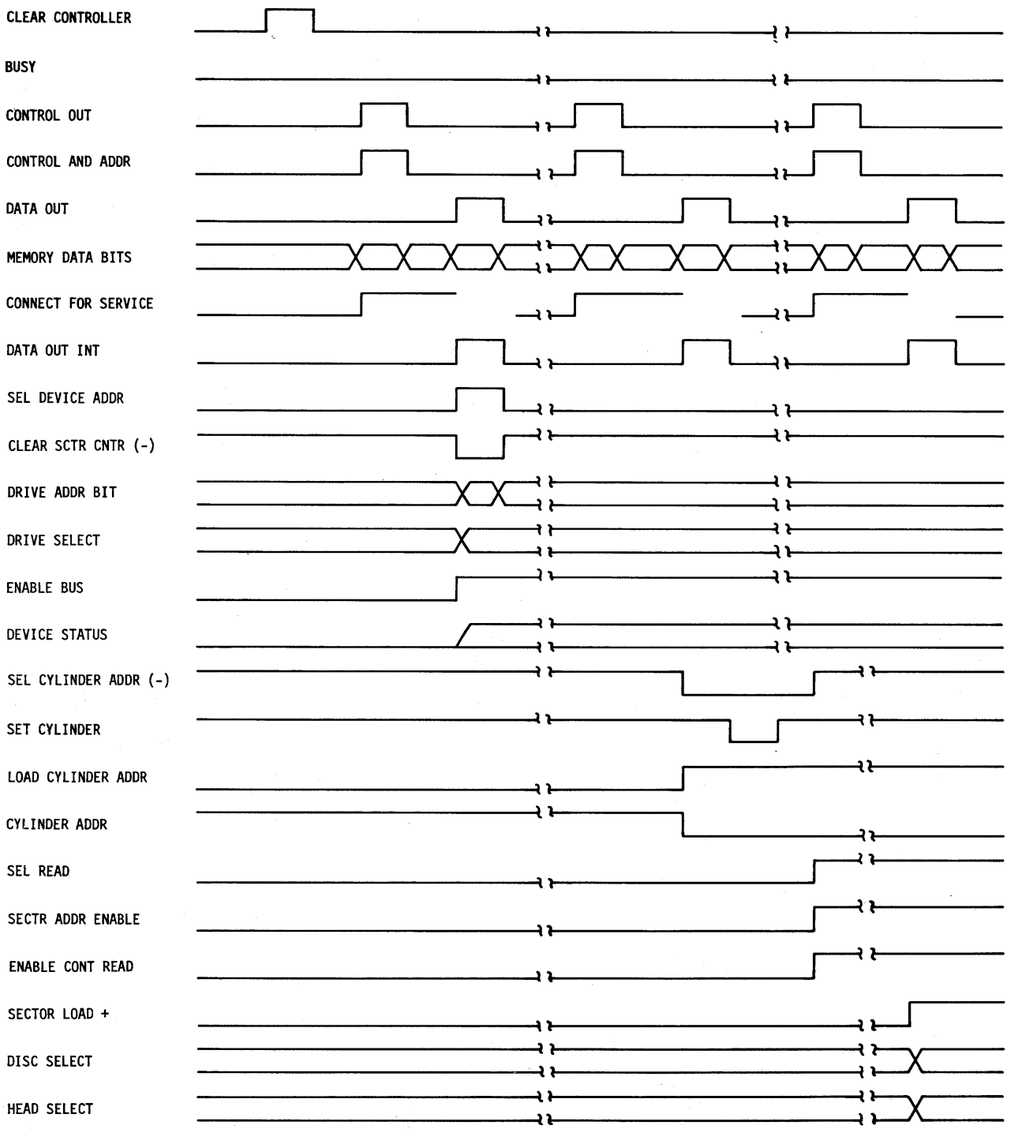
Table 3-2. Function Command Outputs

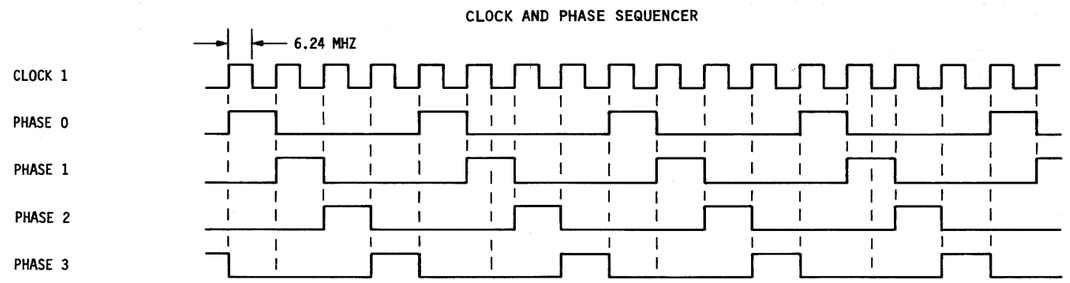
Device Order Code			Resulting Function Commands
Bit 7	Bit 6	Bit 5	
0	0	0	SEL DEVICE ADDR = 1 occurs when DATA OUT INTERNAL goes false.
0	0	1	SET CYLINDER ADDR = 1; LOAD CYLINDER ADDR = 1 occurs when DATA OUT INTERNAL goes false.
0	1	0	SEL READ = 1; SCTR ADDR ENABLE = 1
0	1	1	SEL WRITE = 1; SCTR ADDR ENABLE = 1
1	0	0	SEL INITIAL WRITE = 1; SCTR ADDR ENABLE = 1
1	0	1	RESET STATUS = 1
1	1	0	SEL ALT STATUS = 1

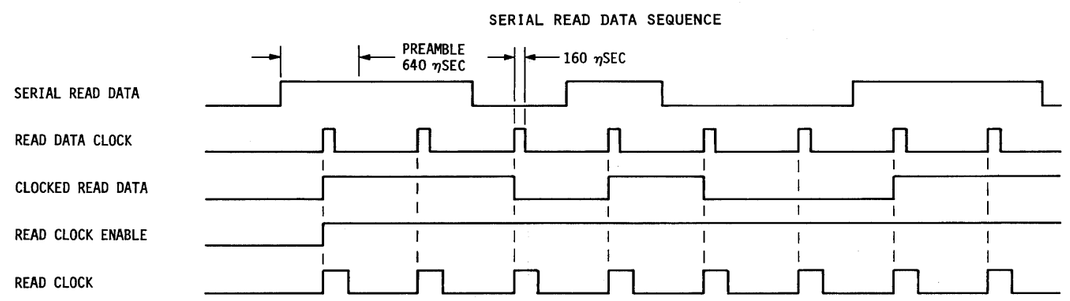
3.7.2.3 Sector Logic (figures 0140 and 0150). The sector logic consists of the sector and sector incrementer counters, their associated control logic, and the sector comparator. The sector counter is an 8-bit counter that is set up for modulo-48 counting operation.

Each time a drive select device order is received from the CPU, or when different discs are selected for consecutive read or write operations, the sector counter is cleared to all 0's. Once every disc revolution, the occurrence of the index pulse (fixed or removable) selected by the state of the DISC ADDR signal, or the occurrence of a full count in the sector counter, produces ENABLE SCTR CNTR LOAD (-) = 0. The occurrence of ENABLE SCTR CNTR LOAD causes the sector counter to be loaded with a starting count (the six least significant counter stages are loaded with 0's and the remaining stages are loaded with 1's, provided that DRIVE STATUS OK = 1 exists).

Once the sector counter is loaded with the starting count, it is advanced one count each time a sector pulse is received from the disc (fixed or removable) selected by the state of the DISC ADDR signal. The count advance occurs on the PHASE 2 clock following the occurrence of ENABLE SCTR INCREMENT = 1. Following the count advance, a SCTR INCM CLOCK occurs coincident with PHASE 1 = 1, and the sector incrementer is parallel-loaded with the count contained in the sector counter. Then







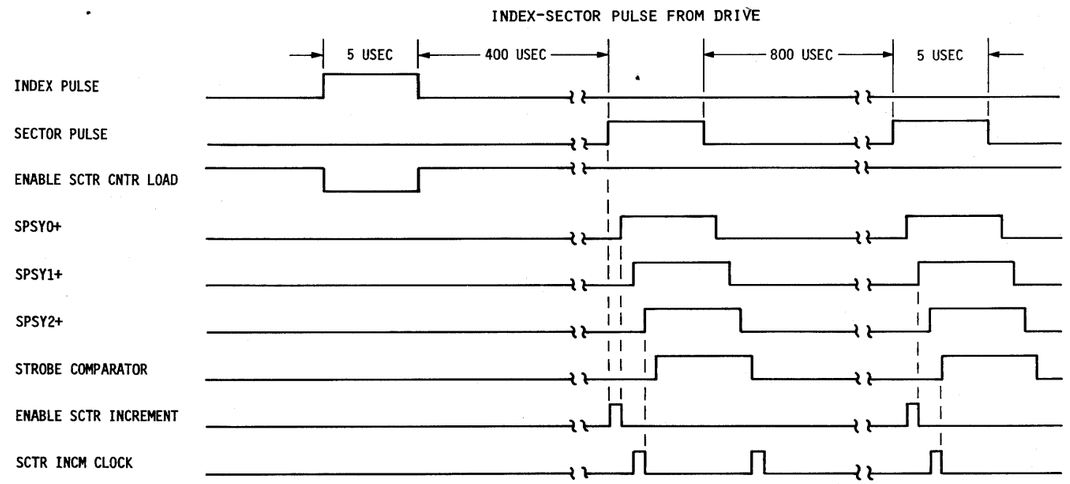


Figure 3-13. Timing Diagram

if WRITE CHECK = 1 exists, a second SCTR INCM CLOCK occurs, advancing the sector incrementer one count above the value stored at the preceding SCTR INCM CLOCK, enabling a sector compare one sector early for a write operation. Next, STROBE COMPARATOR = 1 occurs, and the count in the sector incrementer is compared in the sector comparator with the sector address (REG A BIT 0-5) (stored in register A at the beginning of a read or write operation). If a match is detected, SCTR COMPARE = 1 is produced by the sector comparator. Finally, after STROBE COMPARATOR drops, another SCTR INCM CLOCK occurs coincident with PHASE 1 = 1, and the sector incrementer is again parallel-loaded with the count in the sector counter. This counting and loading action is performed at each sector pulse until another index pulse is received, or until the full count is reached, at which time the sector counter is again loaded with the starting count.

3.7.2.4 Bit/Byte Counters (figure 0160). The bit counter is a modulo-8 counter that counts continuously during a read or write operation (CONTROLLER BUSY = 1). Each occurrence of PHASE 0 = 1 defines the start of a new bit time, and the bit counter is advanced one count. Each time a full count of 8 is reached (BIT CNTR CARRY = 1), the following actions occur:

a. When PHASE 3 = 1 occurs, the DELAYED BIT CARRY flip-flop is set.
b. The bit counter is loaded with a starting count value of 1000_2.
c. The byte counter is advanced one count.

The byte counter is a variable-modulus counter whose counting modulus is controlled by the read and write sequencers. The phase outputs of the sequencers establish the starting count value loaded into the byte counter when LOAD BYTE CNTR = 1 occurs. The byte counter advances from the starting count each time BIT CNTR CARRY = 1 occurs until a full count is reached. At this time BYTE CNT FF = 1 is produced, and when BIT CNTR CARRY = 1 also exists, BIT/BYTE CNTR 7FF = 1 occurs. The number of bytes counted between the starting and ending counts in each read or write sequencer phase is given in figures 3-11 and 3-12.

3.7.2.5 CRC Generator (figure 0110). The CRC generator is a 16-bit shift register that operates as either a straight serial shifter or as a modular shift register generator (MSRG). From phase 3 to phase 5 of a read or write sequence, the CRC generator operates as an MSRG. At the start of read or write phase 3, the register is cleared. Then, each data bit being read from, or written on, the disc is

supplied as READ-WRITE DATA to the CRC generator. At each occurrence of PHASE 1 = 1, the stages of the CRC generator are loaded as follows:

a. Stage CRC 0 is loaded with the exclusive OR of READ-WRITE DATA and the complement of the state of stage CRC F.

b. Stage CRC 1 is loaded with the state of stage CRC 0.

c. Stage CRC 2 is loaded with the exclusive OR of the state loaded into stage CRC 0 and the state of stage CRC 1.

d. Stages CRC 3 through CRC E are loaded with the state of the preceding stage.

e. Stage CRC F is loaded with the exclusive OR of the state loaded into stage CRC 0 and the state of stage CRC E.

When read or write phase 6 occurs, the CRC generator operates as a straight serial shifter that shifts out one bit (CRC BIT F) at each occurrence of the BIT CNT CLOCK.

3.7.3 DATA REGISTERS (figure 0130)

Registers A and B are the main data registers of the controller. At the beginning of a read or write operation (SCTR ADDR ENABLE = 1) when DATA OUT INTERNAL is true, a REG A CLOCK is produced, loading register A with the sector address on the MEMORY DATA INTERNAL BIT 0-7 lines. Subsequently, the operation of registers A and B is determined by whether a read or write operation is in progress, as discussed in the succeeding paragraphs.

3.7.3.1 Data Register Operation During a Read Sequence. During a read sequence, EXPECT READ CLOCK is true, and register A operates in the shift mode. Register B operates in the parallel load mode. While READ CLOCK ENABLE = 1 exists, each CLOCKED READ DATA input is shifted into register A. After the eighth serial bit has been loaded, BIT CNTR CARRY = 1 from the bit/byte counters produces a REG B CLOCK, causing register B to be parallel-loaded with the contents of register A. The outputs from register B are then provided to the data drivers for transmittal to the CPU.

3.7.3.2 Data Register Operation During a Write Sequence. When ENABLE BUS = 0 exists, each occurrence of WRITE DATA REQ = 1 clears register A. Signal EXPECT READ CLOCK is false, and register A operates in the parallel load mode. A REG A clock occurs each time DATA READY INT = 1 occurs, indicating that a data byte is on the

lines from the DMA channel logic. When the REG A CLOCK occurs, the data byte on the MEMORY INTERNAL BIT 0-7 lines is loaded into register A.

Each time DELAYED BIT CARRY = 1 occurs, indicating the end of a write byte, the next occurrent of a REG B CLOCK causes register B to be parallel-loaded with the data byte contained in register A. Then for the next 8 bit times, register B operates in the shift mode to shift out the serial write data (REG B BIT 0) to the write data logic for transmittal to the disc drive.

3.7.4 ADDRESS LOGIC (figure 3-4)

3.7.4.1 Cylinder Address Register (figure 0180). When LOAD CYLINDER ADDR = 1 occurs following receipt of a cylinder select device order, the cylinder address register is parallel-loaded with the cylinder address contained on the MEMORY DATA INTERNAL BIT 0-7 lines from the DMA channel logic. The stored cylinder address is then supplied through drivers to the disc drive as ADDRESS BUS 0-7. When read or write phase 4 occurs, the ADDRESS BUT 0-7 outputs are disabled, and the cylinder address register operates in the shift mode to produce serial cylinder address data (CYLINDER BIT 0) for the write data logic (write operation) or for the error logic (read operation). One cylinder address bit is shifted out at each occurrence of the BIT CNT CLOCK.

3.7.4.2 Unit/Disc/Head Select Logic (figure 0190). When SEL DEVICE ADDR = 1 occurs following receipt of a drive select device order, the drive select code on lines MEMORY DATA INTERNAL BIT 0-1 from the DMA channel logic is stored in the drive select storage register. At the beginning of a read or write operation (SCTR ADDR ENABLE = 1), when DATA OUT INTERNAL = 1 occurs, the head select (MEMORY INTERNAL BIT 6) and disc select (MEMORY INTERNAL BIT 7) signals in the disc/head/sector byte received from the CPU are stored in the disc and head select storage register. Also, the strobe delay counter is loaded with a count of 0001. Then, after DATA OUT INTERNAL drops, the strobe delay counter advances one count at each occurrence of PHASE 0 = 1. After 8 counts have occurred, COMMAND STROBE = 1 is produced. Also, if SET CYLINDER ADDR = 1 exists, a low (active) SET CYLINDER output is supplied to the disc drive.

3.7.4.3 Unit/Disc/Head Select Drivers (figure 0270). The outputs of the disc and head select storage registers are supplied through inverting drivers to the disc

drive. The two-bit output of the drive select storage register is decoded to produce a low (active) output on one of four drive select lines (DRIVE SELECT 0-3) to the disc drives.

This sheet also contains the controller reset logic. A low CLEAR CONTROLLER (-) output is produced, clearing the controller, and producing a low (active) DRIVE RESET output to the disc drive, when either of the following conditions exist:

a. A low MASTER RESET pulse is received.

b. A reset status device order has been received from the CPU (RESET STATUS = 1), and the COMMAND STROBE is true.

3.7.5 WRITE LOGIC (figure 3-5)

3.7.5.1 Write Sequencer (figures 0200 and 0210). The write sequencer is an 8-bit shift register with associated input and output gating logic. A shift clock is enabled each time PHASE 2 = 1 is present. The operation of the write sequencer is fully described in paragraph 3.5.1. The WRITE GATE latch is set when WRITE PHASE 1 = 1 occurs, and is reset when WRITE PHASE 7 = 1 occurs.

3.7.5.2 Write Data Logic (figure 0230). The write data logic includes the DOUBLE FREQ WRITE DATA gate, the READ-WRITE DATA gate, and the address bit multiplexer. The data selected by the DOUBLE FREQ WRITE DATA gate for transmittal to the disc drive during each phase of the write sequence is discussed fully in paragraph 3.5.1.

The gate output occurs during phase 2 of each bit time. During phase 0, the clock is produced (see paragraph 1.5.4). During a write sequence, the selected write data is gated out as the READ-WRITE DATA to the CRC generator. During a read operation, while EXPECT READ CLOCK = 1 exists, the CLOCKED READ DATA is gated out as the READ-WRITE DATA. During read or write phase 6, the READ-WRITE DATA output is inhibited.

The address bit multiplexer is controlled by the count (BIT CNTR 0-2) from the bit counter, and selects one of the eight bit inputs from the sector counter (SCTR CNTR BIT 0-5) and the disc and head select storage registers (DISC ADDR and HEAD ADDR) as the SERIAL SECTOR ADDR output. Table 3-3 lists the input bit selected for each bit count.

Table 3-3. Address Bit Multiplexer Bit Selection

Bit Count			Selected Input Bit
BIT CNTR 2	BIT CNTR 1	BIT CNTR 0	
0	0	0	SCTR CNTR BIT 0
0	0	1	SCTR CNTR BIT 1
0	1	0	SCTR CNTR BIT 2
0	1	1	SCTR CNTR BIT 3
1	0	0	SCTR CNTR BIT 4
1	0	1	SCTR CNTR BIT 5
1	1	0	HEAD ADDR
1	1	1	DISC ADDR

3.7.6 READ LOGIC (figure 3-6)

3.7.6.1 Read Sequencer (figures 0240 and 0250). The read sequencer is an eight-bit shift register with associated input and output gating logic. A shift clock is enabled each time PHASE 2 = 1 is present. The operation of the read sequencer is fully described in paragraph 3.5.2. A true CONTROLLER BUSY output is produced from READ phase 1 to READ phase 7 of a read operation, or when WRITE GATE = 1 exists during a write operation. READ BUSY = 1 is produced during a reader operation while CONTROLLER BUSY is true. The CONTROLLER BUSY output goes false at READ PHASE 7 of a read operation, when the WRITE GATE drops at the end of WRITE PHASE 7 of a write operation, or when CLEAR CONTROLLER = 1 occurs. The READ GATE latch is set when READ PHASE 2 = 1 occurs, and is reset when either READ PHASE 7 = 1 or CLEAR CONTROLLER (-) = 0 occurs. EXTERNAL WRITE = 1 is produced when the READ GATE latch is in the reset state.

If SEL READ = 1 exists when ENABLE BUS = 1 occurs, ENABLE CONT READ = 1 is produced, enabling repetitive read operations.

3.7.6.2 Read Data Logic (figure 0120). The read data logic processes the SERIAL READ DATA and READ DATA CLOCK inputs from the disc drive. The SERIAL READ DATA input is clocked into the read data latch by the READ DATA CLOCK, producing CLOCKED READ DATA. When EXPECT READ CLOCK goes true during a read sequence, the READ CLOCK ENABLE latch is armed for detecting the "1" bit in the preamble byte. The first

time CLOCKED READ DATA = 1 occurs, READ CLOCK ENABLE = 1 is produced, and continues until EXPECT READ CLOCK goes false. READ CLOCK = 1 is produced each time a READ DATA CLOCK occurs, and is used to synchronize the phase sequencer (paragraph 3.7.2.2).

After READ CLOCK ENABLE = 1 occurs during a read operation, a REG A CLOCK is produced each time BIT CNT CLOCK = 1 occurs. At the beginning of a read or write operation (SCTR ADDR ENABLE = 1), SECTOR LOAD = 1 is produced when DATA OUT INTERNAL = 1 occurs, SECTOR LOAD = 1 also produces a REG A CLOCK. During a write operation (WRITE GATE = 1), a REG A CLOCK is produced each time DATA READY INTERNAL = 1 occurs.

Section 4

MAINTENANCE

4.1 GENERAL

This section contains maintenance data for the DMA/Disc Storage Unit Controller (DMA/disc drive controller). The unit requires no periodic or preventive maintenance. Corrective maintenance consists of isolating malfunctions to the integrated circuit element level, and replacing the defective element.

4.2 TROUBLESHOOTING TECHNIQUES

The most effective method of troubleshooting is to place the DMA/disc drive controller on an extender board in the CPU chassis. Then, with the CPU and disc drive connected and operating, test programs are entered into teh CPU that cause the CPU and DMA/disc drive controller to repetitively execute specific actions, permitting the associated waveforms to be observed on an oscilloscope connected to test points on the DMA/disc drive controller. Once the abnormal waveform is identified, additional waveform checks and analyses, using the logic diagrams, are performed to isolate the fault to the integrated circuit element level.

4.3 TROUBLESHOOTING AIDS (table 4-1)

The diagrams in this manual are intended primarily for use in troubleshooting. The block diagrams (figures 3-1 through 3-8) are useful in analyzing faults to determine the logic diagram sheet on which the defective circuit element is located. The logic diagrams (figures 0010 through 0300 in LD 2002) contain all the information required to make detailed signal checks. The flow diagrams (figures 3-9 through 3-12) are useful in analyzing timing relationships, and in determining the particular point in a sequence where abnormal symptoms appear. The timing diagram (figure 3-13) shows major timing relationships.

Table 4-1 is a glossary of the major logic signals in the DMA/disc drive controller. In addition to the signal name and description, the glossary lists the signal

origin (external device and/or logic diagram figure number), and a test point of origin where the signal can be checked.

Table 4-1. Logic Glossary

Signal	Origin	Test Point	Description
ACCESS READY (XARDY+)	Disc Drive (fig. 0260)	P2-B20	Status signal from disc drive. A low (active) level indicates that no seek operation is in progress.
ACCESS READY INT (DST3+)	fig. 0260	10H-4	Signal is true when ACCESS READY is low.
ADDRESS BUS BIT 0-7	fig. 0180		The 8-bit cylinder address code supplied to the disc drive.
Bit 0 (XCYA0+)	fig. 0180	11J-8	
Bit 1 (XCYA1+)	fig. 0180	11J-11	
Bit 2 (XCYA2+)	fig. 0180	11J-3	
Bit 3 (XCYA3+)	fig. 0180	11J-6	
Bit 4 (XCYA4+)	fig. 0180	11K-8	
Bit 5 (XCYA5+)	fig. 0180	11K-11	
Bit 6 (XCYA6+)	fig. 0180	11K-3	
Bit 7 (XCYA7+)	fig. 0180	11K-6	
ADDRESS BYTE COUNT BITS 1-2	fig. 0050		The outputs from the 2-bit address byte counter.
Bit 1 (ACT1+)	fig. 0050	1X-9	
Bit 2 (ACT2+)	fig. 0050	1X-5	
ADDRESS VERIFY (RVCOM+)	fig. 0210	9F-10	A true level indicates that no read error was detected during a read operation.
BIT/BYTE CNTR 7FF (BYCFF+)	fig. 0160	6D-11	The signal is true when the bit and byte counters have reached the maximum count ($7FF_{hex}$).
BIT CNT CLOCK (BCC+)	fig. 0160	9G-6	Clock defines the beginning of each bit time during a read or write operation.
BIT CNTR CARRY (BITC7+)	fig. 0160	5J-15	Signal is true when a full count is contained in the bit counter.
BIT CNTR 0-2	fig. 0160		The bit outputs of the modulo-8 bit counter.
Bit 0 (BC0+)	fig. 0160	5J-14	
Bit 1 (BC1+)	fig. 0160	5J-13	
Bit 2 (BC2+)	fig. 0160	5J-12	

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
BUS ENABLE (ENAB-)	fig. 0030	3C-3	Signal is false during major activity sequencer state 6 when DMA SELECT = 1 exists and no status transfer is in progress.
BYTE CNT FF (BYCNT+)	fig. 0160	5G-15	Signal is true when a full count is contained in the byte counter.
CHANNEL REQUEST (REQC+)	fig. 0280	5E-8	Data transfer request to DMA channel. A low (active) level is produced each time the controller is ready to transfer a data byte to or from the CPU.
CLEAR CONTROLLER (STRS+, D708)	fig. 0270	10N-8	Produces general reset action in controller when signal is true.
CLEAR SCTR CNTR (SCRST-)	fig. 0290	10D-6	A false level clears the sector counter.
CLEAR SCTR CNTR INCM (SCIZ-)	fig. 0140	11M-3	A false level clears the sector incrementer counter.
CLOCKED READ DATA (CSRD+)	fig. 0120	11B-8	Serial read data from the disc drive that has been synchronized with the read clock.
CLOCK 1 (CLK1+)	fig. 0100	10L-12	6.24-MHz square wave used throughout the controller.
CLOCK PHASE 1 (CPH1+)	CPU (fig. 0020)	P1-A6	Phase 1 of the 5-MHz square-wave clock from the CPU.
CLOCK PHASE 2 (CPH2-)	CPU (fig. 0020)	P1-B22	Phase 2 of the 5-MHz square-wave clock from the CPU.
COMMAND ADDRESS (DCADD+)	fig. 0030	2A-6	Signal is true during major activity sequencer states 1 through 4 while DMA SELECT = 1 exists.
COMMAND OR STATUS ADDRESS (CDST+)	fig. 0030	2B-11	Signal is true when a command or status address is being sent to CPU.
COMMAND STROBE (COMST+)	fig. 0190	10M-10	Delayed strobe produced 8 bit times after the trailing edge of DATA OUT.
CONTROLLER BUSY (BUSY+)	fig. 0250	9N-13	Signal is true when a read or write operation is in progress.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
CONTROL AND ADDRESS (CADD+)	fig. 0170	7M-12	Signal is true when a device order byte addressed to the controller is on the memory data bus.
CONTROL OUT (COXX+)	fig. 0010	1B-4	A low (active) level notifies the controller that a device order byte is on the memory data bus.
COUNT ADVANCE (CADV+)	fig. 0080	3G-15	Count advance to the M register, which occurs each time the N register contains a count of FF_{hex}.
COUNT ENABLE (CTEN+)	fig. 0020	5C-6	A true signal allows a one-count advance in the current address contained in the M and N registers.
CRC BIT F (CRCF+)	fig. 0110	8H-10	Serial CRC data from the CRC generator.
CRC ERROR (CRCER+)	fig. 0220	5O-6	Signal is true when a CRC error is detected during a read operation.
CURRENT ADDRESS BITS 0-7	fig. 0080		Outputs from the 8-bit N register/ counter define the low-order bits of the current address.
Bit 0 (CA00+)	fig. 0080	3F-14	
Bit 1 (CA01+)	fig. 0080	3F-13	
Bit 2 (CA02+)	fig. 0080	3F-12	
Bit 3 (CA03+)	fig. 0080	3F-11	
Bit 4 (CA04+)	fig. 0080	3G-14	
Bit 5 (CA05+)	fig. 0080	3G-13	
Bit 6 (CA06+)	fig. 0080	3G-12	
Bit 7 (CA07+)	fig. 0080	3G-11	
CURRENT ADDRESS BITS 8-15	fig. 0090		Outputs from the 8-bit M register/ counter define the high-order bits of the current address
Bit 8 (CA08+)	fig. 0090	3H-14	
Bit 9 (CA09+)	fig. 0090	3H-13	
Bit 10 (CA10+)	fig. 0090	3H-12	
Bit 11 (CA11+)	fig. 0090	3H-11	
Bit 12 (CA12+)	fig. 0090	3J-14	
Bit 13 (CA13+)	fig. 0090	3J-13	
Bit 14 (CA14+)	fig. 0090	3J-12	
Bit 15 (CA15+)	fig. 0090	3J-11	
CURRENT ADDRESS EQUALS END ADDRESS (CEEQ+)	fig. 0060	2L-6	Signal is true when a match exists between the contents of the end addr. register and the contents of the M and N registers.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
CYLINDER ADDRESS ERROR (CYAER+)	fig. 0220	5N-11	Signal is true when a cylinder address error is detected during a read operation.
CYLINDER BIT 0 (CYA0+)	fig. 0180	11G-21	Serial cylinder address from cylinder address register.
DATA OUT (DOXX+)	fig. 0010	1B-6	A low (active) level notifies the controller that an information byte is on the memory data bus.
DATA OUT INTERNAL (DOXI+)	fig. 0290	3C-11	Signal is true when DATA OUT is low.
DATA READY INTERNAL (DRDI+)	fig. 0290	4E-8	Signal is true when memory cycle sequencer is in state 3 during a data transfer sequence.
DELAYED BIT CARRY (DCNT7+)	fig. 0160	5D-5	Delayed indication that bit counter has reached a full count.
DEVICE ADDRESS 06 (DA06+)	fig. 0020	4K-11	Signal is true when a device order addressed to the disc drive controller is present.
DEVICE ADDRESS 16 (DACOX+)	fig. 0020	4J-8	Signal is true when a device order addressed to the DMA channel is present.
DISC ADDRESS (DSEL+)	fig. 0190	11F-9	Signal is true when operation is being performed on fixed disc.
DISC SELECT (XDSEL+)	fig. 0270	11O-11	Disc select command to disc drive. A low level selects the fixed disc; a high level selects the removable disc.
DMA AND DRIVE READY (DDRDY+)	fig. 0260	9F-4	A true level indicates that both the disc drive and the DMA channel are ready to perform a read or write operation.
DMA CLOCK (DCLK+)	fig. 0020	2M-3	The internal 5-MHz clock used by the DMA channel.
DMA DISCONNECT (MRSD-)	fig. 0020	5E-6	Signal is false when a master reset pulse or a DMA disconnect device order is received from the CPU.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
DMA IDLE (MAS00+)	fig. 0020	3A-11	Signal is true when major activity sequencer is in state 0.
DMA REQUEST (DMAR+)	fig. 0030	1G-3	A low (active) signal to CPU initiates a DMA memory cycle. Signal returns to high state when memory is busy.
DMA SELECT (DMAS+)	fig. 0030	1G-6	A low (active) signal to CPU indicates that a DMA memory cycle is in progress.
DMA TERMINATION (SPIT+)	fig. 0070	1E-8	Signal is low (active) when the DMA sends an end of block interrupt to the CPU.
DMA WRITE (DMAW+)	fig. 0040	1D-8	A memory write cycle is initiated when signal is low; a memory read cycle is initiated when signal is high.
DOUBLE FREQUENCY WRITE DATA	fig. 0230		Serial write data supplied to the disc drive. A low level represents a binary 1.
XWDAT-	fig. 0230	11O-3	
XWDAT1-	fig. 0230	11D-8	
XWDAT2-	fig. 0230	11D-3	
XWDAT3-	fig. 0230	11E-8	
DRIVE ADDRESS BIT 0, 1	fig. 0190		The two-bit drive select code stored in the drive select register.
Bit 0 (DSAD0+)	fig. 0190	11F-16	
Bit 1 (DSAD1+)	fig. 0190	11F-15	
DRIVE READY (XDRDY+)	Disc Drive (fig. 0260)	P2-B10	Status signal from disc drive. A low (active) level indicates that disc drive is in a ready condition.
DRIVE READY INT (DRIVR+)	fig. 0260	10H-2	Signal is true when DRIVE READY is low.
DRIVE RESET (XDRS+)	fig. 0270	11M-8	Reset command to disc drive. A low (active) level produces reset action in the disc drive.
DRIVE SELECT 0 (XDRS0+)	fig. 0270	11L-6	A low (active) level selects disc drive 0.
DRIVE SELECT 1 (XDRS1+)	fig. 0270	11D-11	A low (active) level selects disc drive 1.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
DRIVE SELECT 2 (XDRS2+)	fig. 0270	11D-6	A low (active) level selects disc drive 2.
DRIVE SELECT 3 (XDRS3+)	fig. 0270	11E-11	A low (active) level selects disc drive 3.
DRIVE STATUS OK (DRDY+)	fig. 0260	9E-6	A true level indicates that all drive status signals are in their normal states.
ENABLE BUS (ENBD+)	fig. 0280	5F-5	Signal is true while a read or write operation is in progress, enabling the DEVICE STATUS and DATA INPUT lines to the CPU.
ENABLE CONT READ (ECRD+)	fig. 0240	7H-4	Signal is true when both ENABLE BUS and SEL READ are true, enabling repetitive read operations.
ENABLE SECTOR COUNTER LOAD (SCLD+)	fig. 0140	7B-8	A false level enables the sector counter to be loaded with a starting count at the start of each disc revolution.
ENABLE SECTOR INCREMENT (ESCTI+)	fig. 0140	4O-6	Enables counting action in the sector counter.
ENABLE WRITE ADVANCE (EWPH+)	fig. 0200	8C-6	Signal is true each time write sequencer is advanced.
END OF BLOCK (MSK2-)	fig. 0020	4A-11	Signal goes false when an end of block condition is detected.
ERASE GATE (XERGT-)	fig. 0210	11O-6	Signal is supplied to disc drive. A low (active) level enables erase action.
EXPECT READ CLOCK (ERDCL+)	fig. 0250	8D-13	Signal is true between READ PHASE 2 and READ PHASE 7 of a read operation.
EXTERNAL WRITE (REGT+)	fig. 0250	6N-8	Signal is supplied to DMA channel. A low level indicates that data transfer direction is from controller to CPU (read operation). A high level indicates that direction of transfer is from CPU to controller (write operation).

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
HEAD ADDRESS (HSEL+)	fig. 0190	11F-10	Signal is true when lower head is selected.
HEAD SELECT (XDSEL+)	fig. 0270	11O-11	Head select command to disc drive. A low level selects the lower head; a high level selects the upper head.
I/O CONTROL REGISTER BIT 1-3	CPU (fig. 0010)		The 3-bit I/O control code from the CPU.
Bit 1 (I01X+)	CPU (fig. 0010)	P1-B31	
Bit 2 (I02X+)	CPU (fig. 0010)	P1-A31	
Bit 3 (I03X+)	CPU (fig. 0010)	P1-B62	
INCREMENT ADDRESS BYTE COUNTER (IABC-)	fig. 0030	1A-8	Signal controls incrementing of major activity sequencer and address byte counter.
INDEX PULSE FIXED DISC (XIPF+)	Disc Drive (fig. 0140)	P2-B13	Pulse occurs at start of sector 0 on fixed disc.
INDEX PULSE REMOVABLE DISC (XIPR+)	Disc Drive (fig. 0140)	P2-B17	Pulse occurs at start of sector 0 on removable disc.
LOAD (LOAD-)	fig. 0020	10E-6	Low to high transition of this signal causes loading of the upper or lower section of the end address register.
LOAD BYTE COUNTER (LBYTC+)	fig. 0210	9G-12	Signal goes true to enable byte counter to be loaded with a starting count.
LOAD CYLINDER ADDRESS (LDCYLA+)	fig. 0170	8D-1	Signal is true when function decoder contains a cylinder select device order.
LOAD M REGISTER (LDCU-)	fig. 0020	4D-11	When this signal is false, the M register is parallel-loaded with the data on the MEMORY DATA bus.
LOAD N REGISTER (LDCL-)	fig. 0020	4D-8	When this signal is false, the N register is parallel-loaded with the data on the MEMORY DATA bus.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
M REGISTER BIT 0-7	fig. 0090		The eight high-order bits of the memory address supplied to the CPU. A low level is a binary 1.
Bit 0 (M00A-)	fig. 0090	1K-3	
Bit 1 (M01A-)	fig. 0090	1M-8	
Bit 2 (M02A-)	fig. 0090	1L-6	
Bit 3 (M03A-)	fig. 0090	1L-11	
Bit 4 (M04A-)	fig. 0090	1L-3	
Bit 5 (M05A-)	fig. 0090	1K-6	
Bit 6 (M06A-)	fig. 0090	1L-8	
Bit 7 (M07A-)	fig. 0090	1G-11	
MAJOR SEQUENCE 06 (MAS06+)	fig. 0020	3A-8	Signal is true when major activity sequencer is in state 6.
MAJOR SEQUENCE 1-4	fig. 0050		The outputs from the four shift register stages in the major activity sequencer.
1 (MAS1+)	fig. 0050	4B-15	
2 (MAS2+)	fig. 0050	4B-14	
3 (MAS3+)	fig. 0050	4B-13	
4 (MAS4+)	fig. 0050	4B-12	
MASTER RESET (MRST-)	CPU (fig. 0020)	P1-B44	A low (active) level initiates reset action in the controller and the disc drive.
MEMORY BUSY (MBSY+)	CPU (fig. 0040)	P1-A57	Signal is true when memory is busy.
MEMORY CYCLE SEQUENCE 0 (MCS0+)	fig. 0030	5B-1	Signal is true when memory cycle sequencer is in state 5 or 6.
MEMORY CYCLE SEQUENCE 04 (MCS04+)	fig. 0030	5B-4	Signal is true when memory cycle sequencer is in state 1, 5 or 6.
MEMORY CYCLE SEQUENCE 1-4	fig. 0040		The outputs from the four shift stages in the memory cycle sequencer.
1 (MCS1+)	fig. 0040	4C-15	
2 (MCS2+)	fig. 0040	4C-14	
3 (MCS3+)	fig. 0040	4C-13	
4 (MCS4+)	fig. 0040	4C-12	
MEMORY DATA BIT 0-7	CPU (fig. 0010)		The eight-bit byte on the output bus from the CPU. A low level represents a binary 1.
Bit 0 (MD00+)	fig. 0010	P1-B34	
Bit 1 (MD01+)	fig. 0010	P1-B35	
Bit 2 (MD02+)	fig. 0010	P1-B43	
Bit 3 (MD03+)	fig. 0010	P1-B28	
Bit 4 (MD04+)	fig. 0010	P1-A36	
Bit 5 (MD05+)	fig. 0010	P1-B30	
Bit 6 (MD06+)	fig. 0010	P1-B40	
Bit 7 (MD07+)	fig. 0010	P1-B27	

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
MEMORY DATA INTERNAL BIT 0-7	fig. 0010		Same as MEMORY DATA BIT 0-7, except a high level represents a binary 1.
Bit 0 (MDI0+)	fig. 0010	4H-10	
Bit 1 (MDI1+)	fig. 0010	4H-4	
Bit 2 (MDI2+)	fig. 0010	4H-8	
Bit 3 (MDI3+)	fig. 0010	4J-12	
Bit 4 (MDI4+)	fig. 0010	4H-2	
Bit 5 (MDI5+)	fig. 0010	4H-6	
Bit 6 (MDI6+)	fig. 0010	4H-12	
Bit 7 (MDI7+)	fig. 0010	4J-10	
N REGISTER BIT 0-7	fig. 0080		The eight low-order bits of the memory address supplied to the CPU. A low level is a binary 1.
Bit 0 (N00A-)	fig. 0080	1E-11	
Bit 1 (N01A-)	fig. 0080	1D-3	
Bit 2 (N02A-)	fig. 0080	1D-11	
Bit 3 (N03A-)	fig. 0080	1F-3	
Bit 4 (N04A-)	fig. 0080	1F-11	
Bit 5 (N05A-)	fig. 0080	1E-3	
Bit 6 (N06A-)	fig. 0080	1K-11	
Bit 7 (N07A-)	fig. 0080	1M-11	
PHASE 0-3	fig. 0100		The outputs of the phase sequencer, which executes one cycle each bit time during a read or write operation.
PHASE 0 (PH0+)	fig. 0100	10K-13	
PHASE 1 (PH1+)	fig. 0100	10K-12	
PHASE 2 (PH2+)	fig. 0100	10K-11	
PHASE 3 (PH3+)	fig. 0100	10K-10	
READ BUSY (RBUSY+)	fig. 0250	8N-9	Signal is true when a select read device order has been received, and a read operation is in progress.
READ CLOCK (RDCL+)	fig. 0120	11B-5	The buffered read data clock from the disc drive.
READ CLOCK ENABLE (RCLE+)	fig. 0120	11B-9	Signal goes true in READ PHASE 3 of a read operation when the preamble byte is detected.
READ DATA CLOCK	Disc Drive (fig. 0120)	P2-B15 P3-B5 P3-B10 P3-B15	The data clock from the disc drive.
READ ERROR (RDER+)	fig. 0220	6O-12	Signal is true during a read operation when an address or CRC error is detected.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
READ GATE (XRGT)	fig. 0250	11L-3	Signal is supplied to disc drive. A low (active) level enables a read operation in the disc drive.
READ PHASE 0-7	fig. 0240		The outputs of the read sequencer.
0 (RPH0+)	fig. 0240	7O-3	
1 (RPH1+)	fig. 0240	7O-4	
2 (RPH2+)	fig. 0240	7O-5	
3 (RPH3+)	fig. 0240	7O-6	
4 (RPH4+)	fig. 0240	7O-10	
5 (RPH5+)	fig. 0240	7O-11	
6 (RPH6+)	fig. 0240	7O-12	
7 (RPH7+)	fig. 0240	7O-13	
READ SEQUENCER CLOCK (RSQC+)	fig. 0240	8M-12	Clock used to advance the read sequencer.
READ V WRITE PHASE 6 (RWPH6+)	fig. 0160	9C-11	Signal is true when either READ PHASE 6 or WRITE PHASE 6 is true.
READ-WRITE DATA (RWDA+)	fig. 0230	6D-8	The selected read or write data supplied to the CRC generator.
REG A BIT 0-7	fig. 0130		The outputs from register A.
Bit 0 (RA0+)	fig. 0130	3K-21	
Bit 1 (RA1+)	fig. 0130	3K-19	
Bit 2 (RA2+)	fig. 0130	3K-17	
Bit 3 (RA3+)	fig. 0130	3K-15	
Bit 4 (RA4+)	fig. 0130	3K-10	
Bit 5 (RA5+)	fig. 0130	3K-8	
Bit 6 (RA6+)	fig. 0130	3K-6	
Bit 7 (RA7+)	fig. 0130	3K-4	
REG A CLOCK (RGACL+)	fig. 0120	7B-6	The clock for loading and shifting register A.
REG B BIT 0-7	fig. 0130		The outputs from register B.
Bit 0 (RB0+)	fig. 0130	3N-21	
Bit 1 (RB1+)	fig. 0130	3N-19	
Bit 2 (RB2+)	fig. 0130	3N-17	
Bit 3 (RB3+)	fig. 0130	3N-15	
Bit 4 (RB4+)	fig. 0130	3N-10	
Bit 5 (RB5+)	fig. 0130	3N-8	
Bit 6 (RB6+)	fig. 0130	3N-6	
Bit 7 (RB7+)	fig. 0130	3N-4	
REG B CLOCK (RGBCL+)	fig. 0280	7H-10	The clock for loading and shifting register B.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
REQUEST (REQS+)	fig. 0050	3E-5	Signal is true when the disc drive controller is requesting a data transfer.
RESET STATUS (RSTAT+)	fig. 0170	7J-10	Signal is true when function decoder contains a reset status device order byte.
SCTR ADDR ENABLE (SAENB+)	fig. 0170	7K-6	Signal is true when function decoder contains a select read, select write, or select initial write device order byte.
SCTR CNTR BIT 0-7	fig. 0150		The outputs of the sector counter.
Bit 0 (SC0+)	fig. 0150	6L-14	
Bit 1 (SC1+)	fig. 0150	6L-13	
Bit 2 (SC2+)	fig. 0150	6L-12	
Bit 3 (SC3+)	fig. 0150	6L-11	
Bit 4 (SC4+)	fig. 0150	6M-14	
Bit 5 (SC5+)	fig. 0150	6M-13	
Bit 6 (SC6+)	fig. 0150	6M-12	
Bit 7 (SC7+)	fig. 0150	6M-11	
SCTR CNTR CARRY (SCTCC+)	fig. 0150	6L-15	Signal is true when four LSB's of sector counter contain 1111.
SCTR COMPARE (SCOMP+)	fig. 0150	4M-6	When this signal is true, a match exists in the sector comparator.
SCTR INCM BIT 0-5	fig. 0150		The outputs of the sector incrementer counter.
Bit 0 (SCI0+)	fig. 0150	5L-14	
Bit 1 (SCI1+)	fig. 0150	5L-13	
Bit 2 (SCI2+)	fig. 0150	5L-12	
Bit 3 (SCI3+)	fig. 0150	5L-11	
Bit 4 (SCI4+)	fig. 0150	5M-14	
Bit 5 (SCI5+)	fig. 0150	5M-13	
SCTR INCM CARRY (SCTIC+)	fig. 0150	5L-15	Signal is true when four LSB's of sector incrementer counter contain 1111.
SCTR INCM CLOCK (SCICL-)	fig. 0140	9L-8	The clock used for loading and incrementing the sector incrementer counter.
SECTOR ADDR ERROR (SEAER+)	fig. 0220	5N-6	Signal is true during a read operation when an error is detected in the sector address or the head or disc select code.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
SECTOR LOAD (SCTLD+)	fig. 0120	8C-3	When signal is true, the sector address byte is loaded into register A.
SECTOR PULSE FIXED DISC (XFPS+)	Disc Drive (fig. 0140)	P2-B12	Pulse occurs at beginning of each sector on fixed disc.
SECTOR PULSE REMOVABLE DISC (XSPR+)	Disc Drive (fig. 0140)	P2-B16	Pulse occurs at beginning of each sector on removable disc.
SEEK INCOMPLETE (XSING+)	Disc Drive (fig. 0260)	P2-B14	Status signal from disc drive. A low (active) level indicates that a seek operation was not completed due to a malfunction.
SEEK INCOMPLETE INT (XSINC+)	fig. 0260	10J-8	Signal is true when SEEK INCOMPLETE is low.
SEL ALT STATUS (ASFUN+)	fig. 0170	4J-2	Signal is true when function decoder contains an alternate status function device order byte.
SEL CYLINDER ADDR (SLCYL-)	fig. 0170	6K-2	Signal is false when function decoder contains a cylinder select device order byte.
SEL DEVICE ADDR (SDAD+)	fig. 0170	8D-4	Signal is true when function decoder contains a drive select device order byte, and DATA OUT INT is low.
SEL INITIAL WRITE (SWRT2+)	fig. 0170	7J-2	Signal is true when function decoder contains a select initial write device order byte.
SEL READ (SREAD+)	fig. 0170	7J-6	Signal is true when function decoder contains a select read device order byte.
SEL WRITE (SWRT1+)	fig. 0170	7J-4	Signal is true when function decoder contains a select write device order byte.
SERIAL READ DATA (XSRD+)	Disc Drive (fig. 0120)	P2-B11, P3-B4, P3-B9, P3-B14	The serial read data from the disc drive. A low level represents a binary 1.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
SERIAL SECTOR ADDR (SCSDA+)	fig. 0230	5K-5	The selected output (sector count, head select, or disc select) of the address bit multiplexer.
SET BYTE CNT 110 (SC110-)	fig. 0160	10B-10	Byte count is set to the two's complement of decimal 110 when this signal is false.
SET CYLINDER (XSTCY+)	fig. 0190	11M-11	Signal is supplied to disc drive. A low (active) level commands the disc drive to read the cylinder address on the ADDRESS BUS.
SHIFT ONE (S1+)	fig. 0040	2C-6	A memory cycle sequence is initiated each time this signal goes true.
SHIFT ONE A (S1A+)	fig. 0040	6B-2	Initiates a memory cycle sequence during a status transfer sequence.
SHIFT ONE C (S1C-)	fig. 0040	2C-8	Signal goes true each time a memory cycle sequence is initiated for a data transfer.
START (START+)	fig. 0040	1B-2	Signal is true when memory cycle sequencer is in state 6 (idle), the memory is not busy, a status transfer is not in process, and neither a device order nor an information byte is being sent by the CPU.
START MEMORY CYCLE SEQUENCE (SMCS+)	fig. 0030	10C-5	SMCS flip-flop is set to start each memory cycle sequence.
STATUS (STAT+)	fig. 0030	2A-12	Signal is true while a status transfer is in progress.
STATUS IN (INST+)	fig. 0070	4F-3	Signal is true when a status in device order addressed to the DMA channel is received.
STATUS IN PROCESS (STAS+)	fig. 0070	6C-5	Signal is true while a status transfer is in process.
STROBE COMPARATOR (STCOM+)	fig. 0140	9N-4	The sector comparator is enabled when this signal is true.
TIME OUT CNTR (CNTR+)	fig. 0290	7C-11	Signal is true when an abnormal end of operation condition exists.

Table 4-1. Logic Glossary (continued)

Signal	Origin	Test Point	Description
WRITE CHECK (WRCH+)	fig. 0250	7M-8	Signal is true when a select write device order is contained in the function decoder, and read sequencer is in READ PHASE 0. Enables a sector compare one sector early.
WRITE DATA REQ (REQC+)	fig. 0280	5A-8	During a write operation, register A is cleared each time this signal goes true.
WRITE GATE (WRGT+)	fig. 0210	8N-5	Signal is supplied to disc drive. A low (active) level enables the disc drive to perform a write operation.
WRITE PHASE 0-7	fig. 0200		The outputs of the write sequencer.
0 (WPH0+)	fig. 0200	6G-3	
1 (WPH1+)	fig. 0200	6G-4	
2 (WPH2+)	fig. 0200	6G-5	
3 (WPH3+)	fig. 0200	6G-6	
4 (WPH4+)	fig. 0200	6G-10	
5 (WPH5+)	fig. 0200	6G-11	
6 (WPH6+)	fig. 0200	6G-12	
7 (WPH7+)	fig. 0200	6G-13	
WRITE SEQUENCE CLOCK (WSQC+)	fig. 0200	7F-8	The clock used to advance the write sequencer.
WRITE UNSAFE (XWUSF+)	Disc Drive (fig. 0260)	P2-B21	Status signal from disc drive. A low (active) level indicates that a malfunction exists in the disc drive that may prevent correct write operations.
WRITE UNSAFE INT (XWUSF+)	fig. 0260	10J-10	Signal is true when WRITE UNSAFE is low.

Section 5

PARTS LIST

This section contains the parts list for the DMA/Disc Storage Unit Controller, Part Number 900280. The parts are listed in reference designator order. Figure 5-1 is the parts location diagram.

Reference Designator	Part Number	Name	Qty.
C1	101113	Capacitor, 47pf	1
C2, C4, C5, C9, C12, C18, C19, C22, C23, C27, C29, C31, C33, C35, C37	101101	Capacitor, 4.7uf	15
C3, C6, C7, C8, C10, C11, C13, C14, C15, C16, C17, C20, C21, C24, C25, C26, C28, C30, C32, C34, C36, C38, C39, C40	101100	Capacitor, 0.01mfd	24
C41	101118	Capacitor, 220pf	1
C42	101119	Capacitor, 680pf	1
R1	101016	Resistor, 680 ohm, ¼w	1
R3, R4, R5, R6, R7, R34, R39, R40, R41, R42, R43, R48, R50, R53	101003	Resistor, 1K, ¼w	14
R8	101014	Resistor, 330 ohm, ¼w	1
R9	101019	Resistor, 2.2K, ¼w	1
R10, R13, R16, R19, R22, R25, R28, R31	101000	Resistor, 200 ohm, ¼w	8
R12, R15, R18, R21, R24, R27, R30, R33	101013	Resistor, 220 ohm, ¼w	8
R35, R36, R37, R38, R44, R45, R46, R47, R51	101001	Resistor, 100 ohm, ¼w	9

Reference Designator	Part Number	Name	Qty.
R52	101035	Resistor, 510 ohm, ¼w	1
Y1	101300	Crystal, 6.24 MHz	1
1A	101576	I.C., SN74H10N	1
1B	101541	I.C., SN74S04N	1
1C	101558	I.C., SN74H30N	1
1D, 1E, 1F, 1G, 1K, 1L, 1M, 1N, 1O, 2N, 2O, 11D, 11E, 11J, 11K, 11L, 11M, 11O	101514	I.C., SN7438N	18
1H, 1J, 2A, 10J, 10L	101540	I.C., SN74H04N	5
1X, 5D, 5F, 8N, 9O, 10C, 10O	101505	I.C., SN7474N	7
2B	101535	I.C., SN74S00N	1
2C	101543	I.C., SN74S10N	1
2D, 2E, 2K, 2L, 4L, 4M	101515	I.C., SN7485N	6
2F, 2G, 2H, 2J	101549	I.C., SN74175N	4
2M	101577	I.C., SN74H00	1
3A, 4K, 4O, 6D, 8C, 9D	101500	I.C., SN7408N	6
3B	101568	I.C., SN74H20N	1
3C, 4A, 4D, 4N, 5N, 5O, 6E, 6F, 7D, 7N, 8E, 8K, 9C, 9H, 9K, 9L, 10A	101507	I.C., SN7400N	17
3D, 4H, 4J, 6B, 7G, 7J, 8O, 9A, 9E, 10H	101509	I.C., SN7404N	10
3E, 4F, 6C	101504	I.C., SN74107N	3
3F, 3G, 3H, 3J, 5G, 5H, 5J, 5L, 5M, 6L, 6M, 7C	101574	I.C., 9316	12
3K, 3N, 11G	101518	I.C., SN74199N	3
4B, 4C	101575	I.C., 93H00	2
4E, 4G, 5C	101546	I.C., SN74H21N	3

Reference Designator	Part Number	Name	Qty.
5A, 6N, 6O, 7A, 7F, 7K, 8M, 9G, 9M, 10F	101506	I.C., SN7410N	10
5B, 6H, 7H, 8D, 8F, 9F, 9N, 10B, 10G, 11N	101502	I.C., SN7402N	10
5E, 6A, 7E, 8L, 9J	101508	I.C., SN7420N	5
5K	101520	I.C., SN74151N	1
6G, 7O	101551	I.C., SN74164N	2
6J, 11F	101517	I.C., SN7475N	2
6K	101513	I.C., SN7442N	1
7B	101544	I.C., SN7427N	1
7L, 10D	101519	I.C., SN7486N	2
7M, 8B	101545	I.C., SN74H11N	2
8A, 10N	101542	I.C., SN7432N	2
8G, 8H, 8J	101548	I.C., SN74174N	3
9B, 11B	101547	I.C., 74H74N	2
10K, 10M	101503	I.C., SN7495N	2
11C	101536	I.C., SN74153N	1*

*Replaced by a socket, P/N 100162, and jumpered plug, P/N 900796, in some multiple-drive systems, and systems S/N 1100 and up.

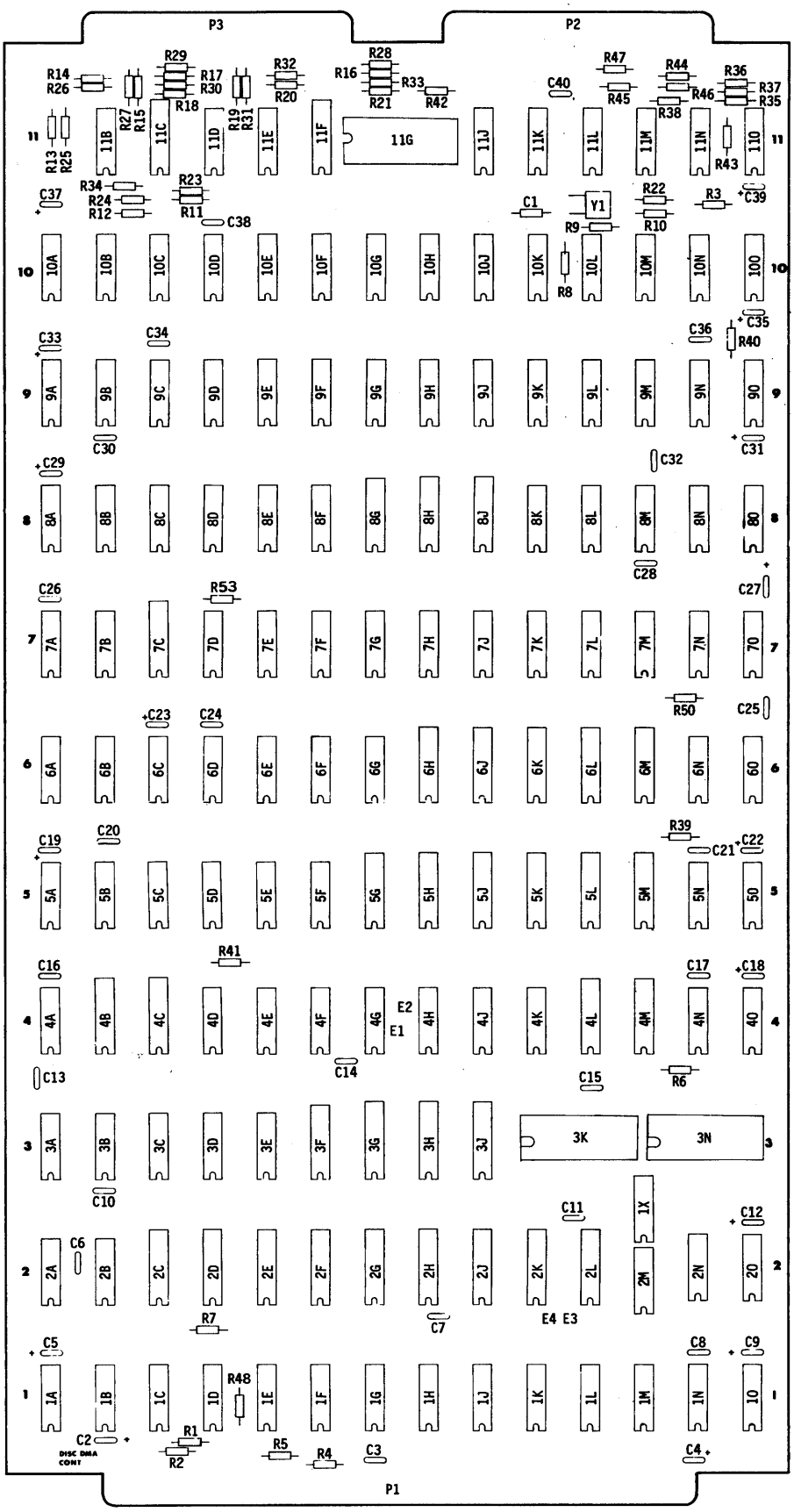


Figure 5-1. Location of Parts