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Towards the Teraflop in CFD

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2 Machine Characteristics

2.1 BBN

The BBN Butterfly is the oldest [3] among the machines considered here. Its history goes back to the late seventies, when the Butterfly development began, mainly as a switching network. The latest product in this series is the Butterfly TC2000. This project is a commercial development by BBN funded through a limited partnership. It is not related to the Monarch project, which was funded in its early stages by DARPA, but is apparently no longer actively pursued by BBN, and has currently no DARPA funding.

The Butterfly TC 2000 uses the new Motorola 88000 RISC chip for the processor nodes. The projected performance of the 88000 with a floating-point unit on the chip is about 10 Mflops for 64 bit computation. Since this is a scalar processor the LINPACK performance is a relatively high 7 Mflops. There will be 4 - 16 Mbyte memory per node.

The switch of the Butterfly TC 2000 is completely redesigned when compared with the earlier Butterfly GP1000. It will support 4 Gbytes global memory access, with a bandwidth of 38 MBytes/sec. An initial configuration will be 64 node system. A final extension to 512 processors and 16 Gbytes of memory is planned.

BBN had an ambitious follow on project to the TC2000 called Coral. However, BBN was unable to attract the necessary funding for continued support and closed down its advanced computing division in August of 1991.

Table 1: BBN TC2000

Processor	
Number of processors	8–504
Chip or technology	88000 with 3 cache chips
Clock rate	20MHz
Architecture	RISC
Peak Mips	20
Peak Mflops 32 bit	20
64 bit	10
Peak Gflops total 64bit	5
Full System Price	$ 20M
IEEE arithmetic	yes
Memory	
Memory per processor	4–16Mbyte
Technology	CMOS 1M DRAM
Instruction Cache	32K
Data cache	16K
Total maximum memory	16Gbyte (?)
Price per Mbyte	$ 2500
Addressing virtual	32bit
Addressing physical	34bit
Peak access rate	38Mbytes /sec
Access rate per processor	
Latency for nonlocal data	2400nsecs = 48 clks
ECC	Parity
Interconnect	
Interconnect topology	Butterfly switch
	Packet routed with retry if blocked
Interconnect technology	gate arrays
	uses 8 X 8 X 8bit Xbars
I/O	
I/O architecture	VME/PE
Bandwidth total	2500 Mb/sec
Achievable	
Striping	No
Software	
Operating System	nX + pSOS
NFS	yes
Languages	own parallel Fortran, PCF like
	Linda

[3] W. Crowther, J. Goodhue, R. Gurwitz, R. Rettberg, and R. Thomas. The Butterfly parallel processor. *IEEE Computer Architecture Tech. Newsletter*, pages 18 – 46, September 1985.