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ABSTRACT and CONTENTS

This document specifies the special functions, branch conditions, and pseudoscratchpad addresses to be used in CPU 1.5.

Parenthesized numbers indicate board on which function is implemented (SP. FCN. #1 or SP. FCN. #2 / BRANCH COND. #1 or #2)

* means VCY must be set.

$ shows differences from CPU 1.0.

% means implemented but not used in CPU 1.5.

SPECIAL FUNCTIONS IN CPU 1.5

	MS	FUNCTION	
	Ø	LCY Ø	— Implemented on Adder/Cycler Card
	1	LCY 1	
	2	LCY 2	
	3	LCY 3	
	4	LCY 4	
	5	LCY 8	
	6	LCY 12	
	7	LCY 16	
	1Ø	LCY 2Ø	
	11	LCL Z	
	12	LCH Z	
$%	13	(Implemented, not used; was called SPFZ) (1)	
	14	ALERT (1)	
	15	POT (1)	
	16	PIN (1)	
	17	Request Strobe Latch #1 (gating with X occurs on request strobe card) (1)	
	2Ø	UNPROTECT (1)	
	21	(Not Implemented)	

22 Load Memory Request Priority Field (LPF) (1)

23 Reset Request Strobe Latch #1 (1)

24 Reset Central Memory Request Unit (1)

25 Request Protect (1)

26 SET B (2) (also generated on (1) as a high true RESET TU)

27 GSB: { E1(23)←E, E1(2Ø)←XCAR, E1(22)←XOV, E1(14)←M94Ø, E1(21)←XTOV } (2)

3Ø SET A (2)

31 CLEARA :(A←B←Ø) (2)

32 RRSL2 :(Request Strobe Latch #2←Ø) (1)

33 SABCDEØ : (SR←Z;A←B←C←D←E←Ø) (2) SMS1' (1)

34 MAPFETCH (1)

35 SETC:(C←1; A←B←D←Ø) (2)

36 SETD:(D←1) (2)

37 MAP (2)

4Ø-47 MEMORY REFERENCES

- 4Ø Release (1)
- 41 Prestore
- 42 Store
- 43 Store and Hold
- 44 Fetch
- 45 Fetch and Hold
- 46 —
- 47 Prefetch

50 CLEARA: (A←B←Ø) (2)

```
      51  MAP+SR : (MAP ; SR←RØ)  (2)
      52  SSOURCE : (SR←Z)  (2)
      53  ZTOMAP:  (PMAP [RØ(VAl)]←Z)  (2)
      54  MAPAD:  (El←VAl(AD))  (2)
      55  PSB:  E←Z(23)  (2)
              XOV←Z(22)
             XTOV←Z(21)
             XCAR←Z(2Ø)
             M94Ø←Z(14)
      56  READS : (El←SR)  (2)
      57  HROV : (OVFLW←OV ; CARRY←CY)  (2)
      6Ø  SBB : (BSELECT←1)  (1)
      61  SBA : (BSELECT←Ø)  (1)
      62  CLEARMAP : (Set Empty Flags in all maps)  (1)
$     63  SCAN :     (Sets SC on next instruction until
                map scan is done) (2)
$%    64  }
$%    65  }  Implemented, not used
      66  ROV : (XTOV←OV ; XOV←XOV OR OV ; XCAR←CY)  (2)
      67  CLEARTOV : (XTOV←Ø)  (2)
      7Ø  ABCDØ : (A←B←C←D←Ø)  (2)
      71  X23LOK : (LOCK←X(23))  (2)
      72  CLEARM94Ø : (M94Ø←Ø)  (2)
      73  CLEARXOV : (XOV←Ø)  (2)
      74  COMAP : (Set Empty Flags in own map)  (2)
$     75  TAKE  (2)
$     76  SET STROBE 2  (2)
```

% 77 (Implemented, not used, called SMS4') (2)

BRANCH CONDITIONS IN CPU 1.5

	MC	CONDITION
	Ø	Never Branch
	1	Always Branch (1)
	2	Z=Ø (1)
	3	Z≠Ø (1)
	4	Z<Ø (1)
	5	Z≥Ø (1)
	6	Z>Ø (1)
	7	Z(15)=Ø (1)
	1Ø	Z(16)=Ø (1)
	11	RØ<Ø (1)
	12	RØ≥Ø (1)
	13	Z≤Ø (1)
	14	Z(18)=1 (1)
	15	Z(18)=Ø (1)
*	16	X≥Ø (1)
*	17	X<Ø (1)
	2Ø	Always Branch (1)
	21	M(1)=1 (1)
	22	LB=Ø (1)
	23	LB≠Ø (1)
	24	RØ(2)=1 (1)
	25	RØ(2)=Ø (1)
	26	ATLAT1=Ø (execution resets the latch) (1)
%	27	SP=Ø : (Request Strobe Latch #1=Ø) (1)

```
*     3Ø  PROTECT ≠X  (1)
%     31  RSL2=Ø  (1)
$     32  STERR:(Y(Ø) or Y(1)=1)  (SP. FCN. #2)
      33  A=1  (1)
      34  B=1  (1)
      35  C=1  (1)
      36  ATLAT 1=1  (execution resets the latch)  (1)
      37  XOV=1  (1)
      4Ø  M(13)=Ø  (1)
$     41  INTRPT : ((RSL1 OR TO)AND LOCK') OR RSL2 OR
                  STEP OR M94Ø OR ((PAR=3777) AND NIREAD) OR
                  (((PAR=Ø) OR A OR B) AND NIREAD')
                  (1,2, SP. FCN. #2)
$     42  XPAGE : ((PAR=3777) AND NIREAD) OR ((PAR=Ø) AND
                  NIREAD')  (1)
$     43  M94Ø=1 : (M94Ø=1) AND (((RSL1 OR TO) AND LOCK')
                  OR RSL2 OR STEP)'  (1, SP. FCN. #2)
      44  CMPE=1 : (Central Memory Parity Error)  (1)
      45  BP=1 : (Breakpoint)  (1)
      46  XCAR=1  (2)
      47  D=1  (2)
      5Ø  M(5)=1  (2)
      51  AORB :  (A OR B = 1)  (2)
%     52  Z=4B7  (2)
*     53  Y<Ø  (2)
$     54  STINST OR A:((12B<M(OPCODE)<2ØB)OR A=1)  (1,2)
```

```
      55  LAX : (Z(3)≠(RØ(OPCODE)=47B))   (2)
$     56  INTRPT3 : (XPAGE OR M94Ø)   (2, SP. FCN. #2)
      57  OVFLW=1   (2)
      6Ø  STEP=Ø   (Execution Resets the Latch)   (2)
      61  CARRY=1   (2)
$     62  RØ(2)=1 OR RØ(Ø)=1 OR A=1 OR B=1 OR D=1   (2,SP.FCN.#2)
%     63  Implemented, not used
      64  INTRPT1 : ((RSL1 OR TO) AND LOCK') OR RSL2 (2)
$     65  INTRPT2 : ((RSL1 OR TO) AND LOCK') OR M94Ø
                (2, SP. FCN. #2)
      66  RØ(1)=1   (2)
%     67  Implemented, not used
      7Ø  SP AND NOT LOCK : (RSL1 AND LOCK')=1   (2)
      71  M(9)=1   (2)
      72  TO : (TO AND LOCK')=1   (2)
      73  M(Ø)=M(1)   (2)
      74  M(4)=1   (2)
      75  M(13)=1   (2)
      76  FPN: { (E1←4, BRANCH←1) IF OVFLW=1, ELSE
                 (E1←5, BRANCH←1) IF (Z=Ø AND LB=Ø), ELSE
                 (E1←6, BRANCH←1) IF (Z=4B7 AND LB=Ø), ELSE
                     Ø            IF (Z(Ø)≠Z(1)), ELSE
                 (E1←1, BRANCH←1) IF (Z(1)≠Z(2)), ELSE
                 (E1←2, BRANCH←1) IF (Z(2)≠Z(3)), ELSE
                 (E1←3, BRANCH←1).                          } (2)
$     77  Always BRANCH
```

PSEUDO SCRATCHPAD REGISTERS IN CPU 1.5

SSP BITS	USAGE
4Ø - 46	Used by multiply (see specification). Note that TSPY and LSPX need not be given with these addresses, as the registers are either read only or write only. Any attempt to use 4Ø - 47 while multiplier is running stops the EU.
5Ø	NIR: Read only, no TSPY needed.