B 9348-50 Operator Display Terminal

TECHNICAL MANUAL
VOLUME 1:

OPERATION and MAINTENANCE

Burroughs

FIELD ENGINEERING

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GENERAL DESCRIPTION

The term B 9348 refers to a series of input and display terminals. The series of units are designated as styles B 9348-50, B 9348-51, B 9348-53, and B 9348-54.

The Burroughs B 9348 Input and Display System (figure 1-1) is a free-standing, self-contained, cathode-ray tube (CRT) display terminal. Input information to the B 9348 is compiled either locally (from the keyboard) or remotely (from a central processor), or from another terminal. Display on the B 9348 is of fully-formed characters rather than dot-matrix characters. The B 9348 has the capacity to display 1920 characters in a format of 24 lines of 80 characters each, plus an additional 80-character status line.

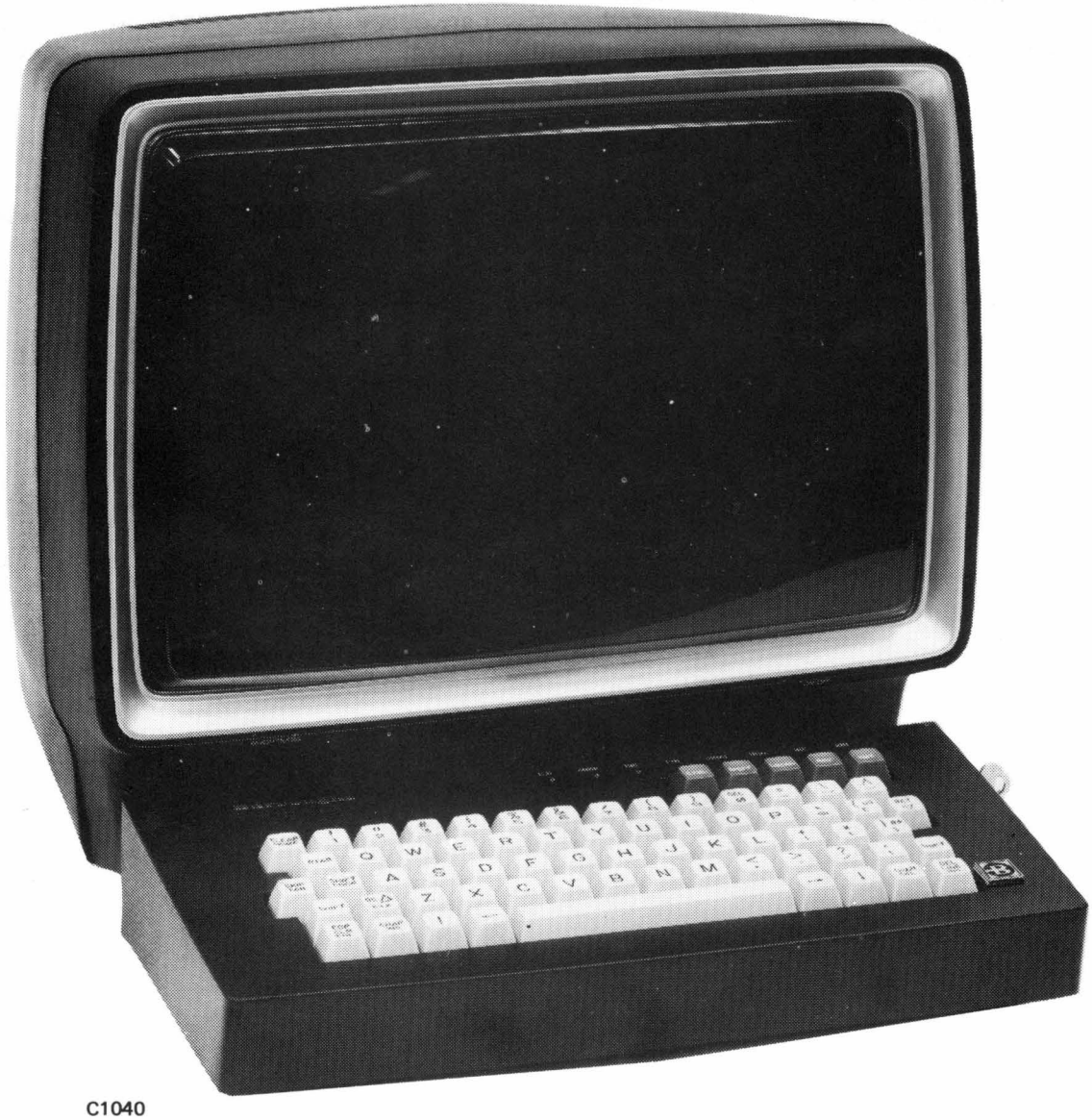

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Figure 1-1. TD 850 Input and Display System (Terminal)

The B 9348 has two physically separate assemblies: the display unit monitor assembly, and the keyboard unit assembly. The two units are connected by a cable which permits the keyboard unit to be located up to six feet away from the display unit (with a standard length of 3 feet). The B 9348 display terminal utilizes Modular Terminal Systems-1 (MTS-1) components and implementation techniques. The basic organization is shown in figure 1-2. MTS-based terminals have a number of system levels used for implementation. The innermost levels are the basic hardware (H-Level) and the native language of the terminal processor (M-Level). An interpreter, together with a set of operators (which are themselves written in the M-Level language), execute S-Level code. S-Level code is designed to support a simple, structured, procedure-based language. The outer level is called Terminal Systems Language (TSL). All functions of the B 9348 are defined through the use of TSL. The TSL source code is compiled to the S-Level. New MTS components continue to support the S-Level and TSL source code, thereby helping to maintain the functional characteristics of the product when new cost-improved components are used.

BASIC CAPABILITIES

The MTS-1 has a wide range of standard features and numerous options, as outlined in figure 1-2. A wide range of data communications capabilities are also available. These capabilities allow data to be transmitted between a terminal and a central processor. Data can also be transmitted from terminal to terminal over half duplex lines. These terminals and the central processor are operated in an asynchronous, synchronous, or direct-connect mode that uses certain multipoint or point-to-point communications procedures.

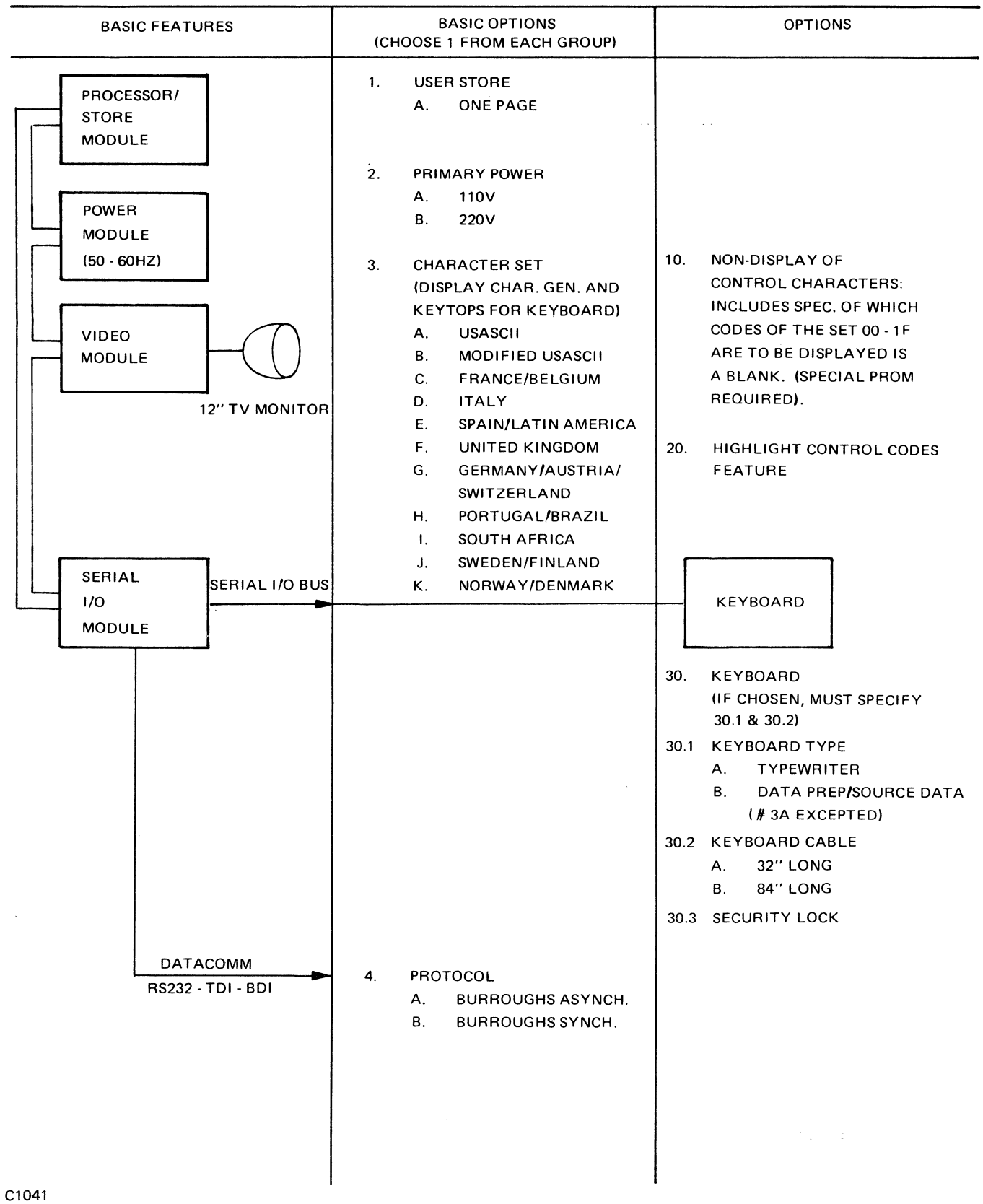

Figure 1-2. B 9348 Features and Options

OPERATION

The B 9348 is a versatile machine with a wide variety of capabilities, including:

a. Multiple page definition for simultaneous data comm and/or peripheral communication and for local data entry.

b. Form creation and definition for sophisticated data entry and display.

c. Editing capabilities, such as character and line insertion and deletion.

d. Highlighting and formatting.

e. Data communication.

These features are principally used in keyboard entry and in the data communication stream. Particular variations of these may be fixed through programmed configuration.

Main Features

By installation option, the B 9348 can be programmed to operate with many features which affect the movement of data within the terminal. Each of these main features is described in the following paragraphs.

CONFIGURATION CONTROL

The B 9348 has 32 bytes of permanently stored data which are used to program the terminal's configuration. When the power is turned on, the permanently stored data is automatically loaded into a read/write memory, where it is used as the active configuration program. The permanently stored data can be changed by the operator or by special escape (ESC) sequences from a remote controller. The active configuration program in read/write memory can be changed by operator (CTRL) control or through data communication escape (ESC) sequence control. If the active configuration program is changed by CTRL or ESC control, the next power off-on sequence will erase the read/write memory and write the permanently stored data back into the read/write memory.

ESCAPE (ESC) FUNCTIONS

The B 9348 has the ability to accept a software control message to enable or disable many of its display functions. The software control escape sequence contains a two, three, four, or five character sequence which produces a specific function code. The escape sequence is contained in the text portion of a receive control message. The CTRL key on the keyboard also produces the ESC code, with the result that most of the software controllable ESC function that can be initialized by the central processor can also be initialized through the keyboard.

DATA COMM POINTER

The data comm pointer is a memory-position marker from which all data are transmitted or received. In single page operation or when the data comm pointer and cursor are on the same page, moving the cursor within the limits of the page causes a like movement of the data comm pointer. The data comm pointer and the cursor therefore remain aligned. In multiple-page operation, the data comm pointer and the cursor can be operated on different pages. This results in data being received on the page containing the data comm pointer, while data can be entered simultaneously from the keyboard on the page containing the cursor.

Moving the cursor without moving the data comm pointer causes the following situations to occur:

a. When the cursor and the data comm pointer are on different pages, the control sequence (CTRL〉) or ESC & cause the cursor to move to the position of the data comm pointer.

b. The control sequence for page advance (CTRL→) or page back (CTRL←) causes the cursor to move to another page independent of the data comm pointer.

c. When the cursor is located on the last line of the page containing the data comm pointer, the control sequence for scroll up (CTRL↑) causes the cursor to move to the next page without moving the data comm pointer.

d. When the cursor is located on the first line of the page containing the data comm pointer, the control sequence for scroll down (CTRL↓) causes the cursor to move the preceding page without moving the data comm pointer.

Moving the data comm pointer causes the following situations to occur:

a. The page select escape sequence (ESC $ PAGE) causes the data comm pointer to be moved to the home position of the selected page.

b. Pressing the transmit (XMT) key causes the data comm pointer to be moved to the cursor position.

c. Pressing the receive (RCV) key moves the data comm pointer to the cursor position.

DISPLAY CAPACITY (WORKING DATA FIELD)

The B 9348 has a variable working data field of up to 1920 characters. The configuration program selects one of four basic configurations: 12 lines of 40 or 80 characters, and 24 lines of 40 or 80 characters. Selection of one of the four basic configurations can be temporarily changed by CTRL or ESC control.

STATUS LINE DISPLAY

The status line is displayed on the 25th line position of the screen and is 80 characters in length. The status line provides information to the operator as follows.

16 Char.	52 Char.	7 Char.
Error Conditions	Special Messages	Page Number

The first 16 characters of the status line are used to display error messages; for example, POWER FAULT, DATA COMM ERROR, KYBD DATA LOST, PRINTER ERROR, or CASSETTE ERROR. The next 52 characters of the status line are used to display special messages from the central processor. Special messages are used to inform the operator of computer or system status, identification of non-displayed pages, or special instructions. To write a special message for display, the fast select, group select, or broadcast select procedure is used in conjunction with escape sequence ESC RA (a) (b) (c), which is interpreted as follows:

a. The four character hexadecimal memory address used to identify the starting address assigned for special messages.

b. The two character hexadecimal byte count used to identify the number of bytes of data contained in part (c) of the ESC sequence.

c. The ASCII data to be displayed as the special message. This data may contain up to 52 characters.

The last seven characters of the status line are used to identify the page number on which the cursor is located.

NEGATIVE VIDEO (NON-FORMS)

The B 9348 has the capacity to display white characters on a black background (normal video) or black characters on a white background (negative video). When power is turned on, the display is in normal video. Negative video is enabled and disabled through keyboard CTRL control or software ESC control.

NEGATIVE VIDEO (IN FORMS)

When forms mode and negative video are both active, the unprotected data areas are displayed as normal video as follows: The GS, US, or left forms delimiter are the start of a reverse video mode, and the RS or right forms delimiter ends the reverse video mode. A reverse video field on a negative video background appears as normal video. Any unprotected data field that continues from the last column to column 1 of the next line does not continue the reverse video.

DATA HIGHLIGHTS

The B 9348 has the capacity of displaying five modes of data highlighting: underline video (SI), bright video (SUB), reverse video (SO), blink video (CAN), secure video (EM).

Data highlighting is enabled by receiving one or more of the five data highlighting control characters (SI, SUB, SO, CAN, or EM) within the text section of a message. The RS control character is used to cancel all data highlighting. The data highlighting modes are independent, thereby permitting a combined action upon the video data. The active data highlighting modes are not displayed beyond an RS character or the end of the display line in which the highlight is used. The data highlight control characters are stored in memory, but they are not displayed. If the terminal is in negative video mode, the effects of data highlighting are reversed.

The independent state of data highlight modes allows nesting and gives a cumulative action upon the video data to the extent that no highlight extends beyond either an end highlight code (RS) or beyond the end of a display line.

Underline Video (SI)

Upon reading an SI code from memory, the screen begins an underline data highlight and maintains it until an end highlight code is read. The underline highlight consists of solid video in contrast with the opposite mode background video.

Bright Video (SUB)

The bright video highlight causes brighter characters to appear when the display is in normal video mode. Actuation of the bright video highlight (when the display is in the negative page video mode) causes brighter background to appear.

Reverse Video (SO)

Upon reading an SO code (ASCII 0.14) from memory, the screen starts a reverse video display. The screen maintains this highlight until an end highlight code is read, thereby ending all selective highlight fields. The reverse video highlight causes negative video to be displayed from the initial SO code to the end highlight code, provided that the display is in normal video mode. Activation of the reverse video highlight (when the display is in a negative video mode) causes normal video to be displayed from the initial SO code to the end highlight code.

Blink Video (CAN)

The screen, upon reading a CAN code (ASCII 1.8) from memory, commences a blinking video display at a 1.5 hertz rate. The screen maintains this highlight until an end highlight character causes video data to alternate with solid background. This solid background mode is dependent upon negative video or normal video mode of display.

Secure Video (EM)

Upon reading an EM code (ASCII 1.9) from memory, the screen begins placing blanks on the display and maintains this highlight until an end highlight character is read. These blanks consist of solid display matrix for each secured character.

CURSOR DISPLAY

The B 9348 generates a visual cursor which indicates the location of data entry from the keyboard. The cursor is displayed as the negative image of the character at the cursor location. The configuration program selects one of three basic configurations: a blinking cursor at a 1.5 hertz rate, a non-blinking cursor, or no cursor displayed. Selection of one of these basic configurations can be temporarily changed by CTRL or ESC control.

CURSOR POSITIONING

The cursor position is stored in the cursor counter and not in the display memory. After each character is loaded into the display memory from the keyboard, the cursor is advanced one position to the right. When a line is filled, the cursor is advanced to the first position of the next line down. The cursor can also be positioned by presetting the cursor counter through CTRL or ESC control.

EDIT FUNCTIONS

Edit functions include the character insert by line or page, character delete by line or page, line insert or delete, line movement up or down, clear to end of line or page, lower case enable or disable, and search mode. All these edit functions may be controlled remotely by ESC codes or locally by CTRL key sequences.

CHARACTER INSERT BY LINE OR PAGE

The terminal is capable of a character insert function. Pressing the CHAR INS key places the terminal into the character insert mode and automatically inserts a single space at the cursor position. Subsequent pressing of an alphanumeric key (including space) causes the alphanumeric character to be inserted at the cursor location. The succeeding characters within the line are moved one space to the right. Surplus characters, if any, are shifted off the end of the line and lost. If the CTRL key is activated prior to pressing the CHAR INS key, the function is performed on a page basis. The succeeding characters are moved one space to the right and down line by line. A second pressing of the CHAR INS key disables the character insert mode.

When in the forms mode, the character insert function causes data shifting within the single unprotected data field (in which the cursor is located). The terminal can also perform the character insert function through program control. The program character insert function differs, however, from the keyboard control function. The character insert mode is not entered by program control. Instead, each character to be inserted requires a new character insert program control code.

CHARACTER DELETE BY LINE OR PAGE

The CHAR DEL key causes the character displayed at the cursor location to be erased. The succeeding characters within the line are moved one space to the left. If the CTRL key is activated prior to pressing the CHAR DEL key, the function is performed on a page basis. The succeeding characters down the entire page are moved one space to the left and up line by line.

When in the forms mode, the character delete function causes data shifting within the unprotected data field (in which the cursor is located). The terminal also performs the character delete functions through central system program control.

LINE INSERT DELETES

The terminal performs the page-specific line insert and delete functions. The line insert function causes all data in the following lines (including the line in which the cursor is positioned) to be moved down one line. The line delete function causes the line in which the cursor is positioned to be erased, and all data in the following lines to be moved up one line. The line insert/delete functions are initiated by the LINE DEL/INS key (shifted and unshifted respectively), or by program control. This function is inhibited in forms mode.

LINE MOVEMENT UP/DOWN

Through keyboard control (CTRL V/CTRL B or program control ESC/ESC), the terminal can cause a line of display data to be interchanged with the line above or below it, depending on the function selected. The line of data to be moved is selected by placing the cursor in that line. When line movement causes data to be displaced, the displaced data reappears in the original position of the line moved. The cursor follows the line moved in all cases. An upward movement of the top line of a page causes the bottom line of the page to be exchanged with the top line of the page. The same exchange occurs if a downward movement is requested for the bottom line of a page. This function is inhibited during forms mode.

CLEAR TO END OF LINE OR PAGE

The terminal can clear data from the cursor position to the end of a line or page. In Non-forms, the unshifted CLR EOP/EOL key clears all data from the cursor position to the end of a line. In forms, the unshifted CLR EOP/EOL key clears all data from the cursor position to the trailing delimiter.

In Non-forms, the shifted CLR EOP/EOL key clears all data from the cursor position to the end of the page. In forms, the shifted CLR EOP/EOL key clears all unprotected data from the cursor position to the end of the page. The terminal is also capable of initiating the clear to end of line or page function through program control (ESC K/ESC J).

LOWER CASE ENABLE OR DISABLE

Through keyboard or program control (CTRL T/CTRL Y and ESC Z/ESC Y), the terminal can enable or disable the display of lower case letters. When the lower case is disabled, all letters are displayed in upper case.

NOTE

Keyboard control disables only keyboard entered lower case. Program control disables only data comm entered lower case.

SEARCH-MODE (ITEM CORRECTION)

The search mode is enabled or disabled through the keyboard CTRL A/S or the central system program ESC E/F control codes. If search mode is enabled, placing the terminal in forms mode causes an immediate search for either the error character (¦), or an opening delimiter. If the cursor stops on an error character (¦) in a protected field, data may be written into that one location. Either entering data or pressing the SKIP key causes a skip to the next unprotected field. In the search mode, entering either 3-character control code ESC - CHAR or CTRL E CHAR assigns a selected search character. CHAR is any selected search character and functionally replaces the error character. Disabling the search feature cancels the selected search character.

After correction of data, with the terminal still in forms mode and search enabled, activation of the XMT key causes the total form (protected and unprotected data) to be transmitted. In Non-forms, the search feature operates the same as in forms, except it does not recognize forms delimiter. (Depressing the SKIP key causes the cursor to search for the next error character).

PAGE ROLL UP OR DOWN

The B 9348 has the ability through CTRL or ESC control to cause the data on a displayed page to roll up or down while the cursor remains in a fixed position in relation to the page. During a roll-up function, all the data on the screen is simultaneously transferred line-for-line up the screen. The data transferred from the top of the page appears at the bottom of the page causing a "wrap-around" effect. For a roll-down function, the movement of data is reversed. In the forms mode, the page roll function is inhibited.

DISPLAY SCROLL UP/DOWN

The B 9348 has the ability through CTRL control to cause the data on the display to scroll up or down while the cursor remains in a fixed position on the display screen. During a scroll-up function, all the data on the display is simultaneously transferred line-for-line up the display. Data on the top line of the display shifts off the display and new data appears on the bottom line of the display. This function can be repeated until the last line of display memory is displayed. When the last line is displayed, additional scroll-up functions are ignored. For a scroll-down function, the movement of data is the reverse to that of a scroll-up function. Scroll functions operate in either forms or non-forms mode.

TABULATION

The B 9348 has the ability of both forward and reverse tabulation, using either fixed tab stops, variable tab stops, or tab field identifiers. The fixed tab stops are located at every eighth character position (1st, 9th, 17th, and so on). The variable tab stops are set or reset through CTRL or ESC control in any of up to 80 column positions. The configuration program selects either fixed or variable tabulation. This selection may be temporarily changed by CTRL or ESC control, so that the terminal can be operated with fixed tab stops or variable tab stops but not both. The tab field identifier option can be operated with either fixed or variable tabulation in either forms or non-forms mode. In forms mode, the TAB key causes a field identifier (→) to be written into memory at the cursor location. If the field is also a right justified field, the field identifier (→) is written into memory at the first position following a left delimeter. During transmission, the character spaces between the field identifier (→) and the next field are not transmitted. In non-forms mode, the TAB key causes a field identifier (→) to be written into memory at the cursor location. The cursor then automatically advances to the next tab stop. During transmission, the character spaces between the field identifier (→) and the next tab stop are not transmitted. The writing of the field identifier (→) into memory can be disabled through CTRL or ESC control.

FORMS DELIMITERS

The B 9348 has the ability, through the configuration program, to accept any two characters as additional forms delimiters. When in forms mode, the B 9348 converts the additional delimiters to the US (▻) and RS (◅) symbols. The US (▻) character is used to signal the start of an unprotected data field, and the RS (◅) character is used to signal the end of an unprotected data field. In addition to the basic forms delimeters, the GS (Δ) character is used to signal the start of an unprotected right justify field, and the FS (🄵) character is used to signal the start of a protected data field that can be transmitted. Both of these special fields are terminated with the RS (◅) character.

RIGHT JUSTIFY FIELD

The B 9348 has the ability to right justify in the forms mode. The GS (Δ) character is used to signal the start of a right justify field, and the RS (◅) character is used to signal the end of the field. When a right justify field is entered, the cursor automatically moves to the right-most position of the field. As data is entered at the cursor position, the data is shifted to the left, as follows:

Δ - - - - - ◅
Δ - - - - 1 ◅
Δ - - - 1 2 ◅
Δ - - 1 2 3 ◅

FIELD OVERFLOW INHIBIT

The field overflow inhibit function operates in forms mode only. If this function is disabled, then a data character that is entered into the last position of an unprotected data field will cause an automatic cursor advance to the first position of the next unprotected data field. If the field overflow inhibit function is enabled, then the entered alphanumeric data will not cause an automatic cursor advance to the next unprotected data field, but the cursor will sit in the last data position and overwrite data characters as they are entered. The field overflow inhibit allows only the TAB, SKIP, or reverse (R tab) keys to move the cursor between unprotected data fields.

TRANSMISSION OF CONTROL MESSAGES

The terminal has the ability to transmit two types of control messages; the cursor position message and the numeric control message. The cursor position message is initialized by pressing the specify (SPCFY) key. Then, when the terminal is polled, the terminal responds with its normal heading, followed by STX, ESC, ", POS, LINE, ETX, BCC. The POS character represents the cursor column position plus 32, and the LINE character represents the cursor row position plus 32. The 32 bit is added to the column and row counts in order to prevent the generation of a communication control character such as ETX. The numeric control message is initialized by pressing the CTRL key, followed by a numeric code (00-99) and XMT. When the terminal is polled, the terminal responds with its normal heading, followed by STX, ESC, NUM, NUM, ETX, BCC. The two NUMs are the numeric code. The numeric control message is not displayed on the screen, and the significance of the numeric code is defined at the central processor.

DATA TRANSMISSION VARIABLE

The terminal has the capability of selectable start and stop positions for the transmission of data in both forms and non-forms modes. In forms mode:

a. Cursor to ETX or beginning of form to cursor, if no ETX (unprotected data only); standard for TD820, TD730, and TD830 operation.

b. Beginning of form to end of form (unprotected data only).

c. Total form when in forms and search mode.

d. Beginning of form to cursor position (unprotected data only); TD700 DL2 through DL4 and TD800 operation.

e. Variable tab field identifier (→) causes a skip of transmitted data in forms.

In non-forms mode:

a. Cursor to ETX or home to cursor, if there is no ETX; standard for TD820, TD730, and TD830 operations.

b. Cursor to ETX or end-of-screen, if there is not ETX.

c. Home to cursor; TD700 DL2 through DL4 and TD800 operation.

d. Home to cursor, or cursor to GS (Δ) or end-of-screen when GS is not used.

I/O Interfaces

Two primary interfaces exist to the MTS architecture: the Serial I/O Bus and Data Comm. The Serial I/O Bus is a shielded, 3-wire bus which supports priority interrupts and bit-serial, character-asynchronous communication with local devices. TSG/ASDO specification 28891141 defines the Serial I/O Bus.

The Data Comm Interface provides capabilities for three types of connections: RS232C, TDI, and BDI. These interfaces are defined in:

RS232C EIA Standard, Interface between Data Processing Terminal Equipment and Data Communication Equipment, August, 1969.

1700 3195 Specification, Two-wire Direct Interface, August 1967.

1498 5303 Specification, Burroughs Direct Interface

I/O Data transfer rates are shown in table 1-1.

Table 1-1. I/O Data Transfer Rate

Type of Interface	Characteristic
Asynchronous Data Set (EIA RS232C or CCITT)	150 to 1800 bps*
Synchronous Data Set (EIA RS232C or CCITT)	1200 to 9600 bps
Two-Wire Direct Interface (TDI) (Asynchronous)	150 to 9600 bps at 1000 feet
Burroughs Direct Interface (BDI) (Asynchronous)	150 to 38,400 bps and up to 15,000 feet (but not concurrently). Maximum of 20 terminals on a single multipoint BDI line.
Concatenation from a Single Asynchronous Data Set	Maximum of 1000 feet of concatenated cable between terminals.
Concatenation from a Single Synchronous Data Set	The maximum total concatenation cable length from first to last terminal is based on data rate, as follows: 9600 bps - 400 feet, 4800 bps - 800 feet, 2400 bps - 1600 feet, 2000 bps - 2000 feet, 1200 bps - 3200 feet, 600 bps - 6400 feet.

* Bits per second.

ASYNCHRONOUS DATA COMMUNICATION

Asynchronous (RS232, TDI, or BDI) data communication uses even parity. Each character is serially transmitted using 10 bits per character. The meaning of each bit of the character is, in order: a space bit, seven ASCII code bits with the least significant bit first, a parity bit, and a mark bit. When data are received or transmitted, the baud rate and baud timing sequence are produced by a baud rate counter in the terminal.

SYNCHRONOUS DATA COMMUNICATION

Synchronous data communication uses odd parity. Each character is serially transmitted using eight bits per character. The meaning of each bit of the character is, in order: seven ASCII code bits with the least significant bit first and a parity bit. When data are received or transmitted, the baud rate timing is received over separate timing lines from the communications interface. The SYN character is used to provide a signal on the line to establish and maintain synchronism between the terminal and the central processor. When a synchronous transmission is started, at least four SYN characters must be transmitted before any other character is transmitted, in order to enable synchronization.

The software controllable ESC functions given in table 1-2 consist of a two, three, four, or five character sequence which produces a specific function code. The first character of the function code is always the ESC character.

Table 1-2. Software Controllable ESC Functions

Character Sequence				Function
1	2	3	4	
ESC	Space	C		Display resident character set
ESC	Space	D		Initiate confidence test
ESC	Space	V		Display of firmware version
ESC	!			Character insert by line
ESC	"	COL	ROW	Program cursor position (see note 2)
ESC	#			Clear all variable tab stops
ESC	$	PAGE		Select page (see note 3)
ESC	%			Character delete by line
ESC	&			Align display cursor to data comm pointer
ESC	(			Transmit page
ESC	-	(Char)		Search character change (see note 6)
ESC	.			Set/reset variable tab stop
ESC	:			Print unprotected data
ESC	;			Print complete page
ESC	<			Line movement down
ESC	>			Line movement up
ESC	?			Sound audible alarm
ESC	@			Character insert by page
ESC	C			Space right
ESC	D			Set mobil home to data comm pointer
ESC	E			Search enable
ESC	F			Search enable
ESC	J			Clear to end of page
ESC	K			Clear to end of line

Table 1-2. Software Controllable ESC Functions (Cont.)

Character Sequence				Function
1	2	3	4	
ESC	L			Line insert
ESC	M			Line delete
ESC	N			Negative video "on"
ESC	O			Negative video "off"
ESC	P			Character delete by page
ESC	R			Configuration control
ESC	S			Roll up
ESC	T			Roll down
ESC	W			Forms enable
ESC	X			Forms disable
ESC	Y			Lockout lower case
ESC	Z			Lower case enable

NOTES

1. ESC - Used as a prefix in a control sequence from communication interface.

2. COL - Column = $(32)_2 + (n)_2$ where $0 \leq n \leq$ one less the number of characters per line.

   ROW - Row = $(32)_2 + (n)_2$ where $0 \leq n \leq 95$ (or less, dependent upon the memory option selected).

3. PAGE - PAGE = $(32)_2 + (n)_2$ where $1 \leq n \leq$ the maximum maximum number of pages of memory.

4. (Char) - Insert character for which a search is to be made.

REMOTE CONTROLLER INITIATED CONFIGURATION CHANGES

After the terminal has been installed and configured so that communication through data comm is possible, the terminal configuration can be changed from the remote controller through the use of escape (ESC) sequences.

NOTE

The ESC RA sequence is used to write data in ASCII code, and the ESC RH sequence is used to write data in hexadecimal code. When writing in ASCII code, bit eight is assumed to be a logic 0. Therefore, if bit eight has a literal significance, the data must be written in hexadecimal by using the ESC RH sequence.

The ESC sequences are described in the following paragraphs.

ESC R A (a) (b) (c)

The ESC R A (a), (b), and (c) sequence enables the data comm to enter data into any read/write memory area. The sequence is interpreted as follows:

a. The four character hexadecimal memory address used to identify the starting address at which the data comm will begin to write data.

b. The two character hexadecimal byte count used to identify the number of bytes of data contained in part (c) of the ESC sequence.

c. The ASCII data to be written into memory. This data may contain up to 255 characters.

ESC R H (a) (b) (c)

The ESC R H (a), (b), and (c) sequence enables the data comm to enter data into any read or write memory area. The sequence is interpreted as follows:

a. The four character, hexadecimal memory address used to identify the starting address at which the data comm begins to write data.

b. The two character, hexadecimal byte count used to identify the number of hexadecimal characters contained in part (c) of the ESC sequence.

c. The hexadecimal configuration data to be written into the memory. This data can contain up to 254 characters, which would load a maximum of 127 memory locations.

ESC R C

The ESC R C sequence causes the terminal to initiate a restart program and is used following an ESC R H sequence that contains configuration data changes. The ESC R C sequence allows the terminal to be operated using the changed data. Thus, the changed data may be checked for accuracy prior to transferring it to permanent storage.

NOTE

The ESC R P sequence should be preceded by the ESC R C sequence. However, it is not required.

ESC R P

The ESC R P sequence causes the terminal to perform the following operations:

a. Enter off-line mode.

b. Transfer the data (that was previously loaded by the ESC R A or ESC R H sequence) into the permanent (EAROM) storage.

c. Return the terminal to the on-line condition (local mode).

ESC R T H1 H2 H3 H4 C1 C2

The ESC R T sequence (receive and transmit) causes the terminal to go into transmit mode and send the contents of selected scratchpad memory areas to a user program through data comm. The starting address of the location to be read is given in hexadecimal by the four hex characters H1, H2, H3, and H4. The count of the number of bytes to be read is also in hexadecimal and is given by the two hex characters C1 and C2. The data read is converted into two ASCII characters per byte which represent the hexadecimal contents of that byte. Thus, the information is received by the program as two EBCDIC hexadecimal characters per byte.

ESC R S C1 C2 D1 D2 . . . Dn-1 Dn

While not used for configuration changes, the ESC RS sequence (Write Status Line) does write ASCII characters into memory at the address of the status line, so it is included in this section. It behaves exactly as would an ESC RA sequence, except that the address is determined to be that of the status line, and the length is limited to a maximum of 56 characters. Writing to the status line is a very convenient way to display a short message without affecting the rest of the screen. The first 16 locations of the status line are used for the "Receiving" message. An ESC RS message starts in column 17. All other locations remain unaltered until another ESC RS sequence is issued or the LOCAL key is pressed.

NOTE

An ESC RS sequence with a count of zero erases all 56 characters of the message on the status line.

Local Input

The local input is from the keyboard.

KEYBOARD SUBSYSTEM

The B 9348 contains a keyboard assembly which provides for the manual entry of data to the display subsystem. The data entered through the keyboard are stored in the display subsystem memory circuits and then displayed. The keyboard subsystem functionally consists of the keyboard and the keyboard interface circuit.

Keyboard

Each key on the keyboard contains a magnetically-triggered key amplifier. When a key is depressed, a small permanent magnet is lowered into the key amplifier, resulting in the production of a signal. The key signal is applied to an encoder circuit which produces a nine-bit code representing that particular key. The first six bits of the code are configured the same as those presented on the ASCII code chart. However, bits 7, 8, and 9 may be coded with all zeros to indicate an alphanumeric from columns 2, 3, 4, or 5; bits 7, 8, and 9 may be configured to something other than all zeros to indicate a function or an alphanumeric from column 0, 1, 6, or 7. In addition to the encoded outputs, the keyboard produces a strobe signal and two non-coded function lines (Insert and Reverse Tab). The keyboard characteristics are given in table 1-3.

Table 1-3. Keyboard Characteristics

Feature	Characteristic
Keystroke	0.2 inches (approximate) (5.08 mm)
Keypressure:	
Alphanumeric and function keys	3 ounces (approximate) (85.2 grams)
Mode control keys	9 ounces (approximate) (255.6 grams)
Output levels:	
Logic 0	+2.6 to 5.0 volts
Logic 1	0 to 0.45 volts
Two key rollover	Two key rollover maintains the data code produced when the first key is depressed and a second key is depressed before the first key is released. When the first key is released, the data code produced by the second key is applied as the output. During any multi-key action, the strobe output is a logic 0.
Shift key	Electronic, non-locking
Shift lock	Mechanical alternate action: Locks shift key in shift position.
Keyboard security lock (where applicable)	Locks keyboard in receive or local mode only. Inhibits unauthorized use of keyboard by disabling the MOS encoder outputs.

KEYBOARD CONFIGURATIONS

Two basic keyboard configurations are available: the typewriter keyboard and the data preparation keyboard. The keyboard is connected to the basic system by means of a cable. Various keyboards are available which satisfy nationalistic requirements.

U. S. Typewriter Keyboards

The keyboard resembles a typewriter keyboard. It is designed to simplify in entering alphanumeric data. Figure 1-3 shows the U. S. typewriter keyboard layout. The function keys, control keys, and indicators of this keyboard are described later in this section.

Data Preparation Keyboards

The keyboard resembles a keypunch keyboard in the placement of numerals (see figure 1-4 for the layout). This keyboard is designed for ease in entering both alphanumeric and numeric data. Numeric date may be entered in both shifted and unshifted condition. The function keys, control keys, and indicators on this keyboard are described later in this section. The data preparation keyboard is recommended for a data entry installation.

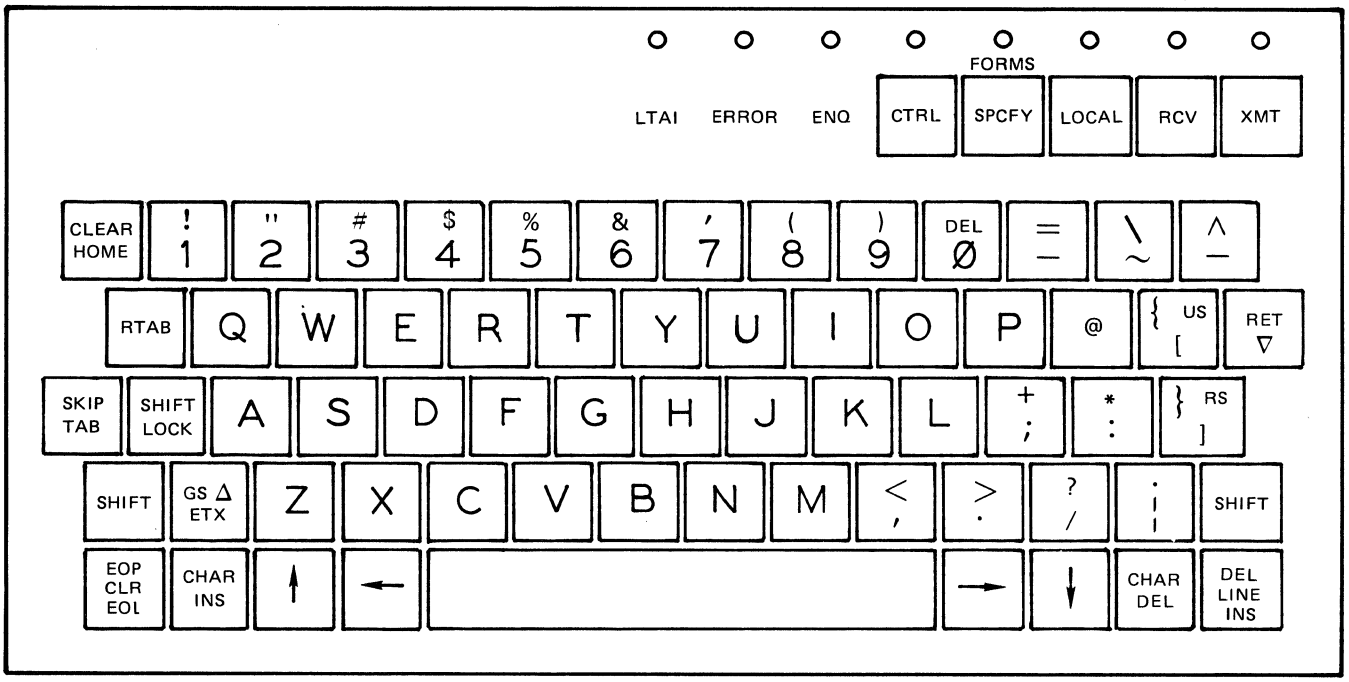

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Figure 1-3. U. S. Typewriter Keyboard, ASCIII

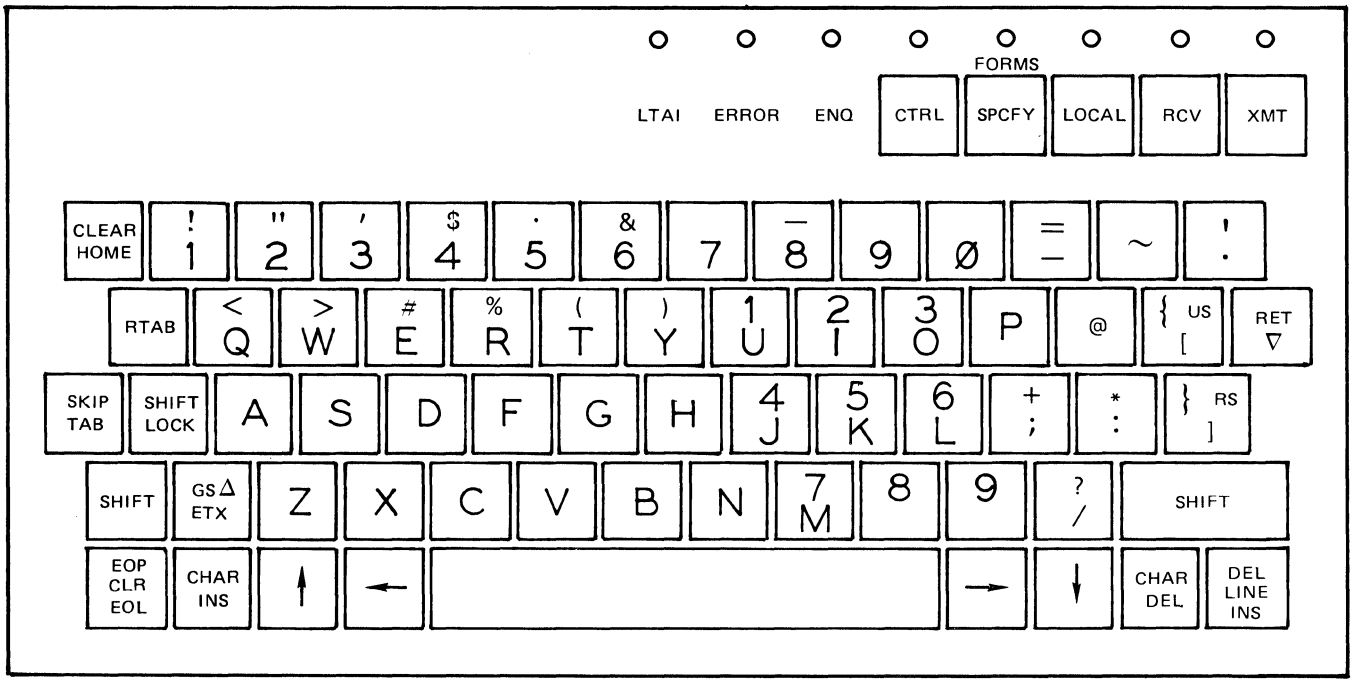

Figure 1-4. Data Preparation Keyboard

Local Output

The local output on these systems is available to the screen.

DISPLAY SUBSYSTEM

The display subsystem can be divided into two function sections: the display monitor section and the display logic section. The display monitor section contains a cathode ray tube (CRT) and all of the solid-state electronics (video amplifier, sync amplifiers, high voltage rectifier, and deflection circuits) needed to generate a television-type display. The display logic section provides (a) the horizontal and vertical timing, and (b) the character generator dot pattern needed to operate the display monitor section. The display characteristics are given in table 1-4.

Table 1-4. Display Characteristics

Feature	Characteristics
CRT Dimensions:	
Diagonal Size	12 inches (305 mm)
Overall Size	74 square inches
CRT Viewing Area:	
Width	8.4 inches (210 mm)
Height	6.3 inches (158.5 mm)
Display Format	Fully formed grey scale characters
Line Length	40/80 characters
Display Character Capacity	1920 Maximum + 80 character status line
Lines (Working Field)	24 Maximum
Lines (Status Line)	1 (25th display screen line)
Character Size:	
Width	0.09 inches (Double for 40 character line length)
Height	0.132 inches (3.30 mm)
Row Spacing	3 blank rows of dots between successive rows
Refresh Rate	Input line frequency (50 Hz to 60 Hz)
Flicker	None observable
CRT Brightness	20 foot Lamberts (maximum)
Contrast Ratio	12 db Min.
Color of Displayed Image	White characters on a black background (normal video)
Viewing angle	100° (minimum)
Deflection	Magnetic
Focus	Electrostatic
X-Ray Radiation	0.5 milliroentgens per hour (maximum)
	No emissions detected above .1 mr/hr

During multiple page operation, this system is able to separate the data communications pointer from the display cursor, thereby allowing keyboard data to be entered on one page and external data (data comm or peripheral) to be entered on, or transmitted from, another. This capability greatly increases efficiency; the operator no longer needs to wait for the display to be serviced by the central system. After the XMT key has been pressed, the operator may immediately advance to the next page and start entering data.

Data verification messages may also be transmitted back while the operator is entering new information. For example, assume that data have been entered on page 1 and transmitted. The operator advances to page 2 and enters data. When the central system completes processing the page 1 information, it responds to page 1 without interrupting local operation roles, etc. Thus, the operator is able to enter data continuously. When selective print of messages is required, the operator can initiate a print function and proceed to enter data on the next page while the system is printing the previous page on an auxiliary printer.

This system allows the user to divide the terminal display memory into one or more pages. The user selects the page size by means of program control. Each page consists of a minimum of four lines of display memory and can be extended up to the limits of the display memory in 4-line increments (refer to table 1-5).

The system performs most edit and format functions on a screen basis. The scroll and tabulation functions are on a system basis. Data highlighting operates on a line-by-line basis, thereby allowing varied data configurations on different screens.

Table 1-5. Page/Screen/Display Memory Relation

Page	Screen			Display Memory			
				Basic		Expanded	
Lines per Page	Lines per Screen	Char. per Line	Pages Displayed	Pages	Usable Char.	Pages	Usable Char.
4	12	40	3	12	1920	25	4000
8	12	40	1½	6	1920	12	3840
12	12	40	1	4	1920	8	3840
4	12	80	3	6	1920	12	3840
8	12	80	1½	3	1920	6	3840
12	12	80	1	2	1920	4	3840
24	12	80	½	1	1920	2	3840
4	24	40	6	12	1920	25	4000
8	24	40	3	6	1920	12	3840
12	24	40	2	4	1920	8	3840
16	24	40	1½	3	1920	6	3840
20	24	40	1¼	2	1600	5	4000
24	24	40	1	2	1920	4	3840
4	24	80	6	6	1920	12	3840
8	24	80	3	3	1920	6	3840
12	24	80	2	2	1920	4	3840
16	24	80	1	1	1280	3	3840
20	24	80	1	1	1600	2	3200
24	24	80	1	1	1920	2	3840

Operator Controls and Functions

The B 9348 terminal can be operated in any of three basic modes: the local (LOCAL) mode, which is used to enter information from the keyboard; the transmit (XMT) mode, which is used to transmit information from the terminal; and the receive (RCV) mode, which is used to receive information from the central processor. While the terminal is in the local mode, the operator can generate CTRL sequences which are used to manipulate data in the terminal, thereby causing temporary changes in the terminal configuration.

The ON-OFF switch and BRIGHTNESS control are located on the front bezel below the CRT. All of the function keys are located on the keyboard. A list of all of the operating controls and indicators and their respective operating functions follows.

ON-OFF Switch

The ON-OFF switch provides the control for activating the terminal with ac-line voltage.

BRIGHTNESS Control

The BRIGHTNESS control is used to adjust the display intensity for optimum viewing level.

XMT Mode Key and Indicator

When the XMT key is pressed, the terminal is set to the transmit mode of operation, and all keyboard keys except LOCAL are disabled. Pressing the XMT key aligns the data comm pointer to the display cursor position. The transmit (XMT) mode indicator is illuminated when the transmit (XMT) key is pressed. The indicator is extinguished when a transmission from the terminal has been positively acknowledged by the receiving station, or when the terminal is changed to the local mode by the operator.

RCV Mode Key and Indicator

The receive (RCV) mode indicator, which indicates that the terminal is ready to receive data, is illuminated when the receive (RCV) key is pressed. The indicator is also illuminated when a transmission from the terminal has been successfully completed. The RCV indicator is extinguished when the terminal is switched to local mode or transmit mode. Pressing the RCV key aligns the data comm pointer with the cursor position.

LOCAL Mode Key and Indicator

The local mode indicator is illuminated when the LOCAL key is pressed or, by the use of the keyboard when the terminal is in the receive mode with no data being received into the terminal. It is also illuminated following the successful completion of received message, if that received message did not contain the DC1 mode-control character. The indicator is extinguished when the terminal is switched to the receive mode or transmit mode.

SPCFY Key

The specify (SPCFY) key is used to initiate the transmission of a cursor position message. When the SPCFY key is pressed, the current cursor location is stored. Then, when the terminal is polled, the terminal automatically responds with its normal heading, followed by STX, ESC, ", a character, a character, ETX, BCC. The first character represents the cursor column position, and the second character represents the cursor row position.

CTRL Key and Indicator

The control (CTRL) key is used to initiate a software control function from the keyboard (see table 1-6). In the shifted mode, pressing the CTRL key locks the system in the control mode, until the CTRL key is pressed in the unshifted mode. The CTRL indicator is illuminated upon activation of the CTRL key, and remains illuminated until the control sequence is completed.

ERROR Indicator

The error indicator is illuminated when a parity error or block check error is detected by the terminal in the data being received, or when buffer overflow is caused by the receipt of more characters than the display memory capacity. The error indicator is extinguished by the successful retransmission to the terminal, the receipt of a new message, or by pressing the LOCAL key.

ENQ Indicator

The enquiry (ENQ) indicator is illuminated when the terminal detects the central processor (CP) attempting to transmit a message to the terminal while the terminal is not in the receive mode. The indicator is extinguished by the operator placing the terminal in the receive or local mode. Also, the audible alarm momentarily sounds when the ENQ indicator is illuminated.

FORMS Indicator

The FORMS indicator is illuminated when the terminal is operating in the forms mode. The terminal is placed in the forms mode either by the receipt of the proper ESC control code from the CP, or by CTRL control code from the keyboard and having at least one leading delimiter in the displayable text. The FORMS indicator is extinquished either by the receipt of a CP message with no ESC control code, with ESC control code, for cancelling forms, or by CTRL control code from the keyboard for cancelling forms.

LTAI Indicator

The line terminal activity indicator (LTAI) is illuminated when data is transmitted from the CP to any terminal on the line. When the addressed terminal responds to the CP, the LTAI indicator is extinguished. In normal operation, the LTAI blinks due to the data line activity. A LTAI which is not illuminated indicates that the CP is not transmitting on that line. A LTAI which remains illuminated indicates that the addressed terminal is not responding.

Table 1-6. Software Control (CTRL) Sequences

Character Sequence					Function
1	2	3	4	5	
CTRL	Space	C	CTRL		Display resident character set
CTRL	Space	D	CTRL		Initiate confidence test
CTRL	Space	E	CTRL		Initiate perpetual RAM test
CTRL	Space	F	CTRL		Initiate printer test
CTRL	Space	G	CTRL		Initiate cassette test
CTRL	Space	H	CTRL		Set data rate to 600 bps
CTRL	Space	J	CTRL		Set data rate to 1200 bps
CTRL	Space	K	CTRL		If asynchronous data interface, sets data rate to 1800 bps. If synchronous data interface, sets data rate to 2400 bps.
CTRL	Space	M	CTRL		Memory saturation test
CTRL	Space	V	CTRL		Display of firmware version
CTRL	N_1	N_2			Numeric control message (see note 3)
CTRL	<	COL	ROW		Program cursor position (see note 2)
CTRL	>				Align display cursor to data comm pointer
CTRL	?				Sound audible alarm
CTRL	@				Transmit page
CTRL	A				Search enable
CTRL	B				Line movement down
CTRL	E	(Char)			Search character change (see note 4)
CTRL	H	(Char)			Control character keyboard entry
CTRL	I				Negative video "off"
CTRL	M				Roll line down
CTRL	N				Roll line up
CTRL	O				Clear all variable tab stops
CTRL	P				Set/reset variable tab stop
CTRL	Q				Forms disable

Table 1-6. Software Control CTRL Sequences (Cont.)

Character Sequence					Function
1	2	3	4	5	
CTRL	R				Configuration control
CTRL	S				Search disable
CTRL	T				Enable lower case
CTRL	U				Negative video "on"
CTRL	V				Line movement up
CTRL	W				Forms enable
CTRL	Y				Lockout lower case
CTRL	↑				Scroll up
CTRL	↓				Scroll down
CTRL	→				Page advance
CTRL	←				Page back

NOTES

1. CTRL - Used as a prefix in a control sequence from the keyboard.
2. COL - Column = $(32)_2 + (n)_2$ where $0 \leq n \leq$ one less than the number of characters per line.

   ROW - Row = $(32)_2 + (n)_2$ where $0 \leq n \leq 95$ (or less, dependent upon the memory option selected).
3. N_1, N_2 - Numeric control messages range from 00 to 99.
4. (Char) - Insert character for which a search is to be made.

Keyboard Function Keys:

Line Feed. Line feed is used to move the cursor one line down. When the cursor is in the bottom line, pressing the line feed key causes the cursor to reappear in the top line.

Reverse Line Feed. Reverse line feed is used to move the cursor one line up. When the cursor is in the top line, pressing the reverse line feed key causes the cursor to reappear in the bottom line.

Backspace. Backspace is used to move the cursor one character to the left. When the cursor is in the first character position (left edge) of the display, pressing the backspace key causes the cursor to reappear in the last character position (right edge) of the next higher line. When the cursor is in the "home" position (top line, left edge), pressing the backspace key causes the cursor to reappear in the last character position (bottom line, right edge).

Forward Space. Forward space key is used to move the cursor one character position to the right. If the cursor is at the right edge of a line, pressing the forward space key causes the cursor to reappear at the left edge, down shifted one line. If the cursor is located in the last character position of the bottom line, pressing the forward space key causes the cursor to reappear in the home position.

CLEAR/HOME

The shifted CLEAR/HOME key activates the clear function. CLEAR erases all data on the page and moves the cursor to the home position. In the forms mode, CLEAR erases the unprotected data only and moves the cursor to the first position of the first unprotected data field on the page. The central system program FF control character causes both HOME and CLEAR functions. If Burroughs enables the CLEAR key option, the CLEAR key clears the entire page in forms mode.

The unshifted CLEAR/HOME key activates the home function. Pressing the CLEAR/HOME key causes the cursor to be moved to the left-most position on the top line of the page (home position). In the forms mode, HOME moves the cursor to the first position of the first unprotected data field. The central system program OC4 control character also performs the home function.

Return (RET)

RETURN moves the cursor from any position in a line to the first position of the next line. If the cursor is in the last line, RETURN moves it to home position. This terminal can write the CR character symbol (∇) into memory and on the screen. The system option of not writing the CR symbol (Δ) into memory can be installed. The central system program CR control character duplicates the return function.

Skip/Tab (TAB)

The TAB key causes the cursor to move forward to the next fixed or variable tab stop location. If the fixed tab option is installed, fixed tab stops are located at positions 1, 9, 17, 25, 33, 41, 49, 57, 65 and 73 of each line. If the variable stop option is installed, the variable tab stop can be set at any position on the display line.

In the forms mode, tab stops (fixed or variable) are ignored, and TAB causes the cursor to move forward to the first character location of the next unprotected field. If the field identifier option is programmatically configured, the TAB key causes a field identifier character (→) to be written into memory and on the screen.

SKIP

SKIP is the shifted TAB key. With the variable tab feature enabled, pressing the SKIP key alternately sets or resets the tab stop at the cursor location. With search mode enabled, the SKIP key causes a skip to the next unprotected data field, error or assigned search character. The SKIP function is not duplicated by program control.

RTAB (Reverse Tab)

In non-forms, the RTAB key causes a reverse tab function to the tab stop preceding the present cursor position. In forms, the RTAB key causes a reverse tab function to the preceding unprotected data field. The RTAB key operates with either fixed or variable tab stops.

EOP CLR (Clear to End of Page)

The shifted EOP key causes the clearing of all data (or unprotected data in forms) from the cursor position to the end of the page.

EOL CLR (Clear to End of Line)

In non-forms, the EOL key causes the clearing of all data from the cursor position to the end of the line. In forms, the EOL key causes the clearing of all data from the cursor position to the next RS or GS character.

DEL LINE (Delete Line)

The shifted DEL LINE key causes the erasure of the line in which the cursor is positioned, and all data in the lines below is moved up one line. This function is inhibited in forms.

INS LINE (Insert Line)

The unshifted INS LINE key causes all data in the lines below, and all data in the line in which the cursor is positioned to be moved down one line. Any data in the bottom line is lost. This function is inhibited in forms.

GS (Δ) (Group Separator)

The shifted GS key causes the GS symbol (Δ) to be written into memory at the cursor position. With forms mode enabled, this symbol is interpreted as the leading delimiter of a right justified field.

ETX (X) (End-of-Text)

The ETX key causes the ETX symbol (X) to be written into memory at the cursor position, and the cursor is then automatically moved to the home position. This symbol is interpreted as the end-of-text character.

US (▷) (Leading (Left) Delimiter)

With the forms mode enabled, the US key causes the symbol (▷) to be written into memory at the cursor position. This symbol is interpreted as the leading delimiter of an unprotected data field.

RS (◁) (Trailing (Right) Delimiter)

With the forms mode enabled, the RS key causes the symbol (◁) to be written into memory at the cursor position. This symbol is interpreted as the trailing delimiter of an unprotected data field.

CHAR INS (Character Insert)

When the CHAR INS key is pressed, the terminal is placed in a character insert mode. While in the character insert mode, pressing an alphanumeric key (including space) causes the alphanumeric character to be inserted at the cursor location. The succeeding characters within the line are moved one space to the right. Surplus characters, if any, are shifted off the end of the line and lost. Pressing the CTRL key prior to pressing the CHAR INS key causes the succeeding characters on the page to be shifted one space to the right and down line to line.

When in the forms mode, the succeeding character shift that takes place during an insert function is limited to the unprotected data field in which the cursor is located.

CHAR DEL (Character Delete)

The CHAR DEL key is used to remove a displayed character from the cursor location. When the CHAR DEL key is pressed, the succeeding characters within the line (or unprotected data field

in forms) are moved one space to the left. Pressing the CTRL key prior to pressing the CHAR DEL key causes the succeeding characters on the page to be shifted one space to the left and up line to line.

KEYBOARD SECURITY LOCKS

A security lock is optionally provided with each keyboard (figure 1-5). The security lock electrically inhibits unauthorized use of the keyboard by disabling the keyboard encoder outputs. The security lock consists of a tumbler lock with a removable key, and is located on the right side of the keyboard assembly. The keyboard can only be locked in the Receive or Local modes.

Operator Cleaning Procedures

Cleaning of the terminal should be done as needed, depending on environmental conditions at the terminal location.

NOTE

To prevent any shock hazard while cleaning, the terminal must be turned off and the a.c.-power cord must be removed from the wall receptacle.

Vacuum the air vent screens at the top and bottom of the display cabinet.

CAUTION

Do not use ammonia type window cleaners, as this discolors the plastic lens on the face of the CRT.

Use a damp cloth and mild soap to clean the face of the CRT and the top of the keyboard. Ensure that the keyboard is completely dry before applying power to the terminal.

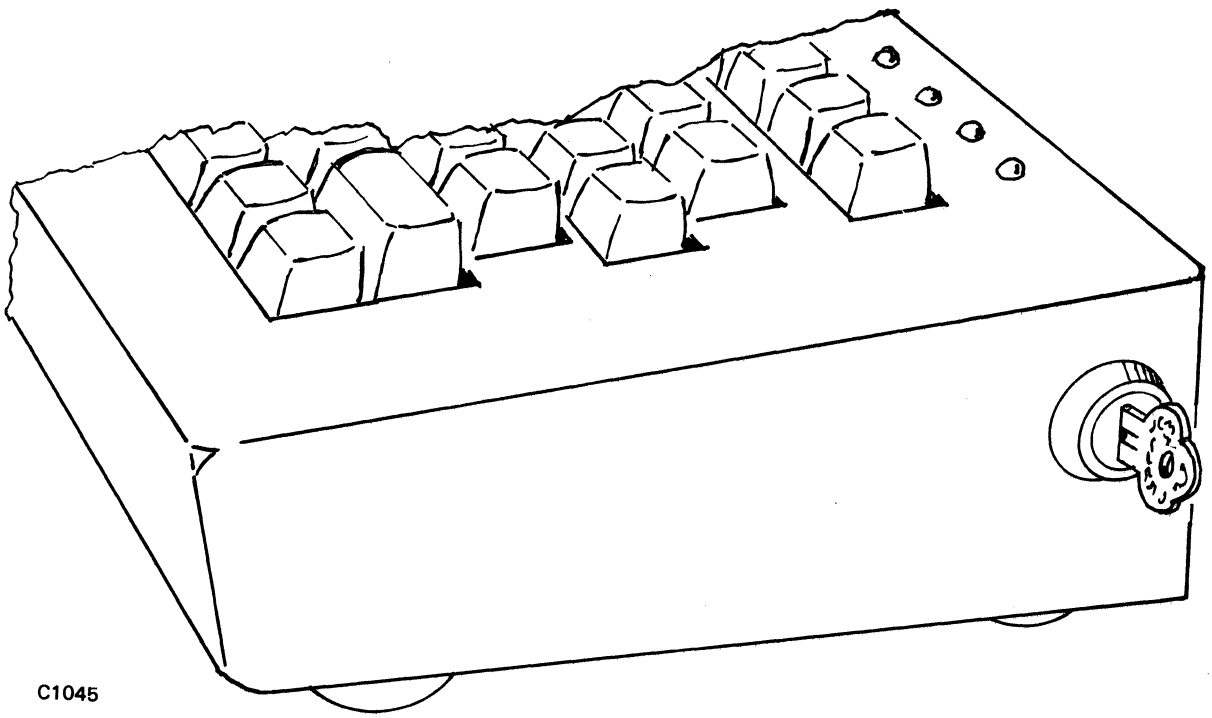

Figure 1-5. Keyboard Security Lock

Character Sets and Codes

A number of character sets and codes are available with the B 9348 (and which correspond to those available on the TD830). Figure 1-6 shows the U.S. ASCII chart; figure 1-7 shows the Modified U.S. ASCII chart. Figure 1-9 shows the code and graphic substitutions made for the various international character sets available.

b_7 b_6 b_5 →						0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
BITS	b_4	b_3	b_2	b_1	COLUMN → / ROW ↓	0	1	2	3	4	5	6	7
	0	0	0	0	0	NUL	DLE	SP	0	@	P	`	P/POL
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q/SEL
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s/FSL
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t/BSL
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL *	ETB	'	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	11	VT	ESC	+	;	K	[	k	{
	1	1	0	0	12	FF	FS	,	<	L	\	l	¦
	1	1	0	1	13	CR	GS	-	=	M	]	m	}
	1	1	1	0	14	SO	RS	.	>	N	^	n	~
	1	1	1	1	15	SI	US	/	?	O	—	o	DEL

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Figure 1-6. B 9348 U.S. ASCII Chart

ROW \ COLUMN →	2	3	4	5
0	SP	0	@	P
1	!	1	A	Q
2	"	2	B	R
3	#	3	C	S
4	$	4	D	T
5	%	5	E	U
6	&	6	F	V
7	'	7	G	W
8	(	8	H	X
9	)	9	I	Y
10	*	:	J	Z
11	+	;	K	[
12	,	<	L	—
13	—	=	M	]
14	.	>	N	}
15	/	?	O	{

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Figure 1-7. Modified U.S. ASCII Chart

COUNTRY GROUP	COL. 2, ROW 3	COL. 2, ROW 4	COL. 4, ROW 0	COL. 5, ROW 11	COL. 5, ROW 12	COL. 5, ROW 13	COL. 2, ROW 1
FRANCE/BELGIUM		FR			\		
ITALY					£		
SPAIN/LATIN AMER.	Ps				~N		
UNITED KINGDOM	£				\		
GER./AUS./SWITZ.			§	Ä	Ö	Ü	
PORTUGAL/BRAZIL				~O	~A	Ç	
SOUTH AFRICA				'N	^E	Ö	
SWEDEN/FINLAND	£		'E	¨A	Ö	Å	
NORWAY/DENMARK	Æ	Å	Ø		Ü		¦

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Figure 1-8. International Character Sets

SECTION 2
INSTALLATION

SITE REQUIREMENTS

The B 9348 Input and Display System is designed for desk top operation, although the unit can be console mounted. When unit is console mounted, refer to console assembly special instructions. The B 9348 measures approximately 15 inches in height, 17 inches in width, and 20 inches in depth (including keyboard). However, the keyboard can be positioned up to six feet from the display unit. The MTS-1 hardware requires 75 watts of either 115 or 230 volts of single phase a.c. power. The MTS-1 is fan-cooled, using ambient air.

The MTS-1 requires the following minimum clearances:

	Sides	Rear	Front	Top
Operating:	12" (30.5 cm)	12" (30.5 cm)	36" (91.4 cm)	36" (91.4 cm)
Maintenance:	36" (91.4 cm)	36" (91.4 cm)	36" (91.4 cm)	36" (92.4 cm)

The power requirements are: 100-127 Volts, a.c., 50/60 Hertz and 200-240 Volts, a.c., 50/60 Hertz.

UNPACKING

1. Unpack and install four rubber feet on the bottom of the unit.
2. Install the plastic face cover.

MTS-1 UNIT PREPARATION PROCEDURES

The unit preparation procedures are discussed in the following paragraphs.

Power Supply Setup

1. Verify that the correct power supply is installed while the unit is unplugged.
2. Remove the outer case and the back plate.
3. Install power supply.
    a. For 110 volts a.c., install power supply 2889 1158.
        (1) Install a 3A 125 volt fuse (part no. 1325 8557).
    b. For 220 volts a.c., install power supply 2889 1238.
        (1) Install a 1.5A 250 volt fuse (part no. to be supplied).
        (2) Install a dropping resistor for the fan.

50/60 Cycle Operation

Depending upon whether the terminal is to be used with 60 cycle or 50 cycle power the following must be considered:

VIDEO BOARD PART NUMBER 2889 1349

For 60 cycle operation make sure that pin 23 on the microprocessor, EF_2, is connected to 0 volts. For 50 cycle operation, lift pin 23 on the microprocessor, EF_2 and solder wire to pin 23 and connect to +5 volts.

VIDEO BOARD PART NUMBER 2889 2453

For 50 cycle operation, cut out the Zero ohm resistor by the microprocessor (see figure 2-1).

RS232, TDI, BDI Configuration

The configurations of RS232, TDI, and BDI are performed as outlined in the following paragraphs.

SIO BOARDS PART NUMBERS 2889 1257 AND 2889 1265

The following listed configurations remove jumpers as required (see figure 2-2):

1. RS232: remove jumpers S100, S101, S104, S106, S107.
2. BDI: remove jumpers S101, S102, S103, S105, S107.
3. TDI: remove jumpers S100, S102, S103, S104, S105, S106.

NOTE

To change from RS232 to BDI or TDI, make the jumper change as shown in figure 2-3.

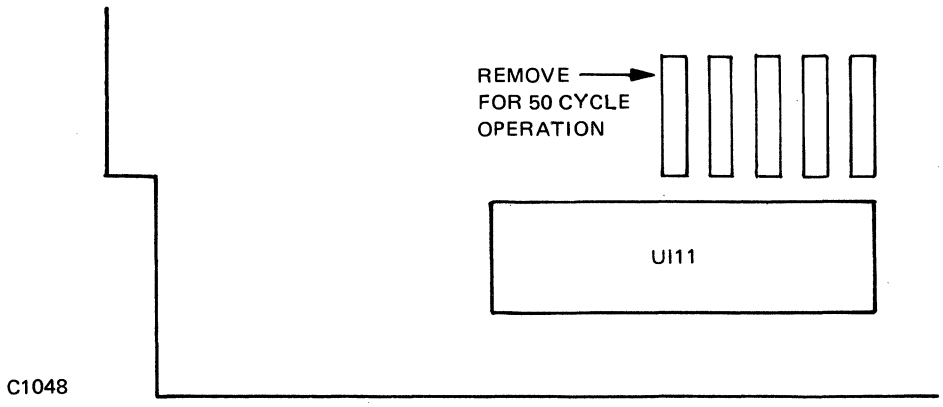


Figure 2-1. Video Board Jumper Location 50/60 Cycle Operation

Set switches as follows (see figure 2-2):

1. RS232: set SW3, SW4, SW6, SW9 to ON; set all others to OFF.
2. BDI: set SW1, SW5 and SW7 to ON; set all others to OFF.
3. TDI: set SW2 and SW8 to ON; set all others to OFF.

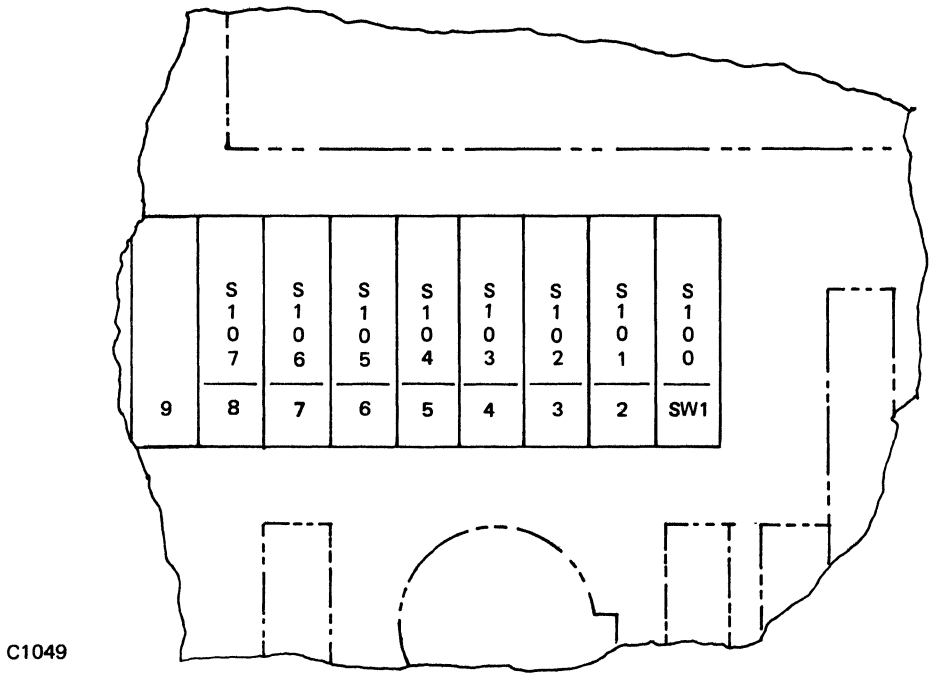


Figure 2-2. View of Jumper Area from Serial I/O

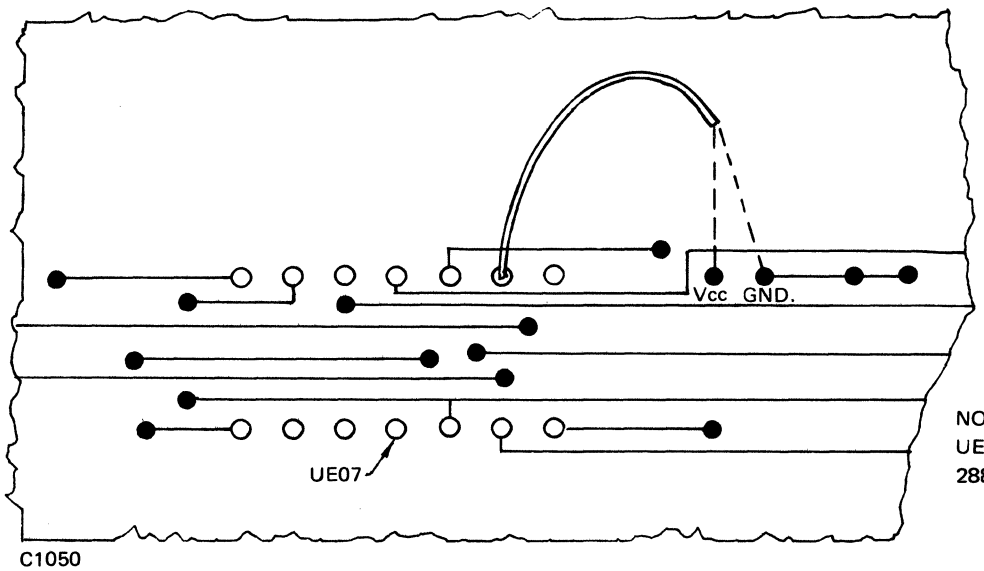


Figure 2-3. View of UE07 Area

Keyboard Setup Without Numeric Keypad Option

If the keyboard cable is packed separately from the keyboard unit, perform the following procedural steps:

1. Remove the bottom cover of keyboard unit and slide J1 end of cable WS through the entrance hole in bottom cover.
2. Install cable and cable clamp as shown in figure 2-4.
3. Replace bottom cover.

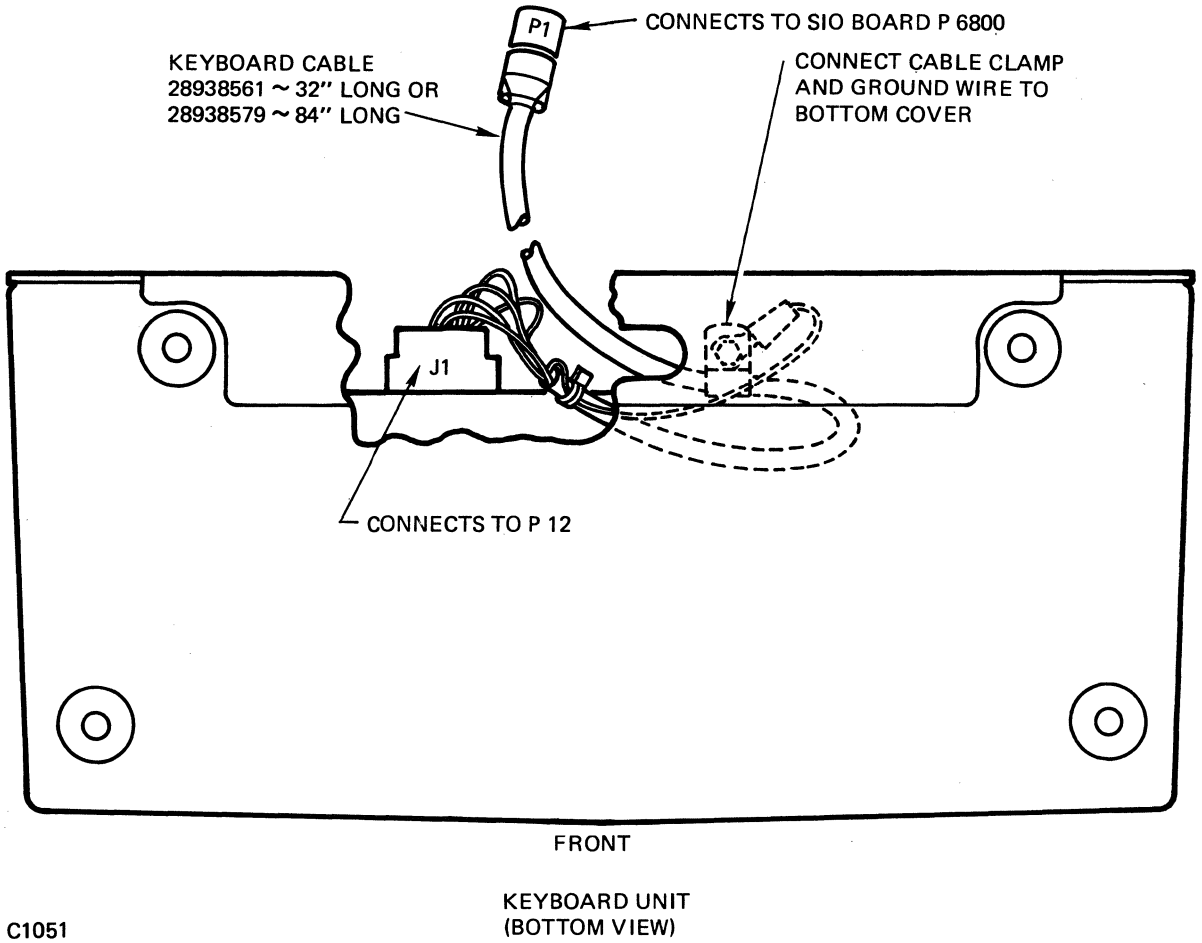


Figure 2-4. Keyboard Without Numeric Keypad Option

Cable Connections and Cable Requirements

1. Connect cables from keyboard, data comm, and peripherals as indicated in figure 2-5.

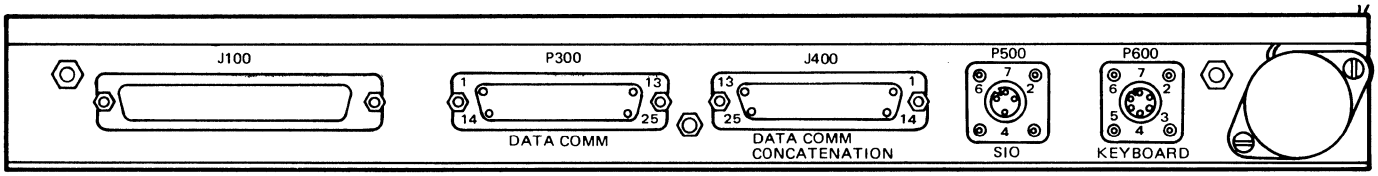


Figure 2-5. Cable Connector Plate

Table 2-1 is a list of possible cables that can be required for the installation of a MTS-1 based terminal.

Table 2-1. Cable Requirements

Cable for:	Description	Style	Number
Keyboard to Control	6 ft cable w/connectors	TD041-5	2893 8579
Control to Modem/ Modem Expander	15 ft cable w/connectors	XC002	1696 4975
	25 ft cable w/connectors	XC003	1696 4983
	50 ft cable w/connectors	XC004	1696 4991
	100 ft cable w/connectors	XC005	1696 2946
TD to TD076	10 ft cable w/connectors	TD111	2555 6895

INSTALLATION OF BASIC FEATURES AND OPTIONS

After all of the cables have been connected, plug in the a.c. power cord and apply power. During the power-on sequence, a confidence test is automatically performed in the terminal. If the confidence test is successfully performed, a message of asterisks (******) is displayed. If the confidence test is not successful, an error message is displayed (refer to Section 4, "Maintenance"). After the confidence test is successfully performed, check the terminal configuration and make configuration changes, as required.

Terminal Configuration Changes

During manufacture, a standard terminal configuration sequence is loaded into the permanent storage (EAROM). When the B 9348 is installed and power is turned on, a copy of the terminal configuration sequence is automatically transferred from the EAROM into scratchpad memory. Since the operating requirements at each installation site are different, some changes have to be made to the basic terminal configuration. The keyboard control sequences shown in the following paragraphs are used to make changes to the terminal configuration sequence.

The consistency of the configuration is automatically checked. If an inconsistency in the configuration is detected, an error message is displayed (refer to the passage on error messages, and table 2-3). If any inconsistency is detected, the following configuration is automatically set at the time the message is displayed:

80 characters per line

24 lines per screen

24 lines per page

1920 character, display store size

1 page

24 lines total

user store length - display store size is the data comm buffer size

CTRL

The CTRL RWMODE (entered by pressing first the control key, then the shifted R, W, M, O, D and E keys) causes the terminal to enter an off-line mode of operation (non-responsive to datacom), clear the display memory, and print " > " at the home position. Internally, the logic for making configuration changes is initialized. This sequence must always be used first before any changes to or display of configuration data in scratchpad memory can be done.

NOTE

"MODE" are the four characters which, by default, must be entered after CTRL RW in order to get into configuration mode, but these can be altered to be any four desired characters by changing the four characters stored at locations 0108-010B. This form of password protection is intended to increase the security of configuration parameters.

While in configuration mode, avoid pressing the LOCAL key or making a mistake in entering any of the subsequent CTRL R sequences; doing so causes the terminal to exit from this mode immediately. Then it would be necessary to start over from the top with CTRL RWMODE again. One very common mistake of this kind is failure to use shifted CTRL R sequences.

CTRL R H H1 H2 H3 H4

The CTRL RH sequence, followed by the four-character hexadecimal scratchpad memory address (H1, H2, H3, and H4), causes the terminal to display a 32-character hexadecimal message, which represents 16 sequential bytes of stored data starting at the selected memory address.

CTRL R A H1 H2 H3 H4

The CTRL RA sequence, followed by the four-character hexadecimal scratchpad memory address (H1, H2, H3, and H4) causes the terminal to display a 16-character ASCII message, which represents 16 sequential bytes of stored data starting at the selected memory address.

NOTE

In locations where the high-order bit of the byte displayed is a logic "1", the ASCII character displayed represents a count that is 128 less than the actual value of that byte.

An example of the kind of display which would be seen after entering first CTRL RWMODE and then CTRL RH 0080 follows:

```
0080  /  0A  A1  01  00  17  4F  7B  7D
         10  36  38  6F  08  00  30  30
```

If instead of CTRL RH, one had entered the sequence CTRL RA 0110, the display would be in ASCII rather than in hexadecimal, and might look like the following:

0110 / DATA COMM ERROR

The latter is just one of several stored messages which are part of the configuration data and which are displayed on the terminal's status line when an error is encountered (these will be discussed in detail later).

Once information is displayed on the screen as a result of either a CTRL RH or CTRL RA sequence, it may then be changed if desired. The changes are entered by first typing over the displayed characters which are to be changed with the new characters desired for that configuration location. Edit functions

such as character or line insert or delete are not to be used, since the terminal expects the new information to be in the same screen positions as the original configuration data. Normal cursor movement and home functions can be used, however. Once the display is updated to reflect the new configuration desired, the actual change is made by using the next keyboard sequence shown in the following paragraphs.

CTRL R C X X X X

The CTRL RC sequence causes the terminal to write the updated display information back into scratchpad memory (not EAROM) at the displayed address from which the information was originally obtained. No address is needed with the CTRL RC sequence, but it is REQUIRED that four, shifted Xs be entered in the place of the four address characters. Thus, the four Xs mean that any four characters can be used. The terminal displays a "check" in the lower-left corner of the screen to confirm that the information actually was rewritten.

The information written back is obviously in the same format as the information originally shown (that is, either one ASCII character per byte or two hexadecimal characters per byte). If the high-order bit (parity bit 8) of the configuration location to be changed has any significance, the displayed message and the edit change should be done in hexadecimal and not in ASCII (that is, use CTRL RH for those cases).

The changes made with the CTRL RC sequence are applied only to the copy of the configuration data in the scratchpad memory and not to the permanent data in the EAROM. In many cases this is desirable, as a change may be only wanted for a very short time. However, any changes made only to scratchpad memory are destroyed when the terminal is powered off. The following sequence is therefore to be used if the changes are to be retained permanently.

CTRL R P X X X X

The CTRLRP sequence causes the terminal to write the updated configuration data (in its scratchpad memory) back into the EAROM for permanent storage. In addition, this sequence initiates an automatic confidence test to check the validity of the new configuration data and cancels the configuration mode, thus bringing the terminal back on-line and making it once again responsive to datacom operations. CTRL RC must be used prior to this sequence or there will be no updated information in scratchpad to be written back to EAROM. When CTRL RP XXXX is entered, the terminal displays a "P" in the lower-left corner of the screen to indicate that the update of the EAROM is in progress. For the 50-60 seconds that this process takes, the keyboard is locked and the display does not change. The end of this new "burn" of the EAROM is indicated by the start of the confidence test.

LOCAL

At any time while in configuration mode (after entering CTRL RWMODE) and prior to performing a CTRL RP sequence, a return can be made to normal mode by simply pressing the LOCAL key. Thus, configuration mode can be entered simply to display some information and can then be exited without making any changes.

If one or more CTRL RC sequences have been done before the LOCAL key is pressed, then certain areas of scratchpad memory will already have been changed.

The terminal displays '******' at the home position to indicate that this has been done without errors.

When writing into memory, addresses other than 007F - 00A0 and 0108 - 016F should not be used. All of the memory below and above these addresses are dedicated for specific internal terminal functions and cannot be used for other purposes. Attempts to read data from these locations yield zeroes; commands to store into such locations have no effect.

Terminal Configuration Parameters

The information in table 2-2 gives the parameters which may be configured into the EAROM of the terminal to define its characteristics. The normal defaults are marked with an asterisk (*). A certain amount of knowledge and discretion is needed to know when these can be changed and what the allowable values are.

Table 2-2. Terminal Configuration

Scratchpad Memory Address	Bit	State	Function	Remarks
0080		0A *	Network/data comm Bit Options	
	7	1	Synchronous data comm	
		0 *	Asynchronous data comm	
	6	1	Point-to-Point Network	(no address used)
		0 *	Multipoint Network	(address required)
	5	1	SOH clears screen first	
		0 *	SOH is a NOP	
	4	1	XMT home to ETX or end page	(forms XMT option)
		0 *	Normal XMT in forms mode	
	3	1 *	DC1 holds in RCV mode	(Programmatic Ctrl)
		0	DC1 erases rest of line	(B 9352 Line Erase)
	2	1	ODT enabled (used for SPO)	(Operator Display)
		0 *	ODT disabled Terminal	(Terminal only)
	1	1 *	Spare	
		0	Spare	
	0	1	Inhibit parity checking	(maintenance aid)
		0 *	Check parity (normal)	
0081		A1 *	First part of Baud Rate	(rest at 008C)
		E9	38.4K baud - - 008C is 08	
		D1	19.2K baud - - 008C is 08	
		A1 *	9600 baud - - 008C is 08	
		F5	4800 baud - - 008C is 09	
		E9	2400 baud - - 008C is 09	
		E1	1800 baud - - 008C is 09	
		D1	1200 baud - - 008C is 09	
		A1	600 baud - - 008C is 09	
		D1	300 baud - - 008C is 0A	
		B9	200 baud - - 008C is 0A	
		A1	150 baud - - 008C is 0A	
		7E	110 baud - - 008C is 0A	
		41	75 baud - - 008C is 0A	
0082		00 *	Clear-to-Send Delay (msc)	(modem CTS delay)
		10	V23 (4-wire), 600-1200 baud	
		C8	V23 (2-wire), 600-1200 baud	
		32	V21 and Bell 202 series	
		FF	Bell 103 series	
		10	Burroughs TA713 or TA783	
		01	Burroughs TDI or BDI	
0083		00 *	Spare	(no longer used)

Table 2-2. Terminal Configuration (Cont)

Scratchpad Memory Address	Bit	State	Function	Remarks
0084		17 *	Lines per Page - 1	(pagesize = 4m)
		03	4 line page	(also 0091, 0093)
		07	8 line page	
		0B	12 line page	
		0F	16 line page	
		17 *	24 line page	
		2E	48 line page (2 screen only)	
0085		4F *	Characters per Line - 1	(linesize = 40,80) (also 0092, bit 2)
		27	40 character line	
		4F	80 character line	

NOTE

The page size for the terminal may be set to any multiple of 4 lines. Display memory for (a) a 1 screen terminal is 24 lines of 80 characters (or 48 lines of 40 characters); and (b) a 2 screen terminal is 48 lines of 80 characters (or 96 lines of 40 characters). The number of pages available is thus the truncated integer obtained by dividing the total number of lines of display memory by the number of lines per page.

0086		7B *	Extra left forms delimiter	(converted to US)
0087		7D *	Extra right forms delimiter	(converted to RS)

NOTE

These two characters may be chosen from any on the keyboard. They will be converted to US and RS forms delimiters when forms mode is entered, thus giving the user a means of setting up his own form entirely through the keyboard. If this is not desired, these two characters can be changed to 1F and 1E, which are US and RS, so that no conversion occurs.

0088		00 *	Data comm Bit Options	
	7	1	Point-to-point Switched	
		0 *	Point-to-point Nonswitched	
	6	1	Enable transmission numbers	(XM# in protocol)
		0 *	Disable transmission numbers	(XM# not used)
	5	1	Enable 128 millisecond Delay	(Turnaround Time)
		0 *	Disable Turnaround Delay	(use 300 microsec.)
	4	1	Enable Clear-to-Send Delay	(set in 0082)
		0	Disable Clear-to-Send Delay	
	3	1	Enable Circuit 116	(CCITT data sets)
		0 *	Disable Circuit 116	
	2	1	Enable Circuit 111/126	(CCITT data sets)
		0 *	Disable Circuit 111/126	
	1	1	Use @ and A for XM#	(non-standard)
		0 *	Use 0 and 1 for XM#	(standard)
	0	1	Optional Poll/Select Chars.	(7B and 7C)
		0 *	Standard Poll/Select Chars.	(70 and 71)

Table 2-2. Terminal Configuration (Cont)

Scratchpad Memory Address	Bit	State	Function	Remarks
0089		XX	AD1 Poll/Select Address	(NDL address)
008A		XX	AD2 Poll/Select Address	(in ASCII code)
008B		XX	GSL Group Select Address	(in ASCII code)
			NOTE	
			AD1 AD2 is the two character NDL-defined address of the terminal. Note that the address defined in NDL and displayed by SYSTEM/ DCSTATUS is in EBCDIC code, but that it (like all other parts of each message) is translated into ASCII before being transmitted to the terminal. Thus, the address characters stored here must be the ASCII equivalent of the EBCDIC NDL-defined address. Bit 7, the parity bit, of each character must be set to zero.	
008C		09 *	ACIA Baud Rate Clock Divisor	(rest at 0081)
		0A	Baud Rate is 75-300	(divide by 64)
		09 *	Baud Rate is 600-4800	(divide by 16)
		08	Baud Rate is 9600-38.4K	(divide by 1)
008D		00 *	Spare	(no longer used)
008E		XX	GPL-AD1 Group Poll Address	(for group poll)
008F		XX	GPL-AD2 Group Poll Address	(in ASCII code)
0090		00 *	Dummy Byte for IBM 3270	(not used here)
0091		2F *	Total lines per system - 1	(for a 2 screen)
		17	1 screen, 80 chars/line	
		2F	1 screen, 40 chars/line	
		2F *	2 screen, 80 chars/line	
		5F	2 screen, 40 chars/line	
			NOTE	
			Total lines per system equals display memory size (1920 characters for 1 screen, 3840 characters for 2 screens) divided by the number of characters per line from location 0085.	
0092		1E *	Display format bit options	
	7	1	Enable 3-bit baud-rate delay	(XMT-to-RCV delay)
		0 *	Disable baud-rate delay	
	6	1	Upper-case only initially	(lower-case lockout)
		0 *	Lower-case enabled initially	
	5	1	Inhibit display of cursor	(cursor invisible)
		0 *	Enable display of cursor	
	4	1 *	Inhibit form field overflow	(remain at end)
		0	Allow form field overflow	(to next field)
	3	1 *	24 line display	(see also 0093)
		0	12 line display	

Table 2-2. Terminal Configuration (Cont)

Scratchpad Memory Address	Bit	State	Function	Remarks
	2	1 *	80 char/line display	(see also 0085)
		0	40 char/line display	
	1	1 *	Blinking cursor	
		0	Solid cursor	
	0	1	Treat LF as LF with auto CR	(treat as newline)
		0 *	Treat LF as only LF, no CR	
0093		17 *	Lines per display - 1	(24 line display)
		0B	12 line display	
		17 *	24 line display	
0094		07 *	End address display memory	(high-order byte)
		07	1920 char	
		0F	3840 char	
0095		80 *	End address display memory	(low-order byte)
		80 *	1920 char	
		00	3840 char	
0096		71	Character display bit options	
	7	1	Inhibit cursor wraparound	(non-forms only)
		0 *	Allow cursor to wraparound	(from end to home)
	6	1 *	Display tab-field identifier	(looks like →)
		0	No visible tab for SKIP/TAB	(keyboard tab only)
	5	1 *	Enable variable tabbing	(user sets/resets)
		0	Enable fixed tabbing	(tab increment 8)
	4	1 *	Display & store data comm ETX	(do ETX option)
		0	Do not store or display ETX	(for scrolling)
	3	1	Clear Key erases entire form	
		0 *	Clear erases unprotected only	
	2	1	TD700 VT look-alike	
		0 *	Standard VT interpretation	
	1	1	FF also clears variable tab stops	
		0	FF is form feed only	
	0	1 *	Interpret DC2 as cursor advance	
		0	Interpret DC2 as forms enable/disable	
0097		4F *	End-of-Line alarm column - 1	(set at col 80)
0098		27 *	End-of-Page alarm row - 1	(set at row 24)
0099		00 *	Start address display memory	(high-order byte)
		00	1 screen terminal	
		00	2 screen terminal	
009A		00 *	Start address display memory	(low-order byte)
		00	1 screen terminal	
		00	2 screen terminal	
009B		08 *	Peripheral bit options	
	7	1		
		0 *		

Table 2-2. Terminal Configuration (Cont)

Scratchpad Memory Address	Bit	State	Function	Remarks
	6	1		
		0 *		
	5	1		
		0 *		
	4	1		
		0 *		
	3	1 *	Hold in RCV mode enabled	(RCV after Receive)
		0	Hold in RCV mode disabled	(LOCAL after Rcvd)
009C		00 *	Start address data comm buffer	(high-order byte)
009D		00 *	Start address data comm buffer	(low-order byte)
009E		07 *	End address data comm buffer	(high-order byte)
		07	1920 char. buffer	
009F		81 *	End address data comm buffer	(low-order byte)
		81	1920 char. buffer	
00A0		50 *	Character interpretation	(new parameter)
	7	1	XMT from start of cursor line	(one-line XMT mode)
		0 *	XMT from mobile home position	(normal XMT mode)
	6	1 *	Store & XMT keyboard CR	(visible input CR)
		0	Do not display keyboard CR	(RET key only)
	5	1	No linefeed with keyboard CR	(auto LF option)
		0 *	Auto LF with keyboard CR	(RET is newline)
	4	1 *	Store & display data comm CR	(visible dc CR)
		0	Do not display data comm CR	
	3	1	No linefeed with data comm CR	(auto dc LF option)
		0 *	Auto LF with data comm CR	
	2	1	Advance cursor on ETX display	(ETX display)
		0 *	Do not advance cursor on ETC	(cursor on top ETX)
	1	1	Spare	(not assigned)
		0 *	Spare	
	0	1	Write data comm HT to memory	(→horizontal tab)
		0 *	Do not display data comm HT	(data comm tab only)

Sample Terminal Configurations

No two terminals are configured exactly the same, and configurations are constantly altered to suit changing individual needs. Since setting up an initial configuration can be a very tricky business, some sample parameters for typical terminal configurations follow.

a. For a 1 screen terminal configured to run at 9600 baud TDI on a B 6700 system, locations 0800 through 00A0 might look something like this:

```
0080/  0A  A1  01  00  17  4F  7B  7D
       10  XX  XX  XX  08  00  XX  XX

0090/  00  2F  5C  17  07  80  01  4F
       17  00  00  08  00  00  07  81

00A0/  54
```

b. For a 2 screen terminal configured to run asynchronously at 1200 baud with a bell 202C modem, the configuration parameters might look like:

```
0080/  0A  D1  32  00  17  3F  1F  1E
       20  XX  XX  XX  09  00  XX  XX

0090/  00  2F  DC  17  0F  00  01  4F
       27  00  00  08  00  00  07  81

00A0/  54
```

c. For a 1 screen terminal configured to run synchronously at 2400 baud as a SPO (ODT) Burroughs TA2401 modem, the configuration parameters might look like:

```
0080/  8A  E9  10  00  17  4F  1F  1E
       10  XX  XX  XX  09  00  XX  XX

0090/  00  2F  5C  17  07  80  01  4F
       17  00  00  08  00  80  07  81

00A0/  54
```

d. Finally, for a 1 screen terminal configured to run at 38.4K baud as a SPO (ODT) for the B 6700 system, the configuration parameters would be:

```
0080/  06  E9  01  00  17  4F  1F  1E
       10  00  00  00  08  7F  00  00

0090/  00  2F  5C  17  07  80  11  4F
       17  00  00  08  00  00  07  81

00A0/  54
```

Preprogrammed Error Messages

During manufacture, standard terminal error messages are preprogrammed into the terminal for display when the appropriate error occurs. Since these messages are also part of the EAROM, they can be personalized (altered) to suit the individual user. Each message can be up to 16 characters in length and is stored starting at the following addresses:

Address	Standard Message	Remarks
0110	DATA COMM ERROR	data comm buffer overflows
0150	DATA LOST	keyboard buffer overflow/message too long
0160	RECEIVING PG.	data comm message being received
0108	MODE	
0140	POWER FAULT	

The word "PAGE" (which is displayed along with the page number on the status line) is stored at locations 010C-020F. If "PAGE" is blanked out, no page number is displayed. If the RECEIVING message in locations 0160-026F is blanked out, no indication is given that input is being received by the terminal.

Table 2-3. Configuration Consistency Error Indicators

Digit	Test Failed
1	Location 85 and bit 2 of location 92 (characters per line).
2	Location 93 and bit 3 of location 92)number of lines per display).
3	Data comm buffer size + display store size (determined from start and end addresses at locations 94-95, 99-9A, 9C-9D and 9E-9F) is not larger than the length of userstore.
4	Characters per line (location 85) * total number of lines (location 91) is not larger than display store size (determined from location 99-9A and 94-95).
5	Total number of lines (location 91) is an integral multiple of the number of lines per page (location 84).
6	Number of lines per page (location 84) is an integral multiple of 4.
7	Number of lines per page (location 84) is at least 4.
8	The data comm buffer size (determined from locations 9C-9D and 9E-9F) is larger than 0, and the display store size (determined from location 99-9A and 94-94) is at least as large as the number of characters per line (location 85) * the number of lines per screen (location 92, bit 3).
9	ODT mode (location 80, bit 2) is not set at the same time that Network Type (location 80, bit 6) is set (point-to-point).

SECTION 3
DOCUMENTATION AND COMPONENTS

GENERAL

This section contains Logic Device Descriptions for the integrated circuits used in the MTS-1. An Index to the logic devices is provided listing the devices by Burroughs part number with a brief description and Logic type. Figure 3-1 shows Logic notation used in the logic diagrams in the Field Test and Repair Book.

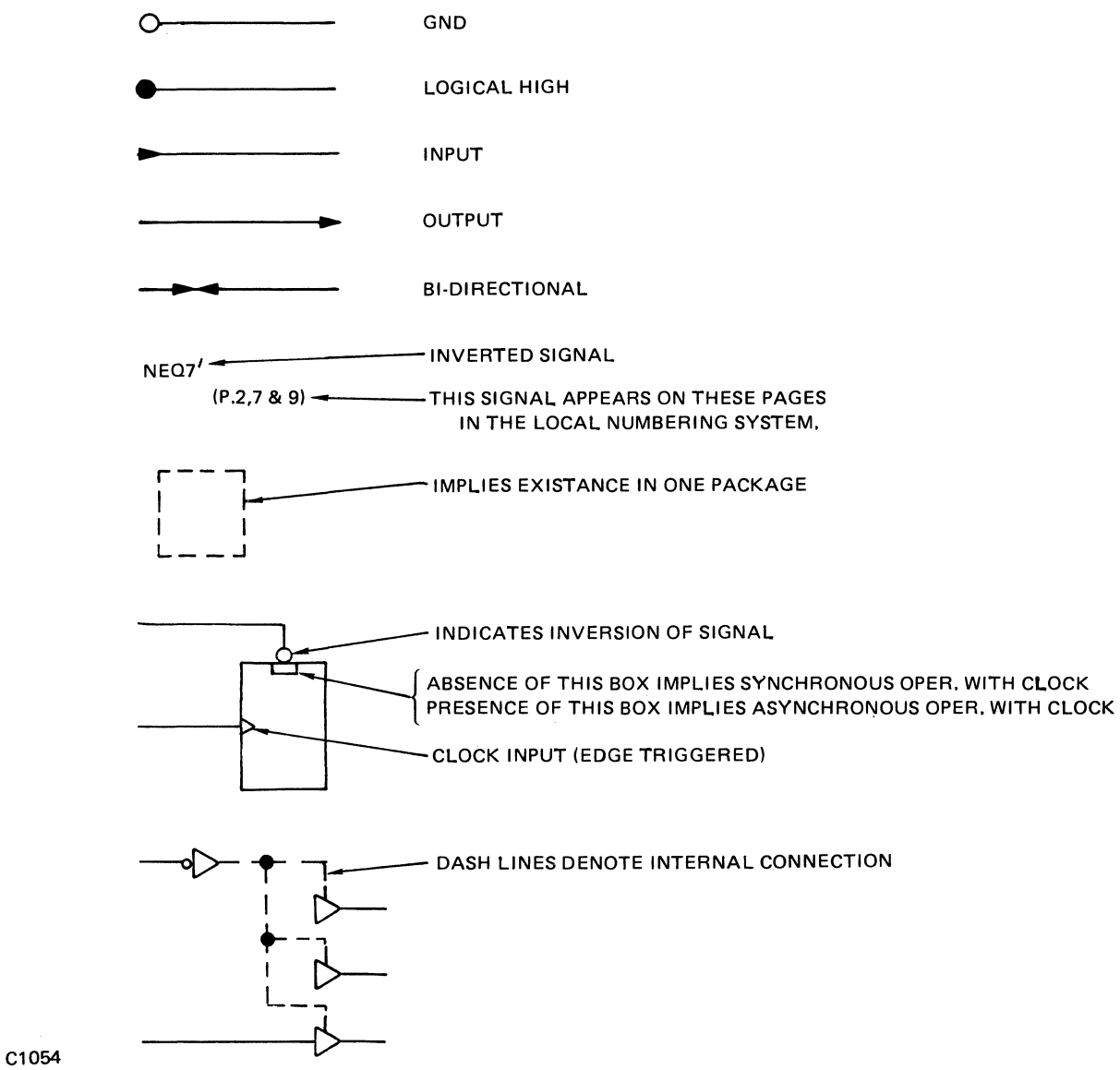


Figure 3-1. Logic Diagram Notation

INDEX

Part Number	Description	Type	Page
2889 1539	32 x 8 PROM (tri-state)	82S123	3-81
2889 1547	32 x 8 PROM (tri-state)	82S123	3-81
2889 1554	32 x 8 PROM (tri-state)	82S123	3-81
2889 1562	32 x 8 PROM (tri-state)	82S123	3-81
2889 1570	32 x 8 PROM (tri-state)	82S123	3-81
2889 1588	512 x 4 PROM (tri-state)	82S131	3-88
2889 1596	512 x 4 PROM	82S131	3-88
2889 1638	BCD to decimal decoder (1 of 10)	74LS42	3-103
2889 1646	Hex inverter	74C04	3-105
2889 1653	Quad D flip-flop	74C175	3-106
2889 1661	32 x 8 PROM (tri-state)	82S123	3-81
2889 1687	Quad 2 input AND gate	74LS08	3-107
2889 1695	8 bit addressable latch	CD4099B	3-108
2889 1711	Dual 4 input NOR gate	CD4002B	3-110
2889 1729	Triple 3 input NOR gate CD 4025B	CD4025B	3-111
2889 2446	1024x4 RAM 18 pin	2114L	3-112
2322 2292	Dual J-K Master Slave Flip-Flop	4027	3-114
1083 4935	Differential Comparator	LM311	3-116

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1619 7451

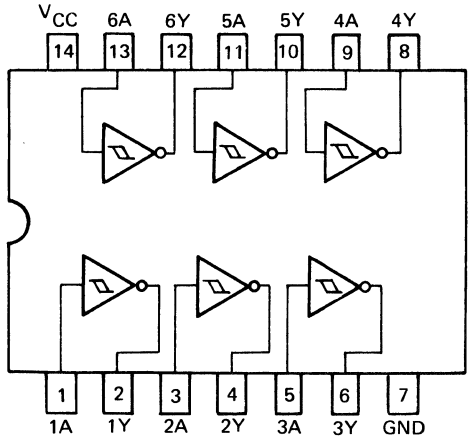
Integrated Circuit

Element Type:	CMOS
Standard Number:	74C14
Circuit Designation:	Hex schmitt trigger

Description of Operation:

This package contains six schmitt trigger circuits. They perform a logical inverting function. The output will go low when the input voltage goes more positive than the schmitt trigger high threshold voltage. The output will stay low until the input goes less positive than the schmitt trigger low threshold voltage.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.0 - 4.3 Volts
Low 0.4 - 0.5 Volts	Low 0.7 - 2.0 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1627 2718

Integrated Circuit

Element Type: TTL
Standard Number: 75110
Circuit Designation: Dual Line Driver

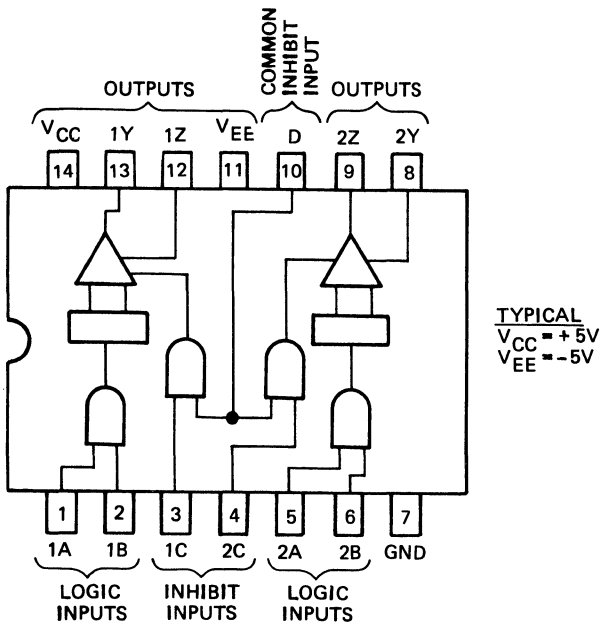
Description of Operation:

The 75110 is a dual line driver featuring independent channels with common voltage supply and ground terminals. The driver circuit features a constant current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by appropriate logic levels on the inhibit inputs.

The inhibit feature is provided so the circuit can be used in party-line or data-bus applications. A strobe or inhibitor, common to the driver, is included for increased driver-logic versatility. The output current in the inhibited mode, I_O (off), is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high - the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of -3 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

Outputs	Inputs
High 2.0 Volts min.	Low .8 Volts max.



Truth Table

Logic Inputs		Inhibitor Inputs		Outputs	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the "ON" state
High output represents the "OFF" state

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1627 5158

Integrated Circuit

Element Type: MOS
Standard Number: 2350
Circuit Designation: Universal Synchronous receiver/transmitter (USRT)

Description of Operation:

The Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines, and status. Common to the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream; bit synchronous with respect to a clock, and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous, formatting a 5, 6, 7, or 8-bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overruns (ROR), receive parity error (RPE), and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs. The function of each input or output pin is given in table 3-1.

Table 3-1. Signal Function of 1627 5158 Module

Pin No.	Signal	Function
1	GND	DC ground
2	VCC	+5 volts ± 5%
3	NPB	No Parity Bit. When NPB = 0 (logic low), the parity circuit for transmit and receive is enabled. When NPB = 1 (logic high), the parity generation for the transmitter is disabled, and the parity in the receiver is not checked. With parity disabled, the RPE status bit is held at a logic low level.
4	POE	Parity Odd/Even. When POE = 1 (logic high), the transmit and receive circuits operate with even parity. When POE = 0 (logic low), the transmit and receive circuits operate with odd parity. When NPB = 1, the POE circuit is disabled.
5	$\overline{CS}$	Control Strobe. When $\overline{CS}$ = 0 (logic low), the control signals NDB1, NDB2, POE, and NPB are loaded into the control register.
6	TSO	Transmitter Serial Output. Data in the transmitter-shift-register is transmitted serially, least significant bit first, over signal TSO at a rate equal to the transmit-clock drequency (TCP). Source of data to the transmitter-shift-register is from the transmitter-holding-register or the transmitter-fill-register.

Table 3-1. Signal Function of 1627 5158 Module (Cont)

Pin No.	Signal	Function
7	FCT	Fill Character Transmitted. Signal FCT is a transmit status bit. When FCT = 1 (logic high), data from the transmitter-fill-register has been transferred to the transmitter-shift-register. Signal FCT goes to a logic low when data are transferred from the transmitter-holding-register to the transmitter-shift-register, or on the positive transition of signal $\overline{SWE}$ or RESET. Signal FCT is multiplexed onto output RD6 when $\overline{SWE}$ = 0 and $\overline{RDE}$ = 1.
8	SCR	Sync Character Received. Signal SCR is a receive status bit. When SCR = 1 (logic high), the data in the receive-shift-register is the same as the data in the receive-sync-register. Signal SCR is multiplexed onto output RD3 when $\overline{SWE}$ = 0 and $\overline{RDE}$ = 1.
9	TBMT	Transmit Buffer Empty. Signal TBMT is a transmit status bit. When TBMT = 1 (logic high), the data in the transmitter-holding-register has been transferred to the transmitter-shift-register, and new data may be loaded. Signal TBMT is multiplexed onto output RD7 when SWE = 0 and $\overline{RDE}$ = 1.
10	RPE	Receive Parity Error. Signal RPE is a receive status bit. When RPE = 1 (logic high), the received character transferred into the receive-output-register has incorrect parity. Signal RPE is reset to a logic low when the next character is received or by restart ($\overline{RR}$), or RESET. Signal RPE is multiplexed onto output RD2 when $\overline{SWE}$ = 0 and $\overline{RDE}$ = 1.
11	ROR	Receiver Overrun. Signal ROR is a receive status bit. When ROR = 1 (logic high), data has been transferred from the receiver-shift-register into the receiver-output-register, while signal RDA is still at a logic high. This condition indicates that no action was ever taken on the data that was previously in the receiver-output-register. Signal ROR is multiplexed onto output RD1 when $\overline{SWE}$ = 0 and $\overline{RDE}$ = 1.
12	RDA	Received Data Available. Signal RDA is a receive status bit. When RDA = 1 (logic high), data is available in the receiver-output-register. Signal RDA is reset to a logic low on the positive transition of signal $\overline{RDE}$ or by restart ($\overline{RR}$) or RESET. Signal RDA is multiplexed onto output RDO when $\overline{SWE}$ = 0 and $\overline{RDE}$ = 1.
13	RR	Receive Restart. A logic low ($\overline{RR}$ = 0) resets the receiver section of the module by clearing status bits RDA, SCR, ROR, and RPE. The positive transition of signal $\overline{RR}$ causes the module to enter a transparent mode which enables a search for a comparison between the contents of the receiver-shift-register and the receiver-sync register. After a compare is made, signal SCR is set high (logic 1) and the sync character is transferred to the receiver-output-register. The module now starts a word synchronous mode which frames the input data bits into character word times.
14	RESET	Master Reset. A logic high (RESET = 1) resets and initializes both the receiver and transmitter sections of the module.

Table 3-1. Signal Function of 1627 5158 Module (Cont)

Pin No.	Signal	Function
15 16 17 18 19 20 21 22	D0 D1 D2 D3 D4 D5 D6 D7	Data Inputs. Data bits 1 through 8 are loaded into the transmitter-holding register by signal $\overline{TDS}$, the transmitter-fill-register by signal $\overline{TFS}$, and the receiver-sync-register by signal $\overline{RSS}$. The data bits are right justified with the least significant bit at D0.
23	$\overline{RSS}$	Receiver Sync Strobe. A logic low ($\overline{RSS}$ = 0) causes input data bits D0 through D7 to be loaded into the receiver-sync-register. This register is used as identification of the code for a SYN character.
24	$\overline{TFS}$	Transmit Fill Strobe. A logic low ($\overline{TFS}$ = 0) causes input data bits D0 through D7 to be loaded into the transmitter-fill-register. The character in the transmitter-fill-register is transmitted when a new character is not loaded in the available time.
25	RSI	Receive Serial Input. Serial data is clocked into the receive-shift-register, least-significant bit first, at a rate equal to the receive-clock-frequency (RCP).
26 27 28 29 30 31 32 33	RD7 RD6 RD5 RD4 RD3 RD2 RD1 RD0	Received Data Outputs. RD0 through RD7 are tri-state outputs. As selected by the logic state of $\overline{SWE}$ and $\overline{RDE}$, outputs RD0 through RD7 can receive data from the receiver-output-register, the status bits, or provide the third state (high impedance) condition. The output conditions of RD0 through RD7 are as follows:

Control		Outputs							
$\overline{SWE}$	$\overline{RDE}$	RD0	RD1	RD2	RD3	RD4	RD5	RD6	RD7
0	0	Z	Z	Z	Z	Z	Z	Z	Z
0	1	RDA	ROR	RPE	SCR	0	0	FCT	TBMT
1	0	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
1	1	Z	Z	Z	Z	Z	Z	Z	Z

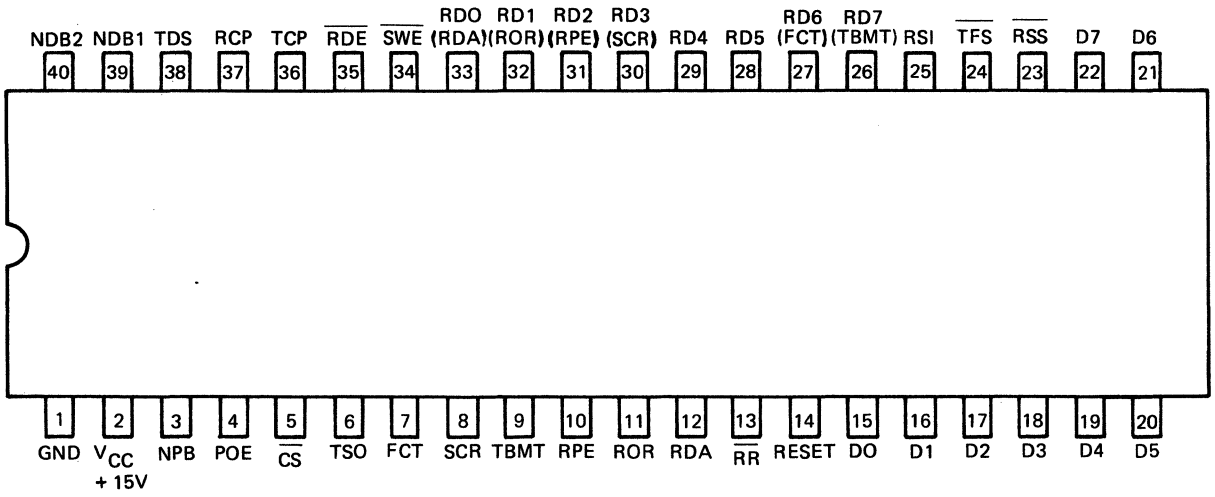
Z = High Impedance Third State Condition

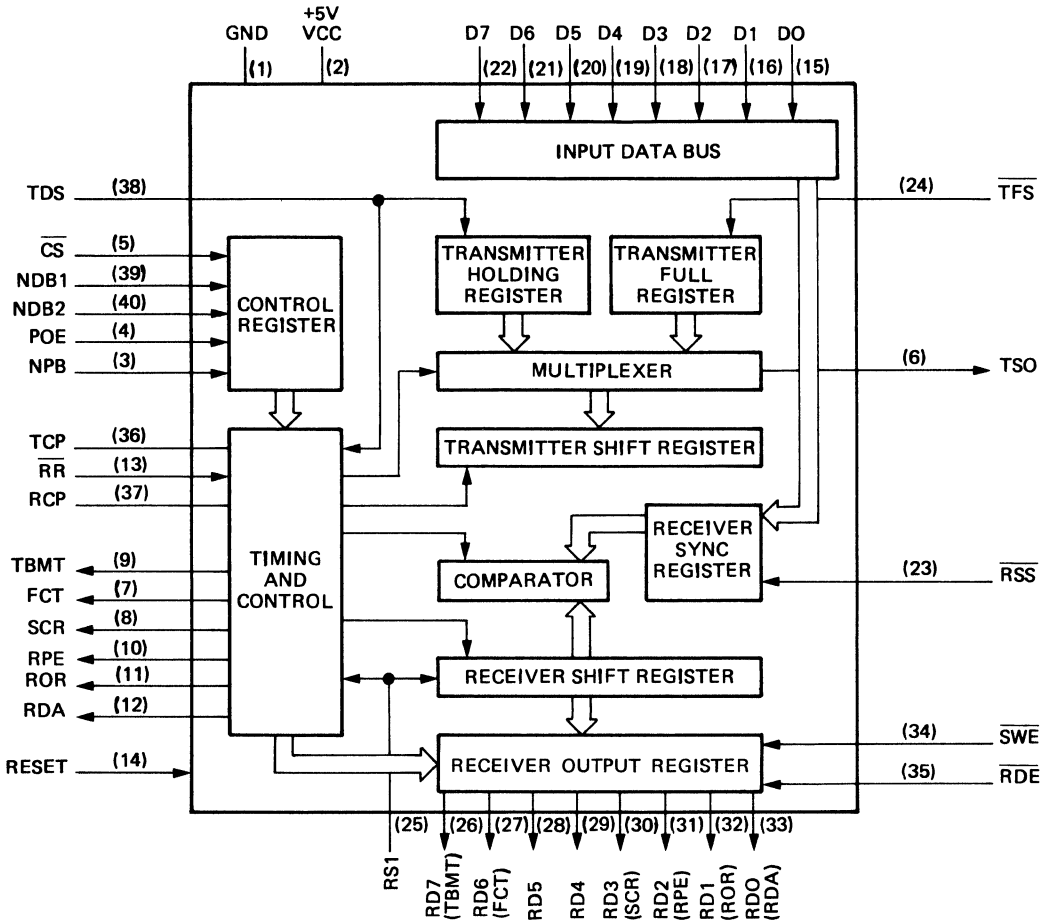
34	$\overline{SWE}$	Status Word Enable. A logic low ($\overline{SWE}$ = 0) enables the status bits to the output data lines (RD0 through RD7). The positive transition of $\overline{SWE}$ resets status bits FCT, ROR, RPE, and SCR.
35	$\overline{RDE}$	Receive Data Enable. A logic low ($\overline{RDE}$ = 0) enables the data from the receiver-output-register onto the output data lines (RD0 through RD7). The positive transition of $\overline{RDE}$ resets status bit RDA.
36	TCP	Transmit Clock. TCP is the transmit frequency. A new data bit is started on each positive transition of TCP.
37	RCP	Receive Clock. RCP is the shift clock for the receiver-shift-register. Each received data bit is detected and shifted on the negative transition of RCP.

Table 3-1. Signal Function of 1627 5158 Module (Cont)

Pin No.	Signal	Function
38	$\overline{TDS}$	Transmit Data Strobe. A logic low ($\overline{TDS}$ = 0) loads the data bits from the transmitter-holding-register into the transmitter-shift-register and it also resets status bit TBMT.
39	NDB1	Number of Data Bits. Signals NDB1 and NDB2 are used to format the number of data bits per character. As indicated below, the number of data bits does not include the parity bit:
40	NDB2	

NDB1	NDB2	Character Length (less parity)
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits




GND (1)
+5V VCC (2)
D7 (22)
D6 (21)
D5 (20)
D4 (19)
D3 (18)
D2 (17)
D1 (16)
DO (15)
INPUT DATA BUS
TDS (38)
CS (5)
NDB1 (39)
NDB2 (40)
POE (4)
NPB (3)
CONTROL REGISTER
TRANSMITTER HOLDING REGISTER
TRANSMITTER FULL REGISTER
MULTIPLEXER
TRANSMITTER SHIFT REGISTER
(24) TFS
(6) TSO
TCP (36)
RR (13)
RCP (37)
TIMING AND CONTROL
RECEIVER SYNC REGISTER
COMPARATOR
(23) RSS
TBMT (9)
FCT (7)
SCR (8)
RPE (10)
ROR (11)
RDA (12)
RECEIVER SHIFT REGISTER
RESET (14)
(34) SWE
(35) RDE
RECEIVER OUTPUT REGISTER
(25) RS1
(26) RD7 (TBMT)
(27) RD6 (FCT)
(28) RD5
(29) RD4
(30) RD3 (SCR)
(31) RD2 (RPE)
(32) RD1 (ROR)
(33) RDO (RDA)

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1627 5513

Integrated Circuit

Element Type: MOS
Standard Number: ER1400
Circuit Designation: 1400 Bit Electrically Alterable Read Only Memory

Description of Operation:

The ER1400 is a serial input/output 1400 bit electrically erasable and programmable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

Addressing is by two consecutive one-of-ten codes.

Model Selection is by a 3 bit code applied to C1, C2 and C3.

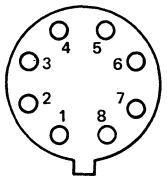
Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transisters. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Outputs	Inputs
High Vss - 1.0 Volts min., Vss + 0.3 Volts max.	High Vss - 1.0 Volts min., Vss + 0.3 Volts max.
Low Vss - 12 Volts max.	Low Vss - 15 Volts min., Vss - 8 Volts max.

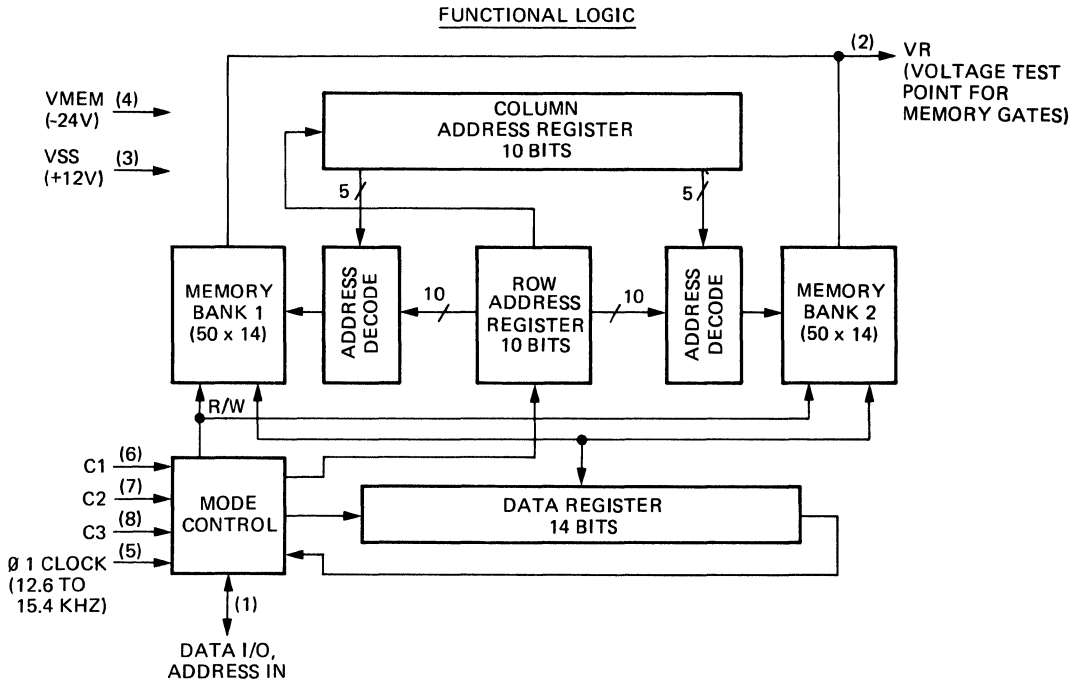
Pin No.	Name	Function
1	Data	In the Accept Address and Accept Data Modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating.
2	V_M	Used for testing purposes only. Should be left unconnected for normal operation.
3	V_{SS}	Chip substrate. Normally connected to ground.
4	V_{CC}	DC supply. Normally connected to -35 volt supply.
5	Clock	14KHZ timing reference.
6,7,8	C1, C2, C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby - contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address - Data presented at the I/0 pin is shifted into the Address Register with each clock pulse.
1	0	0	Read - The address word is read from memory into the data register.
1	0	1	Shift Data Out - The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase - The word stored at the addressed location is erased to all zeros.
1	1	1	Accept Data - The data register accepts serial data presented at the I/0 pin. The Address Register remains unchanged.
1	1	0	Write - The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used.

Bottom View



1. Data 1/0
2. V_M
3. V_{SS}
4. V_{GG}
5. Clock
6. C1
7. C2
8. C3


FUNCTIONAL LOGIC
(2)
VR
(VOLTAGE TEST
POINT FOR
MEMORY GATES)
VMEM (4)
(-24V)
VSS (3)
(+12V)
COLUMN
ADDRESS REGISTER
10 BITS
5
5
MEMORY
BANK 1
(50 x 14)
ADDRESS
DECODE
10
ROW
ADDRESS
REGISTER
10 BITS
10
ADDRESS
DECODE
MEMORY
BANK 2
(50 x 14)
R/W
C1 (6)
C2 (7)
C3 (8)
Ø 1 CLOCK (5)
(12.6 TO
15.4 KHZ)
MODE
CONTROL
DATA REGISTER
14 BITS
(1)
DATA I/O,
ADDRESS IN

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1904 0237

Integrated Circuit

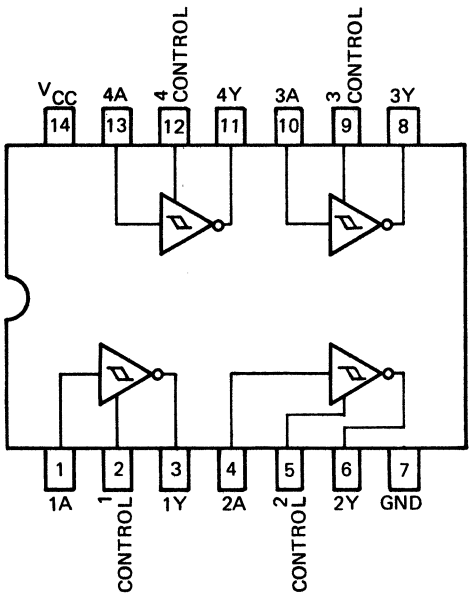
Element Type: TTL
Standard Number: 75189
Circuit Designation: Quad Line Receivers

Description of Operation:

The SN75189 is a monolithic quadruple line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage can be connected between this terminal and ground to shift the input threshold voltage levels. An external capacitor can be connected from this terminal to ground to provide input noise filtering.

Outputs

High 2.6 volts min.
Low .45 volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1904 0229

Integrated Circuit

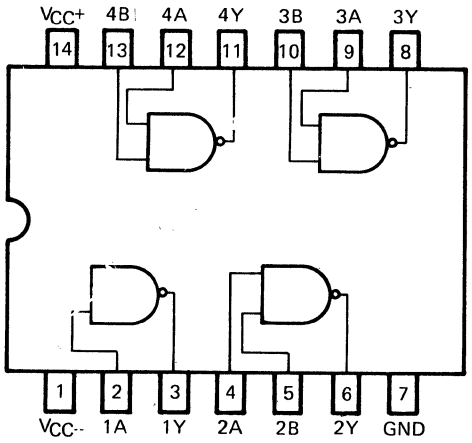
Element Type: TTL
Standard Number: 75188
Circuit Designation: Quad Line Driver

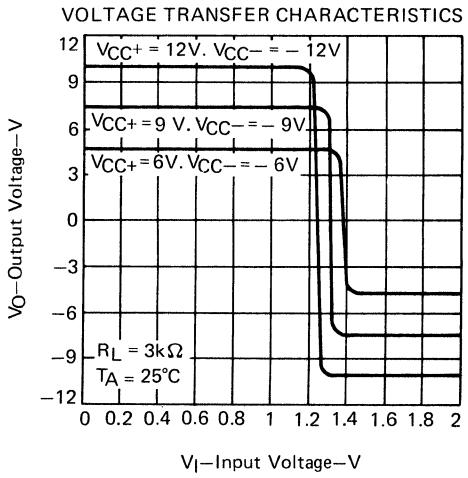
Description of Operation:

The SN75188 is a nonolithic quadruple line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard RS-232C. The device is characterized for operation from 0°C to 75°C.

Inputs

High 1.9 volts min.
Low .8 volts max.





Function Table

A	B	Y
H	H	L
L	X	H
X	L	H

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2607 1787

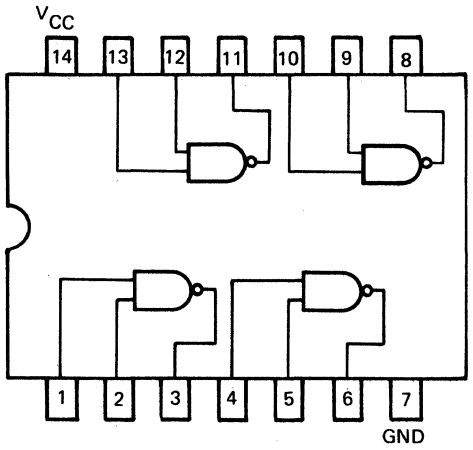
Integrated Circuit

Element Type:	TTL (low power schottky)
Standard Number:	74LS00
Circuit Designation:	Quad 2 input NAND gate

Description of Operation:

This package contains four 2-input NAND gates. The gates perform the function $AB = \overline{Y}$ where A and B are inputs and Y is the output. A low level on either A or B will produce a high level at Y, if both inputs are high, the result at Y will be low.

Outputs	Inputs
High 2.7 Volts min.	High 2 Volts min.
Low .5 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2607 1803

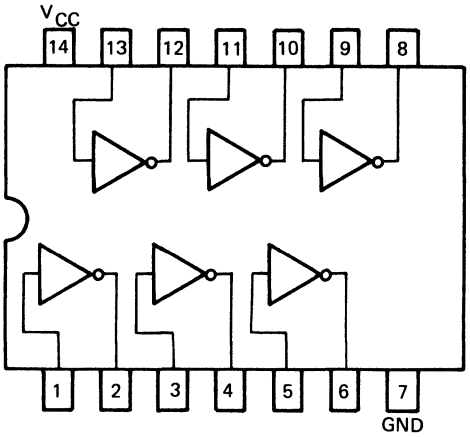
Integrated Circuit

Element Type:	TTL (low power schottky)
Standard Number:	74LS04
Circuit Designation:	Hex inverter

Description of Operation:

This package contains six inverters. A low/high input level will produce a high/low output level, respectively.

Outputs	Inputs
High 2.7 Volts min.	High 2 Volts min.
Low .5 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2607 1811

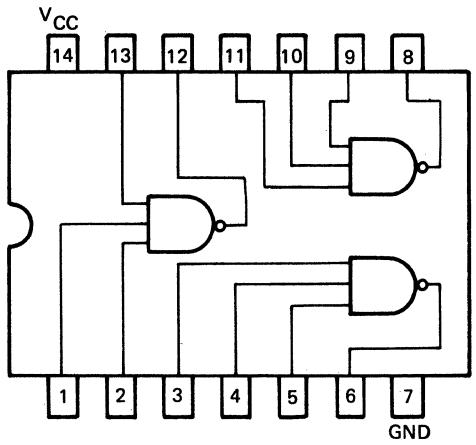
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 74LS10
Circuit Designation: Triple 3-input NAND gate

Description of Operation:

This package contains three-3-input NAND gates. The gates perform the function $\overline{A} + \overline{B} + \overline{C} = Y$. A low level on A or B or C is required to produce a high output level on Y; all inputs must be high to produce a low level at Y.

Outputs	Inputs
High 2.7 Volts min.	High 2 Volts min.
Low .5 max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2607 1829

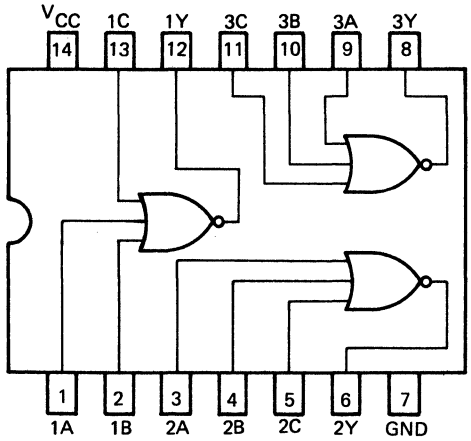
Integrated Circuit

Element Type:	TTL (low power schottky)
Standard Number:	74LS27
Circuit Designation:	Triple 3 input NOR gate

Description of Operation:

This package contains three 3-input NOR gates. The gates perform the function A + B + C = $\overline{Y}$ where A, B, and C are inputs and Y is the output. A low level is required at A, B, and C to produce a high output level, otherwise the level is low.

Outputs	Inputs
High 2.7 Volts min.	High 2 Volts min.
Low .5 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2608 2081

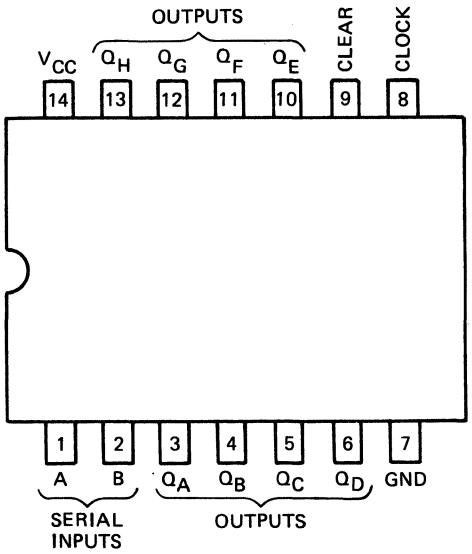
Integrated Circuit

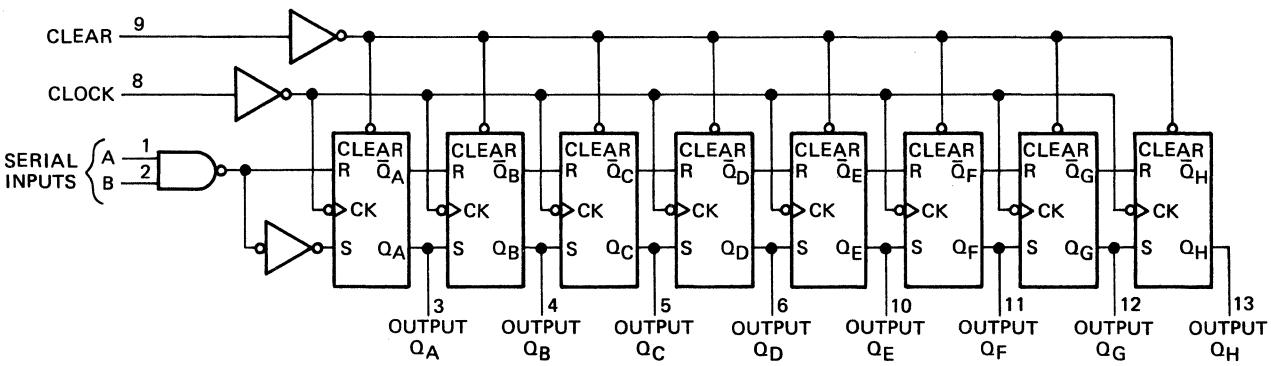
Element Type:	TTL (low power schottky)
Standard Number:	74LS164
Circuit Designation:	8-bit parallel-out serial shift register

Description of Operation:

This package contains one 8-bit parallel-output serial input shift register. This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but the only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input.

Outputs	Inputs
High 2.7 to 3.4 Volts	High 2.0 Volts min.
Low 0.35 to 0.5 Volts	Low 0.8 Volts max.



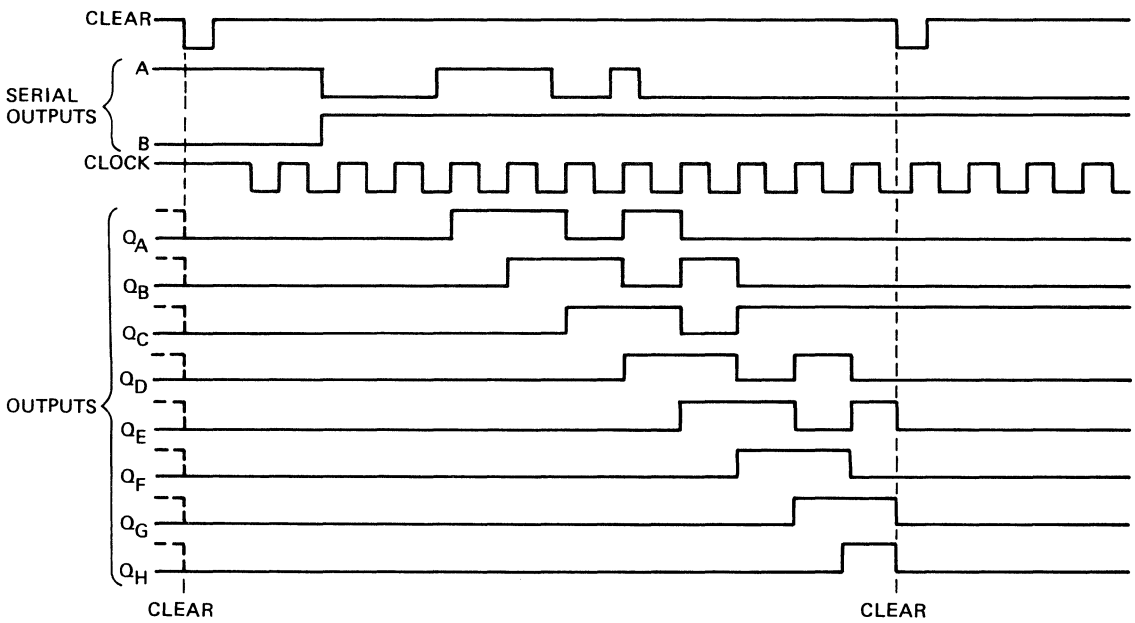


Logic Equation/Truth Table

Inputs				Outputs		
Clear	Clock	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

X = irrelevant (any input, including transitions)
H = high level (steady state)
L = Low level (steady state)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H respectively before the indicated steady-state input conditions were established
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

Typical Clear, Shift, and Clear Sequences



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2608 6306

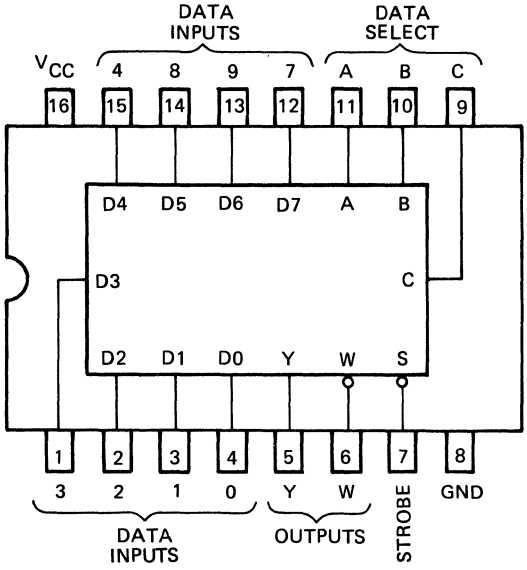
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 74LS251
Circuit Designation: Data select or/ multiplexer w/3-state outputs

Description of Operation:

This package contains one data selector/multiplexer. It performs a binary decode to select one-of-eight data sources to appear at the output. It also has a strobe controlled three state output. When the strobe is low, the outputs are active and follow the selected input.

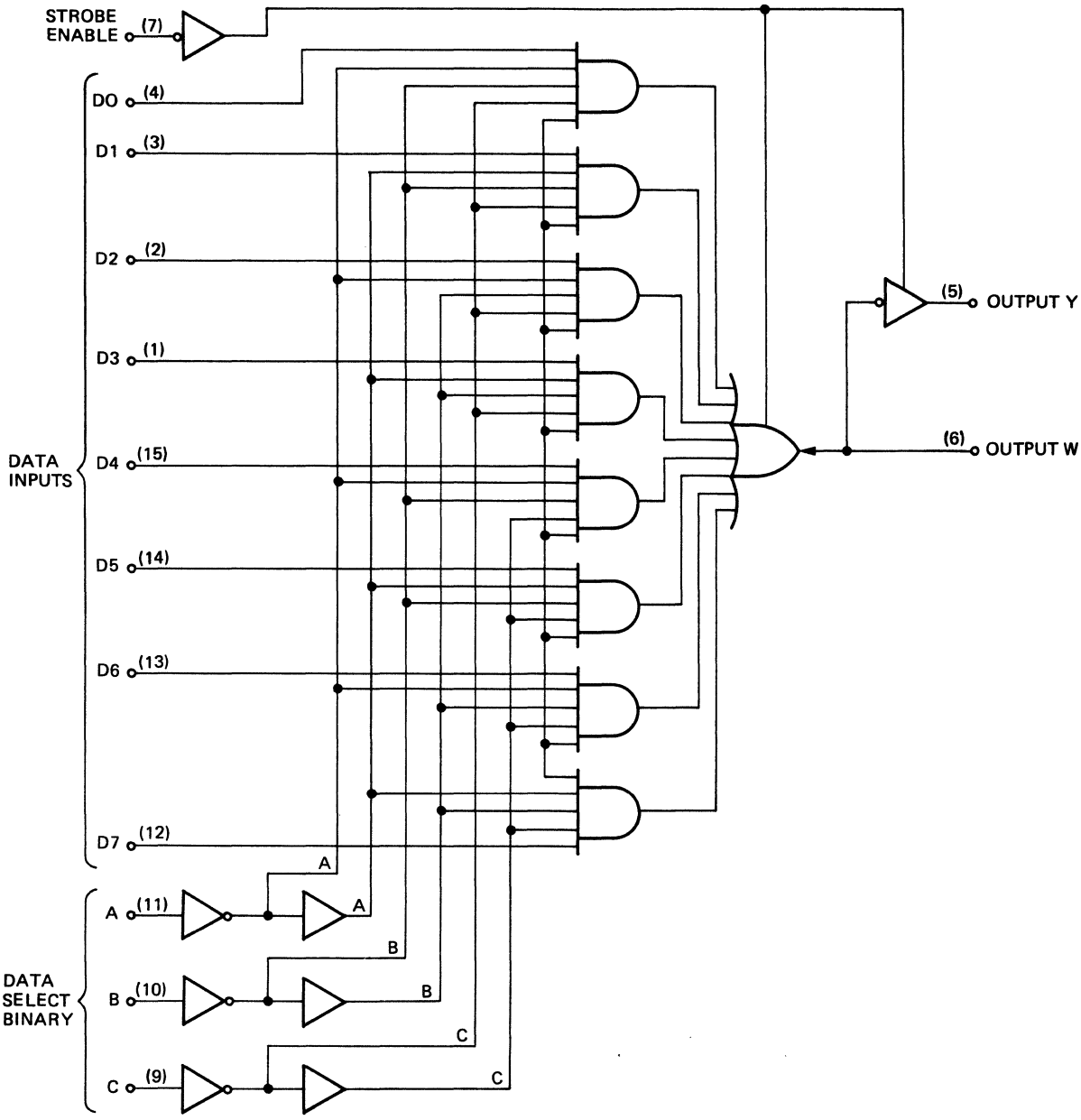
Outputs	Inputs
High 2.7 to 3.4 Volts	High 2.0 min.
Low 0.35 to 0.5 Volts	Low 0.8 max.



Logic Equation/Truth Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level
L = low logic level
X = irrelevant
Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input


STROBE ENABLE
(7)
DO
(4)
D1
(3)
D2
(2)
D3
(1)
DATA INPUTS
D4
(15)
D5
(14)
D6
(13)
D7
(12)
A
(11)
B
(10)
C
(9)
DATA SELECT BINARY
(5)
OUTPUT Y
(6)
OUTPUT W

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2846 6654

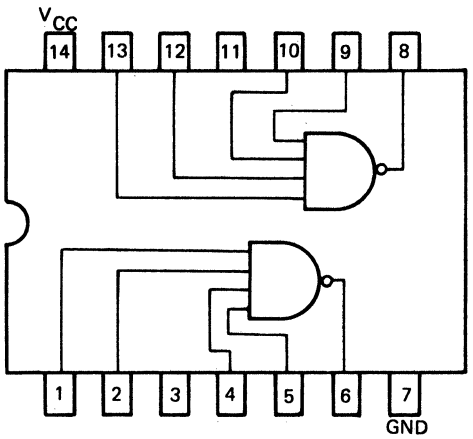
Integrated Circuit

Element Type:	TTL (low power schottky)
Standard Number:	74LS20
Circuit Designation:	Dual 4 input NAND gate

Description of Operation:

This package contains two 4-input NAND gates. The gates perform the function A, B, C, and D = $\overline{Y}$ where A, B, C, and D are inputs and Y is the output. A high level is required on all inputs to produce a low output level, otherwise the level is high.

Outputs	Inputs
High 2.7 Volts min.	High 2 Volts min.
Low .5 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2846 6696

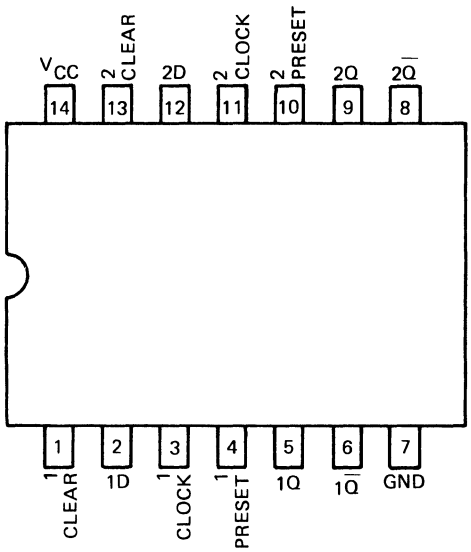
Integrated Circuit

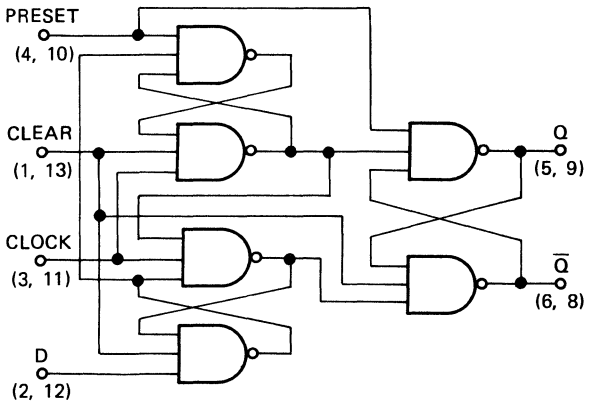
Element Type: TTL (low power schottky)
Standard Number: 74LS74
Circuit Designation: Dual D-type positive edge triggered flip-flop

Description of Operation:

This package contains two D-type positive edge-triggered flip-flops with individual D clock, preset, and clear inputs. Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

	Outputs	Inputs
	High 2.7 to 3.4 Volts	High 2.0 Volts min.
	Low 0.35 to 0.5 Volts	Low 0.8 Volts max.





Logic Equation/Truth Table (Each Flip-Flop)

Inputs				Outputs	
Preset	**Clear**	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
* = This condition is nonstable. It will not remain after clear and preset return to their inactive (high) state.

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2846 6704

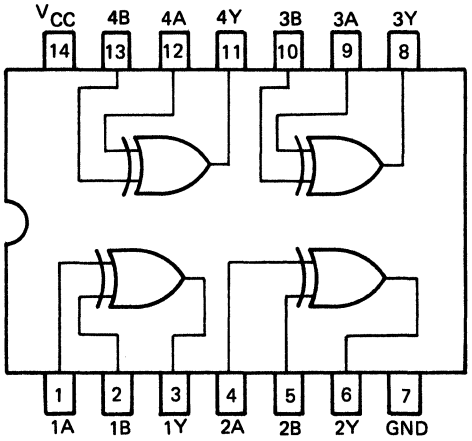
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 74LS86
Circuit Designation: Quad 2 input EXCLUSIVE-OR gate

Description of Operation:

This package contains four 2-input EXCLUSIVE-OR circuits. If A or B is high, the result at Y is high. If A and B are high or low, the result at Y is low.

Outputs	Inputs
High 2.7 to 3.4 Volts	High 2 Volts min.
Low 0.35 to 0.5 Volts	Low .8 Volts max.



Truth Table

Inputs		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

0 = low level
1 = high level

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2846 6738

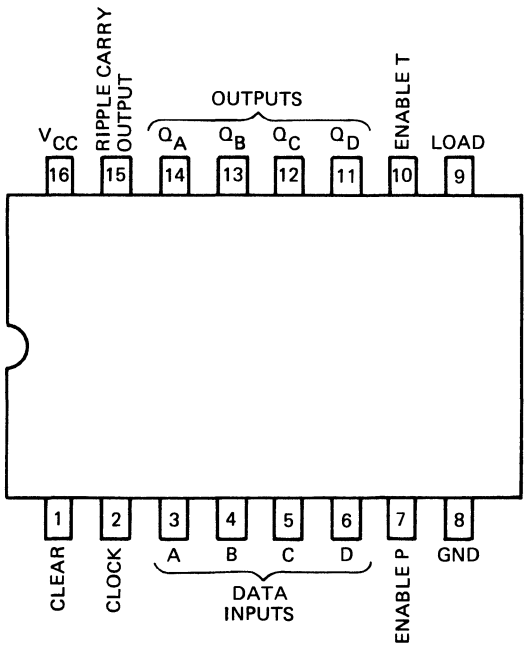
Integrated Circuit

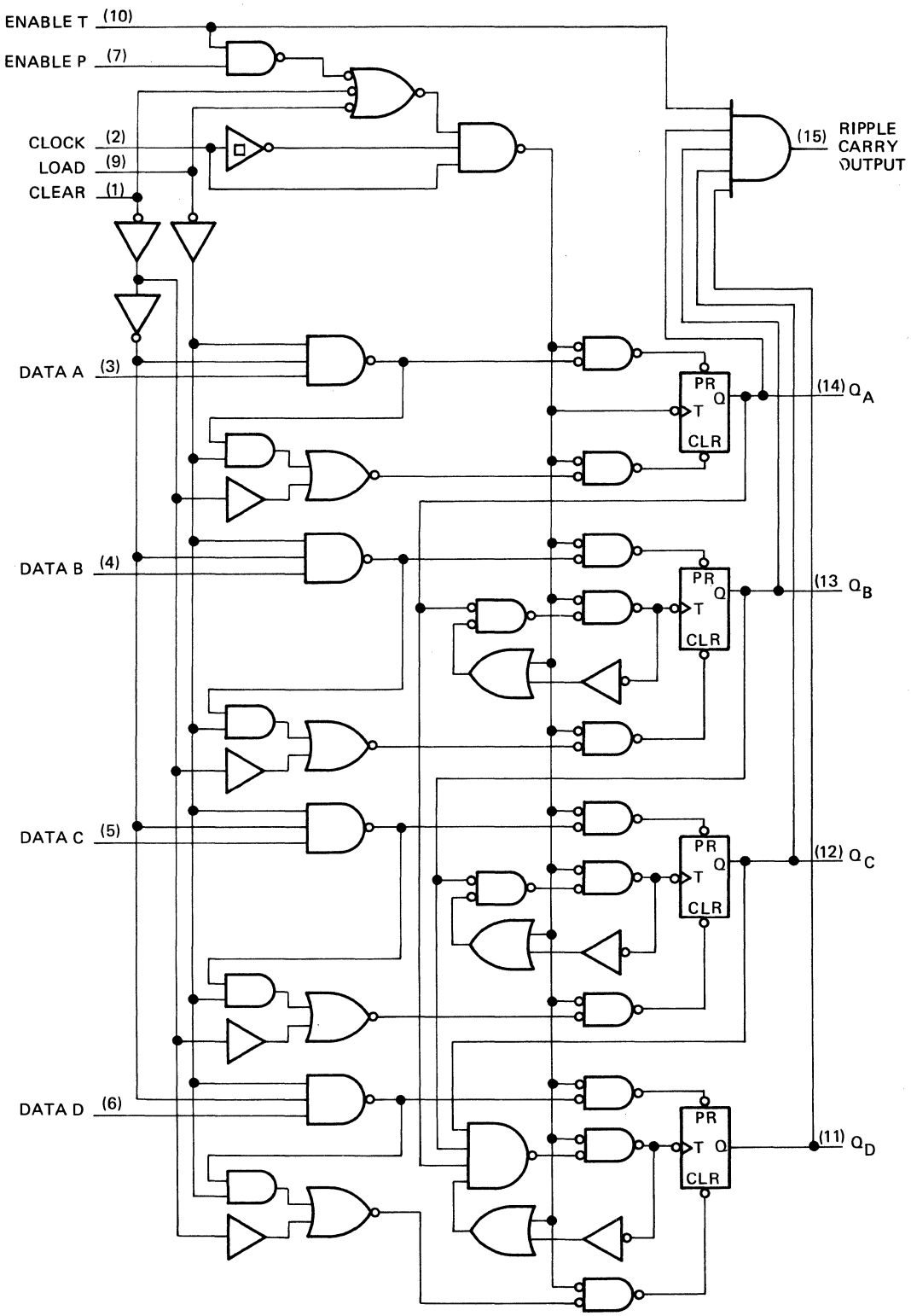
Element Type:	TTL (low power schottky)
Standard Number:	74LS161
Circuit Designation:	Synchronous 4-bit binary counter

Description of Operation:

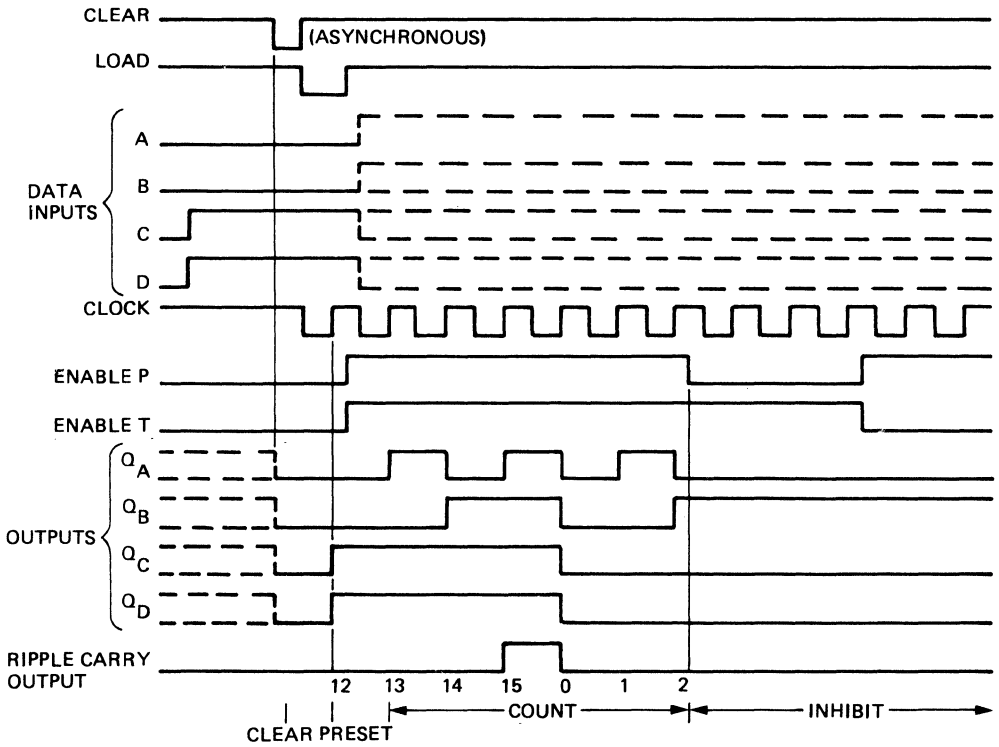
This package contains a synchronous presettable binary counter with an internal carry look ahead for high speed counting applications. Synchronous operation is provided by having all flip-flops clock simultaneously so that the outputs change coincident with each other. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. The counter outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Outputs	Inputs
High 2.7 to 3.4 Volts	High 2.0 Volts min.
Low 0.35 to 0.5 Volts	Low 0.8 Volts max.




ENABLE T (10)
ENABLE P (7)
CLOCK (2)
LOAD (9)
CLEAR (1)
DATA A (3)
DATA B (4)
DATA C (5)
DATA D (6)
(15) RIPPLE CARRY OUTPUT
PR
T
CLR
Q
(14) Q_A
(13 Q_B
(12) Q_C
(11) Q_D

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES
ILLUSTRATED BELOW IS THE FOLLOWING SEQUENCE:
1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY TWELVE
3. COUNT TO THIRTEEN, FOURTEEN, FIFTEEN, ZERO, ONE, AND TWO
4. INHIBIT



LOGIC DEVICE.DESCRIPTION
(Bur.) P/N 2846 6746

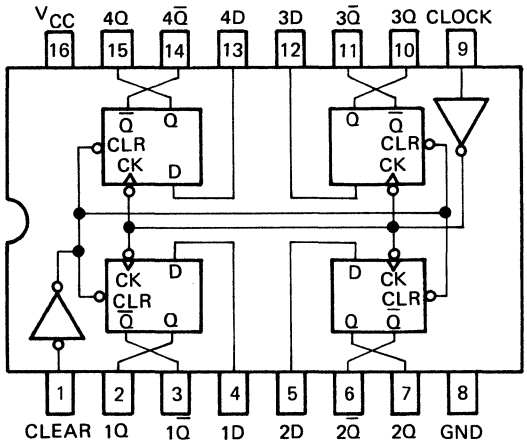
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 74LS175
Circuit Designation: Quad D FF

Description of Operation:

This package contains four D-type edge triggered flip-flops. Information at the D inputs is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

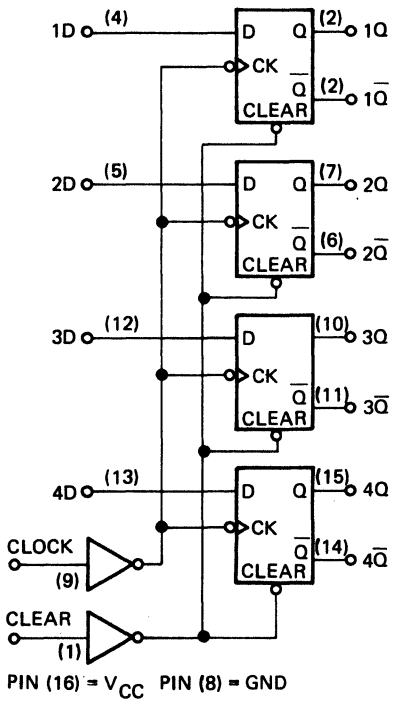
Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.5 min.
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts max.



Logic Equation/Truth Table

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established


1D
(4)
D
Q
(2)
1Q
CK
Q
(2)
1Q
CLEAR
2D
(5)
D
Q
(7)
2Q
CK
Q
(6)
2Q
CLEAR
3D
(12)
D
(10)
3Q
CK
Q
(11)
3Q
CLEAR
4D
(13)
D
Q
(15)
4Q
CK
Q
(14)
4Q
CLEAR
CLOCK
(9)
CLEAR
(1)
PIN (16) = VCC
PIN (8) = GND

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0366

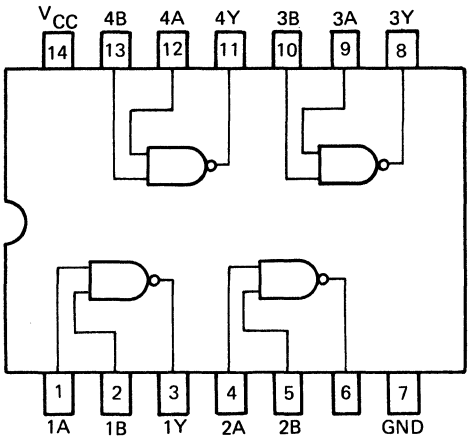
Integrated Circuit

Element Type: CMOS
Standard Number: 74C00
Circuit Designation: Quad 2-input NAND gate

Description of Operation:

This package contains four 2-input NAND gates. They perform the function $AB = \overline{Y}$ where A and B are inputs and Y is the output. If A or B is low, the output will be high. Both A and B must be high to result in a low at Y.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.0 - 3.5 Volts
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0374

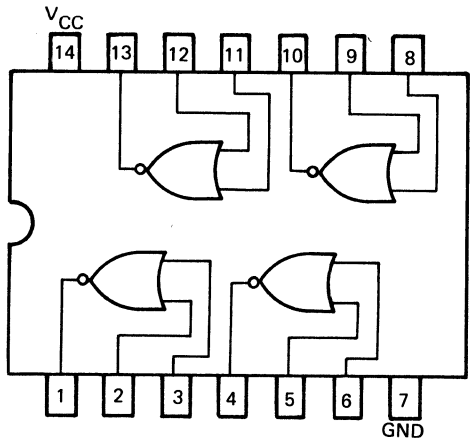
Integrated Circuit

Element Type:	CMOS
Standard Number:	74C02
Circuit Designation:	Quad 2-input NOR gate

Description of Operation:

This package contains four 2-input NOR gates. They perform the function $A+B = \overline{Y}$ where A and B are inputs and Y is the output. If A or B is high, the output is low. Both inputs must be low for the output to be high.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.0 - 3.5 Volts
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0382

Integrated Circuit

Element Type: MOS
Standard Number: 91L30
Circuit Designation: 1024X4 Static Random Access Memory

Description of Operation:

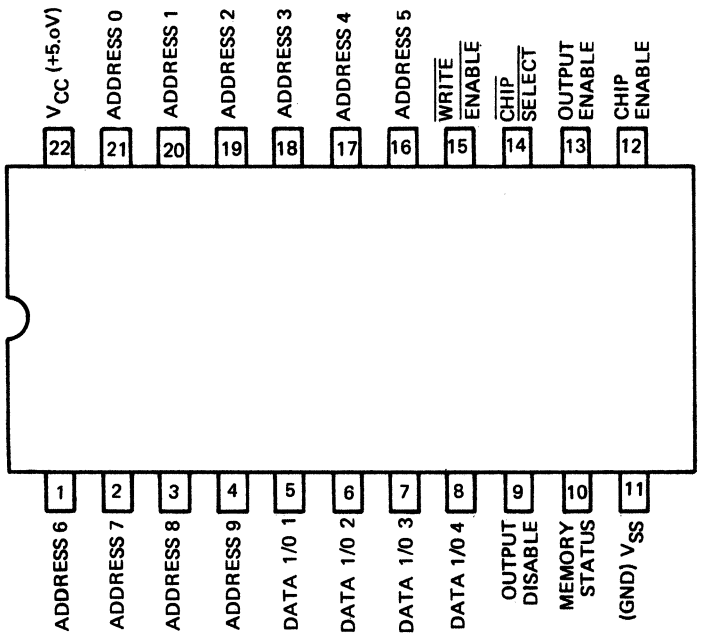
This device is a high performance, adaptive, low-power 4k-bit, static, read/write random access memory. It is implemented as 1024 words by 4 bits per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

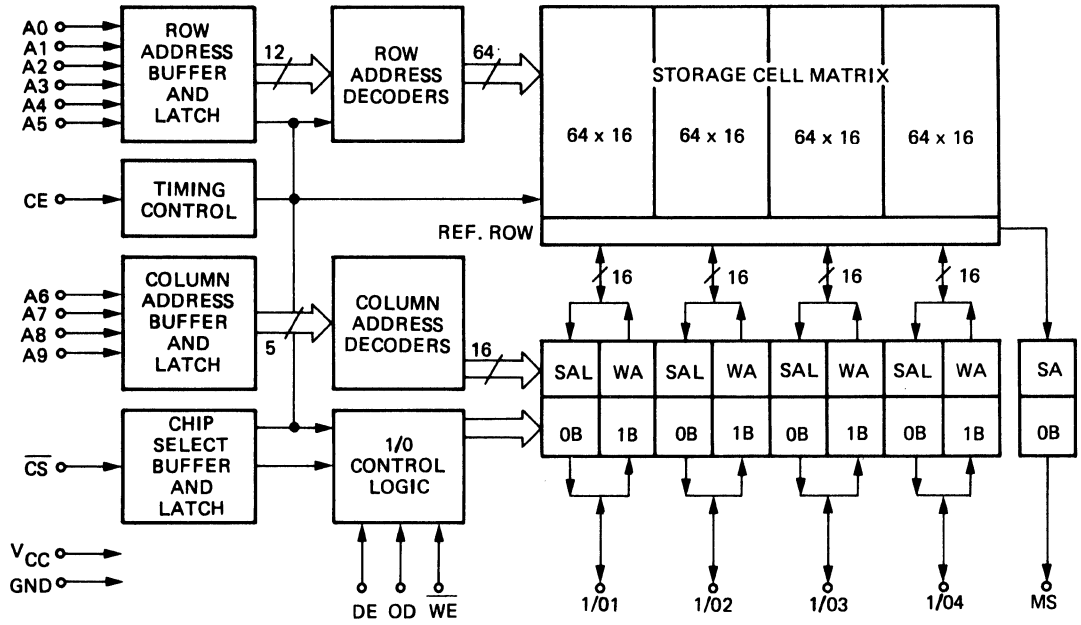
All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power schottky loads.

Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write. Data In and Data Out signals share common I/O pins.

Memory Status is an output signal that indicates when data is actually valid and when the preset interval is complete. It can be used to generate the CE input and to improve the memory performance.

Outputs	Inputs
High 2.4 Volts min.	High 2.0 Volts min.
Low .4 Volts max.	Low .8 Volts max.




A0
A1
A2
A3
A4
A5
ROW ADDRESS BUFFER AND LATCH
12
ROW ADDRESS DECODERS
64
STORAGE CELL MATRIX
64 x 16
64 x 16
64 x 16
64 x 16
CE
TIMING CONTROL
REF. ROW
16
16
16
16
A6
A7
A8
A9
COLUMN ADDRESS BUFFER AND LATCH
5
COLUMN ADDRESS DECODERS
16
SAL
WA
SAL
WA
SAL
WA
SAL
WA
SA
0B
1B
0B
1B
0B
1B
0B
1B
0B
CS
CHIP SELECT BUFFER AND LATCH
1/0 CONTROL LOGIC
VCC
GND
DE
OD
WE
1/01
1/02
1/03
1/04
MS

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0390

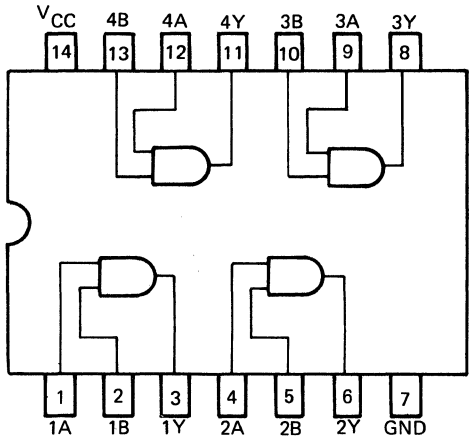
Integrated Circuit

Element Type: CMOS
Standard Number: 74C08
Circuit Designation: Quad 2-input AND gate

Description of Operation:

This package contains four 2-input AND gates. They perform the function AB = Y where A and B are the inputs and Y is the output. Both A and B must be high to result in a high at Y.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.0 - 3.5 Volts
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0408

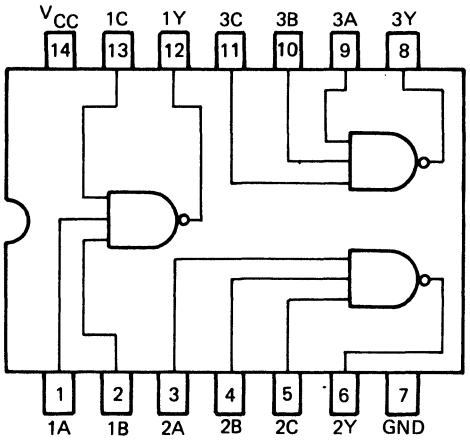
Integrated Circuit

Element Type: CMOS
Standard Number: 74C10
Circuit Designation: Triple 3-input NAND

Description of Operation:

This package contains three 3-input NAND gates. They perform the function ABC = $\overline{Y}$ where A, B, and C are inputs and Y is the output. If any input is low, the output is high.

Outputs	Inputs
High 4.4 - 4.5 Volts	High 3.0 - 3.5 Volts
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0432

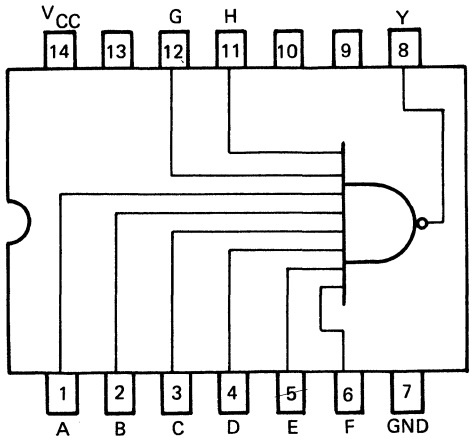
Integrated Circuit

Element Type: CMOS
Standard Number: 74C30
Circuit Designation: 8-input NAND gate

Description of Operation:

This package contains one 8-input NAND gate. It performs the function ABCDEFGH = $\overline{Y}$ where A, B, C, D, E, F, G, and H are inputs and Y is the output. If any input is low, the output is high.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.0 - 3.5 Volts
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0440

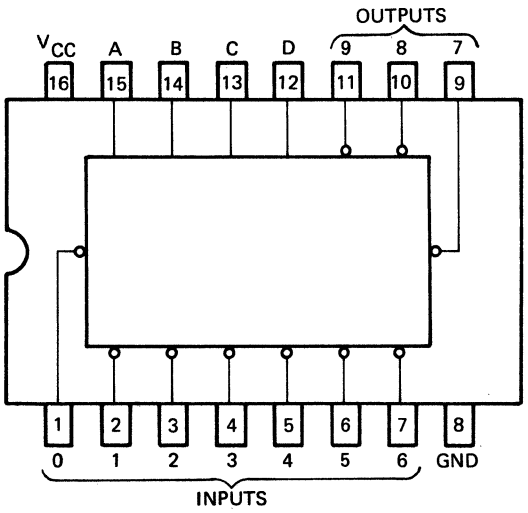
Integrated Circuit

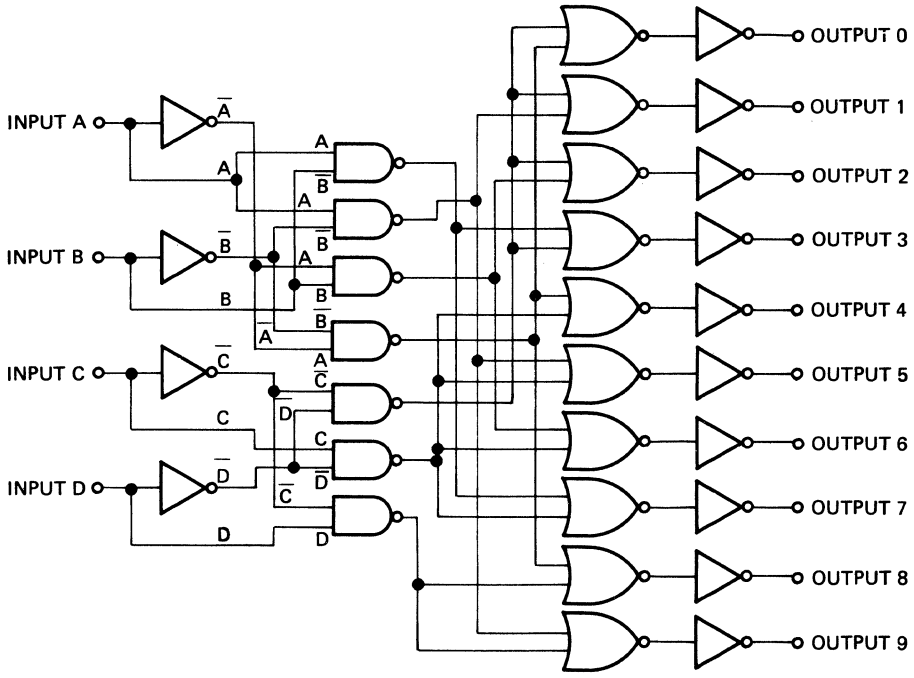
Element Type:	CMOS
Standard Number:	74C42
Circuit Designation:	BCD to decimal decoder

Description of Operation:

This package contains one binary coded decimal input to decimal output decoder. This decoder produces a logical low at the output corresponding to a four bit binary input from zero to nine, and a logical high at the other outputs. For binary inputs from ten to fifteen, all outputs are logical high.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.5 Volts min.
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts max.





Logic Equation/Truth Table

Inputs				Outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0457

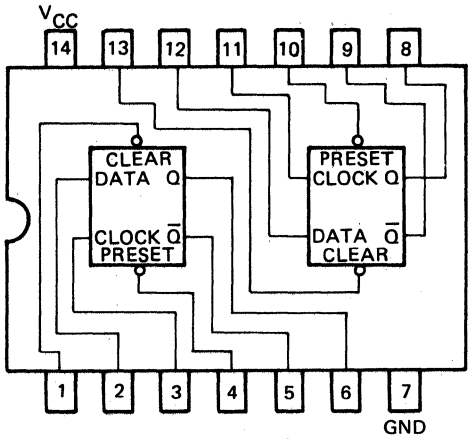
Integrated Circuit

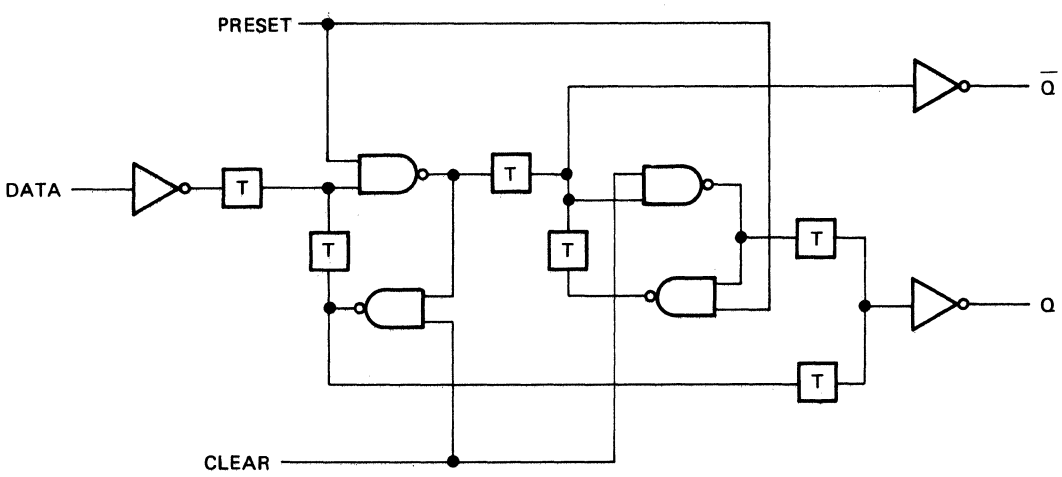
Element Type:	CMOS
Standard Number:	74C74
Circuit Designation:	Dual D flip-flop

Description of Operation:

This package contains two D type flip-flops. Each flip-flop has independent data, preset, clear and clock inputs and Q and Q outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input. A logic low on the clear input sets Q to a logic low. A logic low on the preset input sets Q to a logic high.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.5 Volts min.
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 max.





LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0481

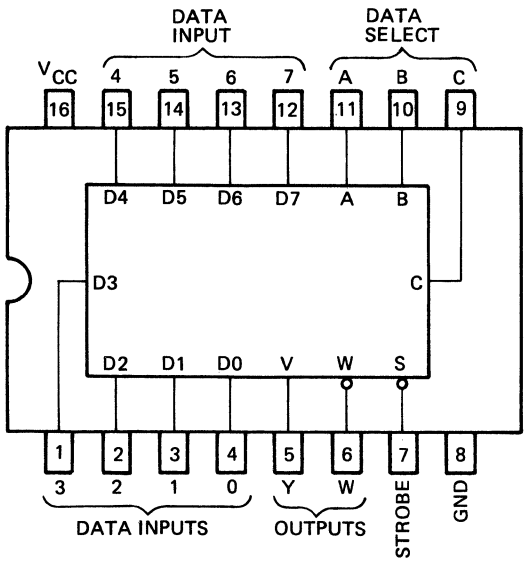
Integrated Circuit

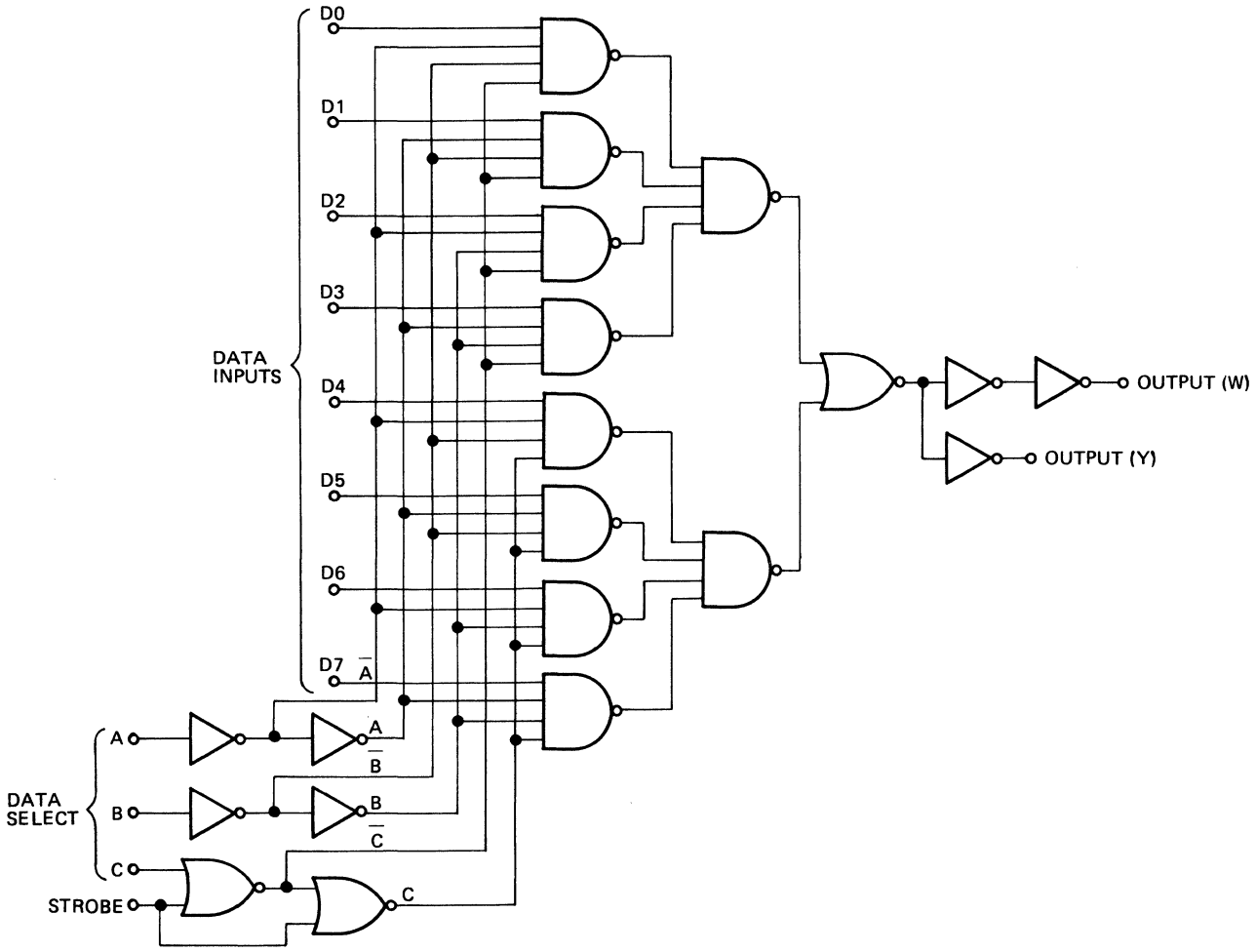
Element Type: CMOS
Standard Number: 74C151
Circuit Designation: 8 Channel digital multiplexer

Description of Operation:

This package contains one 8 channel digital multiplexer. When the strobe input is low, the multiplexer decodes the binary value of the data select inputs and gates that value data bit to output Y. The output on W will be the complement of the selected input. If the strobe is high, the output Y will be low and the output W will be high.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.0 - 3.5 Volts
Low 0.4 - 0.5 Volts	Low .4 - 1.5 Volts





Logic Equation/Truth Table

Inputs												Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

1 = high
0 = low

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0499

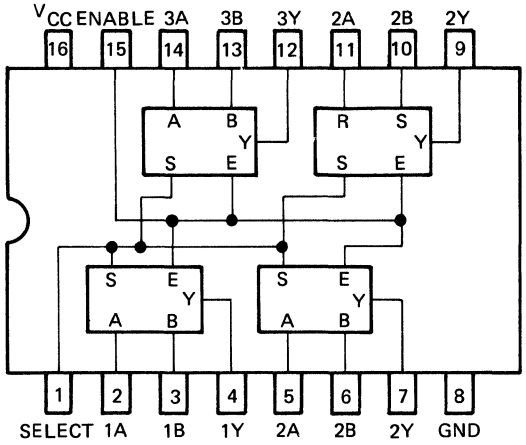
Integrated Circuit

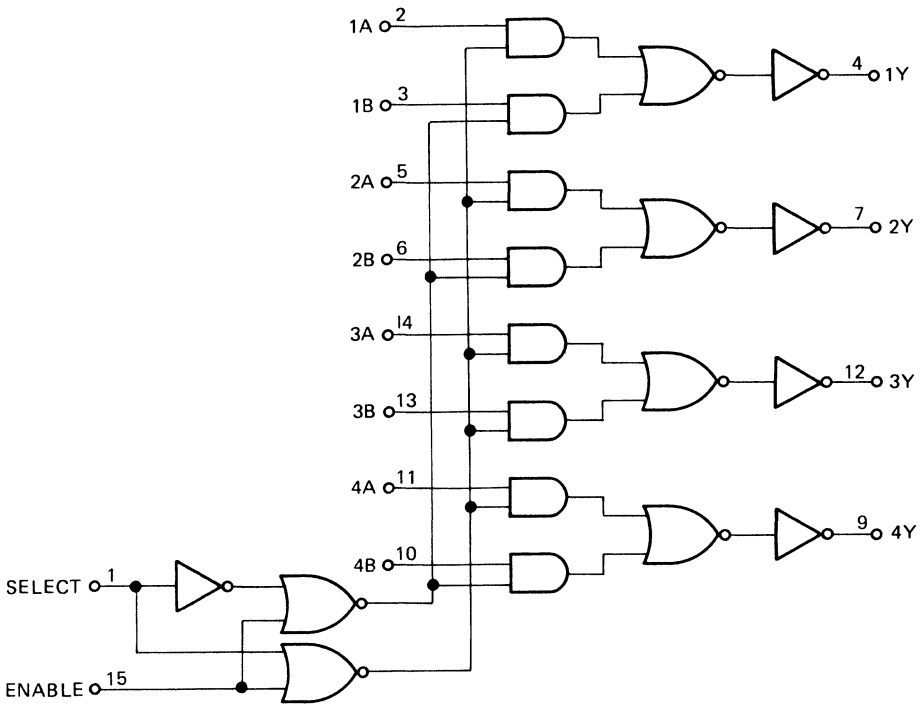
Element Type: CMOS
Standard Number: 74C157
Circuit Designation: Quad 2-input multiplexer

Description of Operation:

This package contains a data multiplexer which selects a 4-bit word from one of two sources and routes it to the four outputs. An enable input is provided. All outputs are held low when the enable is high. With enable low, A input is gated to the output with select low. With enable low, B input is gated to the output with select high.

Outputs	Inputs
High 2.5 - 4.5 Volts	High 3.0 - 3.5 Volts
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts





Logic Equation/Truth Table

Enable	Select	A	B	Output Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	0	L
L	H	X	1	H

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0507

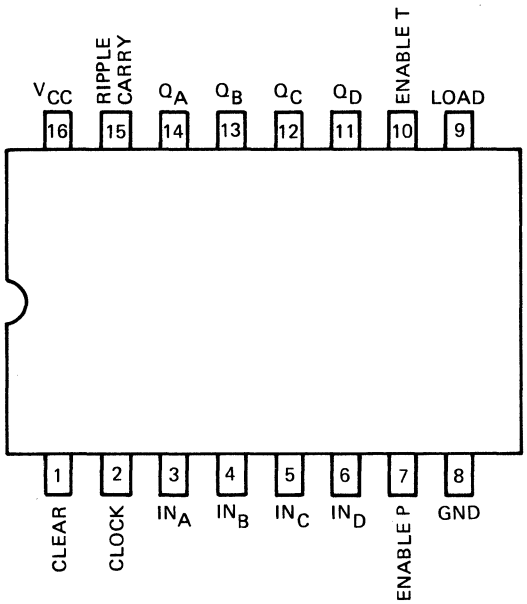
Integrated Circuit

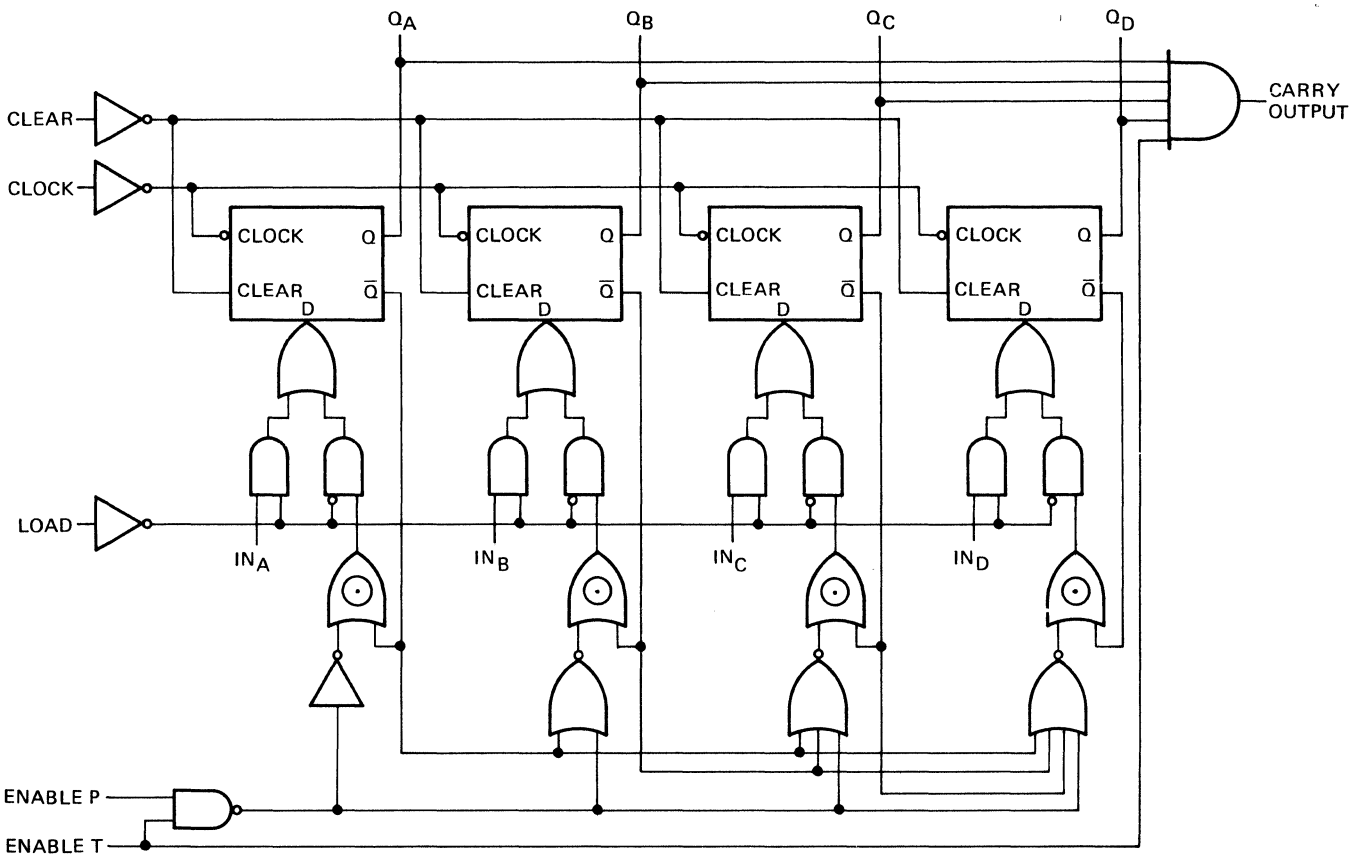
Element Type: CMOS
Standard Number: 74C163
Circuit Designation: Binary counter

Description of Operation:

This package contains one binary counter with synchronous clear capability. A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function is synchronous and a low level at the clear inputs sets all four outputs low after the next positive clock edge. Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Outputs	Inputs
High 4.5 Volts	High 3.5 Volts min.
Low 0.5 Volts	Low 1.5 Volts max.




Q_A
Q_B
Q_C
Q_D
CARRY OUTPUT
CLEAR
CLOCK
CLOCK
Q
CLEAR
$\overline{Q}$
D
LOAD
IN_A
IN_B
IN_C
IN_D
ENABLE P
ENABLE T

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0515

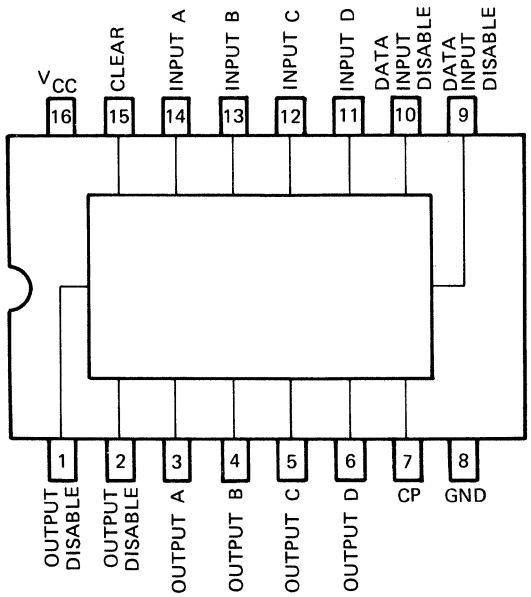
Integrated Circuit

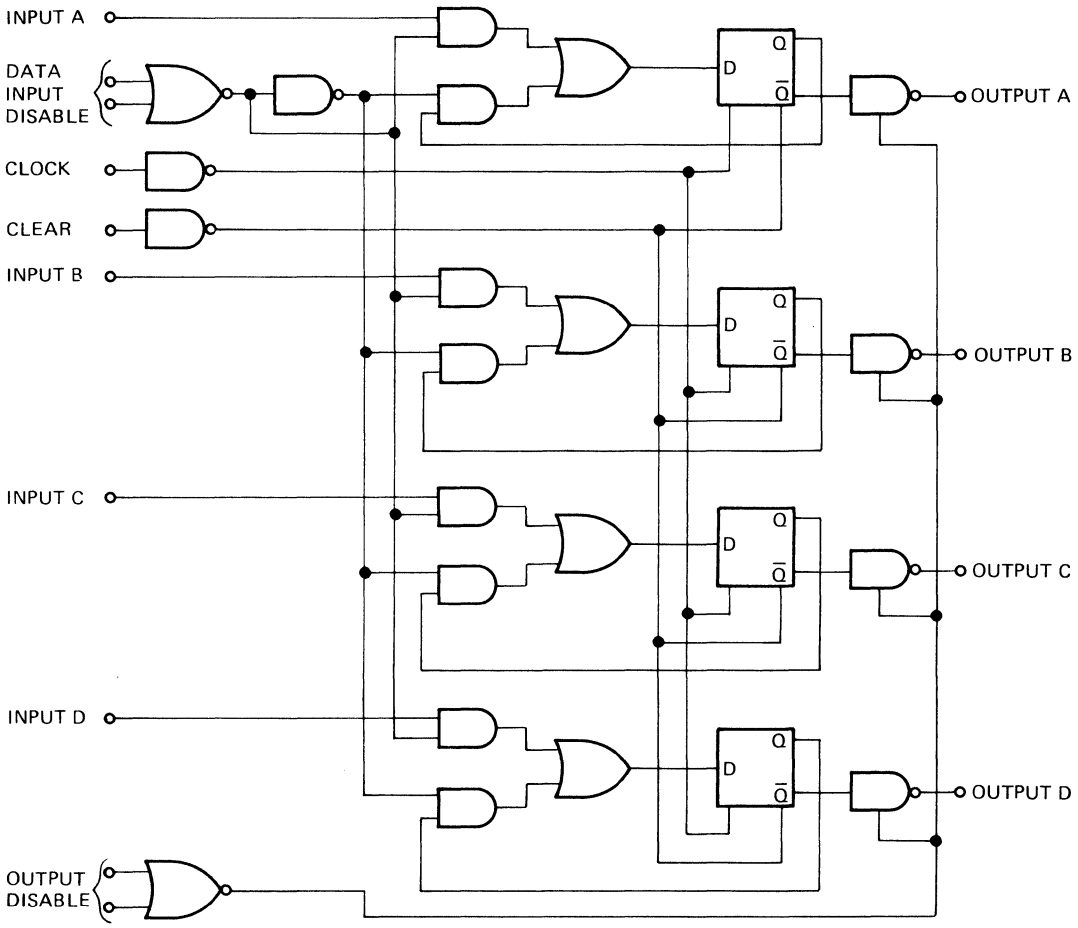
Element Type: CMOS
Standard Number: 74C173
Circuit Designation: Tri-state Quad D flip-flop

Description of Operation:

This package contains four tri-state D flip-flop circuits. The four D type flip-flops operate synchronously from a common clock. The tri-state output allows the device to be used in bus organized systems. The outputs are placed in the tri-state mode when either of the two output disable pins are in the logic high level. The input disable allows the flip-flop to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic high level, the Q outputs are fed back to the inputs and in this manner, the flip-flops do not change state. Clearing is enabled by taking the input to a logic high level. Clocking occurs on the positive going transition.

Outputs	Inputs
High 3.5 Volts min.	High 3.5 Volts min.
Low 0.5 Volts max.	Low 1.5 Volts max.





Logic Equation/Truth Table (Both Output Disables Low)

Data Input Disable	Data Input	Output
Logic high on one or both inputs	X	Q_n
Logic low on both inputs	H	H
Logic low on both inputs	L	L

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0523

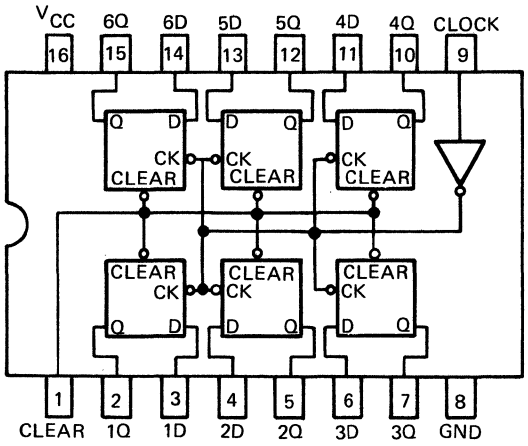
Integrated Circuit

Element Type: CMOS
Standard Number: 74C174
Circuit Designation: Hex D flip-flop

Description of Operation:

This package contains 6 hex D flip-flop circuits. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.5 Volts min.
Low 0.4 - 0.5 Volts	Low 0.9 - 1.5 Volts max.



Truth Table

Inputs			Output
Clear	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0549

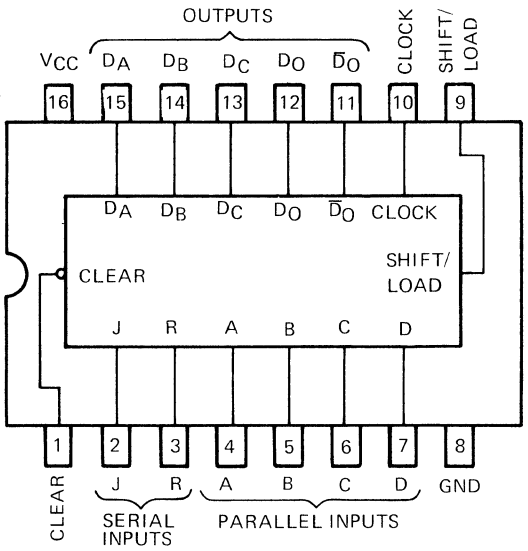
Integrated Circuit

Element Type: CMOS
Standard Number: 74C195
Circuit Designation: 4-Bit register

Description of Operation:

This package contains one 4-bit register that may operate in a parallel input (output or serial input/output mode). Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. During parallel loading, serial data flow is inhibited. Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$, D or T-type flip-flop as shown in the truth table.

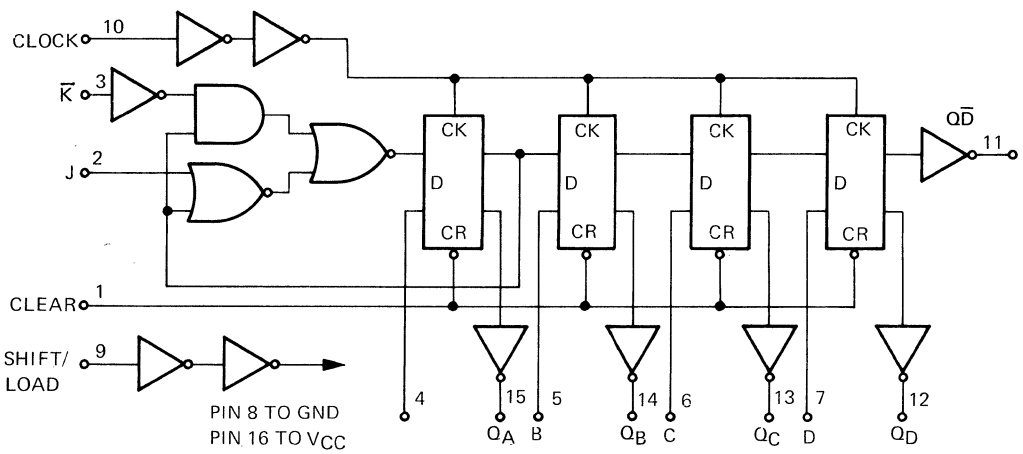
Outputs	Inputs
High 2.4 - 4.5 Volts	High 3.5 Volts min.
Low 0.4 - 0.5 Volts	Low 0.8 - 1.5 Volts max.



Truth Table

J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note: H = High level,
L = Low level



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0556

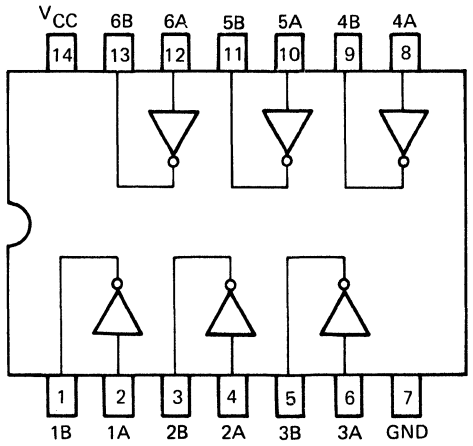
Integrated Circuit

Element Type:	CMOS
Standard Number:	74C901
Circuit Designation:	Hex inverting TTL buffer

Description of Operation:

This package contains six hex buffer circuits. They perform the function $\overline{A} = B$ where A is any input and B is any output. A high level at A will result in a low level at B.

Outputs	Inputs
High 4.5 Volts	High 3 Volts min.
Low 0.5 Volts	Low 0.5 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0564

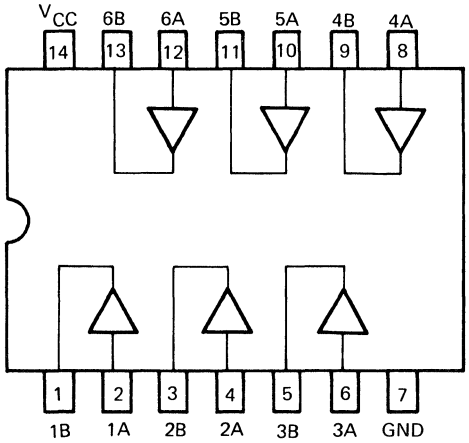
Integrated Circuit

Element Type:	CMOS
Standard Number:	74C902
Circuit Designation:	Hex non-inverting TTL buffer

Description of Operation:

This package contains six hex buffer circuits. They perform the function A = B. Where B is any output and A is any input, a high level at A will result in a high level at B.

Outputs	Inputs
High 4.5 Volts	High 3 Volts min.
Low 0.5 Volts	Low 0.5 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0572

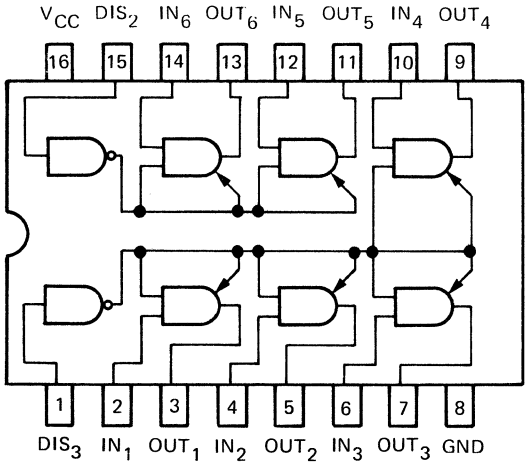
Integrated Circuit

Element Type: CMOS
Standard Number: 80C97
Circuit Designation: Tristate hex non-inverting buffers

Description of Operation:

This package contains six tristate hex non-inverting buffer circuits. They are in two groups. One group contains 2 buffers enabled by one control line. The other group contains 4 buffers enabled by a separate control line. A high level at the control line disables the buffer and places its output in a high impedance state.

Outputs	Inputs
High 2.4 Volts	High 3 Volts
Low 0.5 Volts	Low 0.8 max.



Truth Table

Disable Input		Input	Output
DIS_4	DIS_2		
L	L	L	L
L	L	H	H
X	H	X	H-z*
H	X	X	H-z**

*Output 5 - 6 only
**Output 1 - 4 only
X=Irrelevant

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0580

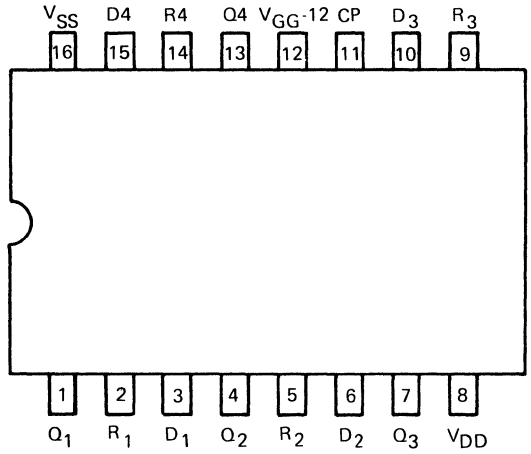
Integrated Circuit

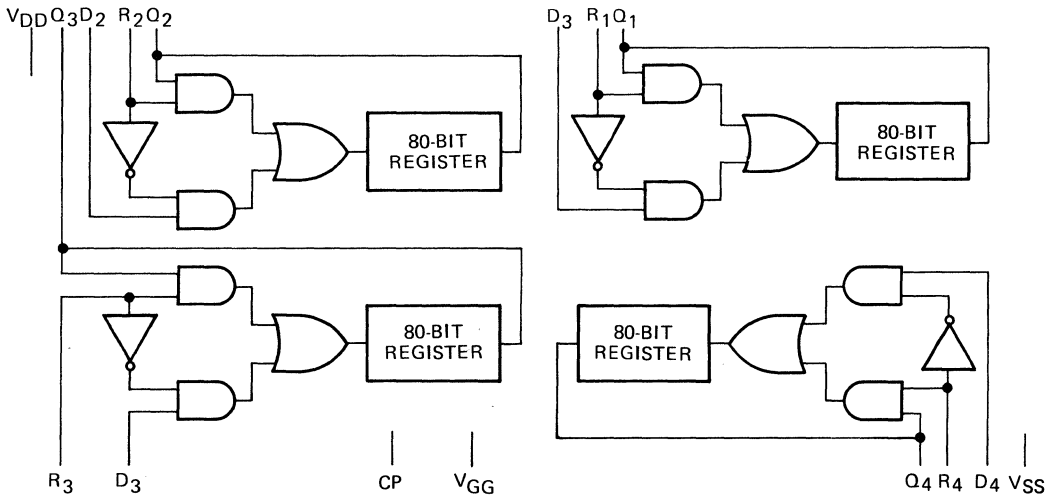
Element Type: PMOS
Standard Number: 33572
Circuit Designation: Quad, 80-bit static shift register

Description of Operation:

This package contains one single phase Quad 80-bit static shift register. Data is loaded into the register on the negative transition of the external clock. The recirculate input choose-between loading new data from the input or recirculating old data from the output. A low on recirculate loads data from the input, and a high loads data from the output.

Outputs	Inputs
High 4.0 Volts min.	High 4.0 Volts min.
Low 0.4 Volts max.	Low 0.8 Volts max.





LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0598

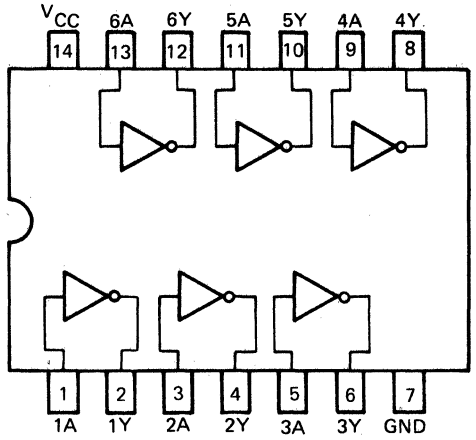
Integrated Circuit

Element Type:	TTL (low power schottky)
Standard Number:	74LS05
Circuit Designation:	Hex inverter w/open collector outputs

Description of Operation:

This package contains six inverters. The outputs are open collectors and can therefore be wire-ended with other open collector or tristate outputs.

Outputs	Inputs
High 2.7 Volts min.	High 2 Volts min.
Low .5 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0606

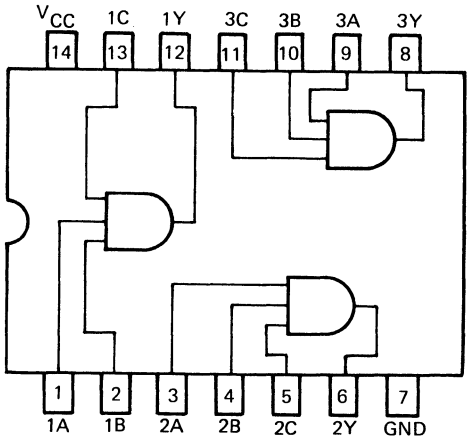
Integrated Circuit

Element Type:	TTL (low power schottky)
Standard Number:	74LS11
Circuit Designation:	Triple 3 input AND gate

Description of Operation:

This package contains three 3-input AND gates. The gates perform the function ABC = Y. A, B, and C are inputs and Y is the output. A high level on A, B, and C is required to produce a high level at Y, otherwise the result at Y is low.

Outputs	Inputs
High 2.7 Volts min.	High 2 Volts min.
Low .5 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0614

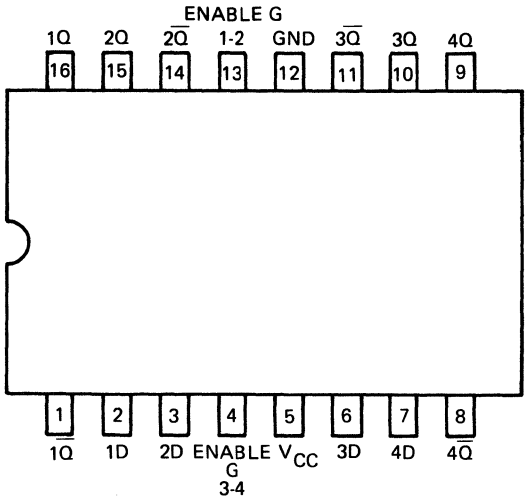
Integrated Circuit

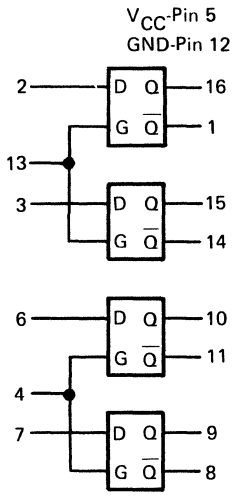
Element Type: TTL (low power schottky)
Standard Number: 74LS75
Circuit Designation: Quad D-type positive edge flip-flop

Description of Operation:

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 2.7 min.
Low .5 max.	Low .8 max.





Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0630

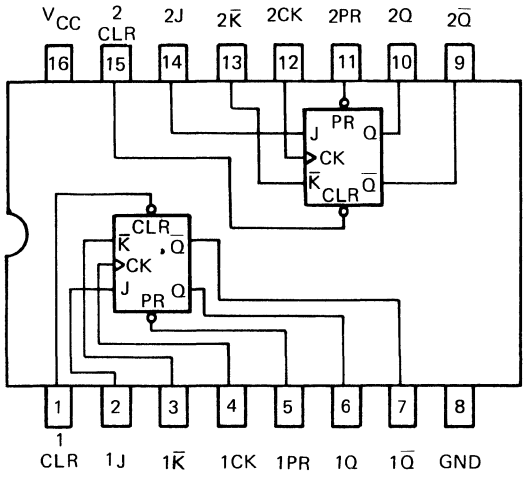
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 74LS109
Circuit Designation: Dual J-K positive edge flip-flop

Description of Operation:

A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Follow-int the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. The J and $\overline{K}$ data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and $\overline{K}$ inputs together.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 2.7 min.
Low 0.5 max.	Low .8 max.



Truth Table

Inputs					Outputs	
Preset	**Clear**	**Clock**	**J**	**$\overline{K}$**	**Q**	**$\overline{Q}$**
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not presist when preset and clear inputs return to their inactive (high) level.

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0648

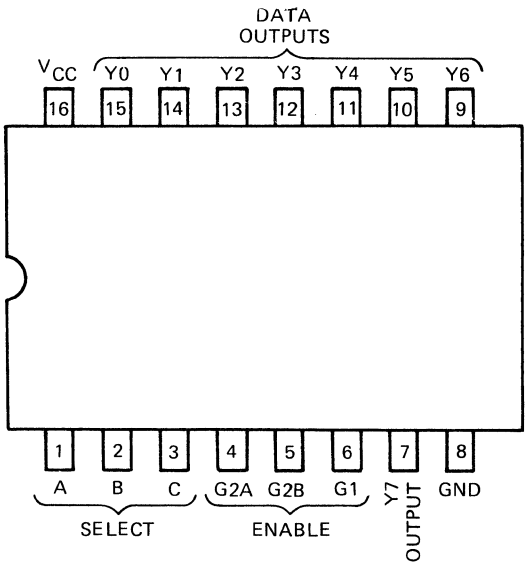
Integrated Circuit

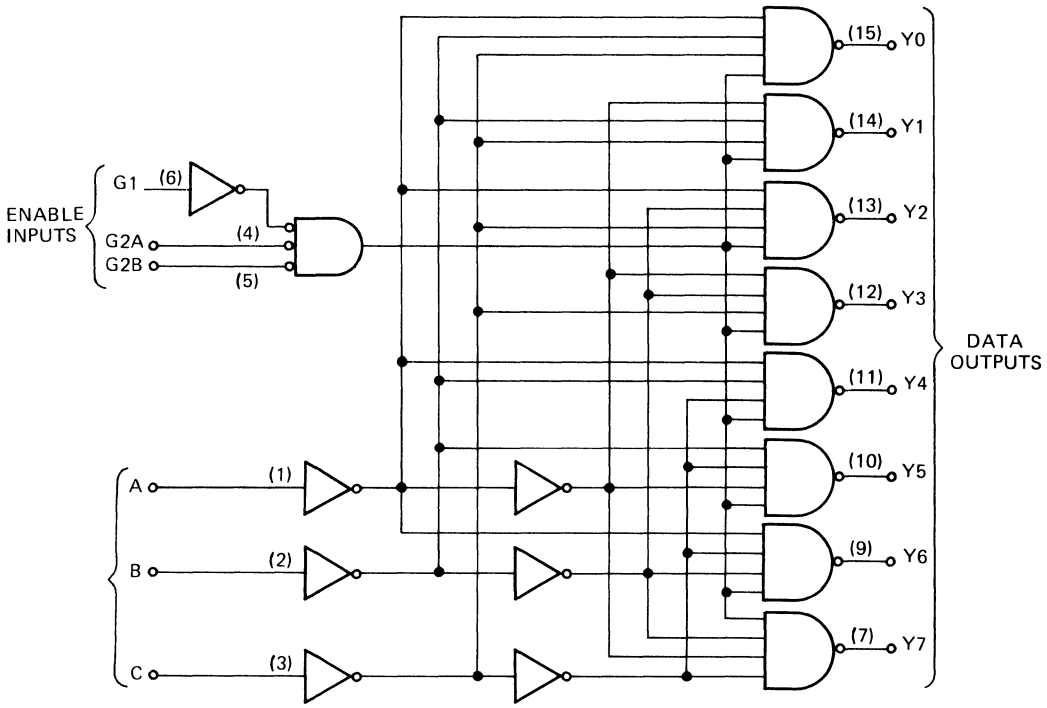
Element Type:	TTL (low power schottky)
Standard Number:	74LS138
Circuit Designation:	3 to 8 line decoder

Description of Operation:

This package contains one 3 to 8 line decoder. If either of the enable inputs G2A or G2B is high, all Y outputs will be high. If the enable input, G1, is low, all Y outputs will be high. If enable inputs are: G1 high, G2A and G2B low; the output Y_n will be low corresponding to the binary value of the select inputs.

Outputs	Inputs
High 2.7 to 3.4 Volts	High 2.0 Volts min.
Low 0.35 to 0.5 Volts	Low 0.8 Volts max.





Truth Table

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0655

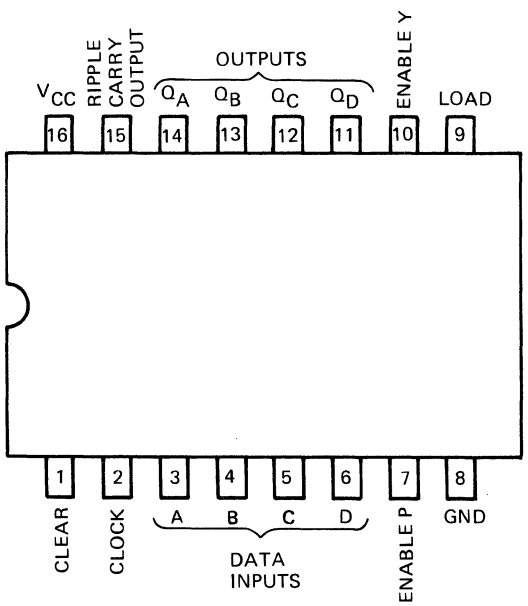
Integrated Circuit

Element Type:	TTL (low power schottky)
Standard Number:	74LS163
Circuit Designation:	Synchronous 4-bit binary counter

Description of Operation:

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms. This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

Outputs	Inputs
High 2.7 Volts min.	High 2.0 min.
Low .5 Volts max.	Low .8 max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0663

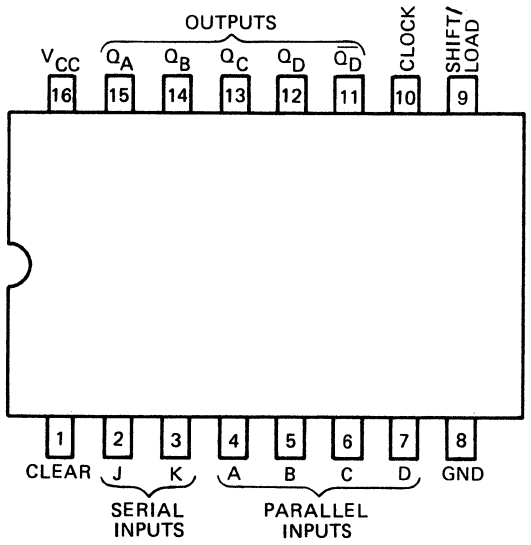
Integrated Circuit

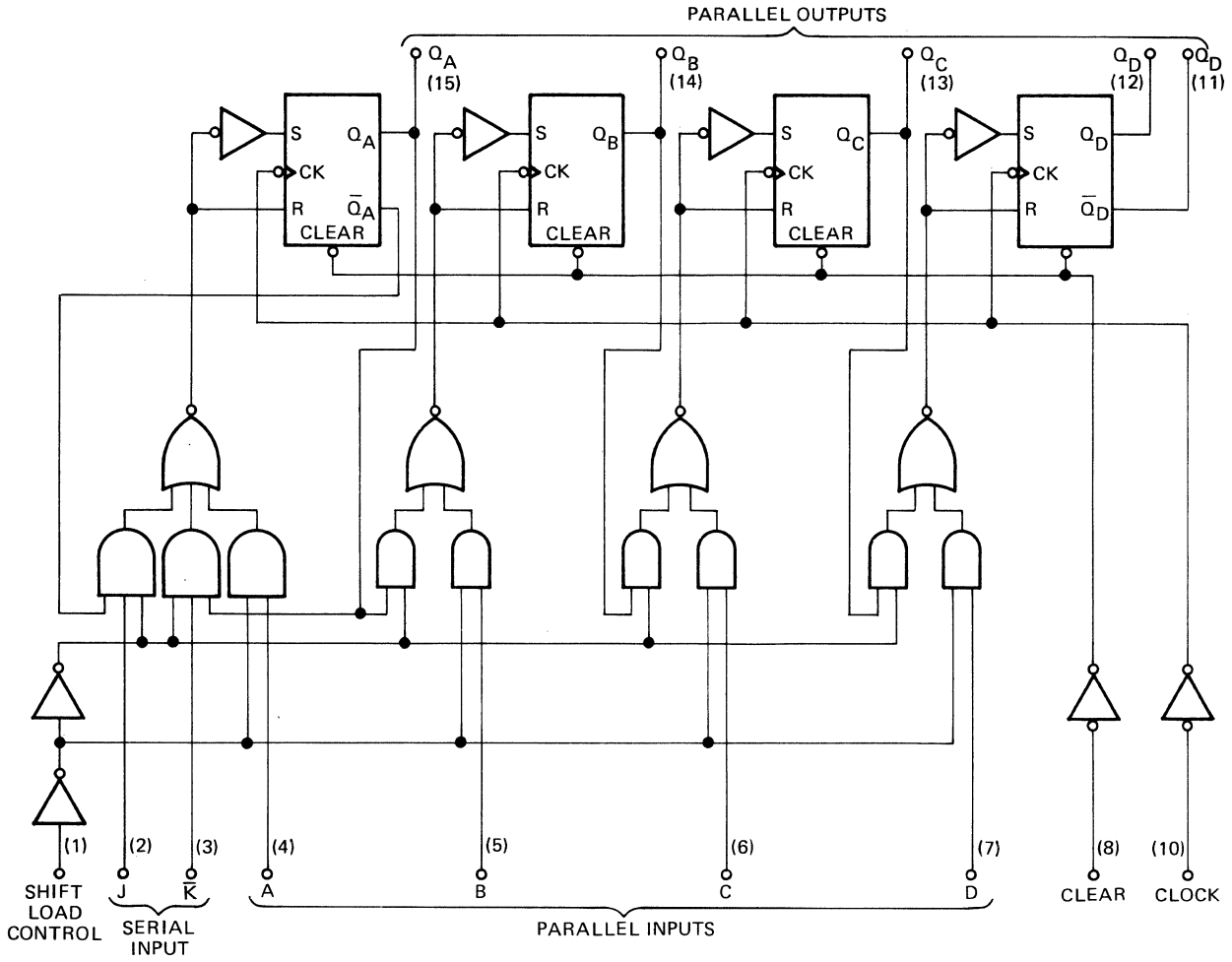
Element Type:	TTL (low power schottky)
Standard Number:	74LS195
Circuit Designation:	4-Bit parallel access shift register

Description of Operation:

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation: Parallel (broadside) load; Shift (in direction Q_A toward Q_D). Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

Outputs	Inputs
High 2.7 Volts min.	High 2.0 Volts min.
Low .5 Volts max.	Low .8 Volts max.





Logic Equation/Truth Table

Inputs									Outputs				
			Serial		Parallel								
Clear	Shift/ Load	Clock	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	d
H	H	L	X	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	$\overline{Q}_{DO}$
H	H	↑	L	H	X	X	X	X	Q_{AO}	Q_{AO}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clock.

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0689

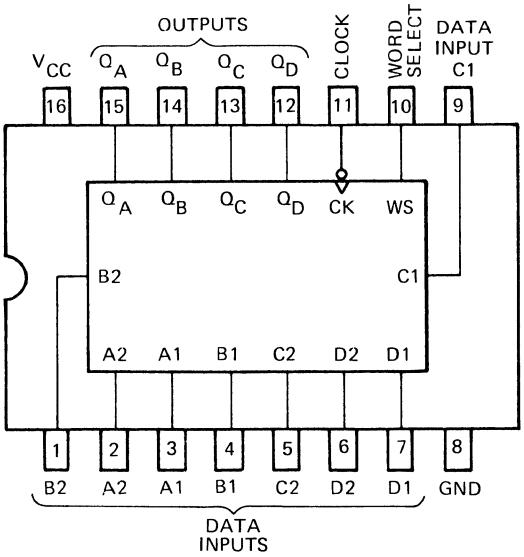
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 74LS298
Circuit Designation: Quad 2-input multiplexer register

Description of Operation:

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

Outputs	Inputs
High 2.4 - 4.5 Volts	High 2.7 min.
Low 0.4 - 0.5 Volts	Low .8 max.



Logic Equation/Truth Table

Inputs		Outputs			
Word Select	**Clock**	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{AO}	Q_{BO}	A_{CO}	Q_{DO}

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0697

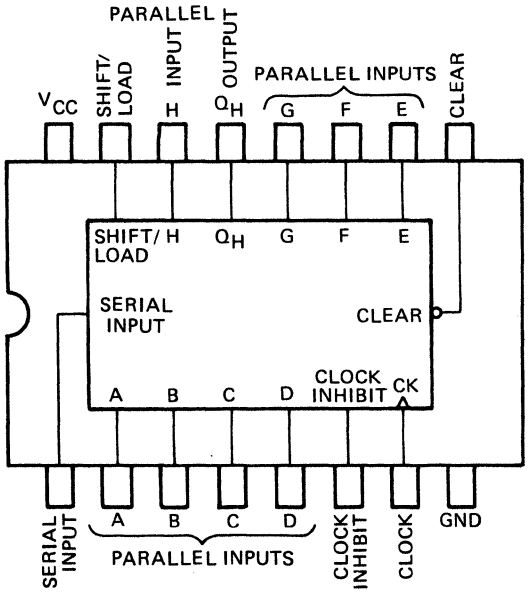
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 74166
Circuit Designation: 8-Bit shift register

Description of Operation:

This parallel-in or serial-in, serial-out shift registers features gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Outputs	Inputs
High 2.4 Volts min.	High 2 Volts min.
Low .4 Volts max.	Low .8 Volts max.



Logic Equation/Truth Table

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	L	↑	X	a . . . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = High level (steady state)
L = low level (steady state)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G, respectively, before the most-recent ↑ transition of the clock.

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0705

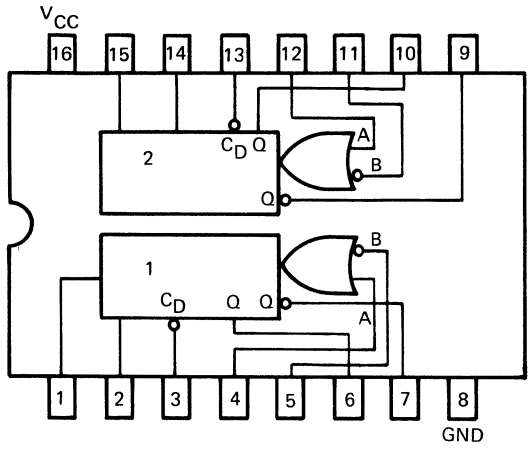
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 96L02
Circuit Designation: Dual monostable multivibrator

Description of Operation:

The 96L02 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active low and one active high. This allows leading edge of trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 96L02 and result in a continuous true output. The output pulse may be terminated at any time by connecting the reset pin to a logic level low. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying the Q output to the active level low input or the Q output to the active level high input.

Outputs	Inputs
High 2.4 Volts min.	High 2.0 Volts min.
Low .3 Volts max.	Low .7 Volts max.



Truth Table

Pin No's.			Operation
5(11)	4(12)	3(13)	
H L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = high voltage
L = low voltage
X = don't care (either H or L)
H→L = high to low voltage level transition
L→H = low to high voltage level transition

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0713

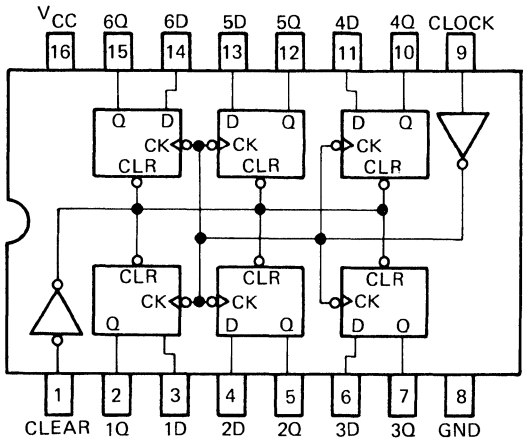
Integrated Circuit

Element Type: TTL (low power schottky)
Standard Number: 74S174
Circuit Designation: Hex D-type Flip-Flop with Clear

Description of Operation:

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the input signal has no effect at the output.

Outputs	Inputs
High 2.7 Volts min.	High 2.0 Volts min.
Low .5 Volts max.	Low .8 Volts max.



Truth Table

Inputs			Outputs
Clear	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_O

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_O = the level of Q before the steady-state input conditions were established

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0721

Integrated Circuit

Element Type: TTL
Standard Number: 8T13
Circuit Designation: Dual Line Driver

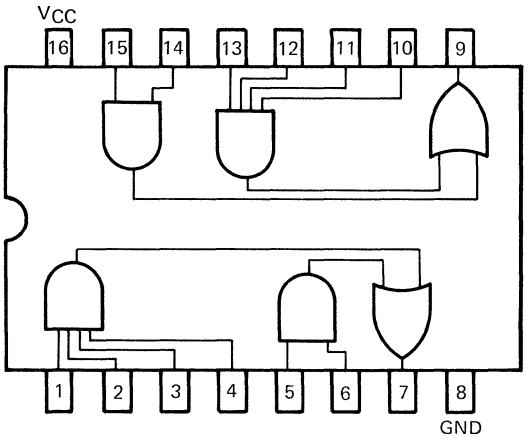
Description of Operation:

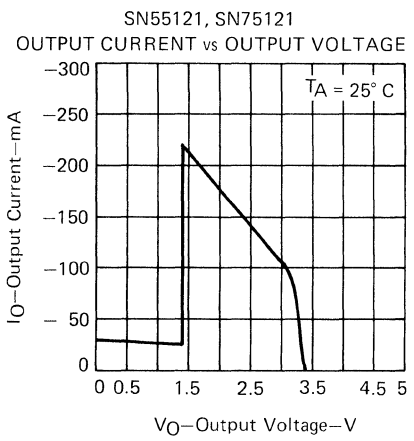
The 8T13 is a monolithic Dual Line Driver designed to drive 50 Ohm or 75 Ohm coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The outputs are designed to drive long lengths of coaxial cable, strip line or twisted pair transmission lines with impedences of 50Ω to 500Ω .

Outputs

Inputs

High 2.0 Volts min.
Low .8 Volts max.





LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0739

Integrated Circuit

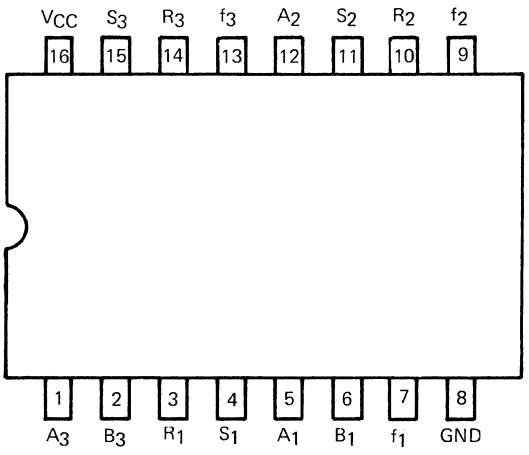
Element Type: TTL
Standard Number: 8T14
Circuit Designation: Triple Line Receiver

Description of Operation:

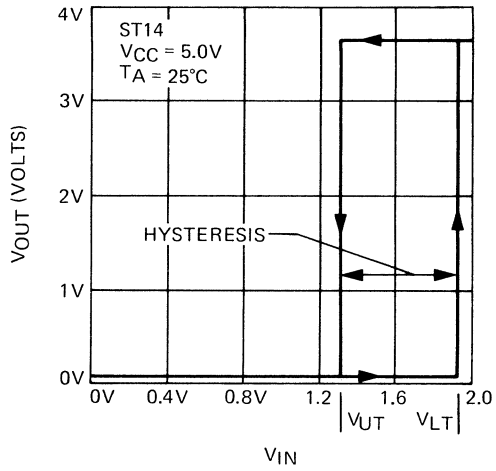
The 8T14 is a Triple Line Receiver designed for applications requiring digital information to be transmitted over long lengths of coaxial cable, strip line, or twisted pair transmission lines. The Receiver's high impedance input structure (-30kΩ) presents a minimal load to the driver circuit and allows the transmission to be terminated in its characteristic impedance to minimize line reflections.

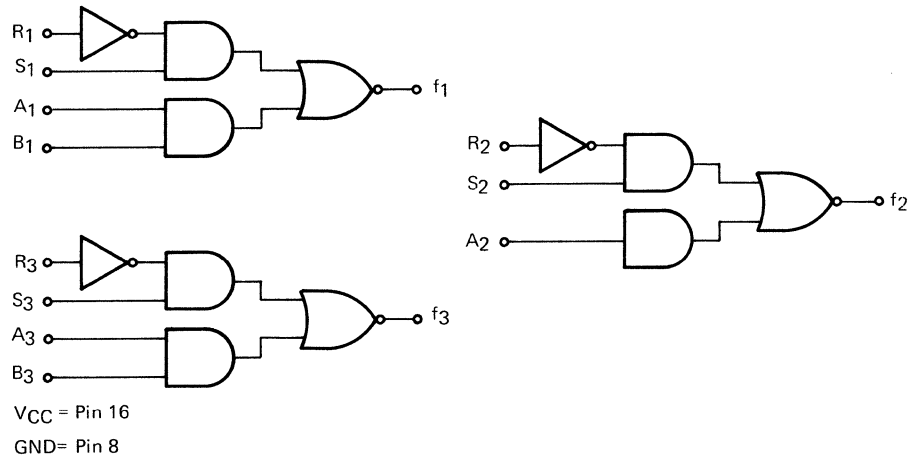
The built-in hysteresis characteristic of the 8T14 also makes it ideal for such applications as Schmitt triggers, one-shots and oscillators.

Outputs	Inputs (S, A, B)
High 2.7 Volts min.	High 2.0 Volts min.
Low .5 Volts max.	Low .8 Volts max.



R - Input Hysteresis





LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0853

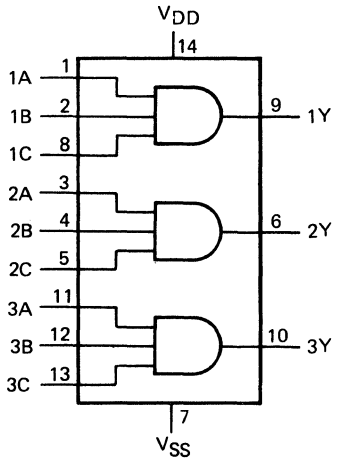
Integrated Circuit

Element Type: CMOS
Standard Number: CD4073B
Circuit Designation: Triple 3-input AND gate

Description of Operation:

This package contains three 3-input AND gates. The gates perform the function ABC = Y where A, B, and C are the inputs and Y is the output. A low level on A, B, or C results in a low level output. All inputs, A, B, and C, must be high to produce a high output level.

Outputs	Inputs
High 4.95 Volts max.	High 1.5 to 2.25 Volts
Low 0.05 Volts	Low .5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0879

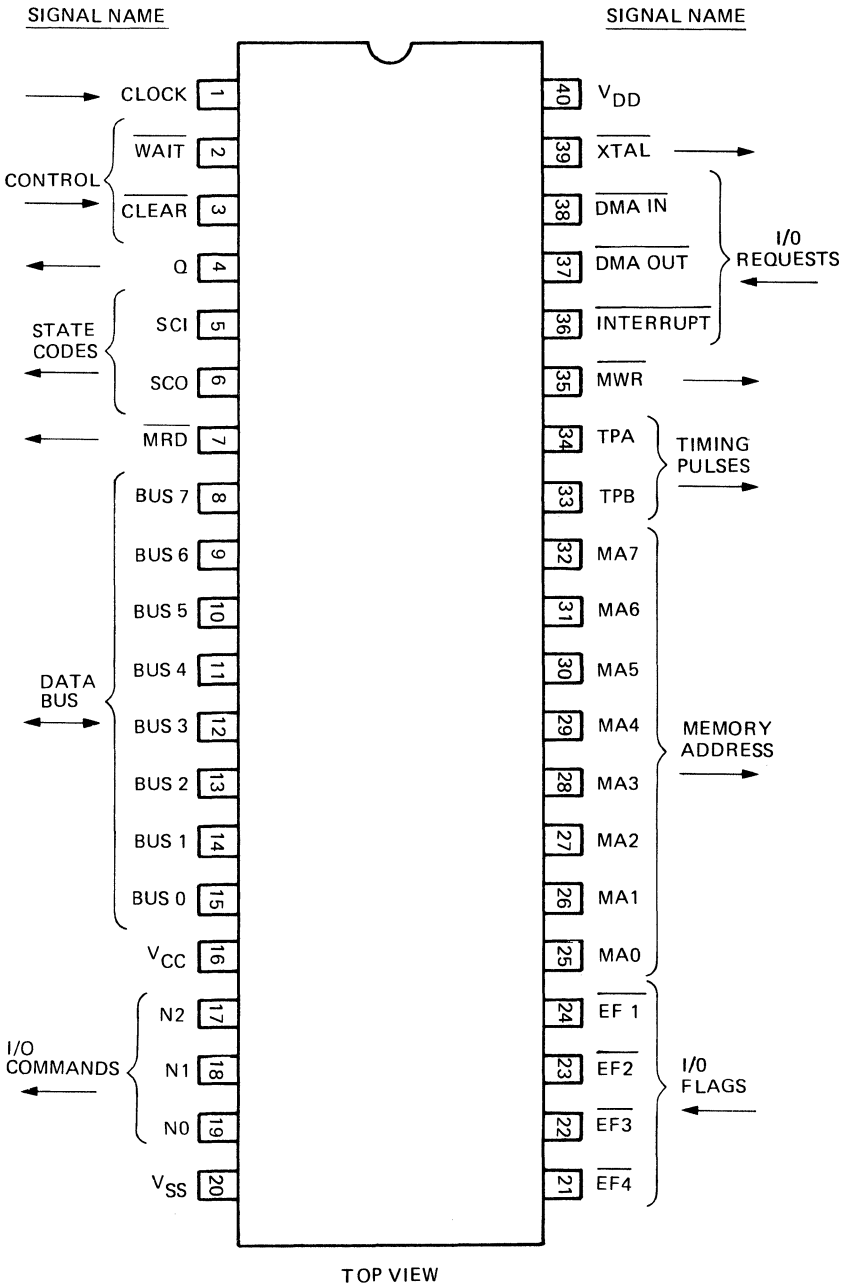
Integrated Circuit

Element Type: CMOS
Standard Number: 1802D
Circuit Designation: 8-bit Microprocessor

Description of Operation:

The RCA-CDP1802 is an LSI COS/MOS 8-bit register-oriented central-processing unit (CPU) designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

Outputs	Inputs
High 4.5 Volts min.	High 3.5 Volts min.
Low .5 Volts max.	Low 1.5 Volts max.



Instruction Summary

The COSMAC instruction summary is given in Table 3-2. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers, bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)
N0 = Least significant Bit of N Register

Operation Notation

M(R(N)) → D; R(N) + 1

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

Table 3-2. Instruction Summary (by Class of Operation)

Register Operations

Instruction	Mnemonic	Op Code	Operation
INCREMENT REG N	INC	1N	R(N) + 1
DECREMENT REG N	DEC	2N	R(N) -1
INCREMENT REG X	IRX	60	R(X) + 1
GET LOW REG N	GLO	8N	R(N).0 → D
PUT LOW REG N	PLO	AN	D → R(N).0
GET HIGH REG N	GHI	9N	R(N).1 → D
PUT HIGH REG N	PHI	BN	D → R(N).1

Memory Reference

Instruction	Mnemonic	Op Code	Operation
LOAD VIA N	LDN	0N	M(R(N)) → D; for N not 0
LOAD ADVANCE	LDA	4N	M(R(N)) → D; R(N) + 1
LOAD VIA X	LDX	F0	M(R(X)) → D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X)) → D; R(X) + 1
LOAD IMMEDIATE	LDI	F8	M(R(P)) → D; R(P) + 1
STORE VIA N	STR	5N	D → M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D → M(R(X)); R(X) - 1

Logic Operations **

Instruction	Mnemonic	Op Code	Operation
OR	OR	F1	M(R(X)) OR D → D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D → D; R(P) + 1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D → D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D → D; R(P) + 1
AND	AND	F2	M(R(X)) AND D → D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D → D; R(P) + 1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D) → DF, 0 → MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76 *	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D) → DF, 0 → LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E *	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
RING SHIFT LEFT	RSHL		

Arithmetic Operations

Instruction	Mnemonic	OP Code	Operation
ADD	ADD	F4	M(R(X)) +D → DF, D
ADD IMMEDIATE	ADI	FC	M(R(P) +D → DF, D; R(P) + 1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF → DF, D
ADD WITH CARRY IMMEDIATE	ADCI	7C	M(R(P) +D +DF → DF, D R(P) + 1
SUBTRACT D	SD	F5	M(R(X)) -D → DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P)) -D → DF, D; R(P) + 1
SUBTRACT D WITH BORROW	SDB	75	M(R(X)) -D -(NOT DF) → DF; D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P)) -D -(NOT DF) → DF, D; R(P) + 1
SUBTRACT MEMORY	SM	F7	D -M(R(X)) → DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D -M(R(P)) → DF, D; R(P) + 1
SUBTRACT MEMORY WITH BORROW	SMB	77	D -M(R(X)) -(NOT DF) → DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D -M(R(P)) -(NOT DF) → DF, D R(P) + 1

Branch Instructions - Short Branch

Instruction	Mnemonic	OP Code	Operation
SHORT BRANCH	BR	30	M(R(P)) → R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38*	R(P) + 1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF DF = 1	BDF		
SHORT BRANCH IF POS OR ZERO	BPZ	33*	IF DF=1, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B*	IF DF=0, M(R(P)) → R(P).0
SHORT BRANCH IF MINUS	BM		ELSE R(P) + 1
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF EF1=1	B1	34	IF EF1=1, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF EF1=0	BN1	3C	IF EF1=0, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF EF2=1	B2	35	IF EF2=1, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF EF2=0	BN2	3D	IF EF2=0, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF EF3=1	B3	36	IF EF3=1, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF EF3=0	BN3	3E	IF EF3=0, M(R(P)) → R(P).0 ELSE R(P) + 1

SHORT BRANCH IF EF4=1	B4	37	IF EF4=1, M(R(P)) → R(P).0 ELSE R(P) + 1
SHORT BRANCH IF EF4=0	BN4	3F	IF EF4=0, M(R(P)) → R(P).0 ELSE R(P) + 1

Branch Instructions – Long Branch

Instruction	Mnemonic	Op Code	Operation
LONG BRANCH	LBR	C0	M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8*	R(P) + 2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P)) → R(P).1 M M(R(P) + 1) → R(P).0 ELSE R(P) + 2
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P)) → R(P).1 M(R(P) + 1) → R(P).0 ELSE R(P) + 2

Skip Instructions

Instruction	Mnemonic	OP Code	Operation
SHORT SKIP (SEE NBR)	SKP	38*	R(P) + 1
LONG SKIP (SEE NLBR)	LSKP	C8*	R(P) + 2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) + 2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) + 2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) + 2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) + 2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) + 2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) + 2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) + 2 ELSE CONTINUE

Control Instructions

Instruction	Mnemonic	OP Code	Operation
IDLE	IDL	00	WAIT FOR DMA OR INTERRUPT; M(R(0)) → BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N → P
SET X	SEX	EN	N → X
SET Q	SEQ	7B	1 → Q
RESET Q	REQ	7A	0 → Q
SAVE	SAV	7B	T → M(R(X))
PUSH X, P TO STACK	MARK	79	(X, P) → T; (X, P) → M(R(2)) THEN P → X; R(2)–1
RETURN	RET	70	M(R(X)) → (X, P); R(X) + 1 1 → IE
DISABLE	DIS	71	M(R(X)) → (X, P); R(X) + 1 0 → IE

Input–Output Byte Transfer

Instruction	Mnemonic	OP Code	Operation
OUTPUT 1	OUT 1	61	M(R(X)) → BUS; R(X) + 1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X)) → BUS; R(X) + 1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X)) → BUS; R(X) + 1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X)) → BUS; R(X) + 1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X)) → BUS; R(X) + 1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X)) → BUS; R(X) + 1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X)) → BUS; R(X) + 1; N LINES = 7
INPUT 1	INP 1	69	BUS → M(R(X)); BUS → D; N LINES = 1
INPUT 2	INP 2	6A	BUS → M(R(X)); BUS → D; N LINES = 2
INPUT 3	INP 3	6B	BUS → M(R(X)); BUS → D; N LINES = 3
INPUT 4	INP 4	6C	BUS → M(R(X)); BUS → D; N LINES = 4
INPUT 5	INP 5	6D	BUS → M(R(X)); BUS → D; N LINES = 5
INPUT 6	INP 6	6E	BUS → M(R(X)); BUS → D; N LINES = 6
INPUT 7	INP 7	6F	BUS → M(R(X)); BUS → D; N LINES = 7

NOTES:

* This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

** The arithmetic operations and the shift instructions are the only instructions that can alter the DF.

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0887

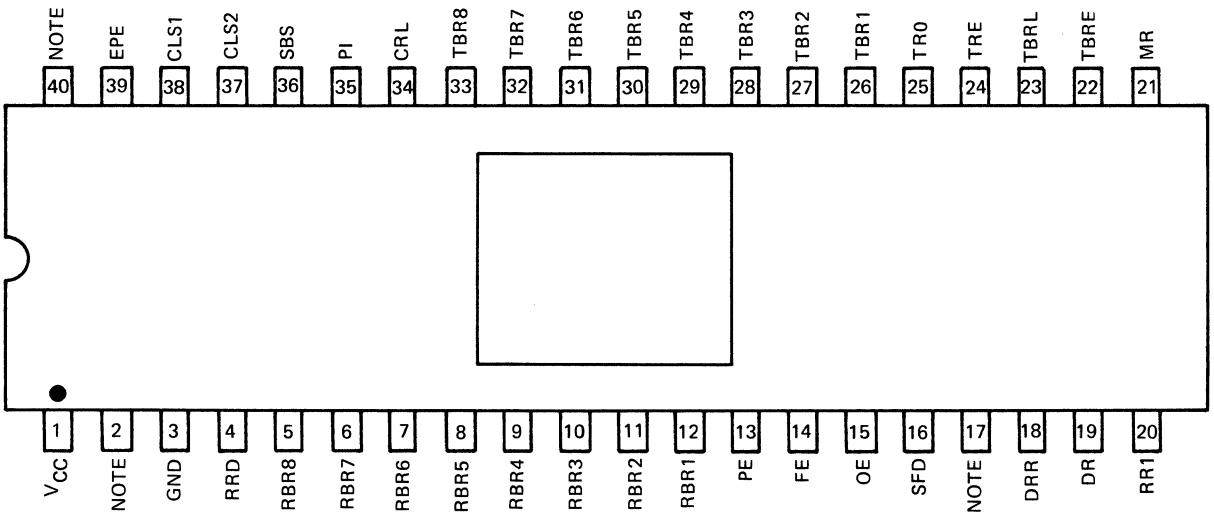
Integrated Circuit

Element Type: CMOS
Standard Number: 6402
Circuit Designation: Universal asynchronous receiver transmitter (UART)

Description of Operation:

The 6402 is a subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

Outputs	Inputs
High 4.99 Volts min. (CMOS Load)	High 3.0 Volts min.
Low .01 Volts max. (CMOS Load)	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 0895

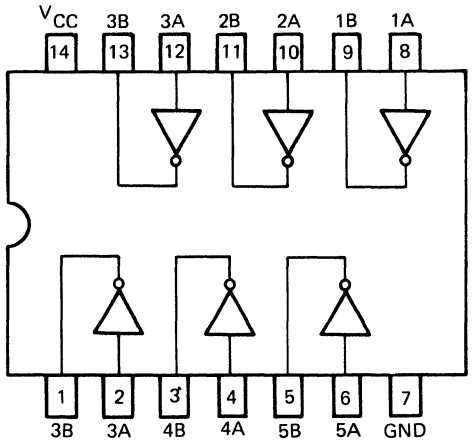
Integrated Circuit

Element Type:	CMOS
Standard Number:	74C906
Circuit Designation:	Hex open drain N-channel buffers

Description of Operation:

This package contains six invertering buffer circuits. The open drain designation means the output may be connected as a "wire OR" or "wire AND" by adding a pull-up or pull-down resistor. A high level input will result in a low level output.

Outputs	Inputs
High 5 Volts	High 3.5 Volts min.
Low 0.5 Volts	Low 1.5 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1026

Integrated Circuit

Element Type: MOS
Standard Number: 9218
Circuit Designation: 2048X8 Read only memory

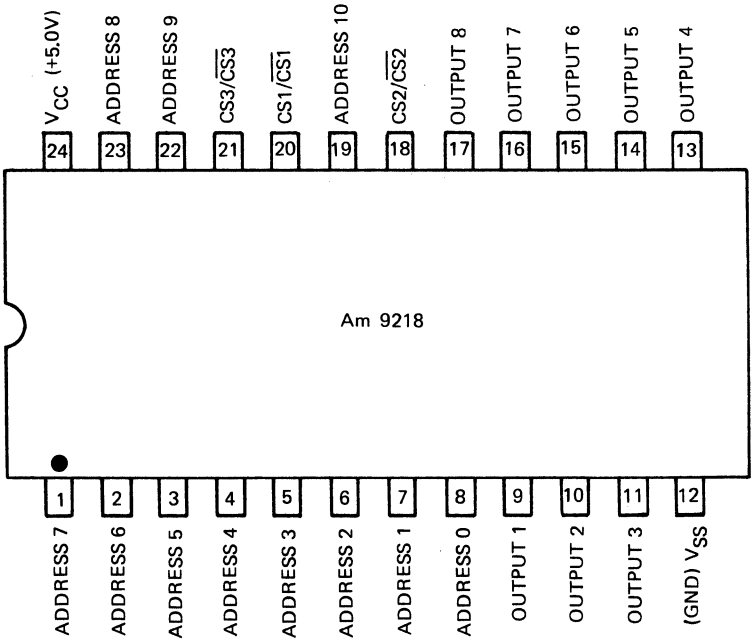
Description of Operation:

These devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer, thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire ORing with additional Am9218 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

Outputs	Inputs
High 2.4 Volts min.	High 2.0 Volts min.
Low .4 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION

(Bur.) P/N 2889 1539
(Bur.) P/N 2889 1547
(Bur.) P/N 2889 1554
(Bur.) P/N 2889 1562
(Bur.) P/N 2889 1570
(Bur.) P/N 2889 1661

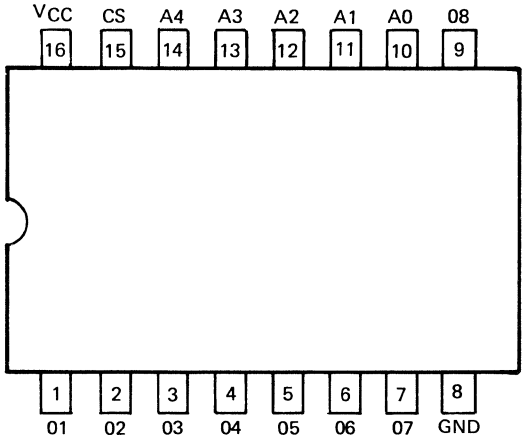
Integrated Circuit

Element Type: TTL
Standard Number: 82S123
Circuit Designation: 32 x 8 Prom (Tri-State)

Description of Operation:

This device is a 256 bit electrically programmable read only memory (Prom) organized as 32 words of 8 bits each. Tri-State outputs and a chip enable allow similar devices to be "OR" wored. Memory addressing is performed via inputs A0 through A4. To enable a read operation, the enable (chip select) must be low (logical false).

Outputs	Inputs
High 2.4 Volts min.	High 2.0 Volts min.
Low .45 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1539

ROM Contents:

Add	HEX Code
0	90
1	90
2	86
3	84
4	DB
5	90
6	86
7	84
8	8C
9	90
10	90
11	90
12	82
13	90
14	90
15	90

Add	HEX Code
16	8A
17	90
18	90
19	90
20	98
21	90
22	90
23	90
24	86
25	84
26	90
27	90
28	80
29	80
30	80
31	80

ROM Contents:

Add	HEX Code
0	B9
1	90
2	86
3	84
4	B5
5	90
6	86
7	84
8	BD
9	90
10	86
11	84
12	10
13	10
14	13
15	04

Add	HEX Code
16	DB
17	90
18	86
19	84
20	D7
21	90
22	86
23	84
24	DF
25	90
26	86
27	84
28	90
29	F1
30	86
31	84

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1554

ROM Contents:

Add	HEX Code
0	FF
1	FF
2	FF
3	FF
4	FF
5	FF
6	FF
7	FF
8	FF
9	FF
10	FF
11	FF
12	FF
13	FF
14	7D
15	7B

Add	HEX Code
16	FF
17	FF
18	FF
19	FF
20	FF
21	FF
22	FF
23	FF
24	77
25	6F
26	5F
27	FF
28	FF
29	FE
30	BF
31	FE

ROM Contents:

Add	HEX Code
0	00
1	01
2	03
3	07
4	0F
5	IF
6	3F
7	7F
8	FF
9	FF
10	FF
11	FF
12	FF
13	FF
14	FF
15	FF

Add	HEX Code
16	00
17	00
18	00
19	00
20	00
21	00
22	00
23	00
24	00
25	00
26	00
27	00
28	00
29	00
30	00
31	00

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1570

ROM Contents:

Add	Hex Code
0	80
1	80
2	80
3	80
4	80
5	80
6	80
7	80
8	80
9	81
10	83
11	87
12	8F
13	9F
14	BF
15	FF

Add	Hex Code
16	00
17	00
18	00
19	00
20	00
21	00
22	00
23	00
24	00
25	00
26	00
27	00
28	00
29	00
30	00
31	00

ROM Contents:

Add	HEX Code
0	71
1	20
2	3C
3	02
4	F8
5	04
6	B2
7	F8
8	00
9	A2
10	A9
11	69
12	B9
13	E0
14	62
15	02

Add	HEX Code
16	E2
17	19
18	61
19	22
20	35
21	14
22	69
23	12
24	99
25	3A
26	11
27	C0
28	04
29	18
30	00
31	00

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1588
(Bur.) P/N 2889 1596

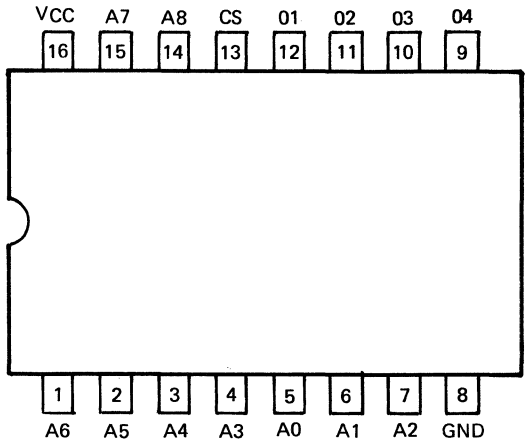
Integrated Circuit

Element Type:	TTL
Standard Number:	82S131
Circuit Designation:	512 x 4 PROM

Description of Operation:

This device is a 2048 bit electrically programmable read only memory (PROM) organized as 512 words of 4 bits each. Tri-state outputs and a chip enable allow similar devices to be "OR" wired. Memory addressing is performed via inputs A0 through AB. To enable a read operation, the enable input must be low (logical false).

Outputs	Inputs
High 2.4 Volts min.	High 2.0 Volts min.
Low .45 Volts max.	Low .8 Volts max.



ROM Content:

Add	HEX Code
0	8
1	8
2	8
3	8
4	8
5	8
6	8
7	8
8	8
9	8
10	8
11	8
12	8
13	8
14	8
15	8
16	8
17	8
18	8
19	8
20	8
21	8
22	8
23	8
24	8

Add	HEX Code
25	8
26	8
27	8
28	C
29	C
30	C
31	C
32	C
33	C
34	C
35	C
36	C
37	C
38	C
39	C
40	C
41	C
42	C
43	C
44	C
45	C
46	C
47	C
48	C
49	C

Add	HEX Code
50	C
51	D
52	D
53	D
54	D
55	D
56	D
57	D
58	F
59	F
60	F
61	F
62	F
63	F
64	F
65	F
66	F
67	F
68	F
69	F
70	F
71	F
72	F
73	F
74	F

ROM Content:

Add	HEX Code
75	F
76	F
77	F
78	F
79	F
80	F
81	F
82	F
83	F
84	F
85	F
86	F
87	F
88	F
89	F
90	F
91	F
92	F
93	F
94	F
95	F
96	F
97	F
98	F
99	F

Add	HEX Code
100	F
101	F
102	F
103	F
104	F
105	F
106	F
107	F
108	F
109	F
110	F
111	F
112	F
113	F
114	F
115	F
116	F
117	F
118	F
119	F
120	F
121	F
122	F
123	F
124	F

Add	HEX Code
125	F
126	F
127	F
128	F
129	F
130	F
131	F
132	F
133	F
134	F
135	F
136	F
137	F
138	F
139	F
140	F
141	F
142	F
143	F
144	F
145	F
146	F
147	F
148	F
149	F

ROM Content:

Add	HEX Code
150	F
151	F
152	F
153	F
154	F
155	F
156	F
157	F
158	F
159	F
160	F
161	F
162	F
163	F
164	F
165	F
166	F
167	F
168	F
169	F
170	F
171	F
172	F
173	F
174	7

Add	HEX Code
175	7
176	7
177	7
178	7
179	7
180	7
181	7
182	7
183	7
184	7
185	7
186	7
187	7
188	7
189	7
190	7
191	7
192	7
193	7
194	F
195	F
196	F
197	F
198	F
199	F

Add	HEX Code
200	F
201	F
202	F
203	F
204	F
205	F
206	F
207	F
208	F
209	F
210	F
211	F
212	F
213	F
214	F
215	F
216	F
217	F
218	F
219	F
220	F
221	F
222	F
223	F
224	F

LOGIC DEVICE DESCRIPTION
P/N 2889 1588

ROM Content:

Add	HEX Code
225	F
225	F
226	F
227	F
228	F
229	F
230	F
231	F
232	F
234	F
235	F
236	F
237	F
238	F
239	F
240	F
241	F
242	F
243	F
244	F
245	F
246	F
247	F
248	F
249	F

Add	HEX Code
250	F
251	F
252	F
253	F
254	F
255	F
256	F
257	F
258	F
259	F
260	F
261	F
262	F
263	F
264	F
265	F
266	F
267	F
268	F
269	F
270	F
271	F
272	F
273	F
274	F

Add	HEX Code
275	F
276	F
277	F
278	F
279	F
280	F
281	F
282	F
283	F
284	F
285	F
286	F
287	F
288	F
289	F
290	F
291	F
292	F
293	F
294	F
295	F
296	F
297	F
298	F
299	F

ROM Content:

Add	HEX Code
300	F
301	F
302	F
303	F
304	F
305	F
306	F
307	F
308	F
309	F
310	F
311	F
312	F
313	F
314	F
315	F
316	F
317	F
318	F
319	F
320	F
321	F
322	F
323	F
324	F

Add	HEX Code
325	F
326	F
327	F
328	F
329	F
330	F
331	F
332	F
333	F
334	F
335	F
336	F
337	F
338	F
339	F
340	F
341	F
342	F
343	F
344	F
345	F
346	F
347	F
348	F
349	F

Add	HEX Code
350	F
351	F
352	F
353	F
354	F
355	F
356	F
357	F
358	F
359	F
360	F
361	F
362	F
363	F
364	F
365	F
366	F
367	F
368	F
369	7
370	7
371	6
372	6
373	6
374	6

ROM Content:

Add	HEX Code
375	6
376	6
377	6
378	6
379	6
380	4
381	4
382	4
383	4
384	4
385	4
386	4
387	4
388	4
389	8
390	0
391	0
392	0
393	0
394	0
395	0
396	0
397	0
398	0
399	0

Add	HEX Code
400	0
401	0
402	0
403	0
404	0
405	0
406	0
407	0
408	0
409	0
410	0
411	0
412	0
413	0
414	0
415	0
416	0
417	0
418	0
419	0
420	0
421	0
422	0
423	0
424	0

Add	HEX Code
425	0
426	0
427	0
428	0
429	0
430	0
431	0
432	0
433	0
434	0
435	0
436	0
437	0
438	0
439	0
440	0
441	0
442	0
443	0
444	0
445	0
446	0
447	0
448	0
449	0

ROM Content:

Add	HEX Code
450	0
451	0
452	0
453	0
454	0
455	0
456	0
457	0
458	0
459	0
460	0
461	0
462	0
463	0
464	0
465	0
466	0
467	0
468	0
469	0
470	0

Add	HEX Code
471	0
472	0
473	0
474	0
475	0
476	0
477	0
478	0
479	0
480	0
481	0
482	0
483	0
484	0
485	0
486	0
487	0
488	0
489	0
490	0
491	0

Add	HEX Code
492	0
493	0
494	0
495	0
496	0
497	0
498	0
499	0
500	0
501	0
502	0
503	0
504	0
505	0
506	0
507	0
508	0
509	0
510	0
511	0

ROM Content:

Add	HEX Code
0	7
1	6
2	5
3	4
4	3
5	2
6	1
7	0
8	7
9	7
10	7
11	7
12	7
13	7
14	7
15	7
16	6
17	5
18	4
19	3
20	2
21	1
22	0
23	7
24	7

Add	HEX Code
25	7
26	7
27	7
28	7
29	7
30	7
31	7
32	4
33	4
34	4
35	4
36	4
37	4
38	4
39	4
40	7
41	7
42	7
43	7
44	7
45	7
46	7
47	7
48	7
49	7

Add	HEX Code
50	7
51	7
52	7
53	7
54	7
55	7
56	7
57	7
58	7
59	7
60	7
61	7
62	7
63	7
64	0
65	1
66	2
67	3
68	4
69	5
70	6
71	7
72	0
73	0
74	0

ROM Content:

Add	HEX Code
75	0
76	0
77	0
78	0
79	0
80	0
81	1
82	2
83	3
84	4
85	5
86	6
87	7
88	0
89	0
90	0
91	0
92	0
93	0
94	0
95	0
96	3
97	3
98	3
99	3

Add	HEX Code
100	3
101	3
102	3
103	3
104	0
105	0
106	0
107	0
108	0
109	0
110	0
111	0
112	0
113	0
114	0
115	0
116	0
117	0
118	0
119	0
120	0
121	0
122	0
123	0
124	0

Add	HEX Code
125	0
126	0
127	0
128	E
129	C
130	A
131	8
132	6
133	4
134	2
135	0
136	E
137	E
138	E
139	E
140	E
141	E
142	E
143	E
144	E
145	C
146	A
147	8
148	6
149	4

LOGIC DEVICE DESCRIPTION
P/N 2889 1596

ROM Content:

Add	HEX Code
150	2
151	0
152	E
153	E
154	E
155	E
156	E
157	E
158	E
159	E
160	8
161	8
162	8
163	8
164	8
165	8
166	8
167	8
168	E
169	E
170	E
171	E
172	E
173	E
174	E

Add	HEX Code
175	E
176	E
177	E
178	E
179	E
180	E
181	E
182	E
183	E
184	E
185	E
186	E
187	E
188	E
189	E
190	E
191	E
192	0
193	2
194	4
195	6
196	8
197	A
198	C
199	E

Add	HEX Code
200	0
201	0
202	0
203	0
204	0
205	0
206	0
207	0
208	0
209	2
210	4
211	6
212	8
213	A
214	C
215	E
216	0
217	0
218	0
219	0
220	0
221	0
222	0
223	0
224	6

ROM Content:

Add	HEX Code
225	6
226	6
227	6
228	6
229	6
230	6
231	6
232	0
233	0
234	0
235	0
236	0
237	0
238	0
239	0
240	0
241	0
242	0
243	0
244	0
245	0
246	0
247	0
248	0
249	0

Add	HEX Code
250	0
251	0
252	0
253	0
254	0
255	0
256	0
257	0
258	0
259	0
260	0
261	0
262	0
263	0
264	0
265	0
266	0
267	0
268	0
269	0
270	0
271	0
272	0
273	0
274	0

Add	HEX Code
275	0
276	0
277	0
278	0
279	0
280	0
281	0
282	0
283	0
284	0
285	0
286	0
287	0
288	0
289	0
290	0
291	0
292	0
293	0
294	0
295	0
296	0
297	0
298	0
299	0

LOGIC DEVICE DESCRIPTION
P/N 2889 1596

ROM Content:

Add	HEX Code
300	0
301	0
302	0
303	0
304	0
305	0
306	0
307	0
308	0
309	0
310	0
311	0
312	0
313	0
314	0
315	0
316	0
317	0
318	0
319	0
320	7
321	7
322	7
323	7
324	7

Add	HEX Code
325	7
326	7
327	7
328	7
329	7
330	7
331	7
332	7
333	7
334	7
335	7
336	7
337	7
338	7
339	7
340	7
341	7
342	7
343	7
344	7
345	7
346	7
347	7
348	7
349	7

Add	HEX Code
350	7
351	7
352	7
353	7
354	7
355	7
356	7
357	7
358	7
359	7
360	7
361	7
362	7
363	7
364	7
365	7
366	7
367	7
368	7
369	7
370	7
371	7
372	7
373	7
374	7

ROM Content:

Add	HEX Code
375	7
376	7
377	7
378	7
379	7
380	7
381	7
382	7
383	7
384	0
385	0
386	0
387	0
388	0
389	0
390	0
391	0
392	0
393	0
394	0
395	0
396	0
397	0
398	0
399	0

Add	HEX Code
400	0
401	0
402	0
403	0
404	0
405	0
406	0
407	0
408	0
409	0
410	0
411	0
412	0
413	0
414	0
415	0
416	0
417	0
418	0
419	0
420	0
421	0
422	0
423	0
424	0

Add	HEX Code
425	0
426	0
427	0
428	0
429	0
430	0
431	0
432	0
433	0
434	0
435	0
436	0
437	0
438	0
439	0
440	0
441	0
442	0
443	0
444	0
445	0
446	0
447	0
448	E
449	E

LOGIC DEVICE DESCRIPTION
P/N 2889 1596

ROM Content:

Add	HEX Code
450	E
451	E
452	E
453	E
454	E
455	E
456	E
457	E
458	E
459	E
460	E
461	E
462	E
463	E
464	E
465	E
466	E
467	E
468	E
469	E
470	E

Add	HEX Code
471	E
472	E
473	E
474	E
475	E
476	E
477	E
478	E
479	E
480	E
481	E
482	E
483	E
484	E
485	E
486	E
487	E
488	E
489	E
490	E
491	E

Add	HEX Code
492	E
493	E
494	E
495	E
496	E
497	E
498	E
499	E
500	E
501	E
502	E
503	E
504	E
505	E
506	E
507	E
508	E
509	E
510	E
511	E

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1638

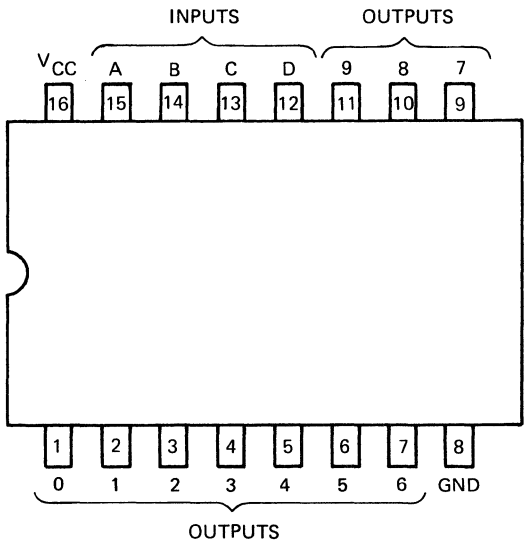
Integrated Circuit

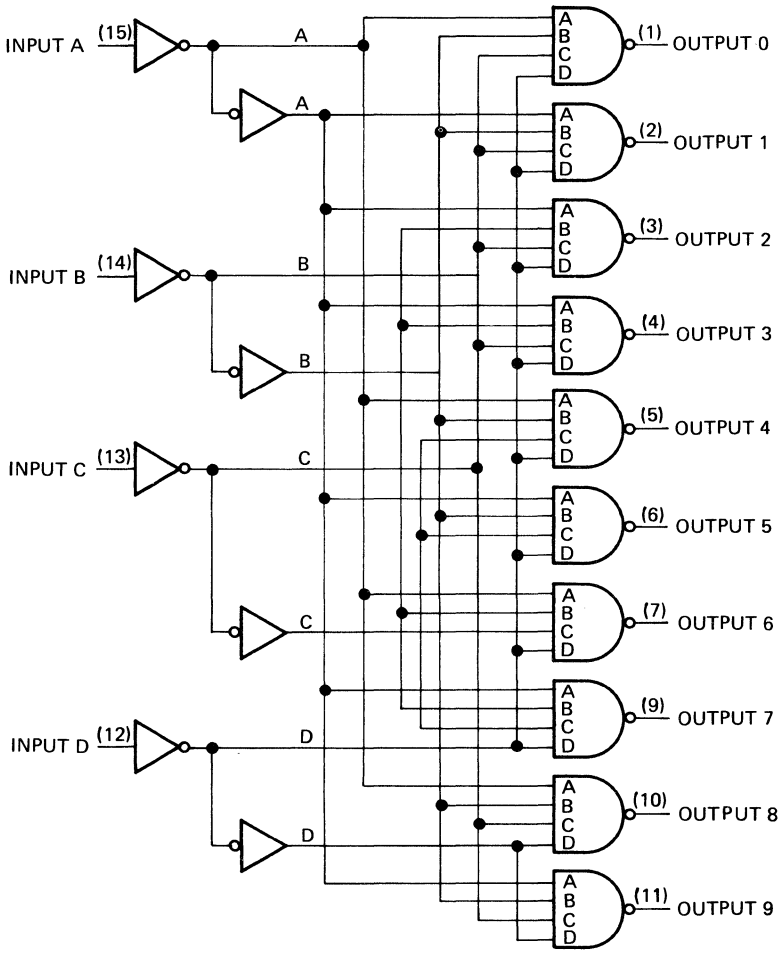
Element Type:	TTL (low power schottky)
Standard Number:	74LS42
Circuit Designation:	BCD-to-decimal decoder (1 of 10)

Description of Operation:

This package contains one binary coded decimal number to decimal coded number decoder. The function performed is to convert a binary coded decimal number applied to inptus A, B, C, and D to a decimal weighted output value of 0 through 9. Refer to truth table for operaton.

Outputs	Inputs
High 2.7 to 3.5 Volts	High 2.0 Volts min.
Low 0.35 to 0.5 Volts	Low 0.8 Volts max.





Truth Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1646

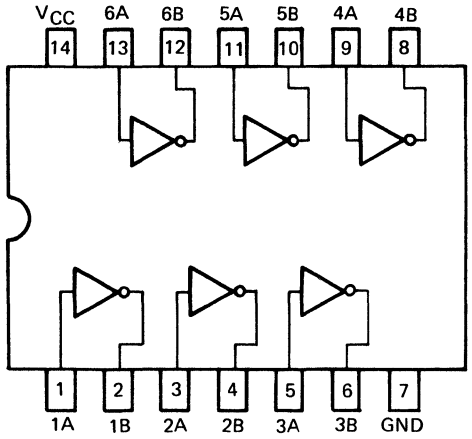
Integrated Circuit

Element Type:	CMOS
Standard Number:	74C04
Circuit Designation:	Hex inverter

Description of Operation:

This package contains six hex inverter circuits. They perform the function $\bar{A} = B$ where A is the input and B is the output. A low at A will result in a high output at B.

Outputs		Inputs
High 2.4	4.5 Volts	High 3.0 - 3.5 Volts
Low 0.4	0.5 Volts	Low 0.8 - 1.5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1653

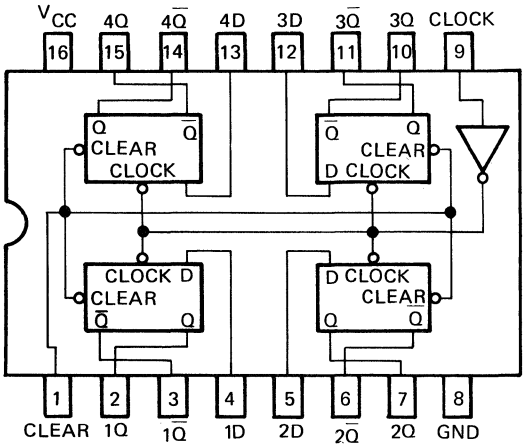
Integrated Circuit

Element Type: CMOS
Standard Number: 74C175
Circuit Designation: Quad D flip-flop

Description of Operation:

This package contains four positive-edge-triggered-D-type flip-flops. Both true and complemented outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive going edge of the clock pulse. The clearing operation, enabled by a negative pulse at clear input, clears all four Q outputs to logical "0" and Q's to logical "1".

Outputs	Inputs
High 2.4 to 4.5 Volts	High 3 to 3.5 Volts
Low 0.4 to 0.5 Volts	Low 0.8 to 1.5 Volts



Truth Table

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\bar{Q}$**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1687

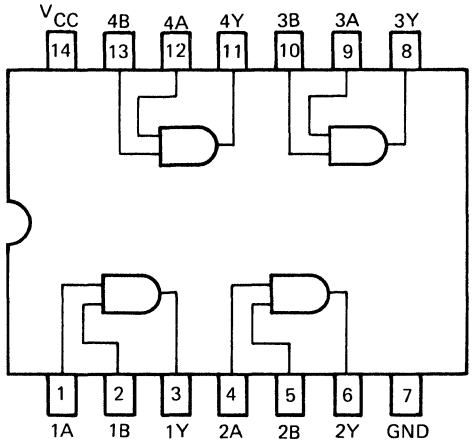
Integrated Circuit

Element Type:	TTL (low power shottky)
Standard Number:	74LS08
Circuit Designation:	Quad 2-input and gate

Description of Operation:

This package contains four 2-input and gates. The gate performs the function AB = Y where both A and B must be high for a high level at Y, otherwise the result at Y is low.

Outputs	Inputs
High 2.7 Volts min.	High 2 Volts min.
Low .5 Volts max.	Low .8 Volts max.



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 18891695

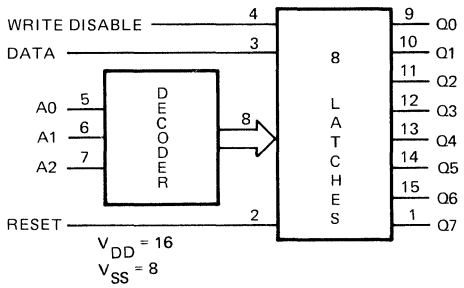
Integrated Circuit

Element Type: CMOS
Standard Number: CD4099B
Circuit Designation: 8-Bit addressable latch

Description of Operation:

This package contains one 8-bit addressable latch. It is a serial-input, parallel output storage register. Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when write disable is at a low level. When write disable is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of write disable and address inputs. A master reset input is available, which resets all bits to a logic "0" level when reset and write disable are at a high level. When reset is at a high level, and write disable is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

Outputs	Inputs
High 4.95 - 5.0 Volts	High 4.2 Volts min.
Low 0.00 - 0.05 Volts	Low 0.8 Volts max.

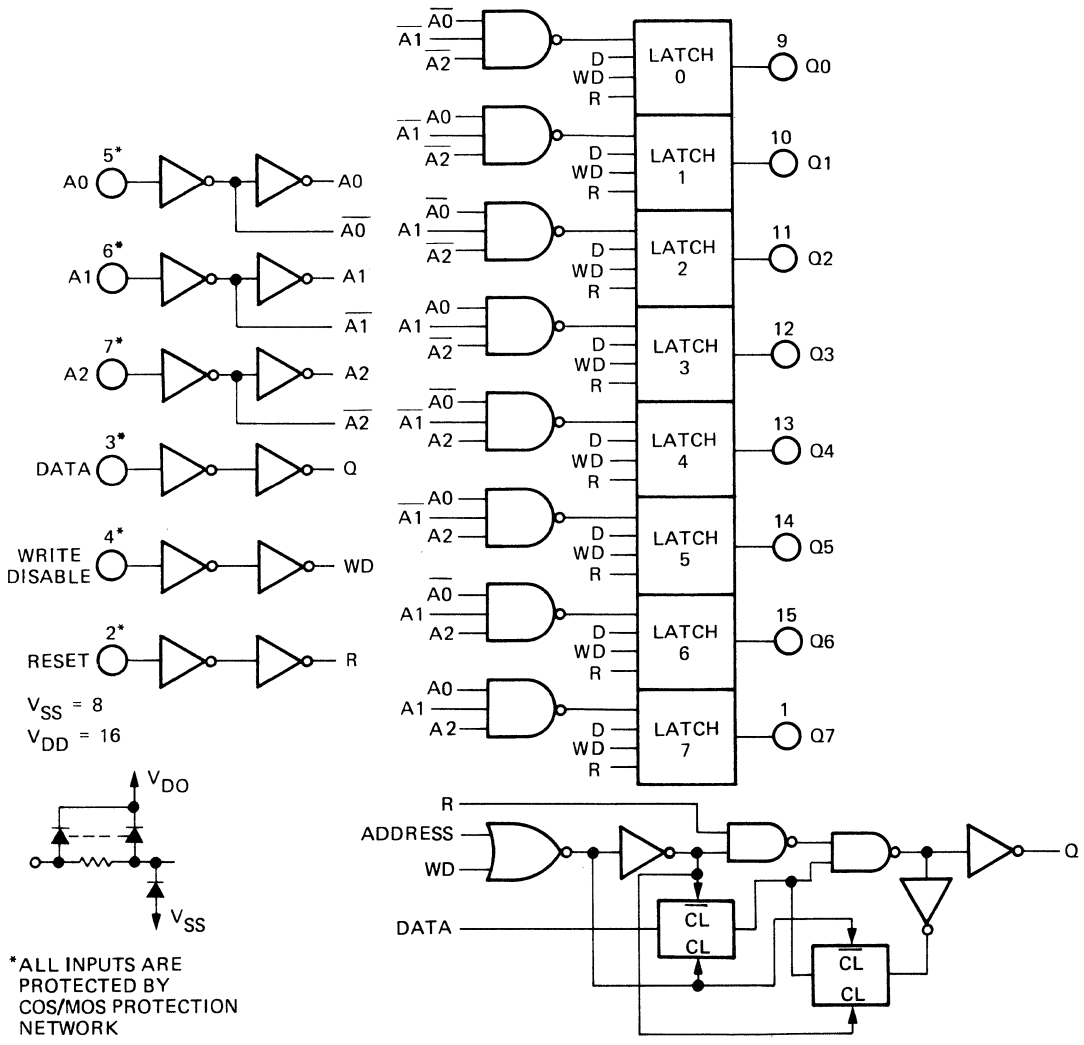


Truth Table

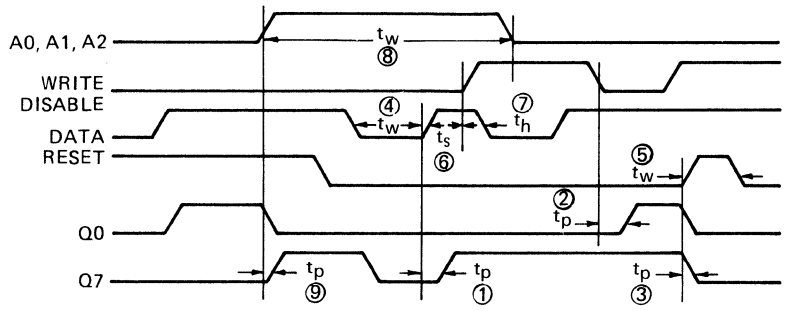
Mode Selection			
WD	**R**	**Addressed Latch**	**Unaddressed Latch**
L	L	Follows data	Holds previous state
L	H	Follows data (Active high 8-channel demultiplexer)	Reset to "0"
H	L	Holds previous state	Holds previous state
H	H	Reset to "0"	Reset to "0"

WD = Write disable
R = Reset

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1889 1695 (Cont)



Timing Diagram



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1889 1711

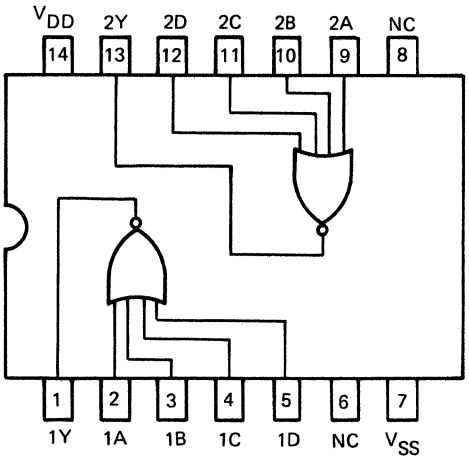
Integrated Circuit

Element Type: CMOS
Standard Number: CD4002B
Circuit Designation: Dual 4-input NOR gate

Description of Operation:

This package contains two 4-input NOR gates. The gates perform the function $\overline{A + B + C + D} = J$ where A, B, C, and D are the inputs and Y is the output. A low level at A, B, C, or D will result in a high level at Y. A, B, C, and D must be at a high level to result in a low level at Y.

Outputs	Inputs
High 4.95 Volts max.	High 1. to 2.25 Volts
Low 0.05 Volts	Low 0.5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 1729

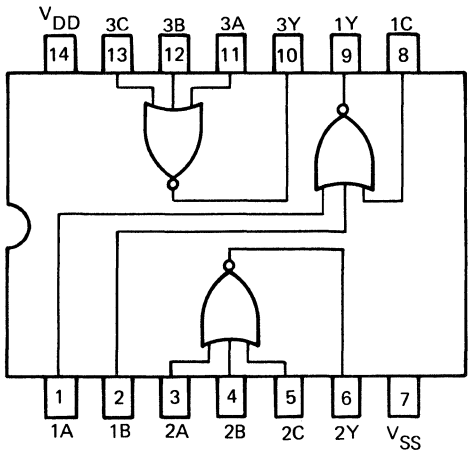
Integrated Circuit

Element Type:	CMOS
Standard Number:	4025B
Circuit Designation:	Triple 3-input NOR gate

Description of Operation:

This package contains three 3-input NOR gates. The gates perform the function $\overline{A + B + C} = Y$ where A, B, and C are the inputs and Y is the output. A low level at A, B, or C will result in a high level at Y. A, B, and C must be at a high level to result in a low level at Y.

Outputs	Inputs
High 4.95 Volts max.	High 1. - 2.25 Volts
Low 0.05 Volts	Low 0.5 Volts



LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2889 2446

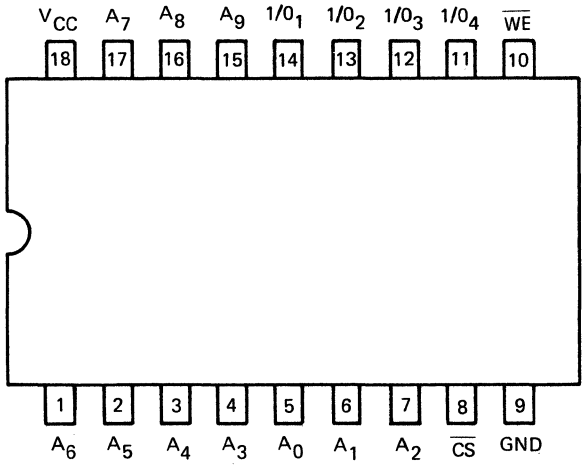
Integrated Circuit

Element Type: MOS
Standard Number: 2114L
Circuit Designation: 1024 x 4 Static RAM

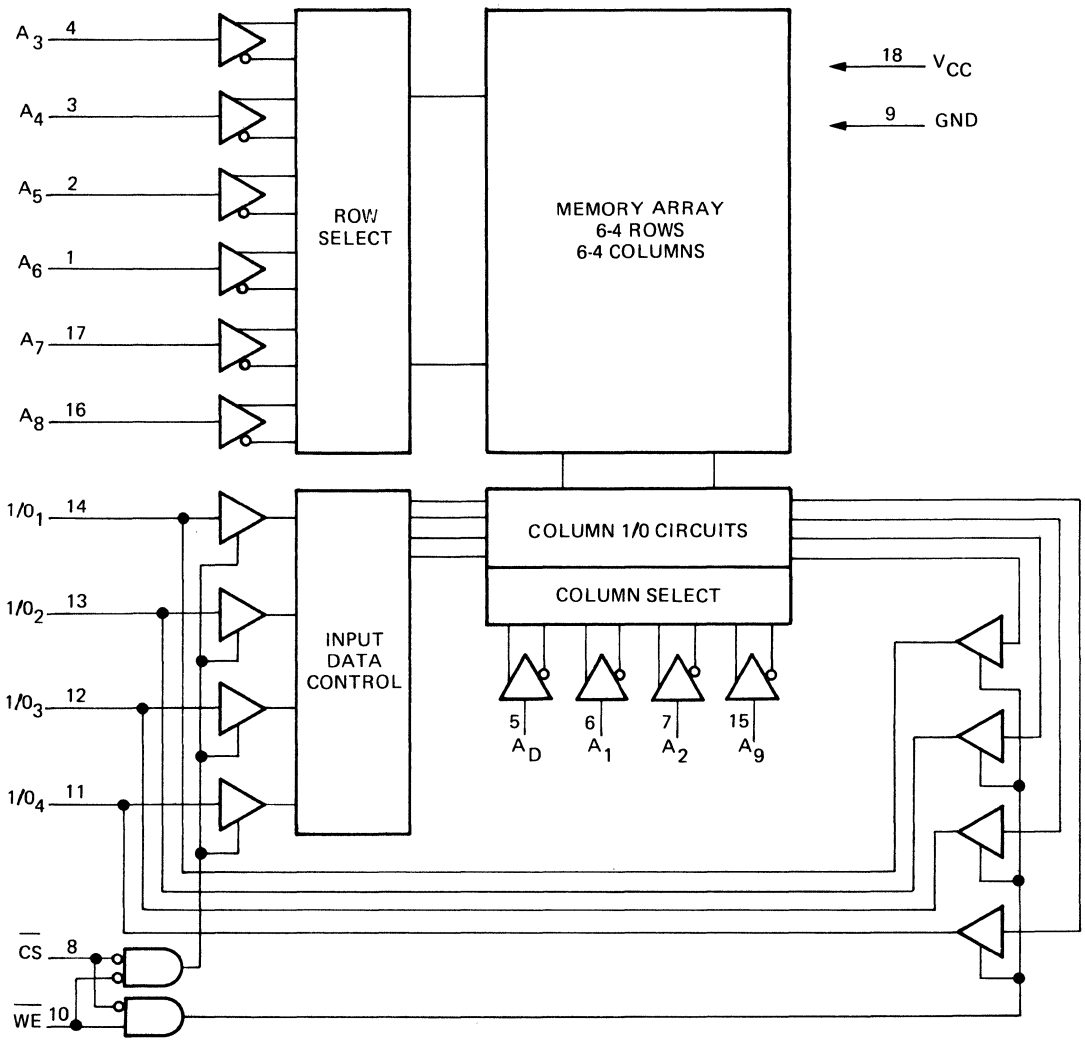
Description of Operation:

This specification defines the requirements and characteristics of a 1K x 4 static Random Access Memory (RAM) device similar to a commercial type 2114L. All inputs and outputs are directly TTL compatible.

Outputs	Inputs
High 2.4 Volts	High 2.0 Volts
Low 0.45 Volts	Low 0.8 Volts



Functional Block Diagram



NOTE: ADDRESS LINES USED FOR COLUMN AND ROW SELECTS MAY VARY WITH DIFFERENT VENDORS

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 2322 2292

Integrated Circuit

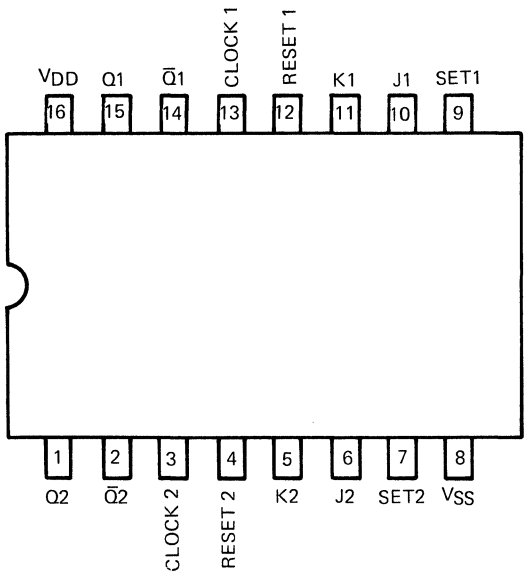
Element Type: CMOS
Standard Number: 4027
Circuit Designation: Dual J-K Master Slave - Flip-Flop

Description of Operation:

This device is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs.

Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

Outputs	Inputs Noise Immunity
High 4.95 Volts min.	1.5 Volts min.
Low .5 Volts max.	



Truth Table

Asynchronized				Sychronized				
Inputs		Outputs		Inputs			Outputs	
S_D	C_D	Q	$\bar{Q}$	CP	J	K	Qn + 1	$\bar{Q}n + 1$
L	H	L	H	_/‾	L	L	No Change	No Change
H	L	H	L	_/‾	H	L	H	L
H	H	H	H	_/‾	L	H	L	H
				_/‾	H	H	$\bar{Q}_n$	Q_n

L = Low Level
H = High Level
_/‾ = Positive Going Transistion
X = Don't Care
Q_n+1 = State After Clock Positive Transition

Conditions: $\overline{S}_D$ - $\overline{C}_D$ - Low

LOGIC DEVICE DESCRIPTION
(Bur.) P/N 1083 4935

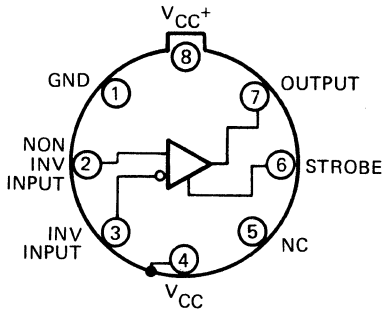
Integrated Circuit

Element Type: Linear
Standard Number: LM311
Circuit Designation: Differential Comparator

Description of Operation:

The LM311 is a single high-speed voltage comparator. This device is designed to operate over a wide range of power supply voltages, including 5 volt supplies for logic systems up to ±18 volt supplies for operational amplifiers. Output levels are compatible with most DTL, TTL and MOS circuits. The comparator is capable of driving lamps or relays and switching voltages up to 50 volts at 50 milliampers. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, Vcc+ or Vcc-. Offset balancing and strobe capability are available and the outputs can be wire-OR connected. If the strobe input is low, the output will be in the off state regardless of the differential input.

Outputs	Inputs
High Collector Voltage Low .23 - .4 volts	High/Low: When Pin 2 is less than or equal to 100 mv, relative to Pin 3, the output transistor is turned on.



NOTE: PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

SECTION 4
MAINTENANCE TECHNIQUES

GENERAL

The design and construction of the Terminal provides for maximum maintainability. Corrective maintenance utilizes a repair to the card level on-site with off-site repair of the cards. Some components are socketed and can be replaced on-site.

Maintenance Concept

The terminal, excluding the display, consists largely of plug-in subassemblies and printed circuit board modules. Repair effected by a field engineer is to the level of the printed circuit board module, although some components, such as ROMs, are socketed and can be repaired in the field.

Personnel Requirements

The terminal can be serviced and maintained on site by a field engineer with an electronic background in solid-state devices, digital circuitry and CRT displays, together with one week's training in servicing and programming the equipment.

Maintenance Equipment and Tools

Effective on-site maintenance of the terminal requires a printed-circuit board extender (Part No. 2889-2420), spare boards, an oscilloscope, a multimeter, and normal hand tools (pliers, screwdriver). Subject to instructional development with a MTS-1, the BDM1200 Digital Meter is to be used in place of an oscilloscope. Card extender cable is available for use in troubleshooting the MTS-1.

SPECIAL TEST EQUIPMENT

No special test equipment is required to maintain the terminal.

Preventive Maintenance

Preventive maintenance for the terminal is not anticipated.

MAINTENANCE TEST ROUTINE (MTR)

The terminal provides the capability of conducting a self-generated confidence test of all major subsystems within the terminal. This type of confidence test can be initiated from any of three sources: power up, keyboard CTRL request, and data comm ESC request. The initiaton of a confidence test causes the erasure of all data in the display refresh memory. Successful completion of the confidence test causes the message ****** to be displayed. A confidence test detecting improper operation of a subsystem area commences a diagnostic routine to the extent allowed by the nature of the failure.

At the successful completion of each subsystem test at least one, and in some cases more, indications are given. The following table summarizes the relationships between the tests and the indicators.

Table 4-1. Confidence Test Indicators

Subsystem	Indications
Main U-Processor	Buzzer sounds All indicators light
Display U-Processor	Indicator #1 goes out (LTAI)
Main memory RAM	Indicator #2 goes out (ERROR)
ROM CRC's	Indicators #3 & #4 go out (ENQ) (CTRL)
SIO generator	Indicator #5 goes out (FORMS)
Data Comm U-Processor	Indicator #6 goes out (LOCAL)
Main/Data Comm Communication links	Indicator #7 goes out (RCV)
Data Comm RAM	Indicator #8 goes out (XMT)

In case of failure, the status displayed on the keyboard lights is also displayed on the screen. A confidence test continues to completion, irrespective of errors located, provided said errors do not affect the confidence test itself. Errors affecting the confidence test (MPU or scratchpad RAM or ROM errors) cause the terminal to go into an idle state after an attempt to diagnose the error is made. The terminal remains off-line after failure of an ESC initiated confidence test. Test results are transmitted only after successful tests.

Tests and Sequences

The MTS-1 system is composed of several subsystems. The system's layout is depicted in figure 4-1. To better understand what any given test's success, or failure, implies about the state of the system, refer to figure 4-1.

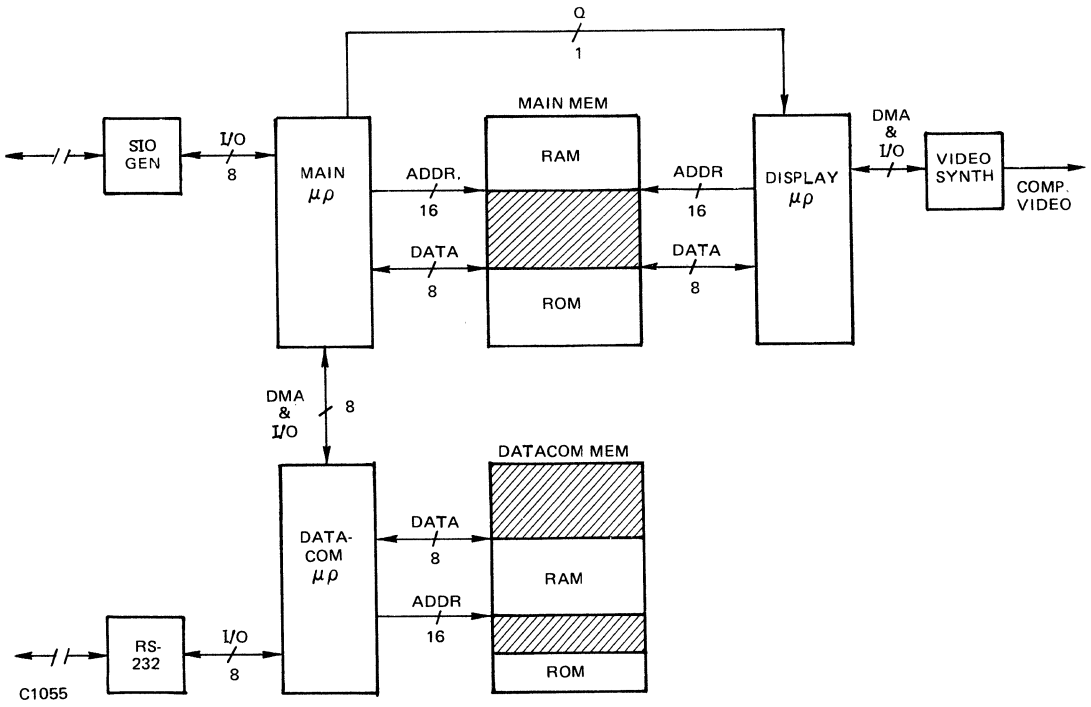


Figure 4-1. MTS-1 System

Figure 4-2 is a flow-chart of the confidence tests. The dotted lines on the diagram indicate that two processors are synchronized at this point in the tests.

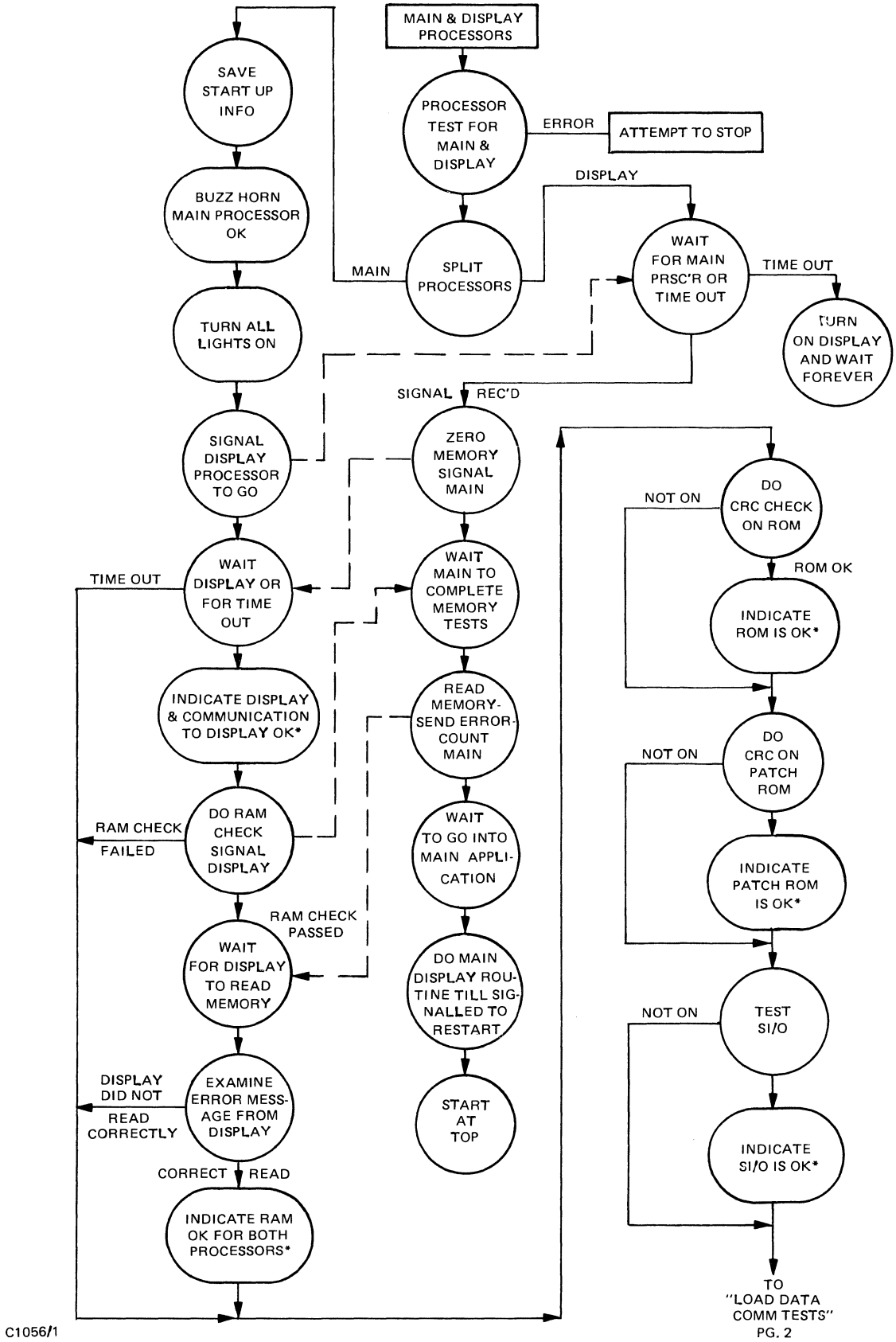


Figure 4-2. Confidence Test Flow Chart (Sheet 1 of 2)

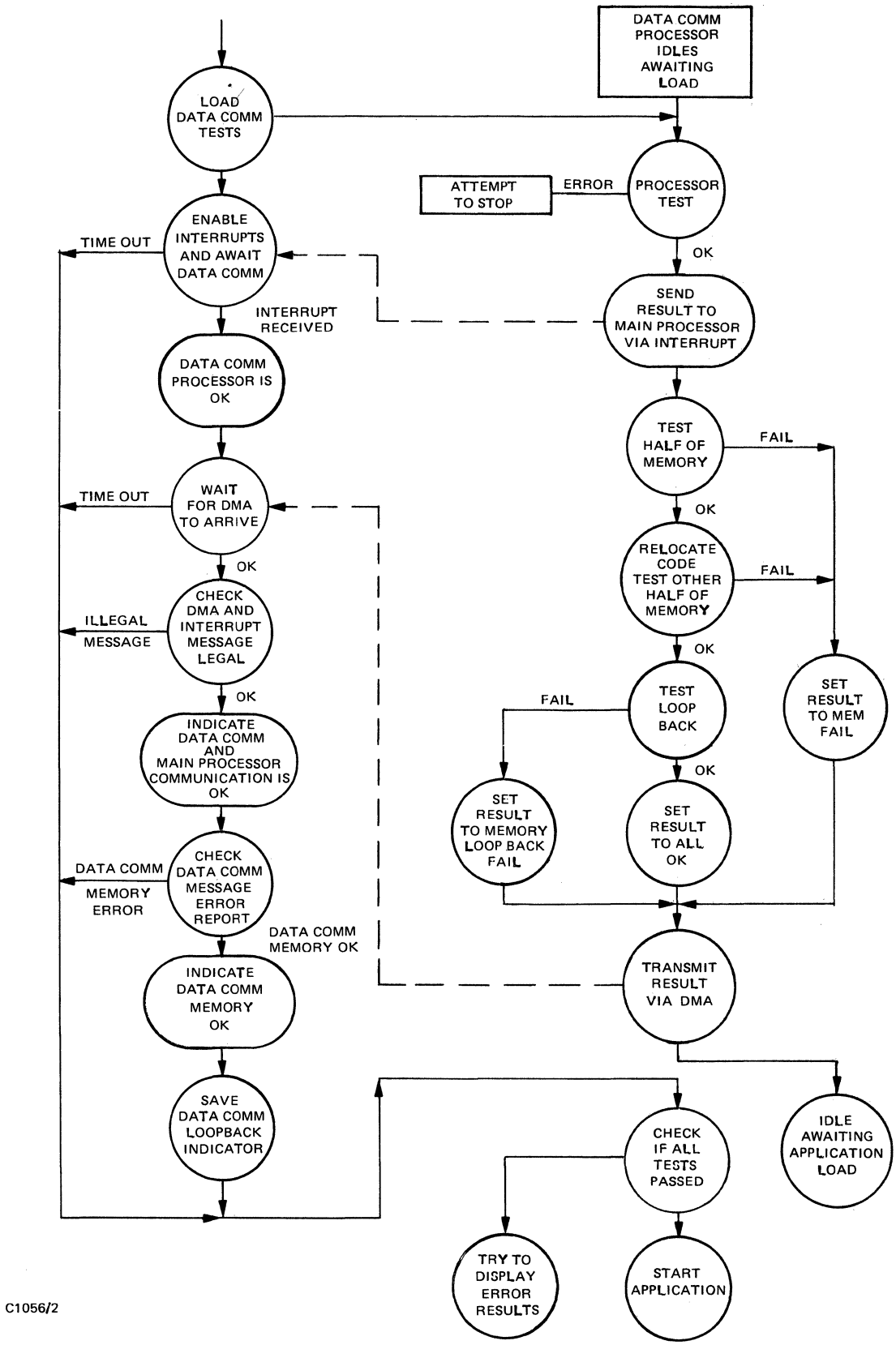


Figure 4-2. Confidence Test Flow Chart (Sheet 2 of 2)

POWER-ON

When the system is initially powered on all the processors in the system are reset. The display and main micro-processors start executing instructions starting at location zero in the main memory's ROM area. The Data Comm micro-processor starts executing at location zero in its own ROM area. The Data Comm ROM contains only a simple loader, so the Data Comm micro-processor should idle until a loader directive is received from the main micro-processor. It will be omitted from the discussion until that directive is issued. The display and main micro-processors both execute the basic processor tests. This subsystem test verifies that the micro-processor can successfully:

a. Fetch and execute instructions from ROM.

b. The arithmetic and logical operators work correctly.

c. Data addressing works correctly.

MAIN PROCESSOR FAILURE

Upon completion of the basic processor test, the display processor determines its identity by sampling a hardware condition and branches off to a separate location from the main processor. It then waits for the main micro-processor to acknowledge that it has successfully completed its basic processor test before continuing into the first phase of the RAM test. If this acknowledgement does not occur within a few seconds, the display processor activates the video synthesizer, supplying it with random data. The screen which is blank until this point starts to flash, flip, and jump. This condition indicates that either the main micro-processor could not pass the basic test, or that the two processors cannot communicate thorugh the common memory.

MAIN PROCESSOR SUCCESS

When the main micro-processor completes its basic test, it lights all the LED indicators on the keyboard and sounds the buzzer. Until this time, the LED indicators have displayed whatever random state they happen to have come up in. The main processor then acknowledges to the display micro-processor that it has completed the basic tests. It then waits for the display processor to complete Phase I of the RAM tests.

If the main processor waits an excessive amount of time for an acknowledgement from the display processor, the micro-processor makes the assumption that the display processor has failed to pass its basic tests, and the main processor continues the tests.

RAM TEST

The RAM test is done in three phases. The first and third phases of the test are performed by the display micro-processor; only the second phase is performed by the main micro-processor. These test phases do not overlap, so at the end of each phase of the testing sequence, the active micro-processor acknowledges that it has completed its phase and then waits for the other processor to complete its phase of the task. At the end of the memory tests, the display processor goes idle. Its part in the confidence tests is completed. It waits for the application to begin.

Phase I

The display micro-processor writes hexadecimal 00 to all memory locations from hexadecimal addresses D000 through FFFF. The act of clearing the last location signals the main micro-processor to begin phase II. The main micro-processor turns off LED indicator 1 when it receives acknowledgement that phase I of the memory test is complete. This acknowledgement is the main micro-processor's first opportunity to discover that the display processor has successfully passed the basic processor test.

Phase II

The main micro-processor starts at Memory Address location FFFF (Hex) and verifies that the first two memory locations contain 00. It then writes AA and 55 to the next two respective locations and verifies that the same pattern is read back. This test is repeated for each two locations with the reversed values 55 and AA. Both locations are then written with the ASCII blank character. The memory pointer is then decremented by two, and the process is repeated. If any of the read data fails to correspond to the expected value, the main micro-processor ORs the logical difference between the expected value and the read value into a table location corresponding to the current 1024 boundary the system is in.

After every location from FFFF through D000 has been tested, the table of errors is examined, starting with the location corresponding to memory addresses D000 through D3FF. As long as both the upper four bits and the lower four bits of the address space both indicate errors and the examined table entry corresponds to an address area below E800, the assumption is made that RAM was not present in this system at those locations.

From the time that the first correct area of RAM is discovered until all of the table is examined, any further detected errors are assumed to be bad chip locations. If (after the table has been examined to find any bad RAM chips) one or more chips are found to be faulty, a display screen image is built which indicates the bad RAM chips. The screen reads:

BAD CHIP(S) = NN = MM . . . . . .

The locations which correspond to chip numbers are shown on figures 4-3 and 4-4. There is a maximum of 24 RAM chips expected on the MTS-1 system.

Phase III

When the main micro-processor finishes phase II or the RAM test, it notifies the display micro-processor and passes it the lower bound of RAM present in the system. The display processor then verifies that all locations above the boundary read back as ASCII blanks. If they fail to do so, the main processor is informed. The display processor then goes into idle mode and awaits a command to display a screen image. Finally the main micro-processor extinguishes LED indicator two, if there were no errors found in memory by either processors.

ROM CRC CHECK

After testing the RAM memory, the main micro-processor tests the ROM memory to make sure there are no errors. Each 2048 bytes of memory have a CRC computed over it using a standard polynomial. These CRCs are stored in the ROM address space 7FE0 thorugh 7FFF. The confidence test recomputes these CRC values for each 2048 bytes of ROM and compares the computed value to the value stored in memory. Any time these values fail to match, a screen message is made which indicates what part of the address space is in error. This message looks like:

BAD ROM(S) = nn = mm . . . . . .

If there are any errors discovered, LED indicator four is left on; otherwise, both LED indicators three and four are extinguished. Because of the bit serial nature of this test and the size of the ROM space on the MTS system, this test typically takes 28 to 30 seconds before a system failure can be assumed.

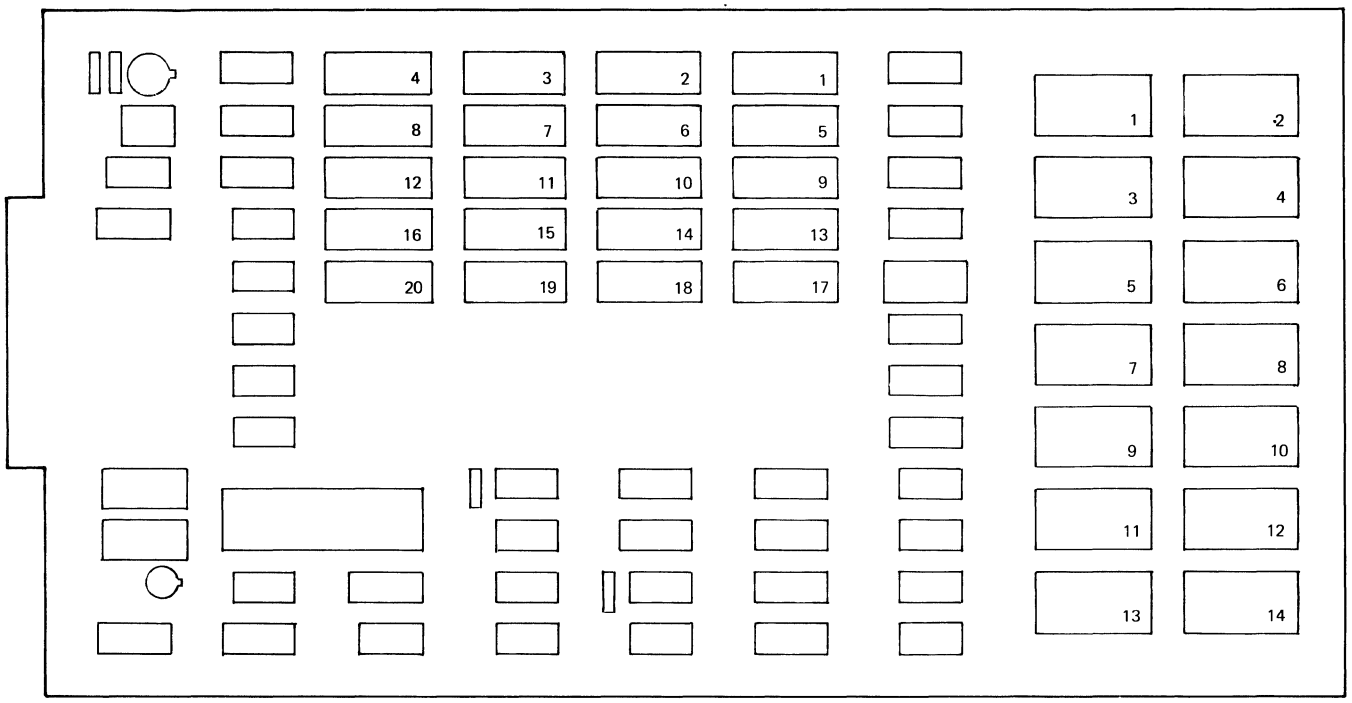


Figure 4-3. RAM and ROM Numbering (22 Pin RAM)

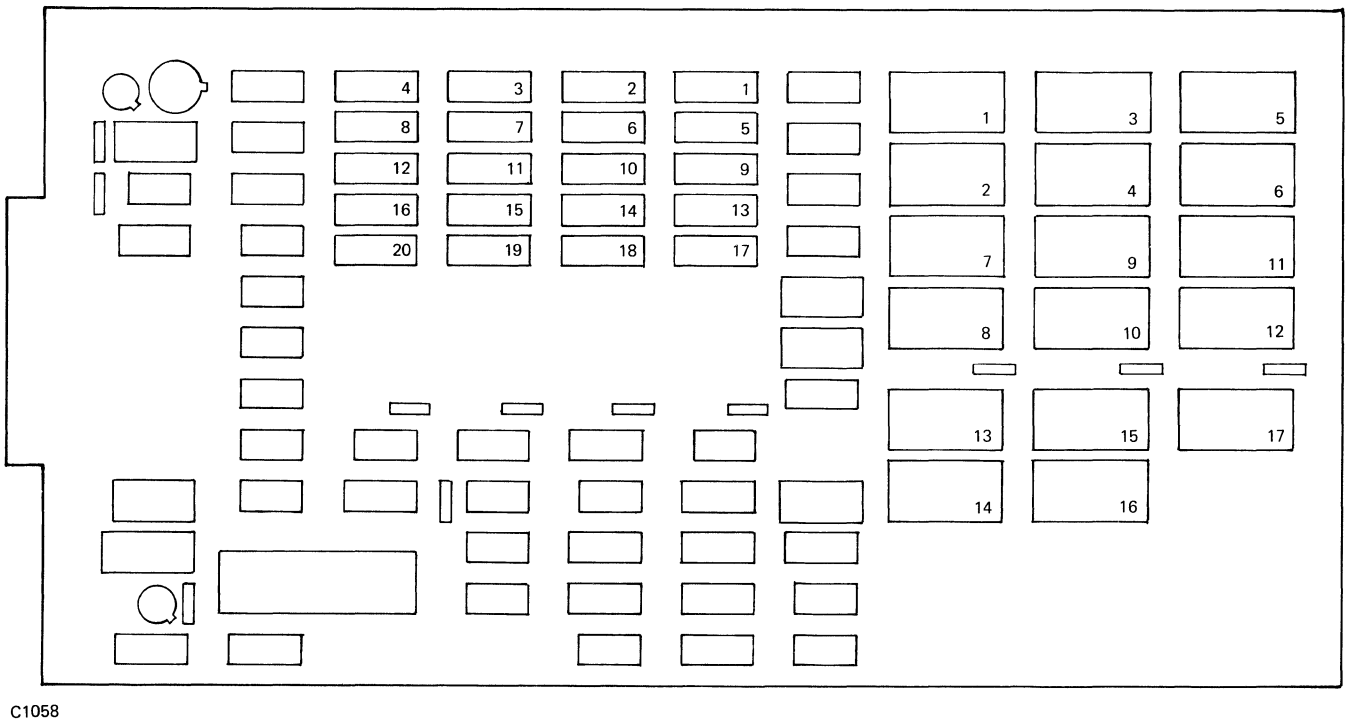


Figure 4-4. RAM and ROM Numbering (18 Pin RAM)

SIO TEST

After the ROM check is completed, the main micro-processor sends two data patterns through the SIO transmitter to verify that the data pattern successfully shifts through the circuit without changing. If this test is successful, LED indicator five is extinguished.

DATA COMM TESTS

The main micro-processor initiates the Data Comm test by setting the DMA pointer register to point to the beginning of the confidence test code, and by sending the data comm micro-processor a LOAD 4 PAGES command. The main micro-processor then enables the interrupt and goes into a wait loop, waiting for the data comm processor to acknowledge that the data comm processor has passed the basic confidence test. If the data comm micro-processor fails to interrupt the main micro-processor with an acknowledgement before the time-out period has elapsed, the main processor again masks off all interrupts and transfers control to the confidence test exit routine.

The data comm processor receives the load directive and then proceeds to load its RAM memory starting at location 0400 with 1024 bytes of the confidence test. The data comm processor then unconditionally transfers execution to location 0416. This location now contains the basic micro-processor tests which the data comm processor tries to execute. When this test is successfully completed, the data comm microprocessor recognizes itself as the data comm machine by testing its own program counter value and branches off to the test code dedicated to the data comm processor. The data comm processor uses the I/O channel to acknowledge successful completion of its confidence tests. The main micro-processor turns off LED indicator 6 as soon as it is interrupted by the data comm processor. This shows that the data comm processor has passed the basic processor tests.

The main and data comm processors then proceed to exchange messages through all their available means of communications that the two processors have - status I/O, interrupt I/O, and DMA (Direct Memory Access) - in order to establish that the channel works in all these modes. If no trouble is encountered, LED indicator number 7 is extinguished.

After the channel has been tested, the data comm micro-processor first performs phases I, II, and III of the RAM test on its local memory, starting at location 0800 through 0BFF. If location 0800 through 0BFF of its RAM passes the test, then the data comm micro-processor copies the code it is executing into locations 0800 - 0BFF and performs all phases of the memory test on locations 0400 - 07FF.

If any memory fails, the data comm processor reports the failure to the main micro-processor and halts. Otherwise, the system performs the data comm loopback test to establish whether or not the data comm link is functioning. The result of the data comm test is passed to the main micro-processor.

The main micro-processor waits for either a report of a memory failure or a data comm loopback report from the data comm processor. If the loopback report is received, the system saves the report (to pass it to the TSL interpreter as an argument) and turns off LED indicator 8 to show that the data comm memory has passed the confidence test. If the memory error report returns or the processor times-out waiting for the reports, the system branches straight to the confidence test exit routine.

CONFIDENCE EXIT ROUTINE

At the end of the confidence test, the main micro-processor checks to see if any of the LED indicators are left on as the result of a subsystem test failure. If this is the case, it adds to the screen image stored in memory the display of the LED configuration on the status line. The character O is used to represent a light which is OFF, and the character * is used to represent an LED, which is ON. The display processor, which should be idling, is sent a command to display the screen image that has been built in memory. The main micro-processor then idles until it is powered off and on again. If all tests are successfully performed, the interpreter is initiated.

Other Maintenance Related Tests

The terminal is capable of displaying the resident character set through the keyboard CTRL or data comm ESC request.

The EAROM is checked after the application program begins. If it fails, a message is displayed on the screen. No light indicators are given.

SECTION 5
SWITCHING POWER SUPPLY

GENERAL DESCRIPTION

The power supply is called a switching power supply because the output voltages from the output transformer are controlled by the switching of a d.c. input voltage to the primary of the transformer. Output voltage amplitudes are controlled by the duty cycle of the power switch that applies the primary voltage to the transformer. Figure 5-1 shows the simplified block diagram of the switching power supply. The error amplifier monitors the +5 volt output and, through the pulse width modulator, adjusts the power switch on to off ratio (to regulate the output voltage).

The power supply normally operates in a switching frequency range of 20 to 25 kilohertz. However, when the power supply output power is below 15 watts, the power supply goes into a discontinuous current mode, and the duty cycle and operating frequency decrease quite rapidly as the output power is further decreased. If no load is applied to the power supply, it operates in the audio frequency range.

INPUT BRIDGE

A full wave bridge circuit is used to convert the a.c. input voltage to the primary d.c. voltage of approximately 200 volts. A filter capacitor C1 provides a 16 millisecond holdover for the d.c. primary voltage. The 220 volt model (part number 28891232) made by Boschert Associates has dual input voltage capability. The input filter and bridge circuitry has been changed from the configuration of the 110 supply (see figure 5-2). When the jumper is removed for 220 volt input operation, the bridge and filter circuit produces approximately 310 volts to the primary of T1. When the jumper is installed for 110 volt input operation, the bridge and filter circuit form a voltage doubler to produce approximately 310 volts to the primary of T1. The operation of the two supplies is the same. The only differences (other than the input voltage doubler) are some component values to accomodate the higher input voltage to T1.

BIAS SUPPLY

The Bias Supply (see figure 5-3) is a linear regulator that provides the power to start and run the Pulse Width Modulator (PWM) oscillator circuit. The linear regulator also provides bias to the current limiting circuit and the opto isolator. During the start mode, Q1 is saturated and allows Q2 to provide a low but usable voltage to the PWM oscillator. When circuit voltages rise to an amplitude such that Q7 and Q8 are being adequately driven, the voltage across the primary (pins 5 and 6) rises. The rising voltage on pins 5 and 6 causes the voltage across the auxiliary windings (pins 1, 2, 3, and 4) to rise, so that when the amplitude is sufficient to forward bias CR6, collector current flows in Q2. The voltage on the bias supply rises until Zener diode CR5 conducts, clamping the base of Q1 to 10V ±1V. The voltage on the collector of Q2 is nominally 25 volts.

PULSE WIDTH MODULATOR (PWM)

The PWM oscillator is built around the 555 timer IC operating in the astable oscillator mode. This circuit performs the switch modulation of the supply (see figure 5-3).

The charging time of C4 (the timing capacitor) is inversely proportional to the current through R3, which is proportional to the input voltage. When C4 charges up to 2/3 of the bias supply voltage (8.8 ±1V), the 555 timer IC changes states, shorting pin 7 to pin 1 (primary circuit ground), thereby starting the discharge cycle. C4 is discharged through a constant current source whose value is proportional to the voltage at the base of Q3 (the duty cycle control voltage point). When the voltage on C4 decreases to 1/3 of the bias supply voltage, the 555 timer changes states again, releasing pin 7, turning off the discharge current source, and allowing the charge current to flow through CR7 and C4 and thus beginning the cycle again.

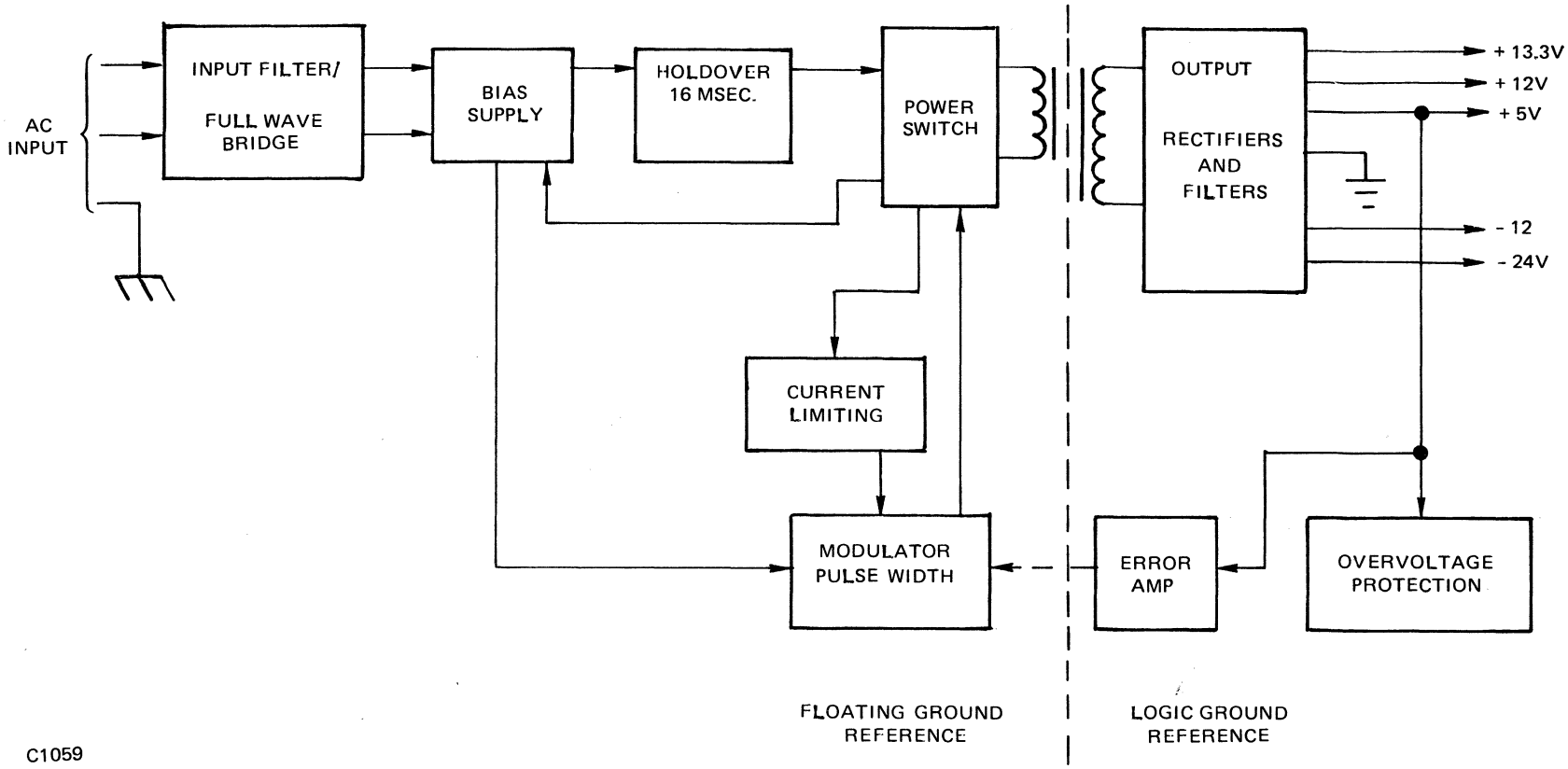
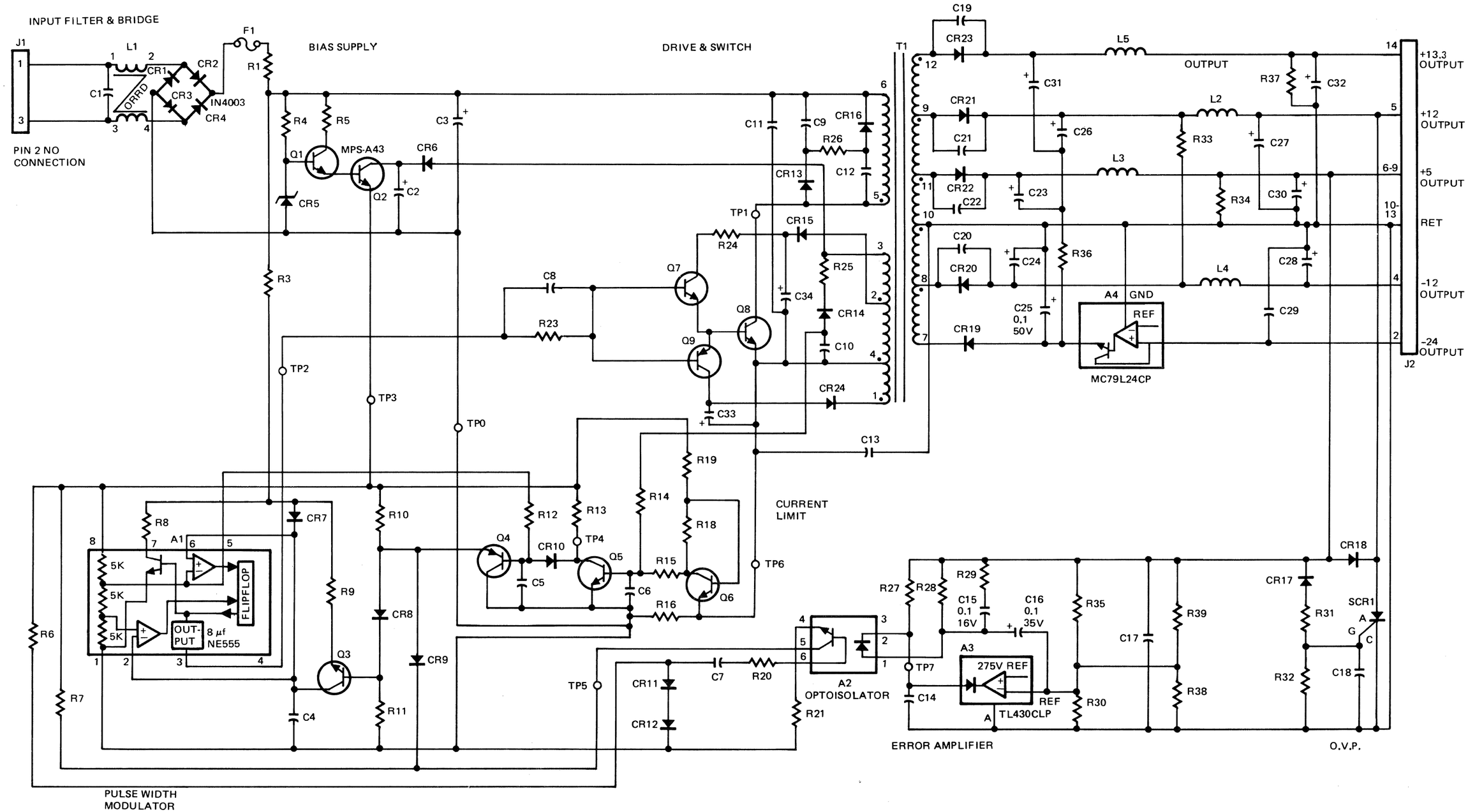


Figure 5-1. Switching Power Supply, Simplified Block Diagram



C1060

Figure 5-2. Power Supply Diagram 110/220 Volts

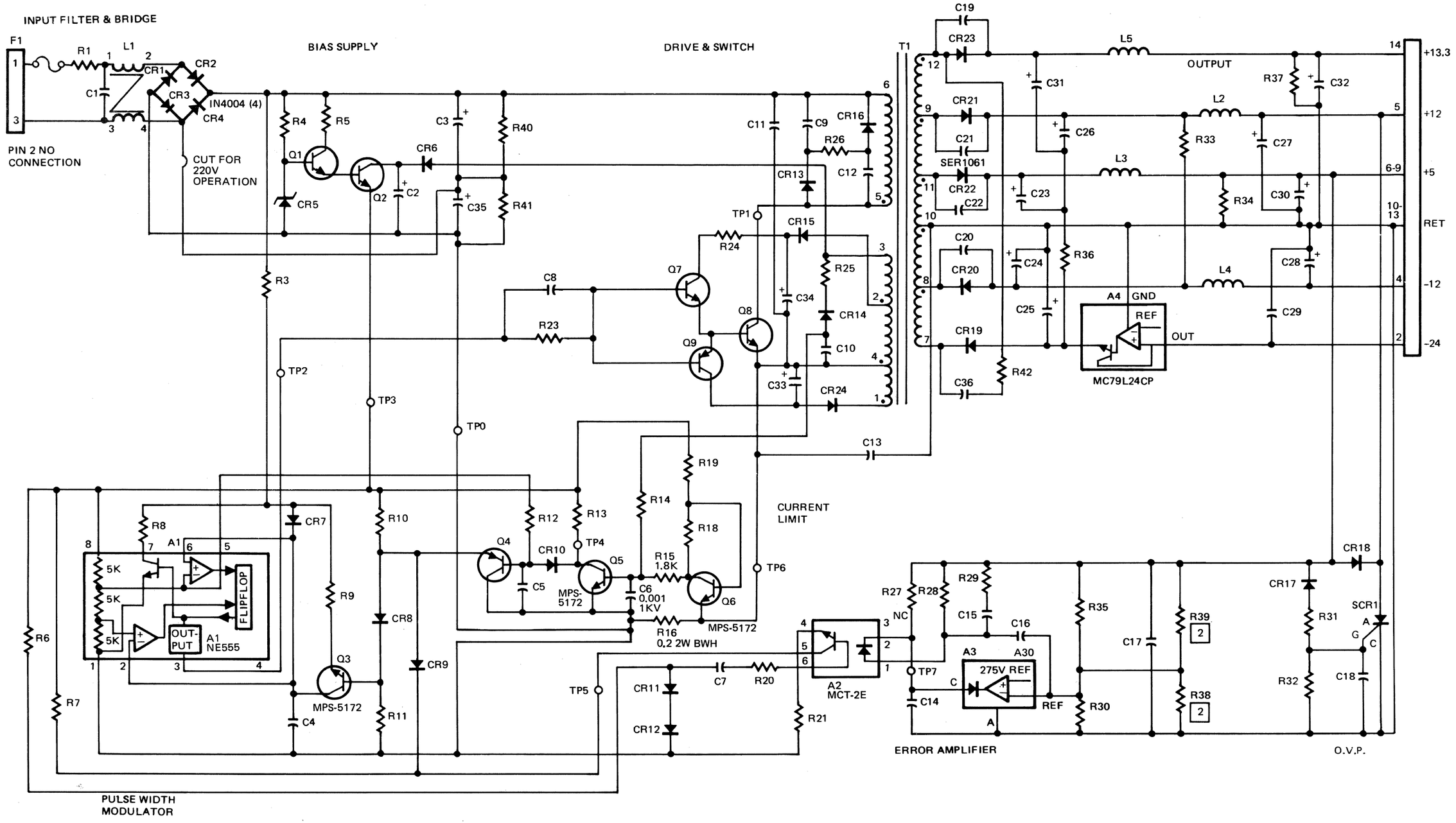


Figure 5-3. Power Supply Diagram (110 volt)

POWER SWITCH

The function of this circuit is to apply the input voltage to the primary of the transformer when the output of the PWM oscillator is positive (pin 3 of A1 in figure 5-3), and to disconnect the input voltage from the primary winding when the output of the PWM oscillator is negative (ground). When pin 3 of A1 rises, positive current flows through R23 and Q7 (base to emitter) into the base of Q8, turning it on. Once the voltage on pin 2 of T2 rises sufficiently to cause CR15 to conduct, the base drive of Q8 rises to its final value. When the output of the PWM oscillator goes negative, Q7 no longer conducts, turning off the base drive current to Q8. When the base voltage of Q7 and Q9 go negative, Q9 conducts shunting the base of Q8 to the -5 volt supply on C33, turning Q8 off.

CURRENT LIMIT

The current limit circuit is a peak detecting type of circuit that compares the current that is flowing in the power switch to a reference. When the current exceeds the reference, the output (Q5) sinks current to the ground, causing the duty cycle control voltage to decrease.

The magnitude of the control voltage, on the base of Q3, is proportional to the output voltage. Thus, when the control voltage fails, the output voltage falls, and the power supply current is limited. The output voltage is fed back by means of R14, giving the input and output power the fold back characteristic.

+5 VOLT ERROR AMPLIFIER

The error amplifier senses the +5 volt output, compares it with its internal reference, and sinks current proportional to the error between the two voltages. The current the amplifier sinks drives the opto coupler Light Emitting Diode (LED), which causes its output transistor to conduct and adjust the duty cycle control voltage point. A low 5 volt voltage causes the error amplifier to drive the opto coupler with a little less current, which causes the duty cycle control voltage to rise, which causes the output voltage to rise and stabilize. The error amplifier has local feedback C15, 16, and R27, 29, and 30, which stabilize the control loop of the power supply.

OVERVOLTAGE

This circuit senses the +5 volt voltage and turns on the SCR to "crowbar" the +5 and +12 volt output to ground when the +5 exceeds the preset overvoltage level. The SCR is activated when the 5 volt supply line exceeds the Zener (CR27, figure 5-3) voltage plus the SCR gate to cathode regeneration voltage set by the divider ratio of R31 and R32.

VOLTAGE REFERENCE GROUND, VOLTAGE ISOLATION AND THE USE OF ELECTRICAL TEST EQUIPMENT

The switching power supply has three grounds, as shown in figure 5-4. The primary input power to the terminal is provided by means of three wires, two of which provide the a.c. input voltage, and the third wire (first ground) (green) is connected to the "Earth" ground at the building power distribution box. The green wire is attached to the terminal chassis. After the a.c. voltage enters the power supply, it is rectified by a diode bridge and then charges an electrolytic capacitor. The cathode of this capacitor defines the internal primary circuit ground (second ground).

CAUTION

The potential of the circuit ground is different from the green wire ground potential. Therefore, when using an oscilloscope or other measuring equipment to measure voltage potentials, electrical isolation must be provided between the power supply and the equipment through the use of measuring equipment capable of making a floating measurement, or by applying power to the supply through an isolation transformer.

WARNING

The primary ground is floating at line voltage: A shock hazard exists.

The third ground is defined by the secondary winding of the output transformer. This ground is electrically isolated from the other two grounds, and is referred to as the "Logic" ground.

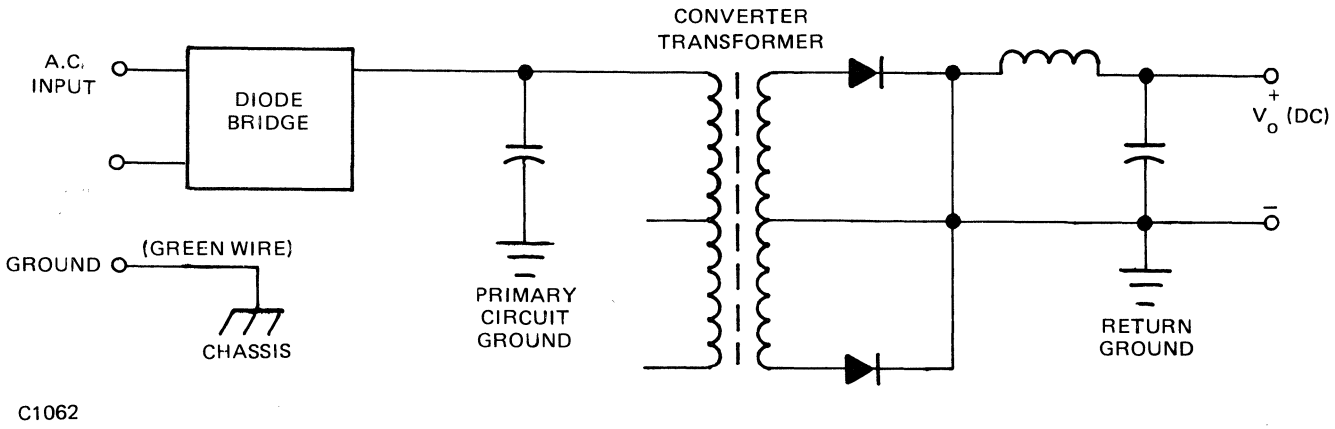


Figure 5-4. Grounding Illustration

Test to Determine if Maintenance is Required

Check the output voltages at the backplane pins shown in figure 5-5 to determine if they are within the following specifications (in volts):

a. +5.1 ±5% 5.35 to 4.84

b. +13.3 ±10% 14.63 to 11.97

c. +12.0 ±10% 13.1 to 10.8

d. -12.0 ±10% -13.2 to -10.8

e. -24.0 ±7.5% -25.8 to -22.2

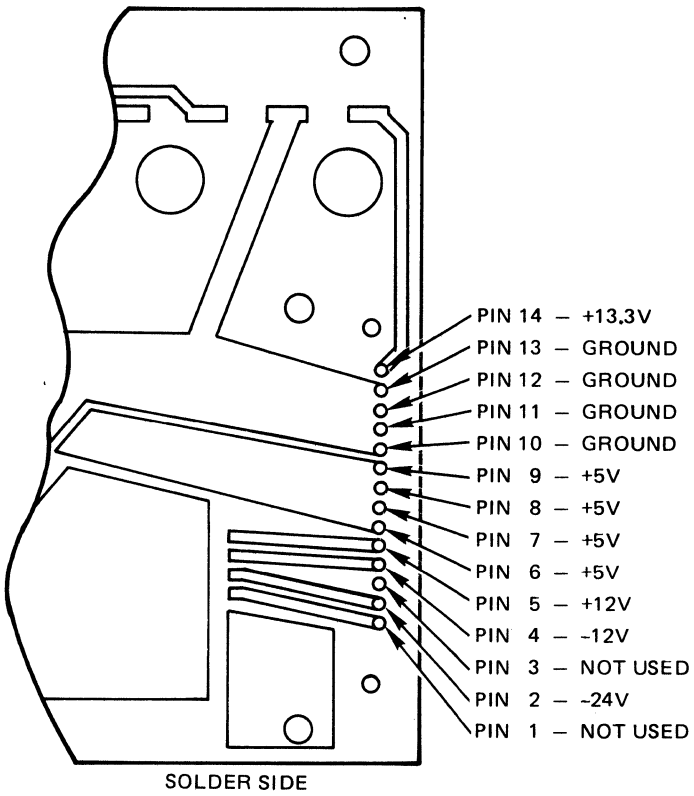


Figure 5-5. Voltage Check Points

TROUBLESHOOTING PROCEDURE

1. Remove power supply from all sources of power and load connections. Visually inspect unit for abnormalities.

2. With a Volt-Ohm Meter, check the impedance of fuse F1, Q8 collector-emitter, CR19 through CR23.

Description	Proper Impedance
Fuse F1	<1Ω
Q8 Collector Positive	>10K
CR19 Through CR23 Cathode Positive	>40Ω

3. Reconnect the power supply to the terminal with the P/S, Video, and SIO boards removed and the CRT driver power disconnected. Observe the waveform of test points 1 through 6 with respect to test point 0. Observe the waveform of test point 7 with respect to secondary return. The test point waveforms are to correspond to the photographs 1 through 8 of figure 5-6. Photographs 9 and 10 are of test point 4 and 5 when the power supply is in current limit. Figure 5-7 shows test point locations on the back of the P.C.B.

4. Use the waveforms (at the test points) and the following troubleshooting flow diagram (figure 5-8) to locate the circuit group that has the malfunction.

ADJUSTMENTS

Under normal conditions, no adjustments are required. At the time of manufacture, R39 and R38 (figure 5-3) are selected so that the output voltages are within specifications. If maintenance is performed on the power supply, it may become necessary to reselect these parts to maintain proper output voltages (refer to the Parts List in the Test and Field Documentation).

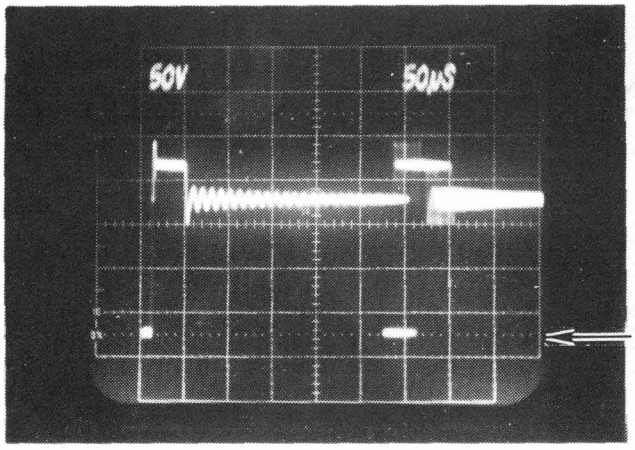
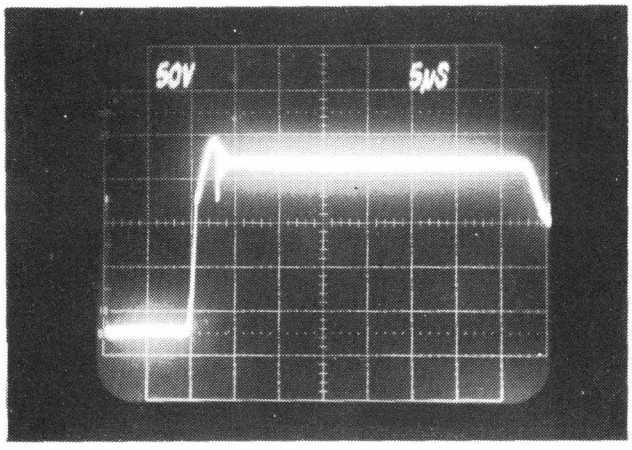


PHOTO NO.

1

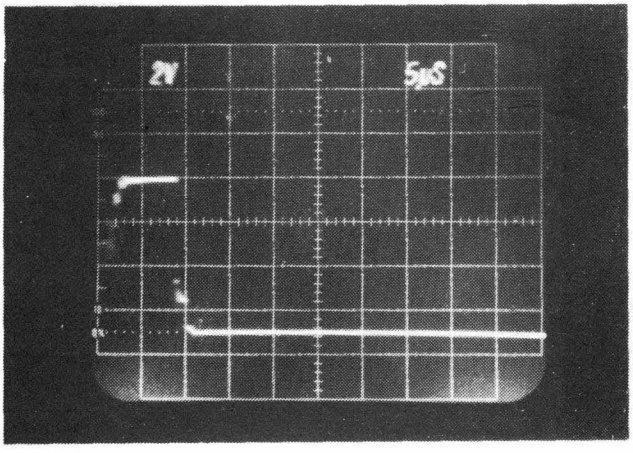
TEST POINT ONE
VERTICAL 50V/DIV
HORIZONTAL 50 µS/DIV

OV. REF.
(TYPICAL)



2

TEST POINT ONE
VERTICAL 50V/DIV
HORIZONTAL 5 µS/DIV



3

TEST POINT 2
VIRTICAL 2V/DIV
HORIZONTAL 5 µS/DIV

C1064/1

Figure 5-6. No Load Test Point Waveforms (Sheet 1 of 4)

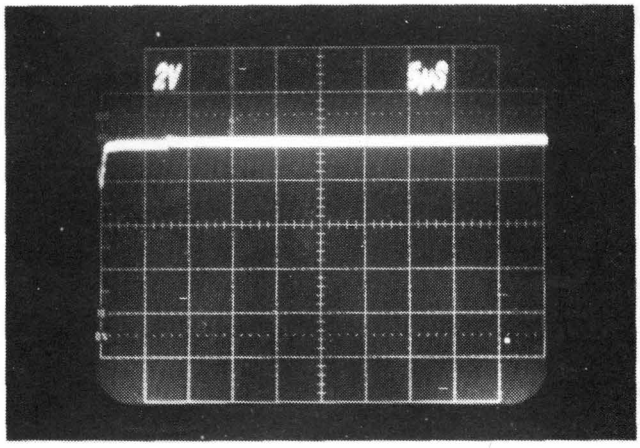
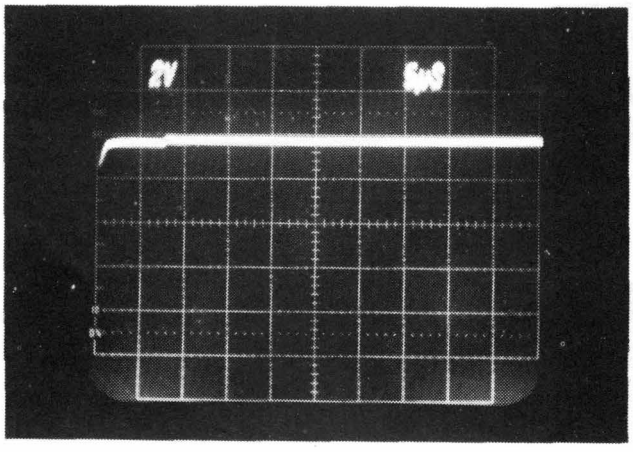
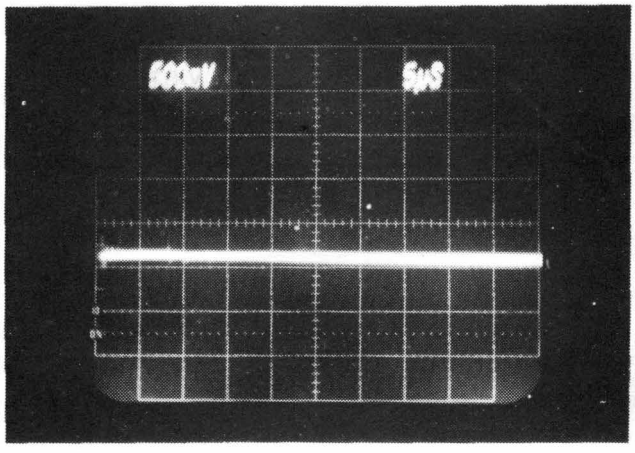


PHOTO NO.	
4	TEST POINT 3 VERTICAL 2V/DIV HORIZONTAL 5 μS/DIV



5	TEST POINT 4 VERTICAL 2V/DIV HORIZONTAL 5 μS/DIV



6	TEST POINT 5 VERTICAL 0.5V/DIV HORIZONTAL 5 μS/DIV

C1064/2

Figure 5-6. No Load Test Point Waveforms (Sheet 2 of 4)

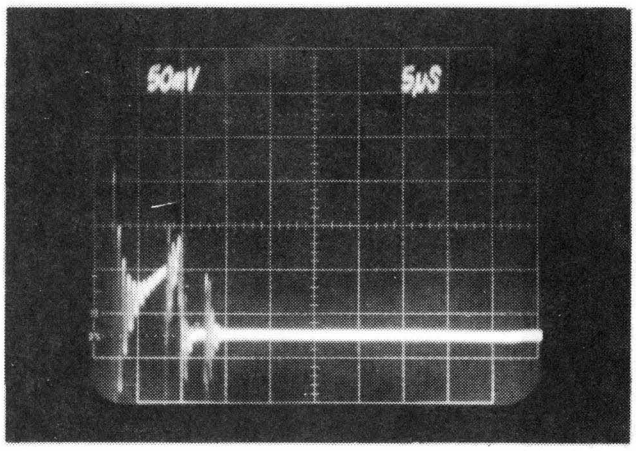
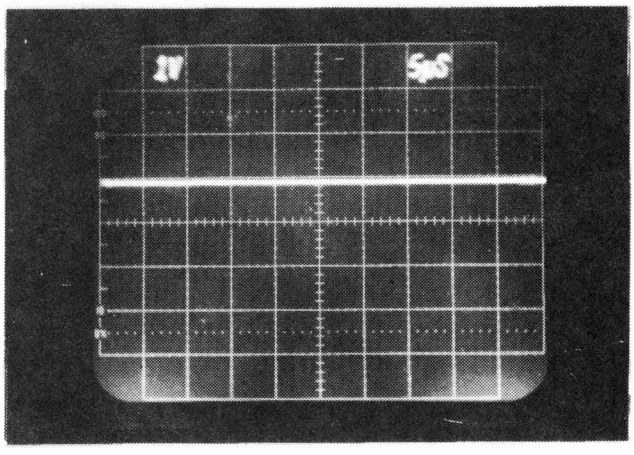


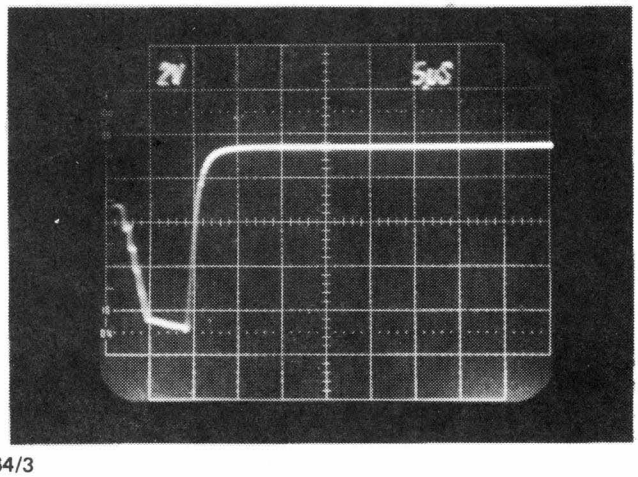
PHOTO NO. 7

TEST POINT 6
VERTICAL 50MV/DIV
HORIZONTAL 5 μS/DIV



8

TEST POINT 7
VERTICAL 1V/DIV
HORIZONTAL 5 μS/DIV



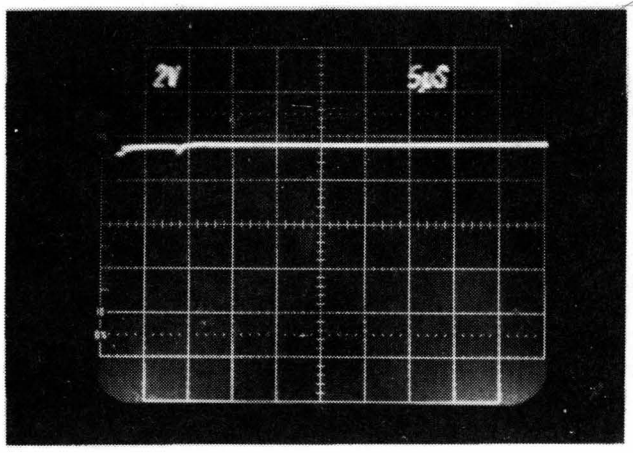
9

TEST POINT 4
POWER SUPPLY IN CURRENT LIMIT.

VERTICAL 2V/DIV
HORIZONTAL 5μS/DIV

C1064/3

Figure 5-6. No Load Test Point Waveforms (Sheet 3 of 4)



C1064/4

PHOTO NO.
10

TEST POINT 5
POWER SUPPLY.IN
CURRENT LIMIT

VERTICAL 2V/DIV
HORIZONTAL 5 μS/DIV

Figure 5-6. No Load Test Point Waveforms (Sheet 4 of 4)

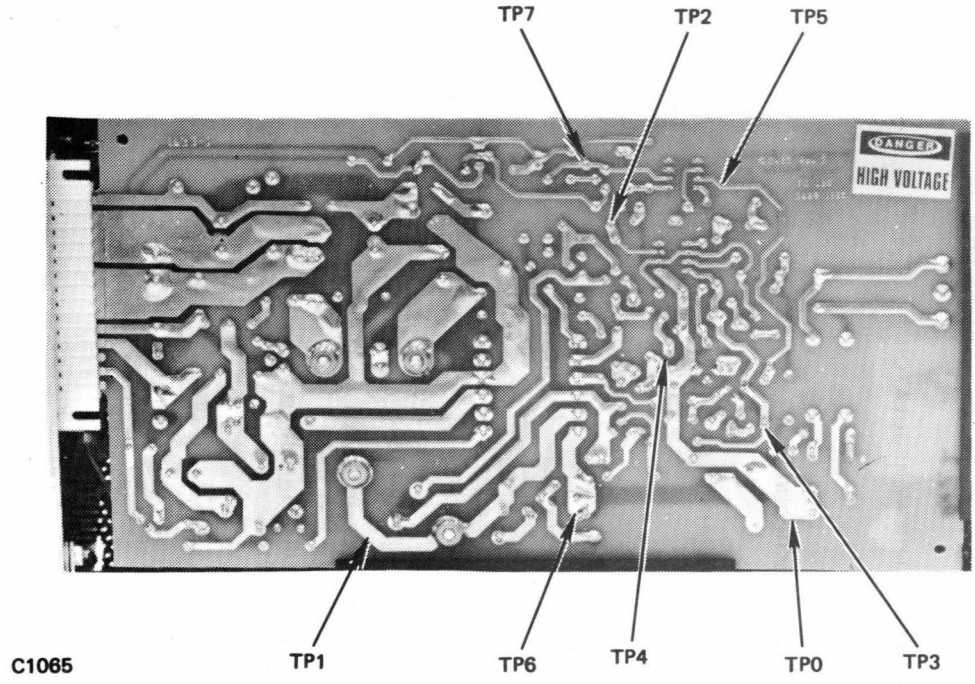


Figure 5-7. Power Supply Test Points

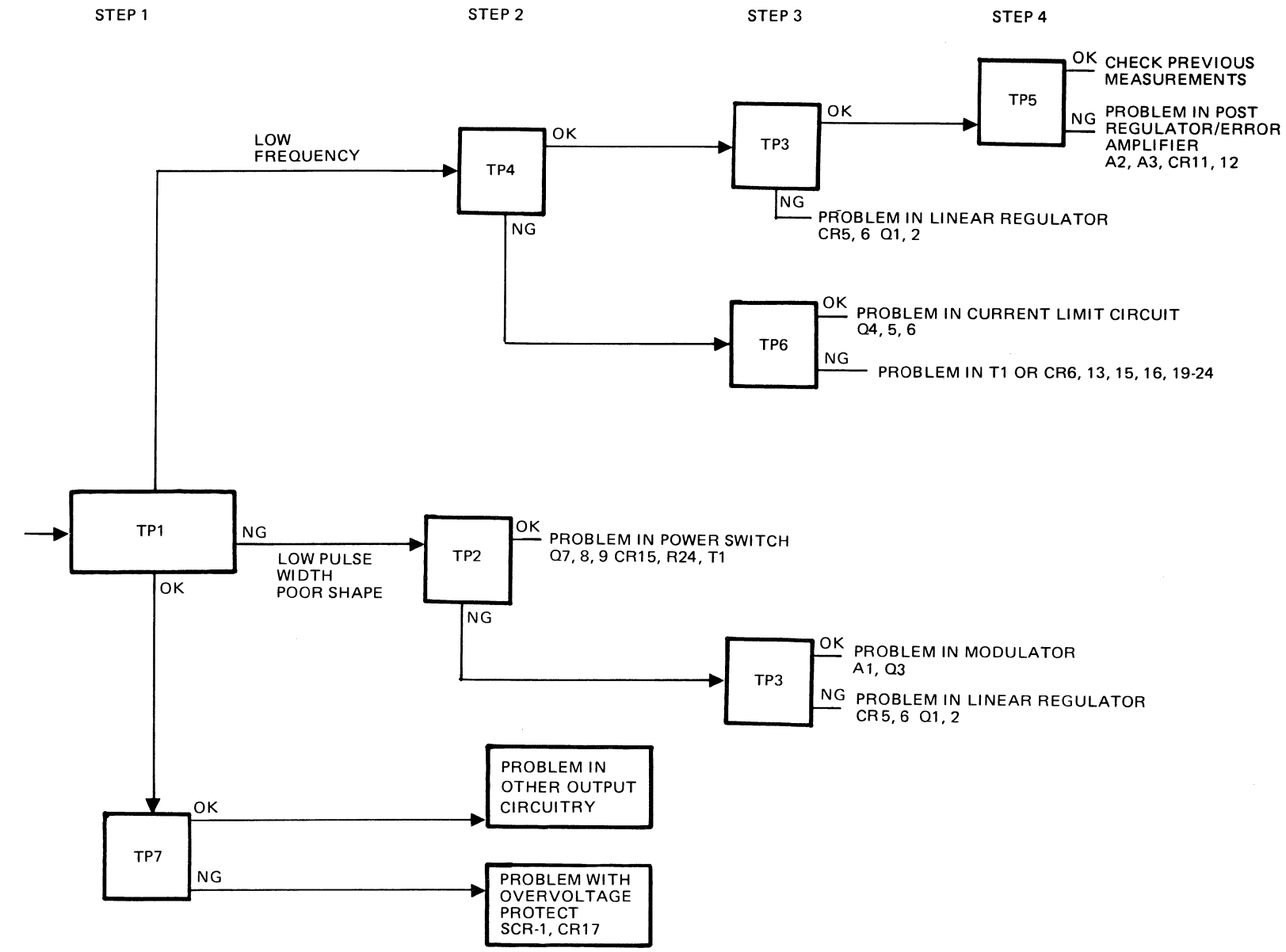


Figure 5-8. Troubleshooting Flow Diagram

POWER SUPPLY REPLACEMENT

Refer to figure 5-9 throughout the following procedures for removal and installation of the power supply. Ensure that the terminal is disconnected from a.c. power before proceeding.

Removal

1. Remove the plate covering the power supply.
2. Loosen the screws on the bracket at the right end of the power supply and slide the bracket aside (screws located at (1) and (2) in figure 5-9).
3. Pull the power supply circuit board to the right until it is clear of the edge connector ((3) in figure 5-9).
4. Tilt the top of the power supply outward and remove the power plug on the right of the component side of the board. Lift out the power supply.

Installation

1. Connect the power plug to the circuit board.
2. Place the edge of the circuit board on the guide (4) at bottom of the chassis and slide it to the left until the board is fully seated in the edge connector.
3. Move the bracket at the right back into place and tighten screws (1) and (2).
4. Replace the cover plate.

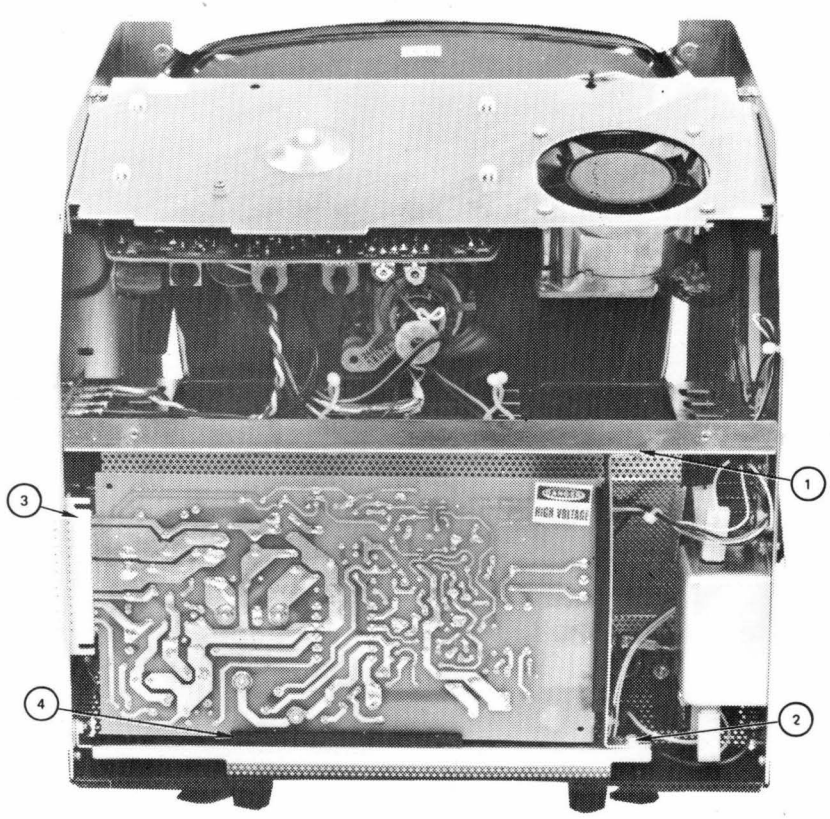


Figure 5-9. Power Supply Replacement

SECTION 6
CRT DRIVER

GENERAL DESCRIPTION

The function of the Cathode Ray Tube (CRT) driver is to take the composite video signal from the display board and generate the proper control signals needed to create a visual display on the CRT. Refer to figure 6-1 for a block diagram of the display board and CRT.

INPUT VOLTAGE REGULATOR

Figure 6-2 shows a block diagram of the voltage regulator circuit. The circuit consists of a series pass transistor Q901, an error detection amplifier, and control driver. The output voltage (Vo) is sampled by the error detection amplifier and compared to a reference voltage set by R903. If a change occurs in the Vo due to a change in load or a change in input voltage, then an error signal is generated by the error detector. This error signal is amplified by the control driver which increases or decreases the base current of Q901 as required to bring Vo back to its proper value, thus eliminating the error signal. R903 is a variable resistor used to adjust the +B voltage.

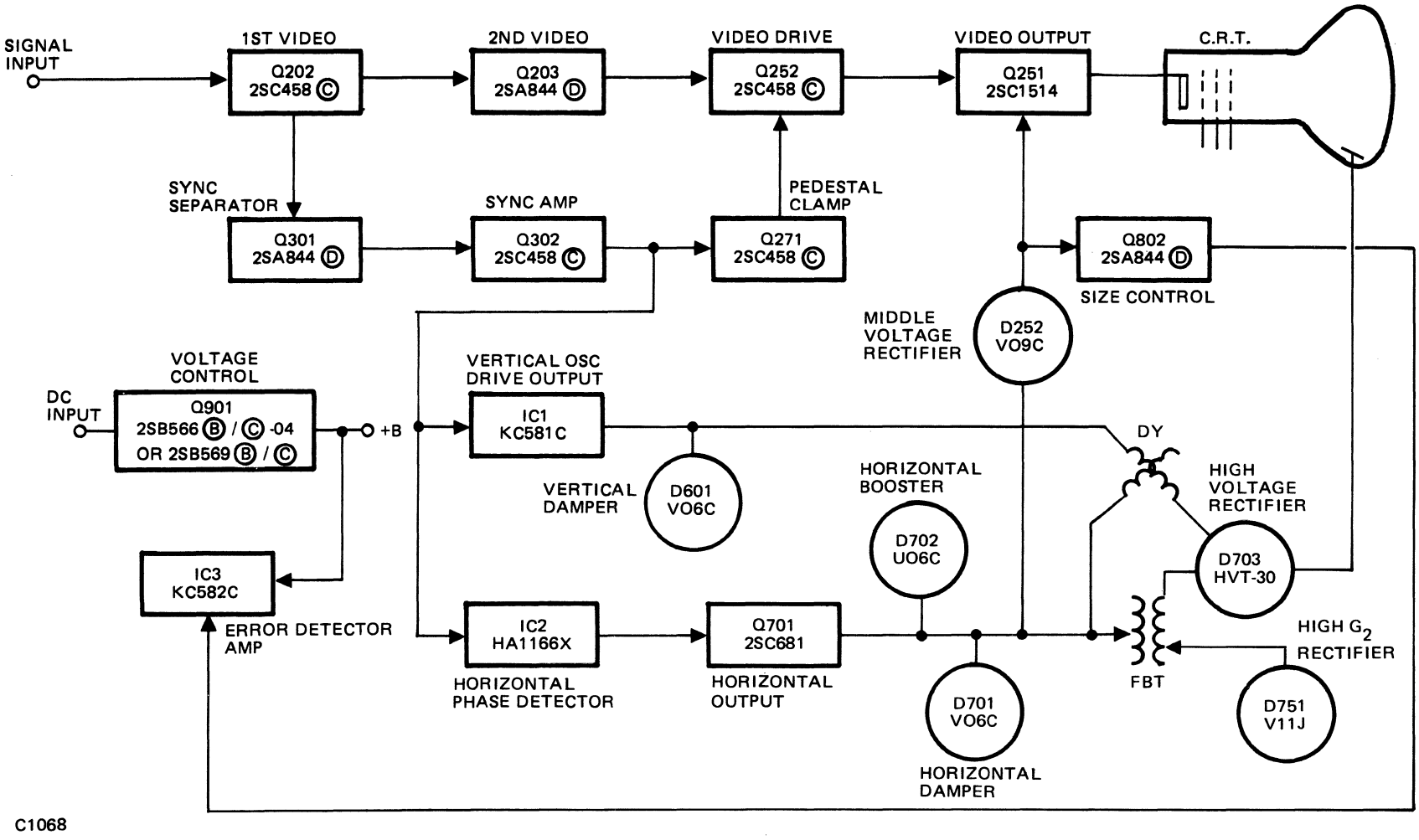


Figure 6-1. Display Board Block Diagram

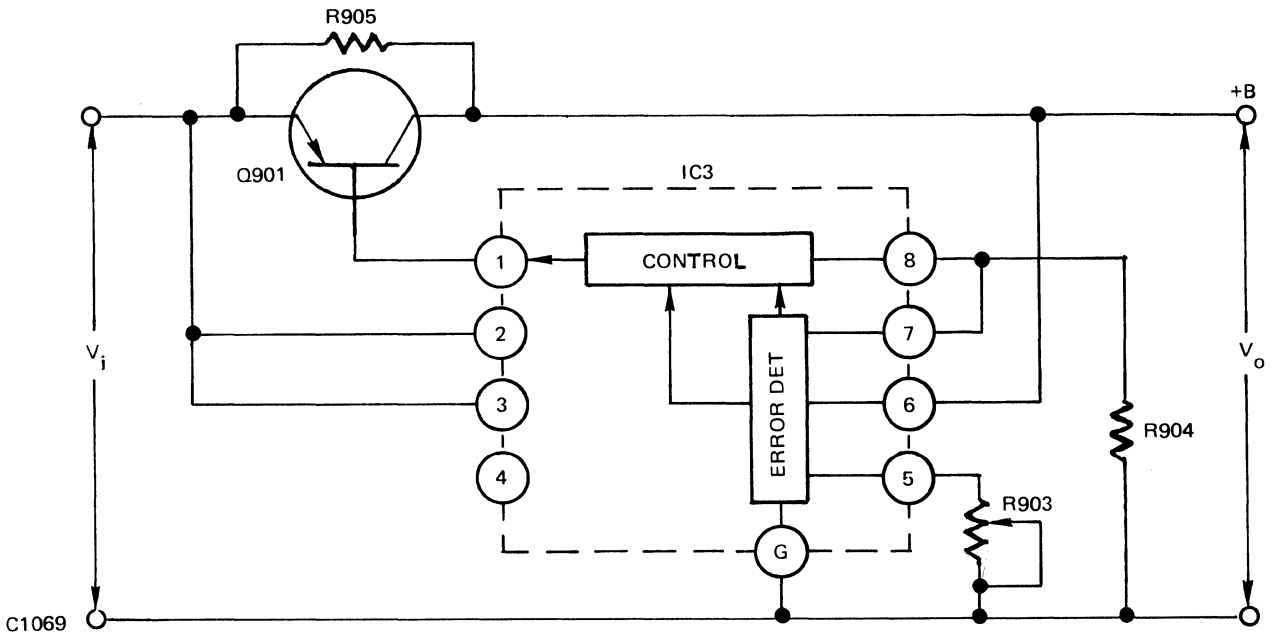


Figure 6-2. Input Voltage Regulator Functional Diagram

VIDEO AMPLIFIER CIRCUIT

The video amplifier circuit of this display unit is shown in figure 6-3. The input section of the video amplifier is a direct-coupled feedback amplifier composed of transistors Q202 and Q203. The output section is composed of common base amplifier Q251 and driver Q252. The dc component of the video signal is set by the back porch clamping circuit of Q271. The clamping voltage of Q271 sets the overall brightness of the picture and is adjusted by R265. Gain of the video amplifier is controlled by the contrast control R213.

SYNC CIRCUIT

Refer to figure 6-4 for a diagram of the sync circuit. Q301 operates as a sync separator. The peaks of the sync signals are made even through the clipping action of Q301. Picture signals are blocked by C301, which is charged by the base current of Q301 when Q301 conducts. The sync signals are amplified by amplitude limiter Q302. Sync signals are supplied from the emitter of Q302 to vertical and horizontal circuits, and to the back porch clamping circuit.

SIZE CONTROL CIRCUIT

Without control of the high voltage, the picture size on the CRT would vary according to the picture brightness because of high voltage variations (refer to figure 6-5). Both the vertical and horizontal sizes are kept nearly constant by the voltage control circuit with negative feedback +B compensation. The size control circuit forms a feedback loop from the high voltage to the error amplifier in the voltage control circuit. The range of the feedback is controlled by middle voltage variations that are amplified by Q802. Middle voltage variation is proportional to high voltage variation.

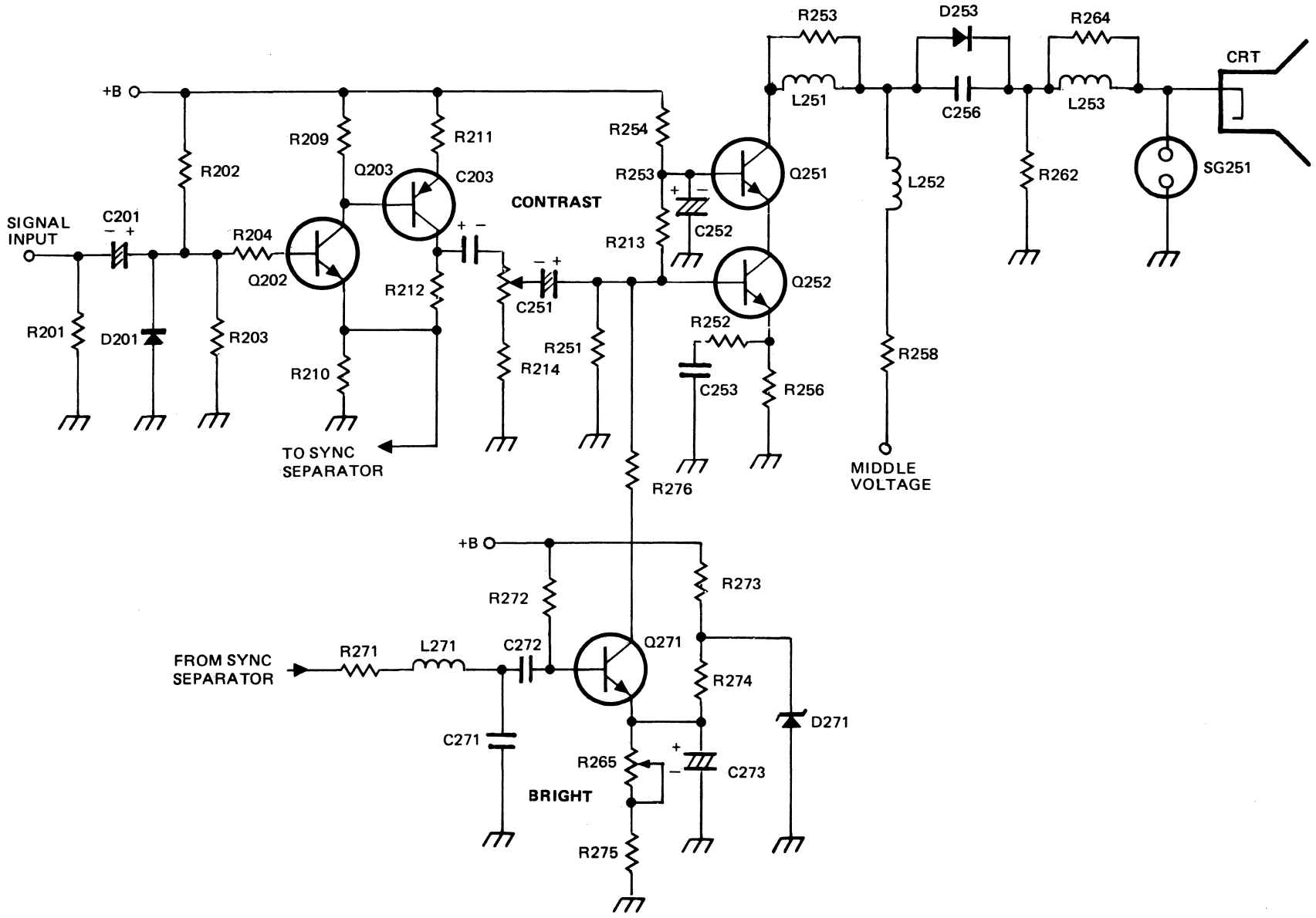


Figure 6-3. Video Amplifier Circuit

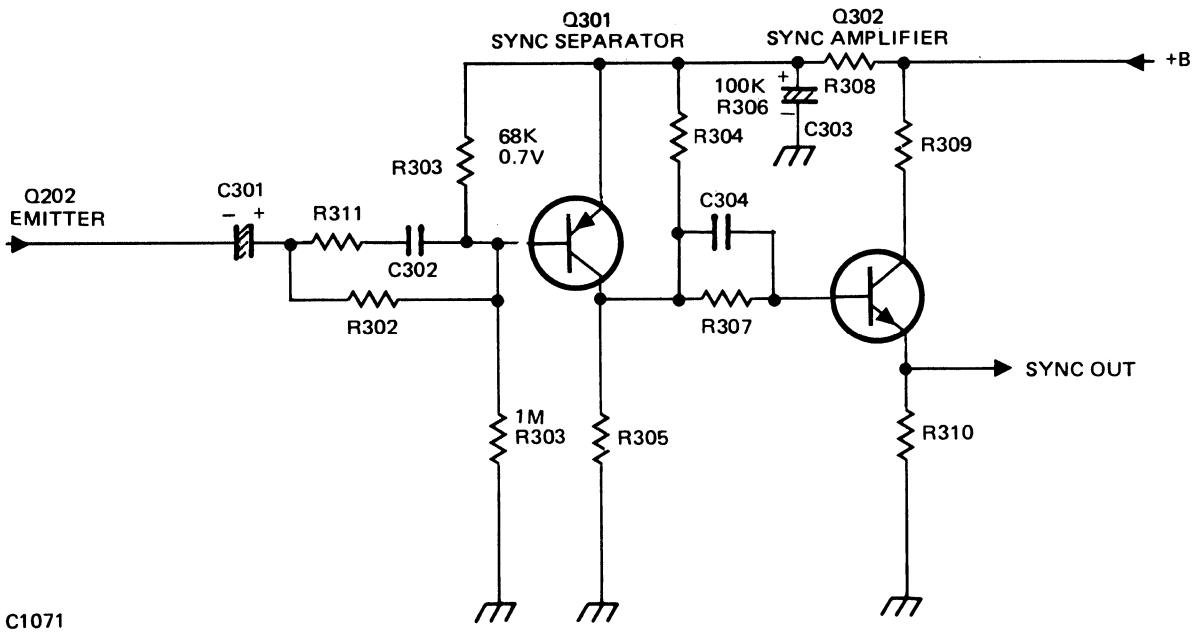


Figure 6-4. Sync Circuit

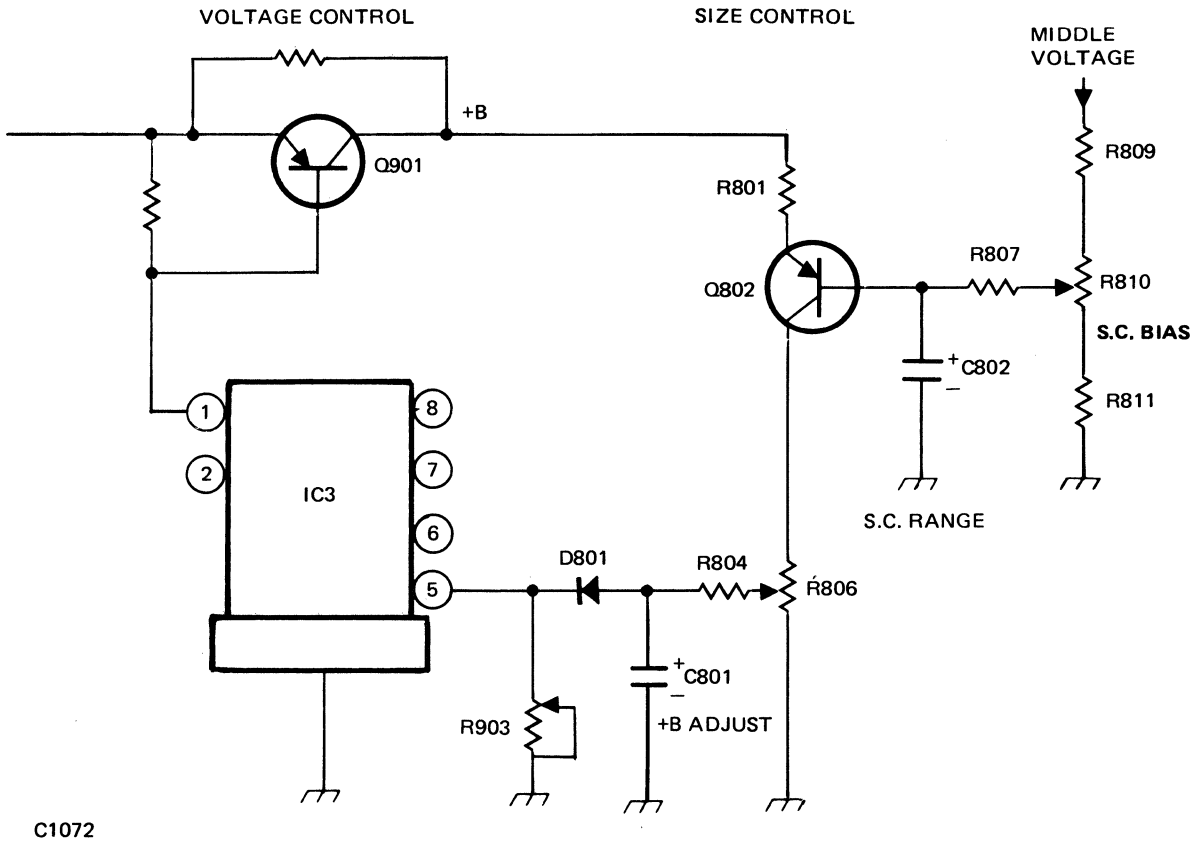


Figure 6-5. Size Control Circuit

VERTICAL DEFLECTION CIRCUIT

The vertical deflection circuit consists of an oscillating circuit, which is synchronized with the vertical sync signal, and an output amplifier circuit. The output amplifier takes the voltage sawtooth waveform from the oscillator, amplifies it, and applies a current sawtooth waveform to the deflection yoke.

Referring to figure 6-6, the sync signal is applied at terminal A, and the vertical sync signal is separated by R601, C601, R602, C602, R614, and applied to pin two of the integrated circuit. This signal is amplified by the sync amplifier and is applied to the vertical oscillator. The oscillating circuit is of the RC type, oscillating according to the time constant determined by C605, R603, and R604. The output of the oscillator is a pulse which is converted to a sawtooth by C606 and R605. Size correction and lineation of the sawtooth waveform is performed by the wave shaping circuit. The corrected waveform is applied to the output amplifier where the power is developed to drive the vertical deflection coils.

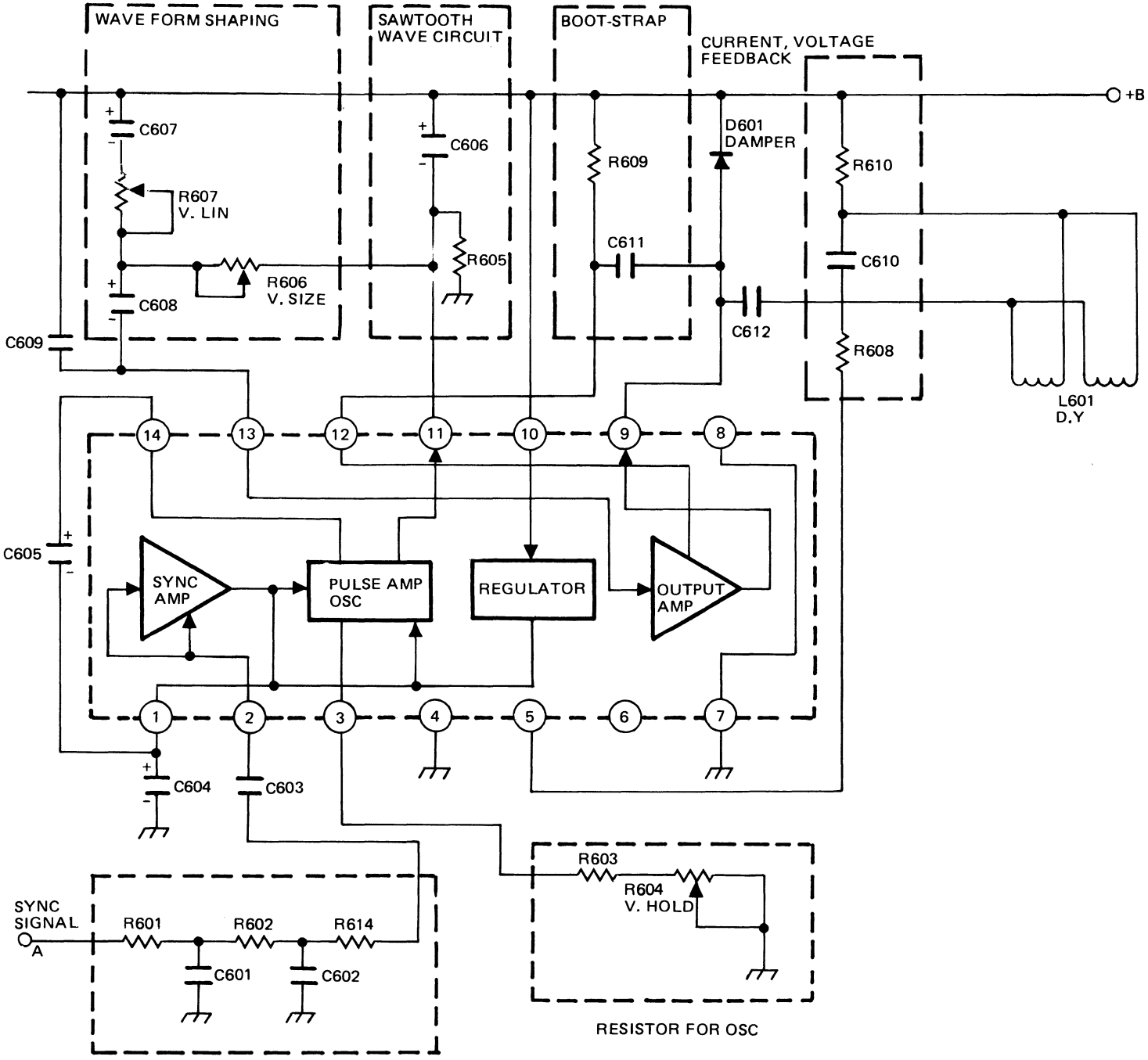


Figure 6-6. Vertical Deflection Circuit

HORIZONTAL DEFLECTION CIRCUIT

This circuit is based on an integrated circuit which incorporates the functions of phase detection, filter circuits, oscillation, and drive. In the following discussion, refer to figure 6-7. A sample of the horizontal drive is compared with the horizontal sync signal in the phase detector. The output from the phase detector is modified by the integrator and frequency control circuitry and is used as a control input to the horizontal oscillator. The output of the oscillator through the horizontal drive is fed to two transformers. One output provides the drive to transistor Q701. Q701 drives the horizontal deflection coils. The second output is applied to the flyback transformer, which provides the high voltage for the CRT anode and focus voltage. The focus voltage is applied to the focus grids of the CRT to provide electrostatic focusing of the electron beam.

SAFETY PRECAUTIONS

WARNING

Service should not be attempted by anyone unfamiliar with the necessary precautions when working on the CRT driver circuits.

The following precautions should be observed:

1. Do not install, remove, or handle the picture tube in any manner unless shatter-proof goggles are worn. People not so equipped should be kept away while picture tubes are handled. Keep the picture tube away from the body while handling.

2. Before removing the anode cap, always be sure to connect the anode of the CRT to ground and confirm that the high voltage potential has actually been discharged.

3. When replacing a chassis in the cabinet, always ensure that all the protective devices such as barriers, non-metallic knobs, and adjustment and compartment covers or shiels are put back into place.

4. When service is required, observe the original lead dress. Extra precautions must be taken to assure correct lead dress in the high voltage circuitry area.

5. Always use the Burroughs recommended replacement component. Especially critical components (so indicated on the circuit diagram in the Test and Field Reference documents) should not be replaced by other makes. When a short circuit has occurred, replace those components that indicate evidence of overheating.

6. Before returning a serviced unit to the customer, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock, and be sure that no protective device built into the instrument by the manufacturer has become defective or inadvertently defeated during servicing.

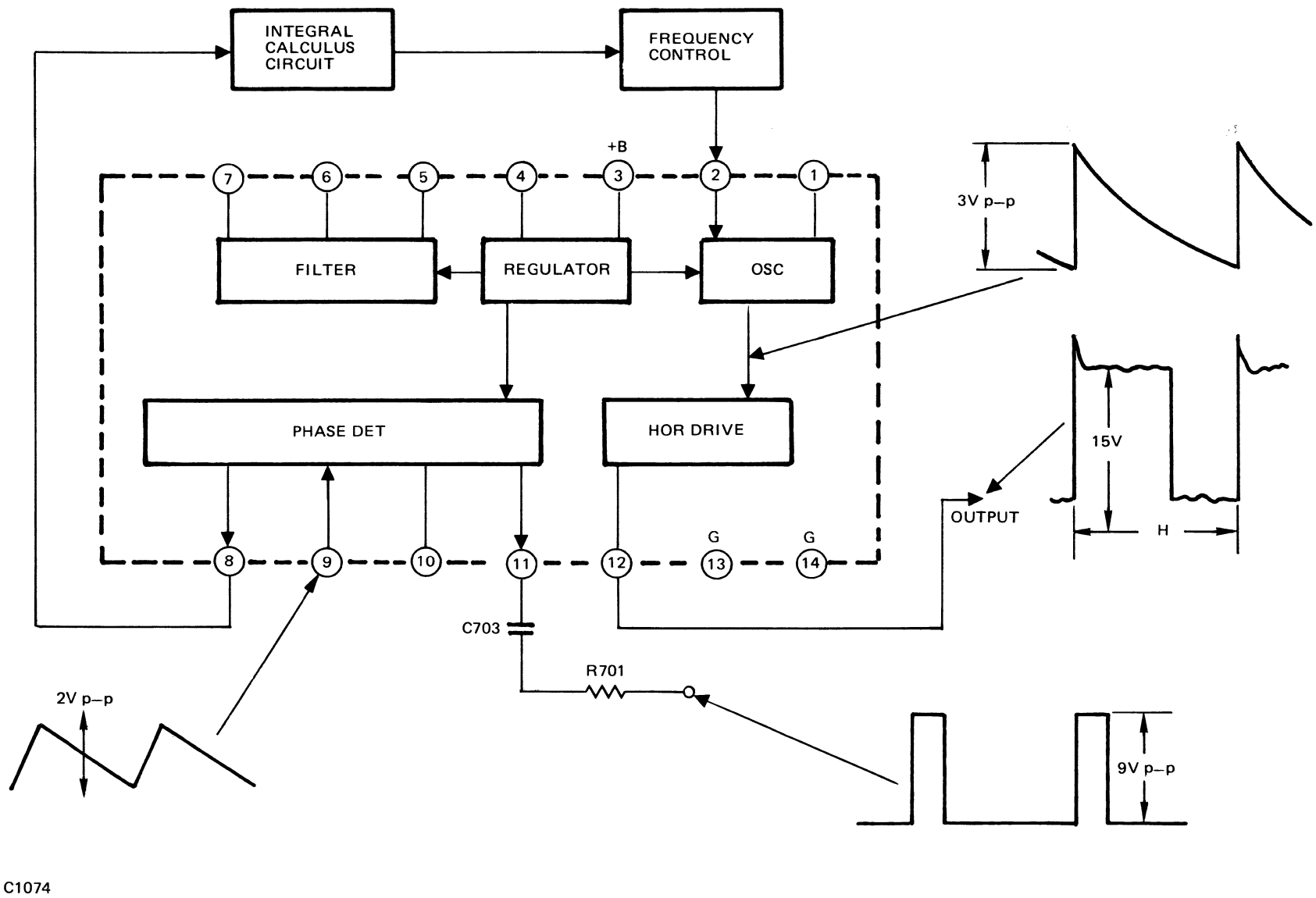


Figure 6-7. Horizontal Deflection Circuit

TROUBLESHOOTING

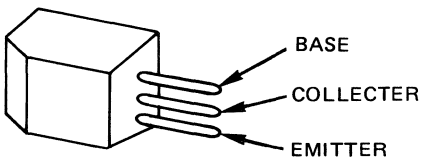
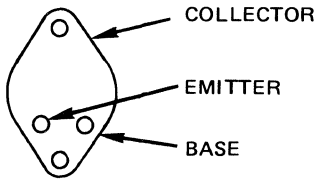
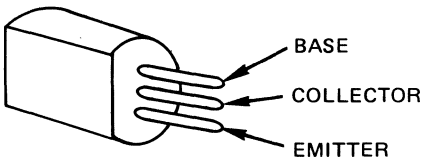
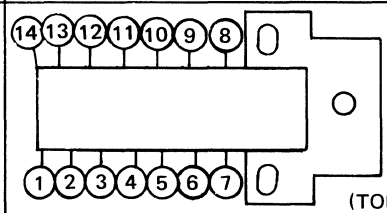
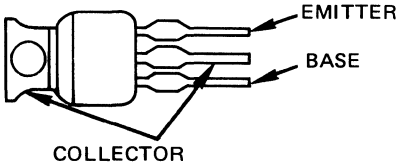
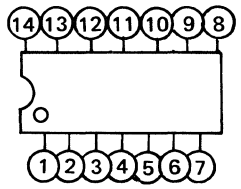
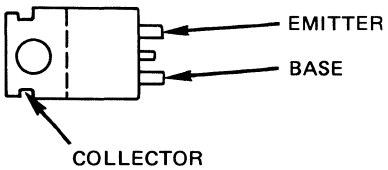
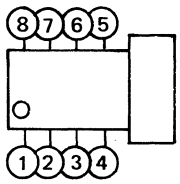
This describes how to replace defective components in the display unit. A defective component can be determined by following the inspection procedures outlined here after confirming a symptom by observing the terminal screen.

1. Carefully observe the video symptom and single out, from the list of symptoms, the particular symptom identical with (or similar to) the symptom observed on the screen.

2. Turn to the sheet indicated by the symptom on the symptoms list.

3. After carefully reading the description on troubleshooting, proceed with the inspection by following the procedures directed by the arrows.

Refer to figure 6-8 for IC and transistor pin connections. Pictures 1 through 9 of figure 6-9 are of typical waveforms found in the CRT driver circuits.

VIEW	TYPE	VIEW	TYPE
	2SC458 2SA844		2SC681
	2SC458 2SC844		KC581C
	2SC1514		HA1166X
	2SC566-04 2SC565		KC582C

C1075

Figure 6-8. Transistor and IC Description

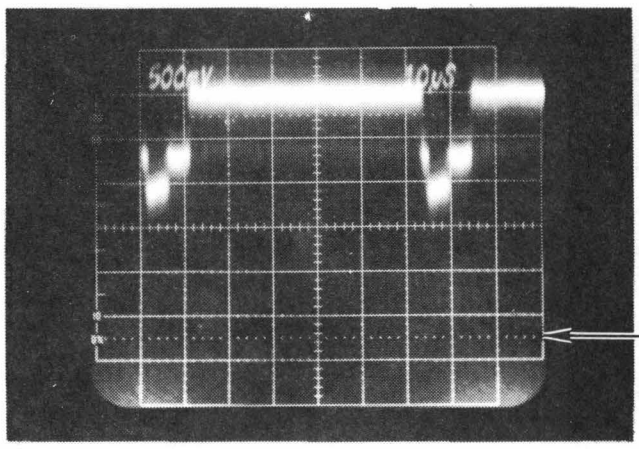
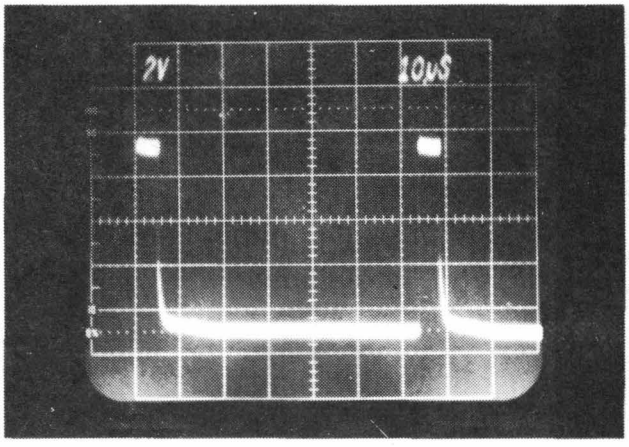


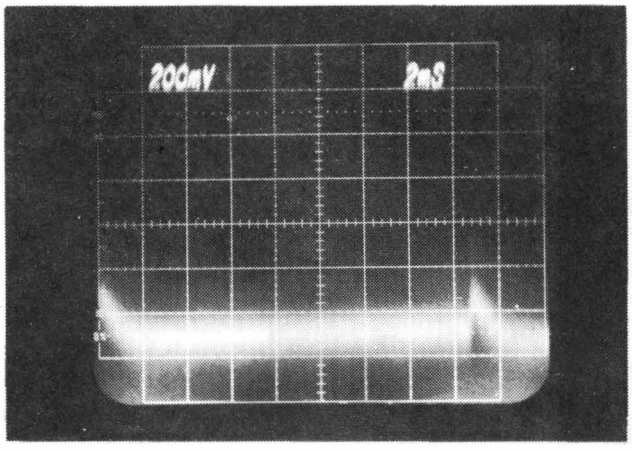
PHOTO NO.
1

Q 202 EMITTER
WITH THE SCREEN
IN NEGATIVE VIDEO



2

Q302 EMITTER



3

IC1 PIN 2
SCOPE SET FOR A.C.
INPUT

C1076/1

Figure 6-9. Typical CRT Driver Circuit Waveforms (Sheet 1 of 3)

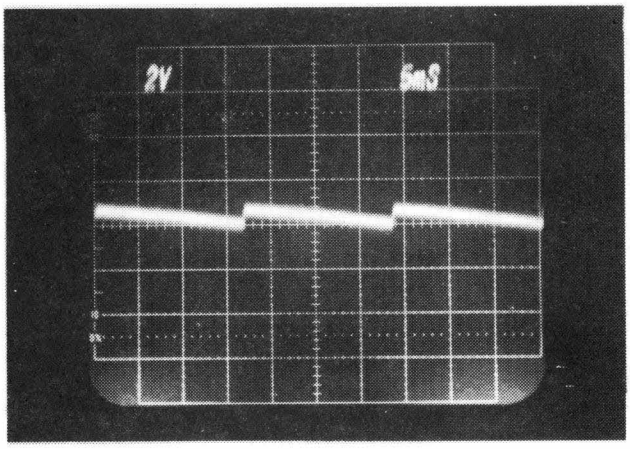
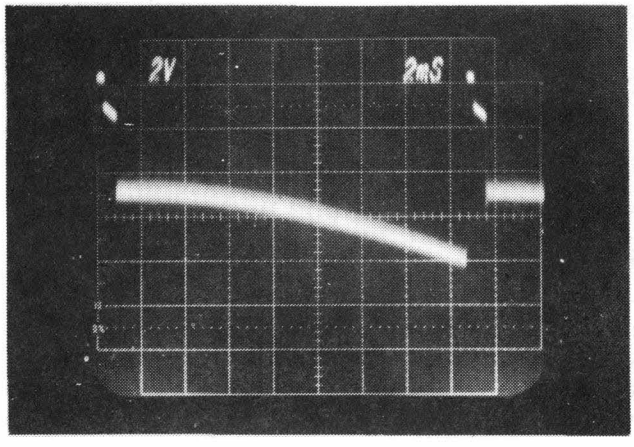


PHOTO NO.

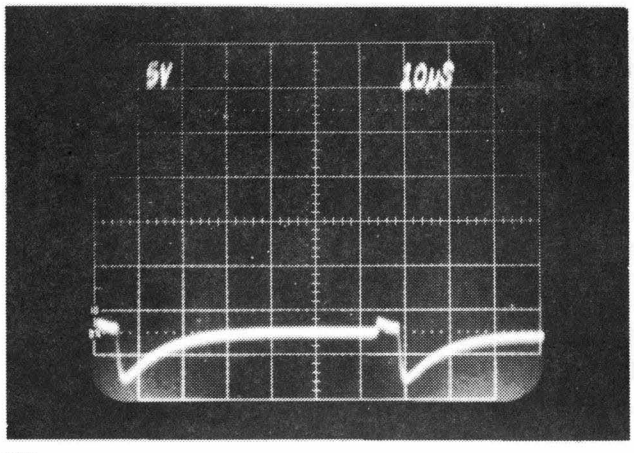
4

IC1 PIN 13



5

IC1 PIN 9



6

IC2 PIN 11

C1076/2

Figure 6-9. Typical CRT Driver Circuit Waveforms (Sheet 2 of 3)

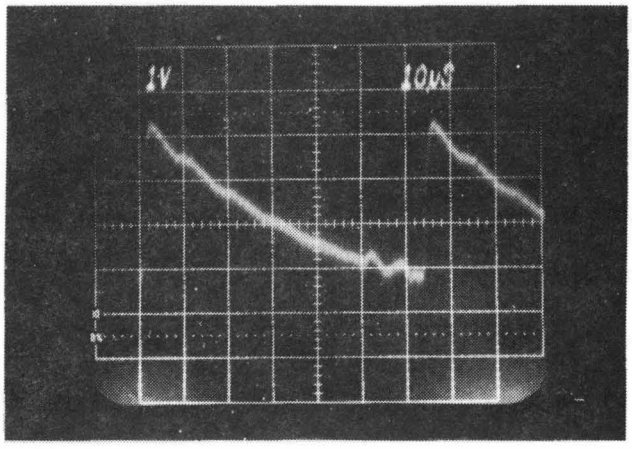
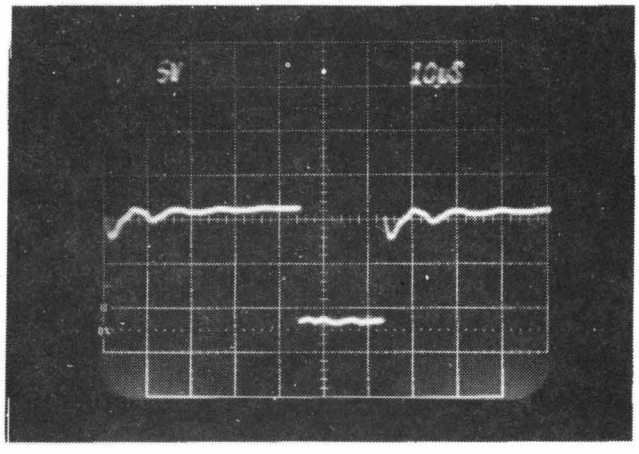


PHOTO NO.

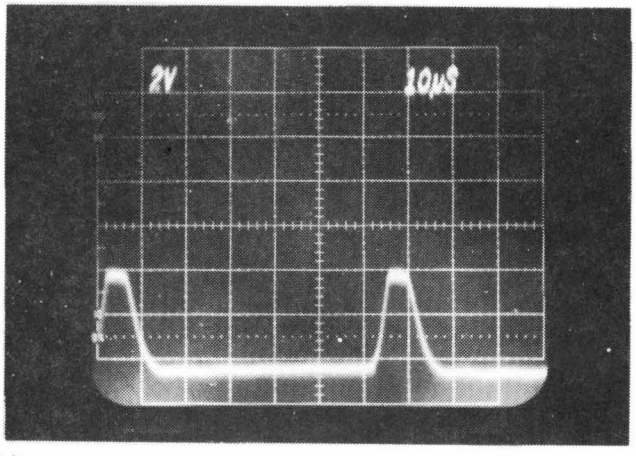
7

IC2 PIN 2



8

IC2 PIN 12



9

Q271 COLLECTOR

C1076/3

Figure 6-9. Typical CRT Driver Circuit Waveforms (Sheet 3 of 3)

The blocks in figure 6-10 have the following meanings:

a. Check voltage measurement or indication called out.

b. Defective parts

Short: Short mode defect

Open: Open mode defect

Fault: Fault in characteristic

c. Related to other troubles.

Consult the following list of symptoms and refer to the sheet of figure 6-10 indicated for detailed CRT driver troubleshooting information.

1. No Raster: Sheet 1 of 6
2. No Video: Sheet 2 of 6
3. No Sync: Sheet 2 of 6
4. No Horizontal Sync: Sheet 3 of 6
5. No Vertical Sync: Sheet 3 of 6
6. No Horizontal Sweep: Sheet 3 of 6
7. No Vertical Sweep: Sheet 4 of 6
8. No DC Restoration: Sheet 5 of 6
9. Size Control Trouble: Sheet 5 of 6
10. Picture Twist waving and Small Picture: Sheet 6 of 6
11. Interference: Sheet 6 of 6
12. Horizontal Foldover: Sheet 6 of 6

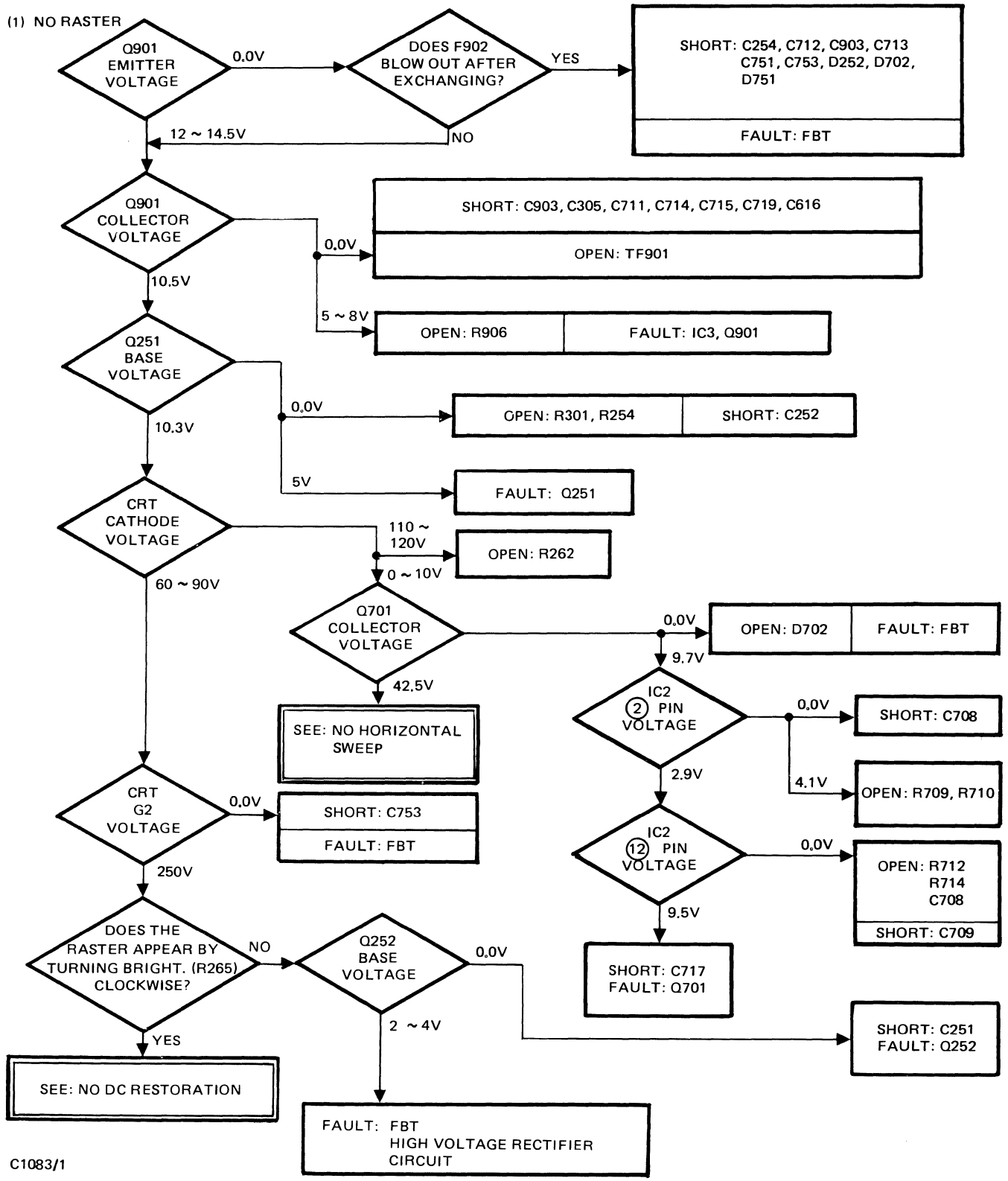


Figure 6-10. Troubleshooting Flow Chart (Sheet 1 of 6)

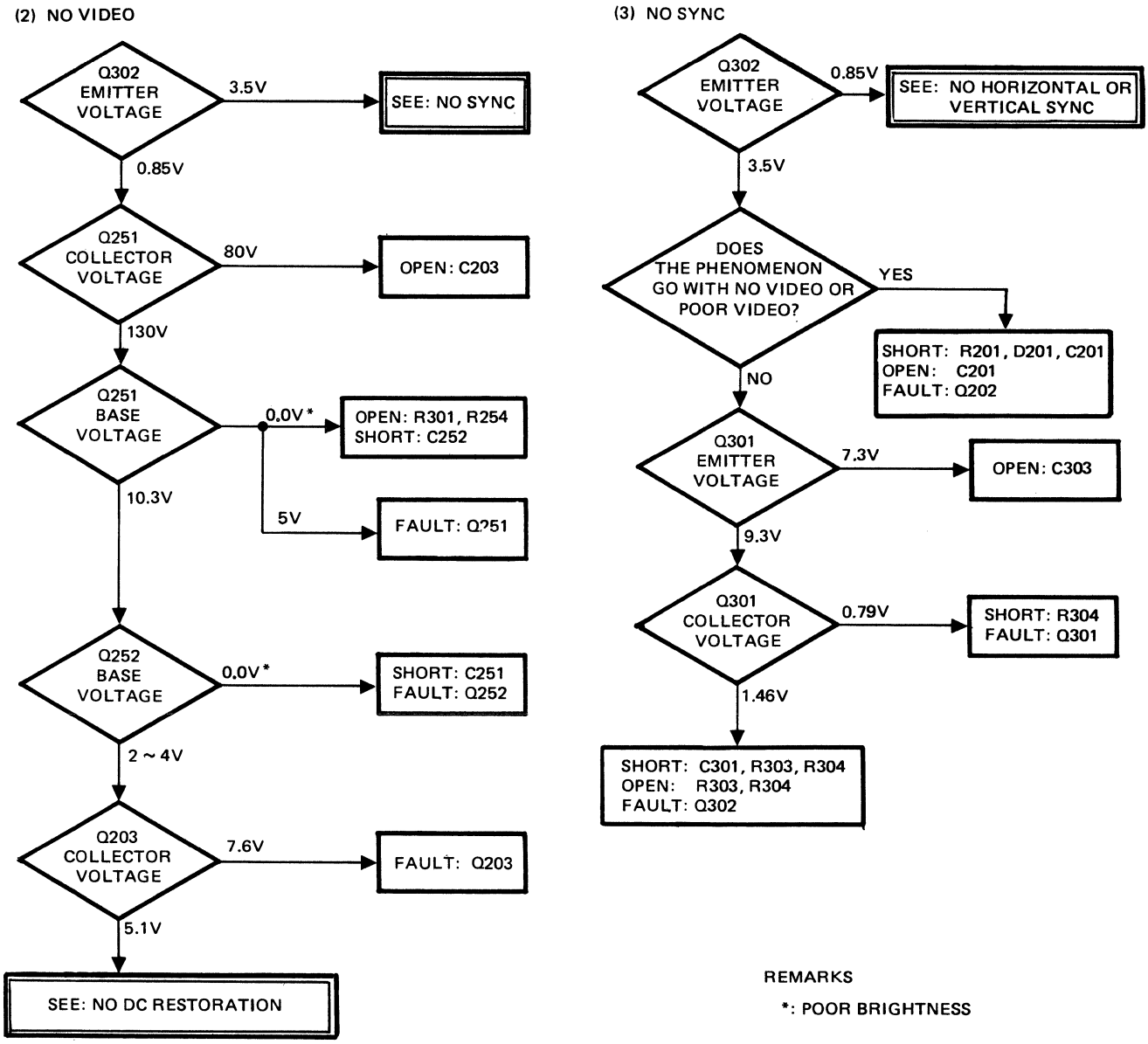
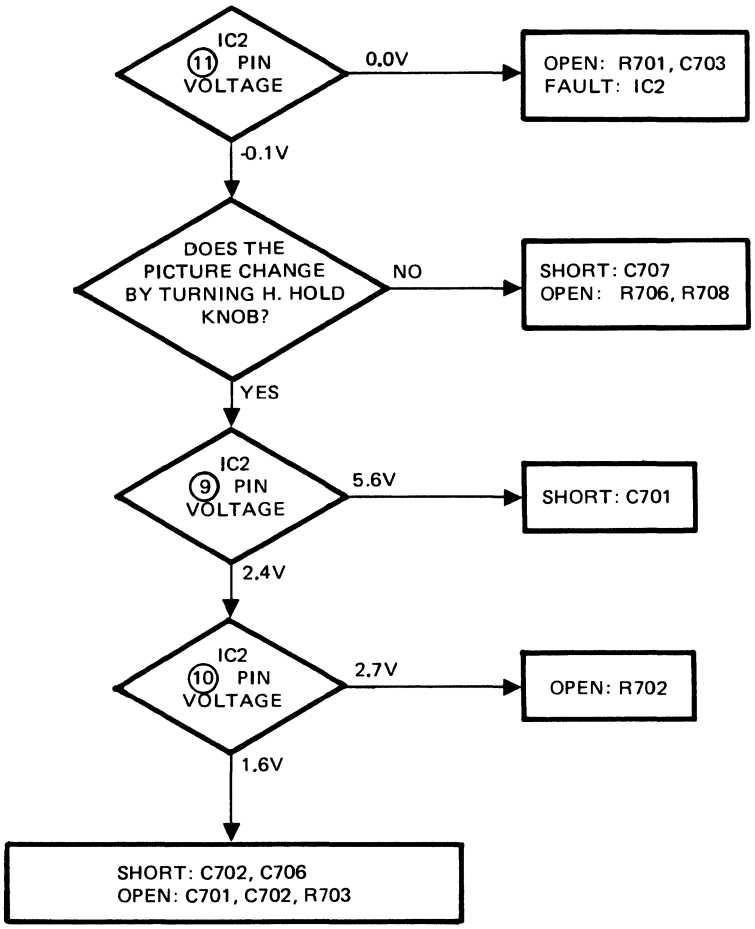
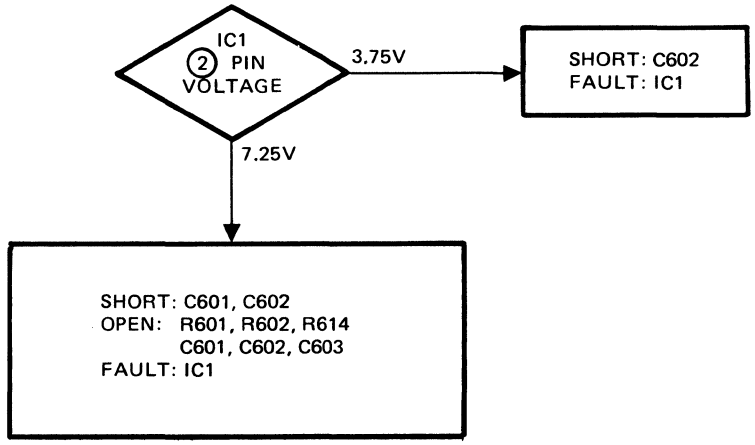


Figure 6-10. Troubleshooting Flow Chart (Sheet 2 of 6)

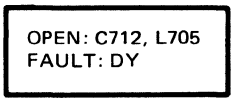
(4) NO HORIZONTAL SYNC



(5) NO VERTICAL SYNC



(6) NO HORIZONTAL SWEEP



C1083/3

Figure 6-10. Troubleshooting Flow Chart (Sheet 3 of 6)

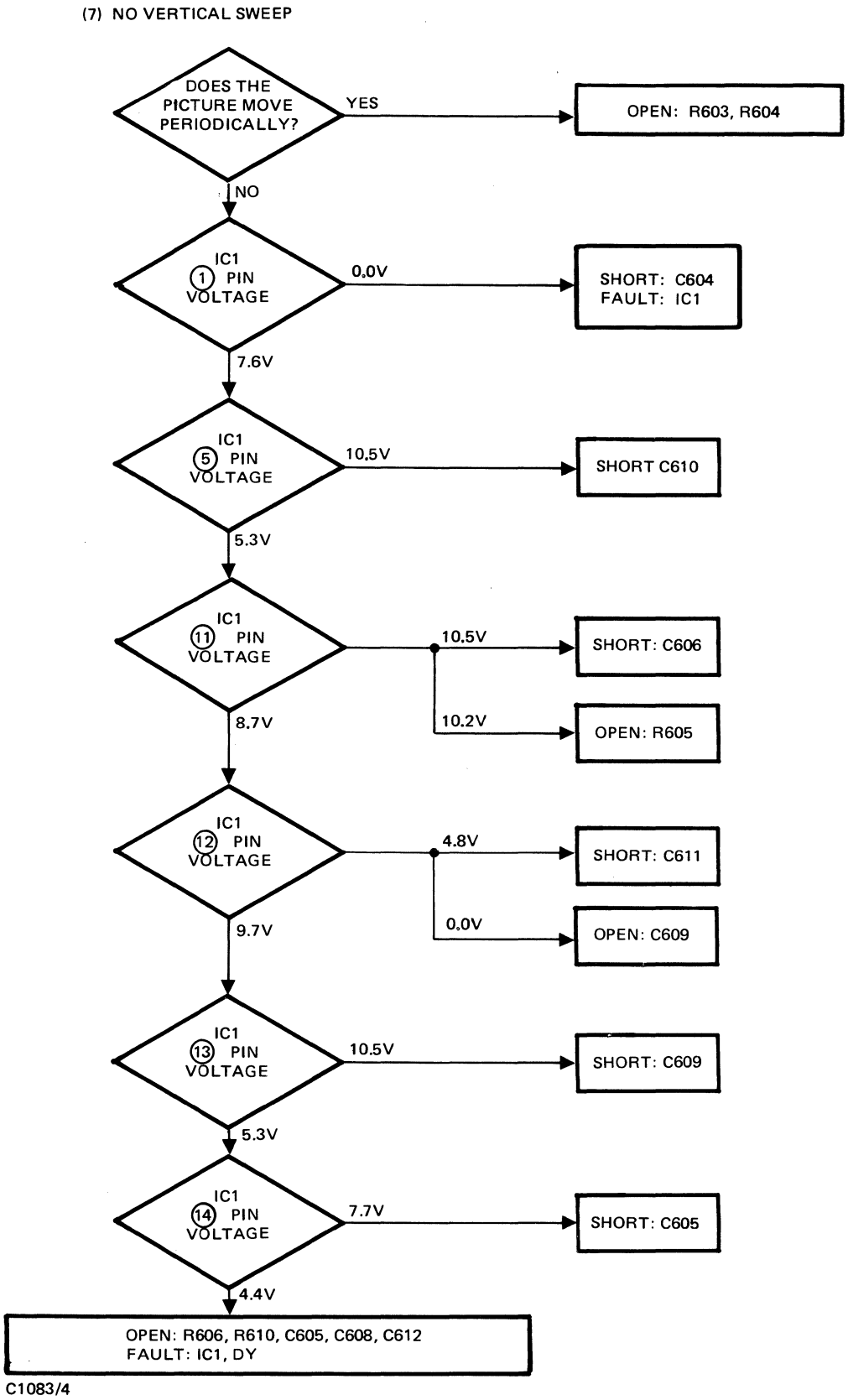


Figure 6-10. Troubleshooting Flow Chart (Sheet 4 of 6)

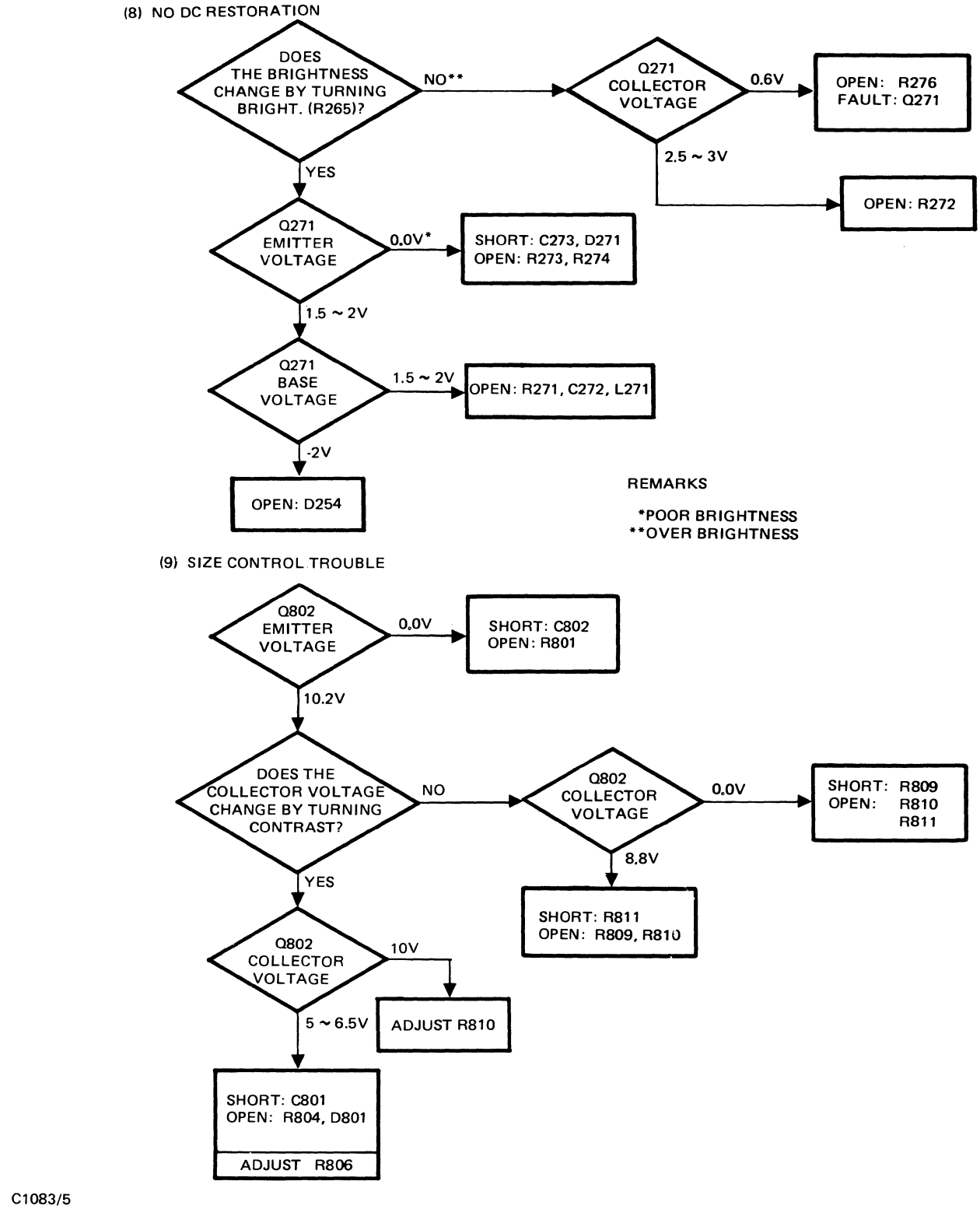
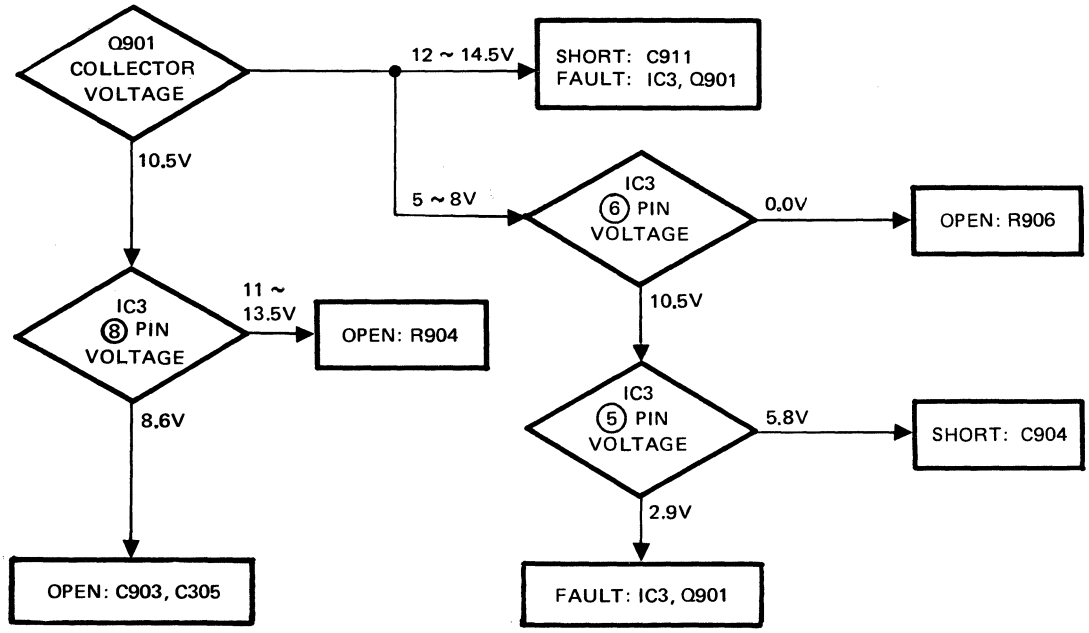


Figure 6-10. Troubleshooting Flow Chart (Sheet 5 of 6)

(10) PICTURE TWIST/WAVING AND SMALL PICTURE



(11) INTERFERENCE

OPEN: C905, C911, C801, C802

(12) HORIZONTAL FOLDOVER

ADJUST R707 OR R709

SHORT: R720
OPEN: R720
FAULT: C711, C715, D702, C713, IC2

C1083/6

Figure 6-10. Troubleshooting Flow Chart (Sheet 6 of 6)

ALIGNMENT INSTRUCTIONS

Alignment of the CRT driver is performed with all the boards of the terminal installed. Figure 6-11 shows adjustment locations and test connections for the CRT driver board.

Horizontal Deflection Circuit

1. Connect a dc voltmeter to TP901 and ensure that the voltage is 10.5 ±2 volts.

2. Set the contrast control (labeled BRIGHTNESS and located on the front of the terminal control unit) to a fully clockwise position.

HORIZONTAL OSCILLATOR ALIGNMENT

The variable resistor (R709) is sealed in the factory so that the resistor cannot be changed, thereby providing protection from X radiation. When the horizontal frequency changes, adjust the variable resistor (R709) accordingly. Adjustment will be needed when any of the following components have been replaced:

Resistor R709, R710

Capacitor C708

IC IC5

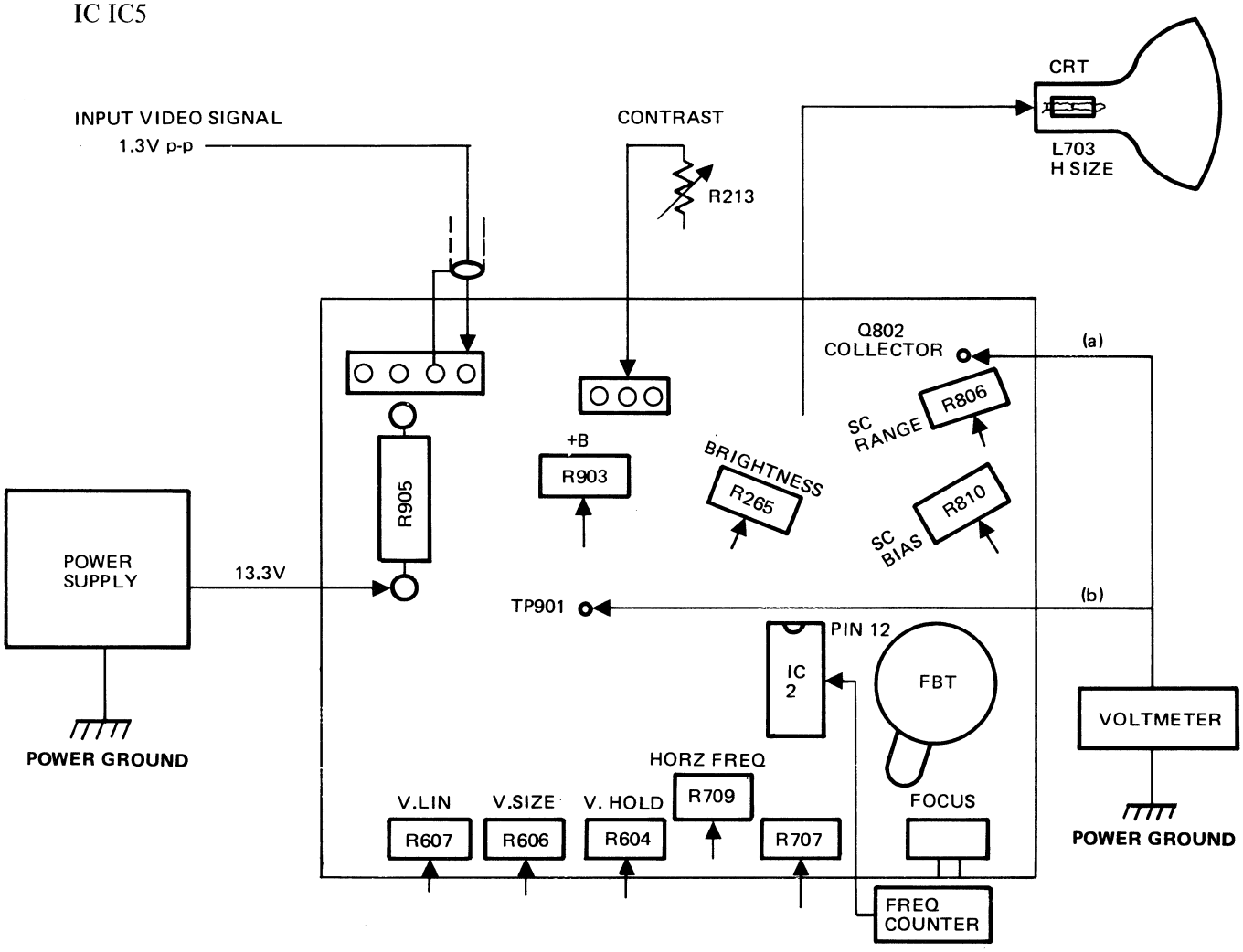


Figure 6-11. Connection and Adjustment Diagram

Refer to the circuit schematic diagram found in the Test and Field Reference documents.

1. Replace the variable resistor (R709) for the horizontal frequency adjustment, since it has been preadjusted and sealed in the factory.

2. Turn the horizontal frequency adjustment variable resistor fully clockwise.

3. Adjust R709 so that the oscillation frequency is 15.734 kHz, while observing a frequency counter or the picture drift.

4. Fix the horizontal frequency adjustment variable resistor (R709) as follows:

   a. Apply adhesive to the variable resistor as shown in figure 6-12.

   b. Put the canoe rivet into the rotator of the variable resistor as shown in figure 6-12.

   c. Apply adhesive over the canoe rivet to seal this resistor.

5. After the adhesive applied to R709 has cured, confirm that the oscillation frequency is coincident with the value in procedural c.

HORIZONTAL SIZE ALIGNMENT

Align the horizontal size coil (L703) on the deflection yoke so that horizontal size is the standard horizontal size of 210 mm.

Vertical Deflection Circuit

1. Set the contrast control clockwise.

2. Connect a d.c. voltmeter to TP901 and ensure that the voltage is 10.5 ±2 volts.

VERTICAL SIZE, VERTICAL LINEARITY ALIGNMENT

1. Fix V HOLD (R604) at the center of vertical hold range.

2. Align R606 and R607 so that the linearity at standard vertical size 158.5 mm is the best obtainable while observing the CRT display.

3. Fix VHOLD (R604) again at the center of vertical hold range.

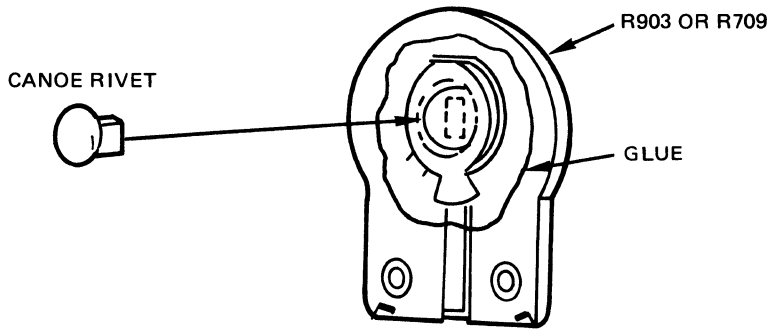


Figure 6-12. R903, R709 Diagram

Picture Position

Align the centering magnets (located on the CRT) so that the picture on CRT screen is in the center.

Brightness Control Circuit

R265 ALIGNMENT

1. Set the contrast control fully clockwise.
2. Adjust R265 so that the scan lines can be seen in the picture area with normal video.
3. Readjust R265 until the scan lines are no longer visible.

Voltage Control Circuit

1. Adjust R806 fully counterclockwise.
2. Adjust contrast control counterclockwise.
3. Connect voltmeter to TP901.

R903 ALIGNMENT

The variable resistor (R903) is sealed in the factory so that the resistor cannot be changed, thereby providing protection from X radiation. When the output voltage changes, adjust the variable resistor (R903) accordingly. Adjustment is needed when the following components have been replaced:

Resistor R903

Transistor Q901

IC IC3

Refer to the circuit schematic diagram found in the Test and Field Reference documents.

1. Replace the variable resistor for the +B adjustment, since it has been preadjusted and sealed in the factory.
2. Turn the +B adjustment variable resistor fully counterclockwise.
3. Connect the voltmeter (precision ±2%) to TP901 to set up the +B voltage.
4. Adjust R903 to obtain 10.7V ±0.2V.
5. Fix the +B adjustment variable resistor (R903) as follows.
   a. Apply adhesive to the variable resistor as shown in figure 6-12.
   b. Put the canoe rivet into the rotator of the variable resistor as shown in figure 6-12.
   c. Apply adhesive over the canoe rivet to seal this resistor.
6. After the adhesive applied to R903 has cured, confirm that the +B voltage is coincident with the value in procedural step 4.

Size Control Circuit

For size control circuit adjustment, adjust R810 and R806.

R810 ALIGNMENT

1. Set contrast control clockwise.
2. Set R806 counterclockwise.
3. Connect voltmeter to the collector of Q802.
4. Align R810 so that Q802's collector voltage is 6.5 ±0.5V.

R806 ALIGNMENT

1. Connect voltmeter to TP901.
2. Align R806 so that +B voltage (TP901) is 10.5 ±0.2V.

OPERATION CONFIRMATION

1. Fix R213 at the end of counterclockwise.
2. Confirm that +B voltage (TP901) is 10.7 ±0.2V.
3. If it is not, align R810 and R806 again.

High Voltage Check

Check the High Voltage (H.V.) as follows, when replacing the components or aligning the Voltage Control Circuit and Horizontal Deflection Circuit.

1. Connect H.V. meter as shown in figure 6-13.
2. Set the input voltage of display unit to 13.3V d.c.
3. Check for normal operation, and that the indication of the H.V. meter is less than 14.5kV at zero beam current (contrast control is minimum).
4. Remove H.V. meter.
5. Turn the power switch on and confirm that the display unit operates normally.

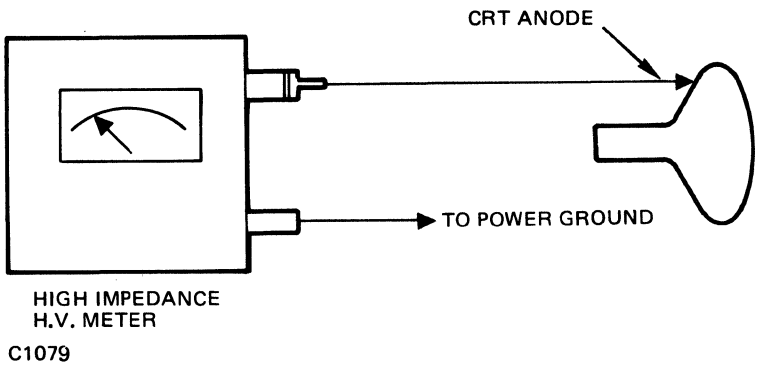


Figure 6-13. High Voltage Measurement

CRT DRIVER REPLACEMENT

Refer to figures 6-14 and 6-15 in the following procedures for removal and installation of the CRT driver module. Ensure that the TD850 is disconnected from a.c. power before proceeding.

Removal

1. Using a screwdriver with an insulated handle, short the anode of the CRT to chassis ground. Do this by inserting the tip of the screwdriver under the rubber cap on the anode lead until it contacts the anode clip; and lay the shank of the screwdriver against the chassis.

2. Remove the three screws labeled 1 in figure 6-14.

3. Tilt the module up and remove the four plugs on the CRT board (labeled 1 in figure 6-15). Remove the plug on the back of the CRT (labeled 2 in figure 6-15). Remove the cable tie item (labeled 3 in figure 6-15).

4. Remove the anode cap by inserting long nose pliers under the cap and squeezing the clip.

5. Release the plastic clip in the center of the board by squeezing it with long nose pliers at the location (labeled 2 in figure 6-14). Release the four plastic clips on the circuit board side of the mounting bracket (labeled 4 in figure 6-15). Remove the CRT driver board.

Installation

1. Place circuit board in position and press the center plastic clip through the hole in the mounting bracket. Press the edges of the circuit board in place under the four clips (labeled 4 in figure 6-15).

2. Install the anode cap on the CRT and the plug on the back of the CRT. Install the four plugs on the circuit board. Ensure that the plug with the green and yellow wire is installed with the yellow wire to the outside edge of the circuit board.

3. Replace the cable tie. Take care to ensure correct lead dress.

4. Place the mounting bracket back down and install the three screws. Make sure that the screw on top has all the insulators in place. There are two insulators: one washer-shaped insulator goes underneath the mounting bracket, and one doughtnut-shaped insulator under the screw.

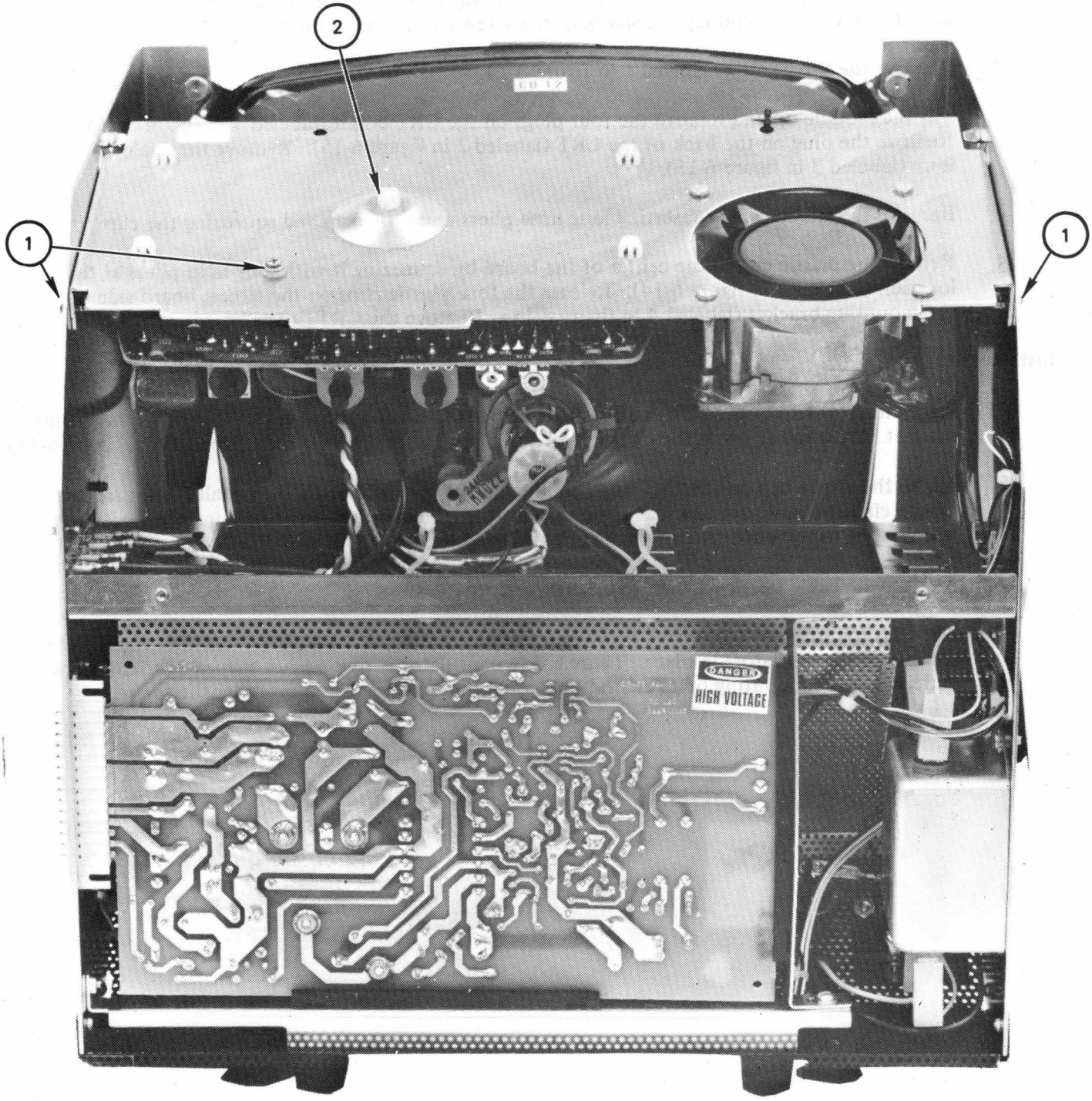


Figure 6-14. CRT Board Replacement Top View

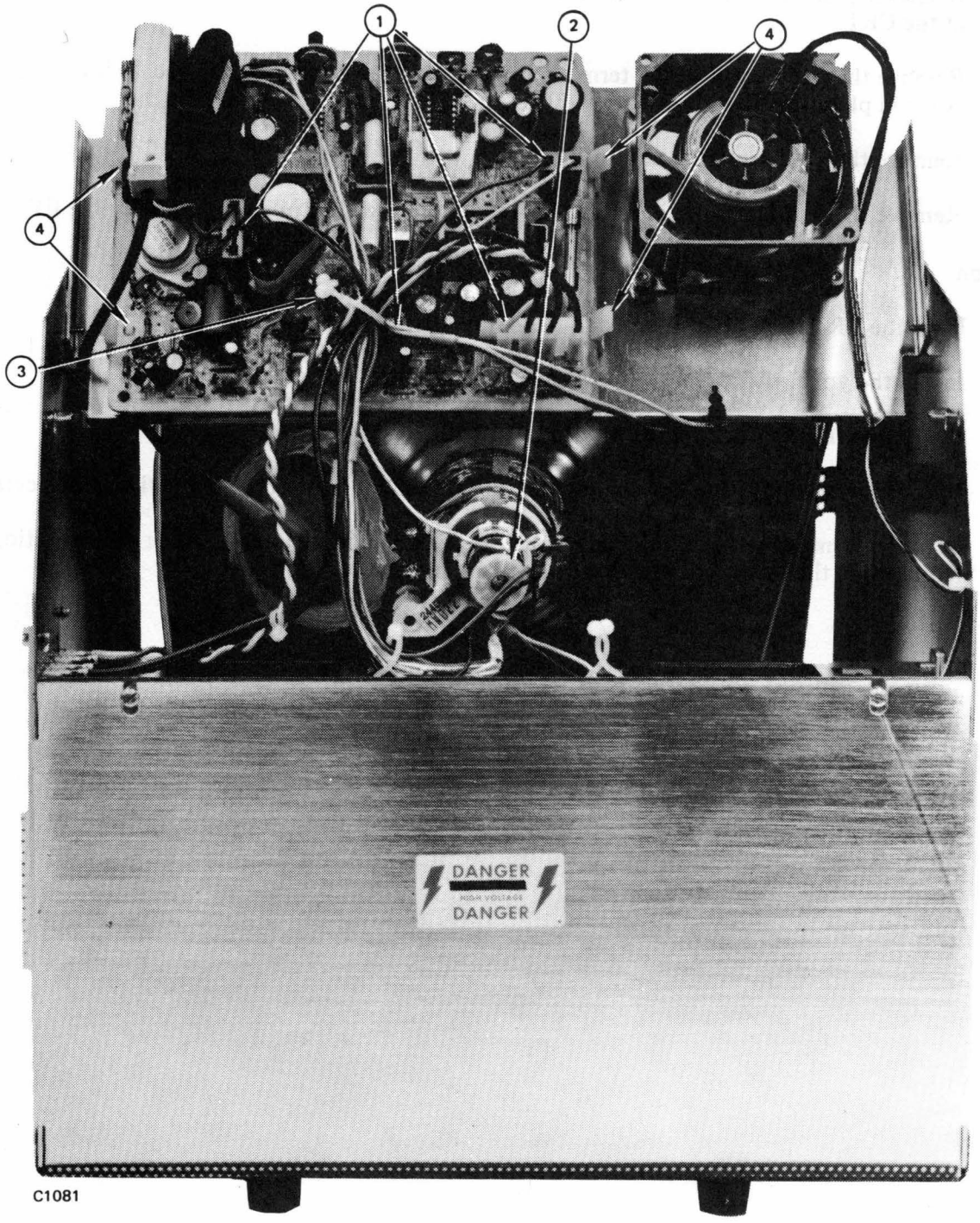


Figure 6-15. CRT Board Replacement Bottom View

CRT REPLACEMENT

See figure 6-16 for removal and replacement of the CRT. Refer to the preceeding safety precautions before continuing.

Removal

1. Discharge the anode of the CRT. Use a screwdriver with an insulated handle to short the anode to chassis ground. Disconnect the anode lead from the CRT. Disconnect the socket on stem at the CRT.

2. Remove the front cover of the terminal by removing the 4 screws (2 on each side) that hold the cover in place (see item 1 in figure 6-16).

3. Remove the yoke from the neck of the CRT.

4. Remove the 4 nuts (item 2 in figure 6-16) that hold the CRT in place. Remove the CRT.

Installation

1. Place the CRT in position and install the 4 nuts that hold it in place.

2. Install the yoke.

3. Fasten the front cover in place with the 4 screws.

4. Reconnect the anode cap and the socket. Ensure that all the wires are positioned correctly.

5. Turn the terminal on and determine if picture alignment is required. Adjust yoke position as required, so that the picture is aligned square to the front of the unit.

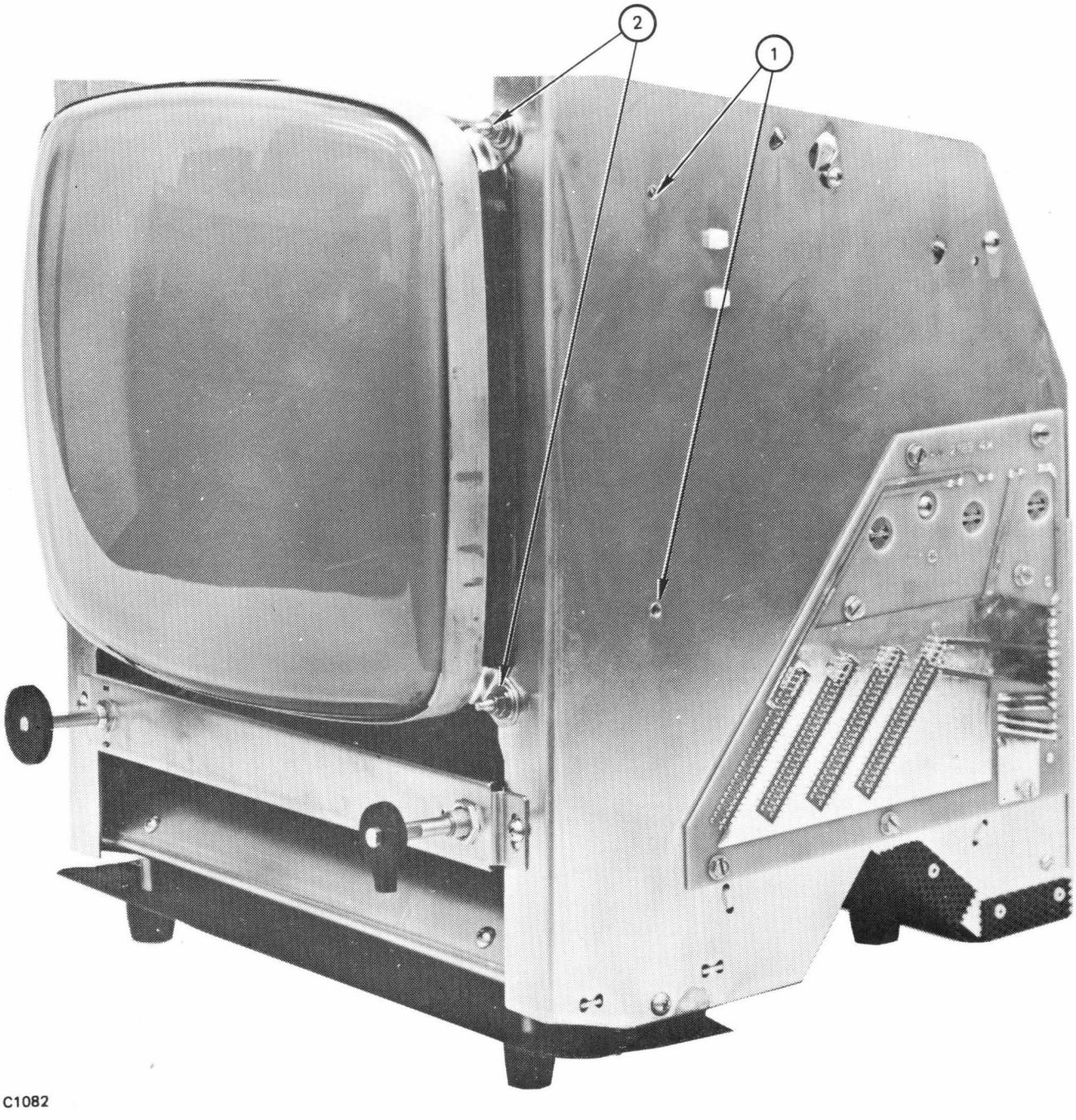


Figure 6-16. CRT Replacement

APPENDIX A
GLOSSARY OF SIGNALS FOR THE VIDEO BOARD

AB0 through AB7	Backplane address bus (8 bits).
ADDEN'	Address bus enable (negative logic).
BBITCLOCK'	Buffered 12 MHz clock
BITCLOCK	12 MHz clock; picture element timing.
BLANK	High during horizontal and vertical retrace. Causes video signal to be at a black level during retrace time.
BLANKOUT	Prevents loading of parallel to serial converters.
BLINK	Causes blinking of characters.
BRIGHT	Makes characters bright.
BTPB'	Signal from microprocessor on P/S board for synchronization.
BTPB	Inverted BTPB.
BUS0 through BUS7	Microprocessor data bus on video board (8 bits).
BVPIX	High during picture display time; low during vertical retrace.
CC0 through CC6	Character code (7 bits).
CHANREQ'	Request for DMA for string transfer or number of scan line pairs.
CHBLNKRATE	Character blink rate.
CHPIX-16	16 BITCLOCK times earlier than HPIX.
CLOCK/2'	12 MHz clock divided by 2 (6 MHz).
CLOCK/4	12 MHz clock divided by 4 (3 MHz).
CLOCKEN	If WIDE = 1, then CLOCKEN = H3, and controls loading of status registers and parallel to serial converters.
COUNTLINE	At end of each scan line, vertical counters advance.
CURSBLINK	Cursor blink rate.
CURSCARRY	If high, the character shifted into the line buffer has cursor to be displayed at this character position. CURSCARRY is developed from the cursor counter.
CURSOR	If high, the character shifted out of the line buffer has cursor.
CVIDEO 1 through CVIDEO2	Composite video signal containing picture and synchronization information.

DACBLNK	Input to Digital-to-Analog converter resistors.
DACSNC	Input to Digital-to-Analog converter resistors.
DAC01 through DAC15	Input to Digital-to-Analog converter resistors.
DATAEN	Data bus enable. Allows data from the microprocessor to be gated onto the backplane bus.
DATAEN'	Inverted data bus enable. Combines with MRD' and MWR' to form READ' and WRITP' respectively.
DATA0 through DATA7	Latched on board data bus (8 bits).
DATA7'	Active low data bit 7.
DBRIGHT	Latched BRIGHT.
DB0 through DB7	Backplane data bus (8 bits).
DCHANACK	DMA acknowledge delayed for one major cycle time.
DEC5	+5 volts; filtered for the output circuitry.
DP, DQ, DR, DS	Next state information for synchronization state machine.
DSECURE	Latched SECURE.
EADDEN	After being latched becomes ADDEN'.
EDATAEN	After being latched becomes DATAEN' and DATAEN.
EGO	After being latched becomes WAIT'.
END'	End of character line signal, as opposed to COUNTLINE.
FIELD	Determines which half of 2:1 interface will be displayed.
FIELD'	Inverted FIELD.
FORMS	High if machine is in forms mode.
GRAY0 through GRAY3	Gray scale bits. Four bits to represent 16 levels of gray.
HBLANK'	Low during horizontal retrace, and is wider than HPIX.
HCARRY'	Decoded output of the horizontal counter used to clear the horizontal counter.
HPIX-16	Sixteen BITCLOCK times earlier than horizontal scan line display time.
HPIX-16'	Sixteen BITCLOCK times earlier than horizontal scan line display time.
HPIX-4	Four BITCLOCK times earlier than horizontal scan line display time.
HPIX-6	Six BITCLOCK times earlier than horizontal scan line display time.
HPIX-8	Eight BITCLOCK times earlier than horizontal scan line display time.

H0 through H9	Output from horizontal countdown counters.
INVISIBLE	The latched combination of BLINK and BLINKRATE which inhibits the display during blink time.
LASTLINE	High during last character line.
LASTLINE'	Inverted LASTLINE.
LBD00 through LBD07	Output of DOWN line buffer (8 bits).
LBU00 through LBU07	Output of UP line buffer (8 bits).
LDNOSCANL'	Load number of scan line pairs into the scan line counter and decoder.
LOADPTS	Load parallel to serial converter for every character.
LOADPTS'	Inverted LOADPTS.
LOADSTATUS	Load status register for characters and left edge of screen.
LSTSCNLINE	Last scan line of a character line.
MA0 through MA7	Microprocessor address bus on the video board (8 bits).
MCLOCK	3 MHz clock going to edge connector only. Master clock used for timing on other logic boards.
MRD'	Memory read line (negative logic).
MWR'	Memory write line (negative logic).
NEGVIDEO	Changes video sense to black characters white background.
NOTLASTSW	Ensures that first line on the screen comes from the UP line buffer.
N0 and N1	Microprocessor output code (uses 2 bits only).
OSCILLATOR'	Output of 12.272726 MHz oscillator.
OUTCLOCK'	Clock to shift characters out of the parallel to serial generators.
OUT1'	Output code used to set up the cursor position. Loads the cursor counter.
OUT2'	Output code used to set up the length of a string. Loads the utility counter.
P	State variable for synchronization state machine.
PTS0 through PTS2'	Output of parallel to serial converter (3 bits).
P00' through P07'	Inputs to parallel to serial register for bit 0 (8 bits).
P10 through P17'	Inputs to parallel to serial register for bit 1 (8 bits).
P20' through P27'	Inputs to parallel to serial register for bit 2 (8 bits).

Q	State variable for synchronization state machine.
QDP	Q bit from video microprocessor is used to clear vertical counters.
QMP	Q bit from processor on P/S board connected to EFA of the display microprocessor.
R	State variable for synchronization state machine.
READ'	Backplane read bus (tristate and negative logic).
RESET	Power-up reset signal generated on P/S board.
RESET'	Power-up reset signal generated on P/S board.
REVERSE	Changes video sense.
S	State variable for synchronization state machine.
SC1	State code from microprocessor. High during DMA cycle.
SECURE	Replaces character display with solid block of reversed video.
SELLBO	Select line buffer output, UP or DOWN.
SHIFTCLOCK	Clock to shift data into the line buffer.
SHIFDN	SHIFTCLOCK for the DOWN line buffer (input or output rate).
SHIFTIN	Gated clock to shift data into the line buffer.
SHIFTOUT	Clock to shift data out of the line buffer for display.
SHIFTUP	SHIFTCLOCK for the UP line buffer (input or output rate).
SHPIX-16'	HPIX-16 synchronized with microprocessor clock.
SWITCHUP/DN	Interchanges line buffers from input to output, and vice versa.
S0' through S7'	Minor cycle times for display microprocessor.
TIP'	Sync tip, video synchronization signal.
TTLHIGH	Logical High level.
T7*'	Generated by sync. State machine if processors are in phase.
UCAR'	Utility counter carry. Channel request if no carry.
UC1 through UC7	Outputs of the utility counters.
UNDER	High if in underline area and underline to be displayed.
UNDERAREA	Determines underline area in CHARACTERSPACE.
UNDERLINE	Determines if characters will be underlined.

UP	If UP = 1, the upper line buffer is written into.
UP'	If UP' = 1, the lower line buffer is written into.
VALIDU	Goes high after first OUTPUT2 instruction occurs and stays high until power is removed. Indicates the count in the utility counter is valid.
VALIDU'	Goes high after reset occurs, and stays high until the first OUTPUT2 occurs. Indicates the count in the utility counter is not valid.
VCLOCK	Clock generated at twice the scan line rate.
VERTSYNC'	Vertical synchronization pulse.
VIDSENSE	Determines if black characters are to be displayed on white background.
VPIX	Vertical synchronization pulse.
V0 through V3	Outputs of vertical counter used as scan line numbers.
WAIT'	Goes low if the microprocessors are out of sync. The WAIT/ signal stops the display processor.
WIDE	Used to generate shift timing for wide characters.
WIDEIN	Used to generate two SHIFTIN signals for each character to be loaded in the line buffer.
WRITEP'	Backplane write bus (tristate, negative logic).

APPENDIX B
GLOSSARY OF SIGNALS FOR THE PROCESSOR AND STORAGE BOARD

AB0 through AB7	Tri state address bus shared by Processor/Storage Board and Video Board.
ADRA00 through ADRA11	Buffered low-order address bits to the RAM and ROM on the Processor/ Storage Board.
ADR00 through ADR15	16-bit address register prior to buffering and decoding.
BAB00 through BAB07	Buffered version of AB0 through AB7.
BTPB'	Complement of TPB on the PSMP. This is the timing reference signal used to generate T0 through T7.
BUS0 through BUS7	Microprocessor tristate data bus.
CHANACK	Channel Acknowledge. This occurs during T4 through T7 when the PSMP enters a DMA state.
CHANIN'	This line causes the PSMP to enter a DMAIN state.
CHANOUT'	Similar to CHANIN', except a DMAOUT state occurs.
CLOCK'	Complement of MCLOCK. Synchronous logic clock source.
CS00' through CS60'	Chip selects for the read-only storage chips. The last two hex digits indicate the starting address. CS30' and ADRA11 select the chip at 3800 hex.
CSCO' through CSFC'	Chip selects for the read/write storage chips. Each signal selects two chips for 1K bytes.
C1, C2, C3	Mode control for the ER 1400 EAROM. Logic levels of 0 and +12V.
DATA	Data line to and from the ER1400. There is a high impedance source in either case. Logic levels of 0 and +12V (refer to Z123H).
DATACOMINT'	Input signal to EF4' on PSMP. Indicates the interrupt is from the data communications and not the Serial I/O interface.
DB0 through DB7	Tristate data bus. PSMP bus driver source. Read-only store, bus driver source. Read/write store, bus driver source.
EF3'	Unused flag input to PSMP.
ENBINP'	Enables the data bus DB0 through DB7 onto the P/S BUS0 through BUS7.

INP7'	Decoded PSMP input instruction to enable data from ER1400 to DB0. DB1 through DB7 will float.
INTERRUPT'	This is the interrupt line to the PSMP.
KLOCK	12 Volt firmware-derived clock for the ER1400.
LSTTLHI	1-kilohm pullup to +5V.
MA0 through MA7	PSMP memory address lines.
MCLOCK	Clock used to drive synchronous logic on the P/S board. The falling edge is used for edge triggered logic.
MRD	Complement of the PSMP MRD' signal. When high it indicates a read of memory is in process.
MWR'	Write pulse issued by the PSMP on a Write to Store.
N0, N1, N2	Output levels from the PSMP during an I/O instruction to select a device.
OUT7'	Decoded PSMP output instruction to load the EAROM Input register from DB0 through DB4.
PADR08 through PADR15	High address register loaded at the end of T2 or T6. These address bits are delayed by one clock period, at which time they become ADR08 through ADR15.
PCLOCK'	Identical to CLOCK' but this signal only drives the PSMP.
QMP	Q bit from the PSMP.
R/ODOE'	This signal enables the read-only store data bits to DB0 through DB7 (through a CMOS tristate buffer).
R/OD00 through R/OD07	Read-only store data bits. These are tristate with a pullup on each line, and are buffered by a CMOS tristate buffer before appearing on DB0 through DB7.
R/WCE	RAM chip enable. This line is used as a clock to the RAM. CS' and the 10 address lines are clocked into the chip with the rising edge of R/WCE.
R/WDOE'	This signal enables the read/write storage data bits to DB0 through DB7 through a CMOS tristate buffer.
R/WD00 through R/WD07	Read/write store data bits. These are tristate bidirectional lines. Data appears from DB0 through DB7 (after buffering) when writing, and data is read from two chips when reading.
READ'	This is the direction control for the data bus. The PSMP has control during T4 through T7 and the video board has control during T0 through T3.

RESET'	This is the master reset which remains low for approximately one-half second on power up or when the +5V drops to approximately +4.6V for more than 50 milliseconds.
SC0, SC1	State code designators of the PSMP.
SHIFTCYCLE'	This is an input to the PSMP EF2'. This signal indicates when a shift cycle is in progress on the serial I/O bus.
TPB	Timing pulse TPB of the PSMP. An inverted version of TPB appears as BTPB'.
T0' through T7'	Timing signals derived from BTPB' and CLOCK'. T7 occurs synchronously with the same clock edge that generates TPB, without the delays encountered with the PSMP.
T1 through T4'	This signal occurs when the PSMP has to put its address onto the blackplane address bus.
T4 through T7	This signal occurs when the PSMP has control of the data bus. It is also used to control READ', WRITE P' and CHANACK signals.
WRITEP'	Write Pulse. This is sourced from the video board during T0 through T3 or from the P/S board during T4 through T7.
Z102A	During power-up, this line charges C100 through R103, causing the power-up delay. If a low voltage condition on the +5V occurs, the open collector output of UI11 (LM 311) quickly discharges C100, causing RESET'.
Z104A	This signal controls when the PSMP is to put data onto the data bus DB0 through DB7.
Z123H	This is a 5-volt CMOS version of data. Chip UH07 on the Processor and Storage Board is being used as a level translator. Note the inversion of data being presented to DB0.

APPENDIX C
GLOSSARY OF SIGNALS FOR THE SERIAL INPUT/OUTPUT BOARD

ASYNCCLK	Asynchronous Clock for UART.
BA	RS232 circuit BA which is transmitted data from the MTS-L.
BB	RS232 circuit BB which is received data by the MTS-L.
BDIBB	Half of BDI balanced transmission line.
BDIRCVDAT	Received data from BDI transmission line.
BDITDI	Indicates the terminal is configured for a BDI or TDI data communication connection.
BDIXMTDAT	Half of BDI balanced transmission line.
BLOCK'	When low, blocks the propagation UPSTREAM of any REQUESTTOSEND from DOWNSTREAM. Also blocks the propagation DOWNSTREAM of a CLEARTOSEND from UPSTREAM.
BTPB	Buffered TPB signal from the PSMP.
BTPB'	Complement of BTPB.
BUFDSBA	RS232 circuit BA (transmitted data) from Downstream.
CA	RS232 circuit CA which is Request to Send level from the MTS-L.
CB	RS232 circuit CB which is Clear to Send level from the data set.
CC	RS232 circuit CC which is Data Set Ready level from the data set.
CCITT116	CCITT circuit 116 which is Select Standby from the MTS-1.
CD	RS232 circuit CD which is Data Terminal Ready level from MTS-1.
CF	RS232 circuit CF which is Received Line Signal Detected level from the data set.
CH	RS232 circuit CH which is Data Signal Rate Selector level from the MTS-1.
CHANACK	Acknowledgement from the PSMP to a DMAIN or DMAOUT request.
CHANACK'	Complement of CHANACK.
CHANIN'	When low, requests a DMAIN operation of the PSMP.

CHANOUT'	When low, requests a DMAOUT operation of the PSMP.
CLOCK	This is the clock that the SIO board uses for all its synchronous logic, including its microprocessor.
CLOCK'	Complement of CLOCK.
CLRINT	Clears the flip-flop that generates EXTEF4'. This signal is developed when the PSMP executes an INPUT 6 instruction.
CLRTOSEND	CLEARTOSEND. A result of either RS232 circuit CB or BDITDT REQTOSEND. The latter case is a synthesis of CB when using a TDI or BDI connection.
CS	A pulse that loads a status word into the UART.
CS'	A negative-going pulse that loads a status word into the USRT.
DATACLK'	A negative-going clock that is used to clock the data portion of the 12-bit shift register in the serial I/O generation logic.
DATAERROR'	A low indicates that an error is associated with the character just received by the UART or USRT. The state of this signal is valid only when the SWE' signal is low (for example only when the status of the UART or USRT is enabled on the URTBUS lines).
DATSETRDY'	Complement of RS232 circuit CC, buffered to TTL level.
DB	RS232 circuit DB, which is Transmit clock from the synchronous data set.
DB0 through DB7	8-bit tristate data lines used to pass data to and from the PSMP (DB7 = MSB). (DB7 is the most significant bit.)
DD	RS232 circuit DD, which is Receive clock from the synchronous data set.
DMABUSY'	When low, indicates that a DMAIN or DMAOUT operation, initiated by SIO board, has been requested, but not yet acknowledged (by a CHANACK).
DMAIN	Used in conjunction with DMAIN operations of PSMP. If set, an OUTPUT 1 instruction of the SIO microprocessor will cause CHANIN' to be developed.
DMAIN'	Complement of DMAIN.
DMAOUT	Same function of DMAIN, except with respect to DMAOUT of PSMP.
DMAOUT'	Complement of DMAOUT.
DTIME	Indicates that the bits being shifted out to the serial I/O bus are data bits, as opposed to Sync and I-code bits.
DWNSTMBA	RS232 circuit BA from downstream concatenation connection (Transmitted data).

DWNSTMBB	RS232 circuit BB to downstream concatenation connection (Received data).
DWNSTMCA	RS232 circuit CA from downstream concatenation connection (Request to Send).
DWNSTMCB	RS232 circuit CB to downstream concatenation connection (Clear to Send).
DWNSTMCC	RS232 circuit CC to downstream concatenation connection (Data Set Ready).
DWNSTMCD	RS232 circuit CD from downstream (not implemented on connector) (Data Terminal Ready).
DWNSTMCF	RS232 circuit CF to downstream concatenation connector (Receive line Signal Detected).
DWNSTMDB	RS232 circuit DB to downstream concatenation connector (Synchronous Transmit Clock).
DWNSTMDD	RS232 circuit DD to downstream concatenation connector (Synchronous Receive Clock).
DWNSTMRTS	RS232 circuit CA from downstream, buffered to TTL level (Request to Send).
EF4	If asynchrohous version of SIO board, this signal indicates the UART transmit buffer is empty. If synchronous version, it indicates that a fill character has been transmitted by the USRT.
EF4'	Complement of EF4, connected to flag EF4' input of the micro-processor.
ENABLEINT	Indicates that, during an invitation to interrupt cycle of the serial I/O generator logic, a device has indicated it wants to interrupt (by the existence of a ONE bit during DTIME). When SCYCLECOMP goes true, ENABLEINT will cause INT to be set, and invitation to interrupt has not been turned off.
ENABLEINT'	Complement of ENABLEINT.
EXTDATRDY'	When low, indicates that data has been loaded into the SIO input register from the PSMP, via an OUTPUT 6 instruction.
EXTEF4'	This signal is connected to the PSMP flag EF4'.
EXTN0, EXTN1, EXTN2	These three signals are the N lines from the PSMP.
EXTREADENA'	A low indicates that the PSMP is presently in time slots T4 through T7, and its MRD' line is low. This signal is used in conjunction with the PSMP N lines (EXTNO - N2) to determine when an output instruction is being executed.

EXWRTENA'	A low indicates that the PSMP is presently in time slots T4 through T7, and its MRD' line is high. This signal is used in conjunction with the PSMP N lines (EXTNO - N2) to determine when an input instruction is being executed.
EXT4 through EXT7	Indicates when the PSMP is in time periods T4 through T7.
EXT4' through EXT7'	Complement of EXT4 through EXT7.
GOODDATA'	A low indicates that a character has been received by the UART or USRT, and no error is associated with it. The state of this signal is valid only when the SWE' signal is low (for example, only when the status of the UART or USRT is enabled on the URTBUS lines).
ICODECLK'	A negative-going clock that is used to clock the I-code portion of the 12-bit shift register in the serial I/O generation logic.
INT	Indicates that a device responded to the invitation to interrupt with its device code. (This signal then generates interrupt if TURNOFFITI is not true.)
INT'	Complement of INT.
INTERRUPT	Indicates that a device on the serial I/O bus has responded to invitation to interrupt and that a Turn Off Invitation to Interrupt instruction is not being executed by the PSMP.
INTERRUPT'	This signal is connected to the PSMP INTERRUPT' input. Note that the signal is not necessarily the complement of interrupt.
INVTOINT	Indicates that the serial I/O generation logic is currently cycling an invitation to interrupt ICODE, soliciting interrupt requests from devices.
LOADDATA'	A low enables the data portion of the Serial I/O Generation Logic Shift register to be loaded with data from the PSMP.
LOADICODE'	A low enables the ICODE portion of the Serial I/O Generation Logic Shift register to be loaded with data from the PSMP.
MA0 through MA7	Address lines from the SIO microprocessor.
MA8 through MA11	These lines are the bits that were on MA0 - MA3 when TPA occurred. They represent the 4 high order bits of the 12-bit addresses used by the SIO microprocessor. (Note that the microprocessor actually uses 16-bit addresses, but the SIO board only uses 12 of these.)
MEMENABLE	The memory enable signal for the RAMs. It is true for T4 through T7 of the SIO microprocessor.
MONMODE	Monitor mode: This signal is true when the terminal is in Monitor mode.
MRD	Complement of MRD'.
MRD'	This is the Memory Read signal of the SIO microprocessor.
MWR'	This is the Memory Write signal of the SIO microprocessor.

NEG12V	-12V from power supply.
NEQ1' through NEQ7'	These signals, when low, indicate when the N lines of the SIO microprocessor have an octal value of 1 through 7, respectively.
N0, N1, N2	The N lines of the SIO microprocessor.
ONEOCCURD'	Indicates that a "one" has occurred during the DTIME of an Invitation to Interrupt cycle of the Serial I/O Generation logic.
POKEBUZZ'	A low-going pulse that triggers the buzzer one-shot.
POKECYCLE	This signal defines a period of time, following a SIO microprocess OUTPUT 4 instruction, during which the contents of the Data Communication Write Buffer are enabled on the URTDAT lines and the UART or USRT is strobed to load the data.
POKECYCLE'	Complement of POKECYCLE.
POKEDAT	If this bit is high during POKECYCLE, the result will be the loading of a transmit data in the UART or USRT.
POKEFILL	If this bit is high during POKECYCLE, the result will be the loading of the USRT fill character register.
POKEPULSE	Positive pulse generated during POKECYCLE and used as a clock to load various portions of the UART and USRT.
POKESTAT	If this bit is high during POKECYCLE, the result will be the loading of the status portion of the UART or USRT.
POKESYNC	If this bit is high during POKECYCLE, the result will be the loading of the USRT Sync Character register.
POS12V	+12V.
RCVCLK	This is the clock that is used to pulse the receive circuitry of the USRT. The mode in which the terminal is operating determines whether RCVCLK is derived from RS232 circuits DB or DD.
RCVLINDET'	Complement of RS232 circuit CF, buffered to TTL level.
RCVRRESET	A high results in the restart of the receiver circuitry of the USRT.
RCVRRESET'	Complement of RCVRRESET.
RCVURTDAT	This signal is the data that is sent to the UART and USRT Receive circuitry. Its source is determined by the mode in which the terminal is in.
RDE'	When low, enables the USRT or UART Receive data to the URTBUS lines.
READ'	MRD' line from the PSMP.
READDATA	Enables data portion of serial I/O shift register to the DB0 thorugh DB7 lines.

READDATA'	Complement of READDATA.
READURTDAT	Enables the receive data of the USRT or UART to the UART bus lines.
REQTOSEND	Request to send -- used to put the terminal in transmit mode.
REQTOSEND'	Complement of REQTOSEND.
RESET	Complement of RESETIN'.
RESET'	Complement of RESET.
RESETIN'	When low, causes the initialization of the terminal.
RSS'	A low pulse that loads the Sync register of the USRT.
SBCLOCK	Serial I/O bus clock line.
SBDATA	Serial I/O bus data line.
SCYCLECOMP	Indicates that the shift cycle of the serial I/O generator is on its last clock period of a shift cycle.
SCYCLECOMP'	Complement of SCYCLECOMP.
SDATAIN	Serial data from the serial I/O bus.
SDATABOUT	Serial data to the serial I/O bus.
SELSTDBY'	When low, develops CCITT circuit 116.
SEL0K', SEL1K', SEL2K'	These low-going signals enable the proper segment of ROM or RAM to the SIO microprocessor, as a function of the MA10 and MA11 signals.
SETDATRDY	Indicates that data has been loaded into the SIO Input register from the PSMP, via an OUTPUT 6 instruction. SETDATRDY, in turn, causes EXTDATRDY' to be developed.
SETITI'	A low indicates that the I-code being loaded in the Serial I/O Generator Shift register is "Invitation to Interrupt."
SHIFTCLK	Clock for serial I/O generation logic. Derived from CLOCK.
SHIFTCLK'	Complement of SHIFTCLK.
SHIFTENAB	Indicates that shift cycle of the serial I/O generation logic is in progress.
SHIFTENAB'	Complement of SHIFTENAB.
STILLITI	Still Invitation to Interrupt. Indicates that all of the following are true: a. ITI is set. b. A turn-off Invitation to Interrupt instruction is not being executed by the PSMP. c. INT has not yet been set.

SWE'	When low, enables the status word of the UART or USRT to the UART bus.
TDIRCVDAT	Receive data from TDI Interface circuitry, buffered to TTL level.
TDIZMITDAT	Transmit data, translated to TDI Interface Voltage levels.
TDS'	Low-going pulse that loads transmit data into the UART or USRT.
TERMRDY'	When low, develops RS232 circuit CD.
TESTMODE	When high, configures the terminal in test mode.
TESTMODE'	Complement of TESTMODE.
TFS'	Low-going pulse that loads the USRT fill character.
TPA	TPA line of SIO microprocessor.
TPB	TPB line of SIO microprocessor.
TRANFRQSEL'	When low, develops RS232 circuit CH.
TTLPUP	Pull-up line for unused TTL inputs.
TURNOFFITI'	Low indicates that an INPUT 2 instruction is being executed by the PSMP, which results in turning off Invitation to Interrupt mode of the serial I/O generation logic.
T0	Indicates that the SIO microprocessor is in time slot T0.
T2	Indicates that the SIO microprocessor is in time slot T2.
T2'	Complement of T2.
T3	Indicates that the SIO microprocessor is in time slot T3.
T6	Indicates that the SIO microprocessor is in time slot T6.

APPENDIX D
GLOSSARY OF SIGNALS FOR THE KEYBOARD SERIAL INPUT/OUTPUT INTERFACE BOARD

BADINT	A positive signal that resets the select flip-flop during an INVTOINT if keyboard has not caused an internal interrupt.
BITCLOCK	A positive clock from the serial I/O cable.
BITPOS0 through BITPOS02	Low-order bits of the I/O Shift Cycle Generator.
B1' through B9'	Keyboard data bits.
CF/F'	An asynchronous signal that clocks the interrupt flip-flop upon a key depression or repeat function.
CLK	Positive clock derived from BITCLOCK.
CLK'	Negative clock derived from BITCLOCK triggering occurs on low to high edge.
CTRL'	Shift Register output to keyboard LED.
DATAIN	Positive data derived from data line.
DATALINE	Positive data to/from the serial I/O cable.
DATAOUT	Tristate keyboard data or device number.
DEVICENO	Tristate device number output.
DEVNOSEL'	A low signal allows the device number to be selected.
DEVN00 through DEVN07	Device number determined by insertion of jumpers.
DEVSELECT	A high level indicates that the keyboard is selected and ready to send or receive data.
DEVSELECT'	The complement of DEVSELECT.
ENDCOUNT	A high pulse that indicates the end of an I/O shift cycle.
ENDCOUNT'	Complement of ENDCOUNT.
ENQ'	Shift Register output to keybord LED.
ENDWORD 1'	A low level allows the first 8 bits from the keyboard to be selected.
ENDWORD 2'	A low level allows the second 8 bits from the keyboard to be selected.

ERROR'	Shift Register output to keyboard LED.
FIRST DATA'	A low pulse indicates that the first bit of data in the I/O shift cycle is present on the bus.
FORMS'	Shift Register output to keyboard LED.
F1'	Data bit from keyboard for character insert key.
F2'	Data bit from keyboard (RTAB).
GETA'	Low level from I-code decoder selects the first 8 bits from the keyboard if the selected flip-flop is set.
GETB'	Same function as GETA', except the second 8 bits are selected.
ICODESHIFT	High level allows the I-code to shift into the Shift Register. A low level holds it in the Shift Register for the remainder of the I/O cycle.
INVTOINT	High level allows the keyboard device number to be compared with the bus data.
INVTOSEL	High level compares the keyboard data with the bus data. If the data is the same, the selected flip-flop remains set.
INVTOSEL'	During an INVTOSEL, a low level prohibits the device number data from being put on the bus.
LOCAL'	Shift Register Output to keyboard LED.
LTAI'	Shift Register output to keyboard LED.
NEWCHAR	High level allows the resetting of the keyboard strobe multivibrators when any keyboard key is released.
NEWCHAR'	High level in conjunction with signal Z506H high denotes a keyboard repeat function. Low level with Z506H denotes a single key stroke.
PUP	Power-up reset.
RCV'	Shift Register output to keyboard LED.
RESET'	Low level resets both multivibrators in repeat logic.
SEND A'	Low level from I-code decoder allows the information on the bus to be shifted into the LED Shift Register if the keyboard is selected.
SINT	High level sets the interrupt flip-flop when a key is pressed.
STARTCOUNT	High level indicates the beginning of an I/O shift cycle.
STROBE'	Low level indicates a key has been pressed and data is ready.
XMIT'	Shift Register output to keyboard LED.
Z506H	Refer to NEWCHAR'.

APPENDIX E
LINS

(Released LINS are to be filed here.)

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B	NO. 8381-001
		STYLE/MODEL B9348-50	PAGE 1 OF 1
ORIGINATOR: TIO Plainfield		TOP UNIT NO. All	
STD. INSTALL. TIME 0.1 Hour	UNITS AFFECTED See Checkpoint	UNIT DESCRIPTION Control Unit	
TITLE ODT HANGS IN NON-RECOVERABLE STATE (ECN 00145)			DATE 19 October 1978

INSTALLATION IS MANDATORY

CHECKPOINT: If Assembly Number is 2889 1273 Rev. H or higher, this LIN is not required.

PREREQUISITE: Coordinate with LIN 8381-002.

CONDITION: The ODT hangs when attempting to transmit to the system at the same time that the system is attempting to access the ODT.

CAUSE: When both Terminal and CPU are bidding for master Data Comm Control at the same time, neither can achieve master state.

CORRECTION: Upgrade Firmware to 4.9 to prevent hang.

* PARTS REQUIREMENTS:

Part Number	Description	Qty.	U.S. Unit List Price
2889 4095	ROM	1	$77.20
2889 4129	ROM	1	$77.20

INSTRUCTIONS:
Replace the following ROMS:

	Old Part Number (4.7FW)	New Part Number 4.9FW)	Location
1.	2889 1505	2889 4095	UAØ1
	2889 3691	2889 4129	UAØ7

2. Relabel PCB Assembly to 2889 1273 Rev. H.

*PARTS PACKAGE NO. 1625 6489 (Pkg. Price $159.10)

(Includes one set of the above parts)

F.E. Dist Code AP

☐ THIS CHANGE IS A RESULT OF FIELD REPORTING

FOR LIBRARY BINDER 327A

FOR F.E. TECHNICAL MANUAL FORM 1098381

Printed in U.S. America

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B	NO. 8381-003R
		STYLE/MODEL B9348-50	PAGE 1 OF 5
ORIGINATOR: TIO Plainfield		TOP UNIT NO. All	
STD. INSTALL. TIME .30 Hrs.	UNITS AFFECTED See Checkpoint	UNIT DESCRIPTION Control Unit	
TITLE CONVERT "GRAY SCALE VIDEO" TO "BINARY VIDEO" (ECN 00199)			DATE 10 January 1979

INSTALLATION IS MANDATORY

CHECKPOINT: If Assembly Number 2889 1349 or 2889 2453 has a ROM or PROM Char. Gen. in location UEØ3 and UEØ4 this LIN is required.

PREREQUISITE: None

CONDITION: The characters appear to be out of focus and are smaller in size than normally desired.

CAUSE: The design of the current Video Board does not provide the required level of display quality.

CORRECTION: Install this LIN which converts "Gray Scale Video" to "Binary Video". This will provide the required level of display quality.

PARTS PACKAGE NO. 1625 6521 (Pkg. Price $60.91)
(Includes one set of the following parts:)

Part Number	Description	Qty.	U.S. Unit List Price
2640 7023	ROM Character Generator	1	$60.91

INSTRUCTIONS:
NOTE: On Video Board Assemblies Part Numbers 2889 1349 or 2889 2453, the following must be done: (Reference the Video Board Logic Schematic Part Number 2889 1745 or Part Number 2889 2461 within T & F Manual Part Number 2889 2594)

1. Cut the following Runs (Solder Side):

From:	To:
UDØ3 Pin 13	UCØ4 Pin 6
UDØ4 Pin 13	UCØ4 Pin 7
UFØ4 Pin 3	UFØ5 Pin 8

   Reference Figures 2, 3, and 4 for parts locations.

2. Add the following Jumpers:

From:	To:
UGØ5 Pin 9	UFØ5 Pin 8
UDØ2 Pin 13	UCØ4 Pin 6 & 7

   Reference Figures 2 and 3.

3. Remove the I.C.'s from the following socket locations:
   a) UEØ2
   b) UEØ3
   c) UEØ4

   Reference Figure 1.

4. Add ROM Character Generator Part Number 2640 7023 into Socket UEØ2. Reference Figure 1.

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5. Delete the following items from Video Board Part List Number 2889 2792 or 2889 2453.
   a) 2889 0333; Character Generator ROM, Domestic
   b) 2889 0341; Character Generator ROM
   c) 2889 0358; Character Generator ROM

6. Add the Following item to the Video Board Part List Number 2889 2792 or 2889 2453.
   a) 2640 7023; Character Generator ROM

7. Relabel P. W. Board Assembly Video Board from 2889 1349 or 2889 2453 to 2640 7064 (Binary Video USASCII ROM, P. W. Board Assembly).

8. Redline Schematic 2889 1745 or 2889 2461 according to the above instructions.

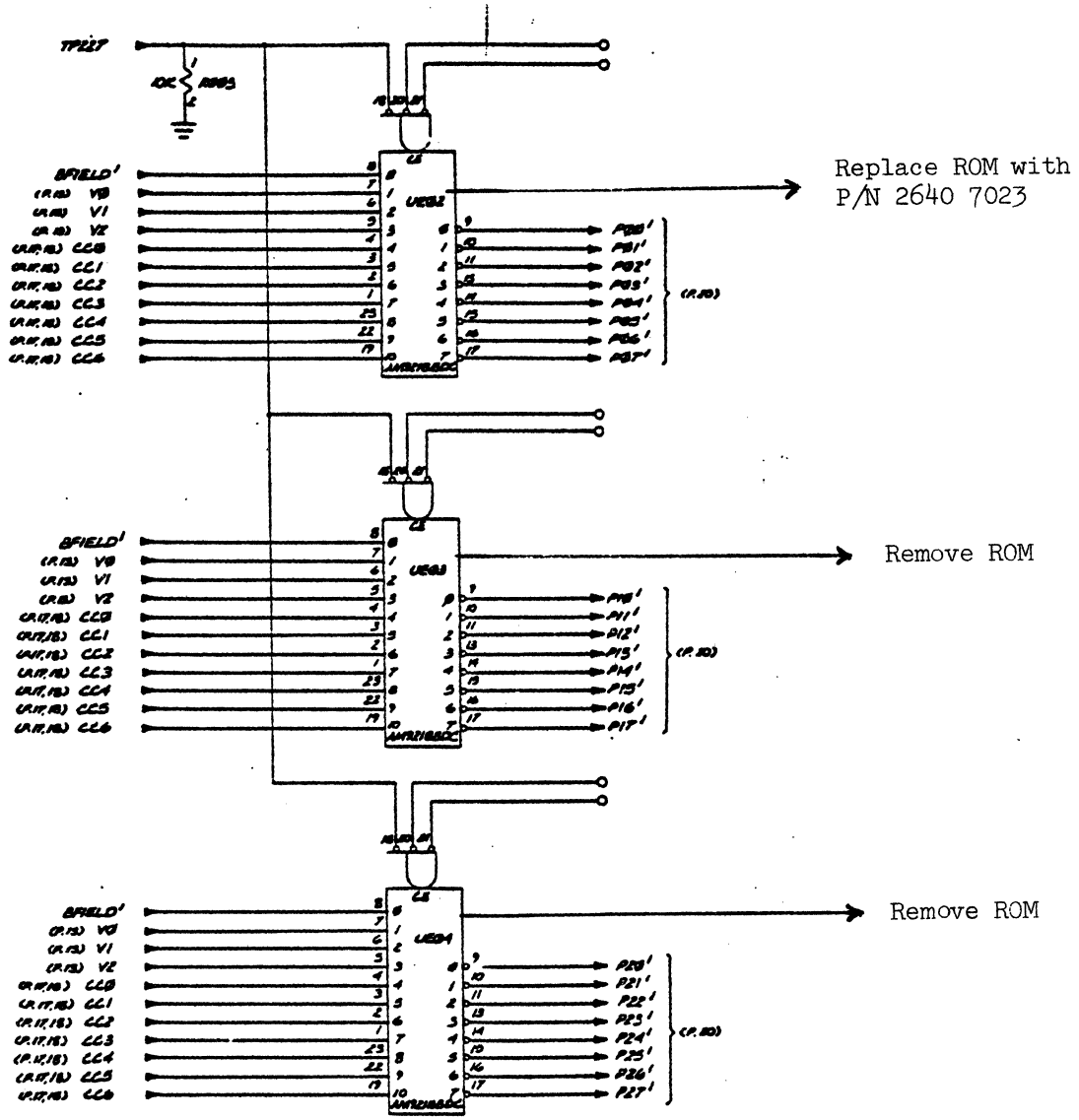

Figure 1

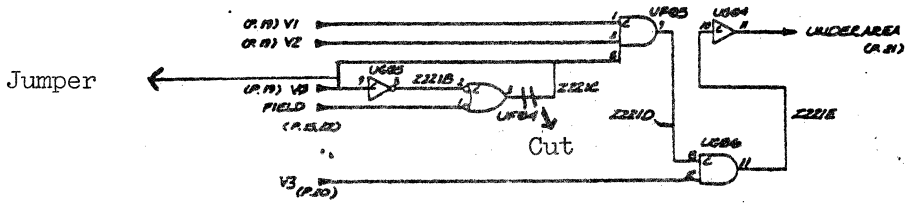

Figure 2

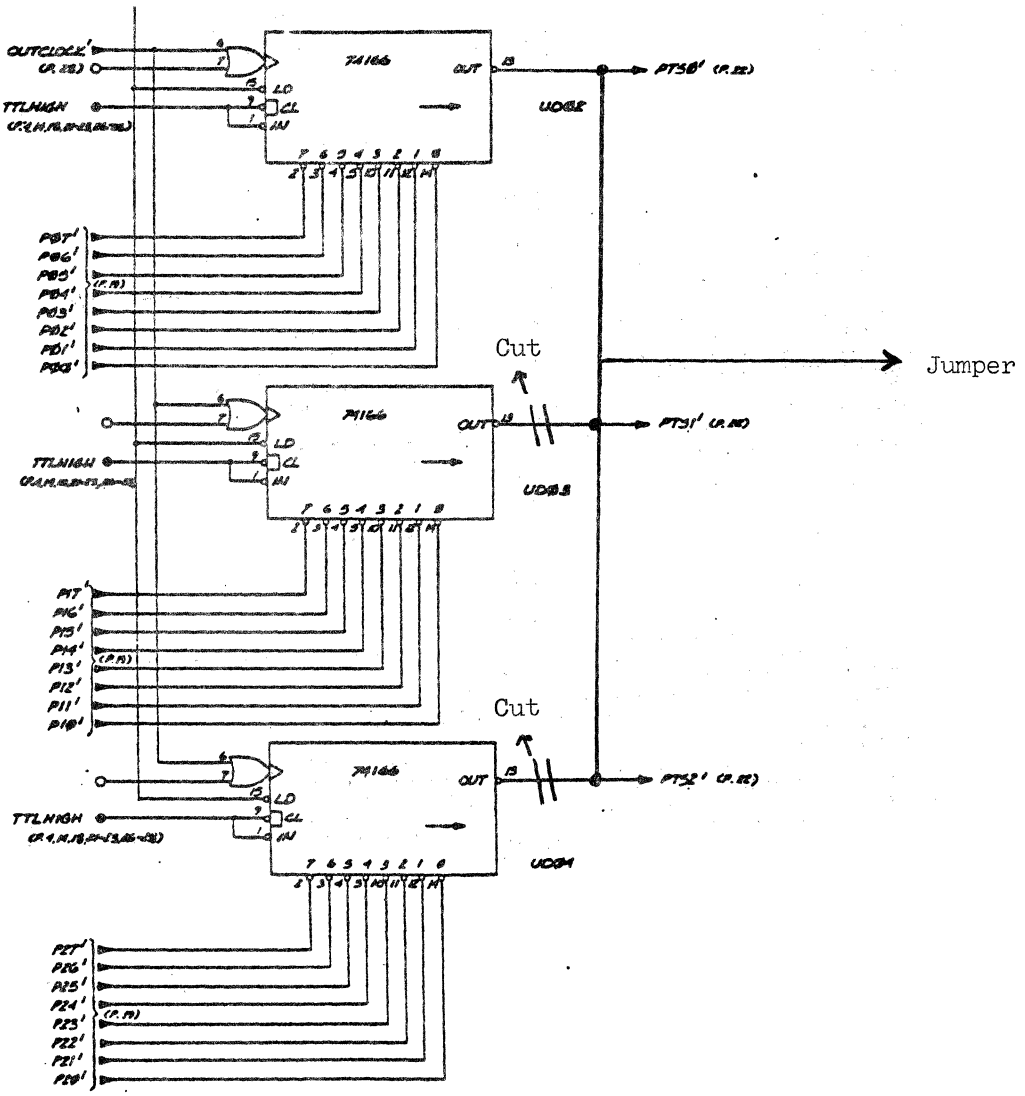

Figure 3

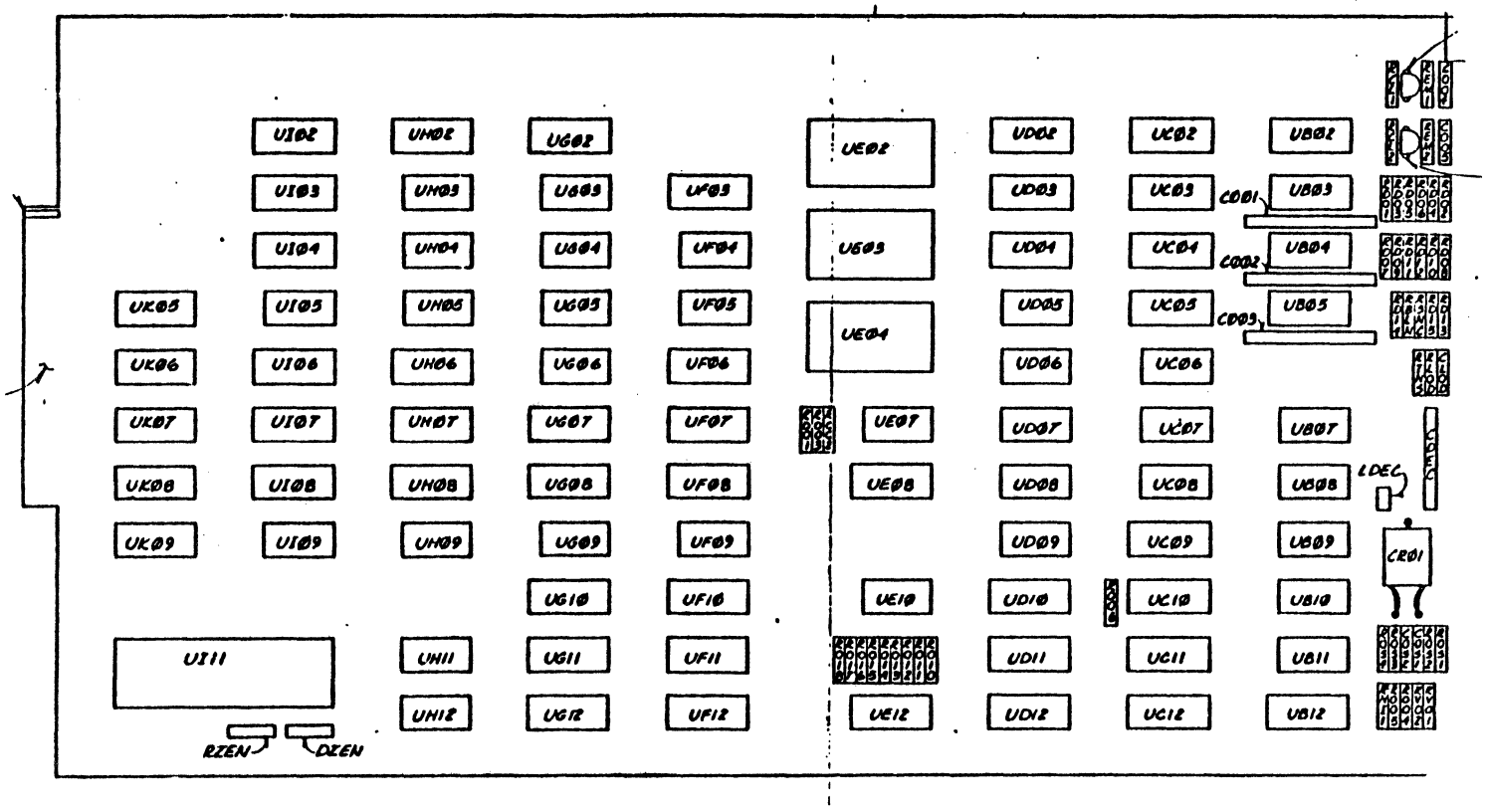

Figure 4

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APPENDIX F
RINS

(Released RINS are to be filed here.)