SuperSTOR-11

128K x 18 Bits
Add-In Memory System
For DEC PDP-11* Family

USER MANUAL

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CONTENTS

CHAPTER I

INTRODUCTION

The SuperSTOR-11 (referred to herein as SS-11) memories comprise a group of MOS semi-conductor, random-access memories that are designed to be used with the PDP-11 Unibus and modified Unibus. Each memory assumes the role of a slave device to PDP-11 processor or to any peripheral device that is designated bus master. The group provides storage for 16- or 18-bit data words (two parity bits are included in the 18-bit word), with capacity ranging from 16K words to 128K words in 16K blocks. An SS-11 memory can be assigned adjacent 16K blocks of addresses anywhere within the 124K Unibus address space. A special feature of the SuperSTOR-11 allows the assignment of part of the I/O page to memory, (although this can be done only for processors without memory management). Table 1-1 lists the significant specifications of a SuperSTOR-11 system.

The logic components of a SuperSTOR-11 memory are mounted on a single hex printed circuit board. The storage elements are 16, 384 x 1-bit, N-channel, MOS memory devices. A column of 16 of these devices is mounted on a module for each 16K block of addresses that is assigned to the memory: e.g., a 16K memory has 1 column of 16 devices and a 64K memory has four columns of devices. Table 1-2 lists the available SuperSTOR-11 memory configurations.

The use of MOS memory circuits provides advantages (both economical and operational) not available with core memory systems. The cost-per-bit for MOS memories is low and, unlike core memory, this cost remains approximately constant with size.

Unlike core, MOS memory provides non-destructive readouts; consequently, the write-after-read cycle time associated with core memory is eliminated. Furthermore, with dynamic MOS devices such as those used in the SuperSTOR-11 power consumption is much lower than with core memory. The disadvantage of MOS, storage volatility (i.e. data is not retained when power is lost), is compensated for by the availability of battery-supported power supplies tnat enable data retention for as long as several hours. The SuperSTOR-11 is designed for a special low-power mode to maximize the effectiveness of battery-powered operation.

Because the data storage element is a capacitor in the MOS storage device, all memory locations in the MOS memory must be periodically refreshed so that data remains valid. The controller on the memory module includes the logic and timing circuits to carry out the periodic refreshing operation.

TABLE 1-1

SuperSTOR-11 Specifications

Performance:

Access Time 350 nsec typical

Cycle Time 475 nsec typical
575 nsec maximum for refresh

Refresh: On Board

Parity: Incorporate all functions of M7850 Parity Controller

Power Requirements:

128K Words

+5v	2.4A Operate*
-15v	0.1A Operate
+12v	0.25A Operate

* Reduces to 1.5 under battery back-up operation

Voltages:

+5v
+12v or +15v and -12v or -15v

Battery Back-Up Mode:

Battery Back-Up input voltage is jumper selectable. In battery back-up mode, power check LED indicates battery is supplying +5v power to board. This LED also indicates memory is protected.

Environmental:

Temperature 0°c to 55°c operating ambient. 55°c Operation requires airflow to restrict temperature rise across module to less than 10°c. -40°c to 125°c storage.

Humidity:

Up to 90% with no condensation.

TABLE 1-2

SuperSTOR-11 Memory Configurations

Model Designation	Word Bit Length	Data Word Capacity
CM1600	16	16K
CM1600P	18	16K
CM3200	16	32K
CM3200P	18	32K
CM4800	16	48K
CM4800P	18	48K
CM6400	16	64K
CM6400P	18	64K
CM8000	16	80K
CM8000P	18	80K
CM9600	16	96K
CM9600P	18	96K
CM1120	16	112K
CM1120P	18	112K
CM1280	16	128K
CM1280P	18	128K

"P" denotes Parity.

CHAPTER II

INSTALLATION

2.1 General.

Installation of the SS-11 is relatively simple. First, the user should verify that factory-installed jumper wires relating to the number of memory chip banks are in place and that the SS-11 has been assigned the proper Unibus address space. The backplane should then be checked to ensure that the required dc voltages are available. Finally, the module is inserted into the backplane and a diagnostic check is carried out to assure correct operation. These procedures are discussed more fully in the following paragraphs.

Figure 2-1 shows the SS-11 module (128K memory is illustrated). The array of chips is located in the lower half of the board. In the upper left hand corner are stake pins E14 through E31. Wire wraps are installed across these pins to configure the address and size of the SS-11. Also in the upper left hand corner is a 16 pin socket which is configured with shorting bars to determine the CSR address for the board (between 772100 and 772136) and, for paging systems, the page address of the board.

2.2 Jumper Verification.

The SS-11 memory is shipped with factory installed jumpers, appropriate for the memory size and location. Section 3.2 describes the memory size and Unibus address jumpers.

2.3 Voltage Check.

Before the module is inserted in the backplane, check the backplane to ensure that the required DC voltages are present within tolerance. The DC voltages are listed in Table 2-1.

Jumpers J1 through J4 should be configured on the board to match the power available in the backplane. Table 2-2 represents the power options available.

All four DC voltages must be supplied if data retention is desired when AC power is removed. If +5 Battery Back-Up is not supplied, data will not be retained.

Table 2-3 lists the SS-11 pin assignments.

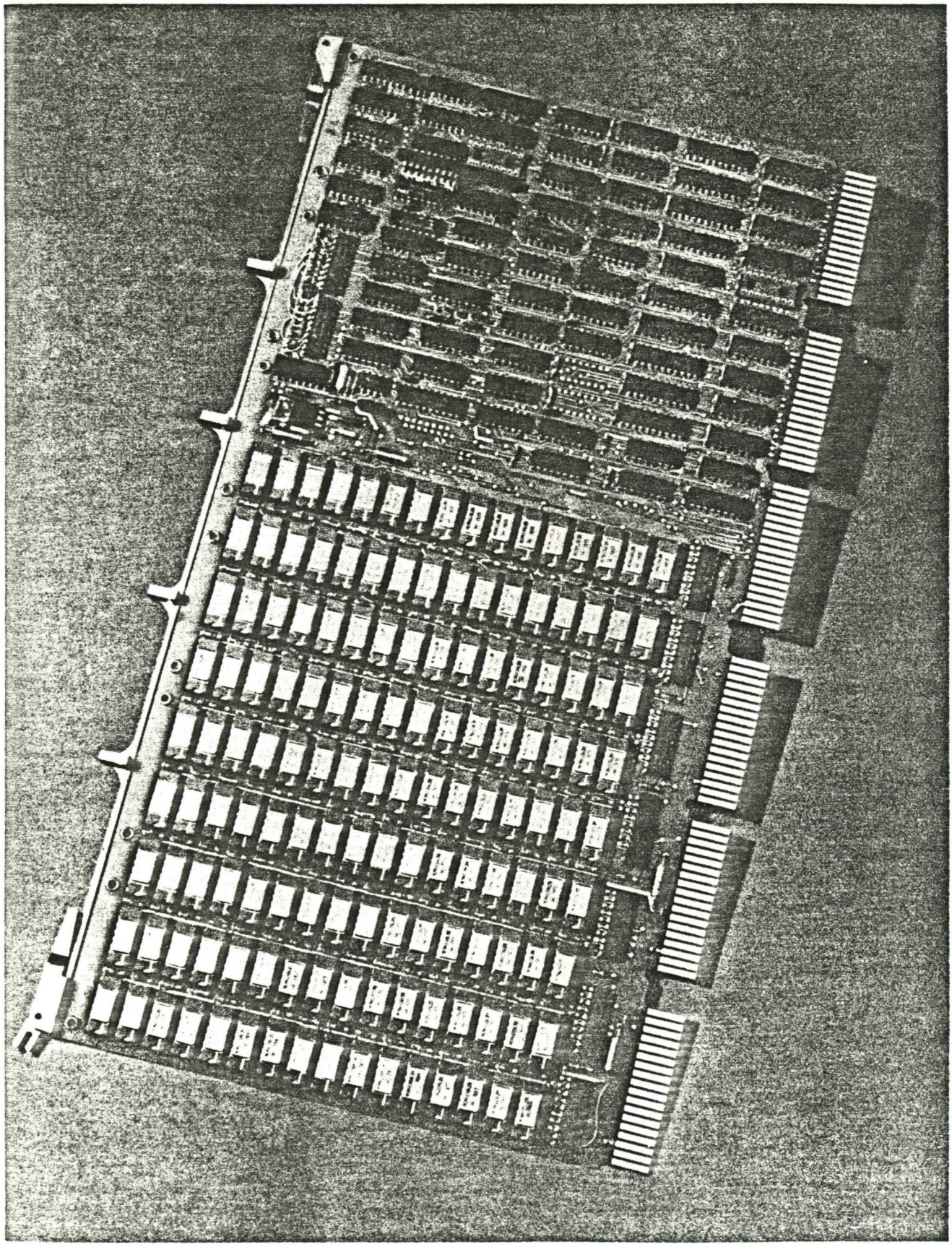

FIGURE 2-1

TABLE 2-1

Voltages Modified Unibus power points		
Voltage	Pin	Margin
+5	AA2, BA2, CA2	± 5%
+5 BBU **	BD1*	± 5%
+12/+15 BBU **	AR1	± 5%
-12/-15 BBU **	AS1	± 10%

+5 or +5 BBU is jumper selectable and used when Battery Back-Up voltage is available.

+12/+15 is jumper selectable.

-12/-15 require no jumpers.

GND AC2, AT1, BC2, BT1
CC2, CT1, DC2, DT1
EC2, ET1, FC2, FC1

*May be optionally left out.

**Battery Back-Up

TABLE 2-2

Power Options
For +5 install J1.
For Battery +5 install J2.
If Resident Power is +12V install J3.
If Resident Power is +15V install J4.

TABLE 2-3

SuperSTOR-11 Pin Assignment List

Signal List

Signal	Pin	Signal	Pin
A00L	BH2	D00L	AC1
A01L	BH1	D01L	AD2
A02L	BJ2	D02L	AD1
A03L	BJ1	D03L	AE2
A04L	BK2	D04L	AE1
A05L	BK1	D05L	AF2
A06L	BL2	D06L	AF1
A07L	BL1	D07L	AH2
A08L	BM2	D08L	AH1
A09L	BM1	D09L	AJ2
A10L	BN2	D10L	AJ1
A11L	BN1	D11L	AK2
A12L	BP2	D12L	AK1
A13L	BP1	D13L	AL2
A14L	BR2	D14L	AL1
A15L	BR1	D15L	AM2
A16L	BS2	INITL	AA1
A17L	BS1	MSYNL	BV1
C0L	BU2	PBL	AN2
C1L	~~BU1~~ BT2	DCLOL	BF2
		SSYNL	BU1

Power List

+15 or +12	AR1
-15 or -12	AS1
+5	AA2, BA2, CA2
+5 Battery	BD1
GND	AC2, AT1, BC2, BT1, CC2, CT1, DC2, DT1, EC2, ET1, FC2, FT1

Bus Grant Lines

BG4	DS2 to DT2
BG5	DP2 to DR2
BG6	DM2 to DN2
BG7	DK2 to DL2

NPGING to NPGOUT - CA1, CB1 (optional jumper)

2.4 Backplane Installation

When the DC voltages have been verified, insert the SS-11 into the Unibus backplane. Presently, three backplanes can be used with the SS-11, although other backplanes may become available; these three are DD11-C, DD11-D, and DD11-P. The DD11-C is a 4-slot backplane; the SS-11 can be inserted into slot 2 or slot 3. The DD11-D is a 9-slot backplane; slots 2-8 can be used for the SS-11. The DD11-P is another 9-slot backplane, which is used with the PDP-11/04 or PDP-11/34.

2.5 Diagnostic Check.

When the memory is connected to the Unibus, run the MS11 diagnostic program to verify that the memory is operable. If a problem arises, follow the instructions in the diagnostic. The SuperSTOR-11 memory is compatible with the existing diagnostic used for DEC MS11-JP, MM11-YP, MM11-DP when used with the M7850 parity module on the MUB*. Diagnostics may not work when memory is extended into the I/O page or if CMI Page Mode is selected.

* Modified Unibus

CHAPTER III

OPTIONS

3.1 Address Selection.

The 18 bits of Unibus addresses provide access to contiguous bytes from 0 to 128K words. Each word consists of two (2) Addresses. 0-124K are typically occupied by memory and the top 4K are usually reserved for memory mapped I/O.

The SS-11 addressing may be configured to start at any 16K boundary and provide contiguous memory up to 124K using wire-wrap jumpers.

The memory size of the board will determine the number of columns of memory chips. For example: A 32K memory board would have two (2) columns of devices (Columns 1 and 2) and wire wraps on stake pins E21 and E20. A 64K board would have four (4) columns of memory chips and wire wraps on E21, E20, E19, E18. (See Table 3-1).

The starting address of the memory depends on which of E24 through E31 the rows are jumpered to. (See Table 3-1). A 64K memory starting at address 0 would then have four (4) columns of memory devices and the first column would be wire wrapped to E30 (0-16K) and the second column would then be wire wrapped to E29 (16-32K), the third column to E28 (32-48K) and the fourth to E27 (48-64K). (See Fig. 1B). A 64K memory starting at 64K would have four (4) rows of memory devices but the first row would be wire wrapped to stake pin E26 (Base address 64-80K). (See Table 3-2). A 128K board would have all 8 rows of memory devices (nine if with parity option) and all stake pins E15-E22 and E24-E31 would have wire wraps.

The SS-11 may also add on to a system with 4 or 8K of memory already resident using jumpers E4, E5, E6, E7. (See Table 3-2).

3.2 I/O Page Relocation.

The I/O page resides in the top 4K of the 128K address range and memory may be extended 1, 2 or 3K words into the I/O page using wrap on pins E32, E33, E34, E35, E36, E37. (See Table 3-3).

WARNING: Some DEC software may not be compatible with reduced I/O page as they may have trouble sizing memory and performing trap instructions.

TABLE 3-1
STARTING ADDRESS

MEMORY-RESIDENT		0K	16K	32K	48K	64K	80K	96K	112K	128K	DESTINATION
	16K	E30	E29	E28	E27	E26	E25	E24	E31		E21
	32K	E29	E28	E27	E26	E25	E24	E31			E20
S 11	48K	E28	E27	E26	E25	E24	E31				E19
SIZE	64K	E27	E26	E25	E24	E31					E18
	80K	E26	E25	E24	E31						E17
	96K	E25	E24	E31							E16
	112K	E24	E31								E15
	128K	E31									E22

TABLE 3-2

4K INCREMENTS				DESTINATION
	0K	E4		E7
DEC	4K	E6		E7
SIZE	8K	E5		E7

TABLE 3-3

I/O Page Select	
Jumper	Description
None	Extend ØK into I/O Page
E32 to E33	Extend 1K into I/O Page
E34 to E35	Extend 2K into I/O Page
E34 to E35 E36 to E37	Extend 3K into I/O Page

3.3 Parity - CSR.

The SuperSTOR-11 generates a parity check bit for each memory byte. The parity control and status information is self-contained in CSR (Control and Status Register) on the SuperSTOR-11 and is program compatible with the DEC M7850 parity module. The CSR address is programmable to any 1 of 16 addresses between 772100 and 772136.

CSR address selection is done using shorting bars S5-S8 in socket Z49. (See Table 3-4 and Figure 3-1).

The CSR captures the high order address bits of a memory location with a parity error.

The CSR controls the memory to enable parity, write wrong parity and to display the Board Select line instead of the address error lines.

It can be addressed only in the word mode.

Register

Bit: 15 Name: PARERR H

Function: This bit is a read/write bit that is used to indicate a parity error by the memory or one force by writing into this bit. A parity error has occurred when it is a logical one.

Bit: 14 Name: CSR 14 H

Function: This bit is a read/write bit that is used to control the data to be loaded into CSR Bit 5 through 11. If Bit 14 is zero, then CSR bit 5 through 11 will contain either the data written into the register or if parity error occurred the address Bit 11-17. If Bit 14 is a one and a parity error has occurred - CSR Bit 5 through 8 will contain Board Sel 0 through Board Sel 3 at the time of the last parity error.

Bits: 13-12 Name: RESERVED CSR 13 & CSR 12

Function: Read these bits will result in a logical zero no matter what was written into them. They are reserved for future application.

Bits: 11 Name: CSR 11-5

Function: These bits are read/write bits and will contain data from the BUS, upper address bit of a parity error of Board Sel address if a parity error has occurred.

Bits: 4-3 Name: RESERVED CSR 4 & CSR 3

Function: Read only as a logical zero. Reserved for future use. Same as CSR 13 and 12.

Bit: 2 Name: CSR 2 Write Wrong Parity

Function: This CSR Bit controls writing wrong parity. If this bit is asserted and writing into the memory will write the wrong parity for that address.

On reading the address location, a parity error (CSR Bit 15) will be generated. This is useful in diagnostic testing of the memory parity function.

Bit: 1 Name: CSR 1 Reserved

Function: Read only as a logical zero. Reserved for future use.

Bit: 0 Name: CSR 0 Enable Parity Error

Function: If set it will generate BUS parity, line PB to be asserted on reading a memory location that has a parity error. This is a R/W bit.

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Table 2-1

Reference is to modified Unibus power pinouts

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Table 2-3

Change: Signal Pin C1L BUT to C1L BT2

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Use of Table 3-1

Example 1: Add 16KW SuperSTOR-11 over ØK resident memory.

E 30 wire wrap to E 21

Example 2: Add 64KW SuperSTOR-11 over 64K resident memory.

Wire wrap E 31 to E 18
Wire wrap E 24 to E 19
Wire wrap E 25 to E 20
Wire wrap E 2Ø to E 21

Example 3: Add 48KW SuperSTOR-11 over 32KW resident memory.

Wire wrap E 26 to E 19
Wire wrap E 27 to E 20
Wire wrap E 28 to E 21

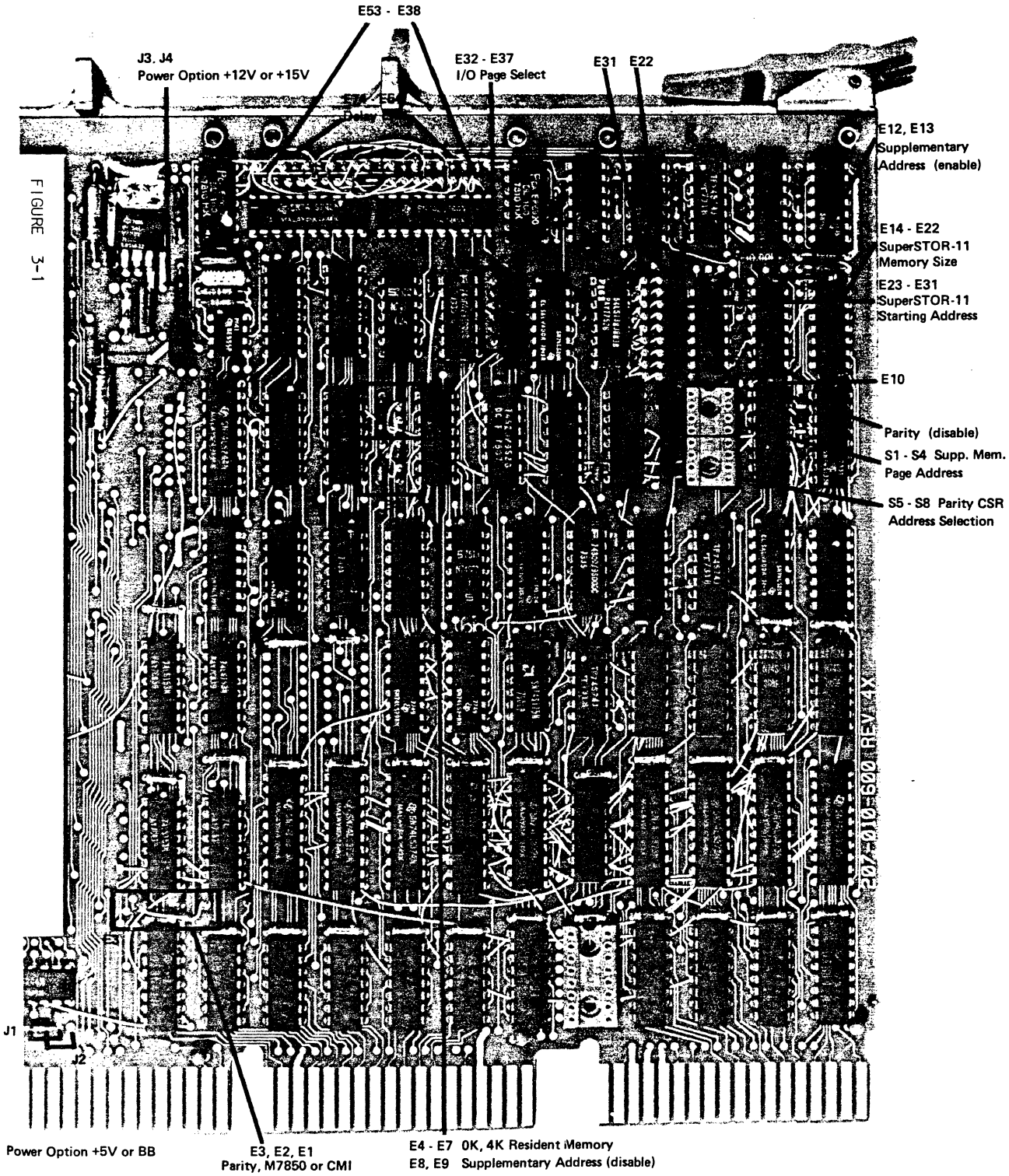
E53 - E38
J3. J4
Power Option +12V or +15V
E32 - E37
I/O Page Select
E31
E22
E12, E13
Supplementary
Address (enable)
E14 - E22
SuperSTOR-11
Memory Size
E23 - E31
SuperSTOR-11
Starting Address
E10
Parity (disable)
S1 - S4 Supp. Mem.
Page Address
S5 - S8 Parity CSR
Address Selection
J1
J2
Power Option +5V or BB
E3, E2, E1
Parity, M7850 or CMI
E4 - E7 0K, 4K Resident Memory
E8, E9 Supplementary Address (disable)

FIGURE 3-1

Pin Function Summary List

E1, E2, E3	Parity, M7850 or CMI
E4 - E7	ØK, 4K, 8K Resident Memory
E8, E9	Supplementary Address (disable)
E10, E11	Parity (disable)
E12, E13	Supplementary Address (enable)
E14 - E22	SuperSTOR-11 Memory Size
E23 - E31	SuperSTOR-11 Starting Address
E32 - E37	I/O Page Select
E38 - E74	Delay Line
S1 - S4	Supplementary Memory Page Address
S5 - S8	Parity CSR Address Selection
J1, J2	Power Option +5V or BB
J3, J4	Power Option +12 or +15V

TABLE 3-4

Shorting Bars				
S5	S6	S7	S8	CSR Address
I	I	I	I	772100
R	I	I	I	772102
I	R	I	I	772104
R	R	I	I	772106
I	I	R	I	772110
R	I	R	I	772112
I	R	R	I	772114
R	R	R	I	772116
I	I	I	R	772120
R	I	I	R	772122
I	R	I	R	772124
R	R	I	R	772126
I	I	R	R	772130
R	I	R	R	772132
I	R	R	R	772134
R	R	R	R	772136

CHAPTER IV

EXTENDED MEMORY OPTIONS

The SuperSTOR-11 is designed to support 22 bits of addressing for paging up to sixteen (16) 128K boards in a system. There are three (3) Supplementary Addressing options available: SAØ, SA1 and SA2.

In addition to the conventional Address Selection switches used to manually set the desired address range of the SuperSTOR-11, each SuperSTOR-11 board contains the necessary logic to allow it to be used as a separate and distinct bank or page of memory with up to 128K words per page. With this on-board logic, up to 16 pages of SuperSTOR-11 can be put on line for a total of two megawords of main memory addressing. Specific pages are brought in and out of the normal address range of the PDP-11 through the use of board enable and Select logic on the SuperSTOR-11.

Supplementary addressing option SAØ is to be used with processors with 22 bit addressing capability. The extended 4 bits of addressing are brought to the fingers of the board with the Standard Unibus address bits Ø - 17. (See Table 4-1). The I/O page is reserved between addresses 1776ØØØØ and 17777776. Board enable information is provided through on board shorting bars in Z49.

TABLE 4-1

Supplementary Address Bit	Finger
BUS A18L	BE2
BUS A19L	BE1
BUS A20L	AP1
BUS A21L	AN1

Also incorporated into the SuperSTOR-11 are unique supplementary addressing options SA1 and SA2 which allow standard PDP-11's which utilize 18 bit addressing to expand main memory capacity far in excess of its normal range.

Using extended addressing system SA1, board select information is programmed into an external parallel output device such as DEC DR11-C. Four select lines are then connected to each SS-11 through a standard on-board 16 pin socket and four enable lines are programmed on the socket. Each board receives board select information externally and simultaneously with all other boards.

Using supplementary addressing system SA2, Board enable and select information is programmed internally to each board using bits 5, 6, 7, and 8 in each CSR. Board select data is written into the CSR with bit 13 set. If a 1 is not being written concurrently into bit 13, bits 5, 6, 7, and 8 will not be written into the board select register. This is to prevent other software from changing pages when not desired.

Selected page data may be read from CSR bits 5, 6, 7, and 8 only if CSR bit 14 is set. To read CSR,page data is bit 14 is not set a user may read the data using the following code:

```
Bis     #40000, @ #7721XX

MOV     @#7721XX, PAGDAT
```

Bits 5, 6, 7, and 8 of PAGDAT now contain the page address programmed into CSR 7721XX. Board enable information is programmed through on Board shorting bars in Z49. Using SA2, each board receives board select information individually and before selecting a new page, the old page should be deselected.

Signals on the Board Select lines determine which page of SuperSTOR-11 memory is currently being accessed by the CPU. These signals are provided by the user and should be present at address time or else latched into a register prior to generating a memory request. These lines can remain latched until another page is desired.

Using SA1, socketed board enable lines are used to set on board switches that determine which board select signals a particular SuperSTOR-11 will respond to, i.e. effectively the page address of that particular board.

Signals on Board Enable lines are high true, the binary number indicating the responding page address. Board Select lines are low true and should be terminated with 120 ohms Thevenin equivalent at the drivers.

Figure 1 shows typical electrical connections for putting several SuperSTOR-11 memory systems on line using SA1. Figure 1 corresponds to the case of fixed page addresses using the on-board Board Enable switches.

Portions of memory such as the upper and lower 4K words can be common memory responsive to all page addresses. This greatly simplifies communication between SuperSTOR-11 pages as well as between pages and the various I/O devices.

Caution must be used when DMA devices exist on the bus to check that data from the DMA device goes to the right page.

Listed below are the steps and pin assignments to be used for paging mode:

Step 1. Connect E12 - E13 to enable supplementary addressing.

Step 2. Set up Board Select Assignment Jumpers. High True.

```
Bit Ø Low Z49 Pin 1 - 16
Bit 1 Low Z49 Pin 2 - 15
Bit 2 Low Z49 Pin 4 - 13
Bit 3 Low Z49 Pin 3 - 14
```

Step 3. Set up Board Select Address Inputs. Low True.

```
Bit Ø  TB1  Pin 1
Bit 1  TB1  Pin 3
Bit 2  TB1  Pin 7
Bit 3  TB1  Pin 5
Ground pins 9-16
```

CHAPTER V

COMPATIBLE BACKPLANES

5.1 The following backplanes can be used with the SuperSTOR-11 in all models of DEC computers from 11/04 up to 11/60 without modification:

DD11C
DD11P(K)(F)
DD11D

5.2 Backplane MF11U can be used with the following modifications:

a. pin 2BU2 is wire wrapped to 2BU1;
b. pin 1BF2 is wire wrapped to 2BF2;
c. pin 2AS1 and 2AR1 must be isolated from ground;
d. pin 2AS1 is wire wrapped to 3AK1;
e. pin 2AR1 should be wire wrapped to 3AA1;
f. S-11 may not be jumpered for battery backup;
g. S-11 board may be plugged into the parity model slot 2.

5.3 The SuperSTOR-11 may also be used in backplanes MF11L (P), ME11L and DD11B with the following modifications:

a. pin AR1 must be isolated from ground and wire wrapped to CU1;
b. pin AS1 must be isolated from ground and wire wrapped to CB2;
c. S-11 may not be jumpered for battery backup.

5.4 If technical questions on SuperSTOR-11 installation still remain unanswered, please contact technical personnel at Cambridge Memories Minicomputer Products Division. Telephone (617) 890-6000.