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1604-A INSTRUCTIONS

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#### PREFACE

This manual describes the characteristics, instructions, and manual controls of the CONTROL DATA\* 1604-A computer.

<sup>\*</sup> Registered trademark of Control Data Corporation.

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#### CHAPTER 1 DESCRIPTION

The CONTROL DATA\* 1604-A is a stored-program, general-purpose digital computer with a large storage capacity, fast computation and transfer speeds, and special provisions for input/output communication. The 1604-A is designed to handle large-volume data processing and to solve large-scale scientific problems. The compact equipment, constructed from solid-state components throughout, is suitable for use in a semipermanent office environment.

#### **1604-A CHARACTERISTICS**

Stored-program general-purpose digital computer	Program interrupt	
Parallel mode of operation	Console, includes: Photo-electric Paper tape pune	
48-bit word, 2 instructions per v	word	Electric typewr Register conter
Single address logic		-
Operation code	6 bits	Flexible instruction
Designator	3 bits	Fixed-point ari
Base Execution Address	15 bits	(integer and fra Floating-point a
Six 15-bit index registers		Logical and ma Indexing
Indirect addressing		Storage searchi
Magnetic core storage		Binary arithmetic
32 768 48-bit words		Parallel additio
01,100 10 510 101 40		access
Two independent 16,384 word ba	nks	Modulus $2^{48}$ - 2
alternatery phased		Real-time clock
1.8 uson offortive quale time	A Second Second	itear time clock
4.0 µsec enective cycle time	١	Completely solid-s
(representative program)	1	Diode logic
6.4 $\mu$ sec total cycle time		Transistor amp
Terret / output		
Danollol transmission of	10-bit word	a
Parallel transmission of	40-DIC MOLO	5
inree separate putter inp	Jui channels	

Electric typewriter Register contents displayed in octal

Paper tape punch

Flexible instructions Fixed-point arithmetic (integer and fractional) Floating-point arithmetic Logical and masking operations Indexing Storage searching

Photo-electric paper tape reader

Binary arithmetic Parallel addition in 1.2  $\mu$ sec without access Modulus 2<sup>48</sup> - 1 (one's complement)

Completely solid-state Diode logic Transistor amplifiers

Three separate buffer output channels

High-speed transfer channel (4.8  $\mu$ sec per word)

<sup>\*</sup>Registered trademark of Control Data Corporation

#### LOGICAL DESCRIPTION

The 1604-A performs calculations and processes data in a parallel binary mode through the step-by-step execution of individual instructions which are stored internally along with the data.

Functionally, the computer may be divided into four major sections. Storage provides internal storage for data and instructions; Control coordinates and sequences all operations for executing an instruction by obtaining the instruction from storage and translating it into commands for the other sections; Arithmetic performs the arithmetic and logical operations required for executing instructions; and Input/Output provides communication between the computer and the external equipment.

The registers in the computer are identified by letters (table 1-1). The arithmetic properties of the registers are detailed in table 1-2. The operational registers usually hold the end result of an operation; their contents are displayed on the console and may be changed manually.

Register	Function	Register	Function
A*	Accumulator	$\mathrm{U}^2$	Auxiliary Program Control
Q*	Auxiliary Arithmetic	R	Address Buffer
$B^1$ through $B^{6}*$	Index registers (six)	$\left. \begin{array}{c} ^{\cdot} CCR \\ CR^{1} \\ through \\ CR^{6} \end{array} \right\}$	Buffer Control
P*	Program Address		
U <sup>1</sup> *	Program Control	x	Exchange

TABLE 1-1. REGISTERS OF THE COMPUTER

\* Operational Registers

#### STORAGE SECTION

The magnetic core storage section of the 1604-A computer provides high-speed, random access storage for 32,768 words. It consists of two independent storage units each with a capacity of 16,384 words. These units operate together during the execution of a stored program and thus are considered as one 32,768 word storage system.

A word is 48 bits in length and is used in two ways: as two 24-bit instructions or as a 48-bit operand (data word). The location of each word in storage is identified by an assigned number or address. When a word is taken (read) from or entered (written) into storage, a reference is made to the storage address which holds the word. All odd storage addresses are located in one storage unit, all even addresses in the other.

The cycle time, or time for a complete storage reference, is 6.4  $\mu$ sec. Since the storage cycles of the two sections overlap one another in the execution of a program, the average effective cycle time for random addresses is about 4.8  $\mu$ sec.

#### CONTROL SECTION

The control section directs the operations required to execute instructions and to initiate the exchange of data with external equipment. It also establishes the timing relationships needed to perform the operations in the proper sequence.

The control section acquires a program word from storage, interprets it and sends the necessary commands to other sections. A program word is a pair of 24-bit instructions which together occupy one storage location as a 48-bit word. The higher-order 24 bits are the upper instruction; the remaining 24 bits, the lower instruction.

f	b	m, y, or k
(6 bits)	(3 bits)	(15 bits)
Operation	Index	Base Execution
Code	Designator	Address

#### Instruction Format

Each of the 62 instructions has a unique 6-bit operation code which specifies the operation to be performed.

The index designator generally specifies one of the six index registers whose content is to be added to the execution address. This process is called address modification. However, the index designator may also specify indirect addressing or a condition for jump and stop instructions.

The execution address may be used in one of three ways: as an address, m, of an operand; as an operand, y; or as a shift count, k.

The eight operational registers in the control section are P,  $U^1$  and  $B^1$  through  $B^6$ .

The program address register (P) is a two's complement additive counter. It provides program continuity by generating in sequence the storage addresses which contain the individual program steps. Usually at the completion of each two instructions the count in P is advanced by one to specify the address of the next program word.

The program control register (U<sup>1</sup>) holds a program word while the two instructions contained in it are executed. The upper instruction is executed first followed by the lower instruction.

After executing an instruction, a half exit, full exit, or jump exit is performed. A half exit allows the lower instruction of a program word to be executed. A full exit advances the count in P by one and executes the upper instruction of the new program word specified by the contents of P. A jump exit allows a new sequence of instructions to be executed; the storage location of the new instruction is specified by the execution address of the jump instruction. The execution address, in this case, is entered into P and specifies the starting location of a new sequence of program words.

The auxiliary program control register  $(U^2)$  is a 15-bit subtractive accumulator used primarily in the modification of the base execution address. The contents of the specified index register are transmitted to the Address Buffer register (R), which has provisions for counting, complementing and storing. The contents of R are then added to the contents of  $U^2$  which holds the execution address.

Index registers  $B^1$  through  $B^6$  are 15-bit registers used to modify the base execution address when relative addressing is used. The index registers are also used to designate the number of words in search and transfer instructions and for other indexing operations.

#### ARITHMETIC SECTION

The arithmetic section of the 1604-A computer consists of two operational registers. A and Q, and one secondary register, X.

Register	No. of Stages	Modulus	Complement Notation*	Arithmetic	Result
A	48	2 <sup>48</sup> -1	one's	subtractive	signed**
Q	48	2 <sup>48</sup> -1	one's		signed
$u^2$	15	$2^{15}$ -1	one's	subtractive	signed
Р	15	$2^{15}$	twots	additive	unsigned
R	15	2 <sup>15</sup>	two's	subtractive	unsigned

TABLE 1-2. ARITHMETIC PROPERTIES OF REGISTERS

The A register (Accumulator) is the principal arithmetic register. Some of the more important functions of A are:

- 1) Arithmetic operation A initially holds one of the operands in addition, subtraction, multiplication and division. The result is usually held in A.
- Shifting A may be shifted to the right or left separately or in conjunction with Q. Right shifting is open-ended; the lowest bits are discarded and sign extended. Left shifting is circular; the highest order bit appears in the lowest order stage after each shift; all other bits move one place to the left.
- 3) Control for conditional instructions A holds the word which conditions jump and search instructions.

The Q register is an Auxiliary Arithmetic register and is generally used in conjunction with the A register. The principal functions of Q are:

- 1) Providing temporary storage of contents of A while A is used for another arithmetic operation.
- 2) Forming a double-length register, AQ or QA.
- 3) Shifting to the right or left, separately or in conjunction with A.
- 4) Participating with the A register in multiplication, division and logical product operations (masking).

<sup>\*</sup> Refer to Appendix

<sup>\*\*</sup> The result of an arithmetic operation in A satisfies A ≤ 2<sup>47</sup> -1 since A always is treated as a signed quantity. When the result in A is zero, it is always represented by 000...00 except when 111...11 is added to 111...11 or 000...00 is subtracted from 111...11. In these cases the result is 111...11 (negative zero).

The X (Exchange) register is used in the exchange of data between storage and the arithmetic section. X provides one of the inputs to the accumulator borrow pyramid.

#### INPUT/OUTPUT

The input/output section controls the flow of data to and from the computer. Data is transmitted in one of two ways: High Speed Transfer or Buffering.

High speed transfer operations are controlled directly by the program (Search and Transfer Sequence) and are used to transfer data between computers or between a 1604-A and high speed external equipment (e.g., a line printer). I/O channel number 7 is used for high speed transfer.

Buffering is an asynchronous transmission of data on I/O channels 1 through 6. Once a buffer operation has been initiated by the program, buffering and program operations proceed concurrently. Computation continues while buffering takes place at rate dependent on the external equipment. Buffering and program operations share access to computer storage; buffer operations have priority. High speed transfer is a program operation.

The buffer channels are paired with input on odd channels and output on even channels:

Input	Output		
Channel 1	Channel 2		
Channel 3	Channel 4		
Channel 5	Channel 6		

All six channels may be used concurrently. Each channel may be connected to several external equipments (figure 1-1) but only one equipment may use a channel at any instant. All I/O operations are parallel transmission of 48-bit words.

#### PROGRAM COMPATIBILITY

The 1604/1604-A switch enables the 1604-A to run programs written for the 1604. A red background light in the leftmost digit of the P register indicates that the switch is in the 1604 position.

Experience to date has shown only two areas of program incompatibility between the 1604 and the 1604-A:

- In the 1604, the EXF code 74.004001 locks out all interrupts; in the 1604-A, this code locks out only external interrupts. (See Appendix, page 29 for internal interrupt codes).
- In the 1604-A, when reading input words into buffer control word addresses (e.g., Auto Load operation), the fast 1604-A control word registers require that the upper address of the input word be the control word address plus one.



Figure 1-1. Typical 1604-A System

#### CHAPTER 2

#### DESCRIPTION OF INSTRUCTIONS

#### WORD FORMAT

A computer word consists of 48 bits and may be interpreted as one 48-bit data word or two 24-bit instructions. Each instruction is composed of three parts or codes: operation code, index designator, and execution address. The higher-order 24 bits of the word are called the upper instruction and the lower-order 24-bits are called the lower instruction.

bit 47		bit 24	
Operation (Function) Code	Index Designator	Execution Address	
f	b, j	m, y, k	
6	L 3	15	
bits	bits	bits	
Code	Range		
Operation f	01 - 76 <sub>8</sub>	Specifies the operation to be performed. A 00 or 77 code is interpreted as a fault, which stops computer operation.	
Index Designator b, j	0 - 7	Specifies the addressing mode, jump or stop condition, index register or external function depending on the operation code.	
Execution Address m, y, k	00000 through 77777 <sub>8</sub>	Used in one of three ways: 1) as a shift count, k 2) as an operand address, m 3) as an operand, y	

#### OPERATION CODE

The f portion of an instruction is the operation code which specifies which instruction is to be done. The interpretation of the rest of the instruction is conditioned by f.

#### INDEX DESIGNATOR

The b or j portion of an instruction designates:

1)	The addressing mode	b = 0	direct addressing
		b = 1 - 6	relative addressing
		b = 7	indirect addressing

2) The condition for jump or stop instructions (see Jumps and Stops, page 2-27).

- 3) The type of EXF instruction
- tion j = 0 select j = 1-6 activate j = 7 sense
- 4) The index register in index instructions

#### EXECUTION ADDRESS

The base execution address may be used as: (1) a shift count, k; (2) an operand, y; (3) an address of an operand, m, in storage; (4) an external function code (chapter 3). The execution address may also be modified or unmodified depending on the instruction and index designator. If unmodified, the address is represented by the lower-case symbol k, y, or m; if the address is modified the symbols are capitalized. The following examples point out the relationship between the unmodified and modified execution address.

The modified shift count K is represented by:

1) $K = k + (B^{D})$ where:	K	= modified shift count
	k b	= unmodified shift count (execution address)
	(B <sub>2</sub> )	= contents of index register b.

If the index designator = 0, then K = k.

The modified operand Y is represented by:

2)	$Y = y + (B^{D})$ where:	Y	÷ 1	modified operand
		у (В <sup>b</sup> )	= 1 = (	unmodified operand (execution address) contents of index register b.

If the index designator = 0, then Y = y.

The modified operand address M is represented by:

3)  $M = m + (B^b)$  where: M = modified address of operand $m_ = unmodified address of operand (execution address)$  $(B^b) = contents of index register b.$ 

If the index designator = 0, then M = m. Note that (3) is the only case in which the execution address is interpreted as an address of an operand.

#### ADDRESS MODIFICATION

The three possible modes of address modification are identified by the index designators as follows:

 b = 0 No Address Modification. In this mode the execution address is interpreted without modification; nothing is added to or subtracted from it. (Direct addressing.)

- 2) b = 1-6 Relative Address Modification. In this mode the execution address is modified and is equal to the initial execution address plus the contents of the designated index register. One's complement arithmetic is used in determining the modified execution address.
- 3) b = 7 Indirect Addressing. In this mode the base execution address specifies the address of the operand address rather than the operand. The 48-bit word is read from storage and the lower-order 18 bits of the word are interpreted as the b designator (3 bits) and execution address (15 bits) of the present instruction. The new index designator may refer to any one of the three modes.

Examples:

fbm1) No Address ModificationLDA 0 address

This instruction is interpreted as load accumulator from the storage location designated by the sum of the execution address and the contents of the specified index register,  $B^b$ . Since b = 0, no index register is designated and m specifies the storage location whose contents are loaded into A.

2) Relative Address Modification LDA 6 address  $(B^6) = 00001_{o}$ 

In this example, the accumulator is loaded from the storage location designated by the execution address plus the contents of index register 6. Therefore, the contents of the storage location named by the execution address plus  $00001_8$  is loaded into the accumulator. M = m + (B<sup>b</sup>).

3) Indirect Addressing



When the b designator of the current instruction is 7, the mode is indirect addressing. The lower 18 bits of the contents of the storage location designated by the execution address, 00100, are read from storage into the  $U^1$  register where they are interpreted as the index designator and execution address of the current instruction.

The index designator is inspected again and because it is not 0 or 7 the relative address mode exists. (Note that the new index designator could reference any one of the three modes of address modification.) The execution address, 00200, plus the contents of  $B^6$ ,  $00001_8$  specify the storage location whose contents will be loaded into the accumulator.  $M = 00200_8 + (00001_8) = 00201_8$ 

#### EXECUTION OF A PAIR OF INSTRUCTIONS

Example: f b m f b m (00300) = LDA 0 00310 ADD 1 00210 (00301) = STA 0 00400 SLS 0 00301 (B<sup>1</sup>) = 00101<sub>8</sub>

The P register holds address 00300 (an even lowest bit indicates the address of the program step is in the even storage unit). The storage reference is initiated; the 48-bit word is read from address 00300 and entered into  $U^1$ . Computer operation is now dependent upon the interpretation of the 24-bit instruction in the upper half of  $U^1$ .

The operation code, LDA, and the index designator, 0, are translated. The function of the upper instruction, LDA, is to load the A register with the contents of the designated storage location. Because the index designator is 0, the execution address is not modified. The translation of the operation code initiates the sequence of the commands which execute the instruction and the operand in address 00310 is loaded into A.

The lower instruction in  $U^1$  is transferred to  $U^1$  upper and translated. The ADD instruction causes the quantity in storage location M to be added to the contents of the A register. Since the index designator is not 0 or 7, the contents of the index register are added to the execution address to form M.  $M = m + (B^b) = 00210_8 + 00101_8 = 00311_8$ . The contents of storage address 00311 are added to the contents of the A register completing the instruction. The contents of the P register are increased by one and the pair of instructions at address 00301 is read from storage and executed.

#### INSTRUCTIONS

The 62 computer instructions are described on the following pages (EXF instructions are discussed in detail in chapter three). The title line contains the numeric code, the mnemonic code and format, name, and average execution time of the instruction. Abbreviations and symbols are defined as follows:

А	Accumulator
A <sub>n</sub>	The binary digit in position n of the A register
→ →	Transmit to
b	Index designator
в <sub>р</sub>	Designated index register
Exit (Full)	Proceed to upper instruction of next program step
Half exit	Proceed to lower instruction of same program step
j	The condition designator for jump and stop instructions
k	Unmodified shift count
K	Modified shift count. $K = k + (B^b)$
LA	Lower address - execution address portion of lower instruction of a program step
m	Unmodified operand address
М	Modified operand address. $M = m + (B^b)$
()	Contents of a register or storage location
( )'	One's complement of contents of a register or storage location
( )f	Final contents of a register or storage location
( )i	Initial contents of a register or storage location
Q	Auxiliary arithmetic register
UA	Upper address
Х	Exchange register
У	Unmodified operand
Y	Modified operand. $Y = y + (B^b)$

#### INSTRUCTION EXECUTION TIME

The time needed to execute an instruction varies from application to application because of the following factors.

If the instruction occupies the upper position in an instruction word, the time needed to read the word from storage must be considered.

If consecutive storage references are made to the same storage unit (even-even or odd-odd) the read access time from storage will be maximized.

If indirect addressing is specified, at least one additional reference will be needed to complete the instruction. (The new index designator may itself specify indirect addressing.)

If buffer operations are using storage, an instruction must wait until storage is released.

If a storage reference is made at the end of the preceding instruction, execution of the next instruction may be delayed.

The instruction execution times listed on the following pages were compiled by averaging the times for a long list of the same instructions. The list was arranged for typical values of the factors.

## ORDER OF INSTRUCTIONS

Numeric Code	Mnemonic Code	Name	Timing*
DATA TRANSMI	SSION	~	
12	LDA	LOAD A	
13	LAC	LOAD A COMPLEMENT	
16	LDQ	LOAD Q	
17	LQC	LOAD Q COMPLEMENT	
20	STA	STORE A	72
21	$\operatorname{STQ}$	STORE Q	
52	LIU	LOAD INDEX (UPPER)	
53	LIL	LOAD INDEX (LOWER)	
56	SIU	STORE INDEX (UPPER)	
57	SIL	STORE INDEX (LOWER)	
SHIFTING			
01	ARS	A RIGHT SHIFT	
02	QRS	Q RIGHT SHIFT	
03	LRS	AQ RIGHT SHIFT	28 + 4 s**
05	ALS	A LEFT SHIFT	2.0 10.
06	QLS	Q LEFT SHIFT	
07	LLS	AQ LEFT SHIFT	
ADDRESS MODE	FICATION		
6.0	SAU	SUBSTITUTE ADDRESS (UPPER)	7.2
61	SAL	SUBSTITUTE ADDRESS (LOWER)	7.2
54	ISK	INDEX SKIP	5.6
55	IJP	INDEX JUMP	4.4

\*Timing is average execution time in  $\mu$ sec

\*\*s = Number of places shifted

ARITHMETIC	C (Fixed)		
14	ADD	ADD	7.2
15	SUB	SUBTRACT	7.2
24	MUI	MULTIPLY INTEGER	25.2 + .8n*
25	DVI	DIVIDE INTEGER	65.2
26	$\mathbf{MUF}$	MULTIPLY FRACTIONAL	25.2 + .8n*
27	$\mathrm{DVF}$	DIVIDE FRACTIONAL	65.2
ARITHMETIC	C (Floating)		
30	FAD	FLOATING ADD	18.8
31	FSB	FLOATING SUBTRACT	18.8
32	FMU	FLOATING MULTIPLY	36.0
33	${ m FDV}$	FLOATING DIVIDE	56.0
34	SCA	SCALE A	2.8 + .4s**
35	SCQ	SCALE AQ	2.8 + .4s**
NO ADDRESS			
04	ENQ	ENTER Q	
10	ENA	ENTER A	
11	INA	INCREASE A	3.0
50	ENI	ENTER INDEX	
51	INI	INCREASE INDEX	
JUMPS AND S	STOPS (Normal)		
22	AJP	A JUMP	
23	QJP	Q JUMP	
75	SLJ	SELECTIVE JUMP	7.2
76	SLS	SELECTIVE STOP	
JUMPS AND S	STOPS (Return)		
22	AJP	A JUMP	
23	QJP	Q JUMP	
75	SLJ	SELECTIVE JUMP	7.2
76	SLS	SELECTIVE STOP	

\*n = Number of ones in multiplier

\*\*s = Number of positions shifted

STORAGE TEST						
36	SSK	STORAGE SKIP		8.8		
37	SSH	STORAGE SHIFT		12.8		
LOGICAL						
40	SST	SELECTIVE SET	]			
42	SCM	SELECTIVE COMPLEMEN'I	}	7,2		
41	SCL	SELECTIVE CLEAR				
43	SSU	SELECTIVE SUBSTITUTE	Ì			
44	LDL	LOAD LOGICAL				
45	ADL	ADD LOGICAL	}	7.4		
46	SBL	SUBTRACT LOGICAL				
47	STL	STORE LOGICAL	-	7.2		
STORAGE SEARCH						
64	EQS	EQUALITY SEARCH				
65	THS	THRESHOLD SEARCH	ζ	4.0 + 3.6r*		
66	MEQ	MASKED EQUALITY	ſ			
67	MTH	MASKED THRESHOLD				
REPLACE			2			
70	RAD	REPLACE ADD	]			
71	RSB	REPLACE SUBTRACT	Ļ	13 2		
72	RAO	REPLACE ADD ONE	ſ	10, 2		
73	RSO	REPLACE SUBTRACT ONE				
TRANSFER						
62	INT	INPUT TRANSFER	l	$4 0 + 4 8 n \times$		
63	OUT	OUTPUT TRANSFER	ſ	1.0 1.01		
			-			

\* r = Number of repeated executions

# DATA TRANSMISSION

- 1) Relative addressing does not take place during LIU, LIL, SIU or SIL instructions. Only direct and indirect addressing are recognized.
- 2) All modes of address modification apply to the remaining data transmission instructions.
- During the execution of data transmission instructions, one storage reference is made. If indirect addressing is designated, at least two storage references are made.

# LDA bm 12 Load A 7.2 µsec Replaces the contents of A with a 48-bit operand contained in storage location M. The initial contents of A are changed during execution; the contents of M remain unchanged.

LAC bm 13Load A Complement7.2 μsecReplaces the contents of A with the complement of a 48-bit operand contained in<br/>storage location M. The initial contents of A are changed during execution; the<br/>contents of M remain unchanged.

# LDQ bm 16 Load Q 7.2 µsec Replaces the contents of Q with a 48-bit operand contained in storage location M. The initial contents of Q are changed during execution; the contents of address M remain unchanged.

LQC bm 17Load Q Complement7.2 μsecReplaces the contents of Q with the complement of a 48-bit operand contained in<br/>storage location M. The initial contents of Q are changed during execution; the<br/>contents of address M remain unchanged.

## **STA bm** 20 Store A

#### 7.2 $\mu sec$

Replaces the contents of the designated storage location, M, with the contents of A. The initial contents of A remain unchanged.

## STQ bm 21 Store Q

### 7.2 $\mu sec$

Replaces the contents of the designated storage location, M, with the contents of Q. The initial contents of Q remain unchanged.



LDA, LAC, LDQ, LQC, STA, and STQ

LIU bm 52 Load Index Upper 7.2 µsec Replaces the contents of the designated index register with the upper address portion of storage location m. If b = 0 this instruction becomes a pass (do nothing) instruction. Initial contents of m remain unchanged.

LIL bm 53 Load Index Lower 7.2 µsec Replaces the contents of the designated index register with the lower address portion of storage location m. If b = 0 this instruction becomes a pass (do nothing) instruction. Initial contents of m remain unchanged.

SIU bm 56 Store Index Upper 7.2 μsec Replaces the upper address portion of storage location m with the contents of the designated index register. The remaining bits of the word in storage remain unchanged. If b = 0, (m<sub>UA</sub>) is cleared. Initial contents of B<sup>b</sup> remain unchanged.

\$ SILbm 58 Store Index Lower 7.2μsec Replaces the lower address portion of storage location m with the contents of the designated index register. The remaining bits of the word in storage remain unchanged. If b = 0, (m<sub>LA</sub>) is cleared. Initial contents of B<sup>b</sup> remain unchanged.



LIU, LIL, SIU, and SIL

# SHIFTING

- 1) All modes of address modification apply to these instructions.
- If the modified shift count, K, is greater than 127<sub>10</sub>, a fault indicator is set. Regardless of the magnitude of count, however, the required number of shifts is executed. (K is reduced by one count for each shift executed and when K = 0, shifting stops.)
- Shifting must be completed before an input/output or interrupt request can be processed. (See chapter three.)

**ARSbk** 01A Right Shift $2.8 + .4s* \mu sec$ Shifts contents of A to the right K places. The sign is extended and the lower bits<br/>are discarded. The largest practical shift count is  $47_{10}$  since the register is now<br/>an extension of the sign bit.

QRSbk 02Q Right Shift $2.8 + .4s \mu sec$ Shifts contents of Q to the right K places. The sign is extended and the lower bits<br/>are discarded. The largest practical shift count is  $47_{10}$  since the register is now<br/>an extension of the sign bit.

LRSbk 03Long Right Shift $2.8 + .4s \, \mu sec$ Shifts contents of AQ to the right K places as one 96-bit register. The A registeris considered as the leftmost 48 bits and the Q register as the rightmost 48 bits.The sign of A is extended. The lower order bits of A replace the higher orderbits of Q and the lower order bits of Q are discarded. The largest practical shiftcount is 95<sub>10</sub> since AQ is now an extension of the sign of A.

**ALSbk** 05A Left Shift $2.8 + .4s \mu sec$ Shifts contents of A to the left K places, left circular. The higher order bits of<br/>A replace the lower order bits. The largest practical shift count  $48_{10}$  returns<br/>the register to its original state.

<sup>\*</sup>s = Number of positions shifted

QLSbk 06Q Left Shift $2.8 + .4s \mu sec$ Shifts contents of Q to the left K places, left circular. The higher order bits of<br/>Q replace the lower order bits. The largest practical shift count  $48_{10}$  returns<br/>the register to its original state.

LLSbk 07 Long Left Shift 2.8 + .4s µsec Shifts contents of AQ to the left K places, left circular, as one 96-bit register. The higher order bits of A replace the lower order bits of Q and the higher order bits of Q replace the lower order bits of A. The largest practical shift count 96<sub>10</sub> returns AQ to its original state.



Shift Instructions

# **ADDRESS MODIFICATION**

- 1) All modes of address modification apply to SAU and SAL instructions.
- 2) Relative addressing cannot be used for ISK or IJP instructions. Only direct or indirect addressing are used.
- 3) During execution of ISK and IJP instructions, no storage reference is made unless indirect addressing is specified which requires at least one reference. For SAU and SAL instructions, one reference is always made. If indirect addressing is designated, at least one additional reference will be needed to complete the instruction.

SAU bm 60Substitute Address Upper7.2 μsecReplaces the upper address portion of M with the lower-order 15 bits of A.Remaining bits of M are not modified and the initial contents of A are unchanged.

SALbm 61Substitute Address Lower7.2 μsecReplaces the lower address portion of M with the lower-order 15 bits of A.<br/>Remaining bits of M are not modified and the initial contents of A are unchanged.



 $\operatorname{SAU}$  and  $\operatorname{SAL}$ 

## **ISK by** 54 Index Skip 7.2 $\mu$ sec Compares (B<sup>b</sup>) with y. If the two quantities are equal, B<sup>b</sup> is cleared and a full exit is performed. If the quantities are unequal, (B<sup>b</sup>) is increased one count in the R register and a half exit is performed. Because the R register is a two's complement subtractive counter, it is possible to count through negative zero and positive zero. (See appendix.) If b = 0 and y $\neq$ 0, a half exit is taken. If b = 0 and y = 0, a full exit is taken. ISK is usually restricted to the upper instruction. If used as a lower instruction it will half exit upon itself until the full exit condition is satisfied; if b = 0 and y $\neq$ 0, the condition will never be satisfied.

## IJPbm

55

Index Jump

#### 7.2 $\mu sec$

Examines (B<sup>b</sup>). If this quantity is not zero, the quantity is reduced one count and a jump is executed to address m. The counting operation is performed in the R register but negative zero is not generated because IJP terminates at positive zero. (See appendix.) The index jump can be used in the upper or lower instruction without reservation; it executes a normal jump upon satisfaction of the jump condition.



ISK and IJP

2 - 16

# **ARI THME TIC**

- 1) All modes of address modification apply to these instructions.
- 2) One storage reference is made for each instruction unless indirect addressing is designated. In this case, at least two references are made.
- 3) If the capacity of the A register  $\pm (2^{47}-1)$  is exceeded during the execution of the instructions an arithmetic overflow fault is produced. When executing the DVI or DVF instructions, if the result exceeds the capacity of the Q register  $\pm (2^{47}-1)$  a divide fault is produced. (Refer to appendix.)

# ADD bm14Add7.2 μsecAdds a 48-bit operand obtained from storage location M to contents of A. A<br/>negative zero may be produced by this instruction if (A) and (M) are initially<br/>negative zero. The contents of storage address M remain unchanged.

**FIXED** 

**SUB bm** 15 Subtract 7.2  $\mu$ sec

Obtains a 48-bit operand from storage location M and subtracts it from the initial contents of A. A negative zero will be produced if the initial contents of A are negative zero and that of storage location M are positive zero. The contents of address M remain unchanged.



ADD and SUB

2 - 17

## **MUIbm** 24 Multiply Integer

25.2 +.8n\*  $\mu$ sec

Forms a 96-bit product from two 48-bit operands. The multiplier must be loaded into A prior to execution of the instruction. The execution address specifies the storage location of the multiplicand. The product is contained in QA as a 96-bit quantity. The operands are considered as integers and therefore the binary point is assumed to be at the lower order (right hand) end of the A register.





\* n = Number of ones in multiplier

# **DVIbm** 25 Divide Integer 65.2 μsec Divides a 96-bit integer dividend by a 48-bit integer divisor. The 96-bit dividend must be formed in the QA register prior to executing the instruction. If a 48-bit dividend is loaded into A, the sign of Q must be set. That is, the sign of the dividend in A must be extended throughout Q. The 48-bit divisor is read

from the storage location specified by the execution address. The quotient is formed in A and the remainder is left in Q at the end of the operation. Dividend and remainder have the same sign.



DVI and DVF

**MUF bm** 26Multiply Fractional $25.2 + .8n* \mu sec$ Forms a 96-bit product from two 48-bit operands. The operands are treated as<br/>fractions with the binary point immediately to the right of the sign bit. The<br/>multiplier must be loaded into A prior to executing the instruction. The multipli-<br/>cand is read into X from the storage location specified by M. The 96-bit product<br/>is contained in AQ.

**DVFbm** 27 Divide Fractional 65.2 µsec Divides a 96-bit quantity by a 48-bit divisor. All operands are treated as fractions with the binary point immediately to the right of the sign bit. The 96-bit dividend must be loaded into AQ prior to executing this instruction. If a 48-bit dividend is loaded into Q, the sign of Q must be extended throughout A. At the end of this operation the quotient is left in A and the remainder in Q. Remainder and dividend have the same sign.

- 1) Refer to appendix for a discussion of floating point format.
- 2) All modes of address modification apply.

#### FLOATING

- One storage reference is made unless indirect addressing is designated. In this case, at least two references are made.
- Floating point range faults (overflow-underflow) occur if the exponent exceeds 2<sup>10</sup>-1 in absolute value. Refer to appendix.

FAD bm 30 Floating Add 18.8 µsec
Forms the sum of two operands packed in floating point format. A floating point operand is read from storage location M and added to the floating point word in A. The result is normalized, rounded, and retained in A at the end of the operation.
Q contains only the residue of the rounding operation at the end of the sequence.

<sup>\*</sup>n = Number of ones in multiplier
**F S B bm** 31Floating Subtract18.8 μsecForms the difference of two 48-bit operands in floating point format. The subtrahend is acquired from storage address M and is subtracted from the minuend in<br/>A. The result is rounded and normalized if necessary and retained in A. The<br/>residue from the rounding operation is left in Q at the end of the sequence.

The basic steps executed in a FSB are the same as those for FAD except the coefficients are subtracted rather than added.



 $\operatorname{FAD}$  and  $\operatorname{FSB}$ 

FMU bm 32Floating Multiply36.0 μsecForms the product of an operand in floating point format with the previous<br/>contents of A also in floating point format. The operand is read from storage<br/>location M. The product is rounded and normalized if necessary and retained<br/>in A. The residue from the rounding operation is left in Q at the end of the<br/>sequence.



FMU

2-22

#### **FDV bm** 33 Floating Divide

#### 56.0 µsec

Forms the quotient of two 48-bit operands in floating point format. The dividend must be loaded into A prior to executing this instruction. The divisor is read from the storage location specified by M. The quotient is rounded and normalized if necessary and retained in A at the end of the operation. The residue from the rounding operation is left in Q at the end of the operation.



FDV

- 1) Address modification does not apply. Rather, the index register is used to preserve the scale factor.
- 2) If b = 0, scaling is executed but the scale factor is lost.
- If b = 7, indirect addressing is used and at least one storage reference is made.
- 4) If (A) i is already scaled or equal to positive or negative zero,  $k \rightarrow B^b$  and scaling is not executed.
- 5) If the execution address is initially equal to 0, B<sup>b</sup> is cleared and no scaling takes place.
- 6) The shift fault indicator is not affected by this instruction.

#### SCAbk 34 Scale A

SCALE

 $2.8 + .4s* \mu sec$ 

Shifts A left circularly until the most significant digit\*\* is to the right of the sign bit or until k = 0. Shift count k is reduced by one for each shift and terminates when k = 0 or the most significant digit is to the right of the sign bit. Upon termination the count (scale factor) is entered in the designated index register.

**SCQ bk** 35 Scale AQ

 $2.8 + .4s \ \mu sec$ 

Shifts AQ left circularly until the most significant digit is to the right of the sign bit. Shift count k is reduced by one for each shift. Operation terminates when k = 0 or the most significant digit is to the right of the sign bit. Upon termination the count (scale factor) is entered in the designated index register.



\*s = Number of positions shifted

\*\*When a negative number is being scaled, "0's" are significant digits.

2-24

## **NO ADDRESS**

- 1) All modes of address modification apply to ENQ, ENA, and INA instructions.
- 2) Relative addressing cannot be used for ENI and INI instructions. Only direct and indirect addressing are used.
- 3) No storage reference is made during these instructions unless indirect addressing is designated. In this case, at least one storage reference is made.

#### **ENQ by** 04 Enter Q

#### $3.0 \ \mu sec$

The 15-bit operand, Y, is entered into Q and its highest order bit is extended in the remaining 33 bits. The largest positive 15-bit operand that can be entered into Q is  $37777_8$  (2<sup>14</sup>-1) and its "0" bit will be duplicated in each of the remaining 33 bits of Q. Negative zero will be formed in Q if:

1)  $(B^{b}) = 77777_{8}$  and  $y = 77777_{8}$  or 2) b = 0 and  $y = 77777_{8}$ .

#### **ENA by** 10 Enter A

#### 3.0 µsec

The 15-bit operand, Y, is entered into the A register and its highest order bit is extended in the remaining 33 bits. The largest positive 15-bit operand that can be entered into A is  $37777_8$  (2<sup>14</sup>-1) and the "0" bit will be duplicated in each of the remaining 33 bits. Negative zero will be formed in A if:

1)  $(B^{b}) = 77777_{8}$  and  $y = 77777_{8}$  or 2) b = 0 and  $y = 77777_{8}$ .

**INA by** 11 Increase A

#### $3.0 \,\mu \text{sec}$

Adds Y to A. The 15-bit operand Y is placed in X and its highest order bit is extended in the remaining 33 bits. The operand in X is added to (A).

ENIby 50 Enter Index 3.0 µsec Replaces (B<sup>b</sup>) with the operand y. If b = 0, this instruction becomes a pass (do nothing) instruction.

INiby 51 Increase Index 3.0 µsec Increases (B<sup>b</sup>) by the operand y. If the b designator is zero, this instruction becomes a pass (do nothing) instruction.



No Address

## JUMPS AND STOPS

#### NORMAL

1) Address modification does not apply to these instructions.

2) One storage reference is made.

A jump instruction causes a current program sequence to terminate and initiates a new sequence at a different location in storage. The Program Address register, P, provides the continuity between program steps and always contains the storage location of the current program step.

When a jump instruction occurs, P is cleared and a new address is entered. In all jump instructions, the execution address, m, specifies the beginning address of the new program sequence. The word at address m is read from storage, placed in  $U^1$  and the upper instruction (first instruction of the new sequence) is executed.

Some of the jump instructions are conditional upon a register containing a specific value or upon the position of an operator's jump or stop key on the console. If the criterion is satisfied, the jump is made to location m. If it is not satisfied, the program proceeds in its regular sequence to the next instruction.

A jump instruction may appear in either position in a program step. If the jump instruction appears in the first (upper) part of the program step and the jump is taken, the second (lower) part of the program step is not executed. If the instruction appears in the lower part, the upper part is executed in the normal manner.

#### AJPjm 22 A Jump

#### 7.2 $\mu sec$

Jumps to m if the conditions of the A register specified by the jump designator, j, exist. If not, the next instruction is executed.

j = 0 Jump if (A) = 0
j = 1 Jump if (A) ≠ 0
j = 2 Jump if (A) = +
j = 3 Jump if (A) = -

When (A) is negative zero the interpretation is:

- j = 0 The jump is executed because, in this case, negative zero is recognized as positive zero.
- j = 1 The jump is not executed.
- j = 2 The jump is not executed because the sign bit is a "1".
- j = 3 The jump is executed because the sign bit is a "1".



AJP, QJP, SLJ, and SLS

QJPjm 23 Q Jump

7.2  $\mu sec$ 

Jumps to m if the condition of the Q register specified by the jump designator, j, exists. If not, the next instruction is executed.

j = 0 Jump if (Q) = 0
j = 1 Jump if (Q) ≠ 0
j = 2 Jump if (Q) = +
j = 3 Jump if (Q) = -

When (Q) is negative zero the AJP interpretation applies.

#### **SLJim** 75 Selective Jump 7.2 μsec Jumps to m if the condition of the jump keys specified by j exists. If not, the next instruction is executed.

- j = 0 Jump unconditionally
- j = 1 Jump if jump key 1 is set
- j = 2 Jump if jump key 2 is set
- j = 3 Jump if jump key 3 is set

#### **SLS jm** 76 Selective Stop

#### 7.2 $\mu sec$

Stops at present step in the sequence if the condition of the stop key specified by j exists. If the stop condition exists, the stop is executed, and the jump is executed unconditionally when the Run/Step key is moved to the RUN or STEP position. If the stop condition is not satisfied, the jump is executed unconditionally.

j = 0 Stop unconditionally
j = 1 Stop if stop key 1 is set
j = 2 Stop if stop key 2 is set
j = 3 Stop if stop key 3 is set

#### **RETURN JUMP**

- 1) Address modification does not apply to these instructions.
- 2) One storage reference is made.

A return jump begins a new program sequence at the lower instruction portion of the program step to which the jump is made. At the same time, the address portion of the upper instruction of that program step is replaced with the address of the next program step in the main program. This instruction allows a return to the main program after completing the subprogram sequence.

#### AJP jm 22 A Jump

7.2  $\mu sec$ 

Executes a return jump to storage location m if the condition of the A register specified by j exists. If not, the next instruction is executed.

- j = 4 Return jump if (A) = 0
- j = 5 Return jump if (A)  $\neq$  0
- j = 6 Return jump if (A) = +
- j = 7 Return jump if (A) = -

Note: If (A) = negative zero, refer to the AJP instruction.



Return Jump

#### QJP jm 23 Q Jump

#### 7.2 $\mu sec$

Executes a return jump to storage location m if the condition of the Q register specified by j exists. If not, the next instruction is executed.

- j = 4 Return jump if (Q) = 0
- j = 5 Return jump if (Q)  $\neq 0$
- j = 6 Return jump if (Q) = +
- j = 7 Return jump if (Q) = -

Note: If (Q) = negative zero, refer to the AJP instruction.

#### **SLJ jm** 75 Selective Jump

#### 7.2 $\mu$ sec

Executes a return jump to storage location m on condition j where condition j represents the setting of the jump keys. If the condition is not satisfied, the next instruction is executed.

- j = 4 Return jump unconditionally
- j = 5 Return jump if jump key 1 is set
- j = 6 Return jump if jump key 2 is set
- j = 7 Return jump if jump key 3 is set

Note: The set position of a jump key is in the up position.

#### **SLS jm** 76 Selective Stop

#### 7.2 $\mu$ sec

Stops on condition j and executes a return jump to storage location m if the Run/ Step key is moved in the RUN or STEP position. If the stop condition is satisfied, the stop is executed and the return jump is executed when the Run/Step key is moved in either position. If the stop condition is not satisfied, the stop is not executed and the return jump is executed unconditionally.

- j = 4 Stop unconditionally
- j = 5 Stop if stop key 1 is set
- j = 6 Stop if stop key 2 is set
- j = 7 Stop if stop key 3 is set

## STORAGE TEST

- 1) All modes of address modification apply to these instructions.
- 2) At least one storage reference is made unless indirect addressing is designated in which case at least two storage references are made.

**SSKbm** 36 Storage Skip 8.8 µsec
Senses the sign bit of the operand in storage location M. If the sign is negative, a full exit is taken. If the sign is positive, a half exit is taken. The contents of the operational registers are left unmodified. SSK is usually restricted to an upper instruction. If used as a lower instruction and the sign of (M) is negative, a full exit will be executed. If the sign is positive, it will half exit upon itself and never execute a full exit.

# SSHbm 37 Storage Shift 12.8 μsec Senses the sign bit of the quantity in storage location M. If the sign bit is negative a full exit is taken, and if the quantity is positive a half exit is taken. In either case the quantity is shifted left circularly one bit before the exit. This instruction is usually restricted to the upper position. If used as a lower instruction and the sign of (m) is positive, the instruction will half exit upon itself until a negative sign bit is found. The contents of the operational registers are left unmodified.



SSH and SSK

## LOGICAL

- 1) All modes of address modification apply to these instructions.
- The LDL, ADL, SBL and STL instructions achieve their result by forming a logical product. A logical product is a bit by bit multiplication of two binary numbers (logical AND condition):

$$0 \ge 0 = 0$$
  
 $0 \ge 1 = 0$   
 $1 \ge 0 = 0$   
 $1 \ge 1 = 1$ 

3) A logical product is used, in many cases, to select specific portions of an operand for entry into another operation. For example, if only a specific portion of an operand in storage is to be added to (A), as the operand passes through X it is subjected to a mask comprised of a predetermined pattern of "0's" and "1's". Forming the logical product of (X) and the mask causes X to retain the original contents only in those stages which have corresponding "1's" in the mask. When only the selected bits remain in X, the instruction proceeds to conclusion.

**SSTbm** 40 Selective Set 7.2 μsec Sets the individual bits of A to "1" where there are corresponding "1's" in the word at storage location M. "0" bits in the word at storage location M do not modify the corresponding bits in A. In a bit by bit comparison of (A) and (M) there are four possible combinations of bits.

1) (A) <sub>i</sub> = 1	2) (A) <sub>i</sub> = 1	3) (A) <sub>i</sub> = 0	4) (A) <sub>i</sub> = 0
(M) <sub>i</sub> = 1	$(M)_{i} = 0$	$(M)_{i} = 1$	$(M)_{i}^{I} = 0$
$(A)_{f} = 1$	(A) <sub>f</sub> = 1	(A) <sub>f</sub> = 1	$(A)_{f} = 0$
$(M)_{f} = 1$	$(\mathbf{M})_{\mathbf{f}} = 0$	$(M)_{f} = 1$	$(\mathbf{M})_{\mathbf{f}} = 0$

```
SCM bm 42Selective Complement7.2 μsecIndividual bits of A are complemented where there are corresponding "1's" in the<br/>word at storage location M. If the corresponding bits at M are "0's", the<br/>associated bits of A remain unchanged.
```

1) (A) <sub>i</sub> = 1	2) (A) <sub>i</sub> = 1	3) (A) <sub>i</sub> = 0	4) (A) <sub>i</sub> = 0
$(M)_{i} = 1$	$(M)_{i} = 0$	$(M)_{i} = 1$	$(M)_{i} = 0$
$(A)_{f} = 0$	(A) <sub>f</sub> = 1	(A) <sub>f</sub> = 1	(A) <sub>f</sub> = 0
$(M)_{f} = 1$	$(\mathbf{M})_{\mathbf{f}} = 0$	$(M)_{f} = 1$	(M) <sub>f</sub> = 0
<b>bm</b> 41	Selective Clear		7.2 µsec

#### SCL bm 41

Clears individual bits of A where there are corresponding "1's" in the word at storage location M. If the corresponding bits at M are "0's", the associated bits of A remain unchanged.

In a bit by bit comparison of (A) and (M) there are four possible combinations of bits.

1) 
$$(A)_{i} = 1$$
  
 $(M)_{i} = 1$   
 $(A)_{f} = 0$   
 $(A)_{f} = 0$   
 $(A)_{f} = 1$   
 $(A)_{f} = 1$   
 $(A)_{f} = 1$   
 $(A)_{f} = 1$   
 $(A)_{f} = 0$   
 $(A)_{f} = 1$   
 $(A)_{f} = 0$   
 $(A)_{f} = 0$   
 $(A)_{f} = 1$   
 $(A)_{f} = 0$   
 $(A)_{f} = 0$ 



SCM, SST, and SCL

SSUbm43Selective Substitute7.4 μsecSubstitutes selected portions of an operand at storage address M into the Aregister where there are corresponding "1's" in the Q register (mask). Theportions of A not masked by "1's" in Q are left unmodified.

LDLbm 44 Load Logical 7.4 µsec Loads A with the logical product of Q and the contents of the designated storage location, M. The operand can be in either Q or M.

ADL bm45Add Logical7.4 μsecAdds to A the logical product of Q and the quantity in location M; the mask may<br/>be in Q or storage. Once the logical product is formed addition follows normal<br/>rules (appendix).

SBLbm 46 Subtract Logical 7.4 μsec
 Subtracts from A the logical product of the Q register and the quantity in storage location M. The mask may be in Q or storage. When the logical product is formed, the subtraction proceeds in the normal manner. (See appendix.)

STLbm 47 Store Logical 7.2 μsec Replaces the bits in storage location M with the logical product of Q and A registers. Neither (A) nor (Q) are modified. The mask may be located in A or Q.



ADL, LKL, SBL, SSU, and STL

2-35

## **STORAGE SEARCH**

- 1) If b = 0 in the following instructions only the word at storage location m will be searched.
- 2) If b = 7, indirect addressing is used to obtain the execution address and b designator.
- 3) If  $(B^b) = 0$ , no search is made.

**EQS bm** 64 Equality Search  $4.0 + 3.6r* \mu sec$ Searches a list of operands to find one that is equal to A. The number of items to be searched is specified by B<sup>b</sup>. These items are in sequential addresses beginning at the location specified by m. The search begins with the last address,  $m + B^b - 1$ . B<sup>b</sup> is reduced one count for each word that is searched until an operand is found that equals A or until B<sup>b</sup> equals zero. If the search is terminated by finding an operand that equals A, a full exit is made. The address of the operand satisfying this condition is given by the sum of m and the final contents of B<sup>b</sup>. If no operand is found that equals A, a half exit is taken. Positive zero and minus zero are recognized as the same quantity. When EQS is used as a lower instruction, the next instruction will always be executed when the search terminates.

#### **T H S bm** 65

Threshold Search

4.0 + 3.6r  $\mu$ sec

Searches a list of operands to find one that is greater than A. The number of items to be searched is specified by  $B^b$ . These items are located in sequential addresses beginning at the location specified by m. The search begins with the last address,  $m + B^{b} - 1$ . The content of the index register is reduced by one for each operand examined. The search continues until an operand is reached that is greater than A or until  $B^b$  is reduced to zero. If the search is terminated by finding an operand greater than the value in A, a full exit is performed. The address of the operand satisfying the condition is given by the sum of m and the final contents of  $B^b$ . If no operand in the list is greater than the value in A, a half exit is performed. If THS is used as a lower instruction, the next instruction will be executed when search terminates. In the comparison made here positive zero is considered as greater than minus zero.

\*r = Number of words searched

**MEQ bm**66Masked Equality Search $4.0 + 3.6r* \mu sec$ Searches a list of operands to find one such that the logical product of (Q) and (M)is equal to (A).This instruction, except for the mask, operates in the samemanner as an equality search.

MTH bm67Masked Threshold Search4.0 + 3.6r µsecSearches a list of operands to find one such that the logical product of (Q) and (M)is greater than (A).Except for the mask, this instruction operates in the samemanner as the threshold search.



Search

<sup>\*</sup>r = Number of words searched

## REPLACE

- 1) All modes of address modification apply to these instructions.
- During the execution of the replace instructions, two storage references are made.
   If indirect addressing is designated, at least three references are made.
- 3) If the capacity of the A register  $\pm (2^{47} 1)$  is exceeded during the execution of the following instructions, an arithmetic overflow fault is produced. (Refer to appendix.)

RAD bm 70 Replace Add 13.2 μsec
Obtains a 48-bit operand from storage location M and adds it to the initial contents of A. The sum is left in A and is also transmitted to location M.
RSB bm 71 Replace Subtract 13.2 μsec
Subtracts (A) from (M) and places the result in both the A register and location M.
RAO bm 72 Replace Add One 13.2 μsec
Replaces the operand in storage location M with its original value plus one. The result is also placed in A.



Replace

#### **RSO bm** 73 Replace Subtract One 13.2 µsec Replaces the operand in storage location M with its original contents minus one. The difference is also left in A; the original contents of A and M are destroyed.

### TRANSFER

- 1) Relative address modification is not used for the following instructions. Only direct and indirect addressing can be used.
- 2) The index registers contain the number of words to be transferred into or out of the computer via channel 7.
- 3) When a transfer is in progress all other computer operations stop except the processing of input/output requests. A transfer is stopped temporarily to process interrupter clock requests.
- 4) If b = 0, one word is transferred to or from address m.



Transfer

#### **INT bm** 62 Input Transfer $4.0 + 4.8r*\mu$ sec Transfers a block of data from an external equipment into storage. The number of words to be transferred is specified by B<sup>b</sup>. These words are stored in sequential addresses beginning at the location specified by the execution address, m. The transfer begins by storing the first input word in the last address in the sequence, m + B<sup>b</sup> -1. As each word is transferred, B<sup>b</sup> is reduced by one until it is equal to zero.

## **OUT bm** 63 Output Transfer $4.0 + 4.8 r \mu sec$ Transfers a block of data from computer storage to an external equipment. The number of words to be transferred is specified by B<sup>b</sup>. The words to be transferred are located in sequential addresses beginning at the location specified by the execution address, m. The transfer begins by obtaining the first output word from the last address, m + B<sup>b</sup> -1. As each word is transferred B<sup>b</sup> is reduced by one until it is equal to zero.

<sup>\*</sup>r - Number of words transferred

#### CHAPTER 3 INPUT/OUTPUT

#### METHODS OF DATA EXCHANGE

The computer communicates with external equipment via a single transfer channel and six buffer channels. The transfer channel which provides for high speed communication is program initiated and controlled. The buffer channels provide for the normal exchange of data and, although program initiated, operate independently of the program.

#### HIGH SPEED TRANSFER CHANNEL

The high speed transfer channel (channel 7) handles both input and output communications between the computer and high speed equipments. The transfer rate is usually dependent on the speed of the external equipment as the computer can perform transfers at a maximum (approximate) rate of one word every 4.8  $\mu$ sec.

As many as five different equipments (optimum conditions) may be connected to the transfer channel. However, only one equipment can use the channel at any given instant and the current transfer operation must be completed before a different equipment can use the channel.

#### BUFFER CHANNELS

The six independent buffer channels are grouped in three pairs:

Input:	Channel 1	Output:	Channel 2
	Channel 3		Channel 4
	Channel 5		Channel 6

All six buffer channels can communicate concurrently with external equipments. This is accomplished by an auxiliary scanner which processes only one channel at a given instant - so that when more than one channel is active each channel is given a turn in rotation to buffer one word of information. The rate of data flow on each buffer channel is determined by the operating speed of the external equipment connected to that channel. A maximum of five equipments may be connected to a buffer channel-pair.

#### INITIATION AND CONTROL OF DATA EXCHANGE

#### TRANSFER

A transfer operation is initiated and controlled by the computer program. An INT or OUT instruction transfers the number of words designated by the contents of an index register. The starting storage location of the transfer is specified by the execution address of the instruction. (See chapter 2 for a discussion of the INT or OUT instructions).

All computer operations, with the exception of previously initiated buffers and processing of interrupt or clock requests, stop while the transferring of words is in progress (refer to page 3-6).

#### BUFFER

A buffer operation transmits a block of data to or from 1604-A core storage. The size and location of the block of data is defined by a buffer control word.

#### Buffer Control Word

Each of the six buffer channels is assigned a buffer control word which controls operations on that channel. The lower address portion of a control word holds the terminal address (one greater than the address of the last word to be buffered). Before a buffer operation is initiated, the terminal address must be entered into the control word by a write instruction (store, substitute, etc). The upper address of a buffer control word holds the current address of a buffer operation. The starting address (address of first word buffered) is automatically entered into the upper address of the control word by the EXF Activate command.<sup>\*</sup> After each word of a buffer operation is transmitted the upper address portion of the control word is automatically increased by one; thus the upper address is the current address (address of next word to be buffered). When the upper and lower addresses of a control word are equal the buffer halts.

The buffer control words are assigned core storage addresses but the address portions are held in 30-bit FF registers called Control registers (CR).

Channel	Control Register	Address of Control Word
1	1	00001
2	2	00002
3	3	00003
4	4	00004
5	5	00005
6	6	00006

\* When reading input words into buffer control word addresses (e.g., Auto Load operation) the upper address of the input word must be the control word address plus one.



BUFFER CONTROL WORD STRUCTURE

When a storage reference is made to one of the buffer control words (00001-6) the address portion is read from or written into the corresponding CR. Because the addresses are contained in the FFs, the control words are destroyed when power is turned off. For programming purposes the buffer control words (addresses 00001-6) are treated as normal core storage addresses.

External Function (EXF) instructions

The EXF instructions initiate a buffer, sense for specified conditions, and select operations and equipment. EXF codes are listed in appendix 6.

There are three kinds of external instructions:

Select	74 0 XXXXX	
Sense	74 7 XXXXX	
Activate	74 j XXXXX	where $j = 1-6$

The composition of an external function instruction is shown below.

DESIGNATOR,

1-6

OPERATION

CODE (74)



STARTING ADDRESS

OF BUFFER

The 74 0 (EXF Select) instructions select the external equipment which is to communicate with the computer. Select instructions also select the mode of operation of external equipment and various internal conditions (allow interrupts etc.). The select instructions do not activate the buffer, but rather establish initial operating conditions within the designated equipment so that information will be properly processed when the buffer is activated.

The 74 7 (EXF Sense) instructions sense the condition of an external equipment or the internal conditions of the computer and will execute a full exit or half exit depending on the presence or absence of the condition.

The location of a 74 7 instruction within an instruction word determines whether a skip or a wait will be performed.

When used in the upper instruction position (Example 1) a 74 7 is a skip instruction.

Example 1:	(00010)	74 7 00010	$75 \ 0 \ 40000$
	(00011)	53 1 00005	$16\ 1\ 00032$

In this example the translation of the upper instruction of a program step 00010 is Exit on Channel 1 active. If channel 1 is active the next instruction to be executed would be the upper instruction of step 00011, i.e., 53 1 00005. If channel 1 were inactive, the lower instruction of step 00010 would be executed.

When used in the lower position (Example 2) a 74 7 is a wait instruction.

Example 2:	(00100)	74 2 00600	74 7 00021
	(00101)	54 2 00005	$75 \ 0 \ 00072$

In this case, the translation of the lower instruction of step 00100 is Exit on Channel 2 inactive. If channel 2 is inactive a full exit is performed to the next pair of instructions, program step 00101. If, however, the channel is active, the instruction half exists and repeats itself until the channel becomes inactive. The sensing of conditions in no way alters the condition.

The 74 j (EXF Activate) instructions activate buffer channel j where j equals 1-6. The execution address of the instruction, m, must designate the starting address of the region in storage. These instructions are the only instructions which can initiate a buffer.

The following steps should be completed prior to initiating a buffer operation.

- 1) Sense for channel inactive.
- 2) Select the external equipment and its mode of operation.
- 3) Sense for equipment ready.
- 4) Store the terminal address in the buffer control word.

Sensing for equipment ready may involve a number of conditions and varies with the different types of external equipments.

A buffer channel is active while data is being buffered. A buffer channel is inactive if the previous input/output operation has been completed.

The buffer must be satisfied (current address = terminating address) to inactivate the channel. This can be accomplished by activating the channel (74 j instruction) at the terminal address. This makes the channel inactive but no additional information is transmitted.

#### Auxiliary Scanner

After being initiated by the main program, data exchange on each buffer channel is controlled by the buffer control section. In order that one buffer channel may not monopolize buffer control, an auxiliary scanner is used to initiate each one word buffer. The auxiliary scanner samples each buffer channel in the order: 1-3-2-6-4-5. When the scanner detects an auxiliary request from one of the buffer channels it stops and initiates a one-word buffer operation. Thus each channel has equal priority.

During a buffer operation the scanner can scan up to four more channels while the present operation is being carried out. However, if another action request is detected, another buffer operation is initiated when the first is finished. This arrangement gives buffer operations priority over program steps in requests for storage time. If no action request is detected on the four channels, a storage reference may be made by a program step and no auxiliary requests may be serviced until storage is released (6.4  $\mu$ sec)



Figure 3-1. 1604-A Flow Chart

3-6

#### INTERRUPT

In each external equipment and in certain computer control circuits conditions may arise which require immediate action by the computer. The signals which notify the computer of these conditions are called interrupts. Interrupts are controlled by the computer program. If an interrupt is desired when a particular condition exists, an external function instruction (74.0) must be used to select the external equipment to interrupt on that condition. Unless such a selection is made, no interrupt is produced when the condition arises. 1604-A interrupts are divided into two classes: (1) interrupts which indicate a fault within the computer (Internal) and (2) interrupts which indicate a fault in external equipment (External).

#### Internal Interrupts

Any one of six arithmetic faults may cause an internal (arithmetic) interrupt. These conditions are controlled collectively by the select instruction: Allow (or Disallow)\* Interrupt on Internal (Arithmetic) Faults (see page 29 of appendix). Internal interrupts have priority over external interrupts. When an internal interrupt occurs the computer jumps to address 00007 and executes the lower instruction at that location.

#### External Interrupts

There are eight external interrupt signals for the 1604-A (one for each of the six buffer channels and two for the high-speed transfer channel). Each of these interrupts may be allowed or disallowed\* by its own select code (see page 29 of appendix). In addition, all external interrupts may be controlled by the instructions:

74 0 04000	Allow Selected External Interrupts (Set Master Interrupt Mask)
74 0 04001	Disallow (Mask) All External Interrupts (Clear Master Interrupt Mask)

When an external interrupt occurs the computer automatically jumps to one of the addresses 00010 - 00017 (see table 3-1) and executes the lower instruction.

<sup>\*</sup> Even though an interrupt is disallowed, it may be sensed with a 74.7 instruction.

Source of Interrupt	Interrupt Address
Internal (Arithmetic), i.e.,	00007
Overflow fault,	
Real Time Clock overflow,	
Divide fault, Shift fault,	
Exponent Overflow fault and	
Exponent Underflow fault.	
Channel 7 (Output Transfer)	00010
Channel 1	00011
Channel 2	00012
Channel 3	00013
Channel 4	00014
Channel 5	00015
Channel 6	00016
Channel 7 (Input Transfer)	00017

TABLE 3-1. INTERRUPT ADDRESSES

#### INTERRUPT SUBROUTINE

An interrupt address (0007-00017) normally contains two jump instructions:

75 0 XXXXX

75 0 YYYYY

When an interrupt occurs, the content of the P register is stored in the upper address portion (XXXXX) of the interrupt address. This provides for return to the main program after the interrupt has been processed. The lower instruction at the interrupt address is a jump to the beginning address (YYYYY) of an interrupt routine. An interrupt routine (table 3-2) senses for possible cause of the interrupt. When the cause of the interrupt is determined, a jump is made to that portion of the routine which corrects the fault (or notifies the operator). The interrupt routine must contain an instruction to remove the interrupt indication.

00007	75 0 XXXXX	75 0 YYYYY	Exit/Entrar	nce
	Address of next	t instruction in r	nain program	
YYYYY	74 7 00131	75 0 ovf00	Sense Over	flow
YYYY1	74 7	75 0		
	74 7	75 0		
YYYYn	74 7	75 0		
ovf00			ſ	
ovf01		<u></u>		
		<	Chan Arithmetic Proc	cess
		74 0 00070 {	Faults Over	rflow
		75 0 00007 {	Jump to Interrupt Address	

#### TABLE 3-2. TYPICAL INTERRUPT SUBROUTINE

After an interrupt has been processed the interrupt routine must provide a jump to its interrupt address (00007-00017). The upper instruction at the interrupt address is a jump back to the main program. At least one instruction of the main program must be executed before another interrupt can occur.

#### REAL TIME CLOCK

Address 00000 in core storage may be selected to provide a continuously operating record of elapsed time. When the real time clock is running, the 48-bit quantity stored at 00000 is advanced by one every 1/60 of a second (accuracy is maintained by the 60-cycle power source). The content of address 00000, which may be sampled at any time, gives an indication of elapsed time from the start of the real-time clock operation. The clock may be started by the EXF instruction 74 0 01000 and stopped by 74 0 02000. Starting the clock does not alter the information already in address 00000.

As shown in figure 3-1, a clock request (generated every 1/60 of a second) has priority over interrupt requests and can break in between any two instructions.

#### INTERNAL SELECT INSTRUCTIONS

74 0	C0000	Clear All Channel C Selections
		Clears all previous selections made on the designated
		channel C except interrupt on channel C inactive.
	000 <b>C</b> 0	Allow Interrupt on Channel C Inactive
		Selects interrupt when channel C becomes inactive. C = 1 - 6
		An interrupt signal is generated whenever the channel becomes
		inactive. More than one interrupt can be selected. The
		interrupt remains selected until cleared.
	000C1	Disallow Interrupt on Channel C Inactive
		Interrupt on channel C inactive selection cleared,
	00100	Allow Interrupt on Internal (Arithmetic) Faults and Clock Overflow
		Selects interrupt on occurrence of any arithmetic fault or clock overflow.
	00101	Disallow Interrupt on Internal (Arithmetic) Faults and Clock over-
		flow
		Prevents arithmetic faults and clock overflow from interrupting program.
	00070	
	00070	Clear Arithmetic Faults and Clock Overflow
		Removes all arithmetic and clock overflow fault indications and
		turns off fault background lights on console.

74 0	01000	INTERNAL SELECT INSTRUCTIONS (Cont'd) Start Real-Time Clock Begins process of adding one to contents of address 00000 each 16.6 ms; address 00000 is not cleared by starting the clock.
	02000	Stop Real-Time Clock Halts process of increasing address 00000. The contents of 00000 remain unchanged.
747	000C0	INTERNAL SENSE INSTRUCTIONS Exit on Channel C Active Full exit if channel C is active
	000C1	Exit on Channel C Inactive Full exit if channel C is inactive
74 7 74 7	001A0 001A1	Exit on Arithmetic Fault A Exit on No Arithmetic Fault A A = 1: Divide 2: Shift 3: Overflow 4: Exponent overflow 5: Exponent underflow
74 7 74 7	0C000 0C001	Exit on Channel C Interrupt Exit on No Channel C Interrupt C = 1-6
74 7 74 7 74 7 74 7	00160 00161 00170 00171	Exit on Channel 7 Output Interrupt Exit on No Channel 7 Output Interrupt Exit on Channel 7 Input Interrupt Exit on No Channel 7 Input Interrupt
74 7 74 7 74 7 74 7 74 7	00200 00201 00300 00301	Exit if Next Main Program Instruction is Upper Exit if Next Main Program Instruction is Lower Exit on Clock Overflow Exit on No Clock Overflow

#### CONSOLE INPUT/OUTPUT EQUIPMENT

Three input/output devices mounted on the console are standard equipment with the 1604-A computer. A Teletype BRPE 11 punch and a CONTROL DATA 350 reader provide for the processing of perforated paper tape. An electric typewriter provides for direct keyboard entry of data and for printed copy output. The console input/output units communicate with the central computer via buffer channels 1 (input) and 2 (output). Other input/output units may share these channels but console input/output units use only these channels.

Data may be transmitted between the computer and the console equipments in either the character or assembly mode. Keyboard input from the typewriter is in the character mode only.

In the character mode one character is buffered at a time. The typewriter uses 6-bit characters. The reader and punch use 8-bit characters. When characters of less than eight bits are desired for the punch and reader the upper bits of the 8-bit character are "0's". A character occupies the lowest bit positions of a 48-bit composite word; the upper bits are "0's".

In the assembly mode the 48-bit word, consisting of eight 6-bit characters, is buffered. During an input buffer in the assembly mode eight successive characters are assembled into a 48-bit word and sent to the computer. The first character occupies the upper 6 bits of the word; the last character occupies the lower order 6 bits.

For an output buffer in the assembly mode a 48-bit word from the computer is disassembled into eight characters, the upper 6 bits first.

#### TYPEWRITER

The typewriter may be used as a keyboard input device (character mode only) or as an output device (either character or assembly mode) for producing printed copy; during output it types approximately 10 characters per second.

All of the typewriter characters and functions are represented by unique combinations of 6 bits. (Codes are in appendix X.) During a keyboard input operation, striking a character key causes the coder to produce the code which is sent to the computer. Space is the only coded typewriter control function which is sent to the computer. For typewriter output, a 6-bit character code sent to the decoder causes the typewriter to print the selected character or perform the designated control function. If the keyboard is selected by code 11140, the interrupt signal occurs for each carriage return (CR).

If an illegal code (unlisted) is sent to the typewriter from the computer, the typewriter hangs up. Striking the carriage return, backspace or shift keys will allow operation to be resumed.

A zero code (all "0" bits) which constitutes a do-nothing code is used to fill out a 48-bit word in the assembly mode.

#### TYPEWRITER CODES

INPU	T SELECT	
74 0	00200	Clear Carriage Return or Tab FF
	11100	Select the Typewriter for Input and No Interrupt on Carriage Return Selects keyboard (character mode only) Interrupt selection cleared, Carriage Return indicator cleared
	11140	Select the Typewriter for Input and Interrupt on Carriage Return Selects keyboard (character mode only) Interrupt selection set, Carriage Return indicator cleared. The next carriage return, which is not output, will set the Carriage Return FF and cause an interrupt. The interrupt selection can be cleared by the external master clear or the 74 0 11100 select only.
OUTF	UT SELECT	
74 0	21100	Select the Typewriter for Output in the Assembly Mode Selects keyboard to print*
	21110	Select the Typewriter for Output in the Character Mode Selects keyboard to print*

<sup>\*</sup> Will not change the Carriage Return FF nor the interrupt selection on channel 1. The code "00" will be ignored; all other illegal codes will cause the typewriter to hang up. It is released by manually performing a function, usually spacing.

#### TYPEWRITER CODES (Cont'd)

SENSE (Input Channel Only)

74 7	11100	Full Exit if Carriage Return Performed on Input
		If a carriage return (which was not the result of an output)
		has been performed since the last input select, a full exit
		is executed; if not, a half exit.
	11101	Full Exit if No Carriage Return Typed on Input
		If the Carriage Return indicator is not set, a full exit is
		executed; if set, a half exit.
	11140	Full Exit Lower Case
		If the typewriter keyboard is in the lower case a full exit is
		performed.
	11141	Full Exit Upper Case
		If the typewriter keyboard is in the upper case a full exit is
		performed.

#### PAPER TAPE READER

The CONTROL DATA 350 Paper Tape Reader enters information into the computer from punched paper tape. The reader, which is always connected to channel 1, operates at a maximum rate of approximately 350 frames per second. A frame, which is across the width of the tape, can store up to 8 bits of information (figure 3-2 shows a seven-level tape). The sprocket or feed holes between levels 3 and 4 generate signals to time the reading of the tape. In the character mode a tape character may be 5, 6, 7, or 8 bits.

In the assembly mode a character is six bits and level seven is used as a control bit (the eighth level is not used in assembly mode). The first of the eight characters in a word is indicated by a hole in the control level (figure 3-2).

Manual controls for the reader are on the punch and reader control panel of the console (figure 4-4). When the Reader Mode switch is raised to ASSEMBLY, the tape is positioned at the first frame in which the seventh level is punched (load point). When the mode switch is depressed to CHARACTER, the tape moves ahead one frame.



Figure 3-2. Seven-Level Punched Paper Tape (Assembly Mode)

Reader tape motion stops on any one of three conditions:

- 1) When buffer operation terminates (assembly or character mode).
- 2) When the load point in assembly mode is reached.
- 3) Absence of a 7th level every 8th character in the assembly mode. \*

The reader End of Tape indicator is set on any of three conditions:

- 1) On a computer master clear.
- 2) Absence of a 7th level every 8th character in the assembly mode. \*
- 3) By a 74 0 11210 instruction. This instruction is used to indicate the end of information in the character mode.

After reading all information on the tape in the assembly mode, tape motion stops and the End of Tape indicator is set because the 7th level control bit is missing. In the character mode, however, motion stops when the buffer operation is satisfied but the End of Tape indicator remains cleared. A 74 0 11210 instruction may be programmed to set the End of Tape indicator after the buffer terminates. The state of the End of Tape indicator, regardless of the mode of operation, may be used to determine if all information on the paper tape has been read.

<sup>\*</sup> Only after at least one seventh level bit has been read.

#### PAPER TAPE READER CODES

SELECT	
74 0 11210	Select Paper Tape Reader and Set End of Tape Indicator Selects Paper Tape Reader Sets End of Tape indicator* Clears interrupt on end of tape
11200	Select the Paper Tape Reader and No Interrupt on End of Tape Selects the reader Interrupt on end of tape cleared
11220	Select the Paper Tape Reader and Interrupt on End of Tape Selects the reader Interrupt on end of tape set. If the End of Tape indicator is set, the interrupt will be immediate.
SENSE	
74 7 11200	Full Exit on End of Tape Indicator Set If the End of Tape indicator is set a full exit is performed; if not, a half exit.
11201	Full Exit on No End of Tape Indicator Set If the End of Tape indicator is not set a full exit is performed; if set, a half exit.
11210	Full Exit on Assembly Mode If the paper tape reader is in the assembly mode a full exit is performed; if not, a half exit.
11211	Full Exit on Character Mode If the paper tape reader is in the character mode a full exit is performed; if not, a half exit.

<sup>\*</sup> This select is usually used in character mode operation only. The End of Tape indicates the logical end of tape, and can be cleared externally only by moving the switch (on the reader control) to the CHARACTER or ASSEMBLY position. Master clear selects the paper tape reader and sets the End of Tape indicator. When the End of Tape indicator has been set the reader is "not ready".
#### PAPER TAPE PUNCH

The punch which prepares paper tape output is always connected to buffer channel 2. The operating rate is 110 characters per second. In character mode, the lower 8 bits of each word sent are punched; the upper bits are ignored. In assembly mode, eight 6-bit characters are punched per word. The upper 6 bits are punched first, with the 7th level supplied automatically every eighth frame.

On the punch, the feedout lever provides for punching out leader. A microswitch is mounted near the roll of paper tape in the punch. When the supply is low, the switch closes and provides an out of tape indication which may be sensed and which lights a console background light.

The paper tape punch is capable of punching 5, 6, 7, or 8 levels.

#### PAPER TAPE PUNCH CODES

SELE	ECT	
74 0	21200	Select the Paper Tape Punch, Assembly Mode Selects the punch, sets mode to assembly Turns the punch motor on
	21210	Select the Paper Tape Punch, Character Mode Selects the punch, sets mode to character Turns the punch motor on
	21240	Turn the Punch Motor Off
SENS	E	
747	21200	Full Exit on Out of Tape If the paper tape punch is out of tape, a full exit is performed; if not, a half exit.
	21201	Full Exit on Not Out of Tape If the paper tape punch is not out of tape, a full exit is performed; if out of tape, a half exit.

#### CHAPTER 4

#### OPERATION

#### DESCRIPTION OF INDICATORS AND CONTROL SWITCHES

All main computer controls and indicators are on the console. Functional significance of console background lights is listed in table 4-1; computer controls are described in table 4-2.

	0.0.0.0.0	The first contract of the second contract of the second se	7 7 7 7 7 7 7 7 0 0
<b>▶ \$ \$ \$ \$ \$ \$ \$ \$</b> \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$			
0 3 7 7 5	7 7 7 0 1	4.0.010.0.01011	67736060
<sup>с с</sup> аларана и народа и народа И стала и народа и на И стала и народа и народа И стала и народа и наро	• • • • • • • • • • • • • • • • • • •	9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	第 ● ● 6 章 ○ ○ ○ ○ ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●
140	0 0 0 0 0	0.0.2.0	7 4 0 0 0 7 1
S. S. D.	**********		

Figure 4-1. Center Panel of Console

The indicators are lamp modules, each of which displays a single octal digit. The lamps, in response to signals from the computer, display the contents of the operational registers in octal form only when the computer is stopped; the display is blank when the computer is running. Each indicator has three push buttons which are numbered in the powers of two, from right to left, starting with zero. Pressing a push button forces that particular stage of the register to the SET state. Each group of three buttons represents an octal digit. To aid in distinguishing between octal digits, the buttons for adjacent octal digits are different shades of blue.

At the right end of each register is a Clear push button (white). This button will clear all the FFs within that register. Set and Clear push buttons should be used only when the computer is stopped; otherwise errors may result. Conditions which stop the computer are listed below. When these conditions exist register contents may be altered by setting or clearing.

- 1) Illegal function codes 00 and 77
- 2) Selective Stops (instruction 76)
- 3) Breakpoint Stop
- 4) Pressing Start/Step switch
- 5) Pressing Clear switch (internal master clear)\*

At some of the modules there are colored background lights which indicate certain internal conditions (figure 4-2, table 4-1). A light is identified by the register in which it is located and its position in the register. For example, AL-4 is fourth from the left in A register left. In general, red lights signify faults and blue lights signify special operating conditions. The background lights may be illuminated when the computer is running as well as when it is stopped.



Figure 4-2. Console Display

<sup>\*</sup> Pressing the Clear switch while the computer is running may destroy the contents of the storage location being referenced

TABLE 4-1.	CONDITIONS	INDICATED	BY	CONSOLE	BACKGROUND	LIGHTS
	COMPLICING	TUDICITI DD	DI	CONSOLL	DICIGUIOUND	LIGHTS

Light	Condition		
AL-1 (blue)	Interrupt Lockout - Computer is in interrupt routine.		
AL-2 (red)* AL-2 (blue)	Internal Interrupt RequestInterrupt request signal is being received from interrupt circuit.		
AL-3 (blue)	Channel 6 Active - Channel 6 is in use for output buffer.		
AL-4 (blue)	Channel 5 Active - Channel 5 is in use for input buffer.		
AL-5 (blue)	Channel 4 Active - Channel 4 is in use for output buffer.		
AL-6 (blue)	Channel 3 Active - Channel 3 is in use for input buffer.		
AL-7 (blue)	Channel 2 Active - Channel 2 is in use for output buffer.		
AL-8 (blue)	Channel 1 Active - Channel 1 is in use for input buffer.		
AR-1 (blue)	Reader Ready - (1) Paper tape is at load point, ready for an input buffer; or (2) input buffer paper tape is in progress.		
AR-2 (red)	Punch Out of Tape - Punch tape reel is nearly empty.		
AR-3 (red)	Odd Storage Fault - Fault in sequence chain of odd storage unit; storage unit is inoperative until master cleared.		
AR-4 (red)	Even Storage Fault - Fault in sequence chain of even storage unit; storage unit is inoperative until master cleared.		
AR-5 (red)	Divide Fault - Improper divide instruction executed.		
AR-6 (red)	Shift Fault - Shift count greater than 127 (decimal).		
AR-7 (red)	Overflow Fault - Required sum or difference exceeds capacity of A register.		
AR-8 (red)	Exponent Fault - In a floating-point instruction, exponent of result is $2^{10}$ or greater.		
QR-7 (green)	Storage Not Busy - Indicates when storage is not in use.		
QR-8 (blue)	Deep End - Computer fails to complete operation in step mode.		
PA-1 (red)	$\overline{1604/1604}$ -A Switch in 1604 position.		
PA-5 (blue)	Lower Instruction - Lower instruction is indicated.		
FUNCTION CODE (blue) (3 lights)	<u>Sweep</u> - Computer is in sweep mode (Mode switch is down).		

<sup>\*</sup> On both internal and external interrupt requests the light is yellow.

# MAIN COMPUTER CONTROLS

Control	Function		
Power ON - green push button	Applies a-c and d-c power to computer by energizing contactor in primary power lines of motor generator.		
OFF - red	Removes d-c and a-c power from computer by de-energizing contactor in primary power lines of motor generator.		
Storage MARGIN Test	Varies the bias applied to storage sense amplifiers. Used for maintenance purposes only; should be in neutral position at all other times.		
Lever switch MODE locks in up, down and	Up: an instruction is executed repeatedly in either the step or start mode.		
neutral posi- tions.	Down: contents of consecutive storage locations may be manually examined by pressing Step. Consecutive half-words are displayed in function code and execution address registers but are not executed.		
Breakpoint Five 8-position switches can be set to octal address 00000 through 77777.	Provides for selection of any storage address as a breakpoint address. Computer stops when program address and breakpoint address arc equal, just prior to performing the upper instruc- tion at the breakpoint address.		
Selective Jumps 1, 2, 3 Three lever switches lock in upper positions, momentary in down positions.	Provide manual conditions for instruction 75, normal jumps, b = 1, 2 or 3, return jumps, b = 5, 6 or 7.		
Selective Stops 1, 2, 3 Three lever switches lock in upper position, momentary in down positions.	Provide manual conditions for stopping the computer on instruction 76, b = 1, 2, 3, 5, 6 or 7.		
Clear Lever switch, momentary in up and down positions.	Up: master clears external equipment, causing most of the registers and control FFs of the external equipment to be cleared and the paper tape reader to be selected. Down: master clears the computer, clears all operational registers and most control FFs. May destroy content of one storage location if pressed while computer is operating.		

### TABLE 4-2. MAIN COMPUTER CONTROLS

Control	Function		
Start/Step Lever switch, momentary	START (up) selects high-speed mode in which a program of instructions and auxiliary operations proceeds until completed or stopped.		
	STEP (down) selects step mode. Each time switch is pressed a single instruction is executed and computer stops (all buffer requests are completed before operation stops). Step selection overrides any previous selection of start.		
Volume Control Black knob under console desk	Controls volume of signal from console loud- speaker.		
*The Set push buttons, numbered in the powers of 2, beginning with zero. Each group of three is an octal digit.	Allow for manual entry of a quantity into a given register. Forces that particular stage of register to the set state.		
*The Clear push buttons	Clear all FFs within that register.		
1604/1604-A Switch Mounted near console speaker	Enables 1604-A to run 1604 programs.		

TABLE 4-2. MAIN COMPUTER CONTROLS (Cont'd)



Figure 4-3. Manual Controls

<sup>\*</sup> Should be used only when the computer is stopped.

# READER AND PUNCH CONTROLS

Switch	Function
Punch Motor	Turns punch motor on or off. (Motor may also be turned on under program control.)
Select/Tape Feed	Select enables use of the punch.
	Tape Feed causes leader to be punched,
Reader Motor	Turns reader motor on or off. (Motor cannot be turned on by any other means.)
Character/Assembly	In character mode each character is sent to computer separately.
	In assembly mode eight consecutive characters are assembled into a word to be sent to computer.

# TABLE 4-3. READER AND PUNCH CONTROLS



Figure 4-4. Reader, Punch, and Auto Load Controls

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#### AUTO LOAD CONTROL

The Auto Load button initiates a bootstrap routine to read into memory (via channel 3) the first record from magnetic tape #1, on 1615 or 1607 equipment #2.

Pressing the Auto Load button selects the tape and loads the bootstrap routine into memory locations 00000 and 00001, and puts an address of 32000 (arbitrary and > 00004) in the lower address of 00003.

The program appears as:

(00000)	$74 \ 0 \ 32005$	Rewind the tape
	74 7 32000	Wait for ready
(00001)	$74 \ 3 \ 00002$	Activate, FWA = $00002$
	74 7 32000	Wait for ready
(00002)	XX X XXXXX	Will be the first
	XX X XXXXX	word read from tape
(00003)	74 3 00002	
	74 7 32000	

The routine will be executed unless Breakpoint is set to 00000 or 00001. The first word read from tape will be read into location 00002 and be executed as soon as the tape is ready again. The second word will be read into the control word address (00003). The lower address of the second word sets the buffer terminating address; the upper address must be 00004 (control word address plus one).

#### **OPERATION**

The 1604-A is a stored-program computer. To load a program in the computer a load program (basic service library) is needed. The load program is entered manually. A paper tape reader, a paper tape punch, an electric typewriter, and a set of magnetic tapes are some of the important external devices used for communicating with the 1604-A. The programmer, before operating any of these devices, should make himself familiar with instructions for these devices and they should be followed in the order recommended.

#### LOAD PROGRAM ENTERING

A load program to be entered in storage is usually on bi-octal paper tape. The following procedure enters the load program:

- 1) Turn on power.
- 2) Master clear, both internal and external.
- 3) Press Start/Step switch once.
- 4) Clear function code and set to 200.
- 5) Clear execution address and set to 00001.
- 6) Set terminal address of buffer in lowest five octal digits of A register right.
- 7) Press Start/Step switch once.
- 8) Load tape into reader.
- 9) Turn on reader motor (wait 10 seconds).
- 10) Raise reader Mode switch to ASSEMBLY position.
- 11) Clear function code and set to 741.
- 12) Clear execution address and set to initial address of buffer.
- 13) Press Start/Step switch once. Wait until tape loads (console lights come on).
- 14) Press Clear switch.
- 15) Perform steps 2 through 8 of operation with pre-stored program.

## STARTING OPERATION WITH PRE-STORED LOAD PROGRAM

When a general loading program which provides for loading other programs is held in storage, the starting procedure is as follows:

- 1) Turn on power (Power On, figure 4-3).
- 2) Make required manual selections:

Selective Jumps Selective Stops Breakpoint

- 3) Set in operation the external device or devices selected to communicate with the computer. (Follow the instructions for the devices given in this chapter.)
- 4) Master clear, both internal and external (press clear, then raise it).
- 5) Set Program Address register to address of first instruction of program.
- 6) Begin computer operation (raise Start switch).
- 7) To shut down the equipment after the operation has stopped, follow the instructions as given for each external device.
- 8) Press Power Off button, which disconnects power from all equipments.

#### READER

The reader is a CONTROL DATA 350 paper tape reader (figure 4-5). It can read either a 5-, a 7-, or an 8-level tape. For a bi-octal tape with the 7th level control holes, assembly mode is selected; for a flex or other code, character mode is selected.

- 1) Check if tape basket is at the proper place. Do not allow the tape to fall on the floor.
- 2) Turn tape release lever clockwise to raise tape guide plate.
- 3) Select the desired tape level by means of the tape level switch.



Figure 4-5. Paper Tape Reader

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- 4) Holding the tape guide down, slide it so that the marker rests above the proper etched mark on the tape deck surface. The outer position is for 8-level tape, the center for 7-level, and the inner for 5-level.
- 5) Insert tape as shown in figure 4-5. Make sure that the tape is properly aligned.
- 6) Turn Tape Release lever counterclockwise to lower the tape guide.
- 7) Select the desired mode of operation by the Mode switch (figure 4-4) on the control panel.
- 8) Turn on Reader switch on control panel (figure 4-4).
- 9) After the reader has read the tape, remove paper tape from reader and basket; rewind tapes.
- 10) Turn off reader motor.

#### PUNCH

The paper tape punch (figure 4-6) is mounted on a hinged rack at the rear of the right wing of the console. Punch tape feeds out of a slot in the compartment door; the chad box is just inside the door.

- 1) To ensure proper performance of the punch, always keep the chad box clean.
- 2) Set Punch switch to SELECT (control panel) and check for sufficient paper in reel.



Figure 4-6. Paper Tape Punch

- 3) If you have used the punch, generate a foot of leader by pressing tape feed; remove feed; remove tape and wind it up.
- 4) Perform the following steps to replace a tape roll at punch.
  - a) Remove the tape reel from cradle at side of punch.
  - b) Unscrew tape hold-down assembly, remove old roll, and place new roll on reel. Replace hold-down assembly and mount reel in cradle.
  - c) Thread tape as shown in figure 4-6. Bring tape around lower roller and into guides leading to punch block.
  - d) Turn on punch motor and advance tape through the punch block by pressing the tape feed-out lever (top of punch block).
  - e) Bring leader out through slot in door. Swing punch back into compartment.

### TYPEWRITER

The typewriter has all of the characters and functions of a standard electric machine. As a keyboard entry device the typewriter is used only in the character mode. After the program selects keyboard and initiates an input buffer, each striking of a key causes a 6-bit coded character to be entered into the lower six positions of a computer word. The remaining bits of the word are all "0". If the keyboard is selected along with an interrupt feature, each carriage return or tab sends an interrupt signal to the computer. This notifies the program of the entry of data from the keyboard.

When the typewriter is used as an output device certain conditions cause it to hang up until the space bar is struck: receipt of an illegal typewriter code, a code to shift up when the carriage is already up, or a code to shift down when the carriage is already down.

If the typewriter is to be used:

- a) Place paper in it.
- b) Set the switch beneath the righthand corner to ON.

#### MAGNETIC TAPE UNITS

The tape units which can be used with 1604-A are CONTROL DATA 606 and CONTROL DATA 1607. To use the 606, the CONTROL DATA 1615 Adapter is needed. The codes for the adapter and the tape unit are given in appendix VI.

606 TAPE UNIT

# Controls and Indicators

The manual controls and indicators for operating each tape unit are mounted on a panel located below the front door of the unit (figure 4-7). The functions of the controls are described in table 4-4.



Figure 4-7. Operator Control Panel

TABLE 4-4.	606	CONTROLS	AND	<b>INDICATORS</b>

NAME		FUNCTION
POWER OFF	*S	Removes power from all components and power supplies.
	** <b>I</b>	Power is available to components and power supplies.
FWD	S	Moves tape forward at 150 ips. Motion stops when end of tape marker is sensed.
	I	Tape is moving forward at 150 ips.
CLEAR	S	Master clears all previous settings and conditions. Stops tape motion immediately. New Manual selections are necessary to reselect tape unit and/or operation required.
	I	606 is cleared

\*Switch

\*\*Indicator

TABLE 4-4.	606 CONTROLS AND INDICATORS	(CONT'D)
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NAME		FUNCTION
$\operatorname{REV}$	*S	Rewinds tape at 225 ips. Motion stops when load point marker is sensed.
	**I	Tape is moving in reverse direction at 150 or 225 ips.
WRITE	I	Write operation is in progress.
UNLOAD	S	Moves tape at 225 ips to unload position (all tape on supply reel). Tape load procedure must be performed to resume operation.
	I	Tape is in unload status.
LOAD POINT	S	Moves tape forward at 150 ips to load point marker. Motion stops when marker is sensed.
	I	Tape is at load point marker.
READY	S	Places 606 under external control.
	I	Unit is under external control.
DENSITY	S	Changes density mode selection.
	I (Hi) I (Low)	High density m <b>o</b> de selected. Low density m <b>o</b> de selected.
READ	I	Read operation is in progress (not on when reading for horizontal checking during write operation).
UNIT SELECTION	S	10-position switch; 0-7 provide input desig- nation while two standby positions disconnect unit from external control.
	I (White) I (Red)	Show selected number. Fault Condition (power failure, tape not in columns, etc.).
OVERHEAD LIGHTS	I	File protection ring is on reel (unit can write) and tape unit is not in the unload position.

\*Switch \*\*Indicator

# Tape Load Procedure

- 1) Make sure that tape unit is properly energized.
- 2) Slide front glass door down to lowest position (figure 4-8).
- 3) Check that supply reel has been file protected as necessary.
- 4) Mount reel on supply reel hub and tighten hub knob. For proper alignment, push reel firmly against hub stop before tightening knob.
- 5) Make sure that tape load arms are in up position.
- 6) Pull sufficient tape from supply reel to reach take-up reel. Thread tape on the outside of the supply tape load arm, over the head assembly, around the outside of the take-up load arm and over the top of the take-up reel hub two or three times.
- 7) Slide tape under head assembly.
- 8) Snap tape load arms down.



Figure 4-8. 606 Tape Load and Unload Mechanics

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- 9) Set Unit Selection switch to one of ten positions (0-7 or standby) to assign a logical program selection number.
- 10) Press Clear switch.
- 11) Press Load Point switch. Tape will drop in columns, move forward, and stop on load point marker. The Load Point light will turn on. (If the light does not turn on, notify maintenance.) If tape continues moving forward for more than 3 or 4 seconds, it indicates either no load point marker was placed on the tape or the operator manually wound the marker onto the take-up reel during step 5.
- 12) If the unit is to be controlled, press the Ready switch. If it is to be manually operated and the Ready switch has been pushed, press the Clear switch.
- 13) Raise the front glass door completely.

If the supply reel contains a file protection ring, the overhead lights should be on, indicating that a write operation may be performed. If the lights are not on, notify maintenance.

#### Tape Unload Procedure

- 1) Press Clear switch.
- 2) Press Unload switch. All tape will automatically be drawn from the take-up reel and wound on the supply reel. The Unload indicator will light.
- 3) Slide down front door.
- 4) Loosen supply reel hub knob and remove supply reel.
- 5) Check if reel needs to be file protected and if it is labeled adequately prior to storage.

# Special Instructions

In order to simulate an unload condition without removing all tape from the take-up reel, simultaneously press the Clear and Unload switches. The unload condition will be simulated but tape will not move. In order to place the unit in operational status, remove all tape from the vacuum columns by revolving the take-up reel clockwise and the supply reel counterclockwise. Snap the tape load arms down and press the Load Point switch. The tape will move forward and stop on the nearest load point marker. The Load Point indicator will turn on.

If all tape is unwound from the supply reel:

- 1) Snap tape load arms up, if necessary.
- 2) Guide tape around the tape load arms, over the head assembly, and wrap approximately ten turns around the supply reel.
- 3) Slide tape under head assembly.
- 4) Press the Load Point switch.
- 5) As soon as the Forward light turns on, press the Clear switch and then the Reverse switch. Tape will rewind on the nearest load point marker.

The following information is applicable when a number of load point or end of tape markers are used on a single tape.

To move forward from a reflective marker and stop at nearest end of tape marker, press the Forward switch.

To move forward off a reflective marker and stop at nearest load point or end of tape marker, press the Forward and then the Load Point switches. Load Point indicator will light if motion stops at load point marker.

To reverse from a reflection marker and stop at nearest load point marker, press the Unload, Clear, and Reverse switches, in that order.

Tape motion may be stopped at any time by pressing the Clear switch. An unload operation may be performed by pressing the Unload switch.

# 1607 TAPE UNIT

#### Controls and Indicators

Each tape unit is provided with push buttons for manual operation. These controls are mounted on a panel above the front door (figure 4-9, table 4-5).

# Tape Load Procedure

- 1) Open door to handler.
- 2) Check that file reel to be loaded has been file protected as necessary.
- 3) Mount the reel on the file reel hub and tighten the hub knob. To insure proper reel alignment push the reel firmly against the reel hub stop before tightening the knob. If the file protection ring has been removed from the reel, check that the Write Lockout lamp turns on when the reel is loaded. If the lamp does not turn on call maintenance.

# TABLE 4-5. 1607 CONTROLS AND INDICATORS

Control		Function		
REWIND	*S	Controls manual rewind to load point.		
	**I	Indicates rewind in progress.		
CHANGE TAPE	S	Drops any manual selection and places tape unit in automatic or program control mode.		
	I	When lighted, indicates tape rewound under program control and interlocked at load point. The interlock prevents operation of the tape unit until the Stop Manual switch is operated.		
WRITE LOCKOUT	S	Drops power from unit and removes program designation.		
	I	When lighted, indicates that tape unit is loaded with a reel which does not contain a file protection ring. The tape cannot be written as long as the light is on, but may be read.		
1, 2, 3 or 4	S	Designates program selection of unit and applies power to unit. Each new unit designation cancels an existing designation.		
-	I	Indicates unit selection and power-on condition.		
REVERSE	S	Initiates reverse tape motion during manual operation.		
	I	Indicates reverse tape motion.		
STOP MANUAL	S	Drops unit from program control or drops forward or reverse selection and places unit in manual mode.		
	I	Indicates manual mode and ready.		
FORWARD	S	Initiates forward tape motion during manual mode.		
	I	Indicates forward tape motion.		

\*switch \*\*indicator



Figure 4-9. 1607 Tape Unit

- 4) Press upper Reel Brake pushbutton to release mechanical brake and check that pulling tape from rcel causes it to rotate clockwise. Pull sufficient tape from reel to reach end of permanent machine leader held by leader clamp.
- 5) Connect file tab to permanent machine leader.
- 6) Take up slack by turning file reel while pressing upper Reel Brake push button.
- 7) Lift leader clamp and close door.
- 8) Press one of the unit selection switches (1, 2, 3, 4) to apply power to the unit and assign the unit a logical program selection number. Wait two minutes. The Stop Manual lamp should turn on; if not, call maintenance.
- 9) Press Stop Manual.
- Press Rewind button. Unit is ready when Rewind lamp turns off. If Stop Manual lamp remains on, unit is not ready; call maintenance.

#### Tape Unload Procedure

- 1) Press Stop Manual button to select manual mode.
- 2) Press Reverse button to move tape backwards to change tape position.
- 3) Open front door of tape unit.
- 4) To secure tape, lower leader clamp.
- 5) Press the upper Reel Brake button to release the mechanical brake and pull tape from file reel to provide slack.
- 6) Unfasten mechanical splice which connects the file tab to the permanent machine leader.
- 7) Loosen file reel hub knob and remove the file reel.
- 8) Check if reel needs to be file protected and also if it is labelled adequately prior to storage.

#### FILE PROTECTION RING

The back of the file reel has a slot near the hub which accepts a plastic file protection ring (figure 4-10). Writing on a tape is possible only when the reel contains a file protection ring. The ring should be removed from the reel after writing is completed to avoid accidental rewriting. Tape may be read either with the ring in place or without it. On the 606 the overhead lights go on immediately after the tape load procedure is



Figure 4-10. File Protection Ring

executed if the file protection ring is in place. The Write Lockout light on the 1607 is off if the file protection ring is in place.

## EMERGENCY PROCEDURES

A fault indication, or a warning signal from the buzzer, may call for special procedures on the part of the operator.

Condition	Procedure
Punch out of tape	Load new roll of tape in punch at end of current operation.
Odd Storage Fault	Master clear. Restart program.
Even Storage Fault	Master clear. Restart program.
Deep End	If all I/O operation has ceased, master clear and restart program. If condition persists, notify maintenance.
Sweep	Place Mode switch in neutral position.
Buzzer Signal	Notify maintenance engineer immediately.

TABLE 4-6.	EMERGENCY	PROCEDURE
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Faults for which the program provides corrective action are: Divide, Shift, Overflow and Exponent Faults. (Refer to appendix.)

# GLOSSARY

A specific storage location; contrast with relative address. ABSOLUTE ADDRESS ACCESS TIME The time needed to perform a storage reference, either read or write. A register with provisions for the addition of another quantity to ACCUMULATOR its content. It is also the name of the A register. A 15-bit quantity which identifies a particular storage location. ADDRESS ALPHABETIC A system of abbreviation used in preparing information for input CODING into a computer, e.g., Q Right Shift would be QRS. A logical function in Boolean algebra that is satisfied (has the AND FUNCTION value "1") only when all of its terms are "1's". For any other combination of values it is not satisfied and its value is "0". Principal arithmetic register; operates as a 48-bit subtractive A REGISTER accumulator (modulus  $2^{48}$ -1). A quantity which defines some system of representing numbers by BASE positional notation; radix. Binary digit, either "1" or "0". BIT BLOCK A specified area of storage to which or from which data is to be transmitted. BOOTSTRAP The coded instructions at the beginning of an input tape, together with the manually entered instructions. BORROW In a subtractive counter or accumulator, a signal indicating that in stage n, a "1" was subtracted from a "0". The signal is sent to stage n+1 which it complements. BRANCH A conditional jump. BREAKPOINT The address at which a program may be stopped by the Breakpoint switches on the computer console. B<sup>1</sup>-B<sup>6</sup> REGISTERS Index registers used primarily for modification of execution address.

BUFFER	A device in which data is stored temporarily in the course of trans- mission from one point to another. To store data temporarily. The operation in which either a word from storage is sent to an external equipment via an output channel (output buffer), or a word is sent from an external equipment to storage via an input channel (input buffer).
BUFFER CON- TROL WORD	Each of the six buffer channels is assigned a buffer control word which controls buffer operations on that channel. The lower address holds the terminal address plus one of the buffer; the upper address holds the current or starting address of the buffer.
CAPACITY	The upper and lower limits of the numbers which may be processed in a register or the quantity of information which may be stored in a storage unit. If the capacity of a register is exceeded, an overflow is generated
CARRY	In an additive counter or accumulator, a signal indicating that in stage n, a "1" was added to a "1". The signal is sent to stage n+1, which it complements.
CHANNEL	Transmission path connecting the computer to an external equipment.
CHARACTER	<ul> <li>Two types of information handled by the computer:</li> <li>1) A group of 6 bits which represents a digit, letter or symbol. In assembly mode, eight 6-bit characters make up a computer word.</li> <li>2) A group of 5 to 8 bits which represents an item of information. In the character mode, this item is one 5 to 8-bit character with "0's" in the remaining (upper) bits of a 48-bit word.</li> </ul>
CLEAR	A command that destroys the quantity in a register by placing every stage of the register in the "0" state.
CLOCK OVERFLOW	A clock overflow occurs whenever the capacity of the A register is exceeded during an advance clock instruction. This condition is indicated by a visible display, can be sensed by an EXF code, or may be selected to cause an interrupt.
CLOCK PHASE	One of two outputs from the master clock, "even" or "odd".
COMMAND	A signal that performs a unit operation, such as transmitting the content of one register to another, shifting a register one place to the left or setting a FF.

- $\begin{array}{c} \mbox{COMMON CONTROL} & \mbox{A 30-bit register used to hold the initial and terminal addresses} \\ \mbox{REGISTER} & (\mbox{CR}_U \mbox{ and CR}_L) \mbox{ of the current buffer operation while the comparator tor samples them.} & \mbox{The CCR also has counting logic which is used} \\ \mbox{ to advance the address from CR}_{II}. \end{array}$
- COMPILER A routine which automatically produces a specific program for a particular problem. The routine determines the meaning for information expressed in a psuedo-code, selects or generates the required subroutine, transforms the subroutine into specific coding, assigns storage registers, and enters the information as an element of the problem program.
- COMPLEMENT Noun: see One's Complement or Two's Complement. Verb: a command which produces the one's complement of a given quantity.

CONTENT The quantity or word held in a register or storage location.

CONTROL 30-bit registers used to hold the address portions of the buffer control words. The upper address portion  $(CR_U)$  is advanced each time a word is buffered and is the current address for a buffer operation.

- CORE A ferromagnetic toroid used as the bistable device for storing a bit in a memory plane.
- COUNTER A register with provisions for increasing or decreasing its content by 1.

EVEN STORAGE The storage unit which contains the 16,384 even addresses.

EXECUTION The lower 15 bits of a 24-bit instruction. Most often used to specify the storage address of an operand. Sometimes used as the operand.

EXIT Initiation of a second control sequence by the first, occurring when the first is near completion; the circuit involved in exiting.

- EXTERNAL1) External Function Select (74.0) selects an external equipmentFUNCTIONor establishes an internal or external condition.
  - 2) External Function Sense (74.7) sends a code to an external equipment or internal circuit to sense its condition.

- FAULT Operational difficulty which stops operation or sets an indicator.
   FIXED POINT A notation or system of arithmetic in which all numerical quantities are expressed by a predetermined number of digits with the binary point implicitly located at some predetermined position; contrasted with floating point.
- FLIP-FLOP (FF) A bistable storage device. A "1" input to the set side puts the FF in the "1" state; a "1" input to the clear side puts the FF in the "0" state. The FF remains in a state indicative of its last "1" input. A stage of a register consists of a FF.
- FLOATING POINT A means of expressing a number X by a pair of numbers, Y and Z, such that  $X = Yn^{Z}$ . Z is an integer, called the exponent or characteristic; n is a base, usually 2 or 10; and Y is called the fraction or mantissa.
- FUNCTION CODE The upper 6 bits of a 24-bit instruction which specify the instruction to be executed.
- INDEX CODE A 3-bit quantity, bits 15, 16, and 17 of an instruction; usually specifies an index register whose contents are added to the execution address; sometimes specifies the conditions for executing the instruction.
- INSTRUCTION A 24-bit quantity consisting of a function code, execution address, and index designator.
- INTERRUPT<br/>MASKING<br/>REGISTER (IMR)Consists of eight FFs which are set or cleared by EXF select<br/>codes to apply a mask to the interrupt lines. If one of these FFs<br/>is set it disallows the corresponding external interrupt.
- INTERRUPT<br/>REQUESTA signal received from an external equipment or internal logic<br/>that may cause a special sequence of instructions to be executed.

INVERTER A circuit which provides as an output a signal that is opposite to its input. An inverter output is "1" only if all the separate OR inputs are "0".

JUMP An instruction which alters the normal sequence control of the computer and, conditionally or unconditionally, specifies the location of the next instruction.

LOAD	To place a quantity from storage in a register.
LOCATION	A storage position holding one computer word, usually designated by a specific address.
LOGICAL PRODUCT	In Boolean algebra, the AND function of several terms. The pro- duct is "1" only when all the terms are "1"; otherwise it is "0". Sometimes referred to as the result of "bit-by-bit" multiplication.
LOGICAL SUM	In Boolean algebra, the OR function of several terms. The sum is "1" when any or all of the terms are "1"; it is "0" only when all are "0".
LOOP	Repetition of a group of instructions in a routine.
LOWER ADDRESS	The execution address portion of a lower instruction; bits 0 through 14 of a 48-bit register or storage location.
LOWER INSTRUCTION	See Program Word.
MASK	In some instructions, one quantity may determine what part of the other quantity is to be considered. If the first quantity, the mask, contains a "1", the corresponding bit of the second quantity is considered.
MASKED INTERRUPT REGISTER (MIR)	A rank of eight FFs through which external interrupt signals enter the 1604-A. The inputs to MIR can be masked (disallowed) by the IMR.
MASTER CLOCK	The source of standard signals required for sequencing computer operation. The clock determines the basic frequency of the computer.
MASTER CLEAR (MC)	A general command produced by placing the Clear switch up (external MC) or down (computer MC) which clears most of the crucial registers and control FFs (some FFs are set by MC).
MASTER INTER- RUPT MASK (MIM)	A FF for masking all external interrupts.
MNEMONIC CODE	A three-letter code which represents the function or purpose of an instruction. Also called Alphabetic Code.

- MODULUS An integer which describes certain arithmetic characteristics of registers, especially counters and accumulators, within a digital computer. The modulus of a device is defined by  $r^n$  for an openended device and  $r^n-1$  for a closed (end-around) device, where r is the base of the number system used and n is the number of digit positions (stages) in the device. Generally, devices with modulus  $r^n$  use two's complement arithmetic; devices with modulus  $r^n-1$ use one's complement.
- NORMALIZE To adjust the exponent and mantissa of a floating-point result so that the mantissa lies in the prescribed standard (normal) range.
- NORMAL JUMP An instruction that jumps from one sequence of instructions to a second, and makes no preparation for returning to the first sequence.
- NUMERIC CODING A system of abbreviation in which all information is reduced to numerical quantities.

ODD STORAGE The storage unit which contains the 16,384 odd addresses.

- ONE'S COMPLEMENT With reference to a binary number, that number which results from subtracting each bit of the given number from "1". The one's complement of a number is formed by complementing each bit of it individually, that is, changing a "1" to "0" and a "0" to a "1". A negative number is expressed by the one's complement of the corresponding positive number.
- ON-LINE A type of system application in which the input data to the system OPERATION is fed directly from the external equipment to the computer.

OPERAND Usually refers to the quantity specified by the execution address. This quantity is operated upon in the execution of the instruction.

OPERATIONAL Registers which are displayed on the operator's console  $(B^1-B^6, A, Q, P, U^1)$ .

OPERATION<br/>CODEThe upper 6 bits of a 24-bit instruction which identify the instruc-<br/>tion. After the code is translated, it conditions the computer for<br/>execution of the specified instruction. This code, which is<br/>expressed by two octal digits, is designated by the letter f.

- $O^1 O^4$  REGISTERS Output registers  $O^{1,2,3}$  are used for output buffer operations;  $O^4$  handles all high-speed output transfer operations.
- OR FUNCTION A logical function in Boolean algebra that is satisfied (has the value "1") when any of its terms are "1". It is not satisfied when all terms are "0". Often called the 'inclusive' OR function.
- OVERFLOW The capacity of a register is exceeded.
- PARITY CHECK A summation check in which the binary digits in a character are added and the sum checked against a previously computed parity digit; i.e., a check which tests whether the number of ones is odd or even.
- PARTIAL ADD An addition without carries. Accomplished by toggling each bit of the augend where the corresponding bit of the addend is a "1".
- P REGISTER The Program Address Counter is a two's complement additive register (modulus 2<sup>15</sup>) which generates in sequential order the storage addresses containing the individual program steps.
- PROGRAM A precise sequence of instructions that accomplishes a computer routine; a plan for the solution of a problem.
- PROGRAM WORD Two 24-bit instructions contained in one 48-bit storage address; the higher-order 24 bits are the upper instruction, lower-order 24 bits, the lower instruction. A pair of instructions is read from storage, and the upper instruction is executed first. The lower one is then executed, except when the upper one provides for skipping the lower one.
- Q REGISTER Auxiliary arithmetic register which assists the A register in the more complicated arithmetic operations (modulus 2<sup>48</sup>-1).
- RANDOM ACCESS Access to storage under conditions in which the next position from which information is to be obtained is in no way dependent on the previous one.
- R REGISTER Address Buffer register. Two's complement subtractive register (modulus 2<sup>15</sup>) which acts as an exchange register for transmissions involving index registers.
- READ To obtain a quantity from a storage location.

READY	<ol> <li>An input/output control signal sent by the computer or an external equipment. The ready signal indicates that a word or character is available for transmission.</li> <li>A status response indicating that the external device being addressed is ready for operation.</li> </ol>
RELATIVE ADDRESS	Identifies a word in a subroutine or routine with respect to its position. Relative addresses are translated into absolute addresses by the addition of some specific reference address, usually that at which the first word of the routine is stored.
REPLACE	In the title of an instruction, the result of the execution of the instruction is stored in the location from which the initial operand was obtained.
RESUME	The input/output control signal sent by either the computer or an external equipment to indicate that it is prepared to receive another word (48 bits) or character (usually 6 bits). The resume signal is thus a request for data.
RETURN JUMP	An instruction that jumps from a sequence of instructions to initiate a second sequence and prepares for returning to the original sequence after the second is completed.
ROUTINE	The sequence of operations which the computer performs under the direction of a program.
S <sup>1</sup> REGISTER	Storage Address register (even storage). Selects the storage address specified by the contents of the P register.
S <sup>2</sup> REGISTER	Storage Address register (odd storage). Selects the storage address specified by the contents of the P register.
SCALE FACTOR	One or more coefficients by which quantities are multiplied or divided so that they lie in a given range of magnitude.
SCANNER	A circuit used to search for one of a number of possible conditions and to initiate action when a condition is detected. The auxiliary scanner scans the six buffer channels for auxiliary requests; the interrupt scanner looks for interrupt requests from external equipments.

SECONDARY REGISTERS	Transient registers not displayed on the console (U <sup>2</sup> , S <sup>1, 2</sup> , $Z^{1, 2}$ , R, X, O <sup>1</sup> -O <sup>6</sup> ).
SHIFT	To move the bits of a quantity right or left.
SIGN BIT	In registers where a quantity is treated as signed by use of one's complement notation, the bit in the highest-order stage of the register. If the bit is "1", the quantity is negative; if the bit is "0", the quantity is positive.
SIGN EXTENSION	The duplication of the sign bit in the higher-order stages of a register.
SKIP	To omit the execution of a lower instruction in a program; occurs only if the upper instruction provides for skipping on a specified condition, and the condition is met.
STAGE	The FFs and inverters associated with a bit position of a register.
STORE	To transmit information to a device from which the unaltered information can later be obtained.
SUBINSTRUCTION	The index code specifies one of eight forms of the instruction indicated by the operation code. Such forms are called "sub- instructions". Thus, 74.0 is a subinstruction of instruction 74.
TOGGLE	To complement each bit of a quantity as a result of an individual condition.
TRANSFER	High-speed data input/output transmission under direct program control.
TRANSMISSION, FORCED	A transfer of bits into a register which has not been cleared previously.
TRANSMISSION, ONES	A transfer of ones into a register which has been cleared.
TRANSMISSION, ZEROS	A transfer of zeros into a register which has been set.
TWO'S COMPLEMENT	Number that results from subtracting each bit of a number from "0". The two's complement may be formed by complementing each bit of the given number and then adding one to the result, performing the required carries.

U <sup>1</sup> REGISTER	Program Control register. Holds a program step while the two instructions contained in it are executed.			
U <sup>2</sup> REGISTER	Auxiliary Program Control register. A 15-bit subtractive accumulator (modulus 2 <sup>15</sup> -1) used primarily for modification of the base execution address.			
UPPER ADDRESS	The execution address portion of an upper instruction; bit positions 24 through 38 of a 48-bit register or storage address.			
UPPER INSTRUCTION	See Program Word.			
WORD	A unit of information which has been coded for use in the computer as a series of bits. The normal word length is 48 bits.			
WRITE	To enter a quantity into a storage location.			
X REGISTER	Exchange register. Most internal transmissions between the arithmetic section and the rest of the computer are made through X.			
Z <sup>1</sup> REGISTER	Storage Restoration register (even storage). Holds the word to be written into a given storage location.			
$z^2$ register	Storage Restoration register (odd storage). Holds the word to be written into a given storage location.			

# **APPENDIX SECTION**

# **APPENDIX I** NUMBER SYSTEMS

Any number system may be defined by two characteristics, the radix or base and the modulus. The radix or base is the number of unique symbols used in the system. The decimal system has ten symbols, 0 through 9. Modulus is the number of unique quantities or magnitudes a given system can distinguish. For example, an adding machine with ten digits, or counting wheels, would have a modulus of  $10^{10}$ -1. The decimal system has no modulus because an infinite number of digits can be written, but the adding machine has a modulus because the highest number which can be expressed is 9, 999, 999, 999.

Most number systems are positional, that is, the relative position of a symbol determines its magnitude. In the decimal system, a 5 in the units column represents a different quantity than a 5 in the tens column. Quantities equal to or greater than 1 may be represented by using the 10 symbols as coefficients of ascending powers of the base 10. The number 984<sub>10</sub> is:

$$9 \times 10^{2} = 9 \times 100 = 900$$
  
+8 \times 10^{1} = 8 \times 10 = 80  
+4 \times 10^{0} = 4 \times 1 = 4  
984<sub>10</sub>

Quantities less than 1 may be represented by using the 10 symbols as coefficients of ascending negative powers of the base 10. The number  $0.593_{10}$  may be represented as:

$$5 \times 10^{-1} = 5 \times .1 = .5$$
  
+9 \times 10^{-2} = 9 \times .01 = .09  
+3 \times 10^{-3} = 3 \times .001 = .003  
0.593\_{10}

#### BINARY NUMBER SYSTEM

Computers operate faster and more efficiently by using the binary number system. There are only two symbols 0 and 1; the base = 2. The following shows the positional value.

The binary number 011010 represents:

$$0 \times 2^{5} = 0 \times 32 = 0$$
  
+1 \times 2^{4} = 1 \times 16 = 16  
+1 \times 2^{3} = 1 \times 8 = 8  
+0 \times 2^{2} = 0 \times 4 = 0  
+1 \times 2^{1} = 1 \times 2 = 2  
+0 \times 2^{0} = 0 \times 1 = 0  
26  
10

Fractional binary numbers may be represented by using the symbols as coefficients of ascending negative powers of the base.

 $2^{-1}$   $2^{-2}$   $2^{-3}$   $2^{-4}$   $2^{-5}$  . . . Binary Point . =1/2 =1/4 =1/8 =1/16 =1/32

The binary number 0.10 110 may be represented as:

$$1 \times 2^{-1} = 1 \times 1/2 = 1/2 = 8/16$$
  
+0 \times 2^{-2} = 0 \times 1/4 = 0 = 0  
+1 \times 2^{-3} = 1 \times 1/8 = 1/8 - 2/16  
+1 \times 2^{-4} = 1 \times 1/16 = 1/16 = 1/16  
11/16\_{10} = 0.6875

#### OCTAL NUMBER SYSTEM

The octal number system uses eight discrete symbols, 0 through 7. With the base eight the positional value is:

 $8^{5}$	$8^4$	$8^{3}$	$8^{2}$	$8^1$	$8^{0}$
32,768	4,096	512	64	8	1

The octal number  $513_8$  represents:

$$5 \times 8^{2} = 5 \times 64 = 320$$
  
+1 \times 8^{1} = 1 \times 8 = 8  
+3 \times 8^{0} = 3 \times 1 = 3  
331\_{10}
Fractional octal numbers may be represented by using the symbols as coefficients of ascending negative powers of the base.

$$8^{-1}$$
  $8^{-2}$   $8^{-3}$   $8^{-4}$  ...  
1/8 1/64 1/512 1/4096

The octal number 0.4520 represents:

$$4 \times 8^{-1} = 4 \times 1/8 = 4/8 = 256/512$$
  
+5 x 8<sup>-2</sup> = 5 x 1/64 = 5/64 = 40/512  
+2 x 8<sup>-3</sup> = 2 x 1/512 = 2/512 = 2/512  
298/512 = 149/256<sub>10</sub> = .5811

### ARITHMETIC

### ADDITION AND SUBTRACTION

Binary numbers are added according to the following rules:

The addition of two binary numbers proceeds as follows (the decimal equivalents verify the result):

Augend	0111	(7)
Addend	+0100	+(4)
Sum	1011	(11)

Subtraction may be performed as an addition:

8 (minuend)		1000 (minuend)
-6 (subtrahend)	or	$\pm 1001$ (one's complement of subtrahend)
2 (difference)		0001 (partial sum)
		1 (carry)
		0010 (difference by addition)

### One's Complement

The 1604-A performs all arithmetic operations in the binary one's complement mode. In this system, positive numbers are represented by the binary equivalent and negative numbers in one's complement notation.

The one's complement representation of a number is found by subtracting each bit of the number from 1. For example:

This representation of a negative binary quantity may also be obtained by substituting "1's" for "0's" and "0's" for "1's".

The value zero can be represented in one's complement notation in two ways:

$$0000 \rightarrow 00_2$$
 Positive (+) Zero  
1111  $\rightarrow 11_2$  Negative (-) Zero

The rules regarding the use of these two forms for computation are:

- 1) Both positive and negative zero are acceptable as arithmetic operands.
- 2) If the result of an arithmetic operation is zero, it will be expressed as positive zero. The one exception to this rule is when negative zero is added to negative zero.\* In this case, the result is negative zero.

One's complement notation applies not only to arithmetic operations performed in A, but also to the modification of execution addresses in the  $U^2$  register. During address modification, the modified address will equal 77777<sub>8</sub> only if the unmodified execution address equals 77777<sub>8</sub> and b = 0 or (B<sup>b</sup>) = 77777<sub>8</sub>.

### Two's Complement

The counters in the computer use two's complement arithmetic. A counter is a register with provisions for increasing its contents by one if it is additive (P register) or decreasing its contents by one if it is subtractive (R register). A two's complement counter is open-ended; there is no end-around carry or borrow.

<sup>\*</sup> When a 1604-A instruction calls for subtracting positive zero from negative zero, the computer complements the subtrahend and adds so that the actual operation is the addition of negative zero to negative zero and the result is negative zero.

Positive numbers have the same representation in both systems while negative values differ by one count.

Count	2's comp. rep.	l's comp. rep.
+2	00010	00010
+1	00001	00001
0	00000	00000
-1	11111	11110
-2	11110	11101

The difference in the representation of negative values in these two systems is due to the skipping of the "all one's" count in one's complement notation. In the one's complement system the end-around-carry feature of the register automatically changes a count of all one's to all zeros. (Note exception under one's complement.)

As an example, if the content of a subtractive counter is positive seven (0111) and is to be reduced by one, add the two's complement expression of negative one. (1111), to 0111 as shown below. The result is six.

$$\begin{array}{r}
 0111 \\
 +1111 \\
 \hline
 0110
 \end{array}$$

Note that the two's complement expression for a negative number may also be formed by adding one to the one's complement representation of the number.

### MULTIPLICATION

Binary multiplication proceeds according to the following rules:

$$0 x 0 = 0 
0 x 1 = 0 
1 x 0 = 0 
1 x 1 = 1$$

Multiplication is always performed on a bit-by-bit basis. Carries do not result from multiplication, since the product of any two bits is always a single bit.

Decimal example:

multiplicand	14
multiplier	12
partial products	28
	<u>14</u> (shifted one place left)
product	<sup>168</sup> 10

The shift of the second partial product is a shorthand method for writing the true value 140.

### Binary example:

multiplicand	(14)	1110	
multiplier	(12)	1100	
	(	0000	
		0000	shift to place digits
partial produc	ts	1110	in proper columns
	L	1110	
product (168	<sup>3</sup> 10)	101010002	

The computer determines the running subtotal of the partial products. Rather than shifting the partial product to the left to position it correctly, the computer right shifts the summation of the partial products one place before the next addition is made. When the multiplier bit is "1", the multiplicand is added to the running total and the results are shifted to the right one place. When the multiplier bit is "0", the partial product subtotal is shifted to the right (in effect, the quantity has been multiplied by  $10_2$ ).

### DIVISION

The following example shows the familiar method of decimal division:

		14	quotient
divisor	13	185	dividend
		_13_	
		55	partial dividend
		52	
		3	remainder

The computer performs division in a similar manner (using binary equivalents):

	1110	quotient (14)
divisor	1101 10111001	dividend
	1101	
	10100	
	1101	
	1110	partial dividends
	1101	
	11	remainder (3)

However, instead of shifting the divisor right to position it for subtraction from the partial dividend (shown above), the computer shifts the partial dividend left, accomplishing the same purpose and permitting the arithmetic to be performed in the A register. The computer counts the number of shifts, which is the number of quotient digits to be obtained; after the correct number of counts, the routine is terminated.

## CONVERSIONS

The procedures that may be used when converting from one number system to another are power addition, double dabble, and substitution.

Conversion	Recommended Method						
Binary to Decimal	Power Addition						
Octal to Decimal	Power Addition						
 Decimal to Binary	Double Dabble						
Decimal to Octal	Double Dabble						
Binary to Octal	Substitution						
Octal to Binary	Substitution						
GENERAL RULES							
$r_i > r_f$ : use Double Dabble, Substitution							
$r_i < r_f$ : use Power Addition, Substitution							
r <sub>i</sub> = Radix of initial system							
$r_{f}^{1}$ = Radix of final system							
-							

Recommended Conversion Procedures (Integer and Fractional)

### POWER ADDITION

To convert a number from  $r_i$  to  $r_f$  ( $r_i < r_f$ ) write the number in its expanded  $r_i$  polynomial form and symplify using  $r_f$  arithmetic.

EXAMPLE I Binary to Decimal (Integer)  $010\ 111_2 = 1\ (2^4) + 0\ (2^3) + 1\ (2^2) + 1\ (2^1) + 1\ (2^0)$ = 1 (16) + 0 (8) + 1 (4) + 1 (2) + 1 (1)= 16 + 0 + 4 + 2 + 1  $= 23_{10}$ Binary to Decimal (Fractional) EXAMPLE 2  $.0101_{2} = 0 (2^{-1}) + 1 (2^{-2}) + 0 (2^{-3}) + 1 (2^{-4})$ = 0 + 1/4 + 0 + 1/16 $= 5/16_{10} = 0.3125$ Octal to Decimal (Integer) EXAMPLE 3  $324_8 = 3 (8^2) + 2 (8^1) + 4 (8^0)$ = 3 (64) + 2 (8) + 4 (1)= 192 + 16 + 4  $= 212_{10}$ Octal to Decimal (Fractional) EXAMPLE 4  $.44_8 = 4 (8^{-1}) + 4 (8^{-2})$ = 4/8 + 4/64 $= 36/64_{10} = 0.5625$ 

DOUBLE DABBLE

To convert a whole number from  $r_i$  to  $r_f (r_i > r_f)$ :

- 1) Divide  $r_i$  by  $r_f$  using  $r_i$  arithmetic
- 2) The remainder is the lowest order bit in the new expression
- 3) Divide the integral part from the previous operation by  $r_{f}$
- 4) The remainder is the next higher order bit in the new expression
- 5) The process continues until the division produces only a remainder which will be the highest order bit in the  $r_f$  expression.

To convert a fractional number from  $r_i$  to  $r_f$ :

- 1) Multiply  $r_i$  by  $r_f$  using  $r_i$  arithmetic
- 2) The integral part is the highest order bit in the new expression
- 3) Multiply the fractional part from the previous operation by  ${\bf r}_{\rm f}$
- 4) The integral part is the next lower order bit in the new expression
- 5) The process continues until sufficient precision is achieved or the process terminates.

**EXAMPLE 1** Decimal to Binary (Integer)

45	÷	2 = 22 1	remainder	1; record	1
22	÷	2 = 11 1	remainder	0; record	0
11	*	2 = 5 1	remainder	1; record	1
5	÷	2 = 2	remainder	1; record	1
2	÷	2 = 1	remainder	0; record	0
1	÷	2 = 0 1	remainder	1; record	1
Th	us:	45 <sub>10</sub> =	1011012		101101

EXAMPLE	2	Decimal to Binary	(Fractional)
	.25 x 2	2 = 0.5; record	0
	.5 x 2	2 = 1.0; record	1
	.0 x 2	2 = 0.0; record	0
		<b>D</b> E = 010	.010

Thus:  $.25_{10} = .010_2$ 

**EXAMPLE 3** Decimal to Octal (Integer)  $273 \div 8 = 34$  remainder 1; record 1  $34 \div 8 = 4$  remainder 2; record 2  $4 \div 8 = 0$  remainder 4; record 4 Thus:  $273_{10} = 421_8$  421 EXAMPLE 4 Decimal to Octal (Fractional) .55 x 8 = 4.4; record 4 .4 x 8 = 3.2; record 3 .2 x 8 = 1.6; record 1 -- -- -- -- --.431... Thus:  $.55_{10}^{-} .431..._{8}$ 

### SUBSTITUTION

This method permits easy conversion between octal and binary representations of a number. If a number in binary notation is partitioned into triplets to the right and left of the binary point, each triplet may be converted into an octal digit. Similarly each octal digit may be converted into a triplet of binary digits.

EXAMPLE	I	Binary to Octal								
		Binary Octal	= :	110 6	000 0	. 0(	D1 I	010 2		
EXAMPLE	2	Octal t	o B	Bina	ry					
		Octal	=	6	5	0		2	2	7
		Binary	= :	110	101	000	•	010	010	111

Decimal	Binary	Octal
00	00000	00
01	00001	01
02	00010	02
03	00011	03
04	00100	04
05	00101	05
06	00110	06
07	00111	07
08	01000	10
09	0 1 0 0 1	11
10	01010	12
11	01011	13
12	01100	14
13	01101	15
14	01110	16
15	01111	17
16	10000	20
17	10001	21

## COMMON PURE NOTATIONS

POWERS OF COMMON NUMBER SYSTEMS

[						
2 <sup>0</sup>	Ξ	1	8 <sup>0</sup> =	1	10 <sup>0</sup> =	1
$2^{1}$	=	2	8 <sup>1</sup> =	8	10 <sup>1</sup> =	10
$2^{2}$	=	4	8 <sup>2</sup> =	64	$10^2 =$	100
$2^{3}$	=	8	8 <sup>3</sup> =	512	$10^{3} =$	1,000
24	=	16	84 =	4,096	10 <sup>4</sup> =	10,000
25	Ξ	32	8 <sup>5</sup> =	32,768	10 <sup>5</sup> =	100,000
$2^{6}$	=	64	8 =	262,144	10 <sup>6</sup> =	1,000,000
$2^{7}$	=	128	87 =	2,097,152		
28	Ξ	256	8 <sup>8</sup> =	16,777,216		
29	=	512				
2 <sup>10</sup>	=	1,024				

### FIXED POINT AND FLOATING POINT NUMBERS

Any number may be expressed in the form  $kB^n$ , where k is a coefficient, B a base number, and the exponent n the power to which the base number is raised.

A fixed point number assumes:

- 1) The exponent n = 0 for all fixed point numbers.
- 2) The coefficient, k, occupies the same bit positions within the computer word for all fixed point numbers.
- 3) The radix (binary) point remains fixed with respect to one end of the expression.

A 1604 fixed point number consists of a sign bit and coefficient as shown below. The upper bit of any 1604 fixed point number designates the sign of the coefficient (47 lower order bits). If the bit is "1", the quantity is negative since negative numbers are represented in one's complement notation; a "0" sign bit signifies a positive coefficient.



The coefficient may be an integer or fraction. The radix (binary) point, in the case of an integer, is assumed to be immediately to the right of the lowest order bit (00). In the case of the fraction, the point is just to the right of the sign bit.

In many instances, the values in a fixed point operation may be too large or too small to be expressed by the computer. The programmer must position the numbers within the word format so they can be represented with sufficient precision. The process, called scaling, consists of shifting the values a predetermined number of places. The numbers must be positioned far enough to the right in the register to prevent overflow but far enough to the left to maintain precision. The scale factor (number of places shifted) is expressed as the power of the base. For example,  $5,100,000_{10}$  may be expressed as  $0.51 \times 10^7$ ,  $0.051 \times 10^8$ ,  $0.0051 \times 10^9$ , etc. The scale factors are 7, 8, and 9.

Since only the coefficient is used by the computer, the programmer is responsible for remembering the scale factors. Also, the possibility of an overflow during intermediate operations must be considered. For example, if two fractions in fixed point format are

multiplied, the result is a number < 1. If the same two fractions are added, subtracted, or divided, the result may be greater than one and an overflow will occur. Similarly, if two integers are multiplied, divided, subtracted or added, the likelihood of an over-flow is apparent.

As an alternative to fixed point operation, a method involving a variable radix point, called floating point, is used. This significantly reduces the amount of bookkeeping required on the part of the programmer.

By shifting the radix point and increasing or decreasing the value of the exponent, widely varying quantities which do not exceed the capacity of the machine may be handled.

Floating point numbers within the computer are represented in a form similar to that used in "scientific" notation, that is, a coefficient or fraction multiplied by a number raised to a power. Since the computer uses only binary numbers, the numbers are multiplied by powers of two.

> $F \cdot 2^E$  where: F = fractionE = exponent

In floating point, different coefficients need not relate to the same power of the base as they do in fixed point format. Therefore, the construction of a floating point number includes not only the coefficient but also the exponent.



### Coefficient

The coefficient consists of a 36-bit fraction in the 36 lower-order positions of the floating point word. The coefficient is a normalized fraction; it is equal to or greater than 1/2 but less than 1. The highest order bit position (47) is occupied by the sign bit of the coefficient. If the sign bit is a "0", the coefficient is positive; a "1" bit denotes a negative fraction (negative fractions are represented in one's complement notation).

### Exponent

The floating point exponent is expressed as an 11-bit quantity with a value ranging from  $0000_8$  to  $3777_8$ . It is formed by adding a true positive exponent and a bias of  $2000_8$  or a true negative exponent and a bias of  $1777_8$ . This results in a range of biased exponents as shown below.

True Positive Exponent	Biased Exponent	True Negative Exponent	Biased Exponent
+0	2000	-0	2000*
+1	2001	-1	1776
+2	2002	-2	1775
+1776	3776	-1776	0001
+17778	3777 <sub>8</sub>	-1777 <sub>8</sub>	00008

The exponent is biased so that floating point operands can be compared with each other in the normal fixed point mode.

As an example, compare the unbiased exponents of  $+52_{8}$  and  $+0.02_{8}$  (Example 1).

EXAMPLE I		Number =	+52			
	0	0 0	000	000	110	(36 bits)
	Coefficient Sign		Expoi	nent		Coefficient
		Number =	= +0.02	2		
	0	1 1	111	111	011	(36 bits)
	Coefficient Sign		Expo	nent		Coefficient

In this case +0.02 appears to be larger than +52 because of the larger exponent. If, however, both exponents are biased, (Example 2) changing the sign of both exponents makes +52 greater than +0.02.

<sup>\*</sup> Minus zero is sensed as positive zero by the computer and is therefore biased by  $2000_8$  rather than  $1777_8$ .

EXAMPLE	2	Number =	+528			
	0	1 0	000	000	110	(36 bits)
	Coefficient Sign		Exp	onent		Coefficient
		Number =	+0.028			
	0	0 1	111	111	011	(36 bits)
	Coefficient Sign		Expo	onent		Coefficient

When bias is used with the exponent floating-point operation is more versatile since floating-point operands can be compared with each other in the normal fixed point mode.

### CONVERSION PROCEDURES

### Fixed Point to Floating Point

- 1) Express the number in binary.
- 2) Normalize the number. A normalized number has the most significant 1 positioned immediately to the right of the binary point and is expressed in the range  $1/2 \le k \le 1$ .
- 3) Inspect the sign of the true exponent. If the sign is positive add 2000<sub>8</sub> (bias) to the true exponent of the normalized number. If the sign is negative add the bias 1777<sub>8</sub> to the true exponent of the normalized number. In either case, the resulting exponent is the biased exponent.
- 4) Assemble the number in floating point.
- 5) Inspect the sign of the coefficient. If negative, complement the assembled floating point number to obtain the true floating point representation of the number. If the sign of the coefficient is positive the assembled floating point number is the true representation.

### **EXAMPLE** I Convert +4.0 to floating point

- 1) The number is expressed in octal.
- 2) Normalize.  $4.0 = 4.0 \times 8^0 = 0.100 \times 2^3$ .
- Since the sign of the true exponent is positive, add 2000<sub>8</sub> (bias) to the true exponent. Biased exponent = 2000 + 3.

- 4) Assemble number in floating point format. Coefficient = 400 000 000 000<sub>8</sub> Biased Exponent = 2003<sub>8</sub> Assembled word = 2003 400 000 000 000<sub>9</sub>
- 5) Since the sign of the coefficient is positive, the floating point representation of +4.0 is as shown. If, however, the sign of the coefficient were negative, it would be necessary to complement the entire floating point word.

**EXAMPLE 2** Convert - 4.0 to floating point

- 1) The number is expressed in octal.
- 2) Normalize.  $-4.0 = -4.0 \times 8^0 = -0.100 \times 2^3$
- 3) Since the sign of the true exponent is positive, add  $2000_8$  (bias) to the true exponent. Biased exponent = 2000 + 3.
- Assemble number in floating point format. Coefficient = 400 000 000 000<sub>8</sub> Biased Exponent = 2003<sub>8</sub> Assembled word = 2003 400 000 000 000<sub>8</sub>
- 5) Since the sign of the coefficient is negative, the assembled floating point word must be complemented. Therefore, the true floating point representation for -4.0 = 5774 377 777 777 777<sub>8</sub>

## EXAMPLE 3 Convert $0.5_{10}$ to floating point

- 1) Convert to octal.  $0.5_{10} = 0.4_{8}$
- 2) Normalize.  $0.4 = 0.4 \times 8^{0} 0.100 \times 2^{0}$
- Since the sign of the true exponent is positive, add 2000<sub>8</sub> (bias) to the true exponent. Biased exponent = 2000 + 0.
- Assemble number in floating point format. Coefficient = 400 000 000 000<sub>8</sub> Biased Exponent = 2000<sub>8</sub> Assembled word = 2000 400 000 000<sub>0</sub>
- 5) Since the sign of the coefficient is positive, the floating point representation of  $+0.5_{10}$  is as shown. If, however, the sign of the coefficient were negative, it would be necessary to complement the entire floating point word. This example is a special case of floating point since the exponent of the normalized number is 0 and could be represented as -0. The exponent would then be biased by 1777<sub>8</sub> instead of 2000<sub>8</sub> because of the negative exponent. The 1604, however, recognizes -0 as +0 and biases the exponent by 2000<sub>8</sub>.

EXAMPLE 4 Convert  $0.04_{g}$  to floating point

- 1) The number is expressed in octal.
- 2) Normalize.  $0.04 = 0.04 \times 8^0 = 0.4 \times 8^{-1} = 0.100 \times 2^{-3}$ .
- 3) Since the sign of the true exponent is negative, add  $1777_8$  (bias) to the true exponent. Biased exponent =  $1777_8 + (-3) = 1774_8$ .
- 4) Assemble number in floating point format. Coefficient = 400 000 000 000<sub>8</sub> Biased Exponent = 1774<sub>8</sub> Assembled word = 1774 400 000 000 000<sub>8</sub>
- 5) Since the sign of the coefficient is positive, the floating point representation of 0.04<sub>8</sub> is as shown. If, however, the sign of the coefficient were negative, it would be necessary to complement the entire floating point word.

Floating Point to Fixed Point Format

- If the floating point number is negative, complement the entire floating point word and record the fact that the quantity is negative. The exponent is now in a true biased form.
- 2) If the biased exponent is equal to or greater than  $2000_8$  subtract  $2000_8$  to obtain the true exponent. If less than  $2000_8$  subtract  $1777_8$  to obtain true exponent.
- 3) Separate the coefficient and exponent. If the true exponent is negative the binary point should be moved to the left the number of bit positions indicated by the true exponent. If the true exponent is positive, the binary point shoud be moved to the right the number of bit positions indicated by the true exponent.
- 4) The coefficient has now been converted to fixed binary. The sign of the coefficient will be negative if the floating point number was complemented in step one. (The sign bit must be extended if the quantity is placed in a register.)
- 5) Represent the fixed binary number in fixed octal notation.

### EXAMPLE | Convert floating point number 2003 400 000 000 000<sub>g</sub> to fixed octal

- 1) The floating point number is positive and remains uncomplemented.
- 2) The biased exponent  $> 2000_8$ , therefore subtract  $2000_8$  from the biased exponent to obtain the true exponent of the number. 2003 2000 = +3
- 3) Coefficient = 400 000 000  $000_8$  = .100<sub>2</sub>. Move binary point to the right 3 places. Coefficient = 100.0<sub>2</sub>

- 4) The sign of the coefficient is positive because the floating point number was not complemented in step one.
- 5) Represent in fixed octal notation.  $100.0 \ge 2^0 = 4.0 \ge 8^0$

EXAMPLE 2 Convert floating point number 5774 377 777 777 777 8 to fixed octal

1) The sign of the coefficient is negative, therefore, complement the floating point number.

Complement = 2003 400 000 000 000<sub>g</sub>

- 2) The biased exponent (in complemented form)  $> 2000_8$ , therefore subtract  $2000_8$  from the biased exponent to obtain the true exponent of the number. 2003 - 2000 = +3
- 3) Coefficient =  $4000\ 000\ 000\ 000_8 = 0.100_2$ Move binary point to the right 3 places. Coefficient =  $100.0_9$
- 4) The sign of the coefficient will be negative because the floating point number was originally complemented.
- 5) Convert to fixed octal.  $-100.0_2 = -4.0_8$

EXAMPLE 3 Convert floating point number 1774 400 000 000 000<sub>g</sub> to fixed octal

- 1) The floating point number is positive and remains uncomplemented.
- 2) The biased exponent  $< 2000_8$ , therefore subtract  $1777_8$  from the biased exponent to obtain the true exponent of the number.  $1774_8 1777_8 = -3$
- Coefficient = 400 000 000 000<sub>8</sub> = .100<sub>2</sub>
   Move binary point to the left 3 places.
   Coefficient = .000100<sub>9</sub>
- 4) The sign of the coefficient is positive because the floating point number was not complemented in step one.
- 5) Represent in fixed octal notation.  $.000100_2 = .04_8$

# APPENDIX II FAULTS

Certain fault conditions may occur in the execution of a computer program which may be sensed by EXF instructions. The occurrence of the fault does not stop operation but sets an indicator that can be sensed. A fault is visually indicated on the console.

### SHIFT FAULT

Any attempt to shift a register more than  $127_{10}$  (177<sub>8</sub>) places right or left results in a shift fault. If the fault exists, the indicator is set prior to execution of the shift instruction and the shift fault background light on the console display panel is lighted. The shifts will be performed regardless of the status of the fault indicator. If an interrupt has been selected, the main program will be interrupted after executing the shift instruction. The shift fault may be sensed by 47 7 00120, 1.

### DIVIDE FAULT

A divide fault occurs in fixed point divide instructions (25 and 27) when the divisor is zero or the required quotient exceeds the 47-bit capacity of the quotient register, Q. The sign bit of Q is examined at the end of the division phase. If it is equal to "1", a divide fault has occurred. If an interrupt has been selected, the main program will be interrupted after the divide instruction is completed. A divide fault is sensed by a 74 0 00110, 1.

### OVERFLOW FAULT

An overflow fault results when the capacity of the A register  $(2^{47}-1)$  is exceeded. The fault is detected at the time the operation causing the overflow takes place.

If an interrupt on arithmetic faults has been selected, the main program will be halted before another instruction can be executed.

An overflow may be sensed by a 74 7 00130, 1.

### CLOCK OVERFLOW

A clock overflow results if the capacity of the A register is exceeded during an advance clock operation. If an interrupt on arithmetic faults has been selected, the interrupt will occur before an instruction can be executed after the advance clock operation. Clock overflow may be sensed by 74 7 00300, 1.

### EXPONENT (Floating Point Range) FAULT

The exponent fault occurs during floating point instructions when the exponent of the result, after rounding and normalizing, is  $\ge 2^{\pm 10}$  (overflow) or  $\le 2^{-10}$  (underflow). The exponent fault is sensed by a 74 7 00140, 1.

### EVEN AND ODD STORAGE FAULTS

These faults indicate a failure in computer storage and turn on background lights on the console display. The indicators may be cleared by an internal master clear. If a storage fault is produced, maintenance should be notified.

# APPENDIX III

TABLE OF POWERS OF 2

# APPENDIX IV

# OCTAL-DECIMAL INTEGER CONVERSION TABLE

			0	1	2	3	4	5	6	7	]		0	1	2	3	4	5	6	7
0000 0	000 [	0000						00.05			1									
to	to	0000	0000	0001	0002	0003	0004	0005	0006	0007		0400	0256	0257	0258	0259	0260	0261	0262	0263
0777 0.	511 simal)	0020	0016	0017	0018	0019	0020	0021	0022	0023		0420	0272	0273	0274	0275	0276	0277	0278	0279
		0030	0024	0025	0026	0027	0028	0029	0030	0031		0430	0280	0281	0282	0283	0284	0285	0286	0287
		0040	0032	0033	0034	0035	0036	0037	0038	0039		0440	0288	0289	0290	0291	0292	0293	0294	0295
Octal Dec	imal	0060	0048	0049	0050	0051	0052	0053	0054	0055		0450	0304	0305	0306	0307	0308	0309	0310	0311
10000 - 40	96	0070	0056	0057	0058	0059	0060	0061	0062	0063		0470	0312	0313	0314	0315	0316	0317	0318	0319
20000 - 81	92	0100	0064	0065	0066	0067	0069	0060	0070	0071		0500	0320	0331	0333	0222	0324	0225	0336	0227
40000 - 163	84	0110	0072	0073	0074	0075	0076	0003	0078	0079		0510	0328	0329	0330	0331	0332	0333	0334	0335
50000 - 204	80	0120	0080	0081	0082	0083	0084	0085	0086	0087	ĺ	0520	0336	0337	0338	0339	0340	0341	0342	0343
60000 - 245	76	0130	0088	0089	0090	0091	0092	0093	0094	0095		0530	0344	0345	0346	0347	0348	0349	0350	0351
/0000 - 286	/2	0140	0096	0097	0098	0099	0100	0101	0102	0103		0540	0352	0353	0354	0355	0355	0357	0358	0359
		0160	0112	0113	0114	0115	0116	0117	0118	0119		0560	0368	0369	0370	0371	0372	0373	0374	0375
		0170	0120	0121	0122	0123	0124	0125	0126	0127		0570	0376	0377	0378	0379	0380	0381	0382	0383
		0200	0128	0129	0130	0131	0132	0133	0134	0135		0600	0384	0385	0386	0387	0388	0389	0390	0391
		0210	0136	0137	0138	0139	0140	0141	0142	0143		0610	0392	0393	0394	0395	0396	0397	0398	0399
		0220	0144	0145	0146	0147	0148	0149	0150	0151		0620	0400	0401	0402	0403	0404	0405	0406	0407
		0240	0160	0161	0162	0163	0164	0165	0166	0167		0640	0416	0417	0418	0419	0420	0421	0422	0423
		0250	0168	0169	0170	0171	0172	0173	0174	0175		0650	0424	0425	0426	0427	0428	0429	0430	0431
	9	0260	0176	0177	0178	0179	0180	0181	0182	0183		0660	0432	0433	0434	0435	0436	0437	0438	0439
	10	0270	0184	0185	0186	0187	0188	0189	0190	0191		0670	0440	0441	0442	0443	0444	0445	0440	0447
		0300	0192	0193	0194	0195	0196	0197	0198	0199		0700	0448	0449	0450	0451	0452	0453	0454	0455
		0320	0208	0209	0210	0211	0212	0213	0214	0215		0720	0464	0465	0466	0467	0468	0469	0470	0471
	0	0330 (	0216	0217	0218	0219	0220	0221	0222	0223		0730	0472	0473	0474	0475	0476	0477	0478	0479
		0340   (	0224	0225	0226	0227	0228	0229	0230	0231		0740	0480	0481	0482	0483	0484	0485	0486	0487
		0350 0	0232	0233	0234	0235	0236	0237	0238	0239		0750	0488	0489	0490	0491	0492	0493	0494	0503
	la	0370 0	0248	0249	0250	0251	0252	0253	0254	0255		0770	0504	0505	0506	0507	0508	0509	0510	0511
	-			• •																
		Г				2		5	6	7						 9		E	e	7
		[	0	1	2	3	4	5	6	7			0	1	2	3	4	5	6	7
1000   05	12	1000	0	1	<b>2</b> 0514	3 0515	4	5	6 0518	7		1400	0 0768	1 0769	2 0770	3 0771	4	5 0773	6 0774	7
1000 05 to t 1777 10	12 o 23	1000	0 0512 0520 0528	1 0513 0521 0529	2 0514 0522 0530	3 0515 0523 0531	4 0516 0524 0532	5 0517 0525 0533	6 0518 0526 0534	7 0519 0527 0535		1400 1410	0 0768 0776 0784	1 0769 0777 0785	2 0770 0778 0786	3 0771 0779 0787	4 0772 0780 0788	5 0773 0781 0789	6 0774 0782 0790	7 0775 0783 0791
1000 05 to t 1777 10 (Octal) (Deci	12 o 23 imal)	1000 1010 1020 1030	0 0512 0520 0528 0536	1 0513 0521 0529 0537	2 0514 0522 0530 0538	3 0515 0523 .0531 0539	4 0516 0524 0532 0540	5 0517 0525 0533 0541	6 0518 0526 0534 0542	7 0519 0527 0535 0543		1400 1410 1420 1430	0 0768 0776 0784 0792	1 0769 0777 0785 0793	2 0770 0778 0786 0794	3 0771 0779 0787 0795	4 0772 0780 0788 0796	5 0773 0781 0789 0797	6 0774 0782 0790 0798	7 0775 0783 0791 0799
1000 05 to t 1777 10 (Octal) (Deci	12 o 23 imal)	1000 1010 1020 1030 1040	0 0512 0520 0528 0536 0544	1 0513 0521 0529 0537 0545	2 0514 0522 0530 0538 0546	3 0515 0523 0531 0539 0547	4 0516 0524 0532 0540 0548	5 0517 0525 0533 0541 0549	6 0518 0526 0534 0542 0550	7 0519 0527 0535 0543 0551		1400 1410 1420 1430 1440	0 0768 0776 0784 0792 0800	1 0769 0777 0785 0793 0801	2 0770 0778 0786 0794 0802	3 0771 0779 0787 0795 0803	4 0772 0780 0788 0796 0804	5 0773 0781 0789 0797 0805	6 0774 0782 0790 0798 0806	7 0775 0783 0791 0799 0807
1000   05 to t 1777   10 (Octal)   (Deci	12 o 23 imal)	1000 1010 1020 1030 1040 1050	0 0512 0520 0528 0536 0544 0552	1 0513 0521 0529 0537 0545 0553	2 0514 0522 0530 0538 0546 0554	3 0515 0523 0531 0539 0547 0555	4 0516 0524 0532 0540 0548 0556	5 0517 0525 0533 0541 0549 0557 0557	6 0518 0526 0534 0542 0550 0558 0558	7 0519 0527 0535 0543 0551 0559 0567		1400 1410 1420 1430 1440 1450	0 0768 0776 0784 0792 0800 0808	1 0769 0777 0785 0793 0801 0809	2 0770 0778 0786 0794 0802 0810	3 0771 0779 0787 0795 0803 0811	4 0772 0780 0788 0796 0804 0812	5 0773 0781 0789 0797 0805 0813 0821	6 0774 0782 0790 0798 0806 0814	7 0775 0783 0791 0799 0807 0815
1000   05 to t 1777   10 (Octal)   (Deci	12 o 23 imol)	1000 1010 1020 1030 1040 1050 1060 1070	0 0512 0520 0528 0536 0544 0552 0560 0568	1 0513 0521 0529 0537 0545 0553 0561 0569	2 0514 0522 0530 0538 0546 0554 0554 0552 0570	3 0515 0523 0531 0539 0547 0555 0563 0571	4 0516 0524 0532 0540 0548 0556 0564 0572	5 0517 0525 0533 0541 0549 0557 0565 0573	6 0518 0526 0534 0542 0550 0558 0566 0574	7 0519 0527 0535 0543 0551 0559 0567 0575		1400 1410 1420 1430 1440 1450 1460 1470	0 0768 0776 0784 0792 0800 0808 0810 0824	1 0769 0777 0785 0793 0801 0809 0817 0825	2 0770 0778 0786 0794 0802 0810 0818 0826	3 0771 0779 0787 0795 0803 0811 0819 0827	4 0772 0780 0788 0796 0804 0812 0820 0828	5 0773 0781 0789 0797 0805 0813 0821 0829	6 0774 0782 0790 0798 0806 0814 0822 0830	7 0775 0783 0791 0799 0807 0815 0823 0831
1000   05 to t 1777 10 (Octal) (Deci	12 o 23 imal)	1000 1010 1020 1030 1040 1050 1060 1070	0 0512 0520 0528 0536 0544 0552 0560 0568 0576	1 0513 0521 0529 0537 0545 0553 0561 0569 0577	2 0514 0522 0530 0538 0546 0554 0554 0570 0578	3 0515 0523 0531 0539 0547 0555 0563 0571 0579	4 0516 0524 0532 0540 0548 0556 0564 0572 0580	5 0517 0525 0533 0541 0549 0557 0565 0573 0573	6 0518 0526 0534 0542 0550 0558 0566 0574 0582	7 0519 0527 0535 0543 0551 0559 0567 0575 0583		1400 1410 1420 1430 1440 1450 1460 1470	0 0768 0776 0784 0792 0800 0808 0616 0824 0832	1 0769 0777 0785 0793 0801 0809 0817 0825 0833	2 0770 0778 0786 0794 0802 0810 0818 0826 0834	3 0771 0779 0787 0795 0803 0811 0819 0827 0835	4 0772 0780 0788 0796 0804 0812 0820 0828 0828	5 0773 0781 0789 0797 0805 0813 0821 0829 0837	6 0774 0782 0790 0798 0806 0814 0922 0830 0838	7 0775 0783 0791 0799 0807 0815 0823 0831 0839
1000   05 to t 1777 10 (Octal) (Deci	12 o 23 imal)	1000 1010 1020 1030 1040 1050 1050 1070 1100 1110	0 0512 0520 0528 0536 0544 0552 0560 0568 0576 0584	1 0513 0521 0529 0537 0545 0553 0561 0569 0577 0585	2 0514 0522 0530 0538 0546 0554 0554 0570 0578 0586	3 0515 0523 0531 0539 0547 0555 0563 0571 0579 0587	4 0516 0524 0532 0540 0548 0556 0564 0572 0580 0588	5 0517 0525 0533 0541 0549 0557 0565 0573 0581 0581	6 0518 0526 0534 0542 0550 0558 0556 0574 0582 0590	7 0519 0527 0535 0543 0551 0559 0567 0575 0583 0591		1400 1410 1420 1430 1440 1450 1460 1460 1470 1500 1510	0 0768 0776 0784 0792 0800 0808 0816 0824 0832 0840	1 0769 0777 0785 0793 0801 0809 0817 0825 0833 0841	2 0770 0778 0786 0794 0802 0810 0818 0826 0834 0842	3 0771 0779 0787 0795 0803 0811 0819 0827 0835 0843	4 0772 0780 0788 0796 0804 0812 0820 0828 0836 0844	5 0773 0781 0789 0797 0805 0813 0821 0829 0837 0845	6 0774 0782 0790 0798 0806 0814 0822 0830 0838 0846	7 0775 0783 0791 0799 0807 0815 0823 0831 0839 0847
1000   05 to t 1777 10 (Octal) (Deci	12 o 23 imal)	1000 1010 1020 1030 1040 1050 1050 1070 1100 1110 1120	0 0512 0520 0528 0536 0544 0552 0568 0568 0576 0584 0592	1 0513 0521 0529 0537 0545 0553 0569 0577 0585 0593	2 0514 0522 0530 0538 0554 0554 0550 0570 0578 0586 0594	3 0515 0523 0531 0539 0547 0555 0563 0571 0579 0587 0595	4 0516 0524 0532 0540 0548 0556 0564 0572 0580 0588 0596	5 0517 0525 0533 0541 0549 0557 0565 0573 0581 0589 0597	6 0518 0526 0534 0542 0550 0558 0566 0574 0582 0590 0598	7 0519 0527 0535 0543 0559 0567 0575 0575 0583 0591 0599		1400 1410 1420 1430 1450 1450 1460 1470 1500 1510 1520	0 0768 0776 0784 0792 0800 0808 0816 0824 0832 0840 0848	1 0769 0777 0785 0793 0801 0809 0817 0825 0833 0841 0849	2 0770 0778 0786 0794 0802 0810 0818 0826 0834 0834 0842 0850	3 0771 0779 0787 0795 0803 0811 0819 0827 0835 0843 0851	4 0772 0780 0788 0796 0804 0812 0820 0828 0836 0844 0852	5 0773 0781 0789 0797 0805 0813 0821 0829 0837 0845 0853	6 0774 0782 0790 0798 0806 0814 0922 0830 0838 0846 0854	7 0775 0783 0791 0799 0805 0815 0823 0831 0839 0847 0855
1000   05 te t 1777   10 (Octal)   (Deci	12 o 23 imal)	1000 1010 1020 1030 1040 1050 1050 1050 1050 1050 1050 105	0 0512 0520 0528 0536 0544 0552 0560 0568 0576 0584 0592 0600	1 0513 0521 0529 0537 0545 0553 0553 0569 0577 0585 0593 0601 0600	2 0514 0522 0538 0546 0554 0554 0570 0578 0586 0594 0612	3 0515 0523 0531 0539 0547 0555 0563 0571 0579 0587 0595 0603 0603	4 0516 0524 0532 0540 0556 0564 0572 0580 0588 0596 0612	5 0517 0525 0533 0549 0557 0565 0573 0581 0589 0597 0613	6 0518 0526 0534 0550 0558 0556 0574 0582 0590 0598 0694	7 0519 0527 0535 0543 0551 0559 0567 0575 0583 0591 0599 0615		1400 1410 1420 1430 1440 1450 1460 1470 1500 1510 1520 1530	0 0768 0776 0784 0792 0800 0808 0816 0824 0832 0840 0848 0856	1 0769 0777 0785 0793 0809 0817 0825 0833 0841 0849 0857 0857	2 0770 0778 0786 0794 0802 0810 0818 0826 0834 0842 0850 0858 0858	3 0771 0779 0787 0795 0803 0811 0819 0827 0835 0843 0851 0859	4 0772 0780 0788 0796 0804 0812 0820 0828 0836 0844 0852 0860 0852	5 0773 0781 0789 0797 0805 0813 0821 0829 0837 0845 0853 0853 0853	6 0774 0782 0790 0798 0806 0814 0822 0830 0838 0846 0854 0854 0854	7 0775 0783 0791 0799 0807 0815 0823 0831 0839 0847 0855 0863 0863
1000   0.5 te t 1777   10 (Octal)   (Deci	12 o 23 imol)	1000 1010 1020 1030 1040 1050 1060 1070 1100 1110 1120 1130 1140	0 0512 0520 0528 0536 0544 0552 0560 0568 0576 0584 0592 0608 0616	1 0513 0521 0529 0537 0545 0553 0553 0569 0577 0585 0593 0601 0609 0617	2 0514 0522 0530 0538 0546 0554 0554 0570 0578 0586 0594 0610 0618	3 0515 0523 0531 0539 0547 0555 0563 0571 0579 0587 0595 0603 0611 0619	4 0516 0524 0532 0540 0548 0556 0564 0572 0580 0588 0596 0604 0612 0620	5 0517 0525 0533 0541 0549 0557 0565 0573 0581 0589 0597 0605 0613 0621	6 0518 0526 0534 0550 0558 0556 0574 0582 0598 0698 0698 0614 0622	7 0519 0527 0535 0543 0551 0559 0567 0575 0583 0591 0599 0607 0615 0623		1400 1410 1420 1430 1440 1460 1460 1470 1500 1510 1520 1530 1540 1550	0 0768 0776 0784 0792 0800 0808 0816 0824 0832 0840 0848 0856 0864 20872	1 0769 0777 0785 0793 0809 0817 0825 0833 0841 0849 0857 0865 0873	2 0770 0778 0786 0794 0802 0810 0818 0826 0834 0842 0850 0858 0856 0858	3 0771 0779 0787 0795 0803 0811 0819 0827 0835 0843 0851 0859 0867 0875	4 0772 0780 0788 0796 0804 0812 0828 0828 0836 0844 0852 0844 0852 0860 0868 0868	5 0773 0781 0789 0797 0805 0813 0821 0829 0837 0845 0853 0845 0853 0861 0869 0877	6 0774 0782 0790 0798 0806 0814 0822 0830 0838 0846 0854 0854 0854 0870 0878	7 0775 0783 0791 0799 0807 0815 0823 0831 0839 0847 0855 0863 0871 0879
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30000 3010 3020 3050 3050 3100 3120 3120 3120 3120 3220 32200 32200 3220 322	0 1536 1544 1552 1600 1568 1576 1584 1592 1600 1608 1624 1624 1624 1624 1648 1656 1664 1648 1656 1702 1720 1720 1728 1736 1744 1752 1760 1768	1 1537 1545 1553 1561 1569 1677 1585 1633 1641 1649 1657 1649 1657 1649 1657 1713 1721 1729 1727 1737 1745 1759	2 1538 1546 1554 1554 1554 1602 1610 1626 1634 1642 1650 1658 1666 1674 1682 1690 1698 1704 1722 1730 1738 1746	3 1539 1547 1555 1563 1571 1579 1675 1603 1611 1627 1635 1643 1659 1667 1659 1669 1707 1715 1723 1731 1739 1747 1755 1763	4 1540 1556 1556 1556 1580 1580 1580 1580 1580 1628 1630 1628 1630 1628 1640 1628 1640 1652 1660 1668 1676 1692 1700 1708 1770 1724 1732 1740 1748 1756	5 1549 1557 1555 1573 1589 1597 1605 1613 1629 1637 1645 1669 1677 1685 1693 1701 1701 1707 1717 1725 1733 1741 1749 1757 1657 1757 1657 1757 1657 1657 1657 1757 1657 1757 1657 1757 1657 1757 1657 1777 1757 1777 1757 1777 1757 1777 1757 1777 1757 1777 1757 1777 1777 1757 1777 1777 1757 1777 1777 1757 1777 1777 1757 1777 1777 1757 177	6 1542 1550 1558 1566 1574 1582 1590 1598 1606 1614 1622 1630 1638 1644 1662 1670 1678 1684 1702 1710 1718 1726 1734 1742 1750 1758	7 1543 1551 1559 1667 1615 1631 1639 1647 1655 1663 1671 1679 1685 1663 1703 1711 1719 1727 1735 1743 1751 1759	3400 3410 3422 3433 3440 3450 3510 3510 3550 3550 3550 3550 3550 35	0 1792 1800 1808 1816 1824 1832 1840 1848 1856 1864 1872 1880 1888 1994 1912 1920 1944 1952 1960 1944 1952 1960 1968 2066 2020 6 2024	1 1793 1801 1809 1817 1825 1833 1841 1849 1857 1865 1913 1921 1929 1937 1945 1953 1951 1953 1951 1953 1957 1957 1977 1985 1993 2001 2002	2 1794 1802 1810 1818 1826 1834 1834 1834 1834 1834 1834 1832 1850 1838 1866 1914 1922 1930 1934 1954 1954 1954 1954 1957 1958 1954 2002 2010 2018 2002	3 1795 1803 1811 1819 1827 1835 1843 1851 1859 1867 1973 1931 1937 1947 1955 1963 1971 1957 1963 2003 2011 2002	4 1796 1804 1812 1820 1828 1836 1844 1852 1860 1868 4876 1884 1892 1900 1908 1916 1924 1956 1956 1956 1956 2004 2012 2020	5 1797 1805 1813 1821 1823 1845 1853 1861 1865 1893 1901 1909 1917 1925 1933 1949 1957 1957 1958 1958 1981 1989 1981 1989 1987 1985 1981 1989 1987 1985 1987 1985 1987 1977 197	6 1798 1806 1814 1822 1830 1838 1846 1854 1862 1870 1870 1870 1870 1870 1870 1978 1960 1910 1918 1926 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1956 1957 1958 1958 1958 1958 1958 1958 1958 1958 1958 1958 1958 1958 1956 1958 2006 2014 2022 2030	7 1799 1807 1815 1823 1831 1839 1847 1855 1863 1871 1887 1903 1911 1919 1927 1935 1943 1951 1959 1967 1959 1967 1983 1991 1999 2007 2015	3000 to 3777 (Octal)	1536 to 2047 (Decimal)
30000 30100 30200 30500 30500 31000 31200 31300 31300 31300 31300 32100 32200 32300 3200 32300 32300 32300 3200 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 32300 3200 3000 3000 3000 30000 30000 300000000	0 1536 1544 1552 1560 1568 1576 1584 1592 1600 1608 1614 1624 1648 1656 1644 1656 1664 1672 1688 1696 1704 1712 1720 1728 1736 1744 1752 1768 1768 1768 1768 1776	1 1537 1545 1553 1561 1569 1609 1617 1625 1633 1641 1649 1657 1665 1673 1689 1697 1705 1713 1721 1729 1737 1745 1753 1761 1755 1775 1765 1769 1776 1769 1775 1769 1775 1769 1776 1769 1776 1769 1776 1769 1776 1769 1769 1776 1769 1776 1777 177	2 1538 1546 1554 1552 1570 1578 1586 1594 1602 1638 1662 1638 1662 1658 1666 1674 1688 1706 1714 1722 1730 1748 1746 1754 1770 1778	3 1539 1547 1555 1563 1571 1579 1587 1595 1603 1611 1627 1635 1643 1659 1667 1659 1667 1659 1669 1707 1715 1723 1731 1739 1747 1747 1747	4 1540 1546 1556 1556 1564 1572 1588 1596 1604 1612 1628 1636 1644 1652 1644 1650 1668 1664 1660 1668 1700 1708 1710 1724 1730 1748 1756	5 1541 1541 1557 1565 1573 1589 1589 1589 1589 1613 4621 16453 1653 1653 1661 1669 1677 1685 1693 1701 1709 1717 1725 1733 1741 1749 1757 1749 1757 1757 1741 1749 1757 1749 1773 1781	6 1542 1550 1558 1556 1574 1582 1590 1598 1606 1614 1622 1630 1638 1646 1654 1662 1702 1710 1718 1726 1734 1750 1758 1754 1754 1754	7 1543 1559 1567 1575 1583 1591 1599 1607 1615 1623 1631 1639 1645 1663 1663 1667 1667 1663 1703 1711 1719 1727 1743 1751 1759 1775 1783	3400 3410 3422 3433 3440 3500 3510 3520 3550 3560 3560 3560 3610 3620 3640 3650 3640 3650 3660 3650 3660 3700 3710 3720 3730 3740 3720 3730	0 1792 1800 1808 1816 1824 1832 1840 1832 1840 1832 1840 1848 1856 1864 1878 1944 1912 1920 1944 1952 1960 1968 1976 1988 1976 1988 1976	1 1793 1801 1809 1817 1825 1833 1841 1849 1857 1865 1873 1841 1849 1857 1865 1973 1913 1921 1929 1953 1953 1953 1953 1957 1953 2001 2009 2017 2025 2023	2 1794 1802 1810 1818 1826 1834 1842 1850 1858 1866 1898 1906 1914 1922 1930 1938 1946 1954 1954 1954 1957 1978 1984 2002 2010 2018	3 1795 1803 1811 1819 1827 1835 1843 1851 1859 1867 1879 1935 1907 1915 1923 1931 1937 1947 1955 1963 1979 1987 1957 2003 2011 2019	4 1796 1804 1812 1820 1828 1836 1844 1852 1860 1948 1972 1940 1948 1956 1956 1956 1956 1956 2004 2028 2028	5 1797 1805 1813 1821 1823 1845 1853 1861 1869 <del>18</del> 7 1885 1893 1901 1909 1997 1957 1957 1957 1957 1957 2005 2013 2029 2037	6 1798 1806 1814 1822 1830 1838 1846 1854 1862 1870 1870 1876 1870 1876 1876 1876 1974 1958 1958 1958 1956 1974 1958 2006 2030 2038 2030 2038 2030 2038 105	7 1799 1807 1815 1823 1831 1839 1847 1855 1863 1871 1855 1903 1911 1919 1927 1935 1943 1951 1959 1959 1967 1958 1959 1959 2007 2015 2023 2031 2039	3000 to 3777 (Octal)	1536 to 2047 (Decimal)

### OCTAL-DECIMAL INTEGER CONVERSION TABLE

		0	1	2	3	4	5	6	7			0	1	2	3	4	5	6	7
	4000	2048	2049	2050	2051	2052	2053	2054	2055	1	4400	2304	2305	2306	2307	2308	2309	2310	2311
4000 2048	4010	2056	2043	2058	2051	2060	2061	2062	2063		4410	2312	2313	2314	2315	2316	2317	2318	2319
to to	4020	2064	2065	2066	2067	2068	2069	2070	2071		4420	2320	2321	2322	2323	2324	2325	2326	2327
4/// 2559 (Octal) (Decimal)	4030	2072	2073	2074	2075	2076	2077	2078	2079		4430	2328	2329	2330	2331	2332	2333	2334	2335
(Ocidi) ( (Deciliar)	4040	2080	2081	2082	2083	2084	2085	2086	2087		4440	2336	2337	2338	2339	2340	2341	2342	2343
	4050	2088	2089	2090	2091	2092	2093	2094	2095		4450	2344	2345	2346	2347	2348	2349	2350	2351
Octal Decimal	4060	2096	2097	2098	2099	2100	2101	2102	2103		4460	2352	2353	2354	2355	2356	2357	2358	2359
10000 - 4096	4070	2104	2105	2106	2107	2108	2109	2110	2111		4470	2360	2361	2362	2363	2364	2365	2366	2367
20000 - 8192	1				0115	0110	0117	9110	0110		45.00	1200	2260	9970	0271	9979	9979	9974	1275
30000 - 12288	4100	2112	2113	2114	2115	2110	2117	2110	2119		4510	2300	2309	2370	2371	2380	2313	2314	2313
40000 - 16384	4110	2120	2121	2122	2123	2124	2123	2120	2121		4520	2384	2385	2386	2387	2388	2389	2302	2303
50000 - 20480	4120	2120	2129	2130	2130	2132	2100	2142	2143		4530	2392	2393	2394	2395	2396	2397	2398	2399
70000 - 24370	4140	2144	2145	2146	2147	2148	2149	2150	2151		4540	2400	2401	2402	2403	2404	2405	2406	2407
/0000 - 288/2	4150	2152	2153	2154	2155	2156	2157	2158	2159		4550	2408	2409	2410	2411	2412	2413	2414	2415
	4160	2160	2161	2162	2163	2164	2165	2166	2167		4560	2416	2417	2418	2419	2420	2421	2422	2423
	4170	2168	2169	2170	2171	2172	2173	2174	2175		4570	2424	2425	2426	2427	2428	2429	2430	2431
	4200	2176	2177	2178	2179	2180	2181	2182	2183		4600	2432	2433	2434	2435	2436	2437	2438	2439
	4210	2184	2185	2186	2187	2188	2189	2190	2191		4610	2440	2441	2442	2443	2444	2445	2446	2447
	4220	2192	2193	2194	2195	2196	2197	2198	2199		4620	2448	2449	2450	2451	2452	2453	2454	2455
	4230	2200	2201	2202	2203	2204	2205	2206	2207		4630	2456	2457	2458	2459	2460	2461	2462	2463
	4240	2208	2209	2210	2211	2212	2213	2214	2210		4650	2404	2400 9279	2400 9474	2401 9475	2400 2476	2409	241U 2479	24/1
	4250	2216	2217	2210	2219	2220	2221	2222	2223		4660	2412	2473	2414	2413	2410	2411	2470	2419
	4200	2224	2223	2220	2221	2220	22237	2238	2239		4670	2488	2489	2490	2491	2492	2493	2400	2495
	4210	2232	2233	2234	2200	2250	2201	2200	2200		1010	2100	2405	2100	2 10 1	2152	2450	2101	2100
	4300	2240	2241	2242	2243	2244	2245	2246	2247		4700	2496	2497	2498	2499	2500	2501	2502	2503
	4310	2248	2249	2250	2251	2252	2253	2254	2255		4710	2504	2505	2506	2507	2508	2509	2510	2511
	4320	2256	2257	2258	<b>2</b> 259	2260	2261	2262	2263		4720	2512	2513	2514	2515	2516	2517	2518	2519
	4330	2264	2265	2266	2267	2268	2269	2270	2271		4730	2520	2521	2522	2523	2524	2525	2526	2527
	4340	2272	2273	2274	2275	2276	2277	2278	2279		4740	2528	2529	2530	2531	2532	2533	2534	2535
	4350	2280	2281	2282	2283	2284	2285	2286	2287		4750	2536	2537	2538	2539	2540	2541	2542	2543
	4360	2288	2289	2290	2291	2292	2293	2294	2295		4760	2544	2545	2546	2547	2548	2549	2550	2551
	4370	2296	2297	2298	2299	2300	2301	2302	2303	J	4770	2552	2553	2554	2555	2556	2557	2558	2559
		0	1	 o	3		 5	6	7			0		 2			5	6	7
		0	1	2	3	4	5	6	7			0	1	2	3	4	5	6	7
5000 2540	5000	0 2560	1 2561	2 2562	3 2563	4 2564	5 2565	6 2566	7 2567		5400	0 2816	1 2817	2 2818	3 2819	4 2820	5	6 2822	7 2823
5000 2560	5000 5010	0 2560 2568	1 2561 2569	2 2562 2570	3 2563 2571	4 2564 2572	5 2565 2573	6 2566 2574	7 2567 2575		5400 5410	0 2816 2824	1 2817 2825	2 2818 2826	3 2819 2827	4 2820 2828	5 2821 2829	6 2822 2830	7 2823 2831
5000 2560 to to 5777 3071	5000 5010 5020	0 2560 2568 2576	1 2561 2569 2577	2 2562 2570 2578	3 2563 2571 2579	4 2564 2572 2580	5 2565 2573 2581	6 2566 2574 2582	7 2567 2575 2583		5400 5410 5420	0 2816 2824 2832	1 2817 2825 2833	2 2818 2826 2834	3 2819 2827 2835	4 2820 2828 2836	5 2821 2829 2837	6 2822 2830 2838	7 2823 2831 2839
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030	0 2560 2568 2576 2584	1 2561 2569 2577 2585	2 2562 2570 2578 2586	3 2563 2571 2579 2587	4 2564 2572 2580 2588	5 2565 2573 2581 2589	6 2566 2574 2582 2590	7 2567 2575 2583 2591		5400 5410 5420 5430	0 2816 2824 2832 2840	1 2817 2825 2833 2841	2 2818 2826 2834 2842	3 2819 2827 2835 2843	4 2820 2828 2836 2844	5 2821 2829 2837 2845	6 2822 2830 2838 2846	7 2823 2831 2839 2847
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030 5040	0 2560 2568 2576 2584 2592	1 2561 2569 2577 2585 2593	2 2562 2570 2578 2586 2594	3 2563 2571 2579 2587 2595	4 2564 2572 2580 2588 2596	5 2565 2573 2581 2589 2597	6 2566 2574 2582 2590 2598	7 2567 2575 2583 2591 2599		5400 5410 5420 5430 5440	0 2816 2824 2832 2840 2848	1 2817 2825 2833 2841 2849	2 2818 2826 2834 2842 2850	3 2819 2827 2835 2843 2851	4 2820 2828 2836 2844 2852	5 2821 2829 2837 2845 2853	6 2822 2830 2838 2846 2854	7 2823 2831 2839 2847 2855
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030 5040 5040	0 2560 2568 2576 2584 2592 2600	1 2561 2569 2577 2585 2593 2601	2 2562 2570 2578 2586 2594 2602	3 2563 2571 2579 2587 2595 2603	4 2564 2572 2580 2588 2596 2604	5 2565 2573 2581 2589 2597 2605	6 2566 2574 2582 2590 2598 2606	7 2567 2575 2583 2591 2599 2697		5400 5410 5420 5430 5440 5450	0 2816 2824 2832 2840 2848 2856	1 2817 2825 2833 2841 2849 2857	2 2818 2826 2834 2842 2850 2858	3 2819 2827 2835 2843 2851 2859	4 2820 2828 2836 2844 2852 2860	5 2821 2829 2837 2845 2853 2853 2861	6 2822 2830 2838 2846 2854 2854 2862	7 2823 2831 2839 2847 2855 2863
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030 5040 5050 5060	0 2560 2568 2576 2584 2592 2600 2608	1 2561 2569 2577 2585 2593 2601 2609	2 2562 2570 2578 2586 2594 2602 2610	3 2563 2571 2579 2587 2595 2603 2611	4 2564 2572 2580 2588 2596 2604 2612	5 2565 2573 2581 2589 2597 2605 2613	6 2566 2574 2582 2590 2598 2606 2614	7 2567 2575 2583 2591 2599 2607 2615		5400 5410 5420 5430 5440 5450 5460	0 2816 2824 2832 2840 2848 2856 2864	1 2817 2825 2833 2841 2849 2857 2865	2 2818 2826 2834 2842 2850 2858 2866	3 2819 2827 2835 2843 2851 2859 2867	4 2820 2828 2836 2844 2852 2860 2868	5 2821 2829 2837 2845 2853 2853 2861 2869	6 2822 2830 2838 2846 2854 2854 2862 2870	7 2823 2831 2839 2847 2855 2863 2871
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030 5040 5050 5060 5070	0 2560 2568 2576 2584 2592 2600 2608 2616	1 2561 2569 2577 2585 2593 2601 2609 2617	2 2562 2570 2578 2586 2594 2602 2610 2618	3 2563 2571 2579 2587 2595 2603 2611 2619.	4 2564 2572 2580 2588 2596 2604 2612 2620	5 2565 2573 2581 2589 2597 2605 2613 2621	6 2556 2574 2582 2590 2598 2606 2614 2622	7 2567 2575 2583 2591 2599 2607 2615 2623		5400 5410 5420 5430 5440 5450 5460 5460	0 2816 2824 2832 2840 2848 2856 2864 2872	1 2817 2825 2833 2841 2849 2857 2865 2873	2 2818 2826 2834 2842 2850 2858 2866 2874	3 2819 2827 2835 2843 2851 2859 2867 2875	4 2820 2828 2836 2844 2852 2860 2868 2876	5 2821 2829 2837 2845 2853 2861 2869 2877	6 2822 2830 2838 2846 2854 2854 2862 2870 2878	7 2823 2831 2839 2847 2855 2863 2871 2879
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030 5040 5050 5060 5060 5070	0 2560 2568 2576 2584 2592 2600 2608 2616 2624	1 2561 2569 2577 2585 2593 2601 2609 2617 2625	2 2562 2570 2578 2586 2594 2602 2610 2618 2626	3 2563 2571 2579 2587 2595 2603 2611 2619, 2627	4 2564 2572 2580 2588 2596 2604 2612 2620 2628	5 2565 2573 2581 2589 2597 2605 2613 2621 2629	6 2566 2574 2582 2590 2598 2606 2614 2622 2630	7 25567 2575 2583 2591 2599 2607 2615 2623 2621		5400 5410 5420 5430 5440 5450 5460 5470	0 2816 2824 2832 2840 2848 2856 2864 2872 2872	1 2817 2825 2833 2841 2849 2857 2865 2873 2873	2 2818 2826 2834 2842 2850 2858 2866 2874	3 2819 2827 2835 2843 2851 2859 2867 2875	4 2820 2828 2836 2844 2852 2860 2868 2876	5 2821 2829 2837 2845 2853 2861 2869 2877	6 2822 2830 2838 2846 2854 2854 2862 2870 2878	7 2823 2831 2839 2847 2855 2863 2871 2879
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030 5040 5050 5060 5070 5100	0 2560 2568 2576 2584 2592 2600 2608 2616 2624 2632	1 2561 2569 2577 2585 2593 2601 2609 2617 2625 2633	2 2562 2570 2578 2586 2594 2602 2610 2618 2626 2634	3 2563 2571 2579 2587 2595 2603 2611 2619, 2627 2635	4 2564 2572 2580 2588 2596 2604 2612 2620 2628 2628 2636	5 2565 2573 2581 2589 2597 2605 2613 2621 2629 2637	6 2566 2574 2582 2590 2598 2606 2614 2622 2630 2638	7 2567 2575 2583 2591 2599 2607 2615 2623 2631 2639		5400 5410 5420 5430 5440 5450 5460 5470 5500 5510	0 2816 2824 2832 2840 2848 2856 2864 2872 2880 2888	1 2817 2825 2833 2841 2849 2857 2865 2873 2873 2881 2880	2 2818 2826 2834 2842 2850 2858 2866 2874 2882 2882	3 2819 2827 2835 2843 2851 2859 2867 2875 2875 2883 2891	4 2820 2828 2836 2844 2852 2860 2868 2876 2884 2892	5 2821 2829 2837 2845 2853 2861 2869 2877 2885 2893	6 2822 2830 2838 2846 2854 2862 2870 2878 2886 2886	7 2823 2831 2839 2847 2855 2863 2871 2879 2887 2895
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030 5050 5060 5070 5100 5110	0 2560 2568 2576 2584 2592 2600 2608 2616 2624 2632 2640	1 2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641	2 2562 2570 2578 2586 2594 2602 2610 2618 2626 2634 2626 2634 2642	3 2563 2571 2579 2587 2595 2603 2611 2619. 2627 2635 2643	4 2564 2572 2580 2588 2596 2604 2612 2620 2628 2636 2644	5 2565 2573 2581 2589 2597 2605 2613 2621 2629 2637 2645	6 2566 2574 2582 2590 2598 2606 2614 2622 2630 2638 2646	7 2567 2575 2583 2591 2599 2607 2615 2623 2631 2639 2647		5400 5410 5420 5430 5440 5460 5460 5470 5500 5510 5520	0 2816 2824 2832 2840 2848 2856 2864 2872 2880 2888 2888 2886	1 2817 2825 2833 2841 2849 2857 2865 2873 2881 2889 2897	2 2818 2826 2834 2842 2850 2858 2866 2874 2882 2890 2898	3 2819 2827 2835 2843 2851 2859 2867 2875 2883 2891 2899	4 2820 2828 2836 2844 2852 2860 2868 2876 2884 2892 2900	5 2821 2829 2837 2845 2853 2861 2869 2877 2885 2893 2901	6 2822 2830 2838 2846 2854 2862 2870 2878 2886 2894 2894 2902	7 2823 2831 2839 2847 2855 2863 2871 2879 2887 2895 2903
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5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5030 5050 5060 5070 5100 5120 5130 5130 5130 5170 5220 5220 5220 5220 5220 5220 5220 52	0 25560 25568 25766 2584 2592 2600 2608 2616 2624 2632 2646 2652 2666 2658 2666 2688 2696 2704 2712 2720 2778 27760 27784	1 2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2641 2667 2665 2673 2681 2689 2697 2705 2713 2729 2705 2713 2729 2737 2745	2 2562 2570 2578 2586 2594 2602 2618 2624 2658 2664 2658 2666 2674 2682 2666 2698 2706 2698 2706 2714 2732 2738 27746	3 2563 2571 2577 2595 2603 2611 2619 2627 2633 2643 2651 2667 2675 2663 2667 2675 2663 2705 2715 2715 2773 27747 27755 27787 27787	4 2564 2572 2580 2682 2692 2620 2628 2636 2636 2636 2636 2636 2636 2636	5 2565 2573 2581 2587 2605 2613 2621 2629 2637 2645 2653 2669 2677 2685 2669 2701 2709 2717 2725 2733 2741 2749 2757 2755 2773 2789	6 25566 25574 2582 2590 2614 2622 2638 2646 2654 2654 2667 2678 2668 2694 2710 2710 2712 2712 2712 2712 2742 2755 2758 2756 2774 2775	7 2567 2575 2583 2591 2607 2615 2623 2631 2639 2647 2055 2663 2671 2679 2687 2679 2687 2703 2711 2719 2727 2743 2751 2759 2767 2775 2785		5400 5410 5420 5430 5440 55470 5510 5520 5550 5550 5550 5550 5550 555	0 2816 2824 2832 2848 2856 2864 2872 2888 2900 2928 2920 2928 2930 2928 2936 2968 2976 2968 2976 2984 2952 2968 2976 3000 3008 3016 3023 3040	1 2817 2825 2833 2841 2849 2857 2865 2873 2887 2905 2913 2929 2937 2929 2937 2945 2953 2969 2977 2965 2977 2969 2977 2965 2969 2977 2965 2969 2977 2965 2969 2977 2965 2969 2977 2965 2969 2977 2965 2969 2977 2965 2977 2965 2977 2965 2977 2969 2977 2969 2977 2969 2977 2969 2977 2975 2977 2975 3000 3000 3003 3033 3041	2 2818 2826 2834 2842 2850 2858 2858 2858 2858 2954 2922 2930 2938 2946 2954 2954 2954 2970 2978 2980 2970 2978 3002 3010 3018 3024	3 2819 2827 2835 2843 2851 2859 2867 2875 2883 2891 2917 2915 2923 2931 2939 2947 2955 2971 2979 2987 3003 3011 3019 3027 3035 3043	4 28200 2828 2836 2844 2852 2860 2956 2914 2932 2940 2948 2956 2954 2956 2972 2980 2972 2980 2972 2980 3004 3012 3020 3028 3036 3034	5 2821 2829 2837 2845 2853 2861 2909 2917 2925 2933 2941 2957 2957 2965 2973 2981 2989 2957 3005 3013 3021 3021	6 2822 2830 2838 2846 2854 2854 2854 2982 2910 2918 2926 2934 2926 2934 2942 2950 2958 2956 2954 2954 2956 2954 2956 3006 3014 3022 3030 3038 3046	7 2823 2831 2839 2847 2855 2863 2977 2935 2943 2951 2959 2975 2983 2995 2975 2983 2995 3007 3015 3039 3039 3047
5000 2560 to to 5777 3071 (Octal) (Decimal)	5000 5010 5020 5040 5050 5060 5070 5100 5120 5120 5140 5170 5200 5210 5220 5240 5250 5240 5250 5240 5250 5240 5250 5240 5230 5240 5250 5240 5250	0 2560 2568 2576 2584 2592 2600 2608 2616 2624 2642 2642 2642 2642 2642 2642	1 2561 2569 2577 2585 2593 2601 2609 2617 2625 2633 2640 2657 2663 2663 2663 2673 2663 2713 2771 2729 2737 2745 2745 2753 2745 2753 2769 2775 2793 2793	2 2562 2570 2578 2586 2594 2602 2618 2626 2638 2664 2634 2658 2664 2658 2664 2658 2664 2658 2664 2658 2664 2658 2664 2658 2664 2674 2674 2774 27754 2776 27786 2784	3 2563 2571 2577 2595 2603 2611 2619. 2627 2633 2651 2659 2667 2683 2699 2707 2715 2723 2733 2731 2739 2747 2747 2745 2747	4 2564 2572 2580 2588 2596 2664 2620 2628 2634 2632 2668 2668 2668 2668 2668 2668 2700 2708 2716 2724 2730 2774 2732 2740 2748 2776 2788 2796	5 2565 2573 2581 2589 2605 2613 2621 2629 2635 2669 2669 2701 2705 2717 2705 2717 2717 2717 2717 2717 2717 2717 271	6 2566 2574 2582 2590 2606 2614 2622 2630 2638 2662 2670 2678 2662 2670 2710 2718 2776 2774 2772 2758 2756 2774 2758	7 25677 2583 25911 2599 26077 2615 2623 2631 2633 26477 2655 2663 26647 2679 2687 2679 2687 2703 2711 2719 2727 2733 2751 2759 2767 2775 27783		5400 5410 5420 5430 5440 5540 55470 5500 5550 5550 5550 55	0 2816 2824 2832 2840 2848 2856 2864 2912 2920 2928 2928 2928 2928 2928 2936 2952 2968 2994 2995 2968 2996 2996 2996 3000 3008 3016 3024 3048	1 2817 2825 2833 2841 2857 2865 2873 2867 2905 2913 2929 2937 2925 2929 2937 2945 2969 2977 2965 2969 2977 2965 3001 3009 3001 3009	2 2818 2826 2834 2842 2850 2858 2858 2858 28574 2898 2994 2992 2930 2938 2994 2954 2954 2954 2954 29970 29978 2998 2994 3002 3010 3002 3018 3026 3034 2054	3 2819 2827 2835 2843 2859 2867 2875 2883 2891 2937 2915 2923 2931 2939 2947 2955 2963 2971 2979 2987 2979 2987 3003 3011 3027 3033 3011	4 28200 2828 28366 2844 2852 2860 2852 2860 2952 2900 2916 2924 2932 2932 2932 2932 2940 2948 2956 2956 2956 2956 2956 2958 3004 3012 3028 30364 3052	5 2821 2829 2837 2845 2853 2861 2869 2937 2925 2933 2941 2949 2957 2981 2989 2997 3005 3013 3029 3037 3029	6 2822 2830 2838 2846 2854 2862 2870 2878 2886 2894 2990 29918 2992 29918 2992 2994 2994 2994 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 2994 29950 29950 29954 29950 29954 20054 200555 200555 2005555 2005555555555	7 2823 2831 2839 2847 2855 2863 2951 2993 2993 2993 29943 2951 2959 29957 29953 29943 29959 29959 29959 29959 29959 29959 29959 29950 29951 29959 29951 29955 29955 29955 29955 29955 29955 29955 29957 200777 20077 20077 20077 200777 20077 20077 20077 200777 200777 20077
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### OCTAL-DECIMAL INTEGER CONVERSION TABLE

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		0	1	2	3	4	5	6	7	1		0	1	2	3	4	5 ·	6	7.		
	6000	2070	207	0 007	4 207	- 0.07					6100		2000		2221	2220			2005		
	6010	3080	2 307. 3081	3 307 1 308	4 307 2 308	5 301 3 308	6 307 4 308	7 307 5 308	5 3079 5 3087		6410	) 3336	3337	3338	3339	3340	3341	3342	3343	6000	3072
	6020	3088	3089	309	0 309	1 309	2 309	3 309-	4 3095		6420	3344	3345	3346	3347	3348	3349	3350	3351	6777	3583
	6030 6040	3104	5 3097	7 309	8 3099 6 310'	9 310 7 310	0 310 8 310	1 310:	2 3103		6430	3352	3353	3354	3355	3356	3357	3358	3359	(Octal)	(Decimal)
	6050	3112	2 3113	3 311	4 311:	5 311	6 311	7 3118	3 3119		6450	3368	3369	3370	3371	3372	3373	3374	3375		
	6060	3120	3121	312	2 312	3 312	4 312	5 3126	3127		6460	3376	3377	3378	3379	3380	3381	3382	3383	Octal	Decimal
	6010	3128	3129	313	0 313	1 313	2 313	3 3134	1 3135		6470	3384	3385	3386	3387	3388	3389	3390	3391	10000 -	4096
	6100	3136	3137	3138	3139	3140	314	3142	3143		6500	3392	3393	3394	3395	3396	3397	3398	3399	20000 -	8192
	6110	3144	3145	5 3146	5 3147	7 3148	3 3149	3150	3151		6510	3400	3401	3402	3403	3404	3405	3406	3407	40000 -	16384
1	6130	3160	3155	3162	$\frac{1}{2}$ 3163	3130	3165	5 3158 5 3166	3159		6530	3408	3409	3410	3411	3412	3413	3414	3415 3423	.50000 -	20480
	6140	3168	3169	3170	3171	3172	3173	3174	3175		6540	3424	3425	3426	3427	3428	3429	3430	3431	60000 -	24576
	6150 6160	3176	3177	3178	3179 3187	) 3180 7 3189	) 3181	3182	3183		6550	3432	3433	3434	3435	3436	3437	3438	3439	/0000 -	20072
	6170	3192	3193	3194	3195	5196	5 3197	3190	3191		6570	3448	3449	3450	3451	3452	3445	3440	3455		
	6900	2200	2001	2200	2000		0005					0450	0.158								
	6210	3200	3201	3202	3203	3204	3205	3206	3207		6610	3456	3457 3465	3458	3459	3460	3461 3469	3462 3470	3463		
	6220	3216	3217	3218	3219	3220	3221	3222	3223		6620	3472	3473	3474	3475	3476	3477	3478	3479		
1	6230	3224	3225	3226	3227	3228	3229	3230	3231		6630	3480	3481	3482	3483	3484	3485	3486	3487		
	6250	3240	3241	3242	3235	3230	3237	3238	3239		6650	3488	3489	3490	3491	3492	3493	3494	3495		
1	6260	3248	3249	3250	3251	3252	3253	3254	3255		6660	3504	3505	3506	3507	3508	3509	3510	3511		
ľ	6270	3256	3257	3258	3259	3260	3261	3262	3263		6670	3512	3513	3514	3515	3516	3517	3518	3519		
	6300	3264	<b>326</b> 5	3266	3267	3268	3269	3270	3271		6700	3520	3521	3522	3523	3524	3525	3526	3527		
f	5310	3272	3273	3274	3275	3276	3277	3278	3279		6710	3528	3529	3530	3531	3532	3533	3534	3535		
4	5320 - 5330 -	3280	3281	3282	3283	3284	3285	3286	3287		6720	3536	3537	3538	3539	3540	3541	3542	3543		
ie	5 <b>34</b> 0	3296	3297	3298	3299	3300	3301	3302	3303		6740	3552	3553	3554	3555	3556	3557	3558	3559		
6	5350   200	3304	3305	3306	3307	3308	3309	3310	3311		6750	3560	3561	3562	3563	3564	3565	3566	3567		
6	5370	3320	3321	3322	3323	3324	3325	3326	3327		6770	3576	3569	3570	3571	3572	3573	3574	3575		
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$\begin{array}{c} 70\\ 70\\ 70\\ 70\\ 70\\ 70\\ 70\\ 70\\ 70\\ 70\\$	0000 : 0200 :	0 3584 3592 3600 3608 3608 3624 3632 3640 3656 3664 3656 3664 3656 3668 3656 3668 3656 3668 3704 3712 3720 3728 3720 3728 3724 3726 3768 3768 3768 3768 3768 3768 3768 376	1 3585 3593 3601 3609 3617 3625 3633 3641 3669 3657 3665 3667 3705 3705 3705 3713 3721 3729 3737 3745 3745 3769 3777 3785	2 3586 3594 3602 3610 3618 3626 3634 3652 3654 3658 3664 3658 3664 3698 3668 3690 3698 3674 3778 3778 3778 3776 3778	3 3587 3595 3603 3611 3619 3627 3643 3651 36659 3663 36651 36693 3667 3683 3691 3699 3707 3715 3707 3715 3771 3739 3747 37771 3775	4 3588 3596 3604 3612 3628 3664 3668 3664 3668 3664 3668 3700 3708 3708 3708 3774 3732 3748 3775 3748 3775 3748 3776 3788 3776	5 3589 3597 3605 3613 3629 3663 3663 36645 3663 36645 3663 3667 3685 3693 3709 3717 3725 3733 3749 3757 3749 3757 3749 3797 3805	6 3590 3598 3606 3614 3632 3630 3638 3646 3654 3664 3654 3673 3702 3718 3710 3718 3726 3734 3743 3750 3753 3756 3774 3775 3776	7 3591 3599 3607 3623 3631 3639 3647 3655 3663 3671 3655 3703 3771 3779 3771 3775 3743 3751 3759 3751 3759 3767 3775 3775 3775 3775		7400 7410 7420 7430 7440 7450 7460 7510 7550 7550 7550 7550 7550 7550 755	0 3840 3848 3856 3864 3872 3880 3988 3988 3992 3928 3928 3928 3928 3928	1 3841 3849 3857 3865 3873 3889 3913 3929 3937 3945 3953 3961 3969 3977 3985 3963 3969 3977 3985 3969 3977 3985 3969 3977 3985 3969 3977 3985 3969 3977 3985 3969 3977 3985 3969 3977 3985 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3985 3961 3969 3977 3965 3961 3967 3965 3977 3965 3961 3977 3965 3961 3977 3965 3961 3977 3965 3961 3977 3965 3961 3977 3965 3961 3977 3965 3961 3977 3965 3961 3977 3965 3961 3977 3965 3977 3965 3977 3965 3977 3965 3977 3965 3977 3975 3967 3975 3977 3975 3977 3975 3977 3975 3977 3975 3977 3975 3977 3975 3977 3975 3977 3975 3977 3975 3977 3975 3977 3977 3975 39777 3977 3977 3977 3977 3977 3977 3977 3977 3977 3977 39	2 3842 3850 3858 3866 3874 3890 3914 3922 3930 3938 3946 3934 3946 3954 3962 3970 3978 3962 3970 3978 3964 4002 3978 3968 3968 3968 3978 3968 3978 3968 3978 3968 3978 3968 3978 3968 3978 3968 3978 3968 3978 3978 3968 3978 3978 3978 3968 3978 3968 3978 3968 3978 3968 3978 3968 3978 3978 3968 3978 3978 3978 3978 3978 3978 3978 3978 3978 3978 3978 4002 400	3 3843 3859 3867 3875 3883 3883 3883 3931 3939 3947 3935 3947 3955 3963 3971 3963 3971 3963 3979 3963 3971 3963 3979 3963 3971 3959 3963 3973 3963 3974 3969 3963 3974 3965 3963 3974 3965 3963 3974 3965 3963 3974 3965 3965 3975 3965 3967 3965 3967 3965 3975 3965 3967 3965 3967 3965 3975 3965 3967 3965 3967 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3977 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3965 3975 3955 3975 3955 3975 3955 3975 3955 3975 3955 3975 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 3957 3955 395	4 3844 3852 3860 3868 3876 3884 3912 3990 3998 3992 3940 3932 3940 3942 3940 3943 3956 3954 3956 3964 3956 3964 3956 3964 3956 3960 3968 3956 3960 3968 3972 3960 3968 3969 3968 3972 3960 3968 3969 3968 3972 3960 3968 3969 3968 3972 3960 3968 3969 3968 3972 3960 3968 3969 3968 3969 3972 3960 3968 3969 3968 3972 3960 3968 3966 3968 3972 3960 3968 3969 3968 3972 3960 3968 3966 3968 3972 3960 3968 3966 3968 3972 3968 3966 3968 3966 3968 3972 3968 3966 3968 3966 3968 3972 3968 396	5 3845 3853 3861 3869 3877 3925 3933 3941 3949 3957 3945 3941 3949 3957 3965 3973 3965 3973 3965 3973 3967 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3967 3973 3973	6 3846 3854 3862 3870 3878 3902 3910 3918 3926 3934 3934 3934 3934 3958 3934 3958 3958 3958 3966 3974 4014 4002 4006 4014 4054 4054	7 3847 3855 3863 3863 3871 3895 3995 3993 3935 3943 3955 3943 3955 3967 3975 3967 3975 3967 3991 3999 4007 4015 4003	7000 to 7777 (Octal)	3584 to 4095 (Decimal)
$\begin{array}{c} 7\\ 7\\ 7\\ 7\\ 7\\ 7\\ 7\\ 7\\ 7\\ 7\\ 7\\ 7\\ 7\\ $	0000 : 0200 :	0 3584 3592 3600 3608 3616 3624 3632 3640 3656 3654 3656 3664 3656 3668 3656 3668 3672 3680 3768 3712 3728 3728 3728 3728 3728 3728 3728 3728 3728 3728 3768 3728 3768 3778 3768 3778 3768 3778 3768 3778 3768 377	1 3585 3593 3601 3609 3617 3625 3633 3641 3669 3697 3705 3713 3721 3729 3737 3745 3753 3745 3753 3745 3775 3745 3775 377	2 3586 3594 3602 3610 3618 3626 3634 3662 3658 3664 3658 3664 3668 3668 3668 3668 3668 3674 3688 3674 3770 3778 3776 3776 3778 3776 3778	3 3587 3595 3603 3611 3619 3627 3643 3651 3659 3663 3663 3669 3667 3663 3691 3699 3707 3715 3773 3771 3775 3773 3771 3775 3771 3777 3777	4 3588 3596 3604 3612 3620 3664 3668 3664 3668 3664 3668 3676 3684 3700 3708 3708 3708 3776 3774 3772 3780 3778 37780 37780 37780 37780 37780 37780 37780 37780 37780 3789 3796	5 3589 3597 3605 3613 3629 3667 3665 3663 3667 3665 3693 3709 3717 3765 3773 3775 3775 3775 3775 3773 3775 3773 3774 3775 3773 3774 3775 3773 3781 3789 3797 3805	6           35590           35598           3606           3614           3623           3638           3646           3654           3653           3664           3654           3658           3678           3678           3678           3678           3673           3710           3718           3770           3753           3776           3778           3798           3806           3814	7 3591 3599 3607 3623 3631 3639 3647 3655 3663 3671 3655 3703 3771 3775 3775 3775 3775 3775 3775 377		7400 7410 7420 7430 7450 7460 7510 7550 7550 7550 7550 7550 7550 7560 7660 76	0 3840 3843 3856 3856 3864 3872 3880 3988 3992 3928 3944 4000 4002 4000 4002 4000 4002 4000 4002 4000 4008 4007 4008 4008 4008 4007 4008 4007 4008 40777 40777 40777 40777 4077777 407777777777	1 3841 3849 3857 3865 3873 3889 3997 3905 3929 3929 3937 3945 3953 3961 3969 3977 3985 3969 3977 3985 3969 3977 4025 4001 4007 4025 4001 4025 4025 4027 4025 4027 3077 3085 3077 3085 3087 3087 3097 3095 3097 4001 4001 4007 4007 40777 4077 40777 4077 4077 4077 4077 4077 4077 4077 4077 4	2 3842 3850 3858 3866 3874 3890 3914 3922 3930 3930 3938 3946 3954 3962 3970 3978 3962 3970 3978 3964 4010 4012 4010 4024 4010 4025 4010 4026 40566 4056 4056 40566 4056 4056 4056 4056 4056 4056 4056 4	3 3843 3859 3867 3875 3883 3899 3907 3915 3923 3931 3939 3947 3955 3963 3971 3979 3963 3979 3963 3971 3975 4003 4011 4019 4027 405 405 405 405 405 405 405 405	4 3844 3852 3860 3868 3876 3884 3892 3900 3908 3912 3932 3940 3940 3942 3940 3943 3956 3954 3956 3964 4020 4000 4020 400	5 3845 3853 3861 3869 3877 3925 3933 3941 3949 3957 3945 3957 3941 3949 3957 3965 3973 3965 3973 3967 3977 397	6 3846 3854 3862 3870 3878 3926 3910 3918 3926 3934 3934 3958 3934 3958 3958 3958 3974 3966 3990 3998 3990 3998 4006 4006 4006 4006 4006 4006 4006 400	7 3847 3855 3863 3863 3871 3879 3903 3911 3919 3927 3935 3943 3955 3943 3955 3943 3957 3967 3975 3967 3963 3991 3999 4007 4015 4023 4007 4015 4065 4065 4065 4065 4070	7000 to 77777 (Octal)	3584 to 4095 (Decimal)
$\begin{array}{c} 770\\ 770\\ 770\\ 770\\ 770\\ 770\\ 770\\ 770$	0000 : 0200 : 0300 :	0 3584 3592 3600 3608 3616 3624 3664 36556 3664 36556 3664 3656 36656 3664 3656 36672 36680 36683 3656 3672 36680 3764 3712 3728 3744 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 3766 37764 37752 37764 37752 37764 37752 37764 37752 37764 37752 37764 37752 37764 37752 37764 37752 37764 37752 37764 37752 37764 37752 37764 37752 37663 37764 37752 37752	1 3585 3593 3601 3609 3617 3625 3633 3641 3649 3657 3665 3667 3665 3667 3765 3773 3765 3775 377	2 3586 3594 3602 3610 3618 3626 3658 36642 3658 36642 3658 36642 3658 36642 36642 36642 36642 3674 3776 3778 3776 3778 3754 3754 3754 3754 3754 3754 3754 3754	3 3587 3595 3603 3611 3619 3627 3643 3663 3663 3663 3663 3663 3663 366	4 3588 3596 3604 3628 3636 3644 3652 3664 3668 3676 3708 3708 3708 3708 3776 3774 3772 3780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 37780 3780 3	5 3589 3597 3605 3613 3629 3637 3645 3663 3663 3701 3775 3733 3709 3717 3765 3773 3749 3757 3749 3757 3749 3757 3749 3757 3749 3757 3749 3757 3761 3779 3797	6 35590 35598 3606 3614 3662 3663 36646 36654 36654 36654 36654 36654 37702 3718 37726 3734 3710 3718 37734 3753 3753 3753 3753 3754 3753 3754 3754	7 3591 3599 3607 3623 3631 3639 3647 3655 3663 3671 3687 3687 3687 3687 3703 3771 3775 3703 3771 3775 3743 3751 3759 3767 3775 3775 37783 3779 3779 3779 3779 3807 3815 3799		7400 7410 7420 7420 7450 7460 7510 7550 7550 7550 7550 7550 7550 755	0 3840 3848 3856 3856 3864 3872 3880 3988 3994 3912 3928 3928 3928 3928 3928 3928 3928 3936 3944 3952 3950 3960 3968 3966 3966 3967 3960 4000 4000 4000 4002 4000 4008 4008 4072 4080 3080 3080 3080 3080 3090 30000 3000 3000 3000 3000 3000 3000 3000 3000 3000 3000 30	1 3841 3849 3857 3865 3873 3889 3997 3905 3913 3929 3937 3945 3929 3937 3945 3953 3953 3961 3969 3977 3985 3997 4007 4007 4007 4007 4007 4007 4008 4017 4025 4037 4025 4037 403	2 3842 3850 3858 3866 3874 3890 3914 3922 3930 3930 3930 3938 3946 3954 3962 3970 3978 3962 3970 3978 3964 4010 4010 4010 4026 40	3 3843 3859 3867 3875 3883 3899 3907 3915 3923 3931 3939 3947 3939 3947 3955 3963 3979 3963 3979 3963 3979 3963 3979 3963 3979 3963 3969 3967 4010 4000 400	4 3844 3852 3860 3868 3876 3884 3892 3900 3908 3912 3940 3946 3940 394	5 3845 3853 3861 3869 3877 3909 3917 3925 3993 3993 3993 3993 3993 3941 3949 3957 3965 3965 3965 3965 3967 3989 3997 3981 4005 4005 4005 4005 4005 4005 4005 400	6 3846 3854 3852 3870 3872 3910 3918 3926 3953 3954 3953 3954 3953 3954 3954 3950 3958 3966 3962 3990 3998 3990 3998 4006 4014 4022 4030 4014 4022 4030 4014 4022 4030 4014 4022 4030 4054 4064 4054 4065 4054 4065 40654 40654 40654 40654 40654 40654 40654 40654 40654 40654 40654 40654 40654 40654 40654 3054 2055 30576	7 3847 3855 3863 3863 3871 3895 3903 3911 3919 3927 3935 3943 3955 3943 3955 3943 3955 3967 3967 3967 3963 3991 3999 4007 4015 4023 4031 4039 40471 4055 4063 4071 4065	7000 to 77777 (Octal)	3584 to 4095 (Decimal)

# APPENDIX V

# OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
. 000	. 000006	. 100	. 125000	. 200	. 250000	. 300	.375000
001	001953	. 101	126953	201	251953	. 301	376953
002	003906	102	128906	202	253906	302	378906
003	005859	103	130859	203	255859	303	380859
.003	.003635	103	122012	204	257919	204	202012
.004	.007812	104	194765	. 204	201012 250765	.304	204765
.005	.009765	.105	.134703	.205	. 209700	. 305	.364765
.006	.011718	. 106	.136/18	.206	. 261/18	.306	.386718
.007	.013671	. 107	.138671	. 207	. 263671	.307	.388671
.010	.015625	. 110	.140625	. 210	.265625	.310	.390625
.011	.017578	. 111	.142578	. 211	.267578	. 311	.392578
.012	.019531	. 112	.144531	. 212	.269531	.312	.394531
.013	.021484	. 113	.146484	.213	.271484	. 313	.396484
.014	.023437	.114	. 148437	.214	.273437	.314	.398437
015	025390	. 115	. 150390	. 215	. 275390	. 315	400390
016	027343	. 116	152343	. 216	. 277343	. 316	402343
017	029296	117	154296	217	279296	317	404296
	.023250	100	15 (950		991950	200	400950
.020	.031250	.120	. 156250	. 220	. 201230	.320	,406250
.021	.033203	. 121	. 158203	. 221	. 283203	. 321	.408203
.022	.035156	. 122	. 160156	. 222	. 285156	. 322	.410156
.023	.037109	. 123	. 162109	.223	,287109	.323	.412109
.024	.039062	. 124	. 164062	. 224	. 289062	.324	,414062
.025	.041015	. 125	.166015	. 225	. 291015	.325	.416015
.026	.042968	. 126	. 167968	. 226	.292968	. 326	.417968
.027	.044921	. 127	.169921	. 227	. 294921	. 327	.419921
. 030	.046875	.130	. 171875	. 230	. 296875	.330	.421875
.031	.048828	. 131	.173828	. 231	. 298828	. 331	. 423828
.032	.050781	. 132	, 175781	. 232	.300781	. 332	. 425781
033	052734	. 133	. 177734	. 233	. 302734	. 333	. 427734
034	054687	. 134	179687	. 234	. 304687	. 334	429687
035	056640	. 135	181640	. 235	. 306640	. 335	.431640
036	058593	136	183593	236	308593	336	433593
037	060546	137	185546	237	310546	337	435546
	.000010	140	107500	940	212500	240	427500
.040	.062500	. 140	. 187300	. 240	.312500	. 340	.437500
.041	.064453	.141	. 189455	. 241	.314455	. 341	.435433
.042	.066406	.142	. 191406	. 242	,316406	.342	.441406
.043	.068359	. 143	. 193359	.243	.318359	. 343	.443359
.044	.070312	. 144	. 195312	. 244	.320312	.344	.445312
.045	.072265	. 145	. 197265	. 245	. 322265	. 345	.447265
.046	.074218	. 146	. 199218	.246	.324218	.346	.449218
.047	.076171	. 147	. 201171	. 247	. 326171	.347	.451171
.050	.078125	. 150	.203125	. 250	.328125	. 350	.453125
.051	.080078	. 151	.205078	. 251	. 330078	.351	.455078
.052	.082031	. 152	.207031	. 252	.332031	. 352	.457031
.053	.083984	. 153	.208984	. 253	. 333984	. 353	.458984
. 054	.085937	. 154	210937	. 254	. 335937	. 354	460937
055	087890	, 155	212890	255	337890	355	462890
056	089843	156	214843	256	339843	.356	464843
057	091796	157	216796	255	341796	357	466796
.001	002750	100	010750	. 201	040750		100700
.060	. 093750	. 160	.218/50	. 260	. 343/30	.360	.400750
.061	.095703	, 161	. 220703	.261	.345703	.361	.470703
.062	.097656	, 162	. 222656	. 262	.347656	. 362	.472656
.063	.099609	. 163	.224609	. 263	.349609	. 363	.474609
.064	.101562	.164	. 226562	. 264	.351562	. 364	. 476562
.065	.103515	. 165	.228515	. 265	.353515	. 365	.478515
.066	.105468	. 166	.230468	.266	.355468	.366	.480468
.067	.107421	. 167	. 232421	. 267	.357421	. 367	.482421
.070	.109375	. 170	.234375	. 270	.359375	. 370	.484375
.071	.111328	. 171	.236328	.271	.361328	. 371	.486328
.072	113281	. 172	.238281	. 272	.363281	. 372	.488281
073	115234	. 173	. 240234	. 273	365234	. 373	490234
.074	. 117187	. 174	.242187	. 274	.367187	.374	492187
075	119140	. 175	244140	275	.369140	375	494140
076	121093	. 176	246093	276	371093	376	496093
077	123046	.177	. 248046	277	373046	377	498046
	. 100010						. 100010
				l		L	

OCTAL-DECIMAL FRACTIO	N CONVERSION TABLE
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			Y
OCTAL DEC.	OCTAL DEC.	OCTAL DEC.	OCTAL DEC.
000000 000000	.000100 .000244	.000200 .000488	.000300 .000732
000001 000003	000101 000247	.000201 .000492	.000301 .000736
000002 000007	000102 .000251	.000202 .000495	.000302 .000740
000003 000011	000103 000255	.000203 .000499	.000303 .000743
000004 000015	000104 000259	.000204 .000503	.000304 .000747
000005 000019	000105 000263	.000205 .000507	.000305 .000751
000003 000013	000106 000267	.000206 .000511	.000306 .000755
000007 000022	000107 000270	000207 000514	.000307 .000759
.000007 .000020	000110 000274	000210 000518	000310 000762
.000010 .000030	.000110 .000274	.000210 .000518	000311 000765
.000011 .000034	.000111 .000278	000212 000522	000312 000770
.000012 .000038	.000112 .000282	000212 000020	000313 000774
.000013 .000041	.000113 .000280	.000218 .000530	000314 000778
.000014 .000045	.000114 .000285	000211 000537	000315 000782
.000015 .000049	.000115 .000295	000215 .000541	000316 000785
.000016 .000053	.000117 .000201	000217 000545	000317 000789
.000017 .000057	.000117 .000301	.000211 .000540	000320 000703
.000020 .000061	.000120 .000305	.000220 .000549	.000320 .000793
.000021 .000064	.000121 .000308	000221 .000555	.000322 .000191
.000022 .000068	.000122 .000312	.000222 .000556	000322 000801
000023 000072	000124 - 000220	000223 000564	000324 000809
.000024 .000076	000124 000320	000224 .000564	000325 000819
.000025 .000080	000126 000324	000220 .000500	000326 000816
.000025 .000083	000120 .000328	000227 000576	000327 000820
.000027 .000087	.000127 .000331	.000221 .000510	.000321 .000820
.000030 .000091	.000130 .000335	.000230 .000579	.000330 .000823
.000031 .000095	.000131 .000339	.000231 .000585	.000332 .000827
.000032 .000099	.000132 .000343	000232 .000581	000333 000831
.000033 .000102	.000133 .000347	.000233 .000391	000334 000835
000034 000106	000134 .000350	000234 .000595	000335 000843
000035 000110	000136 000358	000236 000602	.000336 .000846
000037 000114	000137 000362	.000237 .000606	.000337 .000850
000040 000122	000140 000366	000240 000610	000340 000854
000040 .000122	000141 000370	000241 000614	000341 000858
000042 000129	000142 000373	.000242 .000617	.000342 .000862
000042 000123	.000143 .000377	.000243 .000621	.000343 .000865
000044 000137	.000144 .000381	.000244 .000625	.000344 .000869
000045 000141	.000145 .000385	.000245 .000629	.000345 .000873
000046 000144	.000146 .000389	.000246 .000633	.000346 .000877
.000047 .000148	.000147 .000392	.000247 .000637	.000347 .000881
000050 000152	000150 000396	.000250 .000640	.000350 .000885
000051 000156	000151 000400	.000251 .000644	.000351 .000888
000052 .000160	.000152 .000404	.000252 .000648	.000352 .000892
.000053 .000164	.000153 .000408	.000253 .000652	.000353 .000896
.000054 .000167	.000154 .000411	.000254 .000656	.000354 .000900
.000055 .000171	.000155 .000415	.000255 .000659	.000355 .000904
.000056 .000175	.000156 .000419	.000256 .000663	.000356 .000907
.000057 .000179	.000157 .000423	.000257 .000667	.000357 .000911
000060 000183	.000160 .000427	.000260 .000671	,000360 .000915
000061 000186	.000161 .000431	.000261 .000675	,000361 .000919
.000062 .000190	.000162 .000434	.000262 .000679	.000362 .000923
000063 000194	.000163 .000438	.000263 .000682	.000363 .000926
000064 .000198	.000164 .000442	.000264 .000686	.000364 .000930
000065 000202	.000165 .000446	.000265 .000690	.000365 .000934
000066 .000205	.000166 .000450	.000266 .000694	.000366 .000938
.000067 .000209	.000167 .000453	.000267 .000698	.000367 .000942
000070 000213	.000170 .000457	.000270 .000701	.000370 .000946
000071 000217	.000171 .000461	.000271 000705	.000371 .000949
000072 000221	.000172 .000465	.000272 .000709	.000372 .000953
000073 000225	.000173 .000469	.000273 .000713	.000373 .000957
.000074 .000228	.000174 .000473	.000274 .000717	.000374 .000961
.000075 .000232	.000175 .000476	.000275 .000720	.000375 .000965
.000076 .000236	.000176 .000480	.000276 .000724	.000376 .000968
.000077 .000240	.000177 .000484	.000277 .000728	.000377 .000972

# OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL DEC.	OCTAL DEC.	OCTAL DEC.	OCTAL DEC.
.000400 .000976	.000500 .001220	.000600 .001464	.000700 .001708
.000401 000980	000501 001224	000601 001468	000701 001712
.000402 .000984	.000502 .001228	.000602 001472	000702 001716
.000403 .000988	.000503 .001232	.000603 .001476	000703 001720
.000404 .000991	.000504 .001235	.000604 .001480	.000704 001724
.000405 .000995	.000505 .001239	.000605 .001483	000705 001728
.000406 .000999	.000506 .001243	.000606 .001487	.000706 .001731
.000407 .001003	.000507 .001247	.000607 .001491	.000707 .001735
000410 001007	000510 001251	000610 001495	000710 001739
.000411 .001010	000511 001255	000611 001499	000711 001743
.000412 .001014	.000512 .001258	000612 001502	000712 001747
.000413 .001018	000513 001262	000613 001506	000713 001750
.000414 .001022	.000514 001266	000614 001510	000714 001754
.000415 .001026	000515 001270	000615 001514	000715 001759
.000416 .001029	.000516 .001274	.000616 001518	000716 001762
.000417 .001033	.000517 .001277	.000617 .001522	000717 001765
000420 001027	000530 001391	000000 001585	
.000420 .001037	.000520 .001281	.000620 .001525	.000720 .001770
000422 001041	.000521 .001285	.000621 .001529	.000721 .001773
000422 001045	000522 .001285	.000622 .001533	.000722 .001777
000424 001052	000524 001296	000624 001541	000723 001781
.000425 001056	.000525 001300	000625 001544	000725 001780
000426 001060	000526 001304	000626 001548	.000725 .001789
.000427 .001064	000527 001308	000627 001552	000727 001792
000430 001068	000530 001312	000630 001556	000720 001800
000431 001071	000531 001316	000631 001560	000731 001800
000432 001075	000532 001319	000632 001564	000732 001804
.000433 .001079	.000533 .001323	.000633 .001567	000733 001811
.000434 .001083	.000534 .001327	.000634 .001571	000734 001815
.000435 .001087	.000535 .001331	.000635 .001575	.000735 .001819
.000436 .001091	.000536 .001335	.000636 .001579	.000736 .001823
.000437 .001094	.000537 .001338	.000637 .001583	.000737 .001827
.000440 .00109	.000540 .001342	.000640 .001586	.000740 .001831
.000441 .001102	.000541 .001346	.000641 .001590	.000741 .001834
.000442 .001106	.000542 .001350	.000642 .001594	.000742 .001838
.000443 .001110	.000543 .001354	.000643 .001598	.000743 .001842
.000444 .001113	.000544 .001358	.000644 .001602	.000744 .001846
.000445 .001117	.000545 .001361	.000645 .001605	.000745 .001850
.000446 .001121	.000546 .001365	.000646 .001609	.000746 .001853
.000447 .001125	.000547 .001369	.000647 .001613	.000747 .001857
.000450 .001129	.000550 .001373	.000650 .001617	.000750 .001861
.000451 .001132	.000551 .001377	.000651 .001621	.000751 .001865
.000452 .001136	.000552 .001380	.000652 .001625	.000752 .001869
.000453 .001140	.000553 .001384	.000653 .001628	.000753 .001873
.000454 .001144	.000554 .001388	.000654 .001632	.000754 .001876
.000455 .001148	.000555 .001392	.000655 .001636	.000755 .001880
.000456 .001152	.000556 .001396	.000656 .001640	.000756 .001884
.000457 .001155	.000557 .001399	.000657 .001644	.000757 .001888
.000460 .001159	.000560 .001403	.000660 .001647	.000760 .001892
.000461 .001163	.000561 .001407	.000661 .001651	.000761 .001895
.000462 .001167	.000562 .001411	.000662 .001655	.000762 .001899
.000463 .001171	.000563 .001415	.000663 .001659	.000763 .001903
000465 001174	.000565 001415	000665 001667	000765 001911
000466 001182	000566 001426	000666 001670	000766 001914
.000467 001186	000567 001430	.000667 001674	000767 001919
000470 001190	000570 001434	000670 001679	000770 001029
000471 001194	.000571 001438	.000671 001682	.000771 001926
.000472 001197	.000572 .001441	.000672 .001686	.000772 .001930
.000473 001201	.000573 .001445	.000673 .001689	.000773 .001934
.000474 .001205	.000574 .001449	.000674 .001693	.000774 .001937
.000475 .001209	.000575 .001453	.000675 .001697	,000775 .001941
.000476 .001213	.000576 .001457	.000676 .001701	.000776 .001945
.000477 .001216	.000577 .001461	.000677 .001705	.000777 .001949
1			
		l	

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# APPENDIX VI EXF and Character Codes

1604-A EXF CODES

SELECT INTERNAL

74 0	000C0		Allow Interrupt on Channel C inactive
	000C1		Disallow Interrupt on Channel C inactive
	01000		Start Real-Time Clock
	02000		Stop Real-Time Clock
	00070		Clear Arithmetic Faults and Clock Overflow
	C0000		Clear All Channel C Selections
	C = 1 - 6		
SELE	CT INTERRUP	rs	
74 0	00100		Allow Interrupt on Internal (Arithmetic) Faults or Clock Overflow
	00101		Disallow Interrupt on Internal (Arithmetic) Faults or Clock Overflow
740	03C00		Allow Interrupt on Channel C
	03C01		Disallow (Mask) Interrupt on Channel C
	C = 1 - 6	Channel	1-6
	$\mathbf{C} = 0$	Channel	7 Output
	C = 7	Channel	7 Input
74 0	04000		Allow Selected External Interrupts
	04001		Disallow (Mask) All External Interrupts
SENS	E INTERNAL		
$74 \ 7$	000 <b>C</b> 0		Exit on Channel C Active
	000C1		Exit on Channel C Inactive
	C = 1 - 6		
	001A0		Exit on Arithmetic Fault A
	001A1		Exit on No Arithmetic Fault A
			A = 1: Divide
			2: Shift
			3: Overflow
			4 : Exponent Overflow
			5 : Exponent Underflow

747	0C000			Exit on Channel C Interrupt
747	0C001			Exit on No Channel C Interrupt
	С	= 1	- 6	
747	001Т0			Exit on Channel T Interrupt
747	001T1			Exit on No Channel T Interrupt
				T = 6 = Channel 7 - (Output)
				T = 7 = Channel 7 - (Input)
747	00200		-	Exit if Next Main Program Instruction is Upper
747	00201			Exit if Next Main Program Instruction is Lower
747	00300			Exit on Clock Overflow
74 7	00301			Exit on No Clock Overflow
				CONSOLE EQUIPMENT
				(CHANNEL PAIR 1 and 2)
SELE	<u>CT</u>			
INPIT	r 74	LO	11140	Select Typewriter for Input and Interrupt on Carriage Return
			100	Select Typewriter for Input, and No Interrupt on C B
			100	
			200	Select Paper Tape Reader, and No Interrupt on End of Tape
			210	Select Paper Tape Reader and Set End of Tape Indicator
			220	Select Paper Tape Reader, and Interrupt on End of Tape
OUTP	UT 74	ł 0	<u>21</u> 100	Select Typewriter for Output, Assembly Mode
			110	Select Typewriter for Output, Character Mode
			200	Select Paper Tape Punch, Assembly Mode
			210	Select Paper Tape Punch, Character Mode
			240	Turn Paper Tape Punch Motor Off
GENGE	ק			
001001	-			
INPUI	74	17	11200	Exit on Paper Tape Reader, End of Tape
			201	Exit on Paper Tape Reader, No End of Tape
			210	Exit on Paper Tape Reader in Assembly Mode
			211	Exit on Paper Tape Reader in Character Mode
			140	Exit on Typewriter in Lower Case
			141	Exit on Typewriter in Upper Case
			100	Exit on Carriage Return or Tab from Typewriter
			101	Exit on No Carriage Return or Tab from Typewriter

OUTPUT	$74 \ 7$	$\underline{21}200$	Exit on Paper Tape Punch Out of Tape
		201	Exit on Paper Tape Punch Not Out of Tape
			1607 EXF CODES
			(CHANNEL C, CABINET 2)*
SELECT			
INPUT	74 0	<u>C2</u> 0N1	Select Read Tape N, Binary Mode
		0N2	Select Read Tape N, Coded Mode
		001	Read Selected Tape, Binary Mode
		002	Read Selected Tape, Coded Mode
		004	Interrupt When Selected Tape Ready
		005	Rewind Selected Tape
		006	Backspace Selected Tape
		007	Rewind Selected Tape with Interlock
OUTPUT	74 0	<u>C2</u> 0N1	Select Write Tape N, Binary Mode
		0N2	Select Write Tape N, Coded Mode
		001	Write Selected Tape, Binary Mode
		002	Write Selected Tape, Coded Mode
		003	Write End of File Mark on Selected Tape
		004	Interrupt When Selected Tape Ready
		005	Rewind Selected Tape
		006	Backspace Selected Tape
		007	Rewind Selected Tape with Interlock
SENSE			
INPUT	747	<u>C 2</u> 000	Exit on Ready to Read
		001	Exit on Not Ready to Read
		002	Exit on Read Parity Error
		003	Exit on No Read Parity Error
		004	Exit on Read Length Error
		005	Exit on No Read Length Error
		006	Exit on End of File Mark
		007	Exit on No End of File Mark

\* The equipment designator (fourth octal digit from the right) in 1607 EXF codes may be either 2 or 3. A switch in the rear of the 1607 cabinet determines which number will be recognized as the designator for that cabinet.

OUTPUT	74 7 <u>C2</u> 000	Exit on Ready to Write
	001	Exit on Not Ready to Write
	002	Exit on Write Reply Parity Error
	003	Exit on No Write Reply Parity Error
	004	Exit on Write Reply Length Error
	005	Exit on No Write Reply Length Error
	006	Exit on End of Tape Marker
	007	Exit on No End of Tape Marker

## 1608 EXF CODES

## (CHANNEL C) C = 1-6

## SELECT

INPUT	74 0 <u>C7</u> 7N1	Select Read Tape N, Binary Mode
	7N2	Select Read Tape N, Coded Mode
	001	Read Selected Tape, Binary Mode
	002	Read Selected Tape, Coded Mode
	004	Interrupt When Selected Tape Ready
	005	Rewind Selected Tape
	006	Backspace Selected Tape
	007	Rewind Selected Tape with Interlock
	101	Turn Off "Tape Indicator" on Read Unit
	102	Set Low Density on Read Unit
	103	Set High Density on Read Unit
	104	Search File Mark Forward on Read Unit
	105	Search File Mark Backward on Read Unit
	106	Remove Interrupt Selection on Read Unit
OUTPUT	74 0 <u>C7</u> 7N1	Select Write Tape N,Binary Mode
	7N2	Select Write Tape N, Coded Mode
	001	Write Selected Tape, Binary Mode
	002	Write Selected Tape, Coded Mode
	003	Write End of File Mark on Selected Tape

74 0 <u>C7</u> 004	Interrupt When Selected Tape Ready
005	Rewind Selected Tape
006	Backspace Selected Tape
007	Rewind Selected Tape with Interlock
101	Turn Off "Tape Indicator" on Write Unit
102	Set Low Density on Write Unit
103	Set High Density on Write Unit
104	Skip Bad Spot on Selected Write Unit
106	Remove Interrupt on Write Unit
	$\begin{array}{cccc} 74 & 0 & \underline{C7}004 \\ & 005 \\ & 006 \\ & 007 \\ & 101 \\ & 102 \\ & 103 \\ & 104 \\ & 106 \end{array}$

SENSE

INPUT	$74 \ 7$	<u>C7</u> 000	Exit on Ready to Read
		001	Exit on Not Ready to Read
		002	Exit on Read Parity Error
		003	Exit on No Read Parity Error
		004	Exit on Read Length Error
		005	Exit on No Read Length Error
		006	Exit on End of File Mark
		007	Exit on No End of File Mark
		106	Exit When Read Unit is Rewinding or at Load Point
		107	Exit When Read Unit is Not Rewinding or is at Load Point
OUTPUT	747	<u>C7</u> 000	Exit on Ready to Write
		001	Exit on Not Ready to Write
		002	Exit on Write Reply Parity Error
		003	Exit on No Write Reply Parity Error
		004	Exit on Write Reply Length Error
		005	Exit on No Write Reply Length Error
		006	Exit on End of Tape Marker
		007	Exit on No End of Tape Marker
		106	Exit when Write Unit is Rewinding or at Load Point

### 1610 EXF CODES

# (CHANNEL C) C = 1-6

## SELECT

INPUT	74 0	<u>C4</u> 001	Select Primary Read Station
		002	Select Secondary Read Station
		003	Select Primary and Secondary Read Stations
		005	Select Primary Read Station and Interrupt
		006	Select Secondary Read Station and Interrupt
		007	Select Primary and Secondary Read Stations and Interrupt
OUTPUT	74 0	C4001	Select Printer
		002	Select Punch
		005	Select Printer and Interrupt
		006	Select Punch and Interrupt

## SENSE

INPUT	74 7 <u>C4</u> 002	Exit on Reader Ready
	003	Exit on Reader Not Ready
	004	Exit on 1604 Selected
	005	Exit on 1604 Not Selected
OUTPUT	74 7 <u>C4</u> 002	Exit on Printer Ready
	003	Exit on Printer Not Ready
	004	Exit on Punch Ready
	005	Exit on Punch Not Ready
	010	Exit on 1604 Selected
	011	Exit on 1604 Not Selected

# 1612 EXF CODES (CHANNEL C) C = 1-6

SELECT			
OUTPUT	74 0	<u>C6</u> 000	Select Printer
(ONLY)		001	Single Space the Printer
		002	Double Space the Printer
		003	Select Format Channel 7
		004.	Select Format Channel 8
		010	Clear Monitor Channels 1 - 6
		01 N	Select Monitor Channel N : N = 1 - 6
SENSE			
OUTPUT	74 7	<u>C6</u> 000	Exit on Printer Ready
(ONLY)		001	Exit on Printer Not Ready
			1615 FUNCTION CODES
			(CHANNEL C, CABINET 2)*
OUTPUT			
	$74 \ 0$	C20N1	Select Tape N to Write Binary
		20N2	Select Tape <u>N</u> to Write Coded $(N = 1_8 - 10_8)$
		2001	Prepare Selected Tape to Write Binary
		2002	Prepare Selected Tape to Write Coded
		2003	Write End-of-File Mark on Selected Tape
		2004	Select Interrupt When Write Tape Next Ready
		2005	Rewind Selected Write Tape
		2006	Backspace Selected Write Tape
		2007	Rewind-Unload Selected Write Tape
		2400	Clear Interrupt Selections on Write Tape
		2401	Set Low Density on Selected Write Tape
		2402	Set High Density on Selected Write Tape
		2403	Skip Bad Spot on Selected Write Tape
		2404	Select Interrupt on Next Error

<sup>\*</sup> The equipment designator (fourth octal digit from the right) in 1615 EXF codes may be either 2 or 3. A switch in the 1615 cabinet determines which number will be recognized as the designator for that cabinet.

## SENSE

74 7 C	2000	Exit On Ready To Write
	2001	Exit On Not Ready To Write
	2002	Exit On Write Reply Parity Error
	2003	Exit On No Write Reply Parity Error
	2004	Exit On Write Reply Length Error
	2005	Exit On No Write Reply Length Error
	2006	Exit On End Of Tape Marker
	2007	Exit On Not End Of Tape Marker
	2400	Exit On Ready To Select
	2401	Exit On Not Ready To Select
	2402	Exit On Load Point
	2403	Exit On Not Load Point
	2404	Exit On Interrupt On Write Tape
	2405	Exit On No Interrupt On Write Tape
	2406	Exit On Write Program Error
	2407	Exit On No Write Program Error
INPUT		
74 0 C	20N1	Select Tape <u>N</u> To Read Binary One Record
	20N2	Select Tape <u>N</u> To Read Coded One Record
	22N1	Select Tape <u>N</u> To Read Binary One File
	22N2	Select Tape N To Read Coded One File
	2001	Prepare Selected Tape To Read Binary One Record
	2002	Prepare Selected Tape To Read Coded One Record
	2201 ·	Prepare Selected Tape To Read Binary One File
	2202	Prepare Selected Tape To Read Coded One File
	2003	Move Selected Read Tape Forward One Record
	2203	Search File Mark Forward
	2004	Select Interrupt When Read Tape Next Ready
	2005	Rewind Selected Read Tape
	2006	Backspace Selected Read Tape
	2206	Search File Mark Backward
	2007	Rewind-Unload Selected Read Tape
	2400	Clear Interrupt Selections On Read Tape
	2401	Set Low Density On Selected Read Tape
	2402	Set High Density On Selected Read Tape
	2404	Select Interrupt On Next Error

### SENSE

74 7 C2000	Exit on Ready to Read
2001	Exit on Not Ready to Read
2002	Exit on Read Parity Error
2003	Exit on No Read Parity Error
2004	Exit on Read Length Error
2005	Exit on No Read Length Error
2006	Exit on End of Tape Marker
2007	Exit on Not End of Tape Marker
2400	Exit on Ready to Select
2401	Exit on Not Ready to Select
2402	Exit on Load Point
2403	Exit on Not Load Point
2404	Exit on Interrupt on Read Tape
2405	Exit on No Interrupt on Read Tape
2406	Exit on Read Program Error
2407	Exit on No Read Program Error

### SATELLITE EXTERNAL FUNCTION CODES

# 1604-A EXTERNAL FUNCTION CODES

OUTPUT SELECT		
74 0 C2500	Release Direct Selections	
2501	Select Write Control for 160	
2502	Release Write Control to 1604	
2503	Select Direct 1604 to 160	
2504	Select Action Request	
2520	Clear Communication Flag 2	
2540	Set Communication Flag 1	
2560	Clear Communication Flag 1	
OUTPUT SENSE		
74 7 C2500	Exit on Write Control Available	
2501	Exit on Write Control Not Available	
2520	Exit on Communications Flag 2 Set	
2521	Exit on Communications Flag 2 Not Set	
2560	Exit on Communications Flag 1 Set	
2561	Exit on Communications Flag 1 Not Set	

### INPUT SELECT

74 0 C2501	Select Read Control for 160
2502	Release Read Control to 1604
2503	Select Direct 160 to 1604
2505	Release Interrupt

### INPUT SENSE

74 7 C2500	Exit on Read Control Available
2501	Exit on Read Control Not Available
2504	Exit on 160 Interrupt
2505	Exit on No 160 Interrupt

### 160 EXTERNAL FUNCTION CODES

WRITE SELECT			
	6050	Release Action Request	
	6051	Set Communications Flag 2	
	6052	Release Write Control to 1604	
	6055	Clear Communications Flag 1	
	6056	Clear Communications Flag 2	
READ SELECT			
	5051	Set Communications Flag 1	
	5052	Release Read Control to 1604	
	5053	Select Interrupt	
STATUS RESPONSE*			
	4XXX	Read Control Available	
	2XXX	Write Control Available	
	1XXX	Direct 160 to 1604	
	X4XX	Direct 1604 to 160	
	XXX2	160 Action Request	
	XXX1	Communications Flag 1 Set	

<sup>\*</sup> Bits may be superimposed; e.g., 6XXX means both read control and write control available.
# APPENDIX VII

# Magnetic Tape BCD Codes

Character	Code (Octal)	Character	Code (Octal)	
А	61	2	02	
В	62	3	03	
С	63	4	04	
D	64	5	05	
E	65	6	06	
F	66	7	07	
G	67	8	10	
Н	70	9	11	
I	71	&	60	
J	41	-	40	
К	42	(blank)	<b>2</b> 0	
L	43	/	21	
м	44	. (period)	73	
Ν	45	\$	53	
0	46	**	54	
Р	47	, (comma)	33	
Q	50	70	34	
R	51	#	13	
S	22	@	14	
Т	23	д	74	
U	24	0 (numeric <b>a</b> l zero)	12	
v	25	record mark	32	
W	26	0 (minus zero)	52	
Х	27	0 (plus zero)	72	
Y	30	group mark	77	
Z	31	tape m <b>a</b> rk	17	
0	12			
1	01			

# **APPENDIX VIII**

Flexowriter Codes

UC	LC	CODE	UC	LC	CODE
Α	a	30	Y	Y y	
в	ъ	23	Z	a	21
С	С	16	0	0	56
D	d	22	1	1	74
E	е	20	2	2	70
F	f	26	з	3	64
G	g	13	4	4	62
H	h	05	5	5	66
I	i	14	6	6	72
J	j	32	7	7	60
К	k	36	8	8	33
L	1	11	9	9	37
M	m	07	-	-	52
N	n	06	T	1	44
0	ο	03	(	)	54
Р	р	15	+	,	46
Q	q	35	=	•	42
R	r	12	:	;	50
S	s	24	CR Una an C		45
Т	t	01	Lower (	Case (UC)	57
U	u	34	Color Si	hift (CS)	02
v	v	17	Stop	e (IAD)	43
w	w	31	Space Tape Fe Delete	eed	04 00 77
х	x	27	20000		
Note:	1) Le Ste	eader – Blank tap op – Stop Flexe	oe, Del owriter reader	lete - Delete	d ch <b>a</b> racter
	2) 10	40 41 53 55 6	3 65 67 71	73 75 70	_ 211 1

2) 10, 40, 41, 53, 55, 63, 65, 67, 71, 73, 75, and 76 - illegal

# APPENDIX IX

## Punched Card Codes

Char	Card	BCD	Char	Card	BCD	Char	Card	ВСD	Char	Card	BCD
			+	12	60		11	40			20
l	l	Ol	А	12 1	61	J	11 1	41	/	0 1	21
2	2	02	В	12 2	62	K	11 2	42	S	0 2	22
3	з	03	C	12 3	63	L	11 3	43	Т	0 3	23
4	4	04	D	12 <b>4</b>	64	М	11 4	44	U	0 <b>4</b>	24
5	5	05	Е	12 5	65	N	11 5	45	v	0 5	25
6	6	06	F	12 6	66	0	11 6	46	W	C 6	26
7	7	07	G	12 7	67	Ρ	11 7	47	x	0 7	27
8	8	10	Н	12 8	70	Q	11 8	50	Y	C 8	30
9	9	11	I	12 9	71	R	<b>1</b> 1 9	51	Z	9	31
0	С	12	+	12	72	-	11 0	52			
=	8,3	13	•	12 8,3	73	ť¢	11 8,3	53	,	о 8,3	33
-	8,4	14	)	<sup>12</sup> 8 <b>,4</b>	74	*	11 8 <b>,4</b>	54	(	8 <sup>0</sup> 4	34

# APPENDIX X

		Input/Output Ty	pewriter C	odes	
CHARACTERS UC LC		CODE	CHARA UC	CTERS LC	CODE
A	a	30	x	x	27
В	Ъ	23	ĩ	3	25
C	C	16	Z	Z	21
D	đ	22	)	0	56
E	e	20	¥	1	74
F	f	26	Ø	2	<b>7</b> 0
G	g	13	#	3	64
H	h	05	\$	4	62
I	i	14	%	5	66
J	j	32	¢	6	72
K	k	36	&	7	60
L	l	11	1/2	8	33
M	m	07	(	. 9	37
N	n	06	-	-	52
0	0	03	?	/	44
P	P	15	π	t	54
Q	q	35	0	+	46
R	r	12	•	٠	42
S	8	24	:	;	50
T	t	01	,	,	40
U	u	34	÷	=	02
v	v	17	tab	tab	51
W	v	31	spe	ice	04
Backs	space	61	Carris	ge Return	45
Lower	Case	57	Upper	Case	47

# **APPENDIX XI**

## 1612 Printer Codes

CHAR	CODE	CHAR	CODE	CHAR	CODE	CHAR	CODE
Blank	20	F	66	v	25	≤	15
0	12	G	67	w	26	ŧ	16
1	01	Ħ	70	x	27	C	17
2	02	İ	71	Y	30	I	32
3	03	J	41	Z	31	-	35
4	04	к	42	•	73	=	36
5	05	L	43	-	40	~, ^	37
6	06	М	44	+	60	% or∨	52
7	07	N	45	=	13	\$ or 🗍	5 <b>3</b>
8	10	0	46	(	34	t	55
9	11	Р	47	)	74	ł	56
Α	61	Q	50	1	21	>	5 <b>7</b>
в	6 <b>2</b>	R	51	*	54	<	72
С	63	S	22	,	33	2	75
D	64	т	23	:	00	?	76
Е	65	U	24	ŧ	14	;	77

In last column, codes ~ %  $\$  appear if business application,  $\land \lor \neg$  for scientific application.

#### 1604-A INSTRUCTIONS

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			Desig					Davis
4.0.0	A 11	1 4	Page		MITTO		0.0	Page
ADD	Add	14	2-17		NUF	Multiply Fractional	26	2-20
ADL	Add Logical	45	2-35		MUI	Multiply Integer	24 69	2-18
AJP	A Jump	22	2-27,30		OUT	Output Transfer	63	2-40
ALS	A Left Shift	05	2-13		QJP	Q Jump	23	2-28,31
ARS	A Right Shift	01	2-13		QLS	Q Left Shift	06	2-14
DVF	Divide Fractional	27	2-20		QRS	Q Right Shift	02	2-13
DVI	Divide Integer	25	2-19		RAD	Replace Add	70	2-38
$\mathbf{ENA}$	Enter A	10	2-25		RAO	Replace Add One	72	2-38
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