Reference Manual

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CONTROL DATA® 1604-C COMPUTER



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1604 INSTRUCTIONS

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PREFACE

This manual describes the characteristics, instructions, and manual controls of the CONTROL DATA* 1604 computer. Throughout the manual "1604" designation is used meaning "1604-C" which has become the official designation. Instruction Descriptions in this manual are also applicable to the CONTROL DATA* 1604-B computer.

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Description

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The CONTROL DATA* 1604 is a stored-program, general-purpose digital computer with a large storage capacity, exceedingly fast computation and transfer speeds, and special provisions for input-output communication. The 1604 is designed to handle large-volume data processing and to solve large scale scientific problems. The compact equipment, constructed from solid-state components throughout, is suitable for use in a semi-permanent office environment.

1604 CHARACTERISTICS

Stored-program general-purpose digital computer

Parallel mode of operation

48-bit word, 2 instructions per word

Single address logic	
Operation code	6 bits
Designator	3 bits
Base Execution Address	15 bits

Six 15-bit index registers

Indirect addressing

Magnetic core storage 32,768 48-bit words

- Two independent 16, 384 word banks alternately phased
- 4.8 usec effective cycle time (representative program)
- 6.4 usec total cycle time

Input-output

Transmission of 48-bit words Three separate buffer input channels Three separate buffer output channels High-speed transfer channel 4.8 usec per word Program interrupt

Console, includes: Photo-electric paper tape reader Paper tape punch Electric typewriter Register contents displayed in octal

Flexible instructions Fixed-point arithmetic (integer and fractional) Floating-point arithmetic Logical and masking operations Indexing Storage searching

Binary arithmetic Parallel addition in 1.2 usec without access Modulus 2⁴⁸-1 (one's complement)

Real-time clock

Completely solid-state Diode logic Transistor amplifiers

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LOGICAL DESCRIPTION

The computer performs calculations and processes data in a parallel binary mode through the step-by-step execution of individual instructions which are stored internally along with the data.

Functionally, the computer may be divided into four major sections. INPUT-OUTPUT provides communication between the computer and the external equipment; ARITHMETIC performs the arithmetic and logical operations required for executing instructions; STORAGE provides internal storage for data and instructions; and CONTROL coordinates and sequences all operations for executing an instruction by obtaining the instruction from storage and translating it into commands for the other sections.

The registers in the computer are identified by letters (table 1-1). The arithmetic properties of the registers are detailed in table 1-2. The operational registers usually hold the end result of an operation. Their contents are displayed on the console and may be manually changed by the operator. The transient registers used in formulating the result are secondary registers. They are not displayed and cannot be manually changed.

STORAGE SECTION

The magnetic core storage section of the 1604 Computer provides high-speed, random access storage for 32, 768 words. It consists of two independent storage units each with a capacity of 16, 384 words. These units operate together during the execution of a stored program and thus are considered as one 32, 768 word storage system.

A word is 48 bits in length and is used in two ways: as two 24-bit instructions or as a 48-bit operand (data word). The location of each word in storage is identified by an assigned number or address. When a word is taken (read) from or entered (written) into storage, a reference is made to the storage address which holds the word. All odd storage addresses are located in one storage unit; all even addresses in the other.

The cycle time, or time for a complete storage reference, is 6.4 microseconds. Since the storage cycles of the two sections overlap one another in the execution of a program, the average effective cycle time for random addresses is about 4.8 microseconds.

Register	Function	Register	Function
A*	Accumulator	$\mathrm{U}^{1}*$	Program Control
${f Q}^* \ {f B}^1 \ {f through} \ {f B}^{6*}$	Auxiliary Arithmetic Index registers (six)	${\mathbb U}^2$ R	Auxiliary Program Control Address Buffer
P*	Program Address	Х	Exchange

* Operational Registers

Register	No. of Stages	Modulus	Complement Notation*	Arithmetic	Result
А	48	2 ⁴⁸ -1	one's	subtractive	signed**
Q	48	2^{48} -1	one's		signed
U^2	15	2 ¹⁵ -1	one's	subtractive	signed
Р	15	2^{15}	two's	additive	unsigned
R	15	2^{15}	two's	subtractive	unsigned

TABLE 1-2.ARITHMETIC PROPERTIES OF REGISTERS

* Refer to Appendix

**The result of an arithmetic operation in A satisfies $A \le 2^{47}$ -1 since A always is treated as a signed quantity. When the result in A is zero, it is always represented by 000...00 except when 111...11 is added to 111...11. In this case, the result is 111...11 (negative zero).

INPUT-OUTPUT

The input-output section of the computer handles the flow of information to and from the computer. Prior to executing a program, the data and instructions which comprise the program (input) are loaded into computer storage. After computation is completed, the results (output) are transmitted from storage to an external equipment. All information is transmitted by way of the X register in the form of 48-bit words.

The computer communicates with external equipment through six independent buffer channels which provide for the normal exchange of data (figure 1-1).

Input:	Channel 1	Output:	Channel 2
	Channel 3		Channel 4
	Channel 5		Channel 6

The input and output buffer channels are paired, channels 1 and 2, channels 3 and 4, and channels 5 and 6. Every external equipment is connected to one of these pairs. It is possible to connect as many as eight different equipments to any given pair of channels. All six buffer channels may be concurrently transmitting information. However, only one external equipment can use any one buffer channel at any given instant.

In the 1604 computer, input-output operations are independent of the main computer program. When data is transmitted, the main computer program initiates an automatic cycle which buffers data to and from computer storage. The main computer program then continues while the actual buffering of data is carried out independently and automatically.

This process of asynchronous input-output operations will be termed a buffer. Buffer transmissions employ independent access to computer storage because computation continues while the external equipment is loading or unloading information from computer storage at a rate dictated by the external equipment.

ARITHMETIC SECTION

The arithmetic section of the 1604 computer consists of two operational registers, A and Q, and one secondary register, X.

The A register (accumulator) is the principal arithmetic register. Some of the more important functions of A are:

1-4

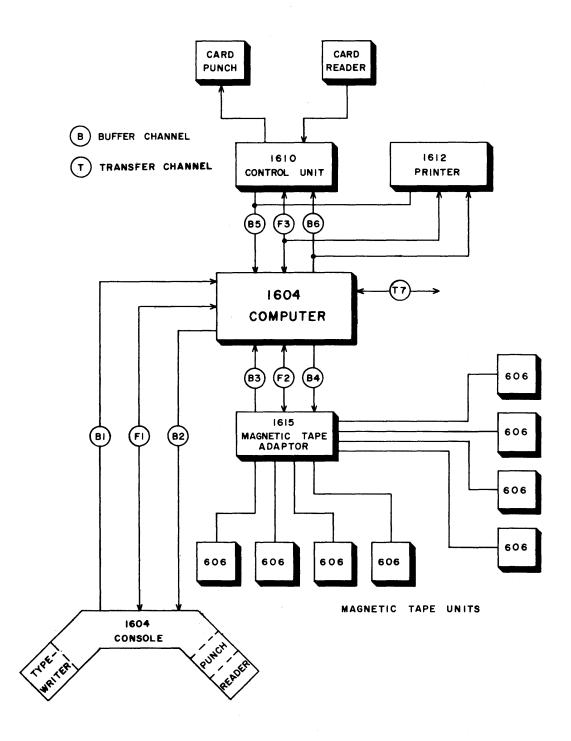


Figure 1-1. Typical 1604 System

- 1) Arithmetic operation A initially holds one of the operands in addition, subtraction, multiplication and division. The result is usually held in A.
- Shifting A may be shifted to the right or left separately or in conjunction with Q. Right shifting is open-ended; the lowest bits are discarded and sign extended. Left shifting is circular; the highest order bit appears in the lowest order stage after each shift; all other bits move one place to the left.
- 3) Control for conditional instructions A holds the word which conditions jump and search instructions.

The Q register is an auxiliary arithmetic register and is generally used in conjunction with the A register. The principal functions of Q are:

- 1) Providing temporary storage of contents of A while A is used for another arithmetic operation.
- 2) Forming a double-length register, AQ or QA.
- 3) Shifting to the right or left, separately or in conjunction with A.
- 4) Participating with the A register in multiplication, division and logical product operations (masking).

The exchange, or X register, is the communication center of the computer. All internal transmissions between the arithmetic section or the input-output section and the rest of the computer are made through X.

CONTROL SECTION

The control section directs the operations required to execute instructions and to exchange data with external equipment. It also establishes the timing relationships needed to perform the operations in the proper sequence.

The control section acquires a program step from storage, interprets it and sends the necessary commands to other sections. A program step is a pair of 24-bit instructions which together occupy one storage location as a 48-bit word. The higher-order 24 bits are the upper instruction; the remaining 24 bits, the lower instruction.

Instruction Format

ſ	f	b	m, y, or k
	(6 bits)	(3 bits)	(15 bits)
. L	operation	index	base execution
	code	designator	address

Each of the 62 instructions has a unique 6-bit operation code which specifies the operation to be performed.

The index designator generally specifies one of the six index registers whose content is to be added to the execution address. This process is called address modification. However, the index designator may also specify indirect addressing or condition jump and stop instructions.

The execution address may be used in one of three ways: as an address, m, of an operand; as an operand, y; or as a shift count, k.

The eight operational registers in the control section are P, U^1 and B^1 through B^6 .

The program address counter (P) is a two's complement additive register. It provides program continuity by generating in sequence the storage addresses which contain the individual program steps. Usually at the completion of each program step the count in P is advanced by one to specify the address of the next program step.

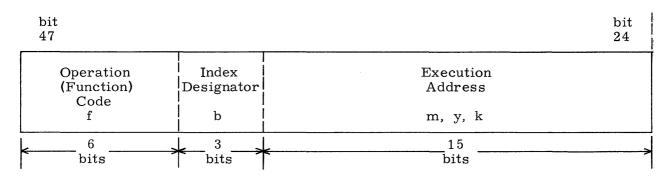
The program control register (U¹) holds a program step while the two instructions contained in it are executed. The upper instruction is usually executed first followed by the lower instruction. After executing an instruction, a half exit, full exit, or jump exit is performed. A half exit always allows the lower instruction of a program step to be executed. A full exit advances the count in P by one and executes the upper instruction of the new program step specified by the contents of P. A jump exit allows a new sequence of instructions to be executed; the storage location of the new instruction is specified by the execution address of the jump instruction. The execution address, in this case, is entered into P and specifies the starting location of a new sequence of program steps. The auxiliary program control register (U^2) is a 15-bit subtractive accumulator used primarily in the modification of the base execution address. The contents of the specified index register are transmitted to the address buffer register (R), which has provisions for counting, complementing and storing. The contents of R are then added to the contents of U^2 which holds the execution address.



Description of Instructions

WORD FORMAT

A computer word consists of 48 bits and may be interpreted as one 48-bit data word or two 24-bit instructions. Each instruction is composed of three parts or codes: operation code, index designator, and execution address. The higher-order 24 bits of the word are called the upper instruction and the lower-order 24 bits are called the lower instruction.



Code	Range	
Operation f	01 - 76 ₈	Specifies the operation to be performed. A 00 or 77 code is interpreted as a fault which stops computer operation.
Execution Address m, y, k	00000 through 77777 ₈	Used in one of three ways: 1) as a shift count k 2) as an operand address, m 3) as an operand, y
Index Designator b	0 1-6 7	No address modification Relative address modification Specifies the index designator whose contents are to be added to the execution address. (Refer to jump and stop instructions for exceptions.) Indirect addressing

Execution Address

The base execution address may be used as: (1) a shift count, k; (2) an operand, y; (3) an address of an operand, m, in storage. The execution address may also be modified or unmodified depending on the index designator. If unmodified, the address is represented by the lower-case symbol k, y, or m; if the address is modified the symbols are capitalized. The following examples point out the relationship between the unmodified and modified execution address.

The modified shift count K is represented by:

 K = k + (B^b) where: K = modified shift count k = unmodified shift count (execution address) (B^b) = contents of index register b.

If the index designator = 0, then K = k.

The modified operand Y is represented by:

2) $Y = y + (B^b)$ where: Y = modified operand y = unmodified operand (execution address) $(B^b) = contents of ind^{ex} register b.$

If the index designator = 0, then Y = y.

The modified operand address M is represented by:

3) $M = m + (B^b)$ where: M = modified address of operand<math>m = unmodified address of operand (execution address) $(B^b) = contents of index register b.$

If the index designator = 0, then M = m. Note that (3) is the only case in which the execution address is interpreted as an address of an operand.

Address Modification

The three possible modes of address modification are identified by the index designators as follows:

 b = 0 No Address Modification. In this mode the execution address is interpreted without modification; nothing is added to or subtracted from it. (Direct addressing.)

- 2) b = 1-6 Relative Address Modification. In this mode the execution address is modified and is equal to the initial execution address plus the contents of the designated index register. One's complement arithmetic is used in determining the modified execution address.
- 3) b = 7 Indirect Addressing. In this mode a storage reference is made to the location designated by the execution address. The 48-bit word is read from storage and the lower-order 18 bits of the word are interpreted as the b designator (3 bits) and execution address (15 bits) of the present instruction. The new index designator may refer to any one of the three modes.

Examples:

- f b m LDA 0 address
 1) No Address Modification LDA 0 address
 This instruction is interpreted as load accumulator from the storage location designated by the sum of the execution address and the contents of the specified index register, B^b. Since b = 0, no index register is designated and m specifies the storage location whose contents are loaded into A.
- 2) Relative Address Modification $LDA \ 6 \ address \ (B^6) = 00001_8$ In this example, the accumulator is loaded from the storage location designated by the execution address plus the contents of index register 6. Therefore, the contents of the storage location named by the execution address plus 00001₈ is loaded into the accumulator. $M = m + (B^b)$.
- 3) Indirect Addressing

Current
Instruction =
$$\stackrel{f}{\text{LDA}} \underbrace{ \stackrel{b}{7} \stackrel{m}{00100}}_{(00100) = \text{FAD } 0 \ 00300 \text{ FMU } \underline{6} \ 00200}_{(B^{6}) = 00001_{8}}$$

When the b designator of the current instruction is 7, the mode is indirect addressing. The lower 18 bits of the contents of the storage location designated by the execution address, 00100, are read from storage into the U^1 register where they are interpreted as the index designator and execution address of the current instruction.

The index designator is inspected again and because it is not 0 or 7 the relative address mode exists. (Note that the new index designator could reference any one of the three modes of address modification.) The execution address, 00200, plus the contents of B^6 , 00001_8 specify the storage location whose contents will be loaded into the accumulator. $M = 00200_8 + (00001_8) = 00201_8$

Execution of a Pair of Instructions

Example:	f b m	f b m
	(00300) = LDA 0 00310	ADD 1 00210
	(00301) = STA 0 00400	SLS 0 00301
	$(B^1) = 00101_8$	

The P register holds address 00300 (an even lowest bit indicates the address of the program step is in the even storage unit). The storage reference is initiated; the 48-bit word is read from address 00300 and entered into U^1 . Computer operation is now dependent upon the interpretation of the 24-bit instruction in the upper half of U^1 .

The operation code, LDA, and the index designator, 0, are translated. The function of the upper instruction, LDA, is to load the A register with the ∞ ntents of the designated storage location. Because the index designator is 0, the execution address is not modified. The translation of the operation code initiates the sequence of the commands which execute the instruction and the operand in address 00310 is loaded into A.

The lower instruction in U^1 is now translated. The ADD instruction causes the quantity in storage location M to be added to the contents of the A register. Since the index designator is not 0 or 7, the contents of the index register are added to the execution address to form M. $M = m + (B^b) = 00210_8 + 00101_8 = 00311_8$. The contents of storage address 00311 are added to the contents of the A register completing the instruction. The contents of the P register are increased by one and the next pair of instructions at address 00301 is read from storage and executed.

INSTRUCTIONS

The 62 computer instructions are described on the following pages, (EXF instructions are discussed in detail in chapter three). The title line contains the numeric code, the mnemonic code and format, name, and average execution time of the instruction. Abbreviations and symbols are defined as follows:

А	Accumulator
A _n	The binary digit in position n of the A register
>	Transmit to
b	Index designator
B^{b}	Designated index register
Exit (Full)	Proceed to upper instruction of next program step
Half exit	Proceed to lower instruction of same program step
j	The condition designator for jump and stop instructions
k	Unmodified shift count
К	Modified shift count. $K = k + (B^b)$
LA	Lower address - execution address portion of lower instruction of a program step.
m	Unmodified operand address
М	Modified operand address. $M = m + (B^{b})$
()	Contents of a register or storage location
()'	One's complement contents of a register or storage location
()f	Final contents of a register or storage location
()i	Initial contents of a register or storage location
Q	Auxiliary arithmetic register
UA	Upper address
Х	Exchange register
У	Unmodified operand
Y	Modified operand. $Y = y + (B^b)$

Instruction Execution Time

The time needed to execute an instruction varies from application to application because of the following factors.

If the instruction occupies the upper position in an instruction word, the time needed to read the word from storage must be considered.

If consecutive storage references are made to the same storage unit (even-even or odd-odd) the read access time from storage will be maximized.

If indirect addressing is specified, at least one additional reference will be needed to complete the instruction. (The new index designator may itself specify indirect addressing.)

If an input-output request exists, the request will, in most cases, be processed before the next instruction is executed. (Refer to chapter three.)

If a storage reference is made at the end of the preceding instruction, execution of the next instruction may be delayed.

The instruction execution times listed on the following pages were compiled by averaging the times for a long list of the same instructions. The list was arranged for typical values of the factors.

Numeric Code	Mnemonic Code	Name	Timing*
DATA TRAN	SMISSION		
12	LDA	LOAD A	
13	LAC	LOAD A COMPLEMENT	
16	LDQ	LOAD Q	
17	LQC	LOAD Q COMPLEMENT	
20	STA	STORE A	7.2
21	\mathbf{STQ}	STORE Q	
52	LIU	LOAD INDEX (UPPER)	
53	LIL	LOAD INDEX (LOWER)	
56	SIU	STORE INDEX (UPPER)	
57	SIL	STORE INDEX (LOWER)	
SHIFTING			
01	ARS	A RIGHT SHIFT	
02	QRS	Q RIGHT SHIFT	
03	LRS	AQ RIGHT SHIFT	2.8 + .4s**
05	ALS	A LEFT SHIFT	2.01.15
06	QLS	Q LEFT SHIFT	
07	LLS	AQ LEFT SHIFT	
ADDRESS M	ODIFICATION		
60	SAU	SUBSTITUTE ADDRESS (UPPER)	7.2
61	SAL	SUBSTITUTE ADDRESS (LOWER)	7.2
54	ISK	INDEX SKIP	5.6
55	IJP	INDEX JUMP	4.4

.....

* Timing is average execution time in usec **s = Number of places shifted

ARITHMETIC (Fixed)

14	ADD	ADD	7.2
15	SUB	SUBTRACT	7.2
24	MUI	MULTIPLY INTEGER	25.2 + .8n*
25	DVI	DIVIDE INTEGER	65.2
26	\mathbf{MUF}	MULTIPLY FRACTIONAL	25.2 + .8n*
27	DVF	DIVIDE FRACTIONAL	65.2

ARITHMETIC (Floating)

30	FAD	FLOATING ADD	18.8
31	FSB	FLOATING SUBTRACT	18.8
32	\mathbf{FMU}	FLOATING MULTIPLY	36.0
33	FDV	FLOATING DIVIDE	56.0
34	SCA	SCALE A	2.8 + .4s**
35	SCQ	SCALE AQ	2.8 + .4s**

NO ADDRESS

U	ADDRESS		٦ ٦		
	04	\mathbf{ENQ}	ENTER Q		
	10	ENA	ENTER A		
	11	INA	INCREASE A	> 3	3.0
	50	ENI	ENTER INDEX		
	51	INI	INCREASE INDEX		

JUMPS AND STOPS (Normal)

22	AJP	A JUMP		
23	QJP	Q JUMP	Ş	7.2
75	\mathbf{SLJ}	SELECTIVE JUMP		
76	SLS	SELECTIVE STOP	J	

٦

* n = Number of ones in multiplier **s = Number of positions shifted

JUMPS AND	STOPS (Return)	2	
22	AJP	A JUMP		
23	QJP	Q JUMP	ζ	7.2
75	SLJ	SELECTIVE JUMP	(1.2
76	SLS	SELECTIVE STOP	J	
STORAGE TE	ST			
36	SSK	STORAGE SKIP		8.8
37	SSH	STORAGE SHIFT		12.8
LOGICAL				
40	SST	SELECTIVE SET)	
42	SCM	SELECTIVE COMPLEMENT	>	7.2
41	SCL	SELECTIVE CLEAR	J	
43	SSU	SELECTIVE SUBSTITUTE	Ĺ	
44	LDL	LOAD LOGICAL	ζ	7.4
45	ADL	ADD LOGICAL	[•• -
46	SBL	SUBTRACT LOGICAL	J	
47	STL	STORE LOGICAL		7.2
STORAGE SE	AKCH			

64	EQS	EQUALITY SEARCH		
65	THS	THRESHOLD SEARCH	Ş	4.0 + 3.6r*
66	\mathbf{MEQ}	MASKED EQUALITY		
6 7	MTH	MASKED THRESHOLD	J	

* r = Number of repeated executions

REPLACE

REFLACE			>
70	RAD	REPLACE ADD	
71	RSB	REPLACE SUBTRACT	13.2
72	RAO	REPLACE ADD ONE	
73	RSO	REPLACE SUBTRACT ONE	
TRANSFER)
			1

62	INT	INPUT TRANSFER	4.0 + 4.8r*
63	OUT	OUTPUT TRANSFER	
)

* r = Number of repeated executions

DATA TRANSMISSION

- Relative address modification does not take place during LIU, LIL, SIU or SIL instructions. Indirect addressing will occur if b=7. A b=0 condition effects a pass.
- 2) All modes of address modification apply to the remaining data transmission instructions.
- During the execution of data transmission instructions, one storage reference is made. If indirect addressing is designated, at least two storage references are made.

LDA b m 12 Load A 7.2 usec

Replaces the contents of A with a 48-bit operand contained in storage location M. The initial contents of A are changed during execution; the contents of M remain unchanged.

LAC b m 13 Load A Complement 7.2 usec Replaces the contents of A with the complement of a 48-bit operand contained in storage location M. The initial contents of A are changed during execution; the contents of M remain unchanged.

LDQ b m 16 Load Q 7.2 usec Replaces the contents of Q with a 48-bit operand contained in storage location M. The initial contents of Q are changed during execution; the contents of address M remain unchanged.

LQC b m 17 Load Q Complement 7.2 usec Replaces the contents of Q with the complement of a 48-bit operand contained in storage location M. The initial contents of Q are changed during execution; the contents of address M remain unchanged.

STA b m 20 Store A

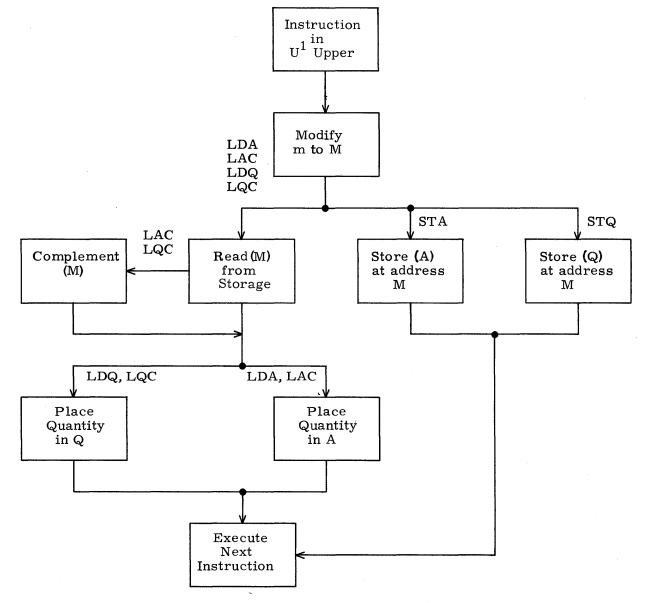
7.2 usec

Replaces the contents of the designated storage location, M, with the contents of A. The initial contents of A remain unchanged.

STQ b m 21 Store Q

7.2 usec

Replaces the contents of the designated storage location, M, with the contents of Q. The initial contents of Q remain unchanged.

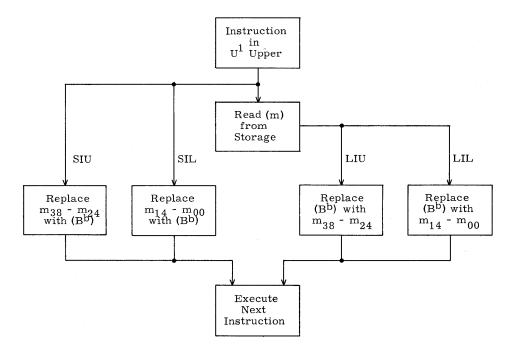


LDA, LAC, LDQ, LQC, STA, and STQ

LIU b m 52 Load Index Upper 7.2 usec
Replaces the contents of the designated index register with the upper address portion of storage location m. If b = 0 this instruction becomes a pass (do nothing) instruction. Initial contents of m remain unchanged.

LIL b m53Load Index Lower7.2 usecReplaces the contents of the designated index register with the lower addressportion of storage location m.If b = 0 this instruction becomes a pass (do nothing)instruction.Initial contents of m remain unchanged.

- SIU b m 56 Store Index Upper 7.2 usec Replaces the upper address portion of storage location m with the contents of the designated index register. The remaining bits of the word in storage remain unchanged. If b = 0, (m_{ua}) is cleared. Initial contents of B^b remain unchanged.
- SIL b m 57 Store Index Lower 7.2 usec
 Replaces the lower address portion of storage location m with the contents of the designated index register. The remaining bits of the word in storage remain unchanged. If b = 0, (m_{la}) is cleared. Initial contents of B^b remain unchanged.



LIU, LIL, SIU, and SIL

SHIFTING

- 1) All modes of address modification apply to these instructions.
- If the modified shift count, K, is greater than 127₁₀, a fault indicator is set. Regardless of the magnitude of count, however, the required number of shifts is executed. (K is reduced by one count for each shift executed and when K = 0, shifting stops.)
- 3) Shifting must be completed before an input-output or interrupt request can be processed. (See chapter three.)

ARS b k 01 A Right Shift 2.8 + .4s* usec
Shifts contents of A to the right K places. The sign is extended and the lower bits
are discarded. The largest practical shift count is 47₁₀ since the register is now
an extension of the sign bit.

QRS b k 02 Q Right Shift 2.8 + .4s usec Shifts contents of Q to the right K places. The sign is extended and the lower bits are discarded. The largest practical shift count is 47₁₀ since the register is now an extension of the sign bit.

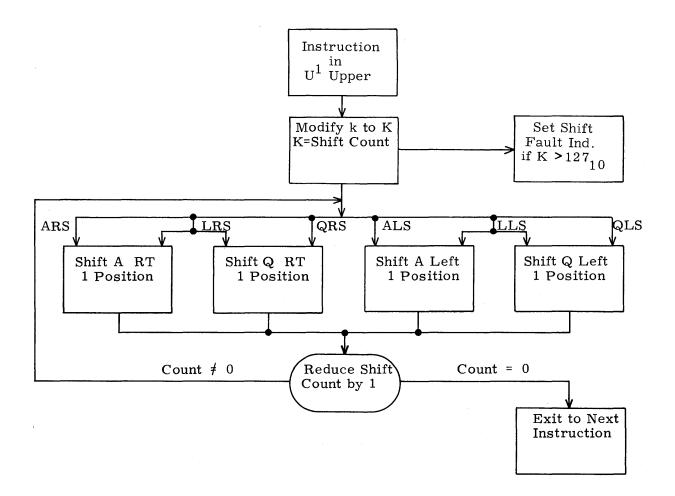
LRS b k 03 Long Right Shift 2.8 + .4s usec
Shifts contents of AQ to the right K places as one 96-bit register. The A register is considered as the leftmost 48 bits and the Q register as the rightmost 48 bits. The sign of A is extended. The lower order bits of A replace the higher order bits of Q and the lower order bits of Q are discarded. The largest practical shift count is 95₁₀ since AQ is now an extension of the sign of A.

ALS bk 05 A Left Shift 2.8 + .4s usec
Shifts contents of A to the left K places, left circular. The higher order bits of A replace the lower order bits. The largest practical shift count 48₁₀ returns the register to its original state.

* s = Number of positions shifted

QLS bk 06 Q Left Shift 2.8 + .4s usec Shifts contents of Q to the left K places, left circular. The higher order bits of Q replace the lower order bits. The largest practical shift count 48₁₀ returns the register to its original state.

LLS b k 07 Long Left Shift 2.8 + .4s usec
Shifts contents of AQ to the left K places, left circular, as one 96-bit register.
The higher order bits of A replace the lower order bits of Q and the higher order
bits of Q replace the lower order bits of A. The largest practical shift count 96₁₀ returns AQ to its original state.



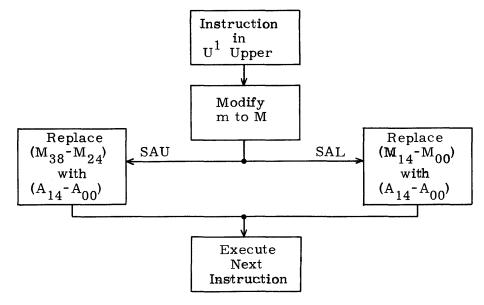
Shift Instructions

ADDRESS MODIFICATION

- 1) All modes of address modification apply to SAU and SAL instructions.
- Relative address modification does not take place during ISK or IJP instructions. Indirect addressing occurs if b=7, and a pass occurs if b=0.
- 3) During execution of ISK and IJP instructions, no storage reference is made unless indirect addressing is specified which requires at least one reference. For SAU and SAL instructions, one reference is always made. If indirect addressing is designated, at least one additional reference will be needed to complete the instruction.

SAU b m 60 Substitute Address Upper 7.2 usec
 Replaces the upper address portion of M with the lower order 15 bits of A.
 Remaining bits of M are not modified and the initial contents of A are unchanged.

SAL b m61Substitute Address Lower7.2 usecReplaces the lower address portion of M with the lower order 15 bits of A.Remaining bits of M are not modified and the initial contents of A are unchanged.



SAU and SAL

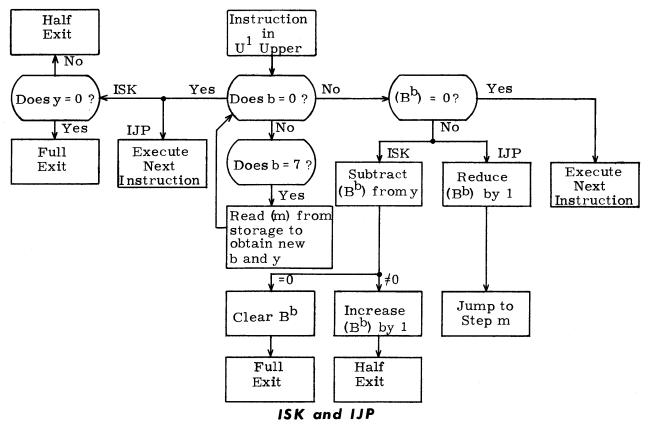
2 - 16

ISK by 54 Index Skip 5.6 usec Compares (B^b) with y. If the two quantities are equal, B^b is cleared and a full exit is performed. If the quantities are unequal, (B^b) is increased one count in the R register and a half exit is performed. Because the R register is a two's complement subtractive counter, it is possible to count through negative zero and positive zero. (See appendix.) If b = 0 and y \neq 0, a half exit is taken. If b = 0 and y = 0, a full exit is taken. ISK is usually restricted to the upper instruction. If used as a lower instruction it will half exit upon itself until the full exit condition is satisfied. If b = 0 and y \neq 0, the condition will never be satisfied.

IJP b m 55 Index Jump

4.4 usec

Examines (B^b). If this quantity is not zero, the quantity is reduced one count and a jump is executed to program step m. The counting operation is performed in the R register but negative zero is not generated because IJP terminates at positive zero. (See appendix.) The index jump can be used in the upper or lower instruction without reservation; it executes a normal jump upon satisfaction of the jump condition.



ARITHMETIC

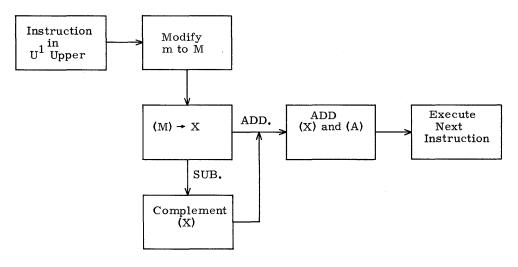
- 1) All modes of address modification apply to these instructions.
- 2) One storage reference is made for each instruction unless indirect addressing is designated. In this case, at least two references are made.
- 3) If the capacity of the A register $\pm (2^{47}-1)$ is exceeded during the execution of the instructions an arithmetic overflow fault is produced. When executing the DVI or DVF instructions, if the result exceeds the capacity of the Q register $\pm (2^{47}-1)$ a divide fault is produced. (Refer to appendix.)

ADD b m14Add7.2 usecAdds a 48-bit operand obtained from storage location M to contents of A. A negative
zero may be produced by this instruction if (A) and (M) are initially negative zero.
The contents of storage address M remain unchanged.

SUB b m 15 Subtract

7.2 usec

Obtains a 48-bit operand from storage location M and subtracts it from the initial contents of A. A negative zero will be produced if the initial contents of A are negative zero and that of storage location M are positive zero. The contents of address M remain unchanged.

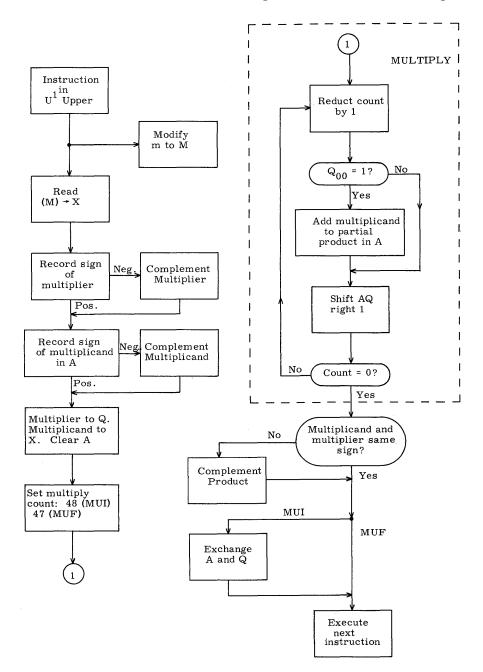


ADD and SUB

FIXED

2-18

MUI b m 24 Multiply Integer 25.2 + .8n* usec Forms a 96-bit product from two 48-bit operands. The multiplier must be loaded into A prior to execution of the instruction. The execution address specifies the storage location of the multiplicand. The product is contained in QA as a 96-bit quantity. The operands are considered as integers and therefore the binary point is assumed to be at the lower order (right hand) end of the A register.

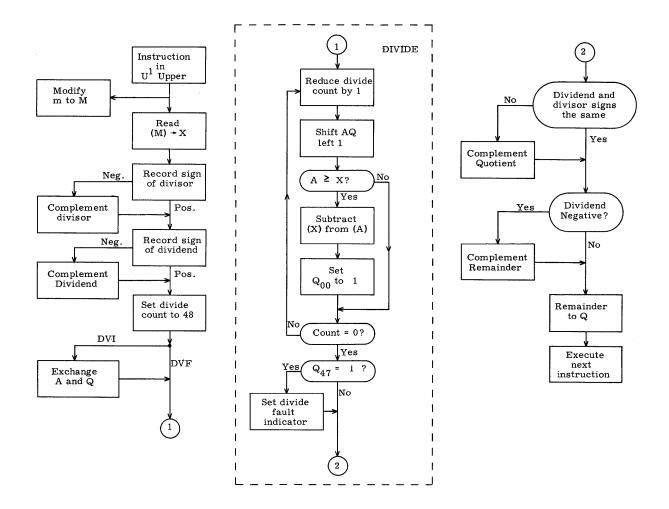


MUI and MUF

2 - 19

^{*} n = Number of ones in multiplier

DVI b m 25 Divide Integer 65.2 usec Divides a 96-bit integer dividend by a 48-bit integer divisor. The 96-bit dividend must be formed in the QA register prior to executing the instruction. If a 48-bit dividend is loaded into A, the sign of Q must be set. That is, the sign of the dividend in A must be extended throughout Q. The 48-bit divisor is read from the storage location specified by the execution address. The quotient is formed in A and the remainder is left in Q at the end of the operation. Dividend and remainder have the same sign.



DVI and DVF

MUF b m26Multiply Fractional25.2 + .8n* usecForms a 96-bit product from two 48-bit operands. The operands are treated as
fractions with the binary point immediately to the right of the sign bit. The
multiplier must be loaded into A prior to executing the instruction. The multipli-
cand is read into X from the storage location specified by M. The 96-bit product
is contained in AQ.

DVF b m 27 Divide Fractional 65.2 usec Divides a 96-bit quantity by a 48-bit divisor. All operands are treated as fractions with the binary point immediately to the right of the sign bit. The 96-bit dividend must be loaded into AQ prior to executing this instruction. If a 48-bit dividend is loaded into Q, the sign of Q must be extended throughout A. At the end of this operation the quotient is left in A and the remainder in Q. Remainder and dividend have the same sign.

- 1) Refer to appendix for a discussion of floating point format.
- 2) All modes of address modification apply.

FLOATING

- One storage reference is made unless indirect addressing is designated. In this case, at least two references are made.
- Floating point range faults (overflow-underflow) occur if the exponent exceeds 2¹⁰-1 in absolute value. Refer to appendix.

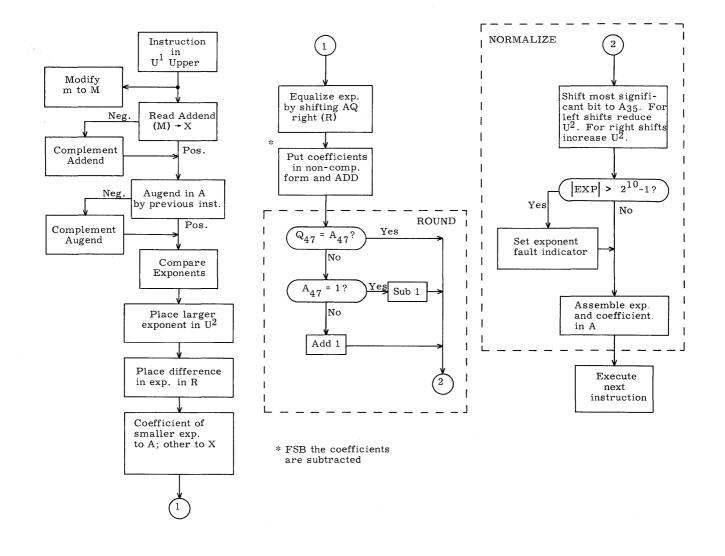
FAD b m 30 Floating Add 18.8 usec

Forms the sum of two operands packed in floating point format. A floating point operand is read from storage location M and added to the floating point word in A. The result is normalized, rounded, and retained in A at the end of the operation. Q contains only the residue of the rounding operation at the end of the sequence.

^{*} n = Number of ones in multiplier

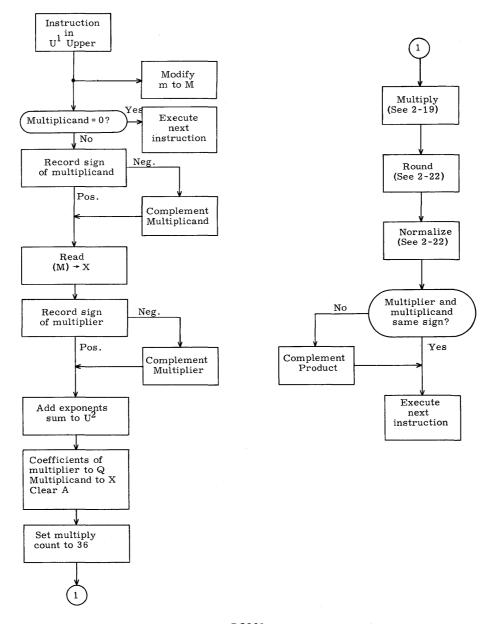
FSB b m 31 Floating Subtract 18.8 usec
Forms the difference of two 48-bit operands in floating point format. The subtrahend is acquired from storage address M and is subtracted from the minuend in A. The result is rounded and normalized if necessary and retained in A. The residue from the rounding operation is left in Q at the end of the sequence.

The basic steps executed in a FSB are the same as those for FAD except the coefficients are subtracted rather than added.



FAD and FSB

FMU b m 32 Floating Multiply 36.0 usec
Forms the product of an operand in floating point format with the previous contents of A also in floating point format. The operand is read from storage location M. The product is rounded and normalized if necessary and retained in A. The residue from the rounding operation is left in Q at the end of the sequence.

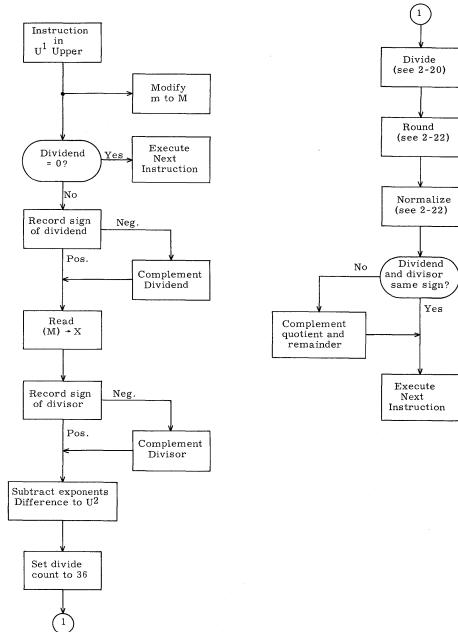


FMU

FDV b m 33 Floating Divide

56.0 usec

Forms the quotient of two 48-bit operands in floating point format. The dividend must be loaded into A prior to executing this instruction. The divisor is read from the storage location specified by M. The quotient is rounded and normalized if necessary and retained in A at the end of the operation. The residue from the rounding operation is left in Q at the end of the operation.





- 1) Address modification does not apply. Rather, the index register is used to preserve the scale factor.
- If b = 0, scaling is executed but the scale factor is lost. 2)
- If b = 7, indirect addressing is used and at least one storage 3) reference is made.

If (A)i is already scaled or equal to positive or negative 4) zero, $k \rightarrow B^{b}$ and scaling is not executed.

- If the execution address is initially equal to 0, B^b is cleared 5) and no scaling takes place.
- The shift fault indicator is not affected by this instruction. 6)

2.8 + .4s usec

Scale A 2.8 + .4s* usec Shifts A left circularly until the most significant digit is to the right of the sign bit or until k = 0. Shift count k is reduced by one for each shift and terminates when k = 0 or the most significant digit is to the right of the sign bit. Upon termination the count (scale factor) is entered in the designated index register.

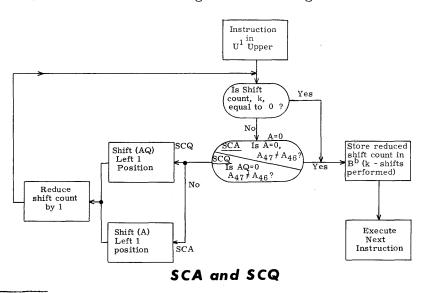
SCQ b k 35 Scale AQ

34

SCALE

SCA b k

Shifts AQ left circularly until the most significant digit is to the right of the sign bit. Shift count k is reduced by one for each shift. Operation terminates when k = 0 or the most significant digit is to the right of the sign bit. Upon termination the count (scale factor) is entered in the designated index register.



* s = Number of positions shifted

2 - 25

NO ADDRESS

- 1) All modes of address modification apply to ENQ, ENA, and INA instructions.
- Address modification does not take place during ENI and INI instructions. The only mode recognized is indirect addressing.
- No storage reference is made during these instructions unless indirect addressing is designated. In this case, at least one storage reference is made.

ENQ b y 04 Enter Q 3.0 usec

The 15-bit operand, Y, is entered into Q and its highest order bit is extended in the remaining 33 bits. The largest positive 15-bit operand that can be entered into Q is 37777_8 (2¹⁴-1) and its "0" bit will be duplicated in each of the remaining 33 bits of Q. Negative zero will be formed in Q if:

1) (B^b) =
$$77777_8$$
 and y = 77777_8 or
2) b = 0 and y = 77777_8 .

ENAby 10 Enter A

3.0 usec

3.0 usec

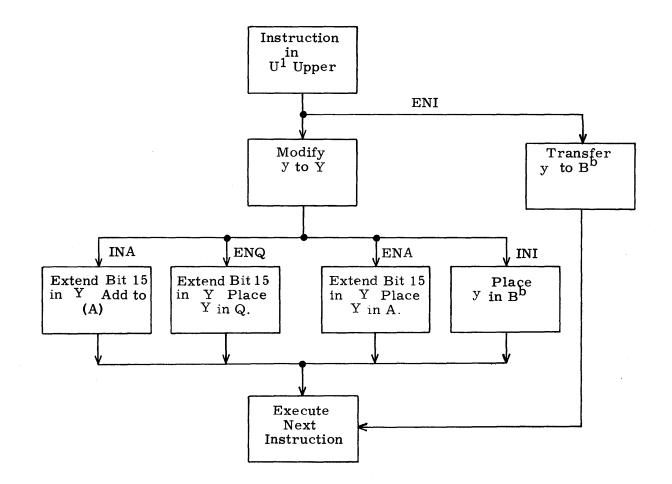
The 15-bit operand, Y, is entered into the A register and its highest order bit is extended in the remaining 33 bits. The largest positive 15-bit operand that can be entered into A is 37777_8 (2¹⁴-1) and the "0" bit will be duplicated in each of the remaining 33 bits. Negative zero will be formed in A if:

1) $(B^b) = 77777_8$ and $y = 77777_8$ or 2) b = 0 and $y = 77777_8$.

INA by 11 Increase A

Adds Y to A. The 15-bit operand Y is placed in X and its highest order bit is extended in the remaining 33 bits. The operand in X is added to (A).

- **ENI b y** 50 Enter Index 3.0 usec Replaces (B^b) with the operand y. If b = 0, this instruction becomes a pass (do nothing) instruction.
- INI b y 51 Increase Index 3.0 usec Increases (B^b) by the operand y. If the b designator is zero, this instruction becomes a pass (do nothing) instruction.



No Address

JUMPS AND STOPS

1) Address modification does not apply to these instructions.

NORMAL

2) One storage reference is made.

Jump

A jump instruction causes a current program sequence to terminate and initiates a new sequence at a different location in storage. The Program Address register, P, provides the continuity between program steps and always contains the storage location of the current program step.

When a jump instruction occurs, P is cleared and a new address is entered. In all jump instructions, the execution address, m, specifies the beginning address of the new program sequence. The word at address m is read from storage, placed in U^1 and the upper instruction (first instruction of the new sequence) is executed.

Some of the jump instructions are conditional upon a register containing a specific value or upon the position of an operator's jump or stop key on the console. If the criterion is satisfied, the jump is made to location m. If it is not satisfied, the program proceeds in its regular sequence to the next instruction.

A jump instruction may appear in either position in a program step. If the jump instruction appears in the first (upper) part of the program step and the jump is taken, the second (lower) part of the program step is not executed. If the instruction appears in the lower part, the upper part is executed in the normal manner.

AJP jm 22 A Jump

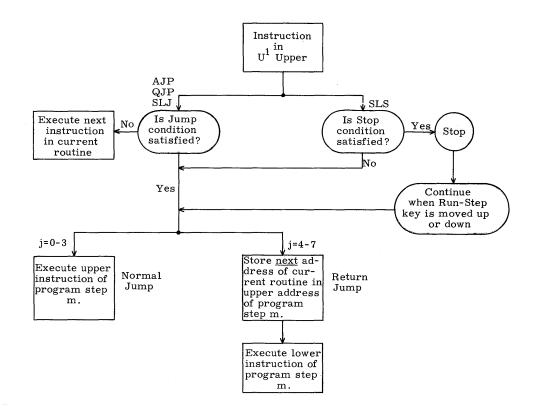
7.2 usec

Jumps to m if the conditions of the A register specified by the jump designator, j, exist. If not, the next instruction is executed.

j = 0 Jump if (A) = 0
j = 1 Jump if (A) ≠ 0
j = 2 Jump if (A) = +
j = 3 Jump if (A) = -

When (A) is negative zero the interpretation is:

- j = 0 The jump is executed because, in this case, negative zero is recognized as positive zero.
- j = 1 The jump is not executed.
- j = 2 The jump is not executed because the sign bit is a "1".
- j = 3 The jump is executed because the sign bit is a "1".



AJP, QJP, SLJ, and SLS

QJP jm 23 Q Jump

7.2 usec

Jumps to m if the condition of the Q register specified by the jump designator, j, exists. If not, the next instruction is executed.

j = 0 Jump if (Q) = 0
j = 1 Jump if (Q) ≠ 0
j = 2 Jump if (Q) = +
j = 3 Jump if (Q) = -

When (Q) is negative zero the AJP interpretation applies.

SLJ j m

75 Selective Jump 7.2 usec Jumps to m if the condition of the jump keys specified by j exists. If not, the next instruction is executed.

j = 0 Jump unconditionally j = 1 Jump if jump key 1 is set j = 2 Jump if jump key 2 is set j = 3 Jump if jump key 3 is set

SLS j m 76 Selective Stop

7.2 usec

Stops at present step in the sequence if the condition of the stop key specified by j exists. If the stop condition exists, the stop is executed, and the jump is executed unconditionally when the Run-Step key is moved to the run or step position. If the stop condition is not satisfied, the jump is executed unconditionally.

j = 0 Stop unconditionally j = 1 Stop if stop key 1 is set j = 2 Stop if stop key 2 is set j = 3 Stop if stop key 3 is set

1) Address modification does not apply to these instructions.

RETURN JUMP

2) One storage reference is made.

A return jump begins a new program sequence at the lower instruction portion of the program step to which the jump is made. At the same time, the address portion of the upper instruction of that program step is replaced with the address of the next program step in the main program. This instruction allows a return to the main program after completing the subprogram sequence.

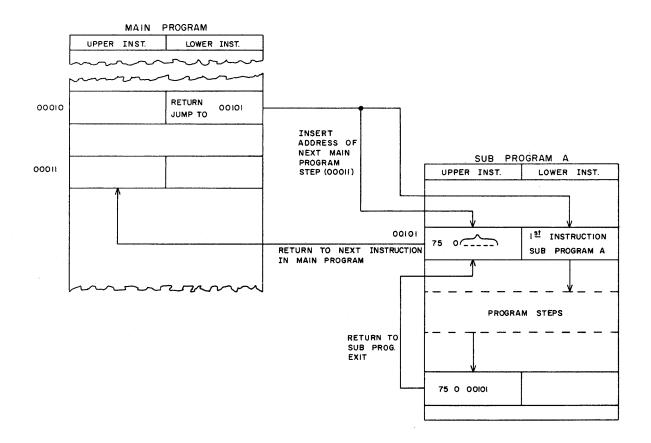
AJP j m 22 A Jump

7.2 usec

Executes a return jump to storage location m if the condition of the A register specified by j exists. If not, the next instruction is executed.

- j = 4 Return jump if (A) = 0
- j = 5 Return jump if (A) $\neq 0$
- j = 6 Return jump if (A) = +
- j = 7 Return jump if (A) = -

Note: If (A) = negative zero, refer to the AJP instruction.



Return Jump

QJP jm 23 Q Jump

7.2 usec

Executes a return jump to storage location m if the condition of the Q register specified by j exists. If not, the next instruction is executed.

j = 4 Return jump if (Q) = 0

- j = 5 Return jump if (Q) $\neq 0$
- j = 6 Return jump if (Q) = +
- j = 7 Return jump if (Q) = -

Note: If (Q) = negative zero, refer to the AJP instruction.

SLJ j m 75 Selective Jump

7.2 usec

Executes a return jump to storage location m on condition j where condition j represents the setting of the jump keys. If the condition is not satisfied, the next instruction is executed.

- j = 4 Return jump unconditionally
- j = 5 Return jump if jump key 1 is set
- j = 6 Return jump if jump key 2 is set
- j = 7 Return jump if jump key 3 is set

Note: The set position of a jump key is in the up position.

SLS j m 76 Selective Stop

7.2 usec

Stops on condition j and executes a return jump to storage location m if the Run-Step key is moved in the run or step position. If the stop condition is satisfied, the stop is executed and the return jump is executed when the Run-Step key is moved in either position. If the stop condition is not satisfied, the stop is not executed and the return jump is executed unconditionally.

- j = 4 Stop unconditionally
- j = 5 Stop if stop key 1 is set
- j = 6 Stop if stop key 2 is set
- j = 7 Stop if stop key 3 is set

STORAGE TEST

1) All modes of address modification apply to these instructions.

12.8 usec

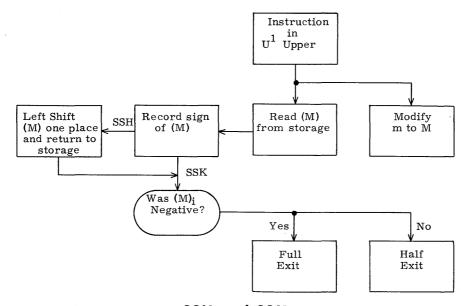
2) At least one storage reference is made unless indirect addressing is designated in which case at least two storage references are made.

SSK b m 36 Storage Skip 8.8 usec

Senses the sign bit of the operand in storage location M. If the sign is negative, a full exit is taken. If the sign is positive, a half exit is taken. The contents of the operational registers are left unmodified. SSK is usually restricted to an upper instruction. If used as a lower instruction and the sign of (M) is negative, a full exit will be executed. If the sign is positive, it will half exit upon itself and never execute a full exit.

SSH b m 37 Storage Shift

Senses the sign bit of the quantity in storage location M. If the sign bit is negative a full exit is taken, and if the quantity is positive a half exit is taken. In either case the quantity is shifted left circularly one bit before the exit. This instruction is usually restricted to the upper position. If used as a lower instruction and the sign of (M) is positive, the instruction will half exit upon itself until a negative sign bit is found. The contents of the operational registers are left unmodified.



SSH and SSK

LOGICAL

- 1) All modes of address modification apply to these instructions.
- 2) The LDL, ADL, SBL and STL instructions achieve their result by forming a logical product. A logical product is a bit by bit multiplication of two binary numbers (logical AND condition):

$0 \ge 0 = 0$	$1 \ge 0 = 0$
$0 \ge 1 = 0$	$1 \times 1 = 1$

- 3) A logical product is used, in many cases, to select specific portions of an operand for entry into another operation. For example, if only a specific portion of an operand in storage is to be added to (A), as the operand passes through X it is subjected to a mask comprised of a predetermined pattern of "0's" and "1's". Forming the logical product of (X) and the mask causes X to retain the original contents only in those stages which have corresponding "1's" in the mask. When only the selected bits remain in X, the instruction proceeds to conclusion.
- SST b m 40 Selective Set 7.2 usec
 Sets the individual bits of A to "1" where there are corresponding "1's" in the word at storage location M. "0" bits in the word at storage location M do not modify the corresponding bits in A. In a bit by bit comparison of (A) and (M) there are four possible combinations of bits.

1)	$(A)_{i} = 1$	2) (A) _i = 1	3) (A) _i = 0	4) (A) _i = 0
	(M) _i = 1	$(\mathbf{M})_{i} = 0$	$(M)_{i} = 1$	$(M)_{i} = 0$
	(A) _f = 1	$(A)_{f} = 1$	$(A)_{f} = 1$	$(A)_{f} = 0$
	$(M)_{f} = 1$	$(\mathbf{M})_{\mathbf{f}} = 0$	$(M)_{f} = 1$	$(\mathbf{M})_{\mathbf{f}} = 0$

SCM b m42Selective Complement7.2 usec

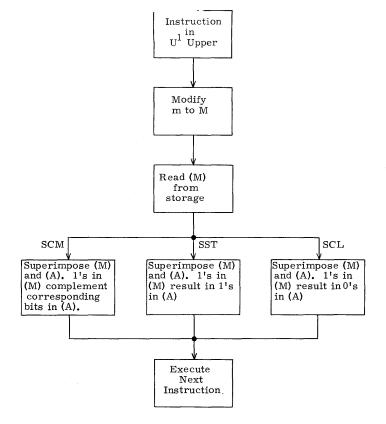
Individual bits of A are complemented where there are corresponding '1's" in the word at storage location M. If the corresponding bits at M are ''0's", the associated bits of A remain unchanged.

$(A)_{i} = 1$ (M)_{i} = 1	$(A)_{i} = 1$ $(M)_{i} = 0$	$(A)_{i} = 0$ $(M)_{i} = 1$	$(A)_{i} = 0$ $(M)_{i} = 0$
$(A)_{f} = 0$ $(M)_{f} = 1$	$(A)_{f} = 1$ $(M)_{f} = 0$	$(A)_{f} = 1$ $(M)_{f} = 1$	$(A)_{f} = 0$ $(M)_{f} = 0$

SCL b m	41	Selective Clear	7.2 usec	
Clear	s individual	bits of A where there	e are corresponding ''1's'' in the word at	Ċ
stora	ge location	M. If the correspond	ding bits at M are ''0's'', the associated bi	its of
A rer	nain unchan	ged.		

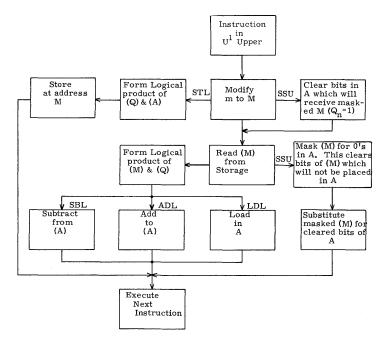
In a bit by bit comparison of (A) and (M) there are four possible combinations of bits.

$(A)_{i} = 1$ (M)_{i} = 1	$(A)_{i} = 1$ $(M)_{i} = 0$	$(A)_{i} = 0$ $(M)_{i} = 1$	$(A)_{i} = 0$ $(M)_{i} = 0$
$(A)_{f} = 0$ $(M)_{f} = 1$	$(A)_{f} = 1$ $(M)_{f} = 0$	$(A)_{f} = 0$ $(M)_{f} = 1$	$(A)_{f} = 0$ $(M)_{f} = 0$



SCM, SST, and SCL

- 7.4 usec SSU b m 43 Selective Substitute Substitutes selected portions of an operand at storage address M into the A register where there are corresponding "1's" in the Q register (mask). The portions of A not masked by "1's" in Q are left unmodified.
- LDL b m 7.4 usec 44 Load Logical Loads A with the logical product of Q and the contents of the designated storage location, M. The operand can be in either Q or M.
- ADL b m 7.4 usec 45 Add Logical Adds to A the logical product of Q and the quantity in location M; the mask may be in Q or storage. Once the logical product is formed addition follows normal rules (appendix).
- SBL b m 46 7.4 usec Subtract Logical Subtracts from A the logical product of the Q register and the quantity in storage The mask may be in Q or storage. When the logical product is formed, location M. the subtraction proceeds in the normal manner. (See appendix.)
- STL b m 47 Store Logical Replaces the bits in storage location M with the logical product of Q and A registers. Neither (A) nor (Q) are modified. The mask may be located in A or Q.



ADL, LDL, SBL, SSU, and STL

2 - 36

7.2 usec

STORAGE SEARCH

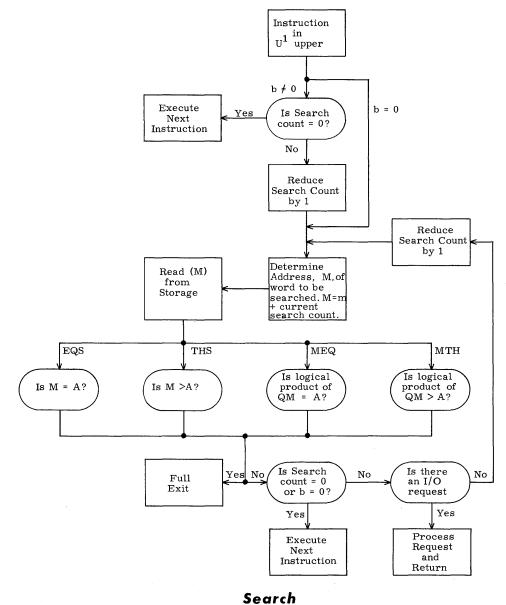
- If b = 0 in the following instructions only the word at storage location m will be searched.
- If b = 7, indirect addressing is used to obtain the execution address and b designator.
- 3) If $(B^b) = 0$, no search is made.

EQS b m 64 Equality Search 4.0 + 3.6r* usec Searches a list of operands to find one that is equal to A. The number of items to be searched is specified by B^b . These items are in sequential addresses beginning at the location specified by m. The search begins with the last address, $m + B^b - 1$. B^b is reduced one count for each word that is searched until an operand is found that equals A or until B^b equals zero. If the search is terminated by finding an operand that equals A, a full exit is made. The address of the operand satisfying this condition is given by the sum of m and the final contents of B^b . If no operand is found that equals A, a half exit is taken. Positive zero and minus zero are recognized as the same quantity. When EQS is used as a lower instruction, the next instruction will always be executed when the search terminates.

THS b m 65 Threshold Search 4.0 + 3.6r usec Searches a list of operands to find one that is greater than A. The number of items to be searched is specified by B^b. These items are located in sequential addresses beginning at the location specified by m. The search begins with the last address, $m + B^{b}$ - 1. The content of the index register is reduced by one for each operand examined. The search continues until an operand is reached that is greater than A or until B^b is reduced to zero. If the search is terminated by finding an operand greater than the value in A, a full exit is performed. The address of the operand satisfying the condition is given by the sum of m and the final contents of B^b . If no operand in the list is greater than the value in A, a half exit is performed. If THS is used as a lower instruction, the next instruction will be executed when search terminates. In the comparison made here positive zero is considered as greater than minus zero.

* r = Number of words searched

- MEQ b m 66 Masked Equality Search 4.0 + 3.6r* usec Searches a list of operands to find one such that the logical product of (Q) and (M) is equal to (A). This instruction, except for the mask, operates in the same manner as an equality search.
- MTH b m 67Masked Threshold Search4.0 + 3.6r usecSearches a list of operands to find one such that the logical product of (Q) and (M)is greater than (A). Except for the mask, this instruction operates in the samemanner as the threshold search.



* r = Number of words searched

REPLACE

- 1) All modes of address modification apply to these instructions.
- During the execution of the replace instructions, two storage references are made. If indirect addressing is designated, at least three references are made.
- 3) If the capacity of the A register $\pm (2^{47}-1)$ is exceeded during the execution of the following instructions, an arithmetic overflow fault is produced. (Refer to appendix.)

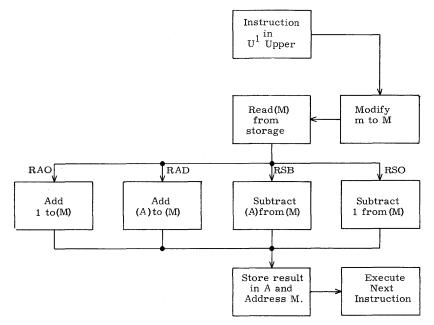
RAD b m70Replace Add13.2 usecObtains a 48-bit operand from storage location M and adds it to the initial contents
of A. The sum is left in A and is also transmitted to location M.

RSB b m71Replace Subtract13.2 usecSubtracts (A) from (M) and places the result in both the A register and location M.

RAO b m 72 Replace Add One

13.2 usec

Replaces the operand in storage location M with its original value plus one. The result is also placed in A.

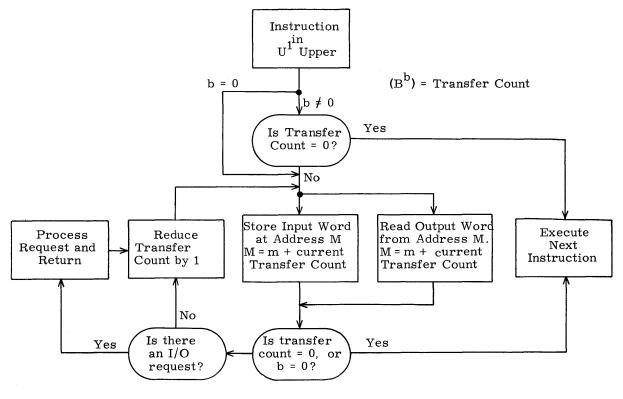


Replace

RSO b m73Replace Subtract One13.2 usecReplaces the operand in storage location M with its original contents minus one.The difference is also left in A; the original contents of A and M are destroyed.

TRANSFER

- Address modification does not take place in the following instructions. The only mode recognized is indirect addressing.
- 2) The index registers contain the number of words to be transferred into or out of the computer via channel 7.
- When a transfer is in progress all other computer operations stop except the processing of input-output requests. (See chapter three.)
- 4) If b = 0, one word is transferred to or from address m.



Transfer

INT b m 62 Input Transfer 4.0 + 4.8r* usec Transfers a block of data from an external equipment into storage. The number of words to be transferred is specified by B^b. These words are stored in sequential addresses beginning at the location specified by the execution address, m. The transfer begins by storing the first input word in the last address in the sequence, $m + B^b - 1$. As each word is transferred, B^b is reduced by one until it is equal to zero.

OUT b m 63 Output Transfer 4.0 + 4.8r usec Transfers a block of data from computer storage to an external equipment. The number of words to be transferred is specified by B^b . The words to be transferred are located in sequential addresses beginning at the location specified by the execution address, m. The transfer begins by obtaining the first output word from the last address, m + B^b -1. As each word is transferred B^b is reduced by one until it is equal to zero.

3

Input-Output

METHODS OF DATA EXCHANGE

The computer communicates with external equipment via a single transfer channel or six buffer channels. The transfer channel which provides for very high speed communication is program initiated and controlled. The buffer channels provide for the normal exchange of data and, although program initiated, operate independently of the program.

HIGH SPEED TRANSFER CHANNEL

The high speed transfer channel (channel 7) handles both input and output communications between computer and high speed equipments. Information is transferred between the computer and external equipment in blocks at a word by word rate. The transfer rate is usually dependent on the speed of the external equipment as the computer can perform transfers at a maximum (approximate) rate of one word every 5 microseconds.

As many as 8 different equipments (optimum conditions) may be connected to the transfer channel. However, only one equipment can use the channel at any given instant and the current transfer operation must continue to completion before a different equipment can use the channel.

BUFFER CHANNELS

The six independent buffer channels are grouped in three pairs:

Input:	Channel 1	Output:	Channel 2
	Channel 3		Channel 4
	Channel 5		Channel 6

Every external equipment is connected to one of these pairs. All six buffer channels may be concurrently transmitting information. However, only one external equipment can use any one buffer channel at a given instant. The rate of data flow on the buffer channels is, as with the transfer channel, dependent on the operating speed of the external equipment.

INITIATION AND CONTROL OF DATA EXCHANGE

TRANSFER

A transfer operation is initiated and controlled by the computer program. An INT or OUT instruction transfers the number of words designated by the contents of an index register. The starting storage location of the transfer is specified by the execution address of the instruction. (Refer to chapter 2 for a discussion of the INT or OUT instructions.)

Once initiated, the transfer operation continues to completion. While the transferring of words is in progress all computer operations stop except the processing of buffer input-output requests. (Refer to pages 3-5 and 3-6.)

BUFFER

A buffer operation is program initiated but, in contrast to transfer operations, proceeds under controls that are independent of the main program.

Buffer Control Word

Information is buffered in blocks at a word by word rate. The initial and terminal storage addresses of the block comprise the buffer control word. Each of the six buffer channels has an assigned storage address which holds the buffer control word.

Address of Control Word	Channel
00001	1
00002 00003	2 3
00004 00005	4 5
00006	6

Buffer Control Word

47	38		24 14	C	00	BIT POSITION
	IOT SED	STARTING ADDRESS	NOT USED	TERMINAL		

The terminal address is one greater than the last address to be used in the buffer. Prior to initiating a buffer operation, the terminating address must be entered into the lower address of the control word. The starting address is automatically entered into the word when the buffer is initiated by an EXF instruction.

External Function (EXF) Instructions

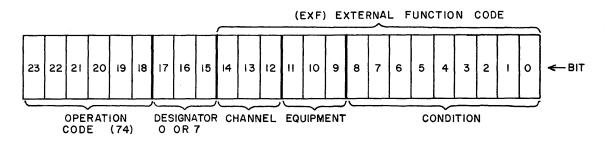
The EXF instructions initiate a buffer, sense for specified conditions, and select operations and equipment. EXF codes are listed in appendix 6.

There are three kinds of external instructions:

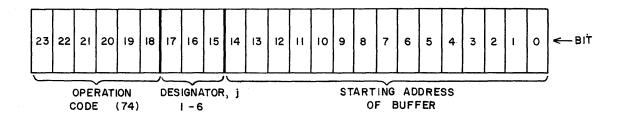
Select	74 0 XXXXX
Sense	74 7 XXXXX
Activate	74 j XXXXX

The composition of an external function instruction is shown below.





Activate



The 74 0 (EXF Select) instructions select the external equipment which is to communicate with the computer and/or its mode of operation. The select instructions do not activate the buffer but, rather, establish initial operating conditions within the designated equipment so that information will be properly processed when the buffer is activated.

The EXF 7 instructions sense the condition of an external equipment or the internal conditions (faults) of the computer and will execute a full exit or half exit depending on the presence or absence of the condition.

The location of a 74 7 y instruction within an instruction word determines whether a skip or a wait will be performed.

When used in the upper instruction position (Example 1) a 74 7 y is a skip instruction.

Example 1 :	(00010)	74 7 00010	75 0 40000
	(00011)	53 1 00005	16 1 00032

In this example the translation of the upper instruction of a program step 00010 is Exit on Channel 1 active. If channel 1 is active the next instruction to be executed would be the upper instruction of step 00011, i.e., 53 1 00005. If channel 1 were inactive, the lower instruction of step 00010 would be executed.

When used in the lower position (Example 2) a 74 7 y is a wait instruction.

Example $2:$	(00100)	$74\ 2\ 00600$	$74 \ 7 \ 00021$
	(00101)	54 2 00005	75 0 00072

In this case, the translation of the lower instruction of step 00100 is Exit on Channel 2 inactive. If channel 2 is inactive a full exit is performed to the next pair of instructions, program step 00101. If, however, the channel is active, the instruction half exits and repeats itself until the channel becomes inactive. The sensing of conditions in no way alters the condition.

The EXF j instructions activate buffer channel j where j equals 1-6. The execution address of the instruction, y, must designate the starting address of the region in storage. These instructions are the only instructions which can initiate a buffer.

The following steps should be completed prior to initiating a buffer operation.

- 1) Sense for: (a) equipment ready and (b) channel inactive.
- 2) Select the external equipment and its mode of operation.
- 3) Substitute the terminal address into the buffer control word.

An equipment is ready if there is no motion, that is, a transmission is not taking place.

A buffer channel is active while data is being buffered. A buffer channel is inactive if the previous input-output operation has been completed.

The buffer must be satisfied (starting address = terminating address) to inactivate the channel. This can be accomplished by activating the channel (74 j instruction) at the terminating address. This makes the channel inactive but no additional information is transmitted.

Buffer Scanner

Data exchange on each of the separate buffer channels is initiated by the program but proceeds under a control that is independent of the main program. This control is the buffer scanner.

The buffer scanner prevents one external equipment from dominating all others by sequentially monitoring the six buffer channels, the interrupt line and the real time clock to sense when any of these require action. When one of the positions demands action, the scanner stops. One word is processed and the scanner is released to resume its monitoring. If none of the positions demand action, a full scan is made in 3.2 usec. If, however, all eight channels demand processing at the same time, the time lapse for processing successive words on the same channel will be 200 usec.

Figure 3-1 shows the relationship between executing instructions and recognizing action requests (input-output requests) from the buffer channels, interrupt line and real time clock. During the time an input-output request is being processed, the scanner is released and resumes monitoring. Four more channels are scanned before the processing of the request is completed. If the scanner halts (indicating one of the four channels demands action) this request will be processed before the main program is allowed to continue.

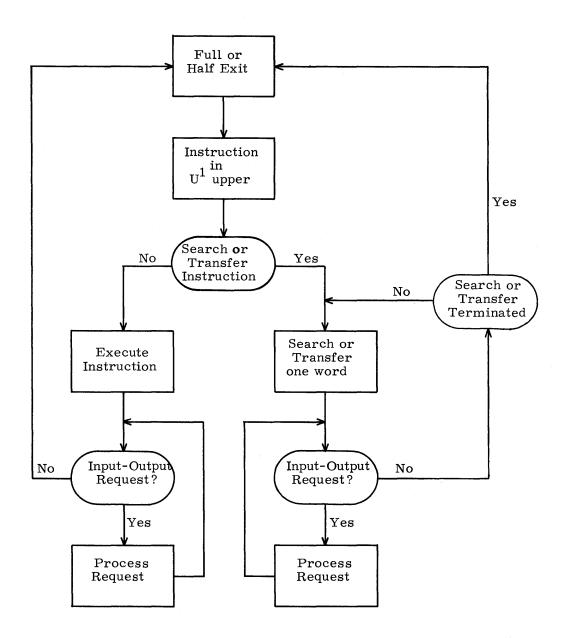


Figure 3-1. Recognition of I/O Requests

3-6

Interrupt

In each piece of external equipment as well as in parts of the internal computer control, certain conditions may arise which make it necessary that the main program be notified of their presence. The signal which notifies the computer of these conditions is called an interrupt and is program controlled. If an interrupt is desired when a particular condition arises, an external function select code (74.0) must select an interrupt on that condition. Unless such selection is made, no interrupt is produced when the condition arises. (See appendix 6 for the codes.)

When an interrupt occurs, the main program is halted and a previously programmed routine of instructions (interrupt routine) is performed which must determine the cause of the interruption and take appropriate action. After completing these operations, the interrupt routine must return to the main program. The main program resumes at the exact point from which the entrance to the interrupt routine was made.

Interrupt Routine

The interrupt is processed by performing a return jump to address 00007. This is a special address allocated for use as the entrance point to the interrupt routine and for the return from this routine to the main program.

Typically, address 00007 (interrupt control word) contains two unconditional jump instructions. For example:

The upper instruction provides for the return to the main program upon completion of the interrupt routine. To accomplish this the upper address portion (XXXXX) is loaded with the contents of the P register when the interrupt routine is entered. The lower instruction jumps to the interrupt routine which begins with an instruction whose address is indicated in the lower address part of 00007 (YYYYY).

In general, the interrupt routine (table 3-1) checks for all possible interrupt conditions by means of sense (74. 7) instructions. After determining which selected condition caused the interrupt a jump is made to that portion of the routine which processes the interrupt.

After having been interrupted the computer cannot again be interrupted without returning to the main program via location 00007.

00007	75 0	75 0 int00	Exit/Entrance
	Address of r	next instruction in	main program
int00	74 7 00131	75 0 ovf00	Sense Overflow
int01	74 7 11101	75 0 crr00	Sense Carriage Return
int02	74 7	75 0	
ovf00	-	\	
ovf01			
		[> Process Overflow
		74 0 00070	Clear Arithmetic Faults
ovf	75 0 00007		Exit to Main Program
		-	
crr00]	
crr01			
		I	> Process Carriage Return
	$74 \ 0 \ 00200$		Clear Carriage Return
crr	75 0 00007		Exit to Main Program

TABLE 3-1. TYPICAL INTERRUPT ROUTINE

When an interrupt occurs, unless the indication of the condition or the interrupt selection is removed, the program will again be immediately interrupted upon return to the main program.

In the process overflow fault above, all arithmetic faults are cleared. In the process carriage return portion of this interrupt routine the interrupt signal is removed by a 74 0 00200 (clear carriage return character). The interrupt selection may be removed by a 74 0 11100 (no interrupt on carriage return).

Real Time Clock

Address 00000 in core storage may be selected to provide a continuously operating record of elapsed time. The 48-bit quantity stored there is advanced by one every 1/60 of a second (accuracy is maintained by the 60-cycle power source). The content of address 00000, which may be sampled at any time by the program, gives elapsed time from the start of the real-time clock operation. The clock may be started by 74 0 01000 and is stopped by 74 0 02000. Starting the clock does not pre-set address 00000 in any way, but begins the periodic incrementing of its previous contents.

By selecting interrupt on arithmetic fault, and presetting the contents of address 00000, the real-time clock may be used to provide an interrupt of the main computer program. When interrupt occurs, check location 00000 for overflow.

CONSOLE INPUT-OUTPUT EQUIPMENT

Three input-output devices mounted on the console are standard equipment with the 1604 computer. A Teletype high speed punch and a high speed tape reader provide for the processing of perforated paper tape. An IBM typewriter, modified by Soroban Engineering, Inc., provides for direct keyboard entry of data and for printed copy output. The console input-output units communicate with the central computer via buffer channel 1 (input) and 2 (output). Other input-output units may share these channels but console input-output units use only these channels.

Data may be transmitted between the console equipments and the computer in either the character or the assembly mode. In the character mode a 7-bit character is buffered one character at a time. The 7-bit character occupies the lowest bit positions of a 48-bit word; the upper 41 bits are "0's".

In the assembly mode the 48-bit word, consisting of eight 6-bit characters, is buffered. During an input buffer in the assembly mode eight successive characters are assembled into a 48-bit word and sent to the computer. The first character occupies the upper 6 bits of the word; the last character occupies the lower order 6 bits. For an output buffer in the assembly mode a 48-bit word from the computer is disassembled into eight characters, the upper 6 bits first.

TYPEWRITER

The typewriter may be used as a keyboard input device or as an output device for producing printed copy; during output it types approximately 10 characters per second.

All of the typewriter characters and functions are represented by unique combinations of 6 bits. (Codes are in appendix 6.) During a keyboard input operation, striking a character key causes the coder to produce the code which is sent to the computer. Space is the only coded typewriter control function which is sent to the computer. For typewriter output, a 6-bit character code sent to the decoder causes the typewriter to print the selected character or perform the designated control function.

If the keyboard is selected by code 1114X, the interrupt signal occurs for each carriage return (CR).

If an illegal code (unlisted) is sent to the typewriter from the computer, operation hangs up. Striking the CR, backspace or shift keys will allow operation to be resumed.

A zero code (all "0" bits) which constitutes a do nothing code is used to fill out a 48-bit word in the assembly mode.

PAPER TAPE READER

The paper tape reader enters information stored on punched paper tape into the computer. The reader, which is always connected to channel 1, operates at a maximum rate of 350 characters (frames) per second; the time interval between successive characters from the reader is 3.3 ms.

Manual controls for the reader are on the punch and reader control panel of the console. When the Reader Mode switch is set to Assembly, the tape is positioned at the first frame of the first word (load point); when it is set to Character, the tape moves ahead one frame. Information is stored on paper tape in seven levels. A frame, which is across the width of the tape, can store 7 bits (figure 3-2). The sprocket or feed holes between levels 3 and 4 generate signals to time and control the reading of the tape.

In the assembly mode, level 7 is used as a control rather than an information level. The first of the eight characters in a word is indicated by a hole in the control level.

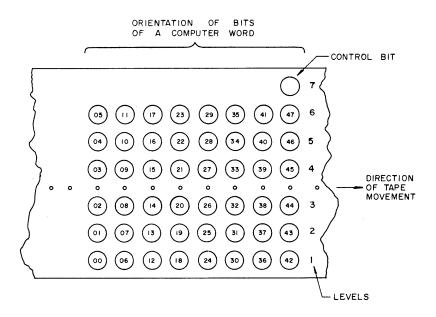


Figure 3-2. Seven Level Punched Paper Tape

Reader tape motion stops on any one of three conditions:

- 1) When buffer operation terminates (assembly or character mode).
- 2) When the load point in assembly mode is reached.
- 3) Absence of a 7th level every 8th character in the assembly mode.

The reader End of Tape indicator is set on any of three conditions:

- 1) On a computer Master Clear.
- 2) Absence of a 7th level every 8th character in the assembly mode.
- 3) By a 74 0 11210 instruction. This instruction is used to indicate the end of information in the character mode.

After reading all information on the tape in the assembly mode, tape motion stops and the End of Tape indicator is set because the 7th level control bit is missing. In the character mode, however, motion stops when the buffer operation is satisfied but the End of Tape indicator remains cleared. A 74 0 11210 instruction may be programmed to set the End of Tape indicator after the buffer terminates. The state of the End of Tape indicator, regardless of the mode of operation, may be used to determine if all information on the paper tape has been read.

PAPER TAPE PUNCH

The punch which prepares paper tape output is always connected to buffer channel 2. Nominal operating rate is 60 characters per second. In character mode, the lower 7 bits of each word sent are punched; the upper bits are ignored. In assembly mode, eight 6-bit characters are punched per word. The upper 6 bits are punched first, with the 7th level supplied.

On the punch, the feedout lever provides for punching out leader. A micro-switch is mounted near the roll of paper tape that supplies the punch. When the supply is low, the switch opens and provides an out of tape indication which may be sensed.

INTERNAL EXF SELECT INSTRUCTIONS

74 0	000C0	Interrupt on Channel C Inactive Selects interrupt when channel C becomes inactive. C = 1 - 6 An interrupt signal is generated whenever the channel becomes inactive. More than one interrupt can be selected. The interrupt remains selected until cleared.
	000C1	Remove Selection Above Interrupt on channel C inactive selection removed
	00100	Interrupt on Arithmetic Faults Selects interrupt on occurrence of any arithmetic fault; remains selected until cleared
	00101	Remove Selection Above Interrupt on arithmetic faults selection removed
	00070	Clear All Arithmetic Faults Removes all arithmetic fault indications and turns off arithmetic fault background lights on console
	01000	Start Real-Time Clock Begins process of incrementing previous contents of address 00000 by one each 16.6 ms; address 00000 is not cleared by starting clock
	02000	Stop Real-Time Clock Halts process of incrementing address 00000. The contents of 00000 remain unchanged.
	C0000	Clear All Channel C Selections Clears all previous selections made on the designated channel C except interrupt on channel C inactive
	00200	Clear the Carriage-Return-Typed Indicator

INTERNAL EXF SENSE INSTRUCTIONS

74 7	000C0	Exit on Channel C Active
		Full exit if channel C is active; if not, half exit
	000C1	Exit on Channel C Inactive Full exit if channel C is inactive; if active, half exit
	00110	Exit on Divide Fault; half exit if no divide fault
	00111	Exit on No Divide Fault; half exit if divide fault
	00120	Exit on Shift Fault; half exit if no shift fault
	00121	Exit on No Shift Fault; half exit if shift fault
	00130	Exit on Overflow Fault; half exit if no overflow fault
	00131	Exit on No Overflow Fault; half exit if overflow fault
	00140	Exit on Exponent Fault; half exit if no exponent fault
	00141	Exit on No Exponent Fault; half exit if exponent fault
		CONSOLE EXF SELECT CODES

(Always Channel 1 and 2, Equipment #1)

INPUT TYPEWRITER

74 0 11100 Select the Typewriter for Input and No Interrupt on Carriage Return Selects keyboard (character mode only) Interrupt selection cleared, Carriage Return indicator cleared

11140 Select the Typewriter for Input and Interrupt on Carriage Return Selects keyboard (character mode only) Interrupt selection set, Carriage Return indicator cleared. The next carriage return, which is not output, will set the Carriage Return FF and cause an interrupt. The interrupt selection can be cleared by the external master clear or the 74 0 11100 select only.

PAPER TAPE READER

74 0 11210	Set End of Tape Indicator
	Sets the End of Tape indicator $\overset{*}{\sim}$
	Clears interrupt on end of tape
11200	Select the Paper Tape Reader and No interrupt on End of Tape Selects the reader
	Interrupt on end of tape cleared
11220	Select the Paper Tape Reader and Interrupt on End of Tape Selects the reader
	Interrupt on end of tape set. If the End of Tape indicator is set,
	the interrupt will be immediate.
OUTPUT TYPEWRITER	
74 0 21100	Select the Typewriter for Output in the Assembly Mode Selects keyboard to print **
21110	Select the Typewriter for Output in the Character Mode

Selects keyboard to print **

^{*}This select is usually used in character mode operation only. The End of Tape indicates the logical end of tape, and can be cleared externally only by moving the switch (on the reader control) to the character or assembly position. Master Clear selects the paper tape reader and sets the End of Tape indicator. When the End of Tape indicator has been set the reader is "not ready".

^{**}Will not change the Carriage Return FF nor the interrupt selection on channel 1. The code "00" will be ignored, all other illegal codes will cause the typewriter to hang-up. It is released by performing a function, usually spacing.

PAPER TAPE PUNCH

74 0 21200	Select the Paper Tape Punch, Assembly Mode
	Selects the punch, sets mode to assembly
	Turns the punch motor on
21210	Select the Paper Tape Punch, Character Mode
	Selects the punch, sets mode to character

Turns the punch motor on

21240 Turn the Punch Motor Off

CONSOLE EXF SENSE CODES

TYPEWRITER

(Sensed on Input Channel Only)

74 7	7 11100	Full Exit if Carriage Return Performed on Input
		If a carriage return (which was not the result of an output) has
		been performed since the last input select, a full exit is executed;
		if not, a half exit.
	11101	Full Exit if No Carriage Return Typed on Input
		If the Carriage Return indicator is not set, a full exit is executed;
		if set, a half exit.
	11140	Full Exit Lower Case
		If the typewriter keyboard is in the lower case a full exit is performed.
	11141	Full Exit Upper Case If the typewriter keyboard is in the upper case a full exit is performed.

PAPER TAPE READER

74 7	11200	Full Exit on End of Tape Indicator Set
		If the End of Tape indicator is set a full exit is performed; if not,
		a half exit.
	11201	Full Exit on No End of Tape Indicator Set
		If the End of Tape indicator is not set a full exit is performed; if
		set, a half exit.
	11210	Full Exit on Assembly Mode
		If the paper tape reader is in the assembly mode a full exit is
		performed; if not, a half exit.
	11211	Full Exit on Character Mode
		If the paper tape reader is in the character mode a full exit is
		performed; if not, a half exit.

PAPER TAPE PUNCH

74 7 21200 Full Exit on Out of Tape If the paper tape punch is out of tape, a full exit is performed; if not, a half exit.

21201 Full Exit on Not Out of Tape If the paper tape punch is not out of tape, a full exit is performed; if out of tape, a half exit.

PROGRAMMED EXAMPLES FOR CONSOLE

Example 1: Type 50_{10} characters which are stored in FILE (one character per word in the lower 6 bits).

LOCN	OPN	B	OPERAND OR M-TERM	REMARKS
FILE	BSS		50	
START	ENA	0	FILE + 50	Terminating Address
-	\mathbf{EXF}	7	00021B	Wait for Channel 2 to be Inactive
	STA	0	2	Control Word for Channel 2
	\mathbf{EXF}	0	21110B	Select Typewriter Character Mode
	\mathbf{EXF}	2	FILE	Activate Channel 2 at First Word Address
	The pro	ogram	would continue f	rom this point while the output goes on.

Example 2: Call for 10_{10} characters to be typed as input to the computer. (Typewriter input is in the character mode only, therefore 10_{10} words must be read in.) If an error is made before the tenth character is typed, press the carriage return key and call for ten new characters. Continue the main program until all ten characters are typed without error.

TYPE	BSS		10	
CONTROL	ENA	0	TYPE $+ 10$	Ten Words, the First at Type
-	EXF	7	00011B	Wait for Channel 1 to be Inactive
	\mathbf{EXF}	0	11140B	Select Typewriter for Input and Interrupt on CR
	SAL	0	1	Terminating Address to Control Word on CR
	\mathbf{EXF}	1	TYPE	Activate Channel 1, the First Character to Type
	\mathbf{EXF}	0	00010	Select Interrupt on Channel 1 Inactive
	The pro typed or jump to	r a cai	rriage return pe	from this point. When 10 characters had been rformed, an interrupt would be executed (return
00007	SLJ	0	XXXXX	Address to Return in Main Program Supplied
	NOP			
00010	EXF	7	11100B	Full Exit if Carriage Return
	SLJ		13B	Must Have Been Channel 1 Inactive
00011	\mathbf{EXF}	0	00200B	Clear Carriage Return Indicator
	EXF	1	TYPE	Call for 10 New Characters
00012	SLJ	0	7	Return to Main Program via 00007
00013	XXX	Х	The	e program to interpret the input would be here. e return to the main program must eventually via location 00007.

Example 3: Punch out on paper tape the contents of location DUMP up to but not including DUMP + 1000_8 . Punch all of each word.

LOCN	OPN	<u>B</u>	OPERAND OR M-TERM	REMARKS
DUMP	BSS		1000B	
OUT	NOP			
-	\mathbf{EXF}	7	21B	Wait for Channel 2 to be Inactive
	\mathbf{EXF}	0	21200B	Select Paper Tape Punch, Assembly Mode
	\mathbf{ENI}	1	DUMP + 1000B	Terminating Address
	SIL	1	2	Store in Location 00002
	\mathbf{EXF}	2	DUMP	Activate Channel 2 at FWA
	The pro	gram	would continue fr	com this point while the output goes on.

Example 4: Read a paper tape and type the characters until a carriage return code is read (45 $_8$). Read them into location CHAR and following locations.

CHAR	BSS	(Max	imum for tape u	sed)
-	ENA	0	CHAR	Inititialize the Activate Instructions
	SAU	0	ACT 1	
	SAU	0	ACT 2	
	SAU	0	ACT $2 + 1$	
-	EXF	7	21B	Wait for Channel 2 to be Inactive
	\mathbf{EXF}	0	21110B	Select the Typewriter for Output
-	EXF	7	11B	Wait for Channel 1 to be Inactive
	\mathbf{EXF}	0	11200B	Select the Paper Tape Reader
	ENA		45B	Enter the Code for Carriage Return
	\mathbf{ENI}	6	CHAR + 1	Set Up First Terminating Address
	NOP			
NEXT	SIL	6	1	Store in Control Word 00001
	SIL	6	2	Store in Control Word 00002
ACT 1	EXF	1	CHAR	Call for One Character
	EXF	7	11B	Wait
ACT 2	\mathbf{EXF}	2	CHAR	Type the Character
	NOP			
	EQS	0	CHAR	Was it a Carriage Return?
	SLJ		CONT	No (next page)
	SLJ		DECODE	Yes

LOCN	OPN	<u>B</u>	OPERAND OR M-TERM	REMARKS
CONT	SIU	6	ACT 1	New Input Address
	SIU	6	ACT 2	New Output Address
	SIU	6	ACT 2 + 1	
	INI	6	1	Increase Address
	SLJ	0	NEXT	Continue Reading
DECODE	At this	point t	he line of input o	could be decoded.

CODE At this point the line of input could be decoded. The carriage return code is in the location specified by (B^b) - 1.



Operation

DESCRIPTION OF INDICATORS AND CONTROL SWITCHES

All main computer controls and indicators are on the console. Functional significance of console background lights is listed in table 4-1; computer controls are described in table 4-2.

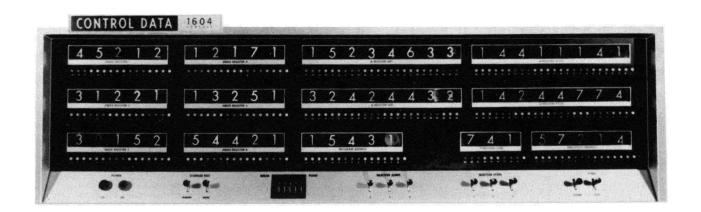


Figure 4-1. Center Panel of Console

The indicators are lamp modules, each of which displays a single octal digit. The lamps, in response to signals from the computer, display the contents of the operational registers in octal form only when the computer is stopped; the display is blank when the computer is running. Each indicator has three push buttons which are numbered in the powers of two, from right to left, starting with zero. Pressing a push button forces that particular stage of the register to the SET state. Each group of three buttons represents an octal digit. Different shades of blue are used in adjacent octal groups; within an octal group the three buttons are of the same shade.

At the right end of each register is a CLEAR push button (white). This button will clear the individual FFs within that register. SET and CLEAR push buttons should be used only when the computer is stopped; otherwise errors may result. Conditions which stop the computer are listed below. When these conditions exist register contents may be altered by setting or clearing.

- 1) Illegal function codes 00 and 77
- 2) Selective Stops (instructions 76)
- 3) Breakpoint Stop
- 4) Pressing START-STEP switch
- 5) Pressing CLEAR switch (internal master clear)

At some of the modules there are colored background lights which indicate certain internal conditions (Figure 4-2, Table 4-1). A light is identified by the register in which it is located and its position in the register. For example, AL-4 is fourth from the left in A register left. In general, red lights signify faults and blue lights signify special operating conditions. The background lights may be illuminated when the computer is running as well as when it is stopped.

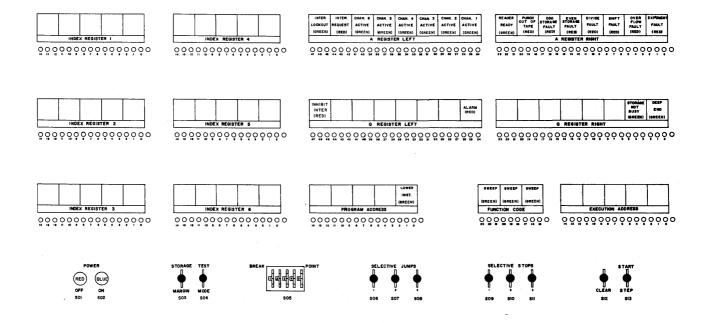


Figure 4-2. Console Display

Rev. E

TABLE 4-1. CONDITIONS INDICATED BY CONSOLE BACKGROUND LIGHTS

Light	Condition		
AL-1 (blue)	Interrupt Lockout - Computer is in interrupt routine.		
AL-2 (red)	Interrupt Request - Interrupt request signal is being received from interrupt circuit.		
AL-3 (blue)	Channel 6 Active - Channel 6 is in use for output buffer.		
AL-4 (blue)	Channel 5 Active - Channel 5 is in use for input buffer.		
AL-5 (blue)	Channel 4 Active - Channel 4 is in use for output buffer.		
AL-6 (blue)	Channel 3 Active - Channel 3 is in use for input buffer.		
AL-7 (blue)	Channel 2 Active - Channel 2 is in use for output buffer.		
AL-8 (blue)	Channel 1 Active - Channel 1 is in use for input buffer.		
AR-1 (blue)	Reader Ready - (1) Paper tape is at load point, ready for an input buffer; or (2) input buffer paper tape is in progress.		
AR-2 (red)	Punch Out of Tape - Punch tape reel is nearly empty.		
AR-3 (red)	Odd Storage Fault - Fault in sequence chain of odd storage unit; storage unit is inoperative until master cleared.		
AR-4 (red)	Even Storage Fault - Fault in sequence chain of even storage unit; storage unit is inoperative until master cleared.		
AR-5 (red)	Divide Fault - Improper divide instruction executed.		
AR-6 (red)	Shift Fault - Shift count greater than 127 (decimal).		
AR-7 (red)	Overflow Fault - Required sum or difference exceeds capacity of A register.		
AR-8 (red)	Exponent Fault - In a floating-point instruction, exponent of result is 2^{10} or greater.		
QL-8 (red)	Alarm - Indicates abnormal condition.		
QR-7 (green)	Storage Not Busy - Indicates storage is not in use.		
QR-8 (blue)	Deep End - Computer fails to complete operation in step mode.		
PA-5 (blue)	Lower Instruction - Lower instruction is indicated.		
FUNCTION CODE (blue) (3 lights)	Sweep - Computer is in sweep mode (Mode switch is down).		

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TABLE 4-2. MAIN COMPUTER CONTROLS

Control		Function
POWER	ON - green	Applies d-c power to computer by energizing contactor in primary power lines of motor-generator.
push button	OFF - red	Removes d-c and a-c power from computer by de- energizing contactor in primary power lines of motor- generator.
STORAGE TEST	MARGIN	Varies the bias applied to storage sense amplifiers. Used for maintenance purposes only; should be in neutral position at all other times.
Lever switch locks in up, down and	MODE	UP: an instruction is executed repeatedly in either the Step or Start mode.
neutral posi- tions.		DOWN: contents of consecutive storage locations may be manually examined by depressing Step. Consecutive half-words are displayed in function code and execution address registers but are not executed.
BREAKPOINT Five 8-position switches can be set to octal address 00000 through 77777.		Provides for selection of any storage address as a breakpoint address. Computer stops when program address and breakpoint address are equal, just prior to performing the upper instruction at the breakpoint address.
SELECTIVE JUMPS 1, 2, 3 Three lever switches lock in upper positions, momentary in down positions.		Provide manual conditions for instruction 75, normal jumps, b = 1, 2 or 3, return jumps, b = 5, 6 or 7 (Same function in all positions)
SELECTIVE STOPS 1, 2, 3 Three lever switches lock in upper position, momentary in down positions.		Provide manual conditions for stopping the computer on instruction 76, b = 1, 2, 3, 5, 6 or 7 (Same function in all positions)
CLEAR Lever switch, momentary in up and down positions.		DOWN master clears the computer, clears all oper- ational registers and most control FFs. UP master clears external equipment, causing most of the registers and control FFs of the external equip- ment to be cleared and the paper tape reader to be selected.

TABLE 4-2. (CONT'D.)

Control	Function
START-STEP Lever switch, momentary in up and down positions.	 START (up) selects high-speed mode in which a program of instructions and auxiliary operations proceeds until completed or stopped. STEP (down) selects Step mode. Each time switch is pressed a single instruction is executed and computer stops (all buffer requests are completed before operation stops). Step selection overrides any previous selection of Start.
VOLUME CONTROL Black knob under console desk	Controls volume of signal from console loudspeaker.
*SET Push Buttons Numbered in the powers of 2, beginning with zero. Each group of 3 is an octal digit.	Allow for manual entry of a quantity into a given register. Forces that particular stage of the register to the Set state.
*CLEAR Push Button	Clears the individual FFs within that register.

* Should be used only when the computer is stopped

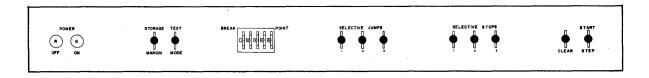


Figure 4-3. Manual Controls

READER AND PUNCH CONTROLS

Switch	Function
PUNCH MOTOR	Turns punch motor on or off. (Motor may also be turned on under program control.)
SELECT-TAPE FEED	Select enables use of the punch.
	Tape Feed causes leader to be punched.
READER MOTOR	Turns reader motor on or off. (Motor cannot be turned on by any other means.)
CHARACTER- ASSEMBLY	In Character mode each character is sent to computer separately.
	In Assembly mode eight consecutive characters are assembled into a word to be sent to computer.

TABLE 4-3. READER AND PUNCH CONTROLS

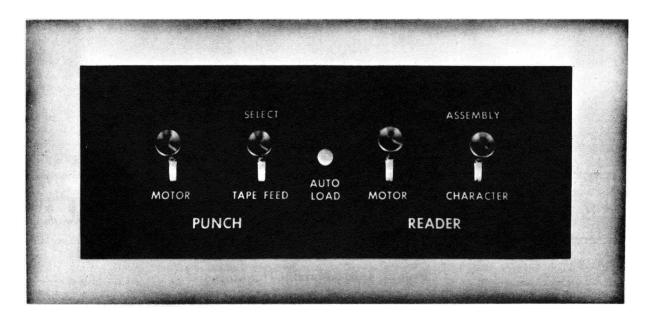


Figure 4-4. Reader and Punch Controls: Auto Load Control

AUTO LOAD CONTROL

The Auto Load button initiates a bootstrap routine to read into memory (via channel 3) the first record from magnetic tape #1, on 1615 or 1607 equipment #2.

Pressing the Auto Load button selects the tape and loads the bootstrap routine into memory locations 00000 and 00001, and puts an address of 32000 (arbitrary and > 00004) in the lower address of 00003.

The program appears as:

(00000)	74 0 32005	Rewind the tape
	74 7 32000	Wait for ready
(00001)	74 3 00002	Activate, FWA = 00002
	74 7 32000	Wait for ready
(00002)	XX X XXXXX	Will be the first
	XX X XXXXX	word read from tape
(00003)	74 3 00002	
	74 7 32000	

If Breakpoint is not set to 00000 or 00001 the routine will be executed. The first word read from tape will be read into location 00002 and be executed as soon as the tape is ready again.

Location 00003 will become XXX00004XXXYYYYY from the second word on tape, inserting a new terminating address.

OPERATION

The 1604 is a stored-program computer. To load a program in the computer a load program (basic service library) is needed. The load program is entered manually. A paper tape reader, a paper tape punch, an electric typewriter, and a set of magnetic tapes are some of the important external devices used for communicating with the 1604. The programmer, before operating any of these devices, should make himself familiar with instructions for these devices and they should be followed in the order recommended.

LOAD PROGRAM ENTERING

A load program to be entered in storage is usually on bi-octal paper tape. The following procedure enters the load program:

- 1) Turn on power.
- 2) Master clear, both internal and external.
- 3) Press Start/Step switch once.
- 4) Clear function code and set to 200.
- 5) Clear execution address and set to 00001.
- 6) Set terminal address of buffer in lowest five octal digits of A register right.
- 7) Press Start/Step switch once.
- 8) Load tape into reader.
- 9) Turn on reader motor (wait 10 seconds).
- 10) Raise reader Mode switch to ASSEMBLY position.
- 11) Clear function code and set to 741.
- 12) Clear execution address and set to initial address of buffer.
- 13) Press Start/Step switch once. Wait until tape loads (console lights come on).
- 14) Press Clear switch.
- 15) Perform steps 2 through 8 of operation with pre-stored program.

STARTING OPERATION WITH PRE-STORED LOAD PROGRAM

When a general loading program which provides for loading other programs is held in storage, the starting procedure is as follows:

- 1) Turn on power (Power On, figure 4-3).
- 2) Make required manual selections:

Selective Jumps Selective Stops Breakpoint

- 3) Set in operation the external device or devices selected to communicate with the computer. (Follow the instructions for the devices given in this chapter.)
- 4) Master clear, both internal and external (press Clear, then raise it).
- 5) Set Program Address register to address of first instruction of program.
- 6) Begin computer operation (raise Start switch).
- 7) To shut down the equipment after the operation has stopped, follow the instructions as given for each external device.
- 8) Press Power Off button, which disconnects power from all equipments.

READER

The reader is a CONTROL DATA 350 Paper Tape Reader (figure 4-5). It can read either a 5, a 7, or an 8-level tape. For a bi-octal tape with the 7th level control holes, assembly mode is selected; for a flex or other code, character mode is selected.

- 1) Check if tape basket is at the proper place. Do not allow the tape to fall on the floor.
- 2) Turn tape release lever clockwise to raise tape guide plate.
- 3) Select the desired tape level by means of the tape level switch.

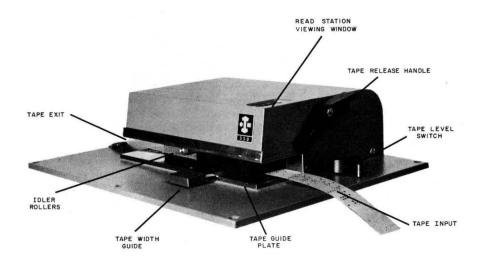


Figure 4-5. Paper Tape Reader

4-9

- 4) Holding the tape guide down, slide it so that the marker rests above the proper etched mark on the tape deck surface. The outer position is for 8-level tape, the center for 7-level, and the inner for 5-level.
- 5) Insert tape as shown in figure 4-5. Make sure that the tape is properly aligned.
- 6) Turn Tape Release lever counterclockwise to lower the tape guide.
- 7) Select the desired mode of operation by the Mode switch (figure 4-4) on the control panel.
- 8) Turn on Reader switch on control panel (figure 4-4).
- 9) After the reader has read the tape, remove paper tape from reader and basket; rewind tapes.
- 10) Turn off reader motor.

PUNCH

The paper tape punch (figure 4-6) is mounted on a hinged rack at the rear of the right wing of the console. Punch tape feeds out of a slot in the compartment door; the chad box is just inside the door.

- 1) To ensure proper performance of the punch, always keep the chad box clean.
- Set Punch switch to SELECT (control panel) and check for sufficient paper in reel.

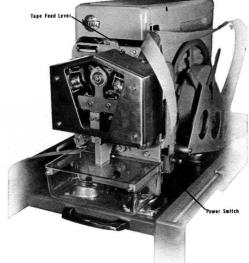


Figure 4-6. Paper Tape Punch

- 3) If the punch has been used, generate a foot of leader by pressing tape feed; remove feed; remove tape and wind it up.
- 4) Perform the following steps to replace a tape roll at punch.
 - a) Remove the tape reel from cradle at side of punch.
 - b) Unscrew tape hold-down assembly, remove old roll, and place new roll on reel. Replace hold-down assembly and mount reel in cradle.
 - c) Thread tape as shown in figure 4-6. Bring tape around lower roller and into guides leading to punch block.
 - d) Turn on punch motor and advance tape through the punch block by pressing the tape feed-out lever (top of punch block).
 - e) Bring leader out through slot in door. Swing punch back into compartment.

TYPEWRITER

The typewriter has all of the characters and functions of a standard electric machine. As a keyboard entry device the typewriter is used only in the character mode. After the program selects keyboard and initiates an input buffer, each striking of a key causes a 6-bit coded character to be entered into the lower six positions of a computer word. The remaining bits of the word are all "0". If the keyboard is selected along with an interrupt feature, each carriage return or tab sends an interrupt signal to the computer. This notifies the program of the entry of data from the keyboard.

When the typewriter is used as an output device certain conditions cause it to hang up until the space bar is struck: receipt of an illegal typewriter code, a code to shift up when the carriage is already up, or a code to shift down when the carriage is already down.

If the typewriter is to be used:

- a) Place paper in it.
- b) Set the switch beneath the righthand corner to ON.

TAPE TRANSPORTS

The tape transports which can be used with 1604 are CONTROL DATA 606 and CONTROL DATA 1607. To use the 606, the CONTROL DATA 1615 Adapter is needed. The codes for the adapter and the tape unit are given in appendix VI.

606 TAPE UNIT

Controls and Indicators

The manual controls and indicators for operating each tape unit are mounted on a panel located below the front door of the unit (figure 4-7). The functions of the controls are described in table 4-4.

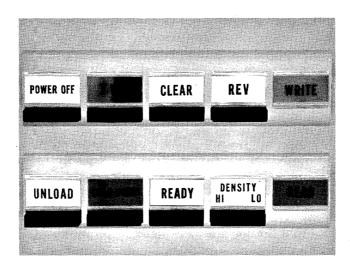


Figure 4-7. Operator Control Panel

TABLE 4-4.	606	CONTROLS AND	INDICATORS
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NAME		FUNCTION
POWER OFF	*S	Removes power from all components and power supplies.
	**I	Power is available to components and power supplies.
FWD	S	Moves tape forward at 150 ips. Motion stops when end of tape marker is sensed.
	I	Tape is moving forward at 150 ips.
CLEAR	S	Master clears all previous settings and conditions. Stops tape motion immediately. New Manual selections are necessary to reselect tape unit and/or operation required.
	<u> </u>	606 is cleared.

*Switch

**Indicator

TABLE 4-4. 606 CONTROLS AND INDICATORS (CONT'D)

NAME		FUNCTION
REV	*S	Rewinds tape at 225 ips. Motion stops when load point marker is sensed.
	**I	Tape is moving in reverse direction at 150 or 225 ips.
WRITE	I.	Write operation is in progress.
UNLOAD	S	Moves tape at 225 ips to unload position (all tape on supply reel). Tape load procedure must be performed to resume operation.
	I	Tape is in unload status.
LOAD POINT	S	Moves tape forward at 150 ips to load point marker. Motion stops when marker is sensed.
	I	Tape is at load point marker.
READY	S	Places 606 under external control.
	I	Unit is under external control.
DENSITY	S	Changes density mode selection.
	I (Hi) I (Low)	High density mode selected. Low density mode selected.
READ	I	Read operation is in progress (not on when reading for horizontal checking during write operation).
UNIT SELECTION	S	10-position switch; 0-7 provide input desig- nation while two standby positions disconnect unit from external control.
	I (White) I (Red)	Show selected number. Fault Condition (power failure, tape not in columns, etc.).
OVERHEAD LIGHTS	I	File protection ring is on reel (unit can write) and tape unit is not in the unload position.

*Switch **Indicator ¢

Tape Load Procedure

- 1) Make sure that tape unit is properly energized.
- 2) Slide front glass door down to lowest position (figure 4-8).
- 3) Check that supply reel has been file protected as necessary.
- 4) Mount reel on supply reel hub and tighten hub knob. For proper alignment, push reel firmly against hub stop before tightening knob.
- 5) Make sure that tape load arms are in up position.
- 6) Pull sufficient tape from supply reel to reach take-up reel. Thread tape on the outside of the supply tape load arm, over the head assembly, around the outside of the take-up load arm and over the top of the take-up reel hub two or three times.
- 7) Slide tape under head assembly.
- 8) Snap tape load arms down.



Figure 4-8. 606 Tape Load and Unload Mechanics

- 9) Set Unit Selection switch to one of ten positions (0-7 or standby) to assign a logical program selection number.
- 10) Press Clear switch.
- 11) Press Load Point switch. Tape will drop in columns, move forward, and stop on load point marker. The Load Point light will turn on. (If the light does not turn on, notify maintenance.) If tape continues moving forward for more than 3 or 4 seconds, it indicates either no load point marker was placed on the tape or the operator manually wound the marker onto the take-up reel during step 6.
- 12) If the unit is to be controlled, press the Ready switch. If it is to be manually operated and the Ready switch has been pushed, press the Clear switch.
- 13) Raise the front glass door completely.

If the supply reel contains a file protection ring, the overhead lights should be on, indicating that a write operation may be performed. If the lights are not on, notify maintenance.

Tape Unload Procedure

- 1) Press Clear switch.
- 2) Press Unload switch. All tape will automatically be drawn from the take-up reel and wound on the supply reel. The Unload indicator will light.
- 3) Slide down front door.
- 4) Loosen supply reel hub knob and remove supply reel.
- 5) Check if reel needs to be file protected and if it is labeled adequately prior to storage.

Special Instructions

In order to simulate an unload condition without removing all tape from the take-up reel, simultaneously press the Clear and Unload switches. The unload condition will be simulated but tape will not move. In order to place the unit in operational status, remove all tape from the vacuum columns by revolving the take-up reel clockwise and the supply reel counterclockwise. Snap the tape load arms down and press the Load Point switch. The tape will move forward and stop on the nearest load point marker. The Load Point indicator will turn on. If all tape is unwound from the supply reel:

- 1) Snap tape load arms up, if necessary.
- 2) Guide tape around the tape load arms, over the head assembly, and wrap approximately ten turns around the supply reel.
- 3) Slide tape under head assembly.
- 4) Press the Load Point switch.
- 5) As soon as the Forward light turns on, press the Clear switch and then the Reverse switch. Tape will rewind on the nearest load point marker.

The following information is applicable when a number of load point or end of tape markers are used on a single tape.

To move forward from a reflective marker and stop at nearest end of tape marker, press the Forward switch.

To move forward off a reflective marker and stop at nearest load point or end of tape marker, press the Forward and then the Load Point switches. Load Point indicator will light if motion stops at load point marker.

To reverse from a reflection marker and stop at nearest load point marker, press the Unload, Clear, and Reverse switches, in that order.

Tape motion may be stopped at any time by pressing the Clear switch. An unload operation may be performed by pressing the Unload switch.

1607 Tape Unit

Controls and Indicators

Each tape unit is provided with push buttons for manual operation. These controls are mounted on a panel above the front door (figure 4-9, table 4-5).

Tape Load Procedure

- 1) Open door to handler.
- 2) Check that file reel to be loaded has been file protected as necessary.
- 3) Mount the reel on the file reel hub and tighten the hub knob. To insure proper reel alignment push the reel firmly against the reel hub stop before tightening the knob. If the file protection ring has been removed from the reel, check that the Write Lockout lamp turns on when the reel is loaded. If the lamp does not turn on call maintenance.

TABLE 4-5. 1607 CONTROLS AND INDICATORS

CONTROL		FUNCTION
REWIND	*S	Controls manual rewind to load point.
	**I	Indicates rewind in progress.
CHANGE TAPE	S	Drops any manual selection and places tape unit in automatic or program control mode.
	I	When lighted, indicates tape rewound under program control and interlocked at load point. The interlock prevents operation of the tape unit until the Stop Manual switch is operated.
WRITE LOCKOUT	S	Drops power from unit and removes program designation.
	I .	When lighted, indicates that tape unit is loaded with a reel which does not contain a file protection ring. The tape cannot be written as long as the light is on, but may be read.
1, 2, 3 or 4	S	Designates program selection of unit and applies power to unit. Each new unit designation cancels an existing designation.
	Ι	Indicates unit selection and power-on condition.
REVERSE	S	Initiates reverse tape motion during manual operation.
	Ι	Indicates reverse tape motion.
STOP MANUAL	S	Drops unit from program control or drops forward or reverse selection and places unit in manual mode.
	Ι	Indicates manual mode and ready.
FORWARD	S	Initiates forward tape motion during manual mode.
	I	Indicates forward tape motion.

*Switch **Indicator

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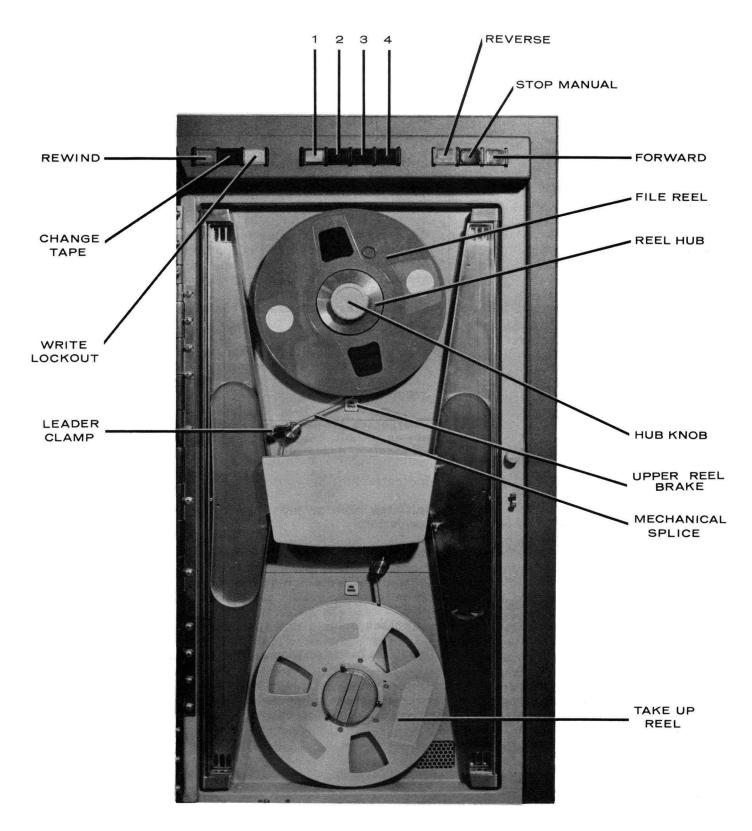


Figure 4-9. 1607 Tape Unit

- 4) Press upper Reel Brake pushbutton to release mechanical brake and check that pulling tape from reel causes it to rotate clockwise. Pull sufficient tape from reel to reach end of permanent machine leader held by leader clamp.
- 5) Connect file tab to permanent machine leader.
- 6) Take up slack by turning file reel while pressing upper Reel Brake pushbutton
- 7) Lift leader clamp and close door.
- 8) Press one of the unit selection switches (1, 2, 3, 4) to apply power to the unit and assign the unit a logical program selection number. Wait two minutes. The Stop Manual lamp should turn on; if not, call maintenance.
- 9) Press Stop Manual.
- 10) Press Rewind button. Unit is ready when Rewind lamp turns off. If Stop Manual lamp remains on, unit is not ready; call maintenance.

Tape Unload Procedure

- 1) Press Stop Manual button to select manual mode.
- 2) Press Reverse button to move tape backwards to change tape position.
- 3) Open front door of tape unit.
- 4) To secure tape, lower leader clamp.
- 5) Press the upper Reel Brake button to release the mechanical brake and pull tape from file reel to provide slack.
- 6) Unfasten mechanical splice which connects the file tab to the permanent machine leader.
- 7) Loosen file reel hub knob and remove the file reel.
- 8) Check if reel needs to be file protected and also if it is labeled adequately prior to storage.

FILE PROTECTION RING

The back of the file reel has a slot near the hub which accepts a plastic file protection ring (figure 4-10). Writing on a tape is possible only when the reel contains a file protection ring. The ring should be removed from the reel after writing is completed to avoid accidental rewriting. Tape may be read either with the ring in place or without it. On the 606 the overhead lights go on immediately after the tape load procedure is

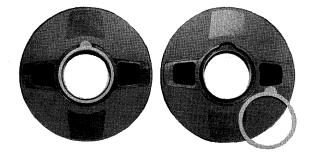


Figure 4-10. File Protection Ring

executed if the file protection ring is in place. The Write Lockout light on the 1607 is off if the file protection ring is in place.

EMERGENCY PROCEDURE

A fault indication, or a warning signal from the buzzer, may call for special procedures on the part of the operator.

CONDITION	PROCEDURE
Punch out of tape	Load new roll of tape in punch at end of current operation.
Odd Storage Fault	Master clear. Restart program.
Even Storage Fault	Master clear. Restart program.
Deep End	If all I/O operation has ceased, master clear and restart program. If condition persists, notify maintenance.
Sweep	Place Mode switch in neutral position.
Buzzer Signal	Notify maintenance engineer immediately.

TABLE 4-6.	EMERGENCY	PROCEDURE

Faults for which the program provides corrective action are: Divide, Shift, Overflow and Exponent Faults. (Refer to appendix.)

GLOSSARY

ABSOLUTE ADDRESS	A specific storage location; contrast with relative address.
ACCESS TIME	The time needed to perform a storage reference, either read or write. In effect, the access time of a computer is one storage reference cycle.
ACCUMULATOR	A register with provisions for the addition of another quantity to its content. It is also the name of the A register.
ADDER	A device capable of forming the sum of two or more quantities.
ADDRESS	A 15-bit quantity which identifies a particular storage location.
ALPHABETIC CODING	A system of abbreviation used in preparing information for input into a computer, e.g., Q Right Shift would be QRS.
AND FUNCTION	A logical function in Boolean algebra that is satisfied (has the value "1") only when all of its terms are "1's". For any other combin- ation of values it is not satisfied and its value is "0".
A REGISTER	Principal arithmetic register; operates as a 48-bit subtractive accumulator (modulus: 2 ⁴⁸ -1).
BASE	A quantity which defines some system of representing numbers by positional notation; radix.
BIT	Binary digit, either "1" or "0".
BLOCK	A group of words transported in and out of storage as a unit.
BOOTSTRAP	The coded instructions at the beginning of an input tape, together with the manually entered instructions.
BORROW	In a subtractive counter or accumulator, a signal indicating that in stage n, a "1" was subtracted from a "0". The signal is sent to stage n+1 which it complements.
BRANCH	A conditional jump.

1

BREAKPOINT	A point in a routine at which the computer may be stopped by a
1	manual switch for a visual check of progress.

B¹-B⁶ REGISTERS Index registers used primarily for modification of execution address.

- BUFFER A device in which data is stored temporarily in the course of transmission from one point to another. To store data temporarily. The operation in which either a word from storage is sent to an external equipment via an output channel (output buffer), or a word is sent from an external equipment to storage via an input channel (input buffer).
- CAPACITY The upper and lower limits of the numbers which may be processed in a register or the quantity of information which may be stored in a storage unit. If the capacity of a register is exceeded, an overflow is generated.
- CARRY In an additive counter or accumulator, a signal indicating that in stage n, a "1" was added to a "1". The signal is sent to stage n+1, which it complements.
- CHANNEL A transmission path that connects the computer to an external equipment.

CHARACTER Two types of information handled by the computer:

- A group of 6 bits which represents a digit, letter or symbol. In the assembly mode, eight 6-bit characters make up a computer word.
- A group of 7 bits which represents an item of information. In the character mode, this item is one 7-bit character and "0's" in the remaining (upper) 41 bits.
- CLEAR A command that removes a quantity from a register by placing every stage of the register in the "0" state.

CLOCK PHASE One of two outputs from the master clock, "even" or "odd".

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- COMMAND A signal that performs a unit operation, such as transmitting the content of one register to another, shifting a register one place to the left or setting a FF.
- COMPILER A routine which automatically produces a specific program for a particular problem. The routine determines the meaning of information expressed in a psuedo-code, selects or generates the required subroutine, transforms the subroutine into specific coding, assigns storage registers, and enters the information as an element of the problem program.
- COMPLEMENT Noun: see One's Complement or Two's Complement. Verb: a command which produces the one's complement of a given quantity.

CONTENT The quantity or word held in a register or storage location.

- CORE A ferromagnetic toroid used as the bistable device for storing a bit in a memory plane.
- COUNTER A register with provisions for increasing or decreasing its content by 1.

EVEN STORAGE The storage unit which contains the 16, 384 even addresses.

EXECUTIONThe lower 15 bits of a 24-bit instruction. Most often used to specifyADDRESSthe storage address of an operand. Sometimes used as the operand.

EXIT Initiation of a second control sequence by the first, occurring when the first is near completion; the circuit involved in exiting.

EXTERNAL1) External Function Select (74.0) sends a code to an externalFUNCTIONequipment to direct its operation.

2) External Function Sense (74.7) sends a code to an external equipment to sense its operating condition.

FAULT Operational difficulty which stops operation or sets an indicator.

- FIXED POINT A notation or system of arithmetic in which all numerical quantities are expressed by a predetermined number of digits with the binary point implicitly located at some predetermined position; contrasted with floating point.
- FLIP-FLOP (FF) A bistable storage device. A "1" input to the set side puts the FF in the "1" state; a "1" input to the clear side puts the FF in the "0" state. The FF remains in a state indicative of its last "1" input. A stage of a register consists of a FF.
- FLOATING POINT A means of expressing a number X by a pair of numbers, Y and Z, such that $X = Yn^{Z}$. Z is an integer, called the exponent or characteristic; n is a base, usually 2 or 10; and Y is called the fraction or mantissa.
- FUNCTION CODE The upper 9 bits of a 24-bit instruction consisting of the operation and index codes.
- INDEX CODE A 3-bit quantity, bits 15, 16, and 17 of an instruction; usually specifies an index register whose contents are added to the execution address; sometimes specifies the conditions for executing the instruction.
- INSTRUCTION A 24-bit quantity consisting of a function code, execution address, and index designator.

INTERRUPTA signal received from an external equipment that may cause a
special sequence of instructions to be executed.

INVERTER A circuit which provides as an output a signal that is opposite to its input. An inverter output is "1" only if all the separate OR inputs are "0".

- JUMP An instruction which alters the normal sequence control of the computer and, conditionally or unconditionally, specifies the location of the next instruction.
- LOAD To place a quantity from storage in a register.

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- LOCATION A storage position holding one computer word, usually designated by a specific address.
- LOGICAL
PRODUCTIn Boolean algebra, the AND function of several terms. The pro-
duct is "1" only when all the terms are "1"; otherwise it is "0".
Sometimes referred to as the result of "bit-by-bit" multiplication.
- LOGICAL SUM In Boolean algebra, the OR function of several terms. The sum is "1" when any or all of the terms are "1"; it is "0" only when all are "0".

LOOP Repetition of a group of instructions in a routine.

LOWER ADDRESS The execution address portion of a lower instruction; bits 0 through 14 of a 48-bit register or storage location.

LOWER See Program Step. INSTRUCTION

- MASK In some instructions, one quantity may determine what part of the other quantity is to be considered. If the first quantity, the mask, contains a "1", the corresponding bit of the second quantity is considered.
- MASTER CLOCK The source of standard signals required for sequencing computer operation. The clock determines the basic frequency of the computer.
- MASTER CLEAR A general command produced by placing the CLEAR switch up (MC) (external MC) or down (computer MC) which clears all the crucial registers and control FFs.
- MNEMONIC CODE A three-letter code which represents the function or purpose of an instruction. Also called Alphabetic Code.
- MODULUS An integer which describes certain arithmetic characteristics of registers, especially counters and accumulators, within a digital computer. The modulus of a device is defined by r^n for an open-ended device and r^n -1 for a closed (end-around) device, where r is

the base of the number system used and n is the number of digit positions (stages) in the device. Generally, devices with modulus r^n use two's complement arithmetic; devices with modulus r^{n-1} use one's complement.

NORMALIZE To adjust the exponent and mantissa of a floating-point result so that the mantissa lies in the prescribed standard (normal) range.

NORMAL JUMP An instruction that jumps from one sequence of instructions to a second, and makes no preparation for returning to the first sequence.

NUMERIC CODING A system of abbreviation in which all information is reduced to numerical quantities.

ODD STORAGE The storage unit which contains the 16, 384 odd addresses.

ONE'S COMPLEMENT With reference to a binary number, that number which results from subtracting each bit of the given number from "1". The one's complement of a number is formed by complementing each bit of it individually, that is, changing a "1" to "0" and a "0" to a "1". A negative number is expressed by the one's complement of the corresponding positive number.

ON-LINE A type of system application in which the input data to the system is OPERATION fed directly from the external equipment to the computer.

OPERAND Usually refers to the quantity specified by the execution address. This quantity is operated upon in the execution of the instruction.

OPERATIONAL Registers which are displayed on the operator's console (B^1-B^6) , A, Q, P, U^1).

OPERATION
CODEThe upper 6 bits of a 24-bit instruction which identify the instruc-
tion. After the code is translated, it conditions the computer for
execution of the specified instruction. This code, which is expressed
by two octal digits, is designated by the letter f.

O¹-O⁴ REGISTERS Output registers O^{1, 2, 3} are used for output buffer operations; O⁴ handles all high-speed output transfer operations.

OR FUNCTION A logical function in Boolean algebra that is satisfied (has the value "1") when any of its terms are "1". It is not satisfied when all terms are "0". Often called the 'inclusive' OR function.

OVERFLOW The capacity of a register is exceeded.

PARITY CHECK A summation check in which the binary digits in a character are added and the sum checked against a previously computed parity digit; i.e., a check which tests whether the number of ones is odd or even.

PARTIAL ADD An addition without carries. Accomplished by toggling each bit of the augend where the corresponding bit of the addend is a "1".

P REGISTER The Program Address Counter is a two's complement additive register (Modulus 2^{15}) which generates in sequential order the storage addresses containing the individual program steps.

- PROGRAM A precise sequence of instructions that accomplishes a computer routine; a plan for the solution of a problem.
- PROGRAM STEP Two 24-bit instructions contained in one 48-bit storage address; the higher-order 24 bits are the upper instruction, lower-order 24 bits, the lower instruction. A pair of instructions is read from storage, and the upper instruction is executed first. The lower one is then executed, except when the upper one provides for skipping the lower one.
- Q REGISTER Auxiliary arithmetic register which assists the A register in the more complicated arithmetic operations (Modulus: 2⁴⁸-1).
- RANDOM ACCESS Access to storage under conditions in which the next position from which information is to be obtained is in no way dependent on the previous one.
- R REGISTER Address Buffer register. Two's complement subtractive register (Modulus: 2¹⁵) which acts as an exchange register for transmissions involving index registers.

READ To remove a quantity from a storage location.

READY

 The input-output control signal sent by the computer or an external equipment. The ready signal indicates that a word or character is available for transmission.

- 2) A status reponse indicating that the external device being addressed is ready for operation.
- RELATIVE ADDRESS Identifies a word in a subroutine or routine with respect to its position. Relative addresses are translated into absolute addresses by the addition of some specific reference address, usually that at which the first word of the routine is stored.
- REPLACE In the title of an instruction, the result of the execution of the instruction is stored in the location from which the initial operand was obtained.
- RESUME The input-output control signal sent by either the computer or an external equipment to indicate that it is prepared to receive another word (48 bits) or character (usually 6 bits). The resume signal is thus a request for data.
- RETURN JUMP An instruction that jumps from a sequence of instructions to initiate a second sequence and prepares for continuing the first sequence after the second is completed.
- ROUTINE The sequence of operations which the computer performs under the direction of a program.
- S¹ REGISTER Storage Address register (even storage). Selects the storage address specified by the contents of the P register.
- S² REGISTER Storage Address register (odd storage). Selects the storage address specified by the contents of the P register.

SCALE FACTOR One or more coefficients by which quantities are multiplied or divided so that they lie in a given range of magnitude.

SCANNER That portion of the computer which automatically samples the state of the buffer channels, interrupt line, and real time clock and initiates action in accordance with the information obtained.

SECONDARY REGISTERS Transient registers not displayed on the console $(U^2, S^{1,2}, Z^{1,2}, R, X, O^{1}-O^{6})$.

SHIFT To move the bits of a quantity right or left.

SIGN BIT In registers where a quantity is treated as signed by use of one's complement notation, the bit in the highest-order stage of the register. If the bit is "1", the quantity is negative; if the bit is "0", the quantity is positive.

SIGNThe duplication of the sign bit in the higher-order stages of aEXTENSIONregister.

SKIP To omit the execution of a lower instruction in a program; occurs only if the upper instruction provides for skipping on a specified condition, and the condition is met.

STAGE The FFs and inverters associated with a bit position of a register.

STORETo transmit information to a device from which the unalteredinformation can later be obtained.

SUBINSTRUCTION The index code specifies one of eight forms of the instruction indicated by the operation code. Such forms are called "subinstructions". Thus, 74.0 is a subinstruction of instruction 74.

TOGGLE To complement each bit of a quantity as a result of an individual condition.

TRANSFER High-speed data input-output transmission under direct program control.

TRANSMISSION, FORCED	A transfer of bits into a register which has not been cleared previously.		
TWO'S COMPLEMENT	Number that results from subtracting each bit of a number from "0". The two's complement may be formed by complementing each bit of the given number and then adding one to the result, performing the required carries.		
u ¹ register	Program Control register. Holds a program step while the two instructions contained in it are executed.		
U ² REGISTER	Auxiliary Program Control register. A 15-bit subtractive accumulator (Modulus: 2^{15} -1) used primarily for modification of the base execution address.		
UPPER ADDRESS	The execution address portion of an upper instruction; bit positions 24 through 38 of a 48-bit register or storage address.		
UPPER INSTRUCTION	See Program Step		
WORD	A unit of information which has been coded for use in the computer as a series of bits. The normal word length is 48 bits.		
WRITE	To enter a quantity into a storage location.		
X REGISTER	Exchange register. All internal transmissions between the arithmetic section or the input-output section and the rest of the computer are made through X.		
z^1 register	Storage Restoration register (even storage). Holds the word to be written into a given storage location.		
z^2 register	Storage Restoration register (odd storage). Holds the word to be written into a given storage location.		

APPENDIX SECTION

APPENDIX I NUMBER SYSTEMS

Any number system may be defined by two characteristics, the radix or base and the modulus. The radix or base is the number of unique symbols used in the system. The decimal system has ten symbols, 0 through 9. Modulus is the number of unique quantities or magnitudes a given system can distinguish. For example, an adding machine with ten digits, or counting wheels, would have a modulus of 10^{10} -1. The decimal system has no modulus because an infinite number of digits can be written, but the adding machine has a modulus because the highest number which can be expressed is 9, 999, 999, 999.

Most number systems are positional, that is, the relative position of a symbol determines its magnitude. In the decimal system, a 5 in the units column represents a different quantity than a 5 in the tens column. Quantities equal to or greater than 1 may be represented by using the 10 symbols as coefficients of ascending powers of the base 10. The number 984_{10} is:

$$9 \times 10^{2} = 9 \times 100 = 900$$

+8 \times 10^{1} = 8 \times 10 = 80
+4 \times 10^{0} = 4 \times 1 = 4
984₁₀

Quantities less than 1 may be represented by using the 10 symbols as coefficients of ascending negative powers of the base 10. The number 0.593_{10} may be represented as:

$$5 \times 10^{-1} = 5 \times .1 = .5$$

+9 \times 10^{-2} = 9 \times .01 = .09
+3 \times 10^{-3} = 3 \times .001 = .003
0.593₁₀

BINARY NUMBER SYSTEM

Computers operate faster and more efficiently by using the binary number system. There are only two symbols 0 and 1; the base = 2. The following shows the positional value.

 2^5	2^4	2^{3}	2^{2}	2^1	2^0	
=32	=16	=8	=4	=2	=1	Binary point

The binary number 0 1 1 0 1 0 represents:

$$0 \times 2^{5} = 0 \times 32 = 0$$

+1 \times 2^{4} = 1 \times 16 = 16
+1 \times 2^{3} = 1 \times 8 = 8
+0 \times 2^{2} = 0 \times 4 = 0
+1 \times 2^{1} = 1 \times 2 = 2
+0 \times 2^{0} = 0 \times 1 = 0
26
10

Fractional binary numbers may be represented by using the symbols as coefficients of ascending negative powers of the base.

 2^{-1} 2^{-2} 2^{-3} 2^{-4} 2^{-5} . . . Binary Point . =1/2 =1/4 =1/8 =1/16 =1/32

The binary number 0.10 110 may be represented as:

 $1 \times 2^{-1} = 1 \times 1/2 = 1/2 = 8/16$ +0 x 2⁻² = 0 x 1/4 = 0 = 0 +1 x 2⁻³ = 1 x 1/8 = 1/8 = 2/16 +1 x 2⁻⁴ = 1 x 1/16 = 1/16 = 1/16 11/16₁₀

OCTAL NUMBER SYSTEM

The octal number system uses eight discrete symbols, 0 through 7. With the base eight the positional value is:

The octal number 5138 represents:

$$5 \times 8^{2} = 5 \times 64 = 320$$

+1 x 8¹ = 1 x 8 = 8
+3 x 8⁰ = 3 x 1 = 3
331₁₀

Fractional octal numbers may be represented by using the symbols as coefficients of ascending negative powers of the base.

8^{-1}	8^{-2}	8-3	8 ⁻⁴
1/8	1/64	1/512	1/4096

The octal number 0.4520 represents:

$$4 \times 8^{-1} = 4 \times 1/8 = 4/8 = 256/512$$

+5 x 8⁻² = 5 x 1/64 = 5/64 = 40/512
+2 x 8⁻³ = 2 x 1/512 = 2/512 = 2/512
298/512 = 149/256₁₀

ARITHMETIC

ADDITION AND SUBTRACTION

Binary numbers are added according to the following rules:

The addition of two binary numbers proceeds as follows (the decimal equivalents verify the result):

Augend	0111	(7)
Addend	+0100	+(4)
Partial Sum	0011	
Carry	1	
Sum	1011	(11)

Subtraction may be performed as an addition:

-8	(minuend)		- 8	(minuend)
- 6	(subtrahend)	or	+4	(10's complement or subtrahend)
2	(difference)		2	(difference - omit carry)

The second method shows subtraction performed by the "adding the complement" method. The omission of the carry in the illustration has the effect of reducing the result by 10.

One's Complement

The 1604 performs all arithmetic operations in the binary one's complement mode. In this system, positive numbers are represented by the binary equivalent and negative numbers in one's complement notation.

The one's complement representation of a number is found by subtracting each bit of the number from 1. For example:

1111	
-1001	9
0110	(one's complement of 9)

This representation of a negative binary quantity may also be obtained by substituting "1's" for "0's" and "0's" for "1's".

The value zero can be represented in one's complement notation in two ways:

 $0000 \rightarrow 00_2$ Positive (+) Zero 1111 $\rightarrow 11_2$ Negative (-) Zero

The rules regarding the use of these two forms for computation are:

- 1) Both positive and negative zero are acceptable as arithmetic operands.
- If the result of an arithmetic operation is zero, it will be expressed as positive zero. The one exception to this rule is when negative zero is added to negative zero.* In this case, the result is negative zero.

One's complement notation applies not only to arithmetic operations performed in A, but also to the modification of execution addresses in the U^2 register. During address modification, the modified address will equal 77777₈ only if the unmodified execution address equals 77777₈ and b = 0 or (B^b) = 77777₈.

Two's Complement

The counters in the computer use two's complement arithmetic. A counter is a register with provisions for increasing its contents by one if it is additive (P register) or decreasing its contents by one if it is subtractive (R register). A two's complement counter is open-ended; there is no end-around carry or borrow.

^{*} When a 1604 instruction calls for subtracting positive zero from negative zero, the computer complements the subtrahend and adds so that the actual operation is the addition of negative zero to negative zero and the result is negative zero.

Positive numbers have the same representation in both systems while negative values differ by one count.

Count	2's comp. rep.	l's comp. rep.
+2	00010	00010
+1	00001	00001
0	00000	00000
-1	11111	11110
-2	11110	11101

The difference in the representation of negative values in these two systems is due to the skipping of the "all one's" count in one's complement notation. In the one's complement system the end-around-carry feature of the register automatically changes a count of all one's to all zeros. (Note exception under one's complement.)

As an example, if the content of a subtractive counter is positive seven (0111) and is to be reduced by one, add the two's complement expression of negative one, (1111), to 0111 as shown below. The result is six.

$$\begin{array}{r}
 0111 \\
 +1111 \\
 0110
 \end{array}$$

Note that the two's complement expression for a negative number may also be formed by adding one to the one's complement representation of the number.

MULTIPLICATION

Binary multiplication proceeds according to the following rules:

 $0 \ge 0 = 0$ $0 \ge 1 = 0$ $1 \ge 0 = 0$ $1 \ge 1 = 1$

Multiplication is always performed on a bit-by-bit basis. Carries do not result from multiplication, since the product of any two bits is always a single bit.

Decimal example	:		
	multiplicand	14	
	multiplier	12	
	partial products	28	
		14	(shifted one place left)
	product	168_{1}	0

The shift of the second partial product is a shorthand method for writing the true value 140.

Binary example:

multiplicand	(14)	1110	
multiplier	(12)	1100	
		0000	
		0000	shift to place digits
partial produc	ets {	1110	in proper columns
	l	1110	
product (16	8 ₁₀)	$10101000_{\textstyle 2}$	

The computer determines the running subtotal of the partial products. Rather than shifting the partial product to the left to position it correctly, the computer right shifts the summation of the partial products one place before the next addition is made. When the multiplier bit is "1", the multiplicand is added to the running total and the results are shifted to the right one place. When the multiplier bit is "0", the partial product subtotal is shifted to the right (in effect, the quantity has been multiplied by 10_2).

DIVISION

The following example shows the familiar method of decimal division:

		14	quotient
divisor	13	185	dividend
		13	
		55	partial dividend
		52_	
		3	remainder

	1110	quotient (14)
divisor	1101 10111001	dividend
	1101	
	10100	
	1101	
	1110	partial dividends
	1101	
	11	remainder (3)

The computer performs division in a similar manner (using binary equivalents):

However, instead of shifting the divisor right to position it for subtraction from the partial dividend (shown above), the computer shifts the partial dividend left, accomplishing the same purpose and permitting the arithmetic to be performed in the A register. The computer counts the number of shifts, which is the number of quotient digits to be obtained; after the correct number of counts, the routine is terminated.

CONVERSIONS

The procedures that may be used when converting from one number system to another are power addition, double dabble, and substitution.

Conversion	Recommended Method
Binary to Decimal	Power Addition
Octal to Decimal	Power Addition
Decimal to Binary	Double Dabble
Decimal to Octal	Double Dabble
Binary to Octal	Substitution
Octal to Binary	Substitution
GENERAL	RULES
$r_i > r_f$: use Double Dabbl	e, Substitution
$r_i < r_f$: use Power Addition, Substitution	
r _i = Radix of initial system	
r_{f} = Radix of final system	

Recommended Conversion Procedures (Integer and Fractional)

POWER ADDITION

To convert a number from r_i to $r_f (r_i < r_f)$ write the number in its expanded r_i polynomial form and simplify using r_f arithmetic.

Binary to Decimal (Integer) EXAMPLE | $010\ 111_2 = 1\ (2^4) + 0\ (2^3) + 1\ (2^2) + 1\ (2^1) + 1\ (2^0)$ = 1 (16) + 0 (8) + 1 (4) + 1 (2) + 1 (1) = 16 + 0 + 4 + 2 + 1 $= 23_{10}$ Binary to Decimal (Fractional) **EXAMPLE 2** $.0101_{2} = 0 (2^{-1}) + 1 (2^{-2}) + 0 (2^{-3}) + 1 (2^{-4})$ = 0 + 1/4 + 0 + 1/16 $= 5/16_{10}$ **EXAMPLE 3** Octal to Decimal (Integer) $324_8 = 3 (8^2) + 2 (8^1) + 4 (8^0)$ = 3 (64) + 2 (8) + 4 (1)= 192 +16 + 4 $= 212_{10}$ EXAMPLE 4 Octal to Decimal (Fractional) $.44_8 = 4 (8^{-1}) + 4 (8^{-2})$ = 4/8 + 4/64 $= 36/64_{10}$

DOUBLE DABBLE

To convert a whole number from r_i to r_f ($r_i > r_f$):

- 1) Divide r_i by r_f using r_i arithmetic
- 2) The remainder is the lowest order bit in the new expression
- 3) Divide the integral part from the previous operation by r_f
- 4) The remainder is the next higher order bit in the new expression
- 5) The process continues until the division produces only a remainder which will be the highest order bit in the r_f expression.

To convert a fractional number from r_i to r_f :

- 1) Multiply r_i by r_f using r_i arithmetic
- 2) The integral part is the highest order bit in the new expression
- 3) Multiply the fractional part from the previous operation by r_{f}
- 4) The integral part is the next lower order bit in the new expression
- 5) The process continues until sufficient precision is achieved or the process terminates.

EXAMPLE	1	Decimal to Binary (Integer)	
	45 ÷	2 = 22 remainder 1; record	1
	22 ÷	2 = 11 remainder 0; record	0
	11 ÷	2 = 5 remainder 1; record	1
	5 ÷	2 = 2 remainder 1; record	1
	2 ÷	2 = 1 remainder 0; record	0
	1 ÷	2 = 0 remainder 1; record	_1
	Thus:	$45_{10} = 101101_2$	101101

EXAMPLE	2	Decimal to Binary	(Fractional)
	.25 x 2	= 0.5; record	0
	.5 x 2	= 1.0; record	1
	.0 x 2	= 0.0; record	0
	Thus:	$.25_{10} = .010_2$.010

EXAMPLE 3

Decimal to Octal (Integer)

273 ÷	8 = 34 remainder 1; record	1
34 ÷	8 = 4 remainder 2; record	2
4 ÷	8 = 0 remainder 4; record	
Thus:	$273_{10} = 421_8$	421

EXAMPLE 4

Decimal to Octal (Fractional)

.55 x 8 = 4.4; record	4
.4 x 8 = 3.2; record	3
.2 x 8 = 1.6; record	1
	-
Thus: $.55_{10} = .4318$. 431

SUBSTITUTION

This method permits easy conversion between octal and binary representations of a number. If a number in binary notation is partitioned into triplets to the right and left of the binary point, each triplet may be converted into an octal digit. Similarly each octal digit may be converted into a triplet of binary digits.

EXAMPLE I Binary to Octal

Binary = 110 000 . 001 010 Octal = 6 0 . 1 2

EXAMPLE 2 Octal to Binary

Octal = 6 5 0 . 2 2 7 Binary = 110 101 000 . 010 010 111

Decimal	Binary	Octal
00	00000	00
01	00001	01
02	00010	02
03	00011	03
04	00100	04
05	00101	05
06	00110	06
07	00111	07
08	01000	10
09	01001	11
10	01010	12
11	01011	13
12	01100	14
13	01101	15
14	01110	16
15	01111	17
16	10000	20
17	10001	21

COMMON PURE NOTATIONS

POWERS OF COMMON NUMBER SYSTEMS

2^{0} 2^{1} 2^{2} 2^{3} 2^{4} 2^{5} 2^{6} 2^{7} 2^{8} 2^{9}		1 2 4 8 16 32 64 128 256 5 12	$8^{0} =$ $8^{1} =$ $8^{2} =$ $8^{3} =$ $8^{4} =$ $8^{5} =$ $8^{6} =$ $8^{7} =$ $8^{8} =$	1 8 64 512 4,096 32,768 262,144 2,097,152 16,777,216	$10^{0} = 10^{1} = 10^{2} = 10^{2} = 10^{3} = 10^{4} = 10^{5} = 10^{6} = 1$	1 10 100 1,000 10,000 100,000 1,000,000
2^{8} 2^{9} 2^{10}	= = =	256 512 1,024				

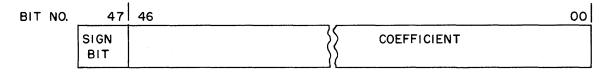
FIXED POINT AND FLOATING POINT NUMBERS

Any number may be expressed in the form kB^n , where k is a coefficient, B a base number, and the exponent n the power to which the base number is raised.

A fixed point number assumes:

- 1) The exponent n = 0 for all fixed point numbers.
- 2) The coefficient, k, occupies the same bit positions within the computer word for all fixed point numbers.
- 3) The radix (binary) point remains fixed with respect to one end of the expression.

A 1604 fixed point number consists of a sign bit and coefficient as shown below. The upper bit of any 1604 fixed point number designates the sign of the coefficient (47 lower order bits). If the bit is "1", the quantity is negative since negative numbers are represented in one's complement notation; a "0" sign bit signifies a positive coefficient.



The coefficient may be an integer or fraction. The radix (binary) point, in the case of an integer, is assumed to be immediately to the right of the lowest order bit (00). In the case of the fraction, the point is just to the right of the sign bit.

In many instances, the values in a fixed point operation may be too large or too small to be expressed by the computer. The programmer must position the numbers within the word format so they can be represented with sufficient precision. The process, called scaling, consists of shifting the values a predetermined number of places. The numbers must be positioned far enough to the right in the register to prevent overflow but far enough to the left to maintain precision. The scale factor (number of places shifted) is expressed as the power of the base. For example, $5,100,000_{10}$ may be expressed as 0.51×10^7 , 0.051×10^8 , 0.0051×10^9 , etc. The scale factors are 7, 8, and 9.

Since only the coefficient is used by the computer, the programmer is responsible for remembering the scale factors. Also, the possibility of an overflow during intermediate operations must be considered. For example, if two fractions in fixed point format are multiplied, the result is a number < 1. If the same two fractions are added, subtracted, or divided, the result may be greater than one and an overflow will occur. Similarly, if two integers are multiplied, divided, subtracted or added, the likelihood of an over-flow is apparent.

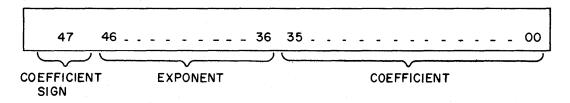
As an alternative to fixed point operation, a method involving a variable radix point, called floating point, is used. This significantly reduces the amount of bookkeeping required on the part of the programmer.

By shifting the radix point and increasing or decreasing the value of the exponent, widely varying quantities which do not exceed the capacity of the machine may be handled.

Floating point numbers within the computer are represented in a form similar to that used in "scientific" notation, that is, a coefficient or fraction multiplied by a number raised to a power. Since the computer uses only binary numbers, the numbers are multiplied by powers of two.

> $F \cdot 2^E$ where: F = fractionE = exponent

In floating point, different coefficients need not relate to the same power of the base as they do in fixed point format. Therefore, the construction of a floating point number includes not only the coefficient but also the exponent.



Coefficient

The coefficient consists of a 36-bit fraction in the 36 lower-order positions of the floating point word. The coefficient is a normalized fraction; it is equal to or greater than 1/2 but less than 1. The highest order bit position (47) is occupied by the sign bit of the coefficient. If the sign bit is a "0", the coefficient is positive; a "1" bit denotes a negative fraction (negative fractions are represented in one's complement notation).

Exponent

The floating point exponent is expressed as an 11-bit quantity with a value ranging from 0000_8 to 3777_8 . It is formed by adding a true positive exponent and a bias of 2000_8 or a true negative exponent and a bias of 1777_8 . This results in a range of biased exponents as shown below.

True Positive Exponent	Biased Exponent	True Negative Exponent	Biased Exponent
+0	2000	-0	2000*
+1	2001	-1	1776
+2	2002	-2	1775
			
			
+1776	3776	-1776	0001
+177788	3777 ₈	-17778	00008

The exponent is biased so that floating point operands can be compared with each other in the normal fixed point mode.

As an example, compare the unbiased exponents of $+52_8$ and $+0.02_8$ (Example 1).

EXAMPLE I Number = +520 0 0 000 000 (36 bits) 110 Coefficient Exponent Coefficient Sign Number = +0.02011 (36 bits) 0 1 1 111 111 Coefficient Exponent Coefficient Sign

In this case +0.02 appears to be larger than +52 because of the larger exponent. If, however, both exponents are biased, (Example 2) changing the sign of both exponents makes +52 greater than +0.02.

^{*} Minus zero is sensed as positive zero by the computer and is therefore biased by 2000_8 rather than 1777_8 .

EXAMPLE	2	Number =	+528			
	0	1 0	000	000	110	(36 bits)
	Coefficient Sign		Exp	onent		Coefficient
		Number =	+0.028			
	0	0 1	111	111	011	(36 bits)
	Coefficient Sign		Expo	onent		Coefficient

When bias is used with the exponent floating-point operation is more versatile since floating-point operands can be compared with each other in the normal fixed point mode.

CONVERSION PROCEDURES

Fixed Point to Floating Point

- 1) Express the number in binary.
- 2) Normalize the number. A normalized number has the most significant 1 positioned immediately to the right of the binary point and is expressed in the range $1/2 \le k \le 1$.
- 3) Inspect the sign of the true exponent. If the sign is positive add 2000₈ (bias) to the true exponent of the normalized number. If the sign is negative add the bias 1777₈ to the true exponent of the normalized number. In either case, the resulting exponent is the biased exponent.
- 4) Assemble the number in floating point.
- 5) Inspect the sign of the coefficient. If negative, complement the assembled floating point number to obtain the true floating point representation of the number. If the sign of the coefficient is positive the assembled floating point number is the true representation.

EXAMPLE I Convert +4.0 to floating point

- 1) The number is expressed in octal.
- 2) Normalize. $4.0 = 4.0 \times 8^0 = 0.100 \times 2^3$.
- Since the sign of the true exponent is positive, add 2000₈ (bias) to the true exponent. Biased exponent = 2000 + 3.

- 4) Assemble number in floating point format. Coefficient = $400\ 000\ 000\ 000_{9}$ Biased Exponent = 2003_{g} Assembled word = 2003 400 000 000 000₈
- Since the sign of the coefficient is positive, the floating point representation of 5) +4.0 is as shown. If, however, the sign of the coefficient were negative, it would be necessary to complement the entire floating point word.

EXAMPLE 2 Convert - 4.0 to floating point

- 1) The number is expressed in octal.
- Normalize. $-4.0 = -4.0 \times 8^0 = -0.100 \times 2^3$ 2)
- Since the sign of the true exponent is positive, add 2000_8 (bias) to the true 3) exponent. Biased exponent = 2000 + 3.
- 4) Assemble number in floating point format. Coefficient = 400 000 000 000₈ Biased Exponent = 2003_{g}

Assembled word = 2003 400 000 000 000_{0}

Since the sign of the coefficient is negative, the assembled floating point word 5) must be complemented. Therefore, the true floating point representation for $-4.0 = 5774 \ 377 \ 777 \ 777 \ 777_{\Omega}$

Convert 0.5_{10} to floating point EXAMPLE 3

- 1)
- Convert to octal. $0.5_{10} = 0.4_8$ Normalize. $0.4 = 0.4 \times 8^0 = 0.100 \times 2^0$ 2)
- Since the sign of the true exponent is positive, add 2000_8 (bias) to the true 3) exponent. Biased exponent = 2000 + 0.
- Assemble number in floating point format. 4)

Coefficient = 400 000 000 000_o

Biased Exponent = 2000_{g}

- Assembled word = 2000 400 000 000 000_{g}
- 5) Since the sign of the coefficient is positive, the floating point representation of $+0.5_{10}$ is as shown. If, however, the sign of the coefficient were negative, it would be necessary to complement the entire floating point word. This example is a special case of floating point since the exponent of the normalized number is 0 and could be represented as -0. The exponent would then be biased by 1777_{9} instead of 2000_g because of the negative exponent. The 1604, however, recognizes -0 as +0 and biases the exponent by 2000_8 .

EXAMPLE 4 Convert 0.04₈ to floating point

- 1) The number is expressed in octal.
- 2) Normalize. $0.04 = 0.04 \times 8^0 = 0.4 \times 8^{-1} = 0.100 \times 2^{-3}$.
- 3) Since the sign of the true exponent is negative, add 1777_8 (bias) to the true exponent. Biased exponent = $1777_8 + (-3) = 1774_8$.
- 4) Assemble number in floating point format.

Coefficient = $400\ 000\ 000\ 000_{9}$

Biased Exponent = 1774₈

Assembled word = $1774 400 000 000 000_{0}$

5) Since the sign of the coefficient is positive, the floating point representation of 0.04₈ is as shown. If, however, the sign of the coefficient were negative, it would be necessary to complement the entire floating point word.

Floating Point to Fixed Point Format

- If the floating point number is negative, complement the entire floating point word and record the fact that the quantity is negative. The exponent is now in a true biased form.
- 2) If the biased exponent is equal to or greater than 2000_8 subtract 2000_8 to obtain the true exponent. If less than 2000_8 subtract 1777_8 to obtain true exponent.
- 3) Separate the coefficient and exponent. If the true exponent is negative the binary point should be moved to the left the number of bit positions indicated by the true exponent. If the true exponent is positive, the binary point shoud be moved to the right the number of bit positions indicated by the true exponent.
- 4) The coefficient has now been converted to fixed binary. The sign of the coefficient will be negative if the floating point number was complemented in step one. (The sign bit must be extended if the quantity is placed in a register.)
- 5) Represent the fixed binary number in fixed octal notation.

EXAMPLE I Convert floating point number 2003 400 000 000 000₈ to fixed octal

- 1) The floating point number is positive and remains uncomplemented.
- 2) The biased exponent > 2000_8 , therefore subtract 2000_8 from the biased exponent to obtain the true exponent of the number. 2003 2000 = +3
- 3) Coefficient = 400 000 000 000₈ = .100₂. Move binary point to the right 3 places. Coefficient = 100.0₂

- 4) The sign of the coefficient is positive because the floating point number was not complemented in step one.
- 5) Represent in fixed octal notation. $100.0 \ge 2^0 = 4.0 \ge 8^0$
- EXAMPLE 2 Convert floating point number 5774 377 777 777 777 777₈ to fixed octal
 - 1) The sign of the coefficient is negative, therefore, complement the floating point number.

Complement = 2003 400 000 000 000₈

- 2) The biased exponent (in complemented form) > 2000_8 , therefore subtract 2000_8 from the biased exponent to obtain the true exponent of the number. 2003 - 2000 = +3
- 3) Coefficient = $4000\ 000\ 000\ 000_8 = 0.100_2$ Move binary point to the right 3 places. Coefficient = 100.0_2
- 4) The sign of the coefficient will be negative because the floating point number was originally complemented.
- 5) Convert to fixed octal. $-100.0_2 = -4.0_8$

EXAMPLE 3 Convert floating point number 1774 400 000 000 000₈ to fixed octal

- 1) The floating point number is positive and remains uncomplemented.
- 2) The biased exponent $< 2000_8$, therefore subtract 1777_8 from the biased exponent to obtain the true exponent of the number. $1774_8 1777_8 = -3$
- 3) Coefficient = $400\ 000\ 000\ 000_8$ = $.100_2$ Move binary point to the left 3 places. Coefficient = $.000100_9$
- 4) The sign of the coefficient is positive because the floating point number was not complemented in step one.
- 5) Represent in fixed octal notation. $.000100_2 = .04_8$

APPENDIX II FAULTS

Certain fault conditions may occur in the execution of a computer program which may be sensed by EXF instructions. The occurrence of the fault does not stop operation but sets an indicator that can be sensed. A fault is visually indicated on the console.

Shift Fault

Any attempt to shift a register more than 127_{10} (177₈) places right or left results in a shift fault. If the fault exists, the indicator is set prior to execution of the shift instruction and the shift fault background light on the console display panel is lighted. The shifts will be performed regardless of the status of the fault indicator. If an interrupt has been selected, the main program will be interrupted after executing the shift instruction. The shift fault may be sensed by 74 7 00120, 1.

Divide Fault

A divide fault occurs in fixed point divide instructions (25 and 27) when the divisor is zero or the required quotient exceeds the 47-bit capacity of the quotient register, Q. The sign bit of Q is examined at the end of the division phase. If it is equal to "1", a divide fault has occurred. If an interrupt has been selected, the main program will be interrupted after the divide instruction is completed. A divide fault is sensed by a 74 0 00110, 1.

Overflow Fault

An overflow fault is produced when the capacity of the A register (> 2^{47} -1) is exceeded. The fault is sensed after the arithmetic operation causing the overflow is completed. An overflow may be sensed by a 74 7 00130, 1.

If an interrupt has been selected, the main program will not be halted until one or two of the next instructions have been executed because the scanner may not immediately recognize the interrupt. If the scanner is within four scanning positions of the interrupt, after executing the first instruction, the second instruction will not be executed. If it is farther than four positions from the interrupt, the second instruction could also be executed.

A pass or sense overflow instruction could be programmed after the arithmetic instruction which causes the overflow. The interrupt would, in this case, be recognized before executing succeeding instructions which might alter the contents of the A register.

Exponent (Floating Point Range) Fault

The exponent fault occurs during floating point instructions when the exponent of the result, after rounding and normalizing, is $\ge 2^{\pm 10}$ (overflow) or $\le 2^{-10}$ (underflow). The exponent fault is sensed by a 74 7 00140, 1.

If an interrupt has been selected on exponent fault, the main program may not be interrupted until one and possibly two of the next instructions are executed.

By using a pass or sense exponent fault instruction following the floating point instruction, the interrupt is recognized prior to executing succeeding instructions.

Even and Odd Storage Faults

These faults indicate a failure in computer storage and turn on background lights on the console display. The indicators may be cleared by an internal master clear. If a storage fault is produced, maintenance should be notified.

APPENDIX III

	,				.			-	T/	٩BL	ЕC	DF F	POV	VER	RS (DF T	TW	0										
					- - -	2" 1 2 4 8	n 0 1 2 3	2 ⁻ " 1.0 0.5 0.25 0.125																	-		-	
						16 32 64 128	4 5 6 7	0.062 0.031 0.015 0.007	25 625	5																		
						256 512 024 048	8 9 10 11	0.003 0.001 0.000 0.000	953 976	125 562	-																	
					8 16	096 192 384 768	12 13 14 15	0.000 0.000 0.000 0.000	122 061	070 035	312 156	25																
					131 262	536 072 144 288	16 17 18 19	0.000 0.000 0.000 0.000	007 003	629 814	394 697	531 265	25 625	5														
				2 4 8	048 097 194 388	152 304 608	20 21 22 23	0 000 0 000 0 000 0 000	000 000 000	476 238 119	837 418 209	158 579 289	203 101 550	125 562 781	25													
				33 67 134	777 554 108 217	432 864 728	24 25 26 27	0.000 0.000 0.000 0.000	000 000 000	029 014 007	802 901 450	322 161 580	387 193 596	695 847 923	312 656 828	25 125												
			2	536 073 147	435 870 741 483	912 824 648	28 29 30 31	0.000 0.000 0.000 0.000	000 000 000	001 000 000	862 931 465	645 322 661	149 574 287	230 615 307	957 478 739	031 515 257	25 625 812											
			8 17 34	589 179 359	967 934 869 738	592 184 368	32 33 34 35	0.000 0.000 0.000 0.000	000 000 000	000 000 000	116 058 029	415 207 103	321 660 830	826 913 456	934 467 733	814 407 703	453 226 613	125 562 281	25									
			137 274 549	438 877 755	476 953 906 813	472 944 888	36 37 38 39	0.000 0.000 0.000 0.000	000 000 000	000 000 000	007 003 001	275 637 818	957 978 989	614 807 403	183 091 545	425 712 856	903 951 475	320 660 830	312 156 078	25 125	F							
		2 4 8	199 398 796	023 046 093	255 511 022	208	43	0.000 0.000 0.000 0.000	000 000 000	000 000 000	000 000 000	454 227 113	747 373 686	350 675 837	886 443 721	464 232 616	118 059 029	957 478 739	519 759 379	531 765 882	25 625 812	5						
		35 70 140	184 368 737	372 744 488	088 177 355	416 832 664 328	45 46 47	0.000 0.000 0.000 0.000	000 000 000	000 000 000	000 000 000	028 014 007	421 210 105	709 854 427	430 715 357	404 202 601	007 003 001	4 <u>3</u> 4 717 858	844 422 711	970 485 242	703 351 675	125 562 781	25					
	1 2	562 125 251	949 899 799	953 906 813	421 842 685	656 312 624 248	50 51	0.000 0.000 0.000 0.000	000 000 000	000 000 000	000 000 000	001 000 000	776 888 444	356 178 089	839 419 209	400 700 850	250 125 062	464 232 616	677 338 169	810 905 452	668 334 667	945 472 236	312 656 328	5 25 125				
3	9 18 36	007 014 028	199 398 797	254 509 018	740 481 963	496 992 984 968	53 54 55	0.000 0.000 0.000 0.000	000 000 000	000 000 000	000 000 000	000 000 000	111 055 027	022 511 755	302 151 575	462 231 615	515 257 628	654 827 913	042 021 510	363 181 590	166 583 791	809 404 702	082 541 270	031 015 507	25 625 812			
14 28 57	44 38 76	115 230 460	188 376 752	075 151 303	855 711 423	936 872 744 488	57 58 59	0.000 0.000 0.000 0.000	000 000 000	000 000 000	000 000 000	000 000 000	006 003 001	938 469 734	893 446 723	903 951 475	907 953 976	228 614 807	377 188 094	647 823 411	697 848 924	925 962 481	567 783 391	626 813 906	953 476 738	125 562 281	25	
1 18	5Z	921	504	606	846	9/6	00	0.000		000	000	000	000	80/	301	131	988	403	54/	205	962	240	095	953	209	140	025	

APPENDIX IV

OCTAL-DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		
0000	0000	0001	0002	0003	0004	0005	0006	0007	0400	0256	0257	0258	0259	0260	0261	0262	0263	0000	0000
0010	0008	0009	0010	0011	0012	0013	0014	0015	0410	0264	0265	0266	0267	0268	0269	0270	0271	to	to
0020 0030	0016 0024	0017 0025	0018 0026	0019 0027	0020 0028	0021	0022 0030	0023 0031	0420	0272 0280	0273 0281	0274 0282	0275 0283	0276 0284	0277 0285	0278 0286	0279 0287	0777	0511
0040	0032	0033	0034	0035	0036	0037	0038	0039	0440	0288	0289	0290	0291	0292	0293	0294	0295	(Octal)	(Decimal)
0050	0040 0048	0041 0049	0042 0050	0043 0051	0044 0052	0045 0053	0046 0054	0047 0055	0450	0296 0304	0297 0305	0298 0306	0299 0307	0300 0308	0301 0309	0302 0310	0303 0311	1	
0070	0048	0057	0058	0059	0060	0055	0062	0063	0470	0312	0313	0314	0315	0316	0317	0318	0319	Octal	Decimal
				0007			0070	0074	0500					0004	0005	0000	0007	10000	4096
0100	0064 0072	0065 0073	0066 0074	0067 0075	0068 0076	0069 0077	0070 0078	0071 0079	0500	0320 0328	0321 0329	0322 0330	0323 0331	0324 0332	0325 0333	0326 0334	0327 0335		8192
0120	0080	0081	0082	0083	0084	0085	0086	0087	0520	0336	0337	0338	0339	0340	0341	0342	0343	1	12288
0130	0088	0089	0090	0091	0092	0093	0094	0095	0530	0344	0345	0346 0354	0347 0355	0348 0356	0349 0357	0350 0358	0351 0359		20480
0140 0150	0096 0104	0097 0105	0098 0106	0099 0107	0100 0108	0101 0109	0102 0110	0103 0111	0540	0352 0360	0353 0361	0354	0363	0364	0365	0356	0355		24576
0160	0112	0113	0114	0115	0116	0117	0118	0119	0560	0368	0369	0370	0371	0372	0373	0374	0375	70000	28672
0170	0120	0121	0122	0123	0124	0125	0126	0127	0570	0376	0377	0378	0379	0380	0381	0382	0383		
0200	0128	0129	0130	0131	0132	0133	0134	0135	0600	0384	0385	0386	0387	0388	0389	0390	0391		
0210	0136	0137	0138	0139	0140	0141 0149	0142 0150	0143 0151	0610 0620	0392 0400	0393 0401	0394 0402	0395 0403	0396 0404	0397 0405	0398 0406	0399 0407	1	
0220 0230	0144 0152	0145 0153	0146 0154	0147 0155	0148 0156	0149	0150	0151	0620	0400	0401	0402	0403	0404	0405	0406	0407		
0240	0160	0161	0162	0163	0164	0165	0166	0167	0640	0416	0417	0418	0419	0420	0421	0422	0423		
0250	0168	0169	0170	0171	0172	0173	0174	0175	0650	0424	0425	0426	0427 0435	0428 0436	0429 0437	0430 0438	0431 0439	1	
0260 0270	0176 0184	0177 0185	0178 0186	0179 0187	0180 0188	0181 0189	0182 0190	0183 0191	0660	0432 0440	0433 0441	0434 0442	0435	0436 0444	0437	0438	0439 0447		
0300	0192	0193	0194	0195	0196	0197	0198	0199	0700	0448	0449	0450	0451	0452	0453	0454	0455		
0310	0200	0201	0202	0203	0204	0205	0206	0207	0710	0456	0457	0458	0459	0460	0461	0462	0463		
0320 0330	0208 0216	0209 0217	0210 0218	0211 0219	0212 0220	0213 0221	0214 0222	0215 0223	0720	0464 0472	0465 0473	0466 0474	0467 0475	0468 0476	0469 0477	0470 0478	0471 0479	-	
0340	0210	0225	0226	0213	0228	0229	0230	0231	0740	0480	0481	0482	0483	0484	0485	0486	0487		
0350	0232	0233	0234	0235	0236	0237	0238	0239	0750	0488	0489	0490	0491	0492	0493	0494	0495		
0360	0240	0241						00.17			0407	0100							
0370	0248	0249	0242 0250	0243 0251	0244 0252	0245 0253	0246 0254	0247 0255	0760 0770	0496 0504	0497 0505	0498 0506	0499 0507	0500 0508	0501 0509	0502 0510	0503 0511		
03/0	0248 0								0760	0496]	
1000	0 0512	0249 1 0513	0250 2 0514	0251 3 0515	0252 4 0516	0253 5 0517	0254 6 0518	0255 7 0519	0760 0770 1400	0496 0504 0 0 0768	0505 1 0769	0506 Ż 0770	0507 3 0771	0508 4 0772	0509 5 0773	0510 6 0774	0511 7 0775	1000	0512
	0	0249 1	0250 2	0251 3	0252 4	0253 5	0254 6	0255 7	0760 0770	0496 0504 0	0505 1	0506 Ż	0507 3	0508 4	0509 5	0510 6	0511 7	to	to
1000 1010 1020 1030	0 0512 0520 0528 0536	0249 1 0513 0521 0529 0537	0250 2 0514 0522 0530 0538	0251 3 0515 0523 0531 0539	0252 4 0516 0524 0532 0540	0253 5 0517 0525 0533 0541	0254 6 0518 0526 0534 0542	0255 7 0519 0527 0535 0543	0760 0770 1400 1410 1420 1430	0496 0504 0 0 0 7 6 0 7 6 0 7 8 4 0 7 92	0505 1 0769 0777 0785 0793	0506 Ż 0770 0778 0786 0794	0507 3 0771 0779 0787 0795	0508 4 0772 0780 0788 0796	0509 5 0773 0781 0789 0797	0510 6 0774 0782 0790 0798	0511 7 0775 0783 0791 0799		to 1023
1000 1010 1020 1030 1040	0 0512 0520 0528 0536 0544	0249 1 0513 0521 0529 0537 0545	0250 2 0514 0522 0530 0538 0546	0251 3 0515 0523 0531 0539 0547	0252 4 0516 0524 0532 0540 0548	0253 5 0517 0525 0533 0541 0549	0254 6 0518 0526 0534 0542 0550	0255 7 0519 0527 0535 0543 0551	0760 0770 1400 1410 1420 1430 1440	0496 0504 0 0 7 6 0 7 6 0 7 8 0 7 8 0 7 9 2 0 800	0505 1 0769 0777 0785 0793 0801	0506 Ż 0770 0778 0786 0794 0802	0507 3 0771 0779 0787 0795 0803	0508 4 0772 0780 0788 0796 0804	0509 5 0773 0781 0789 0797 0805	0510 6 0774 0782 0790 0798 0806	0511 7 0775 0783 0791 0799 0807	to 1777	to 1023
1000 1010 1020 1030 1040 1050 1060	0 0512 0520 0528 0536 0544 0552 0560	0249 1 0513 0521 0529 0537 0545 0553 0561	0250 2 0514 0522 0530 0538 0546 0554 0562	0251 3 0515 0523 0531 0539 0547 0555 0563	0252 4 0516 0524 0532 0540 0548 0556 0564	0253 5 0517 0525 0533 0541 0549 0557 0565	0254 6 0518 0526 0534 0542 0550 0558 0566	0255 7 0519 0527 0535 0543 0551 0559 0567	0760 0770 1400 1410 1420 1430 1440 1450 1460	0496 0504 0 0768 0776 0784 0792 0800 0808 0816	0505 1 0769 0777 0785 0793 0801 0809 0817	0506 Ż 0770 0778 0786 0794 0802 0810 0818	0507 3 0771 0779 0787 0795 0803 0811 0819	0508 4 0772 0780 0788 0796 0804 0812 0820	0509 5 0773 0781 0789 0797 0805 0813 0821	0510 6 0774 0782 0790 0798 0806 0814 0822	0511 7 0775 0783 0791 0799 0807 0815 0823	to 1777	to 1023
1000 1010 1020 1030 1040 1050	0 0512 0520 0528 0536 0544 0552	0249 1 0513 0521 0529 0537 0545 0553	0250 2 0514 0522 0530 0538 0546 0554	0251 3 0515 0523 0531 0539 0547 0555	0252 4 0516 0524 0532 0540 0548 0556	0253 5 0517 0525 0533 0541 0549 0557	0254 6 0518 0526 0534 0542 0550 0558	0255 7 0519 0527 0535 0543 0551 0559	0760 0770 1400 1410 1420 1430 1440 1450	0496 0504 0 0768 0776 0784 0792 0800 0808	0505 1 0769 0777 0785 0793 0801 0809	0506 Ż 0770 0778 0786 0794 0802 0810	0507 3 0771 0779 0787 0795 0803 0811	0508 4 0772 0780 0788 0796 0804 0812	0509 5 0773 0781 0789 0797 0805 0813	0510 6 0774 0782 0790 0798 0806 0814	0511 7 0775 0783 0791 0799 0807 0815	to 1777	to 1023
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to to 3777 2047	3000 3010 3020 3030 3040 3060 3070 3100 3110 3130 3140 3150 3120 3220 3220 3220 3220 3220 3220 3220 3220 3220 3220 3220 3220 3230 3220 3230 3230 3230 3310 3330	1272 0 1536 1544 1552 1560 1568 1576 1584 1576 1584 1592 1600 1608 1616 1624 1632 1648 1656 1648 1656 1664 1672 1712 1720 1772 1728 1738 1752 1752 1755 1757 175	1273 1 1537 1545 1553 1561 1569 1577 1585 1593 1601 1625 1633 1641 1625 1633 1641 1649 1657 1649 1657 1649 1657 1775 1775 1775 1755 1777 1755 1777 1755 1777 1755 1777 1755 1777 1755 1777 1755 1777 1755 1777 1755 1777 1775 1777 1755 1777 1755 1777 1775 1775 175	1274 2 1538 1546 1552 1570 1578 1586 1594 1602 1610 1618 1626 1634 1642 1650 1658 1666 1674 1659 1659 1659 1659 1659 1659 1659 1657 1714 1722 1730 1738 1754	1275 3 1539 1547 1563 1571 1563 1571 1587 1595 1603 1611 1619 1627 1635 1643 1659 1665 1659 1667 1659 1667 1659 1663 1715 1715 1723 1707 1715 1723 1731 1739 1757	1276 4 1540 1548 1556 1564 1572 1588 1596 1604 1612 1628 1628 1628 1628 1628 1628 1628 1628 1628 1628 1628 1628 1628 1628 1644 1758 1628 1700 1718 1724 1732 1748 175	1277 5 1541 1549 1565 1573 1589 1589 1589 1589 1589 1589 1613 1629 1633 1641 1653 1661 1653 1661 1653 1661 1777 1775	1278 6 1542 1550 1558 1566 1574 1580 1598 1606 1614 1630 1638 1644 1654 1654 1654 1654 1654 1718 1778 1778	1271 1279 7 1543 1551 1559 1567 1575 1583 1591 1599 1607 1615 1623 1631 1623 1631 1647 1655 1663 1647 1655 1663 1647 1655 1663 1771 1779 1775 1743		2760 2770 3400 3410 3410 34320 3430 3440 3450 3450 3510 3550 3550 3550 3550 3550 3550 35	1528 0 1792 1800 1808 1816 1824 1842 1844 1848 1856 1844 1848 1856 1844 1849 1849 1944 1952 1968 1976 1984 1992 2008	1529 1793 1801 1809 1817 1825 1833 1841 1849 1857 1849 1857 1953 1905 1913 1921 1925 1969 1977 1985 1963 2009	1530 2 1794 1802 1810 1818 1826 1834 1842 1850 1858 1866 1874 1882 1890 1914 1906 1914 1922 1930 1938 1946 1970 1978 1946 1954 2012 2010	1531 3 1795 1803 1811 1819 1827 1835 1843 1851 1859 1867 1875 1883 1891 1891 1907 1915 1923 1939 1947 1955 1947 1955 2003 2011	4 1796 1804 1812 1820 1828 1844 1852 1860 1868 1864 1884 1852 1860 1868 1916 1908 1916 1924 1936 1948 1956 1956 1956 1957 1988	1533 5 1797 1805 1813 1821 1829 1837 1845 1845 1845 1845 1845 1845 1893 1901 1909 1917 1925 1933 1941 1949 1949 1947 1949 1949 1949 1949	1534 6 1798 1806 1814 1822 1830 1838 1846 1854 1862 1878 1846 1854 1862 1878 1910 1910 1918 1950 1958 1956 1958 195	7 1799 1807 1815 1823 1831 1839 1847 1855 1863 1871 1875 1863 1871 1879 1887 1895 1903 1911 1959 1959 1955 1959 1955 1959 1957 1959 1957 1975 1983 1991 1999 2007 2015
to to 3777 2047	3000 3010 3030 3040 3050 3060 3070 3100 3120 3130 3140 3150 3160 3170 3200 3210 3220 3220 3220 3240 3250 3270 3300 3310 3320 3320 3340	1272 0 1536 1544 1552 1560 1568 1576 1584 1577 1600 1608 1616 1624 1632 1643 1655 1644 1672 1688 1696 1712 1720 1728 1736 1744 1752 1744 1752 1756 1757 1756 1756 1757 1757 1757 1756 1756 1757 1757 1756 1756 1757 1756 1756 1757 1756 1756 1757 1756 1756 1756 1756 1756 1757 1756 175	1273 1 1537 1545 1553 1561 1569 1575 1585 1593 1601 1609 1617 1625 1633 1641 1649 1657 1649 1657 1649 1657 1713 1721 1729 1737 1745 1753 1754 1754 1753 1754 1753 1754 1755 1753 1755 1753 1649 1777 1745 1753 1754 1755 1753 1755 1757 1755 1757 1757 1755 1757 175	1274 2 1538 1546 1554 1562 1570 1578 1602 1610 1618 1626 1634 1642 1650 1658 1666 1674 1689 1690 1698 1704 1722 1730 1744 1758	1275 3 1539 1547 1555 1563 1571 1579 1603 1611 1619 1627 1635 1651 1659 1667 1659 1667 1659 1667 1659 1667 1715 1713 1773 1747 1755 1747 1755 1755 1755 1755 1755 1755 1755 1755 1755 1755 1755 1757 1755 1757 1755 1757 1773 1773 1773 1773 1773 1773 1773 1776 1775 1776 1775 1773 1773 1776 1775 1776 1775 1776 1775 177	1276 4 1540 1548 1556 1564 1554 1554 1554 1558 1558 1558 1558 155	1277 5 1541 1549 1565 1573 1581 1589 1597 1605 1613 1629 1629 1629 1633 1661 1669 1677 1645 1663 1661 1669 1677 1705 1773 1741 1749 1757	1278 6 1542 1550 1558 1556 1574 1580 1590 1598 1606 1614 1622 1630 1638 1646 1654 1662 1670 1678 1654 1702 1710 1718 1726	1271 1279 7 1543 1551 1559 1567 1575 1583 1591 1599 1607 1615 1623 1631 1655 1663 1647 1655 1663 1671 1679 1687 1703 1711 1779 1775 1743		2760 2770 3400 3410 3420 3430 3430 3440 3450 3450 3450 3550 355	1528 0 1792 1800 1808 1816 1824 1824 1840 1840 1840 1840 1840 1840 1844 1856 1864 1850 1880 1880 1880 1880 1994 1992 1950 1954 1956 1954 1956 1954 1956 1954 1956 1954 1956 1956 1957 1956 1957 1958	1529 1793 1801 1809 1817 1825 1833 1841 1849 1857 1865 1873 1867 1867 1867 1875 1875 1875 1973 1995 1945 1953 1969 1977 1985 1969 1977	1530 2 1794 1802 1810 1818 1826 1834 1842 1850 1858 1842 1852 1842 1842 1842 1842 1842 1842 1842 184	1531 1795 1803 1811 1819 1827 1843 1851 1843 1851 1843 1851 1843 1851 1843 1851 1843 1851 1843 1851 1947 1955 1963 1971 1979 1987 1995 2003 2011 2011	1532 4 1796 1804 1812 1820 1820 1828 1836 1860 1864 1884 1852 1860 1868 1916 1924 1932 1948 1916 1948 1956 1954 1956 1954 1956 1954 2004 2020	1533 5 1797 1805 1813 1821 1829 1837 1845 1853 1861 1845 1853 1867 1885 1893 1909 1917 1925 1933 1941 1949 1957 1957 1957 1952 2053 2013	1534 6 1798 1806 1814 1822 1830 1822 1830 1822 1822 1822 1822 1822 1822 1822 1822 1824 1846 1940 194	7 1799 1807 1823 1823 1831 1839 1847 1855 1863 1871 1875 1863 1871 1875 1887 1895 1903 1911 1959 1967 1975 1983 1991 1999 2007 2012
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OCTAL-DECIMAL INTEGER CONVERSION TABLE (Cont'd)

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4020 4030	2064	2065 2073	2066 2074	2067 2075	2068 2076	2069 2077	2070 2078	2071 2079	4420 4430	2320 2328	2321 2329	2322 2330	2323 2331	2324 2332	2325 2333	2326 2334	2327 2335	4777	2559
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40/0	2104	2105	2100	2107	2100	2103	2110	2111	44/0	2300	2301	2302	2303	2304	2303	2300	2307		Decimal - 4096
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4120	2128	2129 2137	2130 2138	2131 2139	2132 2140	2133 2141	2134 2142	2135 2143	4520 4530	2384 2392	2385 2393	2386 2394	2387 2395	2388 2396	2389 2397	2390 2398	2391 2399	40000	- 16384
4140	2144	2145	2146	2147	2148	2149	2150	2151	4540	2400	2401	2402	2403	2404	2405	2406	2407	50000	- 20480
4150	2152	2153	2154	2155	2156	2157	2158	2159	4550	2408	2409	2410	2411	2412	2413	2414	2415		- 24576
4160 4170	2160 2168	2161 2169	2162 2170	2163 2171	2164 2172	2165 2173	2166 2174	2167 2175	4560	2416	2417 2425	2418 2426	2419 2427	2420 2428	2421 2429	2422 2430	2423 2431	70000	- 28672
41/0	2100	2103	2170	21/1	2172	2173	21/4	21/5	45/0	2424	2420	2420	2421	2420	2423	2430	2431		
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4210	2184	2185	2186	2187	2188	2189	2190	2191	4610	2440	2441	2442	2443	2444	2445	2446	2447		
4220 4230	2192 2200	2193 2201	2194 2202	2195 2203	2196 2204	2197 2205	2198 2206	2199 2207	4620 4630	2448 2456	2449 2457	2450 2458	2451 2459	2452 2460	2453 2461	2454 2462	2455 2463		
4240	2208	2209	2210	2211	2212	2213	2214	2215	4640	2464	2465	2466	2467	2468	2469	2470	2471		
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42/0	2232	2233	2234	2233	2230	2231	2230	2235	40/0	2400	2403	2430	2431	2432	2433	2434	2733		
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											2545	2546	2547	2548	2549	2550	2551		
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			2290 2298	2291 2299	2292 2300	2293 2301	2302	2295 2303	4760	2544 2552	2553	2554	2555	2556	2557	2558	2559		
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OCTAL-DECIMAL INTEGER CONVERSION TABLE (Cont'd)

		0	1	2	3	4	5	6	7			0	1	2	3	4	5	6	7
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6000 3072	6000 6010	3072 3080	3073 3081	3074 3082	3075 3083	3076 3084	3077 3085	3078 3086	3079 3087		6400 6410	3328 3336	3329 3337	3330 3338	3331 3339	3332 3340	3333 3341	3334 3342	3335 3343
to to	6020	3088	3089	3090	3083	3092	3093	3094	3095		6420	3344	3345	3346	3347	3348	3349	3350	3351
6777 3583 (Octal) (Decimal)	5030	3096	3097	3098	3099	3100	3101	3102	3103		6430	3352	3353	3354	3355	3356	3357	3358	3359
(octai) (Decimal)	6040	3104	3105	3106	3107	3108	3109	3110	3111		6440	3360	3361	3362	3363	3364 3372	3365 3373	3366 3374	3367 3375
	6050 6060	3112 3120	3113 3121	3114 3122	3115 3123	3116 3124	3117 3125	3118 3126	3119 3127		6450 6460	3368 3376	3369 3377	3370 3378	3371 3379	3380	3381	3382	3383
Octal Decimal	6070	3128	3129	3130	3131	3132	3133	3134	3135		6470	3384	3385	3386	3387	3388	3389	3390	3391
10000 - 4096																•			
20000 - 8192	6100	3136 3144	3137 3145	3138 3146	3139 3147	3140 3148	3141 3149	3142 3150	3143 3151		6500 6510	3392 3400	3393 3401	3394 3402	3395 3403	3396 3404	3397 3405	3398 3406	3399 3407
30000 - 12288	6110 6120	3144	3145	3154	3155	3140	3145	3158	3159		6520	3408	3409	3410	3411	3412	3413	3414	3415
40000 - 16384	6130	3160	3161	3162	3163	3164	3165	3166	3167		6530	3416	3417	3418	3419	3420	3421	3422	3423
50000 - 20480 60000 - 24576	6140	3168	3169	3170	3171	3172	3173	3174	3175		6540	3424	3425	3426	3427	3428	3429	3430	3431
70000 - 28672	6150 6160	3176 3184	3177 3185	3178 3186	3179 3187	3180 3188	3181 3189	3182 3190	3183 3191		6550 6560	3432 3440	3433 3441	3434 3442	3435 3443	3436 3444	3437 3445	3438 3446	3439 3447
10000 20072	6170	3192	3193	3194	3195	3196	3197	3198	3199		6570	3448	3449	3450	3451	3452	3453	3454	3455
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	6230	3224	3225	3226	3227	3228	3229	3230	3231		6630	3480	3481	3482	3483	3484	3485	3486	3487
	6240	3232	3233	3234	3235	3236	3237	3238	3239		6640	3488	3489	3490	3491	3492	3493	3494	3495
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	6270	3246	3249	3250	3259	3260	3261	3262	3263		6670	3512	3505	3506	3515	3516	3509	3510	3519
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	6320	3280	3281	3282	3283	3284	3285	3286	3287		6720	3536	3529	3530	3539	3532	3533	3534	3543
	6330	3288	3289	3290	3291	3292	3293	3294	3295		6730	3544	3545	3546	3547	3548	3549	3550	3551
	6340	3296	3297	3298	3299	3300	3301	3302	3303		6740	3552	3553	3554	3555	3556	3557	3558	3559
	6350	3304	3305	3306	3307	3308 3316	3309 3317	3310	3311	1	6750	3560	3561	3562	3563	3564	3565 3573	3566 3574	3567 3575
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to to 7777 4095	6370 7000 7010 7020 7040 7050 7070 7100 7110 7120 7110 7120 7140 7150 7140 7170 7120 7210 7220 7220 7220 7240 7250 7240 7250 7270 7230	3320 0 3584 3592 3600 3608 3616 3624 3648 3656 3664 3656 3664 3656 3664 3656 3664 3656 3664 3656 3664 3656 3664 3657 3660 3664 3704 3712 3720 3726 3736 3744 3752 3768 3768 3768 3768 3768 3768 3768 3776 3768 3768 3768 3768 3768 3768 3768 3776 377	3321 1 3585 3593 3601 3609 3617 3625 3633 3641 3649 3657 3665 3665 3773 3725 3737 3745 3737 3745 3769 3776	3322 2 3586 3594 3602 3610 3618 3626 3634 3642 3650 3658 3666 3658 3706 3714 3722 3730 3738 3746 3774 3778	3323 3587 3595 3603 3611 3659 3707 3715 3723 3731 3737 3747 3755 3747 3775 3747 3775 37779 3777 37779 37777 37779 37779 37777 37779 37779 37777 37779 37777 37777 37779 37777 37777 37777 37777 37777 37777 37777 37777 37777 37777 37777 37777 37777 37777 377777 37777 37777 37777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 3777777 377777 377777 377777 377777 377777 377777 377777 377777 377777 377777 3777777 377777 377777 377777 377777 377777777	3324 4 3588 3496 3604 3620 3620 3620 3660 3663 3664 3652 3700 3716 3724 3732 3740 3748 3756 3765 3766 3748	3325 5 3589 3605 3613 3621 3629 3637 3645 3653 3645 3663 3701 3709 3717 3725 3733 3741 3749 3757 3765 3733 3741 3749 3757 3765 3733 3773	3326 6 3590 3598 3606 3614 3622 3630 3638 3645 3654 3654 3652 3670 3678 3686 3694 3702 3710 3718 3726 3750 3758 3756 3758 3758 3758	3327 7 3591 3599 3607 3615 3623 3631 3647 3655 3663 3667 3663 3667 3663 3667 3703 3711 3719 3727 3735 3743 3751 3759 3767 3775 37783 37791		6760 6770 7400 7410 7420 7430 7440 7450 7540 7550 7550 7550 7550 755	3576 0 3840 3848 3856 3864 3864 3872 3880 3872 3880 3994 3912 3928 3936 3936 3936 3952 3960 3968 3976 3984 4000 4008 4016 4024	3577 1 3841 3849 3857 3865 3873 3887 3987 3987 3993 3995 3993 3995 3993 3995 3993 3995 3993 3995 3993 4001 4002 4017 4023 4041	2 38578 2 38568 38666 38666 38674 38588 38906 3914 39303 39348 39303 39348 39362 39370 39388 39454 39524 39578 39545 4012 40140 40184 40242	3579 3843 3851 3859 3867 38853 3875 3883 3899 3907 3915 3923 3931 3931 3933 3931 3945 3963 3963 3963 3963 3963 3967 3965 4003 4011 4019 4027 4035	3586 4 3844 3852 3860 3868 3876 3884 3892 3990 39916 39916 3992 39908 39916 3932 3932 3932 3954 3954 3954 3954 40324 4028 40364 4044	3581 5 3845 3853 3861 3867 3883 3890 3907 3909 3917 3925 3933 3933 3934 3941 3945 3945 3945 3945 3945 3945 3945 3945	3582 6 3846 3854 3862 3878 38894 3902 3910 3918 3924 39342 3958 39598 4038	3583 7 3847 3855 3863 3871 3879 3887 3893 3903 3911 3919 3927 3935 3943 3951 3955 3943 3957 3943 3957 3983 3999 4007 4015 4023 4031
to to 7777 4095	6370 7000 7010 7020 7030 7040 7050 7050 7050 7100 7110 7120 7130 7130 7140 7150 7150 7160 7170 7200 7210 7220 7230 7250 7250 7250 7250 7250 7250 7250 725	3320 0 3584 3592 3600 3608 3616 3624 3632 3648 3656 3664 3656 3664 3678 3656 3656 3656 3696 3704 3712 3720 3728 3752 3760 3758 3752 3768 3752 3768 3776	3321 1 3585 3693 3601 3609 3617 3625 3633 3641 3649 3647 3665 3665 3663 3667 3705 3705 3705 3713 3721 3729 3737 3745 3745 3769 3778 3778	2 3586 3594 3602 3610 3618 3626 3634 3642 3658 3666 3658 3666 3668 3658 3666 3674 3659 3704 3770 3778 3770 3778 3786	3323 3587 3595 3603 3611 36595 3663 3659 3663 3659 3663 3659 3663 3659 3669 3707 3707 3723 3723 3731 3747 3775 3763 3771 3779 3795	3324 4 3588 3696 3604 3612 3620 3660 3668 3664 3662 3660 3666 3666 3666 3676 3700 3708 3716 3724 3732 3748 3756 3764 3778	3325 5 3589 3697 3605 3613 3621 3623 3621 3663 3661 3663 3663	3326 6 3590 3614 3622 3630 3638 3646 3652 3652 3652 3652 3652 3652 3652 365	3327 7 3591 3693 3607 3615 3623 3633 3643 3663 36647 3665 3663 36647 3665 3703 3711 3719 3727 3775 3767 3775 3767 3775		6760 6770 7400 7410 7420 7440 7450 7440 7550 7540 7550 7550 755	3576 0 3840 3848 3856 3864 3856 3864 3872 3880 3972 3920 3923 3944 3952 3936 3976 3984 39976 3984 4010 4008 4000 4008 4024	3577 1 3841 3849 3857 3865 3873 3887 3887 3887 3887 3887 3905 3913 3921 3921 3923 3937 3945 3953 3965 3953 3964 4053 4001 4009 4017 4025 4041 4049	2 38842 3850 3858 3866 3858 3864 3850 3858 3860 3898 3914 3922 3930 3954 3954 3954 3954 3954 3954 3954 4002 4018 4002 4018 4026	3579 3843 3851 3859 3867 3885 3885 3885 3885 3885 3885 3987 3997 3997 3997 3997 3997 3993 3931 3933 3931 3939 3947 3955 3963 3979 3987 3997 3997 4003 4001 4019 40027 4003	35860 4 3844 3852 3860 3868 3868 3876 3884 3892 3900 3908 3916 3924 3932 3930 39348 39364 39340 39348 39364 39340 4024 4022 4028 4024	3581 5 3845 3863 3863 3863 3867 3885 3893 3901 3917 3925 3933 3941 3949 3957 3943 3949 3957 3949 3957 3965 3973 3989 3999 3997 39777 3977 3977 3977 3977 3977 3977 3977 3977 3977 39	3582 6 3846 3854 3854 3854 3878 3878 3894 3910 39342 39350 3956 3942 3956 3942 3956 3942 3990 3988 3982 3996 3994 4014 4014 4014 4030 4046 4054 4054	3583 7 3847 3855 3863 3873 3873 3893 3893 3903 3911 3939 3927 3935 3943 3951 3959 3943 3951 3959 3943 3959 3943 3991 3999 4007 4015 4023 4031
to to 7777 4095	6370 7000 7010 7020 7030 7040 7050 7060 7070 7100 7120 7130 7150 7160 7170 7200 7230 7240 7250 7260 7270 7300 7310 7330	3320 0 3584 3592 3600 3608 3616 3616 3616 3624 3632 3640 3644 3656 3664 3656 3664 3668 3668 3704 3712 3728 3736 3776 3776 3776 3776	3321 1 3585 3693 3601 3609 3617 3625 3633 3641 3645 3665 3665 3665 3665 3665 3665 3769 3775 3775 3753 3769 3777 3785 3793 3801	2 3586 5594 3602 3610 3618 3626 3634 3642 3658 3658 3658 3658 3658 3658 3706 3714 3720 3730 3738 3754 3784 3784 3784 3784	3323 3587 3585 3603 3611 3627 3659 3643 3659 3667 3659 3667 3659 3667 3659 3707 3715 3739 3731 3739 3747 3753 3753 3763 3771 3779 3787	3324 4 3588 3496 3604 3612 3628 3668 3664 36668 3664 36692 3700 3708 3778 37780 37740 37780 37780 37780 3780	3325 5 3589 3605 3613 3621 3629 3637 3645 3661 3669 3669 3669 3677 3709 3717 3725 3733 3741 3733 3741 3757 3775 3775 3775 3775	3326 6 3590 3698 3606 3614 3630 3638 3646 3652 3638 3646 3652 3662 3670 3678 3662 3770 3778 3728 3734 3734 3758 3774 3790 3798 37990	3327 7 3591 3699 3615 3623 3663 3663 3663 36647 3665 3663 36647 36679 36679 3667 3703 3711 3719 3727 3735 3743 3735 3743 3759 3759 3759 3759 3759 3759 3759 375		6760 6770 7410 7420 7430 7430 7440 7430 7440 7450 7540 7550 7550 7550 7550 755	3576 0 3840 3848 3856 3864 3856 3864 3872 3880 3888 3896 3912 3920 3928 3936 3928 3934 3952 3944 3952 3960 3954 3954 4008 4006 4006 4002 4008 4008 4006	3577 1 3841 3849 3857 3865 3873 3873 3873 3873 3873 3873 3987 39913 3921 3929 3937 3945 3953 3945 3953 3945 3953 3945 3953 3945 3953 3945 3957 4009 4017 4025 4033 4049 4057	2 3842 3850 3850 3858 3866 3874 3882 3890 3898 3914 3922 3930 39346 3954 3954 3954 3954 3954 3954 4012 4018 4010 4018 4026	3579 3843 3851 3859 3867 3875 3875 3875 3875 3875 3873 3893 3997 3915 3931 3939 3947 3955 3963 3947 3955 3967 3957 4003 3987 4011 4019 4027 4035 4051 4051	35860 4 3844 3852 3860 3868 3860 3868 3867 3884 3892 3900 3908 3916 3916 3914 3932 3948 3948 3948 3956 3948 3956 4002 4028 4026 4028 4036 40452 4060	3581 5 3845 3853 3861 3863 3863 3885 3893 3901 3917 3917 3925 3933 3949 3957 3949 3957 3949 3957 3949 3959 3949 4013 4021 4021 4021 4023 4037	3582 6 3846 3854 3854 3854 3878 3886 3894 3902 3918 3918 3950 3954 3950 3958 3950 3954 3950 3956 3950 3996 4003 4014 4022 4030 4038 40454 4062 4062	3583 7 3847 3855 3863 3871 3879 3887 3893 3903 3919 3927 3945 3945 3945 3945 3945 3951 3951 3951 3951 3951 3951 3951 395
to to 7777 4095	6370 7000 7010 7020 7040 7050 7070 7100 7110 7120 7110 7120 7140 7170 7140 7170 7100 7140 7170 7100 710	3320 0 3584 3592 3600 3608 3616 3624 3648 3656 3664 3656 3664 3656 3664 3656 3664 3656 3664 3656 3664 3656 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3657 3660 3664 3672 3704 3712 3720 3726 3744 3752 3768 3776 3776 3778 3776 3778 3776 3778 3704 3778 3768 3776 3778 3778 3768 3778 3768 3778 3768 3778 3768 3778 3768 3778 3768 3778 3778 3778 3768 3778 3768 3778 3778 3778 3778 3768 3778 3778 3778 3778 3778 3788 3778 3788 3778 3788 3808 3808 3808 3788 3808 3788 3808 3788 3788 3788 3808 3788 3788 3788 3788 3808 3788 3788 3808 3788 3788 3788 3808 37888 3788 3788 3788 3788 3788 3788 3788 3788 3788 37	3321 1 3585 3593 3601 3609 3617 3625 3633 3641 3649 36457 3665 36657 3765 3713 3721 3729 3737 3745 3769 3777 3785 3793 3809	3322 2 3586 3594 3602 3610 3618 3626 3634 3642 3658 3666 3658 3666 3658 3666 3658 3766 3714 3722 3730 3738 3746 3774 3778 3778 3778 3778	3323 3587 3595 3603 3611 3619 3627 3643 3651 3667 3667 3663 3669 3707 3715 3723 3731 3739 3747 3755 3763 3771 3779 3787 3795 3803 3811	3324 4 3588 3496 3604 3620 3620 3620 3660 3663 3664 3652 3700 3708 3716 3724 3732 3740 3748 3756 3768 3768 3768 3768 3768 3772 3780 3804	3325 5 3589 3605 3613 3621 3629 3637 3645 3653 3645 3653 3661 3669 3677 3685 3693 3701 3709 3717 3725 3733 3741 3749 3757 3745 3749 3757 3745 3749 3757 3745 3749 3773 3757 3765 3773 3773 3773 3773 3773	3326 6 3590 3598 3606 3614 3652 3630 3638 3654 3654 3662 3670 3686 3694 3702 3738 3710 3718 3726 3750 3758 3756 3758 3758 3758 3758 3758 3774 3790 3798	3327 7 3591 3693 3607 3615 3623 3633 3643 3663 36647 3665 3663 36647 3665 3703 3711 3719 3727 3775 3767 3775 3767 3775		6760 6770 7400 7410 7420 7440 7450 7440 7550 7540 7550 7550 755	3576 0 3840 3848 3856 3864 3856 3864 3872 3880 3972 3920 3923 3944 3952 3936 3976 3984 39976 3984 4010 4008 4000 4008 4024	3577 1 3841 3849 3857 3865 3873 3887 3887 3887 3887 3887 3905 3913 3921 3921 3923 3937 3945 3953 3965 3953 3964 4053 4001 4009 4017 4025 4041 4049	2 38842 3850 3858 3866 3858 3864 3850 3858 3860 3898 3914 3922 3930 3954 3954 3954 3954 3954 3954 3954 4002 4018 4002 4018 4026	3579 3843 3851 3859 3867 3885 3885 3885 3885 3885 3885 3987 3997 3997 3997 3997 3997 3993 3931 3933 3931 3939 3947 3955 3963 3979 3987 3997 3997 4003 4001 4019 40027 4003	35860 4 3844 3852 3860 3868 3868 3876 3884 3892 3900 3908 3916 3924 3932 3930 39348 39364 39340 39348 39364 39340 4024 4022 4028 4024	3581 5 3845 3863 3863 3863 3867 3885 3893 3901 3917 3925 3933 3941 3949 3957 3943 3949 3957 3949 3957 3965 3973 3989 3997 3989 3997 3989 3999 3997 3989 3997 3989 3997 3989 3997 3989 3997 3989 3997 3989 3997 3989 3997 3989 3997 3989 3997 398	3582 6 3846 3854 3854 3854 3878 3878 3894 3910 39342 39350 3956 3942 3956 3942 3956 3942 3990 3988 3982 3996 3994 4014 4014 4014 4030 4046 4054 4054	3583 7 3847 3855 3863 3873 3873 3893 3893 3903 3911 3939 3927 3935 3943 3951 3959 3943 3951 3959 3943 3959 3943 3991 3999 4007 4015 4023 4031
to to 7777 4095	6370 7000 7010 7020 7030 7040 7050 7060 7070 7100 7120 7130 7150 7160 7170 7200 7230 7240 7250 7260 7270 7300 7310 7330	3320 0 3584 3592 3600 3608 3616 3616 3616 3624 3632 3640 3644 3656 3664 3656 3664 3668 3668 3704 3712 3728 3736 3776 3776 3776 3776	3321 1 3585 3693 3601 3609 3617 3625 3633 3641 3645 3665 3665 3665 3665 3665 3665 3769 3775 3775 3753 3769 3777 3785 3793 3801	2 3586 5594 3602 3610 3618 3626 3634 3642 3658 3658 3658 3658 3658 3658 3706 3714 3720 3730 3738 3754 3784 3784 3784 3784	3323 3587 3585 3695 3695 3695 3693 3611 3627 3659 3659 3667 3659 3667 3659 3707 3715 3739 3731 3739 3747 3753 3753 3779 3787	3324 4 3588 3496 3604 3612 3628 3668 3664 36668 3664 36692 3700 3708 3778 37780 37740 37780 37780 37780 3780	3325 5 3589 3605 3613 3621 3629 3637 3645 3661 3669 3669 3669 3677 3709 3717 3725 3733 3741 3733 3741 3757 3775 3775 3775 3775	3326 6 3590 3698 3606 3614 3630 3638 3646 3652 3638 3646 3652 3662 3670 3678 3662 3770 3778 3728 3734 3734 3758 3774 3790 3798 37990	3327 7 3591 3599 3607 3615 3623 3631 3633 3647 3647 3647 3647 3647 3703 3711 3719 3727 3735 3743 3751 3759 3767 3775 3775 3775 3775 3775 3775		6760 6770 7400 7410 7420 7430 7440 7450 7540 7550 7550 7550 7550 755	3576 0 3840 3848 3856 3864 3864 3864 3872 3880 3978 3994 3992 3928 3936 3936 3936 3952 3960 3952 3960 3976 3984 4016 4024 4040 4042 4042	3577 1 3841 3849 3857 3865 3873 3887 3987 3987 3987 3987 3993 3995 3993 3995 3993 3995 3993 3995 3993 3995 3993 3995 3995 3995 3995 3995 3995 3995 3995 4001 4005 400	2 38578 2 38578 38560 38586 38660 38574 38820 38940 39944 39300 39383 39345 39303 39345 39362 39370 39378 39362 39970 39378 39364 40012 4018 40026 40050 40050 40050	3579 3843 3851 3859 3867 38853 3897 3915 3923 3931 3931 3931 3933 3939 3947 3955 3963 3963 3963 3963 3963 3964 4011 4019 4027 4035 4027	3586 4 3844 3852 3860 3868 3876 3884 3892 3990 39916 39916 3992 3990 39918 3932 3932 3932 3954 3954 3954 3954 3954 4032 4002 4002 4028 4036 4044 4058 4068	3581 5 3845 3863 3861 3869 3877 3885 3893 3901 3909 3917 3925 3933 3931 3941 3945 3947 3945 3945 3947 3945 3947 3945 3947 3945 3947 3945 3947 3945 3947 3945 4015 4012 4024 4053 4065 40555 40555 40555 405555 405555 4055555555 405555555555	3582 6 3846 3854 3862 3878 3878 3894 3902 3910 3918 3926 39342 3958 3998 40140 4052 4070	3583 7 3847 3855 3863 3871 3879 3887 3903 3911 3919 3927 3935 3943 3951 3955 3943 3957 3943 3957 3957 3957 3957 3967 3975 3983 3991 4007 4015 4023 4031 4039 4047

APPENDIX V

OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	106	.136718		.261718		
				.206		.306	.386718
.007	013671	.107	138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	152343	.216	.277343	.316	.402343
.017	.029296	.117	154296	.217	279296	.317	404296
.020	.031250	120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.021	.035156						
		.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	294921	.327	.419921
.030	.046875	.130	.171875	.230	296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.133	.179687				
.034	.056640			.234	.304687	.334	.429687
		.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	146	.199218	.246	324218	.346	.449218
.047	.076171	.140	.201171	.240	.326171	.340	.451171
.050	.078125	150	202125	250	220125]	
.050	.080078	.150	.203125	.250	.328125	.350	.453125
		.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
:054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703				400/00
.061	.097656			.261	.345703	361	.470703
		.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	171	.236328	.270	.361328	.371	.486328
.072	.113281						
		.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
076	.121093	.176	.246093	.276	.371093	.376	.496093
.076 .077	123046						

OCTAL-DECIMAL FRACTION CONVERSION TABLE (Cont'd)

.000000 .000100 .000244 .000200 .000488 .000300 .000011 .00007 .000101 .000251 .000492 .000301 .000003 .000111 .000125 .000255 .000203 .000499 .000303 .000005 .00015 .000164 .000255 .000265 .000507 .000304 .000006 .000015 .000166 .000265 .000507 .000306 .000007 .000166 .000270 .000270 .000514 .000307 .000011 .000274 .000210 .000518 .000310 .000111 .000282 .000211 .000526 .000311 .000112 .000281 .000112 .000282 .000211 .000526 .000313 .00014 .000113 .000283 .000214 .000534 .000313 .000313 .000313 .000313 .000313 .000313 .000313 .000313 .000314 .000313 .000313 .000314 .000313 .000313 .0003	000732 000736 000740 000743 000751 000755 000759 000762 000766 000770 000774 000778 000785 000785 000789 000793 000793
000001 000003 000101 000247 000201 000492 000301 000003 000011 000103 000255 000202 000499 000303 000004 000015 000104 000259 000204 00053 000305 000005 000022 000106 000267 000206 000511 000306 000010 000022 000107 00027 000210 000514 000306 000011 000034 000111 000274 000210 000528 000311 000012 000034 000111 000278 000211 000528 000311 000012 000038 000114 000288 000214 000534 000313 000015 000045 000114 000293 000216 000531 000314 000015 000049 000115 000220 000545 000317 000016 000057 000117 000305 000220 000544 000320	000736 000740 000743 000751 000755 000759 000762 000766 000770 000774 000778 000782 000785 000789 000793
000002 000007 000102 000251 000202 000495 000302 000004 000015 000103 000255 000204 000503 000303 000005 000019 000105 000263 000205 000511 000305 000007 000022 000107 000270 000207 000514 000307 000010 000034 000111 000274 000210 000512 000311 000011 000034 000111 000274 000211 000526 000312 000012 000038 0001112 000282 000212 000526 000313 000014 000045 000115 000297 000216 000534 000314 000015 000057 000116 000227 000216 000545 000312 000020 000064 000120 000305 000220 000545 000322 000021 000064 000120 000305 000220 000566 000322 </td <td>000740 000743 000747 000755 000755 000762 000766 000770 000774 000774 000778 000782 000785 000789</td>	000740 000743 000747 000755 000755 000762 000766 000770 000774 000774 000778 000782 000785 000789
000003 000011 000103 000255 000204 000499 000303 000004 000015 000104 000259 000204 000577 000305 000006 000022 000106 000267 000207 000511 000306 000010 000022 000107 000277 000207 000514 000310 000011 000034 000111 000278 000211 000526 000311 000012 000034 000111 000278 000212 000526 000313 000015 000045 000114 000286 000212 000530 000313 000015 000045 000115 000293 000216 000541 000315 000017 000057 000117 000305 000217 000545 000317 000020 000661 000120 000305 000221 000553 000321 000021 000066 000122 000316 000221 000556 0003221 </td <td>000743 000747 000751 000755 000762 000766 000770 000774 000778 000782 000785 000789 000793</td>	000743 000747 000751 000755 000762 000766 000770 000774 000778 000782 000785 000789 000793
000004 000015 000104 000259 000205 000503 000304 000005 000022 000106 000267 000205 000511 000306 000007 000026 000107 000270 000207 000514 000307 000010 000030 000110 000274 000210 000526 000311 000011 000034 000111 000278 000211 000522 000311 000012 000034 000113 000282 000213 000530 000313 000014 000044 000115 000297 000216 000541 000316 000017 000057 .000116 000220 000545 000317 000021 000064 .000120 000305 000220 000545 000321 000022 000064 .000120 000305 000221 000553 0003221 000020 000064 .000120 000326 000221 000564 000322 <t< td=""><td>000747 000751 000755 000759 000762 000766 000770 000774 000778 000785 000785 000789</td></t<>	000747 000751 000755 000759 000762 000766 000770 000774 000778 000785 000785 000789
000005 000019 000105 000263 000205 000305 000007 000022 001106 000270 000206 000207 000305 000011 000033 000110 000274 000210 000522 000311 000011 000034 000111 000278 000211 000522 000311 000012 000038 000113 000286 000214 000534 000313 000015 000045 000116 000293 000214 000534 000314 000017 000057 000117 000305 0002217 000545 000317 000017 000064 000120 000305 000221 000545 000321 000021 000064 000122 000316 000221 000545 000321 000023 000076 000124 000320 000224 000564 000323 000024 000076 000125 000326 000226 000572 000326	000751 000755 000759 000762 000766 000770 000774 000778 000782 000785 000789 000793
000006 000022 000106 000267 000206 000301 000007 000026 .000107 .000270 .000210 .000301 000011 000030 .000111 .000274 .000211 .000522 .000311 000012 000038 .000111 .000282 .000213 .000530 .000313 000014 .00014 .000114 .000293 .000215 .000334 .000314 000015 .000044 .000114 .000297 .000216 .000537 .000315 000016 .000057 .000117 .000305 .000210 .000544 .000316 .000021 .000664 .000122 .000325 .000221 .000560 .000322 .000022 .00068 .000124 .000324 .000225 .000564 .000322 .000023 .000076 .000126 .000324 .000227 .000566 .000323 .000026 .000080 .000127 .000331 .000227 .000568	000755 000759 000762 000766 000770 000774 000778 000782 000785 000789 000793
.000007 .00026 .000107 .000270 .000207 .000514 .000307 000010 000030 .000110 000274 .000210 .000518 .000310 000011 000038 .000111 .000278 .000212 .000526 .000312 .000012 .00038 .000113 .000286 .000214 .000534 .000314 .000015 .000049 .000116 .000293 .000216 .000541 .000316 .000017 .000057 .000116 .000227 .000216 .000545 .000317 .000020 .000661 .000120 .000305 .000221 .000553 .000321 .000021 .000664 .000121 .0003216 .000221 .000556 .000322 .000022 .000068 .000123 .000324 .000225 .000366 .000324 .000027 .000087 .000126 .000324 .000225 .000366 .000323 .000026 .000087 .000127 .000331	000759 000762 000766 000770 000774 000782 000782 000785 000789 000793
000010 000330 000110 000274 000210 000518 000310 000011 000034 000111 000278 000211 000522 000311 000013 000041 000114 000282 000213 000530 000313 000014 000045 000114 000289 000214 000534 000315 000015 000053 000116 000297 000216 000541 000316 000020 000064 000120 000305 000217 000553 000317 000021 000064 000120 000308 000221 000556 000322 000023 000072 000124 000324 000225 000564 000324 000024 000076 000125 000324 000225 000564 000323 000027 000080 000127 000316 000227 000564 000324 000026 000081 000127 000331 000227 000577 000326 <td>.000762 .000766 .000770 .000774 .000782 .000785 .000789 .000793 .000797</td>	.000762 .000766 .000770 .000774 .000782 .000785 .000789 .000793 .000797
000011 000024 000111 000278 000211 000522 .000311 000012 000038 000112 000282 .000212 .00556 .000313 000014 .00044 .000114 .000286 .000213 .000534 .000314 000015 .00045 .000114 .000286 .000215 .000534 .000315 000016 .000057 .000116 .000293 .000216 .000541 .000316 .000017 .00057 .000117 .000305 .000220 .000549 .000317 .000020 .000064 .000121 .000308 .000221 .000321 .000321 .000021 .000064 .000121 .000308 .000222 .000566 .000322 .000024 .000076 .000124 .000320 .000225 .000568 .000325 .000025 .000083 .000126 .000324 .000227 .000579 .000326 .000027 .000831 .000331 .000233	.000766 .000770 .000774 .000782 .000782 .000785 .000789
000011 000024 000111 000278 000211 000522 .000311 000012 000038 000112 000282 .000212 .00556 .000313 000014 .00044 .000114 .000286 .000213 .000534 .000314 000015 .00045 .000114 .000286 .000215 .000534 .000315 000016 .000057 .000116 .000293 .000216 .000541 .000316 .000017 .00057 .000117 .000305 .000220 .000549 .000317 .000020 .000064 .000121 .000308 .000221 .000321 .000321 .000021 .000064 .000121 .000308 .000222 .000566 .000322 .000024 .000076 .000124 .000320 .000225 .000568 .000325 .000025 .000083 .000126 .000324 .000227 .000579 .000326 .000027 .000831 .000331 .000233	.000766 .000770 .000774 .000782 .000782 .000785 .000789
000012 000038 000112 000282 000212 000526 000312 000014 000045 000114 000289 000214 000530 000313 000015 000049 000115 000293 000216 000537 000315 000017 000057 000117 000305 000217 000545 000317 000020 000064 000121 000305 000220 000545 000320 000021 000064 000121 000308 000221 000553 000322 000022 000068 000122 000316 000223 000566 000322 000024 000076 000125 000324 000225 000568 000322 000025 000080 000127 000318 000226 000568 000322 000026 000083 000127 000318 000226 000566 000327 000027 00087 000127 000331 000230 000576 000331 <td>.000770 .000774 .000778 .000782 .000785 .000789 .000793 .000797</td>	.000770 .000774 .000778 .000782 .000785 .000789 .000793 .000797
.000013 .000014 .000113 .000286 .000213 .000330 .000313 .000014 .000045 .000114 .000289 .000214 .000534 .000314 .000015 .000049 .000116 .000293 .000216 .000541 .000316 .000017 .000057 .000117 .000305 .000217 .000553 .000317 .000020 .000061 .000120 .000305 .000221 .000553 .000321 .000021 .000064 .000121 .000308 .000221 .000556 .000322 .000022 .000068 .000122 .000316 .000223 .000356 .000324 .000024 .000076 .000124 .000324 .000255 .000323 .000025 .000080 .00126 .000324 .00026 .000377 .000327 .000026 .000083 .000127 .000331 .000226 .000577 .000327 .000031 .000095 .000130 .000335 .000231 <td>.000774 .000778 .000782 .000785 .000789 .000793 .000797</td>	.000774 .000778 .000782 .000785 .000789 .000793 .000797
000014 000015 000014 000015 000013 000015 000013 000021 000013 000022 000013 000023 000013 000022 000064 0000132 000022 0000564 0000322 000022 000033 000022 000033 000023 000033 000023 000033 000023 000033 000033 000033 000033 000033 0000	.000778 .000782 .000785 .000789 .000793 .000797
000015 000049 000115 000293 000215 000537 000315 000017 000057 000116 000297 000216 000541 000316 000017 000057 000116 000301 000217 000545 000317 000020 000061 000120 000305 000221 000553 000321 000021 000068 000122 000316 000223 000560 000322 000024 000072 000125 000324 000226 000564 000324 000025 000080 000125 000324 000226 000572 000325 000027 000083 000126 000324 000226 000572 000327 000027 000087 000127 000318 000221 000576 000327 000030 000991 000130 000335 000230 000579 000330 000031 000995 000131 000347 000233 000587 000333 <td>.000782 .000785 .000789 .000793 .000797</td>	.000782 .000785 .000789 .000793 .000797
.000016 .000057 .000117 .000297 .000216 .000541 .000316 .000017 .000057 .000117 .000301 .000217 .000545 .000317 .000020 .000064 .000120 .000305 .000210 .000553 .000321 .000021 .000064 .000122 .000308 .000222 .000556 .0003221 .000023 .000072 .000123 .000316 .000223 .000564 .000322 .000024 .000076 .000124 .000320 .000225 .000564 .000324 .000027 .000083 .000126 .000328 .000227 .000572 .000326 .000027 .000087 .00127 .000331 .000227 .000579 .000327 .000030 .00091 .00130 .000335 .000231 .000587 .000331 .00033 .000102 .000133 .000343 .000234 .000587 .000333 .000034 .000105 .000134 .000354 <td>.000785 .000789 .000793 .000797</td>	.000785 .000789 .000793 .000797
.000017 .000057 .000117 .000301 .000217 .000545 .000317 .000020 .00064 .00120 .000305 .000220 .000549 .000320 .000021 .00064 .00121 .000308 .000221 .000556 .000322 .000023 .00072 .000123 .000316 .000223 .000564 .000323 .000026 .000080 .000125 .000324 .000564 .000325 .000026 .00083 .00126 .000328 .000276 .000326 .000027 .00087 .00127 .000331 .00027 .000578 .000327 .000030 .000911 .000335 .000231 .000583 .000331 .000231 .000331 .000331 .000332 .000332 .000331 .000331 .000331 .000333 .000333 .000333 .000333 .000333 .000333 .000334 .000335 .000333 .000333 .000334 .000335 .000334 .000335 .000334	.000789 .000793 .000797
000020 000061 000120 000305 000221 000549 000320 000021 000068 000121 000308 000221 000553 000321 000022 000068 000122 000316 000223 000560 000323 000024 000076 000125 000324 000225 000568 000324 000025 000083 000125 000328 000226 000572 000326 000027 000087 000127 000335 000226 000572 000326 000030 000991 000130 000335 000230 000579 000333 000032 000099 000132 000343 000232 000587 000332 000033 000102 000133 000347 000233 000591 000333 000034 000196 000134 000356 000234 000595 000334 000035 000114 000136 000354 000236 000602 000335 <td>.000793 .000797</td>	.000793 .000797
.000021 .000064 .000121 .000308 .000221 .000553 .000321 .000022 .000068 .000122 .000312 .000222 .000560 .000323 .000024 .000076 .000125 .000324 .00024 .000564 .000324 .000025 .000083 .000126 .000324 .000276 .000326 .000027 .000087 .000126 .000328 .000226 .000564 .000327 .000027 .000087 .000127 .000331 .000277 .000376 .000327 .000030 .000991 .000130 .000335 .000230 .000579 .000330 .000031 .000995 .000132 .000343 .000232 .000587 .000332 .000033 .000106 .000134 .000350 .000235 .000334 .000335 .000334 .000036 .000114 .000136 .000354 .000236 .000137 .000344 .000336 .000040 .000122 .000140 </td <td>.000797</td>	.000797
.000021 .000064 .000121 .000308 .000221 .000553 .000321 .000022 .000068 .000122 .000312 .000222 .000560 .000322 .000024 .000076 .000125 .000324 .000225 .000564 .000324 .000025 .000083 .000126 .000324 .000226 .000568 .000326 .000027 .000087 .000127 .000331 .000226 .000572 .000327 .000027 .000087 .000127 .000331 .000230 .000579 .000330 .000031 .000995 .000131 .000339 .000231 .000587 .000332 .000033 .000106 .000134 .000350 .000235 .000334 .000333 .000036 .000114 .000136 .000354 .000236 .000595 .000334 .000037 .000118 .000136 .000354 .000236 .00062 .000336 .000037 .000118 .000137 .000236 </td <td>.000797</td>	.000797
.000022 .000068 .000122 .000312 .000222 .000556 .000322 .000023 .00076 .000124 .000320 .000224 .000564 .000323 .000025 .00080 .000125 .000324 .000225 .000568 .000325 .000026 .00083 .000126 .000328 .000226 .000576 .000327 .000027 .00087 .000127 .000331 .000230 .000576 .000327 .000030 .00095 .000131 .000335 .000231 .000583 .000331 .000032 .000999 .000132 .000343 .000233 .000595 .000334 .000035 .000110 .000135 .000234 .000595 .000334 .000036 .000114 .000356 .000234 .000595 .000334 .000036 .000114 .000366 .000237 .000598 .000335 .000037 .000118 .000366 .000240 .000614 .000341	
.000023 .000072 .000123 .000316 .000223 .000560 .000323 .000024 .00076 .000124 .000320 .000224 .000564 .000325 .000025 .000080 .000125 .000324 .000226 .000572 .000325 .000027 .000087 .000127 .000331 .000227 .000576 .000327 .000030 .000991 .000130 .000335 .000230 .000579 .000330 .000031 .000995 .000131 .000339 .000233 .000587 .000332 .000033 .000102 .000133 .000350 .000234 .000595 .000333 .000034 .000166 .000135 .000354 .000237 .000598 .000335 .000037 .000110 .000136 .000366 .000237 .000602 .000336 .000036 .000114 .000358 .000237 .000598 .000337 .000040 .000122 .000140 .000366 .000240 </td <td>CREATER</td>	CREATER
.000024 .00076 .000124 .000320 .000224 .000564 .000324 .000025 .00080 .000125 .000324 .000225 .000568 .000325 .000026 .00083 .000127 .00031 .00027 .000576 .000327 .000030 .00091 .001127 .000331 .000231 .000576 .000331 .000031 .000991 .00132 .000343 .000231 .000583 .000331 .00033 .000102 .000133 .000347 .000233 .000595 .000334 .00034 .000106 .000135 .000354 .000236 .000595 .000334 .00035 .000110 .000136 .000358 .000237 .000598 .000335 .00036 .000114 .000136 .000358 .000237 .000606 .000337 .000037 .000118 .000137 .000362 .000237 .000606 .000337 .000040 .000122 .000141 .000366	.000805
.000025 .000080 .000125 .000324 .000225 .000568 .000325 .000026 .000083 .000126 .000328 .000226 .000572 .000326 .000027 .000087 .000127 .000331 .000227 .000576 .000327 .000030 .000991 .000130 .000335 .000230 .000579 .000330 .000031 .000995 .000131 .000339 .000231 .000587 .000332 .000033 .000102 .000133 .000343 .000233 .000591 .000333 .00034 .000166 .000134 .000356 .000236 .000602 .000336 .000035 .000114 .000358 .000236 .000602 .000337 .000040 .000122 .000140 .000366 .000241 .000610 .000341 .000041 .000125 .000141 .000370 .000241 .000614 .000341 .000042 .000129 .000142 .000377 .000243 </td <td>.000808</td>	.000808
.000026 .000083 .000126 .000328 .000226 .000572 .000326 .000027 .000087 .000127 .000331 .000227 .000576 .000327 .000030 .000991 .000130 .000335 .000230 .000579 .000330 .000032 .000995 .000131 .000339 .000232 .000587 .000332 .000033 .000102 .000132 .000343 .000232 .000587 .000332 .000034 .000106 .000134 .000350 .000234 .000595 .000334 .000035 .000110 .000135 .000354 .000236 .000602 .000336 .000036 .000114 .000137 .000362 .000237 .000606 .000337 .000037 .000118 .000137 .000366 .000240 .000610 .000340 .000040 .000122 .000140 .00366 .000240 .00617 .000342 .000041 .000129 .000142 .000377 <td></td>	
.000027 .000087 .000127 .000331 .000227 .000576 .000327 .000030 .000091 .000130 .000335 .000230 .000576 .000330 .000031 .00095 .00131 .000339 .000231 .000583 .000331 .000032 .00099 .00132 .000343 .000232 .000587 .000332 .000034 .000166 .000134 .000350 .000234 .000595 .000334 .000035 .000114 .000156 .000354 .000237 .000595 .000334 .000036 .000114 .000136 .000358 .000237 .000666 .000337 .000040 .000122 .000140 .000366 .000240 .000610 .000341 .000041 .000125 .000141 .000377 .000241 .000614 .000342 .000043 .000133 .000144 .000377 .000241 .000617 .000342 .000044 .000133 .000144 .000377	.000812
.000030 .00091 .000130 .00035 .000230 .000579 .000330 .000031 .00095 .000131 .000339 .000231 .000583 .000331 .000032 .00099 .000132 .000343 .000232 .000587 .000332 .000034 .000106 .000134 .000350 .000234 .000595 .000334 .000036 .000110 .000135 .000354 .000236 .000595 .000334 .000036 .000114 .000136 .000354 .000236 .000602 .000336 .000037 .000118 .000137 .000362 .000237 .000606 .000337 .000040 .000122 .000140 .000366 .000240 .000610 .000341 .000041 .000125 .000141 .000373 .000241 .000617 .000342 .00043 .000137 .000142 .000377 .000243 .000621 .000341 .000043 .000137 .000144 .000377	.000816
.000031 .000095 .000131 .000339 .000231 .000583 .000331 .000032 .000999 .000132 .000343 .000232 .000587 .000332 .000033 .000102 .000133 .000343 .000233 .000597 .000332 .000034 .000166 .000135 .000356 .000234 .000595 .000334 .000036 .000114 .000136 .000358 .000236 .000660 .000336 .000037 .000118 .000137 .000362 .000237 .000666 .000337 .000040 .000122 .000140 .000366 .000240 .000610 .000341 .000041 .000125 .000141 .000370 .000241 .000614 .000341 .00042 .000133 .000144 .000377 .000241 .000617 .000342 .00043 .000137 .000144 .000381 .000244 .000625 .000344 .00045 .000141 .000145 .000385 <td>.000820</td>	.000820
.000032 .000099 .000132 .000343 .000232 .000587 .000332 .000033 .000102 .000133 .000347 .000233 .000591 .000333 .000034 .000106 .000134 .000350 .000234 .000595 .000334 .000035 .000110 .000135 .000354 .000236 .000595 .000336 .000036 .000114 .000366 .000237 .000606 .000337 .000037 .000122 .000140 .000366 .000240 .000610 .000341 .000040 .000125 .000141 .000370 .000241 .000614 .000341 .000041 .000137 .000142 .000373 .000241 .000614 .000341 .000043 .000137 .000144 .000377 .000243 .000621 .000342 .000044 .000137 .000144 .000377 .000243 .000621 .000343 .000045 .000137 .000144 .000381 .000244<	.000823
.000032 .000099 .000132 .000343 .000232 .000587 .000332 .000033 .000102 .000133 .000347 .000233 .000591 .000333 .000034 .00016 .000134 .000350 .000234 .000595 .000334 .000035 .000114 .000356 .000236 .000598 .000335 .000037 .000118 .000137 .000362 .000237 .000666 .000337 .000040 .000122 .000140 .000366 .000240 .000610 .000341 .000041 .000125 .000141 .000370 .000241 .000614 .000341 .000042 .000129 .000142 .000377 .000241 .000614 .000343 .000043 .000137 .000144 .000377 .000241 .000617 .000343 .000043 .000137 .000144 .000377 .000243 .000625 .000344 .000044 .000137 .000144 .000385 .000244 </td <td>.000827</td>	.000827
.000033 .000102 .000133 .000347 .000233 .000591 .000333 .000034 .000106 .000134 .000350 .000234 .000595 .000334 .000035 .000110 .000135 .000356 .000235 .000598 .000335 .000036 .000114 .000136 .000358 .000236 .000602 .000336 .000037 .000118 .000137 .000366 .000240 .000610 .000341 .000040 .000122 .000140 .000366 .000240 .000610 .000341 .000041 .000125 .000141 .000377 .000242 .000617 .000342 .000043 .000137 .000144 .000381 .000244 .000625 .000344 .000044 .000137 .000145 .000385 .000244 .000625 .000344 .000045 .000141 .000385 .000244 .000625 .000344 .000046 .000144 .000146 .000385 .000246<	.000831
.000034 .000106 .000134 .000350 .000234 .000595 .000334 .000035 .000110 .000135 .000354 .000235 .000598 .000335 .000036 .000114 .000136 .000358 .000236 .000602 .000336 .000037 .000118 .000137 .000362 .000237 .000606 .000337 .000040 .000122 .000140 .000366 .000240 .000614 .000340 .000041 .000125 .000141 .000373 .000242 .000614 .000340 .000042 .000129 .000143 .000373 .000241 .000614 .000342 .000043 .000137 .000144 .000377 .000243 .000621 .000343 .000044 .000137 .000144 .000385 .000244 .000625 .000344 .000045 .000141 .000145 .000385 .000245 .000629 .000345 .000046 .000144 .000147 .000389<	.000835
.000035 .000110 .000135 .000354 .000235 .000598 .000335 .000036 .000114 .000136 .000358 .000236 .000602 .000336 .000037 .000118 .000137 .000362 .000237 .000606 .000337 .000040 .000122 .000140 .000366 .000240 .000610 .000340 .000041 .000125 .000141 .000370 .000241 .000614 .000342 .000043 .000133 .000144 .000377 .000243 .000621 .000343 .000044 .000137 .000144 .000377 .000243 .000621 .000343 .000045 .000141 .000381 .000244 .000625 .000344 .000046 .000144 .000385 .000245 .000629 .000345 .000046 .000144 .000389 .000246 .000633 .000346 .000047 .000148 .000147 .000392 .000247 .000637 .000347<	.000839
.000036 .000114 .000136 .000358 .000236 .000602 .000336 .000037 .000118 .000137 .000362 .000237 .000666 .000337 .000040 .000122 .000140 .000366 .000240 .000610 .000340 .000041 .000125 .000141 .000370 .000241 .000614 .000341 .000042 .000133 .000142 .000377 .000241 .000617 .000342 .000043 .000133 .000144 .000377 .000243 .00625 .000344 .000044 .000137 .000144 .000385 .000245 .000625 .000344 .000045 .000144 .000385 .000245 .000625 .000344 .000046 .000144 .000146 .000389 .000246 .000633 .000346 .000047 .000152 .000150 .000392 .000247 .000637 .000347 .000051 .000156 .000150 .000392 .000247 </td <td>.000843</td>	.000843
.000037 .000118 .000137 .000362 .000237 .000606 .000337 .000040 .000122 .000140 .000362 .000237 .000606 .000340 .000041 .000125 .000141 .000370 .000241 .000614 .000341 .000042 .000129 .000142 .000373 .000242 .000617 .000342 .000043 .000137 .000143 .000377 .000243 .000621 .000343 .000044 .000137 .000144 .000381 .000245 .000629 .000343 .000045 .000141 .000145 .000385 .000245 .000629 .000345 .000046 .000144 .000389 .000245 .000629 .000346 .000047 .000148 .000147 .000392 .000247 .000640 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000351 .000051 .000156 .000151 .000400 .000251<	
.000040 .000122 .000140 .000366 .000240 .000610 .000340 .000041 .000125 .000141 .000370 .000241 .000614 .000341 .000042 .000129 .000142 .000373 .000242 .000617 .000342 .000043 .000133 .000144 .000381 .000244 .000625 .000344 .000046 .000141 .000145 .000381 .000245 .000629 .000344 .000046 .000141 .000146 .000385 .000245 .000629 .000345 .000046 .000144 .000146 .000389 .000246 .00633 .000346 .000047 .000148 .000147 .000392 .000246 .00637 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000156 .000151 .000404 .000250 .000644 .000351 .000052 .000160 .000151 .000404 <td>.000846</td>	.000846
.000041 .000125 .000141 .000370 .000241 .000614 .000341 .000042 .000129 .000142 .000373 .000242 .000617 .000342 .000043 .000133 .000143 .000377 .000243 .000621 .000343 .000044 .000137 .000144 .000385 .000243 .000625 .000344 .000045 .000141 .000146 .000385 .000245 .000629 .000345 .000046 .000144 .000389 .000245 .000633 .000346 .000047 .000148 .000147 .000392 .000250 .000640 .000347 .000050 .000152 .000150 .00396 .00250 .000640 .000350 .000051 .000156 .000151 .00400 .000251 .000644 .000351 .000052 .000160 .000152 .000404 .000252 .00648 .000352 .000053 .000164 .000153 .00408 .000253	.000850
.000042 .000129 .000142 .000373 .000242 .000617 .000342 .000043 .000133 .000143 .000377 .000243 .000621 .000343 .000044 .000137 .000144 .000381 .000243 .000625 .000343 .000045 .000141 .000145 .000381 .000245 .000629 .000345 .000046 .000144 .000145 .000385 .000246 .000633 .000346 .000047 .000148 .000147 .000392 .000247 .000637 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000156 .000151 .000400 .000251 .000644 .000351 .000052 .000160 .000152 .00404 .000252 .00648 .000352 .000053 .000164 .000153 .00408 .000253 .000652 .000353	.000854
.000043 .000133 .000143 .000377 .000243 .000621 .000343 .000044 .000137 .000144 .000381 .000243 .000625 .000344 .000045 .000141 .000145 .000381 .000245 .000629 .000345 .000046 .000144 .000146 .000385 .000246 .000633 .000346 .000047 .000148 .000147 .000392 .000247 .000637 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000156 .000151 .000400 .000251 .000644 .000351 .000052 .000160 .000152 .000404 .000252 .000648 .000352 .000053 .000164 .000153 .000408 .000253 .000652 .000352	.000858
.000044 .000137 .000144 .000381 .000244 .000625 .000344 .000045 .000141 .000145 .000385 .000245 .000629 .000345 .000046 .000144 .000146 .000385 .000246 .000629 .000345 .000047 .000148 .000147 .000392 .000247 .000637 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000156 .000151 .000404 .000252 .000648 .000351 .000052 .000160 .000152 .000404 .000252 .000648 .000352 .000053 .000164 .000153 .000408 .000253 .000652 .000352	.000862
.000044 .000137 .000144 .000381 .000244 .000625 .000344 .000045 .000141 .000145 .000385 .000245 .000629 .000345 .000046 .000144 .000146 .000385 .000246 .000629 .000345 .000047 .000148 .000147 .000392 .000247 .000637 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000156 .000151 .000404 .000252 .000648 .000351 .000052 .000160 .000152 .000404 .000252 .000648 .000352 .000053 .000164 .000153 .000408 .000253 .000652 .000352	.000865
.000045 .000141 .000145 .000385 .000245 .000629 .000345 .000046 .000144 .000146 .000389 .000246 .000633 .000346 .000047 .000148 .000147 .000392 .000247 .000637 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000166 .000151 .000404 .000252 .000644 .000351 .000053 .000160 .000153 .000408 .000253 .000652 .000352	.000869
.000046 .000144 .000146 .000389 .000246 .000633 .000346 .000047 .000148 .000147 .000392 .000247 .000637 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000156 .000151 .000400 .000251 .000644 .000351 .000052 .000160 .000152 .000404 .000252 .000648 .000352 .000053 .000164 .000153 .000408 .000253 .000652 .000352	.000873
.000047 .000148 .000147 .000392 .000247 .000637 .000347 .000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000156 .000151 .000400 .000251 .000644 .000351 .000052 .000160 .000152 .000404 .000252 .000648 .000352 .000053 .000164 .000153 .000408 .000253 .000652 .000353	.000877
.000050 .000152 .000150 .000396 .000250 .000640 .000350 .000051 .000156 .000151 .000400 .000251 .000644 .000351 .000052 .000160 .000152 .000404 .000252 .000648 .000352 .000053 .000164 .000153 .000408 .000253 .000652 .000353	.000881
.000051 .000156 .000151 .000400 .000251 .000644 .000351 .000052 .000160 .000152 .000404 .000252 .000648 .000352 .000053 .000164 .000153 .000408 .000253 .000652 .000353	.000885
.000052 .000160 .000152 .000404 .000252 .000648 .000352 .000053 .000164 .000153 .000408 .000253 .000652 .000353	
.000053 .000164 .000153 .000408 .000253 .000652 .000353	.000888
	.000892
I 0000E4 0001E7 I 0001E4 000411 I 0000E4 000EE I 0000E4	.000896
.000054 .000167 .000154 .000411 .000254 .000656 .000354	.000900
.000055 .000171 .000155 .000415 .000255 .000659 .000355	.000904
.000056 .000175 .000156 .000419 .000256 .000663 .000356	.000907
.000057 .000179 .000157 .000423 .000257 .000667 .000357	.000911
.000060 .000183 .000160 .000427 .000260 .000671 .000360	.000915
000061 000186 000161 000431 000261 000675 000361	.000919
000062 .000190 .000162 .000434 .000262 .000679 .000362	.000923
	.000926
000064 000198 000164 000442 000264 000686 000364	.000930
.000065 .000202 .000165 .000446 .000265 .000690 .000365	.000934
.000066 .000205 .000166 .000450 .000266 .000694 .000366	.000938
.000067 .000209 .000167 .000453 .000267 .000698 .000367	.000942
.000070 .000213 .000170 .000457 .000270 .000701 .000370	.000946
.000071 .000217 .000171 .000461 .000271 .000705 .000371	.000949
000072 000221 000172 000465 000272 000709 000372	.000953
000073 000225 000469 000273 000713 000373	.000957
	.000961
	.000965
000076 000236 000176 000480 000276 000724 000376	000000
.000077 .000240 .000177 .000484 .000277 .000728 .000377	.000968 .000972

OCTAL-DECIMAL FRACTION CONVERSION TABLE (Cont'd)

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001063	.000530	.001312	.000630	.001556	.000730	001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	001682	.000771	.001926
.000472	001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000474							
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
	.001209 .001213 .001216	.000575 .000576 .000577	.001453 .001457 .001461	.000675 .000676 .000677	.001697 .001701 .001705	.000775	.001941 .001945

APPENDIX VI

EXF AND CHARACTER CODES

1604 EXF CODES

SELECT INTERNAL 740 000C0 000C1 01000 02000 00070 C0000 C = 1 - 6SELECT INTERRUPTS 74 0 00100 00101 74 0 04000 04001 SENSE INTERNAL 74 7 000C0 000C1 C = 1 - 6001A0 001A1

Allow Interrupt on Channel C inactive Disallow Interrupt on Channel C inactive Start Real-Time Clock Stop Real-Time Clock Clear Arithmetic Faults and Clock Overflow Clear All Channel C Selections

Allow Interrupt on Internal (Arithmetic) Faults or Clock Overflow Disallow Interrupt on Internal (Arithmetic) Faults or Clock Overflow Allow Selected Interrupts Disallow (Mask) All Interrupts

Exit on Channel C Active Exit on Channel C Inactive

Exit on Arithmetic Fault A

Exit on No Arithmetic Fault A

- A = 1 : Divide
 - 2 : Shift
 - 3 : Overflow
 - 4 : Exponent Overflow
 - 5 : Exponent Underflow

CONSOLE EQUIPMENT (CHANNEL PAIR 1 and 2)

•

SELECT		
INPUT	74 0 <u>11</u> 140	Select Typewriter for Input, and Interrupt on Carriage Return
	100	Select Typewriter for Input, and No Interrupt on C.R.
	200	Select Paper Tape Reader, and No Interrupt on End of Tape
	210	Select Paper Tape Reader and Set End of Tape Indicator
	220	Select Paper Tape Reader, and Interrupt on End of Tape
OUTPUT	$74\ 0\ \underline{21}100$	Select Typewriter for Output, Assembly Mode
	110	Select Typewriter for Output, Character Mode
	200	Select Paper Tape Punch, Assembly Mode
	210	Select Paper Tape Punch, Character Mode
	240	Turn Paper Tape Punch Motor Off
SENSE		
INPUT	74 7 <u>11</u> 200	Exit on Paper Tape Reader,End of Tape
	201	Exit on Paper Tape Reader,No End of Tape
	210	Exit on Paper Tape Reader in Assembly Mode
	211	Exit on Paper Tape Reader in Character Mode
	140	Exit on Typewriter in Lower Case
	141	Exit on Typewriter in Upper Case
	100	Exit on Carriage Return or Tab from Typewriter
	101	Exit on No Carriage Return or Tab from Typewriter
OUTPUT	74 7 21200	Exit on Paper Tape Punch Out of Tape

1607 EXF CODES

(CHANNEL C, CABINET 2)*

PELECI	SE	LE	\mathbf{C}	Т
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INPUT	_	0N1 0N2	Select Read Tape N, Binary Mode Select Read Tape N, Coded Mode
		001 002 004 005 006 007	Read Selected Tape, Binary Mode Read Selected Tape, Coded Mode Interrupt When Selected Tape Ready Rewind Selected Tape Backspace Selected Tape Rewind Selected Tape with Interlock
OUTPUT		0N1 0N2	Select Write Tape N, Binary Mode Select Write Tape N, Coded Mode
		001 002 003 004 005 006 007	Write Selected Tape, Binary Mode Write Selected Tape, Coded Mode Write End of File Mark on Selected Tape Interrupt When Selected Tape Ready Rewind Selected Tape Backspace Selected Tape Rewind Selected Tape with Interlock
SENSE			
INPUT		000 001	Exit on Ready to Read Exit on Not Ready to Read
	(002 003	Exit on Read Parity Error Exit on No Read Parity Error
		004 005	Exit on Read Length Error Exit on No Read Length Error
		006	Exit on End of File Mark

007 Exit on No End of File Mark

* The equipment designator (fourth octal digit from the right) in 1607 EXF codes may be either 2 or 3. A switch in the rear of the 1607 cabinet determines which number will be recognized as the designator for that cabinet.

OUTPUT 74 7 <u>C20</u>

2	2000	Exit on Ready to Write
	001	Exit on Not Ready to Write
	002	Exit on Write Reply Parity Error
	003	Exit on No Write Reply Parity Error
	004	Exit on Write Reply Length Error
	005	Exit on No Write Reply Length Error
	006	Exit on End of Tape Marker
	007	Exit on No End of Tape Marker

1608 EXF CODES

(CHANNEL C) C = 1-6

SELECT

INPUT	74 0 <u>C7</u> 7N1	Select Read Tape N, Binary Mode
	7 N2	Select Read Tape N, Coded Mode
	001	Read Selected Tape, Binary Mode
	002	Read Selected Tape,Coded Mode
	004	Interrupt When Selected Tape Ready
	005	Rewind Selected Tape
	006	Backspace Selected Tape
	007	Rewind Selected Tape with Interlock
	101	Turn Off "Tape Indicator" on Read Unit
	102	Set Low Density on Read Unit
	103	Set High Density on Read Unit
	104	Search File Mark Forward on Read Unit
	105	Search File Mark Backward on Read Unit
	106	Remove Interrupt Selection on Read Unit
OUTPUT	74 0 <u>C7</u> 7N1	Select Write Tape N, Binary Mode
	7N2	Select Write Tape N, Coded Mode
	001	Write Selected Tape, Binary Mode
	002	Write Selected Tape, Coded Mode
	003	Write End of File Mark on Selected Tape

OUTPUT	74 0 <u>C7</u> 004	Interrupt When Selected Tape Ready
	005	Rewind Selected Tape
	006	Backspace Selected Tape
	007	Rewind Selected Tape with Interlock
	101	Turn Off "Tape Indicator" on Write Unit
	102	Set Low Density on Write Unit
	103	Set High Density on Write Unit
	104	Skip Bad Spot on Selected Write Unit
	106	Remove Interrupt on Write Unit

SENSE

INPUT	747	<u>C7</u> 000	Exit on Ready to Read
		001	Exit on Not Ready to Read
		002	Exit on Read Parity Error
		003	Exit on No Read Parity Error
		004	Exit on Read Length Error
		005	Exit on No Read Length Error
		006	Exit on End of File Mark
		007	Exit on No End of File Mark
		106	Exit When Read Unit is Rewinding or at Load Point
		107	Exit When Read Unit is Not Rewinding or is at Load Point
OUTPUT	74 7	<u>C7</u> 000	Exit on Ready to Write
		001	Exit on Not Ready to Write
		002	Exit on Write Reply Parity Error
		003	Exit on No Write Reply Parity Error
		004	Exit on Write Reply Length Error
		005	Exit on No Write Reply Length Error
		006	Exit on End of Tape Marker
		007	Exit on No End of Tape Marker
		106	Exit when Write Unit is Rewinding or at Load Point
		107	Exit when Write Unit is Not Rewinding or is at Load Point

1610 EXF CODES (CHANNEL C) C = 1-6

SE	Ľ	Έ	CT	

INPUT	74 0	<u>C4</u> 001 002 003	Select Primary Read Station Select Secondary Read Station Select Primary and Secondary Read Stations
		005	Select Primary Read Station and Interrupt
		006	Select Secondary Read Station and Interrupt
		007	Select Primary and Secondary Read Stations and Interrupt
OUTPUT	74 0	<u>C4</u> 001	Select Printer
		002	Select Punch
		005	Select Printer and Interrupt
		006	Select Punch and Interrupt
SENSE			
INPUT	747	<u>C4</u> 002	Exit on Reader Ready
		003	Exit on Reader Not Ready
		004	Exit on 1604 Selected
		005	Exit on 1604 Not Selected
OUTPUT	747	<u>C4</u> 002	Exit on Printer Ready
		003	Exit on Printer Not Ready
		004	Exit on Punch Ready
		005	Exit on Punch Not Ready
		010	Exit on 1604 Selected
		011	Exit on 1604 Not Selected

1612 EXF CODES

(CHANNEL C)

C = 1-6

SELECT

OUTPUT	(ONLY)	74 0	<u>C6</u> 000	Select Printer
			001	Single Space the Printer
			002	Double Space the Printer
			003	Select Format Channel 7
			004	Select Format Channel 8
			010	Clear Monitor Channels 1 - 6
			01N	Select Monitor Channel N : N = $1 - 6$
SENSE				
OUTPUT	(ONLY)	747	<u>C6000</u>	Exit on Printer Ready
			001	Exit on Printer Not Ready
			1615 F	UNCTION CODES
			(CHANNI	EL C, CABINET 2)*
			(1	$N = 1_8 - 10_8$)
OUTPUT				
74 0 C	20N1		Select Ta	ape N To Write Binary
	20N2			ape N To Write Coded
	2001			Selected Tape To Write Binary
	2002			Selected Tape To Write Coded
	2003		-	d-Of-File Mark On Selected Tape
	2004			terrupt When Write Tape Next Ready
	2005			elected Write Tape
	2006			ce Selected Write Tape
	2007		-	Unload Selected Write Tape
	2400			errupt Selections On Write Tape
	2401			Density On Selected Write Tape
	2402			Density On Selected Write Tape
	2403		•	Spot On Selected Write Tape
	2404		-	terrupt On Next Error
	- 10 1		201000 111	the service in the service of

* The equipment designator (fourth octal digit from the right) in 1615 EXF codes may be either 2 or 3. A switch in the 1615 cabinet determines which number will be recognized as the designator for that cabinet.

SENSE		
747C	2000	Exit On Ready To Write
	2001	Exit On Not Ready To Write
	2002	Exit On Write Reply Parity Error
	2003	Exit On No Write Reply Parity Error
	2004	Exit On Write Reply Length Error
	2005	Exit On No Write Reply Length Error
	2006	Exit On End Of Tape Marker
	2007	Exit On Not End Of Tape Marker
	2400	Exit On Ready To Select
	2401	Exit On Not Ready To Select
	2402	Exit On Load Point
	2403	Exit On Not Load Point
	2404	Exit On Interrupt On Write Tape
	2405	Exit On No Interrupt On Write Tape
	2406	Exit On Write Program Error
	2407	Exit On No Write Program Error
INPUT		
740C	20N1	Select Tape <u>N</u> To Read Binary One Record
	20N2	Select Tape <u>N</u> To Read Coded One Record
	22N1	Select Tape <u>N</u> To Read Binary One File
	22N2	Select Tape <u>N</u> To Read Coded One File
	2001	Prepare Selected Tape To Read Binary One Record
	2002	Prepare Selected Tape To Read Coded One Record
	2201	Prepare Selected Tape To Read Binary One File
	2202	Prepare Selected Tape To Read Coded One File
	2003	Move Selected Read Tape Forward One Record
	2203	Search File Mark Forward
	2004	Select Interrupt When Read Tape Next Ready
	2005	Rewind Selected Read Tape
	2006	Backspace Selected Read Tape
	2206	Search File Mark Backward
	2007	Rewind-Unload Selected Read Tape
	2400	Clear Interrupt Selections On Read Tape
	2401	Set Low Density On Selected Read Tape
	2402	Set High Density On Selected Read Tape
	2404	Select Interrupt On Next Error

SENSE 747C

2000 Exit On Ready To Read 2001 Exit On Not Ready To Read 2002 Exit On Read Parity Error 2003 Exit On No Read Parity Error 2004 Exit On Read Length Error 2005 Exit On No Read Length Error 2006 Exit On End Of Tape Marker 2007 Exit On Not End Of Tape Marker 2400 Exit On Ready To Select 2401Exit On Not Ready To Select 2402Exit On Load Point 2403 Exit On Not Load Point 2404Exit On Interrupt On Read Tape 2405 Exit On No Interrupt On Read Tape 2406 Exit On Read Program Error 2407 Exit On No Read Program Error

SATELLITE EXTERNAL FUNCTION CODES

1604 EXTERNAL FUNCTION CODES

OUTPUT S	SELECT	1
74 0 C	2500	Release Direct Selections
	2501	Select Write Control For 160
	2502	Release Write Control To 1604
	2503	Select Direct 1604 To 160
	2504	Select Action Request
	2520	Clear Communication Flag 2
	2540	Set Communication Flag 1
	2560	Clear Communication Flag 1

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OUTPUT	SENSE	
747C	2500	Exit On Write Control Available
	2501	Exit On Write Control Not Available
	2520	Exit On Communications Flag 2 Set
	2521	Exit On Communications Flag 2 Not Set
	2560	Exit On Communications Flag 1 Set
	2561	Exit On Communications Flag 1 Not Set
INPUT SE	ELECT	
74 0 C	2501	Select Read Control For 160
	2520	Release Read Control To 1604
	2503	Select Direct 160 To 1604
	2505	Release Interrupt
INPUT SE	ENSE	
747C	2500	Exit On Read Control Available
	2501	Exit On Read Control Not Available
	2504	Exit On 160 Interrupt
	2505	Exit On No 160 Interrupt
<u>160 EXTE</u>	ERNAL FUNCTIC	DN CODES
WRITE SI	ELECT	
	6050	Release Action Request
	6051	Set Communications Flag 2
	6052	Release Write Control To 1604
	6055	Clear Communications Flag 1
	6056	Clear Communications Flag 2
READ SE	LECT	
	5051	Set Communications Flag 1
	5052	Release Read Control To 1604
	5053	Select Interrupt
STATUS	RESPONSE*	
	4XXX	Read Control Available
	2XXX	Write Control Available
	1XXX	Direct 160 To 1604
	X4XX	Direct 1604 To 160
	XXX2	160 Action Request
·	XXX1	Communications Flag 1 Set

* Bits may be superimposed; e.g., 6XXX means both Read Control and Write Control available.

APPENDIX VII

Magnetic Tape BCD Codes

Character	Code (Octal)	Character	Code (Octal)
А	61	2	02
В	62	3	03
С	63	4	04
D	64	5	05
E	65	6	06
F	66	7	07
G	67	8	10
Н	70	9	11
I	71	\$	60
J	41	-	40
K	42	(blank)	2 0
L	43	1	21
М	44	. (period)	73
Ν	45	\$	53
Ο	46	*	54
Р	47	, (comma)	33
Q	50	%	34
R	51	#	13
S	22	@	14
Т	23	Ц	74
U	24	0 (numerical zero)	12
v	25	record mark	32
W	26	0 (minus zero)	52
х	27	0 (plus zero)	72
Y	30	group mark	77
Z	31	tape mark	17
0	12		
1	01		

		APPENDI Flexowriter			
UC	LC	CODE	UC	LC	CODE
Α	a	30	Y	У	2 5
в	b	23	Z	a	21
С	с	16	O	0	56
D	đ	22	1	1	74
E	е	20	2	2	70
F	f	26	з	3	64
G	g	13	4	4	62
Ħ	h	05	5	5	66
I	i	14	6	6	72
J	j	32	7	7	60
к	k	36	8	8	33
L	1	11	9	9	37
М	m	07	-	-	52
N	n	06	t	1	44
0	ο	03	()	54
Р	р	15	+	,	46
Q	q	35	=		42
R	r	12	:	;	50
S	S	24	CR	(mage)	45
т	t	01	Lower C	ase (UC) ase (LC)	47 57
U	u	34	Back Spa Color Sh	nift (CS)	61 02
v	v	17	Tabulate Stop	e (TAB)	51 43
w	w	31	Space Tape Fe	ed	04 00
x	x	27	Delete		77
Note:	Ste	eader - Blank tap op - Stop Flex , 40, 41, 53, 55, (owriter reader,	ete - Delete 73, 75, and 76	

APPENDIX IX

Punched Card Codes

Char	Card	BCD	Char	Card	ВСD	Char	Card	BCD	Char	Card	BCD
			+	12	60		11	40			20
l	l	01	A	12 1	61	J	11 1	41	/	0 1	21
2	2	02	В	12 2	62	К	11 2	42	S	0 2	22
3	з	03	C	12 3	63	L	11 3	43	T	0 3	23
4	4	04	D	12 4	64	М	11 4	44	U	0 4	24
5	5	05	E	12 5	65	N	11 5	45	v	0 5	25
6	6	06	F	12 6	66	0	11 6	46	W	0 6	26
7	7	07	G	12 7	67	Р	11 7	47	x	0 7	27
8	8	10	Н	12 8	70	Q	11 8	50	Y	0 8	30
9	9	11	I	12 9	71	R	1 1 9	51	Z	0 9	31
0	o	12	+0	12 0	72	-	11 0	52			
=	8,3	13	•	12 8,3	73	\$	11 8,3	53	,	о 8 , 3	33
-	8,4	14)	¹² 8 ,4	74	*	11 8 , 4	54	(8 ⁰ 4	34

Input/Output Typewriter Codes								
CHAR/ UC	ACTERS LC	CODE	CHARAC UC	LC	CODE			
A	a	30	x	x	27			
В	Ъ	23	Y	y	25			
C	C	16	Z	Z	21			
D	đ	22)	0	56			
E	e	20	*	1	74			
F	f	26	0	2	7 0			
G	g	13	#	3	64			
Н	h	05	\$	4	62			
I	i	14	95	5	66			
J	j	32	¢	6	72			
K	k	36	&	7	60			
L	1	11	$\frac{1}{2}$	8	33			
М	m	07	(9	37			
N	n	06	-	-	52			
0	o	03	?	/	44			
P	P	15	π	t	54			
Q	q	35	0	+	46			
R	r	12	•	•	42			
S	s	24	:	3	50			
T	t	01	,		40			
υ	u	34	•	=	02			
۷	•	17	tab	tab	51			
W	W	31	spa	.¢e	04			
Back	space	61	Carria	ge Return	45			
Lower Case		57	Upper	Case	47			

APPENDIX X

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APPENDIX XI

1612 Printer Codes

CHAR	CODE	CHAR	CODE	CHAR	CODE	CHAR	CODE
Blank	20	F	66	v	25	5	15
0	12	Ģ	67	w	26	1	16
1	01	Ħ	70	X	27	C	17
2	02	I	71	Y	30	Ξ	32
3	03	J	41	Z	31	-	35
4	04	к	42	•	73	=	36
5	05	L	43	-	40	~, ^	37
6	06	м	44	+	60	% or∨	52
7	07	N	45	=	13	\$ or 🗆	53
8	10	0	46	(34	t	5 5
9	11	Р	47)	74	ŧ,	56
A	61	Q	50	1	21	>	57
в	62	R	51	*	54	<	72
С	63	S	22	,	33	≥.	75
D	64	т	23	:	00	?	76
Е	65	U	24	ŧ	14	· ·	77

In last column, codes ~ % \$ appear if business application, $\land \lor \neg$ for scientific application.

COMMENT SHEET

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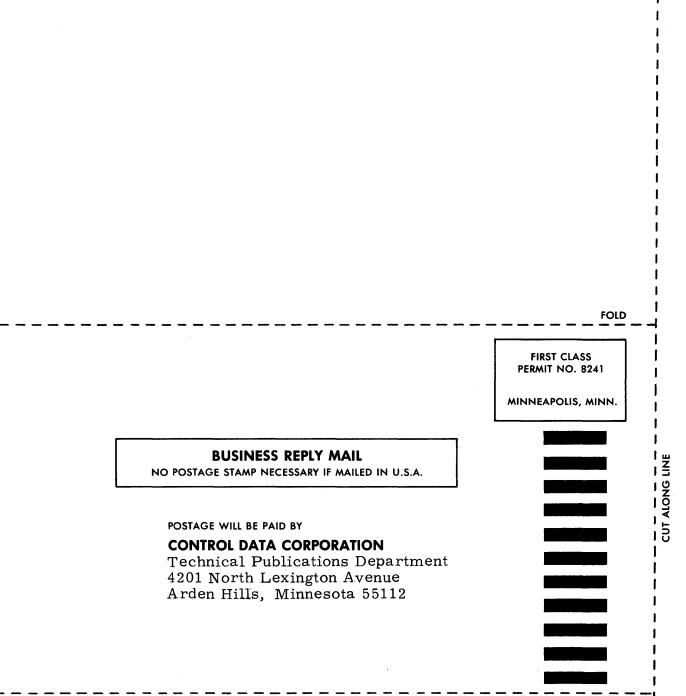
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FOLD

FOLD



FOLD

STAPLE

i

Page Page ADD Add 14 2 - 18MUF **Multiply Fractional** 2 - 21 26 45 2 - 36 2 - 19 ADL MUI **Multiply Integer** 24 Add Logical AJP A Jump 22 2 - 28, 31 OUT **Output Transfer** 63 2 - 41 ALS A Left Shift 05 2 - 14 QJP Q Jump 23 2 - 29, 32 2 - 14 06 ARS A Right Shift 01 QLS Q Left Shift 2 - 15 DVF 2 - 21 2 - 14 **Divide Fractional** 27 QRS **Q** Right Shift 02 DVI **Divide Integer** 25 2 - 20 RAD Replace Add 70 2 - 39 ENA 2 - 26 RAO Replace Add One 72 2 - 39 Enter A 10 RSB ENI Enter Index 2 - 27 **Replace** Subtract 2 - 39 50 71 ENO 2 - 26 RSÒ Replace Subtract One 73 2 - 40 Enter Q 04 EQS Equality Search 64 2 - 37 SAL Substitute Address, L 61 2 - 16 3 - 3 SAU Substitute Address, U 2 - 16 EXF **External Function** 74 60 2 - 36 FAD Floating Add 30 2 - 21 SBL Subtract Logical 46 2 - 25FDV **Floating Divide** 33 2 - 24SCA Scale A 34 2 - 35 FMU **Floating Multiply** 32 2 - 23 SCL Selective Clear 41 FSB **Floating Subtract** 31 2 - 22 SCM Selective Complement 42 2 - 34 2 - 17 SCQ 35 2 - 25 IJР 55 Scale AQ Index Jump INA 11 2 - 26 SEV (not used) 77 Increase A 2 - 13 INI Increase Index 51 2 - 27SIL Store Index, L 57 2 - 13 INT Input Transfer 2 - 41 SIU Store Index, U 56 62 2 - 30, 32 2 - 17 SLJ Selective Jump 75 ISK Index Skip 54 2 - 30, 32 LAC Load A, Complement 2 - 11 SLS Selective Stop 76 13 2 - 33 2 - 11 Storage Shift 37 LDA Load A 12 SSH 2 - 33 LDL 44 2 - 36 SSK Storage Skip 36 Load Logical 2 - 34 2 - 11 SST Selective Set 40 LDQ Load Q 16 2 - 36 LIL Load Index, L 53 2 - 13 SSU Selective Substitute **43** 2 - 12 LIU Load Index, U 52 2 - 27 STA Store A 20 2 - 36 AQ Left Shift STL Store Logical 47 LLS 2 - 15 07 21 2 - 12 LQC Load Q, Complement 17 2 - 11 STQ Store Q 2 - 18LRS AQ Right Shift 03 2 - 14 SUB Subtract 15 Threshold Search 65 2 - 37 THS MEQ Masked Equality 66 2 - 38 00 Masked Threshold 2 - 38 ZRO (not used) MTH 67

1604 INSTRUCTIONS



>>> CUT OUT FOR USE AS LOOSE -LEAF BINDER TITLE TAB



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