Digital Electronics

STUDENT MANUAL

CONTROL DATA
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DIGITAL ELECTRONICS

STUDENT MANUAL

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or use Comment Sheet in the back of this manual.

FOREWORD

This student manual is intended to be a supplement to your study of the course material. No one can learn this material for you, but you can help yourself by paying attention to the way you learn.

Every session is carefully structured to leave you with the ability to do certain things or objectives that are expected of you during the course. These objectives are the basic elements on which you will be tested and information that you will need to be successful when you graduate. Every subject will contain several explicitly stated objectives. Read them, use them to study, and review them again to ask yourself if you have completely learned the material in each subject area.

At times you may be inclined to question whether or not the material that you are studying is really necessary to achieve an objective. Keep in mind that there are succeeding subjects with material you must learn, and some information simply helps you to learn.

Everyone wants to succeed. You would like to consider yourself as a success in a few months. The following suggestions should help you:

1. Read the subject objectives before class. These are goals, and it is your responsibility to attain them.
2. Start now, and be prepared for every class session. It is much more difficult to catch up than it is to prepare adequately.
3. See your instructor immediately if you find yourself becoming confused; do not wait until it is too late. You may see him by appointment, during a break, or before or after class.
4. Do not hesitate to ask questions in or out of class. You may feel that everyone else knows the answers, but the objectives are also your personal objectives. If you knew all the answers, you would not be here.
5. Take careful notes, but do not try to record so much of the lecture that you fall behind.
6. Laboratories are extremely important. Participate actively and rely on your own work. Do not accept someone else's demonstration of their abilities; achieve your own objectives.
7. Most examinations will be open book. Open book examinations are not as easy as they may sound. Your learning process will have to supplement text material in order for you to pass the examinations. The object of open book examinations is to remove the burden of memorization of formulas, tables, and diagrams. These are not course objectives.
8. Assignments listed are designed to prepare you for the material in each subject area. Check ahead for long reading assignments so that you can complete all assignments on time. All review questions that appear in assigned reading material are part of the assignment.

CONTENTS

FIGURES

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TABLES

OBJECTIVES AND ASSIGNMENTS BY SUBJECT

The instructor will identify the subject areas in advance which pertain to given sessions. Although reading assignments may be done in advance, all assignments are due on the day following the day in which the subject is presented.

The textbooks for this course are Introduction to Digital Computers, Volumes I, II, and III, Control Data publication numbers 60241600, 60241700, and 60241800; 3000 Printed Circuits Manual, Control Data publication number 60238500; and Digital Electronics Student Manual, Control Data publication number 60353500.

1. INTRODUCTION TO THE NUMBER SYSTEM

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe integer, real, rational, irrational, imaginary, and complex numbers.
2. Define radix and exponent and describe the differences between positional and non-positional number systems.

ASSIGNMENT

Introduction to Digital
Computers, Volume I: Pages 3-1 through 3-17

2. INTEGER CONVERSION

OBJECTIVES

Upon completion of this subject you will be able to:

1. Compare and contrast the binary, octal, and hexadecimal number systems and make conversions from them to decimal.
2. Make conversions from binary, octal, or hexadecimal to the decimal number system.

ASSIGNMENT

Introduction to Digital
Computers, Volume I: Pages 3-17 through 3-32
Problems 129 through 140, page 3-70

3. ARITHMETIC IN OTHER BASES

OBJECTIVES

Upon completion of this subject you will be able to:

1. Perform addition and subtraction in any number system discussed.

ASSIGNMENT

Introduction to Digital
Computers, Volume I: Pages 3-32 through 3-49

4. BOOLEAN ALGEBRA INTRODUCTION

OBJECTIVES

Upon completion of this subject you will be able to:

1. Define the AND, OR, and NOT functions of Boolean algebra.
2. Write the Boolean statement represented by a logic diagram.
3. Draw the logic diagram for a Boolean statement.

ASSIGNMENT

Student Manual: Reference 1

5. AND/OR AND NAND/NOR CIRCUITS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe the difference between positive and negative logic.
2. Recognize the schematic circuit for an AND/OR or a NAND/NOR circuit.
3. Draw, using logic symbols, given combinations of AND/OR and NAND/NOR circuits.
4. Translate the output of AND/OR and NAND/NOR circuits.
5. Construct and analyze the operation of AND, OR, NAND, and NOR circuits.

ASSIGNMENT

Student Manual: Exercise 1
Laboratory 1
Reference 5

6. LAWS OF BOOLEAN ALGEBRA

OBJECTIVES

Upon completion of this subject you will be able to:

1. Identify and use the first six laws of Boolean algebra.
2. Simplify a Boolean statement by use of these laws.

ASSIGNMENT

Student Manual: Reference 2

7. BOOLEAN ALGEBRA AND VEITCH DIAGRAMS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Identify the last six laws of Boolean algebra.
2. Define DeMorgan's theorem.
3. Simplify a Boolean statement by use of these laws.
4. Construct Veitch diagrams for two, three, and four variables.
5. Simplify Boolean statements using Veitch diagrams.

ASSIGNMENT

Student Manual: References 3 and 4

8. WIRE LISTS AND EQUATION FILES

OBJECTIVES

Upon completion of this subject you will be able to:

1. Define the term wire list.
2. Define, describe, and analyze an equation for a logic circuit.

ASSIGNMENT

None

9. INVERTERS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe the difference between 1604 and 3000 inverters.
2. Describe the electrical connection required to form an AND gate in 1604 logic.
3. Translate the output of circuits using AND, OR, NAND, and NOR.
4. Draw logic diagrams to achieve any given translation.
5. Construct and analyze an inverter circuit.

ASSIGNMENT

Student Manual: Exercise 2
Laboratory 3
Reference 6

10. INTRODUCTION TO THE LOGIC TRAINER

OBJECTIVES

Upon completion of this subject you will be able to:

1. Use the logic trainer to wire and analyze simple logic circuits.

ASSIGNMENT

Student Manual: Laboratory 2

11. FLIP-FLOP CIRCUITS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe the action of a flip-flop.
2. Distinguish between the set and clear states of the flip-flop.
3. Construct and analyze the operation of flip-flop circuits.
4. Describe the operation of flip-flop circuits with the use of timing diagrams.

ASSIGNMENT

Student Manual: Exercise 3
Laboratory 4
Reference 7

12. INPUT/OUTPUT CIRCUITS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Explain the purposes of transmitter and receiver cards for data transmission.
2. Explain the uses of L and M cards with lamps or switches.
3. Determine the outputs of L and M cards with given conditions of inputs.
4. Differentiate between logic and nonlogic voltages.
5. Describe the functions of T and R cards.

6. Describe the function of a twisted-pair transmission line associated with T and R cards.
7. Identify the connections required at the input to an R card for logic conversion.

ASSIGNMENT

Student Manual: Exercise 4
Laboratory 5
Reference 8

13. TRANSMISSION LINES

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe the concept of the high-frequency transmission line.
2. Explain the cabling arrangement for data transfer in a computer system.
3. Briefly describe the concepts of characteristic impedance and reflected impedance of transmission lines.
4. Explain the reason for termination of transmission lines.
5. Define the artificial transmission line.

ASSIGNMENT

None

14. DIGITAL ELECTRONICS EXAMINATION 1

15. INDUCTIVE AND CAPACITIVE DELAYS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Give the reasons for using delays.
2. Describe the function of an inductive delay.
3. List the disadvantages and advantages of inductive and capacitive delays.
4. Describe the function of a capacitive delay.
5. Differentiate between fixed and adjustable delays.

ASSIGNMENT

Student Manual: Exercise 5
Reference 9

16. PULSE-FORMING NETWORKS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Identify and differentiate between leading-edge and trailing-edge networks.
2. Draw a diagram of a leading-edge network using standard logic symbols.
3. Determine the output of a leading-edge network with given input conditions.
4. Draw a diagram of a trailing-edge network using standard logic symbols.
5. Determine the output of a trailing-edge network with given input conditions.

ASSIGNMENT

Student Manual: Exercise 6

17. REGISTERS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Define a register.
2. Determine the output of selected terms within a 6-bit register.
3. Describe a one's transfer.
4. Describe a zero's transfer.
5. Describe a forced transfer.
6. Describe a complement transfer.

ASSIGNMENT

Student Manual: Exercise 7
Laboratory 6
Reference 10

18. CLOCK PYRAMID AND TIMING

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe the need for a master oscillator.
2. Describe the differences between:

   Odd raw clock and even raw clock.
   Even time and odd time.
   Raw clock and clock slaves.

ASSIGNMENT

Student Manual: Exercise 8
Reference 11

19. CONTROL DELAYS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe the function of the control delay.
2. Differentiate between a control delay and a capacitive delay.
3. Determine the time of the output when given a set of H and N or V terms.
4. Determine the H term outputs under given input conditions.
5. Define what is meant by conditioning input and describe its effect on the terms to which it is applied.

ASSIGNMENT

Student Manual: Reference 12

20. COUNTERS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Differentiate between sequential and nonsequential counting.
2. List the reasons for using double-rank counters in preference to single-rank counters.
3. Trace the count in a three-stage, double-rank counter from 0 to 7.
4. Define a gray code.
5. List a group of eight digits, 0 through 7, in correct order to represent a gray code.
6. Recognize and describe the operation of a recycling counter.
7. Construct a counter circuit on the logic trainer.
8. Use an oscilloscope to evaluate the operation of the counter and construct timing diagrams.

ASSIGNMENT

Student Manual: Exercise 9
Laboratory 7
Reference 13

21. SHIFT NETWORKS

OBJECTIVES

Upon completion of this subject you will be able to:

1. List two applications of shift networks.
2. Define left shift.
3. Define right shift.
4. Define sign extension.
5. Determine the final contents of a 3-bit shift network following a left shift.
6. Determine the final contents of a 3-bit shift network following a right shift both with and without sign extension.

ASSIGNMENT

Student Manual: Laboratory 8
Reference 14

22. COMPLEMENT ARITHMETIC

OBJECTIVES

Upon completion of this subject you will be able to:

1. Differentiate between two's and one's complement.
2. Differentiate between eight's and seven's complement.
3. Calculate the complement of any number selected.
4. Perform addition and subtraction using complement notation.
5. Differentiate between positive and negative numbers in a signed register.
6. Recognize and define overflow.

ASSIGNMENT

Introduction to Digital
Computers, Volume I: Pages 3-50 through 3-69, 3-73, and 3-74

23. ADDERS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe the process of adding binary numbers.
2. Differentiate between a half-add and a full-add.

3. Describe the circuit operation of the half-adder.
4. Describe the circuit operation of the full-adder.
5. Derive the output equations for the half-adder and the full-adder.

ASSIGNMENT

Student Manual: Laboratory 9
Reference 15

24. TRANSLATORS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Differentiate between encoders and decoders.
2. Produce a binary translation from any octal digit using an encoder diagram.
3. Derive the output equations for a two-stage, AND-gate decoder.
4. Determine the correct inputs for a three-stage, AND-gate decoder.
5. Determine both input and output equations for a three-stage, inverter decoder.
6. Describe the operation of a function code translator.

ASSIGNMENT

Student Manual: Laboratory 10
Reference 16

25. CIRCUIT APPLICATIONS

OBJECTIVES

Upon completion of this subject you will be able to:

1. Describe the basic construction of a printed circuit board.
2. Analyze standard schematics to describe output signals for a given input and perform troubleshooting.
3. Demonstrate the correct techniques in replacing a component on a printed circuit board.

ASSIGNMENT

None

26. INTEGRATED CIRCUITS

OBJECTIVES

Upon completion of this subject you will be able to:

1. List the advantages of integrated circuits over conventional circuits.
2. List the integrated circuit manufacturing techniques and the advantages of each.
3. Describe the construction and operation of integrated circuits.

ASSIGNMENT

Student Manual: Reference 17

EXERCISE 1

LOGIC AND/OR CIRCUITS

1. Describe AND circuit operation in terms of inputs and outputs.
the output of an and ckt is 1 only if all inputs are one (1)

2. Fill in the following truth table to show the operation of a three-input AND circuit. Use 1 for high voltage and 0 for low voltage.

Input 1	Input 2	Input 3	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3. In the circuit of figure 1, if both inputs are normally at ground potential, in what state are diodes D_1 and D_2? conducting.

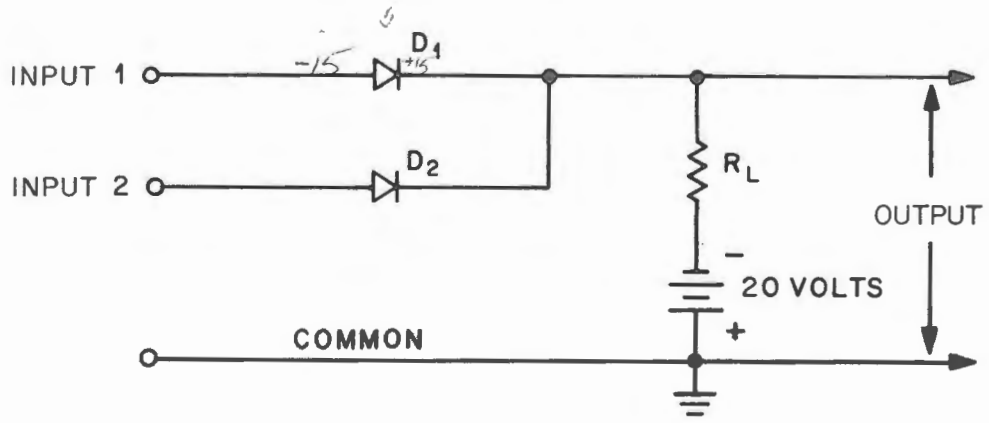


Figure 1. Identifying Diode States

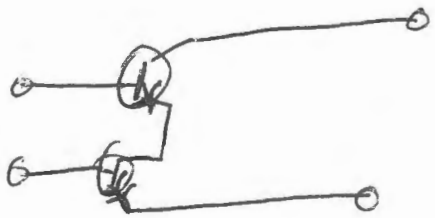
4. With the inputs specified in question 3, the output voltage in the circuit of figure 1 will be — 10 VOLTS.

5. If the voltage applied to input 1 in the circuit of figure 1 is -15 volts (with input 2 grounded), the output voltage will be — 10VOLTS.

6. Explain why output voltage for the conditions specified in question 5 is as indicated.
because in case 1 there is no voltage dropped accross the DIODES in case 2 ~~-15 VOLTS IS ACCROSS D1~~ D 2 is still conducting

7. If the voltages applied to both inputs in the circuit of figure 1 are -15 volts, the output voltage will be ~~-10 VOLTS~~ ~~0~~ -15 VOLTS.

8. Draw a circuit using transistors with two inputs which will perform the AND function.



9. Explain OR circuit operation in terms of the inputs and outputs.
the ~~output~~ is 1 if any of the inputs equal a one

10. Fill in the truth table to show the operation of a three-input OR circuit using 1 for high voltage and 0 for low voltage.

Input 1	Input 2	Input 3	Output
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

11. In the circuit of figure 2, to cause one of the diodes to conduct, the polarity of the voltage required at its input is negative with respect to ground.

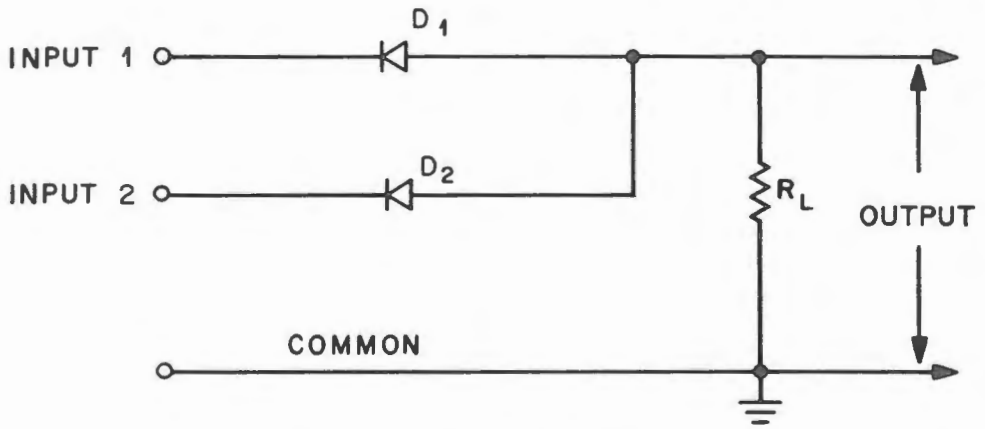


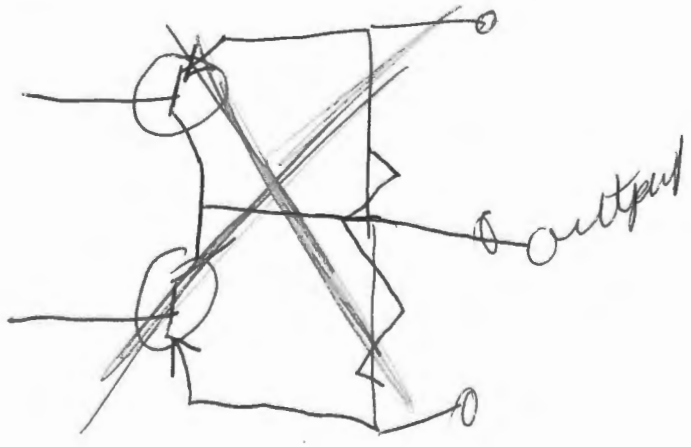
Figure 2. Identifying Input Polarity

12. If the voltage applied to input 1 in the circuit of figure 2 is of the proper polarity to cause D_1 to conduct, the polarity of the voltage developed across R_L will be negative.

13. If the voltage applied to input 1 in the circuit of figure 2 is -10 volts, and the voltage applied to input 2 is -15 volts, the output voltage will be -15 VOLTS.

14. With input voltages specified in question 12, explain why output voltage is unaffected by the voltage applied to input 1. because input 2 is greater and causese D1 to ~~cutoff~~ be reversed bias

15. Draw a two-input circuit using transistors that will perform the OR function.



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EXERCISE 2

INVERTER CIRCUITS

1. The amplifier circuit configuration that is used as the inverter is Common emitter.

2. The inverter circuit performs the Boolean NOT function by 180° phase shift.

3. What is meant by:
   a. positive logic? a more positive logic = 1
   b. negative logic? a more negative logic = 1

4. In Control Data 1604 logic cards, a logical 0 level is represented by ~~0~~ -.5 volts, and a logical 1 level is represented by ~~0~~ -3 volts.

5. It is not desirable to allow a switching transistor to go into saturation because it takes time to recover from this condition.

6. It is not desirable to allow a switching transistor to be driven to cutoff because same as above.

7. The difference between a type 11A circuit card and a type 12A card is 12A - 2 inputs versus 1 in the 11A.

8. The difference between a type 11A circuit card and a type 13A card is 13A - 3 inputs versus 1 in the 11A.

For the remaining questions, refer to the circuit of figure 68 on page 275.

9. With the input to the card open-circuited, the voltage at the junction of R_{01} and CR_{01} is ~~-20 volts~~ -3 VOLTS.

10. Under the condition specified in question 7, the voltage at TP-A is -.5 VOLTS.

11. The purpose of CR_{08} is prevents cutoff.

12. The purpose of CR_{07} is prevents Saturation

13. If pin 1 of the circuit card is grounded, conduction through the transistor will stop ~~10 to 80 nanoseconds~~.

14. The time for the circuit to switch from one state to the other is approximately 10 to 80 nanoseconds.

15. It is not possible to obtain a correct voltage reading on pins 5 through 12 with no load connected to the circuit card because elements of the load will drop some voltage.

16. The ground pin on the circuit cards is always pin 14.

17. If R_{09} open-circuited, the voltage at TP-A would be ~~increased~~ -20.

18. If R_{10} open-circuited, the voltage at the base of the transistor would be +20 ~~increased~~.

EXERCISE 3

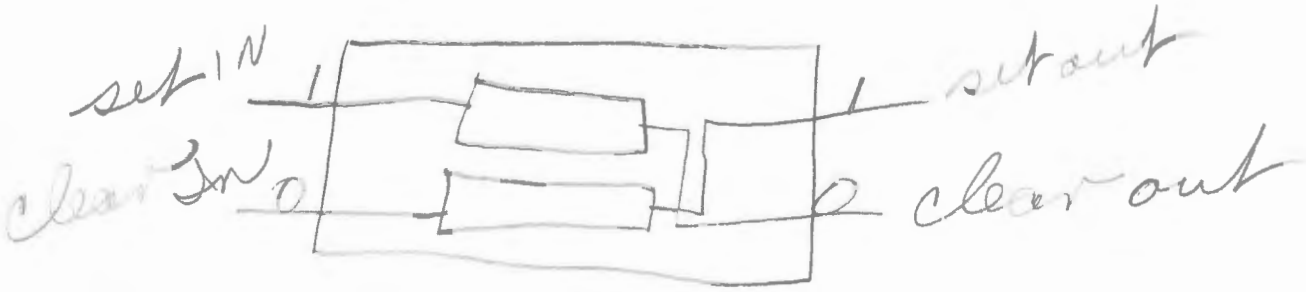
FLIP-FLOPS

1. The basic function of a flip-flop as used in computer systems is maintain logical control of computer functions.

2. The set state of a flip-flop is 1 set 0 clear

3. The clear state of a flip-flop is 0 set 1 clear

4. Draw the standard flip-flop logic circuit using inverter logic symbols. Show the interconnections between the inverters and the method of obtaining the set and clear outputs.



5. When power is first applied to a flip-flop circuit, into which state will the circuit switch? 1

6. The flip-flop remains in the state to which it is switched by an input pulse because it is a bistable multivibrator feedback paths between inverters

7. If a logical 1 level was applied simultaneously to both inputs of a flip-flop, the condition of the outputs at this time would be 0 limbo

8. In the logic symbols of a flip-flop circuit shown in figure 3, the designations K000 and K001 represent [illegible] for set and clear outputs.

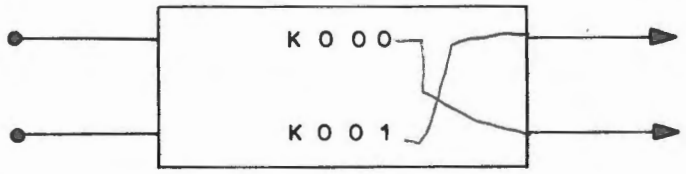


Figure 3. Flip-Flop

9. In the circuit of question 8, the set output is obtained from (~~K000~~/K001) and the clear output is obtained from (K000/~~K001~~).

10. Refer to the circuit of figure ~~32~~ 75 on page ~~54~~ 283. The feedback between stages in the flip-flop is provided by CR 14 A, CR 14 B.

11. Refer to the circuit of figure ~~32~~ 75 on page ~~54~~ 283. Assuming the circuit is in the set state, the logic levels that would exist at the set and clear outputs if CR14A opened are set output logic 0 clear output logic 0

12. If the logic symbol above the flip-flop is clear, K000 equals 0 out. and K001 equals 0 out.

13. What must the inputs and outputs be to produce a state of limbo?

1 & 1

14. If a flip-flop is in limbo, and a 0 is applied to the set input, its new state will be clear.

EXERCISE 4

INPUT/OUTPUT CIRCUITS AND INPUT/OUTPUT CARDS

1. The type of transistor circuit configuration used on the input/output cards is Common emitter.

2. The main difference between the standard inverter circuit and the input/output circuit cards is the inverter shifts 180° the I/O shifts twice for a total of 360° or back in phase and they are not logic voltages.

3. If a logical 1 level is applied to the input of a type 62 card, the output voltage will be ground. If a logical 0 level is applied to the input, the output voltage will be −16 volts.

4. The type 62 or output card is used to change a logic level to a non-logic voltage level.

5. In order to produce a logical 1 level at the output of a type 61 card, the voltage applied to its input must be (ground) 0 volts. In order to produce a logical 0 level at its output, the input voltage must be −16 volts.

6. The type 61 or input card is used to change a voltage level to a logic voltage output level.

7. The type 61 and 62 cards are not considered to be logic inverters because they are always used in pairs and cause a total of 360° phase shift.

8. It is necessary to use voltage levels greater than the normal logic levels for transmission over long cables because R of the cable will cause a voltage drop.

9. In the circuit in figure 4, logic designation L001 represents a type 62 card, and the designation M001 represents a type 61 card.

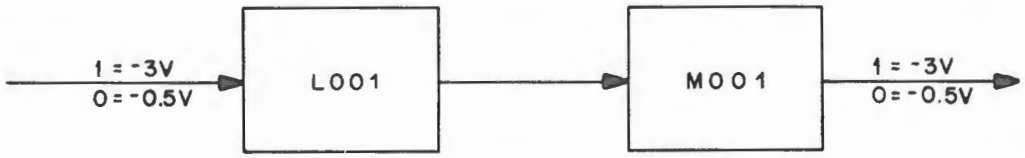


Figure 4. L and M Cards

EXERCISE 5

CAPACITIVE DELAY CIRCUITS

1. The purpose of the delay circuit is delay a logic 1 or a logic 0

2. The delay time of the capacitive delay circuit is determined by value of RCX5.

3. In the circuit of figure 5, the charge path for the delay capacitor is THROUGH R2 TO C TO GROUND.

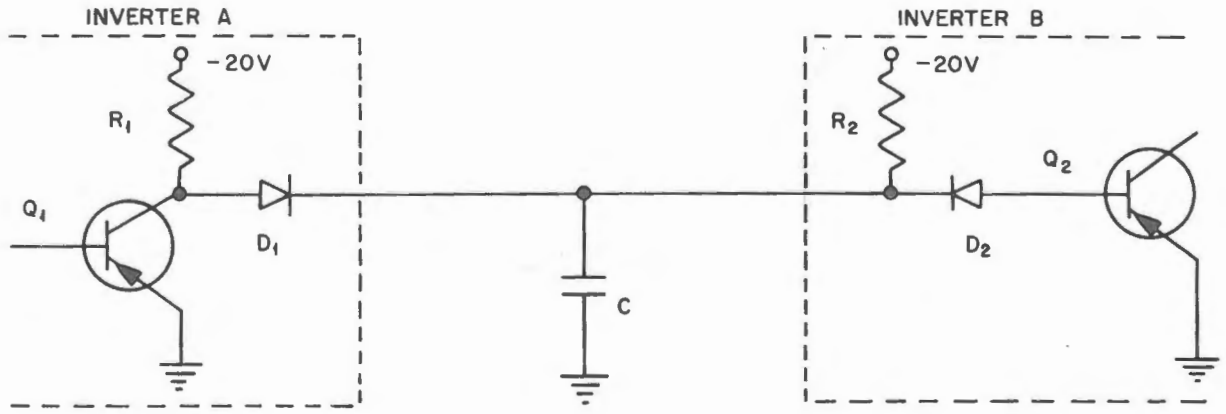


Figure 5. Delay Capacitor Charge Path

4. The discharge path for C in the circuit of figure 5 is D1 - Q1 TO GROUND.

5. The discharge time of C is SHORT compared to the charging time.

6. The transfer of a logical 0 level is not delayed by the delay circuit because short CKT FOR DISH PATH.

7. If the value of C in the circuit of figure 5 is increased, the amount of delay will INCREASE.

8. The threshold voltage of an inverter circuit means voltage at which Q ("turns on").

9. In the circuit of figure 6, the amount of delay is determined by setting of R.

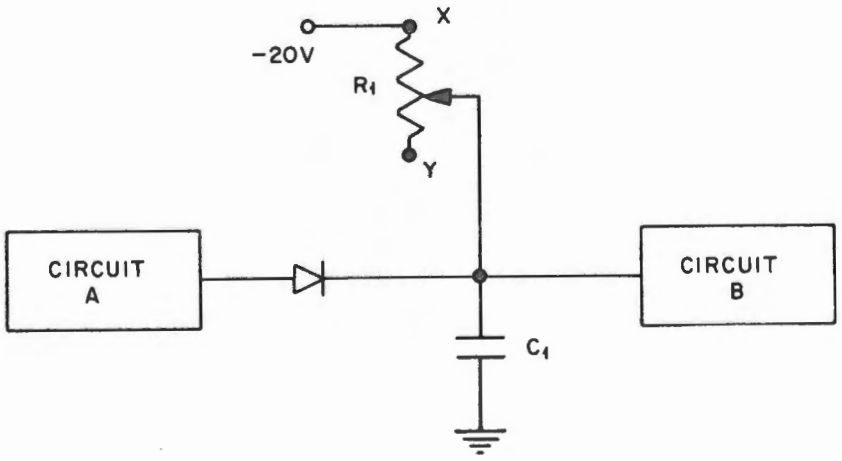


Figure 6. Determining the Amount of Delay

10. In the circuit of figure 6, moving the potentiometer slider toward point X will cause the amount of delay to DECREASE.

11. The amount of delay in the circuit of figure 6 may be increased by MOVING TAP TO Y or INCREASING C_1.

EXERCISE 6

PULSE-FORMING NETWORKS

1. The purpose of a pulse-forming network is provide a pulse for a certain duration.

2. a. Leading-edge network means ouput is logic 1 when input switches from 0 to 1.

   b. Trailing-edge network means ouput is logic 1 when input switches from 1 to 0.

3. The circuit of figure 7 is a leading edge pulse-forming network.

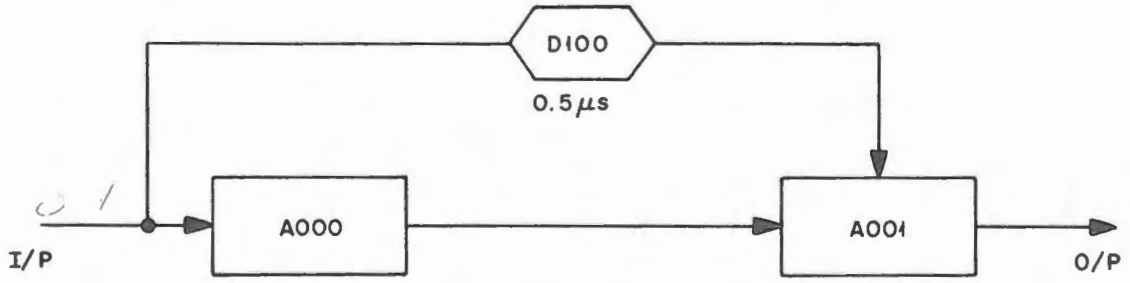


Figure 7. Pulse-Forming Network

4. If the input to A000 in the circuit of figure 7 changes to a logical 1 level, the output of A001 will be .5 second logical 1 pulse (-3 VOLT).

5. If the input to A000 in the circuit of figure 7 changes to a logical 0 level, the output of A001 will be 0 ouput.

6. The circuit of figure 8 is a TRAILING EDGE pulse-forming network.

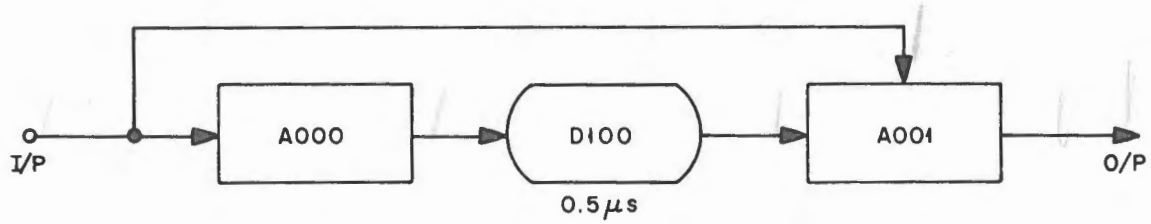


Figure 8. Pulse- Forming Network

7. If the input to A000 in the circuit of figure 8 changes to a logical 0 level, the output of A001 will be .5 usecond logical 1 pulse.

EXERCISE 7

REGISTERS

1. The purpose of a register is temporary storage of data (1 or 0's)

2. The three basic register types found in any computer are A- accumulator P. program address F. REG FUNCTION REGISTER

3. The binary number indicated by a flip-flop is logical 1 when the flip-flop is in its set condition.

4. List the various binary combinations that can be stored by a three-stage register and their octal equivalent as shown:

Binary	Octal
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

111 111 111 111 111 111 111 111

5. The highest octal number that can be stored by a 24-bit register is 77777777

6. The number of register stages that would be required to store a maximum octal number of 3777 is 11 bits.

7. Which of the following flip-flop designations represents the flip-flop in bit position 3?

K000	K240	K630	K120
K001	K241	K631	K121

8. The purpose of the gate or enable input applied to register circuits is _____

_____

_____.

9. Assuming that flip-flop A in the circuit in figure 9 is set, describe the operations required to transfer this condition to flip-flop B. _____

_____ transfer pulse

_____

_____

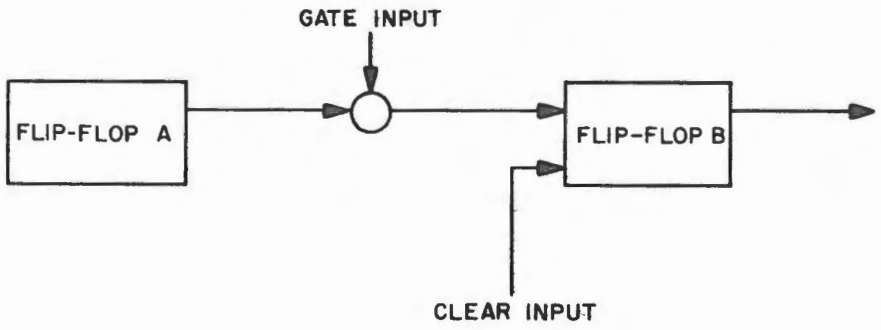


Figure 9. Transferring Conditions

10. The method of transfer shown in the circuit of figure 9 is known as _____ transfer.

11. a. Forced transfer means that _____

_____

_____.

b. Forced transfer is accomplished by _____

_____

_____.

12. A double-rank register means that _____

_____

_____.

EXERCISE 8

CLOCK PYRAMID

1. The function of the master clock oscillator is to provide timing for all operation of the computer.

2. Odd raw clock time means outputs taken from the two II.

3. Even phase time means MMP1 is conducting.

4. It is necessary to form a pyramid because to average a wide

EXERCISE 9

COUNTERS

1. The difference between a sequential counter and a nonsequential counter is _____
is a nonsequential counter operates so as to change only 1 bit per pulse.

2. In the basic two-stage counter shown in figure 10, the AND gates that were last enabled with the conditions shown are 4 & 1

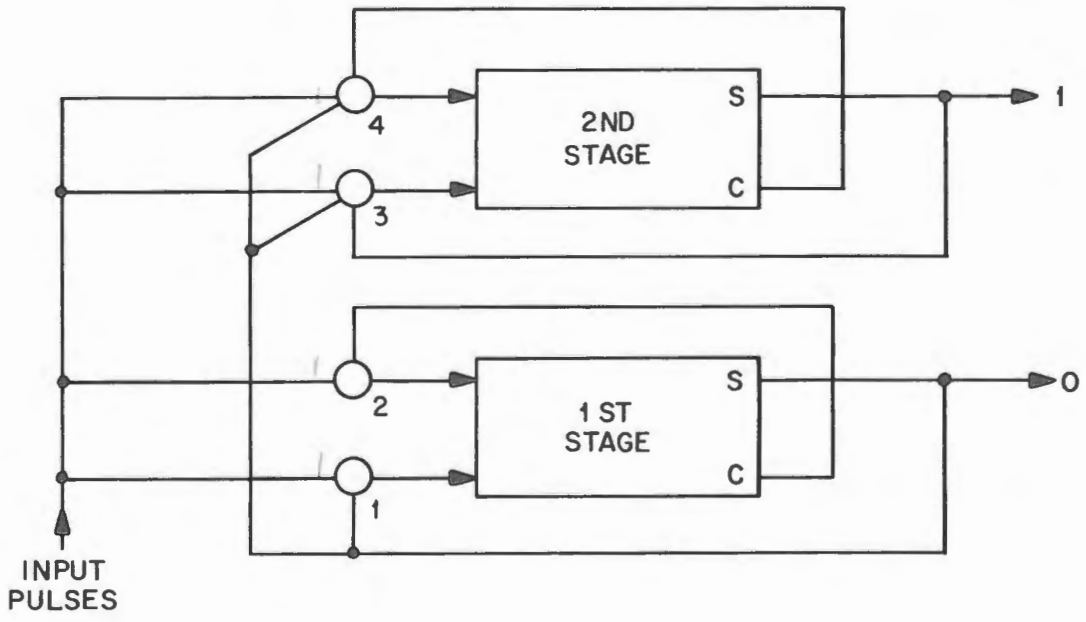


Figure 10. Two-Stage Counter

3. In what state will the flip-flops in the circuit of figure 10 be after the next input pulse? set, set.

4. How many input pulses would be required to cause a four-stage counter to go through its complete counting sequence? ~~8, 2,~~ 16

5. A single-rank counter of the type shown in figure 10 will not operate in modern computer systems because the input pulse could be so long that the transistors might switch more than once causing inaccurate counting.

6. Double-rank means a counter with a second row of FF which hold the pulses after transfer.

Use figure 11 to answer questions 7 through 10.

7. Refer to the accompanying circuit of the double-rank counter. Assume that both ranks are initially cleared and describe the sequence of operations required to produce a count of 1 at the output. advance pulse sets stage I rank I. transfer pulse sets stage I rank II

8. In the double-rank counter, why will the second stage of rank I not set until the first stage in rank II is set? the transfer pulse is required for feedback

9. If the first and second stages of rank I in the double-rank counter are set, and the second stage of rank II is set, the result of applying another advance pulse to the counter would be none.

10. The transfer input to a double-rank counter is normally supplied by 180° phase shift pulse (from advance clock alone of the master clock oscilator.

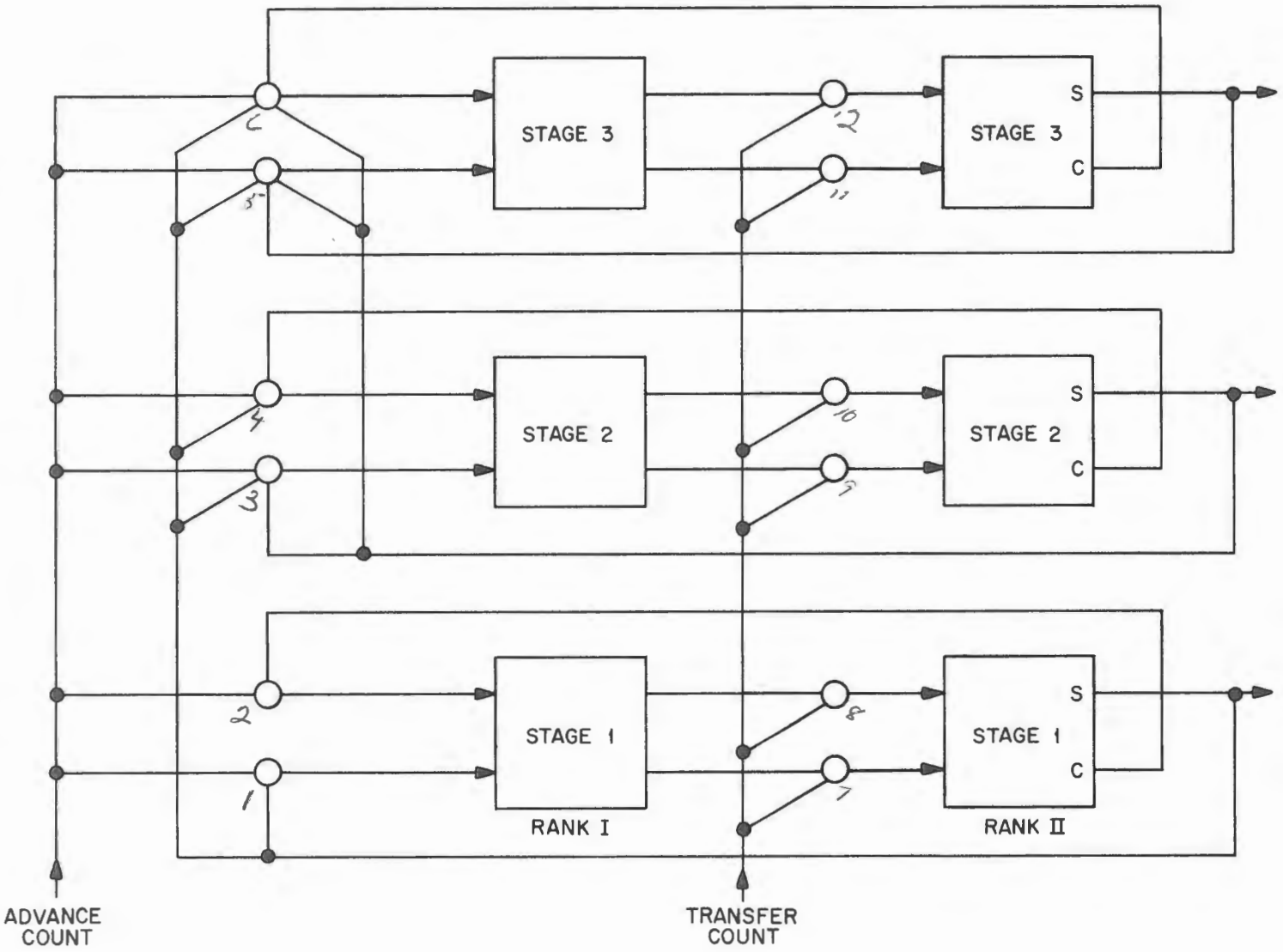


Figure 11. Three-Stage Counter

11. A gray code means non sequential counts one bit changes.

12. Three different combinations of octal digits which represent a gray code are 000 001 003 100 101 111 110 and 000 100 101 111 011 001.

13. In the recycling counter shown in figure 12, the inverters that will produce an output when both flip-flops are in the clear state are ~~J001~~, ~~J002~~ ALL THREE and J002.

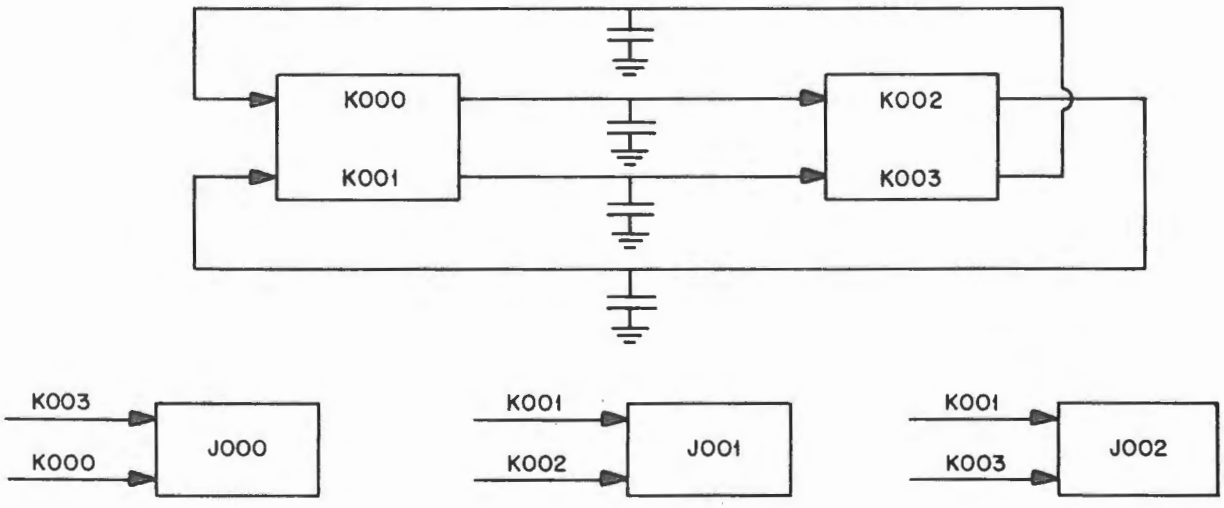


Figure 12. Recycling Counter

LABORATORY 1

DIODE AND/OR GATES

OBJECTIVE

This laboratory is designed to familiarize the student with the operation of the diode AND, OR, and combined AND/OR gates.

EQUIPMENT

Oscilloscope
Laboratory - Volt Kit
Laboratory - Volt Power Supply

INTRODUCTION

You have learned that computer operations are accomplished by the use of logic circuits. There are three basic types of logic circuits that form the building blocks of computer arithmetic and control sections. These are the AND circuit, the OR circuit, and the NOT circuit. These circuits may be combined in specific arrangements to perform various logic functions. The circuit operations within a computer are binary; i.e., they may exist in one of two possible states or voltage levels. A high voltage level is used to represent a logical 1 condition and a low voltage level is used to represent a logical 0 condition.

Because of the binary nature of the various logical operations performed by a computer, these operations are usually described in terms of Boolean algebra. This algebraic representation of logic circuits provides a convenient means of analyzing the operating characteristics of digital electronic systems and can be used in troubleshooting such systems.

In this experiment, observe the operating characteristics of the basic diode AND and OR circuits. Refer to figure 13 for diode code. You found that the output voltage from an AND gate is high, i.e., logical 1, only when the voltage levels at all inputs are high (logical 1). Output voltage from an OR Circuit, however, is equal to a logical 1 when a logical 1 is applied to any input. Set up circuits to verify the characteristics of both types of logic circuits as well as the operation of combined AND and OR gates.

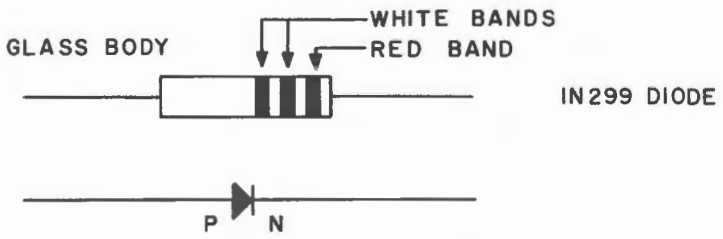


Figure 13. Diode Code

PROCEDURE

DIODE AND GATE

Build the circuit shown in figure 14.

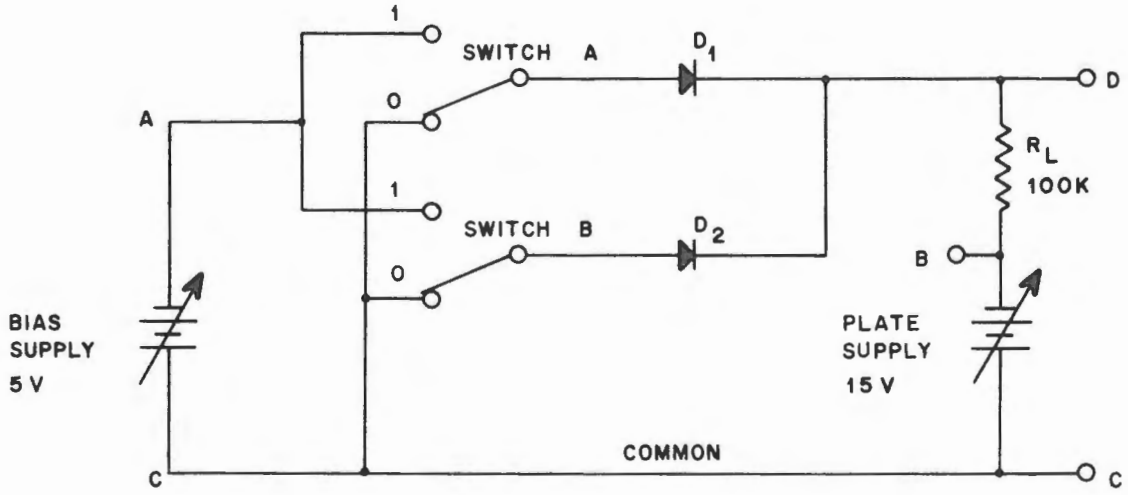


Figure 14. Diode AND Gate

Set the scope to measure DC voltage. Connect the scope between points A and C and adjust the bias supply for 5 VDC. Connect the scope between points B and C and adjust the plate supply for 15 VDC. Connect the scope between points D and C to measure the DC output voltage. Then place switches A and B in their 0 position. Measure the output voltage of points D and C and record it in Table 1. Repeat this procedure for the four switch combinations listed in Table 1, and record the output voltage for each combination.

NOTE

Logical 0 = 0 Volts
Logical 1 = -5 Volts

Using the data obtained from the truth table, write the output equation in terms of A and B.

f =

TABLE 1. DIODE AND GATE

A	B	VOLTAGE	LOGIC
0	0		
0	1		
1	0		
1	1		

Explain why the output voltage was 0 for all combinations other than AB. _____

_____

Disassemble your circuit and proceed to the next paragraph.

DIODE OR GATE

Set up the circuit as shown in figure 15.

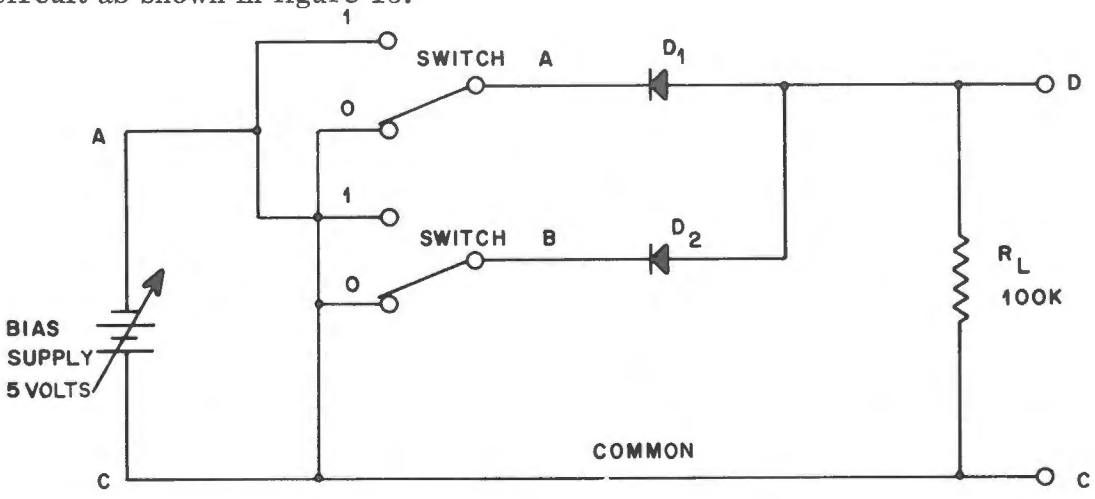


Figure 15. Diode OR Gate

Connect the scope between points A and C and adjust the bias supply for 5 VDC. Place both switches in the 0 position. Connect the scope between points D and C to measure the DC output voltage. Set up the switch combination as indicated by the truth table and record the output voltages in Table 2, for each combination.

TABLE 2. OR GATE

A	B	VOLTAGE	LOGIC
0	0		
0	1		
1	0		
1	1		

Using the data recorded in Table 2, write the output equation in terms of A and B.

f =

Disassemble your circuit and proceed to the next paragraph.

COMBINED DIODE AND/OR GATES

The circuit you are about to build will perform the logical operation indicated by the logic block diagram in figure 16. The following logic still applies:

Logical 0 = 0 Volts
Logical 1 = -5 Volts

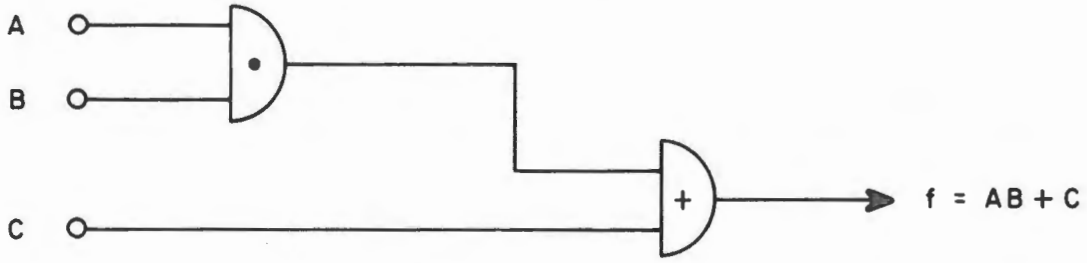


Figure 16. Boolean Diagram AND/OR Gate

Build the circuit shown in figure 17.

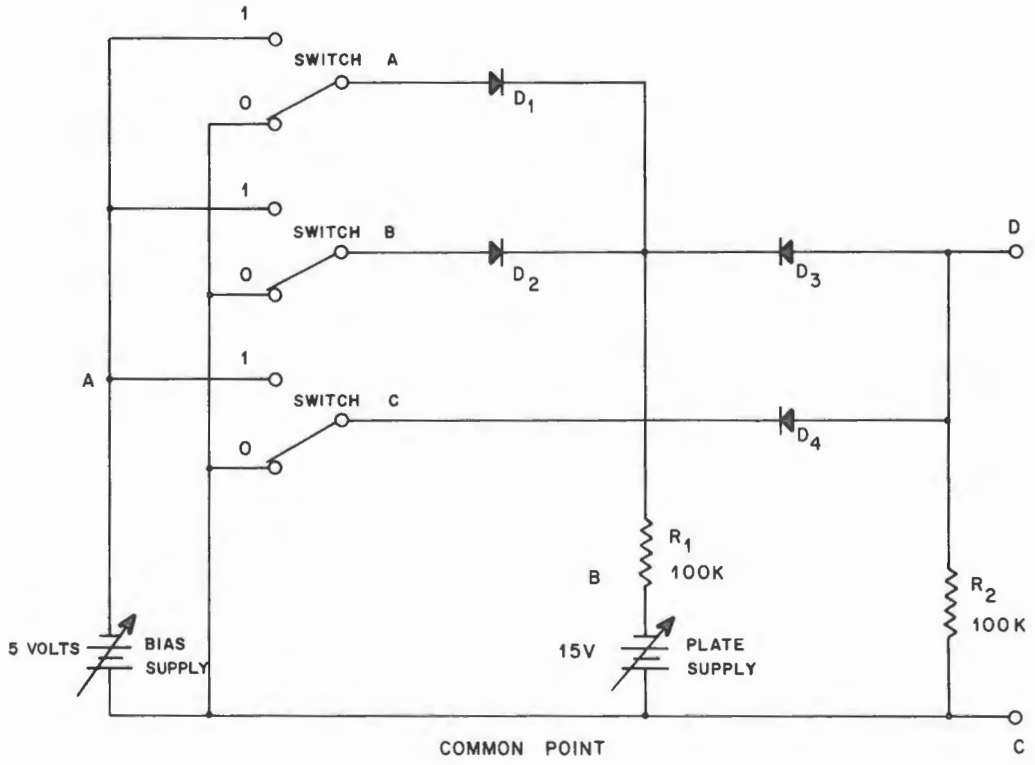


Figure 17. AND/OR Gate

Connect the scope between points A and C and adjust the bias supply for 5 VDC. Then connect the scope between points B and C and adjust the plate supply for 15 VDC. Place all switches in the 0 position and connect the scope between points D and C to measure the DC output voltage.

Following the sequence of the truth table, proceed through the eight combinations of the three switches. Record the output voltage for each combination in Table 3.

TABLE 3. AND/OR GATE

A	B	C	VOLTAGE	LOGIC
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Using the data from Table 3, write the output equation in terms of A, B, and C.

f =

Explain why the output was 0 for all other combinations. _____

_____

Disassemble the circuit and return all components to the laboratory kit.

SUMMARY

1. Explain why the circuit of figure 14 is referred to as an AND gate. _____

_____

_____

2. What would be the effect on the output of figure 14 if diode D1 open-circuited?_____

_____

_____

_____

3. Why is the circuit of figure 15 referred to as an OR circuit?_____

_____

_____

_____

LABORATORY 2

CONTROL DATA INSTITUTE LOGIC TRAINER DESCRIPTION

INTRODUCTION

The Control Data Institute Logic Trainer is a compact, portable, demonstration and experimentation unit designed to offer realistic practice with digital computer logic circuits. The trainer is designed to accommodate the 1604 printed circuit cards and, with modifications, 3000 series printed circuit cards. In the following experiments you will use the logic trainer, a basic chassis for logic experiments.

GENERAL DESCRIPTION

Refer to figures 18 and 19 or the actual logic trainer while reading the following description.

Across the top of the trainer and mounted vertically there are 10 buggies that provide 20 buggie positions. The positions are numbered 1 through 20 and are referred to as buggie position I06, I10, I19, etc. throughout the following experiments. Also note that each buggie position has 15 holes numbered 1 through 15. The male connectors of the card jacks are also numbered 1 through 15. The connectors and the buggies must match. This condition is established if the component side of the card is on the right when inserting the printed circuit card into the buggies, looking from the back of the trainer.

Across the lower level of the trainer, there are also four buggies that allow access to voltage supplies, switches, lights, and the clock. The buggies on the extreme right and left which are labeled A, B, G, and H allow for interconnecting two Control Data Institute Logic Trainer units.

The trainer can be modified to accept 3000 series circuit cards. These modifications must be completed before the experiments using 3000 logic can be performed.

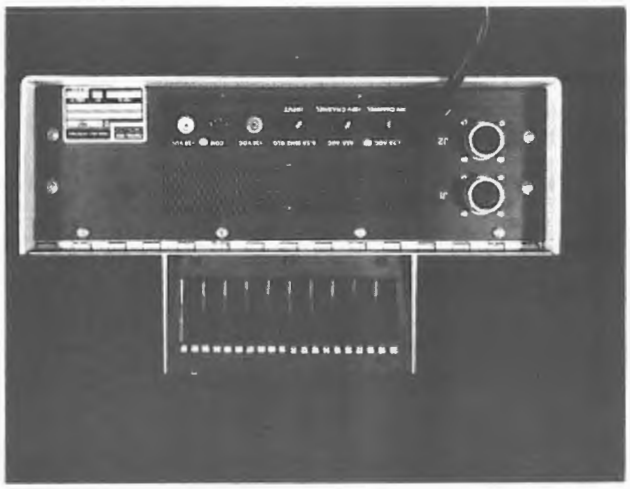


Figure 18. Rear View of Logic Trainer

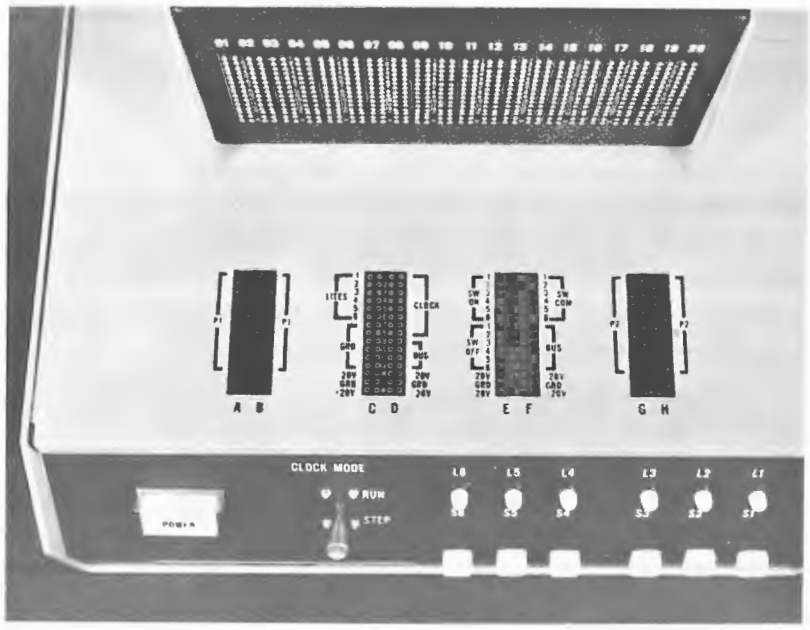


Figure 19. Front View of Logic Trainer

To the right of the front panel, there are six indicator lamps numbered 1 through 6. These lamps will be used for visual indication of the completion of a logic operation; see figure 20.

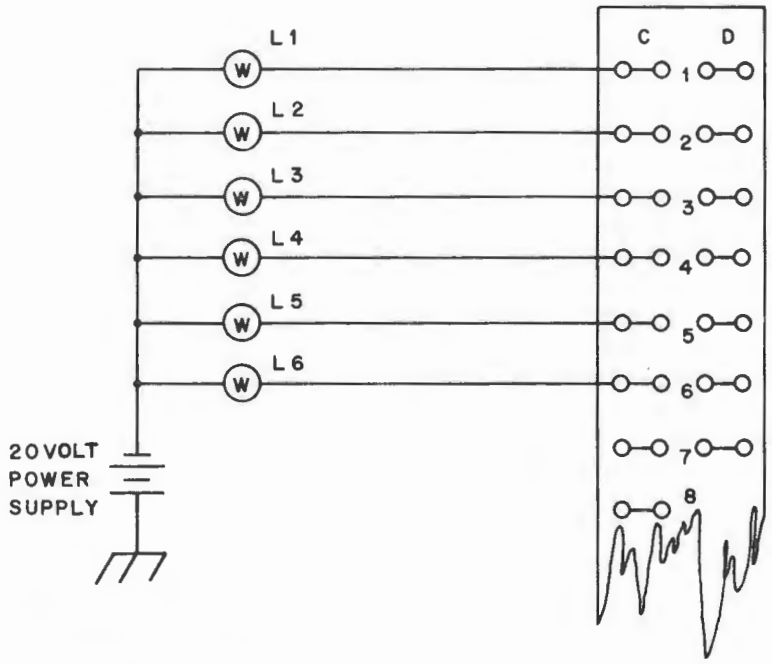


Figure 20. Internal Wiring for Rows C and D

For example, to light lamp 1 a wire should be connected from C1 to any ground. On the trainer, make this connection and note that the circuit is completed to light lamp 1. Repeat this procedure with lamps 2 through 6. All that is necessary to light the lamp is to provide ground or 0 volts to any one of the first six pins of buggie position C.

To the right of the center panel, there are six push-push switches numbered 1 through 6 that are used to enter data into the logic circuit under observation. These switches operate as follows: when pressed they remain closed until pressed again. While pressed, buggie positions F1 through F6 are making contact with buggie positions E1 through E6. In the released position F1 through F6 make contact with E7 through E12, respectively. Refer to figure 21.

To check this operation, place a ground on buggie F pin 1. Run a lead from buggie C pin 1 to buggie E pin 1. Press switch 1 and lamp L1 should light. Test the other switches in the same manner.

Clock output is given in figure 22 and the internal clock is illustrated in figure 23. The clock operates at approximately 25 kHz. The even clock outputs are connected to D2, D4, D6, and D8. The odd clock outputs are fed to D1, D3, D5, and D7.

The clock operates in either run or step mode. During run mode, it outputs a continuous train of square waves; in step mode, it outputs a logical 1 pulse. To test this circuit, each clock output under test must be loaded; i.e., fed to the input of an inverter card.

An on/off, push-push switch, called power, has an inside light which lights when the machine is turned on. The switch is on the front of the trainer. The internal power supply is fused at the back side of the trainer at 120 VAC (Input), -20 VDC, and +20 VDC.

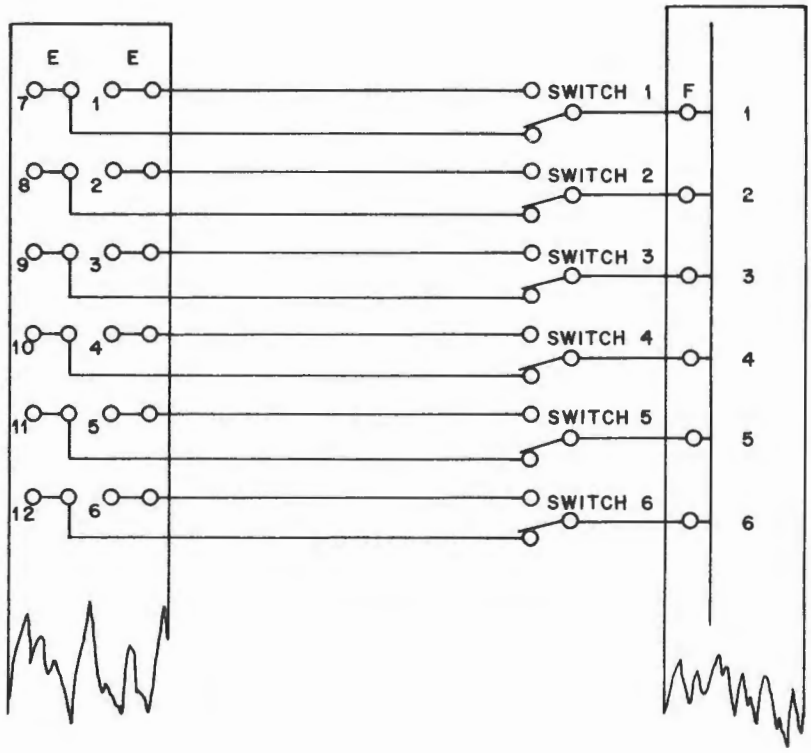


Figure 21. Internal Connections for Rows E and F

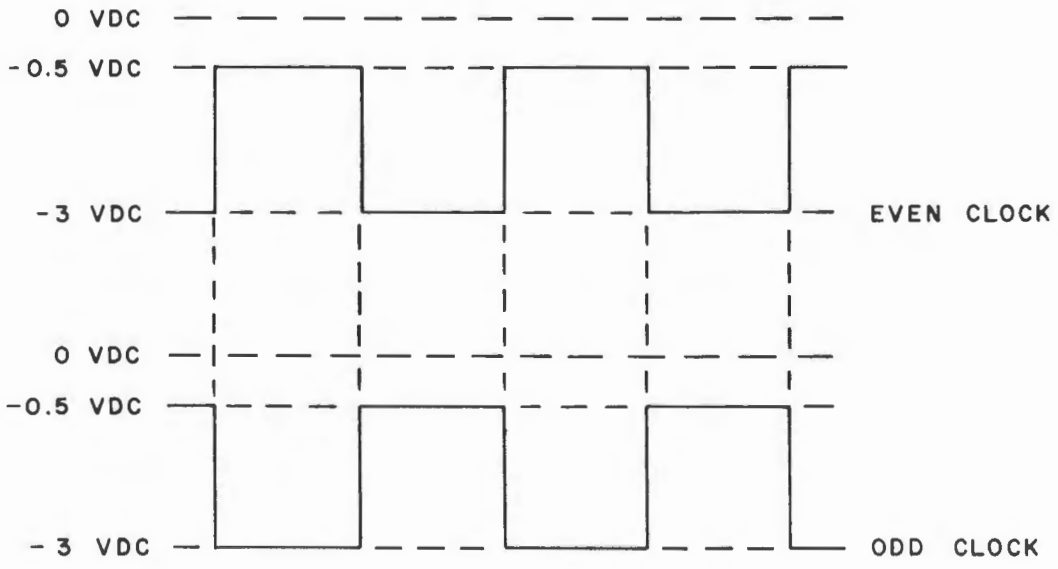
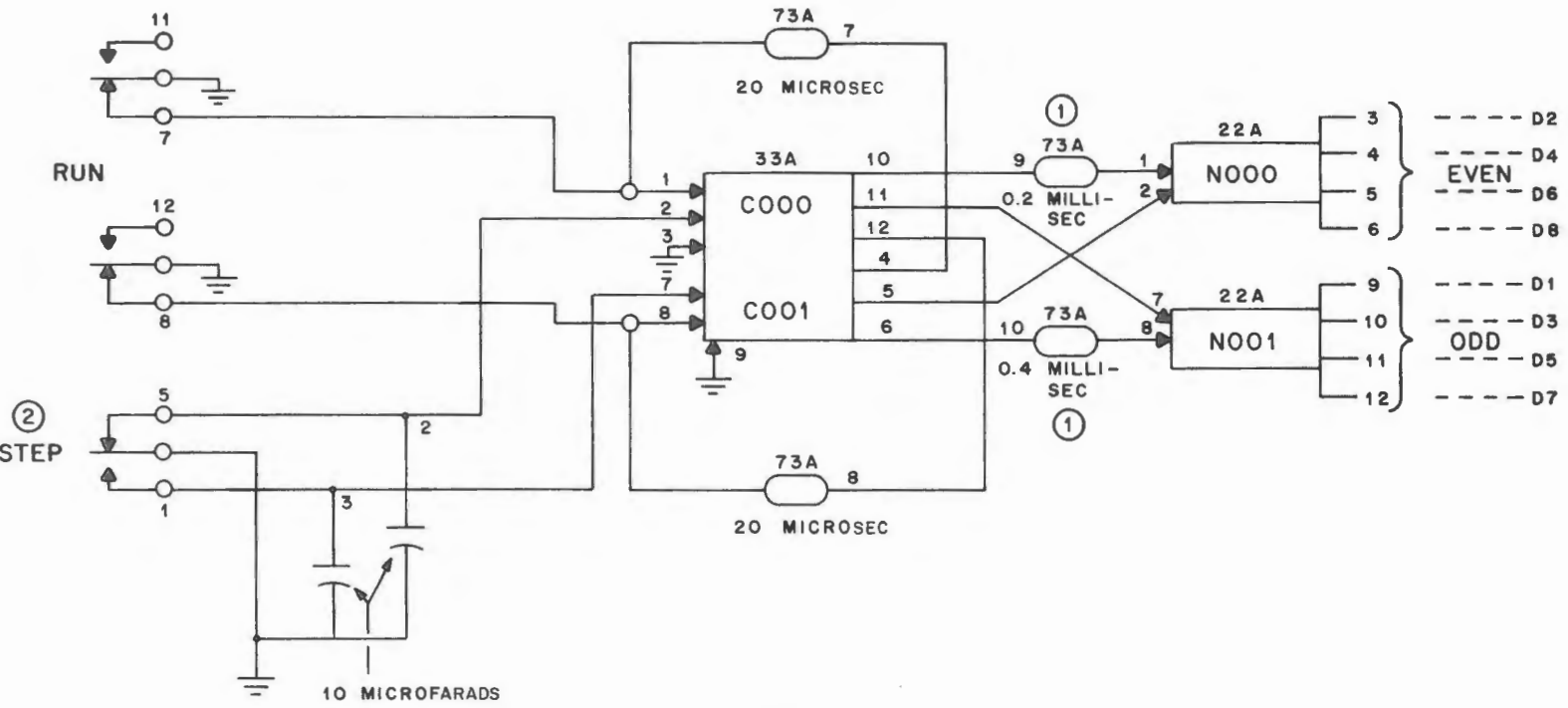


Figure 22. Clock Output



LEGEND

(1) PURPOSE – STEP MODE OF OPERATION ONLY

(2) CHARACTERISTIC OF CONTACTS – MAKE BEFORE BRAKE

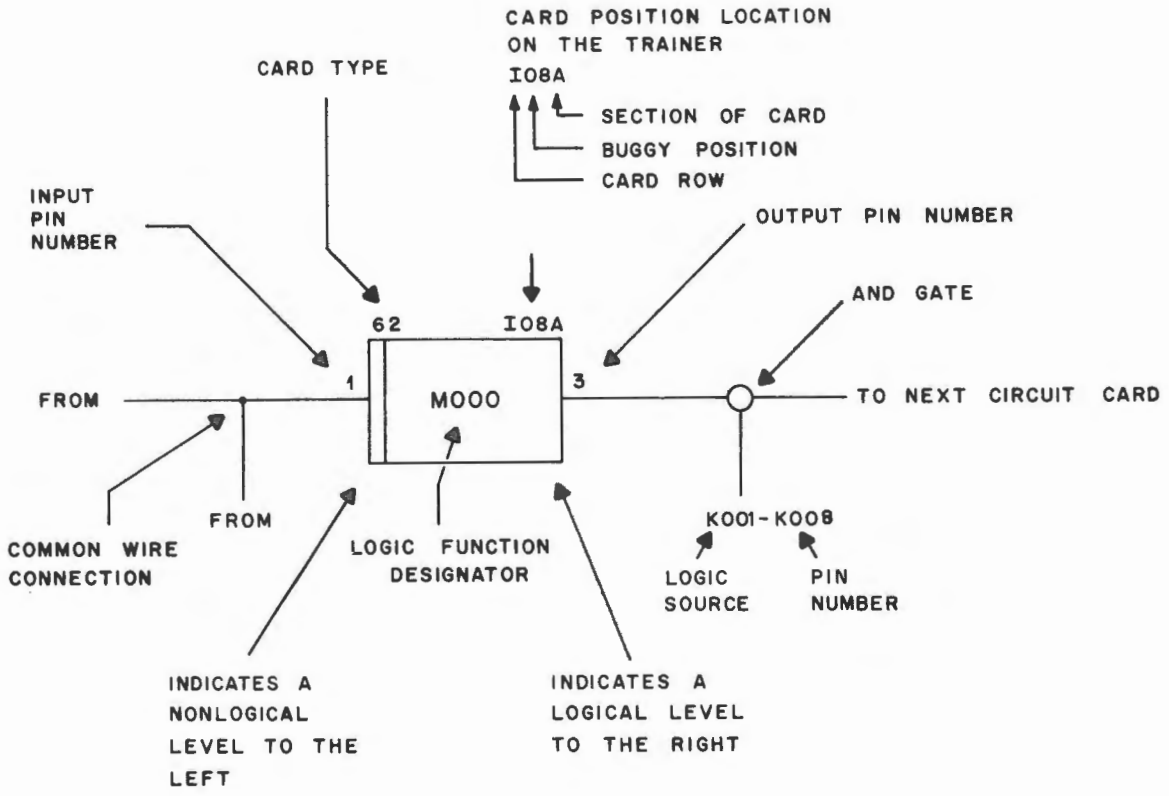
(3) RUN (AUTO) CLOCK FREQUENCY = 25 kHz

(4) STEP (MANUAL) PULSE LENGTH = 0.2 MILLISEC EVEN

= 0.4 MILLISEC ODD

Figure 23. Master Clock

All logic diagrams used throughout the experiments will be designated as shown in figure 24.



Logic Levels	Nonlogic Levels
1604 logical 0 = -0.5 VDC	-20V
1604 logical 1 = -3.0 VDC	0V
3000 logical 0 = -1.1 VDC	0.5V transmission line voltage
3000 logical 1 = -5.8 VDC	

Figure 24. Logic Symbols

USE OF WIRE INSERTION TOOL

The insertion tool is a device designed to insert and remove wire connections in the circuit card connectors. The slotted tip of the tool and the connecting pin on the wire leads are shown in figure 25.

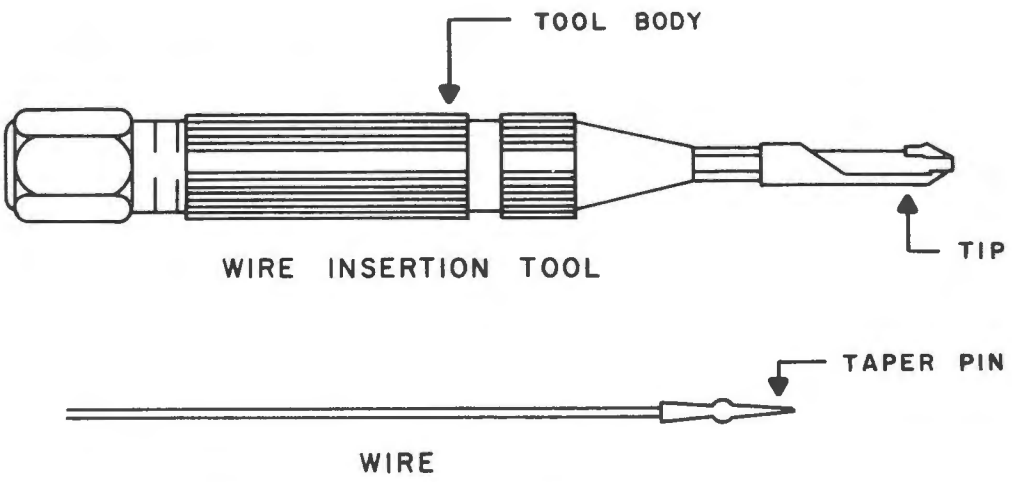


Figure 25. Wire Insertion Tool and Wire

The tip of the insertion tool is spring loaded and requires about 7 to 10 pounds of pressure to overcome the spring tension. Do not force the tip down on any solid object because this will destroy the calibration of the loading spring.

The connecting pins on the wires are inserted into the connecting jacks by first placing the taper pin in the slotted holder in the tip of the insertion tool. Refer to figure 26.

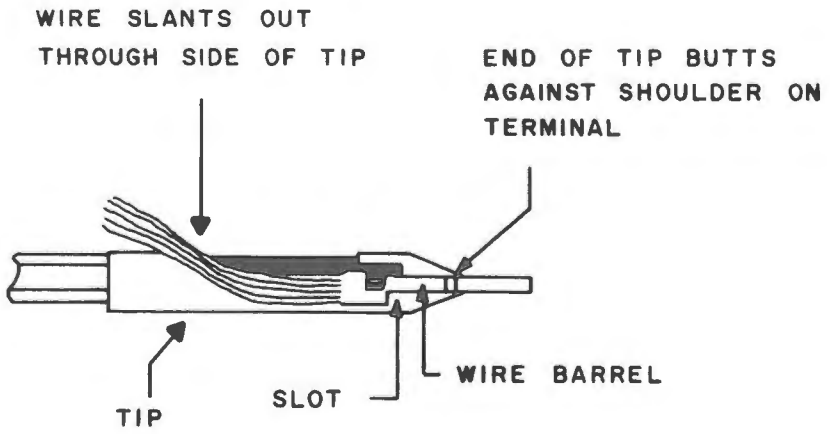


Figure 26. Cutaway View with Wire

Using the insertion tool as a holder, the taper pin is pushed firmly into the connector jack and sufficient pressure is applied to trip the spring mechanism in the insertion tool. This forces the taper pin tightly into place and, if properly done, provides a strong mechanical connection and good electrical connections between the taper pin and connector jack. The insertion tool is removed by pulling it gently to one side and twisting it slightly to free the holder from the taper pin. It is important when inserting the taper pin in the jack to apply pressure evenly and directly above the jack. If this is not done, the taper pin will be bent.

To remove a taper pin from a jack, place the slotted tip of the insertion tool around the barrel of the taper pin as for insertion. Twist the insertion tool about a half turn to the right and, at the same time, pull it directly away from the connector jack.

To practice using the insertion tool and to familiarize yourself with the lamp and switch connections on the trainer, make the following series of connections.

1. Connect a wire from F1 to C1 placing L1 on switch 1.
2. Connect a wire from F2 to C2, etc. until the six lamps are connected to the six switches.
3. Remove wires using the insertion tool taking care not to break or bend the tapered pins.

LABORATORY 3

INVERTERS

OBJECTIVE

Use this experiment to investigate the characteristics and circuit operation of the standard inverter card.

EQUIPMENT

Logic Trainer
Oscilloscope
Logic Trainer Card Box

INTRODUCTION

In the circuit cards that you will be using for these experiments, a logical 1 level is represented by -3 volts and logical 0 level is represented by -0.5 volt.

The inverter circuit negates or complements the logical voltage level that is applied to its input. In other words, if a logical 0 or -0.5 volt is applied to the inverter input, the output level of the circuit will be a logical 1 or -3 volts. The inverter circuit is basically a common-emitter transistor amplifier circuit. In this configuration, the output voltage signal is 180 degrees out of phase with the input voltage signal resulting in a phase inversion of any voltage signal that is applied to it.

In this experiment you will investigate the voltage distribution and operation of the 11A inverter card used in Control Data Corporation computer systems. You will also see how these circuits can be used to control other switching operations or similar circuit actions.

PROCEDURE

VOLTAGE DISTRIBUTION*

Insert an 11A circuit card in buggie I01 on the trainer. Be sure to align the pin numbers on the card with the appropriate pin numbers on the buggie. Turn on the trainer.

Refer to figure 27 and the schematic diagram of the 11A card found in the 1604 Printed Circuits Manual. Set the scope to measure DC voltage. Measure the DC voltages at points A through E in figure 27 and record your readings in the open input column of Table 4. If an 11A card is not available, use an 11 card. Refer to figure 28.

---

*All buggie positions on the trainer are identified by a location number. The buggies are numbered numerically from left to right; i.e., I01, I02, etc.

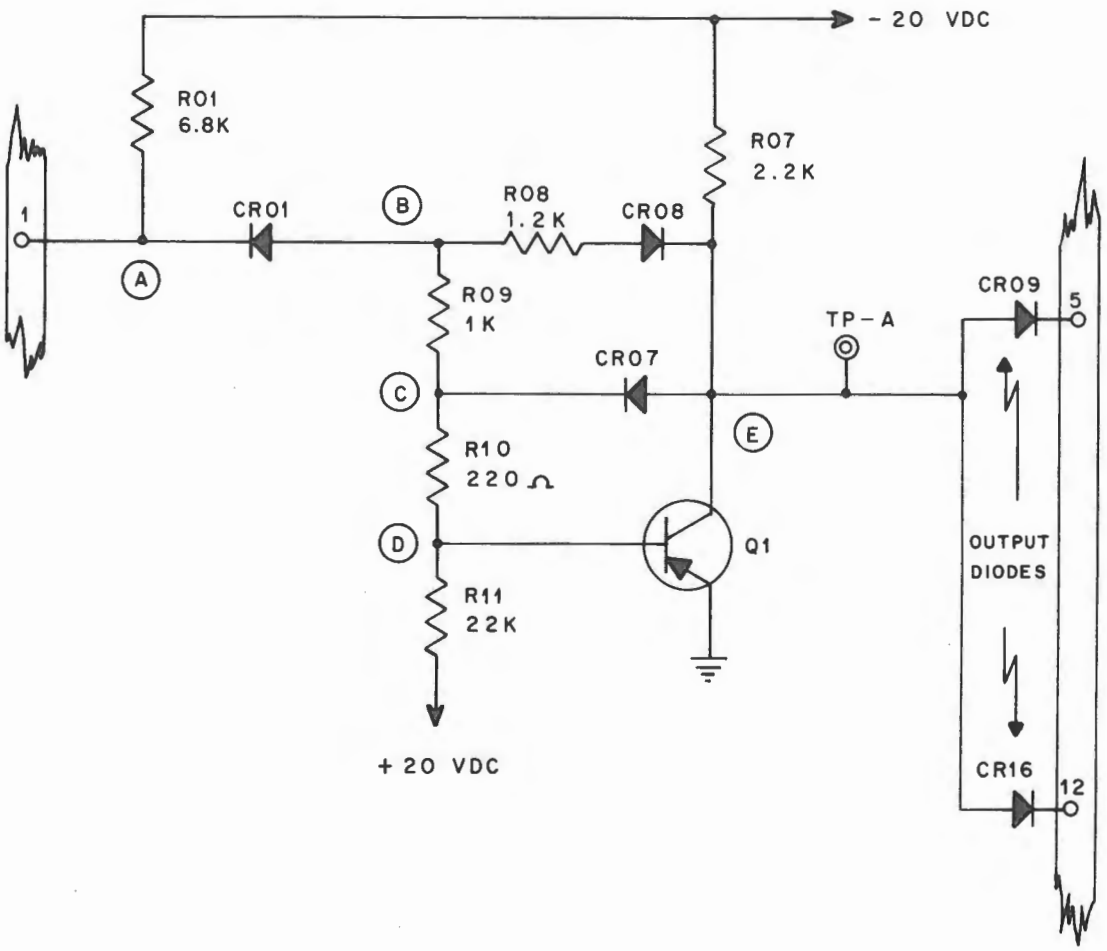


Figure 27. Single Inverter Circuit 11A Card

TABLE 4. 11A CARD

VOLTAGE AT POINT	INPUT OPEN	INPUT GROUNDED
A	-3 — -3	0 -.5
B	-3 —	-1.4
C	-.5 .4	-.4 -.25
D	-1.7 — .2	.8
E	-.5 — .2	-.3 -3

Logical Levels

0 equals -0.5 volt
1 equals -3 volts

CAUTION

Always remove power before connecting wires.

Connect a wire from E1 to I01-1 and from F1 to ground. Press switch 1. This grounds the input to the card. Measure the DC voltages at points A through E in figure 27, and record your readings in the grounded input column of Table 4.

From the results recorded in Table 4, the following conclusions can be drawn.

1. When the switch was released the input voltage at point A was -3 and the output voltage at point E at this time was $-.5$.
2. The logical level represented at the input is 1 and at the output is 0.
3. When the switch was pressed, the input voltage was -5 and the output voltage was -3.
4. The logical level represented at the input under these conditions is 0 and at the output is 1.

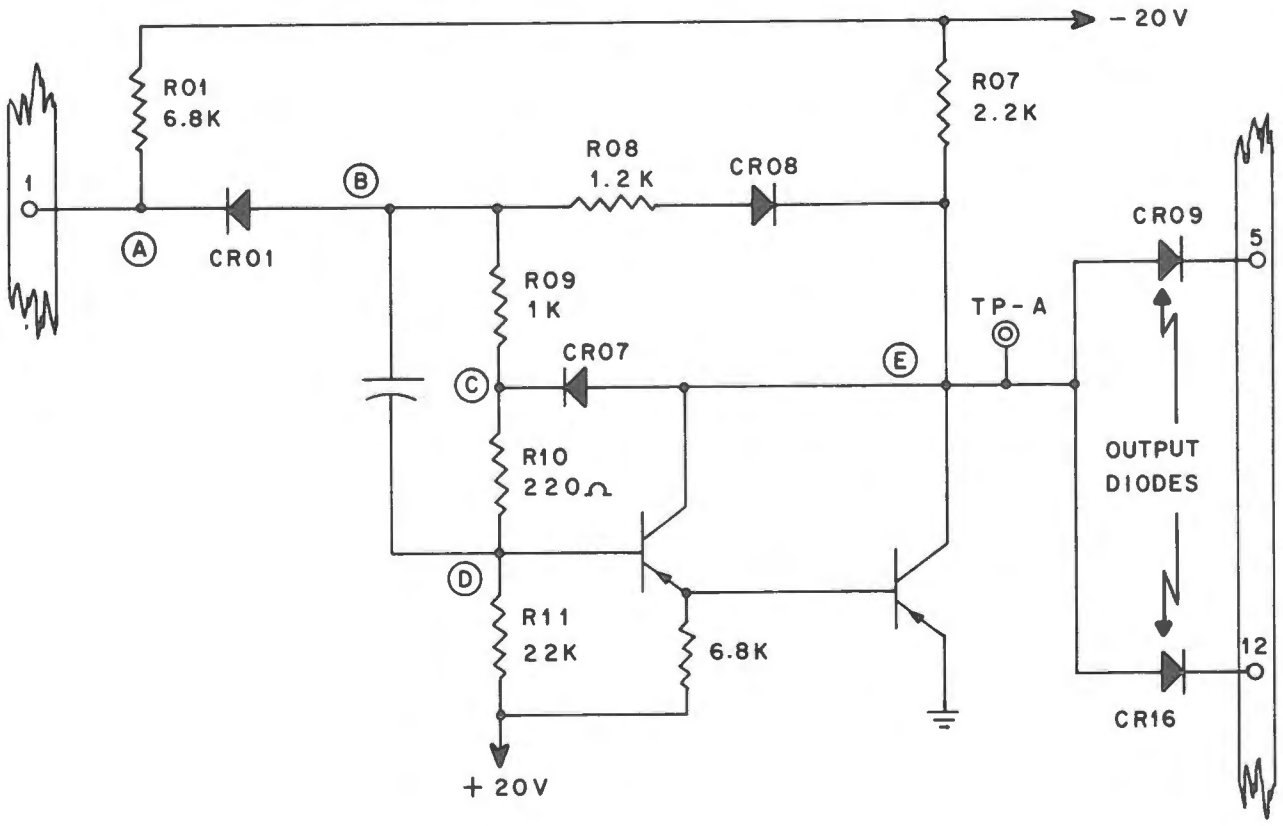


Figure 28. Single Inverter Circuit 11 Card

Insert the light driver card 62 into buggie position I20 and connect a wire from I01-5 to I20-1. Refer to 29. Connect a wire from I20-3 to C1 to complete the wiring shown in figure 29.

NOTE

The light driver circuit is similar to the inverter circuit except that the output voltage change is sufficient to operate one of the lights on the trainer. For example, when the 62 card outputs -20 volts, the lamp remains off because the same voltage potential exists on both sides of the lamp. When the 62 card outputs -0.5 volt, the trainer lamp has 19.5 volts across it and lights.

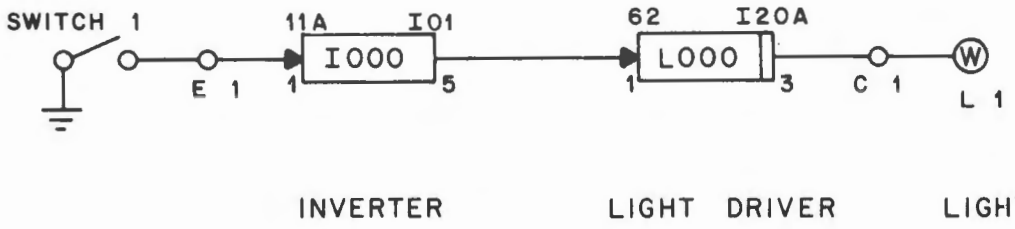


Figure 29. Light Driver

Complete the following statements.

With switch 1 released, measure and record the voltage at I20-1. EI20-1 ____. Lamp 1 is ____. With switch 1 pressed, measure and record the voltage at I20-1. EI20-1 equals ____. Lamp 1 is ____.

From the data you just recorded, the following conclusions can be made. When a logical ____ is present at the input to the 62 card, the lamp is ____. When a logical ____ is present at the input to the 62 card, the lamp is ____. Therefore, the light driver senses the presence of a logical 1 and lights the lamp when this condition exists.

Disconnect the wire from E1 and connect it to D1. This replaces the push-push switch with the Clock Mode switch. With the Clock Mode switch released, measure and record the following voltages and conditions.

EI01-1 equals ____ EI20-3 equals ____
EI20-1 equals ____ Lamp ____

With the Clock Mode switch pressed, measure and record the following voltages and conditions.

EI01-1 equals ____ EI20-3 equals ____
EI20-1 equals ____ Lamp ____

From the data that you recorded, explain the condition of the circuit. ____

Disconnect the wire from D1 and connect it to D2. D2 is one of the even clock outputs. Connect a wire from D4 to the external trigger input of the scope and switch the trigger selector to the external position. Turn the Clock Mode switch to the run position.

Scope the waveform at the input to the inverter card and record its DC voltage levels in figure 30. The condition of the lamp is _____ because _____

_____.

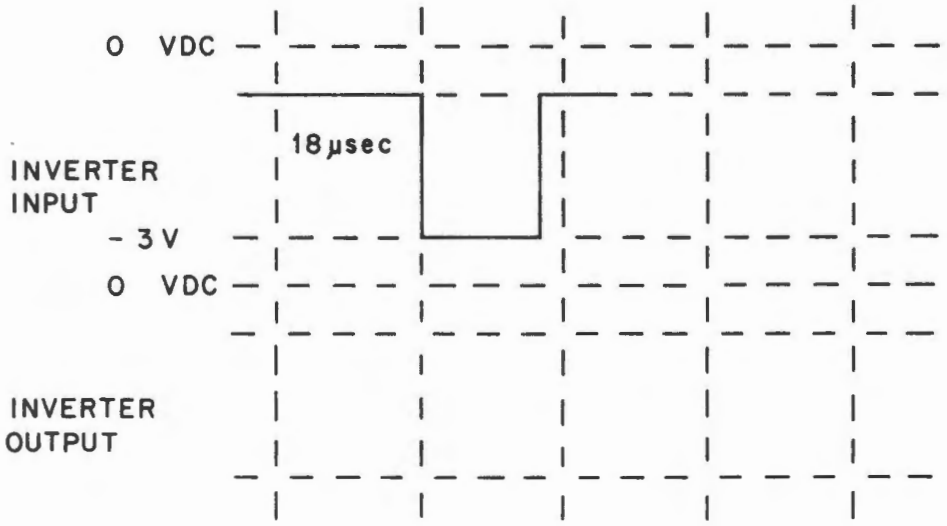


Figure 30. Inverter Output

USE OF MULTIPLE INVERTERS

Build the circuit shown in figure 31. Note card types and locations from the block diagram.

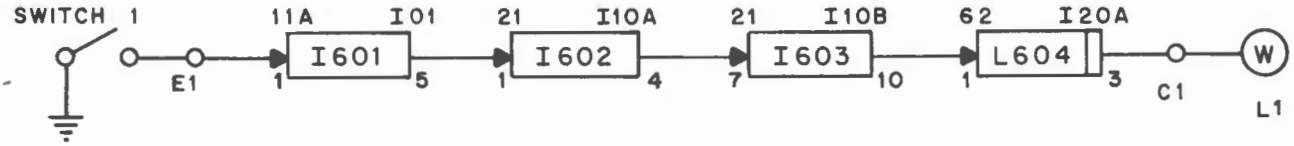


Figure 31. Multiple Inverters

With switch 1 released, measure and record the voltage level at the input to I601. E_{I01-1} equals -3 . The condition of the lamp is off.
Press switch 1, measure, and record the voltage level at the input to I601. E_{I01-1} equals -15 . The condition of the lamp is ON.

Explain the condition of the lamp when the switch is open and closed in terms of the voltage levels at the output of each circuit. SW OPEN LAMP OFF -16VOLTS at output

SW closed Lamp ON 0 VOLTS at output

Turn the power switch on the trainer off and disassemble the circuit.

SUMMARY

1. In the circuit of figure 27, the purpose of CR7 is prevent saturation of Q01.
2. With the input of the inverter open-circuited the voltage level present at the input is -5 VOLTS.
3. The input level exists as specified in question 2 because Q01 forward bias for minimum
4. With the input open-circuited, the state of Q1 is conducting.
5. The output of the inverter circuit must be connected to another card in order to obtain proper output voltage reading because no load exists at output.

LABORATORY 4

FLIP-FLOPS

OBJECTIVE

Use this experiment to investigate the operating characteristics of the flip-flop (31 card) and observe how the circuit can be used to store data.

EQUIPMENT

Logic Trainer
Trainer Card Box
Oscilloscope

INTRODUCTION

You have learned that the flip-flop circuit is basically two inverter circuits on a common card. The output of one inverter is connected back to the input of the other circuit. With this method of interconnection, the circuit remains in one of two steady states until a change is made at the input. One steady state condition is called the set condition, and the other steady state is referred to as the clear condition. The two inputs to the circuit are correspondingly labeled as the set and clear inputs. If a logical 1 pulse is applied to the set input, the circuit will switch to the condition where the set output is equal to a logical 1 level. A logical 1 pulse applied to the clear input causes the circuit to switch to the condition where its clear output is equal to a logical 1 level.

The flip-flop circuit has many applications in computers. It is used in a register as a temporary storage device and as the basis for electronic counting circuits. In this experiment you are to verify the operating characteristics of the flip-flop circuit, as well as the use of one flip-flop to gate the operation of other circuits.

PROCEDURE

BASIC FLIP-FLOP OPERATION

Build the circuit of figure 32. Set the scope to measure DC voltages and then complete Table 5.

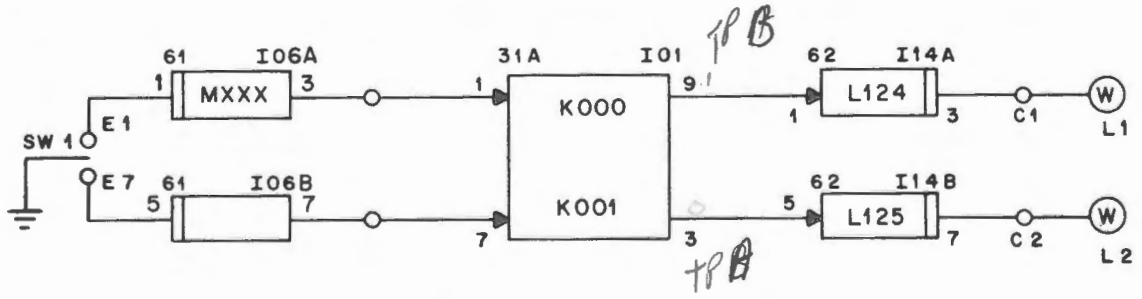


Figure 32. Flip-Flop

TABLE 5. FLIP-FLOP 31A

PIN 9 PIN 3

SWITCH 1 CONDITION	VOLTAGE I01-1	VOLTAGE I01-7	VOLTAGE TP-B	VOLTAGE TP-A	LAMP L1	LAMP L2
RELEASED	~~+6~~ 1	-3.2	~~0~~ -.6	~~+~~ 3	OFF	ON
PRESSED	~~-0~~ -3	-1	~~-0~~ -3	~~-3~~ -.6	ON	OFF

NOTE

Clock Mode switch should be to run position.

From the data recorded in Table 5, the following conclusions can be drawn.

1. When switch 1 is released, the set input to the 31 card is a logical 0, and the clear input is a logical 1. This means the flip-flop is clear. Therefore, the set output TP-B is a logical 0 and the clear output TP-A is a logical 1.
2. When the flip-flop is cleared, L1 is OFF and L2 is ON.
3. When the flip-flop is set, L1 is ON and L2 is OFF.

Modify your circuit of figure 32 to conform to that of figure 33.

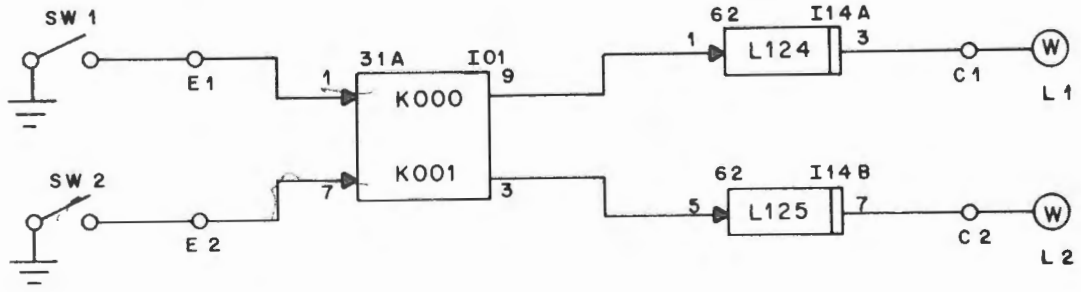


Figure 33. Flip-Flop

Using the scope to measure DC voltages, complete Table 6.

NOTE
Logical 1 = Switch open
Logical 0 = Switch closed

TABLE 6. FLIP-FLOP

SWITCH 1	SWITCH 2	VOLTAGE I01-1	VOLTAGE I01-7	VOLTAGE TP-B	VOLTAGE TP-A	LAMP L1	LAMP L2
0	0	-0	0	-3	-.5	ON	OFF
0	1	0	-3	-.5	-3	OFF	ON
1	0	-3	0	-3	-.5	ON	OFF
1	1	-3	-3	-.5	-.5	OFF	OFF

From the data recorded in Table 6, the following conclusions can be drawn.

1. When both switches are open, both the set and the clear inputs are logical 1. Both the set and clear outputs are logical 0 and both lamps are off. Therefore, when the inputs to the 31 card are left open, it is disabled as a flip flop and acts as a double inverter.
2. When only switch 2 is closed, the flip-flop is set and lamp 1 is on.
3. When only switch 1 is closed, the flip-flop is clear and lamp 2 is on.
4. When both switches are closed, the state of the flip-flops is determined by whichever switch closed last. OK

Disassemble your circuit and proceed to the next step.

FLIP-FLOP AS A GATE CIRCUIT

Build the circuit shown in figure 34.

With SW6 released, open switch 1 and switch 2 and record the conditions of the lamps. L1 equals off and L2 equals off. Using the scope, measure and record the voltages at K000/001, TP-A and TP-B. TP-A equals -.5 and TP-B equals -3. From your recorded data, is the status of K000/001 set or cleared? clear Measure and record the voltages at TP-A and TP-B of K010/011. TP-A equals -.5 and TP-B equals -.5. From your recorded data, K010/011 must be acting as a double inverter. Depressing SW6 has what effect on the circuit? NONE

What effect does it have on the lamps? NONE

K000
K001

With SW6 released, close switch 1 and open switch 2 and record the conditions of the lamps. L1 equals off and L2 equals on. Measure and record the voltages at TP-A and TP-B of K000/001. TP-A equals −.5 and TP-B equals −3. Measure and record the voltages at TP-A and TP-B of K010/011. TP-A equals −.5 and TP-B equals −3. From your recorded data, K000/001 is clear and K010/011 is clear. Pressing SW6 has what effect on the circuit? Causes flip-flop to set

What effect does it have on the lamps? turns L2 off

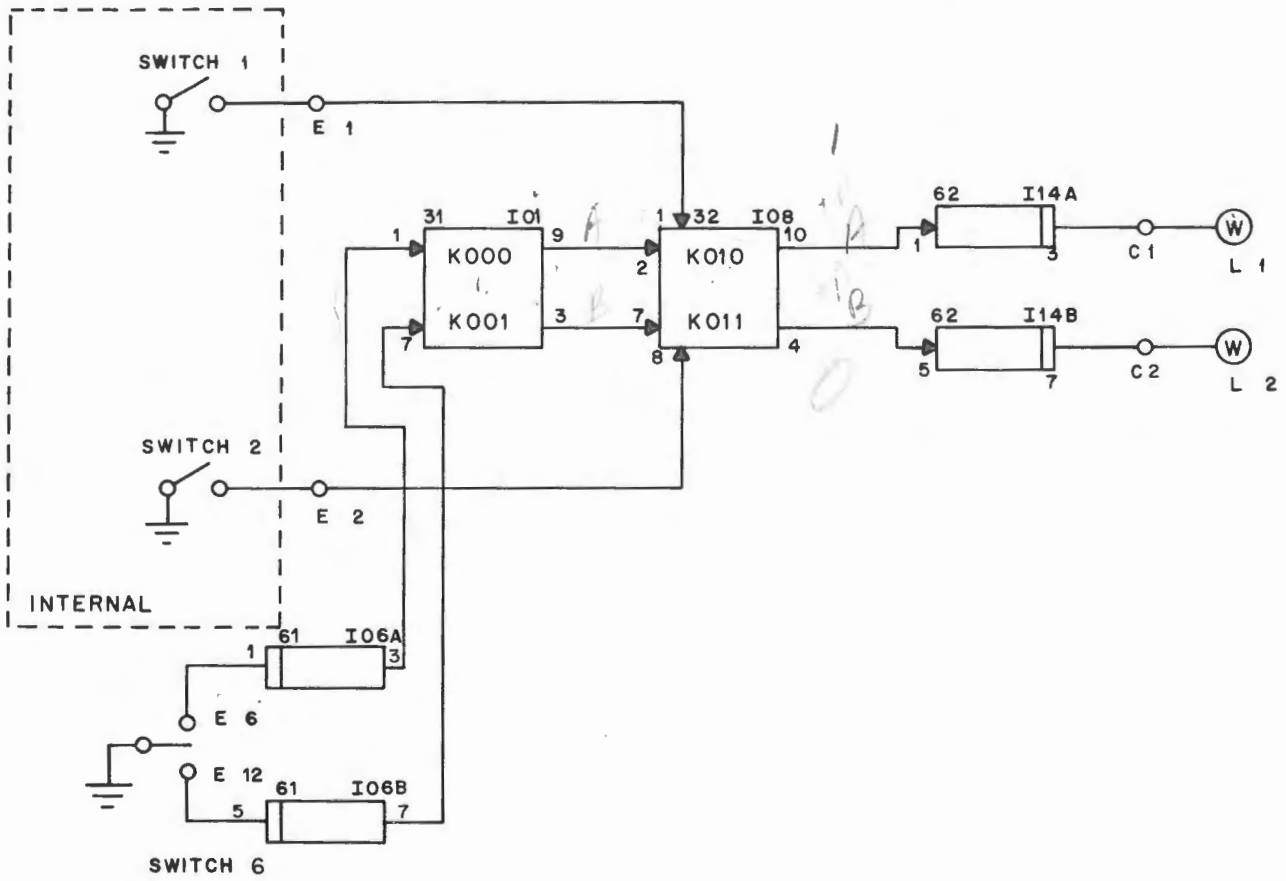


Figure 34. Flip-Flop as Gate Circuit

With SW6 released, close switch 2 and open switch 1 and record the condition of the lamps. L1 equals off and L2 equals off. Measure and record the voltages of TP-A and TP-B of K000/001. TP-A equals −. and TP-B equals −3. From your recorded data, K000/001 is cleared and K010/011 is acting as a [illegible]. Depressing SW6 has what effect on the circuit? Causes output of flip-flop to set

What effect does it have on the conditions of the lamps? [illegible]

With the SW6 released, close switch 1 and switch 2. Record the lamp conditions. L1 equals off and L2 equals on. With the scope, measure and record the voltages at K000/001 TP-A and TP-B. TP-A equals −.5 and TP-B equals ~3. Measure the voltages of K010/011 TP-A and TP-B. TP-A equals −.5 and TP-B equals −3. From your recorded data, K000/001 is clear and K010/011 is opposite. Depressing SW6 has what effect on the circuit? clears to set state

What effect does it have on the lamps? L2 off and L1 on

Disassemble your circuit.

SUMMARY

1. The flip-flop is referred to as a bistable device because it has 2 states (and limbo) set & clear.

2. The 31 card is composed of what basic type of logic circuit? flip flop

3. Label the set and clear inputs and the outputs in figure 35.

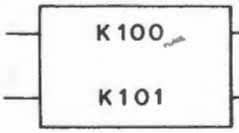


Figure 35. Set and Clear Inputs

4. What test point on a 31 card is the clear output? TP A PIN 3-6
   At what pin numbers can a set output be obtained? TP B 8-12

5. When both inputs to the flip-flop are left open, the outputs are in limbo.

6. The basic difference between a 31 card and a 32 card is 32 has more inputs.

LABORATORY 5

INPUT/OUTPUT CARDS

OBJECTIVES

This experiment will help familiarize the student with the operation and function of the input/output cards used in a digital computer system.

EQUIPMENT

Logic Trainer
Trainer Card Box
Oscilloscope

INTRODUCTION

While studying the support material for the previous day, you learned that input/output cards are used in the conversion of logic voltage into nonlogic voltages and vice versa. In this experiment you will analyze circuits and find out how these voltage levels are produced and give them a numerical value. You will also see how these circuits are used in conjunction with indicator lights and toggle switches.

PROCEDURE

OUTPUT CARD 62 CHARACTERISTICS

Build the circuit shown in figure 36.

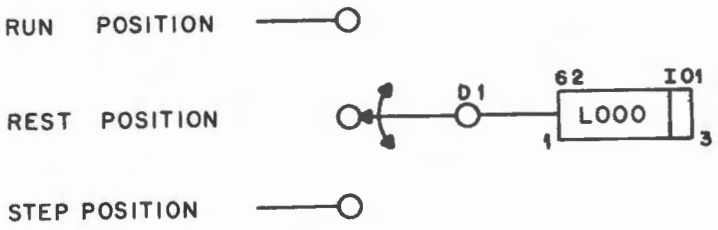


Figure 36. Clock Mode Switch

When the clock mode switch is in the step position, it will output a 1 from even clock pins and a 0 from odd clock pins. When released from the step position, it automatically returns to the rest position. Even clock pins output a 0 and odd clock pins output a 1. When the switch is in the run position, however, it outputs continuous pulses. The waveforms on the even and odd clock pins are 180 degrees out of phase. It will not return to the rest position from the run position unless it is reset to the rest position. Measure and record the waveform observed on the scope in Table 7.

TABLE 7. CLOCK MODE SWITCH

CLOCK MODE SWITCH	INPUT TO 62 CARD	OUTPUT FROM 62 CARD
STEP	-3	0
REST	0	0 -16

Do not disassemble your circuit. Proceed to next step.

USE OF THE L CARD AS A LIGHT DRIVER

Refer to the circuit of figure 37. With the Clock Mode switch in the released position, a logical 0 is present at the input to the L card. The output of the L card will be a nonlogic voltage level of -16 volts. Since the card output and the 20-volts power supply are in series opposition, only 4 volts remain to be dropped across the lamp which is insufficient to light the lamp. When the Clock Mode switch is pressed, the output of the L card is approximately 0 volts which leaves the full 20 volts to be dropped across the lamp. This lights the lamp. To verify this theory, add the necessary wire to modify your existing circuit to match that shown in figure 37.

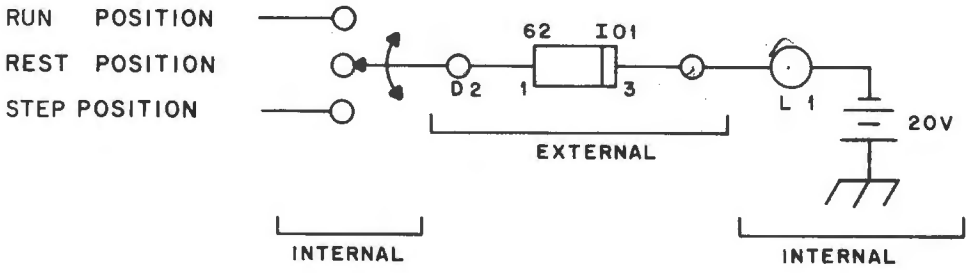


Figure 37. L Card as a Light Driver

Using the scope as a DC voltmeter, measure the voltages at the points specified by Table 8.

TABLE 8. L CARD

CLOCK MODE SWITCH	INPUT TO 62 CARD	OUTPUT OF 62 CARD TP-A	LAMP CONDITION
RUN	[illegible]	−6 to 0 [illegible]	ON (DIM)
REST	−3	0	ON

From the data recorded in Table 8, the following conclusions can be made.

1. With an input of -0.5 volt or logical 0, the output of the 62 card is a nonlogical −16 volts.
2. With an input of -3 volts or logical 1, the output of the 62 card is a nonlogical 0 volts.
3. The lamp will be ON whenever a logical 1 appears at the input to the 62 card.
4. Therefore, when the 62 card is used as a light driver, it will sense the presence of a logical 1, and light the lamp.

Open the input to the 62 card by disconnecting the wire from I01-1 and record the condition of the lamp: ON. When the input is open, a logical 1 is present.

M CARD CHARACTERISTICS

Build the circuit shown in figure 38. The purpose of this portion of the experiment is to verify the theory of M-card operation.

Use the scope as a DC voltmeter to complete Table 9. Measure the 61 card in 107.

NOTE

When measuring the output of the M card, always use the test point.

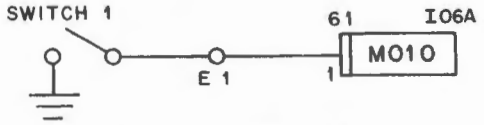


Figure 38. M Card

TABLE 9. L AND M CARDS

SWITCH 1 CONDITION	INPUT TO 61 CARD	OUTPUT FROM 61 CARD TP-A
open ON	−16 VOLTS	0 VOLTS, LOGICAL 0
closed OFF	0 VOLTS	−3 VOLTS, LOGICAL 1

From the data recorded in Table 9 complete the following statements.

1. When the input to the 61 card is -16 volts, the output is a logical 0.
2. When the input to the 61 card is 0 volts, the output is a logical 1.

Therefore, the M or 61 card converts nonlogical voltage levels to logical voltage levels. When the input is -16 volts, the output is a logical 0. When the input is ground or 0 volts, the output is a logical 1.

USE OF THE M OR 61 CARD AS A NONLOGIC-TO-LOGIC CONVERTER

Build the circuit shown in figure 39.

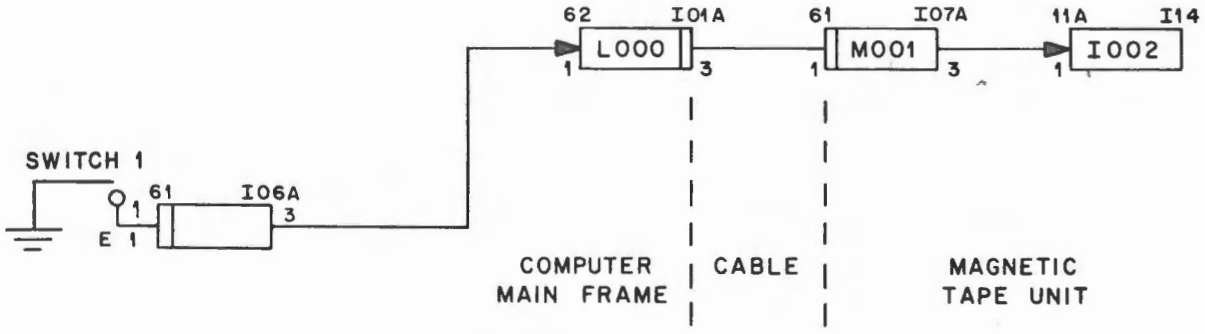


Figure 39. L and M Cards

Using the scope as a DC voltmeter, complete Table 10. Measure the 61 card in 106.

TABLE 10. M CARD

SWITCH CONDITION	INPUT TO 61 CARD	OUTPUT FROM 61 CARD TP-A
OPEN	-16 VOLTS	-.5 VOLTS, LOGICAL 0
CLOSED	0 VOLTS	-3 VOLTS, LOGICAL 1

Using the data recorded in Table 10, complete the following statements.

1. When the switch is open, the output of the 61 card will be a logical 0.
2. When the switch is closed, the output of the 61 card will be a logical 1.

Therefore, the 61 card will deliver a logical 1 whenever the switch is closed converting switch position to logic data.

Disassemble your circuit and proceed to the summary.

SUMMARY

1. I/O cards are needed in the computer because compensate for voltage loss in cable (they raise and lower voltages) (logic to non logic & back).
2. The letter designations normally assigned to 61 and 62 cards are M-61 L-62.
3. True/False. The 61 and 62 cards function as logic inverters.
4. If the input of a 62 card is left open, the output will be -16 volts. This is a logic/nonlogic level. (Circle one.)
5. When the input to a 61 card is left open, the output will be -3 volts or a logical 1.
6. In the logic block shown in figure 40, the switch will be open/closed (circle one) to cause the lamp to light.
7. The card type used as a light driver is the L101.

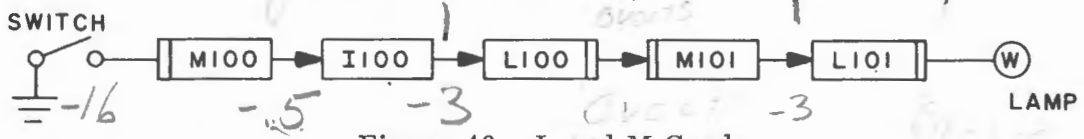


Figure 40. L and M Cards

LABORATORY 6

REGISTERS

OBJECTIVE

This experiment should familiarize the student with the operation of a basic three-stage register.

EQUIPMENT

Logic Trainer
Oscilloscope
Trainer Card Box

INTRODUCTION

In this experiment, you will build a three-stage register. Three numbered push-push switches combined with 61 cards provide the input data, another push-push switch provides the Master Clear, and a fifth push-push switch provides an enable or transfer pulse. The contents of the register will be sensed by a 62 card and by three lamps.

PROCEDURE

Build the circuit in figure 41. You will note in the diagram that one term feeding the AND gate is not completed by a line on the diagram. However, a destination note is recorded. Many of the experiments that follow also do this.

When wiring is complete, proceed as follows:

Open the three input data push-push switches, and press the Master Clear switch. It is necessary to clear the register at this point because this is a ones transfer reg.

Enter number 101_2 by closing switch 1 and switch 3. Using the scope, measure and record the output of test points M400, M401, and M402. M400 equals -3, M401 equals -.5, and M402 equals -3.

Do the voltage levels measured denote the presence of 101_2 at the input to the AND gates? YES The condition of the three lamps is ON OFF ON.

Press and release the Transfer switch and note the condition of the three lamps. UNCHANGED.

Do the lamps indicate the proper contents of the register? YES

At this time, a 101_2 should be present in the register. Press switches 1, 2, and 3 in turn. The switches do not affect the contents of the register because transfer pulse not applied.

Press the Master Clear switch and enter a 011_2 using switches 1, 2, and 3. Push the Transfer switch and check to see that the lamps indicate the presence of a 011_2. Repeat this procedure for eight combinations of the input switches.

Disassemble the circuit.

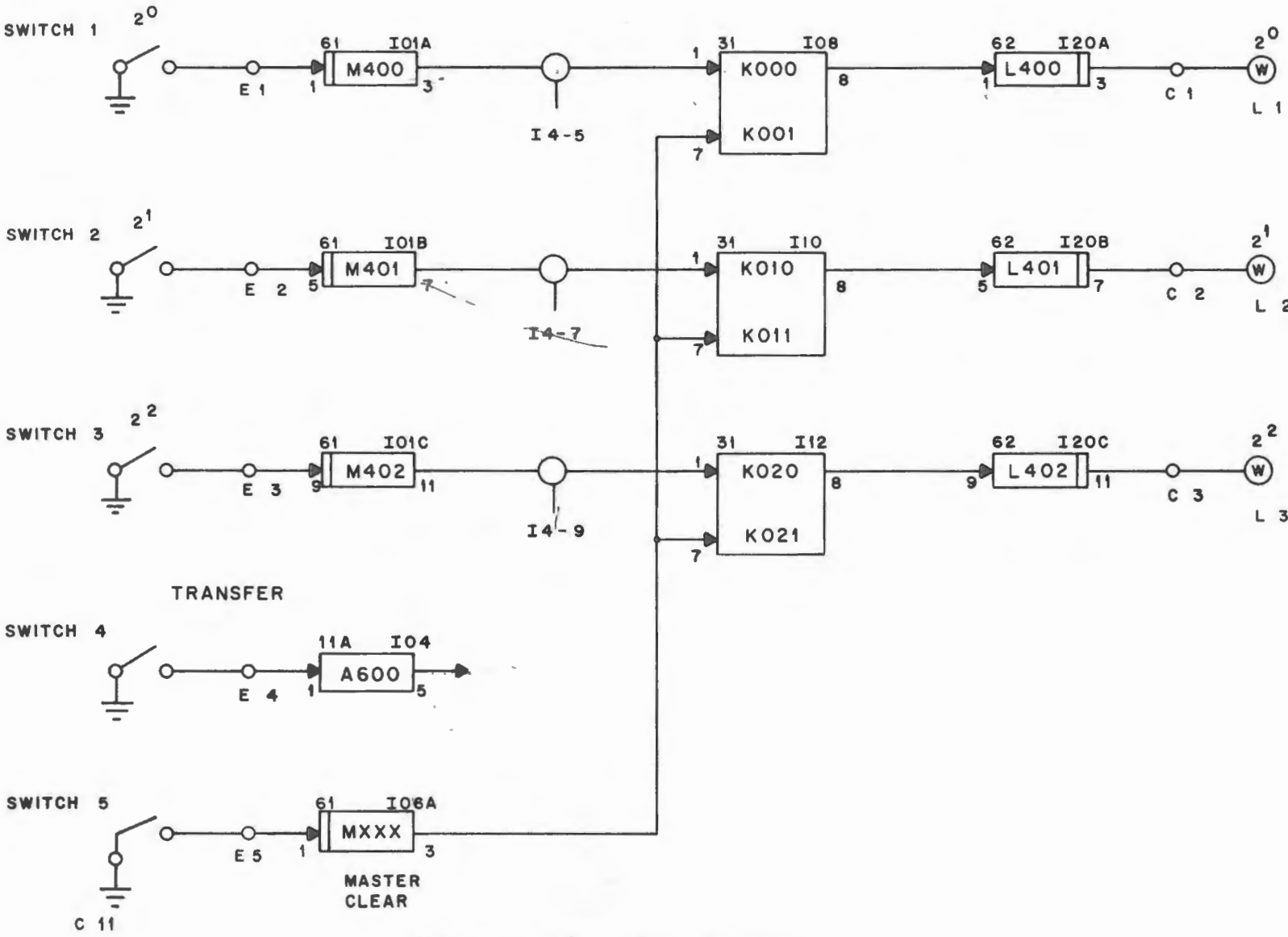


Figure 41. Three-State Register

SUMMARY

1. A register is temporary data storage point.
2. The function of the Master Clear is clear BANK II.
3. The function of the enable or transfer pulse is transfer binary (ones and (zeros).
4. The condition of flip-flops that is demanded before a lamp is turned on is set.
5. New input data is prevented from affecting the status of the register until desired by the transfer pulse.

LABORATORY 7

BINARY COUNTER

OBJECTIVE

This experiment should familiarize the student with the operation and construction details of binary counter.

EQUIPMENT

Logic Trainer
Oscilloscope
Trainer Card Box

INTRODUCTION

In this experiment the student is to build a three-stage, double-rank binary counter. Lamps 1 through 3 will be used to indicate the contents of rank I and lamps 4 through 6 will indicate the contents of rank II. Switches 1 and 2 will be used as the advance and transfer switches. An advance/transfer sequence must be followed to cause the counter to step through its eight possible states. Check off wire connections as you proceed so none of the wires are omitted.

PROCEDURE

Build the circuit as shown in figure 42 using the same colored wires and inserting only the cards shown in the figure. At this point, you should have a single-stage, double-rank counter which has only two possible states in each rank. To check out your circuit at this point, proceed as follows.

1. Check the conditions of L4 and L1.
2. Press the transfer switch, switch 2; L4 should be the same as L1.
3. Press the advance switch, switch 1; L1 should change states.
4. Press the transfer switch, switch 2; L4 should be the same as L1.
5. Step through several of these sequences to be sure the counter is working. If operation is normal, add stage 2 as in figure 43. If operation is abnormal, call your instructor or troubleshoot the circuit yourself.

Turn the trainer off and build the stage 2 portion of figure 43. After the wiring is completed, insert the proper logic cards in the positions indicated in figure 43. Turn the trainer on.

Figure 42. Binary Counter, Stage 1

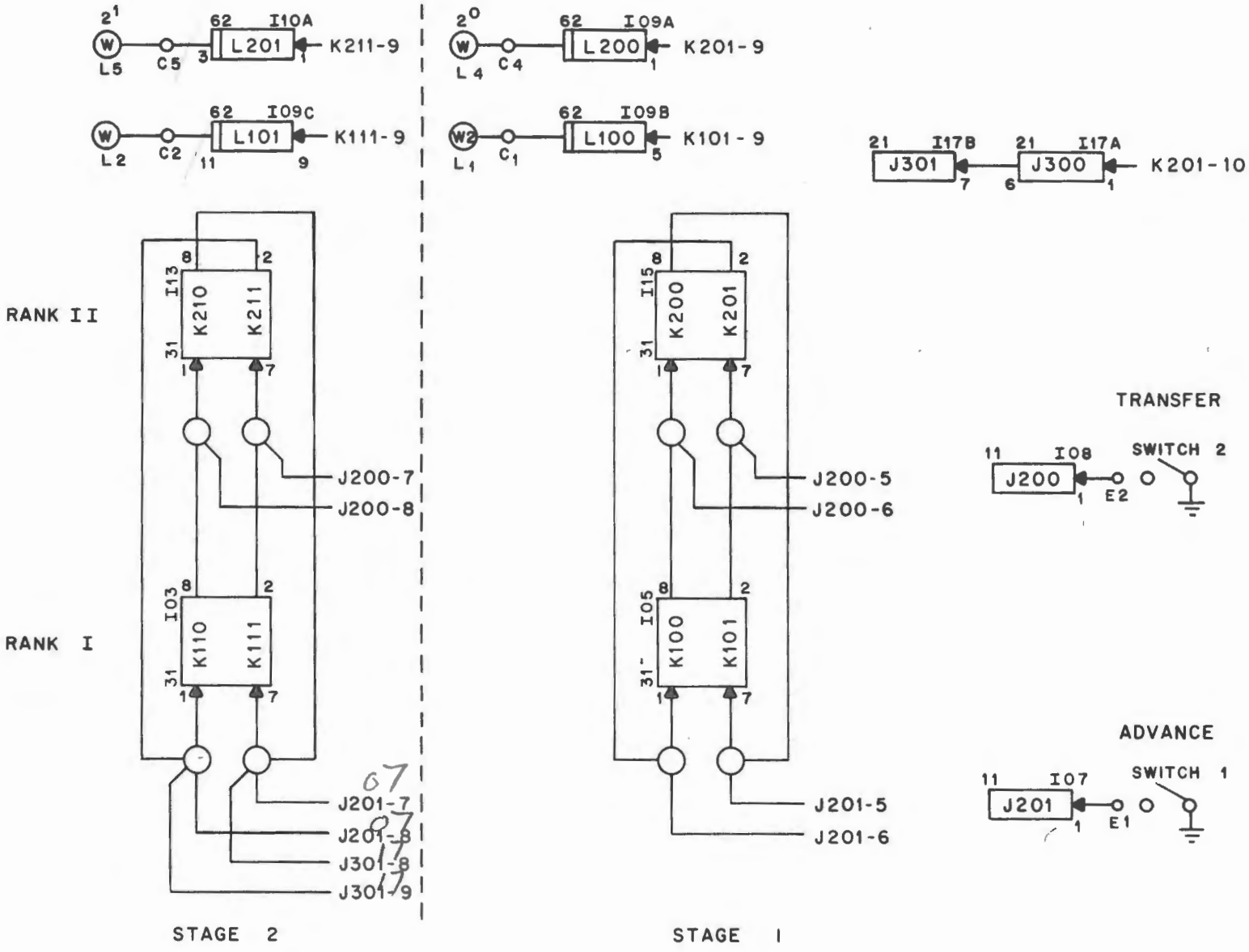


Figure 43. Binary Counter, Stages 1 and 2

At this point, you should have a two-stage, double-rank counter with four possible states. Press the transfer switch and check lamps 5 and 4 to see that they are in the same state as lamps 2 and 1. If so, press the advance switch and then the transfer switch until each of the four states is obtained. If operation is abnormal, call your instructor or troubleshoot the counter yourself. If operation is normal, turn the trainer off and add stage 3 as indicated in figure 44. After wiring is completed, insert the proper cards in the locations indicated by figure 44. Turn the trainer on.

At this point, you should have a three-stage, double-rank counter capable of eight unique states. To check its operation, press the advance and transfer switches until each of the eight states is obtained. Each stage should be displayed as a binary count from 000 to 111. If operation is normal, proceed to the following step. If operation is abnormal, call your instructor or troubleshoot the counter yourself.

After your circuit is completed and operating correctly and you have checked out its operating sequence, have your laboratory partner insert malfunctions. Take turns until you are sure you understand the troubleshooting technique demanded with the 1604 logic circuits.

Disassemble your circuit.

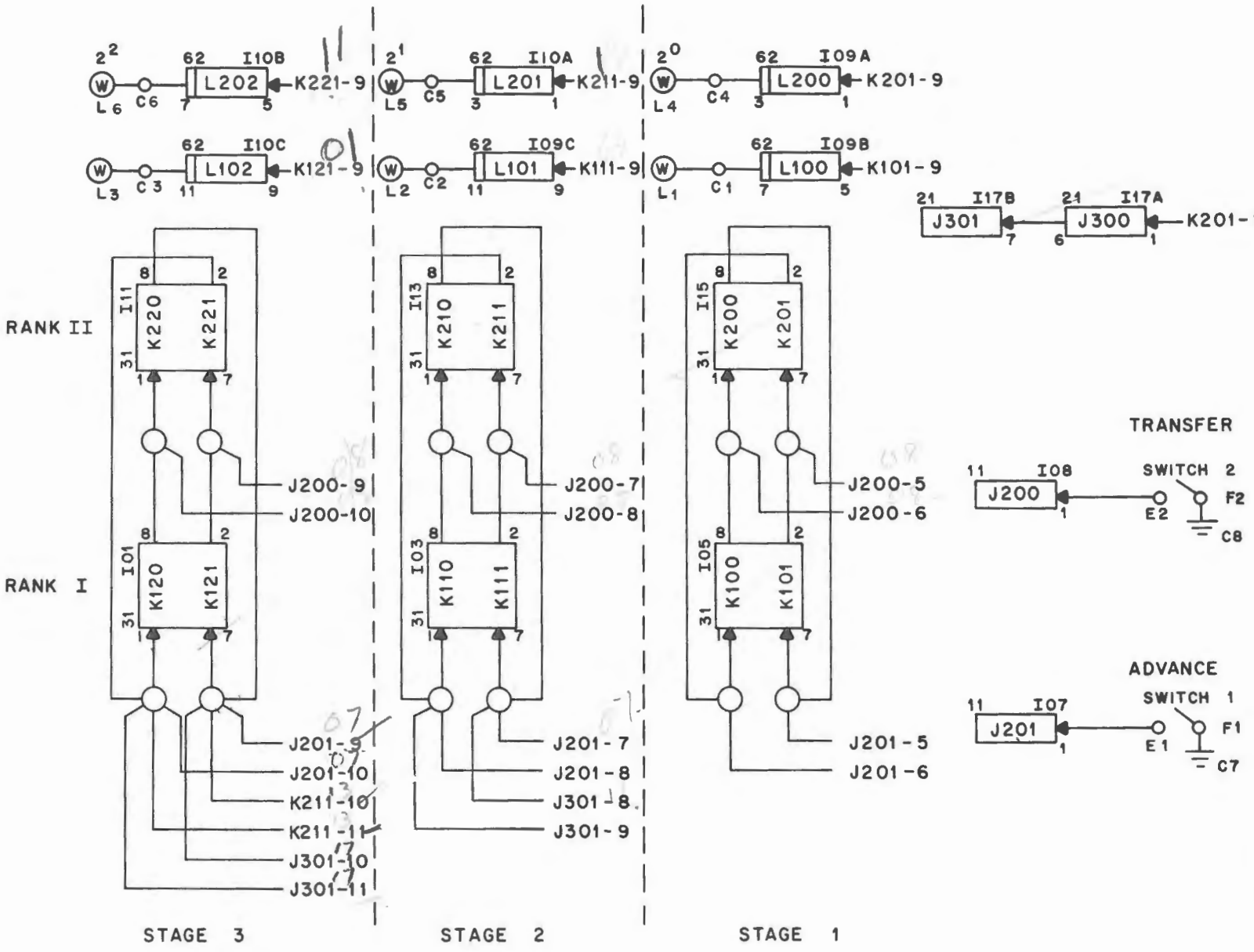


Figure 44. Binary Counter, Stages 1, 2, and 3

LABORATORY 8

SHIFT NETWORKS

OBJECTIVE

This experiment should help familiarize you with the operation and construction of a double-rank shift register.

EQUIPMENT

Logic Trainer
Oscilloscope
Trainer Card Box

INTRODUCTION

This experiment consists of five parts. First you will build an edge network which delivers a single logical 1 pulse when the Step switch (switch 2) is released. Next you will build the pulse generator necessary to produce a four-pulse timed sequence. Then you will build the basic three-stage, double-rank register. In the fourth and fifth parts you will perform necessary modifications to produce the right and left shifts. Lamps 4, 5, and 6 will be used to indicate the contents of the register. Switches 4, 5, and 6 will be used to supply the input data and switch 1 will be the Master Clear.

PROCEDURE

EDGE NETWORK

Build the circuit shown in figure 45. Insert the cards in the positions indicated by figure 45 and turn on the trainer. To check out the leading-edge network, proceed as follows:

1. Switch the time per cm of the scope to 100 ms per cm and connect the scope to A001, TP-B.
2. As the Step switch is pressed and released, a logical 1 pulse should appear. (This may show up as a bright dot at -3 volts on the scope.)

Press and release the Step switch several times and watch for the logical 1 pulse. If the leading-edge network is operating normally, proceed to the next part. If operation is abnormal, troubleshoot or call your instructor.

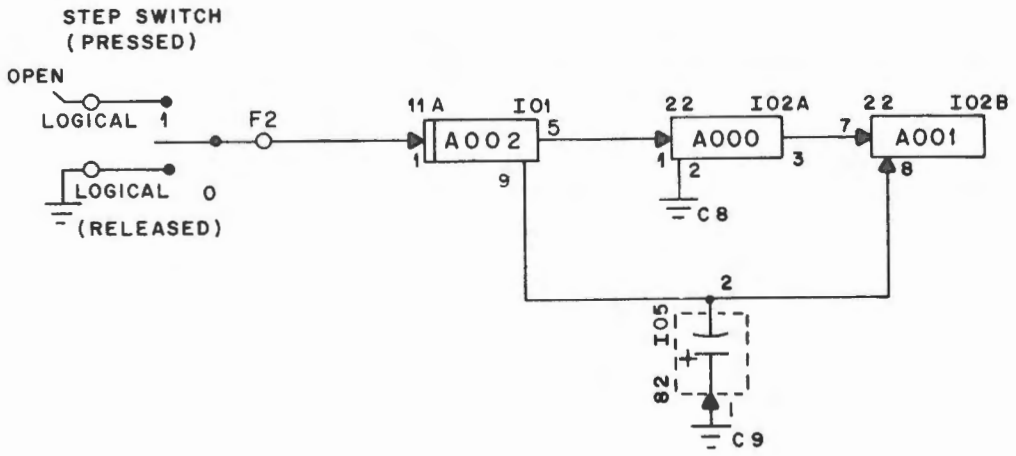


Figure 45. Leading-Edge Network

TIMING-CHAIN GENERATOR

Build the circuit shown in figures 46 and 47. Insert the cards and turn on the trainer. To check out the timing-chain pulse generator and translator, proceed as follows:

1. Set the scope time per cm to 100 ms per cm and connect the scope to I110, TP-A. The DC voltage at TP-A should be -3 volts at this time.
2. Press and release the Step switch; a logical 0 pulse should appear at TP-A.
3. Connect the scope to I111, TP-B. The DC voltage should be -0.5 volt at this time. Press and release the Step switch. A logical 1 pulse should appear.
4. Connect the scope to I112, TP-A. The DC voltage should be -0.5 volt at this time. Press and release the Step switch. A logical 1 pulse should appear.
5. Connect the scope to I113, TP-B. The DC voltage should be -0.5 volt at this time. Press and release the Step switch. A logical 1 pulse should appear.

If the timing-chain pulse generator and translator are operating normally, begin building the circuit shown in figure 48. If operation is abnormal, troubleshoot or call your instructor.

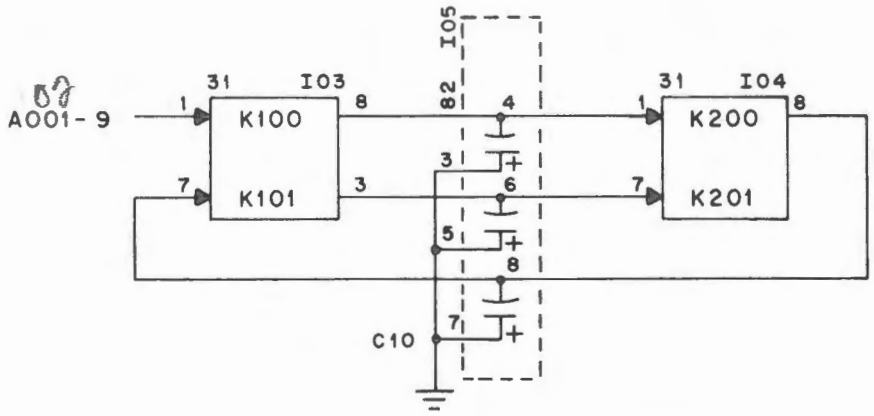


Figure 46. Timing-Chain Pulse Generator

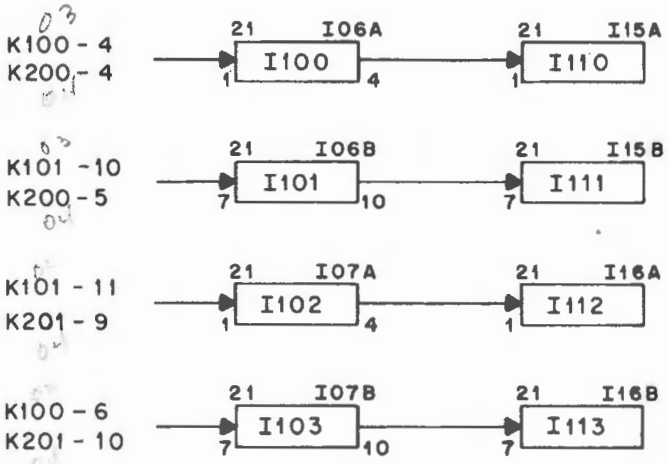


Figure 47. AND Gate Translator

THREE-STAGE, DOUBLE-RANK REGISTER

Build the circuit shown in figure 48, insert the cards, and turn on the trainer. At this point, your circuit is not complete as a shift network, but it should perform the following operations.

1. The Master Clear should clear all lamps.
2. Using switches 4, 5, and 6, you should be able to enter any binary number into the register. Press and release the Master Clear after each entry.
3. Enter an octal 7 into the register using switches 4, 5, and 6. Then press and release the Step switch; the register should clear (all lamps out).

If all of the above operations are normal, proceed to the next operation. If operation is abnormal, troubleshoot or call your instructor.

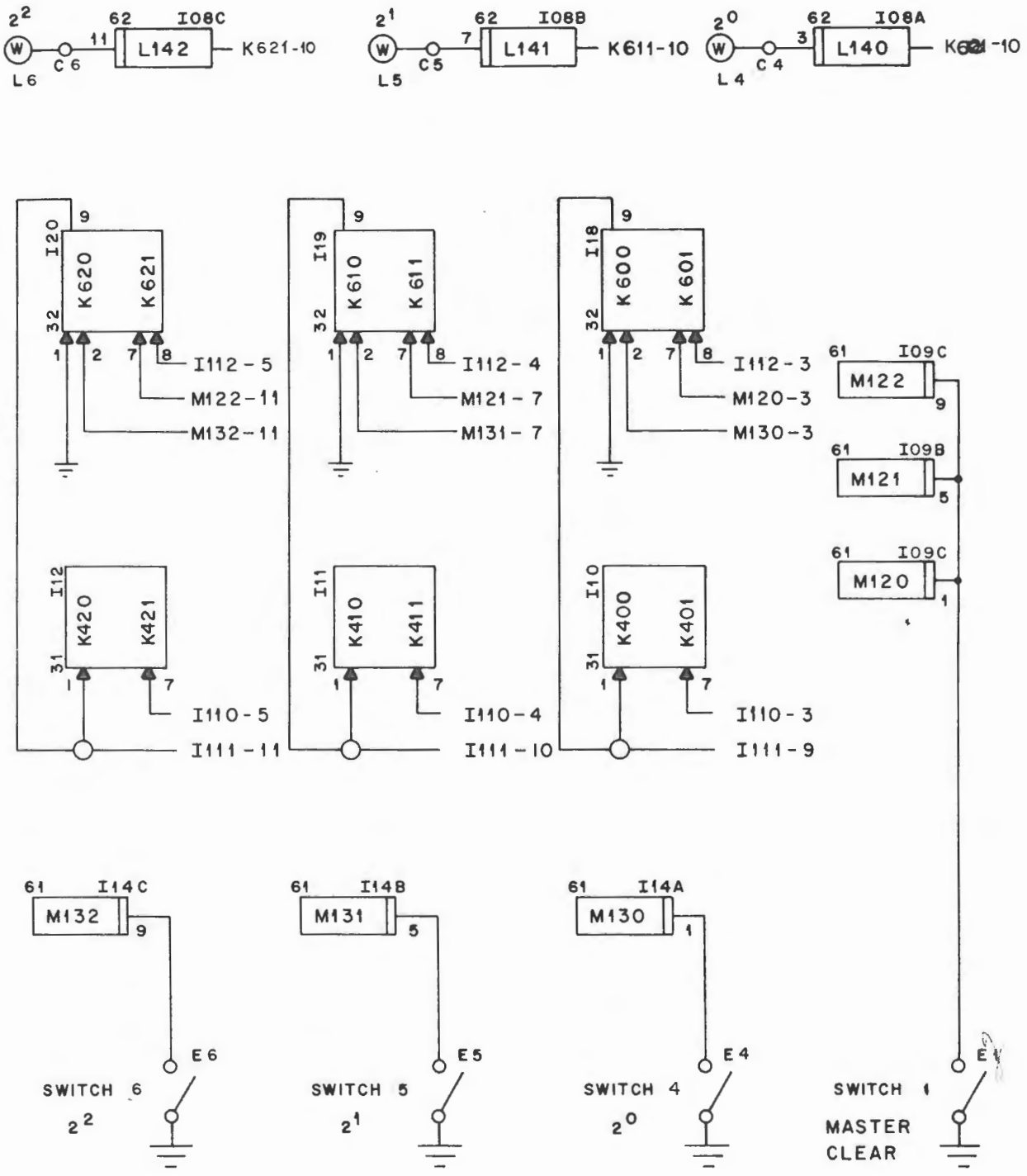


Figure 48. Three-Stage, Double-Rank Register

RIGHT-SHIFT NETWORK

Remove the grounds from pin 1 of K610 and pin 1 of K600, and add the wires shown in figure 49. At this point, you should have a right-shift network. To check its operation, proceed as follows.

1. Press the Master Clear and enter 100_2 into the register.
2. Press and release the Step switch and notice the shift to the right. A 010_2 should now be displayed.
3. Press and release the Step switch again and note a right shift again. A 001_2 should now be displayed.
4. Press and release the Step switch again and note the right shift end-off. A 000_2 should now be displayed.
5. Enter various binary numbers and do a right shift until you are satisfied with the operation of the circuit.

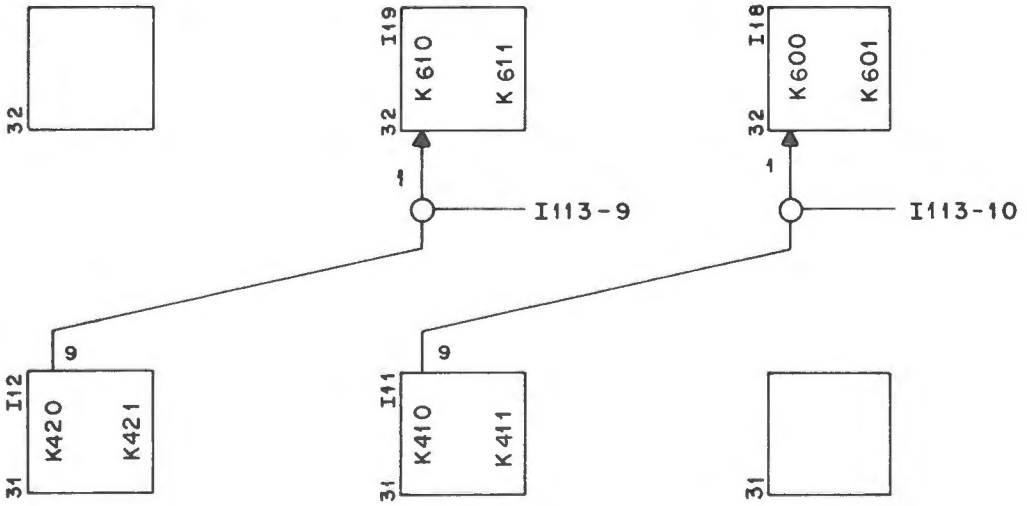


Figure 49. Right-Shift Network

LEFT-SHIFT NETWORK

Remove the ground from pin 1 of ~~K220~~ K620 and the wires added when you built the right-shift network. Make the circuit conform to figure 50. You should now have a left-shift end-around-carry network. To check its operation, proceed as follows:

1. Press and release the Master Clear and then enter 001_2. Press and release the Step switch and note the left shift of one position. A 010_2 should now be displayed.
2. Press and release the Step switch again and note the left shift. A 100_2 should now be displayed.

3. Press and release the Step switch again and note the end-around-carry. A 001_2 should now be displayed.

4. Enter various binary combinations and perform the left-shift operation until you are satisfied with the operation of the circuit. Dismantle your circuit.

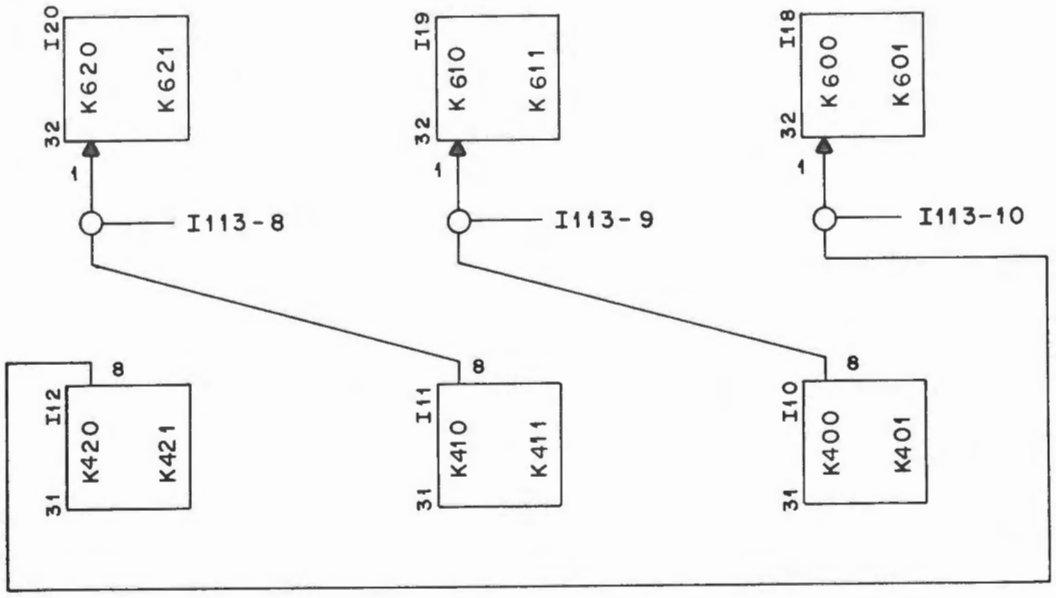


Figure 50. Left-Shift Network

SUMMARY

1. Why was the pulsing network necessary? _____

_____

2. Could the shift be accomplished without timing? _____

3. For a left shift, end-around, if the number 4 was placed in the register, how many shifts would be required in order that the register be cleared? _____

4. For a right shift, end-off, with the conditions given in question 3, how many shifts would be required to clear the register? _____

LABORATORY 9

ADDERS

OBJECTIVE

This experiment should familiarize you with the necessary design consideration in building an adder.

EQUIPMENT

Logic Trainer
Oscilloscope
Trainer Card Box

INTRODUCTION

This experiment consists of two parts. In the first part, you will build a half-adder or exclusive OR circuit. In the second part, you will build a full-adder.

PROCEDURE

HALF-ADDER OR EXCLUSIVE OR GATE

Build the circuit shown in figure 51.

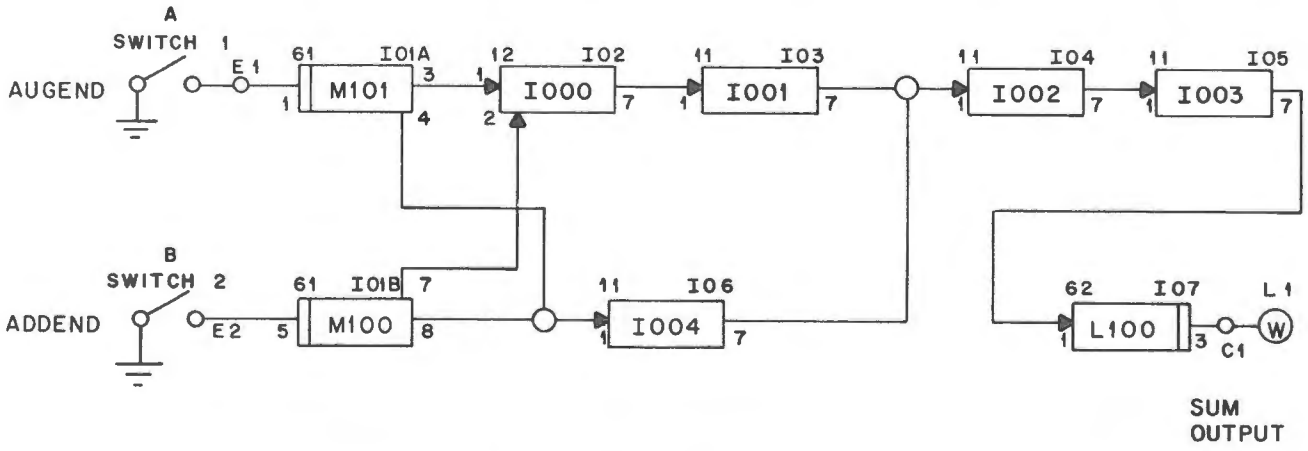


Figure 51. Half-Adder

Proceed through a binary count using the two switches and note when the lamp is on. Record this data in Table 11.

NOTE

Logical 0 = Switch open
Logical 1 = Lamp on

TABLE 11. HALF-ADDER

SWITCH 1 (A)	SWITCH 2 (B)	LAMP	LOGIC
0	0	off	0
0	1	on	1
1	0	on	1
1	1	off	0

Write the output equation in terms of A and B. f = _____
Can your equation be simplified? If so write its simplest form. f = _____
If your circuit is operating correctly, the lamp should be on whenever switch 1 or switch 2 is closed, but off when both switch 1 and switch 2 are closed simultaneously.

Disassemble your circuit and proceed to the next part.

FULL-ADDER

Build the circuit shown in figure 52. After the circuit is completed, check it out as follows:

1. Using the three switches, proceed through a binary count shown in Table 12 and note when the lamps come on.

NOTE

Logical 0 = Switch open
Logical 1 = Switch closed
Lamp on = Logical 1
Lamp off = Logical 0

TABLE 12. FULL-ADDER

CARRY	SWITCH 3	01010101
AUGEND	SWITCH 2	00110011
ADDEND	SWITCH 1	00001111
SUM	LAMP 1	01101001
CARRY	LAMP 3	00010111

2. Assume addend = A, augend = B, and carry = C. Write and simplify the sum and carry equation in terms of A, B, and C.

Sum f =
Carry f =

NOTE

To expand this adder, the logic trainers may be interconnected through J1 and J2 located on the back of the trainer.

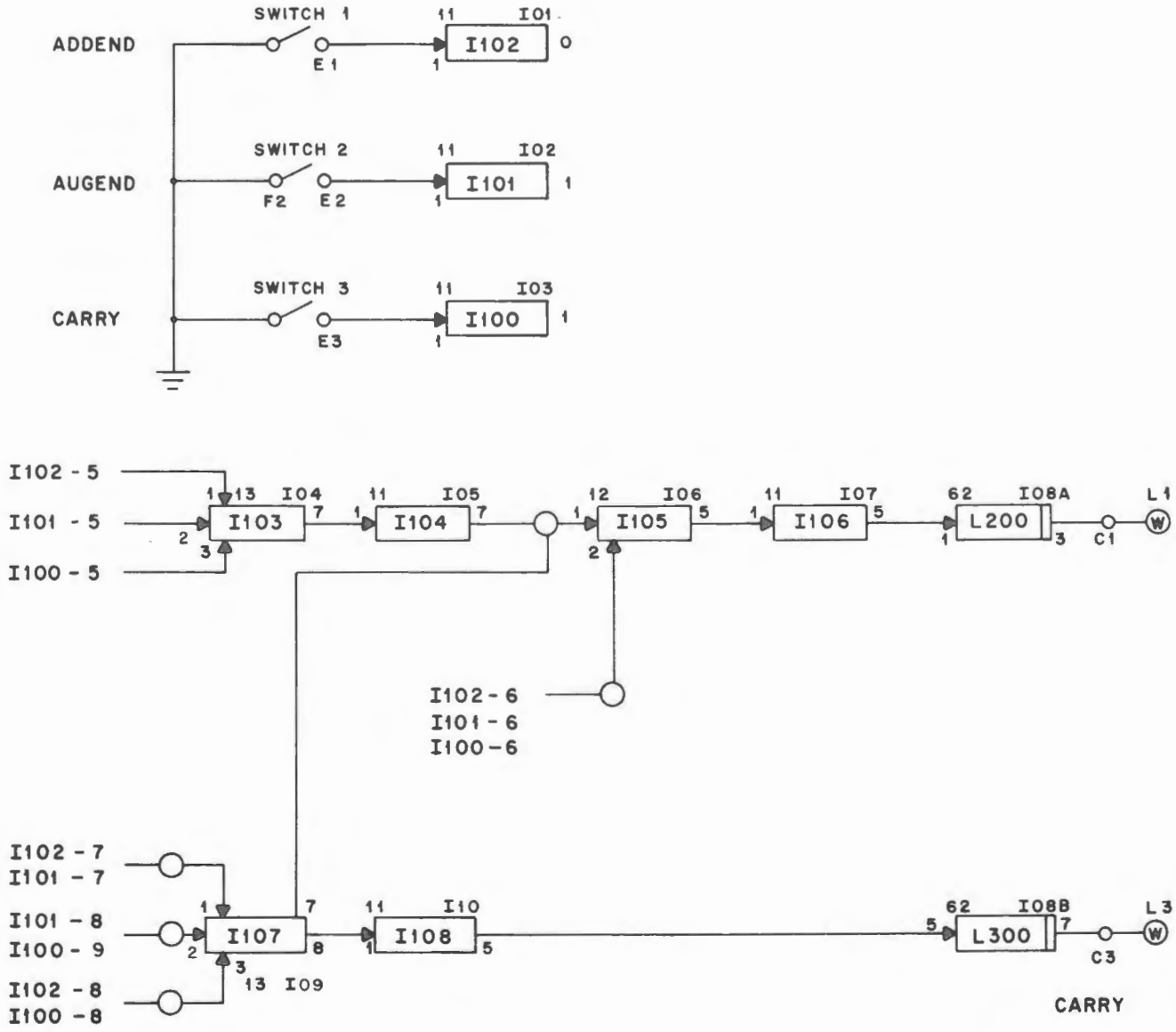


Figure 52. Full-Adder

Digital Electronics

SUMMARY

1. Did this circuit do a full-add? YES
2. Were all possible combinations of the switch positions used? YES
3. Could 24 of these be hooked up to perform a 24-bit add? YES
4. If a closed switch represents a 1 and an open switch represents a 0, did this adder add correctly? YES

LABORATORY 10

TRANSLATION AND DECODING NETWORKS

OBJECTIVE

This experiment should familiarize you with the operation of translating and decoding networks. You will be required to connect the translator so as to detect selected octal numbers represented by the three flip-flops.

EQUIPMENT

Logic Trainer
Oscilloscope
Cards as Needed

INTRODUCTION

In the logic block of figure 53, there are three flip-flops shown at the left of the diagram. On the right of the diagram, five inverter cards are shown with their associated lamp drivers. You will provide the pin numbers, card locations, and wiring data needed for the translators to detect only the numbers recorded beside the lamps.

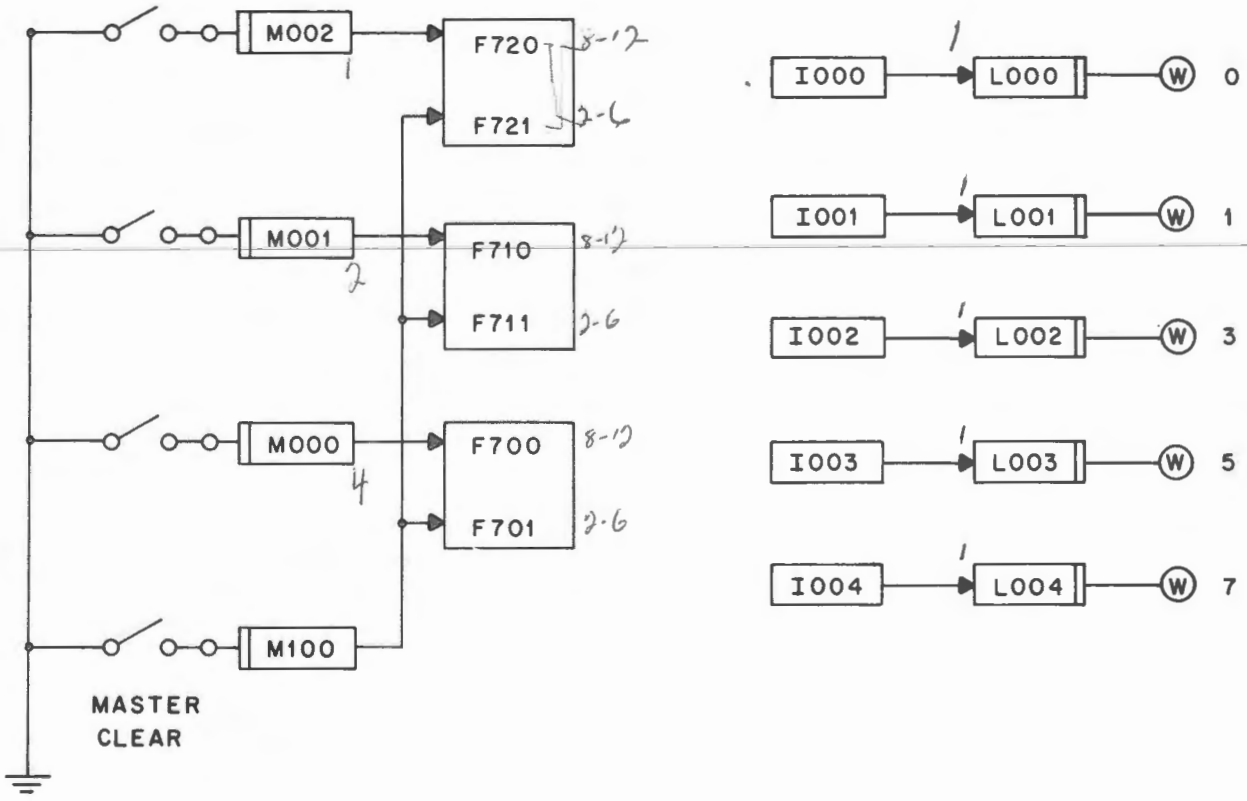


Figure 53. Translation and Decoding Network

PROCEDURE

Translate the term by writing the input equation to each inverter, in the format of the equation: I000=F720+F710+F700 (example only).

I000 =
I001 =
I002 =
I003 =
I004 =

Now build your circuit. When your circuit is complete, use the following procedure to check it out.

1. Press the Master Clear switch and the 0 lamp should be on.
2. Proceed through a binary count using the three switches. Remember to clear after each step in the binary count.
3. As the binary count is executed, check to see if the lamps light for only their designated number.

REFERENCE 5

AND/OR CIRCUITS AND NAND/NOR CIRCUITS

AND CIRCUITS

A computer has been described by many people as a high-speed moron. It is high speed; it can perform millions of operations per second. Perhaps it is a moron; it definitely cannot think. However, it can make simple decisions, and perform functions based on these decisions. It can determine if statements are true or false; it can distinguish between positive and negative numbers; it can determine whether or not a particular circuit has an input or an output. It can work with anything that has two possible states on, off; true, false; yes, no. It cannot work with subjective if's, but's, or maybe's. The work is done with the numeric values logical 0 and logical 1. These values are called logic levels and are represented by voltages called logic voltages. Normally, high voltage represents a logic level of 1, and low voltage represents a logic level of 0. The voltages are not standard and vary from computer to computer, even those of the same make. For example, in 1604 logic, a logical 1 is represented by -3 volts and a logical 0 by a -0.5 volt. In 3000 logic a logical 1 is represented by -5.8 volts and a logical 0 by -1.1 volts. You will notice that when switching from a logical 0 to a logical 1, the logic voltage moves in a negative direction to become more negative. This is called negative logic. If these voltages had been positive and the voltage level had become more positive when switching from a logical 0 to a logical 1, it would be called positive logic.

It was stated that a computer is able to make simple decisions. These decisions are based on the truth of certain statements. A function can be implemented if two or more statements are true. For example, to cause the lamp to light in figure 54, switches A, B, and C must must all be closed. If a closed switch is used to represent a true statement or a logical 1, then statements A, B, and C must all be true in order to implement the function of lighting the lamp.

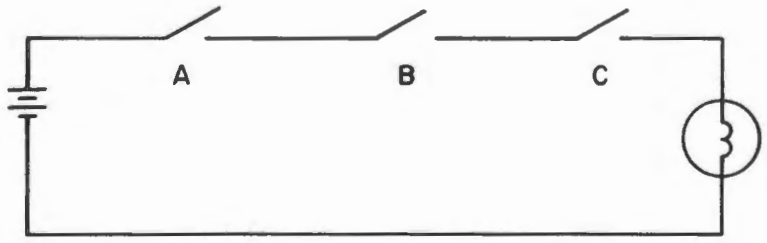


Figure 54. AND Circuit

Figure 55 shows the military specification symbol for an AND gate. It is concerned with logic voltages and levels only. The output on the right will be at a logical 1 level only when all three inputs are at a logical 1 level. If any input switches to a logical 0, the output will also switch to a logical 0. The output can be illustrated as A•B•C. Often the period is left out and the output is expressed as ABC and is read as A and B and C. The three inputs are said to be ANDed together. An AND circuit or gate is shown in figure 56.

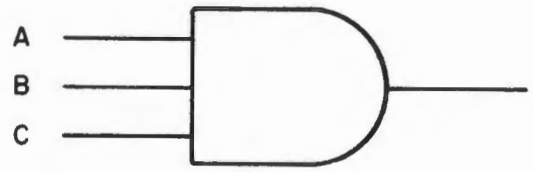


Figure 55. AND Gate Symbol

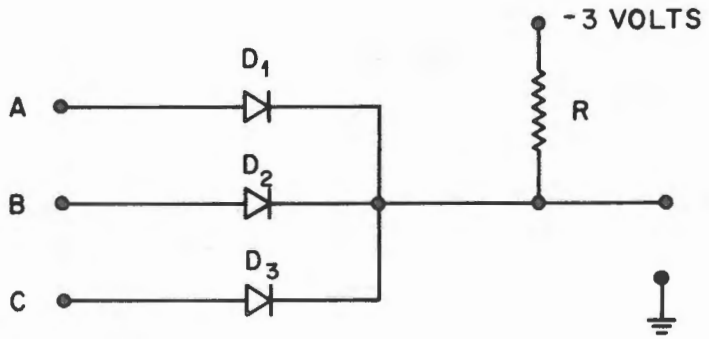


Figure 56. Diode AND Gate Negative Logic

If all inputs are at logical 0 which is a -0.5 volt, all three diodes will conduct. Since a diode is virtually a short circuit when it conducts, the output will be -0.5 volt or logical 0.

If, for example, input B were switched to a logical 1, D_2 would stop conducting since it will now be reverse biased. The output will be held to -0.5 volt by D_1 and D_3 still conducting.

If input A were to switch to a logical 1 so that both A and B were the same, the output would still be logical 0 since D_3 is still conducting.

When input C also switches to logical 1, the output switches because the three diodes are nonconducting. There is no current flow and no voltage dropped across resistance R. Therefore, the output is -3 volts or logical 1.

For use on positive logic, turn the diodes around and change the supply to +3 volts. Figure 57 shows a diode AND gate with a positive logic.

If +0.5 volt equals a logical 0 and +3 volts equals logical 1 the circuit will function in exactly the same manner as before.

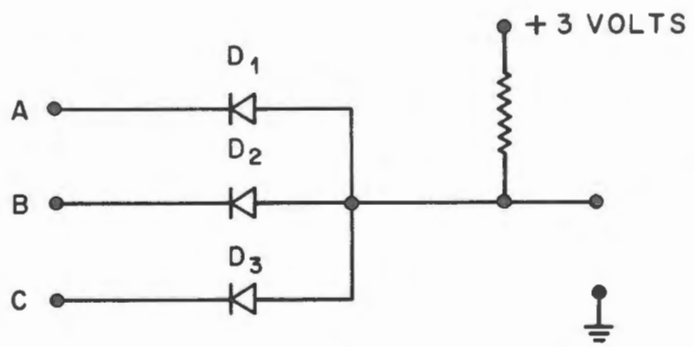


Figure 57. Diode AND Gate Positive Logic

OR CIRCUIT

In some cases, to implement a function, it is necessary that only one input is present. In the OR circuit of figure 58, the lamp lights when any or all of the switches are closed. Therefore, if A or B or C is true, the function of lighting the lamp is implemented.

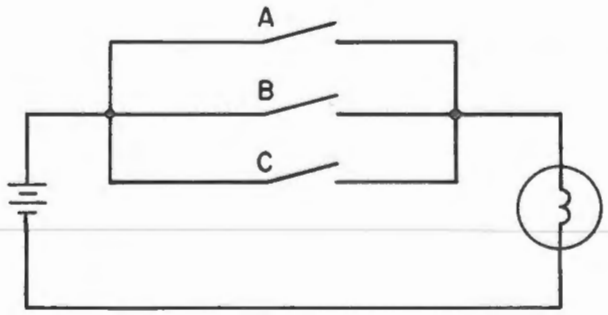


Figure 58. OR Circuit

Figure 59 shows the military specification symbol for an OR gate. The output on the right will be at a logical 1 level when any of the inputs are at a logical 1 level. The output can be expressed as A+B+C. The plus sign is used to denote that these inputs are ORed together and are read as A or B or C.

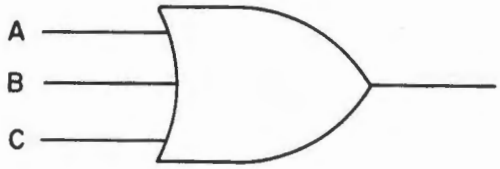


Figure 59. OR Gate Symbol

Referring to figure 60 and using the same logic levels as before, assume that all inputs are at a logical 0 of -0.5 volt. All diodes will be for most purposes nonconducting, and the output will be -0.5 volt.

Switching input B to a logical 1 of -3 volts places forward bias on D_2 and increases conduction. The output voltage would then switch to -3 volts. With this voltage at the output, diodes D_1 and D_3 cut off. If inputs A and C switch to logical 1, they will not affect the output.

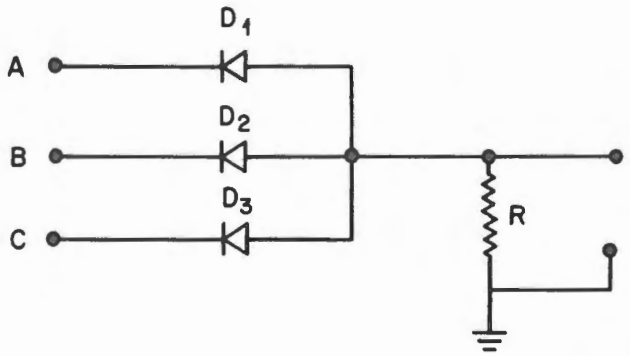


Figure 60. Diode OR Gate Negative Logic

SUMMARY

The output of an AND circuit can implement a function with a logical 1 only when all of its inputs are present or true. If any input is not present or is false, the function will not be implemented.

The output of an OR circuit can implement a function with a logical 1 when any of its inputs are present or true. If all inputs are not present or are false, then the function will not be implemented.

NAND CIRCUIT

Just as some functions can be implemented when certain statements are true, other functions can be implemented when certain statements are not true or false. For example, in the statement, "We will go to a ball game providing it is not raining," the function of going to a ballgame will be implemented if the input statement, "It is raining," is false.

If we use the letter A to represent the statement "It is raining," the statement "It is not raining" can be represented by a term called A not. A and A not are opposites. The statement, A not, which is written $\overline{A}$, is the complement or negation of A. When the one is true (logical 1), the other is false (logical 0).

The negation of a statement is accomplished through the use of a circuit called an inverter.

Inverter circuits use the common emitter transistor circuit in which there is a 180-degree phase reversal between output and input. Therefore, if a logical 1 is applied to the input, a logical 0 will be developed at the output.

If an inverter has an AND gate connected to its input, the two form a NAND gate. The logic symbol is shown in figure 61.

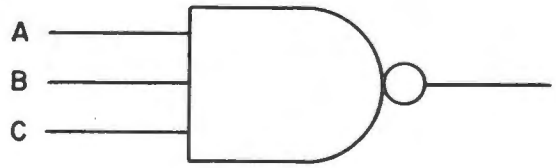


Figure 61. NAND Gate Symbol

The small circle in figure 61 represents the inverter. The output of the AND gate applied to the inverter is ABC and is read as A and B and C. The output of the inverter will be $\overline{ABC}$ which is read as A and B and C negated.

Read this next part carefully since it is important and can be confusing. The output of the NAND gate will be a logical 0 when all inputs are present or true. If any one of the inputs drops or becomes false the output will be a logical 1. If an input becomes false, its complement will be true. Therefore, we can say that $\overline{ABC}$ equals $\overline{A}+\overline{B}+\overline{C}$. A schematic diagram for a NAND circuit is shown in figure 62.

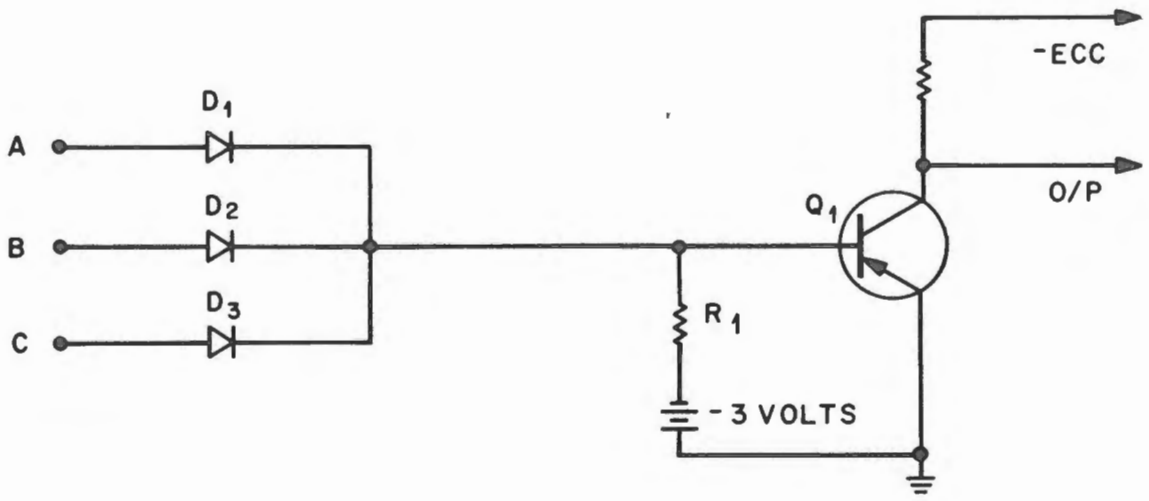


Figure 62. Diode/Transistor NAND Gate

Components D_1, D_2, D_3, R_1, and the -3-volts battery form an AND circuit. When all those inputs are at -3-volt level, -3 volts will be applied to the base of transistor Q_1, and it will conduct heavily. The output will be low (logical 0). If any of the inputs drop to -0.5 volt, this voltage will be applied to the base of Q_1 reducing forward bias. Conduction through the transistor decreases and the output voltage rises (logical 1).

A NAND gate outputs a logical 0 when all inputs are present or true. It outputs a logical 1 if any input drops or becomes false.

NOR CIRCUIT

When discussing the OR circuit, it was shown that the circuit would output a logical 1 whenever any of the inputs were a logical 1. When all inputs were logical 0, the output was logical 0. The NOR circuit is the opposite as the name suggests. It consists of an OR gate feeding into an inverter. Thus, if all inputs are logical 0, the output of the NOR circuit will be logical 1. If any input becomes logical 1, the output will be logical 0. Figure 63 shows the military specification symbol for the NOR gate.

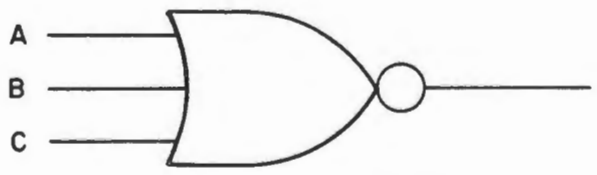


Figure 63. NOR Gate Symbol

This next part should be read carefully since this is the counterpart of the NAND circuit and is as important. The input is expressed as A+B+C which is also the input to the inverter. Inverter output will be $\overline{A+B+C}$. This means that if either A or B or C or any combinations of these is true, the output will be false (logical 0). Therefore, to have a true output, all inputs must be false (logical 0). This may be expressed another way; $\overline{A+B+C}$ equals $\bar{A} \bullet \bar{B} \bullet \bar{C}$.

A schematic diagram of a NOR circuit is shown in figure 64. Components D_1, D_2, D_3, and R_1 form an OR circuit. When inputs A, B, and C are all at -0.5-volt level, this voltage is applied to the base of Q_1. Its conduction will be negligible. The output will be a high voltage of a logical 1. If any of the inputs switches to -3 volts, the diode connected to that input conducts and puts the other diodes into reverse bias. In this way, -3 volts will be applied to the base of Q_1, and the transistor conducts heavily. The output drops to a low voltage of a logical 0.

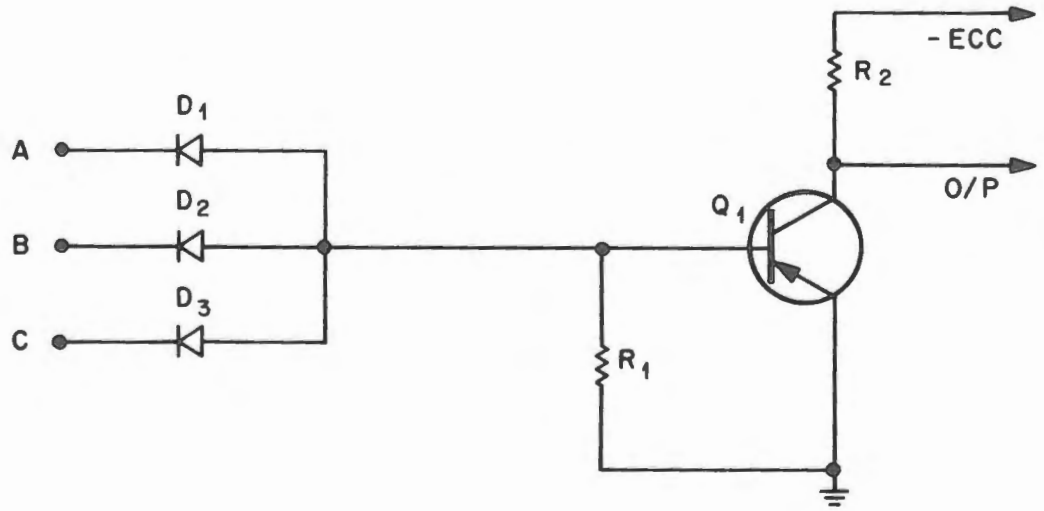


Figure 64. Diode/Transistor NOR Gate

SUMMARY

The output of a NAND circuit can implement a function with a logical 1 when any inputs are not present or false. If all inputs are present or true, the function will not be implemented.

The output of a NOR circuit can implement a function with a logical 1 when all inputs are not present or false. If any input is present or true, the function will not be implemented.

CONCLUSION

NAND and NOR circuits are used exclusively in 1604 and 3000 series logic. Be sure that you understand how they function. Figure 65 shows other logic diagrams used to represent AND/OR and NAND/NOR circuits.

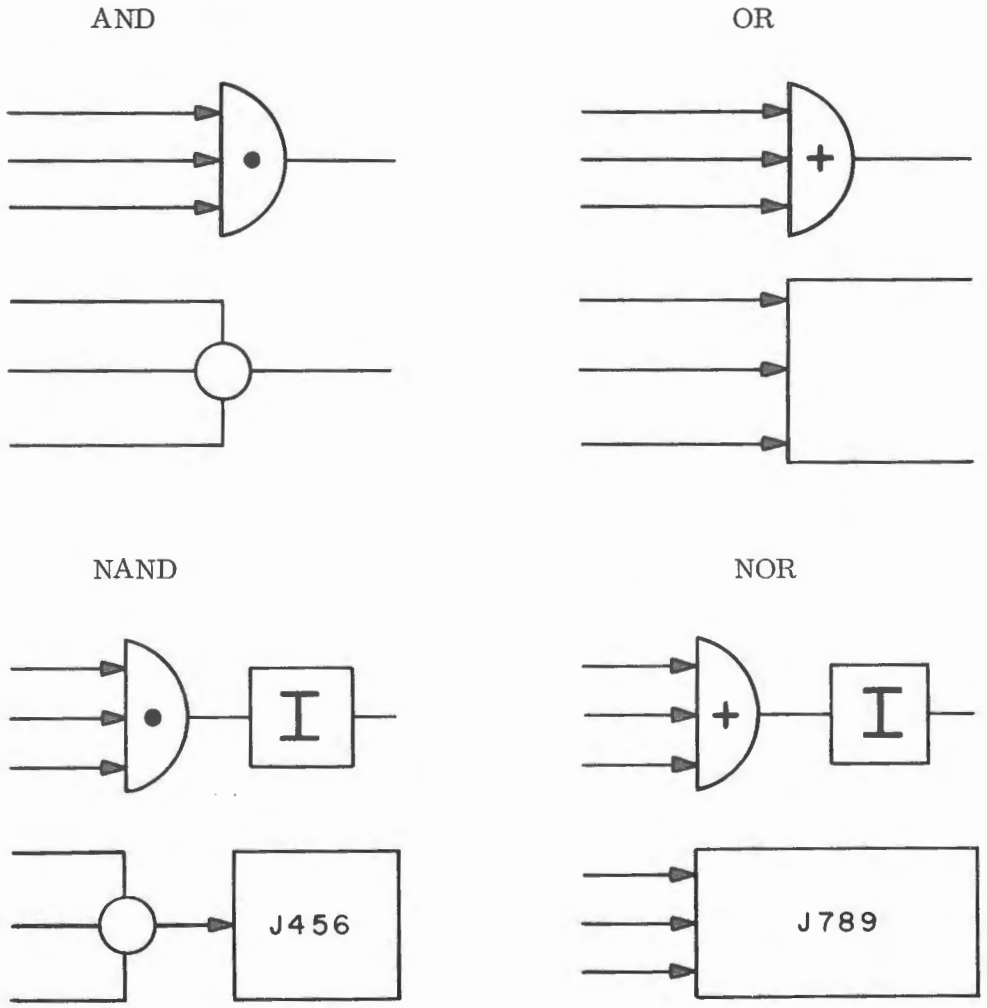


Figure 65. AND/OR and NAND/NOR Symbols

REFERENCE 6

INVERTERS

LOGIC SYMBOL

The logic symbol which will be used to denote an inverter is simply a rectangle with a letter and three numerical digits inside for identification. The inverter in figure 66 is typical of that found in computer logic diagrams.

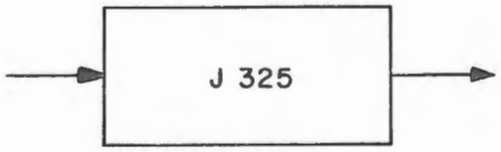


Figure 66. Inverter

In many cases the alphabetical character gives a clue as to the inverter location. For example, J indicates a general purpose inverter; K indicates an inverter used in a flip-flop, N or V indicates inverters used in control delays.

ANALYSIS OF SINGLE INVERTER 11A

The inverter circuit shown in figure 67 is mounted on a standard logic card made from a copper-clad, glass epoxy laminate. The circuit is etched by a photo-etching process. A 15-pin plug is assembled at the bottom. The plug provides connections for inputs and outputs as well as +20-volt and -20-volt supplies. Pin 1 provides the input, and pins 5 through 12 are output pins. The circuit can provide a maximum of eight outputs to other parts of the computer. The -20-volts supply is brought in through pin 13. Pin 14 connects directly to ground, and pin 15 connects to a +20-volts supply.

In the standard inverter circuit shown in figure 67, transistor Q01 is connected as an amplifier. The collector circuit of the transistor has two feedback loops that prevent the transistor from being driven to cutoff or saturation. Switching from one state to the other is accomplished in 10 to 80 nanoseconds.

An input signal is applied through isolation diode CR01 to a voltage divider network composed of resistors: R07, R08, R09, R10, and R11. An input signal of -0.5 volt at point A results in -1.5 volts at point B and +0.8 volt at the base of Q01 (point C) so that Q01 does not conduct. CR01 is biased 1 volt in the backward direction to provide for noise suppression at the input of the inverter.

An open input circuit has the same effect as a -3-volts signal. Point A is biased at -3 volts and CR01 conducts. A voltage of -1.1 volts appears at the base of Q01 causing it to conduct.

Transistor Q01 provides the minimum beta* current gain of 25. The collector current of Q01 develops the output voltage across resistor R07. Output diodes CR09 minus CR16 isolate the output lines from each other. Diodes CR07 and CR08 form the feedback loops that prevent transistor Q01 from being driven to cutoff or saturation. The positive going limit allows a maximum transistor conduction that is less than saturation; the negative going limit fixes a minimum conduction for the transistors.

When the transistor approaches cutoff, the collector approaches -3 volts. The collector potential is coupled back to the base of Q01 through CR08, R08, R09, and R10. The base of Q01 is always held at a sufficiently negative voltage to permit some minimum conduction of Q01.

When the transistor approaches saturation, the collector approaches 0 volts. The collector potential is coupled back to the base of Q01 via CR07 and R10. In this way the base of Q01 is prevented from becoming so negative that saturation occurs.

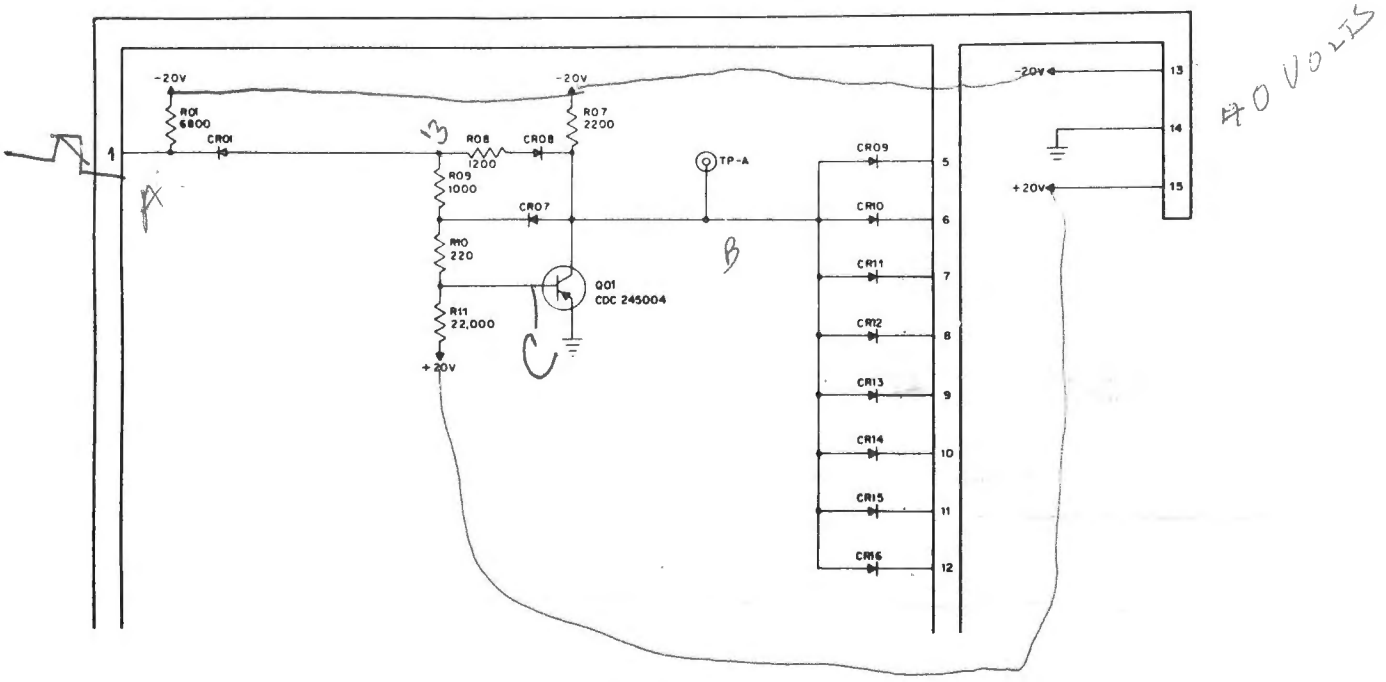


Figure 67. Standard Inverter (1604)

*The beta current gain is the ratio of collector current to base current.

SINGLE INVERTER 13A

The operation of the single inverter type 13A circuit is much the same as the type 11A. The major difference as can be seen in figure 68 is that there is provision for three separate inputs instead of one.

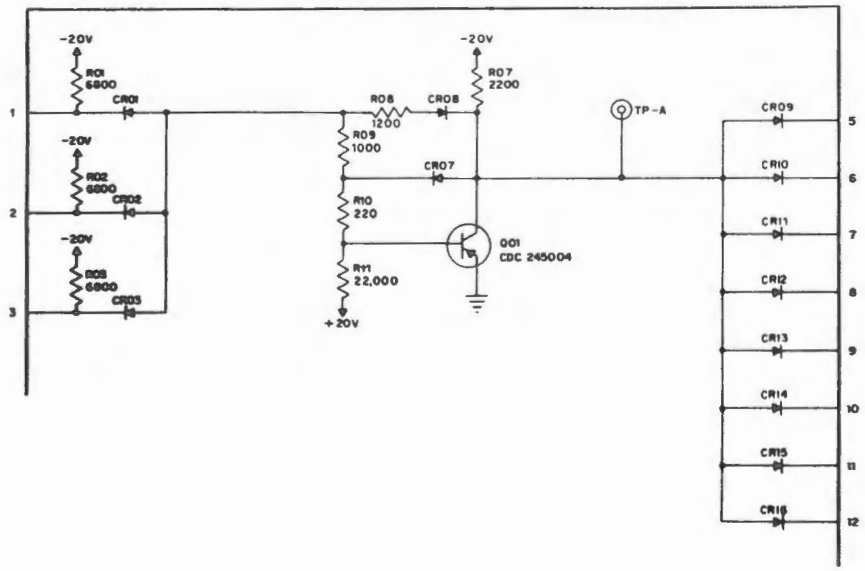


Figure 68. Three-Input Inverter

Each input operates independently from the others forming a three input or gate. This means that a -3 volts applied to pin 1, 2, or 3 will switch the transistor Q01 on and drop the output to -0.5 volt.

AND CONNECTION

It is often required that several inputs are ANDed together. To do this, all inputs to be connected this way are connected to one single input pin. This method is shown in figure 69.

The outputs of the individual cards A, B, and C are taken from any one of the eight pins 5 through 12 on each card. These outputs are connected to a single input pin on card D. This would be pin 1 on a 11A card or either pin 1, 2, or 3 on a 13A card.

OR CONNECTION

Inputs that are to be ORed require the use of specific cards. For example, if three circuits are to be ORed, a type 13A card must be used, and connections must be made as shown in figure 70.

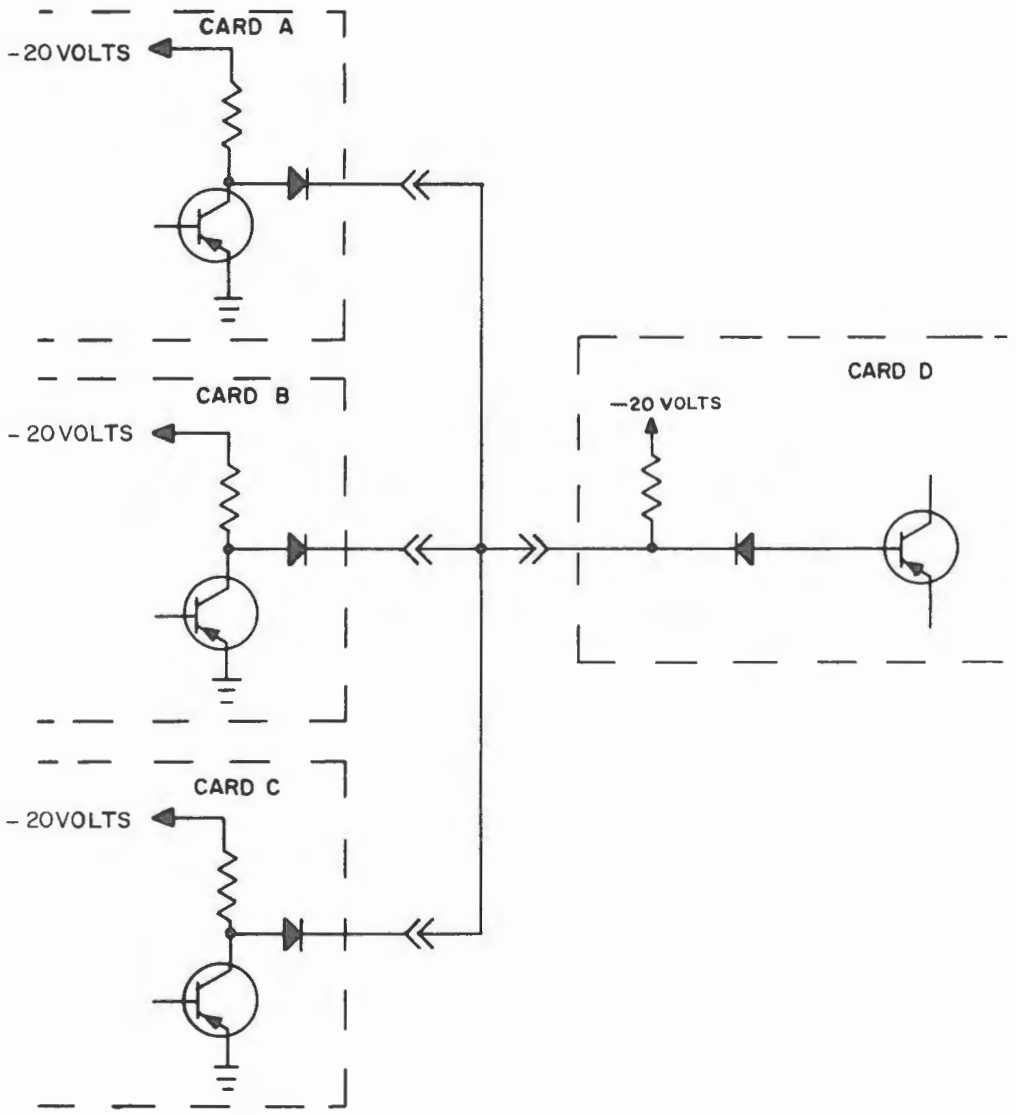
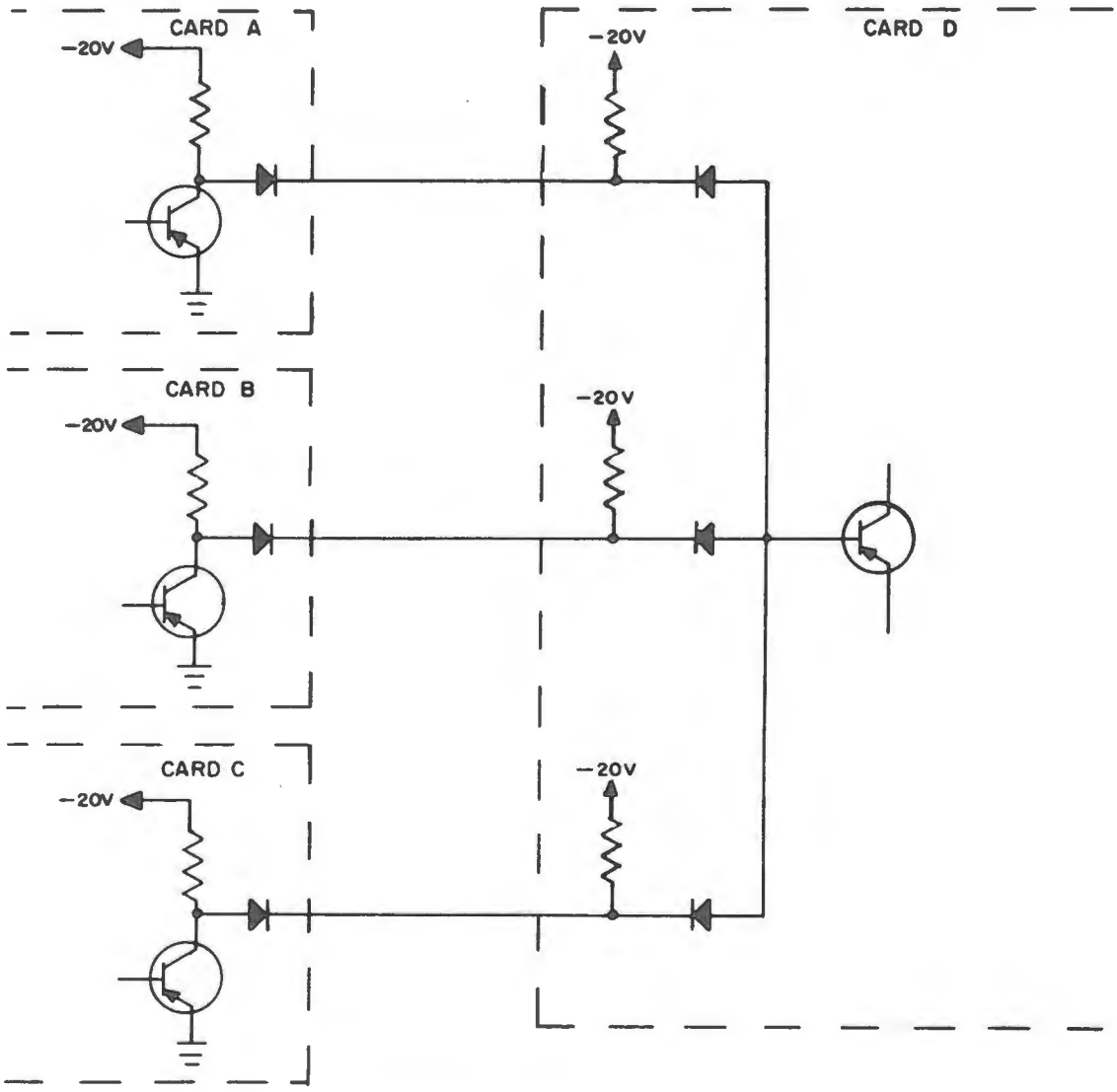


Figure 69. Three-Input AND Circuit



CONVENTIONAL REPRESENTATION

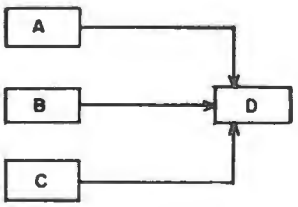


Figure 70. Three-Input OR Circuit

3000 SERIES INVERTER

The inverter used in the 3000 series computer performs the same function as the 1604 but accomplishes this function in a different manner. The logic voltages used are -5.8 volts for logical 1 and -1.1 volts for logical 0. Figure 71 shows the schematic diagram for the HA inverter card.

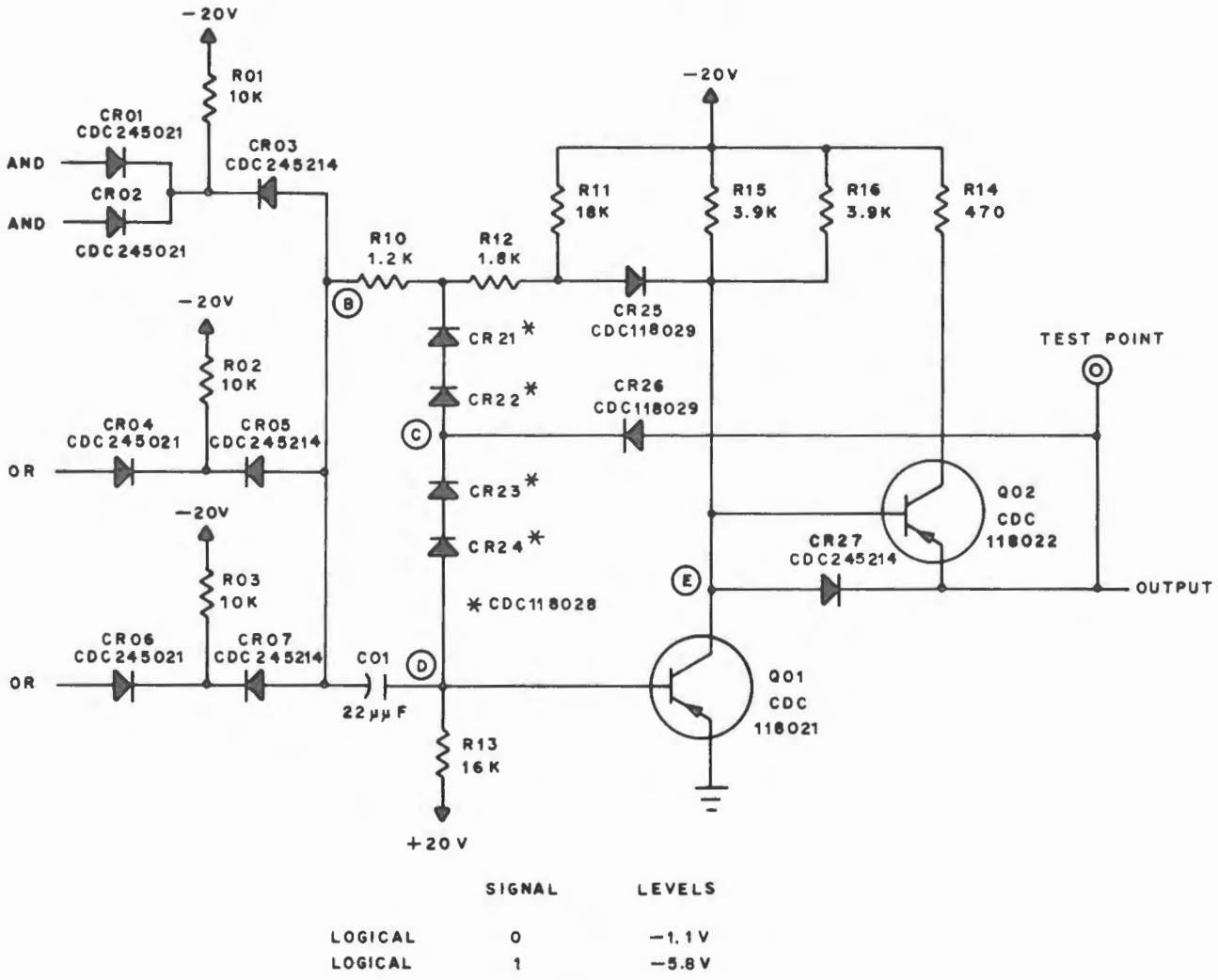


Figure 71. 3000 Series Inverter

The advantages of this type of card over the 1604 inverter are that more input and output connections are available. The 1604 inverter has 12 pins available; eight for output and four for input. If more inputs are required, they are available at the expense of output pins. The 3000 series cards have AND gates and OR gates assembled at the input terminals and can be combined in any manner. Of the 12 pins available, 11 are used for input and only one is used for output. However, this one output can drive up to eight loads. Another advantage of the 3000 series cards is their higher switching speeds.

Capacitor C01 is a speedup capacitor, CR 26 is the saturation diode, and CR25 is the cutoff clamp.

REFERENCE 7

FLIP-FLOPS

USE OF THE FLIP-FLOP

The flip-flop is, perhaps, one of the most versatile circuits used in a computer in that it can serve a variety of functions. It can temporarily store logical 1's or logical 0's, indicate a status within the computer such as BUSY, READY, CLEAR, GO, STOP, READ, WRITE, etc., or it can be used to lockout certain functions or allow certain functions to be performed. A number of flip-flops can be connected to form a register or connection. This usage is discussed in a later session.

BUILDING THE FLIP-FLOP

The flip-flop is not confined to computer use. In fact, it originated in the form of the Ecceles-Jordan trigger circuit long before computers became a reality. This trigger circuit was used in radar systems. It consisted of two DC amplifiers connected in cascade with the output of the second stage connected to the input of the first. The two amplifiers used vacuum tubes since transisters had not been developed at that time. The basic operation was simple in that only one tube could conduct at a time; the other was cut off. It required that a trigger pulse was applied to the cutoff tube to cause the circuit to switch conditions and another trigger pulse to bring it back again.

The modern day flip-flop functions in the same way. The vacuum tubes have been replaced by transistors, and the time required to switch from one state to another has been greatly reduced.

The flip-flop circuit to be studied at this point is built with two inverter circuits on a card known as type 31A. The method of connection and logic values are shown in figures 72 and 73.

If logical 1 is applied to point A, the output of inverter 1 goes to logical 0 and inverter 2 outputs a logical 1. Refer to figure 72. This output is coupled back into inverter 1 in an OR function. Refer to figure 73. Therefore, if the input to point A drops to logical 0, the state of the two inverters will not change.

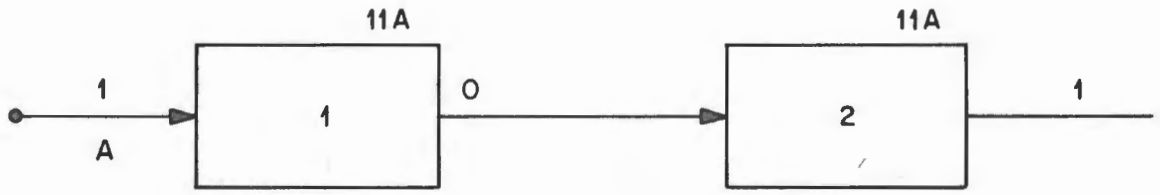


Figure 72. Two Inverters

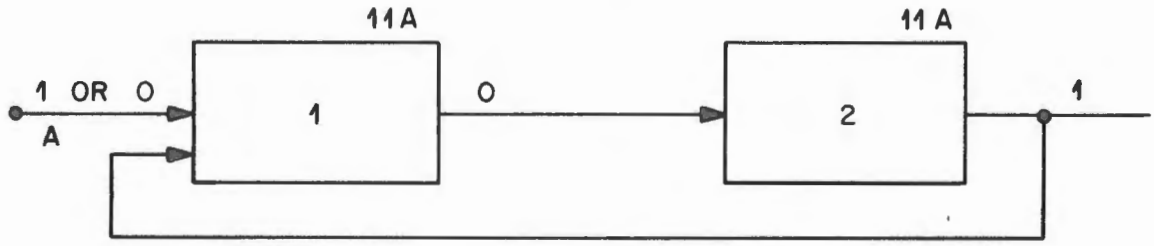


Figure 73. Two Inverters with Feedback

If a second input B is applied to inverter 2 and is put to logical 1 then the condition of the inverter will change as shown in figure 74.

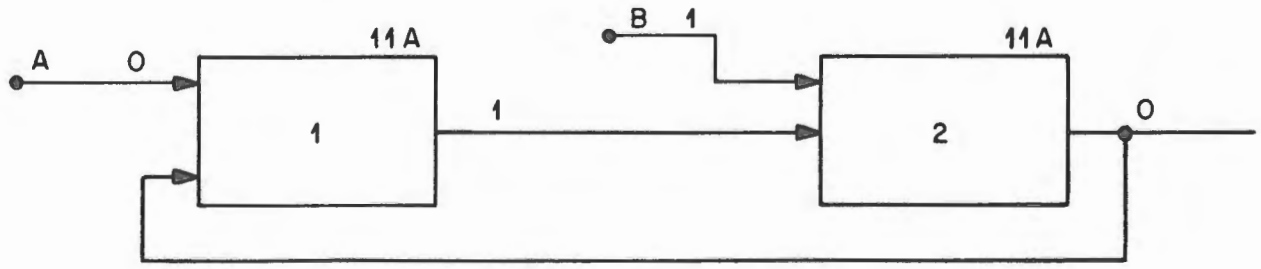


Figure 74. Basic Flip-Flop

Figure 75 shows the schematic diagram of a type 31A flip-flop. If each circuit is examined, it can be seen that they are identical to the other and, in turn, identical to the type 11A inverter.

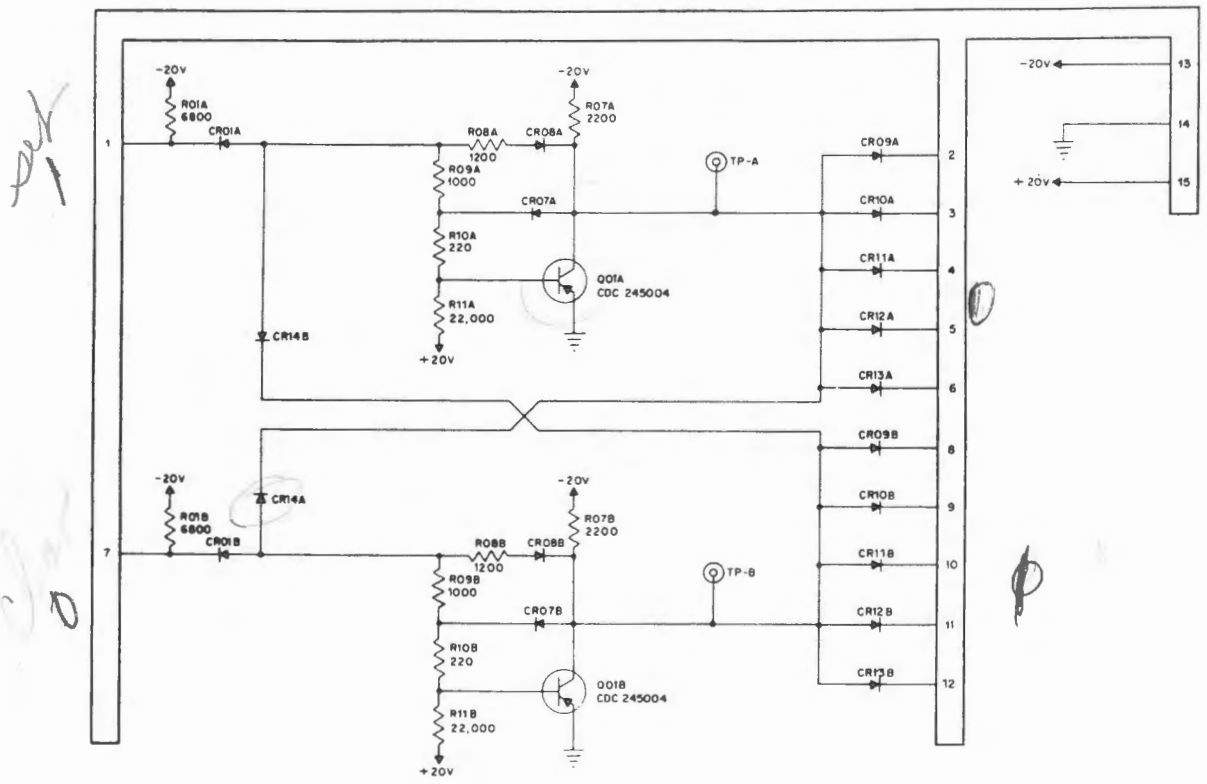


Figure 75. Standard Flip-Flop

If a logical 1 of -3 volts is applied to pin 1, transistor Q01A will conduct. Its collector voltage will be held to -0.5 volt or a logical 0. If the input to pin 7 is also logical 0, CR01B and CR14A will both be reverse biased and Q01B will be cut off. Its collector voltage will be -3 volts or a logical 1. This voltage is coupled via CR14B (forward biased) to the base circuit of Q01A so that when the input to pin 1 drops to logical 0 of -0.5 volt, Q01A still conducts and Q01B remains cut off.

If a logical 1 of -3 volts is applied to pin 7, CR01B will be forward biased and transistor Q01B conducts. Its collector voltage drops to -0.5 volt or a logical 0, and CR14B is reverse biased. Transistor QI1A now becomes reverse biased and cuts off. Its collector voltage goes to a -3 volts for a logical 1 which is coupled through CR14A, or forward biased, to the base circuit of Q01B so it remains conducting. The circuit now remains in this condition until another logical 1 is applied to pin 1.

The flip-flop is a bistable device. The two stable states are called set and clear. Pin 1, in figure 75 is the set input, and when a logical 1 is applied to this pin, the circuit enters its set state. A logical 1 will be available at pins 8 through 12 which are called set outputs. When a logical 1 is applied to pin 7, the clear input pin, the circuit goes into its clear state and a logical 1 will be available at pins 2 through 6 which are the clear outputs.

If a logical 1 is simultaneously applied to pins 1 and 7, the flip-flop goes into limbo with a logical 0 on both outputs. The circuit is neither set nor clear in this condition, but will take the condition of the input retaining the logical 1 should one of the inputs drop to logical 0.

LOGIC SYMBOL

Figure 76 shows the conventional logic symbol for a flip-flop. A and B are the set side input and output, respectively, and C and D are the clear side input and output, respectively. The terms K000 and K001 represent the inverters that make up the flip-flop. Since the set output is at point B and is provided by K001, there is a crossover inside the symbol that is not shown. Figure 77 shows the details of the inverters and the crossover.

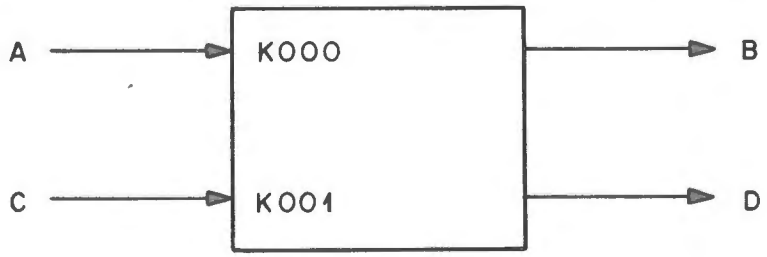


Figure 76. Logic Symbol

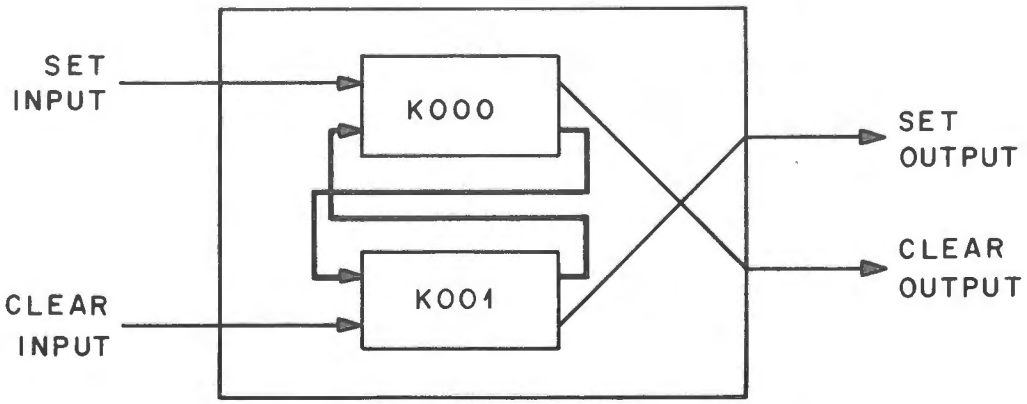
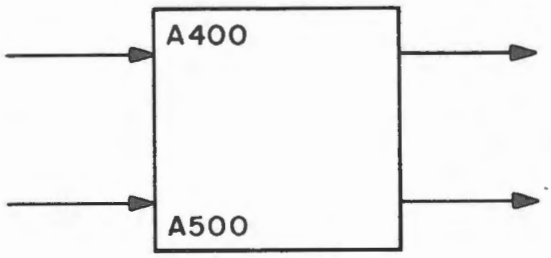


Figure 77. Internal Connections

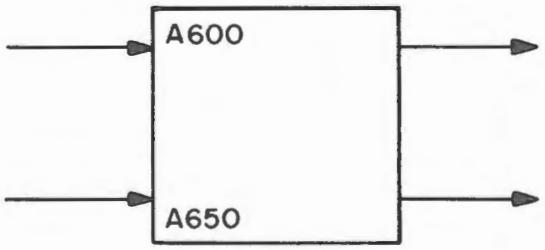
NUMBERING SYSTEMS

Control Data uses three methods to number the inverters of a flip-flop as shown in figure 78.

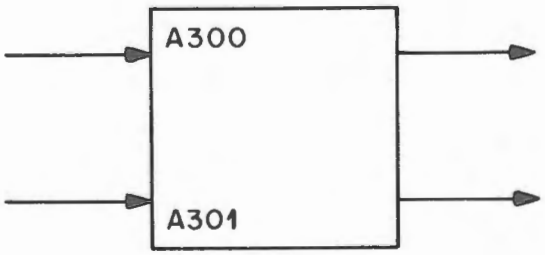
In the three cases, the larger term denotes the set output and the smaller term denotes the clear output.

1. 

Set input to A400 and set output from A500.
Clear input to A500 and clear output from A400.

2. 

Set input to A600 and set output from A650.
Clear input to A650 and clear output from A600.

3. 

Set input to A300 and set output from A301.
Clear input from A301 and clear output from A300.

Figure 78. Numbering Methods

The method most commonly used on this course is number 3 where the letter denotes the register in which the flip-flop is used. The upper two digits represent the position of the flip-flop within the register. The lower digit is either a 0 or a 1 making one number even and the other number odd.

If the letter is a K, this usually means that the flip-flop is not associated with any register and is used to indicate a particular status within the computer. In this case, the digits bear no real significance other than the top one is always even and the bottom one is always odd.

DATA STORAGE

Information and data that is stored in a computer in the form of logical 1's and 0's, can be held in a register consisting of a number of flip-flops connected together. Individual flip-flops in the register will be either set or clear.

If a flip-flop is set, it is storing a logical 1; if it is clear, it is storing a logical 0. If a flip-flop is set, the odd term outputs a 1 and the even term outputs a 0. If a flip-flop is clear, the even term outputs a 1 and the odd term outputs a 0. These facts on data storage must be committed to memory. They can mean your rise or downfall when studying computer hardware.

REFERENCE 8

INPUT/OUTPUT CIRCUITS

Digital computer systems consist of a central computer and various pieces of input/output (I/O) equipment. The central computer processes information sent to it from input devices such as card readers, tape units, typewriters, etc. When the computer has processed the input information, it sends the information to an output device such as a line printer, a card punch, or a typewriter for printing on paper or punching on cards. The information would now be in a form that can be used by humans.

Communication between the central computer and the I/O equipment is accomplished by interconnecting the units with cables as shown in figure 79. The connecting cables in a computer system vary in length according to system layout.

When transmitting information or control signals over long cables, it is not practical to use low voltage levels, such as those found inside the modern day computer. This is true because of the drop in signal voltage due to resistance of the wire in the cable. The longer the cable is, the more resistance it has and the greater the voltage drop will be.

This problem makes it necessary to increase the logical voltage levels as they leave the computer for transmission to I/O devices and to decrease the nonlogical voltage levels as they enter the logic circuits of the I/O controller units.

Voltage level change is accomplished with the I/O cards. The output cards convert low-level logic voltage to the high-level voltages necessary for cable transmission. The input cards convert the high-level voltages to the low-level voltages used in the central computer and the I/O controllers.

The I/O cards that are commonly used for this purpose are the 61 input card and the 62 output card. * These cards are similar to the standard Control Data inverter card in that they contain a common-emitter amplifier configuration. Although these cards produce a 180-degree electrical phase shift, they are not used as logical inverters. Instead, they are used in pairs so that the total phase shift is 360 degrees. The initial and final voltage levels are identical. Figure 80 illustrates the use of the 61 and 62 cards.

From figure 80 it can be seen that a logical 1 into the 62 card produces a ground level output, ground level fed into the 61 card produces a logical 1 output. When a logical 0 or ground is fed into the 62 card, its output goes to a -16 volts. When this -16 volts is fed into the 61 card, it produces a logical 0 output. The output of the 61 card will always be the same as the input to card 62.

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*On logic drawings the 61 card is shown as an M card, and the 62 card is shown as an L card.

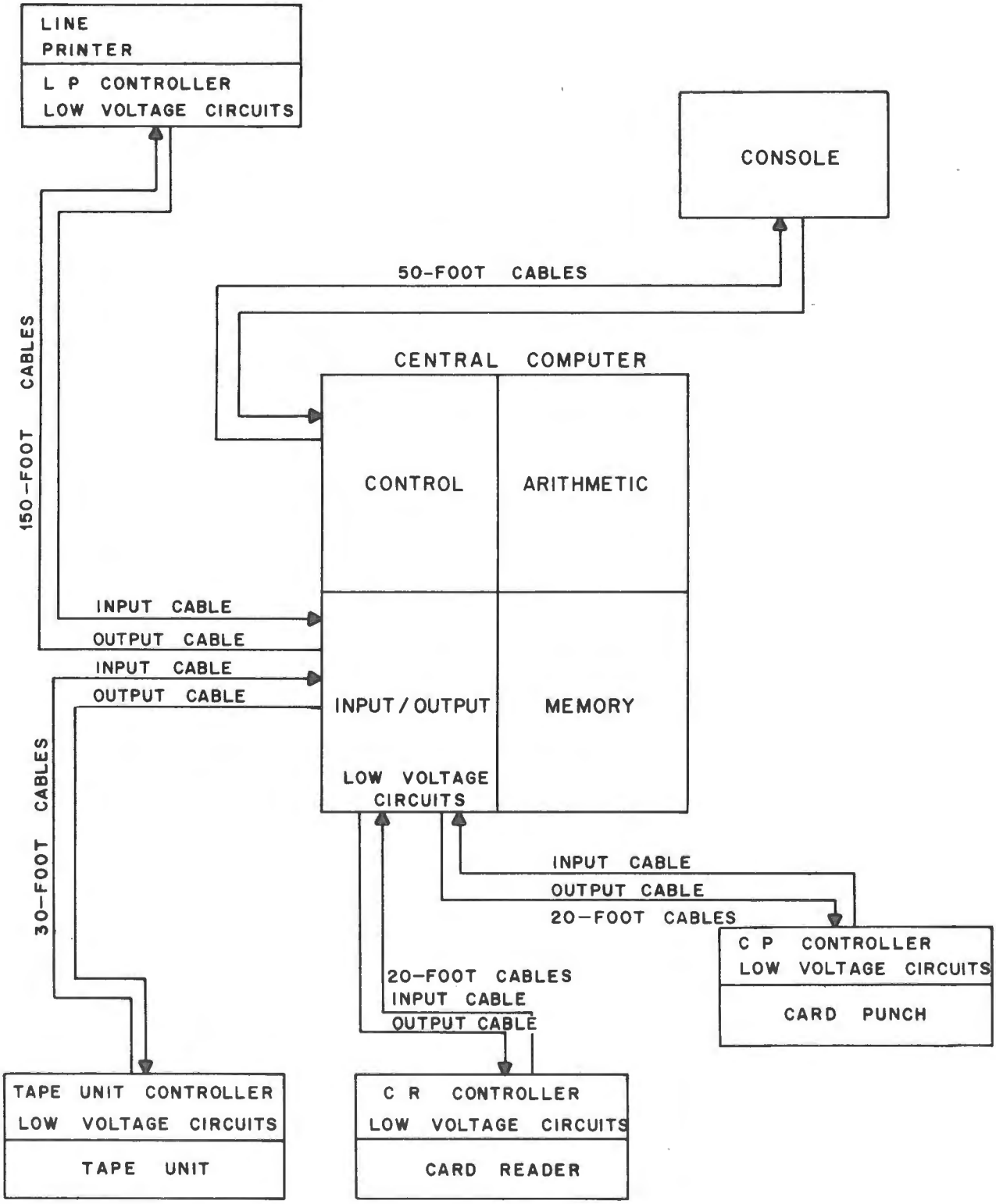


Figure 79. Computer System Block Diagram

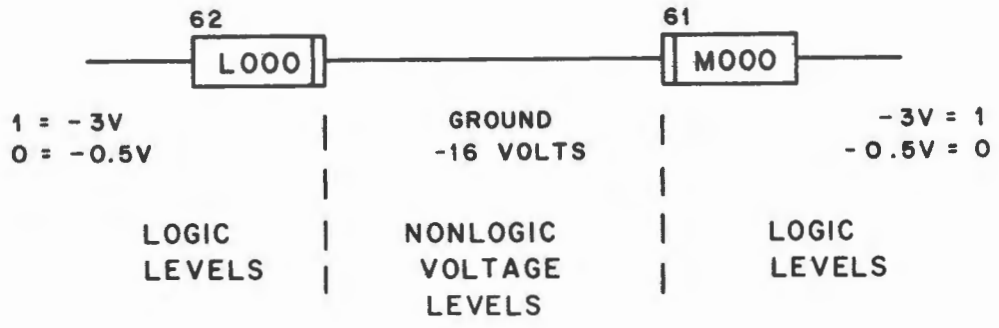


Figure 80. L and M Card Operation

Figure 81 illustrates how 61 and 62 cards are used to transmit logic information between the computer and the magnetic tape unit.

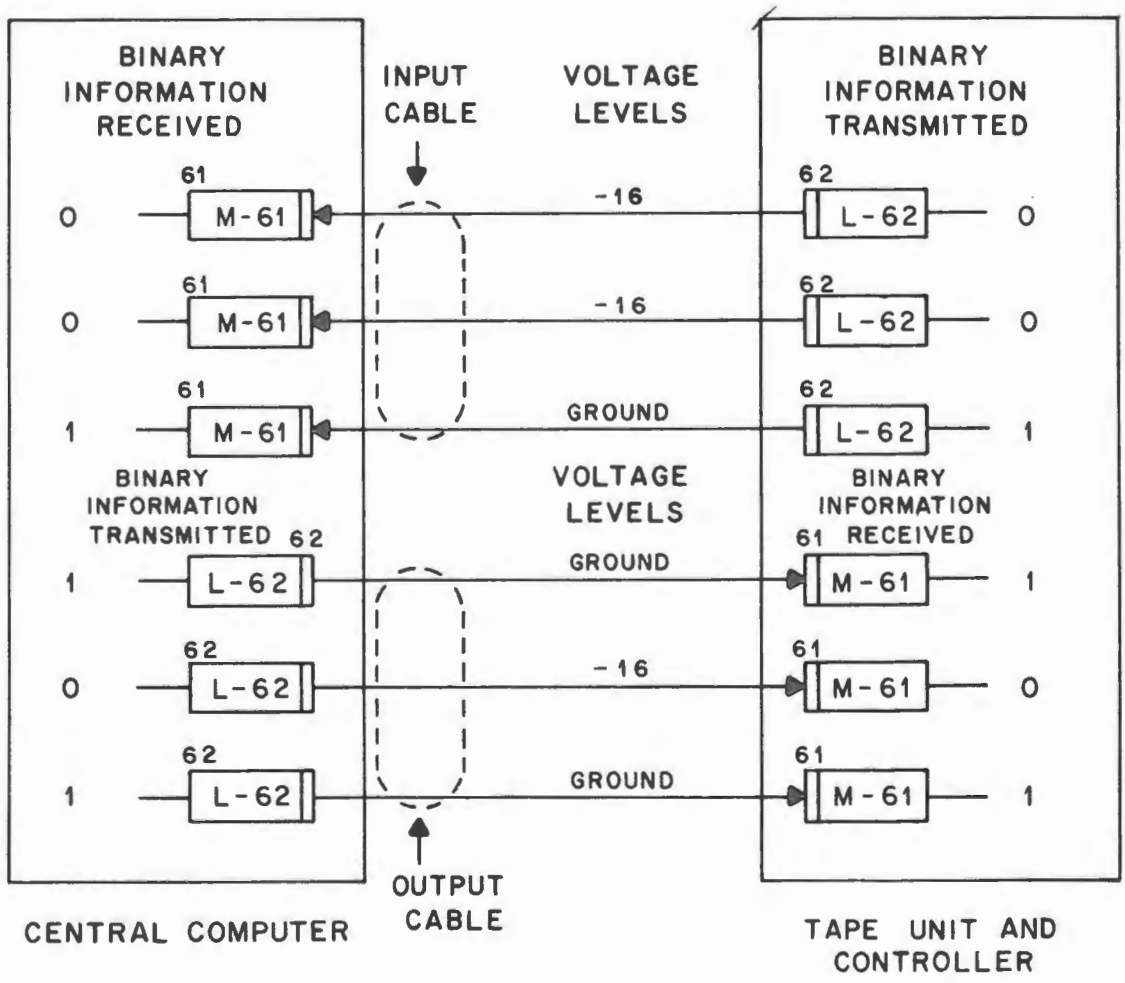


Figure 81. Transmission Lines

L CARD

A schematic diagram shown in figure 82 is that of an L or type 62 card.

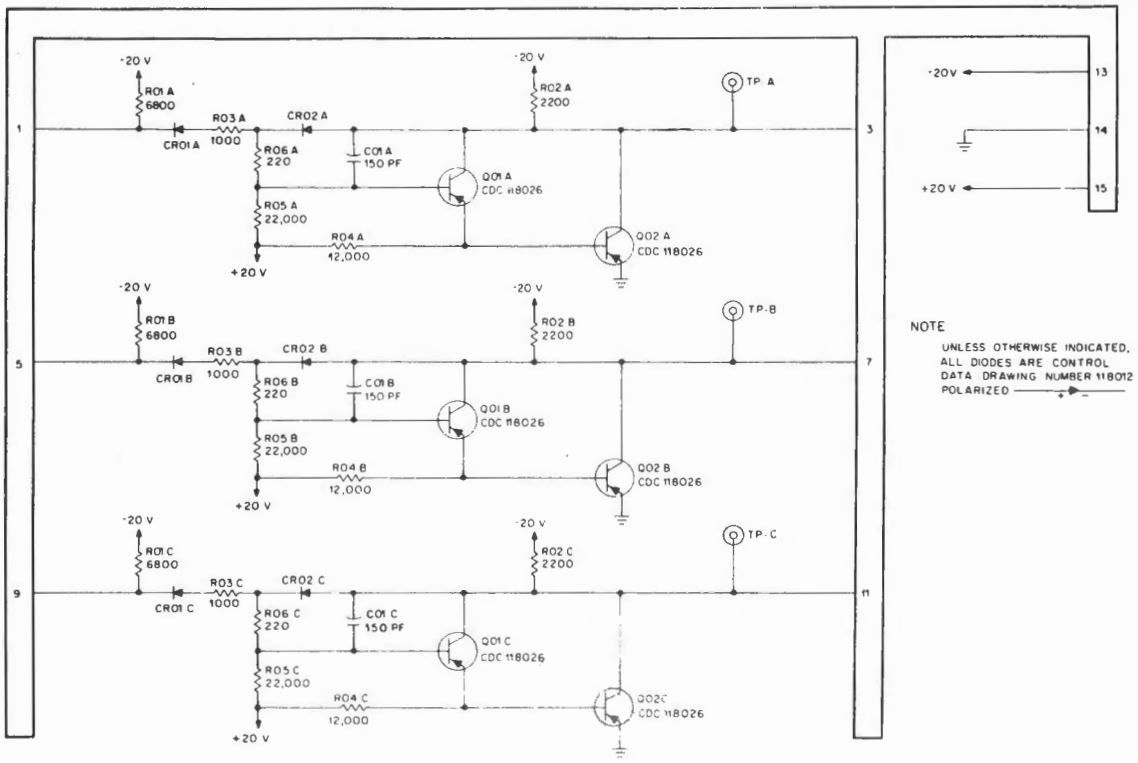


Figure 82. L Card

There are three sections on this card, each independent of the others. As can be seen by the component lettering, the sections are labeled A, B, and C. Each circuit has one input and one output pin.

If a logical 1 of -3 volts is applied to an input, the transistors in that section will be forward biased and will conduct heavily. The output pin will be grounded by the heavy conduction through transistor Q02. This output of 0 volts must not be construed as a logical 0; it is a nonlogic voltage.

If a logical 0 of -5 volts is applied to an input, the transistors will be reverse biased and nonconducting in that section. The output voltage will rise to approximately -20 volts. This is also a nonlogic voltage, and must not be construed as a logical 1. With this type of output, the 6 card is often used as a light driver as shown in figure 83.

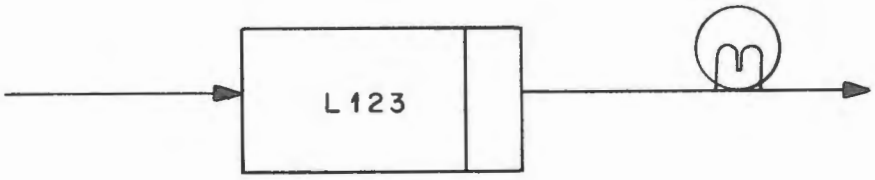


Figure 83. L Card as a Light Driver

When a logical 1 is applied to the input of L123, its output goes to 0 or ground. This puts 20 volts across the lamp lighting it.

When a logical 0 is applied to the input of L123, its output goes to approximately -20 volts. There is no voltage across the lamp, and it does not light. An arrangement such as this indicates the presence of a logical 1.

M CARDS

The M card, type 61, performs the opposite function of the L card. It will convert nonlogic voltage inputs into logic voltage output. Figure 84 shows the schematic diagram for the M card.

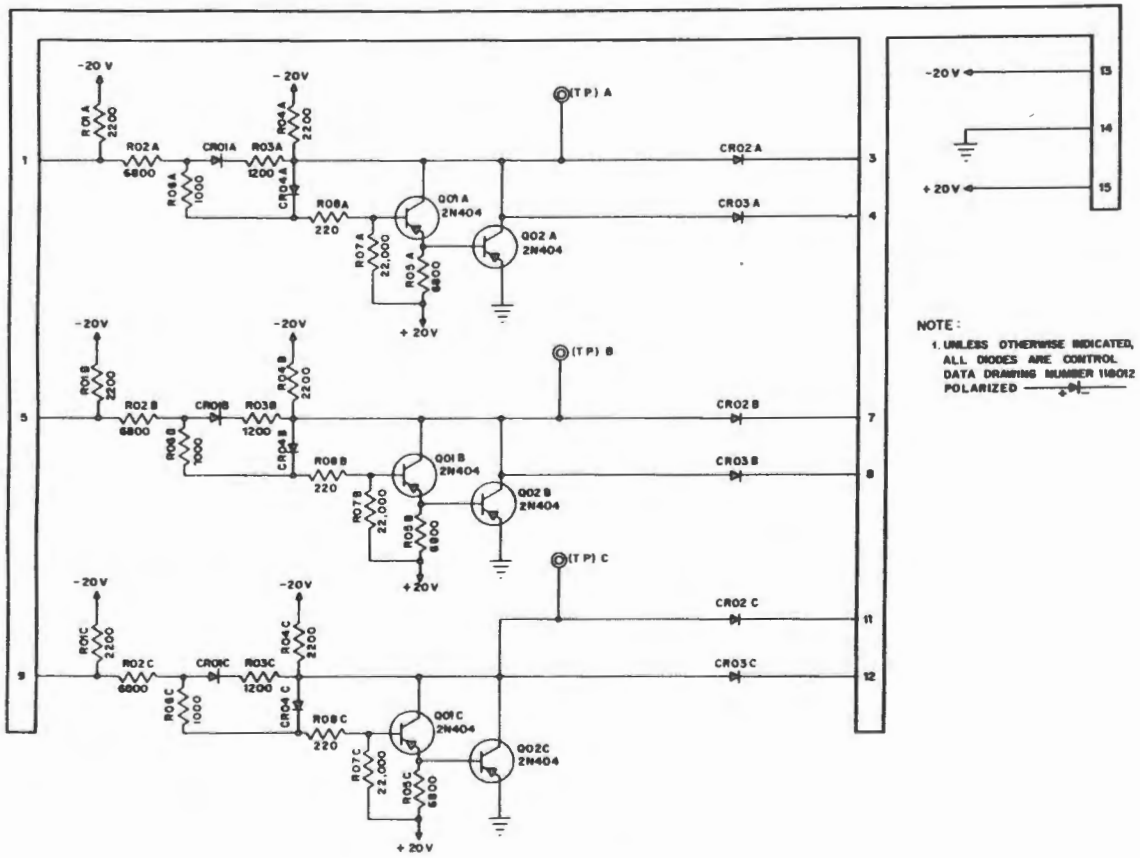


Figure 84. M Card

When the applied input is -20 volts, it is the equivalent to an open circuit input. A current flows from the -20-volt source through R01, R02, R08, and R07 to the +20-volt source. The transistors conduct heavily, however, the output voltage will be clamped to -0.5 volt by CR04 conducting. The output in this case is a logical 0.

When the input is grounded, the transistors are only slightly forward biased and the output is clamped to -3 volts by CR01 conducting. In this case, the output is a logical 1.

Eleven cards are often used in conjunction with switches. This is shown in figure 85.

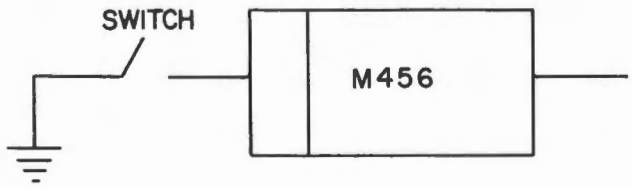


Figure 85. M Card with Switch Input

With the switch open, the output of M456 will be logical 0. With the switch closed, the input to M456 is grounded, and its output will be a logical 1.

T CARDS

Transmitter cards and their associated receiver cards perform the same function as L and M cards when it comes to transmitting data through long cables. The method, however, is quite different. The output is balanced about ground which means that there are two output lines. One is positive with respect to ground, while the other is negative by an equal amount. The difference of potential between the lines remains the same. In 3000 series logic the potential difference between the lines if 0.5 volt, and a logical 1 is distinguished from a logical 0 by a complete polarity reversal between the lines. This is shown in figure 86.

TRANSMISSION LINES

The output of the transmitter card feeds into what is called a twisted pair transmission line which performs the same function as the flat connecting wire at the back of a television set that connects the antenna to the set. It connects a source to a load with a minimum of loss. The twisted pair line allows data to be transmitted from the transmitter card to the receiver card without loss eliminating the need for the high nonlogic voltage used with L and M cards.

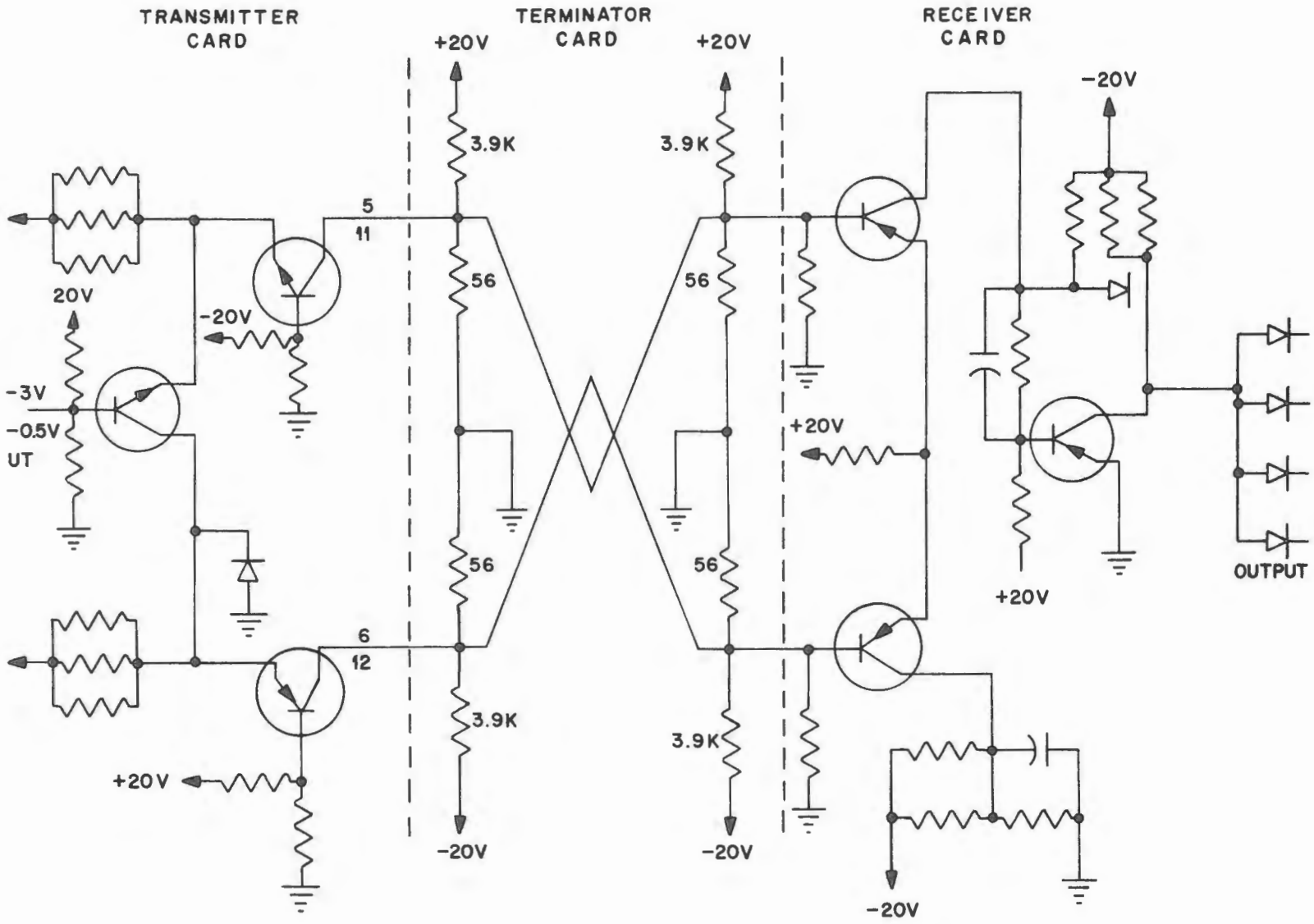


Figure 86. Transmitter/Receiver Circuit

R CARDS

The receiver card functions as a differential amplifier. It provides an output of either logical 1 or logical 0 according to the polarity of the input from the transmission line. These inputs are connected directly to the bases of Q04 and Q05. Since they are balanced about ground, when one input shifts by 0.25 volt in the positive direction, the other input shifts by 0.25 volt in the negative direction.

If a negative input is applied to the base of Q04 and a positive input is applied to the base of Q05, Q04 conducts more than normal and Q05 conducts less. A logical 1 will be developed at the output. If the polarity of the input reverses, Q05 will conduct more than normal and Q04 will conduct less. A logical 0 will be developed at the output.

To obtain a logic inversion in the receiver card, the inputs are reversed. Figure 87 (A) shows the logic symbol for the straight receiver, and figure 87 (B) shows the symbol for the receiver inverter card.

A B

Figure 87. Receiver Cards

REFERENCE 9

INDUCTIVE AND CAPACITIVE DELAYS

In many applications throughout a computer system, it is necessary to delay an input or output signal by a predetermined amount of time. The reason could be to ensure that two pulses arrive at a certain point simultaneously, or to produce a pulse of a specified time duration.

Since inductors and capacitors oppose any change in current or voltage, and time is involved in changing their states, they are used to provide any required delay time.

INDUCTIVE DELAYS

Perhaps you may recall that inductance is a circuit property that opposes any change in circuit current flow. Therefore, in the circuit shown in figure 88, on the instant the switch is closed, the current flow begins at 0 and slowly rises to the maximum value. The amount of time required depends upon the size of the components. The voltage across the resistor is in phase with current flow and rises with it. If the battery potential is 3 volts, this could be compared to a logical 1 in 1604 terms and could be referred to as the circuit input. Therefore, when the switch is open, a logical 0 is applied to the circuit, and the voltage across the resistor is 0 volts. This could also be compared to a logical 0. When the switch is closed, 3 volts or logical 1 is applied to the circuit; however, this voltage will not appear across the resistor until the current has reached its maximum value some time later. The voltage across the resistor can be used as the output and is delayed with respect to the input by an amount determined by the LR time constant. When the switch is opened, a logical 0 is applied to the circuit; however, the voltage across the resistor will not drop to 0 until the current does. This results when the drop in current flow is opposed by the inductance.

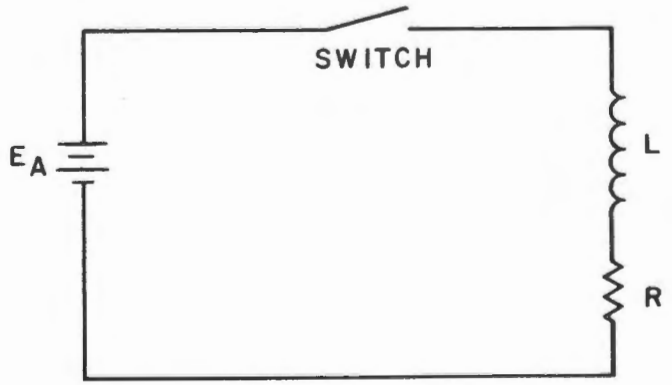


Figure 88. Basic RL Circuit

An inductive delay is shown in figure 89.

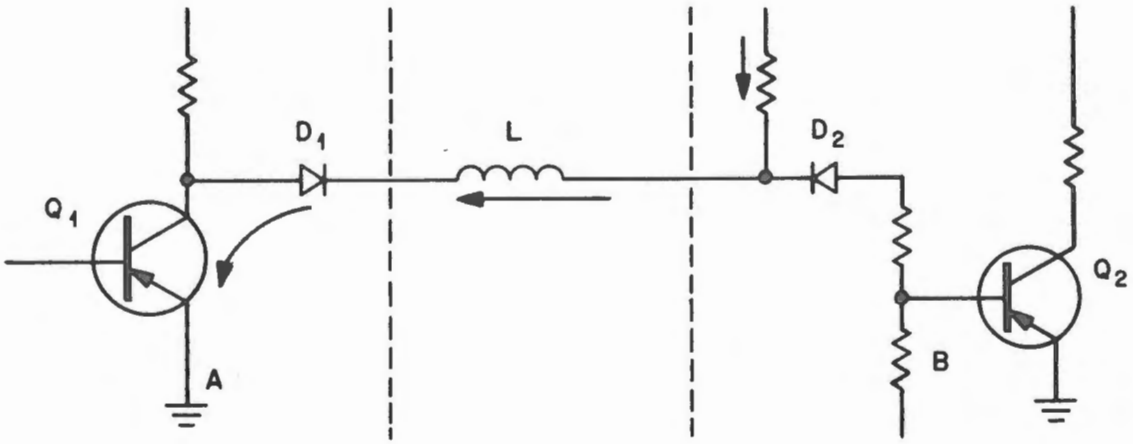


Figure 89. Inductive Delay

If the output of circuit A is a logical 0 of -0.5 volt, Q1 and D1 conduct and current flows through L as indicated in figure 89. The voltage dropped across L is negligible so that the input to circuit B is also -0.5 volt or a logical 0.

The output of circuit A can switch from a logical 0 to a logical 1 instantaneously. When it does, Q1 and D1 stop conducting, but the inductance opposes the drop in current flow and maintains the input to circuit B at a logical 0. However, as current flow drops, input to circuit B rises to a point where D2 becomes forward biased and conducts. At this point, the input to circuit B switches to a logical 1. In this manner, output of circuit A has been delayed.

When the output of circuit A switches back to a logical 0, Q1 and D1 return to conduction, but the rise of current flow is delayed by the inductance. Therefore, input to circuit B is held at a logical 1 for a while.

There are disadvantages to rising inductive delays. One is bringing in the inductance; another is the fact that both 0's and 1's are delayed. Mostly, it is only 1's that require a delay. With this in mind, capacitive delays are preferred.

CAPACITIVE DELAYS

A more effective delay can be realized if the series inductance is replaced by a shunt capacitor. As you may recall, it takes time to charge or discharge a capacitor since it opposes any voltage change. Referring to figure 90, the capacitor charges when the switch is closed to point A, and the voltage across it rises to the battery voltage at a rate determined by C and R. Again, it makes contact with point B, represents a logical 0, then some time after making this contact, the voltage across C drops to a logical 0. An output can be taken from across the capacitor.

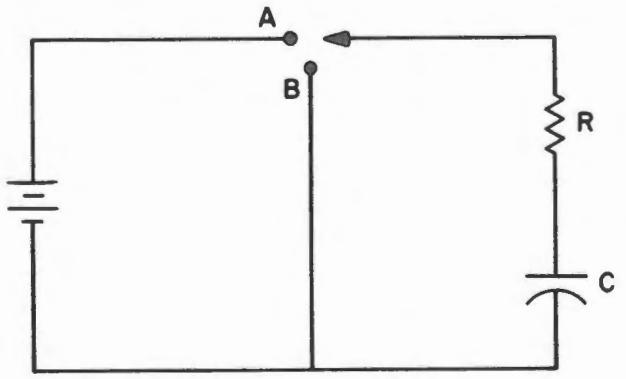


Figure 90. Basic RC Circuit

ADJUSTABLE OR CRITICAL

There are two kinds of capacitive delays used in both the 1604 and the 3000 series logic. One of them is shown in figure 91. For this circuit, assume that circuit A is outputting a logical 0 of -0.5 volt. The capacitor will be charged to -0.5 volt, and this voltage will be at the input to circuit B. When circuit A output switches to a logical 1 of -3 volts, diode D1 goes into reverse bias and is not able to conduct. D2 is also in a nonconducting state, therefore, capacitance C can start charging towards -20 volts through variable resistor R. No matter how long it takes to reach this value, it reaches the threshold voltage of circuit B, and circuit B input switches from a logical 0 to a logical 1. The charge on C is held to -3 volts, and the circuit remains this way until circuit A output switches back to a logical 0. When this happens, D1 and Q1 conduct heavily and form a short or low resistance path across capacitor C which discharges very rapidly. The time required to discharge the capacitor is negligible. Therefore, there is no delay in applying a logical 0 into circuit B from A. The delay is active only when circuit A switches from a logical 0 to a logical 1. The amount of delay is adjustable by varying resistor R.

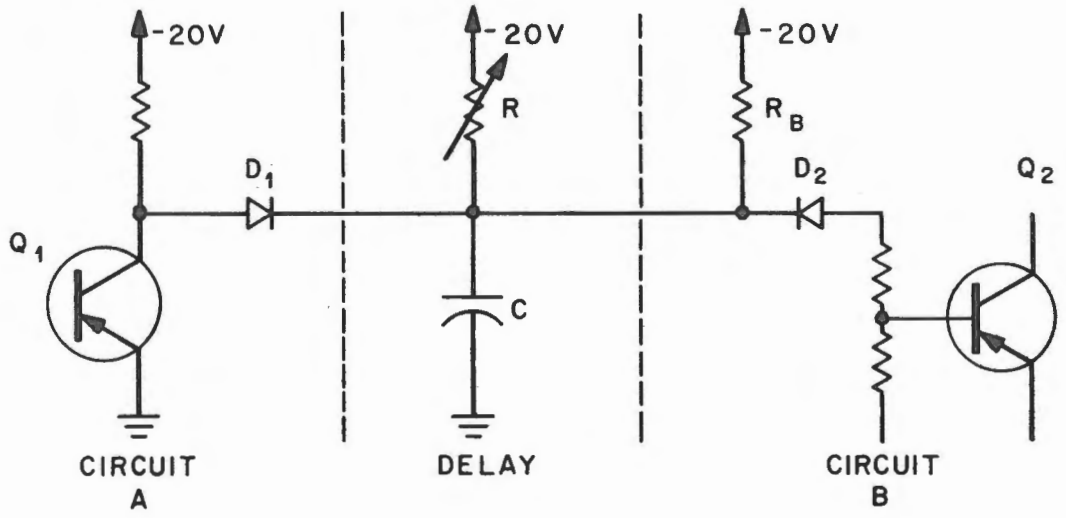


Figure 91. Capacitive Delay

FIXED OR NONCRITICAL DELAY

For a fixed or noncritical delay, the variable resistor R is omitted so that the charge path will be through resistor R_B. This resistor must not be made variable nor should it be changed to vary the delay time. If this is done, incorrect biasing values on Q2 result, and the logic voltage levels at circuit B output are incorrect. Even with this change in charge path of C, the circuit operation remains effectively the same.

PULSE-FORMING NETWORKS

Capacitive delays are used extensively in forming pulses of a required duration. Pulses can be formed when input switches either from a logical 0 to a logical 1 or a logical 1 to a logical 0.

LEADING-EDGE NETWORKS

If an output pulse is required when an input switches from a logical 0 to a logical 1, then a leading edge network must be employed. In figure 92, if the input to J123 is a logical 0, the output of J123 is a logical 1 which holds the output of J789 to a logical 0. There is no inversion between the output and input of a delay card.

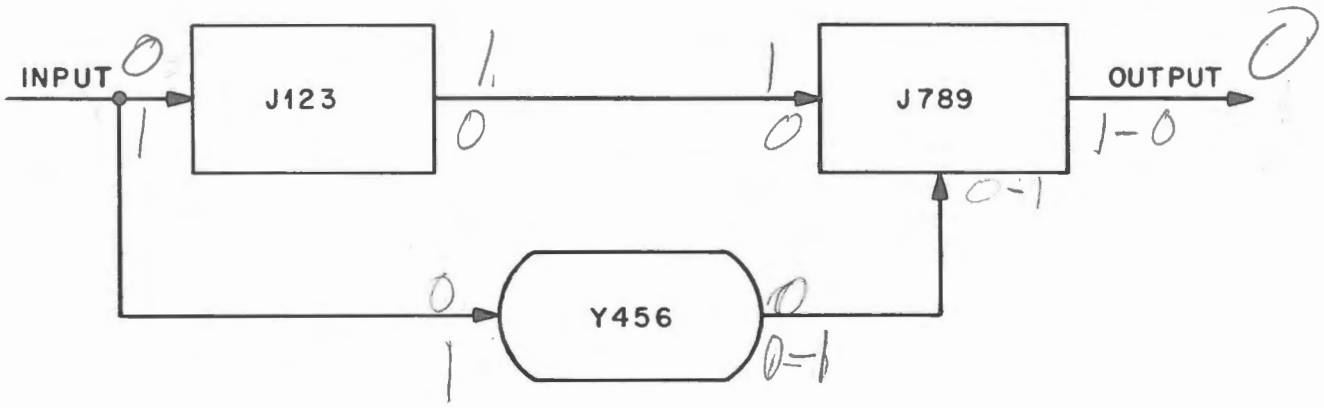


Figure 92. Leading-Edge Network

When the input switches to a logical 1, the output of J123 goes to a logical 0. Although the logical 1 input is applied to Y456, its output remains logical 0 for a while. Therefore, J789 has two logical 0's input and its output will be a logical 1. When Y456 times out, it applies a logical 1 to the bottom input of J789, and J789 output goes back to a logical 0. The length of time that the output is at a logical 1 level is determined by the delay card. On a set of logic prints the delay time is written under the delay symbol.

When the input switches back to a logical 0, the logical 1 output from J123 holds J789 to a logical 0 so that no pulse is produced.

TRAILING-EDGE NETWORKS

If an output pulse is required when an input switches from a logical 1 to a logical 0, a trailing edge network must be used. Refer to figure 93.

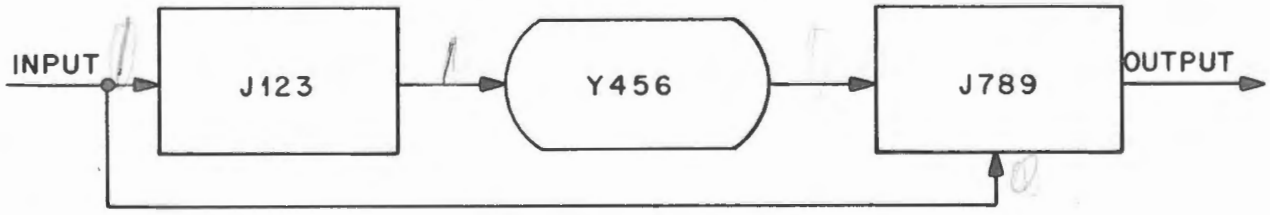


Figure 93. Trailing-Edge Network

Assume the input to J123 is a logical 0. Then its output will be a logical 1. If this is the static condition of the circuit, Y456 will have timed out and a logical 1 input to J789 will hold the output to a logical 0. Even when the input switches to a logical 1, the output will be held to a logical 0 by the logical 1 now applied to the bottom input to J789. The outputs of J123 and Y456 will go to a logical 0 simultaneously.

When the input switches back to a logical 0, the output switches to a logical 1 since both inputs to J789 are logical 0's. After a while, Y456 will time out again, and J789 will drop back to a 0.

REFERENCE 10

REGISTERS

DEFINITION

A register is a group of individual flip-flops used for the temporary storage of data in a computer. Data is stored in the form of logical 1's and 0's called binary digits. The binary number system will be covered later in the course, but for now all you need to know about this system is that it deals with only two digits; 0 and 1. This means that a number such as 1001101001 is called a binary number. Each of the digits is called a bit which is an acronym of the two words BInary digiT. The length of a register is determined by the number of bits it is capable of holding.

TYPES AND USES

Data is stored in a register for a variety of purposes. Some of the registers and their uses are outlined in the following paragraphs:

A REGISTER

The A register is often called the accumulator. It is in the arithmetic section of the computer and is used to hold an operand or to accumulate the results of arithmetic operations. In the Control Data 3000 series computer, this register is 24 bits long.

Q REGISTER

At one time, this register was called the quotient register because it held the quotient following a divide operation. Some systems still retain this function for the Q register. The Q register in the Control Data 3000 series computer is 24 bits long and is called the auxiliary arithmetic register. It works in conjunction with the A register to hold the least significant bits of operands that are too big to fit in the A register. Registers A and Q are often used together forming one big 48-bit register referred to as the AQ register.

P REGISTER

Although listed as a register, the P register is often, and more correctly called the program address counter. Instructions and data are stored in separate locations in computer memory. Each location is assigned an address in much the same way as houses along a street are assigned addresses. To solve a problem, instructions must be executed sequentially. It is the job of the P register to keep track of the addresses of the instructions so that they can be executed in the correct sequence. It is 15 bits long.

F REGISTER

The F register which is 24 bits long is used to hold an instruction while it is being analyzed for execution. Each instruction has its own numerical code contained in the upper 6 bits. The lower 18 bits contain other information pertinent to the instruction.

C REGISTER

This register is also 24 bits long and is called the Communications register. All data entered into the computer via the keyboard goes to the C register first so that the operator can check to see that it is correct.

The contents of any memory location can be brought into the C register to be examined.

B REGISTER

There are three B or Index registers in the 3000 series of computers. Each one is 15 bits long and is used in a process called indexing or address modification. This process will be covered in programming.

STORING A NUMBER

To find out what number is being stored in a register, we look at the set side outputs of all the flip-flops. As you may recall, when a flip-flop is set there is a logical 1 on the set side output. In this condition, it will be storing a binary 1. When a flip-flop is clear, a logical 0 appears on the set side output, and it is storing a binary 0.

One flip-flop then has two possible conditions and can store two possible numbers; either a logical 0 or a logical 1. Two flip-flops can store four numbers; 0, 1, 2, and 3. Three flip-flops can store eight numbers; 0 through 7.

In seeing how this is done, remember that a set flip-flop stores a 1 and a clear flip-flop stores a 0. Now look at Table 13. It represents a group of three flip-flops having a total of eight possible combinations representing numbers 0 through 7.

TABLE 13. STORING A NUMBER

CONDITION OF FF	BINARY EQUIVALENT	ACTUAL NUMBER
ccc	000	0
ccs	001	1
csc	010	2
css	011	3
scc	100	4
scs	101	5
ssc	110	6
sss	111	7

If another group of three flip-flops is added, there would be a total of 64 possible combinations to represent 64 different numbers. There is, however, something strange occurring.

There are six flip-flops in the register shown in figure 94; three in group A and three in group B. Suppose all the flip-flops in group A are set and the group holds a 7. The next number would normally be 8. Flip-flop 1 in group B sets, however, and that group holds a 1. All the flip-flops in group A clear so that group holds a 0. Therefore, the number following 7 is 10. It appears that 7 plus 1 equals 10 rather than 8. Closer examination of this 6-bit register will show that it can not hold any number involving 8 and 9; i.e., no 18 or 19, 28 or 29, etc. This involves another number system that you will learn later called the octal system. Add 7 and 3 and see if you can come up with 12.

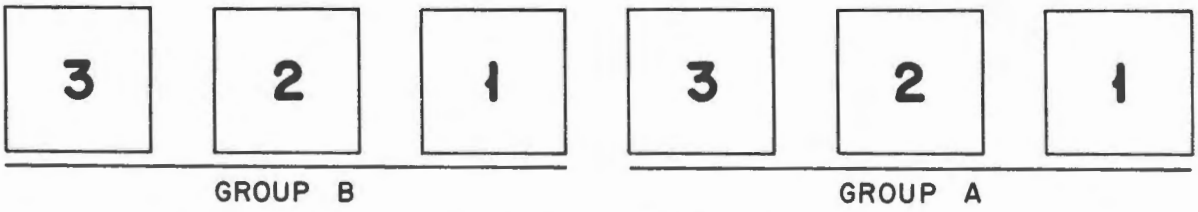


Figure 94. 6-Bit Register

METHODS OF TRANSFER

There are four methods that can be used in transferring data into a register from another place in the computer such as memory or another register.

ONES TRANSFER

Assume K000/001 is set and K010/011 and K020/021 are clear in figure 95. In order to transfer this data from rank I to rank II, clear all flip-flops in rank II, and then apply a transfer pulse to all AND gates. Because K000/001 is set, the logical 1 from the set side output will complete the bottom AND gate and cause K500/501 to set. Since K010/011 and K020/021 are both clear, 0's will be on the set side outputs and the top two AND gates will be broken. Therefore, K510/511 and K520/521 will remain clear. The data held in rank I has now been transferred into rank II through a transfer of 1's.

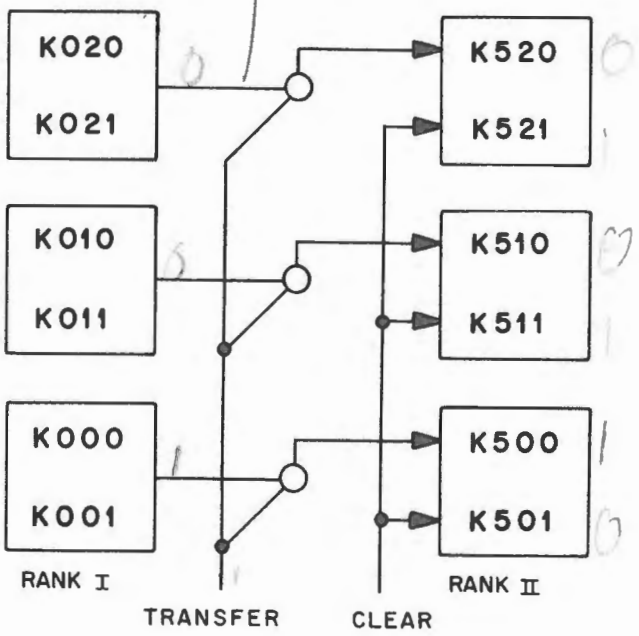


Figure 95. Ones Transfer

ZEROS TRANSFER

Assume the same conditions as are given for rank 1 in figure 96. First, a set pulse will set all flip-flops in rank II. When the transfer pulse is applied, the bottom AND will be broken by the 0 on the clear side of K000/001. The top two AND gates will be made this time since K010/011 and K020/021 are both clear, and K510/511 and K520/521 will both clear. Rank II again has the same data as rank I following a transfer of 0's.

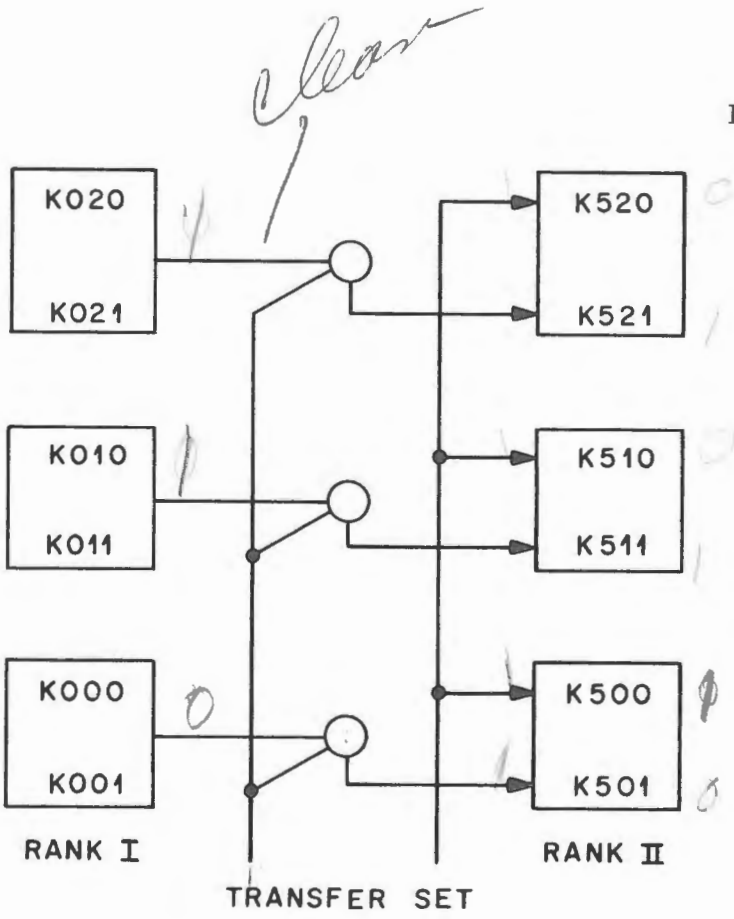


Figure 96. Zeros Transfer

FORCED TRANSFER

The forced transfer shown in figure 97 is perhaps the simplest. Assuming the same data as before in rank I, when the transfer pulse is applied AND gates 2, 3, and 5 will be made, while AND gates 1, 4, and 6 will be broken. Rank II is then forced to the same condition as rank I. If the data is changed in rank I, it will not change in rank II until the next transfer pulse is applied.

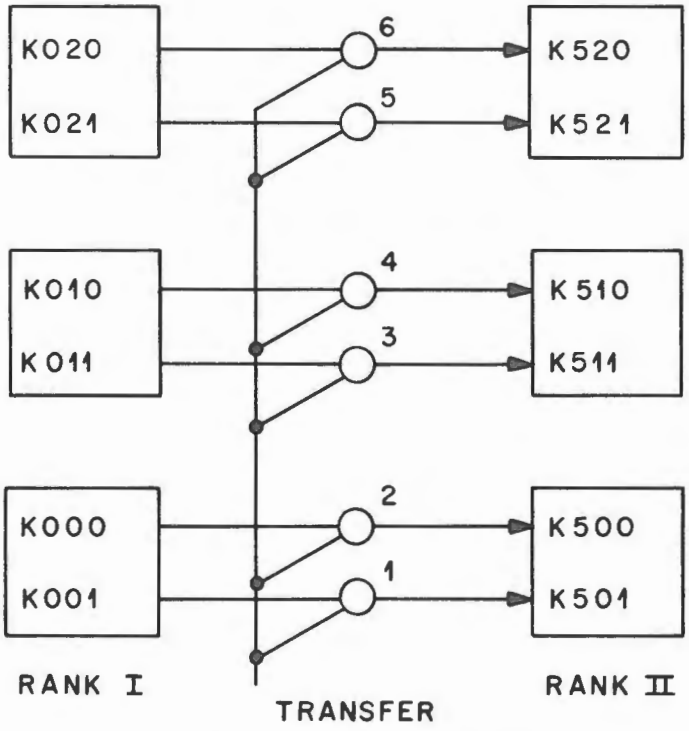


Figure 97. Forced Transfer

COMPLEMENT TRANSFER

The complement transfer shown in figure 98 is similar to the forced transfer. After the transfer pulse is applied, the complement of rank I is forced into rank II.

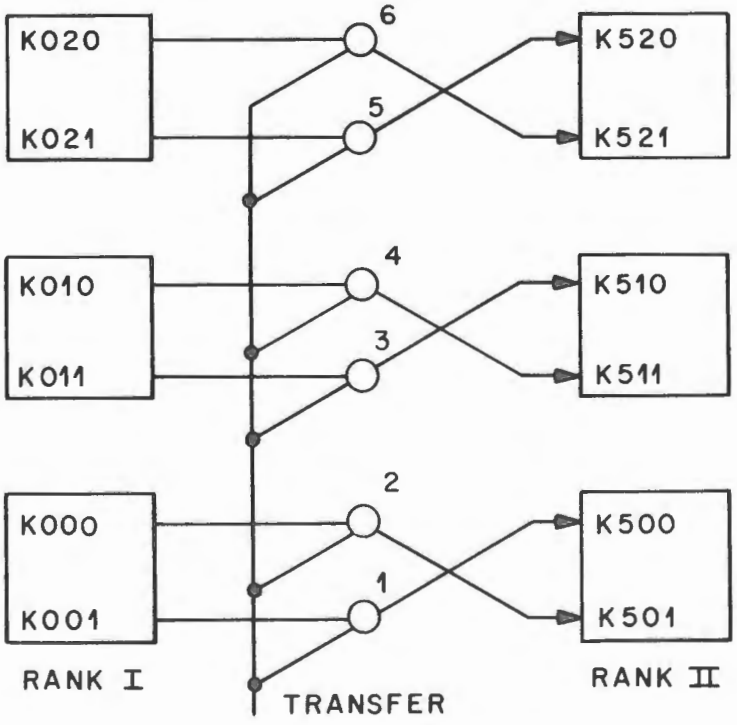


Figure 98. Complement Transfer

REFERENCE 11

CLOCK PYRAMIDS

MASTER OSCILLATOR

The heart of a digital computer timing system is the clock oscillator. All operations performed by a computer are accurately timed by pulses produced by this circuit. With high speed computers, these circuits are a necessity, RF oscillators operating in the range of 1 through 10 megacycles per second. Any of the three basic circuits can be used; the Armstrong, Hartley, or Colpitts. For example, the Control Data 1604 computer uses a type of Hartley circuit for its clock oscillator and the 3100 uses a variation of the Armstrong oscillator.

Regardless of the type of circuit used, the circuit configuration will invariably be push-pull. This will provide two outputs, each of which is 180 degrees out of phase with the other. These are then used to provide odd and even clock pulses.

In the circuit shown in figure 99, the oscillatory tank circuit is formed by C01, 800 pf, and the center-tapped inductance. The circuit is tuned to a frequency of 6 megahertz in the 3100 computer so that the period of one cycle is 166.6 nanoseconds.

If this circuit is to be used as a master clock oscillator, pin 13 or 14 will be connected to pin 6 and pin 2 or 3 will be connected to pin 10 to form a push-pull Armstrong oscillator. A 6-megahertz crystal can be connected in series with one of the leads to improve frequency stability. If the circuit is to be used as an amplifier, these connections are omitted.

The output at pin 1 is a voltage that varies from +1 volts to -7 volts, and can be used as a logic voltage. The output at pin 15 has the same voltage levels but is 180 degrees out of phase with the output at pin 1. The outputs at pins 4 and 12 are used when it is necessary to maintain an in-phase condition between all amplifiers in the same rank. The outputs at pins 2 and 3 and at 13 and 14 are used for connection to amplifiers in the next rank.

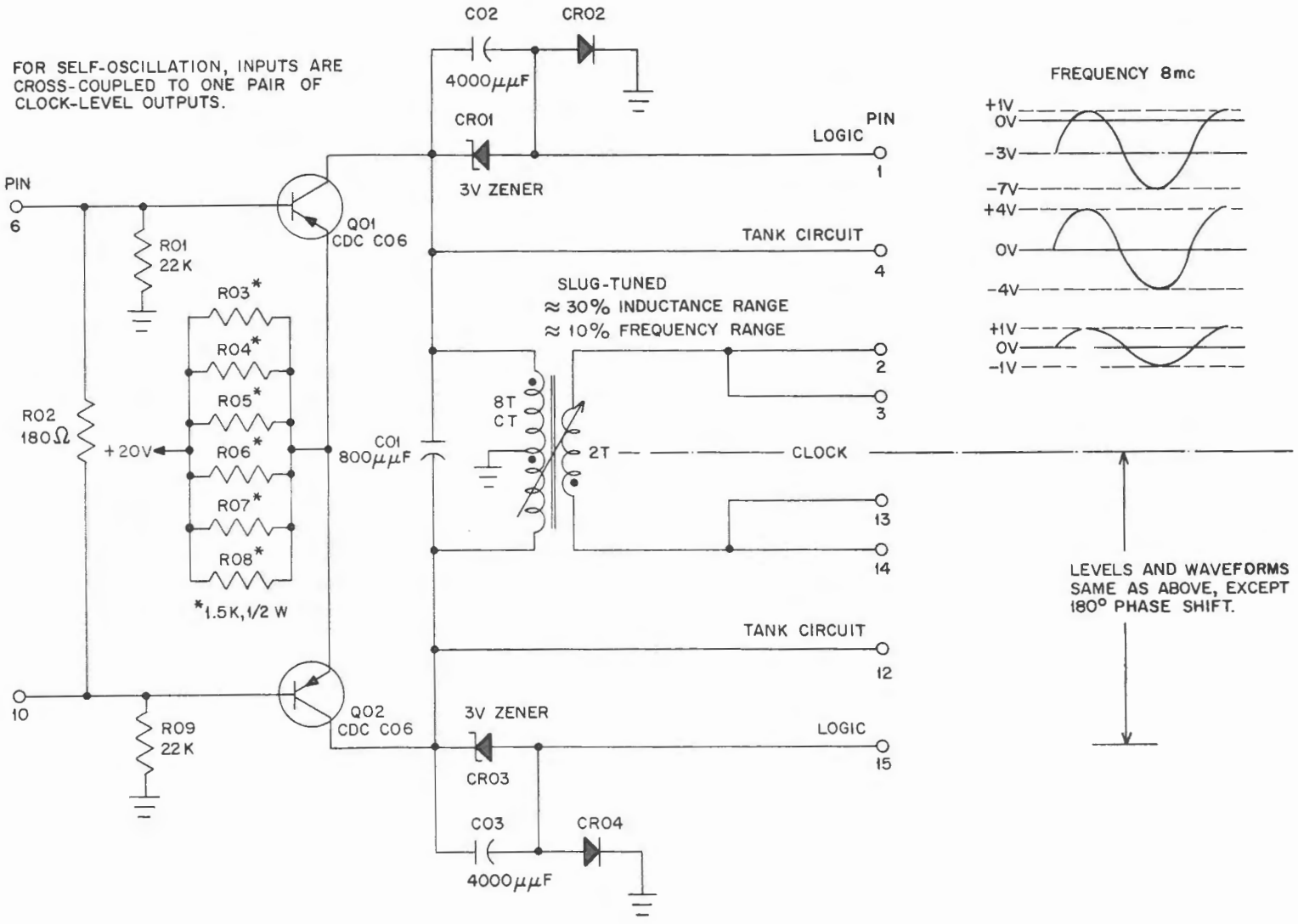


Figure 99. Clock Oscillator

PYRAMID

Many different sections of a computer use pulses derived from the clock oscillator. Perhaps over one hundred circuits require clock pulses for timing. To connect this many circuits to an oscillator would place too heavy a load on it and cause it to stop working. Therefore, a system of amplifiers that are connected to form a pyramid is used.

The clock oscillator drives just two RF amplifiers placing a light, unvarying load on it and allowing it to function normally. The amplifiers used in the pyramid are allocated to ranks; thus, rank I will contain two amplifiers. Each of these will drive an additional four so that rank II contains eight amplifiers. This pyramid continues with each amplifier driving four others. Rank III contains 32 amplifiers and rank IV has 128. Thus, the numbers of clock amplifiers would be, from rank I to rank IV; 2, 8, 32, and 128. This is the maximum for each rank, respectively. However, each rank may not contain the maximum number of amplifiers if the maximum outputs are required. The diagram in figure 100 shows how a pyramid is formed.

The output signals of each amplifier in any rank are all in phase with the others of the same rank, but they are not necessarily in phase with the output of the amplifiers in another rank.

CLOCK SLAVES

Outputs are taken from amplifier circuits in rank IV and are called raw clock pulses. These are sine waves of which two are taken from each amplifier card. They are 180 degrees out of phase with each other and provide odd and even raw clock pulses. The voltage levels of these pulses are from +1 volts to -7 volts so when a raw clock signal goes through its negative half-cycle, it could be compared to a logical 1.

When raw clock pulses are applied to an inverter, the output will be a chain of square wave pulses varying between the logic levels of the computer. These inverters are called clock slaves; their outputs are called phase times. Clock slaves are denoted by N terms, and the three digit number will show whether the output will be at an even phase time or an odd phase time. Figure 101 shows a typical arrangement.

C480 is the output of a clock amplifier in rank IV of the pyramid. Since it is an even term, it will be at a logical 1 level at even raw clock time. At this time N050 will be a 0. When C480 goes to a logical 0 at odd raw clock time, N050 will output a logical 1 denoting that this is even phase time.

In conclusion it can be said that raw clock pulses and phase times are 180 degrees out of phase with each other. Even phase time is a logical 1 at odd raw clock time; odd phase time is a logical 1 at even raw clock time.

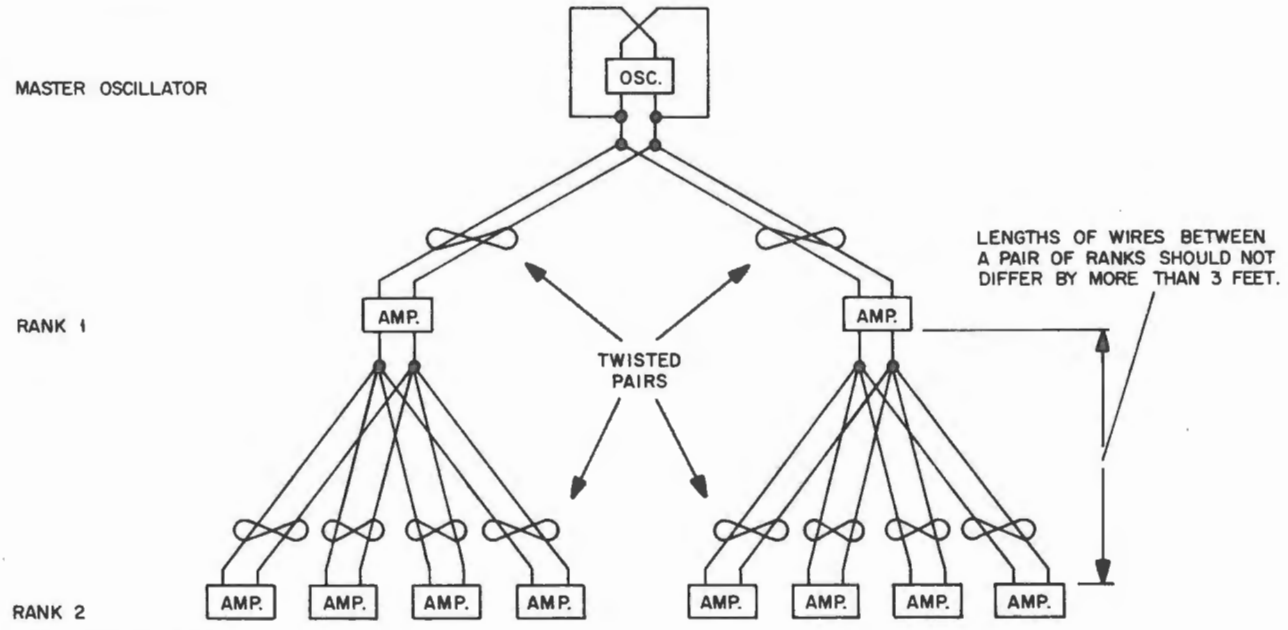


Figure 100. Clock Pyramid

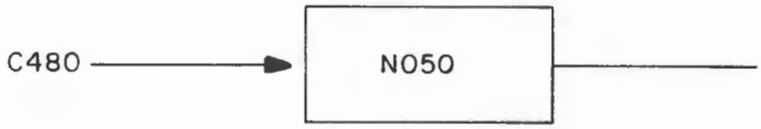


Figure 101. Clock Slave

REFERENCE 12

CONTROL DELAY

FUNCTIONS OF CONTROL DELAY

The control delay is a combination of three interconnected inverters with additional clock inputs from the master clock circuit. Its function is to delay a logical 1 input for a controlled amount of time.

The computer is able to execute instructions by performing various operations in a logical sequence. Interconnected control delays form a timing chain to which a logical sequence of events may be synchronized. The delay time, using 3100 logic, is 83.3 nanoseconds. All control delays in the computer are synchronized by the same master clock to ensure constant delay times. Less expensive RC delays could be used, but variations in delay times would present timing problems.

Inputs to control delays are normally present for one phase time and are usually synchronized by the output of a preceding control delay. Figure 102 illustrates a typical configuration. Notice that term numbers alternate; even, odd, even.

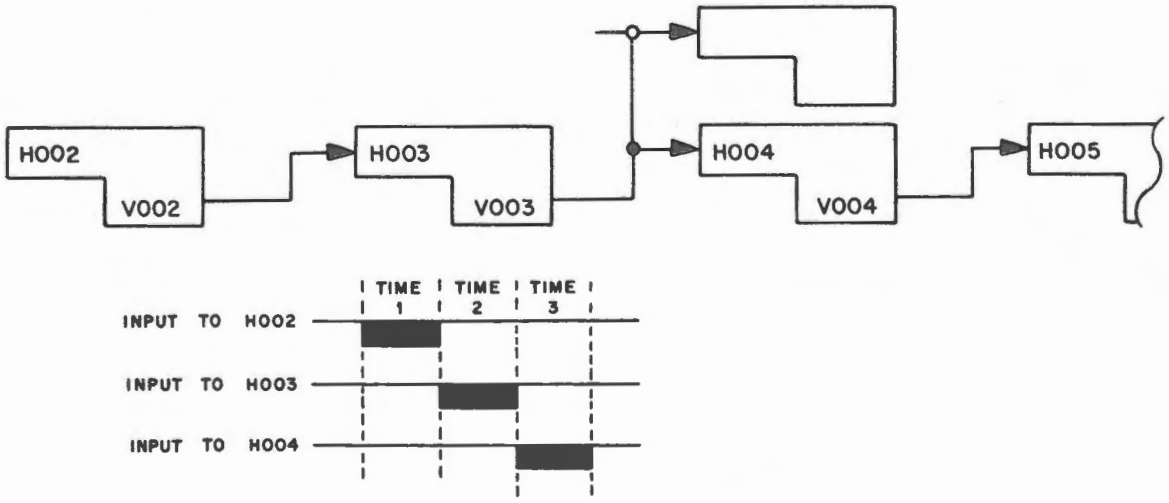


Figure 102. Control Delay Network

CLOCK PULSES

The master clock oscillator drives a parallel string of clock amplifier cards, type C01. If the output is taken directly from the C01 card, it is referred to as a raw clock. If the C01 card feeds a standard inverter, the inverter is referred to as a clock slave. Due to the inverter switching time, slave outputs delay the raw clock by 20 nanoseconds.

The alternating pulses from the raw clock are referred to as odd and even. A raw clock odd will have a logical 1 output at even time and a logical 0 output at odd time. The same relationship holds true for the raw clock even. Refer to figure 103.

Most CXXX terms in the computer are raw clock outputs with the exception of communication register terms. A clock slave term, however, is usually an NXXX term.

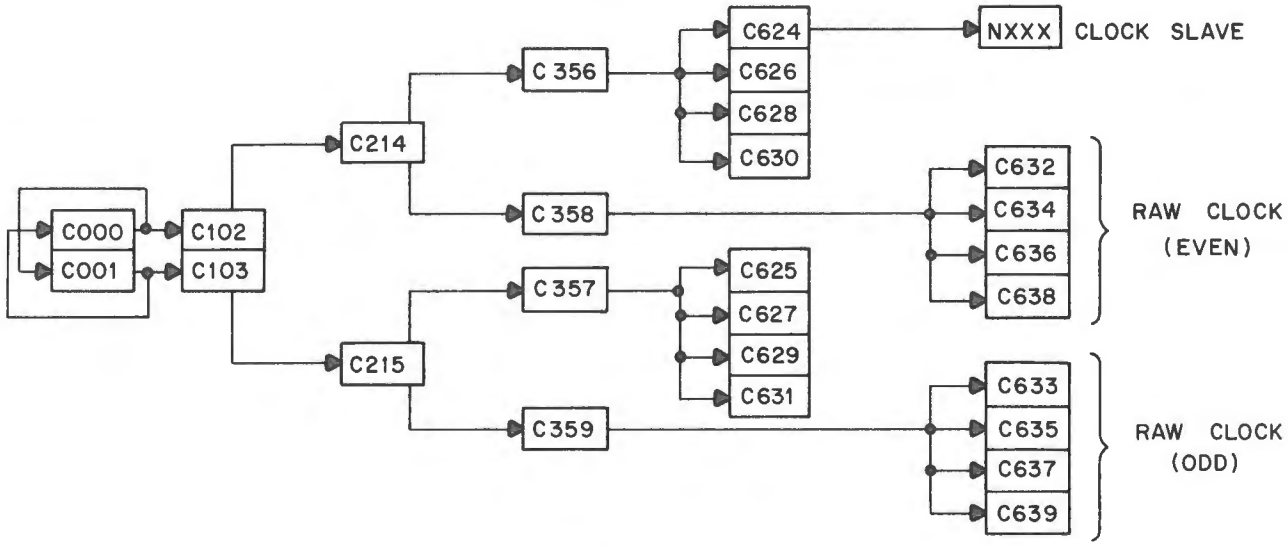


Figure 103. Master Clock Pyramid

DESCRIPTION

The control delay consists of flip-flop HOOO which has its feedback ANDed with a raw clock signal plus one or more inverters such as VOOO or NOOO. Each inverter has two ORed inputs; one from the A section of the flip-flop and the other from a raw clock. Refer to figure 104.

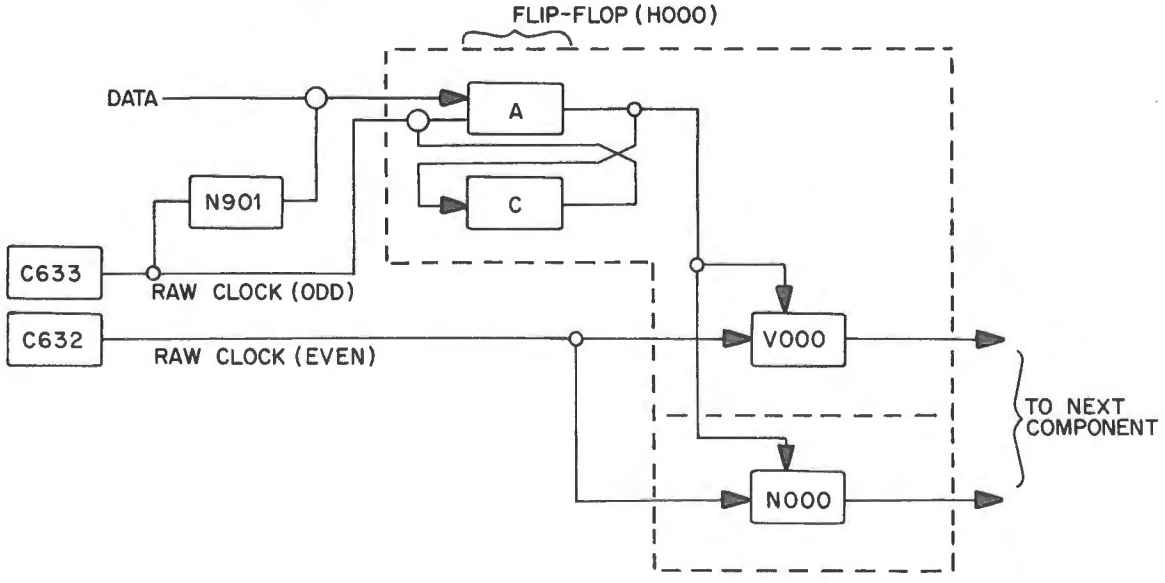


Figure 104. Even Control Delay

Because the preceding control delay is even (HOOO, VOOO), the data input must be at an odd time, and the output will occur during the following time which is even. The overall circuit does not invert the input, but it provides an 83.3-nanosecond delay between input and output.

The clock inputs to a control delay are not shown on logic diagrams. All even control delays will have the same inputs as figure 104. The two raw clock terms would be reversed for an even time.

CIRCUIT OPERATION

For circuit operation, refer to figure 104.

The basic operation of the control delay is as follows:

1. Set the flip-flop for two phase times.
   a. Set by using data pulse during first phase time.
   b. Latch up by the odd clock during second phase time.
2. Enable the output. While the flip-flop is set, the side output will be a logical 0. During the second phase time when the even clock is also a logical 0, inverters VOOO and NOOO will produce logical 1's out.
3. Clear the flip-flop. During the third phase time, the data pulse will be absent breaking the associated AND gate, and the odd clock will be a logical 0 breaking its associated AND gate. Inverter A will output a logical 1 which effectively produces a clear input to the flip-flop. The logical 1 output from inverter A prevents further outputs from the control delay.

Figure 104 and figure 105 should aid in understanding the actual circuit operation of the control delay. Figure 105 illustrates the quiescent condition and then the series of events as the data pulse is applied.

Prior to the arrival of the data pulse, both inputs to inverter A are logical 0's and it outputs a logical 1. This forces logical terms out of inverter C and VOOO and NOOO.

The data pulse arrives, and 20 nanoseconds later N901 outputs a logical 1 forming the AND gate and providing the set input to the flip-flop. Inverter A outputs a logical 0 allowing inverter C to output a logical 1. VOOO and NOOO can not output logical 1's because the even clock is a logical 1 during phase time (odd).

During the next phase time, the flip-flop latches by forming the odd clock and inverter C AND gate. This keeps inverters A and C in the same condition as during the previous phase time. VOOO and NOOO now output a logical 1 because both the even clock and inverter A outputs are logical 0's.

The flip-flop clears during the next phase time odd because the absence of an input data pulse breaks that AND gate, and the odd clock is now a logical 0 breaking the feedback AND gate. Inverter A outputs a logical 1 forcing 0's out of VOOO, NOOO, and inverter C.

Another data input at some later time would reinitiate the entire sequence of events. If the data pulse is a continuous signal, the control delay would output pulses at every even time.

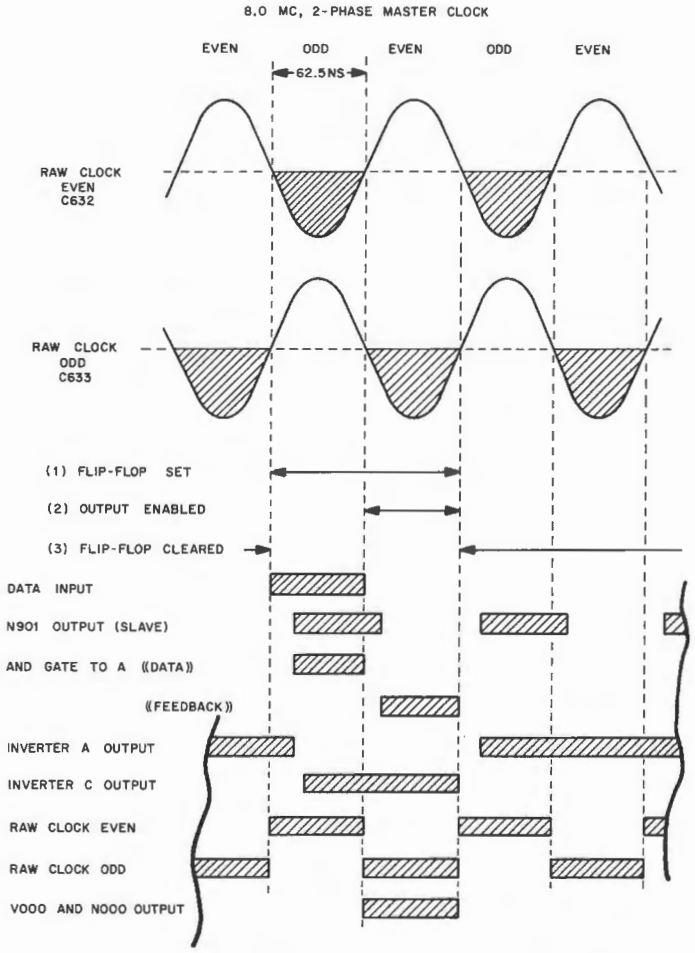


Figure 105. Control Delay Timing

REFERENCE 13

COUNTERS

BINARY COUNTING

Imagine that there is a counting device with three display windows such as that given in figure 106 and that each window can display only a 0 or a 1. On the right side is a lever with which the counter can be advanced one unit at a time. Starting at 0 the counter is cleared. Pressing the lever at the side advances the counter, and window C shows a 1. By pressing the lever a second time, C will return to 0 while window B advances a 1. The third time the lever is pressed, B stays at 1 and C displays a 1 again. So as the lever continues to be pressed, the count advances as shown in figure 107. Notice that on the count of three the display is 011. On the fourth count, A goes to a 1, while B and C both go to 0's. On the seventh count the display is 111. When the lever is pressed for the eighth time, all displays return to 000 to begin again.

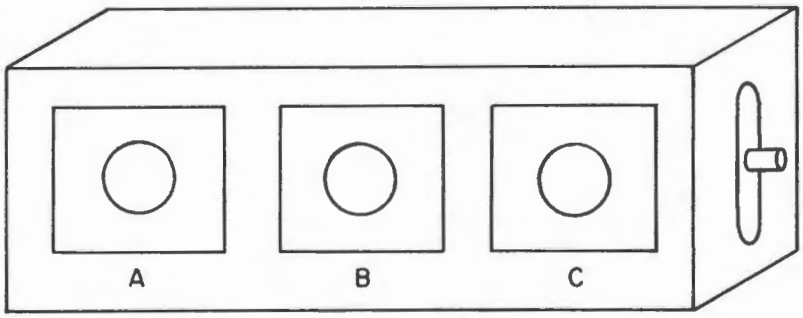


Figure 106. Mechanical Counter

COUNT	WINDOW DISPLAY		
	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Figure 107. Counter Display

TWO-STAGE, SINGLE-RANK COUNTER

Figure 108 shows a two-stage binary counter. When both flip-flops are cleared, AND gate 2 is partially enabled so that when the first advance pulse is applied, K000/001 sets and K010/011 remains clear.

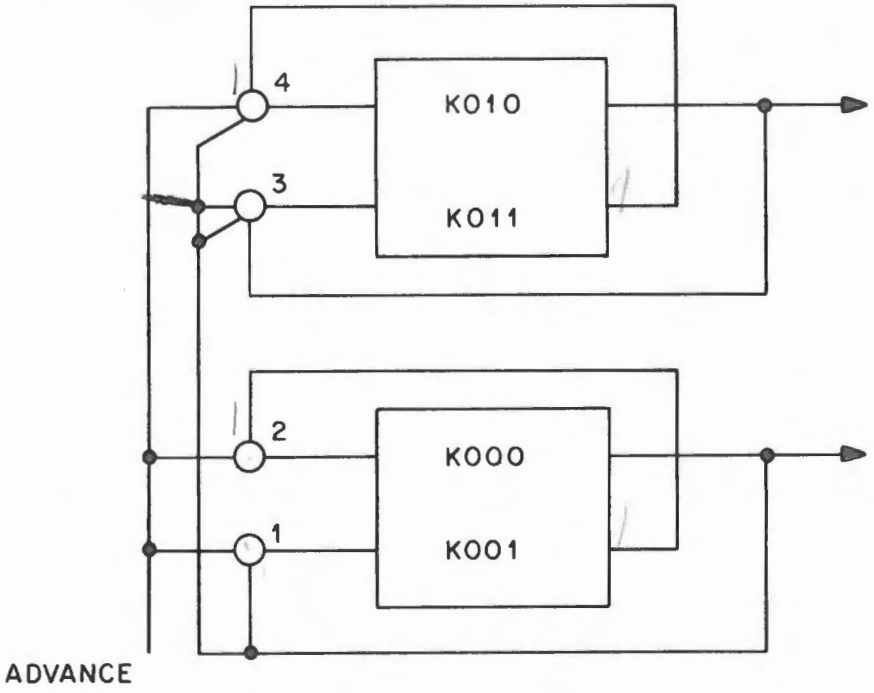


Figure 108. Two-Stage, Single-Rank Counter

At this time, AND gates 1 and 4 are partially enabled, while AND gates 2 and 3 are disabled. When the second advance pulse comes up, K000/001 clears and K010/011 sets.

Gate 2 is again partially enabled and gates 1, 3, and 4 are disabled. When the third pulse comes, K000/001 sets so that both flip-flops are set indicating that the count is 3.

Gates 1 and 3 are partially enabled, and gates 2 and 4 are disabled so that on the fourth pulse both flip-flops clear. The cycle is repeated on succeeding counts.

The single-rank counter has a serious disadvantage in that the circuit transistors switch so rapidly that incorrect counting results. The transistors switch states before the advance pulse drops causing a double count. One way of eliminating this problem is to use a double-rank counter.

THREE-STAGE, DOUBLE-RANK COUNTER

A three-stage, double-rank counter is essentially a double-rank register which increases or decreases the quantity stored in a single increment at a time. The three-stage counter circuit shown in figure 109 is additive from binary 000 through 111.

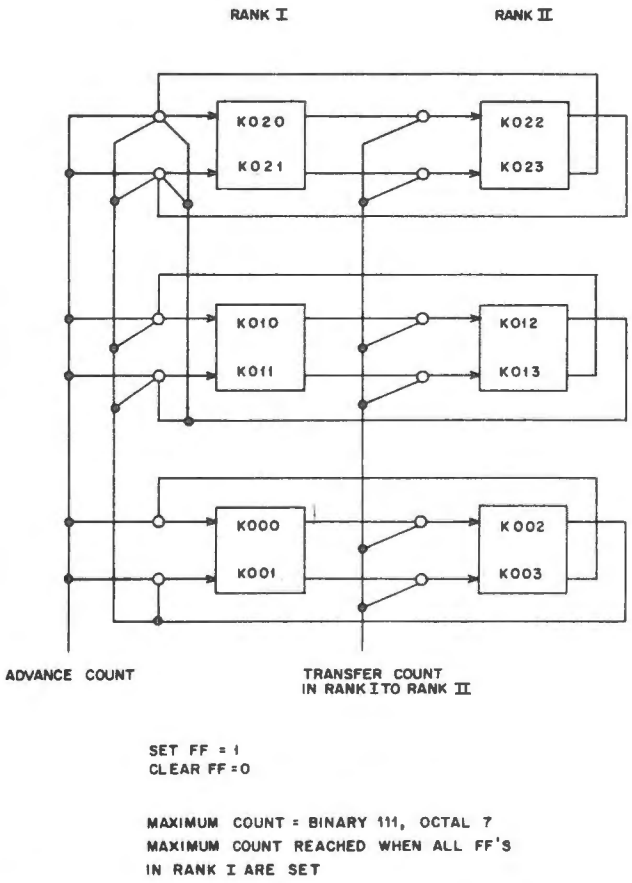


Figure 109. Three-Stage, Double-Rank Counter

A count is stored in two steps. In the first step a logical 1 input on the advance line sets a flip-flop in rank I. This occurs consecutively, and when all three are set, the next input clears them.

During the second step, a logical 1 input on the transfer line causes the flip-flops in rank II to assume the identical states of their corresponding flip-flops in rank I.

To analyze the operation of the counter, assume that both ranks are initially cleared so the count stored is 0. The first advance command finds the AND gate to K000 enabled, and, therefore, enters the count 001 or an octal 1 into rank I. This partially enables the AND gate to K002 so that the transfer command enters the count 001 into rank II. The next advance command finds the AND gate to K001 and K010 enabled. It, therefore, enters count 010 or octal 2 into rank I. The operation continues in this manner as shown in Table 14 until the count reaches 111 or octal 7 which is the highest possible count in a three-stage counter. This is followed by a command sequence that returns both ranks to count 000.

TABLE 14. COUNTING SEQUENCE FOR THREE-STAGE COUNTER

COMMAND	QUANTITY STORED (OCTAL)	RANK I			RANK II		
		K02-	K01-	K00-	K02-	K01-	K00-
Initial Conditions	0	0	0	0	0	0	0
Advance	1	0	0	1	0	0	0
Transfer		0	0	1	0	0	1
Advance	2	0	1	0	0	0	1
Transfer		0	1	0	0	1	0
Advance	3	0	1	1	0	1	0
Transfer		0	1	1	0	1	1
Advance	4	1	0	0	0	1	1
Transfer		1	0	0	1	0	0
Advance	5	1	0	1	1	0	0
Transfer		1	0	1	1	0	1
Advance	6	1	1	0	1	0	1
Transfer		1	1	0	1	1	0
Advance	7	1	1	1	1	1	0
Transfer		1	1	1	1	1	1
Advance	0(or8)	0	0	0	1	1	1
Transfer		0	0	0	0	0	0

GRAY CODE COUNTER

The two preceding counters are called sequential counters because they count in sequence; i.e., 0, 1, 2, 3, 4, etc. The next two counting devices are nonsequential. The gray code counter is a system of binary counting wherein only one bit changes with each count. For example, in going sequentially from 3 to 4, the binary count would go from 011 to 100. All three bits have changed. However, in going nonsequentially, i.e., from 3 to 7, the binary count would be from 011 to 111.

There are many possible combinations of numbers that can form a gray code. To assist in finding these numbers, a simple diagram has been devised. Refer to figure 110.

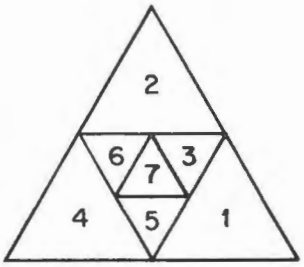


Figure 110. Gray Code Triangle

Zero is any point outside of the main triangle. To find a group of numbers, draw a line from 0 passing it through all triangles. The line must pass through the sides and not through the angles. Refer to figure 111.

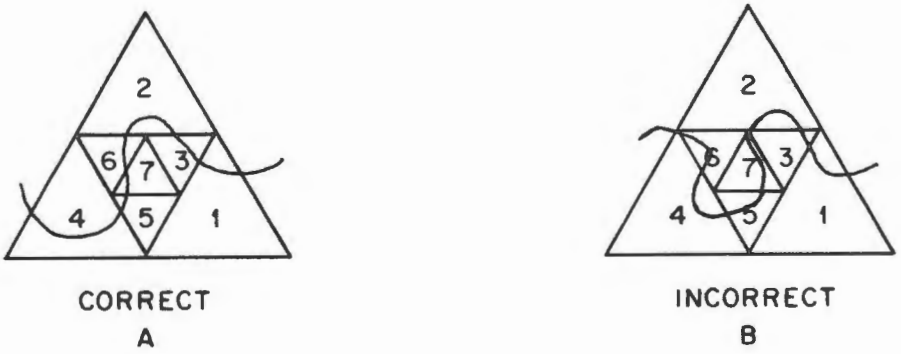


Figure 111. Triangle Use

The correct method shown in figure 111 (A) reveals a group of numbers 0, 1, 3, 2, 6, 7, 5, 4. If these are converted to binary and examined, you will see that only one bit changes with each count. Refer to Table 15.

TABLE 15. CORRECT USE OF GRAY CODE TRIANGLES

NUMBER	BINARY
0	000
1	001
3	011
2	010
6	110
7	111
5	101
4	100
0	000

If, however, the other diagram is analyzed, it produces Table 16.

TABLE 16. INCORRECT USE OF GRAY CODE TRIANGLES

NUMBER	BINARY
0	000
1	001
3	011
2	010
7	111 *
5	101
4	100
6	110
0	000 *

The diagram in figure 112 is wired for the sequence shown in Table 15, Table 16, and Table 17 will indicate the counting operation.

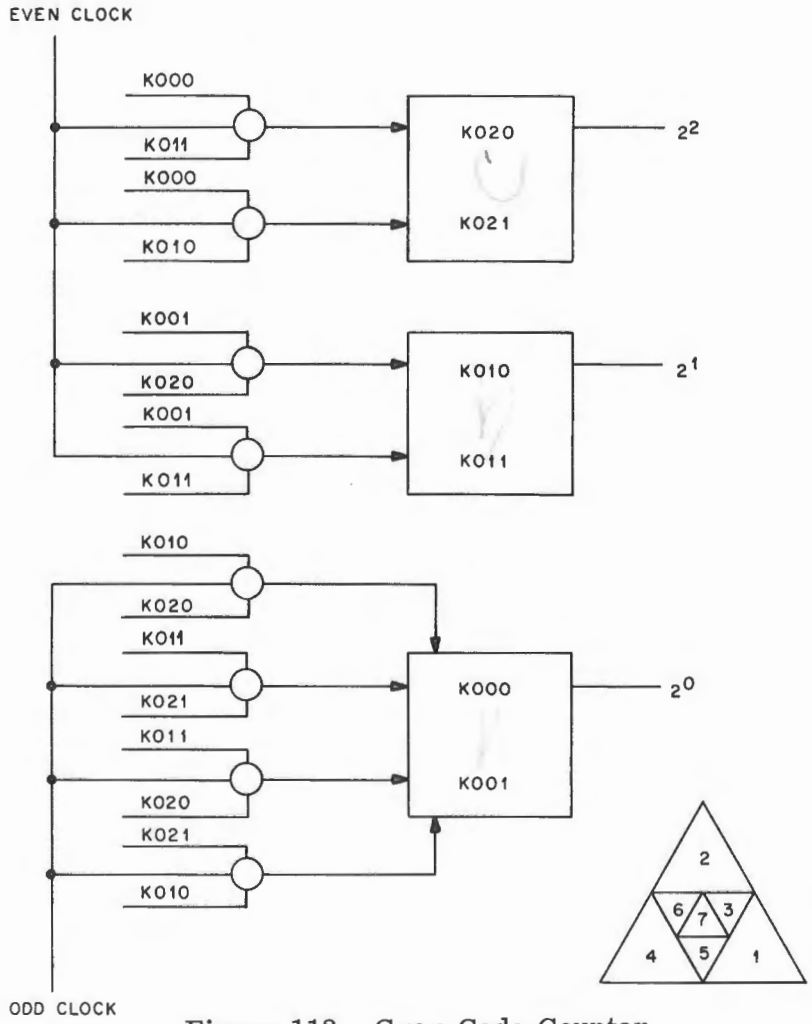


Figure 112. Gray Code Counter

*Two bits change. This does not conform with gray code specifications.

TABLE 17. COUNTING OPERATION

TIME	K021	K011	K001	ADVANCE
INITIAL	0	0	0	
ODD	0	0	1	1st
EVEN	0	1	1	2nd
ODD	0	1	0	3rd
EVEN	1	1	0	4th
ODD	1	1	1	5th
EVEN	1	0	1	6th
ODD	1	0	0	7th
EVEN	0	0	0	8th

RECYCLING COUNTER

Recycling counters are used in many applications to provide timing pulses that occur one after another. In the circuit of figure 113 the two flip-flops K000/001 and K010/011 are connected together with capacitive delays in each lead.

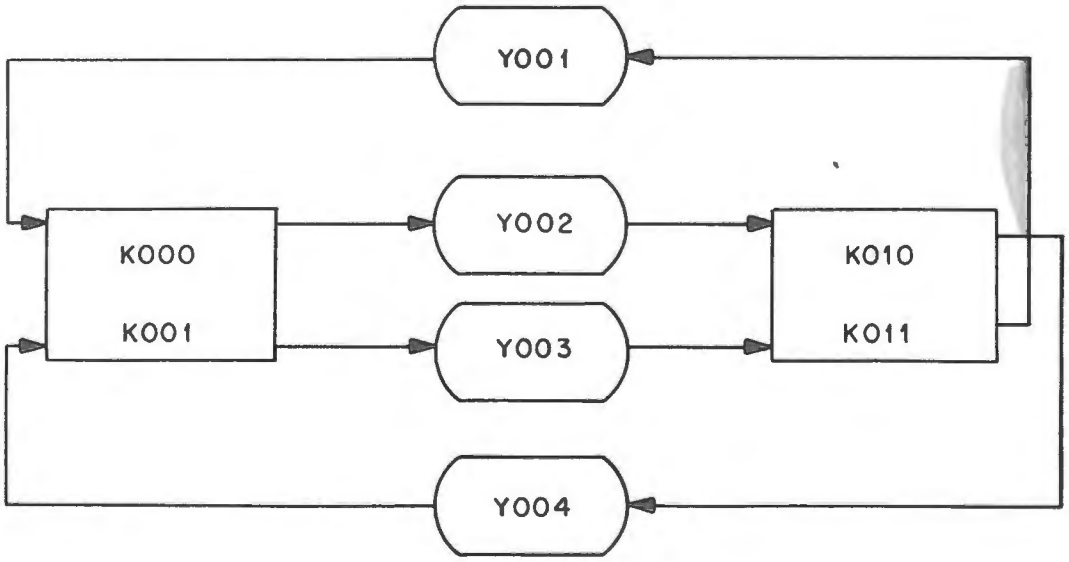


Figure 113. Recycling Counter

Starting with both flip-flops cleared, the sequence of operations is as follows:

1. The output of K010 is a logical 1.
2. Input to set side of K000/001 is delayed by Y001.
3. K000/001 sets when Y001 times out.
4. A logical 1 input to set side of K010/011 is delayed by Y002.
5. K010/011 sets when Y002 times out.
6. A logical 1 input to clear side of K000/001 is delayed by Y004.
7. K000/001 clears when Y004 times out.
8. A logical 1 input to clear side of K010/011 is delayed by Y003.
9. K010/011 clears when Y003 times out.

This cycle is repeated for as long as power is applied.

To obtain the required timing pulses, the set and clear outputs of the flip-flops are applied to a set of four inverters. See figure 114.

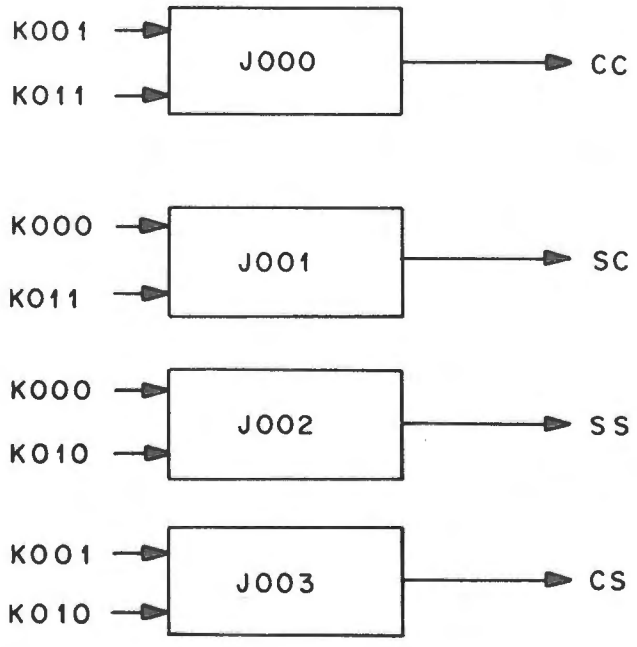


Figure 114. Translator

Each of the inverters will output a logical 1 for each condition of the flip-flops shown at the right. For each of these conditions, the inputs to the inverters are both 0's.

REFERENCE 14

SHIFT NETWORKS

SHIFT NETWORK APPLICATION

For various reasons, the shift network is often required to manipulate data in a register or a memory location so that it can be used more than one way. Two examples, which you will learn about during your study of software are: 1) changing a word address into a character address and vice versa and 2) changing the result of an arithmetic operation into a suitable code so that it can be printed out by a peripheral equipment such as a typewriter or a line printer.

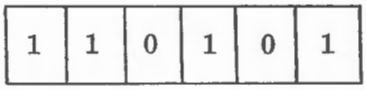
Shifting data in a register also provides a means and only a means of multiplying or dividing.

BASIC SHIFT OPERATIONS

Figure 115 (A) shows the contents of a register before a left shift is made, and figure 115 (B) shows the contents after the left shift. During the shift, all bits are shifted one place to the left. The uppermost bit does end around and into the least significant bit position dividing the numbers into groups of three and converting them to octal. The register held the octal number 23 before the shift and 46 after the shift. As you can see, shifting the number one place to the left has resulted in multiplying it by 2, but this does not always work. See figure 116. Sixty-five times 2 is not equal to 53; therefore, in this instance, the multiplication does not work.

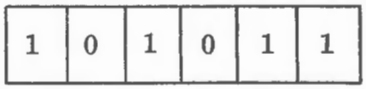
BEFORE (A) AFTER (B)

Figure 115. Left Shift, Zero End-Around



= 65

BEFORE



= 53

AFTER

Figure 116. Left Shift, One End-Around

In shifting the contents of a register to the right, as shown in figure 117 (A) and 117 (B), the least significant bit is discarded. The number started out as 23 again and following the right shift, the result is 11. This, of course, is division by 2 with the 1 remainder discarded. Even with the number 65, following right shift we get 32 with a discarded 1 remainder. The divide operation falls apart at the seams, however, if sign extension is specified.

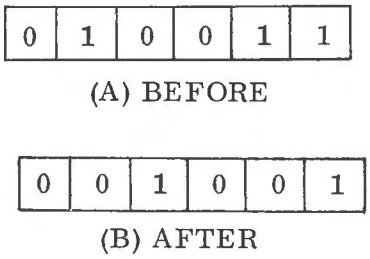


Figure 117. Right Shift

SIGN EXTENSION

A computer can not store positive and negative numbers per se; therefore, the most significant bit of a register, or binary number, is reserved for the sign. Zero is used for positive and one is used for negative. Referring back to the number 65 that was used earlier, if it is converted to binary (110101), the uppermost bit is a one which indicates that the number 65 is actually negative. If, however, this number is in a register and a right shift is made, the result is 011010 and the number is no longer negative.

Sign extension allows the original sign bit to be maintained in the uppermost bit position. In this case, if the number to be shifted is 110101 and a right shift is followed with sign extension, the result is 111010 (72). The division does not work too well in this case. Sign extension must be used when right shifting negative numbers; it is optional with positive numbers.

LEFT-SHIFT NETWORK

Figure 118 shows the layout for a three-bit shift network for left shifting. The number to be shifted is first of all in rank II, the operating register. The flip-flops in rank I are cleared, and a transfer pulse will copy rank II into rank I. Next, rank II is cleared and then a shift pulse will gate rank I into rank II at the same time it is performing the left shift. Notice that the most significant bit K020/021 is brought end around into K500/501. All left shifts are end-around.

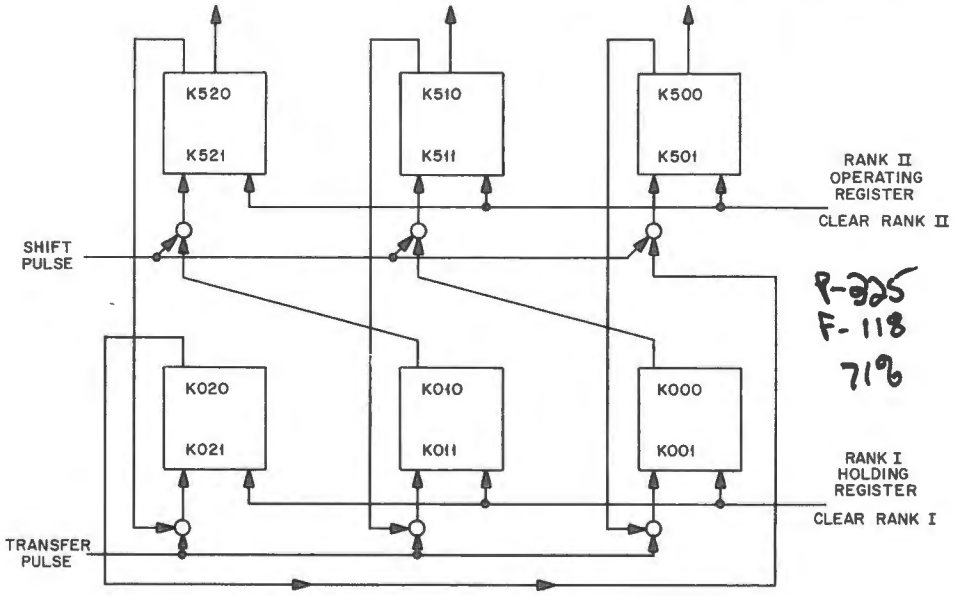


Figure 118. Left-Shift Network

RIGHT-SHIFT NETWORK

The diagram for a right-shift network is shown in figure 119. The sequence of operations is the same as in the left-shift network except, of course, that the data in rank I is shifted right into rank II. The contents of K000/001 is discarded or goes end off. Notice that the set side of K520/521 has a sign extension term into the AND gate. If sign extension is required, this term will be a 1 and K020/021 will be copies into K520/521. If no sign extension is specified, this term will be a 0 and no matter what the state of K020/021 is, K520/521 will remain clear when the shift pulse is applied. All right shifts are end-off, with sign if it is specified.

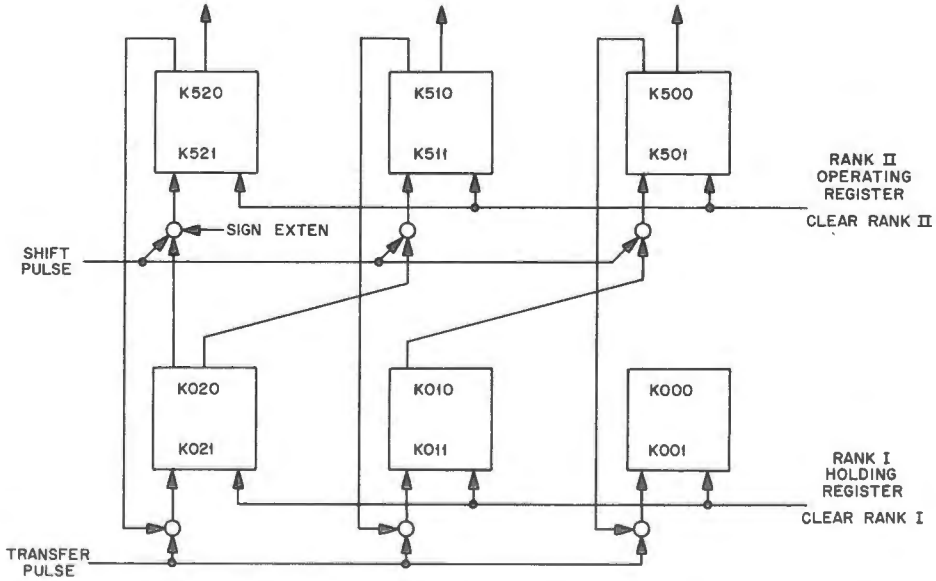


Figure 119. Right-Shift Network

REFERENCE 15

ADDERS

In most computers the process of addition is the basis for all arithmetic computations. In this reference you will learn how addition is used to perform subtraction and multiplication, and how division is performed primarily by subtraction. In order for you to thoroughly understand how the computer performs these different functions, it is essential that you understand the operation of adder and subtractor circuits. The input into these circuits is provided by different counters and registers that contain the information upon which these different functions will be performed. The data in the counters and registers also determines the time when these functions will occur.

HALF-ADDER

As in decimal addition, the sum of two quantities is obtained by adding the digits in corresponding places or columns. If the sum of the digits in any column equals or exceeds the base number, one unit is carried over to be added to the next higher column. In binary addition, the sum of two 0's is always 0 with no carry; the sum of 1 and 0 is always 1 with no carry; the sum of two 1's is always 0 with a 1 carried to the next column. This is shown in the truth table; see Table 18.

TABLE 18. TRUTH TABLE FOR HALF-ADDER

AUGEND	A	0	1	0	1	AUGEND = 1
ADDEND	B	0	0	1	1	ADDEND = 1
SUM	S	0	1	1	0	SUM = 0
CARRY	C	0	0	0	1	CARRY = 1

From the truth table it is seen that a sum is produced when the augend, A, is 1 and the addend, B, is 0, and vice versa. A carry is produced when both A and B are 1. Logical equations may be written for the sum and the carry in terms of A and B. The equations are as follows:

$$\text{Sum} = A\overline{B}+\overline{A}B$$
$$\text{Carry} = AB$$

These conditions are fulfilled by a logical circuit known as a half-adder, having two inputs and two outputs. The half-adder shown in figure 120 will produce a sum output when one, but not both inputs are present. When a signal is applied to both inputs, no signal is produced at the sum output, but a signal is produced at the carry output.

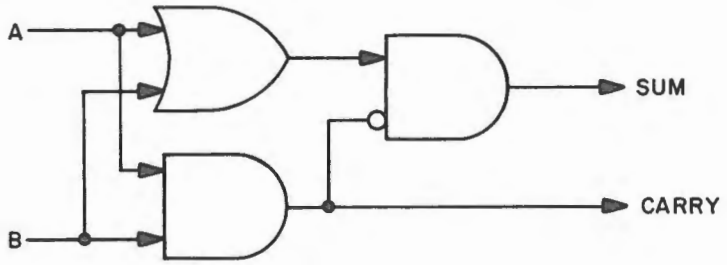


Figure 120. Half-Adder Logic Diagram

The equation for the sum describes the exclusive OR function; one input, but not both, will produce an output.

The truth table and logical diagram considered only two inputs. Practically, an adder must be able to accept a carry from a previous column and add it to the augend bits in the next higher column. The half-adder is limited in that it does not consider a possible carry from a previous column.

FULL-ADDER

A full-adder considers the possibility of a carry from a previous column. Figure 121 shows that a full-adder in effect consists of two half-adders. One half-adder adds the augend and addend in a particular column. The other half-adder adds the resulting sum to a carry from a previous column. As a result of these two additions, a single sum and a single carry output is produced for that particular column.

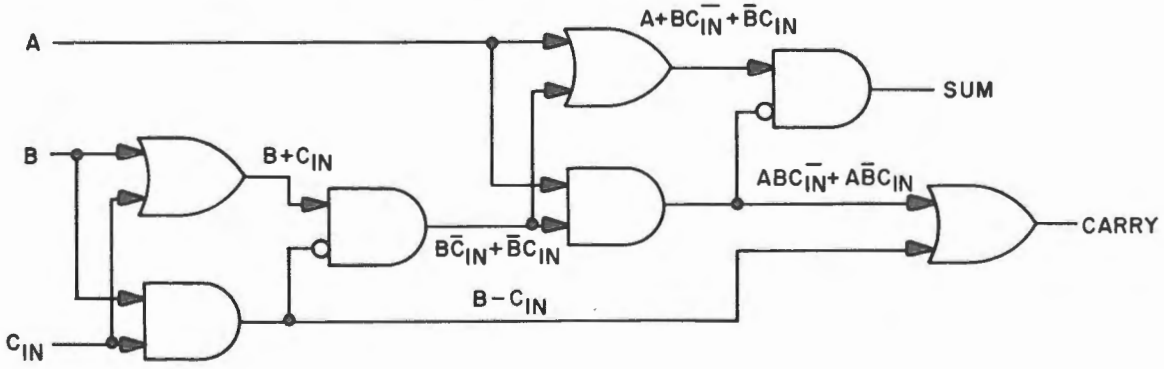


Figure 121. Full-Adder Logic Diagram

A truth table, Table 19, indicates, for the full-adder, all possible combinations when using three inputs.

TABLE 19. TRUTH TABLE FOR FULL-ADDER

AUGEND A	0	1	0	1	0	1	0	1
ADDEND B	0	0	1	1	0	0	1	1
CARRY IN	0	0	0	0	1	1	1	1
SUM	0	1	1	0	1	0	0	1
CARRY OUT	0	0	0	1	0	1	1	1

The truth table shows that there are four combinations that produce a sum and four combinations that produce a carry. They are as follows:

$$\text{Sum} = A\overline{BC}_{in} + \overline{A}B\overline{C}_{in} + \overline{AB}C_{in} + ABC_{in}$$
$$\text{Carry (Out)} = AB\overline{C}_{in} + A\overline{B}C_{in} + \overline{A}BC_{in} + ABC_{in}$$

Terms may be so collected so that the operation of a full-adder becomes more apparent.

$$\text{Sum} = C_{in}\,(\overline{AB}+AB) + \overline{C_{in}}\,(A\overline{B}+\overline{A}B)$$
$$\text{Carry (Out)} = C_{in}\,(AB+A\overline{B}+\overline{A}B) + \overline{C_{in}}AB$$

A full-adder showing the application of the previous terms is shown logically in figure 121. The full-parallel adder is shown in figure 122.

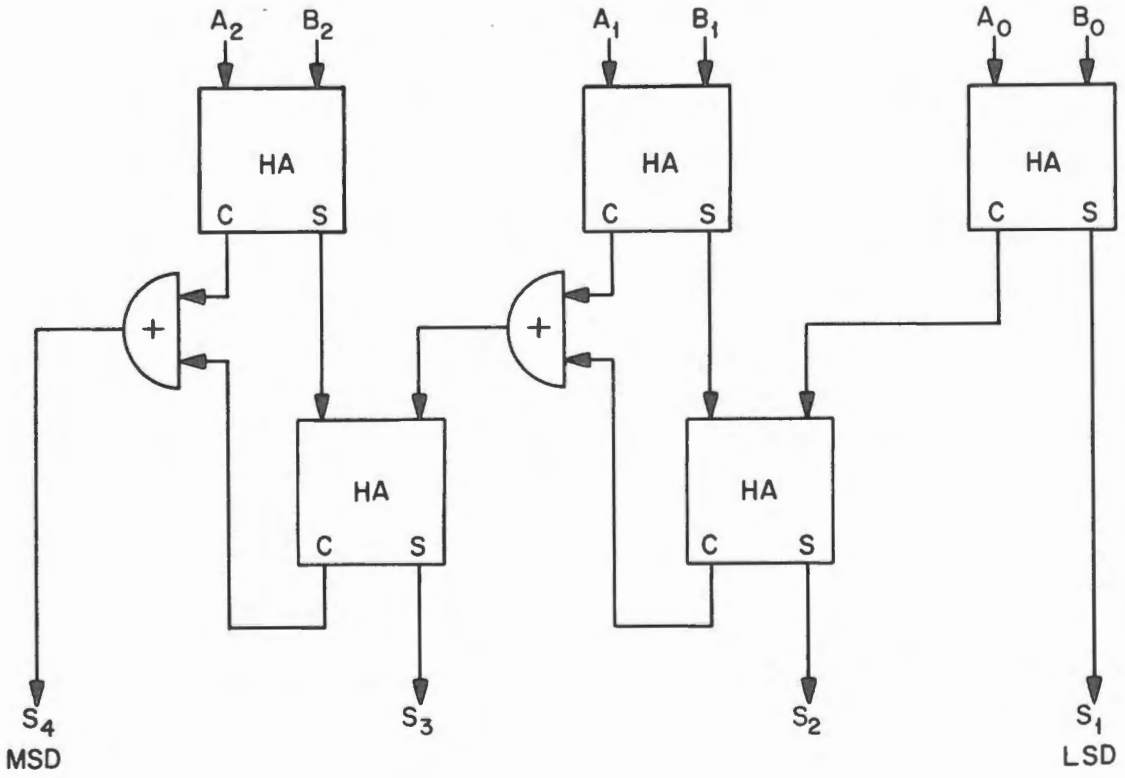


Figure 122. Full-Parallel Adder

The least significant digit of the A and B numbers is applied to the half-adder on the extreme right. The numbers, 1 and 0, develop a sum output but, no carry, so the least significant digit of the sum, S_1, now equals 1. In the second order, both A and B are equal to 1, the sum from the upper half-adder portion is 0, but a carry is generated. No carry from the previous order was generated; hence the sum of the lower half-adder for the second order is 0. In the third order A and B again equal 1; the sum from the upper half-adder is 0 and a carry is developed. The sum of 0 is added to the carry of 1 from the second order, resulting in a sum output from the third order of 1. This is all the numbers there are to add; therefore, the third order carry becomes the most significant digit of the sum, at S_4.

REFERENCE 16

TRANSLATORS

PURPOSE

The translator is a network which receives signals representing information in a certain code, and the output of the network consists of signals representing the same information, but in a different code.

There are several binary codes for decimal numbers in common use. Some may represent individual decimal digits with a group of four binary digits for each decimal digit up to 9. For any number greater than 9, 11 for example, two groups of four each would be used: 9 equals 1001 11 equals 0001 0001. Other systems may only use digits that go as high as 7 or use the octal numbering system to feed in or take out information from the computer. Only three binary digits are needed to represent each octal digit.

Octal Digit	Binary Code
0	000 000
1	000 001
2	000 010
3	000 011
4	000 100
5	000 101
6	000 110
7	000 111
10	001 000

Letters may also be inserted by representing each letter of the alphabet with a particular octal number.

A (21)	010 001
B (22)	010 010
C (23)	010 011
Etc.	

TYPES

ENCODER

The encoder is used to put data into coded form so that the computer can use it. Its job is to establish the connection between the inputs to it and the inputs to the computer while keeping the inputs buffered apart (isolated from each other). It will take decimal or octal information and convert it into information that the computer can work with, usually binary. An example of encoder operation using 1604 logic cards is shown in figure 123.

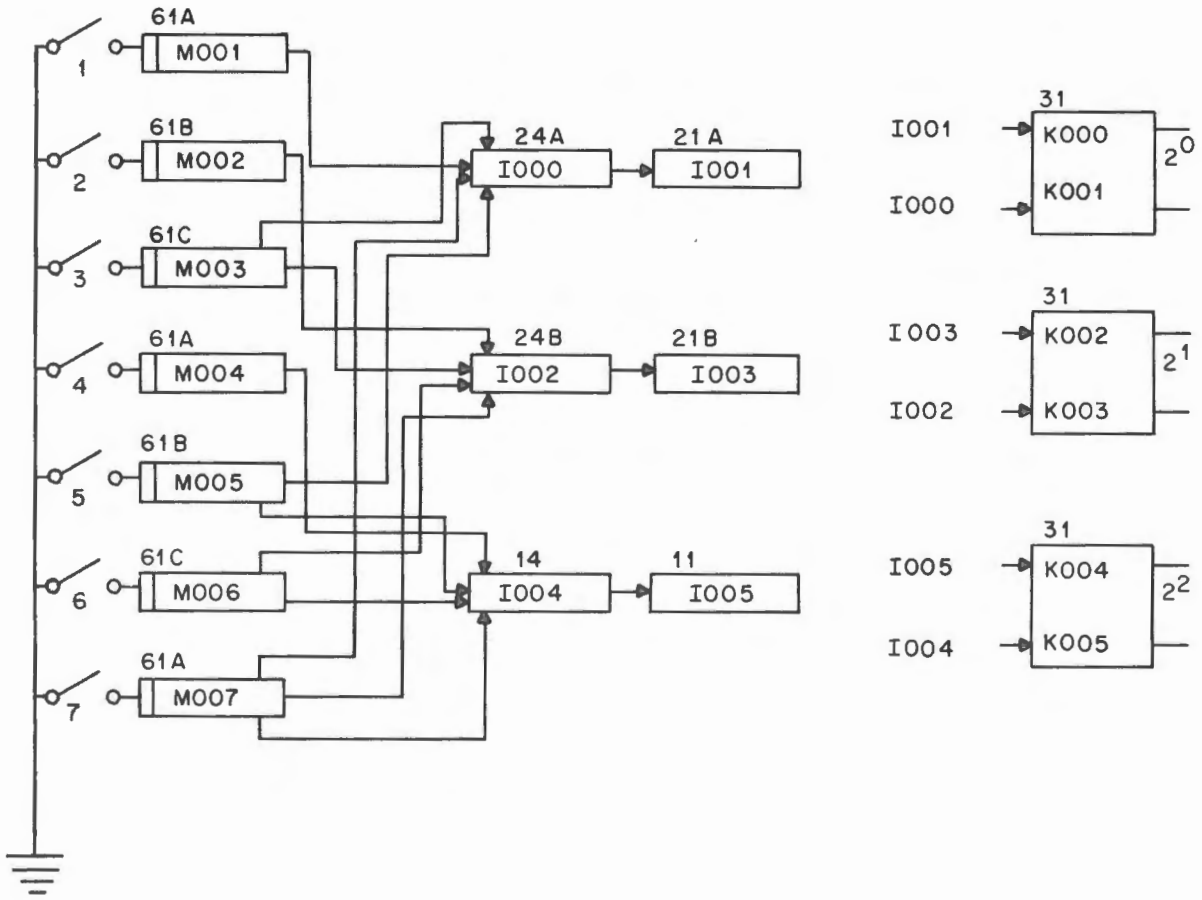


Figure 123. Encoder

When the switches are open, high voltages are being supplied to the inputs of all the 61 (input) cards. Logical 0's will be produced in their outputs. The 0's from the 61 cards are then fed to inverters I000, I002, and I004. With 0's into these inverters, they will, in turn, output logical 1's. These 1's are then fed to inverters I001, I003, and I005. They will produce logical 0's. By examining the inputs to the flip-flops, it can be seen that they will now be in the clear state which represents 000 in binary form. With all switches open, an octal 0 has been encoded.

If switch 1 is closed, a ground is applied to M001, which then outputs a logical 1. This logical 1 goes to I000, which outputs a logical 0. The logical 0 goes to I001, which outputs a logical 1. At this time, flip-flop K000/K001 will become set, and the other flip-flops will remain cleared. This condition will exist until switch 1 is opened, upon which time all flip-flops will return to the 0 or cleared state.

By closing the appropriate switch, any number from 1 through 7 may be encoded. The binary equivalent of that number will be stored in the flip-flops. A set flip-flop represents a binary 1 and a cleared flip-flop represents a binary 0.

DECODER

The decoder is used to convert binary coded information into a form which can be easily recognized and read.

AND GATE

The AND gate shown in the right portion of figure 124 will output a logical 1 only when both flip-flops are set. When both flip-flops are set, they hold the number 3.

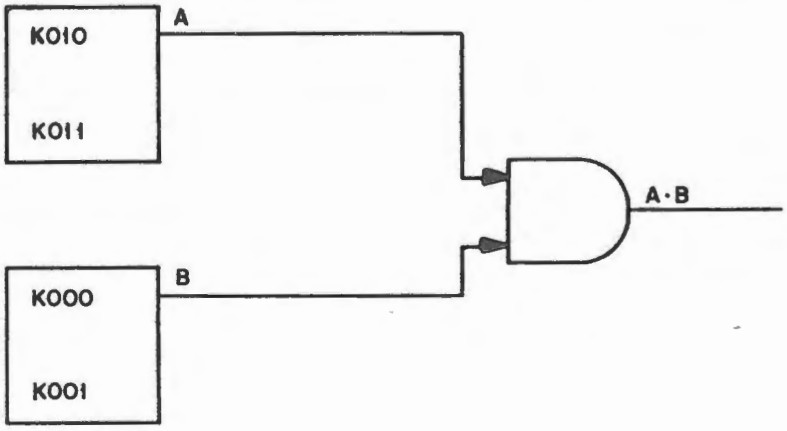


Figure 124. AND Gate Decoder

As seen in figure 125, if the output of the AND gate feeds a light driver it can be made to display the number 3.

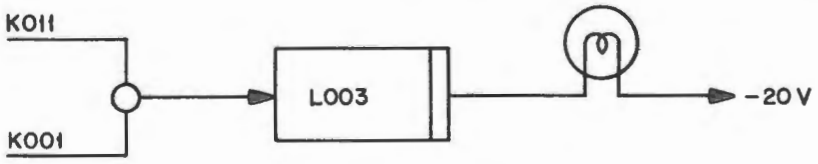


Figure 125. Decoder and Light Driver

To translate all four conditions of the flip-flops in figure 126, four AND gates and light drivers are required.

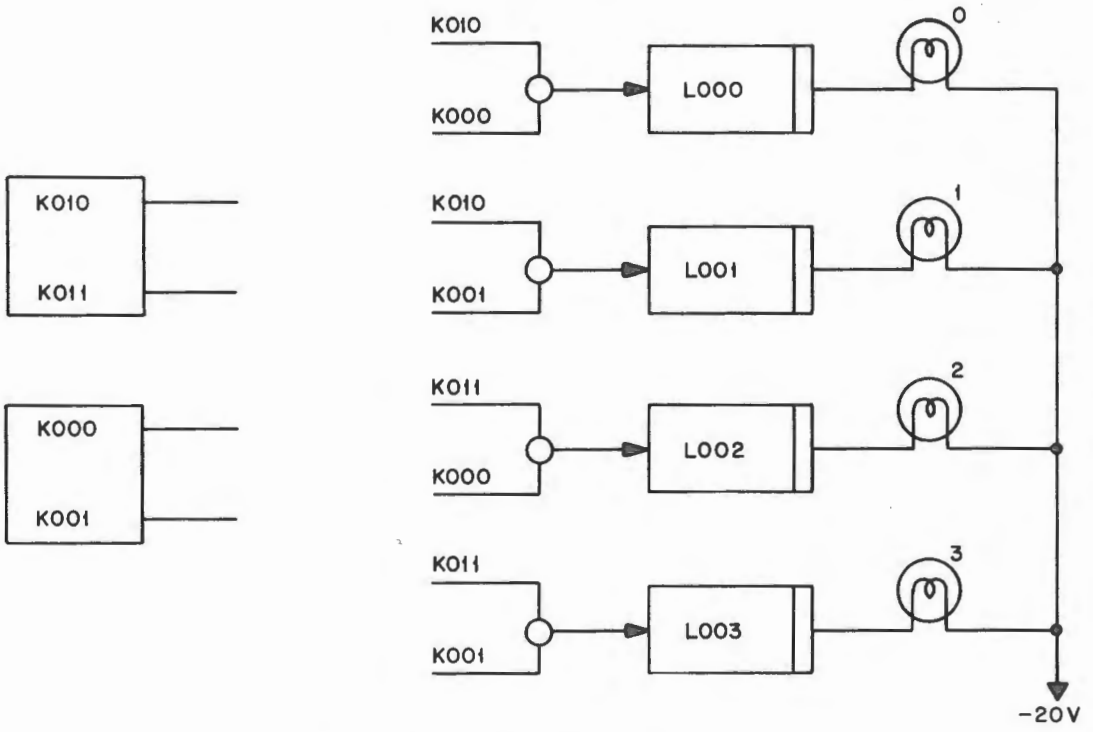


Figure 126. Four-Stage Decoder

For each condition of the flip-flops, one AND gate will be made, and a logical 1 will be fed to a light driver. The corresponding lamp will light to indicate the binary value held.

INVERTERS

The method of using inverters to translate the contents of a register is just the opposite of the method used with AND gates. All inputs to the inverter must be ORed as shown in figure 127.

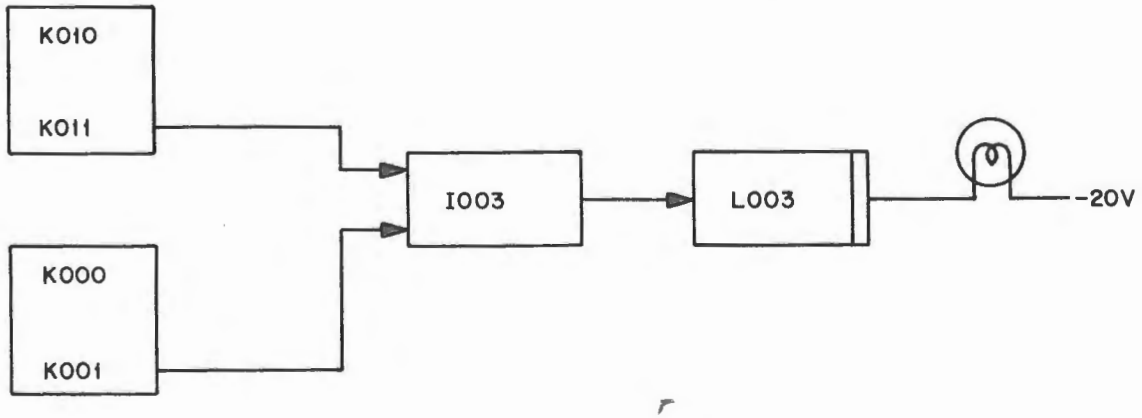


Figure 127. Inverter Decoder

When both flip-flops are set the 0's from the clear side outputs are fed to the inverter I003. I003 outputs a logical 1 to L003 and the lamp lights. For any other combination at least one of the inputs to I003 will be a logical 1, holding its output to a 0.

To translate all conditions of the flip-flops, four inverter/light driver combinations must be used as shown in figure 128.

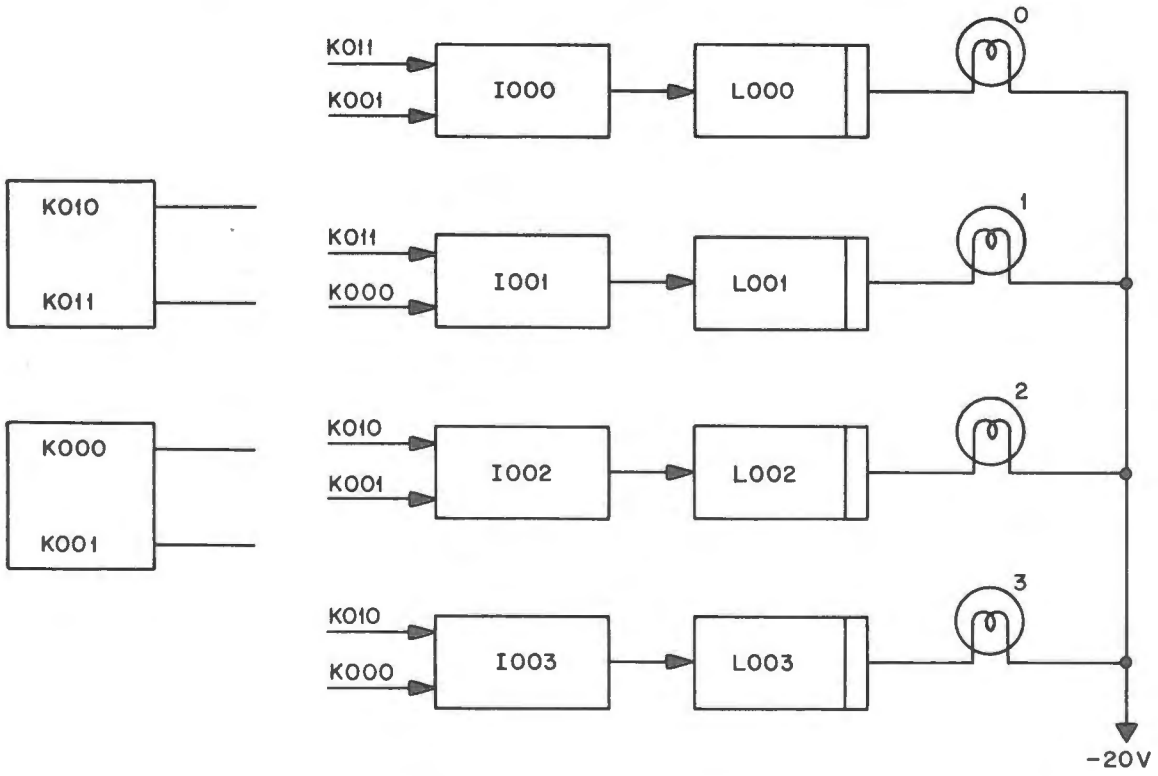


Figure 128. Four-Stage Inverter Decoder

REFERENCE 17

INTEGRATED CIRCUIT TECHNIQUES

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The already wide and yet expanding field of integrated circuits includes several basic approaches for the fabrication of very small electronic circuits and a vast multitude of combination techniques. Each has its own particular characteristics, advantages, and limitations. Just as the various construction methods in building houses are selected according to the end requirements and desires, so must the particular fabrication process for integrated circuits be chosen according to the specific needs and required characteristics.

Since no one integrated circuit technique yet developed can fully satisfy all purposes and required specifications, it is well that we have several from which to choose. In this article we will look at several possible methods for fabricating integrated circuits and discuss their special characteristics with emphasis on their features and limitations. Included will be the monolithic, isolated monolithic, thin-film and thick-film, and MOS techniques with several possible combinations.

This article is directed to the engineer and technician who will be dealing with the finished integrated circuit product either in equipment fabrication, checkout, or repair and will attempt to answer the question "What can I expect of integrated circuits?" Even though your present job has no direct connection with integrated circuits right now, you will want to become familiar with them. It is very likely that you will be seeing a lot of them in the near future.

The integrated-circuit techniques already developed have allowed a fantastic degree of microminiaturization. Going back just a few years to the time before the "semiconductor revolution", the accomplishment seems even greater. Who would have thought that we could contain the circuit function of a dozen or more tubes with associated resistors and capacitors within the size of this letter "O"?

Development of the integrated-circuit techniques has resulted not only in the tremendous reduction of physical size, but has also produced great improvements in the operating reliability of the over-all circuit through the reduction of connecting wires and large, vibrating components.

Let's look at some of the common techniques for making integrated circuits and see just what each method can offer and consider where each might run into trouble.

Monolithic Circuits

Monolithic means "single stone" and a monolithic circuit is one which is fabricated within a single crystal of semiconductor material, usually silicon. The transistors, diodes, resistors, and capacitors are all built right in the semiconductor material. The bulk properties of the material along with the various characteristics of p-n junctions are used.

The same basic processes for the fabrication of silicon transistors may be used to make monolithic integrated circuits. The most common ones are the diffusion process, the epitaxial process, or a combination of the two. The transistors, diodes, and passive elements are made at the same time within the body of the silicon by diffusing appropriate impurities through windows cut into an oxide coating by photochemical etching.

The monolithic process has the greatest single capability of any of the processes. It is possible to fabricate both active and passive components within a very small volume and with all interconnections made by an aluminum evaporation that is etched to provide the desired paths. The technique is basically that which has been successfully used in the preparation of many transistors and hence is quite well developed.

One of the main limitations of the monolithic technique is the presence of distributed diodes connecting the fabricated components to the silicon substrate material proper. While it is possible to greatly reduce their effect by making sure that they are always reverse-biased, we still have to contend with leakage currents which may flow and with unwanted coupling capacitances which are present in any diode.

Another limitation of the monolithic process is the difficulty in obtaining proper passive components. The range of the resistances which are practical is only about 20 to 20,000 ohms which places a severe restriction on the circuit designer. In addition, the resistors even within the range of practicality have a rather large temperature coefficient (approximately 0.7%/°C).

The capacitors are actually reversed-biased diodes; and care must be taken to make sure that they stay reverse-biased. Their value, which must be restricted to rather small sizes, will be a function of the applied reverse voltage as is the case with any semiconductor diode.

Still another limitation in producing monolithic circuits is the expense in making the precision masks; several being required for each circuit. This restricts the use of monolithic techniques to those applications where large quantities of the same circuit are required. Even minor changes usually require scrapping the finished integrated circuit and all masks. New masks must be made and the entire process repeated.

Isolated Monolithic Circuits

A variation of the monolithic process which overcomes many problems present with standard monolithic techniques warrants separate consideration. In this approach, portions of the original semiconductor block are isolated from each other either by surrounding sides and bottoms with SiO_2 (glass), a very good insulator.

Let's look at the basic process as currently being used by "Radiation, Inc." The process starts with a lapped and polished silicon wafer about 0.010 inch thick upon whose surface a thin layer of SiO_2 is formed by heating in an oxidizing atmosphere. Moats or grooves are then etched around the areas which are to be isolated by a normal photo-etching process to produce the results shown in FIGURE 1.

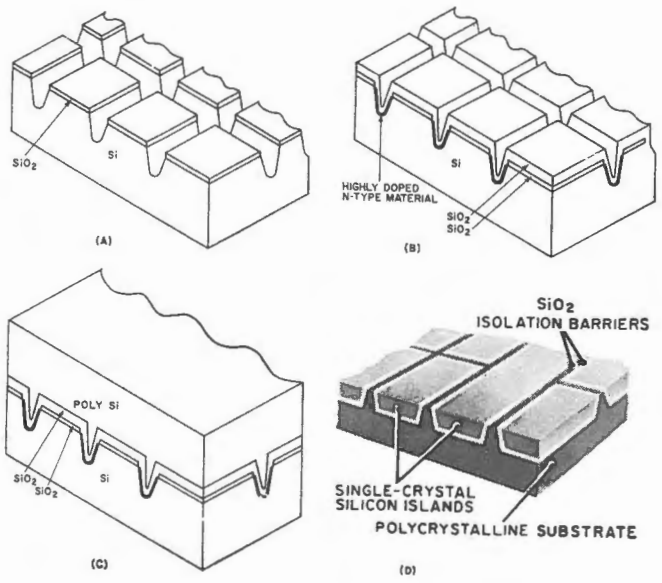


FIGURE 1 - Isolated Monolithic Process (A) Silicon "waffle" wafer showing moats. (B) Oxide grown on moats of wafer. (C) Polycrystalline silicon grown on wafer. (D) Final device.

Very highly doped n- or p-type silicon is epitaxially deposited or grown within the groove and then covered by $Si0_2$, formed by heating again. The resulting structure is shown in FIGURE 1-B. Polycrystalline material, (not having a carefully arranged lattice structure as does the monocrystalline material required for transistors and diodes) is then deposited over the entire surface. The grooves are filled and the entire surface is covered with a thick coating, as shown in FIGURE 1-C.

The wafer is turned over and the original silicon wafer material is ground off until the polycrystalline material is reached. The surface is then polished and etched to leave small islands of the original silicon wafer from the polycrystalline material. These islands act merely as a structural agent via a thin layer of $Si0_2$, as shown in the photograph of FIGURE 1-D. This photo does not show the heavily doped n-region which is not always required.

Each of the isolated islands of silicon may then be treated as a separate chip and processed in the same way as in the normal monolithic process. Very careful control of the thickness of the wafer and the deposited coating is required. Let's look at some of the features of this process.

Because of the glass isolation, we no longer have to make sure that we back- or reverse-bias the isolation diodes and we have less than one-tenth the stray capacitances present. Also, the leakage current between elements is greatly reduced, especially if operated at high temperatures. Further, breakdown voltages of 1000 volts between adjacent elements is practical. Another advantage of this technique is the possiblity of making both p-n-p and n-p-n transistors on the same substrate and the capability of selective gold doping to achieve different characteristics for adjacent devices on the same substrate.

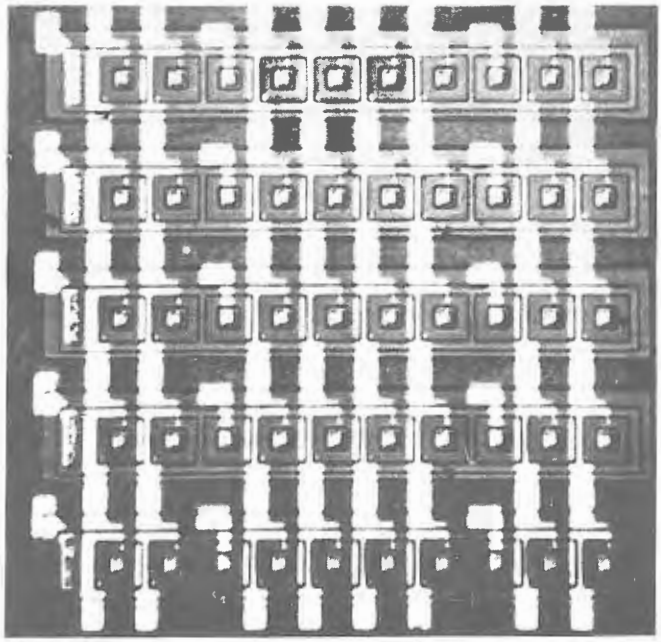


FIGURE 2 - Diode matrix made with isolated monolithic process.

A diode matrix, manufactured by "Radiation, Inc." by the isolated monolithic technique, is shown in the photograph of FIGURE 2. The glass isolation region may be seen surrounding each row of diodes in the matrix as well as the heavily doped n-regions. The n-regions conveniently tie all of the cathodes of the diodes in a given row together.

This photograph also shows an interconnection means in which all diodes are connected to the vertical interconnect buses and then disconnected by blowing out a portion of the metallization. This is done by electrical discharge to remove those connectors not needed in the matrix.

Thin-Film Circuits

Another technique which may be used to fabricate integrated circuits is the evaporation and deposition (usually performed in a vacuum) of metals and dielectrics upon a smooth surface, such as glass or vitrified ceramics. The usual method is to raise the temperature of the material to be deposited above its boiling point in a vacuum. The vapor is then allowed to condense upon the substrate through appropriate masks. The resulting depositions are very thin and are measured in microns (millionths of a meter).

Thin-film circuits have the advantage in that higher values of resistance are possible and the temperature coefficient may be held to nearly zero if desired. Because the resistance material is on the surface of the substrate, it is possible to trim a given resistor physically to a precise value. This is achieved by making it a little low in value to begin with and then carefully removing a small portion of the material until the desired value is reached. It is also possible to control the value of the resistance during deposition by monitoring it with a precision bridge. The process is then stopped at an appropriate point and the resistance value "frozen" at that level.

Capacitors made by the thin-film process are not voltage sensitive as is the case with p-n junction capacitance. By careful alternation of metal and dielectric deposition during the fabrication process, a multiple plate capacitor having substantial capacitance is possible. Since the dielectric films must be very thin, breakdown voltage can be a problem if even a very small defect occurs during the deposition of the insulating material (usually silicon dioxide).

Since the deposition is generally made using a substrate of insulating material, isolation between various parts of the circuit is much better than for the monolithic technique. One of the greatest limitations to the use of the thin-film process in its purest form is the lack of quality active devices. Although development transistors and diodes have been made by this method, they have not been found suitable for general use.

The thin-film circuit process has the same problem as the monolithic circuit techniques regarding the requirement for precision masking. If a wide range of resistance values is to be included within a given circuit, the number of masks required is large and the actual number of process steps will almost always be greater than for monolithic techniques. This is especially true if the circuit is complex.

Thick-Film Circuits

It is possible to fabricate circuits utilizing a thick-film technique in which the interconnections and components are applied to a substrate by a silk-screen process. This basic approach has been in use for many years with RC networks found in radios, television sets, and hearing aids. The more recent development of the Cermet materials (basically a combination of metal and glass) has improved the basic capabilities of this technique considerably.

Interconnections used in the thick-film process are usually a silver-bearing material and are fired at a rather high temperature. Temperature coefficients for thick-film resistors are not as low as those obtainable with thin-films. Typically, they are much better than those possible with monolithics.

Thick-film capacitors may be quite large in value since the dielectric to be screened can have a large dielectric constant (300 to 500). Breakdown voltages can be made as high as needed by increasing the thickness of the dielectric. This, however, will decrease the capacitance.

No thick-film active devices are currentlv in use. We must therefore combine thick-films with active devices made by another process, as discussed later in this article.

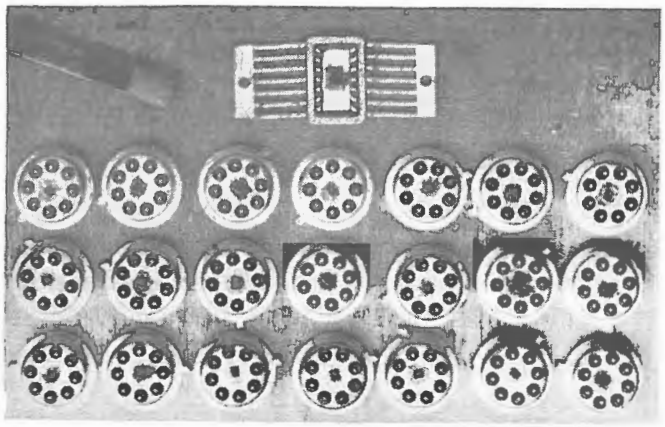


FIGURE 3 - A 21-bit register (top) whose heart is a microscopic wafer of silicon containing 110 transistors and 48 resistors, replaces 21 separate microcircuits (shown here) in computers.

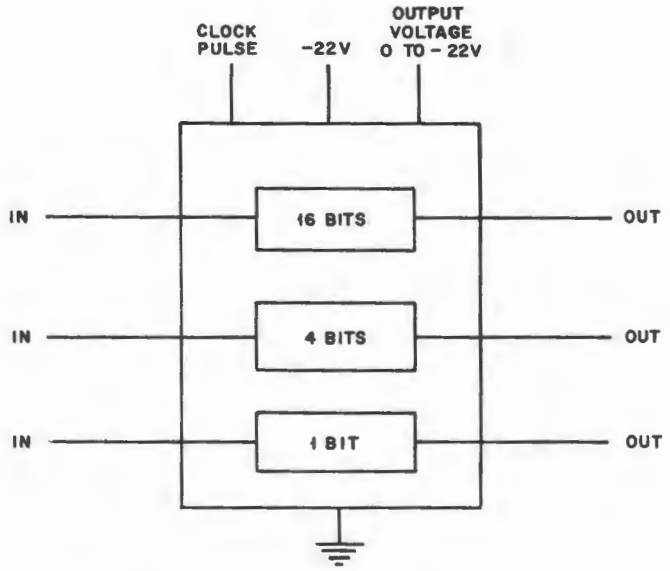
MOS Technique

The metal-oxide-semiconductor (MOS--a field-effect device) process has been applied to monolithic integrated circuits with notable success. Because the active components on the chip are essentially insulated from each other, isolation gimmicks are not required. The technique lends itself to low-cost, high-density digital integrated circuits. These devices have a lower frequency than other devices and consequently clock rates for digital functions are limited to a few megacycles.

An example of the use of this new process is a 21-bit shift register developed by General Instrument Corp. (FIGURE 3). The silicon wafer measures 0.07 inch long and 0.06 inch wide and contains 110 transistors and 48 resistors. Clock rate is 500 kc, and the unit replaces 21 separate microcircuits. FIGURE 4 is a block diagram and a photomicrograph of the circuit. (Also refer to the cover illustration.) The register is actually three shift registers in one package sharing a common supply and clock pulses. The three can be used either independently or connected in series to give a total of 21 bits of delay to an arbitrary data stream. By letting the output voltage be just a few volts, it is possible to have the register drive other types of low-voltage n-p-n logic.

FIGURE 5 provides a cross-sectional view of an n-channel MOS. The two n-regions labeled "source" and "drain" are diffused into the p-wafer by such methods as used in the planar process (e.g., photo resist and oxide masking). The source and drain are analogous to the cathode and plate of a vacuum tube, respectively. The third element, the gate (analogous

to the grid of a vacuum tube), is evaporated over the silicon oxide between the two n-regions. The gate is insulated from the silicon wafer and exhibits a resistance on the order of 10^{10} or more ohms.



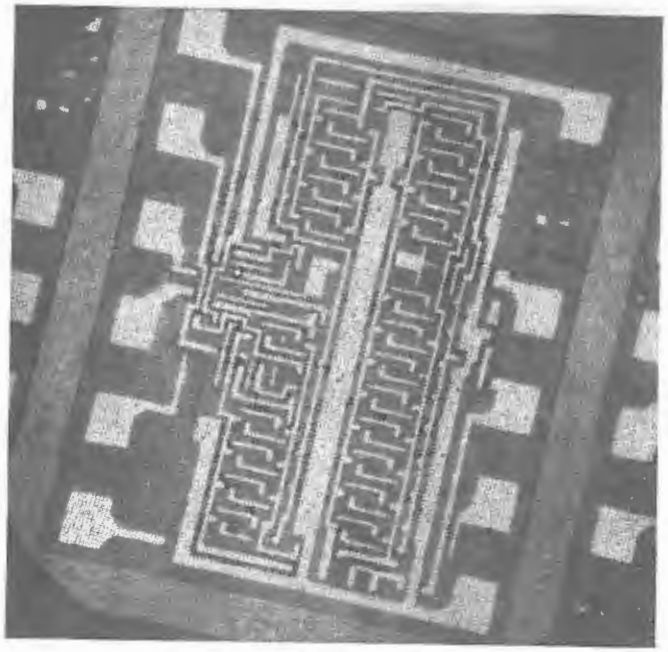


FIGURE 4 - A 21-bit shift register. The functional block diagram and a photomicrograph of the actual structure used.

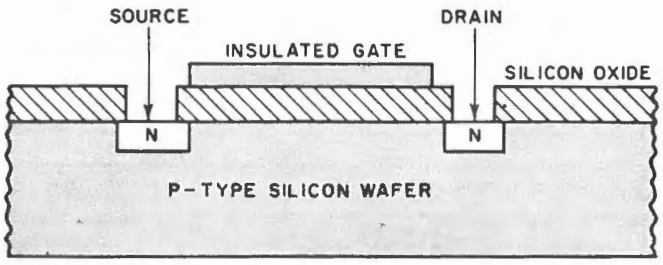


FIGURE 5 - Cross-sectional view of an "n"-channel MOS device.

In a type called the n-channel depletion MOS, drain current will flow even if the drain-source (input) circuit is zero biased. For integrated digital circuits, however, the n-channel enhancement MOS which exhibits zero drain current for zero bias, is perferred. A significant characteristic of the enhancement type is its low saturation voltage. This permits the design of simple direct-coupled transistor logic (DCTL).

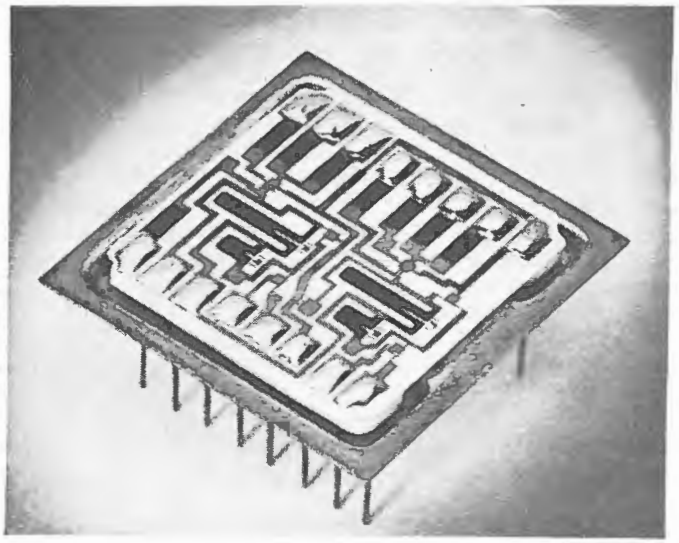
Hybrid Circuits

Each of the basic techniques described has limitations which might restrict their use in many areas for one reason or another. However, each technique has certain advantages. There are many possible combinations of portions of the basic techniques which will result in an expansion of the capability of any of the single processes with many of the desirable features retained. This approach leads to the hybrid circuit.

One of the simplest forms of hybrid fabrication is the combination of several "chips" or discrete monolithic blocks within a single package. This allows more complicated circuitry to be fabricated than might be possible if the entire circuit were to be made as a single monolith. In some cases, it is either impossible or at least impractical to make certain combinations of p-n-p and n-p-n transistors on a single chip. For example, if matching is required for one reason or another, it is much easier to perform the matching before assembly than to try to obtain a perfect match with two devices on a single chip.

Isolation can be improved by the use of multiple chips and the circuit components contained on each chip may be optimized independently. This becomes especially important where it is necessary to include many active and passive components of different types within a single circuit. Since the interconnections must be made by small wires bonded to the individual connection terminals on each chip, assembly labor can become relatively high. Each extra connection will also decrease the overall reliability of the device.

The multiple chip arrangement is also useful in developing prototype circuits of configurations which are subject to change. It is possible to alter the design of one chip without affecting any of the others and to add small discrete components to the circuit.



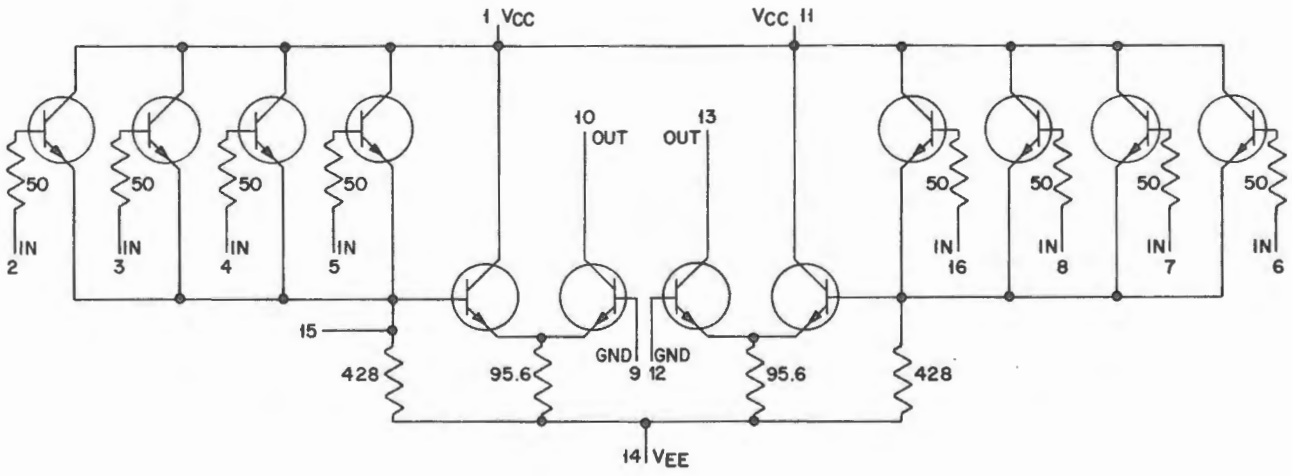


FIGURE 6 - Photo and schematic of hybrid 4-input gate.

Another hybrid form is the combination of thin-film passive components with monolithic circuits. This is especially useful in the fabrication of circuits requiring large resistances or low temperature coefficients. The monolithic portion is made in the usual manner and then the thin-film portions of the circuit are deposited on top of an insulation layer formed on the surface of the monolithic block. In a sense, most monolithic circuits are in this category of hybrid because the final interconnection is usually a thin-film deposition of aluminum.

Thick-films may also be combined with monolithic blocks in just about the same manner as described for the thin-film combination. However, this is not as common. A more usual combination of monolithic and thick-film circuits is the addition of monolithic active devices or circuit chips to the substrate on which the thick-film circuit has been screened. This combination allows all of the passive components to be fabricated independently from the active components and can result in a very workable arrangement.

An interesting hybrid combination is shown in the photograph of FIGURE 6. This particular circuit is for a four-input gate also shown in FIGURE 6. The technique, developed by Corning Glass Works, combines monolithic circuit chips with thin-film resistors and thick-film interconnections and capacitors. The capacitors, if required, are fabricated on top of the substrate first by silk screening a sandwich of gold paste, niobate glass frit, another layer of gold paste, and finally a layer of protective glass. A portion of each of the gold paste layers is left exposed to allow connection to be made to the electrodes.

The substrate containing all the required capacitors, whose values may be controlled by varying the physical area of the electrodes or the thickness of the dielectric layer, is then placed in an oven and "fired" at a very high temperature. This permits the binding of all layers together, devitrification of the glass dielectric, and provides a hermetic seal over the finished capacitor. The dielectric constant of the glass used for the dielectric is around 400 and the thickness may be a little more than one-thousandth of an inch. This means that capacitance values up to 3000 pf. are practical.

If interconnection crossovers are required (or if they might greatly simplify the circuit layout), they are easily made at the same time as the capacitors. When the first layer of gold paste is screened, a small stripe of gold paste is placed where the crossover is desired. During the screening of the sealing glass, the mid portion of this crossover stripe is covered with a glass seal. This allows another interconnection path to pass over the gold stripe without shorting and with very little coupling capacitance. The dielectric constant of the sealing glass is only around 5 or 6.

The substrate containing the capacitors and crossover stripes is then covered with a thin film of tin oxide deposited without requiring a vacuum. The tin oxide is etched away except where a resistor or interconnection line is required, employing a photoresist technique. Places where a resistor is required are masked off by vinyl silk screened on top of the tin oxide and the remaining area of tin oxide is plated with copper. An electroless plating technique is used and copper is left only on the exposed tin oxide.

Individual resistors may be trimmed to as close a tolerance as required (down to 1/2%) by making the initial value a little too small and then sandblasting a notch in a loop provided for that purpose. Several of these are visible in the picture.

Semiconductor devices of the "flip-chip" form are added to the tinned copper interconnection. The flip-chip can be just a diode or transistor, or it might be a complicated integrated circuit in monolithic form. FIGURE 7 illustrates a "worm's-eye" view of a single transistor as might be seen looking through the substrate.

This type of hybrid fabrication permits monolithic circuits of moderate complexity to be combined with stable resistors. These resistors have a relatively low temperature coefficient and are capable of being trimmed to close tolerances even after final assembly. The fact that capacitors, having the characteristics of a hermetically sealed ceramic unit, may also be included as a valuable asset.

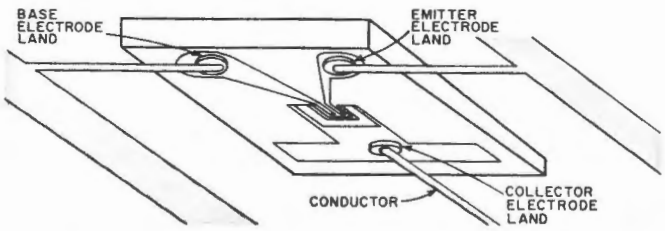


FIGURE 7 - Construction of a transistor of the flip-chip form.

Since the monolithic circuits may be broken down into functional sections, very complicated circuit configurations are feasible with a minimum of interaction and undesirable coupling. In addition, the availability of crossovers can greatly simplify a layout design and decrease the distributed capacitances and inductances in high-speed circuit interconnections.

Although the circuits as currently produced by Corning are enclosed in a hermetically sealed package to protect the semiconductor devices, it should be possible to adequately protect them by normal passivation techniques or glass encasements. A mild conformal coating would give added protection.

Converting to Integrateds

Let us consider the various factors involved in taking a circuit from an arrangement using standard or full-size components and developing an integrated circuit which will perform the same basic function. The difficulty and the over-all direction taken would depend very greatly upon the actual circuit requirements.

Digital circuits are typically easier to integrate than analog functions since any capacitors required are usually small in comparison with those which might be required for an audio amplifier. Radio-frequency circuits often require coils and transformers. While it is possible to fabricate a coil with a limited amount of inductance by the thin-film technique, the range is very restricted and the "Q" is very low. The large capacitor or coil problem is solved by means of adding on miniature discrete components.

Let us assume that we must integrate a simple audio amplifier and study the design decisions involved with the conversion from an arrangement using standard components. A normal arrangement might use RC-coupled amplifier stages. Since the rather large capacitors would be impossible to make in monolithic or thin-film form, we would do well to consider a redesign to eliminate as many capacitors as possible and preferably all of them. We may do this by careful design and by using a differential amplifier or temperature compensation techniques to stabilize the bias conditions.

If a very minimum of size were required, we would perhaps best consider the monolithic circuit process since it would be possible to contain the entire amplifier within the volume of a TO-5 can or in a flat package roughly a quarter of an inch square and 0.050" thick. To do this, however, we would have to eliminate all capacitors. The circuit could be made of one monolithic block or it could be formed from several monolithic chips within the single can.

Another approach might be preferable if the output power requirements were too large for the monolithic technique; also, if the quantity were not sufficient to warrant the fabrication of precision masks which might have to be modified several times before the exact performance requirements could be met. In this case, we would best turn to the over-all hybrid approach using the flip-chip monolithic active components with plated interconnections and thin-film tin oxide resistors.

The hybrid approach allows us to use standard chips for the matched pair differential stage and other transistors with the custom-designed resistors and interconnections. With this technique we have the advantage of circuit adjustment after fabrication and can raise the value of certain critical resistors to insure proper balance or setting of the bias point or gain.

Should an input isolation capacitor be necessary, we might consider the use of a field-effect transistor (FET) for the input stage. The input impedance level would then be high enough to allow the use of rather small coupling capacitors which may be fabricated on the substrate. We could perhaps squeeze in a small miniature tantalum capacitor attached to terminals provided on the substrate.

Some Examples

Examples of an integrated four-input gate and a shift register have already been shown. Many digital circuits have been integrated in a monolithic form as might be expected since certain forms of circuits are repeated many times within a given piece of digital equipment. Also, the same type of circuit is more likely to appear in different pieces of equipment of two different manufacturers.

Digital circuits can usually tolerate the rather coarse tolerances and limited ranges for monolithic resistors. They may also be designed to operate over a wide range of speed without any capacitors. A large number of companies offer monolithic integrated flip-flops, gates, shift registers, and other digital circuits as standard items.

Analog circuits are much more likely to be custom designed although common circuits such as operational amplifiers are currently available as standard circuits. FIGURE 8 shows the circuit diagram of one such amplifier (A-702-A) offered by Fairchild Semiconductor and yielding an open-loop voltage gain of several thousand and an equivalent input drift due to temperature of about 5 μv./^{o}C.

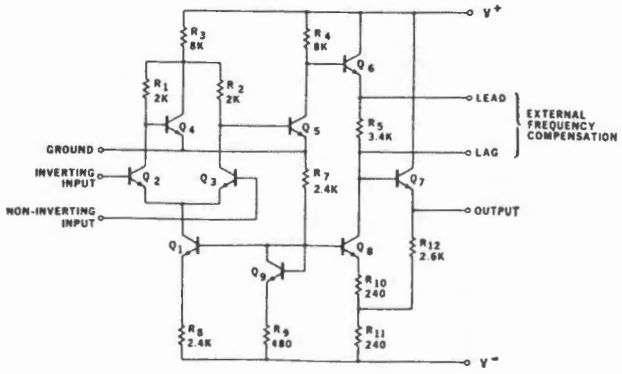


FIGURE 8 - An example of an integrated operational amplifier.

Radio-frequency amplifiers require tuned circuits and are, consequently, not the easiest circuits to integrate. Nonetheless, some units have been built using monolithic chips combined with discrete microminiature inductors. Motorola has developed a 60-mc. amplifier with a 10-mc. bandwidth and an over-all gain of 61 db minimum. Eight modules of four different types (input matching network, standard amplifier stage, interstage tuning network and filter, and detector) are used and each is contained within a 10-lead T0-5 can.

Testing Integrated Circuits

Testing of integrated circuits might at first seem practically impossible from the service technician's viewpoint. He cannot get at any of the individual components within a given module for replacement. Actually, if we consider any given integrated circuit as a component with a given input and output requirement, the task becomes more reasonable. Since we cannot repair the inside parts of an integrated circuit, we need not concern ourselves with pinpointing the specific component which failed, unless a critical failure analysis is necessary in order to provide direction for a design change.

The integrated circuit is tested by applying the required bias levels, providing the various input conditions, and monitoring the output to see if the specs are satisfied. Since temperature effects may be the cause of some troubles, it will generally be necessary to perform some testing at the extreme temperature conditions to eliminate marginal circuits which might work perfectly well at room temperatures.

In the fabrication of integrated circuits, especially those of the monolithic variety, the testing cost represents a sizable portion of the total. Many circuits of the same type are usually made on a single wafer of semiconductor material. It is necessary to test these individual circuits as soon as possible in order to prevent any waste of labor on units which are defective. In some cases, it is only necessary to do a rough check on the individual chip and then perform a more complete test after the chip has been packaged.

Circuits using the hybrid thin-film, thick-film, and monolithic combination may be modified by trimming their individual resistors. It may be wise to perform a complete functional test on the circuit before the conformal coating is added. The resistor adjustment can be made while the circuit is actually operating.

GLOSSARY

accumulator	A register; holds either an operand or the result of an arithmetic operation
addend	number to which the augend is added in an arithmetical sum; for example: ADDEND AUGEND SUM
array	series of items arranged in a meaningful pattern
assembler	software translator which converts instructions and data in mnemonic codes to machine language
augend	number which is added to the addend in an arithmetical sum; for example: ADDEND AUGEND SUM
binary number system	number system in which only two digits are used, 0 and 1; hence it has a radix or base of two
bit	digit used in the binary number system; can be either 0 or 1; the word bit is an acronym of BInary digiT
byte	group of bits forming a part of a word; usually 12
complement	something which is added to make an item complete
complex numbers	real and imaginary numbers mixed together
data	information which is to be used in solving a problem
difference	result of a mathematic subtraction operation
discrete value	individual value
dividend	number to be divided
divisor	number by which a dividend is divided

eight's complement	octal number obtained by subtracting the number for which the complement is to be found from the modulus of the system
end-around borrow	borrow generated in the most significant stage is subtracted from the least significant stage
end-around carry	carry generated in the most significant stage and added to the least significant stage
factoring	process by which a term which is common to all parts of an expression is extracted
function	operation to be performed
hexadecimal number system	number system in which 16 digits are used, 0 through 9 and the letters A, B, C, D, E, and F; radix or base is 16
imaginary numbers	number that is or can be expressed as the square root of a negative number; e.g., $\sqrt{-1}$, $\sqrt{-15}$, and $\sqrt{-25}$.
implement	to carry out
instruction	coded program step that tells a computer what to do for a single operation in a program
integer numbers	whole numbers starting at zero and extending either positively or negatively in whole increments
minterm	symbolic product of a given number of variables having neither vincula over more than one variable nor signs of grouping
minterm expression	expression composed of minterm and/or minterm-type terms separated by OR signs and having no parentheses or vincula extending over more than one variable
minterm-type term	minterm with one or more variables missing
minuend	number from which the subtrahend is subtracted in an arithmetical difference; for example:

MINUEND
SUBTRAHEND
DIFFERENCE

modulus	number of discrete states a counting device can attain; found by raising the base of the number system to a power given by the number of counting positions
multiplicand	number that is to be multiplied by another
multiplier	number by which another number is to be multiplied
nine's complement	decimal number obtained by subtracting the number for which the complement is to be found from the modulus of the system minus one
nonpositional number system	system wherein a symbol always has the same value regardless of its position in a number
octal number system	number system in which eight digits are used, 0 through 7; hence, the radix or base is eight
one's complement	binary number obtained by subtracting the number for which the complement is to be found from the modulus of the system minus one
operand	number to be used in an arithmetic operation
overflow	condition which occurs if the modulus of a device is exceeded
positional number system	system wherein the position of a digit determines the value of the number
product	result of a multiplication operation
program	logical sequence of instructions to be executed by a computer to solve a problem
quotient	result of a division operation
radix	number of distinct values that may be expressed in any given position
rational numbers	numbers that are divided into two catagories: integer and fractional
real numbers	number which is considered either rational or irrational

remainder	that part of the dividend which is left after a division operation
seven's complement	octal number obtained by subtracting the number for which the complement is to be found from the modulus of the system minus one
sign bit	most significant bit of a binary number in a signed register
subtrahend	number which is subtracted from the minuend in an arithmetical difference; for example: MINUEND SUBTRAHEND DIFFERENCE
sum	result of a mathematical addition operation
symbolic product	result of ANDing several variables together
ten's complement	decimal number obtained by subtracting the number for which the complement is to be found from the modulus of the system
truth table	table that describes a logical function by listing all possible combinations of input values and indicating the true output values for each such combination
two's complement	binary number obtained by subtracting the number for which the complement is to be found from the modulus of the system
vincula	plural of vinculum
vinculum	bar placed over a Boolean expression or term to denote negation

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