

*Equipment Diagrams*

**CONTROL DATA 8092**  
TELEPROGRAMMER

*Equipment Diagrams*

**CONTROL DATA 8092**  
TELEPROGRAMMER

# RECORD OF REVISIONS

REVISION NUMBER	NOTES
368 109 01 (Rev A)	(4-15-65) Includes ECO's 1163, 1198, 1268, 1334, 1354, 1402, 1403, 1411, 1431, 1470, 1505, and 1585.
368 109 00b (Rev B)	(8-18-66) Includes ECO numbers 2041 and 2085 (Reprinting with revision).
Revision C	(3-10-67) Includes ECO's DP2329 and DP2383.
Revision D	(8-29-67) Includes ECO's DP2055, 2249, 2279, 2500, 2590, 2356, 2329, 2328, 2370, 2365, 2512, 2450, and 2383 (Reprinting with revision).
Revision E	(11-8-67) Incorporated FCO's DP 2329, 2450
Revision F	(1-25-68) Revised to incorporate FCO DP2870. Pages revised: Pages 2, 5, 18.
Revision G	(4-23-68) Reprint with revision. Includes ECO DP2886. Addition of list of terms.
Revision H	(8-15-68) Revised to incorporate FCO DP03130. Page revised: Page 2 of 36042600.
Revision J	(1-30-69) Revised to incorporate ECO DP03333 and to add a schematic for the display panel. New product designations: 8092-A22/_B23/_-D08/_-E03. Revised Table of Contents, Pages vii, 16, and added pages 28, 29, 30 and 31.
Publication Number 368 109 00	

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10	Registers - P & P'	360430	27	8092 Display Schematic Note: For units having display panel (part number 47091200), use this schematic.	47094800
11	Register - PSR	364159	31	Power Supply Schematic (8092-D/-E)	47046500
12	Register - S & S'	364160			
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8092 TERM LIST

<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>	<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>
A000, A010, A070	A Register	8	F081	001 XXX	4
A100, A110, A170	A' Register	7	082	01X XXX	4
C000- C007	Clocks	13	083	01X XXX	4
E000, E010-, E070	Stage Enable (SE) F/F's	6	084	100 XXX	4
E001, E011-, E071	No Stage Enable (SE) F/F's	6	085	101 XXX	4
E200, E201, E202	Group Enable (GI) A' Register	7	086	110 XXX	4
E300, E301, E302	Group Borrow Generators (GBG) A' Register	7	087	111 XXX	4
E400, E401, E402	Group Borrow Input (GBI) A' Register	7	088	000 XXX	4
E500, E501-, E507	Stage Probe Input (SPI) A' Register	7	089	000 XXX	4
F002	XXX XX0	4	090	001 XXX	4
003	XXX XXI	4	091	100 XXX	4
012	XXX XOX	4	092	101 XXX	4
013	XXX XIX	4	093	101 XXX	4
014	XXX XOX	4	094	110 XXX	4
015	XXX XIX	4	095	110 XXX	4
022	XXX OXX	4	096	111 XXX	4
023	XXX IXX	4	097	111 XXX	4
025	XXX IXX	4	098	111 XXX	4
031	XX0 XXX	4	099	111 XXX	4
041	XOX XXX	4	101	XIX XXX XX	4
042	XOX XXX	4	112	000 XXX	4
050	IXX XXX	4	114	111 XXX	4
052	OXX XXX	4	115	111 IXX, 111 111	4
053	IXX XXX	4	120	111 01X	4
054	XXX 100	4	121	111 01X	4
056	XXX 000	4	122	111 01X	4
057	XXX XII	4	123	111 01X	4
059	XXX IXX, XXX 111	4	124	111 101	4
060	XXX X10	4	125	111 101	4
061	XXX 001	4	127	111 01X	4
062	XXX 010	4	130	000 101	4
063	XXX 011	4	131	XXX IX1	4
064	XXX 100	4	132	OXI XXX	4
065	XXX 110	4	133	OXI XXX	4
066	XXX 111	4	134	011 XXX	4
067	XXX X01	4	F200	$G \rightarrow \overline{[(Ent. + Swp.) (SSI)]} \overline{[(4X + SX.C')]}$	5
068	XXX X00	4	F206	$\overline{[(SSI) (OBA) + C \overline{[(Ent. + Swp.) (SSI)]}]} \overline{[(4X + 5X.C' + 76) + 72.C'B \overline{[(Ent. + Swp.) (SSI)]}]} \overline{[(SSI)]} A (Ent)(Swp.) (SSI) + D \overline{[(Ent. + Swp.) (SSI)]} + (Swp.)}$	5
069	XXX X10	4	F208	(Buff BSY) (04 + 05 + 70 + 71) + 6X (Jump SAT)	5
070	XXX 00X	4	F209	F208	5
071	XXX 001	4	F211	6X (Jump SAT) + (Buff BSY) (04 + 05 + 70 + 71)	5
072	XXX 010	4	F213	$\overline{17 + 23 + 24 + 27 + 33 + 37 + 44 + 45 + 46 + 47 + 52 + 56}$	5
073	XXX 011	4	F214	$31 + 35 + 41 + 45 + 51 + 55 + 72.C' + 73.C'$	5
074	XXX 100	4			
075	XXX 110	4			
076	XXX 111	4			
077	XXX X01	4			
078	XXX 00X	4			
079	XXX IX1	4			
080	000 XXX	4			

<u>Logical Symbol</u>	<u>Function</u>	<u>Page</u>	<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>
F216	$\overline{[(Ent. + Swp.) (SSI)]} [B (11 + 15 + 41 + 45 + 51 + 55 + 72.C' + 73.C') + C (load + 00 + 04 + 05 + 10 + 14 + 20 + 24 + 30 + 34 + 6X + 70 + 71 + 72 + 73 + 74 + 75)] + A [(Ent.) (Swp.) (SSI)] + D (Ent. + Swp.) (SSI) + (Ent. + Swp.)$	5	F311	$\overline{Z \rightarrow F/F'}$	5
F222	$\overline{[(Ent. + Swp.) (SSI)]} [B (11 + 15 + 41 + 45 + 51 + 55 + 72.C' + 73.C') + C (Load + 00 + 04 + 05 + 10 + 14 + 20 + 24 + 30 + 34 + 6X + 70 + 71 + 72.C' + 73.C' + 74 + 75)] + A [(Ent.) (Swp.) (SSI)] + D [(Ent. + Swp.) (SSI)] + (Ent. + Swp.)$	5	F313	$\overline{Z \rightarrow Ou}$	5
F226	$12 + 16 + 22 + 26 + 32 + 36 + 42 + 46$		F315	$\overline{+Z \rightarrow R}$	5
F229	$11 + 12 + 13 + 15 + 16 + 17 + 22 + 23 + 26 + 27 + 31 + 32 + 33 + 35 + 36 + 5X.C' + 4X$	5	F316	$\overline{-Z \rightarrow R}$	5
F232	$04 + 05 + 20 + 21 + 22 + 23 + 30 + 31 + 32 + 33 + 5X + 70 + 72 + 74 + 75 + IX + 4X + 6X$	5	F317	$\overline{+I \rightarrow R}$	5
F233	$72 + 73 + 75$	5	F318	$\overline{A \rightarrow R}$	5
F235	01	5	F319	$\overline{A \rightarrow Q}$	5
F236	$5X + 72 + 73 + 75$	5	F320	$\overline{A.2' \rightarrow Q}$	5
F239	$5X.C' + 75.C' + (72 + 73) (A' 0) (I/O Seq.)$	5	F321	$\overline{+I \rightarrow Q}$	5
F242	$(Load) + 6X (Jump SAT) + 40 + 44 + 77 + (Buff BSY) (04 + 05 + 70 + 71)$	5	F322	Block Probe A'	5
F243	$C' + 55 + 75$	5	F323	$\overline{A' \rightarrow A}$	5
F248	A/O	5	F324	$\overline{A \rightarrow Tag Reg}$	5
F251	Jump SAT	5	F325	$\overline{Tag Reg \rightarrow A}$	5
F252	Jump SAT	5	F326	$\overline{A \rightarrow BER, I_3 \rightarrow BER}$	5
F256	$20 + 21 + 22 + 23 + 30 + 31 + 32 + 33 + (72 + 73) C [(Ent. + Swp.) (SSI)]$	5	F327	$\overline{A \rightarrow BXR, I_3 \rightarrow BXR}$	5
F261		5	F328	$\overline{BER \rightarrow A}$	5
F271	13	5	F329	$\overline{A' \rightarrow P, Tag \rightarrow P'}$	5
F300	$\overline{Adv. P_1 \text{ by } I}$	5	F331	$\overline{INP \rightarrow Z: 76 + \bar{C} + (Ent + Swp) + (SSI)}$	5
F301	$\overline{P_2 - P_1}$	5	F332	$01 + \bar{D} + (Ent. + Swp) + (SSI)$	7
F302	$\overline{P \rightarrow S, P' \rightarrow S'}$	5	F580	$70 + 71$	18
F303	$\overline{5.C'}$	12	F502	$\overline{[(Load + (Clear F/F') + (Ent + Swp))] (70 + 71)}$	18
F304	$\overline{Z \rightarrow S}$	5	F503	$\overline{[(Load) (Clear F/F') (Ent + Swp)] (70 + 71)}$	18
F305	$\overline{Tag \rightarrow S'}$	5	G000 - G207	Read Write Drivers	13
F306	$\overline{A \rightarrow S}$	5	H000 - H007	Plain Timing Delay's	3
F307	$\overline{MCS \rightarrow Z}$	5	H201 - H231	SSC Timing Delay's	2
F308	$\overline{INP \rightarrow Z: (Ent. + Swp.) (SSI) [B.72.C' + C(load)]}$	5	I001 - I005	Z Register	9
F310	$\overline{Clear F/F'}$		I006	Enables -- S	12
			I011 - I015	Z Register	9
			I016	S Register	12
			I021 - I025	Z Register	9
			I026	S Register	12
			I031 - I034	Z Register	9
			I036	S Register	12
			I041 - I045	Z Register	9
			I046	S Register	12
			I051 - I055	Z Register	9
			I056	S Register	12
			I061 - I065	Z Register	9
			I066	S Register	12
			I071 - I075	Z Register	9

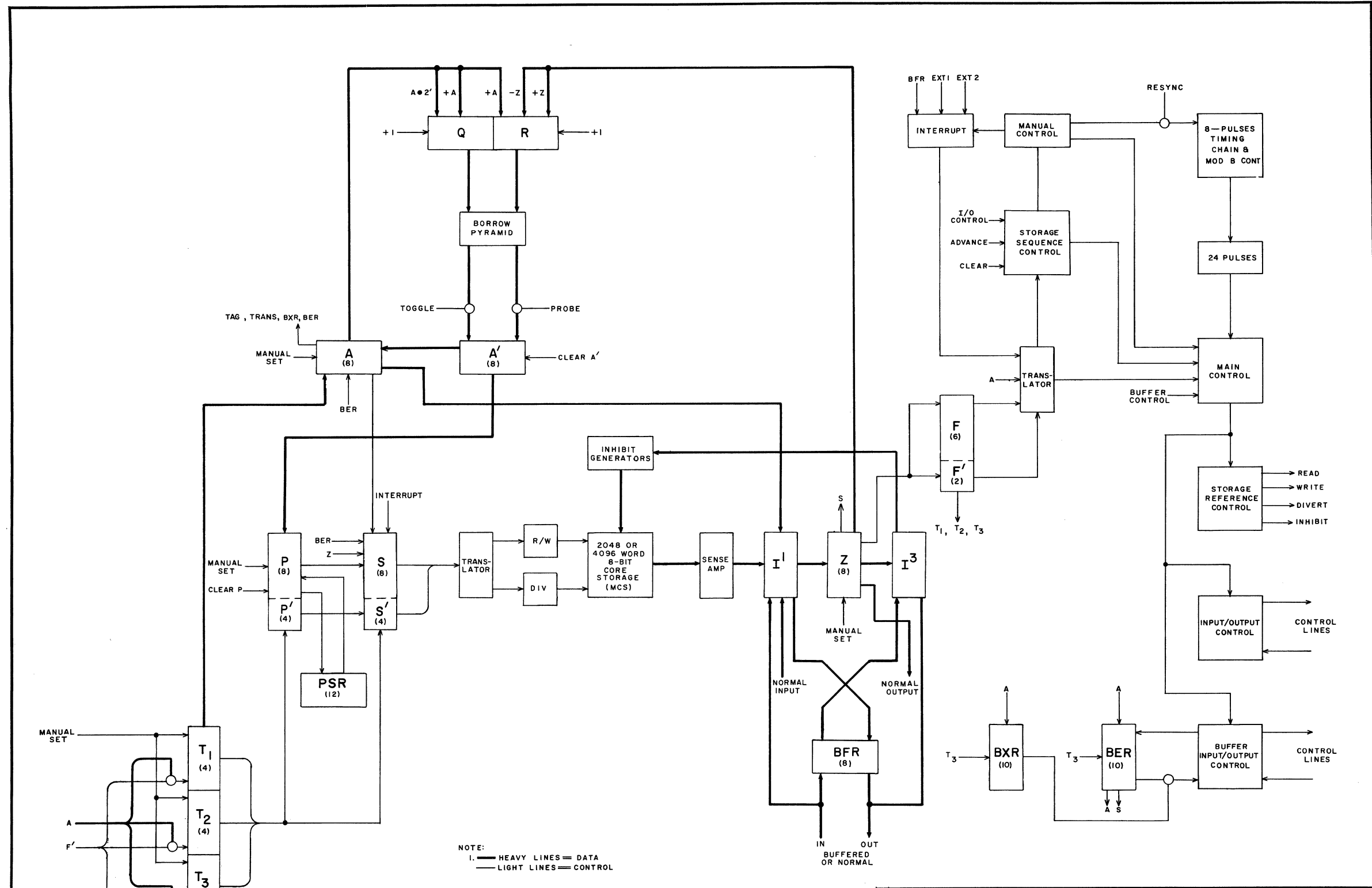
<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>
I076	S Register	12
I200 - I219	A Register	8
I300 - I369	Tag Register 1, 2, 3	15
I400 - I401	A' Register	7
I402	A' ≠ 0	7
I403	A' = 0	7
I404 - I414	O Register	8
I500 - I538	BFR, BER, BXR	19
I519	BER = BXR	
I550	A ( $\overline{\text{Ent}}$ ) ( $\overline{\text{Swp}}$ ) ( $\overline{\text{SSI}}$ ) + B ( $\overline{\text{Ent} + \text{Swp}}$ ) ( $\overline{\text{SSI}}$ ) + (74 + 75 + 76) [ $\overline{\text{D}}$ ( $\overline{\text{Ent} + \text{Swp}}$ ) ( $\overline{\text{SSI}}$ )] (Load + [ $\overline{\text{Ent.} + \text{Swp}}$ ] (13) (00 + 01 + 02 + 03 + 06 + 07 + 77) (011 5X (Jump SAT) + (04 + 05 + 70 + 71) (Buff BSY)] + C ( $\overline{\text{Ent} + \text{Swp}}$ ) ( $\overline{\text{SSI}}$ ) (55 + 75)	18
I551	( $\overline{\text{IBA}}$ ) + ( $\overline{\text{OBA}}$ )	18
I554	(Buffer Cycle)	18
I560	BFR → Buff Output Cable (B. O. C)	18
I561	Z → B.O.C.	18
I562	Z → B.O.C.	18
I570	(Buff RDY) + (IBA) + ( $\overline{\text{input RDY}}$ )	18
I571	INP → BFR	18
I573	(Buffer Cycle) + (OBA) + (Time 22)	18
I574	MCS → BFR	18
I577	Buff INP Cable → Z	18
I580	Clear Buffer Controls	18
I582	Clear Buffer	18
I588	(Buffer Busy)	18
I590	(SSI)	18
I593	(Buff Cycle)	18
I852	(Int. 10, 20, 30, 40)	17
I853	Block P → S	17
I857	(Block P → S) (I/O Seq) ( $\overline{\text{Ent} + \text{Swp}}$ ) ( $\overline{\text{Load}}$ ) ( $\overline{\text{I3}}$ )	17
I859	(Master Clear) (Time 26) (D ( $\overline{\text{Ent} + \text{Swp}}$ ) ( $\overline{\text{SSI}}$ ))	17
I860	Clear P, P'	17
I861	Interrupt Address → S	17
I862	(Int. 10, 20, 30, 40)	17
I863	Interrupt Address Enable → S	17 & 12
I872	Interrupt Address → PSR	17
J000 - J031	Main Control Timing	2
J100 - J103	<u>Main</u> Control Timing	3
J103	Recirc	

<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>
J104 - J107	Main Timing	3
J109 - J111	I/O Control	16
J107	Timing Error Stop	2
J200	A + (Ent) + (Swp) + (SSI)	2
J211 - J212	B [ $\overline{\text{Ent.} + \text{Swp.}}$ ] ( $\overline{\text{SSI}}$ )	2
J221 - J222 - J223	C [ $\overline{\text{Ent.} + \text{Swp.}}$ ] ( $\overline{\text{SSI}}$ )	2
J224 - J225 - J226	C'	2
J227 - J228	$\overline{\text{C}}$ '	2
J231 - J232 - J233	D ( $\overline{\text{Ent.} + \text{Swp.}}$ ) ( $\overline{\text{SSI}}$ )	2
J235		2
J243		2
J400 - J440	I/O Control	16
J441	(I/O Seq. Set)	16
J446	(Load) + B [ $\overline{\text{Ent.} + \text{Swp}}$ ] ( $\overline{\text{SSI}}$ )	16
J560	(Main Timing Fault)	2
J562 - J565	Storage	13
J900	(Master Clear)	3
J901 - J902 - J903		
J904	(Master Clear)	3
J907	(Master Clear ( $\overline{\text{Clear Z}}$ ))	3
J908	(Master Clear) (Clear P)	3
J909 - J910	Clear P'	3 & 10
J912	Load	3
J913	Load	3
J914	Enter	3
J917 - J921	(Enter + Sweep)	3
J923	Load	3
J930	(Master Clear)	3
K000 - K002	Timing Chain Excursion Counters	2
K010 - K013		
K100	Divert	13
K110	Read	13
K120	Write	13
K130	Inhibit	13
K140	Timing Fault	2
K200	A Cycle	2
K210	B Cycle	2
K220	C Cycle	2
K222 - K224	C' Cycle	2
K230	D Cycle	2
K240	Block P <sub>2</sub> = P <sub>1</sub>	3
K320	Wait Output	16
K322	Function Ready	16
K420	Wait Input	16

<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>	<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>
K440	I/O Seq.	16	N212	$\overline{[(A \rightarrow \text{Tag}) + D + (\text{Ent.} + \text{Swp.}) + (\text{SSI})]}$ (Time 01)	7
K522	Sample	16	N230	Toggle A': $\overline{N232}$	7
K524	Enable	16	N232	$\overline{[(A \rightarrow \text{Tag}) + \overline{D} + (\text{Ent.} + \text{Swp.}) + (\text{SSI})]}$ (Time 23)	7
K800 - K802 - K810	Resync. Counter	2	N800 - N801	Clocks	2
K812	Manual Interrupt	16	0000 - 0010 - 0050	O Register	6
K850	Manual Interrupt	16	P000 - P010 - P070	P <sub>1</sub> Register	10
K852	Manual Interrupt	16	P002 - P012 - P072	P <sub>2</sub> Register	10
K854	Manual Interrupt 10	16	P100 - P110 - P120	P <sub>1</sub> Register	10
K856	Buffer Interrupt	16	P130	P <sub>1</sub> Register	10
K858	Buffer Interrupt 20	16	P102 - P112 - P122	P <sub>2</sub> Register	10
K860	External Interrupt 30	16	P132	PSR - Register	11
K862	External Interrupt 40	16	P200 - P314	Q Inverters	6
K864	Interrupt Lockout	16	Q000 - Q010 - Q070	R Inverters	6
K900	Run	3	R000 - R010 - R070	Divert F/F's, S Register	13/12
K902	Step	3	S000 - S010 - S050	R/W Driver F/F's, S Register	13/12
K904	Neutral	3	S060 - S070	R/W Drive F/F's, S Register	13/12
L000 - L010 - L110	O Register Inputs	8	S100 - S110 - S120	Storage Translators	13
L321	Information Ready	16	S130	Stage Borrow F/F's (SB)	6
L322	Function Ready	16	T000 - T507	Timing	3
L323	Master Clear	16	U000 - U010 - U070	Storage Sequence Control	2
L330	I/O Sequence	16	V000 - V046	I/O Start of Timing	16
L331	Load Mode	16	V201 - V231	Resync Timing	2
L421	Input Request	16	V521	Adv. P <sub>1</sub> by 1	10
L500 - L510 - L610	BFR Outputs	19	V901 - V903	Clear S and S'	12
L512	Information Ready	18	W000 - W005	Adv. BER: $\overline{(\text{Buff Cycle})}$ (time 13)	19
L513	Input Request	18	W020 - W023	ADV. BER	19
L514	Function Ready	18	W028	I0-6 → S	12
L515	Master Clear	18	W058	P <sub>1</sub> → P <sub>1</sub> P <sub>1</sub> → P <sub>2</sub> , P <sub>1</sub> → P <sub>2</sub>	10
M000 - M010 - M070	Z Register Inputs	9	W070 - W073	Clear Z	9
M330	Output Resume	16	W100	Strobe	9
M420	Input Ready	16	W102	Enable Z → S	12/17
M424	Input Disconnect	16	W110	Input → Z	9
M500 - M510 - M570	BFR Inputs	19	W122 - W124	Clear F, Z → F	4
M512	Output Resume	18	W130 - W160		
M513	Input Ready	18			
M514	Input Disconnect	18			
M850	Manual Interrupt Input	17			
M851 - M852	External Interrupt Input	17			
M900	Run	3			
M901	Step	3			
M902	Neutral	3			
M903	Load	3			
M904	Master Clear	3			
M905	Clear A	3			
M906	Clear Z	3			
M907	Clear P	3			
M908	Enter	3			
M909	Sweep	3			
N000 - N005	Timing Control	2			
N210	Clear A' : N212	7			

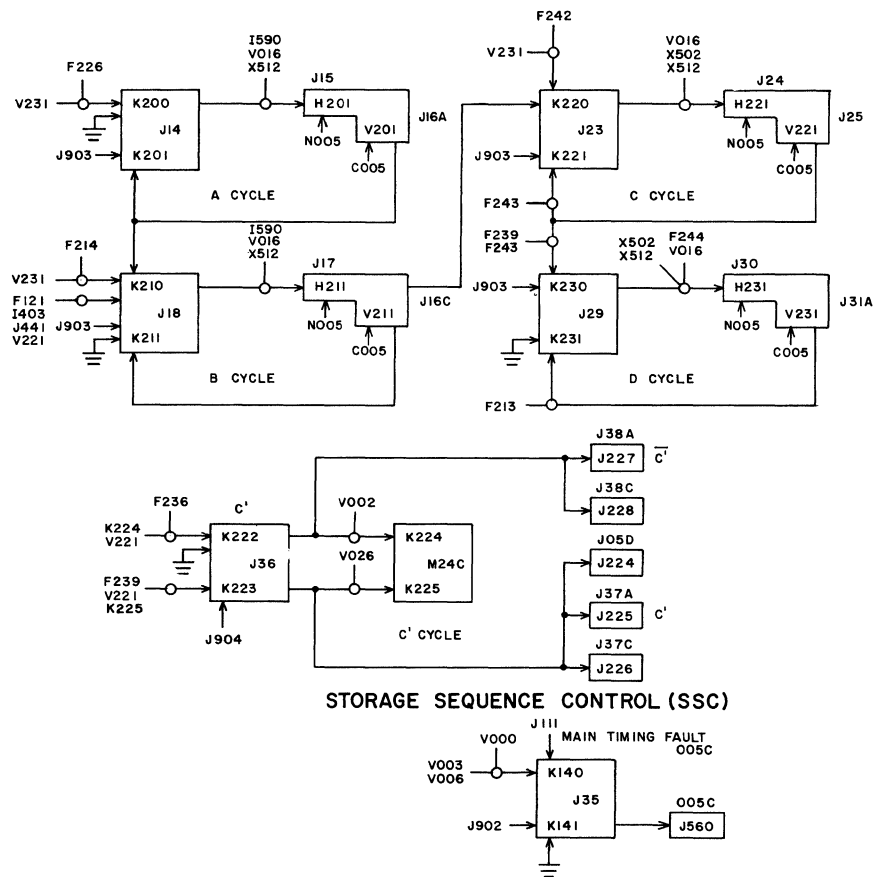


<u>Logic Symbol</u>	<u>Function</u>	<u>Page</u>
W162 - W164	Z → 0	8
W200 - W314	R & Q Inverters	6
W250 - W264	A <sup>†</sup> → A, BER → A, TAG → A	8
W266 - W269	A → BER	19
W320 - W327	Z Register	9
W330 - <del>W363</del>	BXR	19
W364 - W368	TAG 1, 2, 3	15
W370 - W375	(Buff Cycle) (Time 02)	19
W460 - W464	A <sup>†</sup> → P, TAG → P <sup>†</sup>	10
W800	P → P <sup>†</sup>	11
W810	$\overline{13} + (\text{Load}) + (\overline{\text{Clear F}}) + (\text{Ent.} + \text{Swp}) +$ (Time 23)	11
W813	13 (Load) (Clear F) ( $\overline{\text{Ent.} + \text{Swp.}}$ ) (Time 23)	11
X000 - X010 - X020 X030	Tag 1 Register	15
X100 - X110 - X120 X130	Tag 2 Register	15
X200 - X210 - X220 X230	Tag 3 Register	15
X500	Block Seq. Interrupt (F/F)	18
X502	Storage Seq. Interrupt (SSI) (F/F)	18
X504	Buffer Cycle (F/F)	18
X506	Buffer Ready (F/F)	18
X508	Buffer Input (IBA) (F/F)	18
X510	Buffer Output (OBA) (F/F)	18
X512	Buffer Step (F/F)	18
X514	Initiate Buffer Output (F/F)	18
X516	Buffer Busy (F/F)	18
X518	Buffer Sync. (F/F)	18
X700 - X710 - X770	BFR Register	
X800 - X810 - X890	BXR Register	19
X900 - X910 - X990	BER Register	19
X902 - X912 - X992		
Y006 - Y507	Storage	13
Z000 - Z010 - Z070	Z Register	9

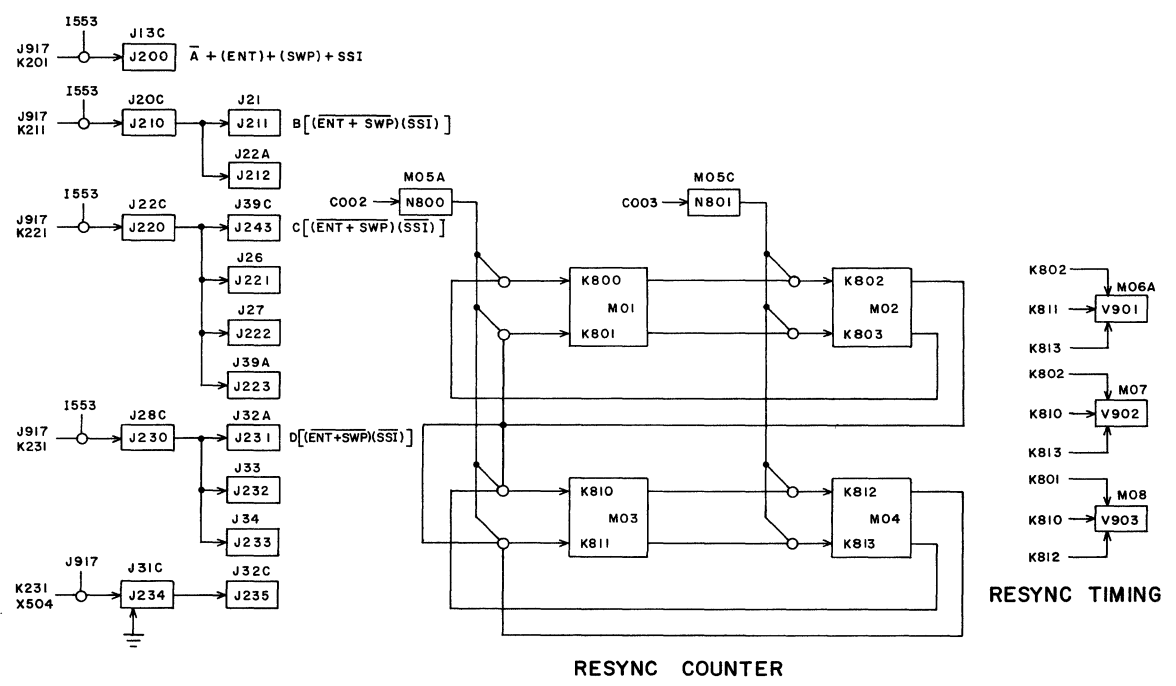


NOTE:  
 1. HEAVY LINES = DATA  
 2. LIGHT LINES = CONTROL

APPROVED: <i>[Signature]</i> DESIGNED: <i>[Signature]</i> DRAWN: <i>[Signature]</i> CHECKED: <i>[Signature]</i> REV. DATE: <i>[Date]</i> REVISIONS:	REFERENCE DRAWINGS		CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT	
	COMPONENTS (UNLESS OTHERWISE INDICATED)			
	TOLERANCE	VALUE		SIZE
	RESISTORS			
CAPACITORS				
TITLE: <b>BLOCK DIAGRAM, TELEPROGRAMMER - MODEL 8092</b>			DRAWING NUMBER: <b>364038</b>	
			REV: <b>A</b>	
			PAGE: <b>1</b>	

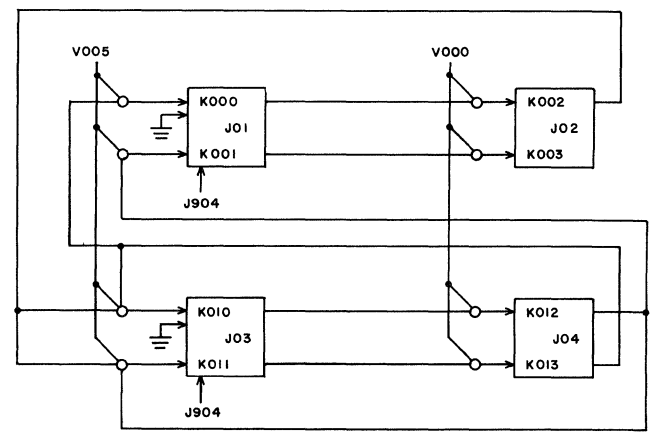


STORAGE SEQUENCE CONTROL (SSC)

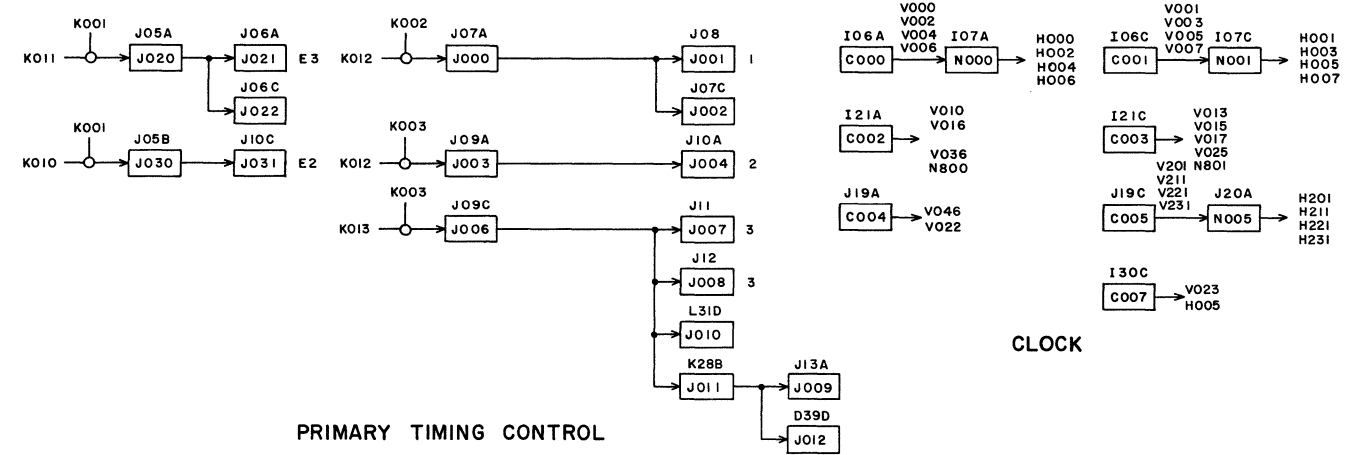


RESYNC COUNTER

RESYNC TIMING



TIMING CHAIN EXCURSION COUNTER (EK)



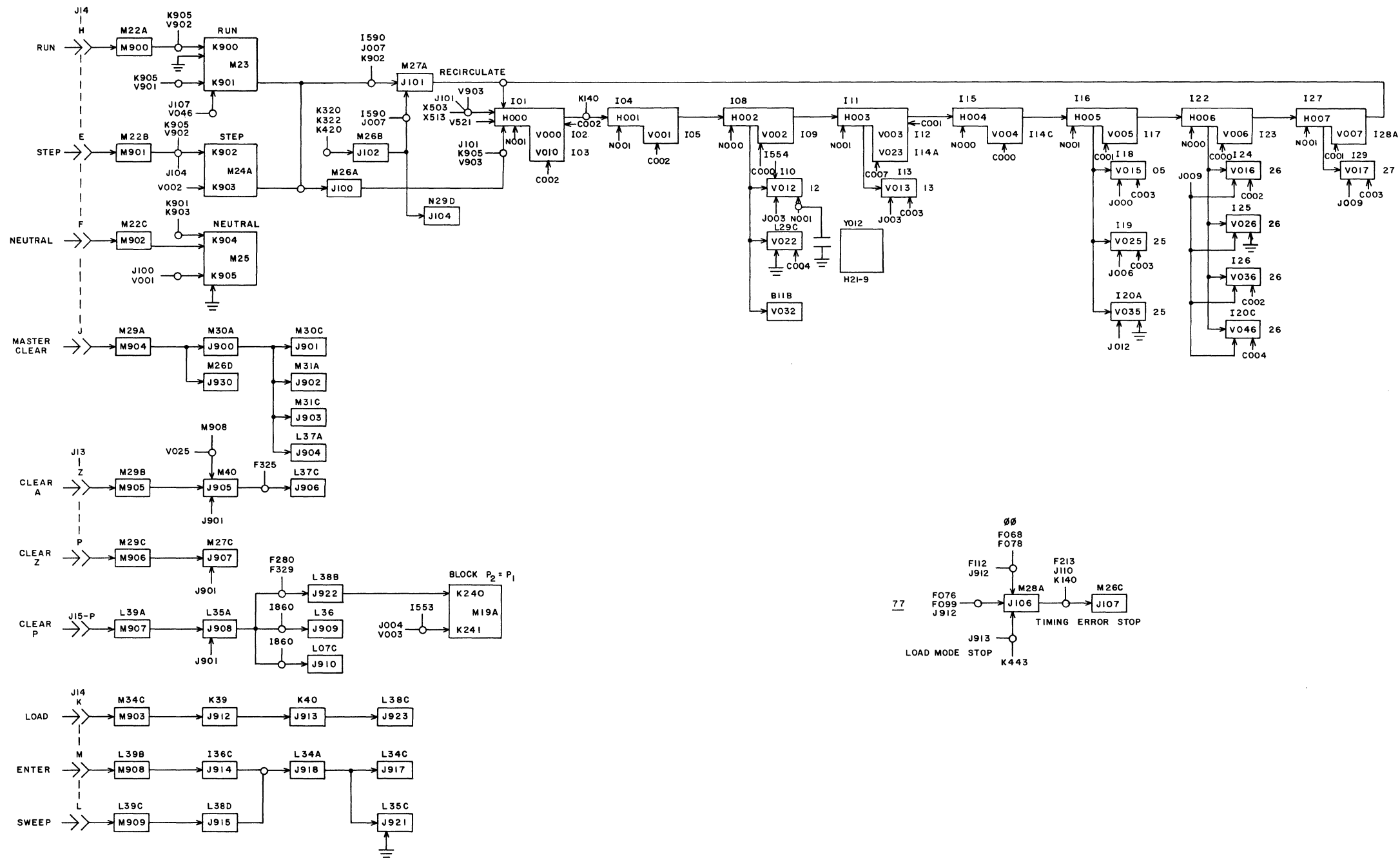
PRIMARY TIMING CONTROL

CLOCK

REV.	DATE	BY	CHKD.	REVISIONS
D	3/30/64	W.P.	K.H.	REVISED
C	3/27/64	W.P.	K.H.	REVISED
B	3/23/64	W.P.	K.H.	REVISED
A	3/18/64	W.P.	K.H.	REVISED

REFERENCE DRAWINGS		
COMPONENTS (UNLESS OTHERWISE INDICATED)		
RESISTORS	VALUE	SIZE
CAPACITORS		
TITLE		
LOGIC DIAGRAM, MAIN CONTROL		

CONTROL DATA CORPORATION  
I D P DIVISION  
PROJECT OR PRODUCT  
8092 TELEPROGRAMMER  
DRAWING NUMBER 36042600  
REV D  
PAGE 2



REV.		DATE	BY	CHK.	APPROVED
C	2041	2/24/64	J.H. NIPP		
B	1585	3/15/63	K.H. [unclear]		
A	1198	4/24/61	W.B. [unclear]		

REV.		DATE	BY	CHK.	APPROVED
APPROVED: J.H. NIPP					
CHECKED: J.H. NIPP					
DRAWN: F.N.K. BECK					
DESIGNED: [unclear]					

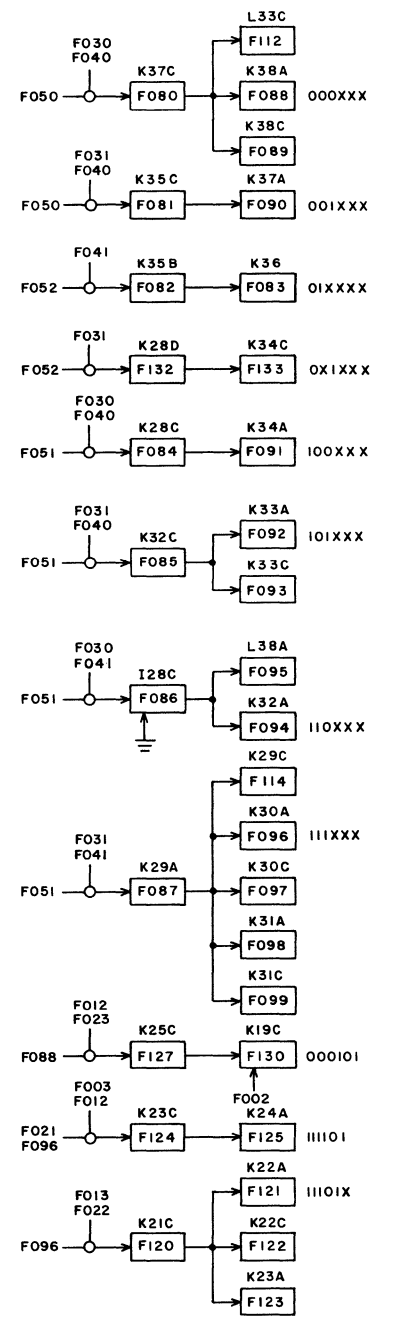
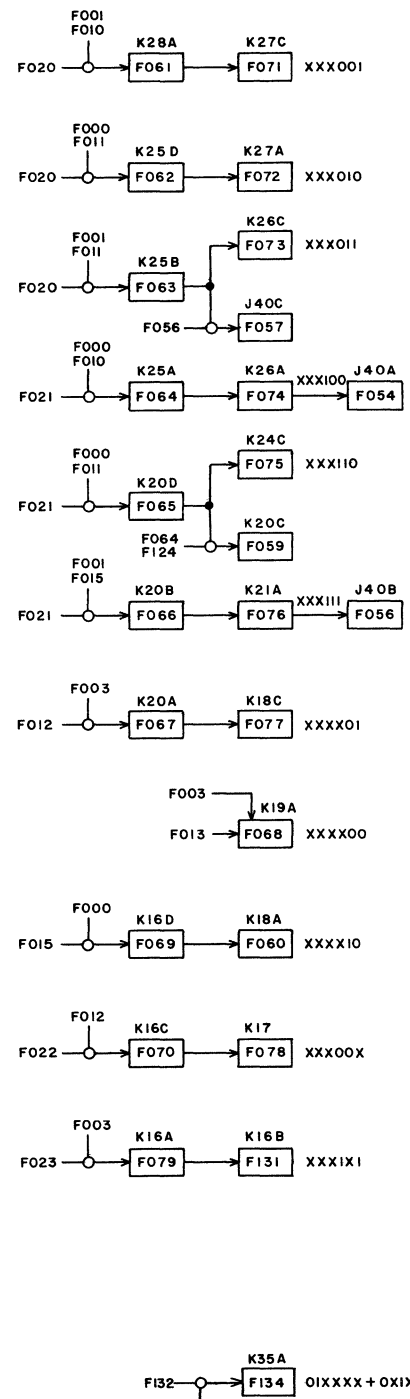
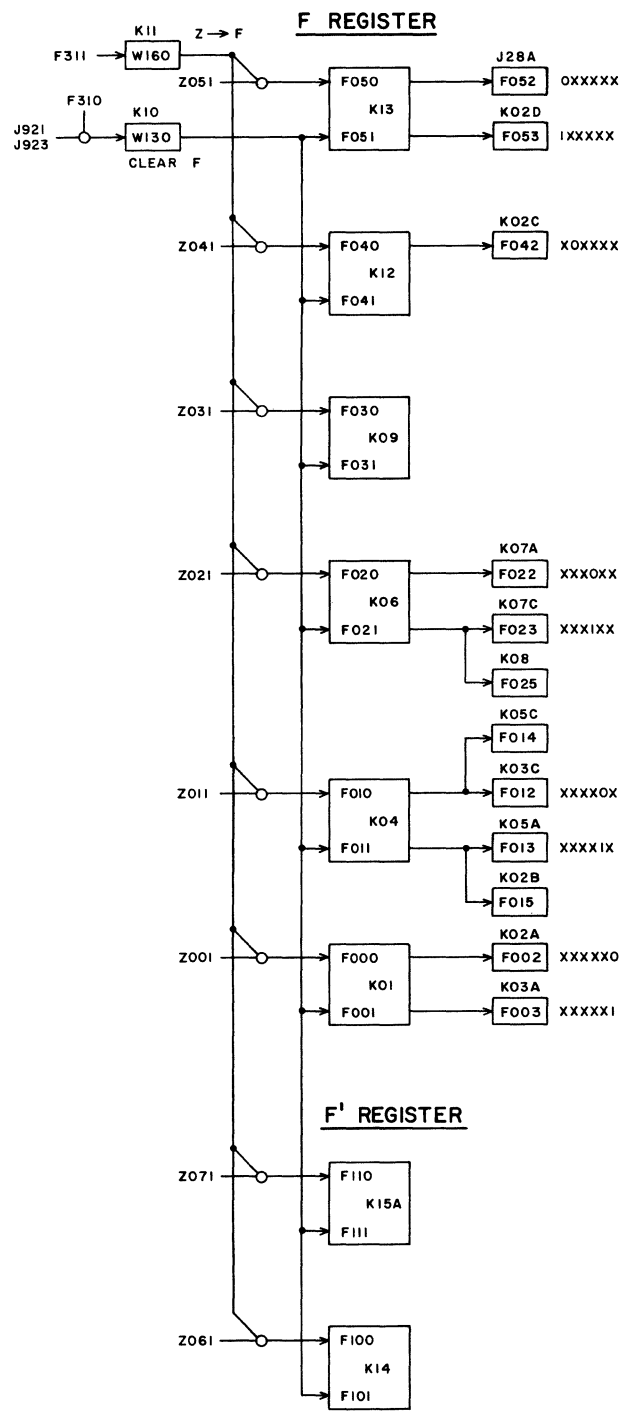
  

REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)			
RESISTORS	TOLERANCE	VALUE	SIZE
CAPACITORS			

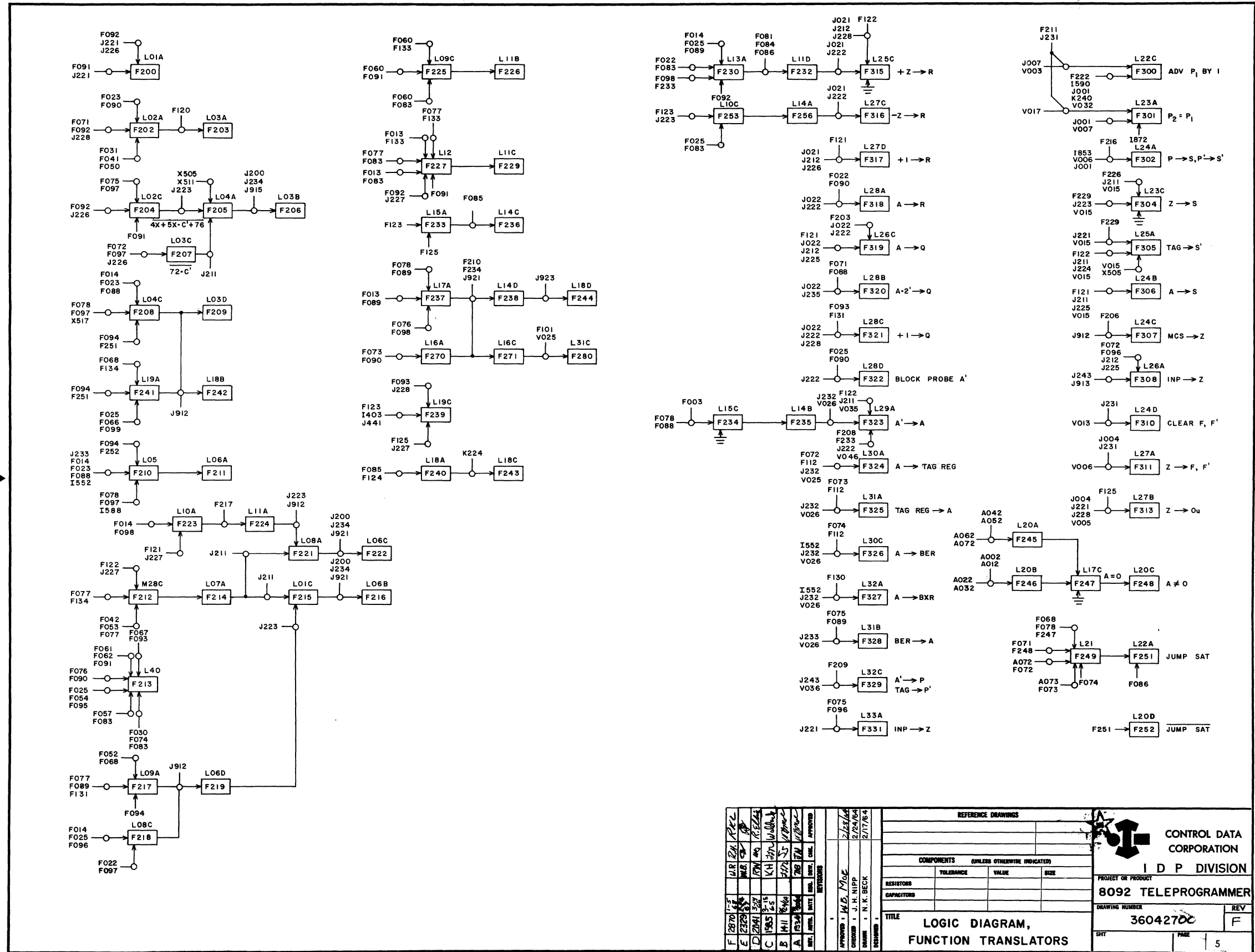
  

TITLE		LOGIC DIAGRAM, MAIN TIMING	
DRAWING NUMBER		364156	
REV		C	
SHT	PAGE	3	

CONTROL DATA CORPORATION  
I D P DIVISION  
PROJECT OR PRODUCT  
**8092 TELEPROGRAMMER**  
DRAWING NUMBER  
**364156**  
REV  
**C**  
SHT PAGE  
3



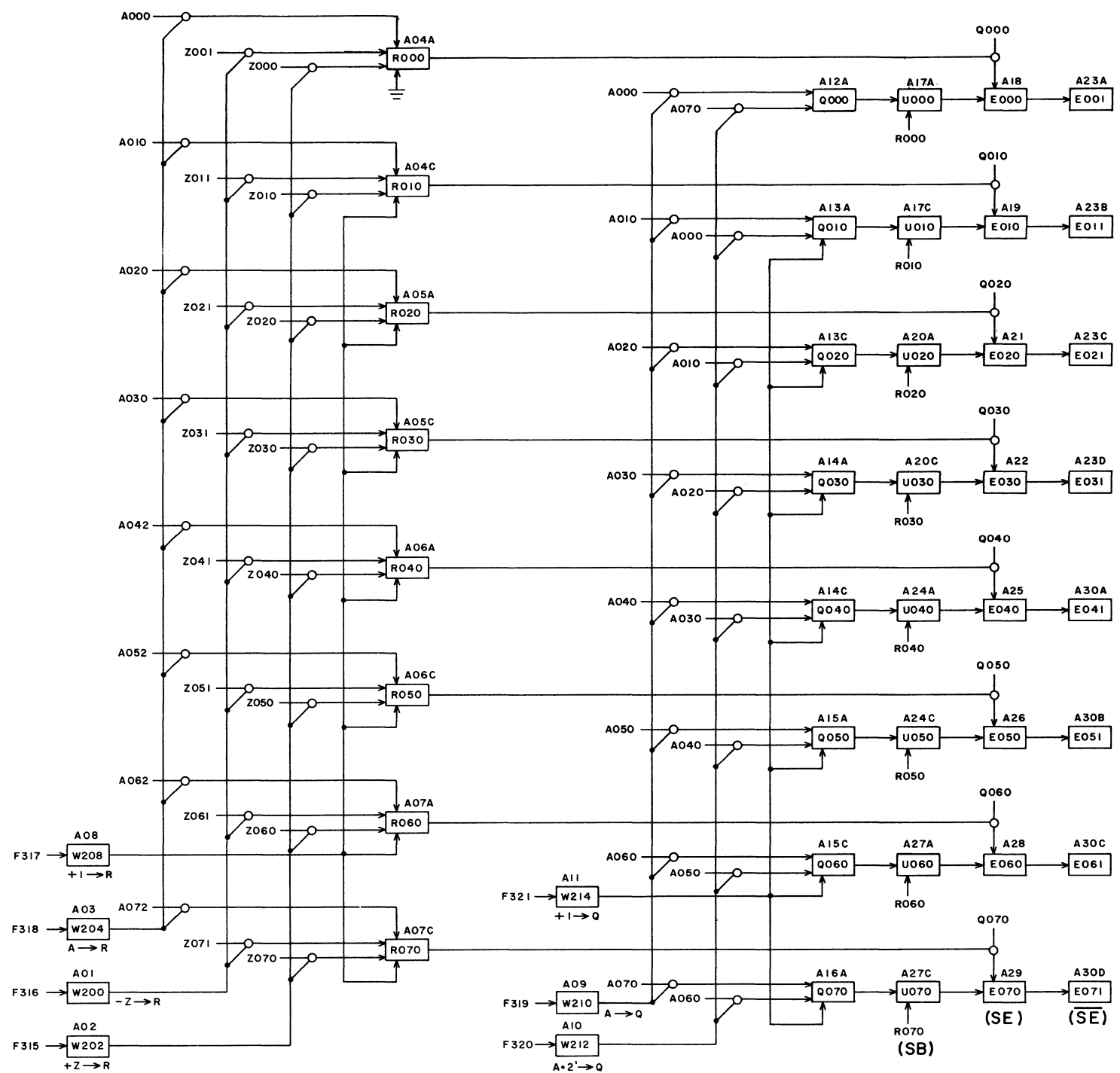
REV. NO.		REV. DATE		REV. BY		REV. CHK.		REV. APPR.	
C	2/14/64	B	1/25/64	A	1/22/64				
APPROVED: W.B. MOE CHECKED: J.H. NIPP DRAWN: I.K. BECK DESIGNED: I.K. BECK DATE: 2/14/64									
REFERENCE DRAWINGS COMPONENTS (UNLESS OTHERWISE INDICATED) RESISTORS CAPACITORS									
TITLE: LOGIC DIAGRAM, REGISTERS, F & F' & TRANSLATORS									
CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT: 8092 TELEPROGRAMMER								DRAWING NUMBER: 360449 REV: C	
DRAWING NUMBER: 360449 REV: C								SHEET: 4	



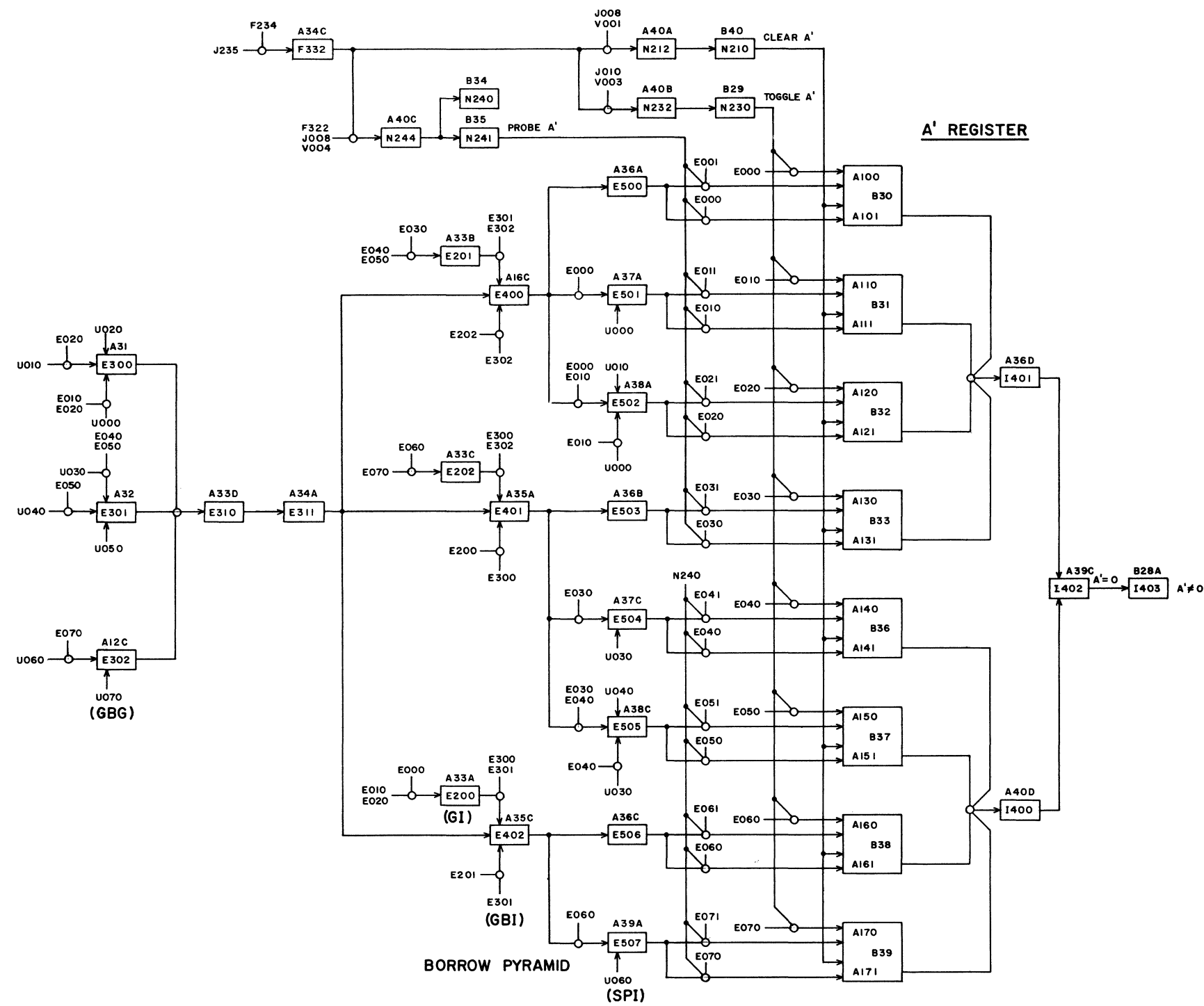
REV	DATE	BY	CHKD	APP'D	REVISIONS
F	2/27/64	W.B. McE	J.H. NIPP	N.K. BECK	2/28/64
E	2/27/64	W.B. McE	J.H. NIPP	N.K. BECK	2/28/64
D	2/27/64	W.B. McE	J.H. NIPP	N.K. BECK	2/28/64
C	2/27/64	W.B. McE	J.H. NIPP	N.K. BECK	2/28/64
B	2/27/64	W.B. McE	J.H. NIPP	N.K. BECK	2/28/64
A	2/27/64	W.B. McE	J.H. NIPP	N.K. BECK	2/28/64

REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)			
RESISTORS	TOLERANCE	VALUE	SIZE
CAPACITORS	TOLERANCE	VALUE	SIZE
TITLE			
LOGIC DIAGRAM, FUNCTION TRANSLATORS			
PROJECT OR PRODUCT			REV
8092 TELEPROGRAMMER			F
DRAWING NUMBER			REV
36042700			F
SHEET	PAGE		5



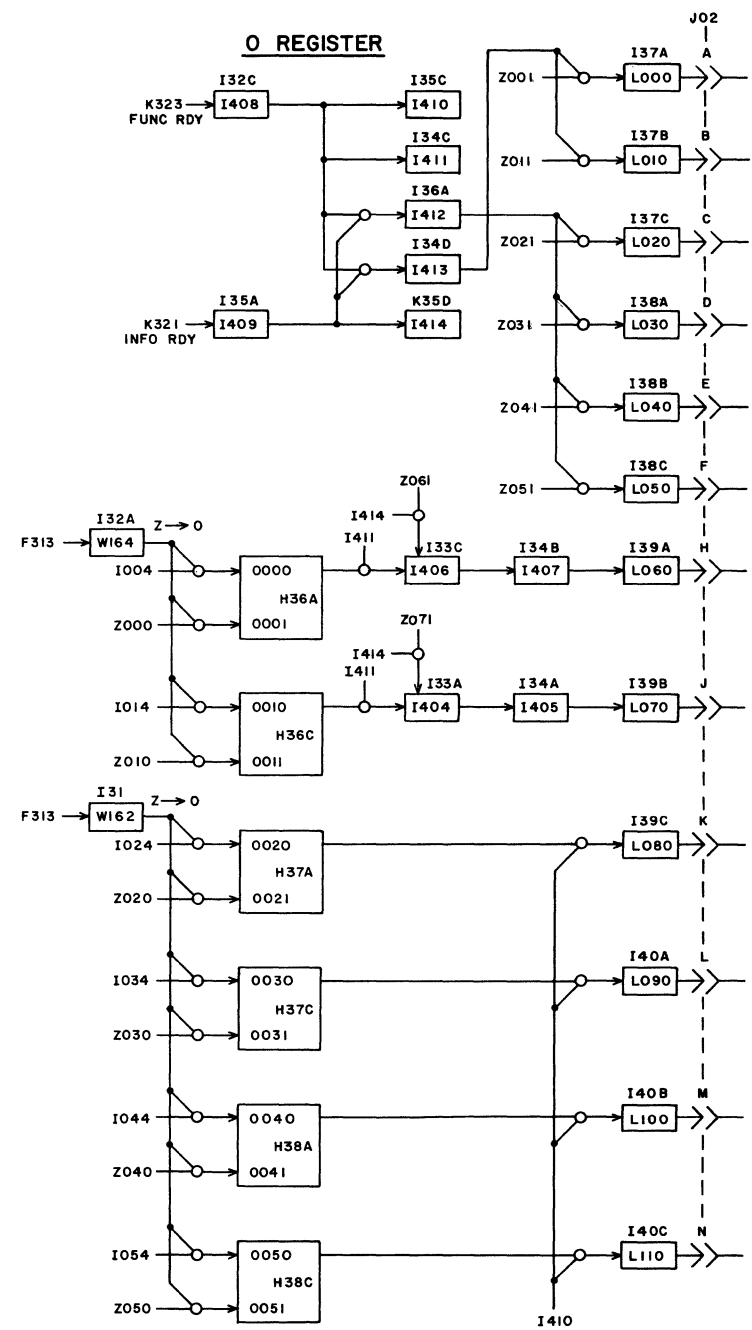
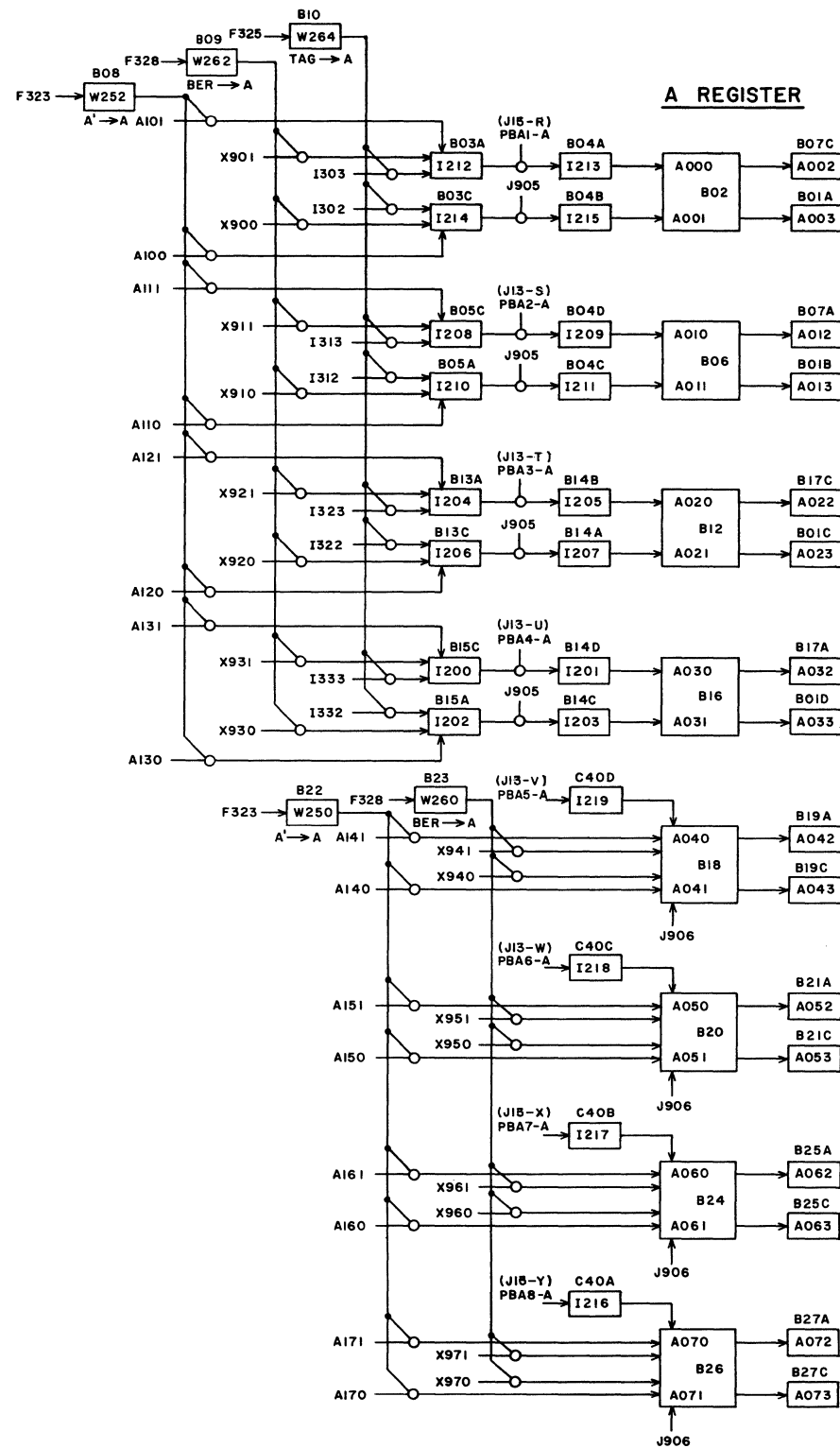


REV. AUTH. DATE REC. DRW. CHG. APPROVED REVISIONS 7/1/64 2/24/64 2/19/64 W.B. MOSE J.H. NIPP N.K. BECK DISBURSED	REFERENCE DRAWINGS		
	COMPONENTS (UNLESS OTHERWISE INDICATED)		
	RESISTORS	TOLERANCE	VALUE
	CAPACITORS		SIZE
TITLE LOGIC DIAGRAM, R AND Q INVERTERS			
CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER			DRAWING NUMBER 360428 REV
SHEET 6			PAGE 6



REV. AUTH. DATE 2/18/64 2/19/64 2/19/64	REFERENCE DRAWINGS		
	COMPONENTS (UNLESS OTHERWISE INDICATED)		
	TOLERANCE	VALUE	SIZE
	RESISTORS		
CAPACITORS			
TITLE			
LOGIC DIAGRAM, REGISTER - A'			
CONTROL DATA CORPORATION I D P DIVISION			
PROJECT OR PRODUCT			
8092 TELEPROGRAMMER			
DRAWING NUMBER		REV	
364157			
SHEET	PAGE		
7			





REV.	DATE	BY	CHK.	DESCRIPTION
C	12/11/54	R.M.	R.E.	REVISED
B	11/15/54	K.H.	J.H.	REVISED
A	11/14/54	T.B.	N.K.	REVISED

APPROVED: W.B. MOE	2/2/54
CHECKED: J.H. NIPP	2/2/54
DRAWN: N.K. BECK	2/9/54
DESIGNED:	

REFERENCE DRAWINGS	
COMPONENTS (UNLESS OTHERWISE INDICATED)	
RESISTORS	TOLERANCE VALUE SIZE
CAPACITORS	
TITLE	
LOGIC DIAGRAM	
REGISTERS - A AND O	

CONTROL DATA CORPORATION  
I D P DIVISION

PROJECT OR PRODUCT  
8092 TELEPROGRAMMER

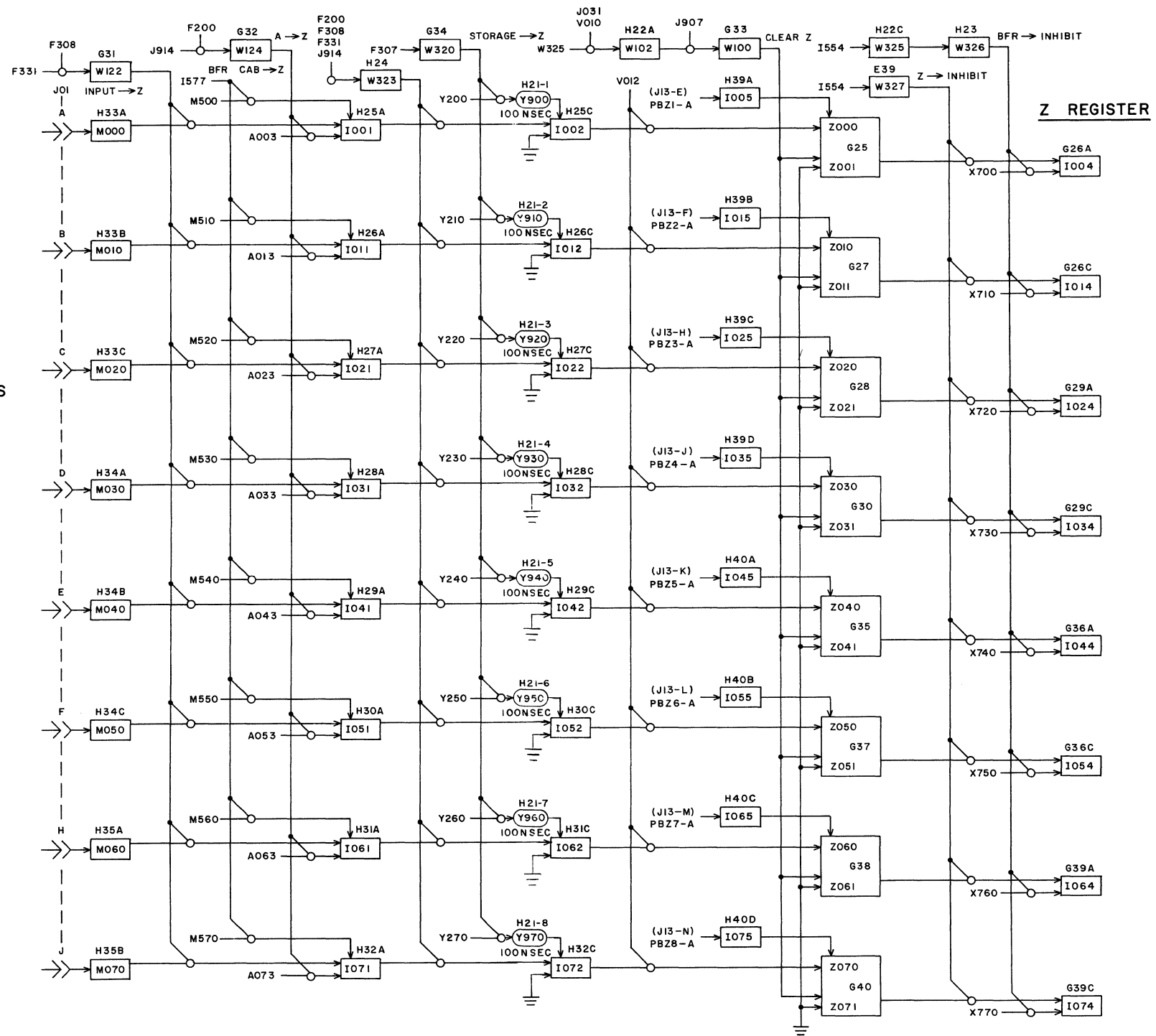
DRAWING NUMBER  
360429

REV  
C

SHT  
PAGE  
8

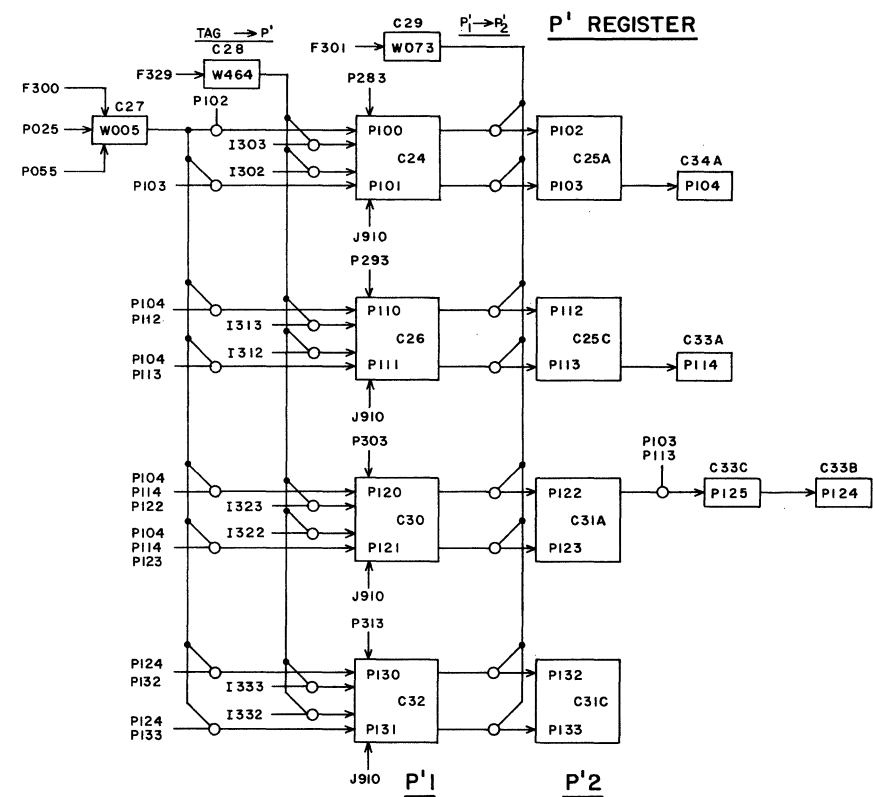
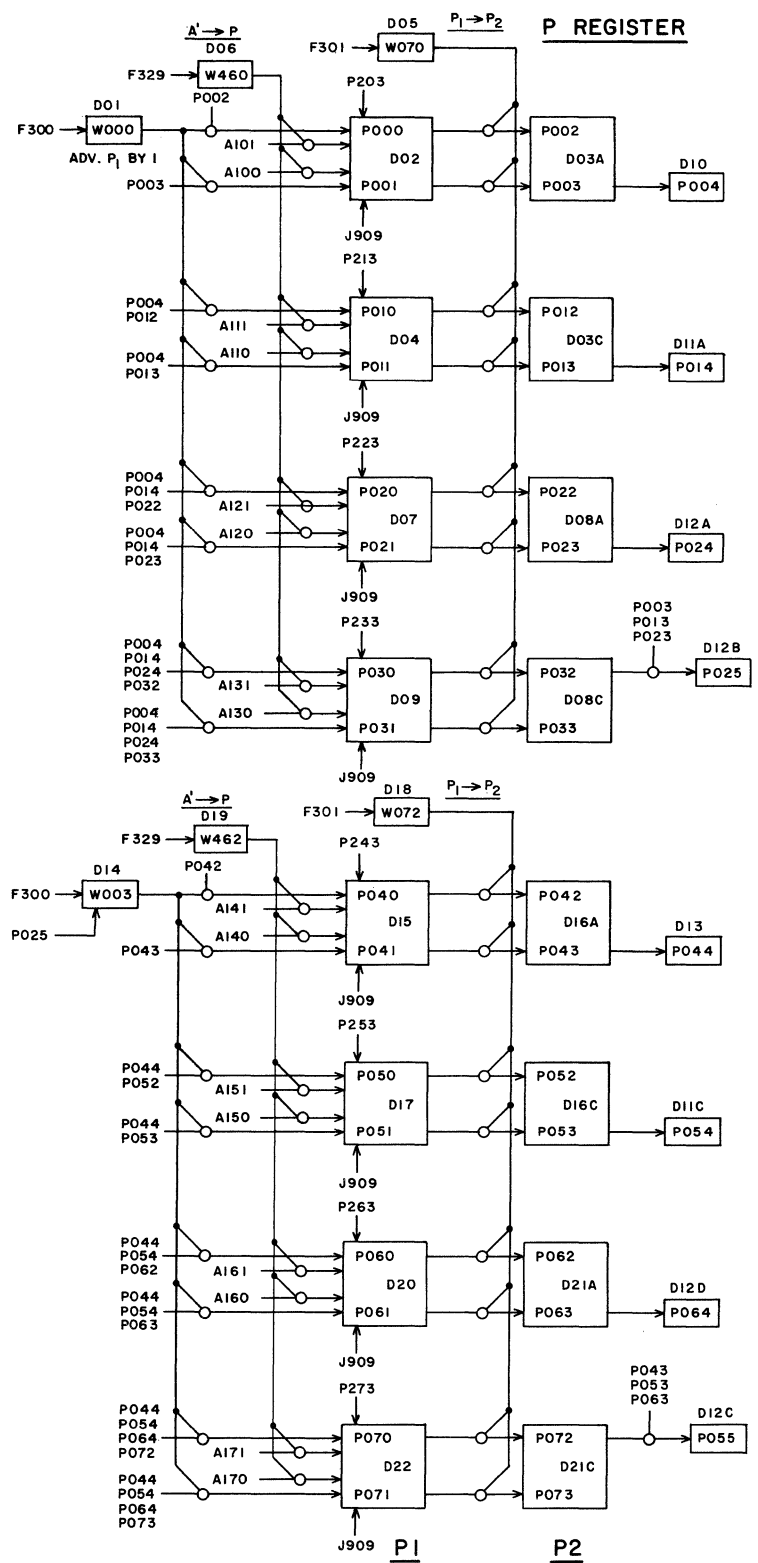
**SENSE AMPLIFIERS**

- H01 Y200
- H02 Y210
- H03 Y220
- H04 Y230
- H05 Y240
- H06 Y250
- H07 Y260
- H08 Y270

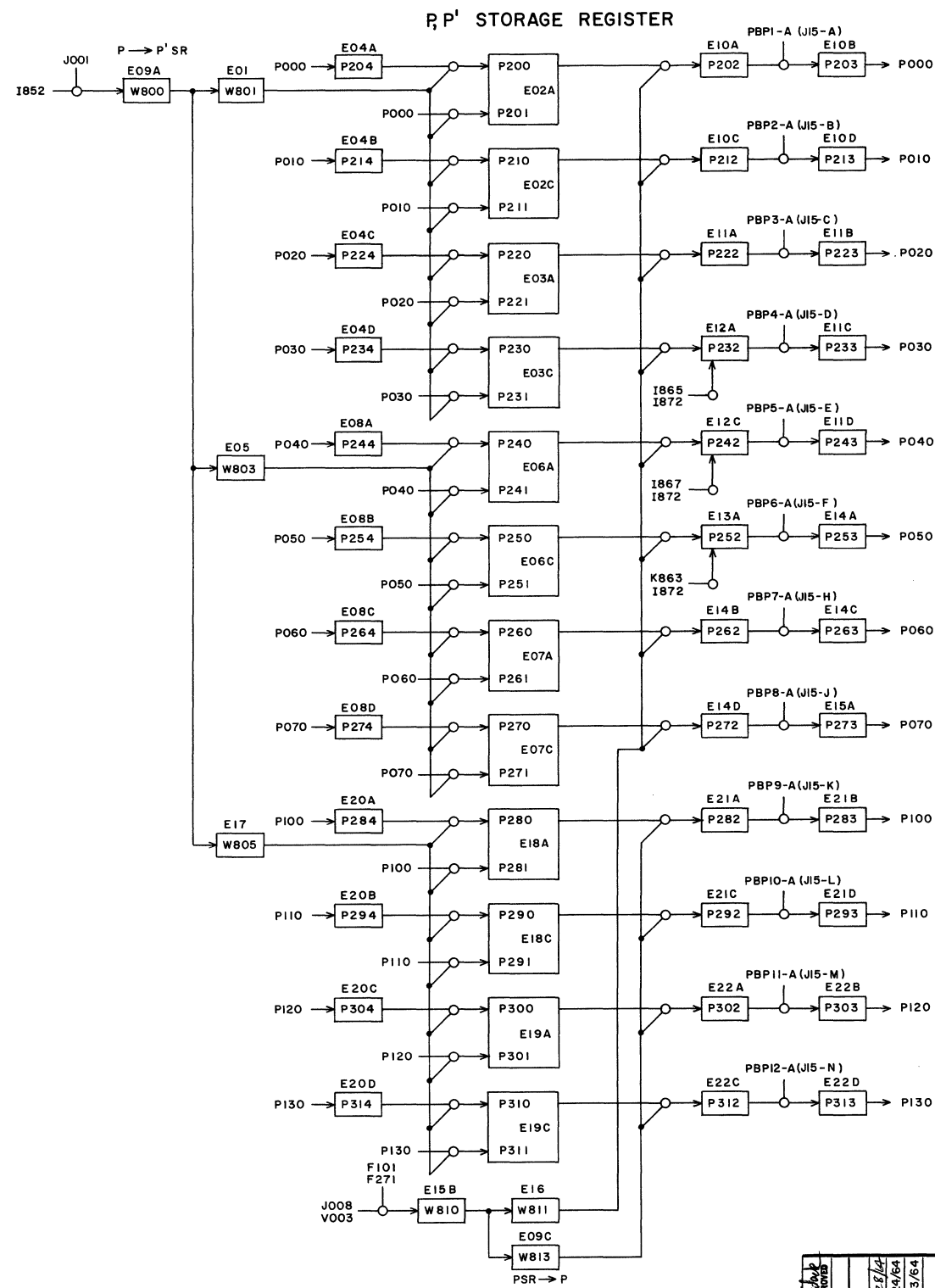


REVISIONS		REFERENCE DRAWINGS		COMPONENTS (UNLESS OTHERWISE INDICATED)		CONTROL DATA CORPORATION	
REV.	DATE	BY	CHK.	TOLERANCE	VALUE	SIZE	I D P DIVISION
B	1/5/65	KH	SS				PROJECT OR PRODUCT
A	1/4/64	J.H. NIPP	2/24/64				8092 TELEPROGRAMMER
		N. K. BECK	2/7/64				DRAWING NUMBER
							364158
							REV
							B
							SHEET
							PAGE
							9

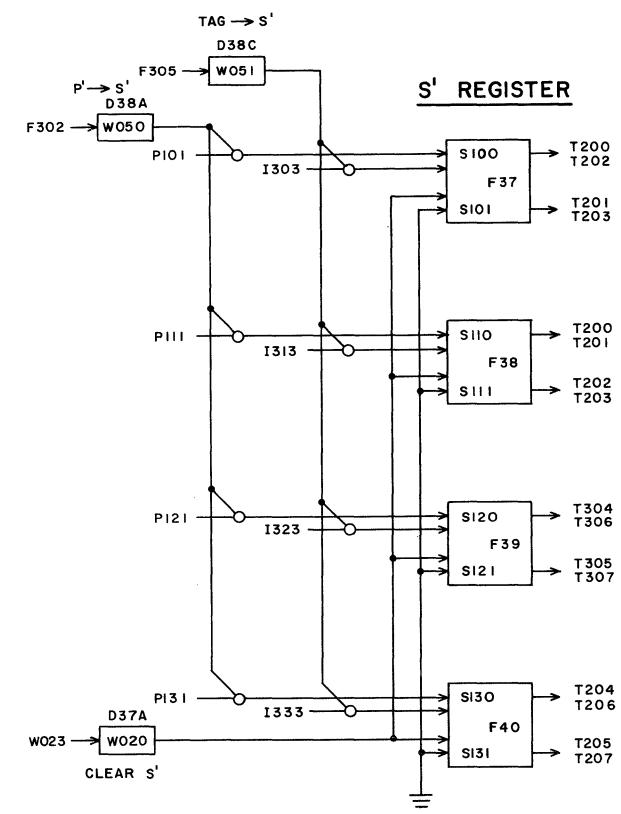
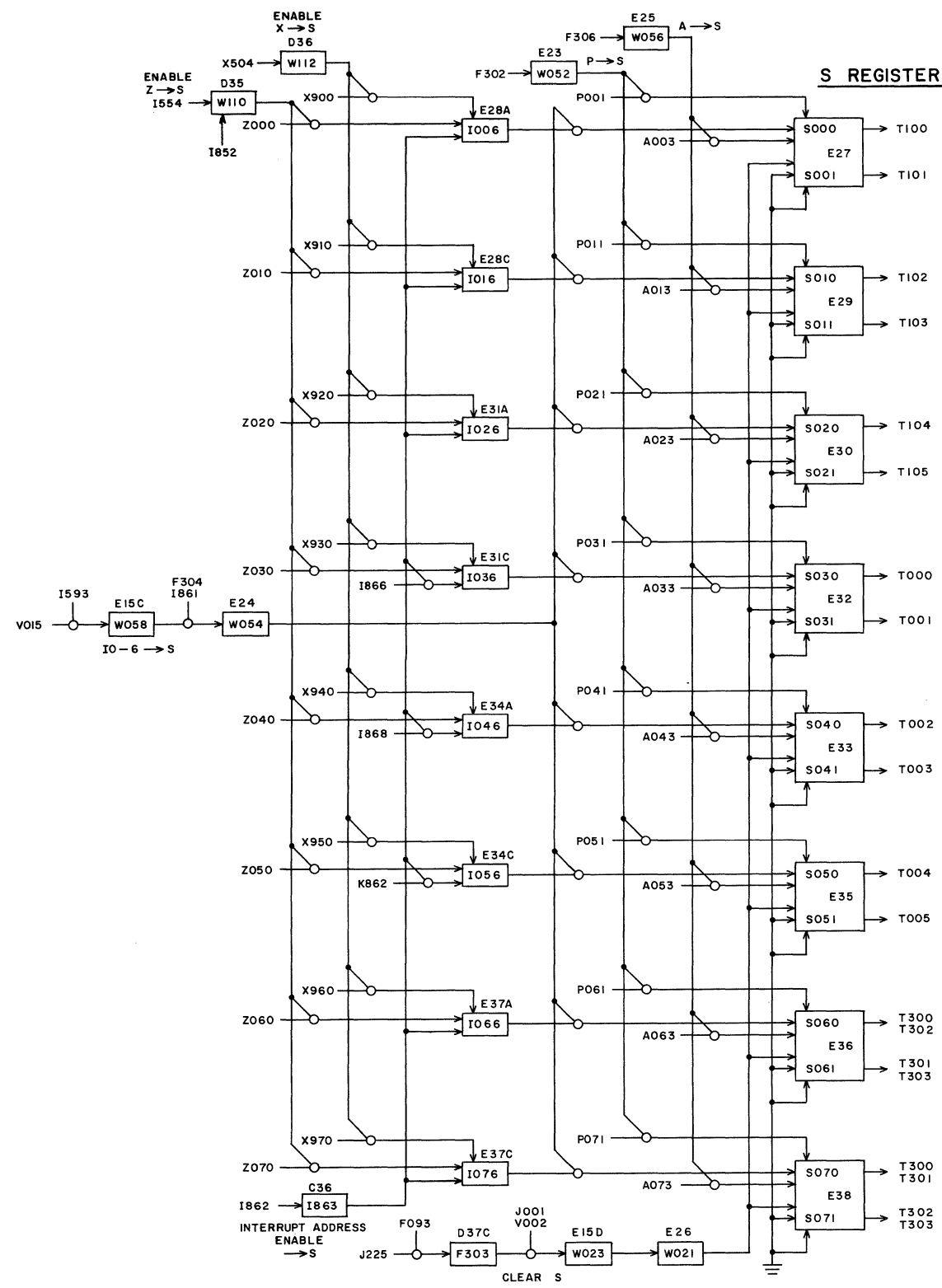
**LOGIC DIAGRAM  
REGISTER-Z**




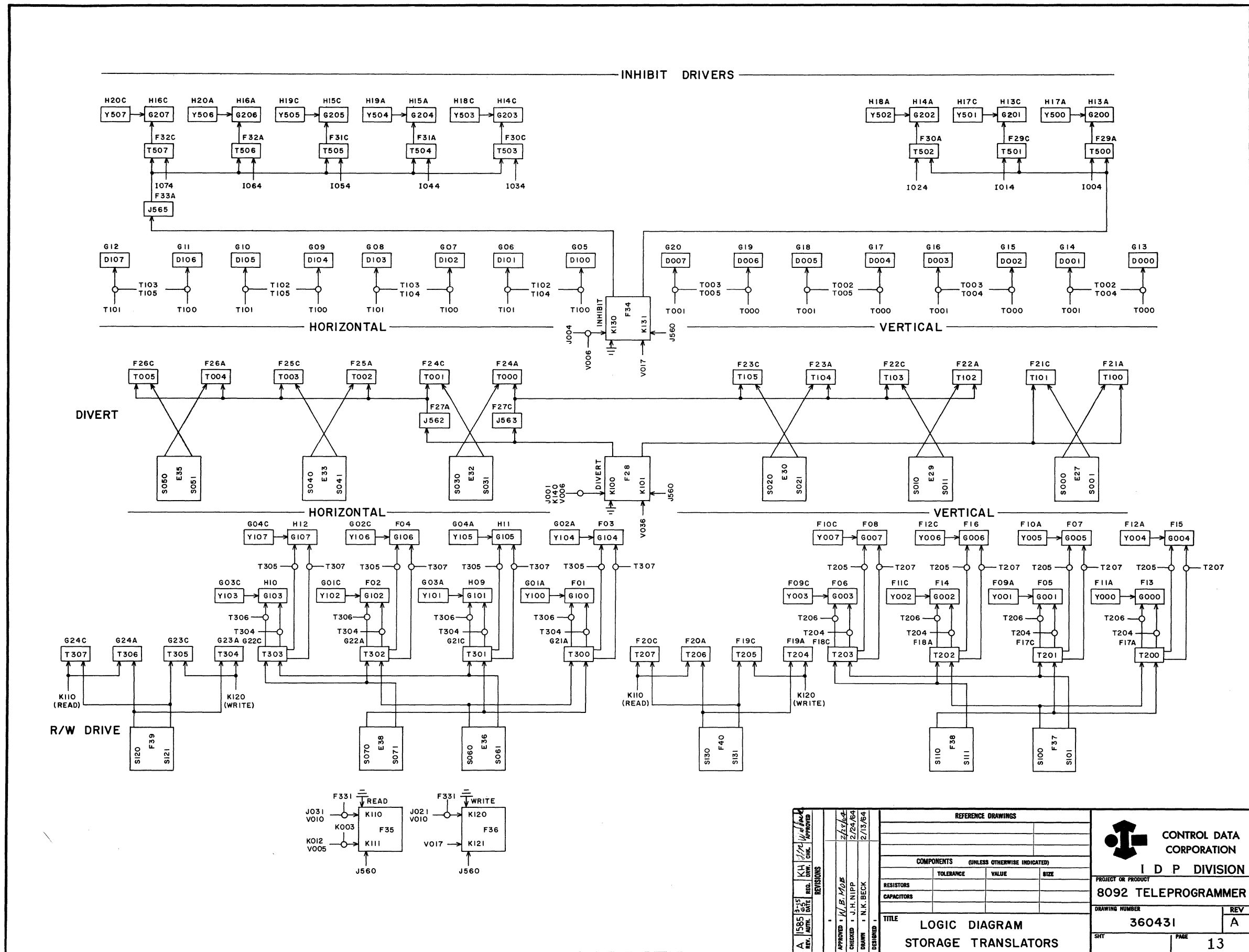
REVISIONS			REFERENCE DRAWINGS			CONTROL DATA CORPORATION	
APPROVED	W.B.M.A.E.	2/28/64				I D P DIVISION	
CHECKED	J.H.N.I.P.P.	2/24/64					
DRAWN	N.K.BECK	2/4/64				PROJECT OR PRODUCT	
DESIGNED			COMPONENTS (UNLESS OTHERWISE INDICATED)			8092 TELEPROGRAMMER	
			RESISTORS	TOLERANCE	VALUE	SIZE	DRAWING NUMBER
			CAPACITORS				360430
			TITLE			REV	
			LOGIC DIAGRAM			A	
			REGISTERS - P AND P'			PAGE	
						10	



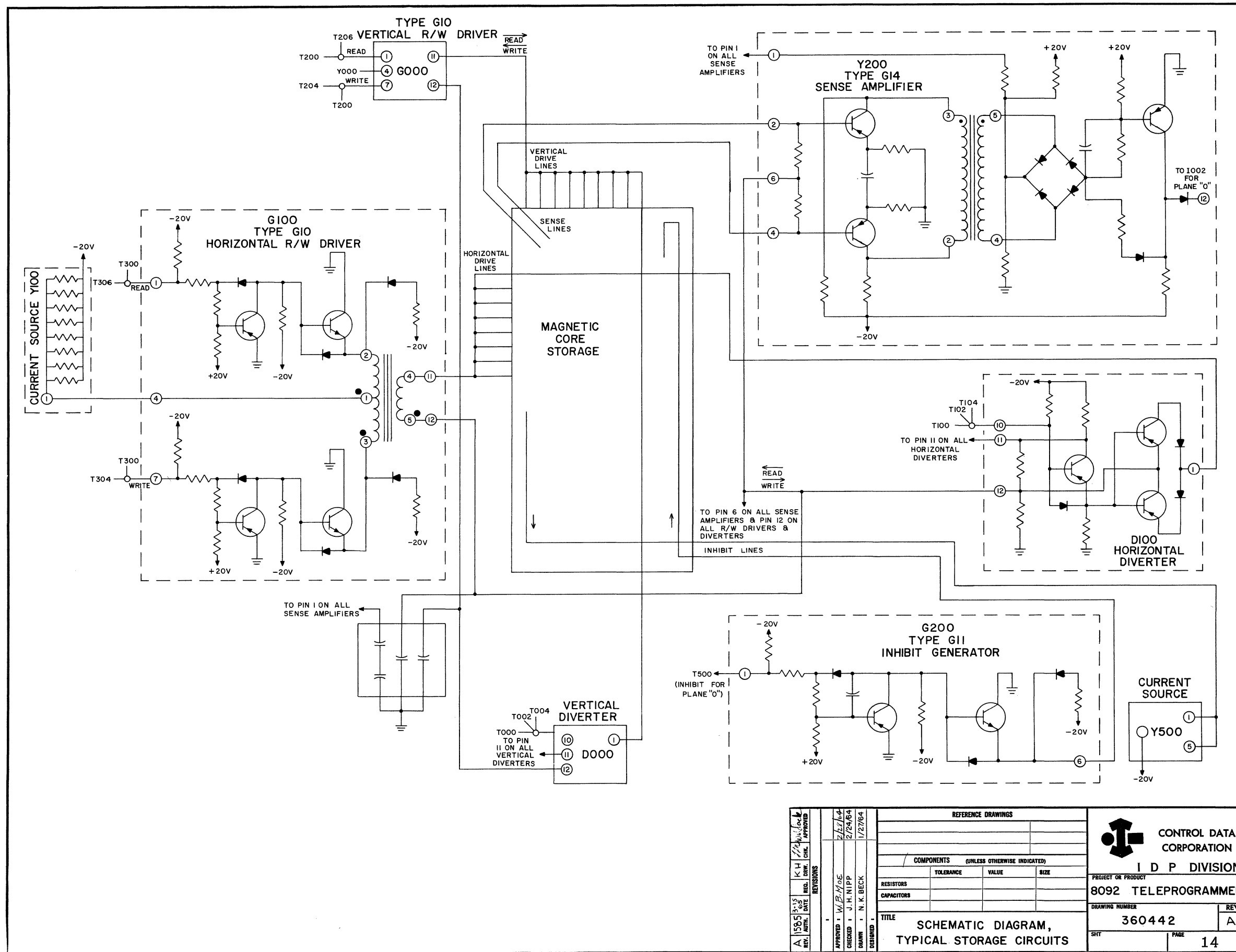
APPROVED: <i>[Signature]</i> CHECKED: J.F. NIPP DRAWN: N.K. BECK DATE: 2/13/64	REFERENCE DRAWINGS _____ _____ _____	CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT <b>8092 TELEPROGRAMMER</b>	COMPONENTS (UNLESS OTHERWISE INDICATED) <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th>TOLERANCE</th> <th>VALUE</th> <th>SIZE</th> </tr> </thead> <tbody> <tr> <td>RESISTORS</td> <td></td> <td></td> <td></td> </tr> <tr> <td>CAPACITORS</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>		TOLERANCE	VALUE	SIZE	RESISTORS				CAPACITORS				DRAWING NUMBER <b>364159</b> REV <b>A</b>
	TOLERANCE	VALUE	SIZE													
RESISTORS																
CAPACITORS																
TITLE <b>LOGIC DIAGRAM REGISTER - PSR</b>		SHEET <b>11</b>														



APPROVED: <i>[Signature]</i> CHECKED: J. H. NIPP DRAWN: N. K. BECK DESIGNED:		REFERENCE DRAWINGS _____ _____ _____ _____		 CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT <b>8092 TELEPROGRAMMER</b>											
REVISIONS 1. 1/28/64 2. 2/24/64 3. 2/5/64		COMPONENTS (UNLESS OTHERWISE INDICATED) <table border="1"> <thead> <tr> <th></th> <th>TOLERANCE</th> <th>VALUE</th> <th>SIZE</th> </tr> </thead> <tbody> <tr> <td>RESISTORS</td> <td></td> <td></td> <td></td> </tr> <tr> <td>CAPACITORS</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>				TOLERANCE	VALUE	SIZE	RESISTORS				CAPACITORS		
	TOLERANCE	VALUE	SIZE												
RESISTORS															
CAPACITORS															
TITLE <b>LOGIC DIAGRAM          REGISTERS - S AND S'</b>		DRAWING NUMBER <b>364160</b>		REV <b>A</b>											
SHEET <b>12</b>		PAGE <b>12</b>													



REVISIONS 1. 1/15/64 2. 2/10/64 3. 2/13/64	REFERENCE DRAWINGS	
	COMPONENTS (UNLESS OTHERWISE INDICATED)	
	TOLERANCE	VALUE
	RESISTORS	SIZE
CAPACITORS		
TITLE		
LOGIC DIAGRAM		
STORAGE TRANSLATORS		
CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER		
DRAWING NUMBER		REV
360431		A
PAGE		13



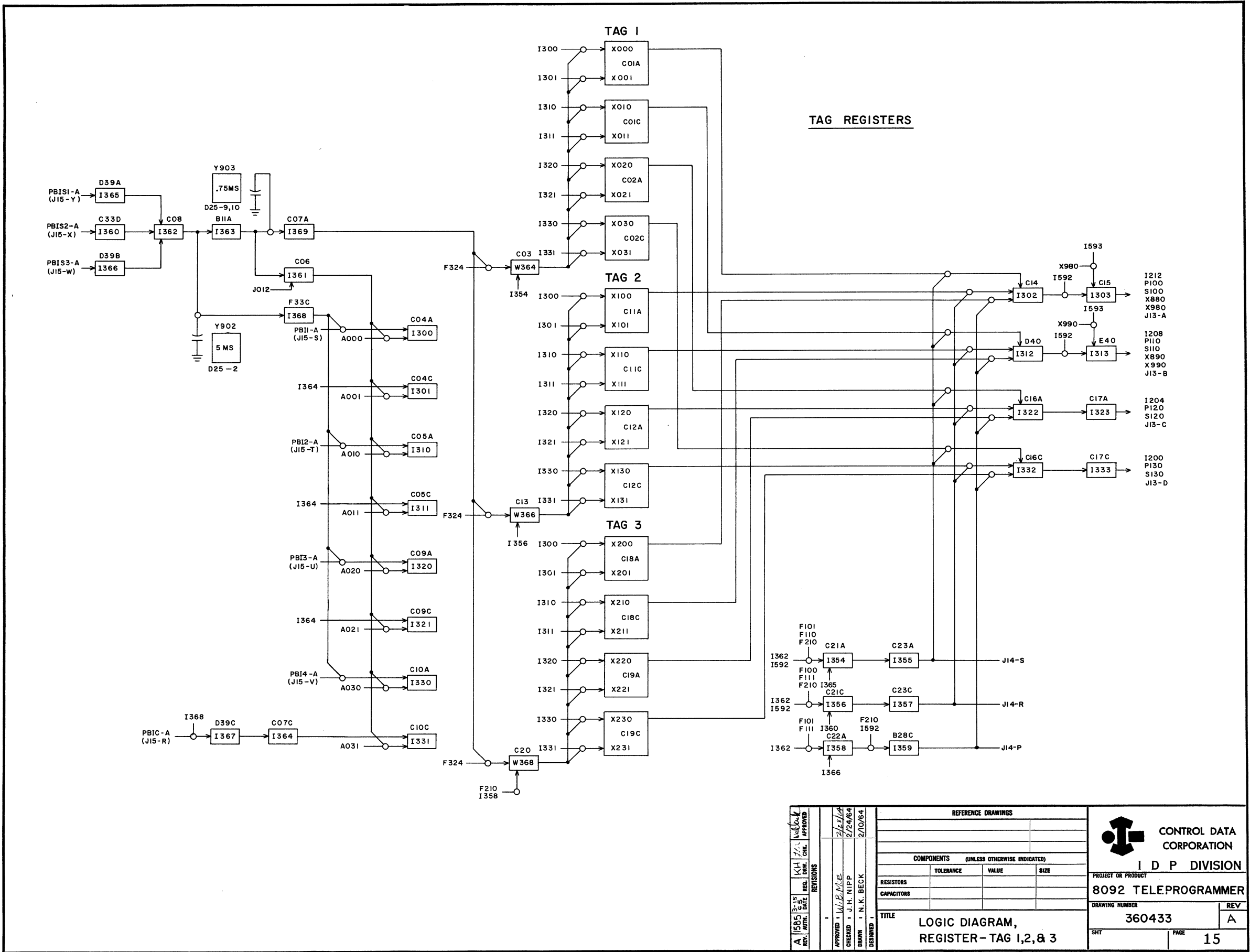
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APPROVED	W.B. MOE	CHECKED	J.H. NIPP	DRAWN	N.K. BECK	DESIGNED			

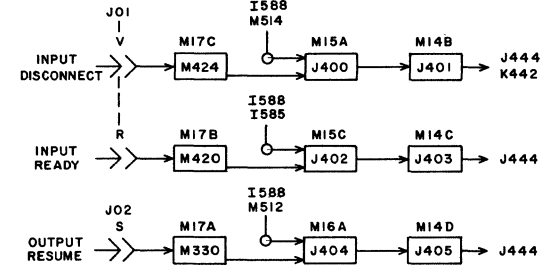
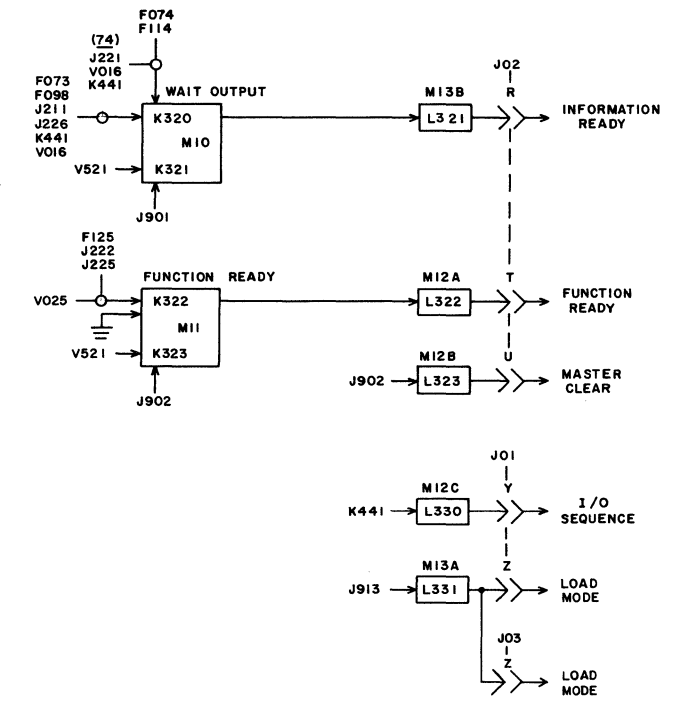
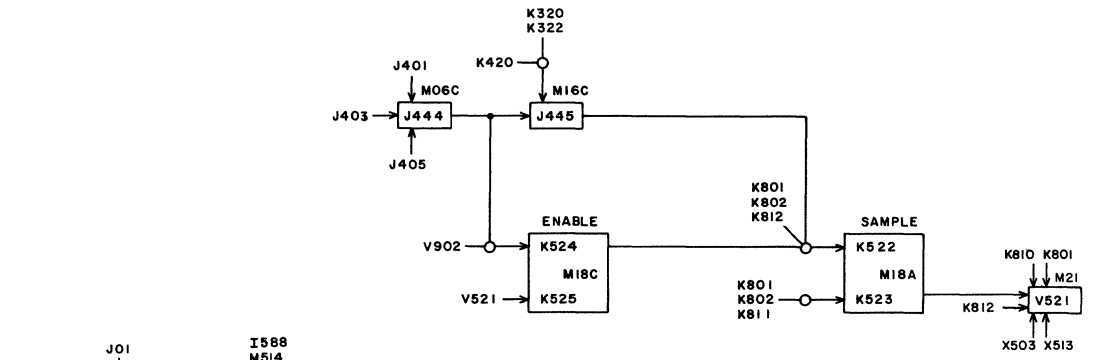
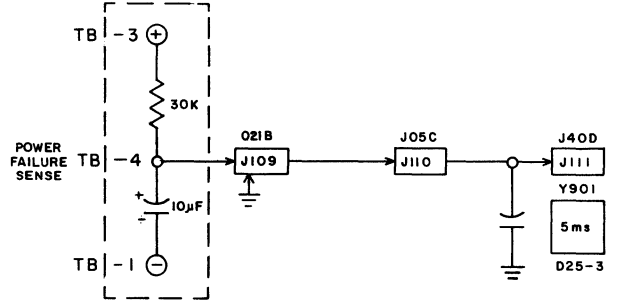
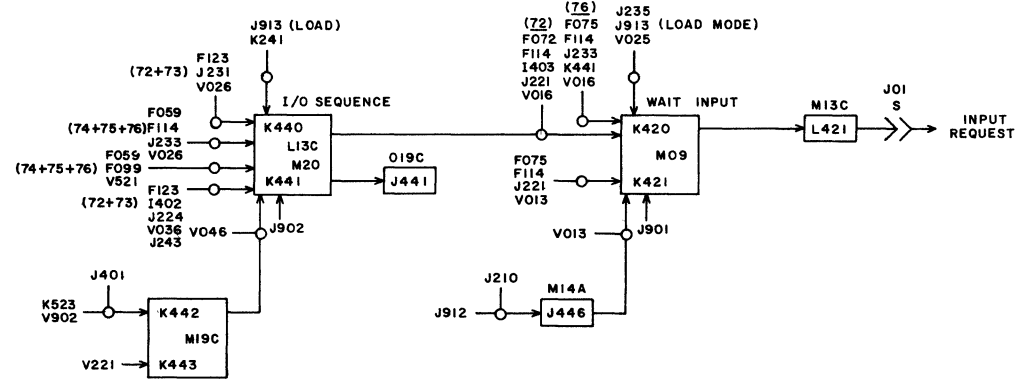
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COMPONENTS (UNLESS OTHERWISE INDICATED)		
TOLERANCE	VALUE	SIZE
RESISTORS		
CAPACITORS		
TITLE		
SCHEMATIC DIAGRAM, TYPICAL STORAGE CIRCUITS		

CONTROL DATA CORPORATION I D P DIVISION		PROJECT OR PRODUCT
		8092 TELEPROGRAMMER
DRAWING NUMBER	REV	
360442	A	
SHEET	PAGE	
14	14	





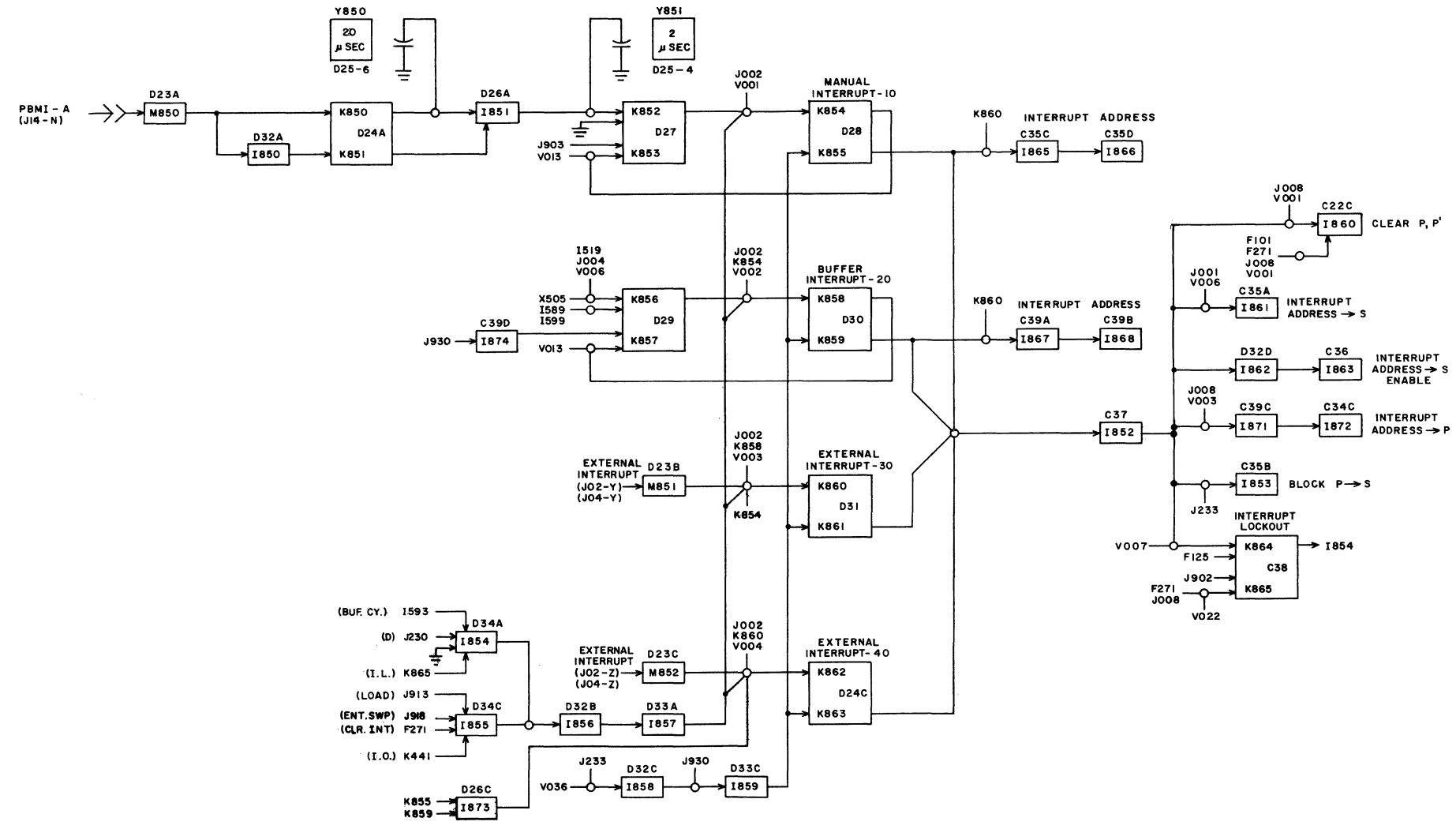


REV.	DATE	BY	CHK.	APPROVED
D	2/21/64	W. B. Mc...		
C	1/28/64	K...		
B	1/11/64	...		
A	1/8/64	...		

REV.	DATE	BY	CHK.	APPROVED
APPROVED	1/28/64	W. B. Mc...		
CHECKED	1/28/64	J. H. NIPP		
DRAWN	1/28/64	N. K. BECK		
DESIGNED	1/28/64			


REFERENCE DRAWINGS		
COMPONENTS (UNLESS OTHERWISE INDICATED)		
RESISTORS	TOLEANCE	VALUE
CAPACITORS	TOLEANCE	VALUE
TITLE		
LOGIC DIAGRAM, INPUT/OUTPUT CONTROL		

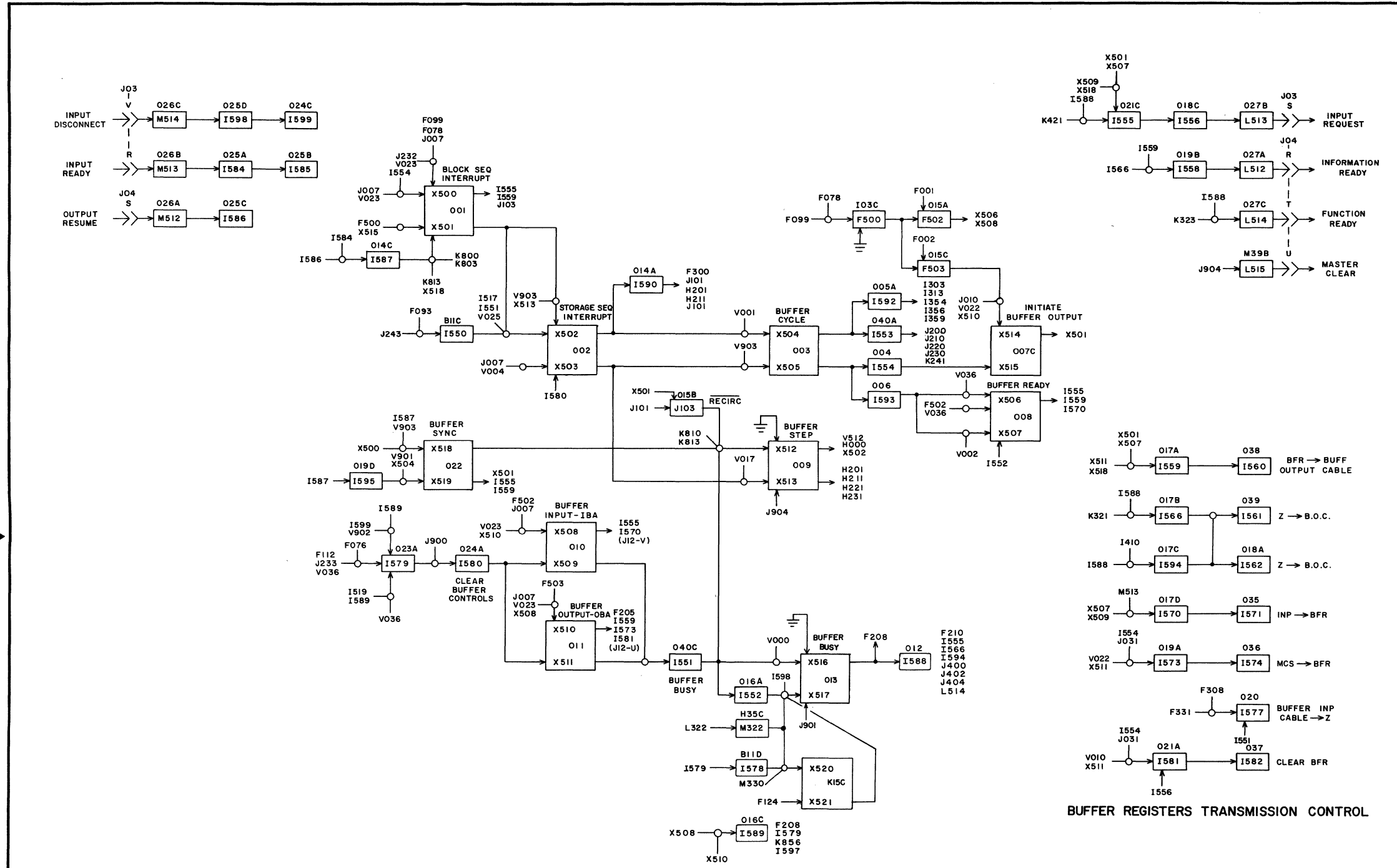
**CONTROL DATA CORPORATION**  
**I D P DIVISION**  
 PROJECT OR PRODUCT  
**8092 TELEPROGRAMMER**  
 DRAWING NUMBER  
**360425**  
 SHEET 2 OF 2 PAGE 16



REV	DATE	BY	CHKD	APP'D	REVISIONS
E	12/28/64	W.B.M.	W.B.M.	W.B.M.	
D	12/24/64	W.B.M.	W.B.M.	W.B.M.	
C	12/17/64	W.B.M.	W.B.M.	W.B.M.	
B	12/10/64	W.B.M.	W.B.M.	W.B.M.	
A	12/3/64	W.B.M.	W.B.M.	W.B.M.	

REFERENCE DRAWINGS		
COMPONENTS (UNLESS OTHERWISE INDICATED)		
RESISTORS	TOLERANCE	VALUE
CAPACITORS	TOLERANCE	VALUE
TITLE		
LOGIC DIAGRAM INTERRUPT		


**CONTROL DATA CORPORATION**  
**I D P DIVISION**  
 PROJECT OR PRODUCT  
**8092 TELEPROGRAMMER**  
 DRAWING NUMBER  
**360434**  
 REV  
**E**  
 SHEET  
**17**



BUFFER REGISTERS TRANSMISSION CONTROL

REV. NO.		DATE	BY	CHK.	APPROVED
1	1	2/24/64	J.H. NIPP		
2	1	2/24/64	N.K. BECK		
3	1	2/24/64			
4	1	2/24/64			
5	1	2/24/64			
6	1	2/24/64			
7	1	2/24/64			
8	1	2/24/64			
9	1	2/24/64			
10	1	2/24/64			

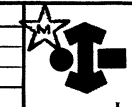
REFERENCE DRAWINGS	

COMPONENTS (UNLESS OTHERWISE INDICATED)		
TOLERANCE	VALUE	SIZE
RESISTORS		
CAPACITORS		

<b>TITLE</b> LOGIC DIAGRAM BUFFER CONTROLS	<b>CONTROL DATA CORPORATION</b> I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 36044700 REV H
--	--

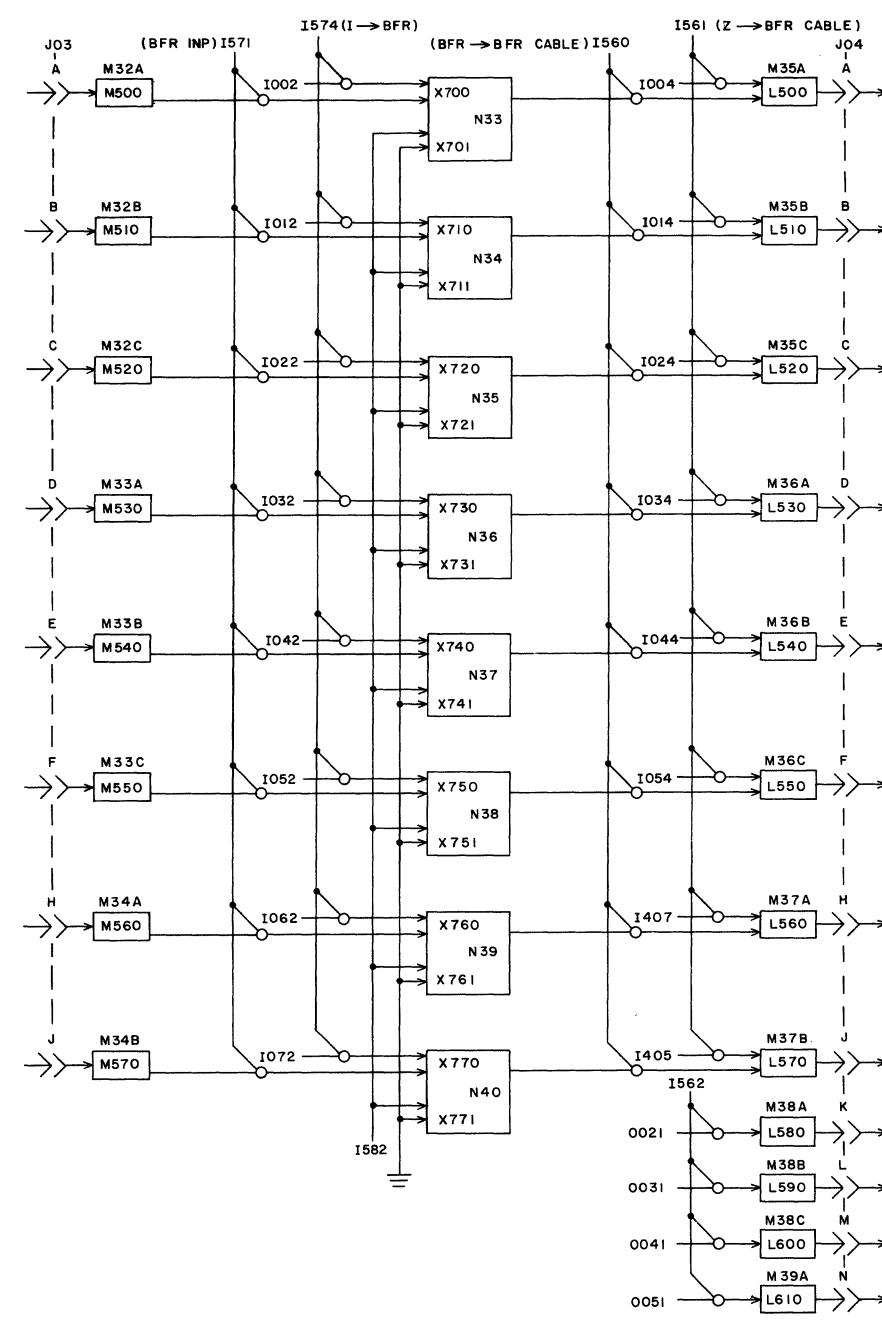


CONTROL DATA CORPORATION  
I D P DIVISION

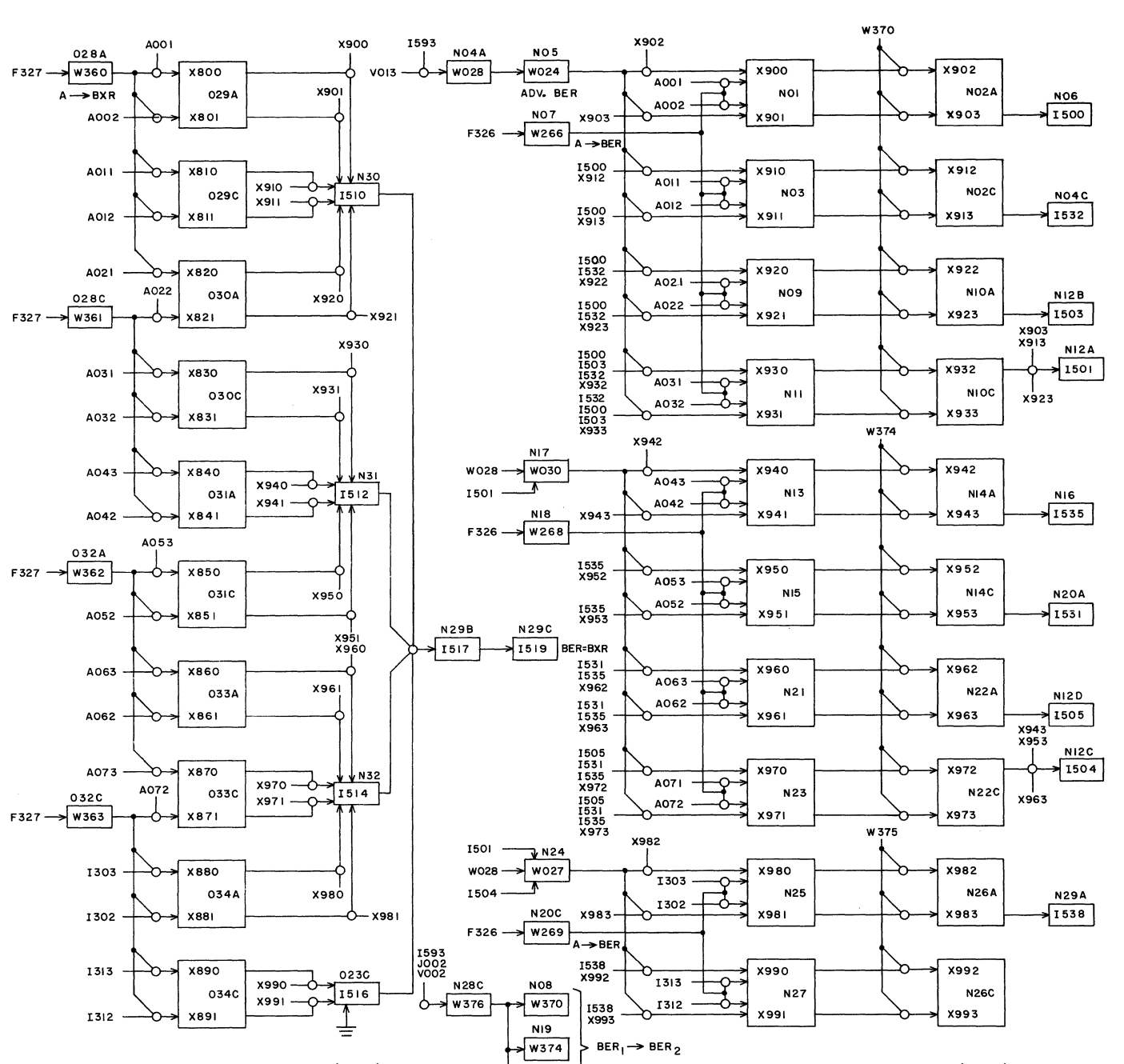
PROJECT OR PRODUCT  
8092 TELEPROGRAMMER

DRAWING NUMBER  
36044700

REV  
H



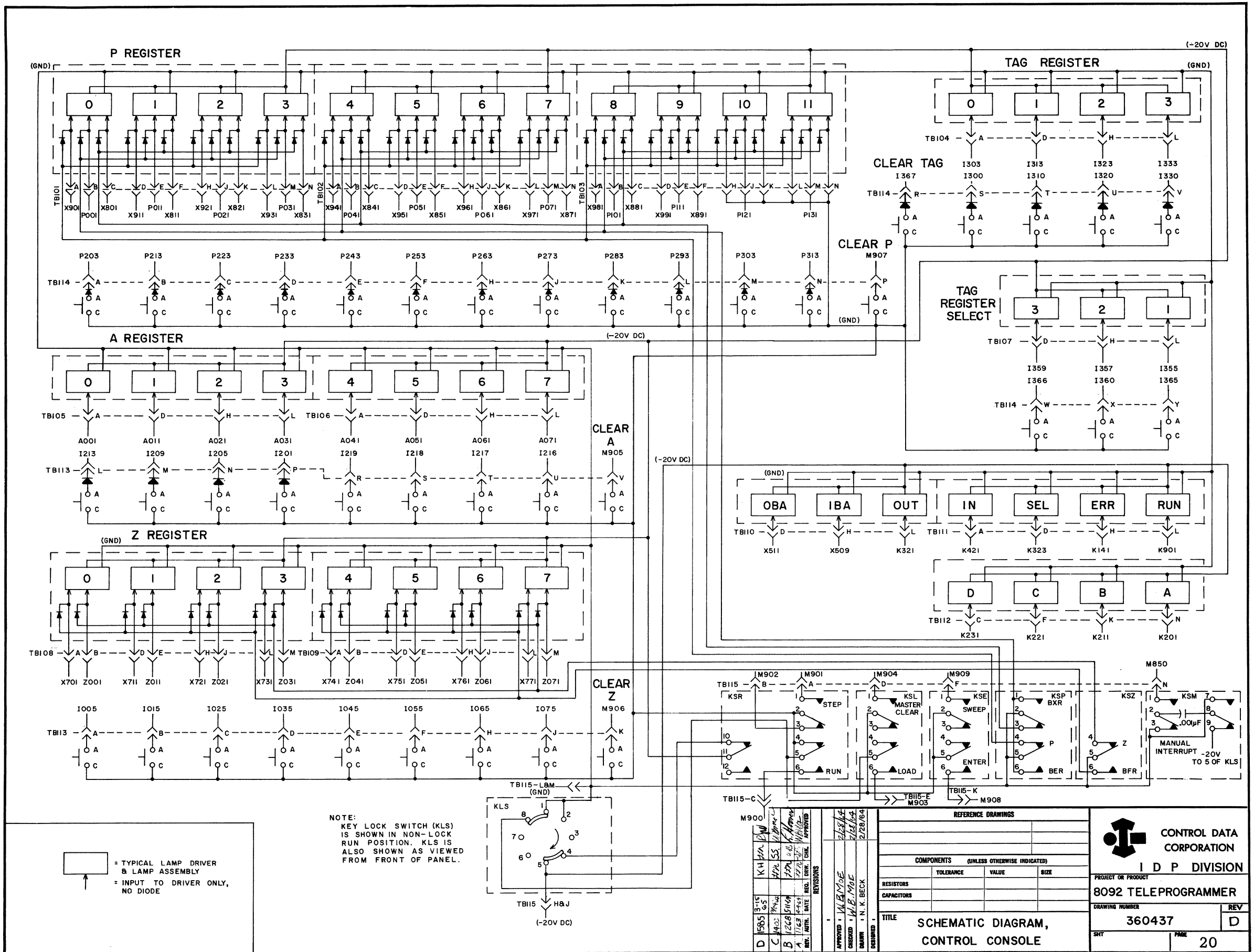
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



**BUFFER EXIT REGISTER (BXR)**

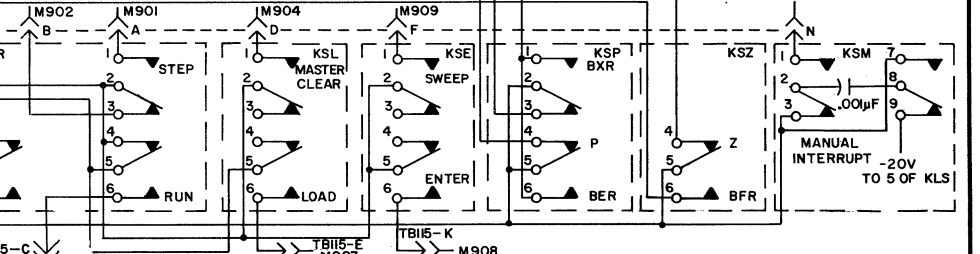
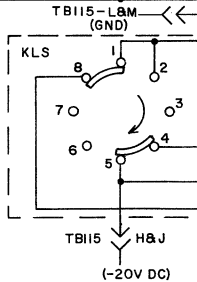
**BUFFER ENTRANCE REGISTER (BER)**

REFERENCE DRAWINGS _____ _____ _____ _____		<b>CONTROL DATA CORPORATION</b> I D P DIVISION PROJECT OR PRODUCT <b>8092 TELEPROGRAMMER</b>											
COMPONENTS (UNLESS OTHERWISE INDICATED) <table border="1"> <thead> <tr> <th></th> <th>TOLERANCE</th> <th>VALUE</th> <th>SIZE</th> </tr> </thead> <tbody> <tr> <td>RESISTORS</td> <td></td> <td></td> <td></td> </tr> <tr> <td>CAPACITORS</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>				TOLERANCE	VALUE	SIZE	RESISTORS				CAPACITORS		
	TOLERANCE	VALUE	SIZE										
RESISTORS													
CAPACITORS													
TITLE <b>LOGIC DIAGRAM          REGISTERS-BFR, BXR, BER</b>		DRAWING NUMBER <b>360432</b>											
DESIGNED _____ _____ _____		REV <b>A</b>											
APPROVED _____ _____ _____		PAGE <b>19</b>											




 = TYPICAL LAMP DRIVER & LAMP ASSEMBLY  
 = INPUT TO DRIVER ONLY, NO DIODE

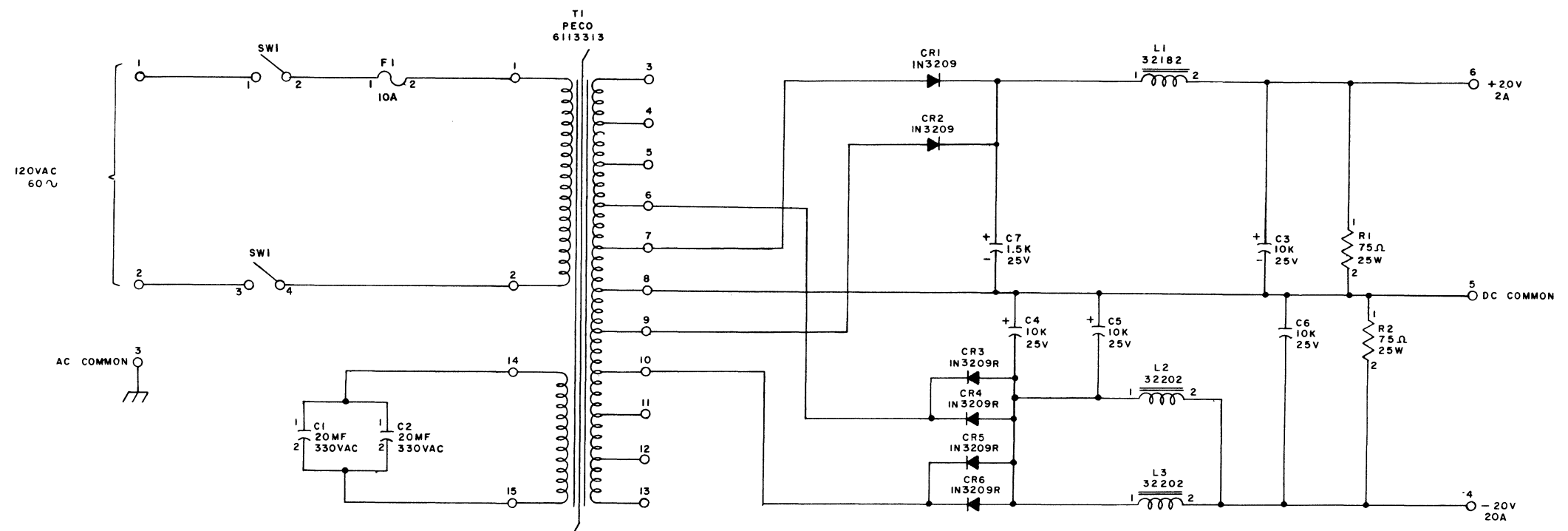
NOTE:  
 KEY LOCK SWITCH (KLS)  
 IS SHOWN IN NON-LOCK  
 RUN POSITION. KLS IS  
 ALSO SHOWN AS VIEWED  
 FROM FRONT OF PANEL.




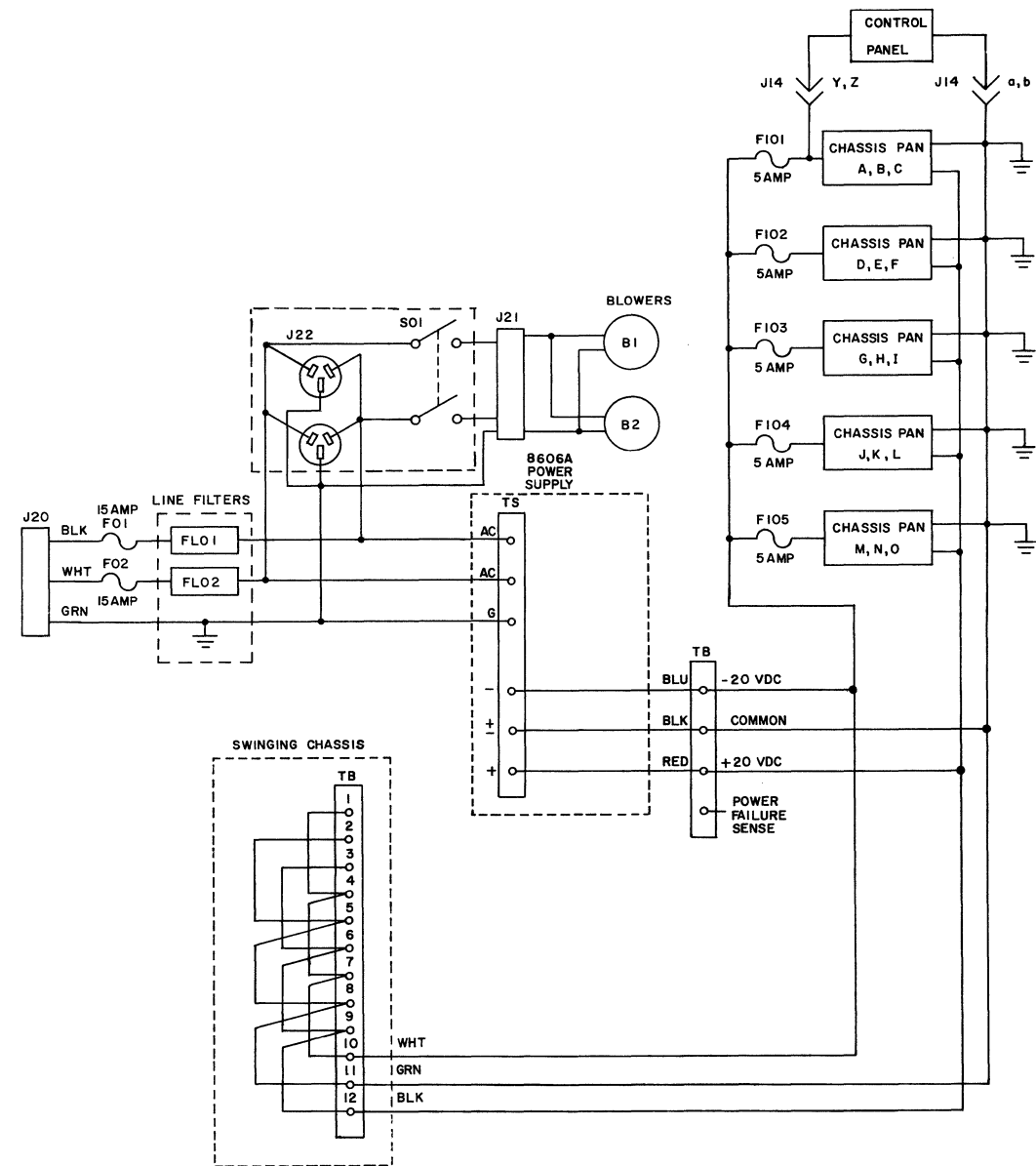
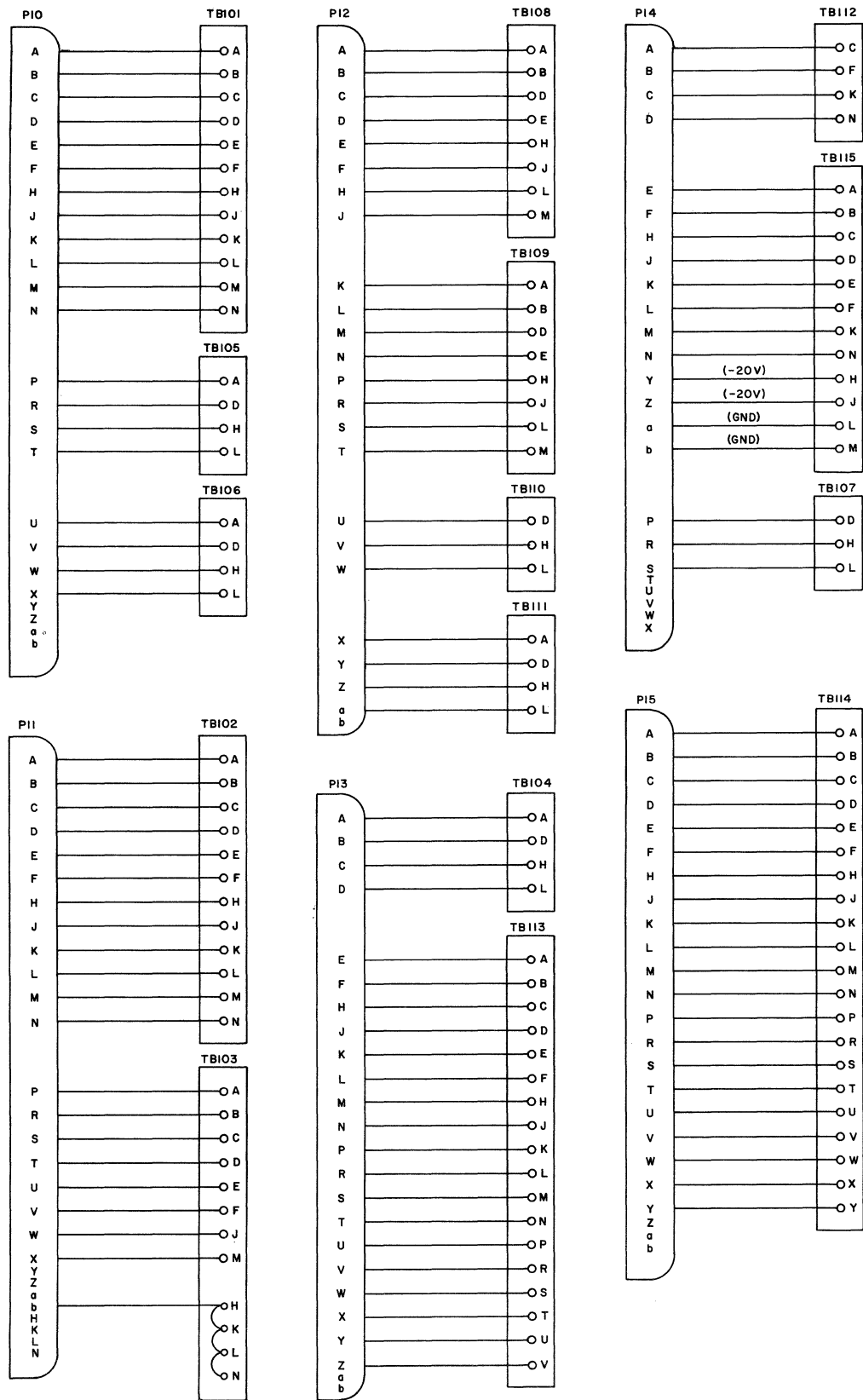
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C	1/28/64	K.H.	J.S.	N.K.	REVISED
B	1/28/64	K.H.	J.S.	N.K.	REVISED
A	1/28/64	K.H.	J.S.	N.K.	REVISED

REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			
TITLE SCHEMATIC DIAGRAM, CONTROL CONSOLE			

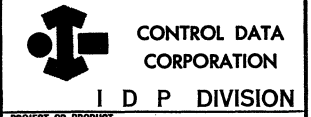
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 I D P DIVISION  
 PROJECT OR PRODUCT  
**8092 TELEPROGRAMMER**  
 DRAWING NUMBER  
**360437**  
 REV  
**D**  
 SHEET  
 PAGE  
**20**



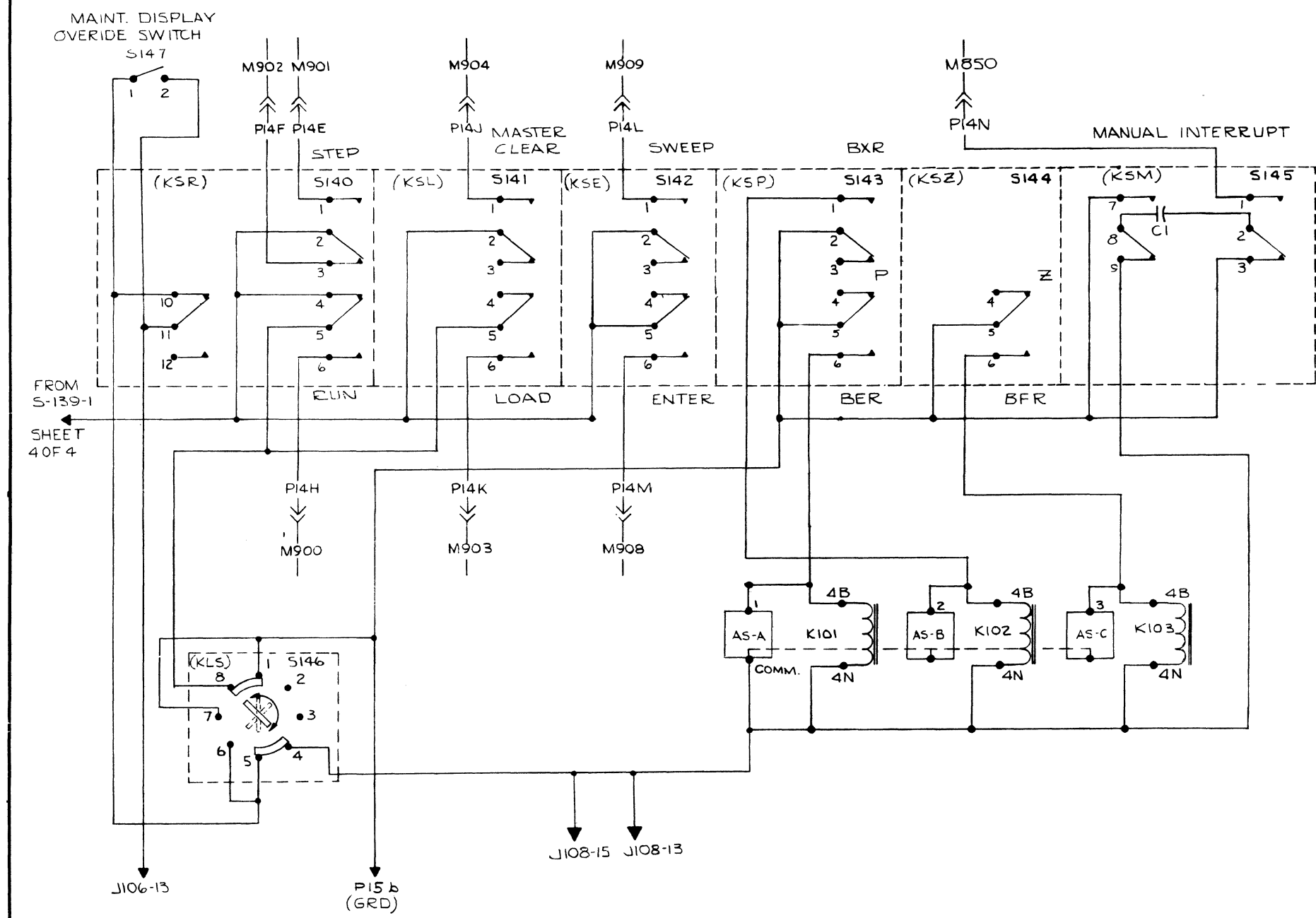
REF. DATE	REV. DATE	CHK. APPROVED	REFERENCE DRAWINGS	 <b>CONTROL DATA CORPORATION</b> <b>I D P DIVISION</b>											
			COMMENTS												
			COMMENTS (UNLESS OTHERWISE INDICATED)												
			<table border="1"> <thead> <tr> <th></th> <th>TOLERANCE</th> <th>VALUE</th> <th>SIZE</th> </tr> </thead> <tbody> <tr> <td>RESISTORS</td> <td></td> <td></td> <td></td> </tr> <tr> <td>CAPACITORS</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>			TOLERANCE	VALUE	SIZE	RESISTORS				CAPACITORS		
	TOLERANCE	VALUE	SIZE												
RESISTORS															
CAPACITORS															
APPROVED			TITLE	DRAWING NUMBER											
CHECKED			<b>SCHEMATIC, POWER SUPPLY-</b>	<b>364071</b>											
DESIGNED			<b>MODEL 8606-A</b>	REV											
				PAGE											
				<b>21</b>											



1985 REV. AUTH. DATE A 1/1/85	KH REC. DATE 1/1/85	APPROVED 1/1/85	CHECKED 1/1/85	DRAWN N. K. BECK	DATE 3/4/64	
		REVISIONS				
		REFERENCE DRAWINGS				
		COMPONENTS (UNLESS OTHERWISE INDICATED)				
RESISTORS		TOLERANCE	VALUE	SIZE		
CAPACITORS						
TITLE <b>CABLING &amp; AC-DC DIST</b>						
PROJECT OR PRODUCT <b>8092 TELEPROGRAMMER</b>				DRAWING NUMBER <b>360441</b>	REV <b>A</b>	
SHEET <b>22</b>				PAGE <b>22</b>		



REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.
A			RELEASED		11-10-64		WAV
B	8230		REVISED PER ECO	RAH	4-5-65		FES



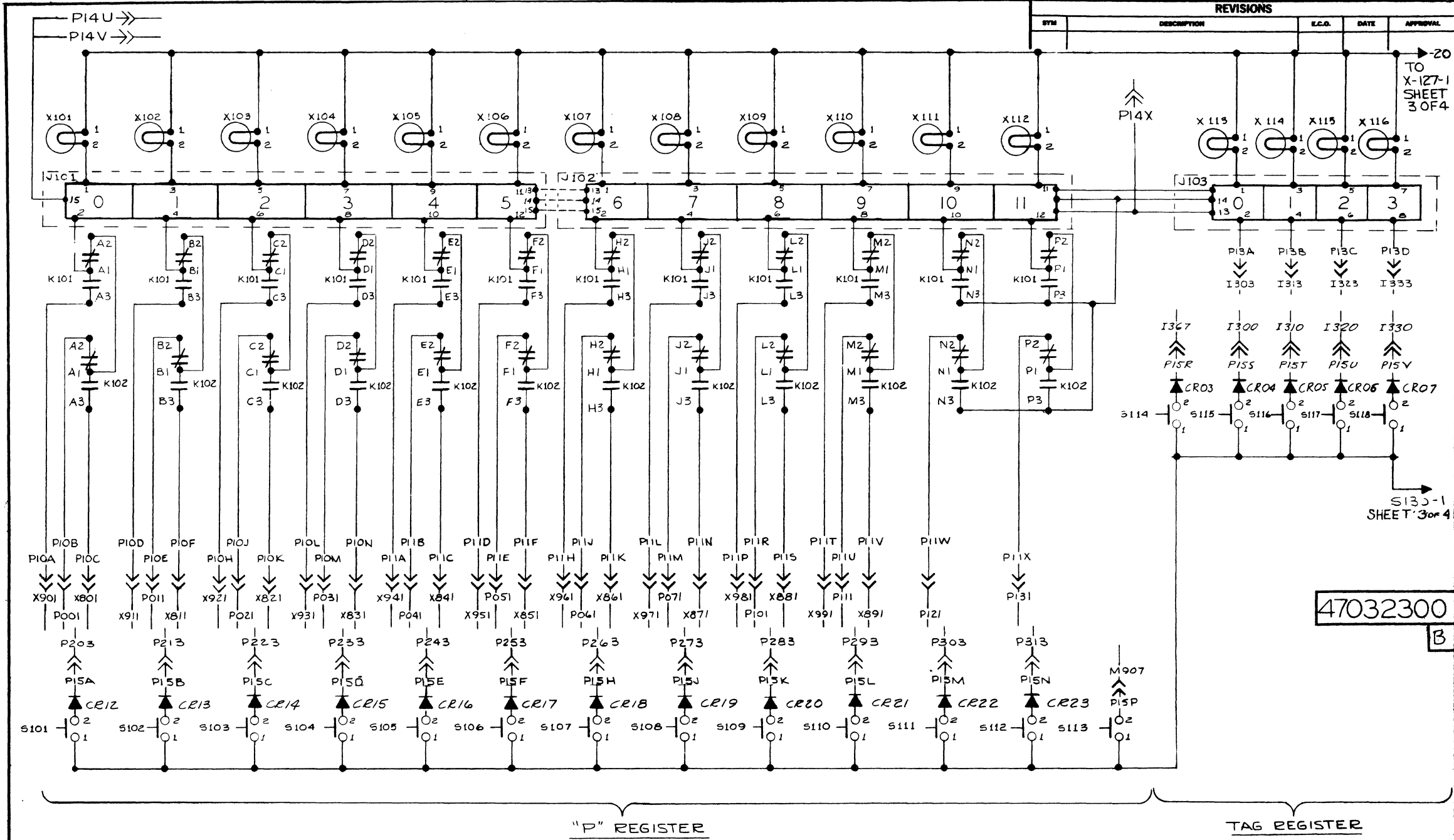
2. DOTTED LINES SHOW CONNECTIONS WITHIN A CONNECTOR OR COMPONENT.

1. KEY LOCK SWITCH KLS IS SHOWN IN NON-LOCK RUN POSITION. KLS IS ALSO SHOWN AS VIEWED FROM FRONT OF PANEL.

NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES:		CONTROL DATA		TITLE	
DO NOT SCALE DRAWING		CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MILWAUKEE, WISCONSIN		SCHEMATIC DIAGRAM 8092 DISPLAY	
MATERIAL	PRODUCT	DATE	SIZE	DRAWING NO.	REV
	8092 DISPLAY	11-13-64	C	47032300	B
FINISH	CHECKED	ENGINEER	APPROVED	SCALE	Page 23
					SUBSET 1 OF 4





SYM	DESCRIPTION	E.C.O.	DATE	APPROVAL

TO X-127-1  
SHEET 3 OF 4

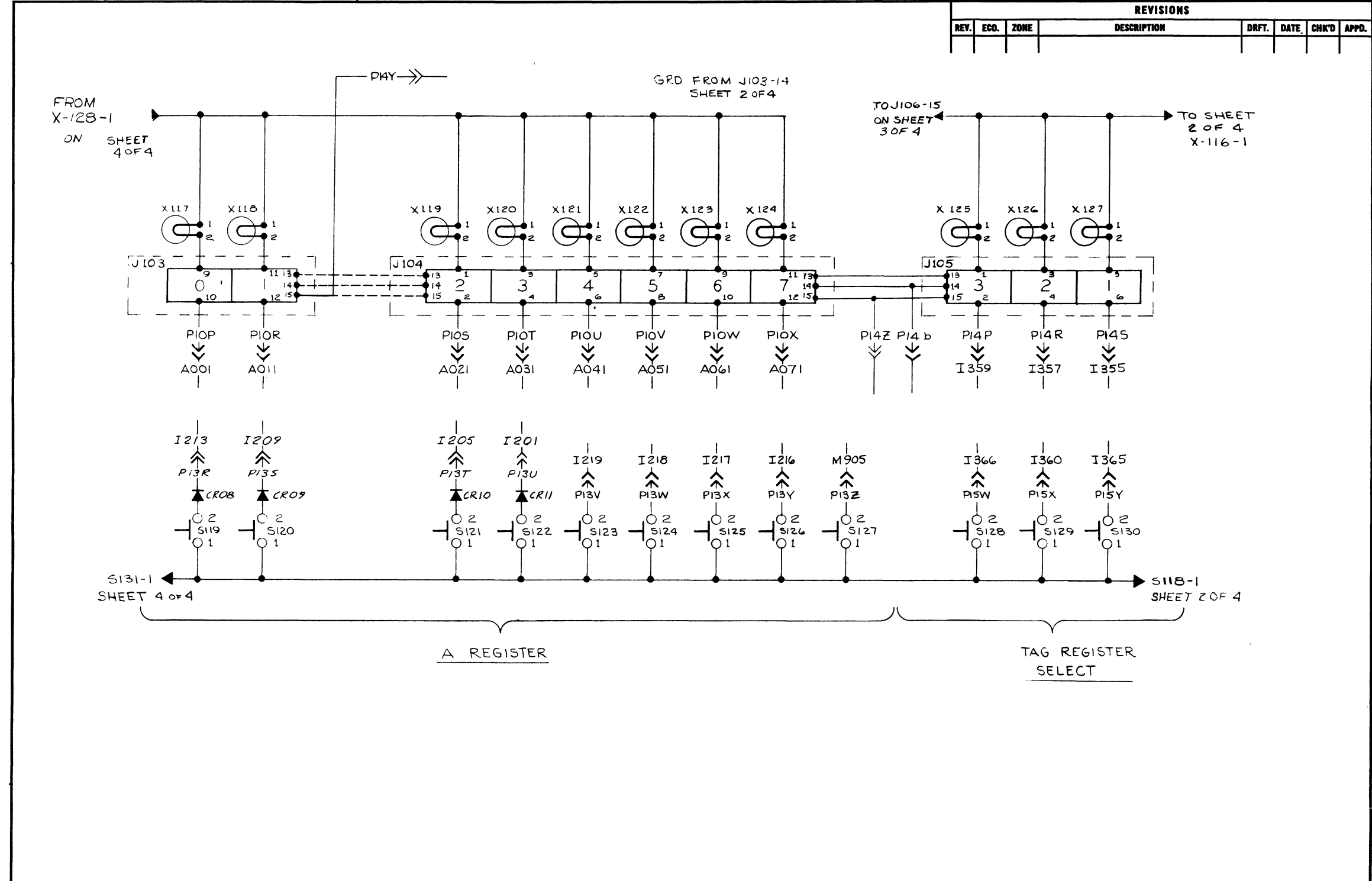
47032300  
B

"P" REGISTER

TAG REGISTER

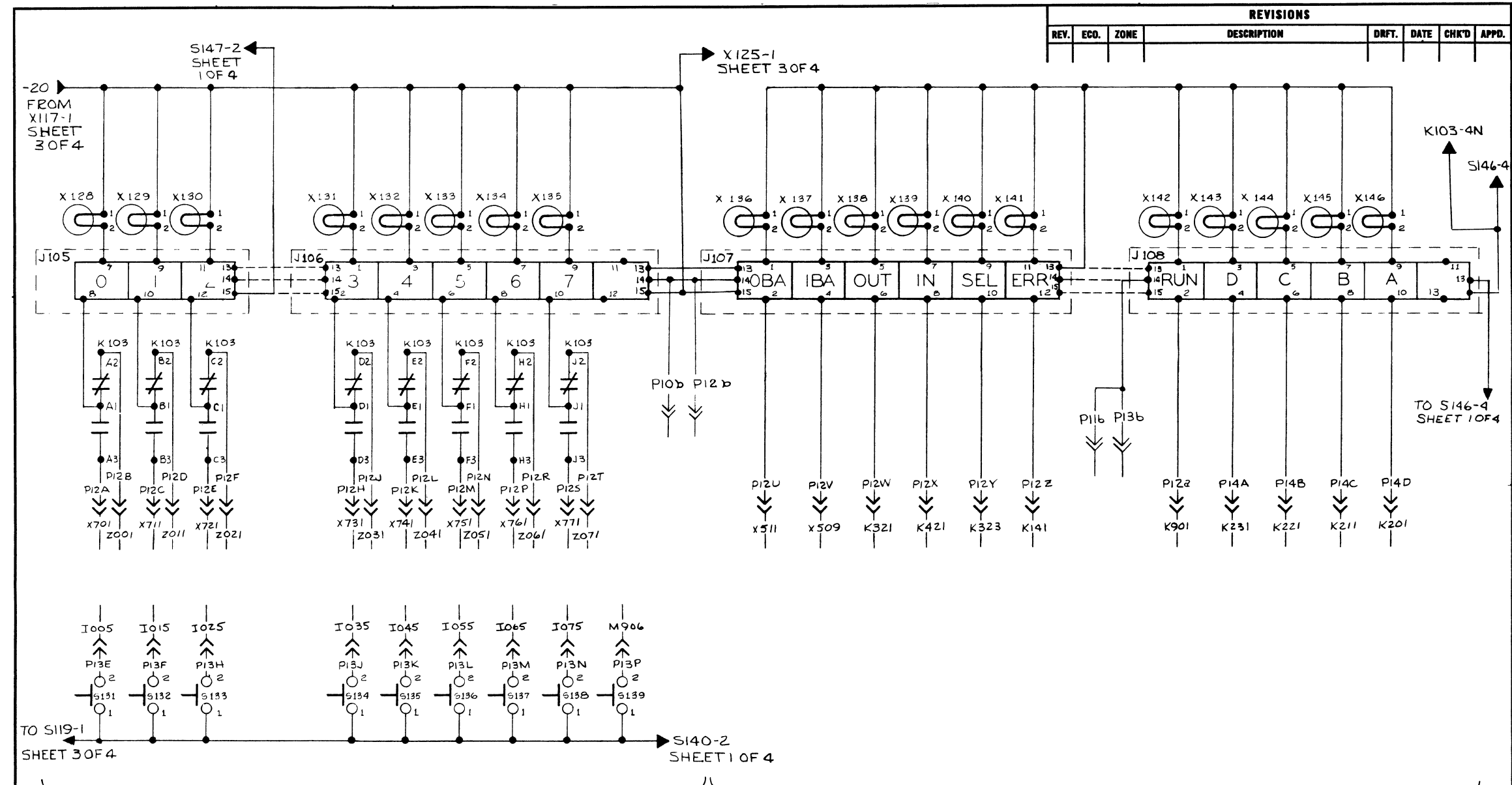
ITEM	REQD.	PART NO.	DESCRIPTION	MATL.	MATL. SPEC.	NEXT ASSY.	USED ON	QTY. RECD.
<b>LIST OF MATERIAL</b>								
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: FRACTIONS: ±1/64 DECIMALS: (0.00)±0.005 (0.01)±0.005 BREAK ALL EDGES AND SHARP CORNERS TO 1/16". DIMENSIONS APPLY AFTER PLATING OR HEAT TREAT. SHARPEN NO LOOSE CORNERS PERMITTED. TIGHT SPACES PERMITTED IF THEY CANNOT BE DETECTED BY NORMAL VISION OR TOUCH. SURFACE FINISH: ✓ ALL INSIDE SURFACES ✓ ALL OUTSIDE SURFACES			BY: _____ DATE: _____ NAME: _____		SCHEMATIC DIAGRAM 8092 DISPLAY		CONTROL DATA CORP CEDAR ENGINEERING DIVISION 5000 WEST 50TH ST. MINNEAPOLIS 16 MINNESOTA	
DRAWN: _____ CHECKED: _____ ENG. _____ PROD. _____ FURNISH: _____			Page 24					
							47032300	
							2 OF 4	

REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRAFT.	DATE	CHK'D	APPD.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: * * * DO NOT SCALE DRAWING	<b>CONTROL DATA</b> CORPORATION CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA	TITLE SCHEMATIC DIAGRAM 8092 DISPLAY	
		PRODUCT 8092 DISPLAY	DRAWING NO. 47032300
MATERIAL FINISH	DRAWN CHECKED ENGINEER APPROVED	SIZE C	REV B
SCALE		Page 25	SHEET 3 OF 4

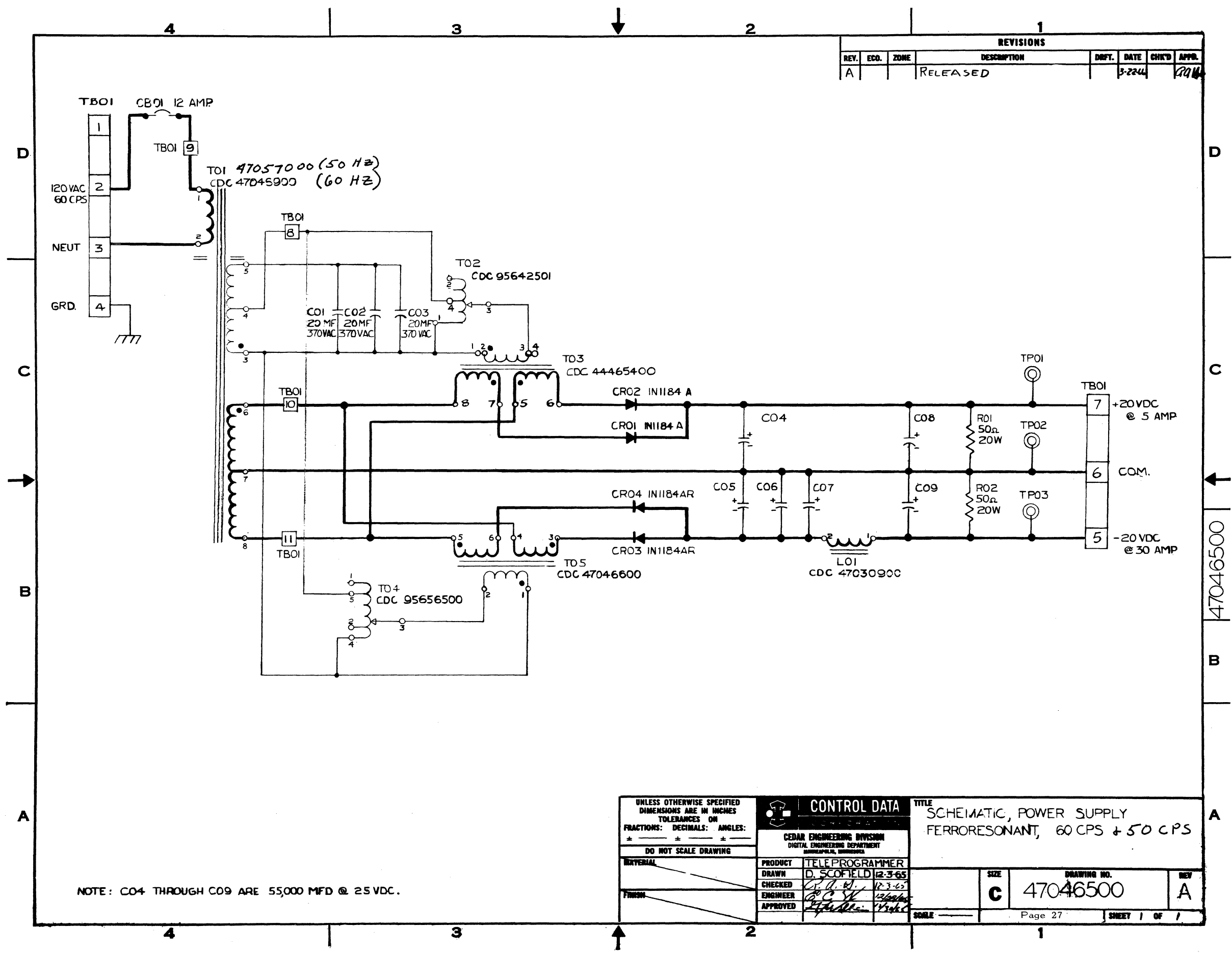
REVISIONS						
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D APPD.



'Z' REGISTER LEGENDS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: * * *	<b>CONTROL DATA</b> CORPORATION		TITLE SCHEMATIC DIAGRAM, 8092 DISPLAY	
	CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MUNICIPAL, MINNESOTA		PRODUCT 8092 DISPLAY	DRAWING NO. 47032300
DO NOT SCALE DRAWING	DRAWN	CHECKED	ENGINEER	APPROVED
SCALE	SIZE C	Page 26	SHEET 4 OF 4	REV B

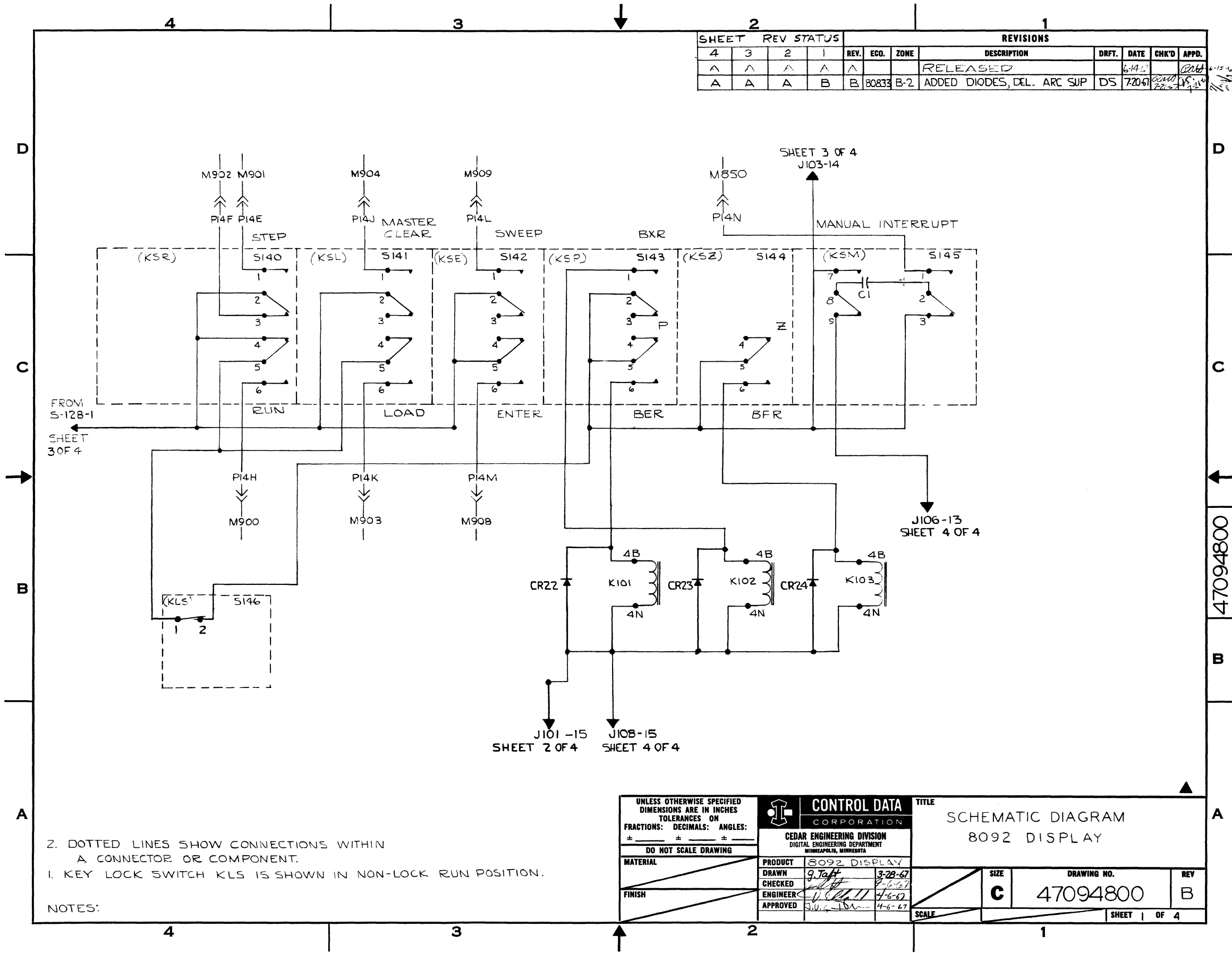
REVISIONS						
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D APPR.
A			RELEASED		3-22-64	RAH



NOTE: C04 THROUGH C09 ARE 55,000 MFD @ 25 VDC.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: * * *		<b>CONTROL DATA</b>		TITLE SCHEMATIC, POWER SUPPLY FERRORESONANT, 60 CPS + 50 CPS	
DO NOT SCALE DRAWING		CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT BIRMINGHAM, ALABAMA		DRAWING NO. 47046500	
PRODUCT	TELEPROGRAMMER	SIZE	C	REV A	
DRAWN	D. SCOFIELD 12-3-65	SCALE		Page 27 SHEET 1 OF 1	
CHECKED	<i>[Signature]</i> 12-3-65				
ENGINEER	<i>[Signature]</i> 12-3-65				
APPROVED	<i>[Signature]</i> 12-3-65				

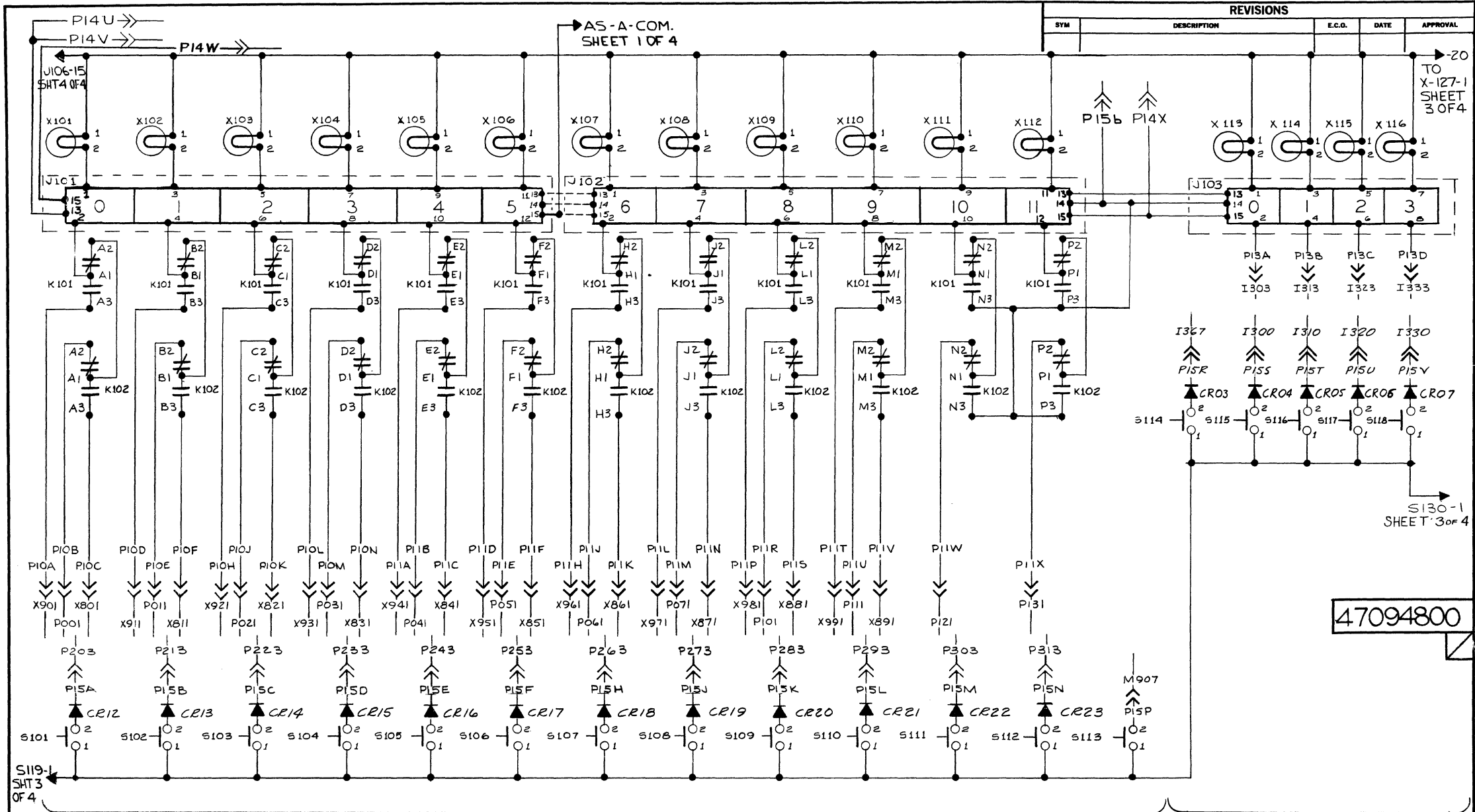
SHEET REV STATUS				REVISIONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.				
4	3	2	1	REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.
A	A	A	A	A			RELEASED		6-14-67		Pat
A	A	A	B	B	80833	B-2	ADDED DIODES, DEL. ARC SUP	DS	7-20-67	Paul	Pat



2. DOTTED LINES SHOW CONNECTIONS WITHIN A CONNECTOR OR COMPONENT.  
 1. KEY LOCK SWITCH KLS IS SHOWN IN NON-LOCK RUN POSITION.

NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: ± .005 ± .005 ± .005		<b>CONTROL DATA CORPORATION</b> CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		TITLE <b>SCHEMATIC DIAGRAM          8092 DISPLAY</b>	
DO NOT SCALE DRAWING		PRODUCT	8092 DISPLAY	SIZE	DRAWING NO.
MATERIAL		DRAWN	G. Toft	3-28-67	REV
FINISH		CHECKED		4-6-67	B
		ENGINEER	J. J. [Signature]	4-6-67	
		APPROVED	J. J. [Signature]	4-6-67	
SCALE				SHEET 1 OF 4	

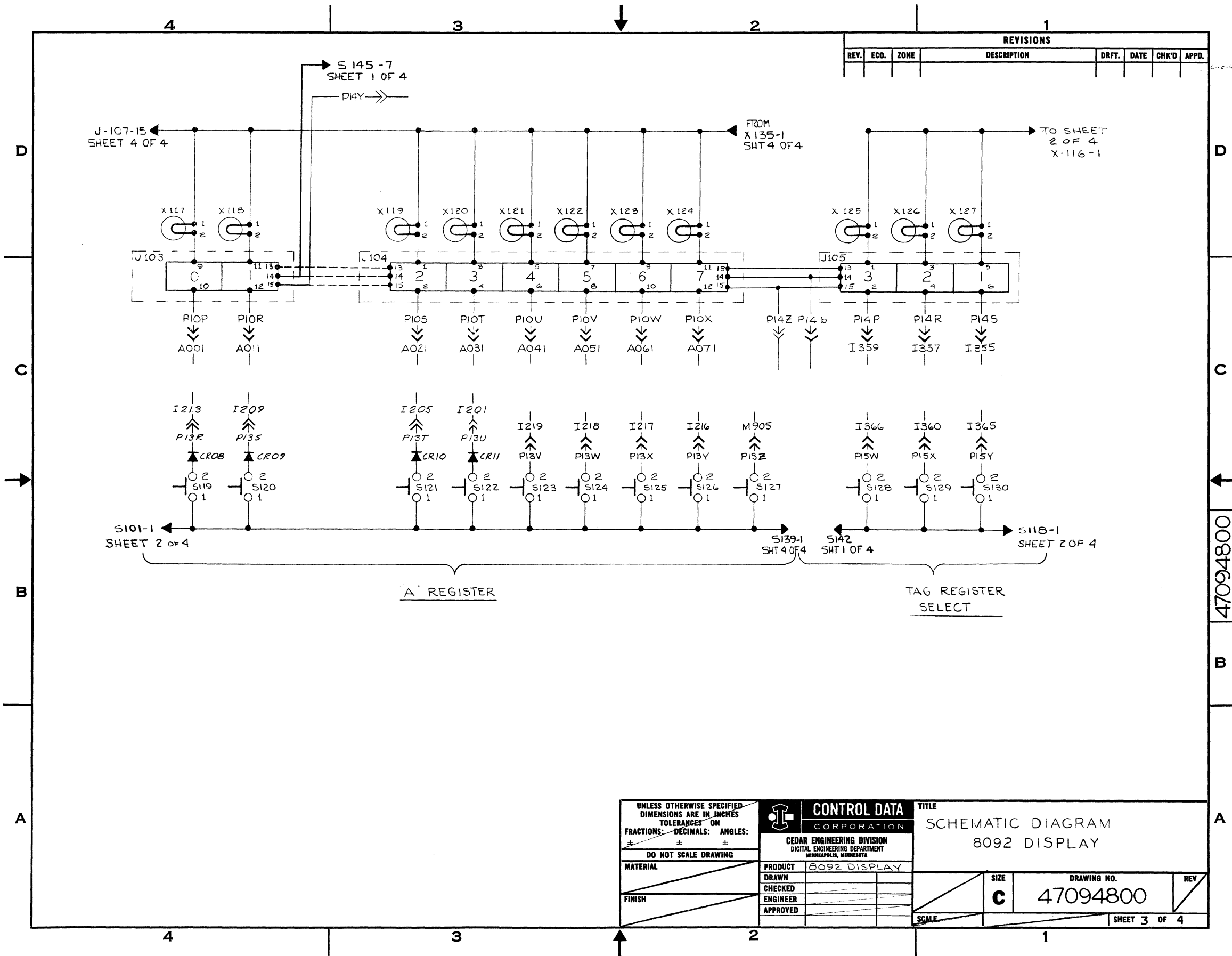


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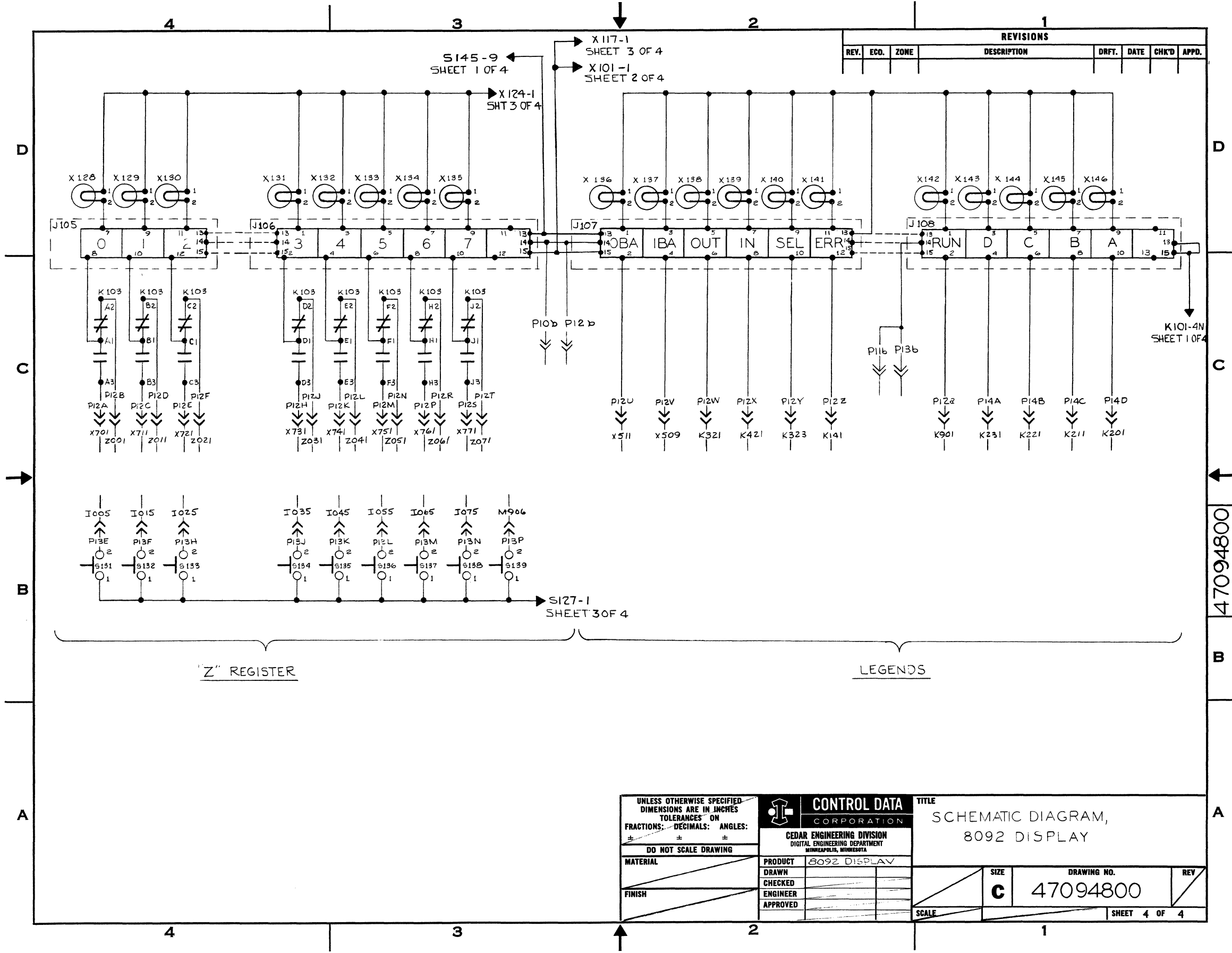
TAG REGISTER

47094800

ITEM	REQD.	PART NO.	DESCRIPTION	MATL.	MATL. SPEC.	NEXT ASSY.	USED ON	FINAL ASSY.	NEXT ASSY.
<b>LIST OF MATERIAL</b>									
UNLESS OTHERWISE SPECIFIED									
DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:									
FRACTIONS: ±1/64    DECIMALS: (0.0025:0.01) ±0.0005    ANGLES: ±1'									
BREAK ALL EDGES AND SHARP CORNERS 0.10 MAX.									
DIMENSIONS APPLY AFTER PLATING OR HEAT TREAT.									
BURRS: NO LOOSE BURRS PERMITTED. TIGHT BURRS PERMITTED IF THEY CANNOT BE DETECTED BY NORMAL VISION OR TOUCH.									
SURFACE FINISH:    ✓ ALL INSIDE SURFACES    ✓ ALL OUTSIDE SURFACES									
DRAWN				BY				DATE	
CHECKED				NAME				SCHEMATIC DIAGRAM	
ENG.				8092 DISPLAY				CONTROL DATA CORP.	
PROD.				FINISH:				CEDAR ENGINEERING DIVISION	
SCALE				WT.				8806 WEST 38TH ST.	
								MINNEAPOLIS 16, MINNESOTA	
								DWG. NO. 47094800	
								SHEET 2 OF 4	



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: ±      ±      ±		<b>CONTROL DATA</b> CORPORATION		TITLE SCHEMATIC DIAGRAM 8092 DISPLAY	
DO NOT SCALE DRAWING		CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		DRAWING NO. 47094800	
MATERIAL	PRODUCT 8092 DISPLAY	SCALE	SIZE C	REV	SHEET 3 OF 4
FINISH	DRAWN	CHECKED	ENGINEER	APPROVED	



REVISIONS						
REV.	ECD.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D APPD.

"Z" REGISTER

LEGENDS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES:		<b>CONTROL DATA CORPORATION</b> CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA	TITLE SCHEMATIC DIAGRAM, 8092 DISPLAY	
DO NOT SCALE DRAWING			PRODUCT 8092 DISPLAY	SIZE <b>C</b>
MATERIAL	FINISH	DRAWN	CHECKED	ENGINEER
		APPROVED		
SCALE				REV
			SHEET 4 OF 4	

47094800



**COMMENT SHEET**

MANUAL TITLE 8090 TELEPROGRAMMER Equipment Diagrams

PUBLICATION NO. 36810900 REVISION \_\_\_\_\_

**FROM:** NAME: \_\_\_\_\_  
BUSINESS ADDRESS: \_\_\_\_\_

**COMMENTS:**

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**COMMENT SHEET**

MANUAL TITLE 8090 TELEPROGRAMMER Equipment Diagrams

PUBLICATION NO. 36810900 REVISION \_\_\_\_\_

**FROM:** NAME: \_\_\_\_\_  
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MINNEAPOLIS, MINN.

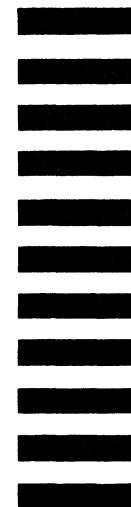
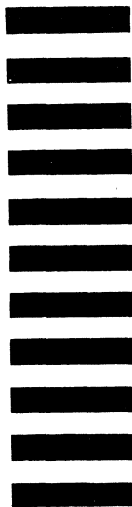
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