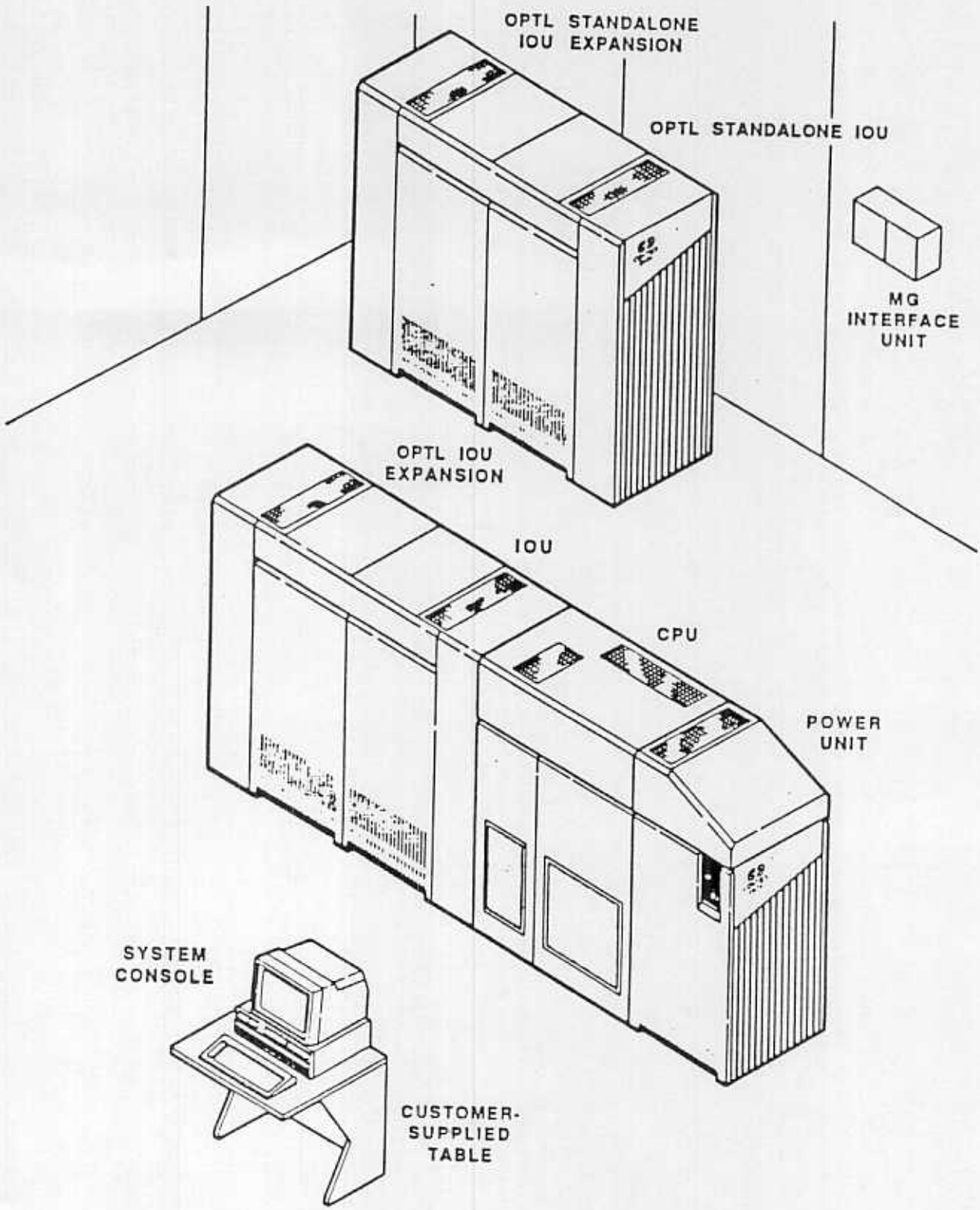
CY 960 / 962

Prepared by JB COUVREUR

Sept. 88


OPTL STANDALONE
IOU EXPANSION
OPTL STANDALONE IOU
MG
INTERFACE
UNIT
OPTL IOU
EXPANSION
IOU
CPU
POWER
UNIT
SYSTEM
CONSOLE
CUSTOMER-
SUPPLIED
TABLE

960 / 962 SERIES SYSTEMS

FEATURES :

- INCREASED CPU PERFORMANCE THOUGH TECHNOLOGY CHANGE
- INCREASED REAL MEMORY CAPACITY AND ADDRESSABILITY
- SUPPORT FOR 1 OR 2 INPUT/OUTPUT UNITS
- HI PERFORMACE I/O CHANNELS
- AIR COOLED CABINETS

MODELS :

		SOFTWARE SUPPORT
- 960-11	1 CPU, 64MB MEMORY, 1 IOU	NOS, NOS/VE
- 960-31	1 CPU, 64MB MEMORY, 1 IOU	NOS, NOS/VE
- 960-32	2 CPU, 64MB MEMORY, 1 IOU	NOS, NOS/VE
- 962-11	1 CPU, 64MB MEMORY, 1 IOU	NOS/VE
- 962-31	1 CPU, 64MB MEMORY, 1 IOU	NOS/VE
- 962-32	2 CPU, 64MB MEMORY, 1 IOU	NOS/VE

PERFORMANCE UPGRADES :

- 960-11 TO 960-31 TO 960-32
- 962-11 TO 962-31 TO 962-32

CENTRAL PROCESSOR FEATURES :

- WORD SIZE 64 BITS / 8 BITS BYTES
- CLOCK 11,2 NS
- NUMBER OF GENERAL OPERATING REGISTERS 32
- DATA / INSTRUCTION CACHE 32 KB
- CONTROL STORE MEMORY 32 KB WITH 32 KB OF SHADOW MEMORY
- FLOATING POINT ARITHMETIC
  - SINGLE PRECISION = 16 BITS EXPONENT, 48 BITS COEFFICIENT
  - DOUBLE PRECISION = 16 BITS EXPONENT, 96 BITS COEFFICIENT
- PIPELINE ARCHITECTURE
- ONE CENTRAL MEMORY PORT PER CPU
- INSTRUCTION LOOKHEAD
- BRANCH PREDICTION
- INSTRUCTION RETRY
- TECHNOLOGY HI DENSITY ECL FGE 6300 LOGIC ARRAY
  HI SPEED ECL C200 LOGIC ARRAY

CENTRAL MEMORY FEATURES:

- WORD SIZE — 64 BITS / 8 BITS BYTES
- WORD AND BYTE ADDRESSABLE
- REAL MEMORY ADDRESSING LIMIT — 2 GIGA BYTES
- CAPACITY — MINIMUM 32 MB, MAXIMUM 256 MB
- 8 BANKS PHASED
- BANK R/W CYCLE — 6 x 44,8NSEC
- SECDED / PARITY
- PORTS — 2 FOR CPU'S, 2 FOR IOU'S
- VIRTUAL MEMORY ADDESSING
  TASK = 8,8 x 10*12 BYTES
  4096 SEGMENTS PER TASK
  2147 MEGABYTES PER SEGMENT
- VARIABLE PAGE SIZE
- TECHNOLOGY — 1 MEGABIT DRAM

960 INPUT/OUTPUT UNIT : I4AC

- BASE UNIT : NIO
  20 PERIPHERAL PROCESSORS — 250 NSEC CYCLE TIME, 16 KB MEMORY WITH SECDED
  24 CYBER 170 I/O CHANNELS — 24 MBITS/S XFER RATE (3MB/S)
- BASE UNIT OPTION : CIO
  ADDITION OF 5 OR 10 DMA I/O PROCESSORS
  ADDITION OF 5 OR 10 DMA I/O CHANNEL INTERFACES
  DMA I/O CHANNELS SUPPORTED
  ISI (INTELLIGENT STANDARD INTERFACE) 12MB/S
  CYBER 170/DMA 15 OR 3MB/S
  IPI (INTELLIGENT PERIPHERAL INTERFACE) 10MB/S
- MAXIMUM BASE IOU CONFIGURATION — 30 PROCESSORS, 34 I/O CHANNELS
- SECOND IOU OPTION — ADD A SECOND 962 TYPE IOU

962 INPUT/OUTPUT UNIT : I4C

- BASE UNIT : CLUSTER
  10 I/O PROCESSORS WITH DMA CAPABILITY
  INDEPENDENT I/O PROCESSORS BY 5
  250 NSEC CYCLE TIME
  16 KB MEMORY WITH SECDED
  8 EXTERNAL DMA I/O CHANNEL INTERFACES
  DMA I/O CHANNELS SUPPORTED
  ISI/DMA 12MB/S
  CYBER 170/DMA 15 OR 3 MB/S
  IPI/DMA 10MB/S
- BASE UNIT OPTIONS
  ADDITION OF 5 OR 10 DMA I/O PROCESSORS
  ADDITION OF 5 OR 10 DMA I/O CHANNELS
- MAXIMUM BASE IOU CONFIGURATION — 20 I/O PROCESORS, 18 DMA I/O CHANNELS
- SECOND IOU OPTION — ADD A SECOND IDENTICAL IOU

OTHER IOU FEATURES :

- MICRO-PROCESSOR BASED DEAD START
- REAL-TIME CLOCK
- WALL CLOCK
- OPERATOR CONSOLE INTERFACE
- REMOTE TECHNICAL ASSISTANCE INTERFACE

RELIABILITY, AVAILABILITY,MAINTAINABILITY (RAM) FEATURES :

- PARITY ON ALL INTERNAL AND EXTERNAL INTERFACES
- SECDED FOR MAIN AND I/O PROCESSOR MEMORIES
- CPU INSTRUCTION RETRY
- DEGRADABLE COMPONENTS
- MAINTENANCE REGISTERS ACCESSIBLE BY MAINTENANCE CONTROL UNIT
- CONFIDENCE LEVEL TESTS RUN PRIOR TO SYSTEM OPERATION
- CONCURRENT/ON-LINE DIAGNOSTICS
- ENGINEERING FILE

COOLING :

- AIR COOLED — CPU, CENTRAL MEMORY, POWER CABINET, IOU
- HEAT DISSIPATION — 91000 BTU'S PER HOUR

POWER REQUIREMENTS : 1CPU 64MB

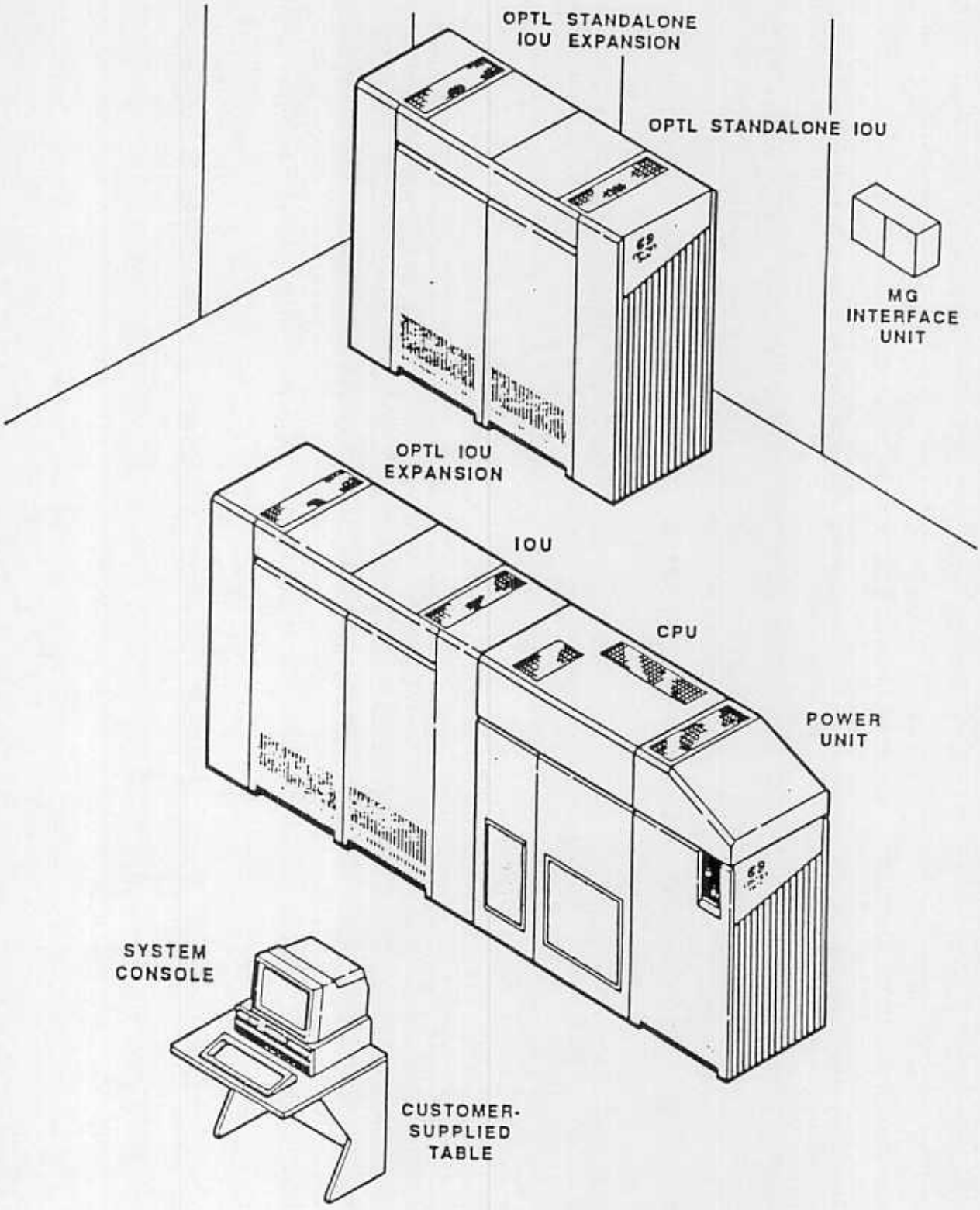
- 400HZ 16.5 KVA
- 50/60HZ 5.2 KVA

ENVIRONMENTAL :

- COMPUTER ROOM ENVIRONMENT
- TEMPERATURE RANGE (OPERATING) 60F to 90F
- HUMIDITY RANGE (OPERATING) 35% to 60%

TECHNOLOGY :

- FAIRCHILD C200 LOGIC ARRAY
  ECL
  HIGH SPEED
  56 LEAD FLAT PACK
- FAIRCHILD FGE6300 LOGIC ARRAY
  ECL
  HIGH DENSITY
  301 PIN GRID ARRAY (PGA)
- DYNAMIC RANDOM MEMORY ACCESS (DRAM) 1 MEGABIT
  HITACHI
  MITSUBISHI


OPTL STANDALONE
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INTERFACE
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TABLE

PACKAGING

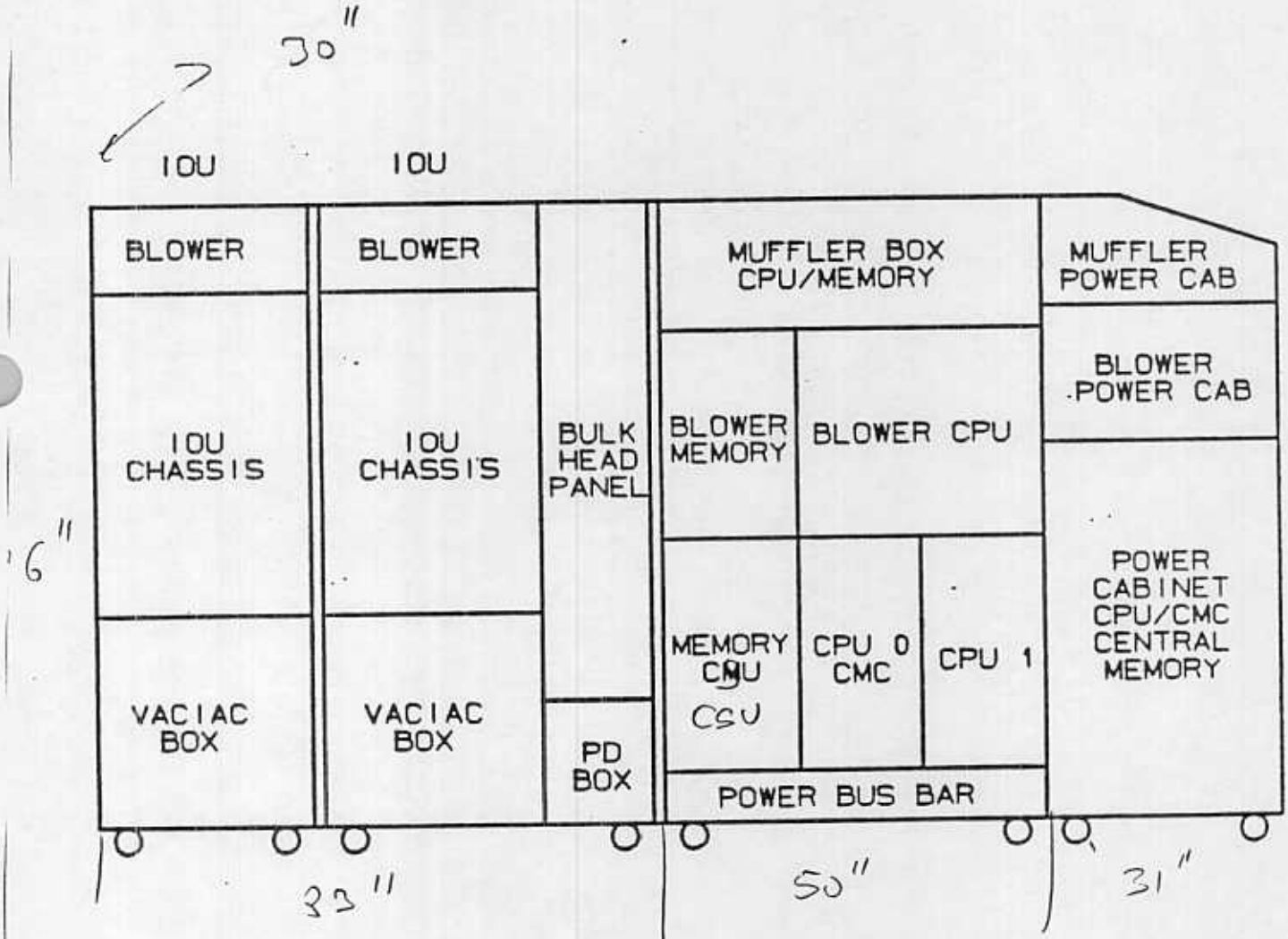
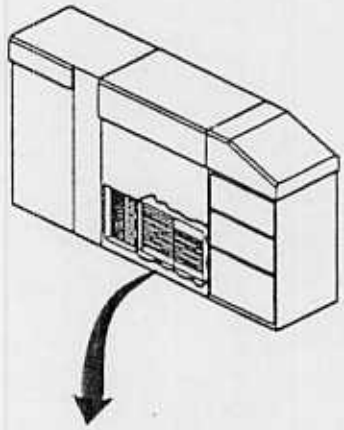
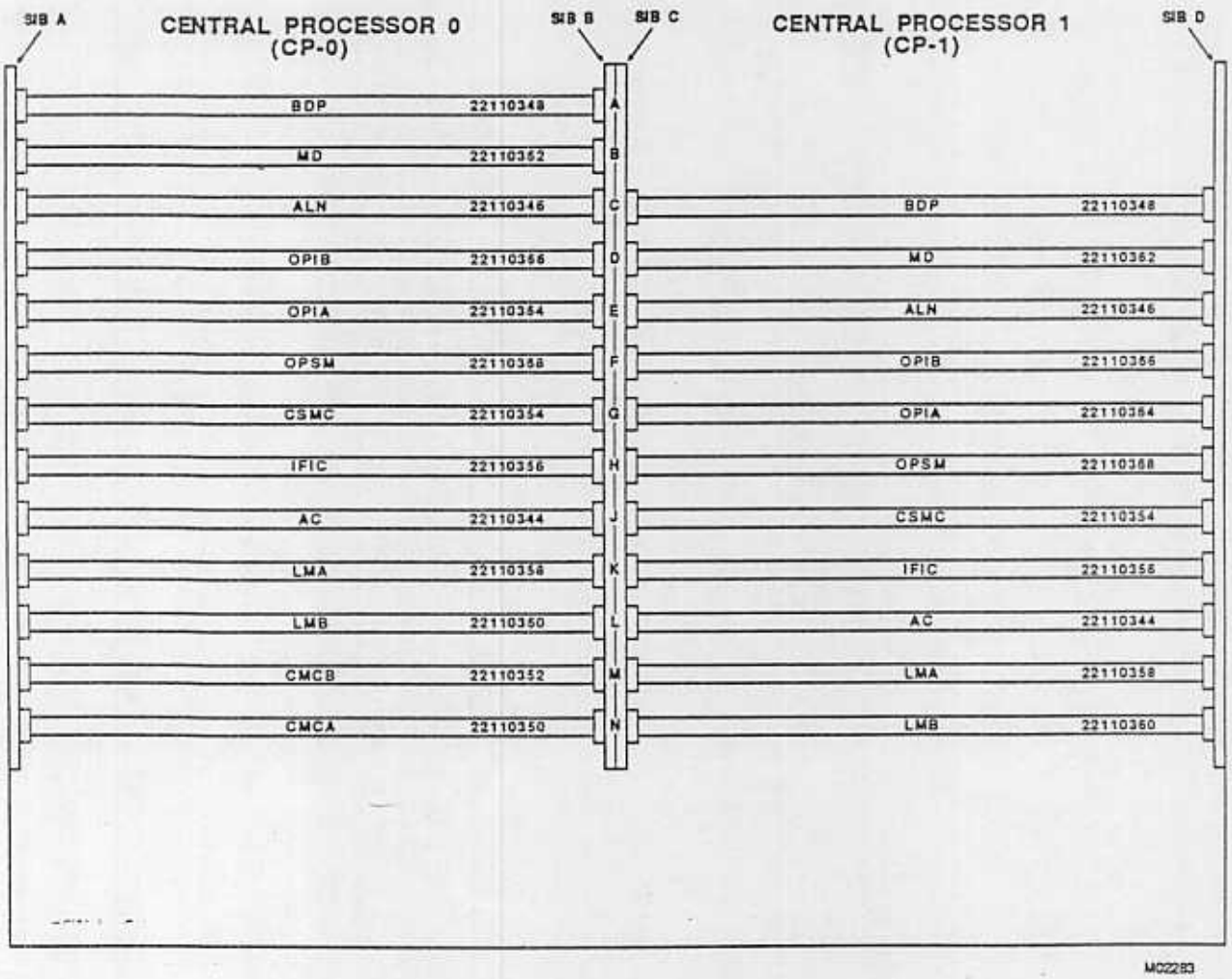
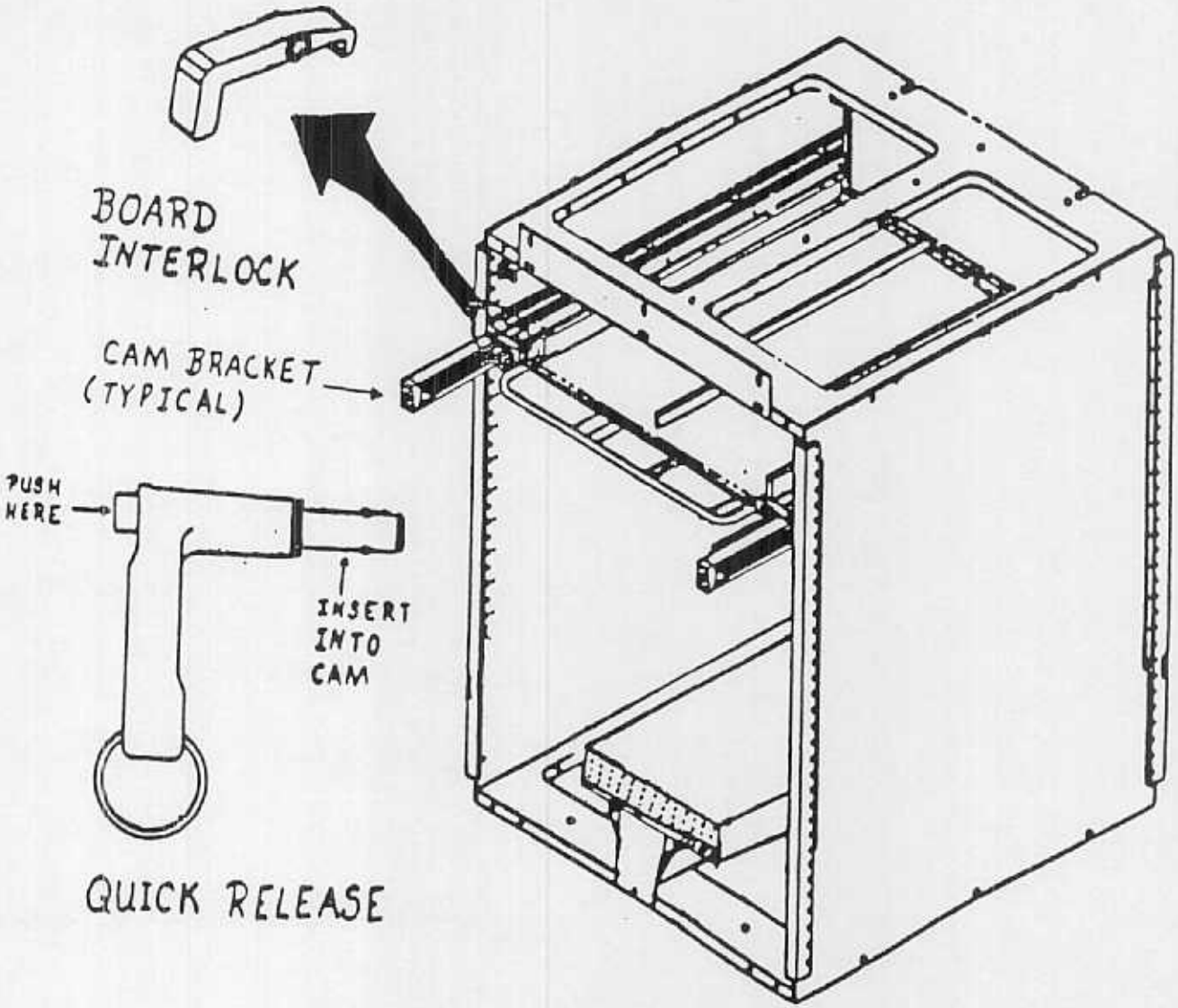


Figure 3.2.3.6-2. PIP3 Front View





dule Locations



CENTRAL PROCESSOR CAGE ASSY

3.2.3.6.1.1 CP BOARD, LIF CONNECTORS, AND TEST POINTS

The reference designations for the CP boards which contain the LIF connector and test points are as shown in Figures 3.2.3.6.1.1-1 through -3.

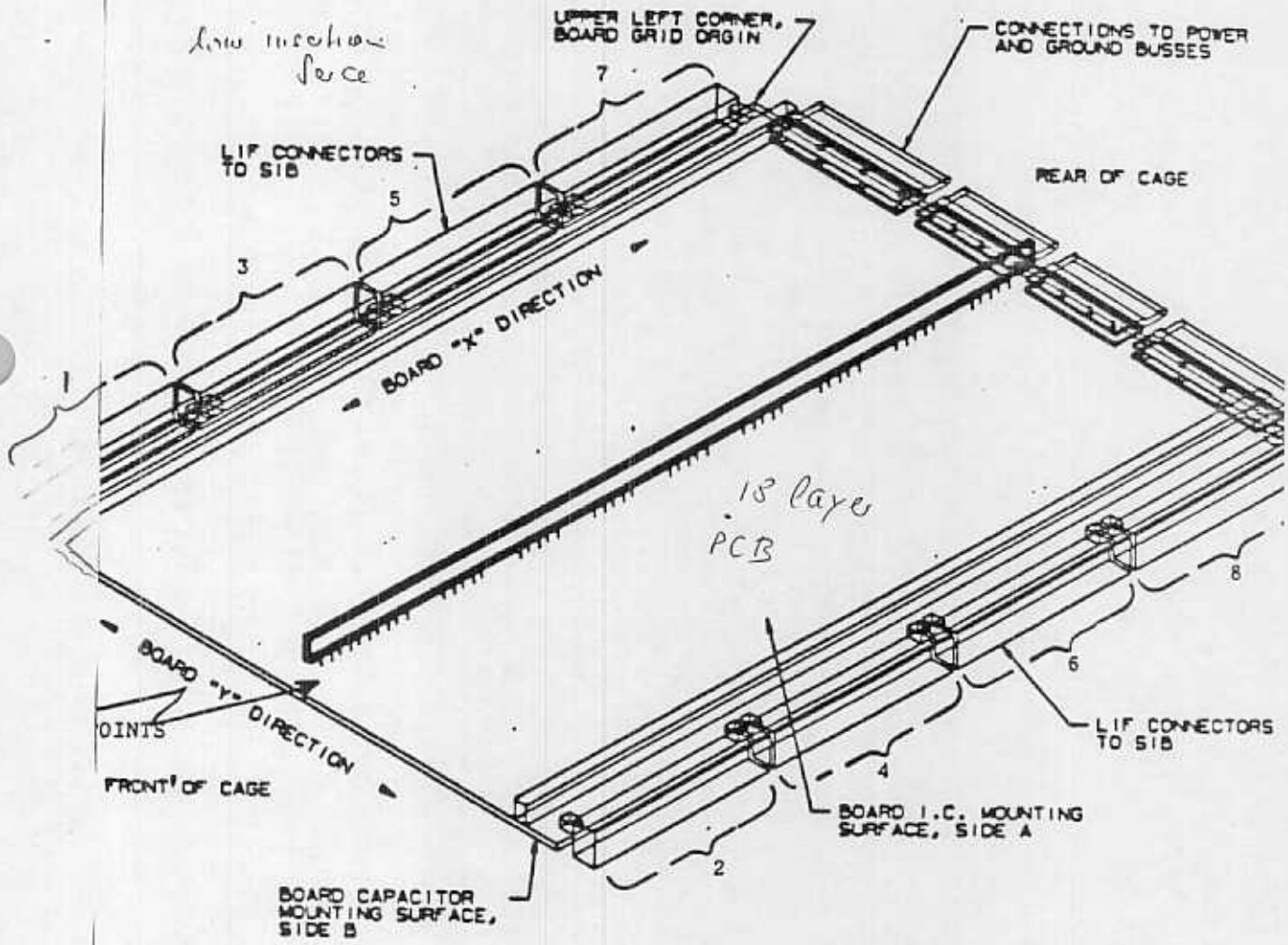
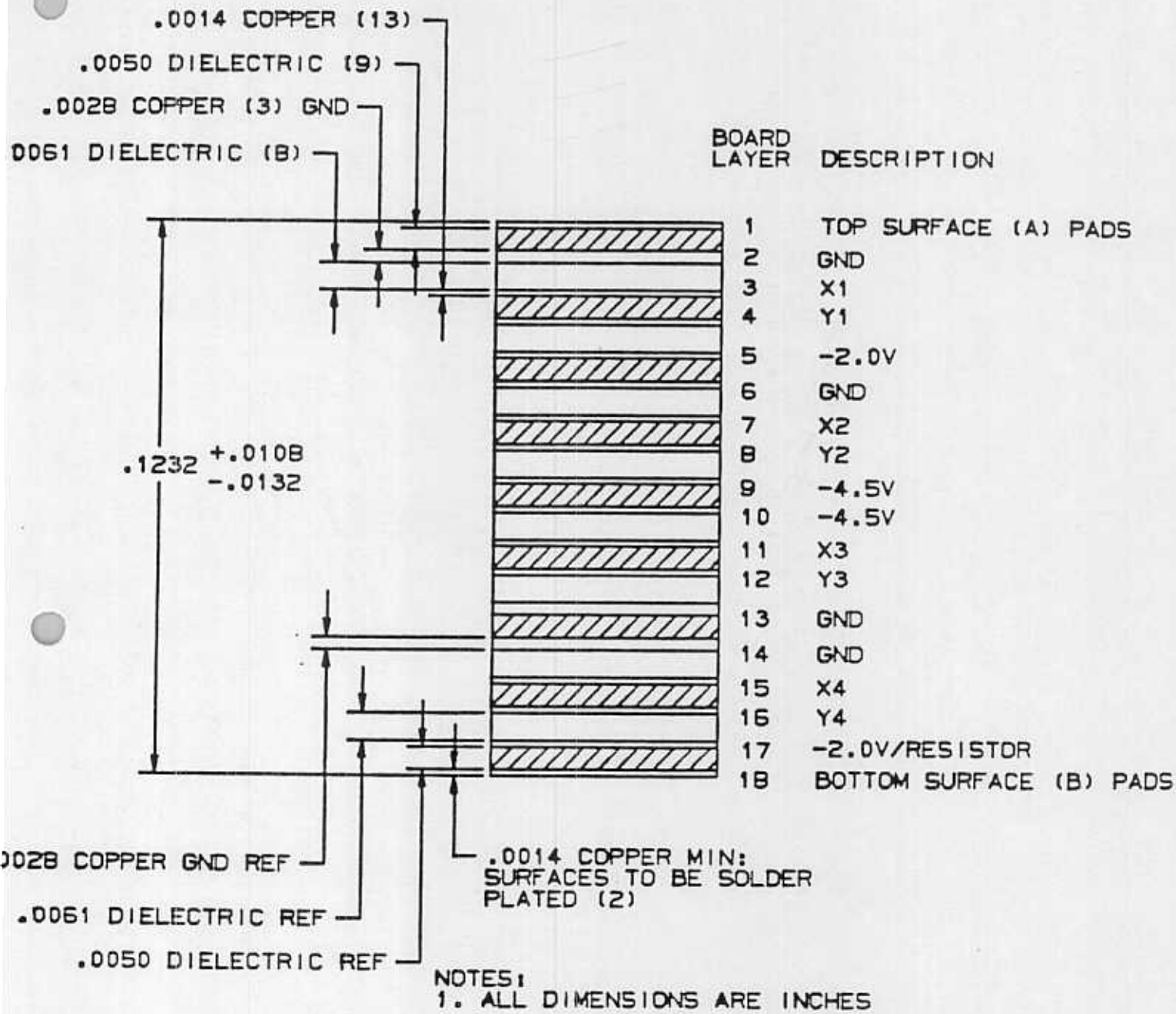


Figure 3.2.3.6.1.1-1. CP Board

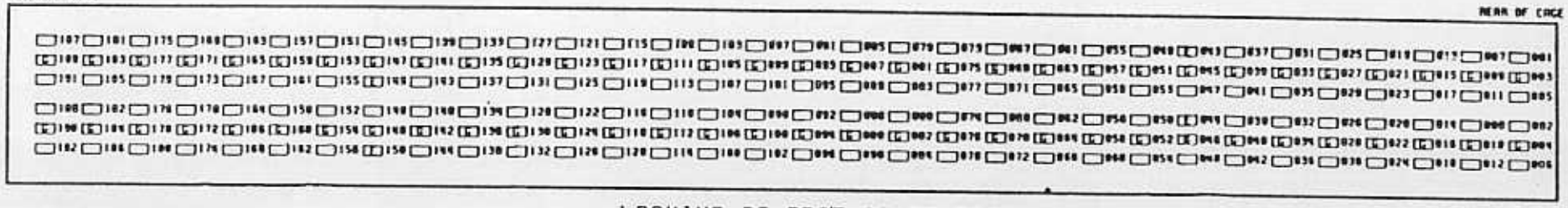


CPU BOARD EIGHT SIGNALS LAYERS

FOR CONNECTORS 2,4,6, AND 8

TOP OF BOARD

FRONT OF CAGE



REAR OF CAGE

BOTTOM OF BOARD

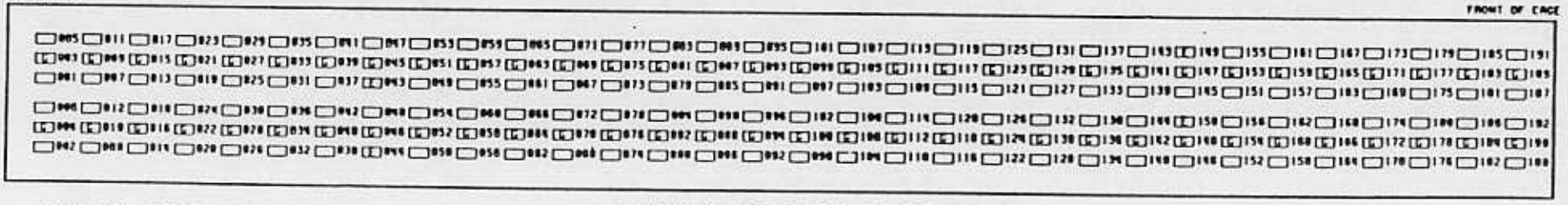
LOOKING AT EDGE OF CP BOARD

(AS VIEWED FROM THE SIB)

FOR CONNECTORS 1,3,5, AND 7

TOP OF BOARD

REAR OF CAGE



FRONT OF CAGE

BOTTOM OF BOARD

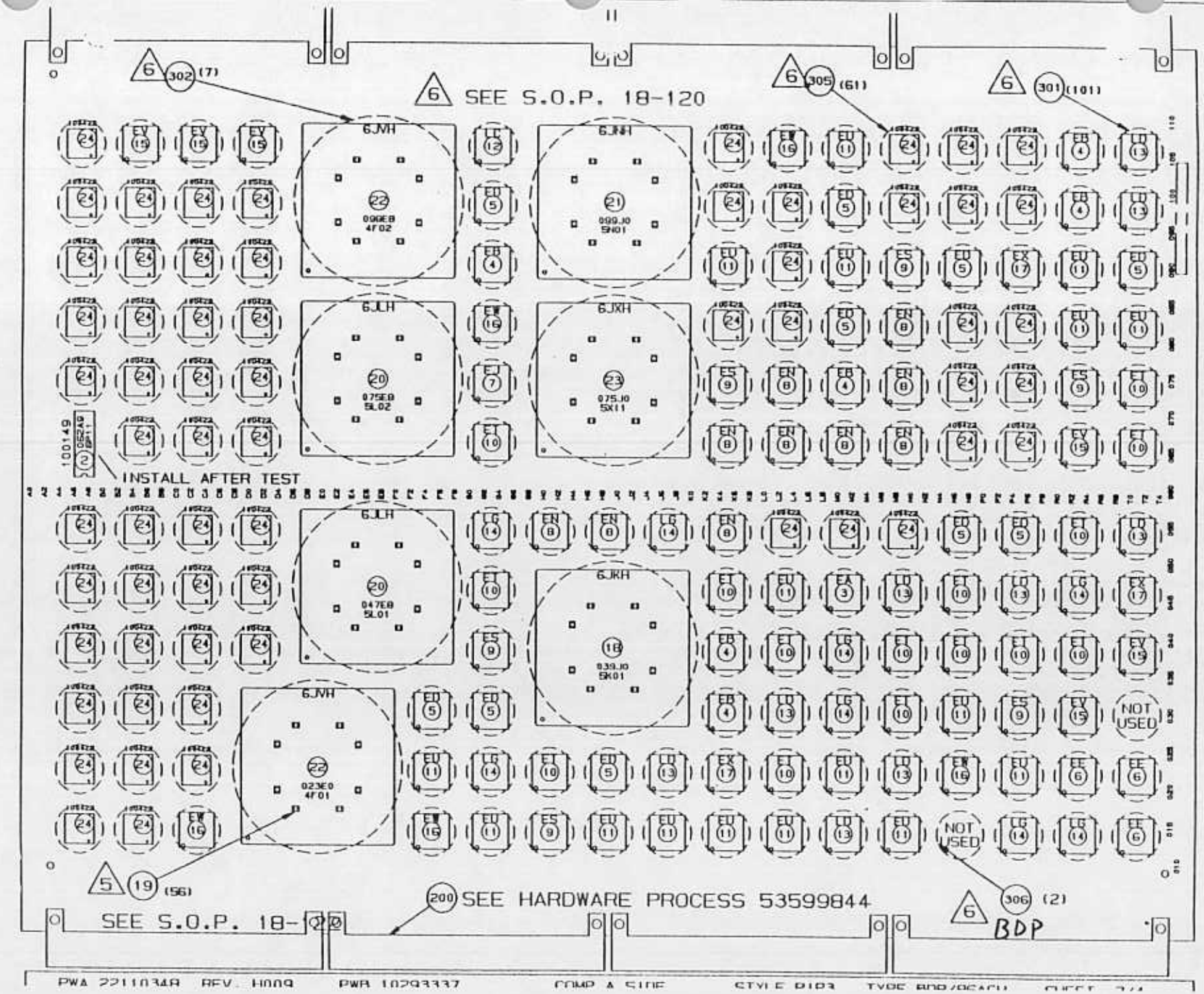
LOOKING AT EDGE OF CP BOARD

(AS VIEWED FROM THE SIB)

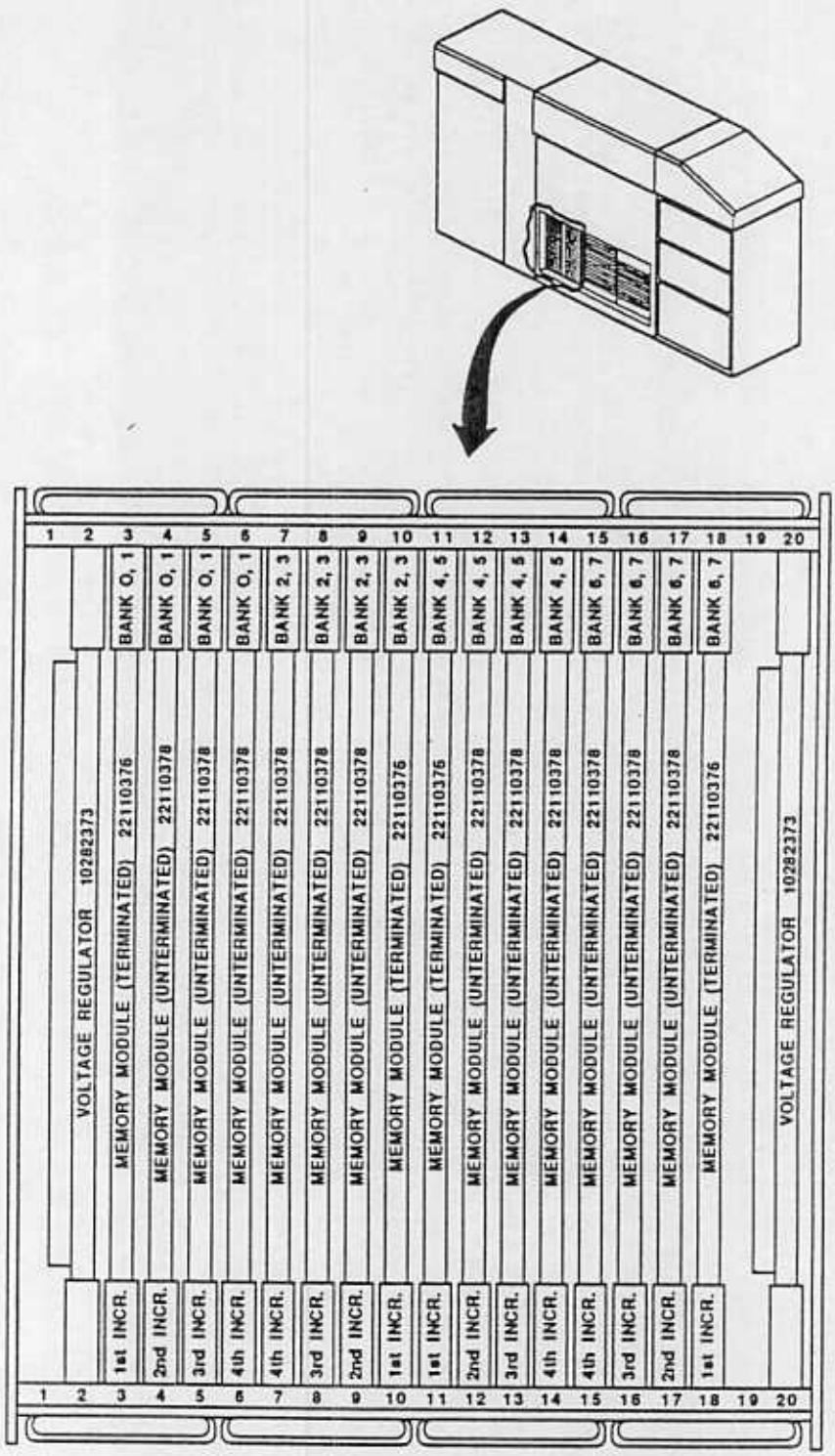
G = REQUIRED GROUND PIN

E = PREFERRED ECO PIN

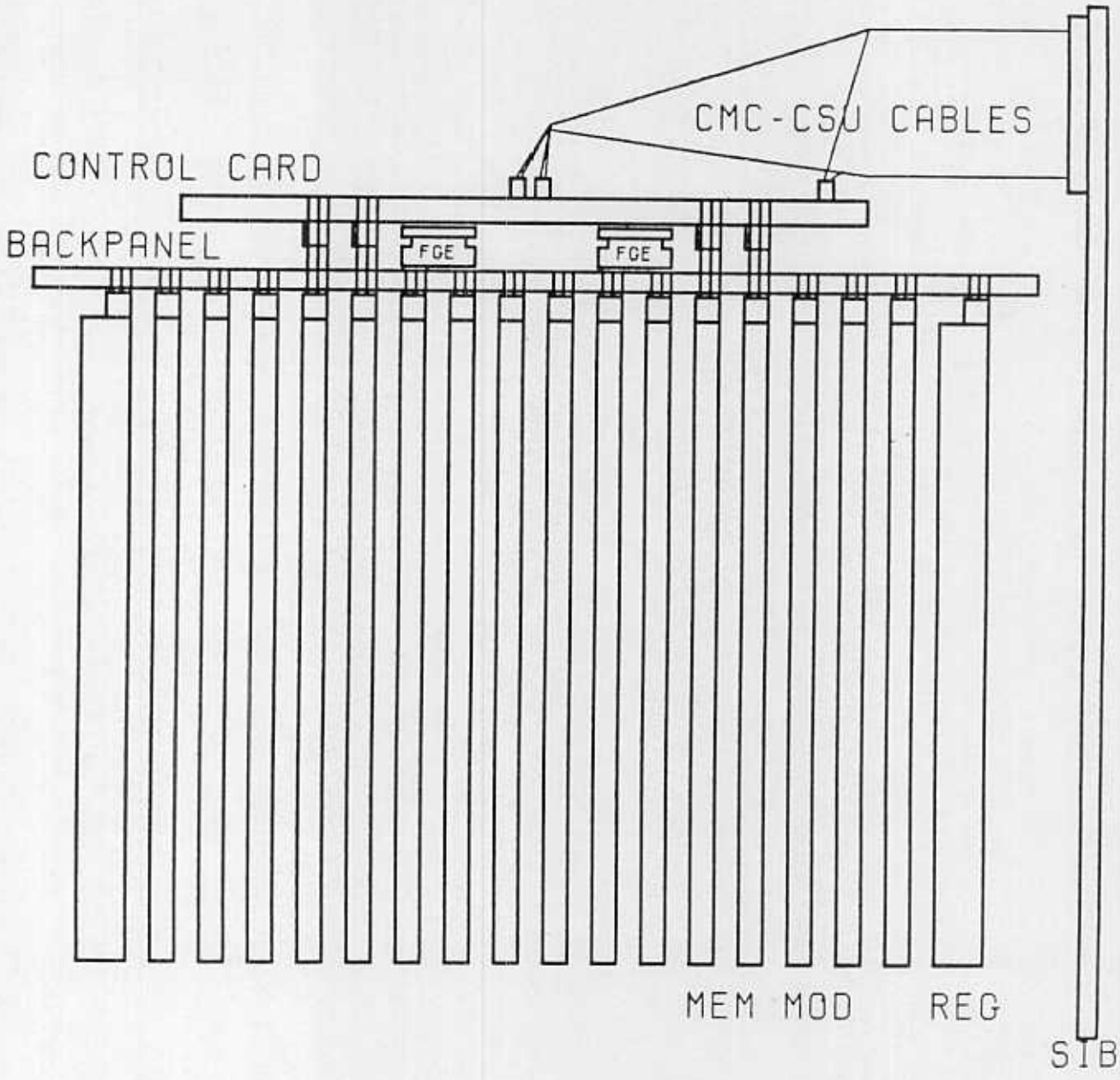
CONTROL DATA CORPORATION	FUJITSU CONNECTOR PIN NUMBERING	EDGE	DWG NO	REV
COMPUTER DEVELOPMENT ENGINEERING DIVISION		SHEET		PAGE


6 302 (7)
6 SEE S.O.P. 18-120
6 305 (61)
6 301 (101)
6JVH
6JJH
6JLH
6JXH
6JLH
6JXH
6JVH
INSTALL AFTER TEST
NOT USED
NOT USED
5 19 (56)
200 SEE HARDWARE PROCESS 53599844
SEE S.O.P. 18-120
6 306 (2)
BDP

3-8

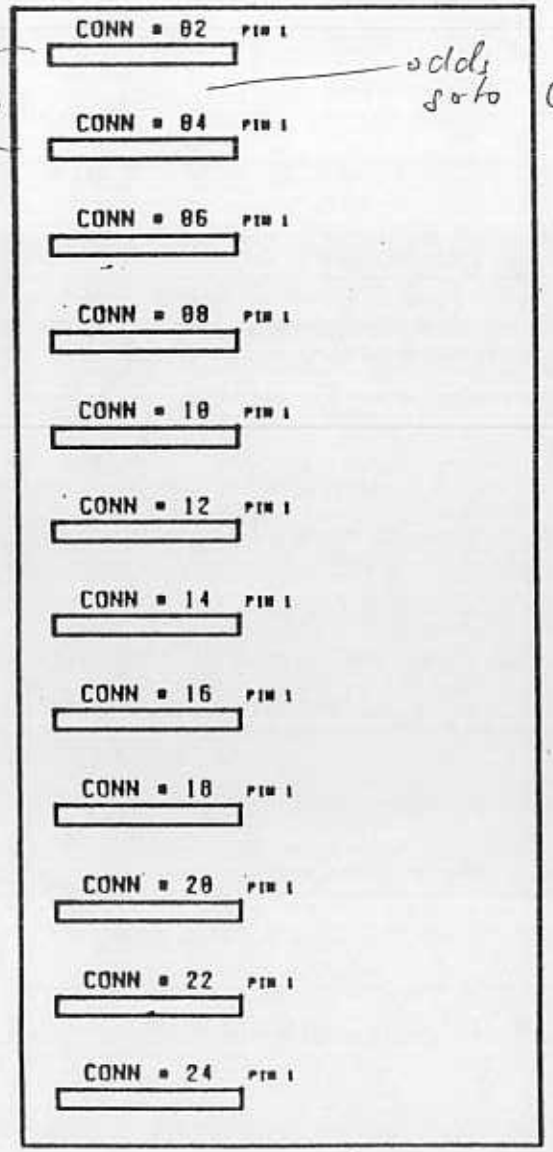

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
VOLTAGE REGULATOR 10282373
MEMORY MODULE (TERMINATED) 22110376
MEMORY MODULE (UNTERMINATED) 22110378
BANK 0, 1
BANK 2, 3
BANK 4, 5
BANK 6, 7
1st INCR.
2nd INCR.
3rd INCR.
4th INCR.
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

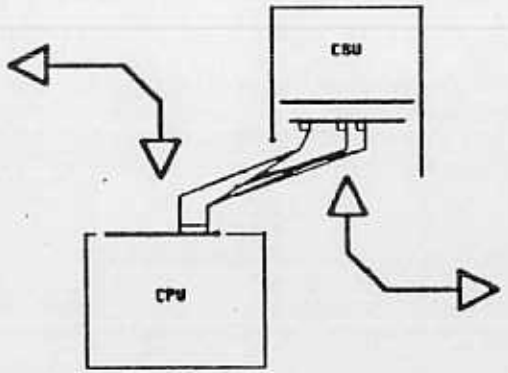
M02284



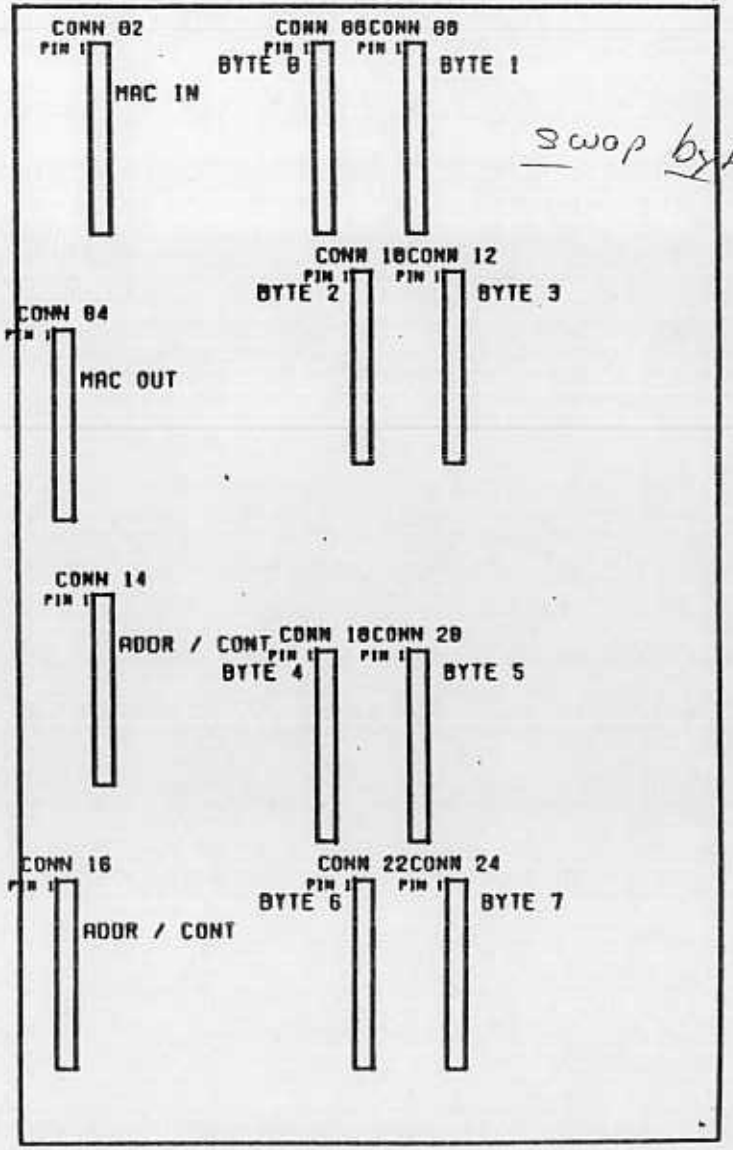
CSU CAGE top view

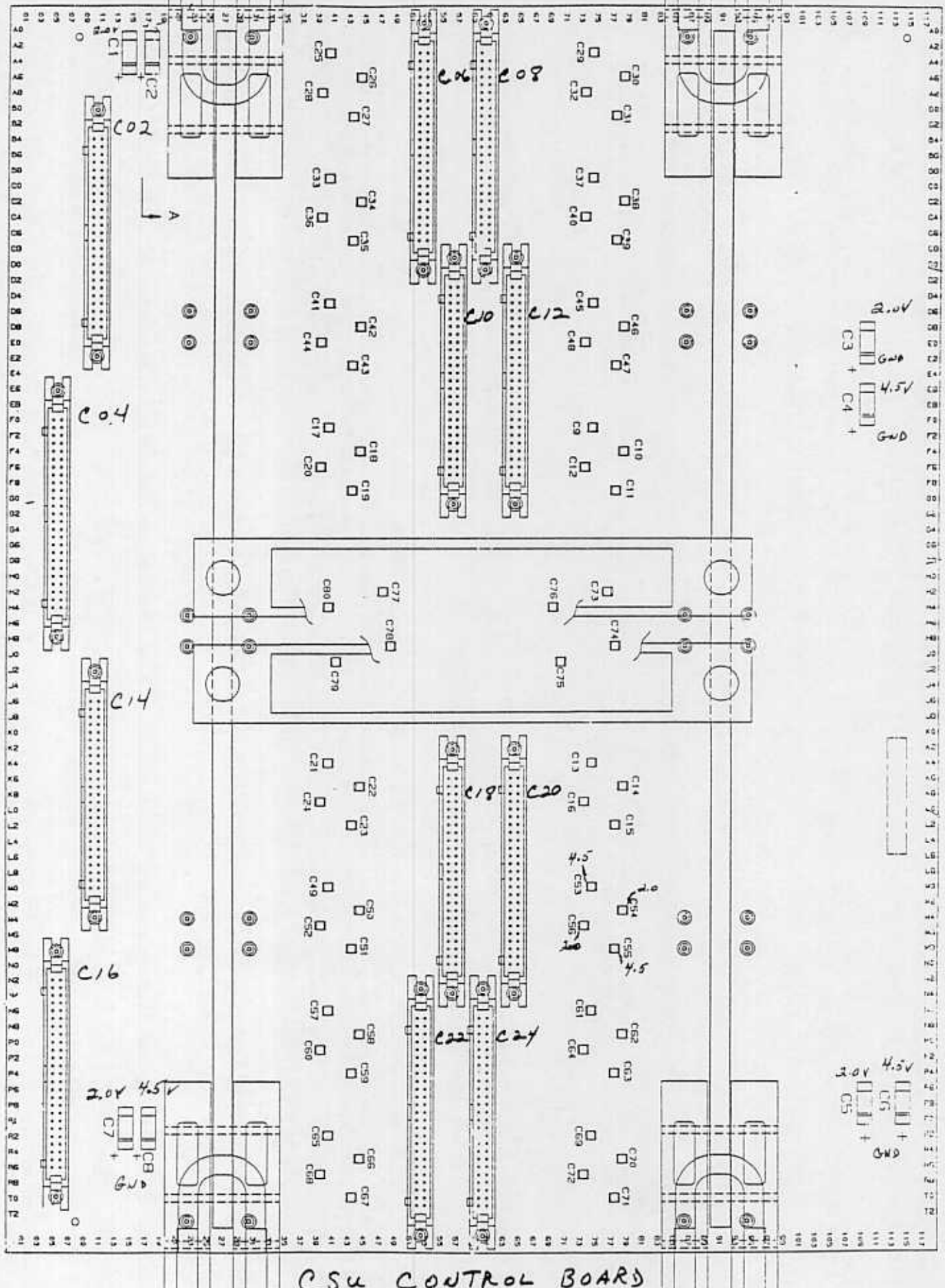
SIB A





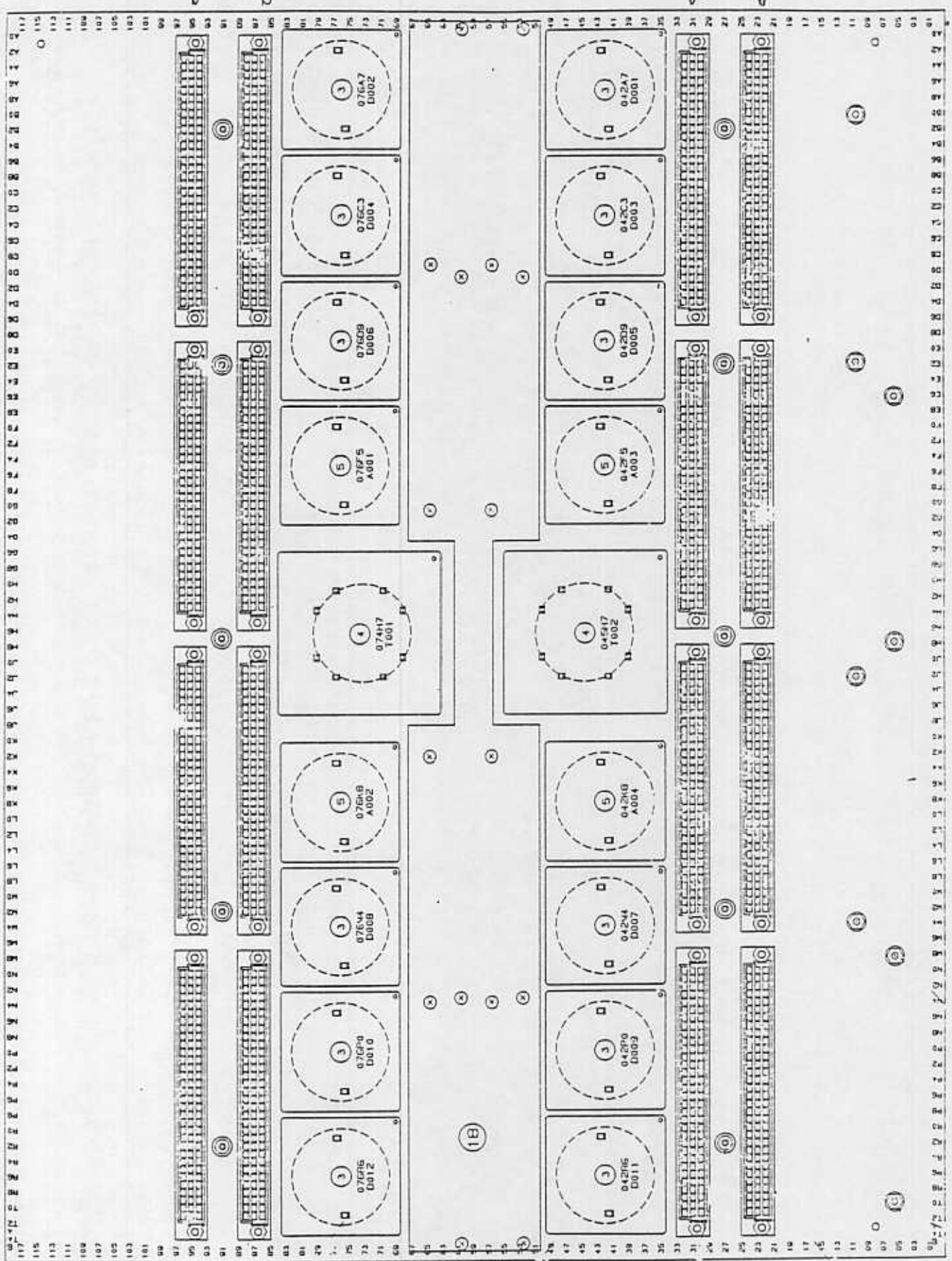
MEM CONT BRD
MIDAS (REV 1)

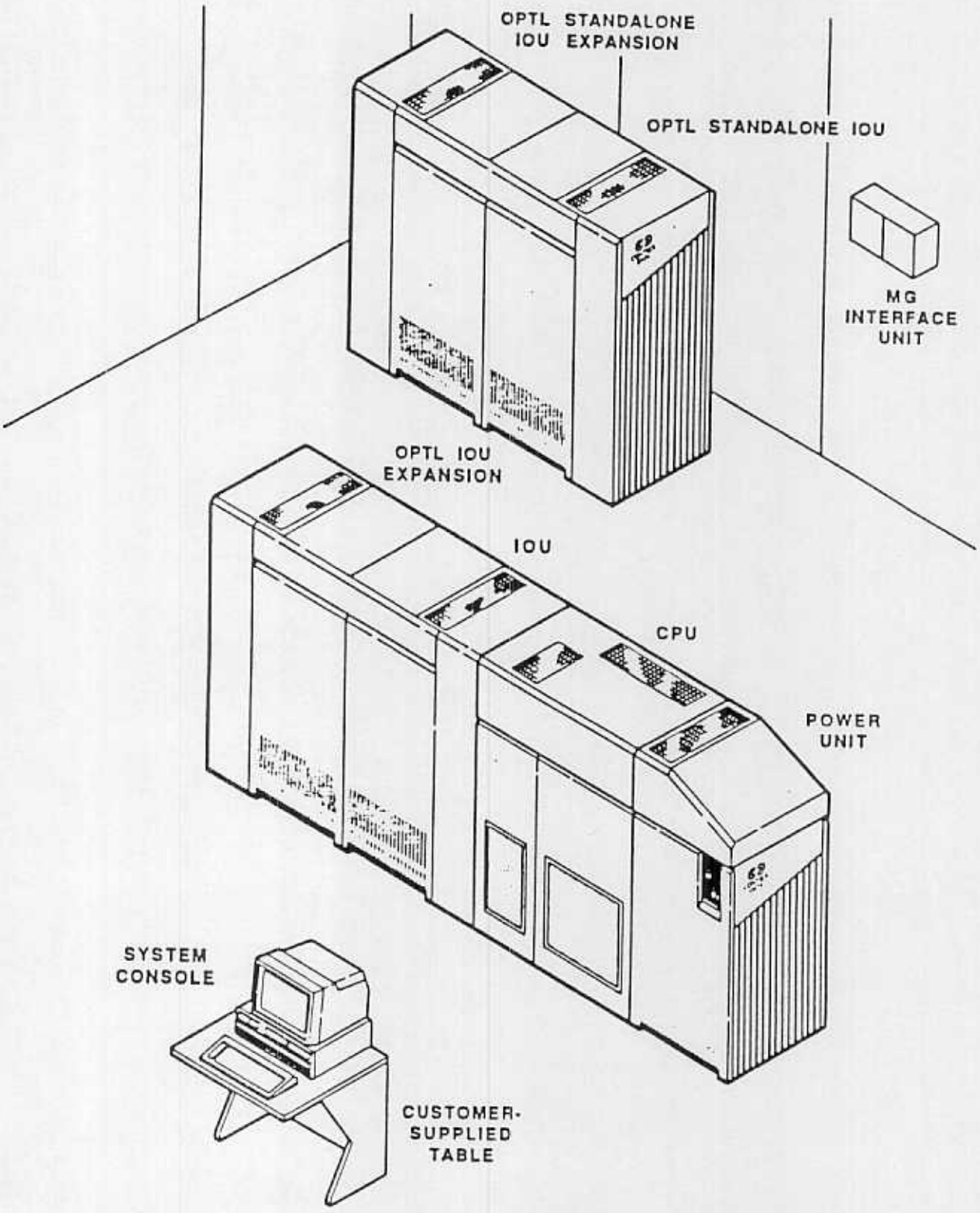




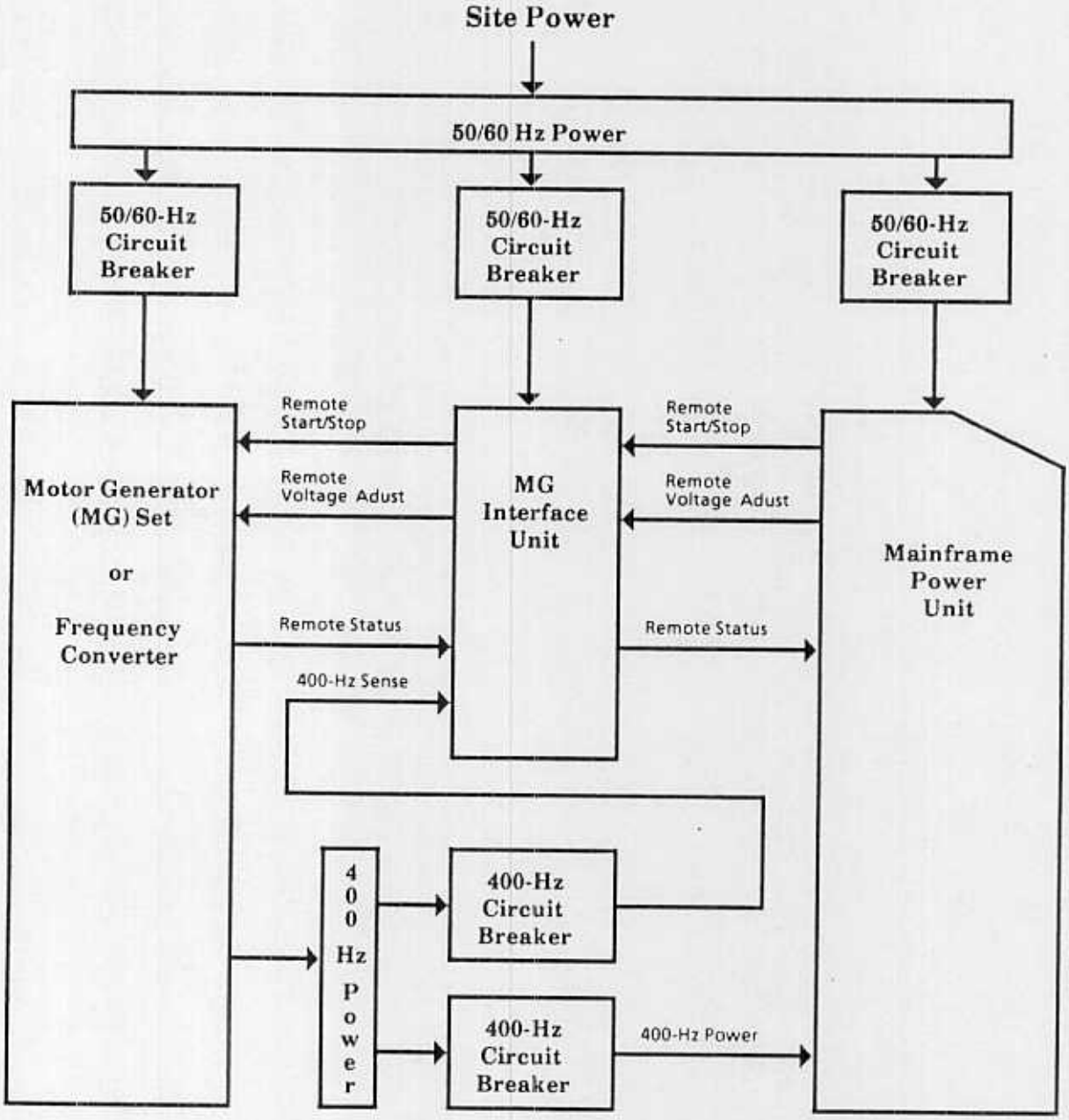
CSU CONTROL BOARD
A SIDE

Connector side of backplane





GD311 POWER UNIT


Site Power
50/60 Hz Power
50/60-Hz Circuit Breaker
50/60-Hz Circuit Breaker
50/60-Hz Circuit Breaker
Motor Generator (MG) Set
or
Frequency Converter
Remote Start/Stop
Remote Voltage Adust
Remote Status
400-Hz Sense
MG Interface Unit
Remote Start/Stop
Remote Voltage Adust
Remote Status
Mainframe Power Unit
400 Hz Power
400-Hz Circuit Breaker
400-Hz Circuit Breaker
400-Hz Power

. INPUT POWER

60/400 Hz Factory Cords

60 Hz	10A, 120/208v
400 Hz	40A, 120/208v

50/400 Hz customer Hardwired

50 Hz	5A, 220/380v
or	5A, 240/415v
400 Hz	40A, 120/208v

. SITE POWER CONFIGURATION

60.50 Hz direct from site breaker panel

400 Hz controlled by mainframe power unit via MG interface unit.

. MG INTERFACE UNIT

Warning : MG interface unit contains unswitched line voltage.

Controls 400 Hz MG

- 1 unit controls up to 2 MG's
- Units can be daisychained to control additional MG's.

Controls room contactors

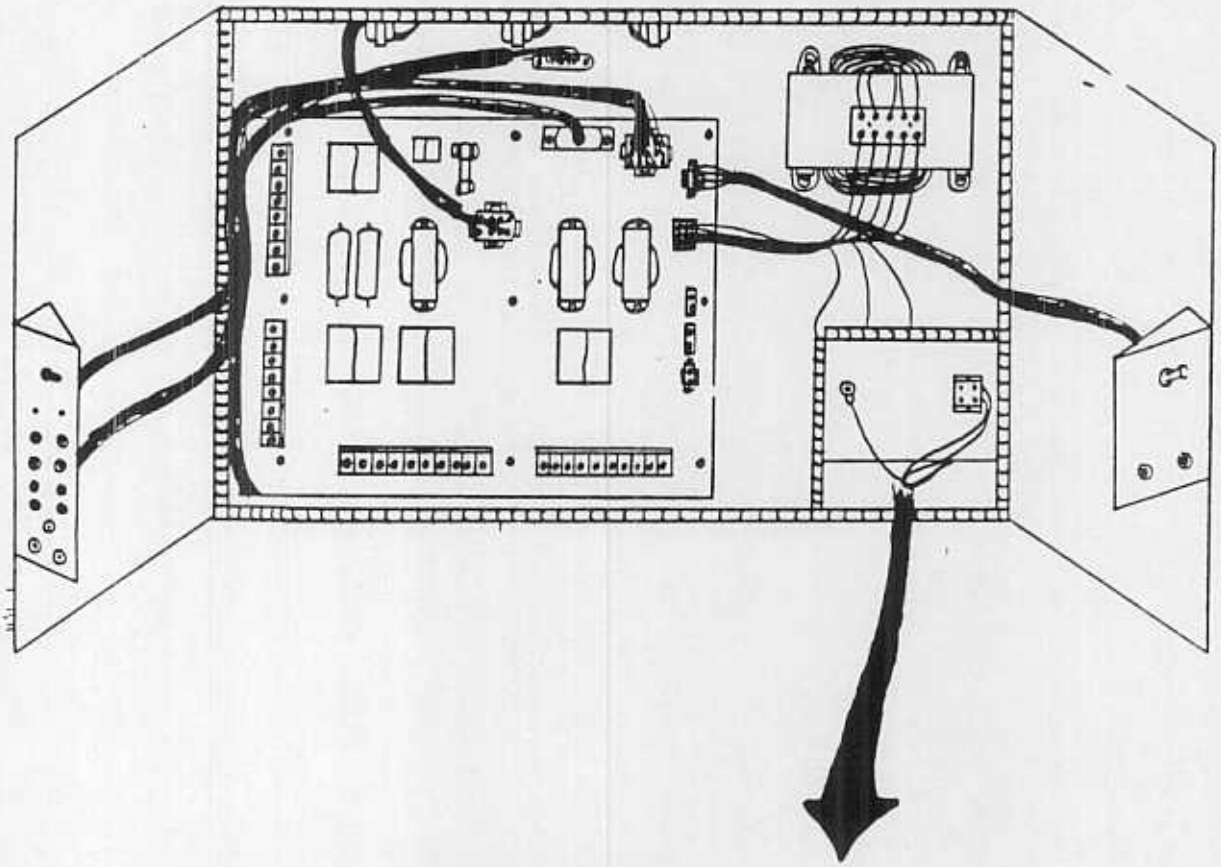
- Up to 3 sets of contacts for each Mg interface unit.
- Up to 2 external horns for each Mg interface unit.

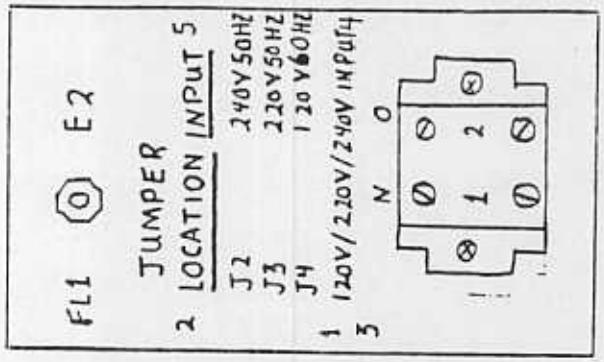
Facilitates MG checkout before mainframe arrives.

Provides logic level interface to control power deuces.

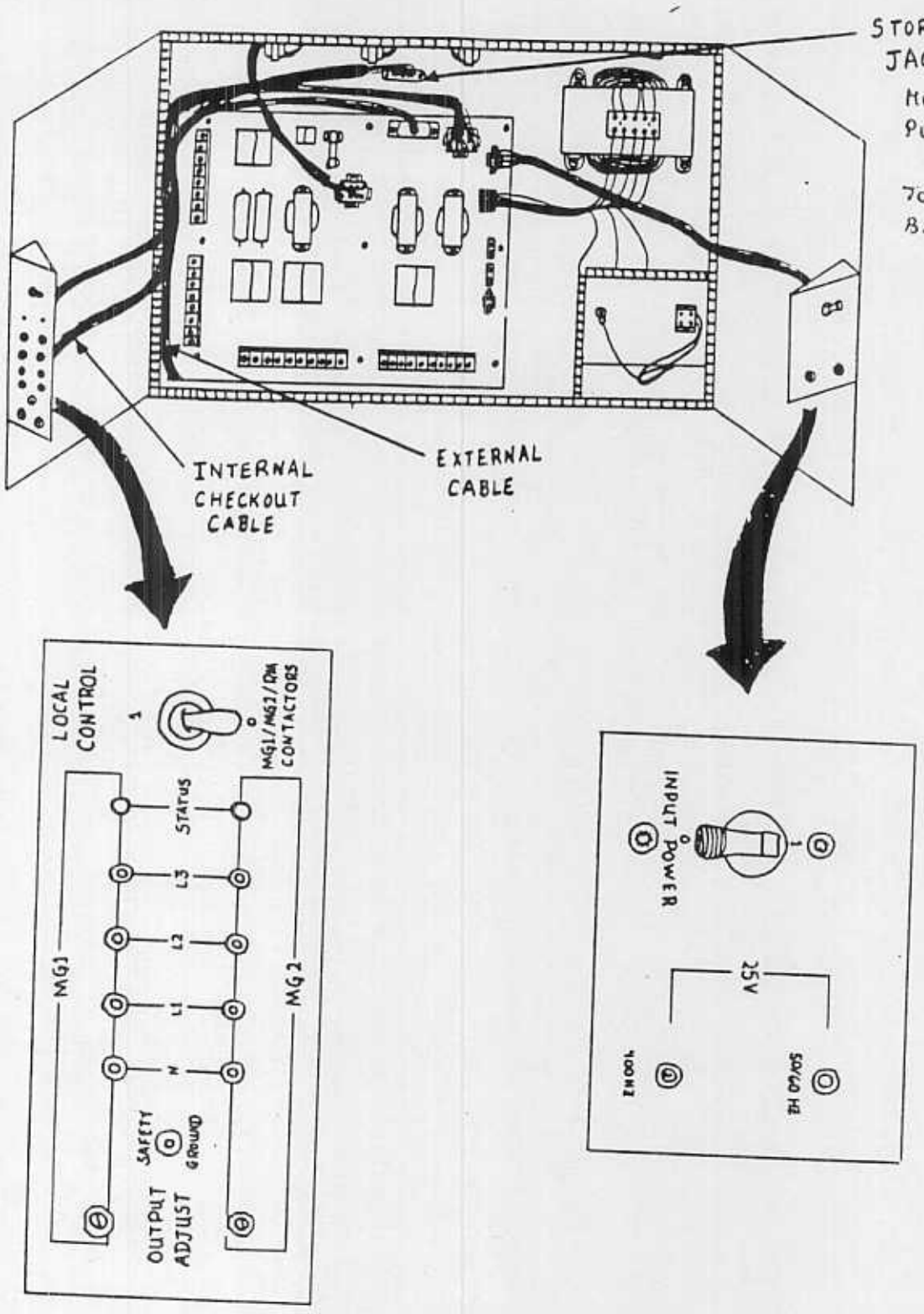
MG power input (customer hardwired)

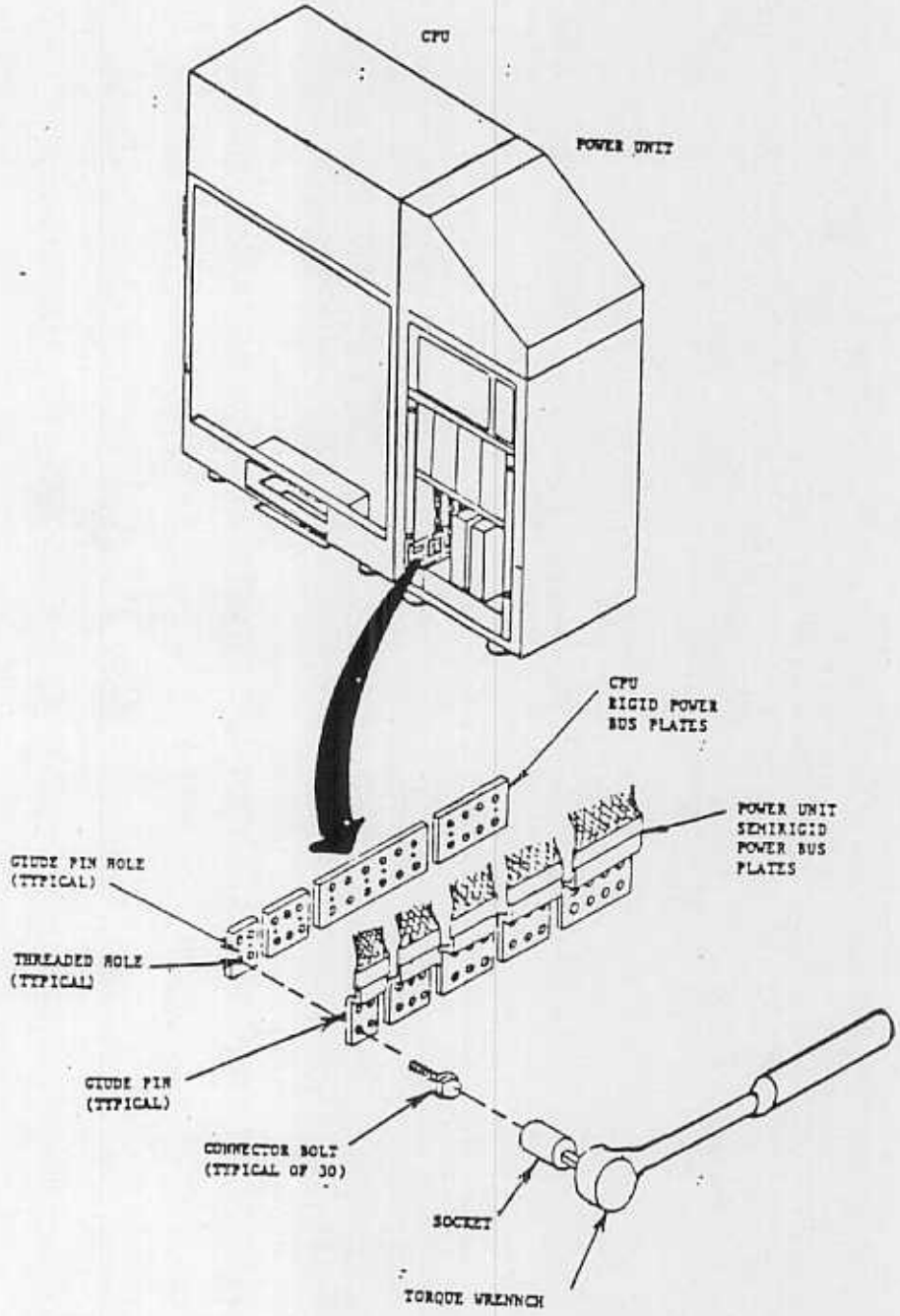
60 Hz	2.5A, 120v
50 Hz	1.5A, 220v
	1.5A, 240v

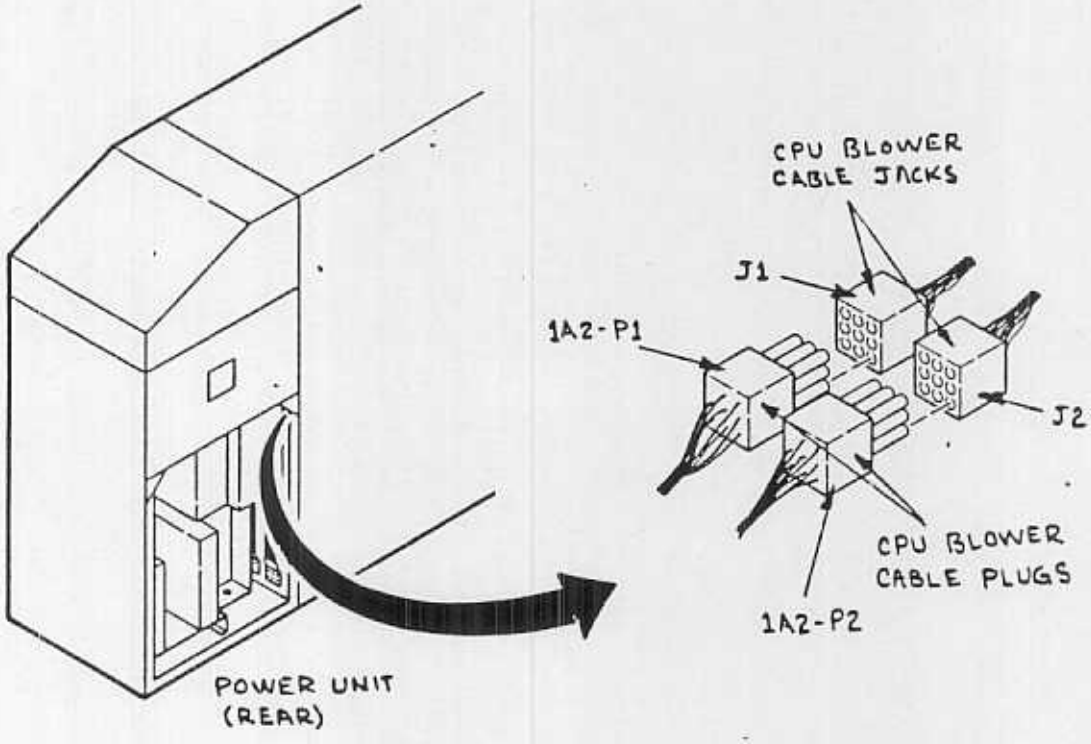


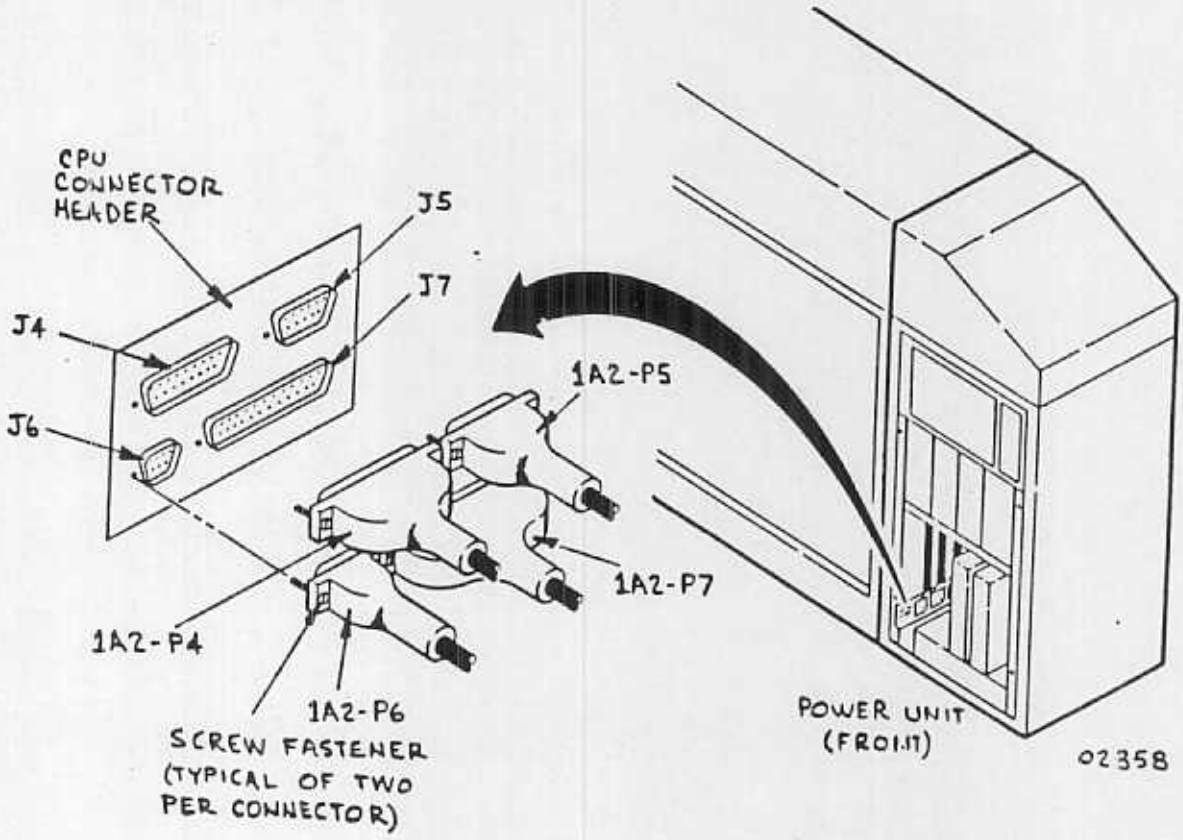


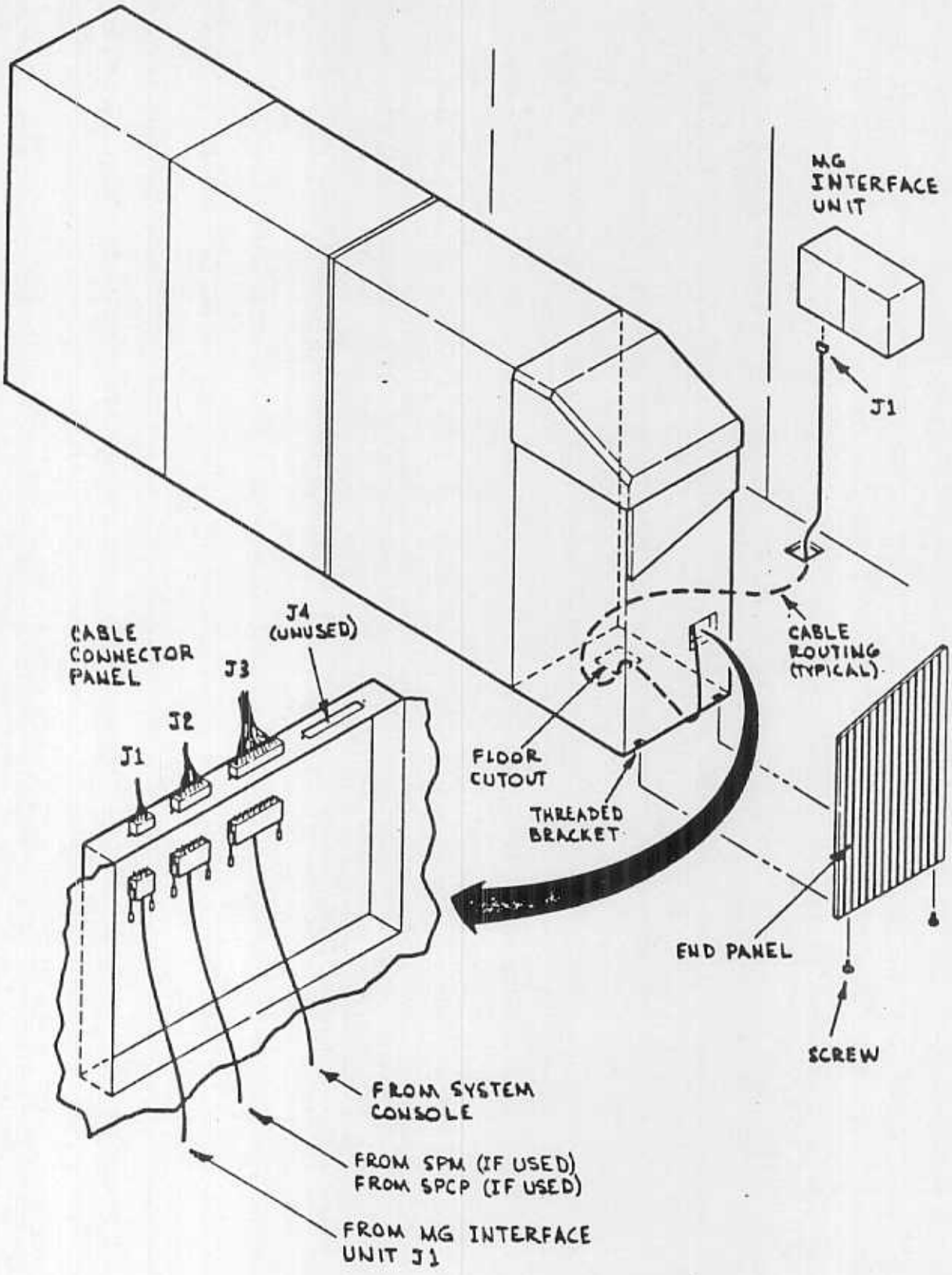
MG INTERFACE


STORAGE JACK
MG CHECKOUT PURPOSE
TO BE CONNECTED BELOW
INTERNAL CHECKOUT CABLE
EXTERNAL CABLE
LOCAL CONTROL
1
0
MG1/MG2/RM CONTACTORS
STATUS
L3
L2
L1
N
MG1
MG2
SAFETY GROUND
OUTPUT ADJUST
INPUT POWER
0
1
25V
TOOL
SERVO


CPU
POWER UNIT
CPU
RIGID POWER
BUS PLATES
POWER UNIT
SEMIRIGID
POWER BUS
PLATES
GUIDE PIN HOLE
(TYPICAL)
THREADED HOLE
(TYPICAL)
GUIDE PIN
(TYPICAL)
CONNECTOR BOLT
(TYPICAL OF 30)
SOCKET
TORQUE WRENNCH


CPU BLOWER
CABLE JACKS
J1
1A2-P1
J2
CPU BLOWER
CABLE PLUGS
1A2-P2
POWER UNIT
(REAR)


CPU
CONNECTOR
HEADER
J5
J7
J4
J6
1A2-P5
1A2-P7
1A2-P4
1A2-P6
SCREW FASTENER
(TYPICAL OF TWO
PER CONNECTOR)
POWER UNIT
(FRONT)
02358

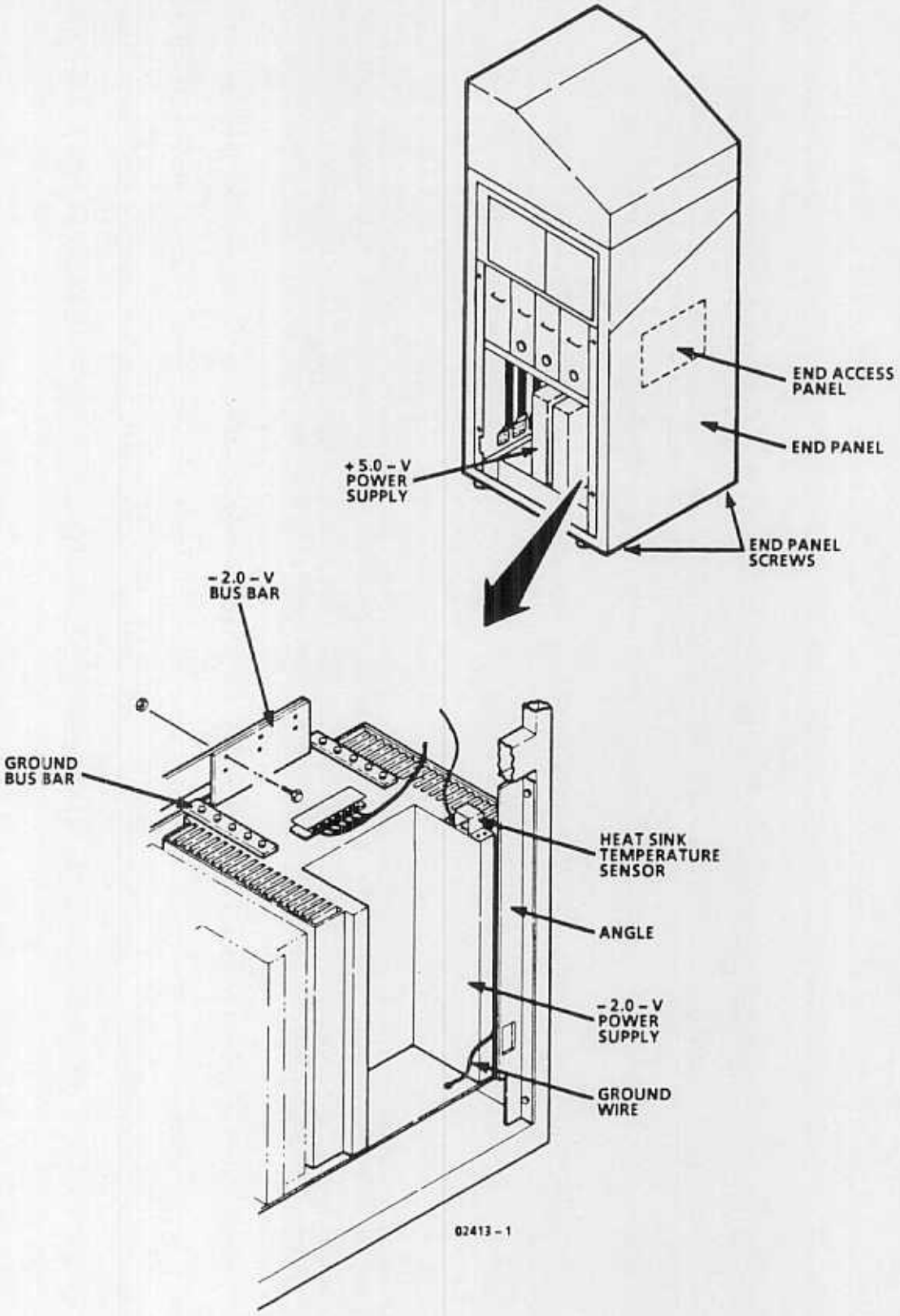

MG
INTERFACE
UNIT
J1
CABLE
CONNECTOR
PANEL
J4
(UNUSED)
J3
J2
J1
CABLE
ROUTING
(TYPICAL)
FLOOR
CUTOUT
THREADED
BRACKET
END PANEL
SCREW
FROM SYSTEM
CONSOLE
FROM SPM (IF USED)
FROM SPCP (IF USED)
FROM MG INTERFACE
UNIT J1

.POWER SUPPLIES
-4.5v
-2.0v
+5.0v
Aux bulk power supply

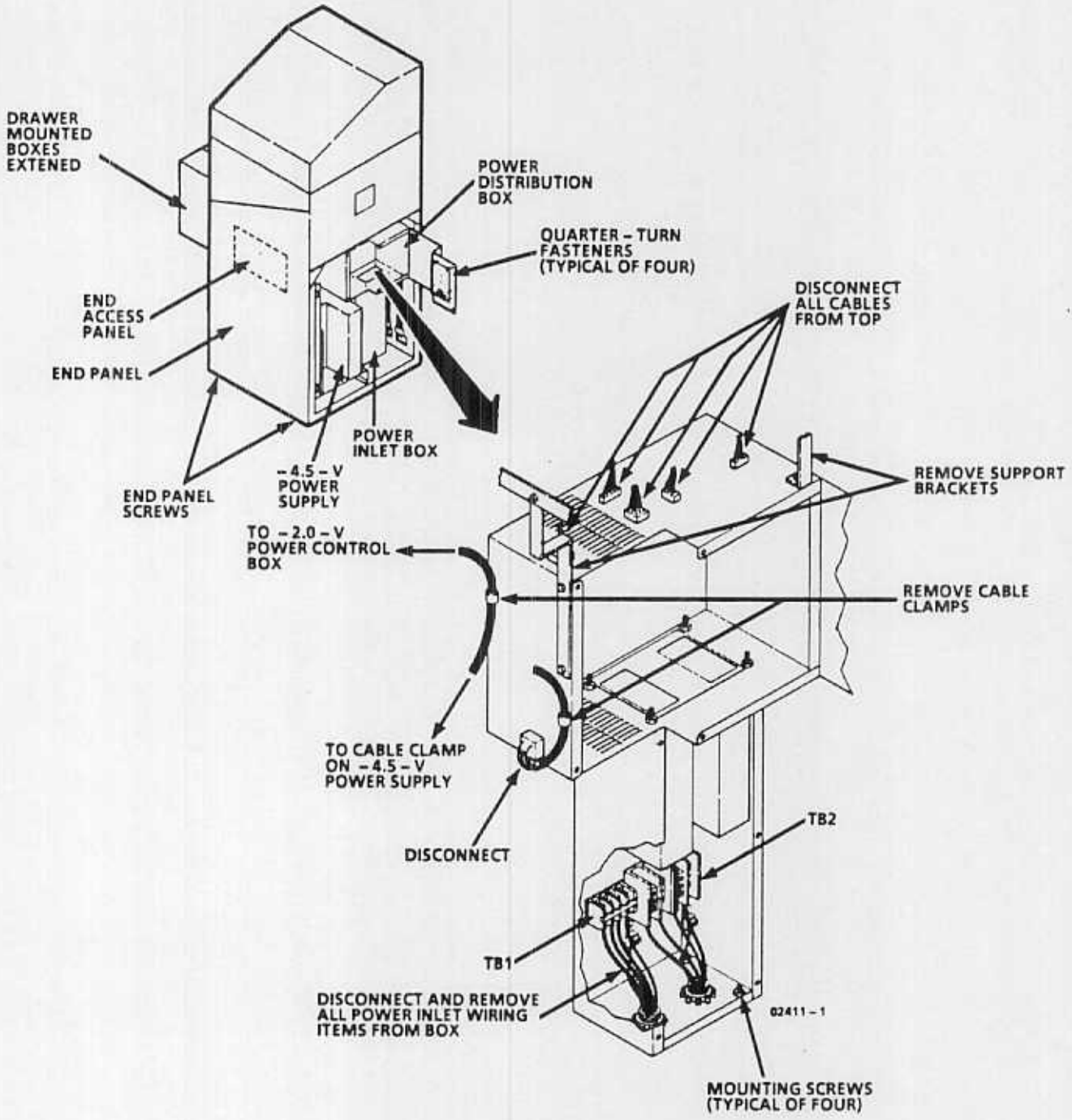
.PD/FILTER BOXES
Warning: PD/ filter boxez contain unswitched line voltage.

.TAP CHANGE PANEL
Blower rotation jumper

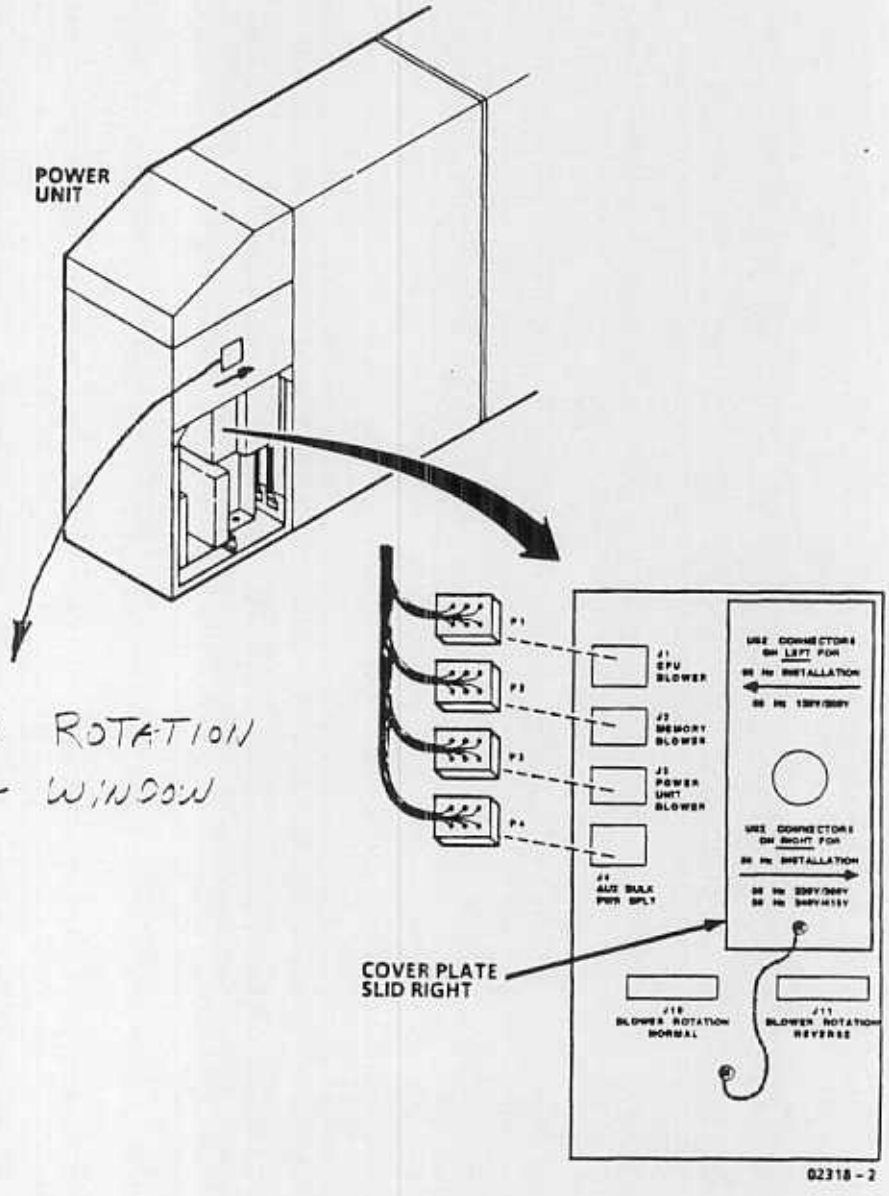
.AUX BULK POWER SUPPLY
Step down transformer
60/50 Hz isolation transformers for maintenance power
Maintenance power: +/- 25v
+ 5v (monitor system only)



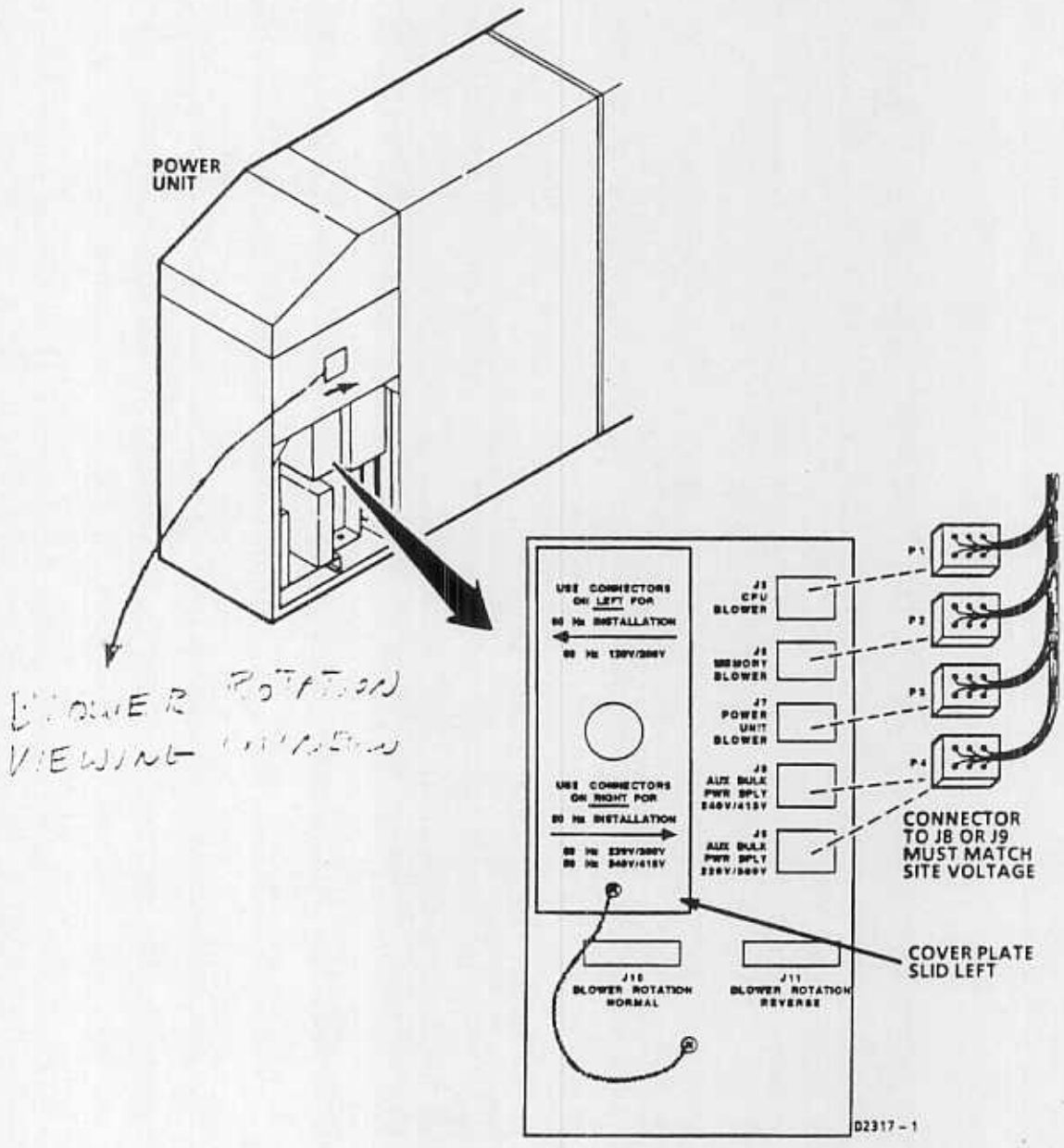
-2.0-V Power Supply



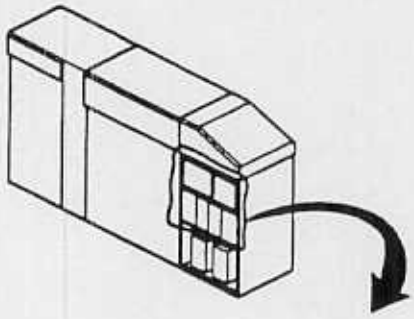
-4.5-V Power Supply

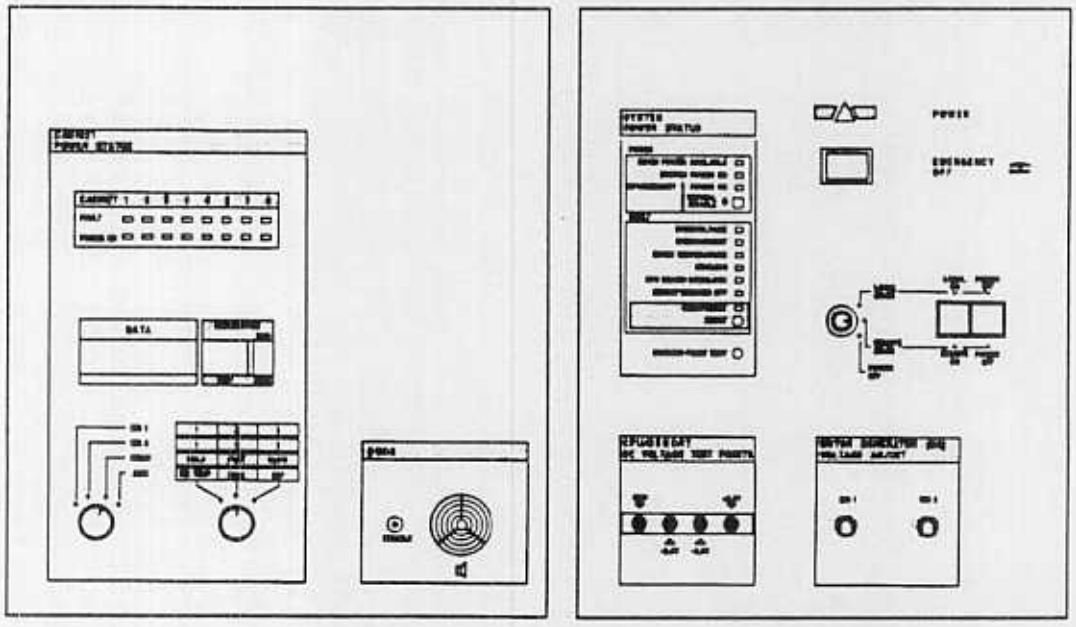


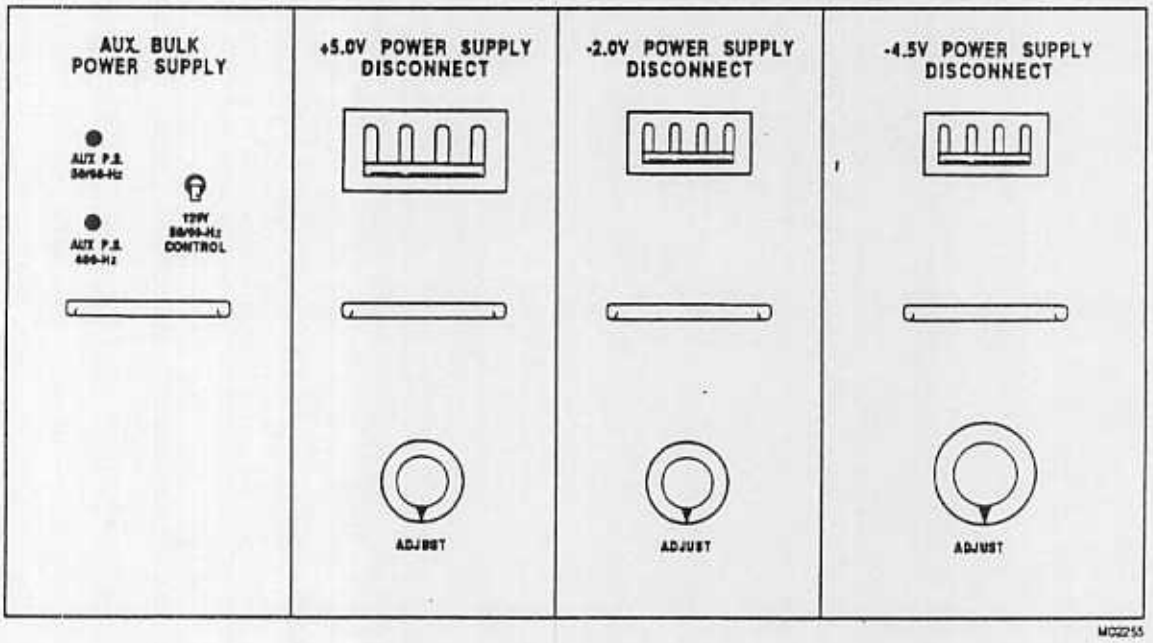
Power Unit 60-Hz Cable Connections



Power Unit 50-Hz Cable Connections






AUX. BULK
POWER SUPPLY
AUX P.S.
AUX P.S.
+5.0V POWER SUPPLY
DISCONNECT
ADJUST
-2.0V POWER SUPPLY
DISCONNECT
ADJUST
-4.5V POWER SUPPLY
DISCONNECT
ADJUST
MCG255

.POWER CONTROL BOX

Modules:

- Power control display
- Power control
- Switch
- Mux/display
- Monitor

.POWER MONITOR SYSTEM (left half of power control box)

Monitors power status only - both mainframe and IOU's.
Does not provide system control.
Fault codes isolate faults displayed on system power status LED's
i.e : Overcurrent LED lit, monitor can isolate to -2v CPU0 overcurrent or bad sense lead.
Allows monitoring of analog signals.
Note: If system goes down on a fault, do not press the reset button on the system status panel (right panel) until you have recorded all fault message.

.POWER CONTROL SECTION

-Turning on of input power disconnects:
- -Get green room power available light.
- -Get red press reset light.
- -Get red fault light if any faults present.

-Local on button pushed, local mode:
- -Starts timing sequence of MG starts, and room contactor starts via MG interface unit.

-Enabling CPU/CM (assume normal)
Push reset buttom (no fault LED's lit):
- -50/60 Hz power appliied to blowers.
- - -4.5v and -2.0v power applied to busses.
- - 5.0v applied to bus after short delay.
- -Get green power on light.
- -Get green indicator light.

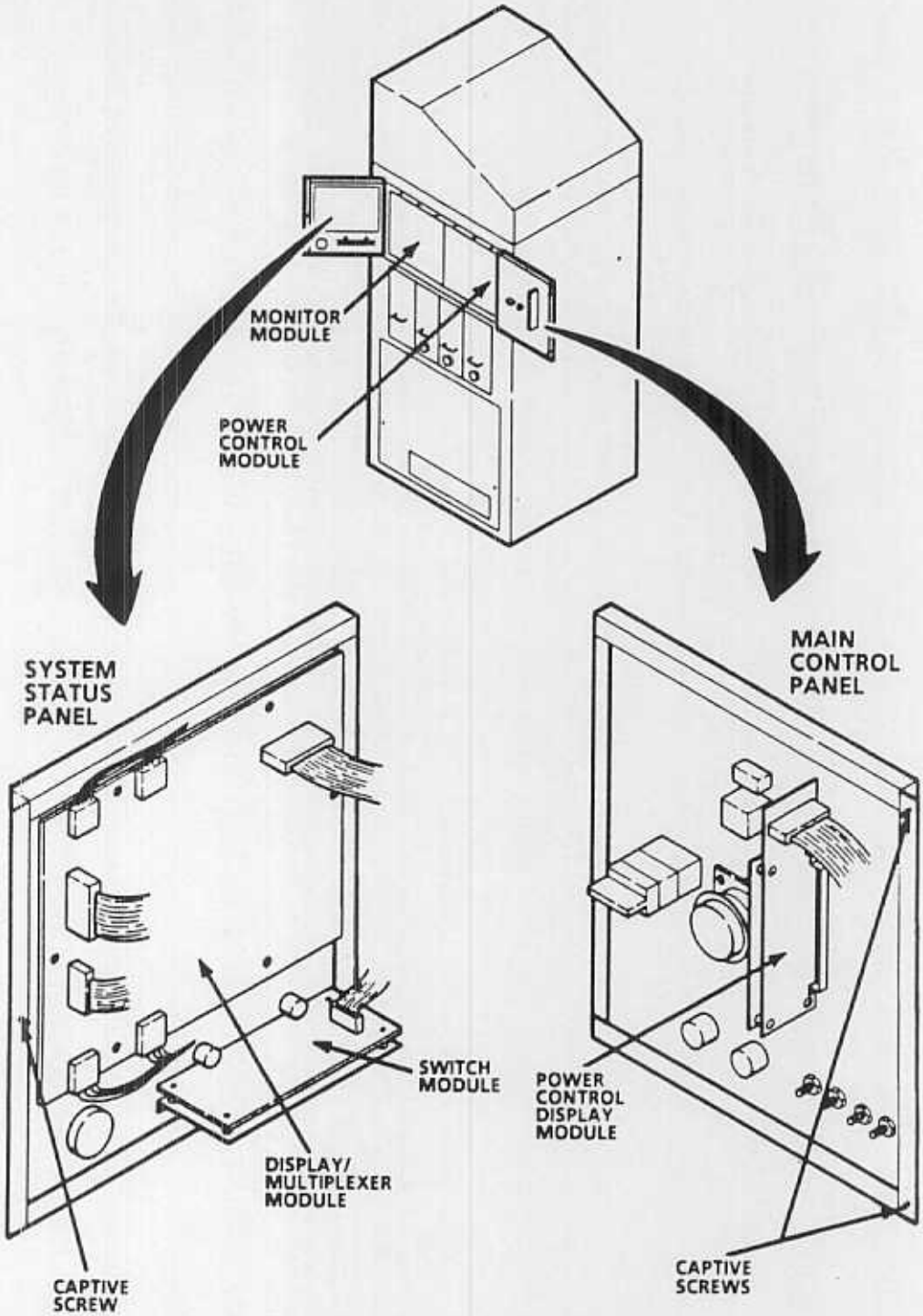
.DISABLE CPU/MEMORY (i.e to change logic board)

Move CPU.CM toggle switch to disable position. Do not use red power off button. Using the red power off button will shut down MG's and any controlled peripherals.

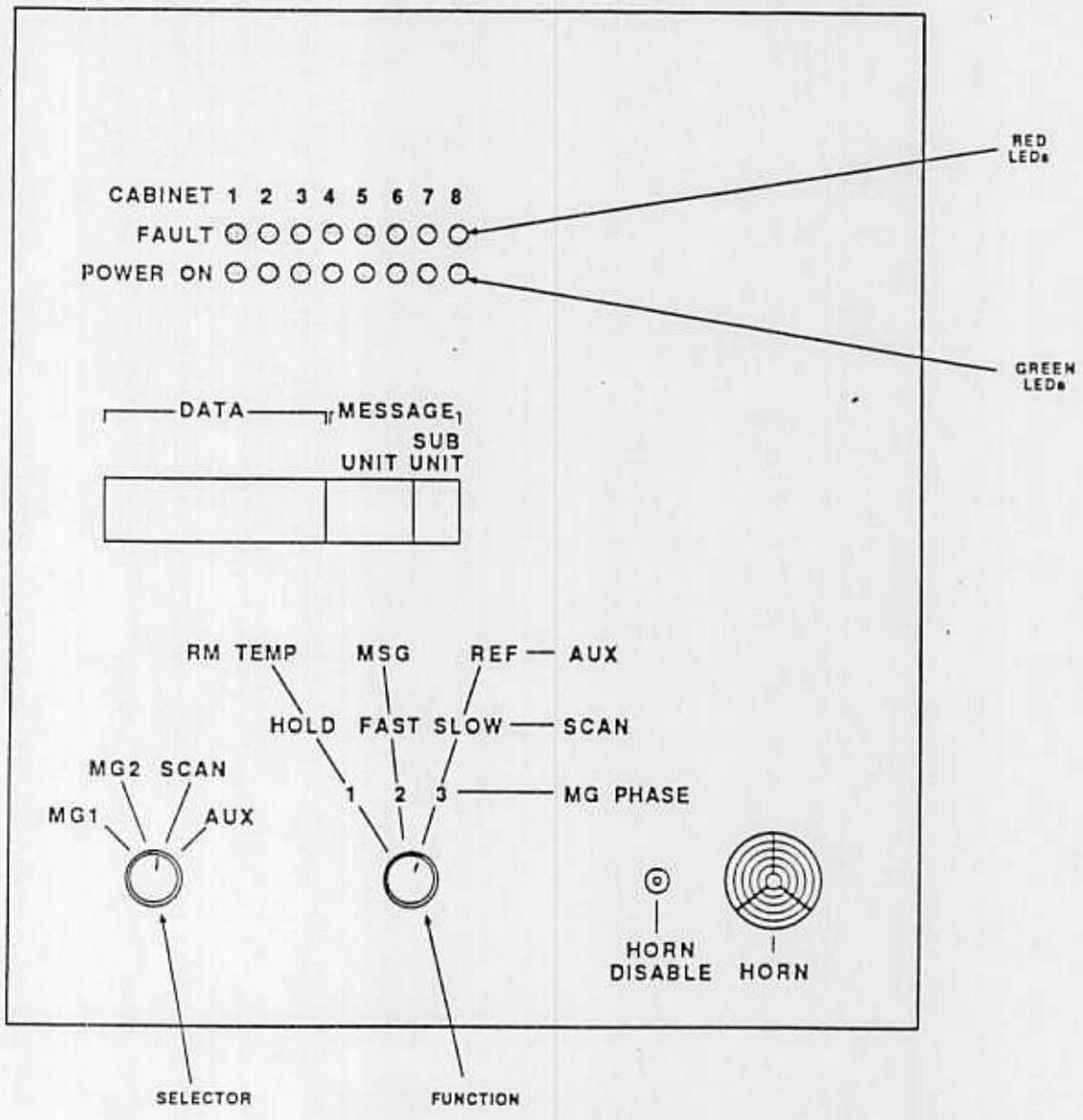
- -Green indicator light goes out.
- -Green CPU/CM power on LED goes out.
- -Removes logic and blower power.

.EMERGENCY POWER OFF

Presing the red emergency off button trips power unit main disconnects, resulting in:
- -Removal of all power to 960 mainframe power unit except for unswitched AC in PD box.
- -Disables all MG's and peripherals controlled by MG interface unit.
- -Disable signal to IOU's.

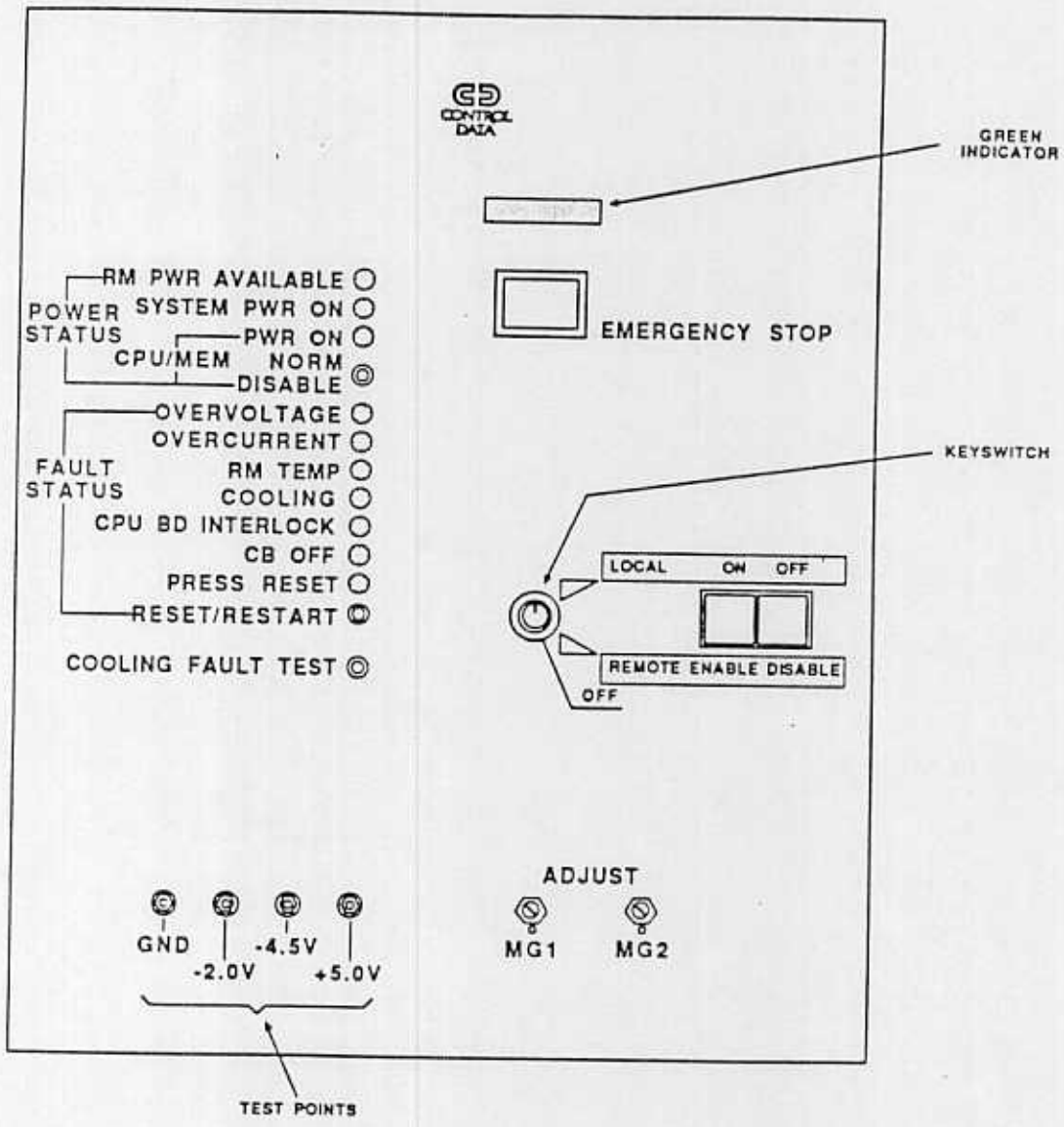

MONITOR MODULE
POWER CONTROL MODULE
SYSTEM STATUS PANEL
MAIN CONTROL PANEL
SWITCH MODULE
DISPLAY/ MULTIPLEXER MODULE
CAPTIVE SCREW
POWER CONTROL DISPLAY MODULE
CAPTIVE SCREWS

System Status Panel



Power-Unit System Status Panel

Main Control Panel



Power-Unit Main Control Panel

FAULTS

SYTEM FAULTS
- -MG status
- -Elevated room temperature .... above 93F

CPU/CM FAULTS
- -Overvoltage
  - -4.5v bus
  - -2.0v bus
  - +5.0v bus
- -Overcurrent
  - -4.5v bus
    - CPU 0
    - CPU 1
    - CM
  - -2.0v bus (sensed at regulators)
    - CPU 0
    - CPU 1
    - CM
  - +5.0v bus (sensed at regulators)
    - CM only

    Note: Overcurrent fault detects only gross bus overcurrent, "dead shorts". This is not current transient proctection and won't detect intermittent shorts such as to a touching scope probe ground to a bus voltage.
- -Room Temperature

  Fault results when average of CPU and CM ambients exceeds:

  89F EEW (early environmemtal warning) no shutdown
  93F LW 2 minutes to shutdown
- -Cooling
  - Blower SW 2.5 seconds to shutdown
  - Power unit
  - CPU
  - CM
- - Shunt: EEW, LW, SW
  - CPU 0
  - CPU 1
- -CPU outlet SW
  - CPU 0
  - CPU 1

  Relative trip level. Trips when outlet temperature minus CPU ambient temperature exceeds 32F.
- -CM outlet SW
  - Memory 1
  - Memory 2
  - Release airflow

  Memory 1 and 2. Trips when outlet temp minus ambient temperature exceeds 32F.

  Reverse airflow. Trips when reverse airflow sensor temperature minus memory ambient temperature exceeds 14F.

Table 4-1. Two-Character Coded Fault Messages

Code Displayed in MESSAGE	Type Warning	Fault
00	LW (2 min)	Invalid temperature indication from −2.0 V power supply heat sink sensor in power unit.[1,2]
03	LW (2 min)	Invalid temperature indication from −4.5 V power supply heat sink sensor in power unit.[1,2]
06	LW (2 min)	Invalid temperature indication from CP-0 shunt sensor in CPU cabinet.[1,2]
09	LW (2 min)	Invalid temperature indication from CP-1 shunt sensor in CPU cabinet.[1,2]
0C	SW	Invalid temperature indication from CP-0 outlet sensor in CPU cabinet.[1,2]
0F	SW	Invalid temperature indication from CP-1 outlet sensor in CPU cabinet.[1,2]
12	SW	Invalid temperature indication from memory 1 outlet sensor in CPU cabinet.[1,2]
15	LW (2 min)	Temperature at −2.0-V power supply heat sink in power unit exceeds 93°C (200°F).[2]
18	LW (2 min)	Invalid temperature indication from memory 2 outlet sensor in CPU cabinet.[1,2]
1b	LW (2 min)	Invalid temperature indication from CP ambient sensor in CPU cabinet.[1,2]
1E	LW (2 min)	Invalid temperature indication from CM ambient sensor in CPU cabinet.[1,2]
21	LW (2 min)	Invalid temperature indication from reverse air flow sensor in CPU cabinet.[1,2]
27	LW (2 min)	Temperature at −4.5 V power supply heat sink in power unit exceeds 93°C (200°F).[2]

Notes:

1. Reading from sensor is out of acceptable range of −4° to 121°C (25° to 250°F).

2. Results in an emergency shutdown of logic voltages to CPU cabinet if fault continues to end of warning time.

(Continued)

Table 4-1. Two-Character Coded Fault Messages *(Continued)*

Code Displayed in MESSAGE	Type Warning	Fault
2A	EEW	Temperature at CP-0 shunt sensor in CPU cabinet exceeds 55°C (131°F).
2d	LW (2 min)	Temperature at CP-0 shunt sensor in CPU cabinet exceeds 60°C (140°F).[1]
30	SW	Temperature at CP-0 shunt sensor in CPU cabinet exceeds 63°C (145°F).[1]
33	EEW	Temperature at CP-1 shunt sensor in CPU cabinet exceeds 55°C (131°F).
36	LW (2 min)	Temperature at CP-1 shunt sensor in CPU cabinet exceeds 60°C (140°F).[1]
39	SW	Temperature at CP-1 shunt sensor in CPU cabinet exceeds 63°C (145°F).[1]
3C	EEW	Temperature of room ambient air exceeds 32°C (89°F).[2]
3F	LW (2 min)	Temperature of room ambient air exceeds 34°C (93°F).[2,3]
42	SW	CP-0 outlet temperature exceeds CP ambient temperature by more than 18°C (32°F).[1]
45	SW	CP-1 outlet temperature exceeds CP ambient temperature by more than 18°C (32°F).[1]
48	SW	Memory 1 outlet temperature exceeds CM ambient temperature by more than 18°C (32°F).[1]
4b	SW	Memory 2 outlet temperature exceeds CM ambient temperature by more than 18°C (32°F).[1]
4E	SW	Reverse air flow temperature exceeds CM ambient temperature by more than 7°C (14°F).[1]

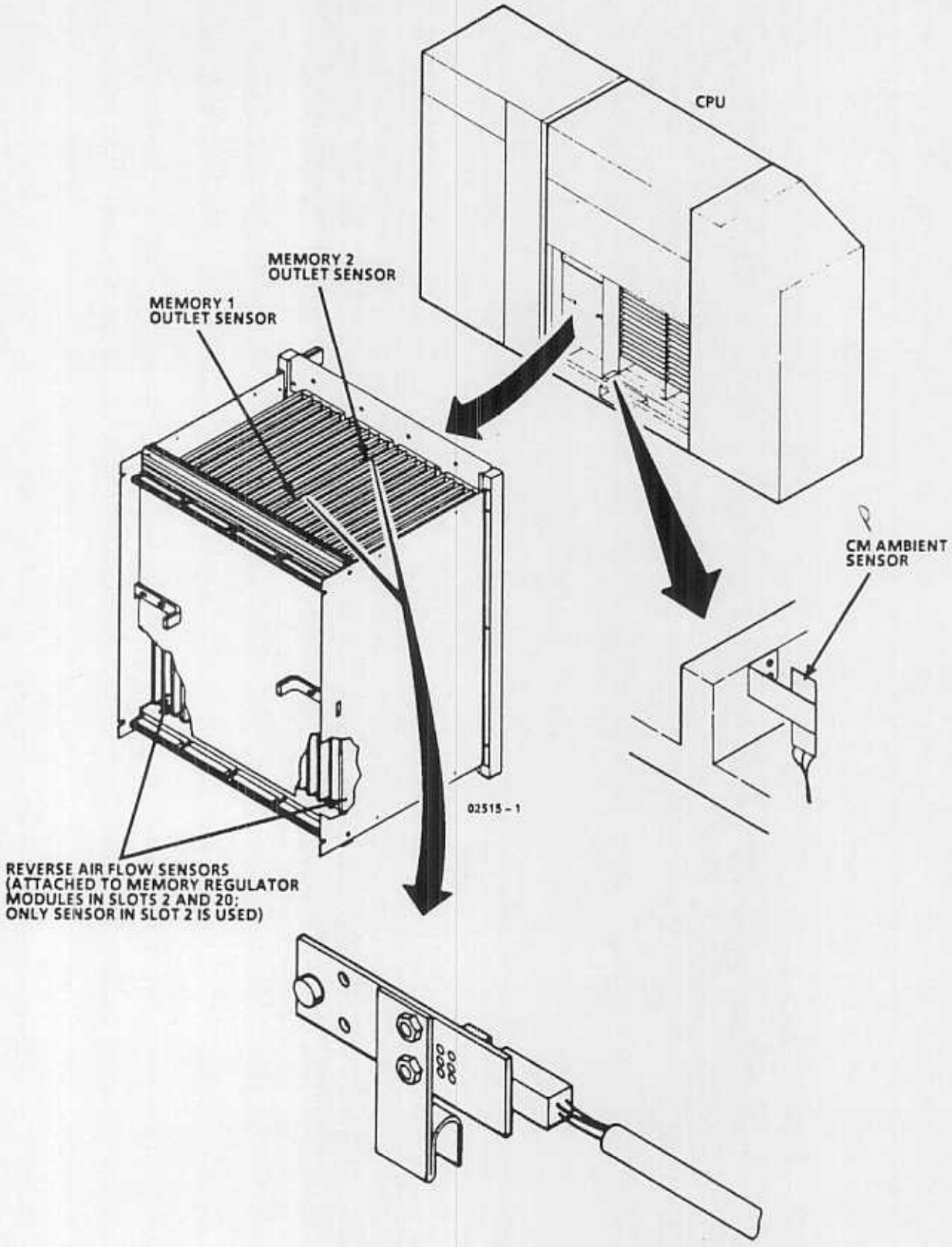
Notes:

1. Results in an emergency shutdown of logic voltages to CPU cabinet if fault continues to end of warning time.

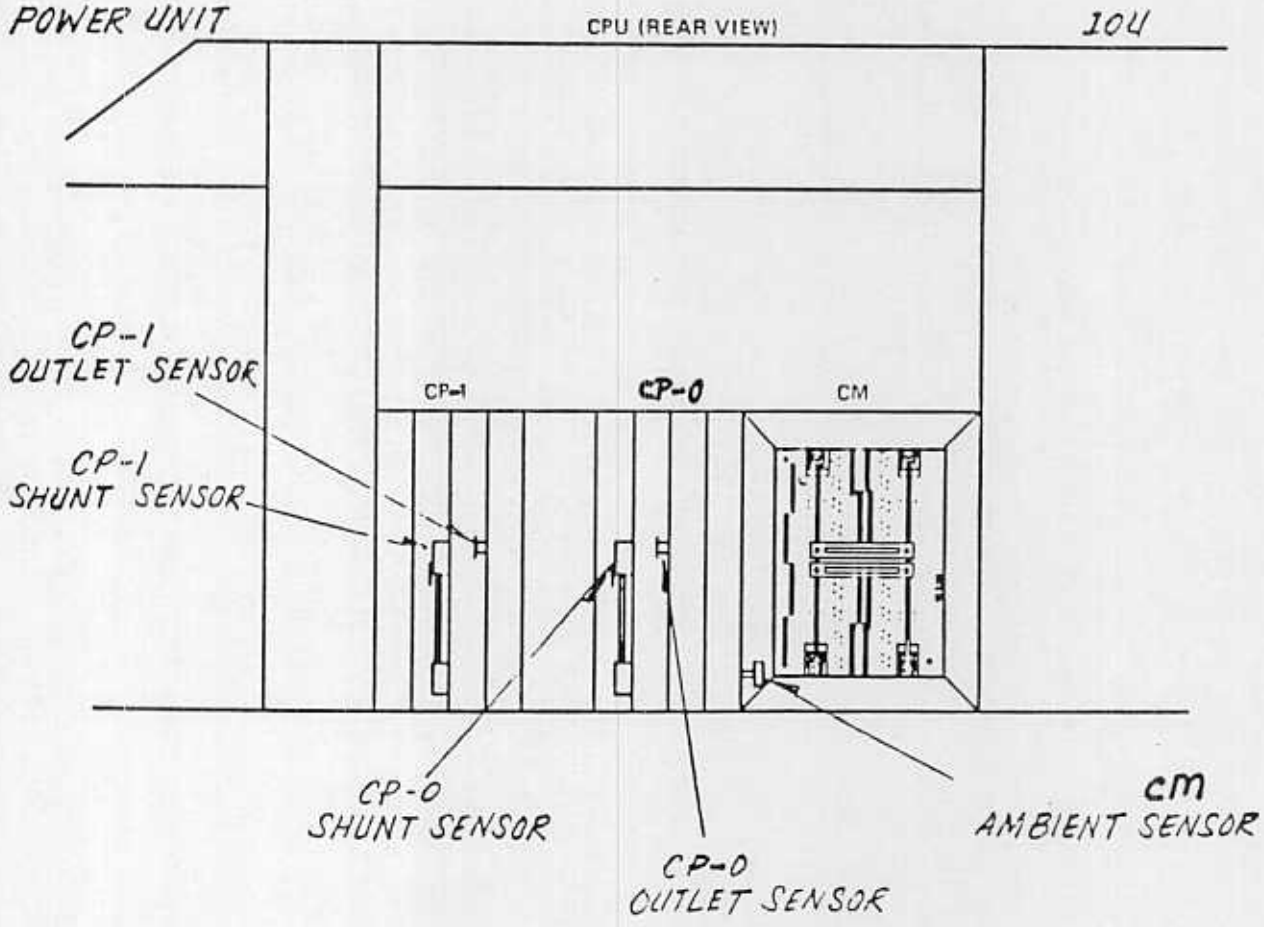
2. Temperature of room ambient air is average between temperatures from CP and CM ambient sensors.

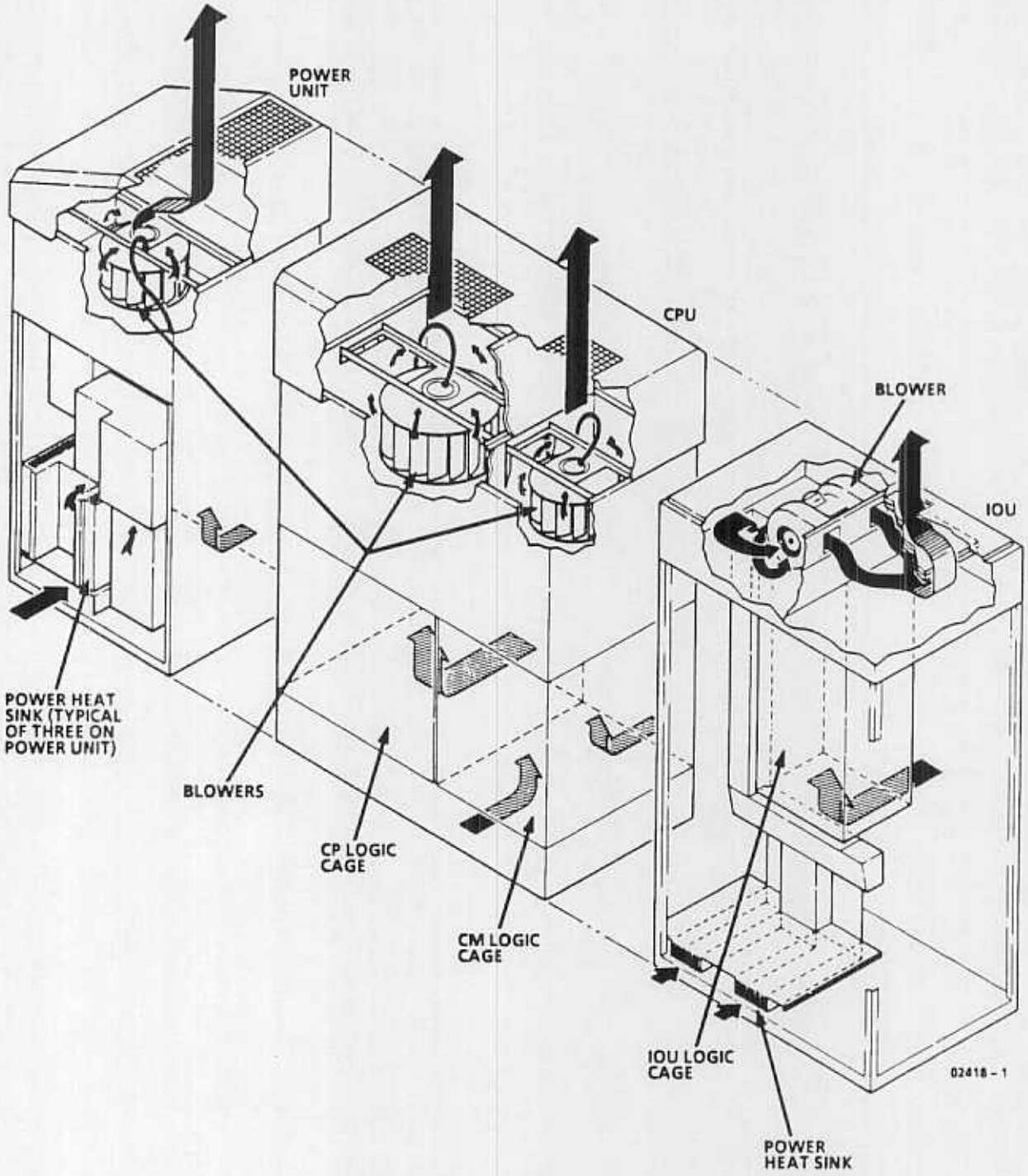
3. Results in an emergency shutdown of system if fault continues to end of warning time.

(Continued)

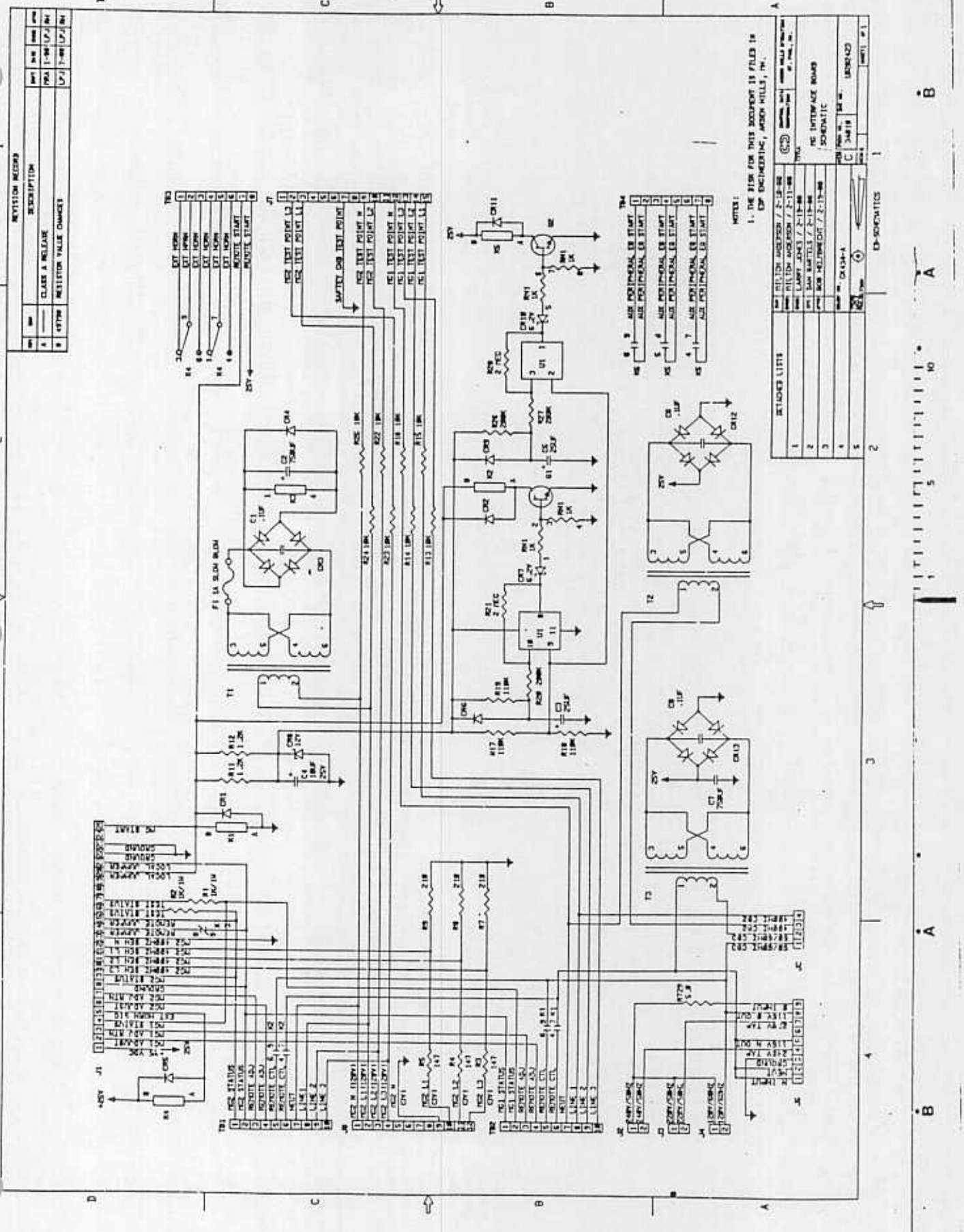


Locations of Temperature Sensors in CPU Cabinet (Front)


POWER UNIT
CPU (REAR VIEW)
104
CP-1
OUTLET SENSOR
CP-1
SHUNT SENSOR
CP-1
CP-0
CM
CP-0
SHUNT SENSOR
CP-0
OUTLET SENSOR
CM
AMBIENT SENSOR

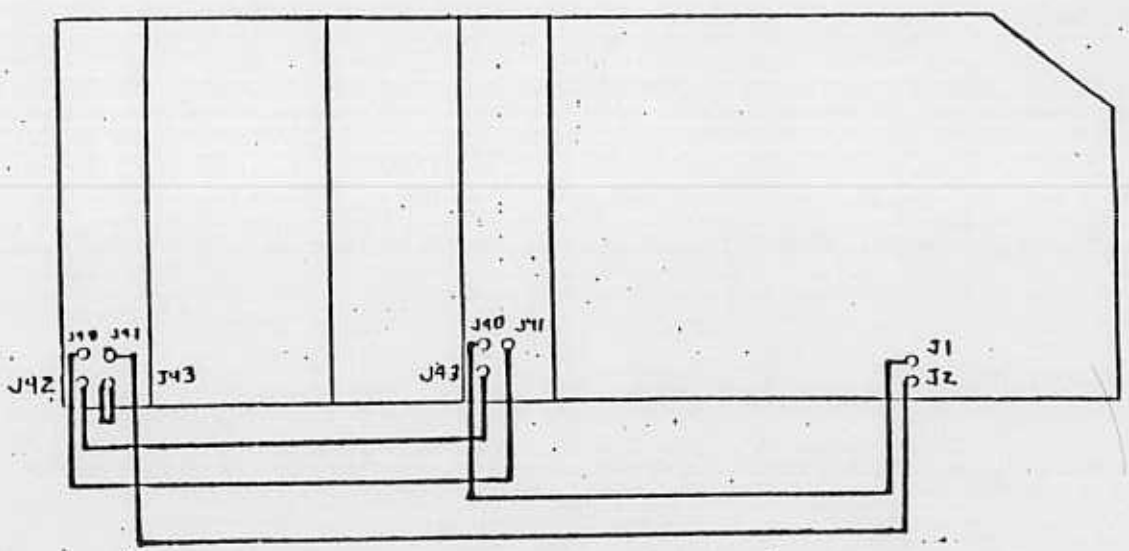


Mainframe Air Flow

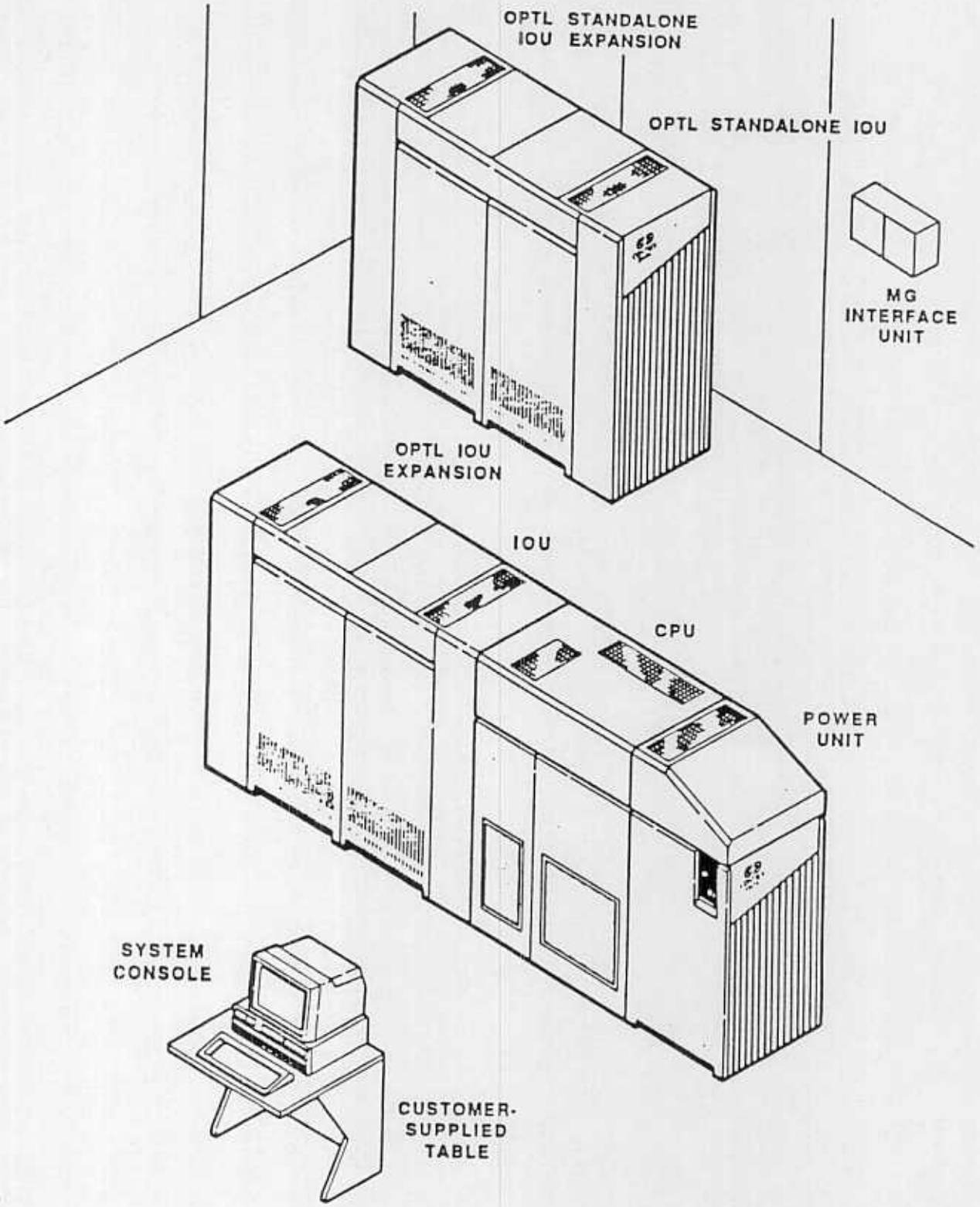


Warning Cables

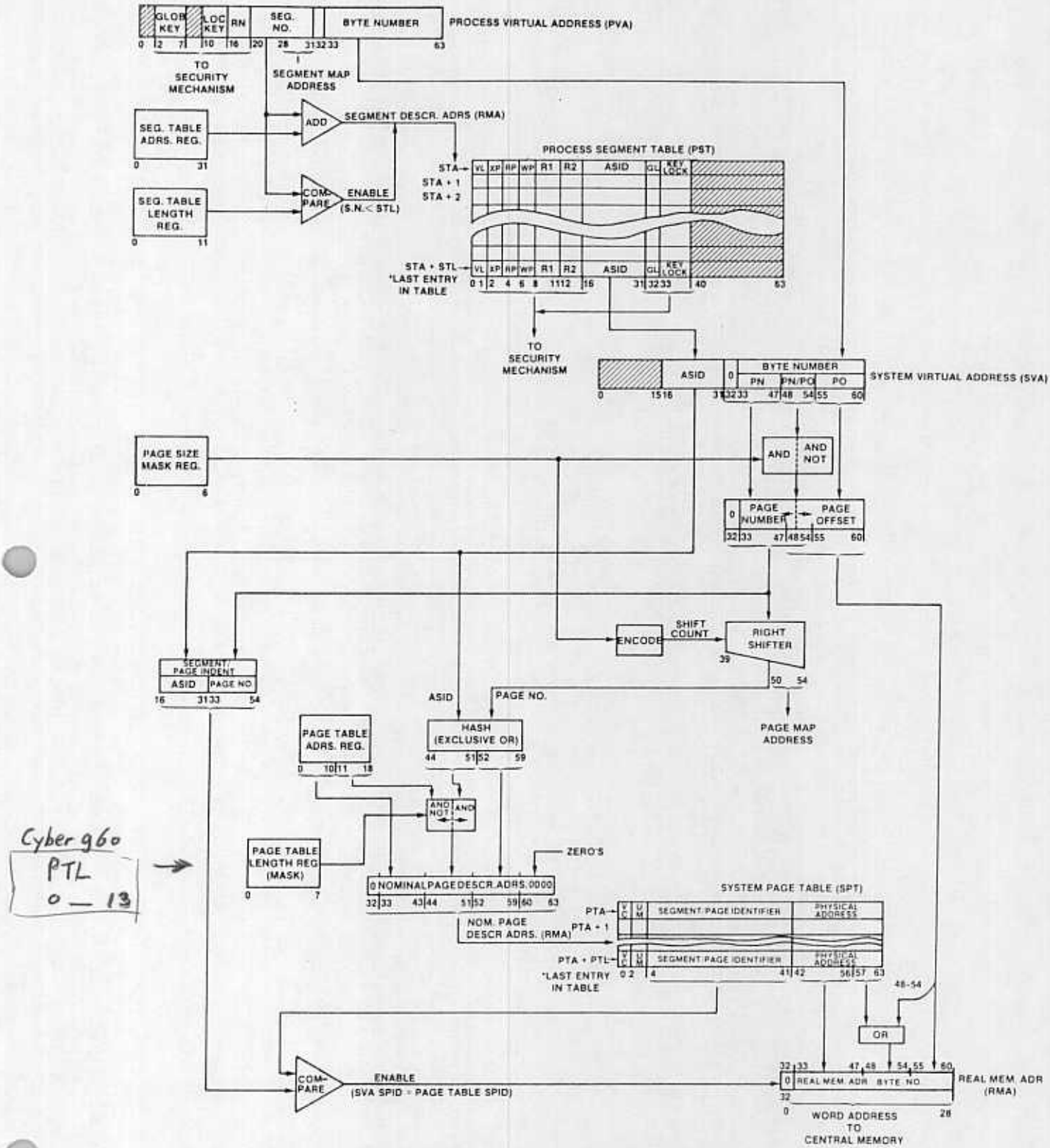
10 Ft Cable =	53615356	(J1 to J40) (J41 to J40) (J42 to J43)
50 Ft Cable =	53615357	(J41 to J2)
TERMINATOR =	23102122	(J43)



J1 = REM START / S.W. OUT
J40 = REM START / S.W. IN
J41 = REM START / S.W. OUT
J42 = L.W. IN
J43 = L.W. OUT
J2 = REM START / S.W. IN

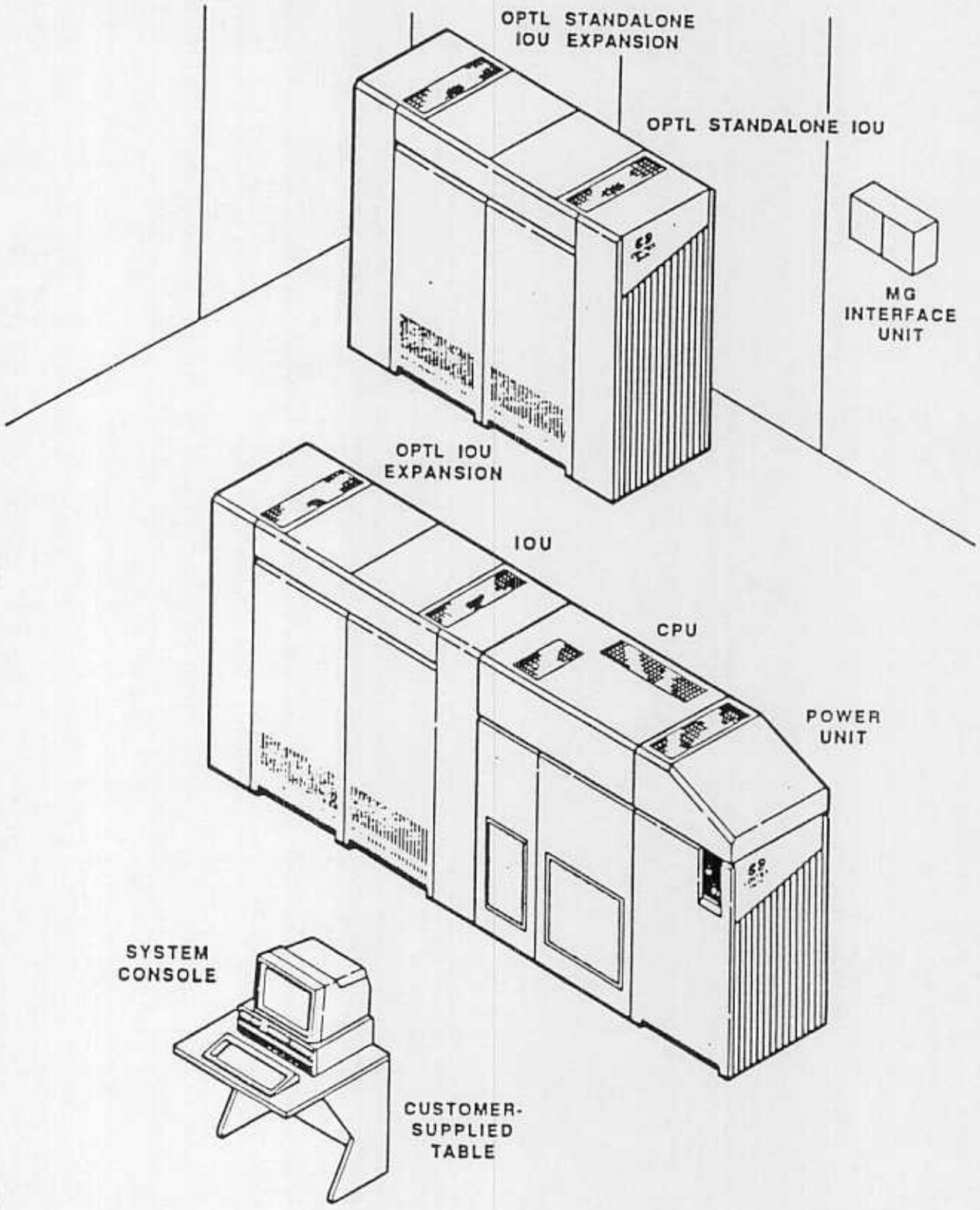


VIRTUAL ADDRESSING MECHANISM



Cyber 960
PTL
0 — 13

CYBER 180
VIRTUAL TO REAL ADDRESS CONVERSION



CLOCK SYSTEM

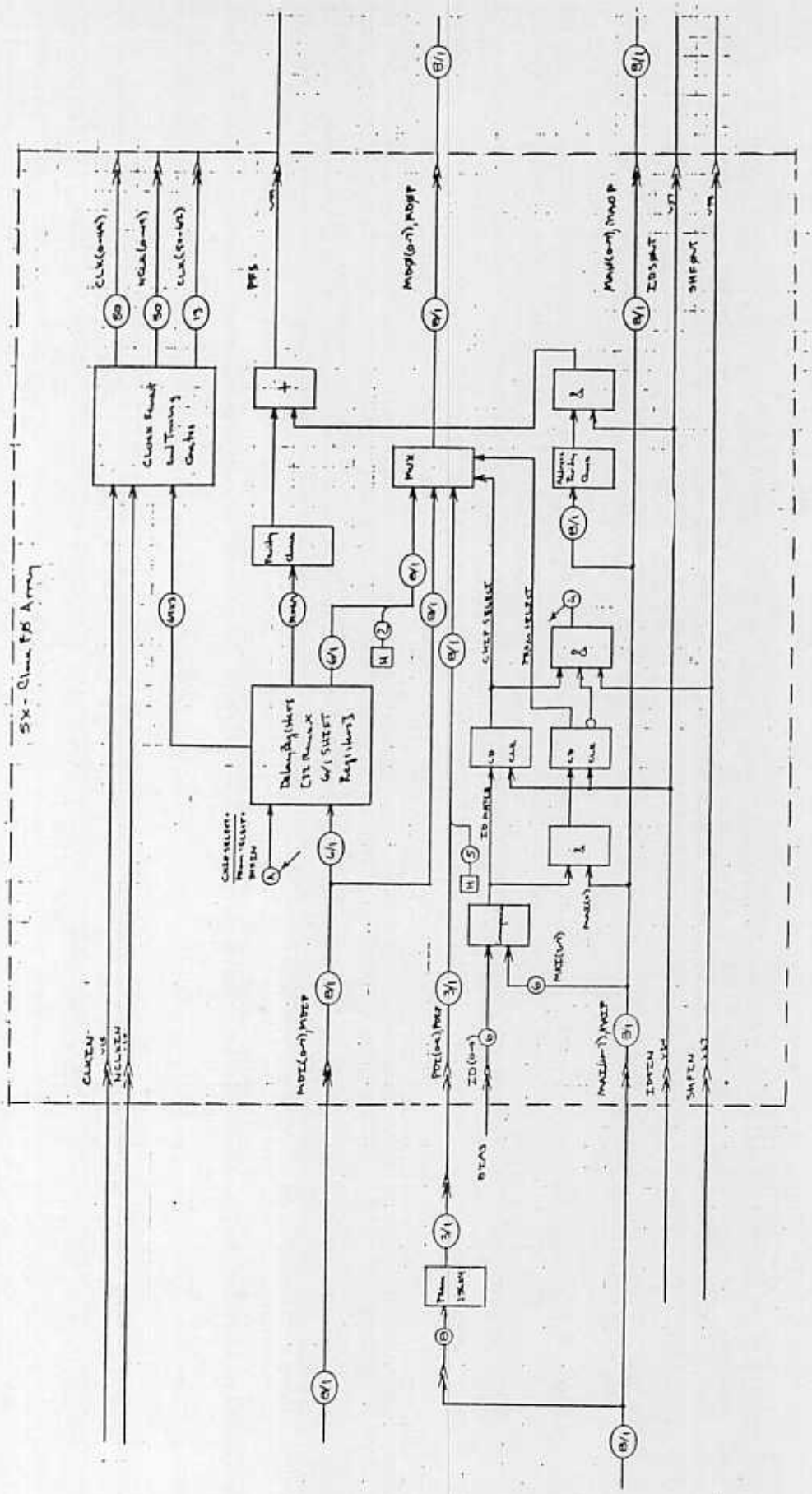
CLOCK SYSTEM

COMPONENTS:

- OSCILLATORS, 11.2NS, 11.0NS, 11.4NS, AND 62.5NS
- 6GMH MASTER CLOCK ARRAY (FGE)
- 6JXH WORKING RANK FANOUT ARRAY (FGE)
- MAC ADDRESS AND DATA BUS

FEATURES:

- SUPPLIES MINOR AND MAJOR CYCLE TIMING FOR:
  - . CENTRAL MEMORY (CM)
  - . CENTRAL MEMORY CONTROL (CMC)
  - . I4 CENTRAL MEMORY INTERFACE (CMI)
  - . BOTH CENTRAL PROCESSORS (CPU0 AND CPU1)
- SUPPLIES A ONE MICRO-SECOND TICK FOR THE CMC AND BOTH CPU0 AND CPU1 FOR TIMER SYNCHRONIZATION.
- PROVIDES ELECTRONIC TUNING TO PROVIDE FOR THE MINIMIZING OF CLOCK SKEW IN THE SYSTEM.
- PROVIDES A PROM FOR THE STORING OF CLOCK TUNING INFORMATION ON AN INDIVIDUAL CP-BOARD BASIS.
- PROVIDES A UNIFORM INTERFACE TO FACILITATE CP-BOARD TUNING IN A MANUFACTURING CLOCK FIXTURE.
- CLOCK INITIALIZATION VIA CTI.



2nd STAGE CLOCK ARRAY

CLOCK RELATED MAC FUNCTIONS

- CLOCK CHIP SELECTION
  - FUNCTION CODE = 2
  - TYPE CODE = 2
  - CHIP STAYS SELECTED UNTIL ANOTHER CHIP IS SELECTED
  - DISABLES THE MAC BUS

- PROM READ
  - FUNCTION CODE = 4
  - TYPE CODE = 2
  - BEGINNING PROM ADDRESS SPECIFIED BY CONTROL WORD 2
  - PROM CONTAINS 3 BITS OF DATA PLUS PARITY PER ENTRY
  - 256 ENTRIES , 64 ENTRIES REQUIRED FOR 64 CLOCK CONTROLS PER CLOCK CHIP

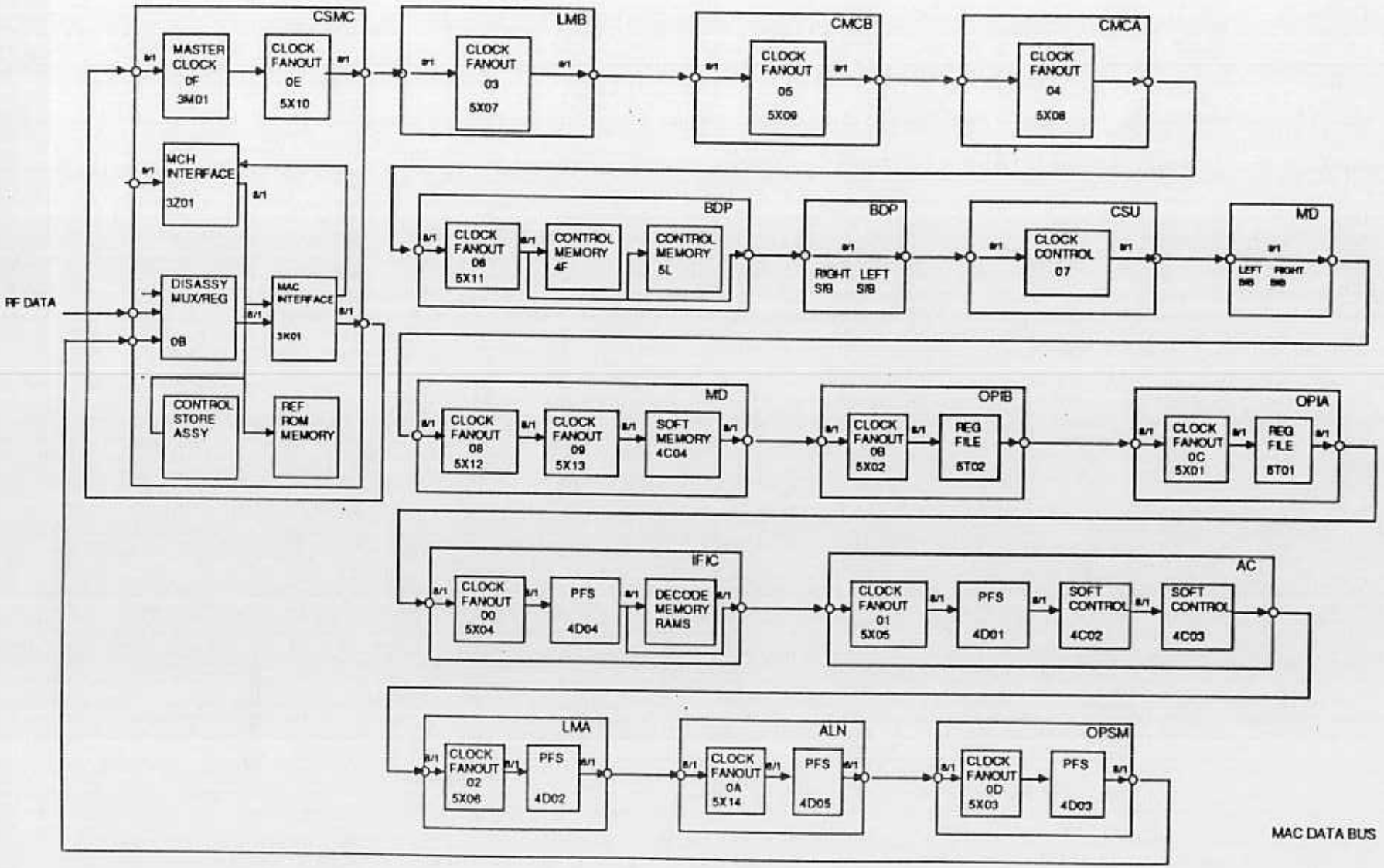
- DELAY REGISTER LOAD
  - FUNCTION CODE = 5
  - TYPE CODE = 2
  - LOAD DATA IS 6 BITS WIDE, 32 RANKS DEEP

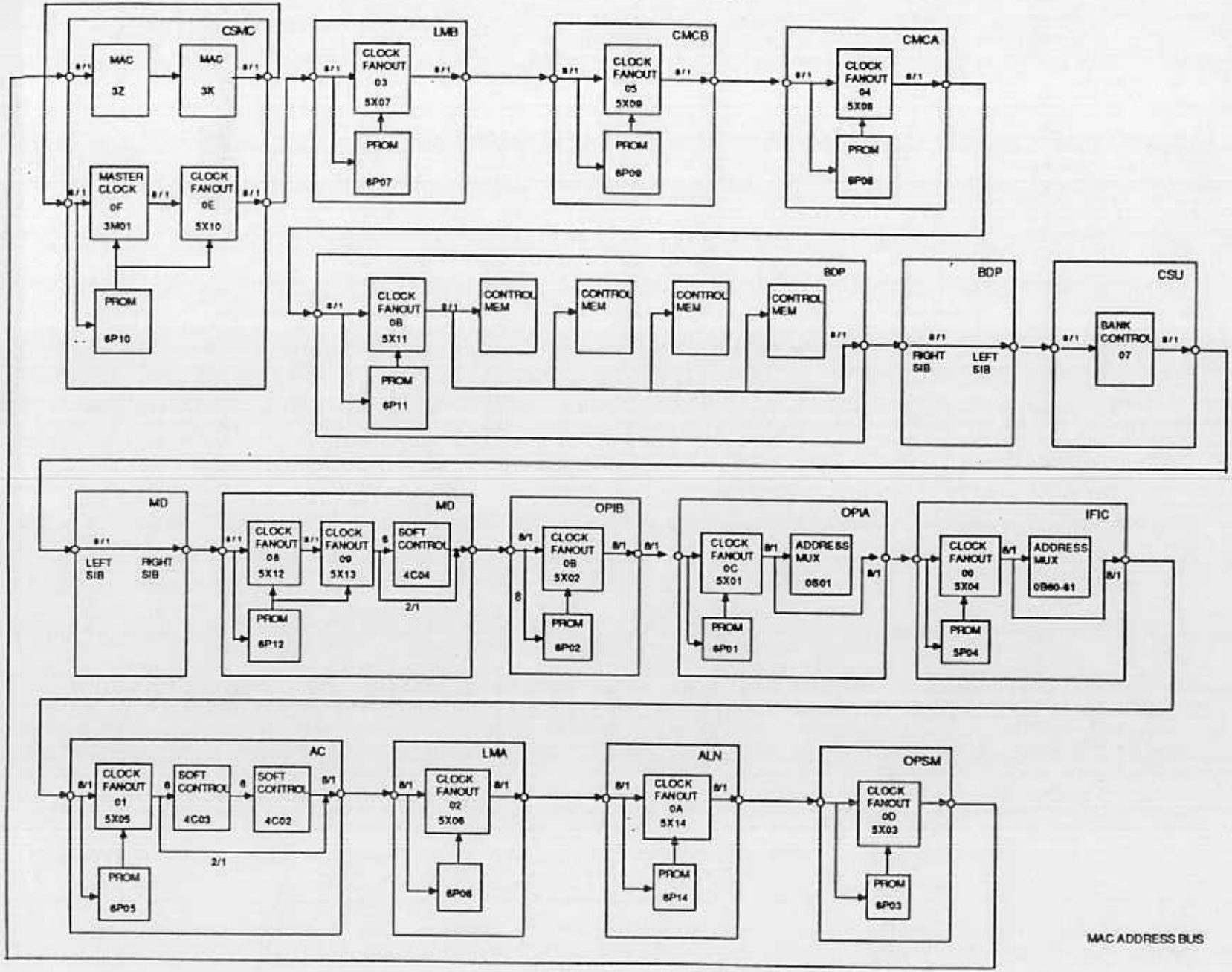
- DELAY REGISTER READ (MAINTENANCE FEATURE)
  - FUNCTION CODE = 4
  - TYPE CODE = 2
  - TYE READ IS DESTRUCTIVE
  - DATA IS 6 BITS WIDE, 32 RANKS DEEP

- ADDRESS AND DELAY REGISTER PARITY CHECK

CLOCK INITIALIZATION VIA CTI

- READS THE PROM DATA FOR EACH CP BOARD
- FORMATS THE PROM DATA INTO DELAY REGISTER DATA
- LOADS THE DELAY REGISTERS IN EACH CLOCK FANOUT ARRAY WITH THE PROM DATA
- CHECKS STATUS TO ASSURE GOOD LOAD


CSMC
MASTER CLOCK 0F 3M01
CLOCK FANOUT 0E 5X10
MCH INTERFACE 3Z01
DISASSY MUX/REG 0B
MAC INTERFACE 3K01
CONTROL STORE ASSY
REF ROM MEMORY
RF DATA
LMB
CLOCK FANOUT 03 5X07
CMCB
CLOCK FANOUT 05 5X09
CMCA
CLOCK FANOUT 04 5X08
BDP
CLOCK FANOUT 06 5X11
CONTROL MEMORY 4F
CONTROL MEMORY 5L
BDP
RIGHT S/B
LEFT S/B
CSU
CLOCK CONTROL 07
MD
LEFT S/B
RIGHT S/B
MD
CLOCK FANOUT 08 5X12
CLOCK FANOUT 09 5X13
SOFT MEMORY 4C04
OPIB
CLOCK FANOUT 0B 5X02
REG FILE 5T02
OPIA
CLOCK FANOUT 0C 5X01
REG FILE 5T01
IFIC
CLOCK FANOUT 00 5X04
PFS 4D04
DECODE MEMORY RAMS
AC
CLOCK FANOUT 01 5X05
PFS 4D01
SOFT CONTROL 4C02
SOFT CONTROL 4C03
LMA
CLOCK FANOUT 02 5X06
PFS 4D02
ALN
CLOCK FANOUT 0A 5X14
PFS 4D05
OPSM
CLOCK FANOUT 0D 5X03
PFS 4D03
MAC DATA BUS


CSMC
MAC 3Z
MAC 3K
MASTER CLOCK 0F 3M01
CLOCK FANOUT 0E 5X10
PROM 6P10
LMB
CLOCK FANOUT 03 5X07
PROM 6P07
CMCB
CLOCK FANOUT 05 5X09
PROM 6P09
CMCA
CLOCK FANOUT 04 5X08
PROM 6P08
BDP
CLOCK FANOUT 0B 5X11
PROM 6P11
CONTROL MEM
CONTROL MEM
CONTROL MEM
CONTROL MEM
BDP
RIGHT SIB
LEFT SIB
CSU
BANK CONTROL 07
MD
LEFT SIB
RIGHT SIB
MD
CLOCK FANOUT 08 5X12
CLOCK FANOUT 09 5X13
SOFT CONTROL 4C04
2/1
PROM 6P12
OPIB
CLOCK FANOUT 0B 5X02
PROM 6P02
OPIA
CLOCK FANOUT 0C 5X01
ADDRESS MUX 0B01
PROM 6P01
IFIC
CLOCK FANOUT 00 5X04
ADDRESS MUX 0B60-61
PROM 5P04
AC
CLOCK FANOUT 01 5X05
SOFT CONTROL 4C03
SOFT CONTROL 4C02
2/1
PROM 6P05
LMA
CLOCK FANOUT 02 5X06
6P06
ALN
CLOCK FANOUT 0A 5X14
PROM 6P14
OPSM
CLOCK FANOUT 0D 5X03
PROM 6P03
MAC ADDRESS BUS

I. CLOCK SYSTEM

A. OVERVIEW

The PIP3 clock system consists of the following components and features:

-Clock oscillators residing on the CSMC CP board. These oscillators are provided for nominal, fast and slow clock frequencies. In addition, an oscillator is provided for a time of day clock.

-A 1st stage clock fanout array. This array provides for clock frequency selection, pulse width formation, major cycle definition, and for fanout to the 2nd state clock fanout arrays which deliver clocks to the working registers. This array resides in the CSMC CP board.

-2nd stage clock fanout arrays. Every CP board in the PIP3 has at least one of these arrays. The MD CP board has two. This array receives a differential clock from the 1st stage clock array and fans it out to the FGE logic arrays and the C200 logic arrays residing on a CP board. This array provides 50 differential clocks and 13 single ended clocks. There are 14 2nd stage clock arrays in the PIP3 processor and Central Memory Control.

-Clock PROM. Each CP board has an associated PROM which is used to record the clock tuning information for a given CP board. In addition, the PROM will contain ASCII data for purposes of CP board documentation. The PROM is written during the manufacturing process.

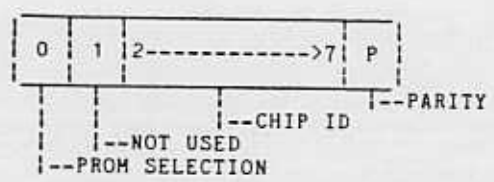
-Programmable clock tuning. Clock adjustments will be made in the PIP3 by storing clock delay information into the 1st and 2nd stage clock arrays. This will be done through the MAC. It is intended that the delay information for the CP board is first read from the PROM and then written to the clock array(s). Additionally, the ability is provided to read the delay information from the clock arrays. This is provided for testability. Note that the read is destructive and cannot be performed while the machine is in an on-line state.

-Clock system parity checks. The delay data in both the 1st and 2nd stage clock arrays is stored in shift registers, each rank of which is continually checked for correct parity. Additionally, the MAC address is checked for correct parity during the clock chip selection process. Note that when delay information is being written to or read from these arrays, clock outputs and the array's parity status will become undefined. The state of the machine following a read or write of clock array is therefore undefined and must be treated much like a power-on state.

B. CLOCK ARRAY SELECTION SEQUENCE

The first step in reading a clock PROM, writing a clock array, or reading a clock array is selecting the array. The array to be selected is determined by the MAC address as follows:

MAC ADDRESS



The clock array ID's are assigned as follows:

0 - Instruction Fetch/Instruction Control (IFIC)
1 - Address Control (AC)
2 - Local Memory A (LMA)
3 - Local Memory B (LMB)
4 - Central Memory Control A (CMCA)
5 - Central Memory Control B (CMCB)
6 - Business Data Processor (BDP)
7 - Central Storage Unit (CSU)
8,9 - Multiply/Divide (MD)
A - Arithmetic Logical Network (ALN)
B - Operand Issue B (OPIB)
C - Operand Issue A (OPIA)
D - Operand Issue/Segment Map (OPSM)
E - Control Store/MAC (CSMC, 2nd Stage)
F - Control Store/MAC (CSMC, 1st Stage)

The following PPU code will select a clock array:

```
FCN Op Code = 2  Type Code = 2
ACN
LDC 0
OAN
LDC  Array ID = Array to be selected.
OAN
FJM
DCN  This initiates the array selection.
```

To deselect a 1st or 2nd stage clock array, select an array with a different MAC bus address, or perform a select on a non-existant array. Note that following clock initialization, all clock arrays must be left unselected in order for the MAC bus to work properly.

I. CLOCK SYSTEM -- Continued

B. CLOCK ARRAY SELECTION SEQUENCE -- Continued

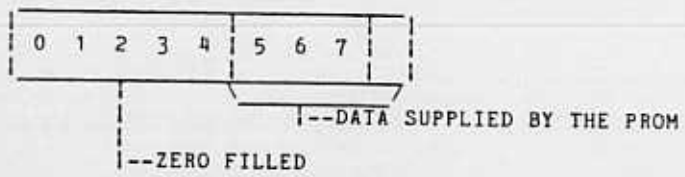
Note that if bit 0 of the MAC address is set in the selection sequence, the PROM input from the selected clock array will be read in subsequent read operations. If bit 0 is clear, clock delay information will be read from the delay registers inside the selected array.

Parity on the MAC address but is checked during the selection sequence. This parity is shared with the parity checkers on the shift registers containing the delay data. This status is undefined, therefore, until the array has been initialized. Once defined, this status can be used to isolate errors on the MAC address bus.

C. READ PROM DATA

Following the selection of the clock array with bit 0 of the MAC address set, the PROM associated with the selected array can be read. The PROM data includes 256 entries. The clock delay data in the PROM has the following format:

PROM DATA FORMAT



The 256th entry in the PROM shall contain bad parity. This will aid in error isolation on the MAC data bus. In addition, two entries in the PROM will be reserved for the Chip ID of the associated clock chip. This too will aid in error isolation on the MAC address bus.

On most CP boards, the first 64 entries in the PROM will comprise the clock tuning information for that CP board. On the MD board, the first 128 locations will be used. The remaining locations will be used for the special locations previously mentioned and any ASCII data which may be used to document the CP board, such as serial number, rev., date code, etc.

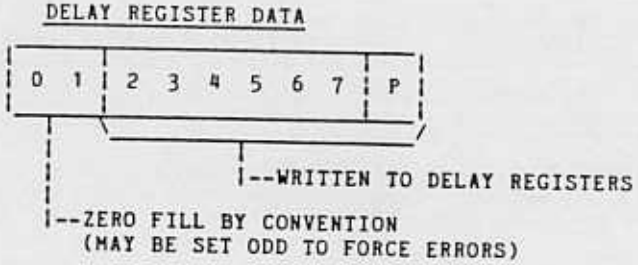
C. READ PROM DATA -- Continued

Any amount of PROM data may be read, beginning at any address. An Op Code = 4 and a Type Code = 2 will read the PROM following selection:

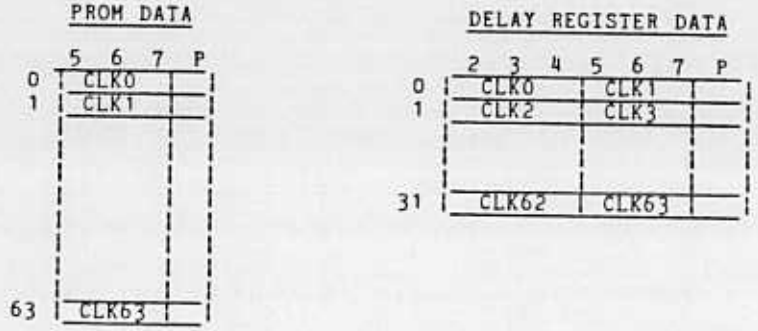
```
FCN  Op Code = 4  Type Code = 2
ACN
LDC 0
OAN
LDC (1st word adress of the PROM)
OAN
FJM
DCN
LDC (# of bytes to be transferred)
ACN
IAM BUFF
```

D. WRITE CLOCK DELAYS

Following the selection of a clock array with bit 0 of the MAC address clear, the array delay data may be written. This data consists of 32 entries of the following format:



Note that the delay data as it comes from the PROM is of the format 64x3, and the data to be written back to the array is of the format 32x6. This means that the PROM data must be assembled into the 32x6 format before it is written back. The relationship is as follows:



The three bit clock values have the following significance:

001 - earliest clock
000 -
011 -
010 -
101 -
100 -
111 -
110 - latest clock

D. WRITE CLOCK DELAYS -- Continued

An Op Code = 5 and a Type Code = 2 will write the clock delays. Because the delays are stored in shift registers, exactly 32 entries must be written. Following the writing, error status should be cleared, and then checked for the presence of errors in the shift registers just written.

```
FCN  Op Code = 5  Type Code = 2
ACN
LDC 0
OAN
LDC 0
OAN
FJM
DCN
LDC 32
ACN
OAM WTBUFF
```

E. READ CLOCK DELAY DATA

For testability reasons, the delay data in the clock arrays can read on the MAC data bus. Following selection of the array, the data may be read with an Op Code = 4 and Type Code = 2. All 32 entries should be read. The read process has much the same affect on the machine as the write, that is it leaves the PIP3 in an undefined state. Normal operation cannot proceed until the processor is initialized. The format and significance of the read data is identical to the write data.

```
FCN  Op Code = 4  Type Code = 2
ACN
LDC 0
OAN
LDC 0
OAN
FJM
DCN
LDC 32
ACN
IAM RDBUFF
```

WRITE AND READ CLK REG
(MAC SECOND STAGE CLKS)

```
QRUN
QCX,1
QCSP
QFC,1,E,2,2
QES,0,1218 0003 1212 0801
QES,1,0012 1212 1212 1212
QES,2,1212 1212 1212 1212
QES,3,1212 1212 1212 0312
QEKB,1,0,2,0,1
QAKB,1,0,2,A,1
QFC,1,10,2,2
QGO
QEND
```

QFC,RIC,CW12,TC,OP
QFC = FUNCTION OF THE MAINTENANCE CHANNEL
CW12 = BOARD SELECT (REGISTER NUMBER)
TC = 2 FOR CLOCK REGISTER
OP = 2 FOR THE OPERATION CODE

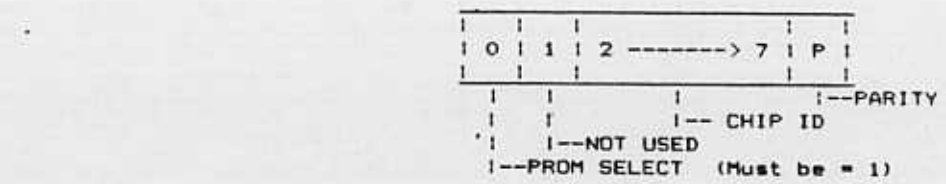
THE SECOND QFC COMMAND IS USED FOR DESELECTING THE CLOCK REGISTER AND THIS IS DONE BY SELECTING A BOARD SELECT NUMBER THAT IS NOT BEING USED FOR ANYTHING.

AFTER A READ OF THE MAINTENCE CHANNEL (QAKB) IS DONE, FOR THERE TO BE VALID DATA IN THE CLOCK REGISTER YOU MUST WRITE THE MAINTENCE CHANNEL AGAIN. THE REASON FOR THIS IS BECAUSE THE CLOCK REGISTER IS A SHIFT REGISTER. WHEN A WRITE TO THIS REGISTER IS BEGING DONE THE DATA IS SHIFTED IN AND ON A READ THE DATA IS SHIFTED OUT, SO THERE IS NO LONGER VALID DATA IN THE REGISTER.

THIS PROGRAM CAN ALSO BE USED TO READ THE CLOCK PROMS BY PUTTING AN B IN FRONT OF THE BOARD SELECT NUMBER, EX.(BE) AND TAKING OUT THE WRITE MAINTENANCE CHANNEL COMMAND (QEKB).

PIP3 BOARD PROM

In order to read information in the board PROM's, you must first select the chip with a MAC channel select function. The maintenance channel function will have an OP code of 2 with a type code of 2. Bit 0 of the MAC address must be a one, and bits 2 - 7 will provide the chip select ID.



The clock chip ID's are assigned as follows :

0 - IFIC
1 - AC
2 - LMA
3 - LMB
4 - CMCB
5 - CMCA
6 - BDP
7 - CSU (Has no PROM. Delay register loaded from file)
8,9 - MD (One PROM two delay registers)
A - ALN
B - OPIB
C - OPIA
D - OPSM
E - CSMC (2ND Stage Clocks)
F - CSMC (1ST Stage Clocks

Clock select code :

```
FCN       Op Code = 2    Type code = 2
ACN
LDC       0
OAN
LDC       Array ID
OAN
FJM
DCN       Initiates array selection
```

*** NOTE ***

All clock ID's must be left unselected in order for the MAC bus to work properly. Select an unused chip ID when finished with PROM functions to accomplish this.

PIP3 BOARD PROM

Addresses	0 - 127	Contain absolute delay values.
	128 - 213	UNUSED.
	214 - 253	Contain display code formatted info. Requires 2 locations to display 1 Char.
	254 - 255	Contain the absolute chip ID value in HEX. Requires 2 locations for 0 - F.

PROM ADDR	CONTENTS	
0 - 63	CLK0 - CLK63 delay values for 1ST clock fanout array.	
64 - 127	CLK64 - CLK127 delay values for 2ND clock fanout array (See MD board ID select).	
128 - 213	UNUSED	
214 - 225	PAK TYPE	(86AFH - 6 digits max) *
226 - 231	PAK S/N	(3 digits max) *
232 - 247	PAK P/N	(8 digits max) *
248 - 253	PAK REV	(3 digits max) *
254 - 255	CHIP ID	(1 digit max) *

* See next page for typical PROM of data area breakdown.

TYPICAL PROM CONTENTS

Board Type = Control Store/MAC (CSMC)
PAK type = 86AFH PAK P/N = 22110354 PAK REV = 006
PAK S/N = 301 CHIP ID = F (1ST STAGE CLOCKS)

PROM ADDR	PROM CONTENTS	CHARACTER	INFORMATION
214	4		PAK TYPE
215	3	8	|
216	4		|
217	1	6	|
218	0		|
219	1	A	|
220	0		|
221	6	F	|
222	1		|
223	0	H	|
224	5		|
225	5	(SPACE)	PAK TYPE
226	3		PAK S/N
227	6	3	|
228	3		|
229	3	0	|
230	3		|
231	4	1	PAK S/N
232	3		PAK P/N
233	5	2	|
234	3		|
235	5	2	|
236	3		|
237	4	1	|
238	3		|
239	4	1	|
240	3		|
241	3	0	|
242	3		|
243	6	3	|
244	4		|
245	0	5	|
246	3		|
247	6	3	PAK P/N
248	3		PAK REV
249	3	0	|
250	3		|
251	3	0	|
252	4		|
253	1	6	PAK REV
254	1		CHIP ID
255	7	F	|

(LOC. F)

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5		BYTE 6		BYTE 7	
					RANK 10		RANK 9		RANK 8	
					CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
					12	13	10	11	8	9

BYTE 0		BYTE 1		BYTE 2		BYTE 3		BYTE 4		BYTE 5		BYTE 6		BYTE 7	
RANK 7		RANK 6		RANK 5		RANK 4		RANK 3		RANK 2		RANK 1		RANK 0	
CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
6	7	4	5	2	3	0	1	I/O 20/20	I/O 40/40	CSU 10/10	I/O 10/10	CPU1 5/5	P.WIDTH	CSU 5/5	CPU0 5/5

CLOCK	SIG. NAME	SOURCE	SIB CONN.	DESTINATION	SIB CONN.
CLOCK 0	3M01V70	CSMC	2073	CSMC	2007
CLOCK 1	3M01V71	CSMC	2085	BBF	2007
CLOCK 2	3M01V72	CSMC	2097	MD	2007
CLOCK 3	3M01V73	CSMC	2109	MD	2012
CLOCK 4	3M01V74	CSMC	2121	ALN	2007
CLOCK 5	3M01V75	CSMC	2133	DP1B	2007
CLOCK 6	3M01V76	CSMC	2145	DP1A	2007
CLOCK 7	3M01V77	CSMC	2157	DPSM	2007
CLOCK 8	3M01V78	CSMC	2078	IFIC	2007
CLOCK 9	3M01V79	CSMC	2090	AC	2007
CLOCK 10	3M01V80	CSMC	2102	LMA	2007
CLOCK 11	3M01V81	CSMC	2114	LMB	2007
CLOCK 12	3M01V82	CSMC	2126	CMCA	2007
CLOCK 13	3M01V83	CSMC	2138	CMCB	2007

BRITE						RANK 10	RANK 9	RANK 8
READ	RANK 10	RANK 9	RANK 8	RANK 7	RANK 6	RANK 5	RANK 4	RANK 3

RANK 7	RANK 6	RANK 5	RANK 4	RANK 3	RANK 2	RANK 1	RANK 0
RANK 2	RANK 1	RANK 0					

SECONDARY CLOCK SKEW

BYTE 0		BYTE 1		BYTE 2		BYTE 3		BYTE 4		BYTE 5		BYTE 6		BYTE 7	
RANK 31		RANK 30		RANK 29		RANK 28		RANK 27		RANK 26		RANK 25		RANK 24	
CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
62	63	60	61	58	59	56	57	54	55	52	53	50	51	48	49

BYTE 0		BYTE 1		BYTE 2		BYTE 3		BYTE 4		BYTE 5		BYTE 6		BYTE 7	
RANK 23		RANK 22		RANK 21		RANK 20		RANK 19		RANK 18		RANK 17		RANK 16	
CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
46	47	44	45	42	43	40	41	38	39	36	37	34	35	32	33

BYTE 0		BYTE 1		BYTE 2		BYTE 3		BYTE 4		BYTE 5		BYTE 6		BYTE 7	
RANK 15		RANK 14		RANK 13		RANK 12		RANK 11		RANK 10		RANK 9		RANK 8	
CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
30	31	28	29	26	27	24	25	22	23	20	21	18	19	16	17

BYTE 0		BYTE 1		BYTE 2		BYTE 3		BYTE 4		BYTE 5		BYTE 6		BYTE 7	
RANK 7		RANK 6		RANK 5		RANK 4		RANK 3		RANK 2		RANK 1		RANK 0	
CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
14	15	12	13	10	11	8	9	6	7	4	5	2	3	0	1

BYTE 7		
RANK 0		
MU	CLOCK	CLOCK
	0	1
01	234	567

CLOCK SETTINGS

CHANGES SKEW FOR BOTH CLOCKS IN A RANK

SETTINGS	HEXIDECIMAL	BINARY	AMOUNT OF CHANGE
1 (EARLIEST CLK)	09	00001001	-200 PS
0	00	00000000	-300 PS
3	1B	00011011	-100 PS
2 (NOMINAL)	12	00100010	0
5	2D	00101101	+400 PS
4	24	00100100	+100 PS
7	3F	00111111	+50 PS
6 (LATEST CLK)	36	00110110	+50 PS

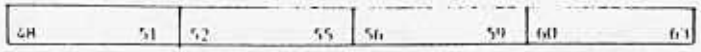
WHILE LEAVING THE RIGHT-MOST CLOCK IN A RANK AT NOMINAL CHANGE THE LEFT-MOST CLOCK

SETTINGS	HEXIDECIMAL	BINARY
1	0A	00001010
0	02	00000010
3	1A	00011010
2	12	00010010
5	2A	00101010
4	22	00100010
7	3A	00111010
6	32	00110010

WHILE LEAVING THE LEFT-MOST CLOCK IN A RANK AT NOMINAL CHANGE THE RIGHT-MOST CLOCK

SETTINGS	HEXIDECIMAL	BINARY
1	11	00010001
0	10	00010000
3	13	00010011
2	12	00010010
5	15	00010101
4	14	00010100
7	17	00010111
6	16	00010110

MAINTENANCE CHANNEL FUNCTION WORD



NOT USED | CONNECT CODE | OP-CODE | TYPE CODE

CONNECT CODE	RADIAL INTERFACE SELECTED		LOCATION
0	IOU MAINTENANCE REG.	I-4	JQ at A22
1	RADIAL INTERFACE 1	MEM & CPU-0	JR at A23
2	RADIAL INTERFACE 2		JR at A23
3	RADIAL INTERFACE 3	CPU-1	JR at A23
4	RADIAL INTERFACE 4		JR at A24
5	RADIAL INTERFACE 5		JR at A24
6	RADIAL INTERFACE 6		JR at A24
7	NU		
8 thru F	INTER-PP COMMUNICATION		

			I-4		P-3		M-3	
FUNCTION	HEX	OCT	HEX	OCT	HEX	OCT	HEX	OCT
CLEAR LED	3	3	030	0060				
READ	4	4	040	0100	140	0500	14A	512
WRITE	5	5	050	0120	150	0520	15A	532
MC	6	6	060	0140	160	0540	16A	552
CLR FSR	7	7	070	0160	170	0560	17A	572
ECHO	8	10	080	0200	180	0600	18A	612
REQ SS	C	14	0C0	0300	1C0	0700	1CA	712

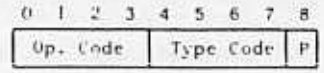
ANY CONNECT CODE FROM 10 to 17 OCTAL SHALL DISABLE THE TIMEOUT COUNTER AND THE MAINTENANCE CHANNEL MAY THEN BE USED FOR INTER- PP COMMUNICATION.

THE TYPE CODE IN THE I-4 MUST BE 0 ,OR A DUMMY READ/WRITE OPERATION WILL OCCUR

CLR FSR= CLEAR FAULT STATUS REGISTER
REQ SS = READ SUMMARY STATUS REG.

REGISTER VALUES	
HEX	OCT
00	00
10	20
12	22
20	40
21	41
30	60
31	61
32	62
40	100
80	200
81	201
82	202
83	203
84	204
85	205
86	206
87	207
88	210
89	211
A0	240

the information present on the data lines at the time a Function is received from the I/O Unit is designated the Function Byte and has the following format.



The Operation Code specifies six functions which are implemented in the P3/M3 MAC.

Op. Code	Description
0	STOP
1	START
* 2	CLOCK ARRAY SELECT
4	Read
5	Write
6	MASTER CLEAR
7	CLEAR ERROR
8	ECHO
9-15	Not Implemented

Type Codes Supported by P3/M3 MAC

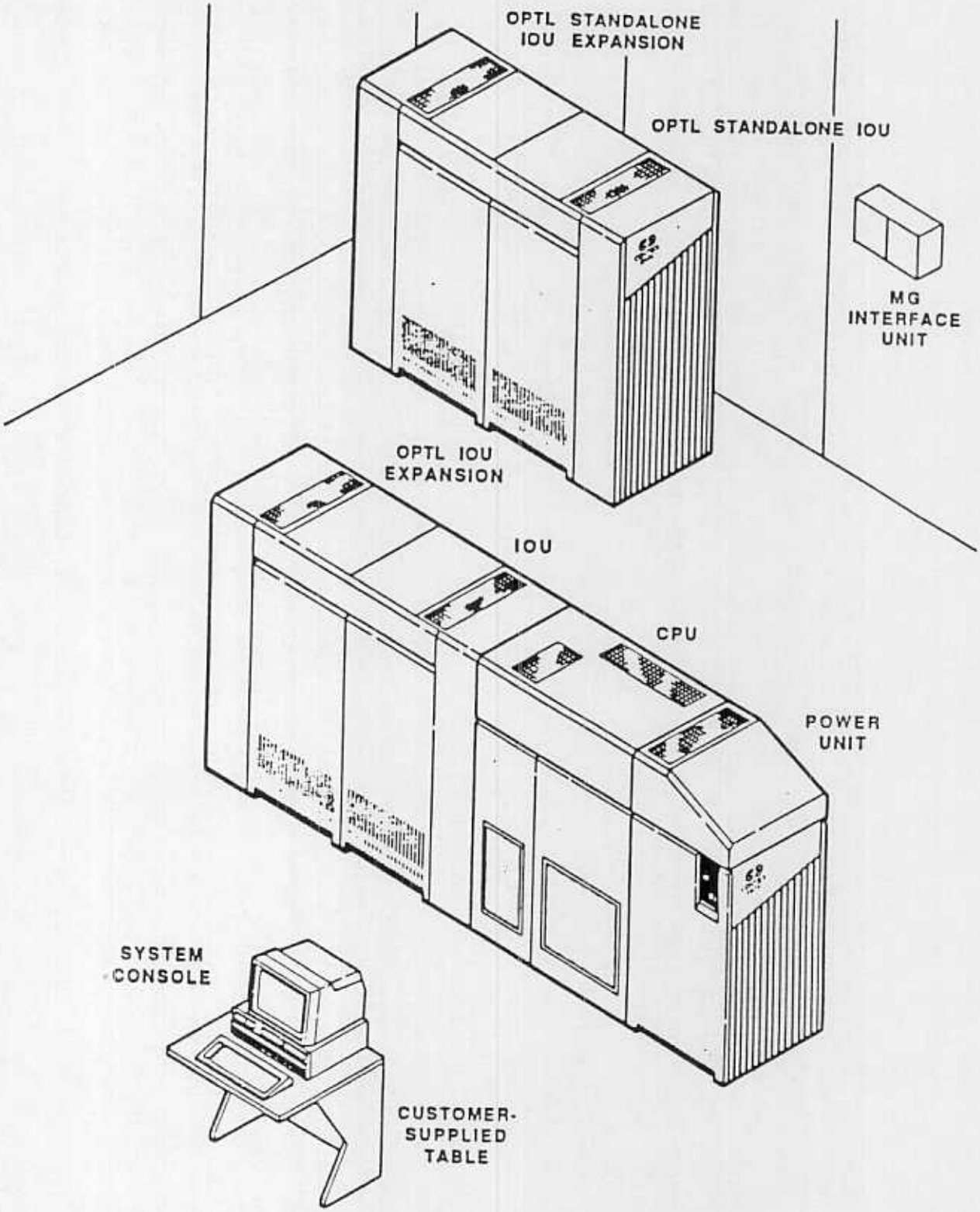
Nine Type Codes are specified for the MAC as follows.

Type Code	Description
0	P3 Processor State and Process State Registers
1	Control Store Microrand Data
* 2	CLOCK OR PROM DATA
3	Copy Instruction Ref Rom Memory
4	Soft Control Memories
5	BDP Decode and Control Memories
6	Instruction Fetch decode Memories
7	Register File
8-9	Unassigned
A	M3 Maintenance Registers
B-F	Unassigned

Immediate Operations

Immediate Operations require only a Function signal and a companion Function Byte. Immediate operations are as follows:

Op. Code	P3 (Type 0)	M3 (Type A)
0 - STOP	X	N/A
1 - START	X	N/A
6 - MASTER CLEAR	X	X
7 - CLEAR ERROR	X	X


OPTL STANDALONE
IOU EXPANSION
OPTL STANDALONE IOU
MG
INTERFACE
UNIT
OPTL IOU
EXPANSION
IOU
CPU
POWER
UNIT
SYSTEM
CONSOLE
CUSTOMER-
SUPPLIED
TABLE

CONTROL STORE

COMPONENTS:

- MICROCODE MEMORY RAMS
- GENERAL MICRAND REGISTER
- FUNCTIONAL UNIT MICRAND REGISTERS AND FANOUT
- ASSEMBLY REGISTER
- DISASSEMBLY REGISTER
- MICROSEQUENCER

FEATURES:

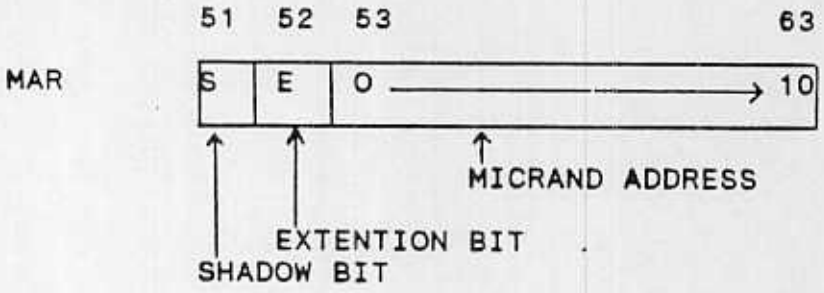
- 4K-144 BIT MICRANDS, INCLUDING PARITY
- 4K-144 BIT SHADOW FOR BACKUP IN CASE OF SOFT ERROR
- READ MOSTLY, WRITE DURING PROCESSOR INITIALIZATION
- CYCLE TIME, 1 MAJOR CYCLE, 44.8NS
- PROVIDES FOR:
  - . MICROCODE CONTROL OF THE INSTRUCTION UNIT AND FUNCTIONAL UNITS
  - . STARTING/STOPPING/BREAKPOINT
  - . INITIALIZATION OF PROCESSOR VIA MICRO-SEQUENCES
  - . SENSE CONDITIONS FOR MICRO-BRANCH DECISION
  - . MAC ACCESS TO SYSTEM REGISTERS VIA MICRO-SEQUENCES

CONTROL STORE

DIFFERENCES:

- PARTITIONING
- TWICE AS MUCH MICRAND SPACE AS THE 860.
  - . PROVIDES SEPARATE SPACE FOR 180 AND 170 MICROCODE.
  - . SHOADOW MEMORY FEATURE FROM 860 MAINTAINED.
- SPECIAL MICROTRAP ADDRESSES FOR PROCESSOR DETECTED MALFUNCTIONS.
  - . PROVIDES FOR IMPROVED ERROR LOGGING ON RETRIES.

CONTROL STORE MICRAND ADDRESS EXTENTION



SHADOW BIT	EXTENDED BIT	
0	0	180 MICROCODE
0	1	170 MICROCODE
1	0	180 MICROCODE (SHADOW)
1	1	170 MICROCODE (SHADOW)

HALT VECTOR EXAMPLES:

MAR = 0005 - 180 HALTED

0805 - 170 Halted

1005 - 180 Halted (SHADOW)

1805 - 170 Halted (SHADOW)

CONTROL STORE

ENTRY POINTS

MICRAND ADDRESS (HEX)

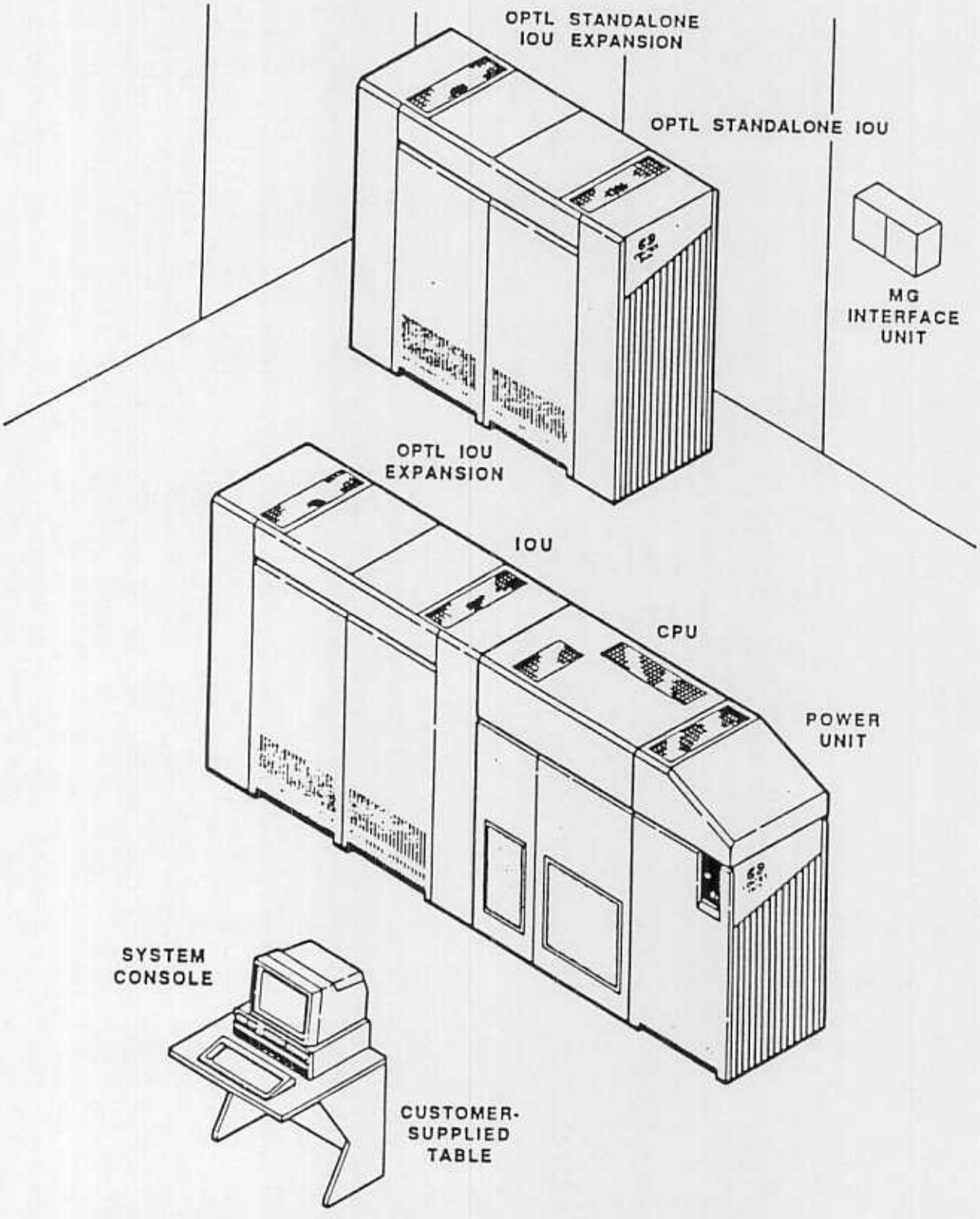
004: STOP
008: UNIMPL INSTR
010: IB12 NOT VALID (UNCOND EXIT)
020: IB12 NOT VALID (COND EXIT)
030: } RESERVED ENTRY
031: } POINTS FOR MAC
032: }
040: RETRY WITH PURGE
041: RETRY
042: TRAP WITH PURGE
043: TRAP
044: CY80 EXCHANGE WITH PURGE
045: CY80 EXCHANGE
046: CY170 EXCHANGE
047: HALT
050: DFT RETRY VECTOR
051: DFT RETRY VECTOR
052: DFT TRAP VECTOR
053: DFT TRAP VECTOR
054: DFT EXCHANGE VECTOR
055: DFT EXCHANGE VECTOR

1XX: CY80 INSTRUCTIONS
2XX: CY80 DESCRIPTORS

300:
THRU CY170 INSTRUCTIONS
37F:

380: NON-EXECUTABLE

3FF: DEBUG HOUSKEEPING


OPTL STANDALONE
IOU EXPANSION
OPTL STANDALONE IOU
MG
INTERFACE
UNIT
OPTL IOU
EXPANSION
IOU
CPU
POWER
UNIT
SYSTEM
CONSOLE
CUSTOMER-
SUPPLIED
TABLE

The following description of the CYBER 180 model 860/962 Central Processor (CP) is intended for use with the Level 0 Diagram. Central Memory (CM) and the following major functional areas of the CP appear in the diagram.

Maintenance Access Control (MAC)
Instruction Fetch (IF)
Control Store (CST)
Instruction Control Pipeline (ICP)
Operand Issue (OPI)
Instruction Completion Control (ICC)
Arithmetic and Logical Network (ALN)
Address Control (AC)
Business Data Processor (BDP)
Segment Map (SM)
Local Memory (LM)
Central Memory Control (CMC)

This section includes analysis of all functional areas and major signal paths. Additional text traces the execution of three instructions through the CP.

FUNCTIONAL AREAS

MAC

MAC is the CP interface with the Maintenance Control Unit (MCU) in the IOU. The Maintenance Channel connects MAC to the MCU.

MAC initializes the CP by loading information required for system operation into Random Access Memories (RAMs). These RAMs are distributed throughout the CP to perform code conversions and provide control facilities. The MAC Data and Address buses connect them to MAC. MAC also provides Dependent Environment Control (DEC) signals to activate performance and maintenance features of the machine, and Processor Test Mode (PTM) signals to force parity errors for maintenance purposes. MAC monitors error signals from all functional areas in the processor, except CM and CMC. It stores the error signals in Processor Fault Status (PFS) registers. MAC indicates the presence of such errors by means of a status summary and supplies PFS data to the MCU for error logging purposes.

IF

IF requests instructions from LM and reformats them for eventual processing in ICP and CST. Instruction buffer ranks in IF minimize delays encountered in other sections of the CP that result from waiting for instructions.

Branch Address Adder

The Branch Address Adder issues IF Address, the byte number address of an instruction word. IF Address accompanies IF Request, the instruction request, to LM.

Data Interchange (DAI) enters the Branch Address Adder to become the first IF Address of the instruction sequence. P (lower) provides addresses for subsequent instructions in a Read Next Instruction (RNI) sequence. IF Address also may be a branch address.

Instruction Formatting and Buffering

IF parcels out the instructions contained in the requested LM Read Data word in Instruction Assembly. The instruction words contain from two to four instructions, which in C170 mode are either 15 or 30 bits long. In C180 mode the instructions are 16 or 32 bits long. C180 BDP instruction descriptors have 32 bits. The instruction opcode addresses the First Level Instruction Decoder, which issues supplementary information needed for instruction execution. The instruction parcel and decoder output are placed in an expanded format before loading into the Buffer Rank 2, 3, 10, 11, and 12 registers. From the Buffer Rank 12 Register the instruction opcode goes to CST to address the first 128-bit micrand needed to execute the instruction. IF also sends immediate operands (operand fields contained in the instruction), control information, and the program address (P lower) of the instruction to ICP.

Rank Designators

Rank numbers in IF and ICP designate how many major and minor cycles elapse between an instruction's departure from Instruction Assembly and its arrival at a buffer register. A single-digit rank designator is the number of 16-ns minor cycles. The leftmost digit of a two-digit rank designator is the number of 64-ns major cycles and the rightmost digit is the number of additional minor cycles.

The time interval specified by the rank designator is valid only if an instruction's movement in the pipeline is not suspended and no buffer register ranks are bypassed. When Buffer Rank 2, 3, 10, 11, and 12 Registers are empty, the instruction parcel and First Level Instruction Decoder output are loaded directly into Buffer Rank 12 Register.

Movement in the pipeline may be suspended for several reasons. Once an instruction enters ICP Rank 22, its various components remain there until the micrand sequence is finished. The effect is to block all pipeline movement behind the Rank 22 instruction.

An individual micrand may stall in Rank 22 if an operand the micrand needs is being acted upon by another micrand and shortstop paths cannot resolve the conflict.

A micrand may remain in Rank 32 as long as the functional area it needs to use is busy. Also, if a micrand makes a memory reference and Segment Map Miss activates in SM, a hardware-controlled Segment Descriptor fetch sequence occurs. Microcode control is suspended in the CP and the micrand stalls in Rank 32 until the required Segment Descriptor returns from CM.

A micrand executing in Rank 41 typically does not move to Rank 50 with a valid result until Response returns from the functional area the micrand is using.

Conditional Branching

A conditional branch instruction, which initiates a new instruction sequence, leaves IF and proceeds through ICP before the associated condition can be tested in ALN. If ALN determines at Time 43 that the condition has not been met, ALN sends ALN Unbranch to IF. ALN Unbranch indicates the RNI sequence must be substituted for the instruction sequence addressed by the branch instruction. Rank 50 P, the preserved address of the branch instruction, enters the Branch Address Adder, where it is added to a constant of four. The new address points to the instruction following the branch instruction in the RNI sequence.

C170 Mode Address Out of Range (AOR) Detector

The C170 Mode AOR Detector performs C170 range testing for instruction addresses.

NOTE

Because the Branch Address Adder does not supply end-around carries, no dedicated AOR test hardware is required to detect adder overflow. If the adder produces a result that exceeds the C170 address length (21 bits), the carry out is to three zero bits to the left of the address. When set, any of these bits causes the detector to sense an AOR condition.

CST

The CST RAM contains microcode required to execute the C170 and C180 instruction sets. The Disassembly Network, used to disassemble 64-bit data words, also is in CST.

Microcode

The CST RAM contains the C170 and C180 instruction micrand sequences, consisting of one or more micrands for each instruction. A micrand consists of a 64-bit General Micrand and a 64-bit Functional Unit Micrand. The General Micrand and the i, j, and k designators from ICP govern reading and writing of OPI Register File locations. The General Micrand also controls selection of Immediate Operands in OPI. The Functional Unit Micrand controls operations in ALN, BDP, LM, AC, and SM. The functional unit field within the General Micrand determines which functional area(s) uses the Functional Unit Micrand.

An instruction's Rank 12 Opcode addresses the starting location of a micrand sequence in the CST RAM. The Micrand Sequence Control (MSC) Field in each General Micrand determines the address of the next micrand. If an error or exception occurs while an instruction is executing, ICC typically generates a Microtrap Code at Time 52 to address an interrupt microcode routine in the CST RAM.

Disassembly Network

The CST Disassembly Network disassembles 64-bit Register File Read Data or Functional Unit Micrand Register data into 8-bit bytes for transfer to MAC. The CST Disassembly Network obtains General Micrand or Functional Unit Micrand data via the Functional Unit Micrand Register. The data proceeds to MAC on the MAC Data bus. PFS Bus Data bytes also can enter the MAC Data bus through this network.

ICP

ICP provides five buffer ranks, corresponding to five stages in the execution of a micrand.

Rank 13 - Micrand Access

Program Address (P) and the Instruction Mux Bits leave IF's Buffer Rank 12 Register for ICP. At the same time, the Rank 12 Opcode goes to Microcode Address Control in CST to select a micrand. P and the Instruction Mux Bits load into the Rank 13 Register.

Rank 22 - Operand Selection

When Rank 13 j, k Operand Select, Immediate Operand, P, and other control signals load into the Rank 22 Register at Time 22, the General Micrand loads into the General Micrand Register in CST. The Rank 22 Register remains latched until the instruction exits after the execution of its micrand sequence.

From Time 23 to Time 31, the General Micrand's RDSa, b, and c fields control addressing of the Register File or selecting of Immediate Operands. Concurrently, i, j, j+1, k, and k+1 designators from the Rank 22 Register enter Register File Address Select and Rank 22 P and Immediate Operand enter OPI's Immediate Operand Select network. (j+1 and k+1 designators are used in floating-point arithmetic operations.) The selected operands are then sent to SM, AC, or ALN.

Rank 32 - Functional Area Selection

At Time 32, the RDS Write (RDSw) field (RDSa or RDSd) enters a minipipe delay network within OPI to control writing into the Register File at Time 52. RDSw and a portion of the General Micrand from CST load into the Rank 32 Register along with j, k Operand Selects, P, and various control signals from the Rank 22 Register. The RDS Write field later returns to OPI to control writing into the Live Registers. The functional unit field of the General Micrand generates the appropriate Go signal after the preceding micrand's Response returns to ICP. Go selects a functional area to perform the task specified by the Functional Unit Micrand. Go usually is issued if the selected functional unit is not busy.

Rank 41 - Functional Unit Microrand Execution

Once Go activates, the remaining General Microrand fields and instruction information load into the ICP Rank 41 Register. Typically, they remain in the Rank 41 Register until Response returns to ICP from the functional area selected by the microrand. Response permits the next General Microrand field (in Rank 32) to issue a Go signal and transfer itself to Rank 41. The length of time a microrand remains in the Rank 41 Register may exceed one major cycle. The stay normally depends on how long the selected functional area takes to complete its operation and submit Response.

Rank 50 - Result Selection

The Rank 50 Register sends Rank 50 Control signals to ICC. They are used in conjunction with errors and exceptions generated during microrand execution to determine if an interrupt routine will be activated. The Rank 50 Untranslatable Pointer (UTP) Register saves instruction addresses or operand addresses for examination if a Page Table search without find exception occurs.

OPI

OPI contains the Register File and various Live Registers. Registers in the Register File hold operands and exchange package data required for instruction execution. Live Registers supply data for various operations and collect data from the CP operating environment.

Register File

The 64-word Register File contains operating registers (A, B and X) for C170 and C180 instructions. It also holds other exchange package information and provides holding registers for intermediate results.

The RDSa, b and c fields from the General Microrand and the RDSd field from the Functional Unit Microrand determine Register File read and write addresses. An RDS field may contain the address, or a code within the field may select an instruction's i, j, j+1, k, or k+1 designator as the address. Separate i designators are available for C170 and C180 mode operations. A Start and X Start register bits become the Register File address in the event a C180 Load or Store Multiple (80, 81) instruction, a call, a return, or C170 exchange jump operation is taking place.

The RDS fields also can select an Immediate Operand, P, or Live Register Read Data instead of Register File Read Data for loading into the Operand Registers.

DAI Register

The DAI Register can select result data from ALN, LM, or AC for input to the Register File or the Live Registers. Result data is available at the same time ICP Rank 50 is loaded. The DAI Register also can select the Functional Unit Microrand for input to the Register File.

Live Registers

The Live Registers in OPI contain control information for various C170 and C180 CP operations. Some of the Live Registers are written only under microcode control. Normally they are loaded from the exchange package at the same time the exchange package enters the Register File from CM.

Some of the write only Live Registers also may be loaded during execution of C180 Copy from Xk per (Xj) instructions (OF).

The CP uses the constant output of these Live Registers during on-line operations. The Live Registers give the CP quicker access to exchange package information, which otherwise would have to be obtained from the Register File.

Other Live Registers in OPI are considered to be read only under microcode control. The process interval and system interval timers are examples. The contents of read only registers change as a consequence of changes in the CP hardware environment. These changes typically impact system operation and require monitoring.

ICC

When an error or exception occurs while a micrand is executing, ICC selects and synchronizes the start of an interrupt routine.

Errors and exceptions accumulate in the Monitor and User Condition Registers and are examined in the Condition to Mask Comparators. C170 mode error exit conditions load into the Exit Mode Condition Register for processing in Exchange Interrupt Control. The Monitor, User, and Exit Mode Mask Register Bits enable ICC to interrupt selectively. Those errors and exceptions in the Monitor and User Condition Registers which are stackable (deferred interrupts permitted) trigger interrupts only when the corresponding mask bits are set. Mask bits determine the type of mandatory interrupt that will occur for unstackable errors and exceptions. Exit Mode Mask Register Bits enable C170 exchanges when set.

Microtrap Code

The Halt, Exchange, Trap Interrupt Control and Retry Control produces Microtrap Code. The code, which determines the type of interrupt, is based on control signals supplied by ICC and the error inputs. The code addresses the appropriate microcode routine in the CST RAM.

Clear Pipe

Clear Pipe becomes active if ALN discovers that the required condition is not met during execution of a conditional branch instruction. Instructions that have been requested by the branch instruction must be removed by the pipeline. Clear Pipe also activates to empty the pipeline of instructions before executing an interrupt routine.

ALN

ALN contains circuitry for integer and floating-point arithmetic, operand shifting, logical operations, normalizing of floating-point operands, and conditional branch comparisons.

The Normalize Encoder performs all normalize operations. The Multiply/Divide Network carries out multiplies and divides of integers and floating-point coefficients. The Shifter Ranks 1 and 2 and the Shift Count Generator act together to perform shift operations. The 97-bit Large Adder performs addition, subtraction, and logical operations on integers and floating-point coefficients. The Exponent Arithmetic Network does exponent calculations. Branch Condition Control evaluates operands to determine if a conditional branch instruction should proceed.

The B and C Operands from OPI are the principal data inputs to ALN. ALN Result returns to OPI for entry into the Register File. Other data inputs are BDP Convert Binary and the AC Shift Count, a selectable input which typically controls the amount and direction of a shift operation. BDP Convert Binary is a byte input which a multiply algorithm assists in converting from decimal to binary form.

ALN generally performs one's complement arithmetic in C170 mode and two's complement arithmetic in C180 mode.

Go initiates ALN arithmetic operations, which are controlled by the Functional Unit Microrand.

AC

AC contains the hardware to create CM byte addresses. AC also supplies data to and receives results from BDP during C180 BDP operations.

Address Formation

The Address Formation network in AC forms the byte number portion of the address sent to LM for Register File data or BDP stream data. The A/B Operand input to the Address Formation network can contain an operand or address selected by an RDSa or b field in OPI. For BDP instructions the C Operand is an A or B stream length field. Address Offset, normally an Immediate Operand from the instruction, is a third address component. In the C170 mode, the Address Formation network performs 18-bit and 21-bit one's complement addition or subtraction. (Operands are 18-bit quantities and RAC is 21 bits.) In the C180 mode, the Address Formation network performs 32-bit two's complement addition.

The byte number from the Address Formation network merges with an Active Segment Identifier (ASID) from SM or from the A/C, B Stream ASID Register. Together they comprise AC Address, which is a system virtual address (SVA).

BDP Instructions

BDP uses CM data provided by LM via AC. AC's data inputs and outputs for BDP operations are LM Read and Write Data. LM Read Data is a 64-bit word disassembled by the A Stream Disassembly network or the B Stream Disassembly network into A Stream Data or B Stream Data bytes. C Stream Data bytes produced in BDP are assembled into a 64-bit word in the C Stream Assembly network and sent to LM as LM Write Data. OPI can also send C Operand data to LM as LM Write Data.

Since the A and C streams are never busy at the same time, they share common hardware within AC - the A/C Stream ASID Register, the A/C Stream Address and Length counters, and the A/C Stream Disassembly/Assembly Network.

Load/Store Instructions

Load Byte and Load Bit instructions, which transfer data from any location within a memory word to the least significant byte or bit of an operand in the Register File, are processed in AC. The A/C Stream Disassembly/Assembly network shifts the LM Read Data byte or bit and sends it to OPI as Load Data. For Store Byte and Store Bit instructions, the A/C Stream Disassembly/Assembly network shifts Register File data from the least significant position to the desired location in a memory word.

NOTE

Because CM does not directly support bit addressing, store bit operations are performed by means of read and set lock and read and clear lock functions for one and zero states, respectively. These functions impose additional requirements on the AC data path to LM.

AC also processes C180 Load and Store Word, Address, and Multiple Word instructions to transfer 64 bits between memory and the Register File.

AC Control

A Functional Unit Micrand field accompanied by Go provides primary control of AC operations. Soft control memories, loaded from the MAC Data bus during system initialization, contain control signals that are similar to micrand bits but which are issued each minor clock cycle.

The ALN Shift Count Register holds a shift count for use in ALN during ALN shift operations. ALN shift counts are formed by the same adder within the AC Address Formation Network otherwise used to perform memory address arithmetic.

The C170 Mode Range Tester is similar to the C170 Mode AOR Detector in IF except that it detects operand AOR conditions rather than instruction AOR conditions.

NOTE

The C170 Mode Range Tester evaluates addresses produced in the Address Formation Network adder, which has an end-around carry network. If overflow occurs, the adder result may erroneously appear to be in range due to the end-around carry. The C170 Mode Range Tester must sense overflow separately when evaluating a CM address.

BDP

BDP executes C180 mode business data processing instructions in conjunction with AC. AC links BDP to the rest of the CP. AC supplies A and B Stream Data to BDP from LM and receives C Stream Data results for return to LM.

Data Flow

BDP works with bytes only and processes no more than 256 byte pairs in a single operation. The operand fields enter BDP through A and B Stream Stages 1 through 4 and reach the ALU at the maximum rate of one byte pair per minor cycle. From the ALU, results pass through Common Stages 5 and 6 and enter the Buffer RAM. Once all result data has entered the Buffer RAM, C Stream Data returns to AC through C Stream Stages 1 through 5. When required, the Binary/Decimal Converter changes bytes leaving C Stream Stage 5 from binary to decimal form and sends the data back to the Buffer RAM by way of the A Stream and the ALU.

Register Files A and B, both with 256-byte capacity, are available to process Compare Collate and other instructions for which tabular information is required. When placed in a Register File, that information is used to control processing of data. An Edit instruction requires that a source and a mask field be entered into the Register Files. The fields proceed to the Edit circuitry and produce a result which is stored in the Buffer RAM.

During system initialization, MAC loads RAMs in BDP Control with instruction/data validation data, EBCDIC convert data, and binary/decimal convert data via the MAC Data bus.

Stream Pausing

Pause A and B Stream signals synchronize the input of A and B Stream Data bytes to the BDP ALU. Pause C stream delays the output of the BDP result until AC forms an address for storing the data in memory. A Functional Unit Microrand controls a BDP operation after Go arrives.

SM AND LM

SM and LM constitute the virtual memory address circuitry. SM converts the process virtual address (PVA) to an SVA by changing the user's segment number into an ASID. LM converts the SVA to a real memory address (RMA). All memory protection is based on segmentation, with validation performed by SM.

Segment Map RAM

The Segment Map RAM contains up to 32 most-recently-used Segment Descriptor entries from the process segment table in CM. When the ASID contained in an instruction sequence's Segment Descriptor is latched into the P Descriptor Save Register, it joins IF Address (a byte address) in becoming the IF SVA. Subsequent instruction requests within the segment continue to use the output of the P Descriptor Save Register as the IF ASID.

The contents of the P Descriptor Save Register also serve as the ASID portion of the AC Address (operand SVA) during C180 Load Bytes, Displaced Relative (86) instructions and during all C170 CM operand references. The ASID for other operand SVAs enters AC directly from the Segment Map RAM. Operand and instruction SVAs become RMAs in LM.

If the required Segment Descriptor entry is not available in the Segment Map RAM, a Segment Descriptor Fetch sequence obtains it from the process segment table in CM. Segment Descriptor Fetches occur under hardware control rather than microcode control. Microcode control is suspended during Segment Descriptor fetch memory references.

Access Validation Testing

SM performs all of the access validations for addressing memory. Security ring tests are performed, as are key/lock tests and read, write and execute privilege validity tests. The tests are comparisons between Access Control Fields in the Segment Descriptor and the Ring and Keys contained in a PVA, supplied by the accessor. SM Access Violation is an exception indicating that an illegal memory reference has been attempted. SM Access Violation initiates an interrupt routine by producing a Microtrap Code in ICC. A Functional Unit Micrand field controls various SM operations.

Cache Memory

LM contains up to 4K words of high-speed Cache Memory to provide storage for the most recently used CM data. A four-word block of CM Read Data words enters Cache Memory, a word at a time in an order that is not necessarily predetermined. The word of interest in four-word block goes to other destinations within the CP as LM Read Data. When the CP addresses the data a second time, the data is recalled from Cache Memory as LM Read Data. An intermediate storage device, Cache Memory enhances CP performance in reading CM data.

When the CP sends LM Write Data to CM, the CP writes the Cache Memory location containing the same CM data the write is modifying in CM.

Page Map RAM

LM contains 128 entries from the CM system page table (SPT) in the Page Map RAM. An SPT entry is required to convert an SVA into an RMA to access CM when the requested data is not available in Cache Memory. The presence of the most recently used SPT entries in the Page Map RAM accelerates addressing of CM. The Map Address from the SVA obtains the Page Frame Address (PFA). The PFA combines with the Page Offset (PO) from the SVA to generate the RMA.

If the desired SPT entry for a memory access is not in the Page Map RAM, Page Table Search Control creates Page Table Address (PTA) Hash. PTA Hash is an RMA into the SPT created from the SVA's ASID and page number. The required SPT entry returns from CM as CM Read Data. It enters the Page Map RAM at the same time it is gated back to CMC as the PFA portion of a new RMA. The CM Read Data words addressed by this second RMA enter Cache Memory at the same time the word of interest goes to a functional area as LM Read Data.

CMC Tag

During CM read operations the CP typically uses CMC Tag to determine where to send data entering the CP from CM. The RMA Network and Control generates the tag to accompany an RMA to CMC. The tag enters a delay circuit in CMC which synchronizes it with the data the RMA obtains from CM. CMC Tag returns from CMC to LM Control to guide LM Read Data into the CP and, when applicable, Cache Memory. During an exchange jump, LM Control sends CMC Tag to OPI to enter LM Read Data into the Register File and, in some cases, the Live Registers.

A/C Stream LM Requests, IF Request, or Instruction Issue Request Enable initiate LM operations. Functional Unit Microrand fields control the operations and Stream A/C, B Response, IF Response, or Instruction Issue Response signals indicate their completion.

CMC AND CM

LM (A), LM (B), IOU and an auxiliary port all have access to CM through CMC. CMC contains Conflict and Bank Busy Control, which resolves bank conflicts and simultaneous CM request conflicts. Memory is contained in a single stand-alone cabinet, available to CP-0 and an optional CP-1.

Refresh

The Conflict and Bank Busy Control generates a refresh request every 15 clock periods and sends it to Bank Control via the Go Bank signal. To refresh memory, a read cycle is performed on each row address of each memory array. When refresh is not active, Conflict and Bank Busy Control prioritizes and initiates other requests such as write, read, and partial write.

Write

During a CM write operation, Address, Control, and Write Data enter CMC through an Input Port. The Input Port routes the Bank Code, part of the Address, to the Conflict and Bank Busy Control. There the Bank Code produces a Go Bank signal, which passes through Bank Control and selects one of eight Memory Banks in CM. The remaining Address and Control signals also proceed to CM's Bank Control. Write Data enters the Write Error Correction Code (ECC) Generator, where an ECC is formed to accompany the data to Bank Control. Go Bank starts the write sequence in the Memory Bank, ultimately resulting in data being stored in that bank.

Read

During a CM read operation, Bank Code, Address, and Control signals become active as they do for a write, except that a write request is absent. Read Data departs a Memory Bank along the bidirectional read/write path, passes through Bank Control, and enters the Single Error Correction, Double Error Detection (SECDED) network in CMC. SECDED corrects any single bit errors and flags double bit errors. An Output Port then sends the Read Data to the device that initiated the read request.

Partial Write

CMC is capable of modifying an individual byte or bytes within a memory word. The operation requires two passes. The modifying write data enters CMC through an Input Port, goes through the Write ECC Generator and loads into a holding register in CM's Bank Control. Write Data from that holding register and Read Data from a Memory Bank (by way of Bank Control and SECDED) enter the Partial Write (PW) Network and ECC Generator in CMC. The combination of the two words creates a PW Data word, which returns to memory after an ECC is generated. Mark bits control the Partial Write Network. Memory word bytes which have corresponding mark bits set are modified. The remaining bytes return to CM unchanged.

Maintenance Registers

The Maintenance Registers monitor CMC and CM errors. The Maintenance Registers also provide

the means for testing and reconfiguring CM for maintenance purposes. MAC can transfer CMC Data error signals from a Maintenance Register to the MCU. MAC also loads various Maintenance Registers with MAC Data.

INSTRUCTION EXECUTION

An exchange sequence starts normal execution of program instructions. All instructions have the following common steps.

1. IF Instruction Assembly parcels out instruction.
2. Opcode addresses First Level Instruction Decoder.
3. Decoder output and instruction parcel load into IF buffer registers.
4. Rank 12 Opcode addresses first word of instruction's microand sequence in CST.

   Rank 12 P and Instruction Mux Bits load into ICP Rank 13 Register.
5. General Microand loads into General Microand Register in CST.

   Contents of instruction pipeline load into Rank 22 Register.

   The i, j, and k fields from ICP, RDSa, b, and c fields from General Microand, and RDSd field from Functional Unit Microand control reading and writing in Register File. Pipeline data remains latched in Rank 22 Register, feeding Rank 32 Register, until instruction exits.
6. General Microand and pipeline data load into Rank 32 Register. Go activates functional area specified by General Microand Functional Unit field.

From this point, instruction execution can proceed along a number of paths and depends on the unique requirements of each instruction specified by its microand sequence. The C180 instruction descriptions that follow demonstrate various uses of system hardware.

INTEGER SUM, (Xk) REPLACED BY (Xk) PLUS (Xj)

The arithmetic operation performed by this instruction takes place in ALN with operands provided from the Xk and Xj registers in the Register File. The sum returns to the Xk Register.

1. General Microand RDSb and c fields gate Rank 22 j and k Operand Select through OPI's Register File Address Select to Register File.
2. Functional Unit Microand departs CST at Time 31. It determines that add operation will be performed in ALN's Large Adder.
3. ICP generates Go at Time 32.

4. Operands addressed by j and k designators in Register File proceed to ALN at Time 40 as B and C Operands. C Operand goes to Large Adder. B Operand's path to Large Adder is through Multiply/Divide Network (no op).
   Response goes to ICP.

5. Large Adder Result enters ALN Output Mux. At Time 50 ALN Result is available to OPI.

6. Register File Address (k designator) arrives at Register File from delay circuit in Register File Address Select.

   ALN Result passes through DAI Register and enters Register File Xk register at Time 52.

If at any time before new data is written into the Xk register an error or exception occurs, ICC evaluates the error or exception to determine if an interrupt routine is required. The interrupt clears the pipeline, blocks the write into the Register File, and proceeds with a different microrand sequence.

LOAD Xk FROM (Aj) DISPLACED BY Q

The data word stored in CM location (Aj) plus eight times Q loads into the Register File Xk register.

This instruction uses the Address Formation network in AC and the PVA-to-RMA conversion circuitry in SM and LM to address a CM location.

The instruction sequence is as follows:

1. General Microrand's RDSa field selects Rank 22 j Operand Select in OPI to become A register read address.

   RDSd field selects Rank 22 k Operand Select as X register write address.

   Designator k enters delay circuit in Register File Address Select to address Register File when requested CM data arrives from LM.

   Rank 22 Immediate Operand provides quantity Q to Immediate Operand Select in OPI, where it is multiplied by eight (left-shifted three places).

2. Eight times Q goes to Address Formation network in AC as Address Offset.

   Byte number portion of PVA from Aj register enters Address Formation network as A/B Operand.

   PVA segment and ring numbers from Aj register enter PVA Register in SM as Register File Data.

3. AC Address Formation network adds Address Offset and A/B Operand to form Address Adder Byte Number, which becomes AC Address (lower). Tests determine if Address Specification Error has occurred.

   Segment number addresses Segment Map RAM. RAM supplies ASID portion of Segment Descriptor to AC.

PVA ring number goes to Key/Lock, Ring Validity Tests in SM. There Keys from P Register and ring number are compared to Access Control Fields of Segment Descriptor. Tests determine if the segment is invalid or SM Access Violation has occurred.

Functional unit field of General Micrand in ICP issues Instruction Issue Request Enable to LM.

4. ASID and Address Adder Byte Number enter LM as AC Address, the operand SVA.

   Instruction transfers to ICP Rank 41. Further movement in pipeline or along write address delay path in OPI is blocked until Response arrives in ICP from LM.

5. When Instruction Issue Request Enable arrives in LM, it initiates Cache Memory Addressing. If Cache Memory contains word, LM sends LM Read Data to DAI Register in OPI and generates Response.

   LM simultaneously forms RMA to obtain word from CM, provided SPT entry needed to produce RMA is in LM's Page Map RAM.

6. If word is not present in Cache Memory, LM Address and additional Control signals enter CMC through Input Port and perform CM read operation.

7. CM Read Data returns to LM, where it enters Cache Memory and proceeds to OPI as LM Read Data. LM blocks generation of Response until read data returns from CM. Response is further delayed if SPT entry needed to produce RMA is not in LM's Page Map RAM.

8. Once Response reaches ICP, instruction advances in pipeline and Register File write address in OPI places incoming LM Read Data in Xk register.

DECIMAL SUM, D(Ak) REPLACED BY D(Ak) PLUS D(Aj)

This BDP instruction adds decimal data field D(Ak) to decimal field D(Aj) and returns the result to CM as decimal data field D(Ak).

Ten microands are required to execute the instruction, which processes data field D(Aj) as A Stream Data, data field D(Ak) as B Stream Data and the result field D(Ak) as C Stream Data. Two 32-bit BDP descriptors accompany the instruction through IF and ICP to specify the field lengths, data types, and address offsets for the A and B streams.

The instruction sequence is as follows:

1. First micrand issues Go to BDP.

   Functional Unit Micrand enters BDP and remains latched there through course of instruction to control arithmetic operations.

   First two microands use j and k designators from ICP to address A registers.

   Contents of Aj and Ak registers load into scratch registers in Register File.

The next four microands utilize the contents of the two BDP descriptors to form the addresses needed to read A and B stream data from CM. Two microands produce the A stream SVA and two microands produce the B stream SVA.

2. First descriptor loads into Rank 22 Register in ICP. Because j and k designators are now no longer available in instruction pipeline for Register File addressing, subsequent microrands obtain Aj and Ak from scratch registers.

3. Contents for Aj register are read from Register File. Thirty-two least significant bits enter Address Formation network adder in AC as A/B Operand.

   Rank 22 Immediate Operand (offset field from first descriptor) reaches Address Formation network as Address Offset.

   Third addend is C Operand (A stream byte length field from descriptor).

   A stream byte length field also enters A/C Stream Length Counter to decrement when A stream data begins arriving from LM.

   Sixteen most significant bits from Aj register (ring and segment number) enter PVA Register in SM as Register File Data.

4. Invalid segment and access violation tests are performed and ASID is read from Segment Map RAM.

   Address Offset, A/B Operand, C Operand and -1 input are added in Address Formation network to form rightmost stream address. Sum enters A/C Stream Address Counter. (Output of counter is byte number portion of A stream SVA. Counter addresses successive A stream words in LM.)

   ASID proceeds to A/C Stream ASID Register in AC, where together with A/C Stream Address Count, ASID forms AC Address.

   AC generates A/C Stream LM Request to start A stream data transfer from LM.

5. Second descriptor loads into Rank 22 Register in ICP and B stream operations begin. B stream address formation circuitry includes adder, B Stream Length Counter, B Stream Address Counter, and B Stream ASID Register. Together they generate and update addresses needed to complete B stream data transfer to AC.

6. Once addresses are formed and requests submitted, LM returns 64-bit LM Read Data and Stream A/C or B Response to AC. Data enters A/C or B Stream Disassembly network, depending on which response signal is active. A/C or B Stream LM Requests return to LM as required, accompanied by new AC Addresses from counters. Appropriate length counter decrements with each word transfer.

   Disassembled A Stream Data and B Stream Data bytes enter BDP's A and B Stream Stages 1 through 3. Two streams are synchronized in Stage 3 by Pause A and B Stream signals, which return to AC to regulate data flow.

   ALU adds A and B Stream Data one digit at a time and places result in Buffer RAM for future output as C Stream Data.

7. A/C and B Stream LM Requests terminate once length counters in AC reach zero.

8. AC blocks returning C Stream Data with Pause C Stream while last group of microrands validates C stream PVA and generates SVA. AC Address for C Stream is recalculated B Stream SVA. AC Address is produced from saved contents of Ak Register and second descriptor's length and offset fields.

9. Once C stream SVA enters A/C Stream ASID Register and A/C Stream Address Counter, AC drops Pause C Stream.

   AC begins to assemble 64-bit LM Write Data words in C Stream Assembly network.

   When 64-bit word is assembled, AC issues A/C Stream LM Request to initiate write sequence to LM.

10. LM Write Data enters CM and associated Cache Memory locations.

    A/C Stream Address Counter forms next memory address. A/C Stream Length Counter decrements. AC continues to submit A/C Stream LM Requests and AC Addresses for each assembled word until A/C Stream Length Counter equals zero. LM acknowledges receipt of data with Stream A/C Response.

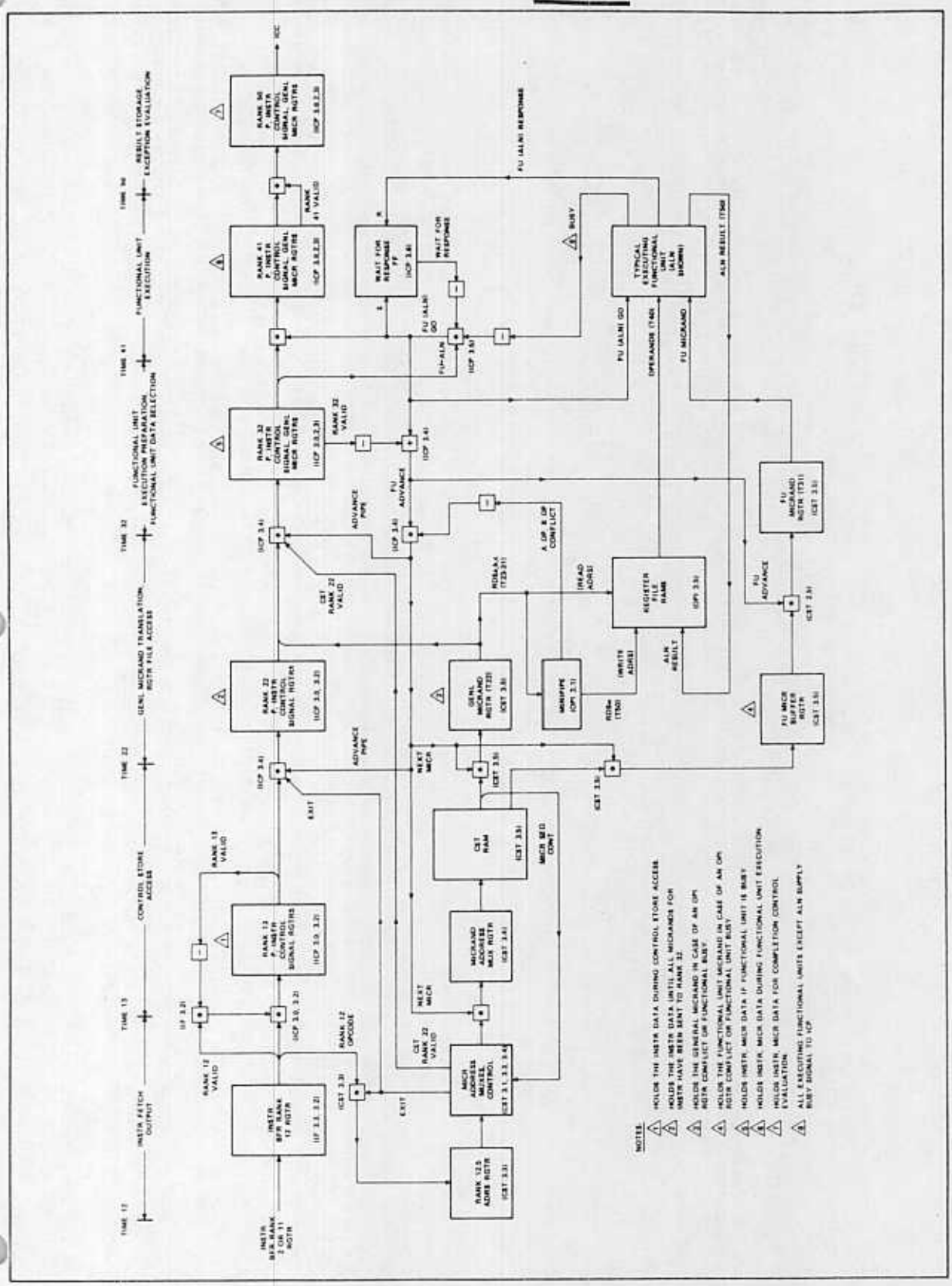


Figure 3-15. Instruction Unit Operation

ICP, CST, OPI, and ICC initiate and conclude execution of instructions IF obtains from memory. The role of ICC is reserved for discussion in section 6.

The CP's instruction buffering hardware, which pipelines instructions through IF and ICP, accommodates a maximum of 14 instructions/micrands. Included are as many as four unassembled instructions in IF. Ranks 2, 3, 10, 11, 12, and 13 in IF and ICP contain assembled instructions. The remaining ranks in ICP contain individual micrands associated with the instruction in the process of executing. An instruction's micrands advance through four execution stages in the ICP. One micrand enters a given stage after another departs.

If an instruction is already in the pipeline when its memory copy is changed, a self-modifying code error exists. Hardware provides the means to prevent execution of these unmodified instructions, but CP performance is reduced substantially when the feature is used.

A simplified picture of the coordinated operation of ICP, CST, OPI, and a typical executing functional unit is shown in figure 3-15.

The following sequence is based on signals and hardware shown in figure 3-15. A more detailed view of the hardware associated with instruction execution is available in the Level 3 diagrams referred to in figure 3-15.

1. Formatted instruction enters Instruction Buffer Rank 12 Register from Instruction Buffer Rank 2 or 11 if Rank 12 valid is inactive.

2. Rank 12 Valid activates to latch instruction in Rank 12.

3. At conclusion of micrand sequence of instruction currently in Rank 22, Micrand Sequence Control generates exit. Last micrand enters General Micrand Register and FU Micrand Buffer Register.

   Contents of Rank 12.5 Register enter Micrand Address Mux Register. Register contains first CST RAM address associated with instruction in Rank 13.

4. Exit gates Rank 12 Opcode into Rank 12.5 Address Register and partially enables instruction in Rank 13 to Rank 22.

5. Second-to-last General Micrand of Rank 22 instruction activates FU Go while in Rank 32 and initiates micrand-controlled execution in Functional Unit. FU Go activates, provided response signal associated with previous micrand clears Wait For Response FF and Functional Unit the micrand needs to use is not busy. FU Go enters selected functional unit to latch Functional Unit Micrand into holding register.

6. FU Go gates General Micrand from Rank 32 to Rank 41, activates FU Advance, and sets Wait For Response FF.

7. FU Advance generates Advance Pipeline and Next Micrand, provided micrand entering Rank 41 does not have operand conflict. (Movement of micrands in pipeline may be delayed until required operands are available to Functional Unit receiving FU Go.)

   FU Advance gates last FU Micrand of Rank 22 instruction to FU Micrand Register from FU Micrand Buffer Register.

8. Advance Pipe and CST Rank 22 Valid (a derivative of Next Micrand) gate final General Micrand of Rank 22 instruction to Rank 32. Rank 22 instruction fields enter Rank 32 for last time (these fields accompany all micrands of instruction through pipeline).

Advance Pipe and Exit gate next instruction from Rank 13 to Rank 22.

First micrand associated with new instruction entering Rank 22 enters General Micrand Register and FU Micrand Buffer Register.

Micrand Sequence Control field from same micrand enters Micrand Address Mux Register to select next micrand from CST RAM.

9. Operand read addresses (RDSa, b, c) for first micrand of new instruction begin Register File access. Read addresses also are compared to contents of Minipipe delay network to detect possible conflicts.

   Register File write address (RSDw) for first micrand of new instruction enters Minipipe. Delay circuit synchronizes entry of write address into Register File with arrival of result.

10. Rank 12 Valid and inactive Rank 13 Valid gate instruction from Rank 12 to Rank 13.

11. Instruction from Instruction Buffer Rank 2 or 11 enters Instruction Buffer Rank 12.

12. Final General Micrand of first instruction activates FU Go.

13. Operation associated with FU Go begins in Functional Unit, employing operands from Register File RAMs under Functional Unit Micrand Control.

14. Steps 6 and 7 repeat. (Variation - first FU Micrand of new Rank 22 instruction enters FU Micrand Register in step 7.)

15. Advance Pipe and CST Rank 22 Valid gate first General Micrand of new instruction to Rank 32 along with new P and Instruction Control Signals.

    Second micrand associated with new instruction in Rank 22 enters General Micrand Register and Functional Unit Micrand Buffer Register.

    Second Micrand Sequence Control field associated with new instruction in Rank 22 enters Micrand Address Register to select third micrand from CST RAM.

16. Step 9 repeats (with fields from second General Micrand).

17. Result of operation associated with last micrand of first instruction proceeds to location in Register File addressed by RDSw.

18. First micrand of new Rank 22 instruction activates FU Go, provided Response associated with previous micrand has cleared Wait For Response FF and Functional Unit the micrand intends to use is not busy.

19. Operation associated with FU Go begins in Functional Unit, employing operands from Register File RAMs under Functional Unit Micrand Control.

20. Steps 6 and 7 repeat. In step 6 new P and Instruction Control Signals enter Rank 44 with General Micrand. In step 7 second FU Micrand enters FU Micrand Register.

21. Advance Pipe and CST Rank 22 Valid gate second General Micrand of Rank 22 instruction to Rank 32.

    Third micrand associated with Rank 22 instruction enters General Micrand Register and Functional Unit Micrand Buffer Register.

Third Microrand Sequence Control field associated with Rank 22 instruction enters Microrand Address Register to select fourth Microrand from CST RAM.

22. Step 9 repeats (with fields from third General Microrand).

23. Result of first microrand operation associated with Rank 22 instruction proceeds to Register File. Register File is addressed by RDSw (which entered Minipipe in step 9).

Steps 1 through 23 repeat until the instruction sequence is exhausted or an interrupt occurs. Traps, calls, and exchanges are typical means of ending one instruction sequence and starting another.

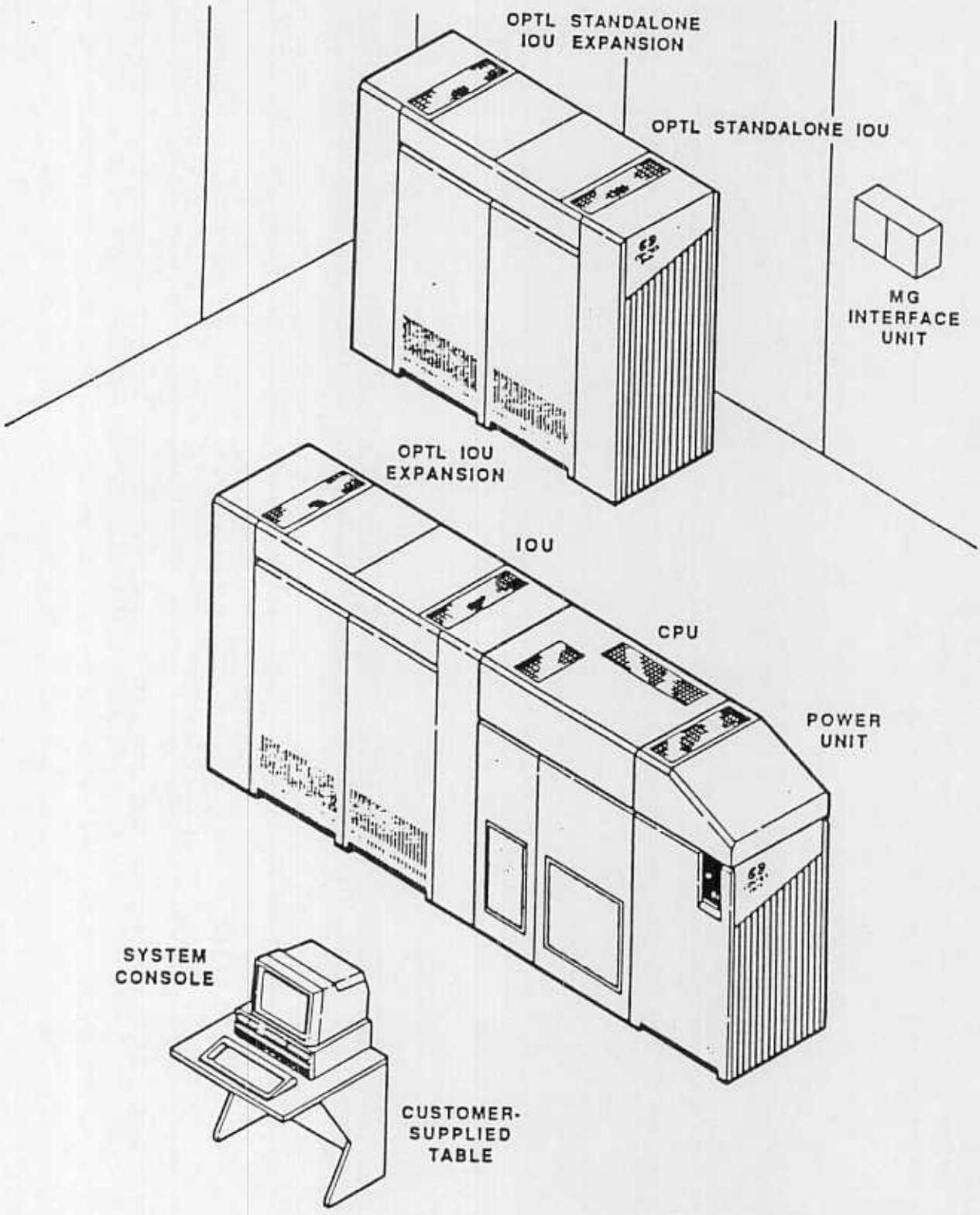

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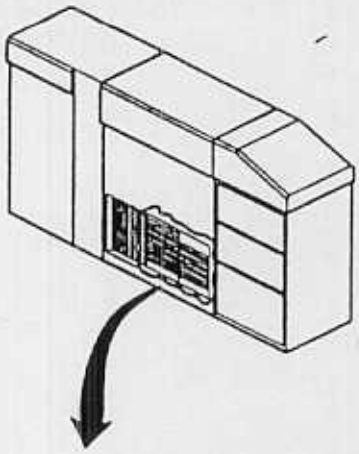
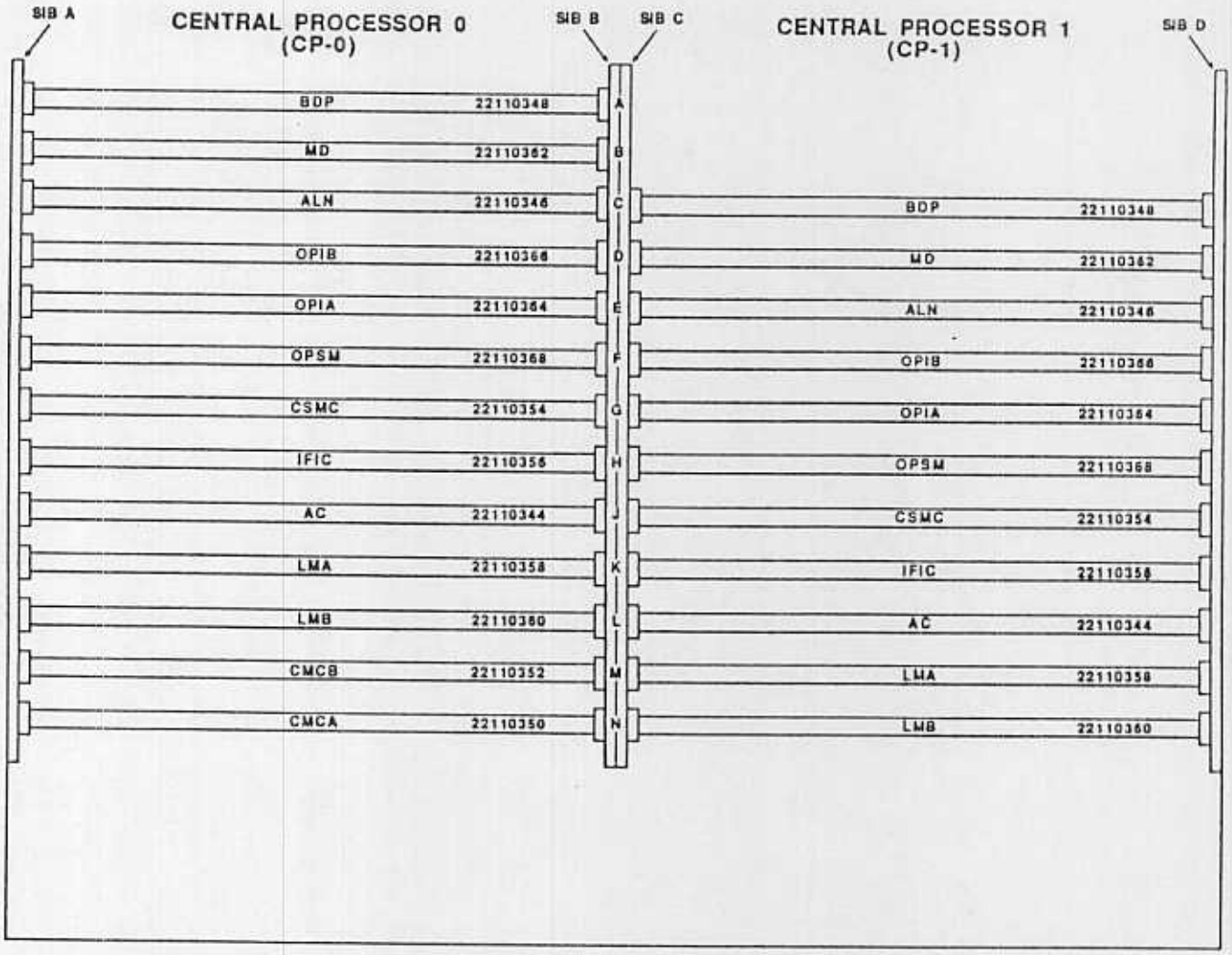
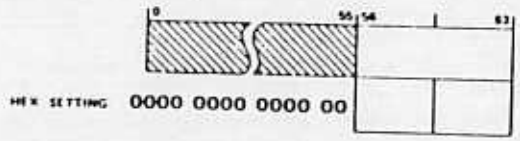
TABLE




SIB A
CENTRAL PROCESSOR 0
(CP-0)
SIB B
SIB C
CENTRAL PROCESSOR 1
(CP-1)
SIB D
BDP 22110348
MD 22110362
ALN 22110346
OPIB 22110366
OPIA 22110364
OPSM 22110368
CSMC 22110354
IFIC 22110356
AC 22110344
LMA 22110358
LMB 22110360
CMCB 22110352
CMCA 22110350
A
B
C
D
E
F
G
H
J
K
L
M
N
BDP 22110348
MD 22110362
ALN 22110346
OPIB 22110366
OPIA 22110364
OPSM 22110368
CSMC 22110354
IFIC 22110356
AC 22110344
LMA 22110358
LMB 22110360

STATUS SUMMARY REGISTER (00)

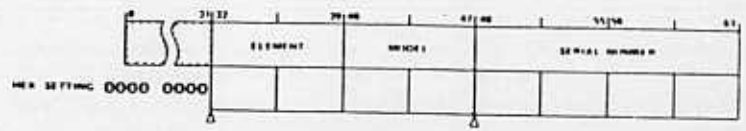


PIP3 STATUS SUMMARY REGISTER 00

0 - 55 (Not Used)

56. (Not Used)
57. (Not Used)
58. C180 Monitor Mode
59. Short Warning
60. Processor Halt
61. Uncorrectable Error
62. Corrected Error
63. Long Warning

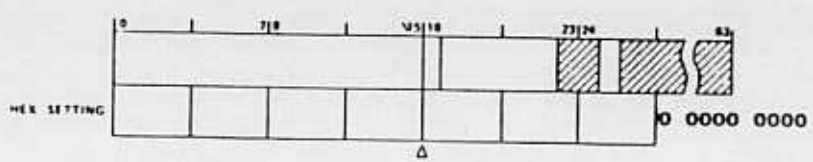
EID REGISTER (10)



P3 and PIP3 ELEMENT I.D. REGISTER 10

P3	855	30
P3	845	31
P3	860	32
P3	860 A	32
P3	870 A	32 - Dual Proc.
P3	850	33
P3	850 A	33
P3	840	34
P3	840 A	34
P3	845 S	35
P3	855 S	36
P3	840 S	37
PIP3	960	3A

OI REGISTERS (12)



OPTIONS INSTALLED REGISTER 12

Bits 0 - 63 All Bits Unused.

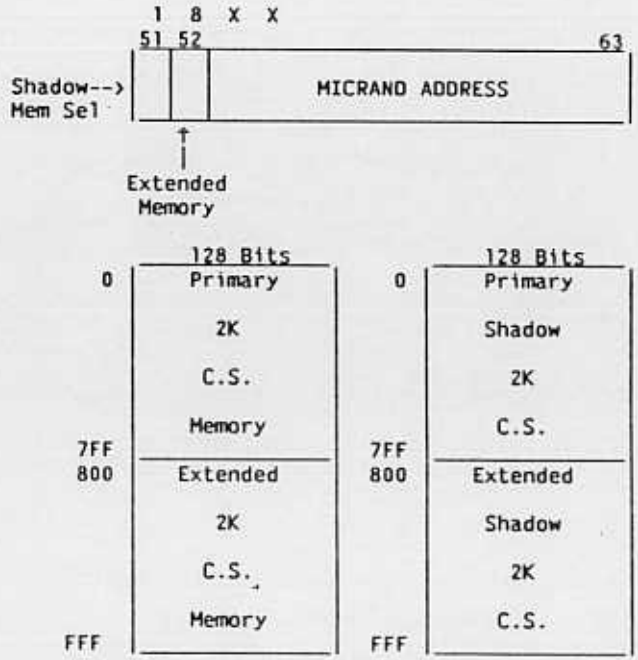
960 DEC REG. 30 (PIP)

BIT		GENERATOR AFFECTED	PAGE	SIB OUT	SIB IN
32		Enable SHADOW MEMORY	CST4.0-11	AC 7163	CSMC 3078
33		Test Mode Enabled	CST4.0-02	AC 7167	CSMC 3080
34		Enable First Failure Capture	CST4.1-00	AC 7169	CSMC 3084
35		Disable Corrected Error to SS	MAC4.0-06	AC 7173	CSMC 3086
36		Page Map Enable Set 0	LM4.6A-01	AC 8002	LMB 6013
37		Page Map Enable Set 1	LM4.6B-01	AC 8006	LMB 6017
38		Page Map Enable Set 2	LM4.6C-01	AC 8008	LMB 6019
39					
40		Segment Map Enable Set 0	SM4.0-05	AC 5122	OPSM 3192
41		Segment Map Enable Set 1	SM4.0-05	AC 5126	OPSM 3083
42		CST RAM Sweep Enable	CST4.0-06	AC 7175	CSMC 3090
43		Enable PDM Halt	CST4.0-05	AC 7179	CSMC 3092
44		Breakpoint Enable	CST4.0-10	AC 7181	CSMC 3096
45		Step Enable	CST4.0-06	AC 7185	CSMC 2098
46		Enable Expanded CST	CST4.0-11	AC 7187	CSMC 3102
47		Disable PDMs	CST4.3-00	AC 7191	CSMC 3104
48		Control Store Expan (Future Use)	CST4.0-11	*	
49		Not Used	NU		
50		Enable Lookahead (DISABLED)	LM4.0-09		
51		Enable Block Request	LM4.0-09		
52		Retry Limit	ICC4.1-12	LMA 7023	IFIC 7168
53		Retry Limit	ICC4.1-12	LMA 7025	IFIC 7170
54		Retry Limit	ICC4.1-12	LMA 7029	IFIC 7174
55		Retry Limit	ICC4.1-12	LMA 7031	IFIC 7176
56		Retry Limit	ICC4.1-12	LMA 7035	IFIC 7180
57		Enable Cache Set 0	LM4.8A-07		
58		Enable Cache Set 1	LM4.8B-07		
59		Enable Cache Set 2	LM4.8C-07		
60		Enable Cache Set 3	LM4.8D-07		
61		Cache Fake Central Memory	LM4.0-05		
62		Force Real Memory Address	LM4.0-02		
63		Not Used	NU		

* Selection of Address when Expanded Control Store enabled. When Clear, the expansion reflects CY170/CY180 state. When Set, the expansion bit is under toggle control via the MCS field.

MICROCODE SPACE

SHADOW BIT 32	EXTENDED BIT 46	
0	0	PRIMARY 2K MICRANDS
0	1	EXTENDED 2K MICRANDS
1	0	PRIMARY SHADOW 2K MICRANDS
1	1	EXTENDED SHADOW 2K MICRANDS



PFS REGISTER 80

BIT	SIGNAL	PAGE	DESCRIPTION	AC SIB/CHIP
0	SUE	ICC4.0-02	Uncorrected Error MCR(0)	7161
1	SCE	ICC4.0-10	Corrected Error	7155
2	PFSAC(56)	OPI4.7-02	Address Fanin PE Byte 2	8019
3	PFSAC(57)	OPI4.7-02	Address Fanin PE Byte 3	8023
4	PFSAC(58)	AC4.2-04	Address Fanin PE Byte 4	106J7-7
5	PFSAC(59)	AC4.2-04	Address Fanin PE Byte 5	106H9-7
6	PFSAC(60)	AC4.2-04	Address Fanin PE Byte 6	106H1-7
7	PFSAC(61)	AC4.2-04	Address Fanin PE Byte 7	106G3-7
8	PFSAC(8)	AC4.0-00	Input Data Strm PE Byte 0	30F5-7
9	PFSAC(9)	AC4.0-00	Input Data Strm PE Byte 1	30G3-7
10	PFSAC(10)	AC4.0-00	Input Data Strm PE Byte 2	30H1-7
11	PFSAC(11)	AC4.0-00	Input Data Strm PE Byte 3	30H9-7
12	PFSAC(12)	AC4.0-00	Input Data Strm PE Byte 4	30K5-7
13	PFSAC(13)	AC4.0-00	Input Data Strm PE Byte 5	30L3-7
14	PFSAC(14)	AC4.0-00	Input Data Strm PE Byte 6	30M1-7
15	PFSAC(15)	AC4.0-00	Input Data Strm PE Byte 7	30J7-7
16	PFSAC(16)	AC4.0-01	A Data Strm Hold Reg PE Byte 0	14A7-6
17	PFSAC(17)	AC4.0-01	A Data Strm Hold Reg PE Byte 1	14B5-6
18	PFSAC(18)	AC4.0-01	A Data Strm Hold Reg PE Byte 2	30E7-6
19	PFSAC(19)	AC4.0-01	A Data Strm Hold Reg PE Byte 3	22F5-6
20	PFSAC(20)	AC4.0-01	A Data Strm Hold Reg PE Byte 4	22N7-6
21	PFSAC(21)	AC4.0-01	A Data Strm Hold Reg PE Byte 5	22P5-6
22	PFSAC(22)	AC4.0-01	A Data Strm Hold Reg PE Byte 6	14P5-6
23	PFSAC(23)	AC4.0-01	A Data Strm Hold Reg PE Byte 7	14T1-6
24	PFSAC(24)	AC4.1-00	B Data Strm Hold Reg PE Byte 0	14C3-6
25	PFSAC(25)	AC4.1-00	B Data Strm Hold Reg PE Byte 1	22C3-6
26	PFSAC(26)	AC4.1-00	B Data Strm Hold Reg PE Byte 2	22D1-6
27	PFSAC(27)	AC4.1-00	B Data Strm Hold Reg PE Byte 3	22D9-6
28	PFSAC(28)	AC4.1-00	B Data Strm Hold Reg PE Byte 4	22M1-6
29	PFSAC(29)	AC4.1-00	B Data Strm Hold Reg PE Byte 5	22M9-6
30	PFSAC(30)	AC4.1-00	B Data Strm Hold Reg PE Byte 6	14N7-6
31	PFSAC(31)	AC4.1-00	B Data Strm Hold Reg PE Byte 7	14R3-6

BIT	SIGNAL	PAGE	DESCRIPTION	AC SIB/CHIP
32	PFSAC(32)	OPI4.4-09	A Stream SVA Latch PE Byte 0	8001
33	PFSAC(33)	OPI4.4-09	A Stream SVA Latch PE Byte 1	8005
34	PFSAC(34)	OPI4.4-09	B Stream SVA Latch PE Byte 0	8007
35	PFSAC(35)	OPI4.4-09	B Stream SVA Latch PE Byte 1	8011
36	PFSAC(2)	AC4.2-01	OPI Address PE Byte 0	22J7-7
37	PFSAC(3)	AC4.2-01	OPI Address PE Byte 1	22K5-7
38	PFSAC(0)	AC4.4-04	OPI Address PE Byte 0	74K6-W14
39	PFSAC(1)	AC4.4-04	OPI Address PE Byte 1	74K6-Y17
40	PFSAC(40)	AC4.2-06	Recovery Address PE Byte 0	106K5-7
41	PFSAC(41)	AC4.2-06	Recovery Address PE Byte 1	106L3-7
42	PFSAC(42)	AC4.2-06	Recovery Address PE Byte 2	106M1-7
43	PFSAC(43)	AC4.2-06	Recovery Address PE Byte 3	106M9-7
44	PFSALN(40)	ALN4.4-01	ALN Soft Control PE	7001
45	PFSAC(45)	AC4.6-01	AC Soft Control PE PAK 1	46K6-Y1
46	PFSAC(46)	AC4.5-01	AC Soft Control PE PAK 2	46N0-Y1
47	PFSAC(36)	AC4.2-05	Shift Count PE	82F5-6
48	PFSAC(6)	AC4.4-04	A Length Counter PE	74K6-V14
49	PFSAC(7)	AC4.4-04	B Length Counter PE	74K6-W16
50	PFSAC(37)	AC4.0-01	Aj In Mux PE	30D9-7
51	PFSAC(38)	AC4.1-00	Ak In Mux PE	106F5-7
52	PFSAC(39)	AC4.0-00	Left Bit Shift PE	38H1-7
53	PFSALN(41)	ALN4.1-06	Convert to Bin Data Byte PE	8017
54	PFSBDP(26)	BDP4.7-02	Ak Port Input PE	7079
55	PFSBDP(23)	BDP4.7-02	Aj Port Input PE	7073
56	PFSBDP(6)	BDP4.7-02	Reg File A Address Count PE	7029
57	PFSBDP(7)	BDP4.7-02	Reg File B Address Count PE	7031
58	PFSBDP(8)	BDP4.7-02	Reg File A Data PE	7035
59	PFSBDP(18)	BDP4.7-02	Reg File B Data PE	7005
60	PFSBDP(10)	BDP4.7-02	Convert ALU PE	7037
61	PFSBDP(17)	BDP4.7-02	Limit Reg PE	7049
62	PFSBDP(16)	BDP4.7-02	Stage 7 PE	7047
63	Internal	MAC4.2-03	PFS PAK 1 PE (Board 0)	

PFS REGISTER 81

BIT		SIGNAL	PAGE	DESCRIPTION	AC SIB/CHIP
0		PFSBDP(5)	BDP4.7-02	Input Stream Buffer Address PE	7025
1		PFSBDP(11)	BDP4.7-02	Output Stage 2 PE	7083
2		PFSBDP(21)	BDP4.7-02	RAM Pak1-Mem A/B Address PE	7065
3		PFSBDP(22)	BDP4.7-02	RAM Pak1-Mem A/B Data PE	7067
4		PFSBDP(14)	BDP4.7-02	Port j 2nd Data Latch PE	7071
5		PFSBDP(15)	BDP4.7-02	Port k 2nd Data Latch PE	7077
6		PFSBDP(12)	BDP4.7-02	Aj Descriptor Latch PE	7007
7		PFSBDP(13)	BDP4.7-02	Ak Descriptor Latch PE	7011
8		PFSBDP(20)	BDP4.7-02	RAM Pak0-Mem A Address PE	7061
9		PFSBDP(24)	BDP4.7-02	RAM Pak0-Mem A Data PE	7053
10		PFSBDP(19)	BDP4.7-02	RAM Pak0-Mem B Address PE	7059
11		PFSBDP(25)	BDP4.7-02	RAM Pak0-Mem B Data PE	7055
12		PFSBDP(0)	BDP4.7-02	Micrand Reg PE Bytes 0-1	7013
13		PFSBDP(1)	BDP4.7-02	Micrand Reg PE Bytes 2-3	7017
14		PFSBDP(2)	BDP4.7-02	Micrand Reg PE Bytes 4-5	7019
15		PFSBDP(3)	BDP4.7-02	Micrand Reg PE Bytes 6-7	7023
16		AC	AC4.7-00	Clock Chip PE	
17		CMCB		Clock Chip PE	5043
18		CSU		Clock Chip PE	1031
19		CXSU		Clock Chip PE	1174
20		HI			
21		HI			
22		HI			
23		HI			

PFS REGISTER 82

BIT	SIGNAL	PAGE	DESCRIPTION	LMA SIB/CHIP
0	PFSBDP(4)	BDP4.7-02	Scale Counter PE	2071
1	PFSBDP(9)	BDP4.7-02	Edit Mask PE	2073
2	PFSLM(0)	LM4.1-02	Cache Addr Reg PE Byte 0	98J8-W8
3	PFSLM(1)	LM4.1-02	Cache Addr Reg PE Byte 1	98J8-Y5
4	PFSLM(2)	LM4.1-02	Cache Addr Reg PE Byte 2	98J8-W6
5	PFSLM(3)	LM4.1-02	Cache Addr Reg PE Byte 3	98J8-V8
6	PFSLM(4)	LM4.2-04	Cache Addr Reg PE Byte 4	98G4-E17
7	PFSLM(5)	LM4.2-04	Cache Addr Reg PE Byte 5	98G4-B20
8	PFSLM(6)	LM4.9-02	Cache Write Data PE Byte 0	22R4-Y3/7126
9	PFSLM(7)	LM4.9-02	Cache Write Data PE Byte 1	22R4-V6/7128
10	PFSLM(8)	LM4.9-02	Cache Write Data PE Byte 2	22R4-Y2/7132
11	PFSLM(9)	LM4.9-02	Cache Write Data PE Byte 3	22R4-U5/7134
12	PFSLM(10)	LM4.9-02	Cache Write Data PE Byte 4	22R4-W3/7138
13	PFSLM(11)	LM4.9-02	Cache Write Data PE Byte 5	22R4-V4/7140
14	PFSLM(12)	LM4.9-02	Cache Write Data PE Byte 6	22R4-U3/7144
15	PFSLM(13)	LM4.9-02	Cache Write Data PE Byte 7	22R4-V2/7146
16	PFSLM(14)	LM4.9-00	Cache Multi Hit (-MTHIT)	22R4-B16
17	PFSLM(15)	LM4.9-01	Cache Multi Allocate	22R4-A16
18	PFSLM(16)	LM4.4-02	Tag File PE	22L4-B10
19	PFSLM(17)	LM4.4-02	Tag File Addr PE	22L4-Y1
20	PFSOPI(0)	SM4.4-00	LM Mux Pointer-Direct CMC Data	2175
21	PFSOPI(1)	SM4.4-00	LM Mux Pointer-Cache Read Data	2176
22	PFSOPI(2)	SM4.4-00	LM Mux Pointer-Read Mem Addr	2179
23	PFSOPI(3)	SM4.4-00	LM Mux Pointer-Buff CMC Data	2180
24	PFSLM(18)	LM4.9-02	Cache Write Data From CPU PE	22R4-W4
25	PFSLM(19)	LM4.9-02	Cache Write Data From CM PE	22R4-V5
26	PFSLM(20)	LM4.3-11	Cache Assoc Tag PE (-CHTGPE)	46L4-B3
27	PFSLM(21)	LM4.9-02	Cache Mark PE	22R4-U6
28	PFSLM(22)	LM4.3-12	Cache Addr Reg PE Invalidate	46L4-C4
29	PFSLM(23)	LM4.3-12	Cache Addr Reg PE Addr Control	46L4-C3
30	PFSLM(24)	LM4.3-12	Cache Addr Reg PE Inst Fetch	46L4-D4
31	PFSLM(25)	LM4.3-12	Cache Addr Reg PE Internal	46L4-A1

BIT	SIGNAL	PAGE	DESCRIPTION	LMA SIB/CHIP
32	PFSLM(26)	LM4.0-08	LM MODIFIED PAGE CODE	74K6-A9
33	PPFSLM(27)	LM4.0-08	LM Input PE from Mcode Byte 0	74K6-C10
34	PFSLM(28)	LM4.0-08	LM Input PE from Mcode Byte 1	74K6-B9
35	PFSLM(29)	LM4.6-04	High	
36	PFSLM(30)	LM4.6-02	Map LRU PE Set 0 (MPLRPE)	2074
37	PFSLM(31)	LM4.6-02	Map LRU PE Set 1 (MPLRPE)	2080
38	PFSLM(32)	LM4.6-02	Map LRU PE Set 2 (MPLRPE)	2086
39	PFSLM(33)	LM4.6-02	Map LRU PE Set 3 (MPLRPE)	2092
40	PFSLM(34)	LM4.6-02	Map Assoc PE Set 0 (MPASPE)	2072
41	PFSLM(35)	LM4.6-02	Map Assoc PE Set 1 (MPASPE)	2078
42	PFSLM(36)	LM4.6-02	Map Assoc PE Set 2 (MPASPE)	2084
43	PFSLM(37)	LM4.6-02	Map Assoc PE Set 3 (MPASPE)	2090
44	PFSLM(38)	LM4.10-01	Map Page Frame Addr PE	98N0-V6
45	---------	---------	Not Used	
46	---------	---------	Not Used	
47	---------	---------	Not Used	
48	PFSLM(42)	LM4.10-05	Page Table Length PE	98N0-V12
49	PFSLM(43)	LM4.10-05	Page Table Addr PE	98N0-C15
50	PFSLM(44)	LM4.10-05	Page Offset Parity Error	98N0-A18
51	PFSLM(45)	LM4.2-02	Page Size Mask PE	98G4-V16
52	PFSLM(46)	LM4.3-09	Exchange Tag PE	46L4-U18
53	---------	---------	Not Used	
54	---------	---------	Not Used	
55	---------	---------	Not Used	
56	PFSLM(50)	LM4.9-06	CM Corrected Write	22R4-B18
57	PFSLM(51)	LM4.9-06	CM Corrected Read	22R4-D16
58	PFSLM(52)	LM4.9-06	CM Uncorrected Write	22R4-C16
59	PFSLM(53)	LM4.9-06	CM Uncorrected Read	22R4-A19
60	PFSLM(54)	LM4.9-06	CM Reject	22R4-B17
61	PFSLM(55)	LM4.9-06	CM Response Code PE	22R4-D15
62	PFSLM(56)	LM4.4-04	CM Tag PE	22L4-A11
63	Internal	MAC4.3-03	PFS Pak2 PE (Board 1)	

PFS REGISTER 83

BIT	SIGNAL	PAGE	DESCRIPTION	LMA SIB/CHIP
0	PFSLM(57)	LM4.3-11	Cache Addr PE Set 0 CADR	46L4-C4
1	PFSLM(58)	LM4.3-11	Cache Addr PE Set 1 CADR	46L4-C3
2	PFSLM(59)	LM4.3-11	Cache Addr PE Set 2 CADR	46L4-D4
3	PFSLM(60)	LM4.3-11	Cache Addr PE Set 3 CADR	46L4-A1
4	PFSLM(61)	LM4.9-01	Cache Tag RAM PE Set 0 CRAM	22R4-W18
5	PFSLM(62)	LM4.9-01	Cache Tag RAM PE Set 1 CRAM	22R4-U16
6	PFSLM(63)	LM4.9-01	Cache Tag RAM PE Set 2 CRAM	22R4-Y19
7	PFSLM(64)	LM4.9-01	Cache Tag RAM PE Set 3 CRAM	22R4-V16
8	PFSOPI(4)	SM4.4-00	Cache Mux PE Set 0	2181
9	PFSOPI(5)	SM4.4-00	Cache Mux PE Set 1	2182
10	PFSOPI(6)	SM4.4-00	Cache Mux PE Set 2	2185
11	PFSOPI(7)	SM4.5-00	Cache Mux PE Set 3	2186
12	PFSOPI(8)	SM4.5-00	DAI Mux PE 0 LM	2187
13	PFSOPI(9)	SM4.5-00	DAI Mux PE 1 AC	2188
14	PFSOPI(10)	SM4.5-00	DAI Mux PE 2 ALN	2191
15	PFSOPI(11)	SM4.5-00	DAI Mux PE 3 FU	2192
16	LMA	LM4.16-00	Clock Chip PE	74N8-C16
17	LMB	LM4.15-00	Clock Chip PE	2096
18	CMCA	CMC4.17-00	Clock Chip PE	2098
19	HI			
20	HI			
21	HI			
22	HI			
23	HI			

PFS REGISTER 84

BIT	SIGNAL	PAGE	DESCRIPTION	OPSM SIB/CHIP
0	PFSSG(0)	SM4.0-09	Set 0 Parity Error	22J8-W12
1	PFSSG(1)	SM4.0-09	Set 1 Parity Error	22J8-Y9
2	PFSSG(8)	SM4.0-09	Seg Map Output PE Byte 0	22J8-A11
3	PFSSG(9)	SM4.0-09	Seg Map Output PE Byte 1	22J8-B11
4	PFSSG(10)	SM4.0-09	Seg Map Output PE Byte 2	22J8-A12
5	PFSSG(11)	SM4.0-09	Seg Map Output PE Byte 3	22J8-C11
6	PFSSG(12)	SM4.0-09	Seg Map Output PE Byte 4	22J8-B12
7	PFSSG(13)	SM4.0-09	Seg Map Output PE Byte 5	22J8-A13
8	PFSSG(20)	SM4.4-03	Seg Table Length PE Byte 0	74J8-W1
9	PFSSG(21)	SM4.4-03	Seg Table Length PE Byte 1	74J8-T4
10	PFSSG(22)	SM4.0-11	Job Mode STA PE Byte 0	22J8-A14
11	PFSSG(23)	SM4.0-11	Job Mode STA PE Byte 1	22J8-C12
12	PFSSG(16)	SM4.5-03	New P Reg PE Byte 0	74G4-U4
13	PFSSG(17)	SM4.5-03	New P Reg PE Byte 1	74G4-Y1
14	PFSSG(18)	SM4.5-03	New P Reg PE Byte 2	74G4-U3
15	PFSSG(19)	SM4.5-03	New P Reg PE Byte 3	74G4-V2
16	PFSSG(7)	SM4.0-11	Addr Input PE Byte 0	22J8-C9
17	PFSSG(6)	SM4.0-11	Addr Input PE Byte 1	22J8-A7
18	PFSSG(4)	SM4.4-03	Addr Input PE Byte 2	74J8-U5
19	PFSSG(5)	SM4.4-03	Addr Input PE Byte 3	74J8-W3
20	PFSSG(2)	SM4.0-09	Bypass Reg PE	22J8-V10
21	PFSSG(3)	SM4.0-09	Seg Map Valid RAMS Error	22J8-W19
22	PFSSG(14)	SM4.0-11	Seg Map Micrand PE Byte 0	22J8-A6
23	PFSSG(15)	SM4.0-11	Seg Map Micrand PE Byte 1	22J8-B8
24	PFSSG(24)	SM4.4-06	Input Purge Code PE	74J8-A10
25	PFSIC(12)	ICP4.1-02	Data Type Rank 32 PE	3128
26	PFSIC(13)	ICP4.2-02	Jk Rank 32 PE	3144
27	PFSIC(8)	ICP4.2-07	UTP Rank 50 (16-23) PE	3109
28	PFSIC(4)	ICP4.0-07	UTP Rank 50 (32-39) PE	3110
29	PFSIC(5)	ICP4.1-07	UTP Rank 50 (40-47) PE	3126
30	PFSIC(6)	ICP4.2-07	UTP Rank 50 (48-55) PE	3138
31	PFSIC(7)	ICP4.0-07	UTP Rank 50 (56-63) PE	3116

BIT	SIGNAL	PAGE	DESCRIPTION	OPSM SIB/CHIP
32	PFSIC(14)	ICC4.0-07	Write Data PE (0-7)	3085
33	PFSIC(15)	ICC4.0-07	Write Data PE (8-15)	3089
34	PFSIC(10)	ICP4.1-05	WDS(24,25)RDSw(29-31)Rank 41 PE	3132
35	PFSIC(9)	ICP4.0-05	General Micrand PE (16-23)	3120
36	PFSIC(0)	ICP4.0-07	P Reg PE (0-7)	3108
37	PFSIC(1)	ICP4.1-07	P Reg PE (8-15)	3122
38	PFSIC(2)	ICP4.2-07	P Reg PE (16-23)	3134
39	PFSIC(3)	ICP4.0-07	P Reg PE (24-31)	3114
40	PFSIC(11)	ICP4.2-05	RDSw PE (32-39)	3146
41	PFSIC(20)	ICC4.1-08	Successful Retry	3158
42	PFSIC(17)	ICP4.3-12	Deadman Timeout	3170
43	PFSIC(18)	SM4.5-02	Debug Mask PE	3162
44	PFSIC(16)	ICC4.0-01	PDM on MAC Operation	3090
45	PFSIC(19)	ICC4.1-13	Retry Counter PE	3156
46	PFSIC(21)	ICC4.1-06	Exchange malfunction	3152
47	PFSIC(22)	ICC4.1-11	DUE1 Before PONR MCR(0)	3091
48	PFSOPI(27)	OPI4.1-04	DAI Data PE Byte 0	1091
49	PFSOPI(28)	OPI4.1-04	DAI Data PE Byte 1	1095
50	PFSOPI(29)	OPI4.1-04	DAI Data PE Byte 2	1097
51	PFSOPI(30)	OPI4.1-04	DAI Data PE Byte 3	1101
52	PFSOPI(31)	OPI4.4-02	DAI Data PE Byte 4	2091
53	PFSOPI(32)	OPI4.4-02	DAI Data PE Byte 5	2095
54	PFSOPI(33)	OPI4.4-02	DAI Data PE Byte 6	2097
55	PFSOPI(34)	OPI4.4-02	DAI Data PE Byte 7	2101
56	PFSOPI(35)	OPI4.0-03	Write Addr Mini-Pipe PE	4017
57	PFSOPI(36)	OPI4.2-00	Reg File Data Out PE Bytes 0-3	4019
58	PFSOPI(37)	OPI4.3-01	Reg File Data Out PE Bytes 4-7	3005
59	PFSOPI(25)	OPI4.1-04	Tag PE	1089
60	----------	---------	Not Used	
61	----------	---------	Not Used	
62	----------	---------	Not Used	
63	Internal	MAC4.4-03	PFS Pak3 PE (Board 2)	

PFS REGISTER 85

BIT	SIGNAL	PAGE	DESCRIPTION	OPSM SIB/CHIP
0	PFSOPI(12)	OPI4.1-04	XIC 220 PE 0	1049
1	PFSOPI(13)	OPI4.1-04	XIC 220 PE 1	1053
2	PFSOPI(14)	OPI4.1-04	XIC 220 PE 2	1055
3	PFSOPI(15)	OPI4.1-04	XIC 220 PE 3	1059
4	PFSOPI(16)	OPI4.1-04	SIC 221 PE 0	1061
5	PFSOPI(17)	OPI4.1-04	SIC 221 PE 1	1065
6	PFSOPI(18)	OPI4.1-04	SIC 221 PE 2	1067
7	PFSOPI(19)	OPI4.1-04	SIC 221 PE 3	1071
8	PFSOPI(20)	OPI4.1-04	XIC 223 PE 0	1073
9	PFSOPI(21)	OPI4.1-04	XIC 223 PE 1	1077
10	PFSOPI(22)	OPI4.1-04	RDSw PE 0	1079
11	PFSOPI(23)	OPI4.1-04	RDSw PE 1	1083
12	PFSOPI(24)	OPI4.1-04	XIC 221 PE	1085
13	----------	---------	Not Used	
14	----------	---------	Not Used	
15	----------	---------	Not Used	
16	OPSM	SM4.6-00	Clock Chip PE	
17	OPIB	OPI4.10-00	Clock Chip PE	2103
18	OPIA	OPI4.9-00	Clock Chip PE	2107
19	HI			2104
20	HI			
21	HI			
22	HI			
23	HI			

PFS REGISTER 86

BIT	SIGNAL	PAGE	DESCRIPTION	IFIC SIB/CHIP
0	--------	---------	Not Used	
1	--------	---------	Not Used	
2	--------	---------	Not Used	
3	PFSCST(0)	CST4.0-06	Micr Addr PE	4115
4	PFSCST(1)	MAC4.0-10	Micro RAMS Data Fanout PE Even	4125
5	PFSCST(2)	MAC4.0-10	Micro RAMS Data Fanout PE Odd	4127
6	PFSCST(3)	CST4.0-03	Micr Seg Control (0-7) PE	4109
7	PFSCST(4)	CST4.0-03	Micr Seg Control (8-15) PE	4113
8	PFSCST(5)	CST4.3-00	Func Unit Micr BFR PE Byte 0	4041
9	PFSCST(6)	CST4.3-00	Func Unit Micr BFR PE Byte 1	4047
10	PFSCST(7)	CST4.3-00	Func Unit Micr BFR PE Byte 2	4049
11	PFSCST(8)	CST4.3-00	Func Unit Micr BFR PE Byte 3	4059
12	PFSCST(9)	CST4.3-00	Func Unit Micr BFR PE Byte 4	4055
13	PFSCST(10)	CST4.3-00	Func Unit Micr BFR PE Byte 5	4053
14	PFSCST(11)	CST4.3-00	Func Unit Micr BFR PE Byte 6	4061
15	PFSCST(12)	CST4.3-00	Func Unit Micr BFR PE Byte 7	4065
16	PFSCST(13)	CST4.4-00	Func Unit Micr Reg PE Byte 0	4067
17	PFSCST(14)	CST4.4-00	Func Unit Micr Reg PE Byte 1	4071
18	PFSCST(15)	CST4.4-00	Func Unit Micr Reg PE Byte 2	4073
19	PFSCST(16)	CST4.4-00	Func Unit Micr Reg PE Byte 3	4085
20	PFSCST(17)	CST4.4-00	Func Unit Micr Reg PE Byte 4	4083
21	PFSCST(18)	CST4.4-00	Func Unit Micr Reg PE Byte 5	4077
22	PFSCST(19)	CST4.4-00	Func Unit Micr Reg PE Byte 6	4089
23	PFSCST(20)	CST4.4-00	Func Unit Micr Reg PE Byte 7	4091
24	PFSCST(21)	CST4.6-00	General Micr Reg PE Byte 2	4029
25	PFSCST(22)	CST4.6-00	General Micr Reg PE Byte 3	4023
26	PFSCST(23)	CST4.6-00	General Micr Reg PE Byte 4	4025
27	PFSCST(24)	CST4.6-00	General Micr Reg PE Byte 5	4031
28	PFSCST(25)	CST4.6-00	General Micr Reg PE Byte 6	4035
29	PFSCST(26)	CST4.6-00	General Micr Reg PE Byte 7	4037
30	PFSOPI(39)	OPI4.8-00	A Start, X Start PE	7047
31	PFSOPI(40)	OPI4.8-01	A Terminate, X Terminate PE	6035

BIT	SIGNAL	PAGE	DESCRIPTION	IFIC SIB/CHIP
32	PFSMAC(0)	MAC4.0-1	MAC Read Path PE	4119
33	PFSMAC(1)	MAC4.0-1	MCH PE	4121
34	PFSMAC(2)	MAC4.1-11	MAC Data Fanout PE	4095
35	PFSMAC(3)	MAC4.1-11	MAC Bus Data PE	4097
36	PFSMAC(4)	MAC4.1-11	RAM Addr Mux PE	4101
37	PFSMAC(5)	MAC4.1-11	Addr Translation Mux PE	4103
38	PFSMAC(6)	MAC4.1-11	REF ROM PE	4107
39	PFSOPI(38)	OPI4.8-00	N Counter PE	6001
40	PFSIF(0)	IF4.0-01	C170 Odd RAM Pak0 PE	74D2-E4
41	PFSIF(2)	IF4.0-01	C170 Even RAM Pak0 PE	74D2-C2
42	PFSIF(1)	IF4.0-01	C180 RAM Pak0 PE	74D2-B1
43	PFSIF(17)	IF4.0-02	IB12 (0-7) Pak0 PE	74D2-W14
44	PFSIF(18)	IF4.0-02	IB12 (9-16) Pak0 PE	74D2-Y17
45	PFSIF(19)	IF4.0-02	IB12 (18-22) Pak0 PE	74D2-V13
46	PFSIF(21)	IF4.0-02	IB12 (39-47) Pak0 PE	74D2-Y16
47	PFSIF(20)	IF4.0-02	IB12 (30-38) Pak0 PE	74D2-W15
48	PFSIF(3)	IF4.1-01	C170 Odd RAM Pak1 PE	74J0-E4
49	PFSIF(5)	IF4.1-01	C170 Even RAM Pak1 PE	74J0-C2
50	PFSIF(4)	IF4.1-01	C180 RAM Pak1 PE	74J0-B1
51	PFSIF(22)	IF4.1-02	IB12 (0-7) Pak1 PE	74J0-W14
52	PFSIF(23)	IF4.1-02	IB12 (9-16) Pak1 PE	74J0-Y17
53	PFSIF(25)	IF4.1-02	IB12 (39-47) Pak1 PE	74J0-Y16
54	PFSIF(24)	IF4.1-02	IB12 (30-38) Pak1 PE	74J0-W15
55	---------	--------	Not Used	
56	PFSIF(6)	IF4.5-00	BRA (0-7) PE	98C3-7
57	PFSIF(7)	IF4.5-00	BRA (8-15) PE	98D1-7
58	PFSIF(8)	IF4.5-00	BRA (16-23) PE	106D9-7
59	PFSIF(9)	IF4.5-00	BRA (24-31) PE	98E7-7
60	PFSIF(10)	IF4.5-00	BRB (8-15) PE	98F5-7
61	PFSIF(11)	IF4.5-00	BRB (16-23) PE	98G3-7
62	PFSIF(12)	IF4.5-00	BRB (24-31) PE	98H1-7
63	Internal	MAC4.5-03	PFS Pak4 PE (Board 3)	

PFS REGISTER 87

BIT	SIGNAL	PAGE	DESCRIPTION	IFIC SIB/CHIP
0	PFSIF(13)	IF4.4-01	Branch Addr (0-7) PE	74F7-A9
1	PFSIF(14)	IF4.4-06	Branch Addr (8-15) PE	74F7-Y14
2	PFSIF(15)	IF4.4-06	Branch Addr (16-23) PE	74F7-W13
3	PFSIF(16)	IF4.4-09	Branch Addr (24-31) PE	74F7-C7
4	PFSIF(56)	IF4.5-01	IFAD (32-39) PE	106C3-34
5	PFSIF(57)	IF4.5-01	IFAD (40-47) PE	106C3-6
6	PFSIF(58)	IF4.5-01	IFAD (48-55) PE	106D1-34
7	PFSIF(59)	IF4.5-01	IFAD (56-63) PE	106D1-6
8	PFSIF(26)	IF4.2-00	IB02 (0-7) PE	46F5-34
9	PFSIF(27)	IF4.2-00	IB02 (8-15) PE	46F5-6
10	PFSIF(28)	IF4.2-00	IB02 (16-23) PE	46G3-34
11	PFSIF(29)	IF4.2-00	IB02 (24-31) PE	46G3-6
12	PFSIF(38)	IF4.2-01	IB11 (0-7) PE	54F5-34
13	PFSIF(39)	IF4.2-01	IB11 (8-15) PE	54F5-6
14	PFSIF(40)	IF4.2-01	IB11 (16-23) PE	54G3-34
15	PFSIF(41)	IF4.2-01	IB11 (24-31) PE	54G3-6
16	IFIC	IF4.8-00	Clock Chip PE	
17	CLK	CLK4.1-00	Clock Chip PE	3001
18	BDP	BDP4.13-00	Clock Chip PE	6005
19	PFSOR(0)	MAC 4.2-06	1st Fail 4D01 AC - 80, 81	7156
20	PFSOR(1)	MAC 4.3-06	1st Fail 4D02 LMA - 82, 83	3101
21	PFSOR(2)	MAC 4.4-06	1st Fail 4D03 OPSM - 84, 85	7049
22	PFSOR(3)	MAC 4.5-06	1st Fail 4D04 IFIC - 86, 87	22H9-53
23	PFSOR(4)	MAC 4.6-06	1st Fail 4D05 ALN - 88, 89	7013

PFS REGISTER 88

BIT	SIGNAL	PAGE	DESCRIPTION	ALN SIB/CHIP
0	PFSIF(42)	IF4.4-16	IAPR (0-7) PE	2072
1	PFSIF(43)	IF4.4-16	IAPR (8-15) PE	2074
2	PFSIF(44)	IF4.4-16	IAPR (16-23) PE	2078
3	PFSIF(45)	IF4.4-16	IAPR (24-31) PE	2080
4	PFSIF(46)	IF4.4-16	IAPR (32-39) PE	2084
5	PFSIF(47)	IF4.4-16	IAPR (40-47) PE	2086
6	PFSIF(48)	IF4.4-16	IAPR (48-55) PE	2090
7	PFSIF(49)	IF4.4-16	IAPR (56-63) PE	2092
8	PFSIF(50)	IF4.4-16	IAPRA (48-55) PE	2096
9	PFSIF(51)	IF4.4-16	IAPRA (56-63)	2098
10	PFSIF(52)	IF4.4-01	PMUX (0-7) PE	2018
11	PFSIF(53)	IF4.4-09	PMUX (8-15) PE	2102
12	PFSIF(54)	IF4.4-09	PMUX (16-23) PE	2104
13	PFSIF(55)	IF4.4-09	PMUX (24-31) PE	2108
14	PFSALN(62)	ALN4.1-06	Soft Control Reg PE 0	5089
15	PFSALN(63)	ALN4.1-06	Soft Control Reg PE 1	5091
16	PFSALN(0)	ALN4.1-06	Multiply C Reg PE Byte 0	54A7-55
17	PFSALN(1)	ALN4.1-06	Multiply C Reg PE Byte 1	54A7-56
18	PFSALN(2)	ALN4.1-06	Multiply C Reg PE Byte 2	54A7-01
19	PFSALN(3)	ALN4.1-06	Multiply C Reg PE Byte 3	54A7-02
20	PFSALN(4)	ALN4.1-06	Multiply C Reg PE Byte 4	54A7-41
21	PFSALN(5)	ALN4.1-06	Multiply C Reg PE Byte 5	54A7-40
22	PFSALN(6)	ALN4.1-06	Multiply C Reg PE Byte 6	54A7-39
23	PFSALN(7)	ALN4.1-06	Multiply C Reg PE Byte 7	54A7-37
24	PFSALN(8)	ALN4.1-06	Multiply B Reg PE Byte 0	22K6-A2
25	PFSALN(9)	ALN4.1-06	Multiply B Reg PE Byte 1	22K6-D5
26	PFSALN(10)	ALN4.1-06	Multiply B Reg PE Byte 2	22K6-B3
27	PFSALN(11)	ALN4.1-06	Multiply B Reg PE Byte 3	22K6-C4
28	PFSALN(12)	ALN4.1-06	Multiply B Reg PE Byte 4	22K6-C3
29	PFSALN(13)	ALN4.1-06	Multiply B Reg PE Byte 5	22K6-D4
30	PFSALN(14)	ALN4.1-06	Multiply B Reg PE Byte 6	22K6-E4
31	PFSALN(15)	ALN4.1-06	Multiply B Reg PE Byte 7	22K6-C5

BIT	SIGNAL	PAGE	DESCRIPTION	ALN SIB/CHIP
32	PFSALN(16)	ALN4.3-10	Gen Net Adder PE 0	54M1-11
33	PFSALN(17)	ALN4.3-10	Gen Net Adder PE 1	46M1-11
34	PFSALN(18)	ALN4.3-10	Gen Net Adder PE 2	38M1-11
35	PFSALN(19)	ALN4.3-10	Gen Net Adder PE 3	30M1-11
36	PFSALN(20)	ALN4.3-10	Gen Net Adder PE 4	22M1-11
37	PFSALN(21)	ALN4.3-10	Gen Net Adder PE 5	14M1-11
38	PFSALN(22)	ALN4.3-10	Gen Net Adder PE 6	46M9-11
39	PFSALN(23)	ALN4.3-10	Gen Net Adder PE 7	22M9-11
40	PFSALN(24)	ALN4.3-10	Gen Net Adder PE 8	14M9-11
41	PFSALN(25)	ALN4.3-10	Gen Net Adder PE 9	38N7-11
42	PFSALN(26)	ALN4.3-10	Gen Net Adder PE 10	30N7-11
43	PFSALN(27)	ALN4.3-10	Gen Net Adder PE 11	22N7-11
44	PFSALN(28)	ALN4.3-10	Gen Net Adder Carry Miscomp 0	54M1-5
45	PFSALN(29)	ALN4.3-10	Gen Net Adder Carry Miscomp 1	46M1-5
46	PFSALN(30)	ALN4.3-10	Gen Net Adder Carry Miscomp 2	38M1-5
47	PFSALN(31)	ALN4.3-10	Gen Net Adder Carry Miscomp 3	30M1-5
48	PFSALN(32)	ALN4.3-10	Gen Net Adder Carry Miscomp 4	22M1-5
49	PFSALN(33)	ALN4.3-10	Gen Net Adder Carry Miscomp 5	14M1-5
50	PFSALN(34)	ALN4.3-10	Gen Net Adder Carry Miscomp 6	46M9-5
51	PFSALN(35)	ALN4.3-10	Gen Net Adder Carry Miscomp 7	22M9-5
52	PFSALN(36)	ALN4.3-10	Gen Net Adder Carry Miscomp 8	14M9-5
53	PFSALN(37)	ALN4.3-10	Gen Net Adder Carry Miscomp 9	38N7-5
54	PFSALN(38)	ALN4.3-10	Gen Net Adder Carry Miscomp 10	30N7-5
55	PFSALN(39)	ALN4.3-10	Gen Net Adder Carry Miscomp 11	22N7-5
56	----------	---------	Not used	
57	----------	---------	Not used	
58	PFSALN(42)	ALN4.1-06	Shift PE 0	22K6-T4
59	PFSALN(43)	ALN4.1-06	Shift PE 1	22K6-U3
60	PFSALN(44)	ALN4.1-06	Mult Carry Miscomp 0	106L3-5
61	PFSALN(45)	ALN4.1-06	Mult Carry Miscomp 1	98L3-5
62	----------	---------	Not used	
63	Internal	MAC4.6-03	PFS Pak5 PE (Board 4)	

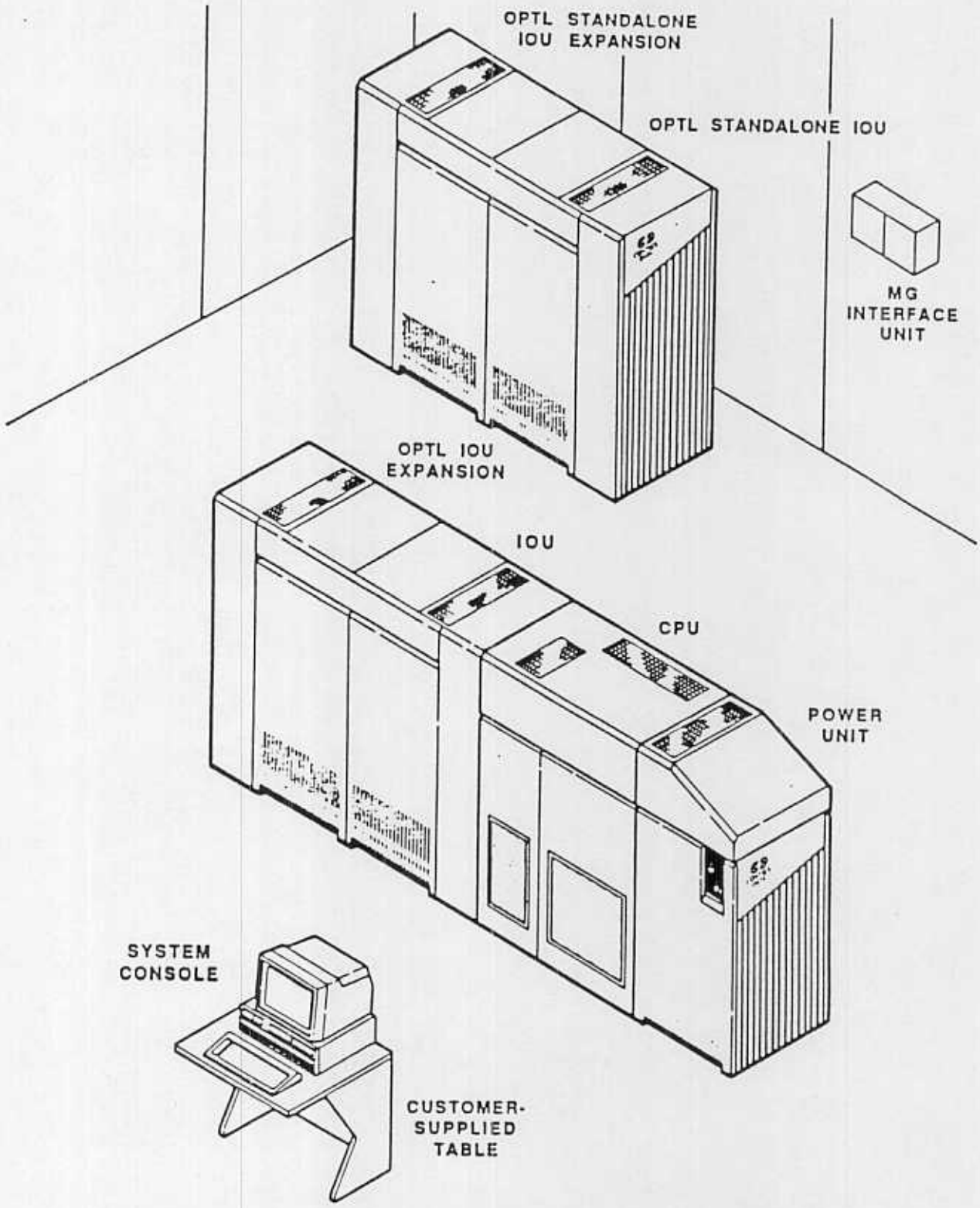
PFS REGISTER 89

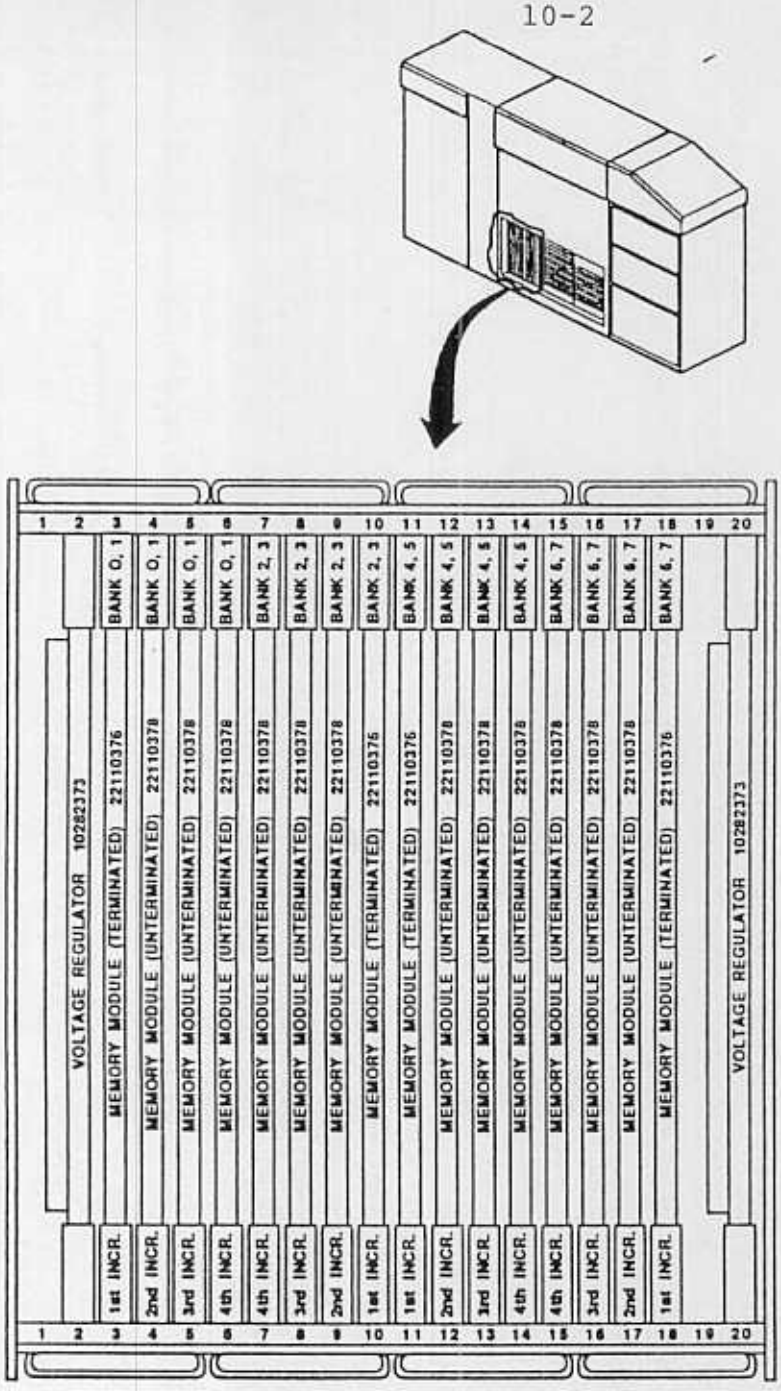
BIT	SIGNAL	PAGE	DESCRIPTION	ALN SIB/CHIP
0	PFSALN(46)	ALN4.1-06	Multi Carry Miscomp 2	90L3-5
1	PFSALN(47)	ALN4.1-06	Multi Carry Miscomp 3	82L3-5
2	PFSALN(48)	ALN4.1-06	Multi Carry Miscomp 4	74L3-5
3	PFSALN(49)	ALN4.1-06	Multi Carry Miscomp 5	66L3-5
4	PFSALN(50)	ALN4.1-06	Multi Carry Miscomp 6	54L3-5
5	PFSALN(51)	ALN4.1-06	Multi Carry Miscomp 7	46L3-5
6	PFSALN(52)	ALN4.1-06	Multi Carry Miscomp 8	46M1-5
7	----------	---------	Not used	
8	PFSALN(54)	ALN4.1-06	Micrand Reg PE Byte 0	22K6-V7
9	PFSALN(55)	ALN4.1-06	Micrand Reg PE Byte 1	22K6-W5
10	PFSALN(56)	ALN4.1-06	Micrand Reg PE Byte 2	22K6-W7
11	PFSALN(57)	ALN4.1-06	Micrand Reg PE Byte 3	22K6-Y4
12	PFSALN(58)	ALN4.1-06	Micrand Reg PE Byte 4	22K6-W6
13	PFSALN(59)	ALN4.1-06	Micrand Reg PE Byte 5	22K6-V2
14	PFSALN(60)	ALN4.1-06	Micrand Reg PE Byte 6	22K6-W3
15	PFSALN(61)	ALN4.1-06	Micrand Reg PE Byte 7	22K6-W1
16	ALN	ALN4.7-00	Clock Chip PE	
17	MD	ALN4.8-00	Clock Chip PE	6005
18	MD	ALN4.8-00	MD Clock Chip PE	6007
19			HI	
20			HI	
21			HI	
22			HI	
23			HI	

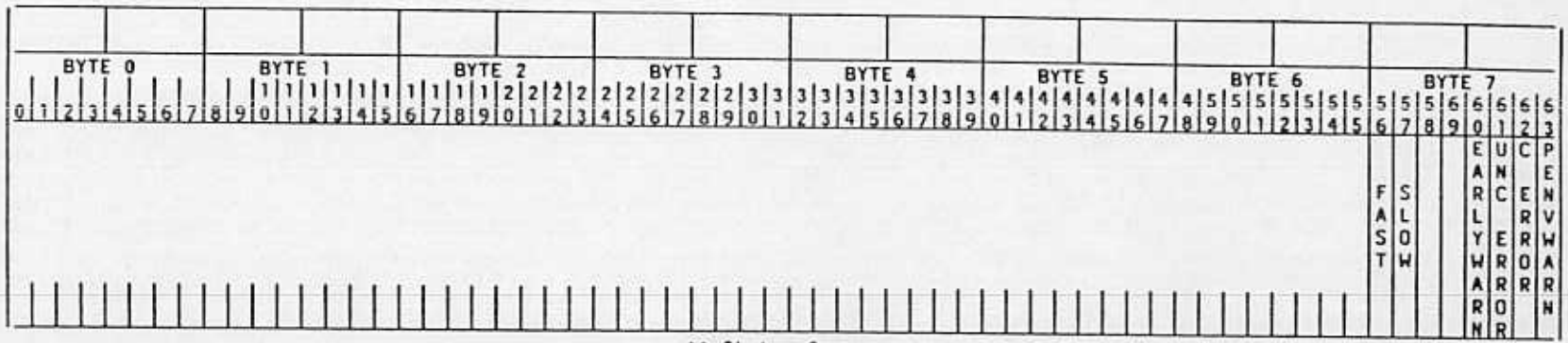
PIP-960 - PROCESSOR TEST MODE REGISTER (PTM, A0)

BIT	PAGE	GENERATOR AFFECTED	OUT-SIB	IN-SIB/CHIP
0	AC4.2-02	Addr Cont, Data to Length Counter	OPSM 1002	AC 1061
1	AC4.2-00	Addr Cont, 8-bit Adder	OPSM 1006	AC 1065
2	AC4.2-05	Addr Cont, ALN Shift Count	OPSM 1008	AC 1067
3	BDP4.7-02	BDP, AJ Port Formatting	OPSM 1103	BDP 1062
4	BDP4.7-02	BDP, AK Port Formatting	OPSM 1107	BDP 1066
5	BDP4.7-02	BDP, Scan Reg File Addr	OPSM 1109	BDP 1068
6	BDP4.0-00	BDP, Spec Error ROM Addr	OPSM 8044	BDP 8044
7	BDP4.5-02	BDP, Encode	OPSM 1115	BDP 1072
8	ICC4.0-15	Test Retry Hardware	OPSM 1014	IFIC 1113
9	AC4.2-06	Addr Control, MARK LINES	OPSM 6006	AC 6013
10	LM4.2-03	Local Mem, Page Offset	OPSM 2012	LMA 2077
11	LM4.1-01	Local Mem, Segment/Page ID	OPSM 2018	LMA 2079
12	OPI4.0-03	Op Iss, Wr Addr Pipeline Input	OPSM 2109	OPIA 2018
13	OPI4.1-01	Op Iss, Data Subfunct Select	OPSM 2113	OPIB 2116
14	OPI4.1-01	Op Issue, Literal Data	OPSM 2115	OPIB 2120
15	CST4.3-00	Instr Fetch, Instr Decode Muxes	OPSM 1012	CSMC 1007
16	ALN4.0-02	ALN, Force C Reg PE	IFIC 8067	MD 8002
17	ALN4.3-07	ALN, Force Shift Fault	IFIC 8049	ALN 8036
18	MAC4.0-00	MAC, Data Output Force 0 Parity	IFIC 8065	CSMC 8150
19	CMC4.10-04	CMC Partial Parity Disable	IFIC 8002	CMCA 2085
20	CMC4.10-01	CSU Partial Parity Disable	IFIC 8006	CMCA 2089
21	----------	Not Used		
22	LM4.0-11	LM, Purge Addr Count Parity Inv	IFIC 6068	LMA 6191
23	LM4.6-04	LM, Pg Map Status Parity Inv Set 0	IFIC 6084	LMB 6001
24	LM4.6-04	LM, Pg Map Status Parity Inv Set 1	IFIC 6086	LMB 6005
25	LM4.6-04	LM, Pg Map Status Parity Inv Set 2	IFIC 6090	LMB 6007
26	LM4.6-04	LM, Pg Map Status Parity Inv Set 3	IFIC 6092	LMB 6011
27	LM4.4-00	LM, Tag File Parity Invert	IFIC 6072	LMA 6002
28	LM4.3-10	LM, LM Tag to CMC Parity Invert	IFIC 6074	LMA 6006
29	CMC4.11-04	CMC Response Code Parity Invert	IFIC 1008	CMCB 3168
30	LM4.10-03	LM, RMA Parity Invert Byte 0	IFIC 6078	LMA 6008
31	LM4.10-03	LM, RMA Parity Invert Byte 1	IFIC 6080	LMA 6012

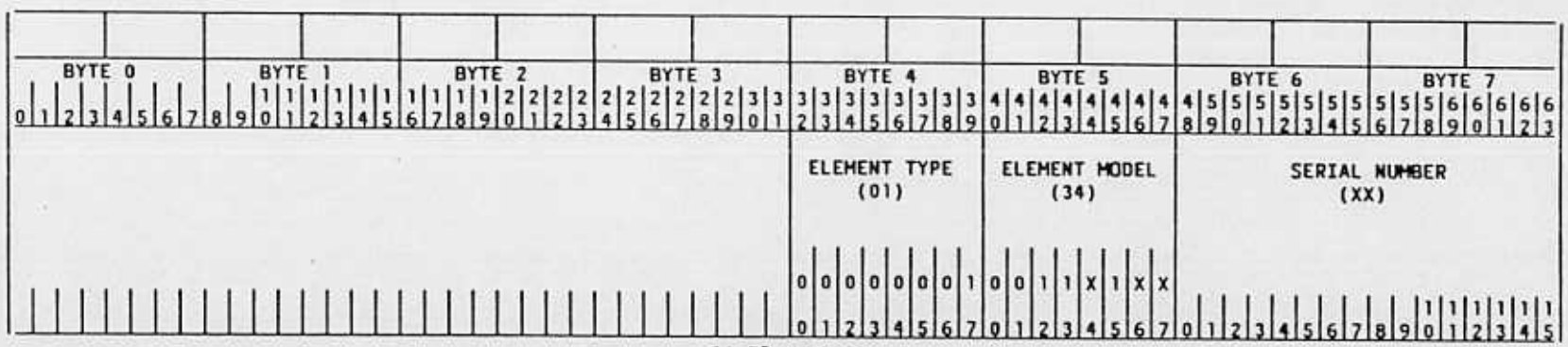
BIT	PAGE	GENERATOR AFFECTED	OUT-SIB	IN-SIB/CHIP
32	LM4.10-03	LM, RMA Parity Invert Byte 2	ALN 8002	LMA 8001
33	LM4.10-03	LM, RMA Parity Invert Byte 3	ALN 8006	LMA 8005
34	LM4.3-09	Loc Mem Func Code CMC Parity Invert	ALN 8008	LMA 8007
35	OPI4.1-01	Op Iss Data Subfunc Sel(w/PTM[13])	ALN 2012	OPIB 2071
36	OPI4.0-00	Op Iss, Force PE on RDSW Inst Cont	ALN 8012	OPIA 8001
37	OPI4.7-00	Op Iss, Force PE on Microsec Counter		
38	----------	Not Used		
39	OPI4.9-01	Force Cache Set (1) Allocate	ALN 8014	LMA 8011
40	LM4.4-03	Set Tag File (0) Full	ALN 8018	LMA 8013
41	LM4.4-03	Set Tag File (1) Full	ALN 8020	LMA 8017
42	LM4.4-03	Set Tag File (2) Full	ALN 8024	LMA 8019
43	LM4.14-06	Force LRU Parity=0 on Cache Tag Bds	ALN 8026	LMA 8023
44	OPI4.0-03	Force LM Tag Error	ALN 8030	OPIA 8005
45	----------	Not Used		
46	----------	Not Used		
47	----------	Not Used		
48	----------	Zero		
49	----------	Zero		
50	----------	Zero		
51	----------	Zero		
52	----------	Zero		
53	----------	Zero		
54	----------	Zero		
55	----------	Zero		
56	----------	Zero		
57	----------	Zero		
58	----------	Zero		
59	----------	Zero		
60	----------	Zero		
61	----------	Zero		
62	----------	Zero		
63	----------	Zero		


OPTL STANDALONE
IOU EXPANSION
OPTL STANDALONE IOU
MG
INTERFACE
UNIT
OPTL IOU
EXPANSION
IOU
CPU
POWER
UNIT
SYSTEM
CONSOLE
CUSTOMER-
SUPPLIED
TABLE

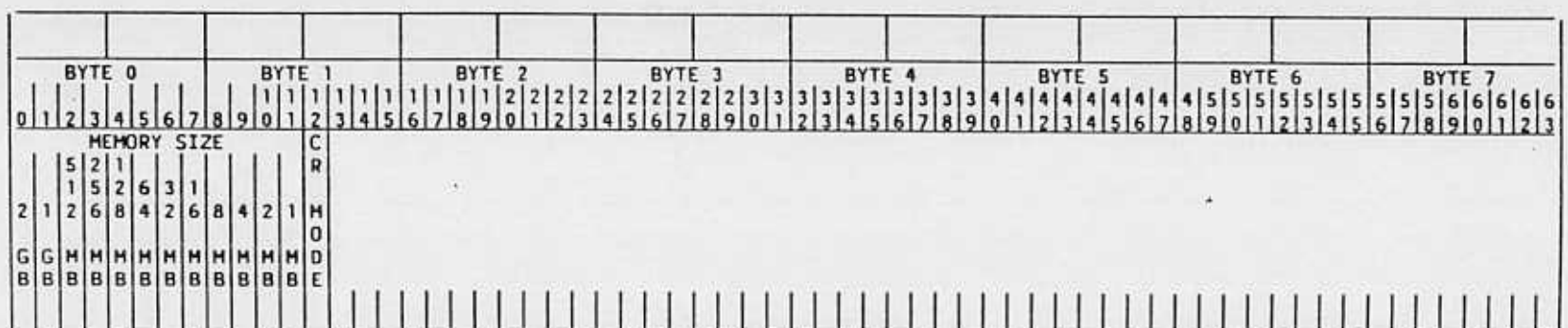

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
VOLTAGE REGULATOR 10282373
MEMORY MODULE (TERMINATED) 22110376
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (TERMINATED) 22110376
MEMORY MODULE (TERMINATED) 22110376
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (UNTERMINATED) 22110378
MEMORY MODULE (TERMINATED) 22110376
VOLTAGE REGULATOR 10282373
BANK 0, 1
BANK 0, 1
BANK 0, 1
BANK 0, 1
BANK 2, 3
BANK 2, 3
BANK 2, 3
BANK 2, 3
BANK 4, 5
BANK 4, 5
BANK 4, 5
BANK 4, 5
BANK 6, 7
BANK 6, 7
BANK 6, 7
BANK 6, 7
1st INCR.
2nd INCR.
3rd INCR.
4th INCR.
4th INCR.
3rd INCR.
2nd INCR.
1st INCR.
1st INCR.
2nd INCR.
3rd INCR.
4th INCR.
4th INCR.
3rd INCR.
2nd INCR.
1st INCR.
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20



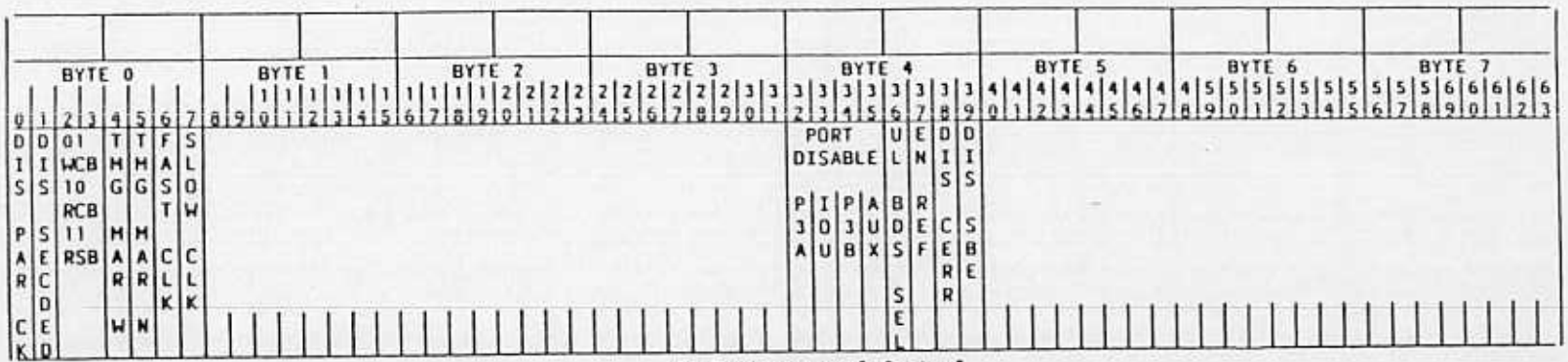
00 Status Summary



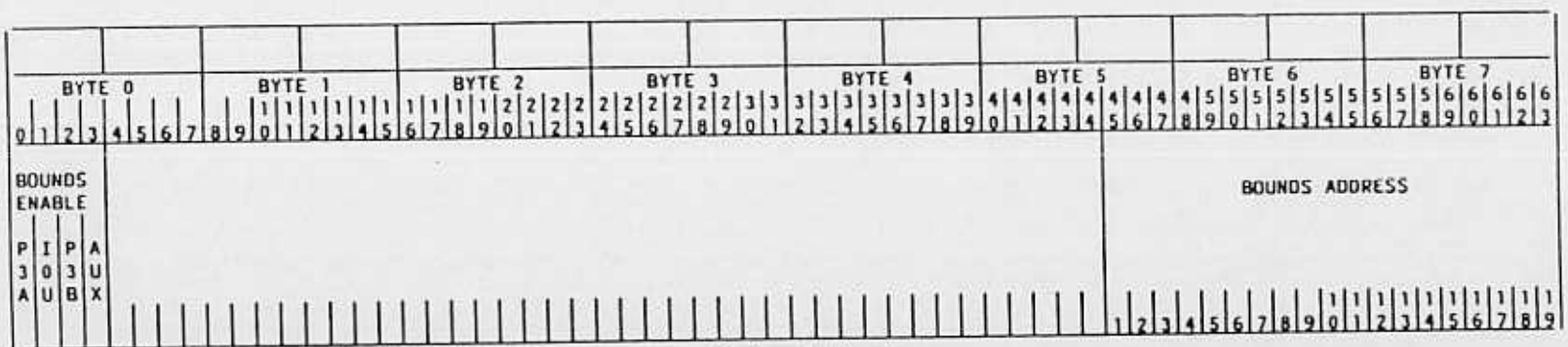
10 Element ID



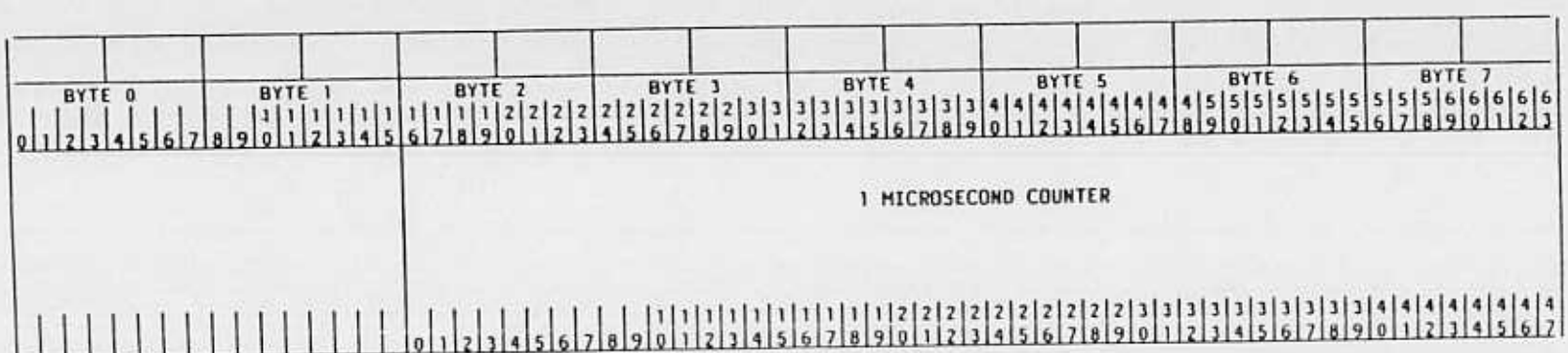
12 Options Installed



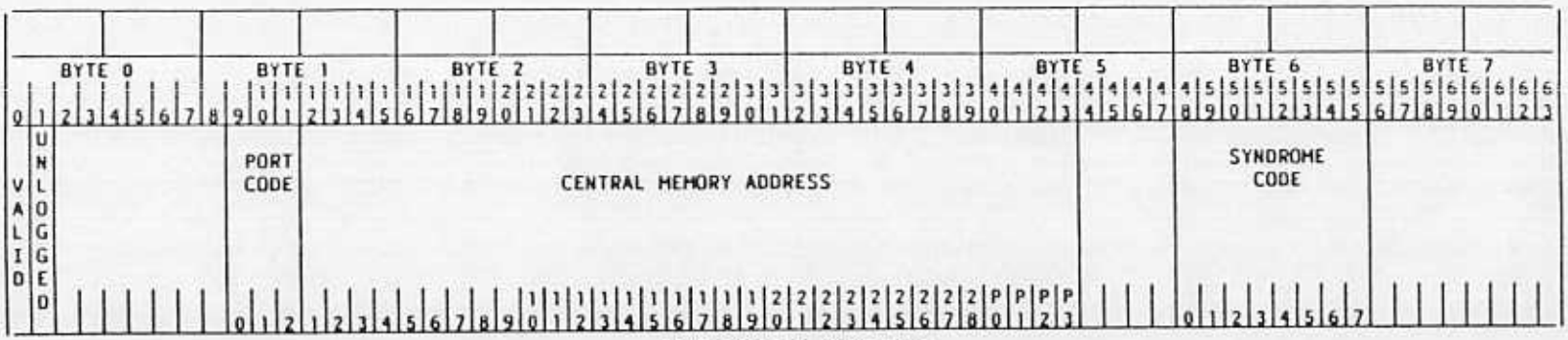
20 Environmental Control



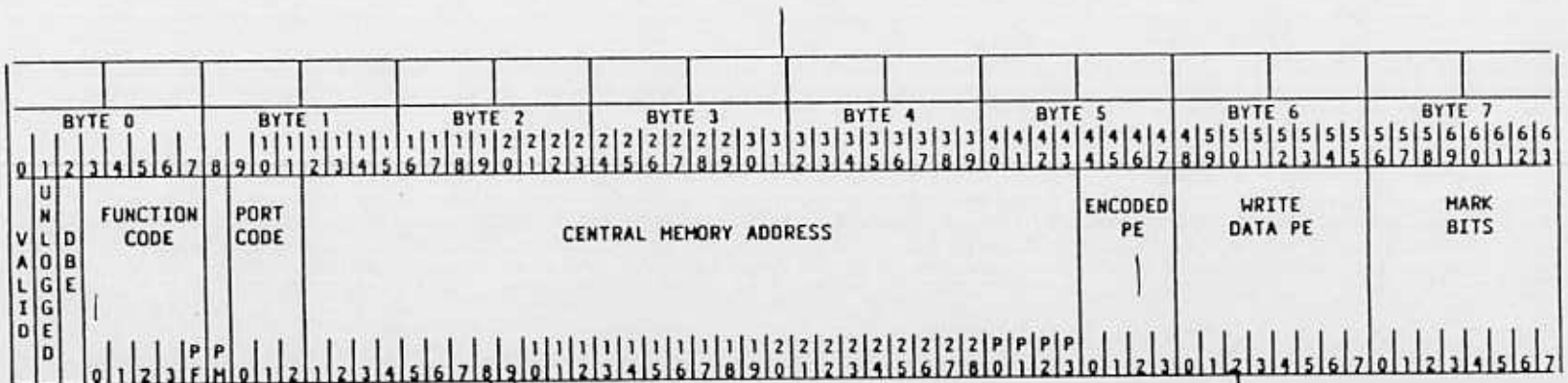
21 Bounds Checker



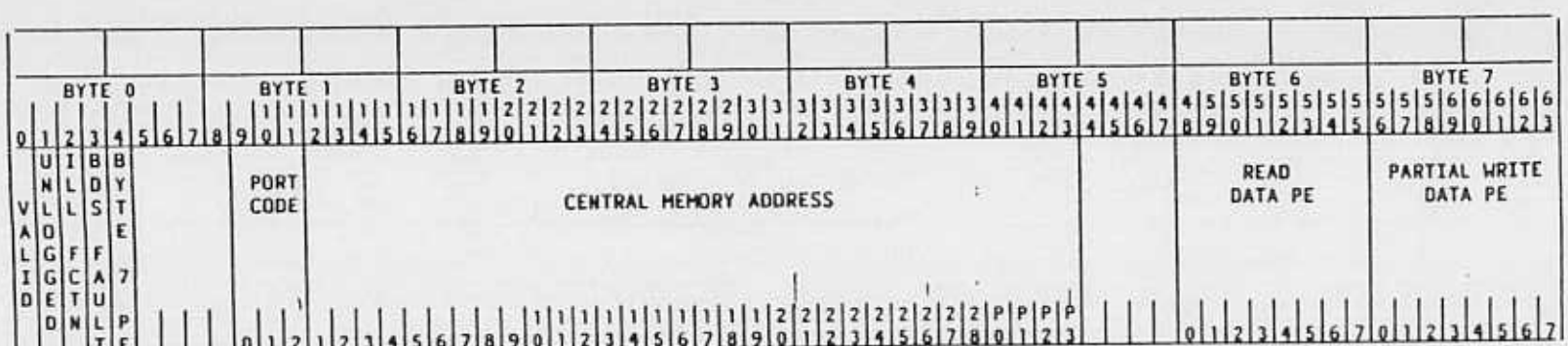
B0 Free Running Counter



A0 Corrected Error Log

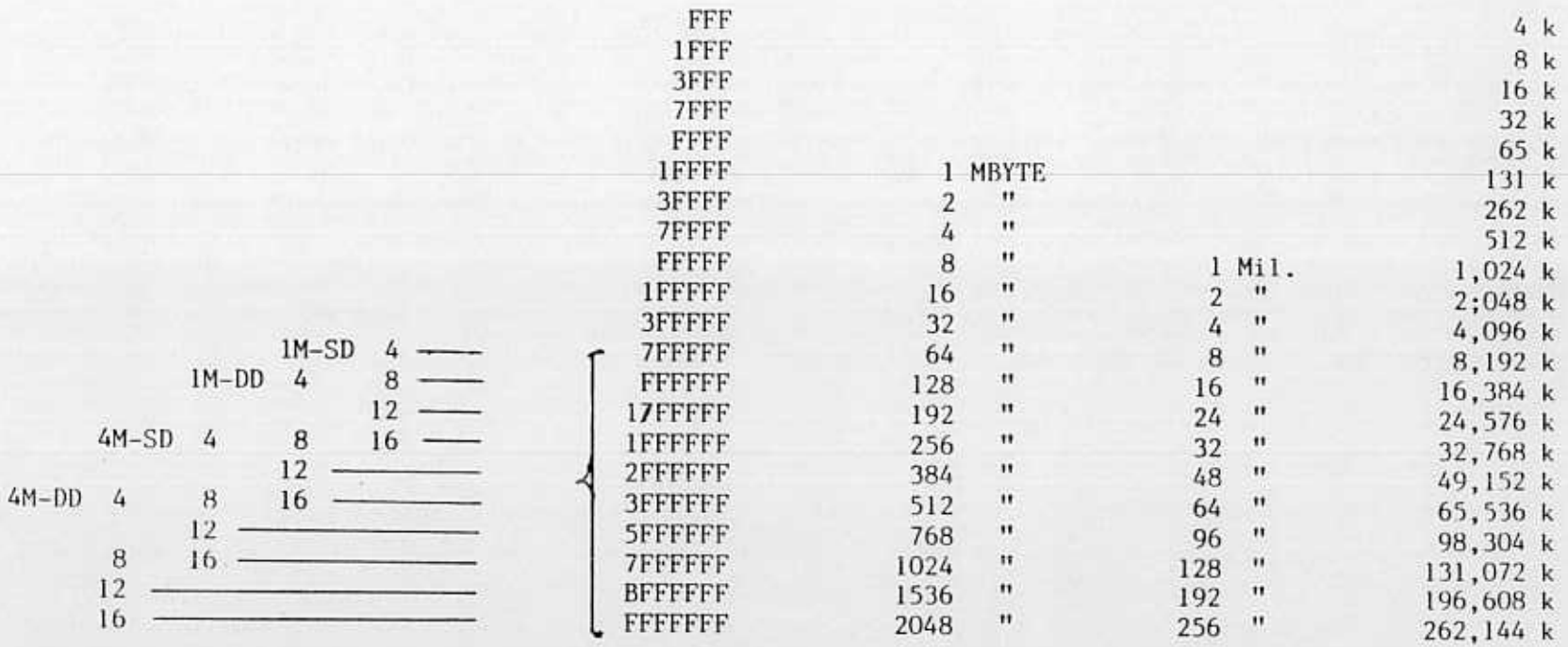


A4 Uncorrected Error Log #1



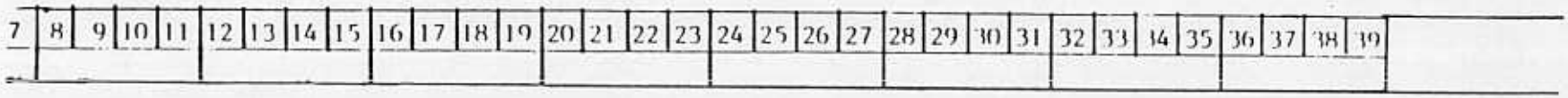
A8 Uncorrected Error Log #2

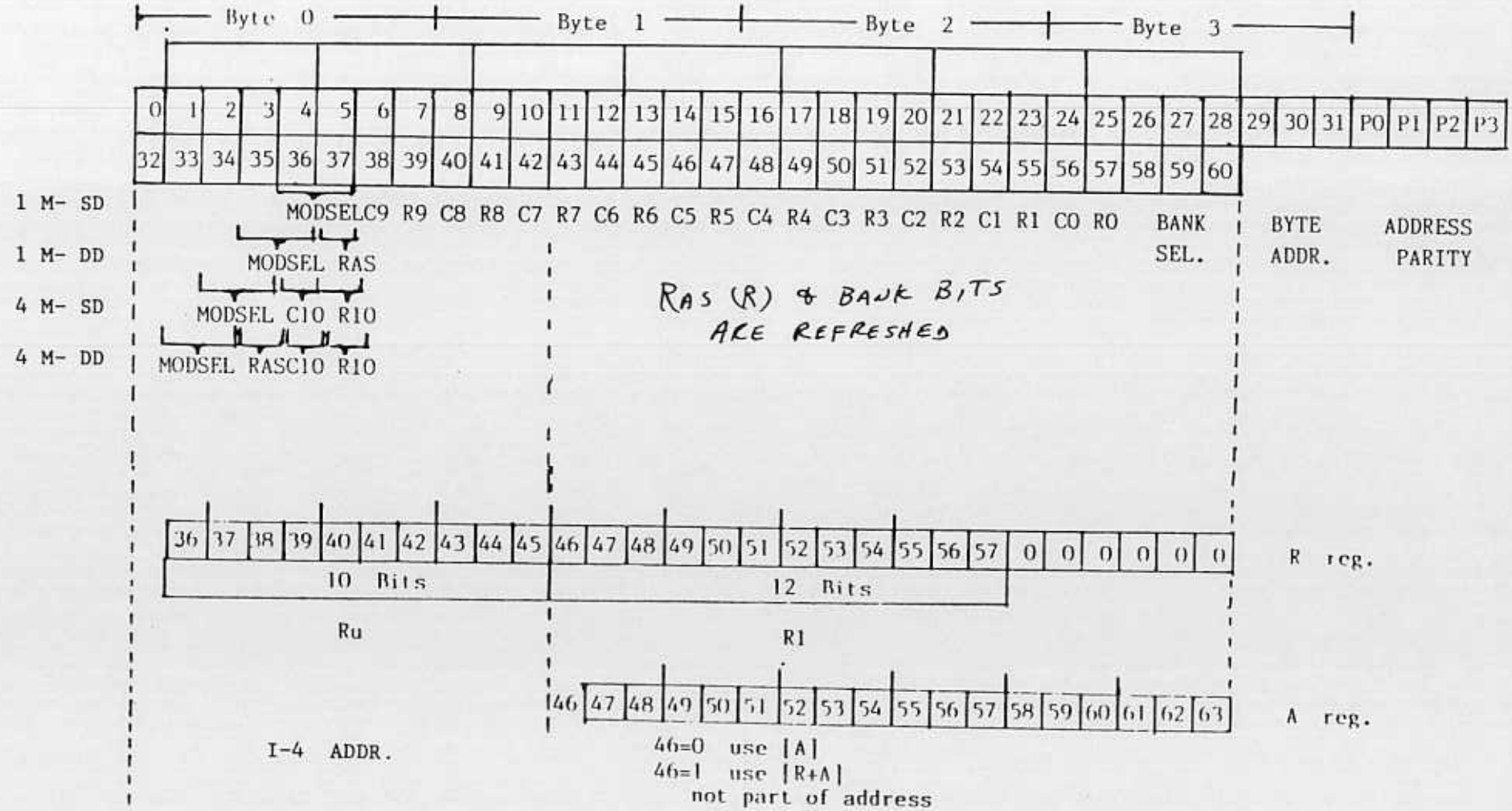
MAXIMUM ADDRESS



1M-SD - 1 Meg array, single density 4 - 16 modules
1M-DD - 1 Meg array,double density 4 - 16 modules
4M-SD - 4 Meg array,single density 4 - 16 modules
4M-DD - 4 Meg array,double density 4 - 16 modules

A0, A4, A8 REGISTERS





960 PIP ADDRESSING SCHEMES

A4 UCELI ENCODED PARITY ERRORS

PARITY ERROR	PIP3 CODE 0	1	2	3	PRIORITY
NO ERROR	0	0	0	0	
FUNCTION CODE	0	0	0	1	1
MARK LINES	0	0	1	0	2
CMC ADDRESS BYTE 0	0	1	0	0	3
CMC ADDRESS BYTE 1	0	1	0	1	4
CMC ADDRESS BYTE 2	0	1	1	0	5
CMC ADDRESS BYTE 3	0	1	1	1	6
CM ADDRESS BYTE 0 I	1	0	0	0	7
CM ADDRESS BYTE 1 I	1	0	0	1	8
CM ADDRESS BYTE 2 I	1	0	1	0	9
CM ADDRESS BYTE 3 I	1	0	1	1	10
CM ADDRESS BYTE 0 II	1	1	0	0	11
CM ADDRESS BYTE 1 II	1	1	0	1	12
CM ADDRESS BYTE 2 II	1	1	1	0	13
CM ADDRESS BYTE 3 II	1	1	1	1	14
TAG	0	0	1	1	15
	44	45	46	47	
	A4 BIT				

PORT CODES	
0	= CPU-0
1	= IOU
2	= CPU-1
3	= AUX
4	= REF

FUNCTION CODES

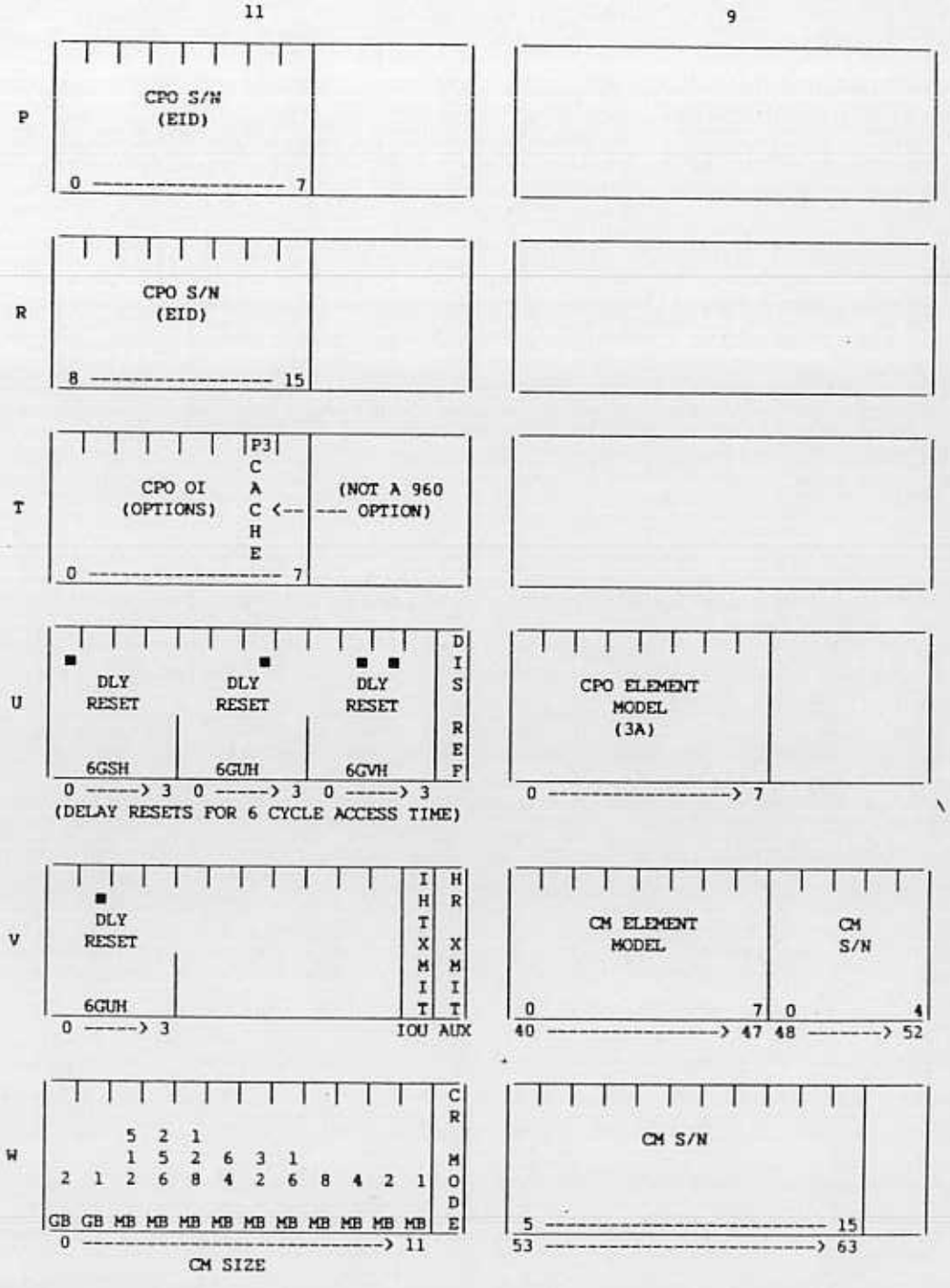
0000	Read
0001	*
0010	Write
0011	*
0100	Read and Set Lock (OR)
0101	Read and Clear Lock (AND)
0110	Exchange
0111	*
1000	*
1001	*
1010	Read Free Running Counter
1011	Refresh Counter Resync
1100	Interrupt
1101	*
1110	*
1111	*

* Function codes 1, 3, 7, 8, 9, D, E, and F are ILLEGAL and will result in a REJECT response from the port.

MEMORY RESPONSES

000	Write Response
001	Write Response Uncorrectable Error
010	Write
011	Interrupt Response
100	Read Response
101	Read Response Uncorrectable Error
110	Read Response Corrected Error
111	Reject

PIP3 JUMPER PLUGS



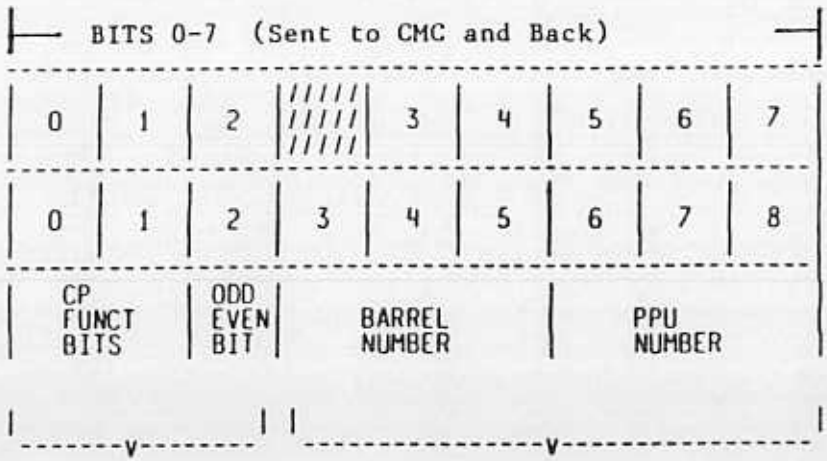
Code	Bit	Code	Bit	Code	Bit	Code	Bit	Code	Bit	Code	Bit	Code	Bit	Code	Bit
00	⑦	20	66 ②	40	65 ②	60	③	80	64 ②	A0	③	C0	0/1 ⑥	E0	32 ①
01	71 ②	21	③	41	③	61	④	81	③	A1	④	C1	④	E1	32 ⑤
02	70 ②	22	③	42	③	62	④	82	③	A2	④	C2	④	E2	36 ⑤
03	6/7 ⑥	23	④	43	④	63	③	83	④	A3	③	C3	③	E3	36 ①
04	69 ②	24	③	44	③	64	④	84	③	A4	④	C4	④	E4	34 ⑤
05	③	25	④	45	④	65	③	85	④	A5	③	C5	③	E5	34 ①
06	③	26	④	46	④	66	③	86	④	A6	③	C6	③	E6	38 ①
07	24 ①	27	28 ⑤	47	26 ⑤	67	30 ①	87	25 ⑤	A7	29 ①	C7	27 ①	E7	31/38 ⑤
08	68 ②	28	③	48	③	68	④	88	③	A8	④	C8	④	E8	33 ⑤
09	③	29	④	49	④	69	③	89	④	A9	③	C9	③	E9	33 ①
0A	③	2A	④	4A	④	6A	③	8A	④	AA	③	CA	③	EA	37 ①
0B	16 ①	2B	20 ⑤	4B	18 ⑤	6B	22 ①	8B	17 ⑤	AB	21 ①	CB	19 ①	EB	23/37 ⑤
0C	4/5 ⑥	2C	④	4C	④	6C	③	8C	④	AC	③	CC	③	EC	35 ①
0D	8 ①	2D	12 ⑤	4D	10 ⑤	6D	14 ①	8D	9 ⑤	AD	13 ①	CD	11 ①	ED	15/35 ⑤
0E	0 ①	2E	4 ⑤	4E	2 ⑤	6E	6 ①	8E	1 ⑤	AE	5 ①	CE	3 ①	EE	7/39 ⑤
0F	③	2F	④	4F	④	6F	③	8F	④	AF	③	CF	③	EF	39 ①
10	67 ②	30	2/3 ⑥	50	③	70	56 ①	90	③	B0	48 ①	D0	40 ①	F0	③
11	③	31	④	51	④	71	56 ⑤	91	④	B1	48 ⑤	D1	40 ⑤	F1	④
12	③	32	④	52	④	72	60 ⑤	92	④	B2	52 ⑤	D2	44 ⑤	F2	④
13	④	33	③	53	③	73	60 ①	93	③	B3	52 ①	D3	44 ①	F3	③
14	③	34	③	54	④	74	58 ⑤	94	④	B4	50 ⑤	D4	42 ⑤	F4	④
15	④	35	③	55	③	75	58 ①	95	③	B5	50 ①	D5	42 ①	F5	③
16	④	36	③	56	③	76	62 ①	96	③	B6	54 ①	D6	46 ①	F6	③
17	24 ⑤	37	28 ①	57	26 ①	77	30/62 ⑤	97	25 ①	B7	29/54 ⑤	D7	27/46 ⑤	F7	③
18	③	38	④	58	④	78	57 ⑤	98	④	B8	49 ⑤	D8	41 ⑤	F8	④
19	④	39	③	59	③	79	57 ①	99	③	B9	49 ①	D9	41 ①	F9	③
1A	④	3A	③	5A	③	7A	61 ①	9A	③	BA	53 ①	DA	45 ①	FA	③
1B	16 ⑤	3B	20 ①	5B	18 ①	7B	22/61 ⑤	9B	17 ①	BB	21/53 ④	DB	19/45 ⑤	FB	23 ①
1C	④	3C	③	5C	③	7C	59 ①	9C	③	BC	51 ①	DC	43 ①	FC	③
1D	8 ⑤	3D	12 ①	5D	10 ①	7D	14/59 ⑤	9D	9 ①	BD	13/51 ⑤	DD	11/43 ⑤	FD	15 ①
1E	0 ⑤	3E	4 ①	5E	2 ①	7E	6/63 ⑤	9E	1 ①	BE	5/55 ⑤	DE	3/47 ⑤	FE	7 ①
1F	④	3F	③	5F	③	7F	63 ①	9F	③	BF	55 ①	DF	47 ①	FF	③

Notes:

① Corrected single-bit error.
② Syndrome code bit failed (single code bit set).
③ Double error or multiple error (even number of code bits set).
④ Multiple error reported as a single error.
⑤ Double error or multiple error with indicated bit(s) inverted.
⑥ Double error or multiple error or forced double error due to a partial write parity error on one of the two bytes.
⑦ No error detected.

SECDED Syndrome Codes/Corrected Bits

ADU TAG BITS



Tag bits 0-2 and the function define the type of request. See CMI table 1. Tag bits 3-7 identifies the PP number or channel. See CMI table 2 and 3.

TAG BITS 0-2	FUNCTION
000 = ADU Even Request	X
001 = ADU Odd Request	X
010 = ADU Even Request	X
011 = DMA Channel Request	X
100 = ADU EXJ (2600)	Read
100 = ADU Cache Invalidate	Write
101 = ADU EXJ (2601)	Read
101 = ADU Cache Invalidate	Write
110 = ADU EXJ (2602)	Read
110 = ADU Cache Invalidate	Write
111 = DMA Request	Read
111 = DMA Cache Invalidate	Write

CMI - Table 1.

ADU TAG BITS
8 <--> 9 CONVERSION

TAG BITS		3-8	3-7
BARR #	PP #	9 BIT	8 BIT
0	0	0	0
0	1	1	1
0	2	2	2
0	3	3	3
0	4	4	4
1	0	10	10
1	1	11	11
1	2	12	12
1	3	13	13
1	4	14	14
2	0	20	20
2	1	21	21
2	2	22	22
2	3	23	23
2	4	24	24
3	0	30	30
3	1	31	31
3	2	32	32
3	3	33	33
3	4	34	34
4	0	40	7
4	1	41	6
4	2	42	27
4	3	43	26
4	4	44	5
5	0	50	17
5	1	51	16
5	2	52	37
5	3	53	36
5	4	54	15

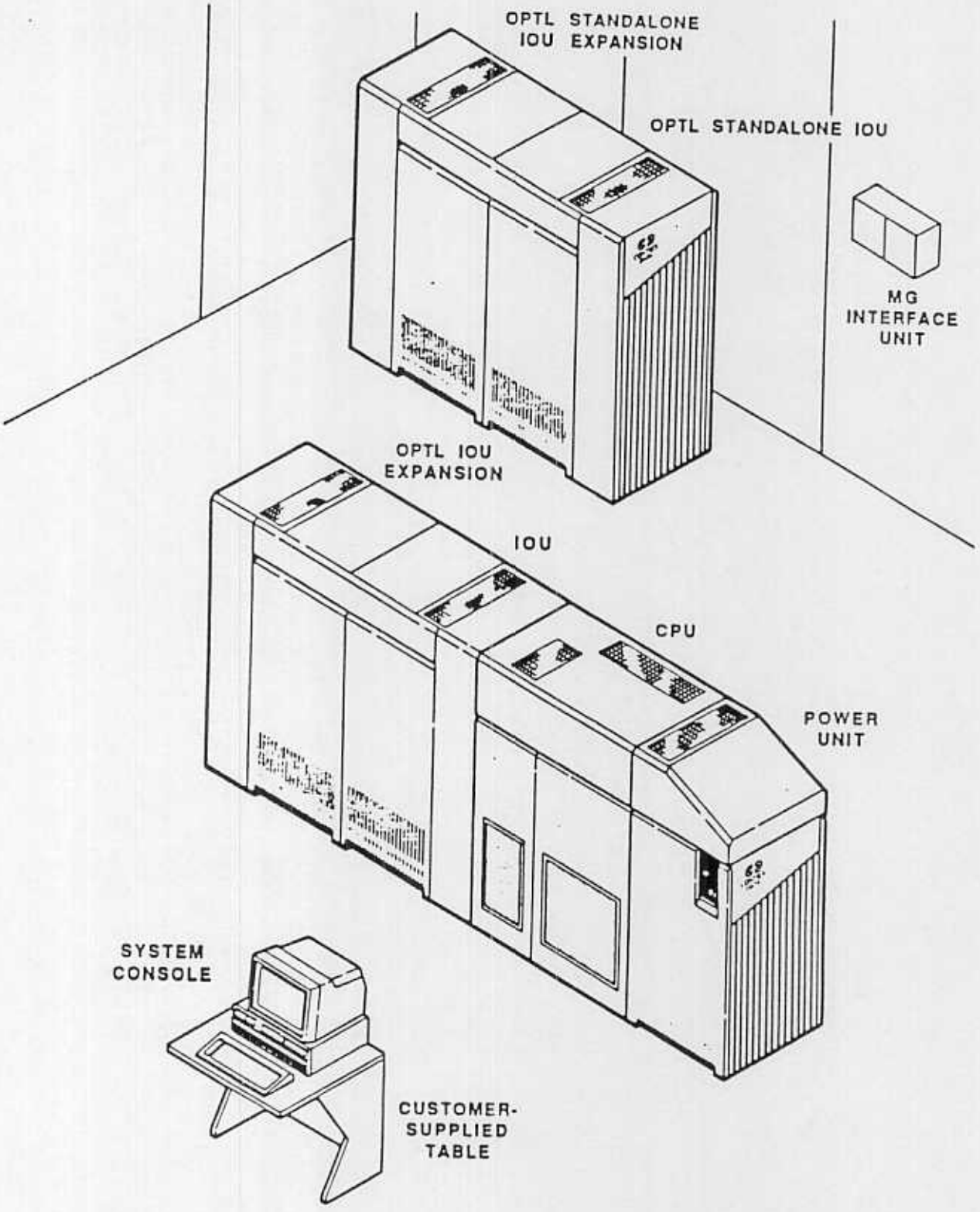
TABLE - 2 CMI

BUS TAG BITS

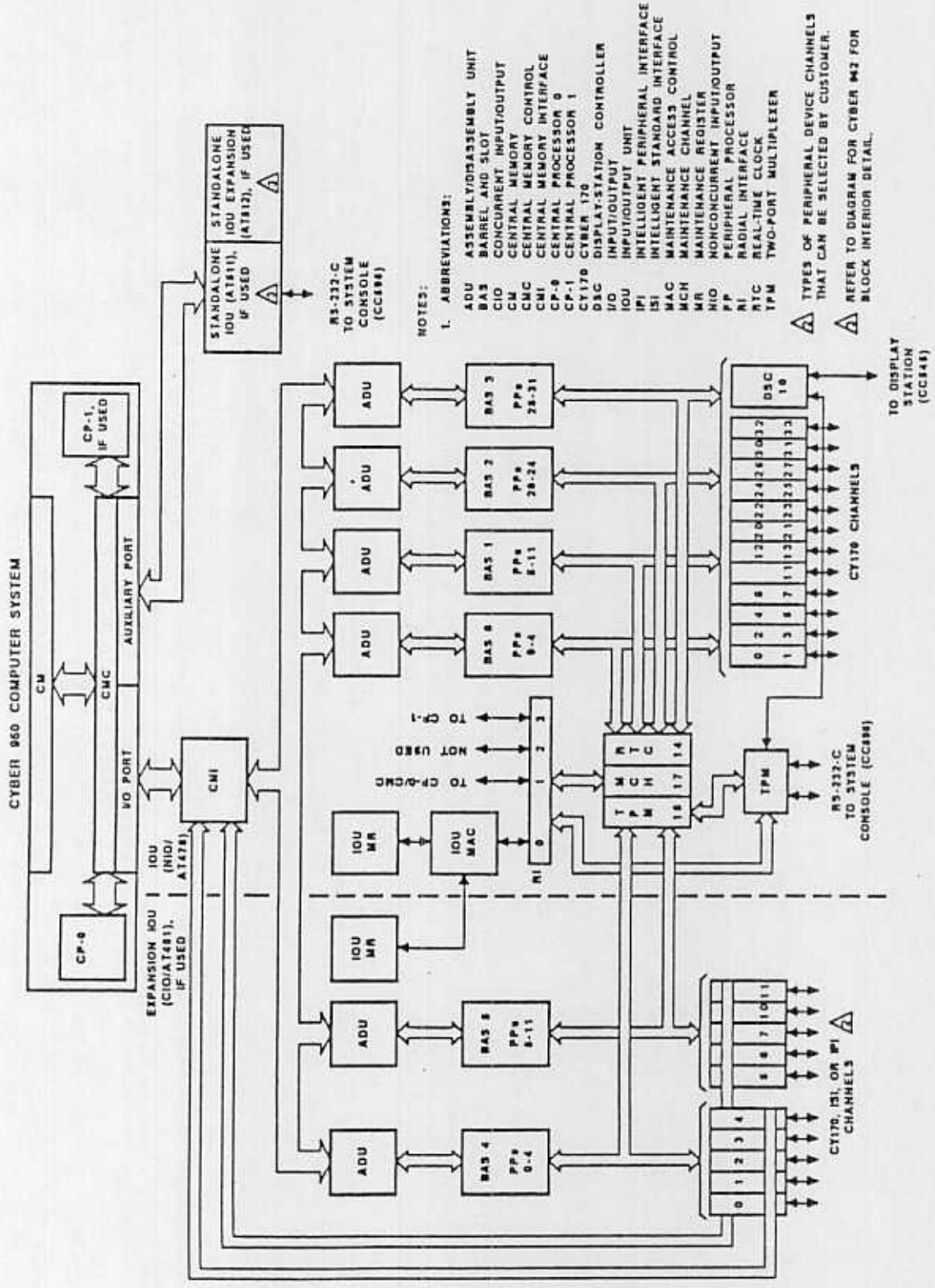
TAG BITS 3-6 *		
BUS	CH. #	TAG
0	0	0
0	1	1
0	2	2
0	3	3
0	4	4
1	0	5
1	1	6
1	2	7
1	3	10
1	4	11

* TAG BIT 7 EQUALS THE LEAST SIGNIFICANT CH ADDRESS BIT.

TABLE - 3 CMI



INPUT OUTPUT UNIT

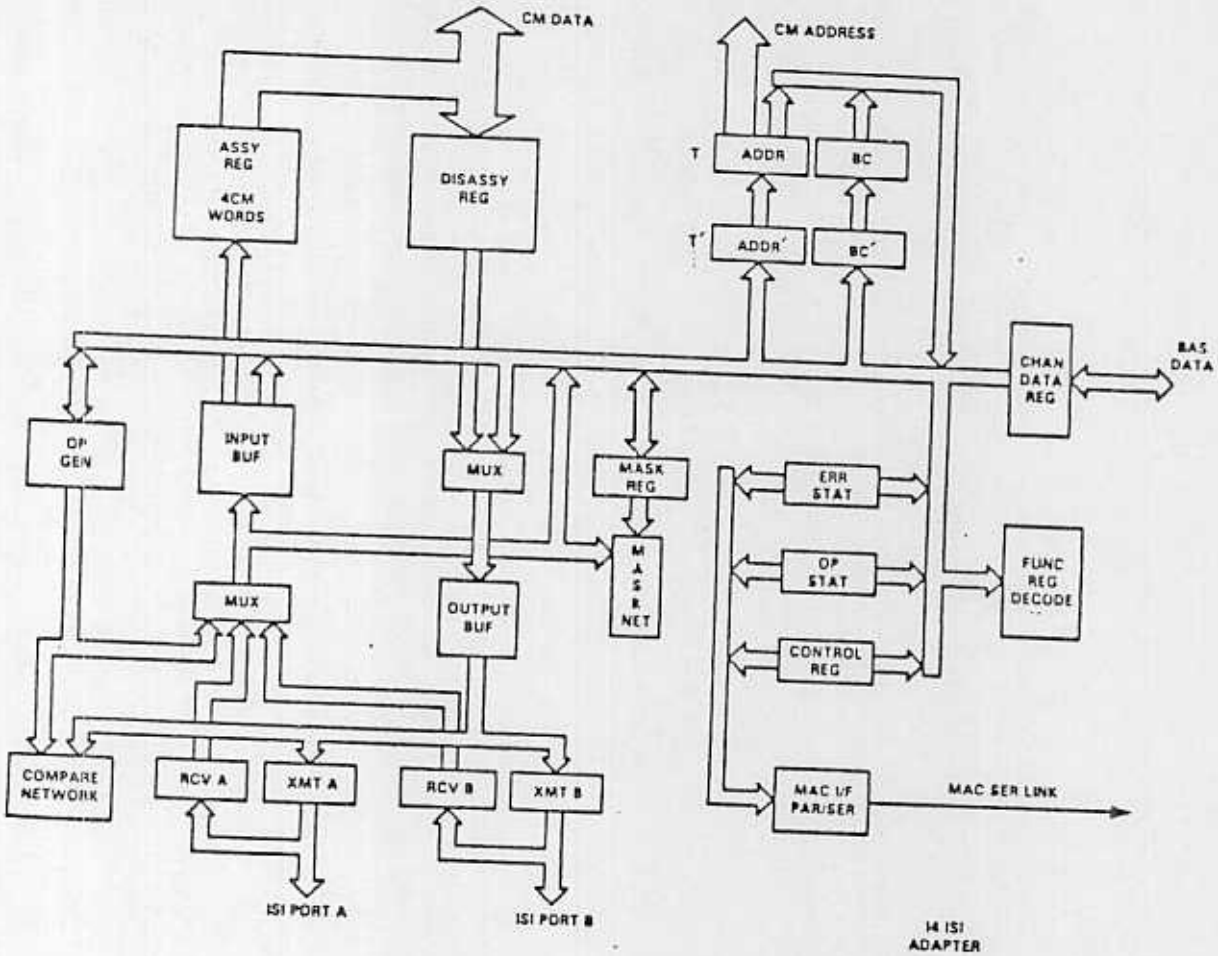


IOU Relationships in a CYBER 960 Computer System

JX Barrel $Slot interface

JZ External interface

JY Assy / Disassembly



I4 DMA ISI Channel

CHANNEL CONFIGURATION TYPES (NIO-CIO) FOR IOU MODEL I4A

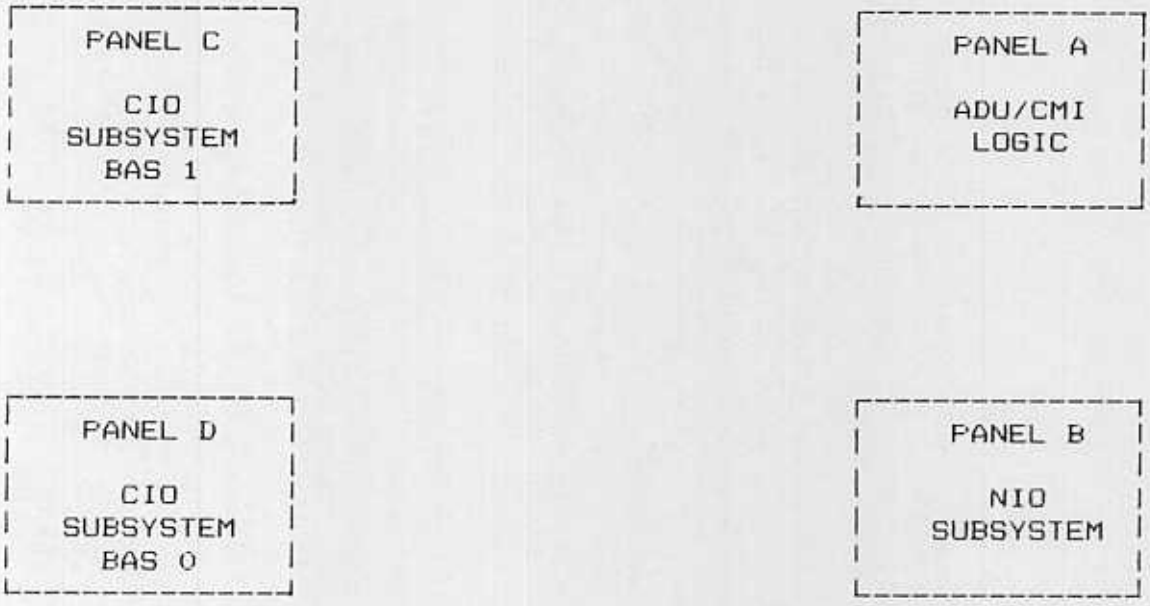
NIO	170 CH	JL pack	2 channels/pack
CIO	ISI CH	JX/JZ/JY packs	1 channel/pack-group
	IPI CH	LX/LZ/JY packs	1 channel/pack-group
	170 DMA CH	KX/KZ/JY packs	1 channel/pack-group

DISKS	CAPACITE	TRANS RATE	CH TYPE	
885	600 MB	1 MB/s	NIO 170	
895	700 MB	3 MB/s	NIO 170	2xPP's on ping-pong
895	700 MB	3 MB/s	CIO 170	CH 170 DMA 1xPP
887	700 MB	12 MB/s	CIO ISI	NOS 10Mb/s sect:16Kb VE 8Mb/s sect: 4Kb 4 heads in //
XMD3	1.2 GB	3 MB/s	CIO IPI	VE ONLY sect: 4Kb

IPI : INTELLIGENT PERIPHERAL INTERFACE

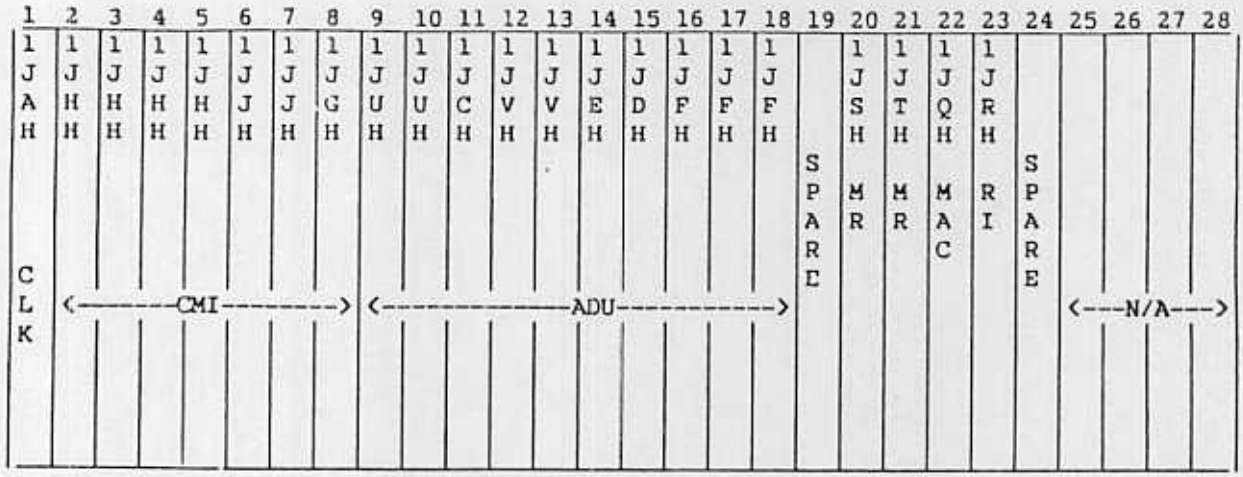
ISI : INTELLIGENT STANDARD INTERFACE

I4 AC PANEL MAP

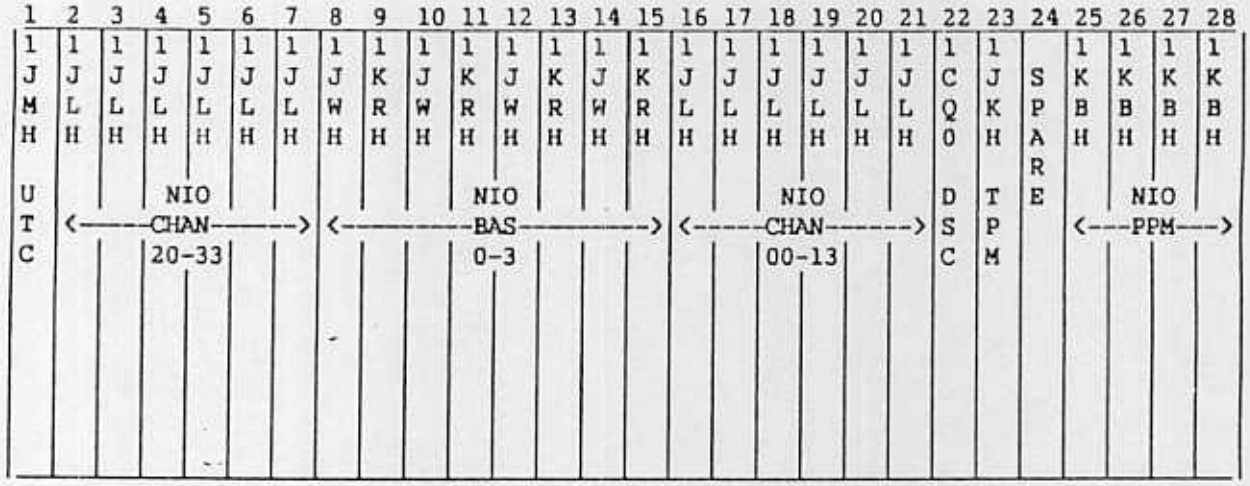


I4 AC PANEL MAP

PANEL A

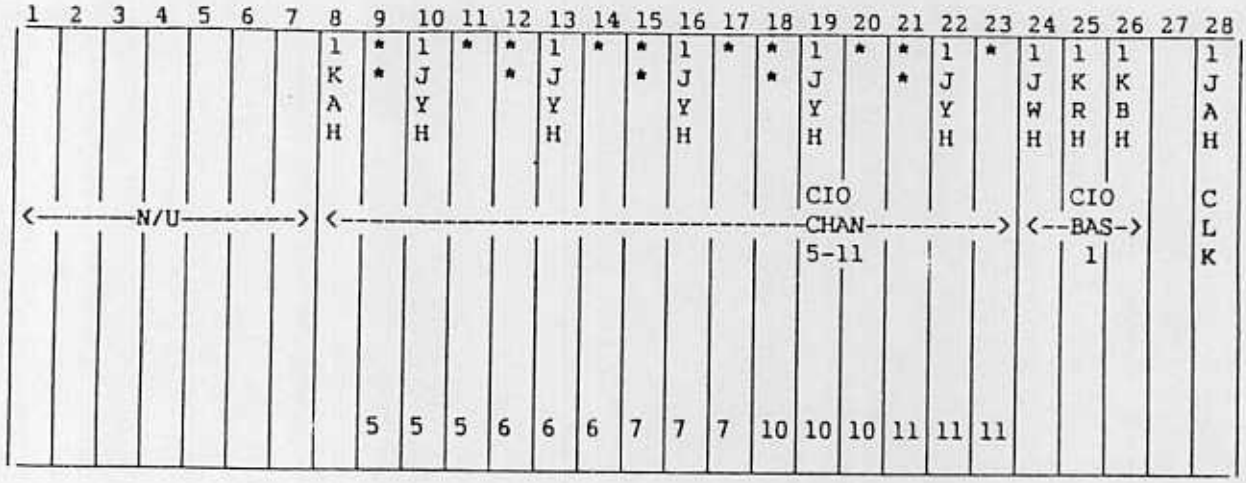


PANEL B

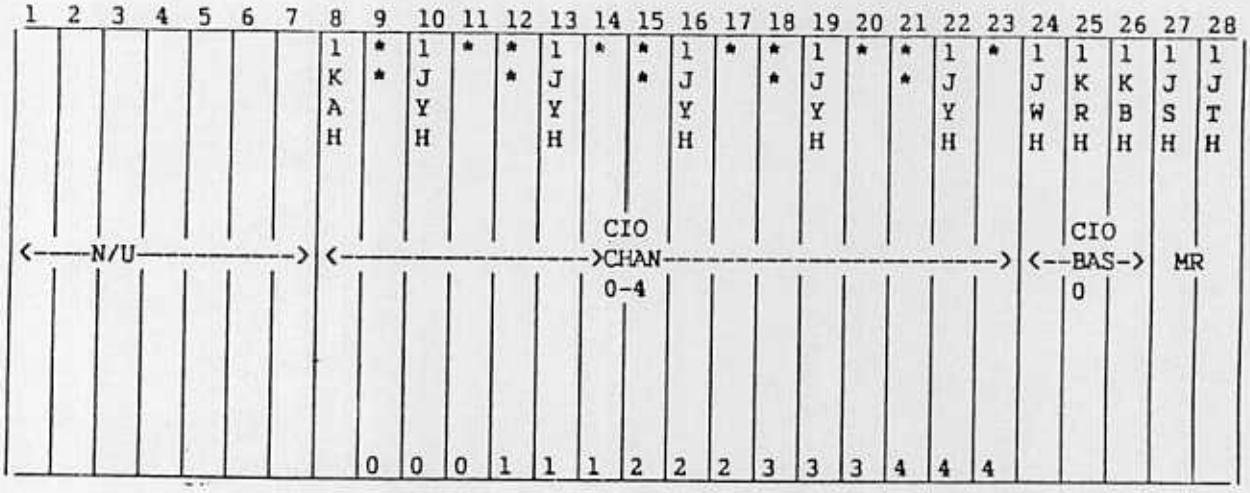


I4 AC PANEL MAP

PANEL C



PANEL D

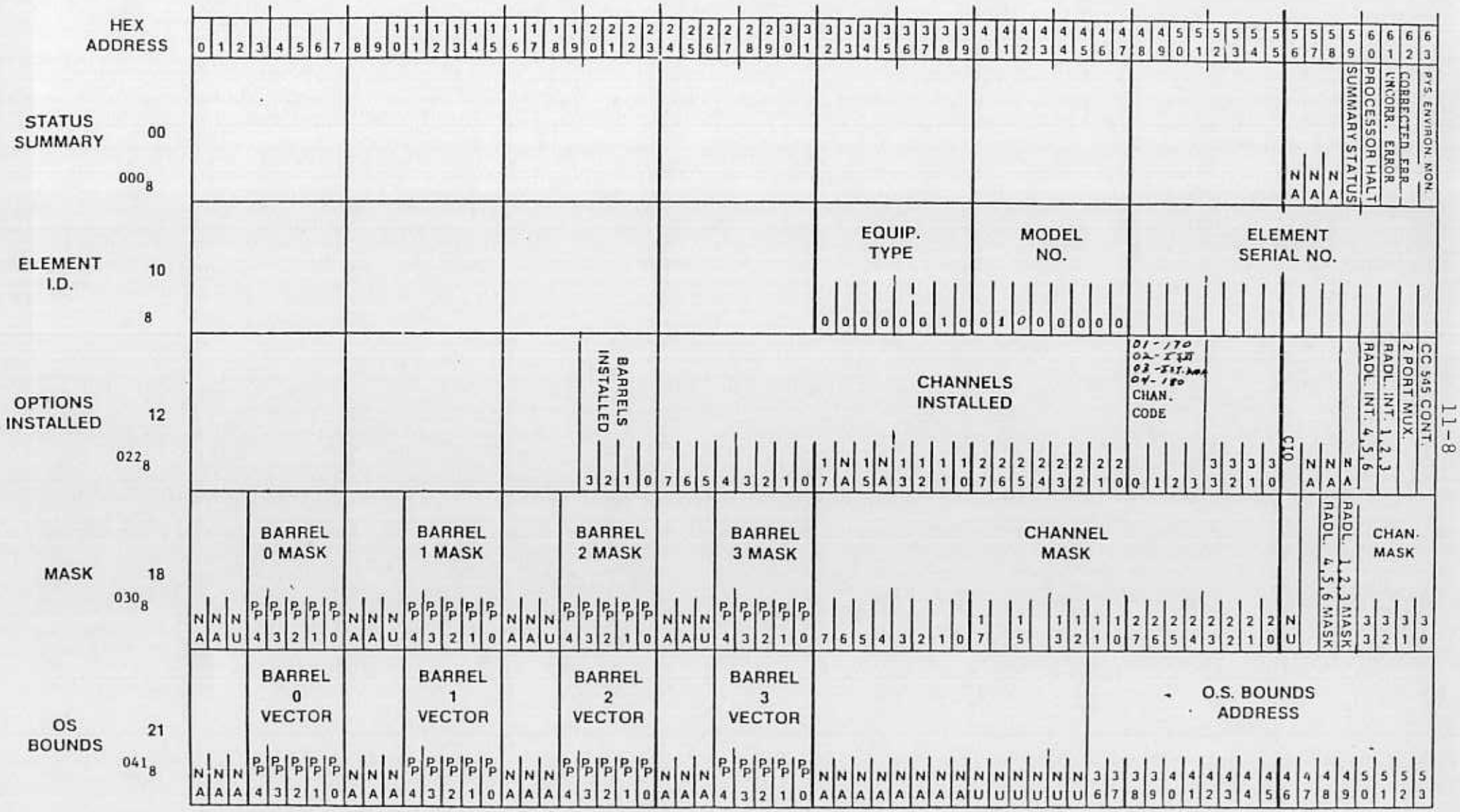


* ISI 1JXH
170 1KXH
IPI 1LXH

** ISI 1JZH
170 1KZH
IPI 1LZH

IOU MAINTENANCE REGISTERS PART 1

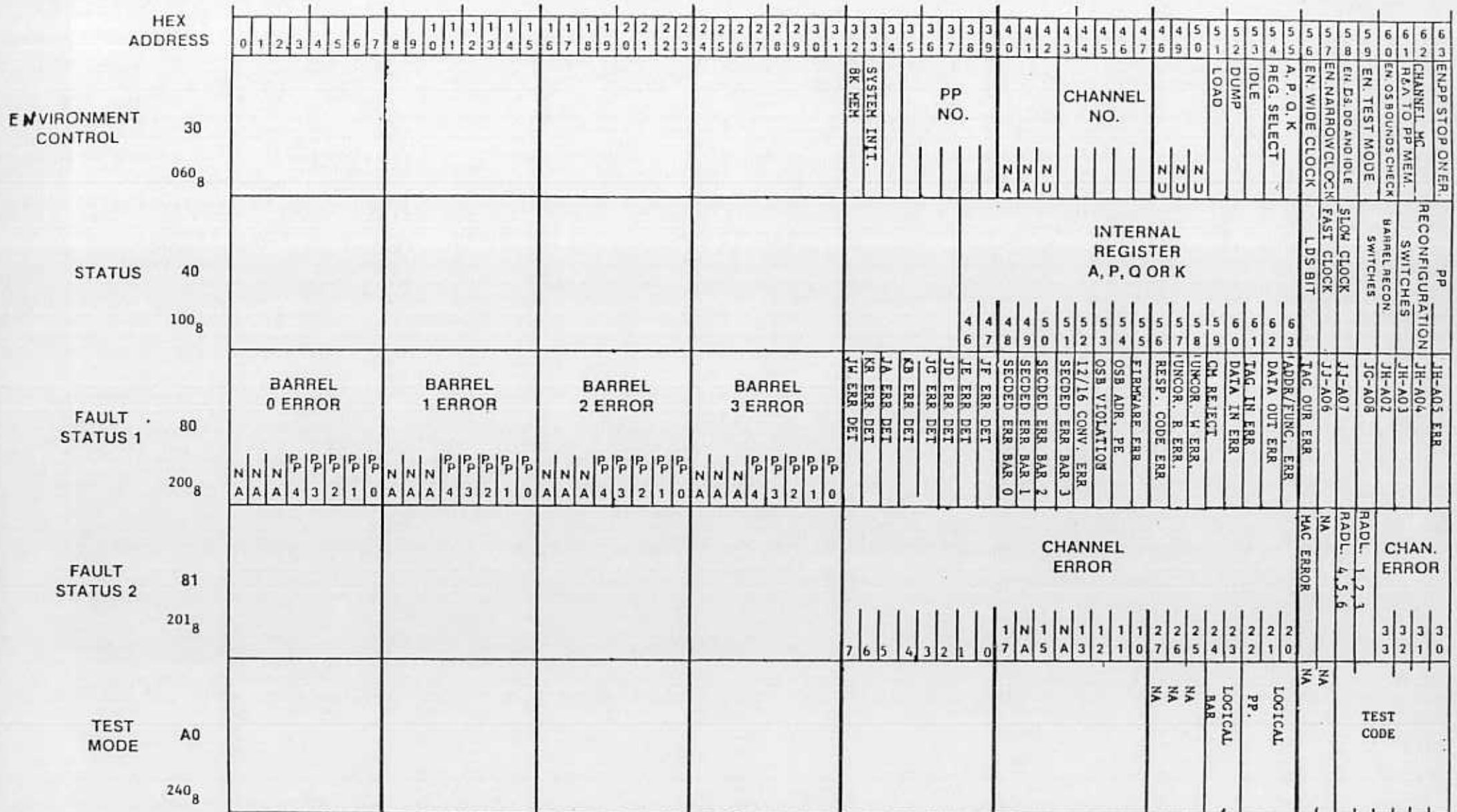
I4 AC NIO



NOTE: NU-IMPLIES BIT AVAILABLE BUT NOT USED, CAN BE WRITTEN INTO AND READ
NA-IMPLIES BIT NOT AVAILABLE, CAN NOT BE WRITTEN INTO AND IF READ WILL BE ZERO
ALL UNMARKED BITS ARE NA

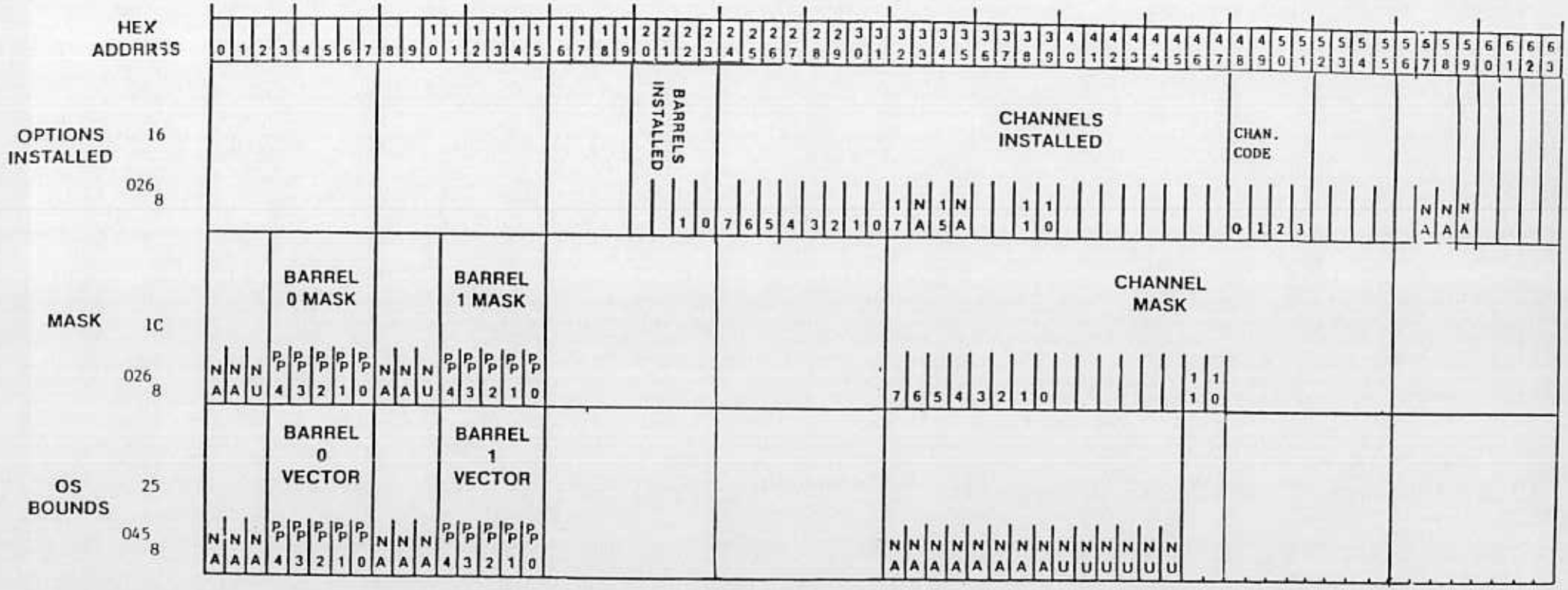
IOU MAINTENANCE REGISTERS PART 2

I4 AC NIO

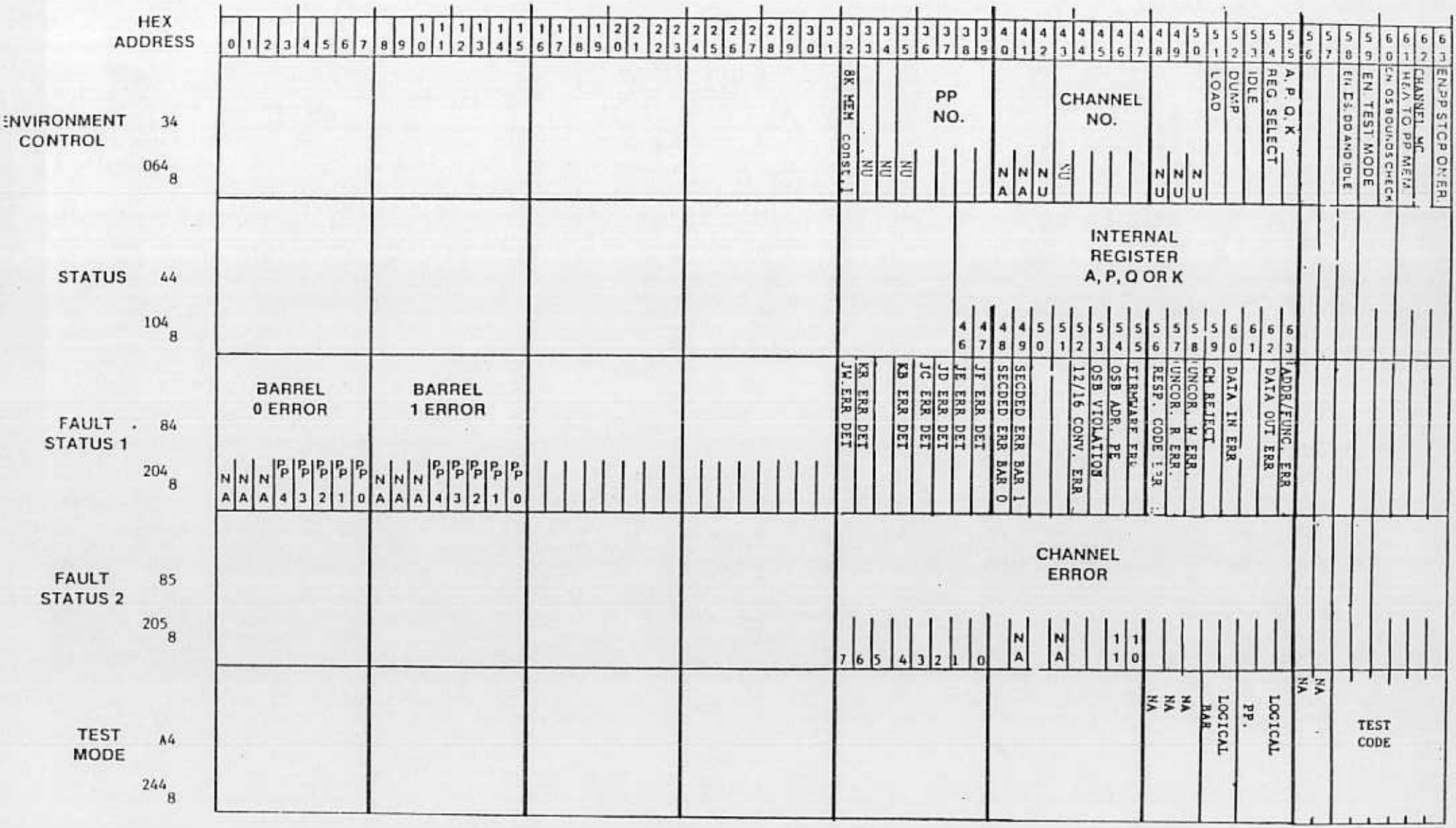


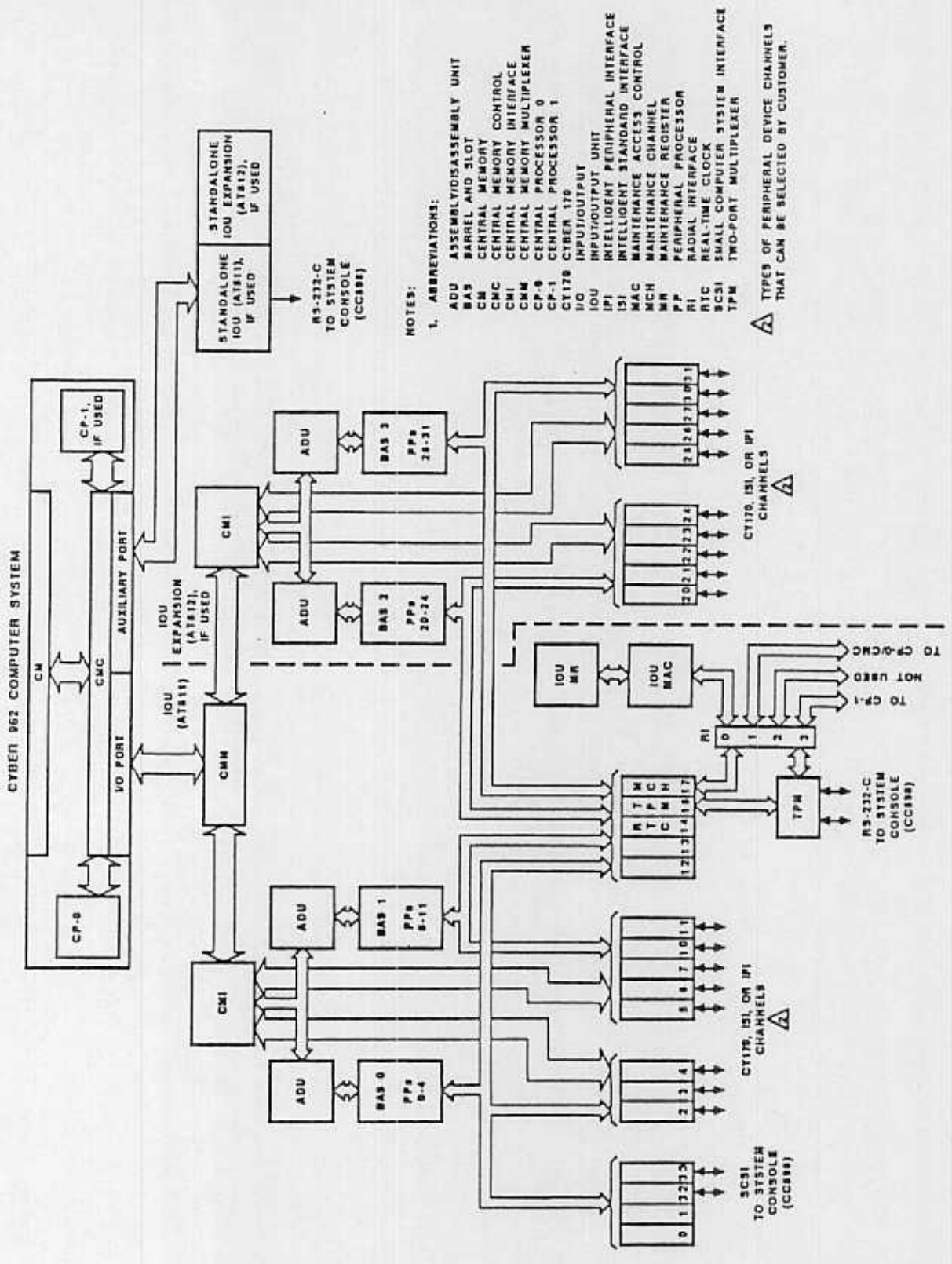
NOTE: NU, NA } SEE NOTE PART 1

IOU MAINTENANCE REGISTERS PART 1



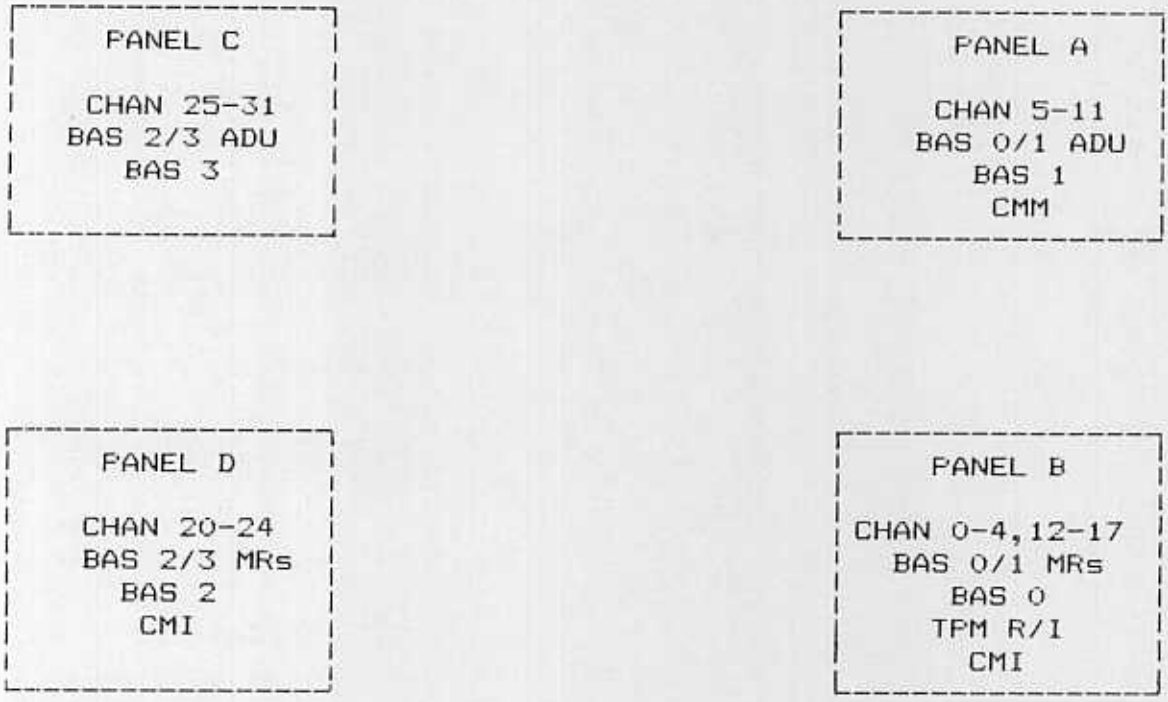
IOU MAINTENANCE REGISTERS PART 2



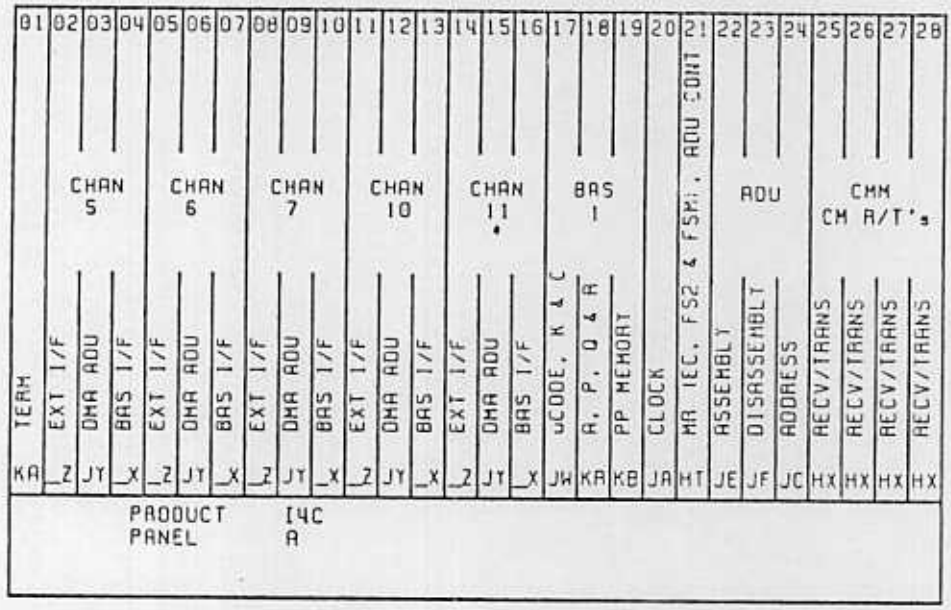


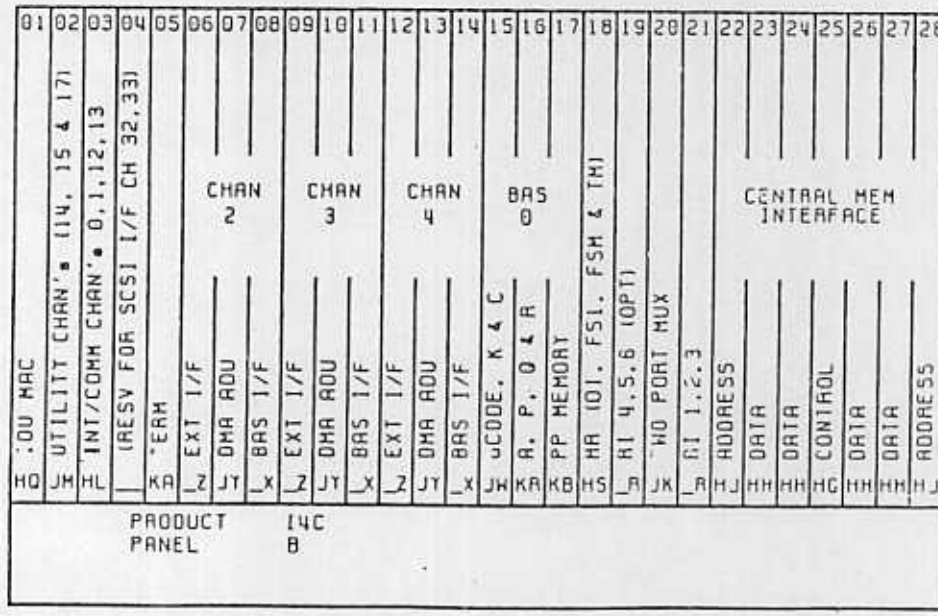
IOU Relationships in a CYBER 962 Computer System

I4 C PANEL MAP

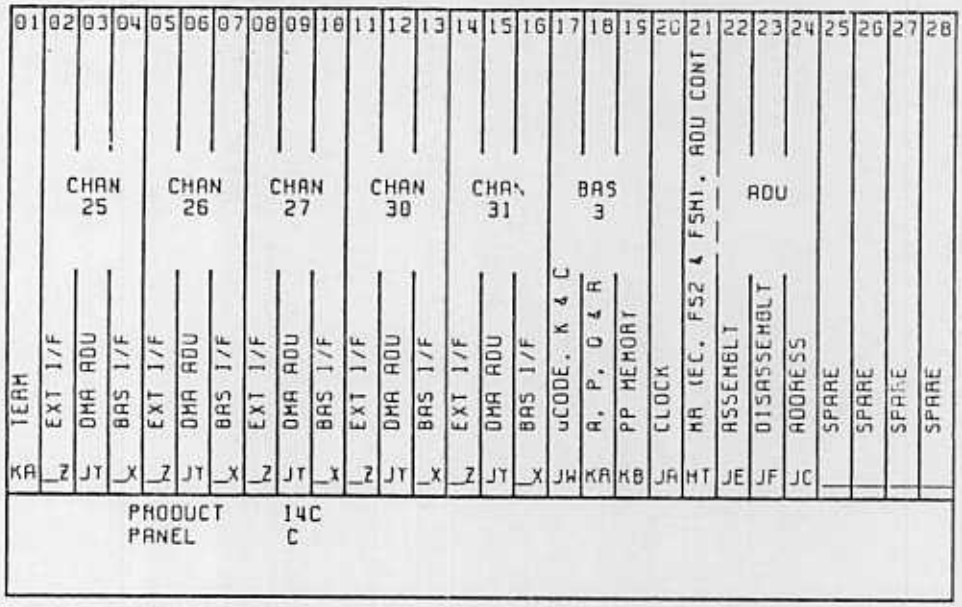


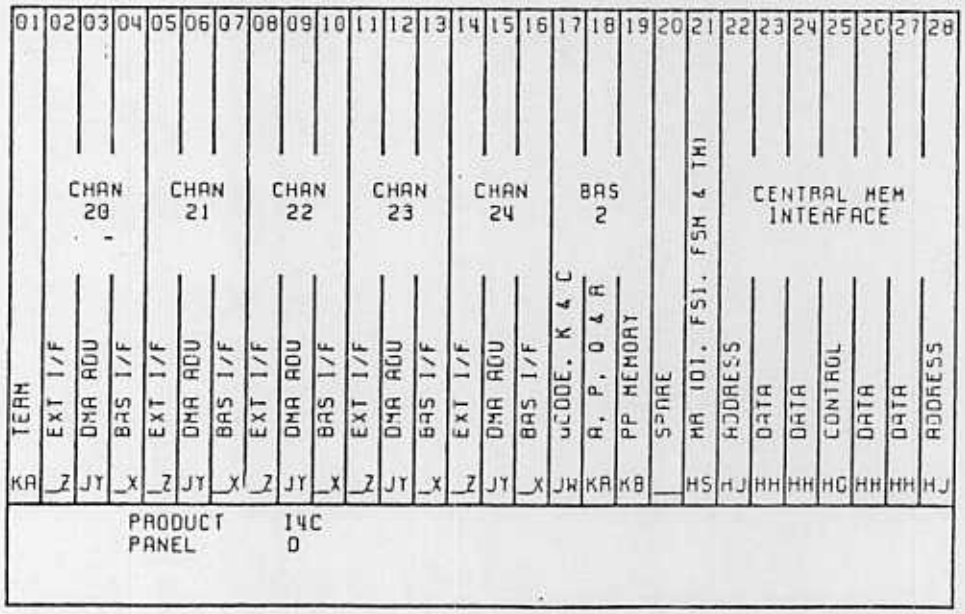
I4 C PANEL MAP





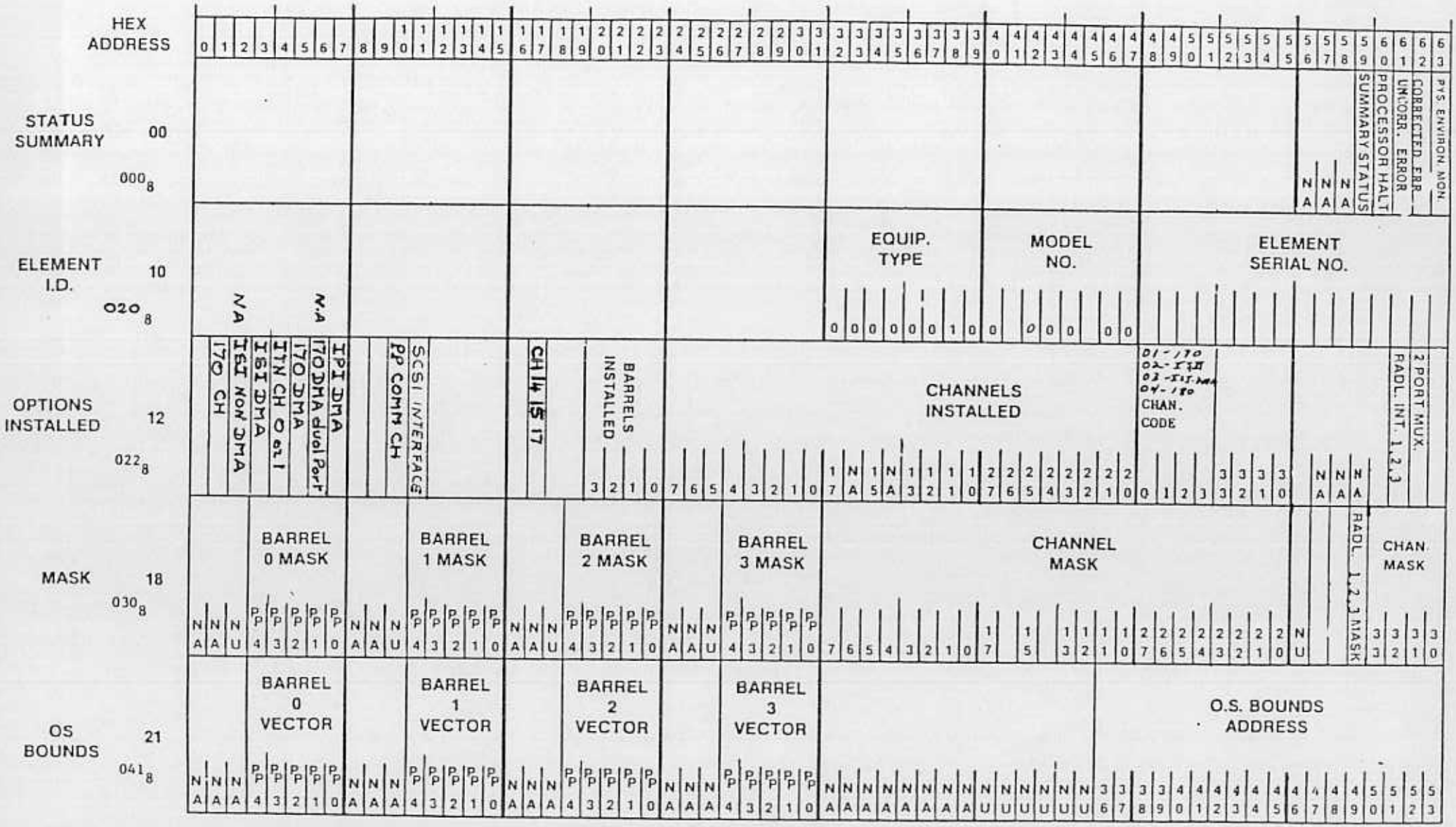
I4 C PANEL MAP





IOU MAINTENANCE REGISTERS PART 1

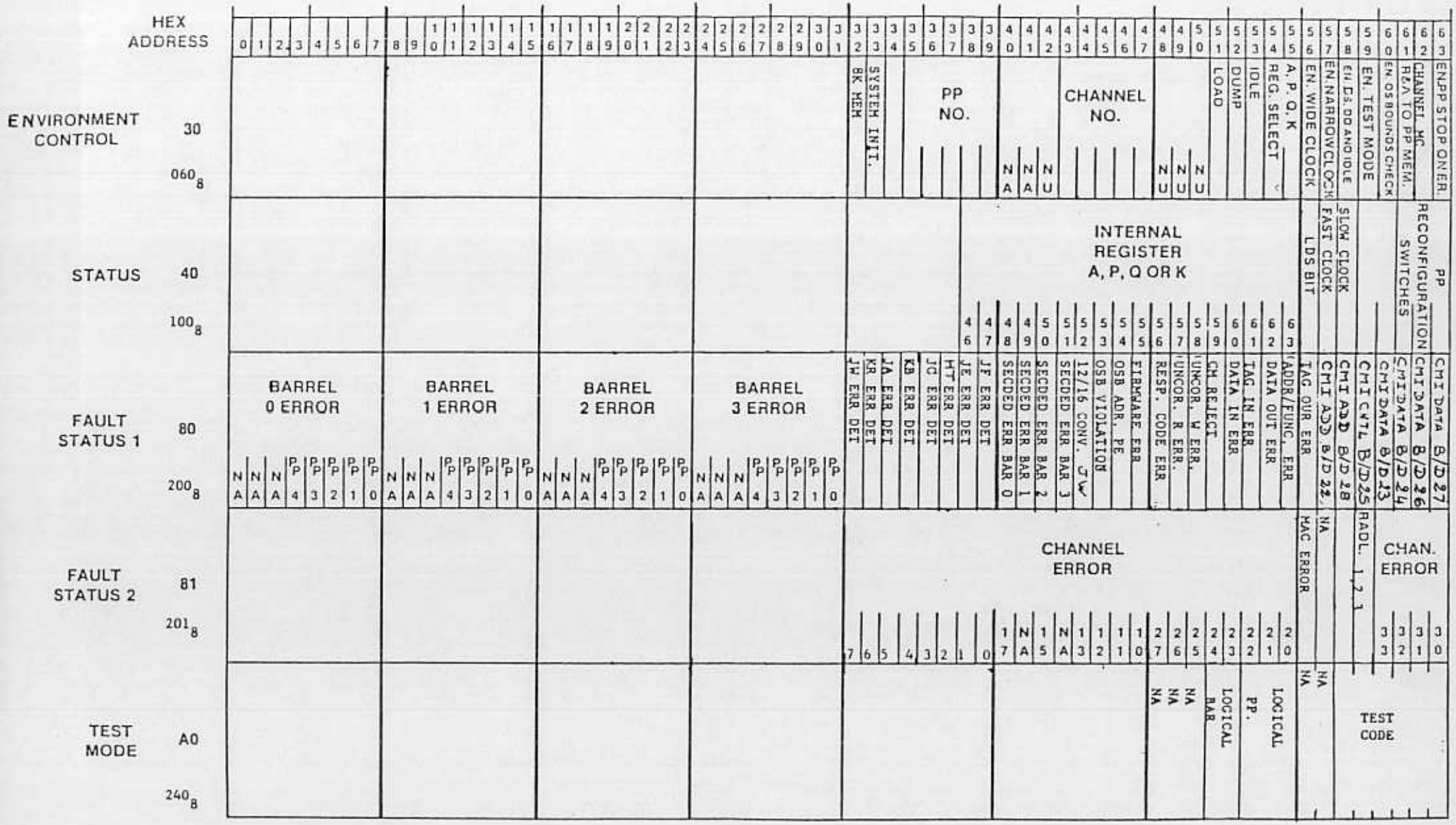
I4 C



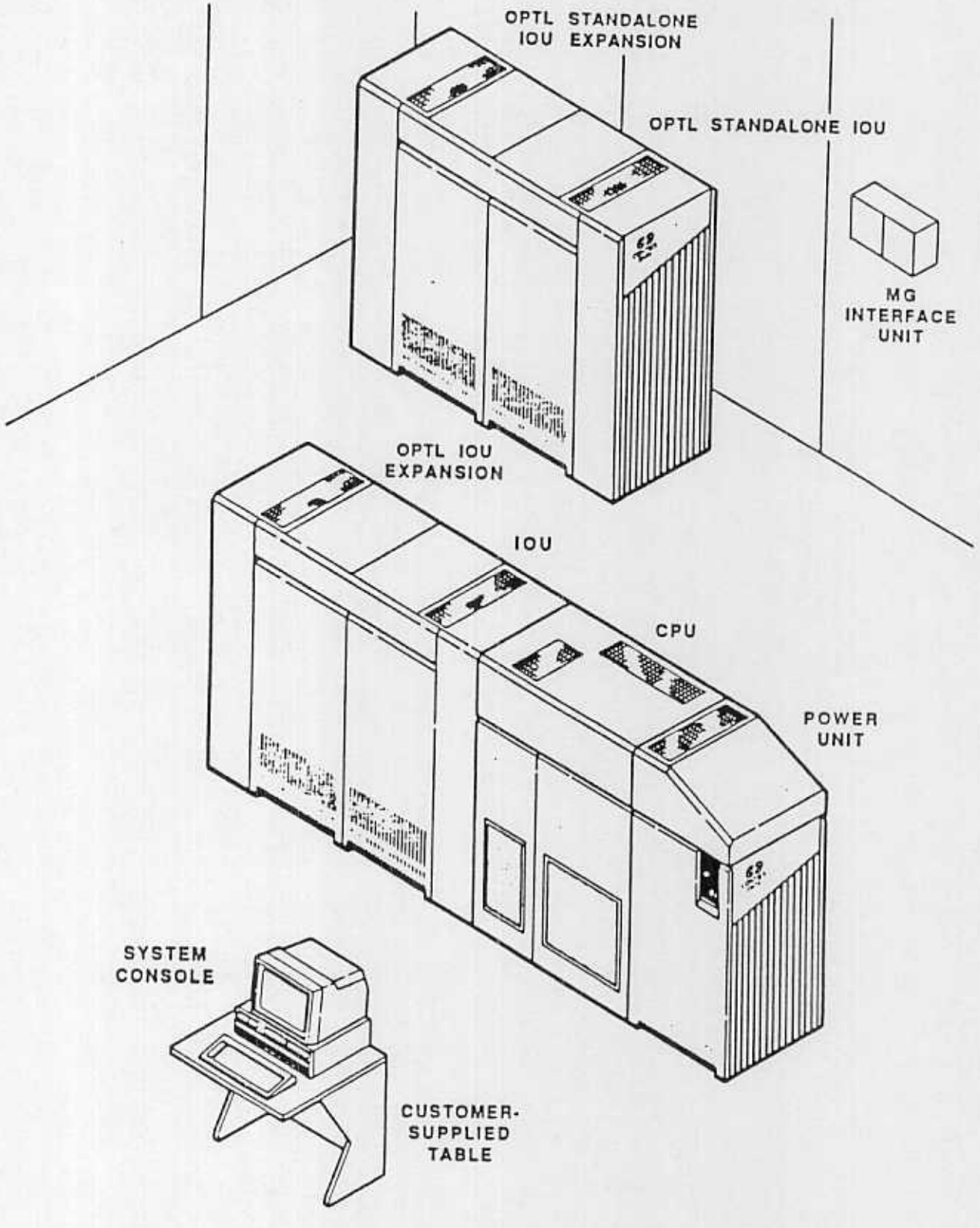
NOTE: NU-IMPLIES BIT AVAILABLE BUT NOT USED, CAN BE WRITTEN INTO AND READ
NA-IMPLIES BIT NOT AVAILABLE, CAN NOT BE WRITTEN INTO AND IF READ WILL BE ZERO
ALL UNMARKED BITS ARE NA

IOU MAINTENANCE REGISTERS PART 2

I4C



NOTE: NU, NA } SEE NOTE PART 1


OPTL STANDALONE
IOU EXPANSION
OPTL STANDALONE IOU
MG
INTERFACE
UNIT
OPTL IOU
EXPANSION
IOU
CPU
POWER
UNIT
SYSTEM
CONSOLE
CUSTOMER-
SUPPLIED
TABLE

CONSOLE

HARDWARE DESCRIPTION

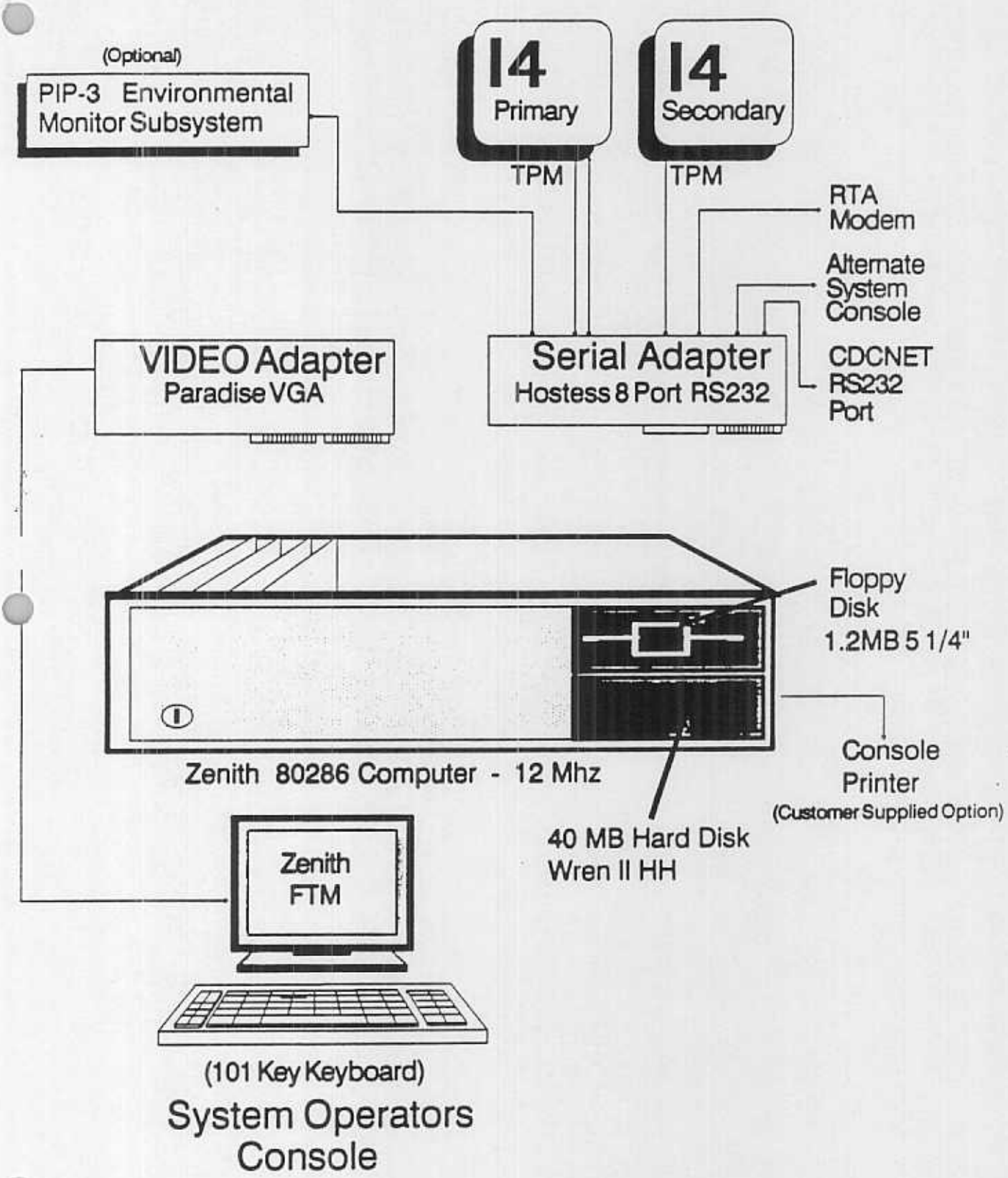
19003-2 Operator Console

This console consists of a 12 MHZ Zenith ZBO 2503-EK AT class PC with 1 MB of memory, a 91 MB WREN hard disk, one 360K/1.2M floppy disk drive, an 8 serial port adaptor board, three SCSI adaptor boards and a Zenith color monitor. This console will function as the CIP Device. That is, it will contain the CIP package on its own hard disk. The customer's disk and tape will not be required to initialize the system. A customer tape will be required to initially load the CIP Device, however. This console will be used only on the NOS/VE standalone 962 and 992 systems.

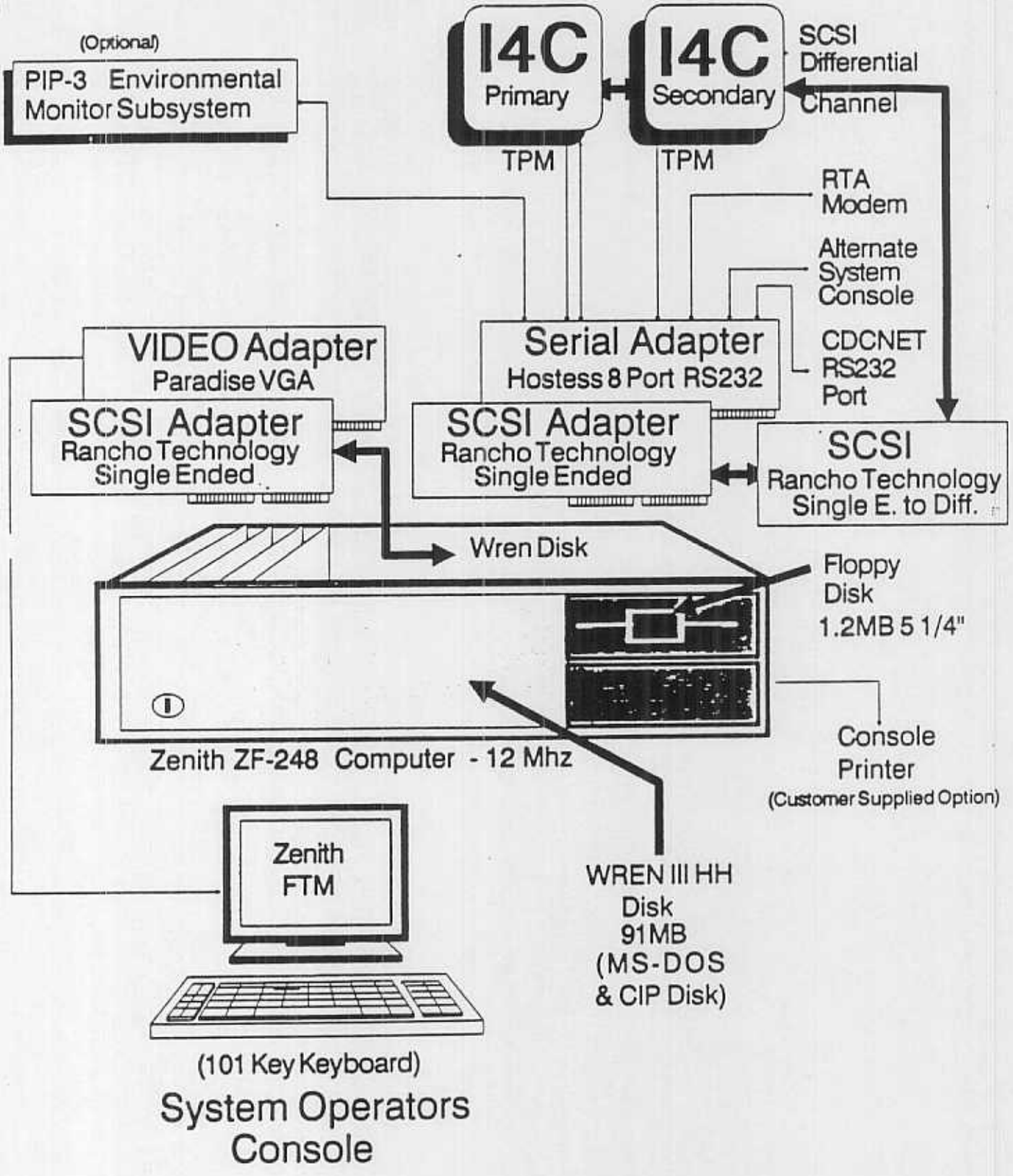
19003-3 Operator Console

This console consists of a 12 MHZ Zenith ZBO 2503-EK AT class PC with 1 MB of memory, a 40 MB hard disk, one 360K/1.2M floppy disk drive, an 8 serial port adaptor board and a Zenith color monitor. This console supports 132 character displays and will take the place of both the 721 and CC545 consoles presently being used for NOS and NOS/VE systems. This console will be used on Dual I4 860 and 990 systems, 960 systems and 994 systems. This console is a replacement for the 19003-1 console which was initially shipped on Dual I4 systems.

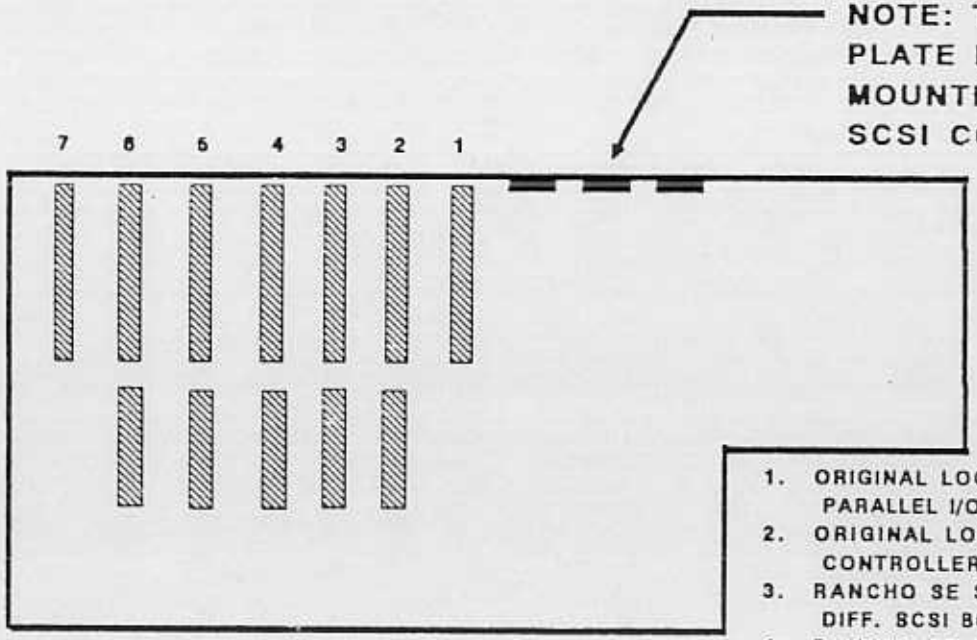
19003-3 (CC598-B) CONSOLE



19003-2 (CC598-A) CONSOLE



CONTROL DATA CORPORATION		CODE IDENT	SHEET	CA	DOCUMENT NO.	REV

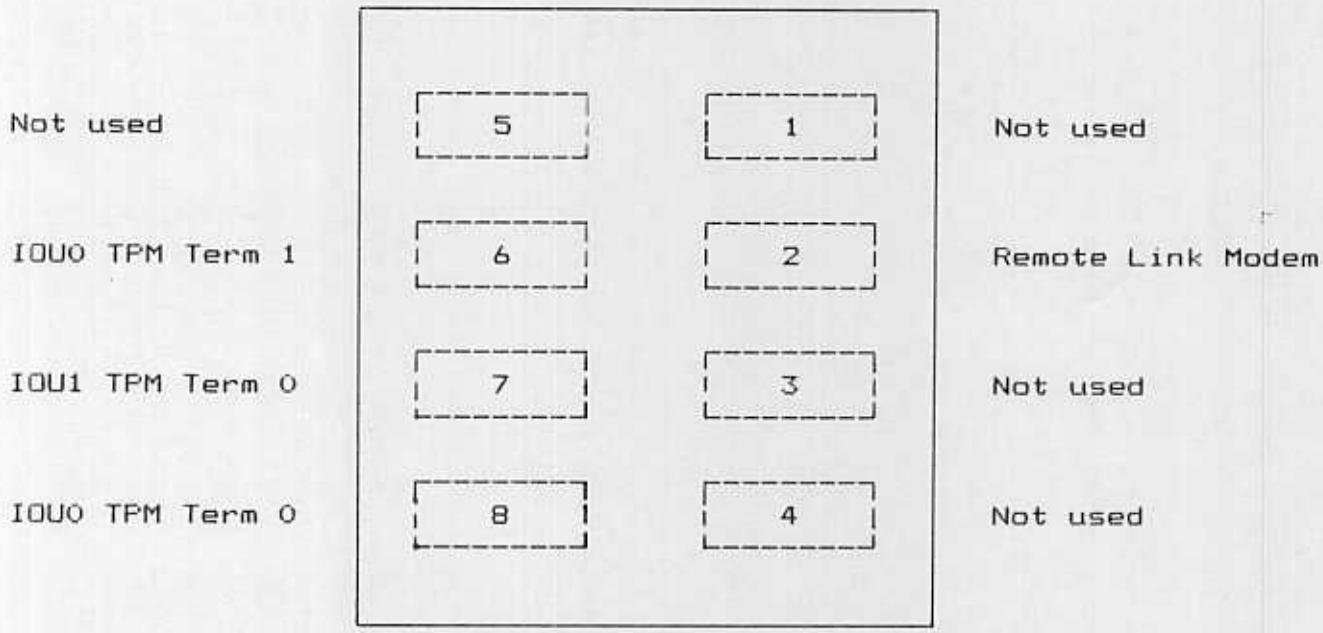


NOTE: THIS METAL COVER PLATE IS REMOVED FOR MOUNTING OF EXTERNAL SCSI CONNECTOR

1. ORIGINAL LOCATION OF THE SERIAL PARALLEL I/O BOARD.
2. ORIGINAL LOCATION OF THE FDD CONTROLLER BOARD.
3. RANCHO SE SCSI BOARD TO THE DIFF. SCSI BOARD.
4. RANCHO SE SCSI BOARD TO THE CDC WREN III HARD DISK DRIVE.
5. HOSTESS 550 CIRCUIT BOARD ASSY.
6. AVAILABLE
7. PARADISE VIDEO BOARD.

PC CARD PLACEMENT

MULTIPORT NETWORK ADAPTER CABLE CONNECTIONS



ZENITH PC TESTING

Power-on Tests

A Power-On/Boot test is automatically run on the PC whenever power is turned on or the PC is rebooted (Ctrl/Alt/Del). This consists of a memory test and basic CPU/IO tests.

ROM Based Tests

The next level of testing is called the ROM based tests. These tests are more extensive and are located in ROM memory. The tests can be individually selected to test the disk, memory, expanded memory or keyboard.

To run the ROM based diagnostics on the Zenith PC, press the Ctrl, Alt and Ins keys at the same time.

The PC will re-boot itself and a display similar to the following display will appear:

```
MFM-200 Monitor, Version 1.6A
Memory Size: 640K
Enter "?" for help
->
```

At this time type the word TEST.

```
MFM-200 Monitor, Version 1.6A Memory Size: 640K
Enter "?" for help
->TEST
```

At this time the following display will appear:

```
CHOOSE ONE OF THE FOLLOWING:

1. DISK READ TEST
2. KEYBOARD TEST
3. BASE MEMORY TEST
4. EXPANSION MEMORY TEST
5. POWER-UP TEST
6. EXIT

ENTER YOUR CHOICE:
```

At this time type in the number of the selection you want.

Disk Based Tests

The third level of testing is done using a set of diagnostics that are contained on a diskette. These are Zenith proprietary diagnostics that provide a very high level of detection and isolation of failures within the Zenith PC boards. These diagnostics do not test the Hostess Board or the SCSI boards that are added to the PC.

To run the diskette based diagnostics, insert the diskette in the floppy drive and press the Ctrl, Alt and Ins keys at the same time.

The PC will re-boot itself and a display similar to the following will appear:

```
MFM-200 Monitor, Version 1.6A Memory Size: 640K
Enter "?" for help
->
```

At this time type the characters bf.

```
MFM-200 Monitor, Version 1.6A Memory Size: 640K
Enter "?" for help
->bf
```

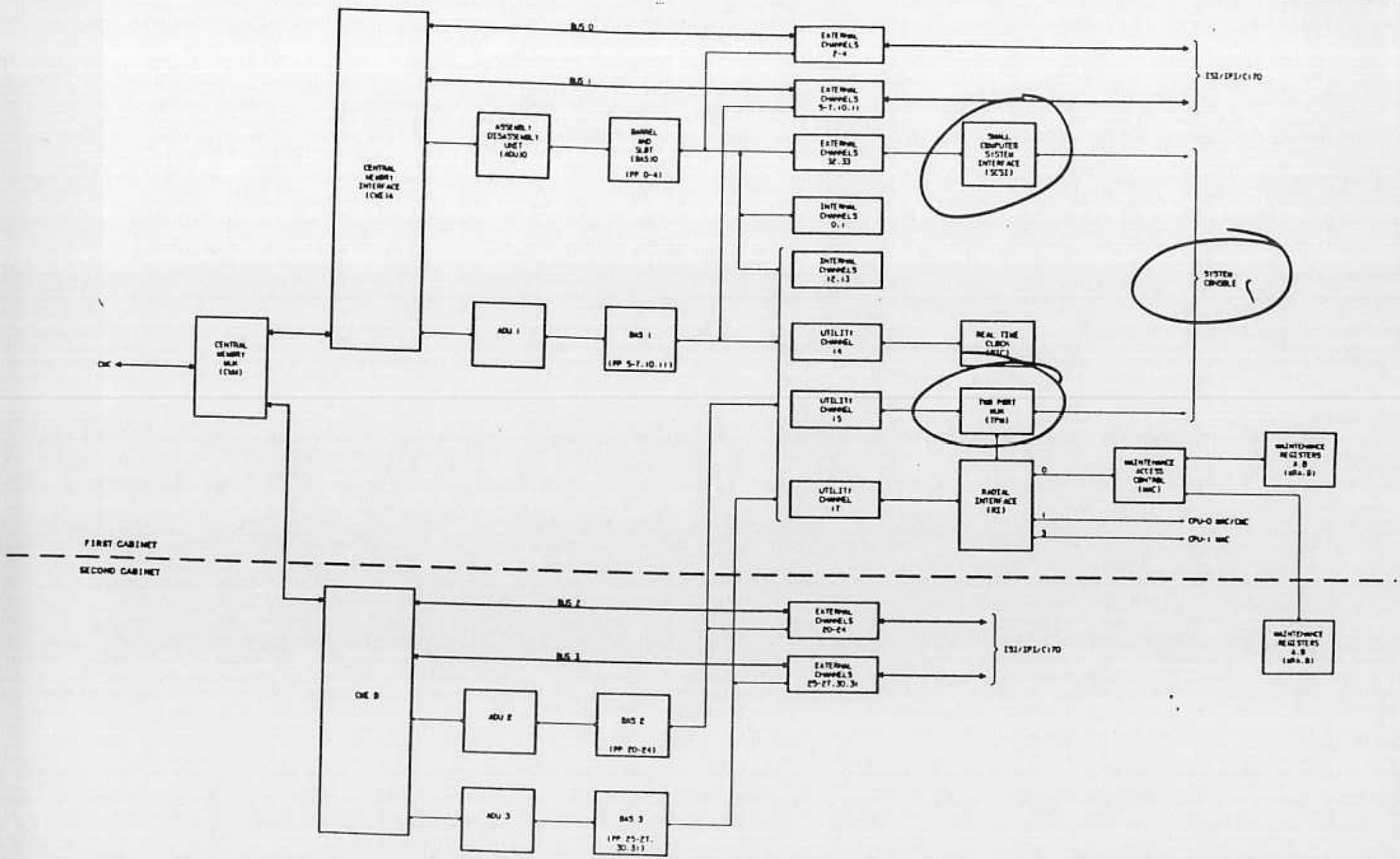
At this time the PC will load the diskette based diagnostics from the diskette and a selection menu will appear.

Hostess Board Testing

A special test for the Hostess Multi-port Adaptor board is contained on a diskette by itself. This test is provided by the manufacturer of the Hostess Board (Control Systems).

A bootable diskette should have been created during the console installation procedure. Instructions are in the Console Manual (Pub. No. 60463610).

Instructions for running the Hostest diagnostics are also in the Console Manual. A jumper plug is required to test each port of the Hostess Board. This jumper plug is provided as part of the console.

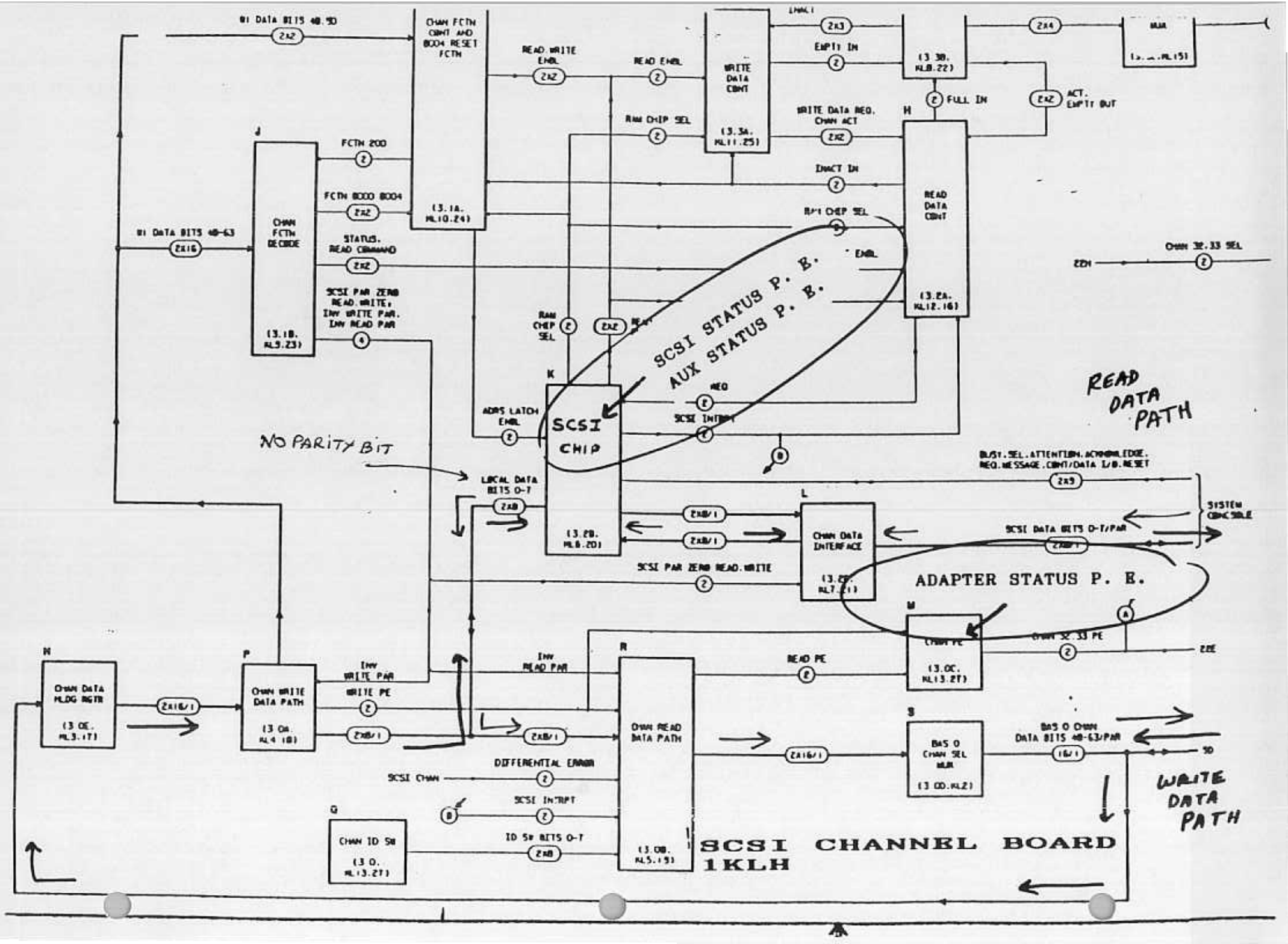


12-9

INPUT/OUTPUT UNIT

IHC

235 A


SCSI CHANNEL BOARD
1KLH
SCSI CHIP
CHAN FCTN DECODE
CHAN FCTN CONT AND BOOT RESET FCTN
WRITE DATA CONT
READ DATA CONT
CHAN DATA INTERFACE
CHAN WRITE DATA PATH
CHAN READ DATA PATH
CHAN DATA HLDG RGTR
CHAN ID SW
BUS 0 CHAN SEL MUX
SCSI STATUS P. B.
AUX STATUS P. B.
ADAPTER STATUS P. E.
NO PARITY BIT
READ DATA PATH
WRITE DATA PATH
FCTN 200
FCTN 8000 8004
STATUS. READ COMMAND
SCSI PAR ZERO READ. WRITE, INV WRITE PAR. INV READ PAR
ADRS LATCH ENBL
LOCAL DATA BITS 0-7
SCSI PAR ZERO READ. WRITE
INV WRITE PAR
INV READ PAR
WRITE PE
READ PE
DIFFERENTIAL ERROR
SCSI CHAN
SCSI INTRPT
ID SW BITS 0-7
EMPTY IN
FULL IN
ACT. EMPTY OUT
INACT IN
SCSI DATA BITS 0-7/PAR
BUS 0 CHAN DATA BITS 48-63/PAR

SYSTEM LEVEL INFORMATION

Equipment Configuration

The CSD will be deadstart loaded into a Cyber 180 I4C's PP via the File Server (or PC Console). The I4C's SCSI interface includes an I4C/SCSI Adapter that contains Western Digital's SBIC chip (WD33C92); which acts as a differential Initiator SCSI device. Connected to the Adapter is a differential SCSI bus that can attach multiple I4Cs to one File Server; which is a PC Console with the Dedicated Load Device (DLD) being a Wren III disk drive. The PC Console uses its built-in operating system, MS-DOS, to perform the various file and directory operations on the DLD. Figure 10 will show the complete hardware picture.

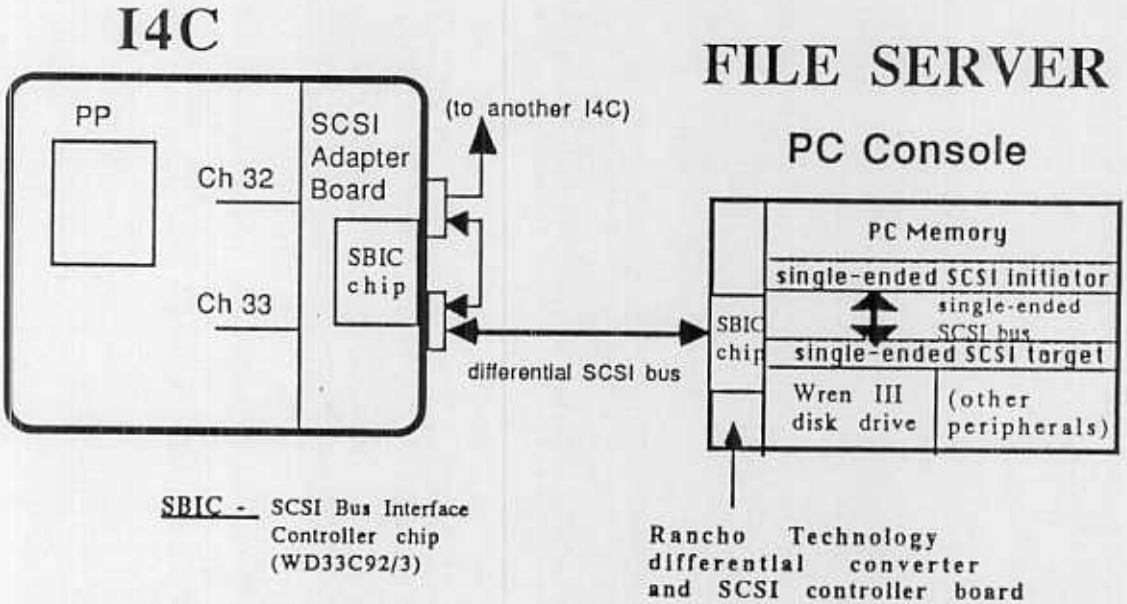


Figure 10 - Equipment Environment for the CSD

RAM

The CSD will be available via the CIP tape and on the DLD disk. The CSD will be maintained via PSR control.

Security and Controls

The CSD can only pervent itself from hanging the PP up. It can't be concerned about being ordered to delete a file one moment, and then being ordered to read that same file the next moment. The responsibility of this kind of problem belongs to the CSD's calling program.

The CSD does provide the calling program with the ability to master clear all of the logic on the I4C/SCSI Adapter board, which includes a RESET command to its SBIC chip. This Master Clear does not affect the differential SCSI bus or the PC Console hardware or software in any way. After reporting any detected errors, the PC Console software will reset its own SCSI hardware and "prime" its SBIC chip by issuing the Wait-for Select-and-Receive command to it. This will ensure that the PC Console will be waiting indefinately for the CSD to select it for another operation.

Human Factors

(Not applicable; since the CSD interfaces with Maintenance Software on its upper end, and with the File Server (PC Console, DLD) software on its lower end. The main goal of the CSD is to accurately pass the calling program's designated task information to the File Server, and to accurately receive the results of the task from the File Server and pass it all to the calling program. So the File Server does all the actual work for each task.)

Installability

The CSD is designed to be loaded into any part of an I4C's PP. The File Server will load the CSD into a PP at deadstart time via the I4C's Two-Port Multiplexer (TPM). The CSD will use less than 2048 (decimal) 16-bit PP words.

Restrictions and Limitations

The Maintenance Software programs are limited to using the FMT features that are described in section 4.0. The maximum data transfer length for each calling of the write or read-type tasks is dependent on the size of the calling program's PP data buffer, and is given as an input parameter for each pass/calling of an FMT. The number of files that a directory on the DLD can have is limited only by the amount of available space on the disk drive. The number of file names that are given to the CSD and calling program as data (with the LIST DIRECTORY task) are also limited only by the quantity specified by the calling program. The Own ID address of the target (PC Console) end of the differential SCSI bus must always be fixed (presently to a 1).

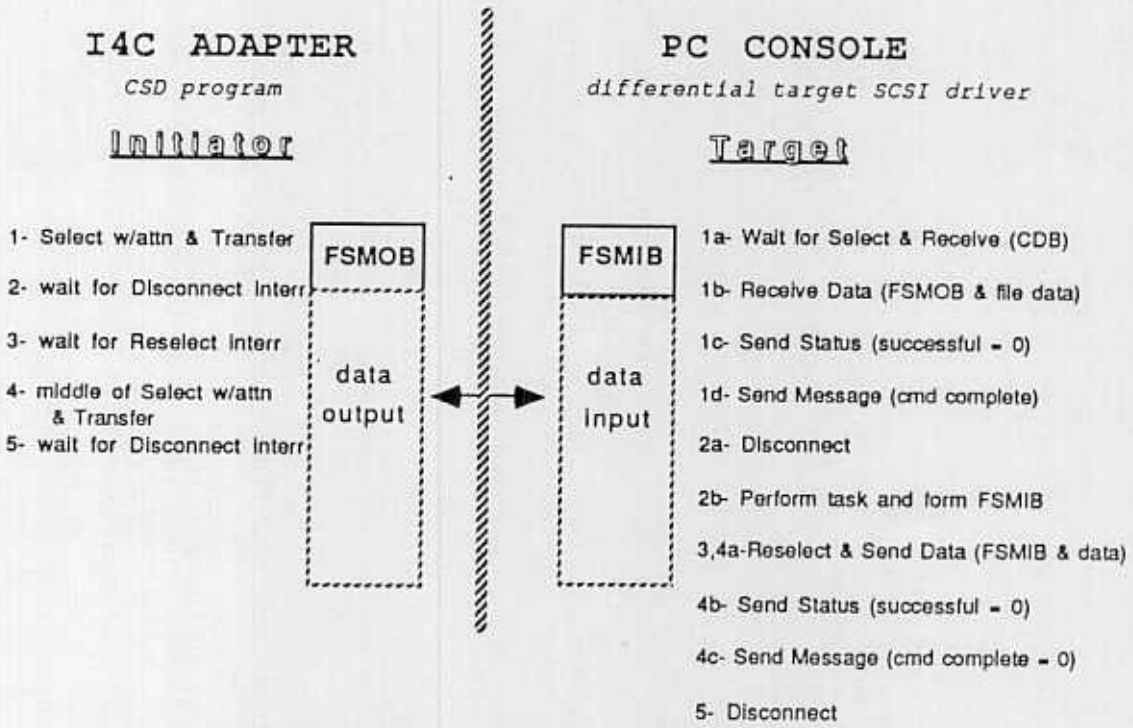
SPECIAL CONSIDERATIONS

SCSI Command Usage

This section will describe the SBIC commands that are used by the CSD to perform the FMTs that are described in section 4.0. The CSD employs a simple plan to communicate instructions and data with the PC Console across the differential SCSI bus. The FSMOB and any data associated with it gets sent to the PC Console in order to start or continue the task that the calling program requested. The FSMIB and any related data gets sent back to the CSD and calling program's data buffer in response to the given task. The FSMOB is sent to the PC Console via the SEND (0A) standard SCSI command. The FSMIB is inputted from the PC Console with the RECEIVE (08) standard SCSI command. Both of these commands are put in the first byte of the Command Description Block (CDB) registers of the SBIC chip. Bytes 4 and 5 of the CDB will contain the total number of data bytes that the current task is requesting to be transferred. This value is specified by the calling program as a PP word count. The second byte of the CDB will contain the value of the Sync Transfer Count that must be used by both the initiator and target for data transfer timing synchronization.

SCSI Command Usage (con't)

Figure will show the low-level WD33C92/3 SBIC commands that are used to perform the simple SCSI protocol that was explained above. Remember that all of these sequences reflect command activity at the SBIC-chip/SCSI bus level.



SEQUENCE STEP DEFINITIONS

0 - Target "primes" SBIC chip with Wait for Select and Receive cmd
1 - FSMOB and any file data is sent to Target
2 - Target disconnects from Initiator and performs task
3 - Target reselects Initiator
4 - Target sends FSMIB and any file data to Initiator
5 - Target disconnects from Initiator and returns to step 0

SBIC chip commands used by the CSD and PC Console

Fault Detection

This section will be on the fault detection of the CSD and its processor environment components. The CSD is designed to stop on any error to isolate it, assign an error code to it, and pass this error code up to the calling program. The data path that these CSD errors cover is from the PP to the I4C/SCSI Adapter (including the Western Digital SBIC chip), and across the differential SCSI bus to the target SCSI device's SBIC chip in the PC Console, and to the internal memory of the PC Console's differential SCSI controller board (the Rancho SCSI board). The PC Console has the responsibility to cover the DLD (Wren III disk drive) to PC memory data path, across the single-ended SCSI bus, with a set of error codes that it passes up to the CSD via the File Server Message Input Block (FSMIB). This is the File Server's error code that gets passed to the CSD's calling program via the TSB+FSEC status word (see section 5.2.2.1). See section 9.4 for a description of all the CSD-generated error codes.

A 1 millisecond delay had to be put in the CSD just before the SCSI Phase register is read because the Western Digital SBIC chip will not update the Phase register until after the Command Complete interrupt has been raised.

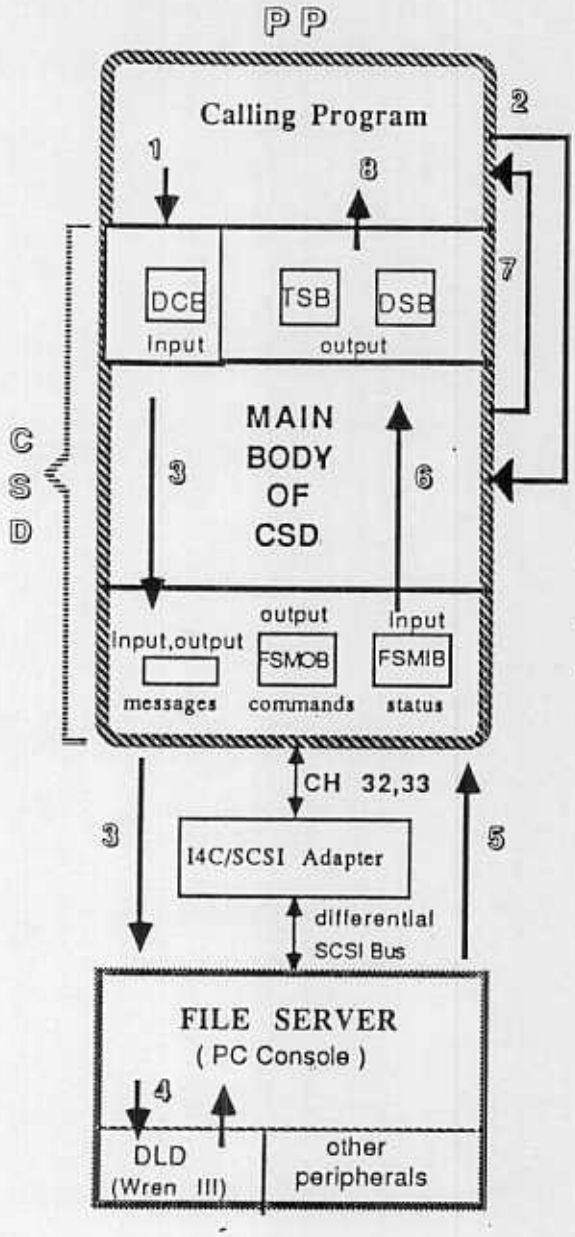
CONCURRENCE WITH REQUIREMENTS

The CSD complys fully with its Design Direction document, dated 8/28/87.

APPENDIX

Process Flow of a File Management Task (FMT)

Figure 12 contains a summary of all the steps involved during the processing of a File Management Task that is initiated by the CSD's calling program.



1 - Calling Program (ie: CMSE) loads CSD's Driver Control Block (DCB) with the File Management Task (FMT) and associated information.

2 - Calling Program calls the CSD via an RJM PP instruction.

3 - CSD reads DCB and initiates designated task by making the SCSI Adapter operate the SCSI phases to get the FMT's command/data down to the File Server.

4 - File Server performs the CSD's command.

5 - File Server sends status and/or data from the FMT back to the CSD.

6 - CSD fills interface 1's status blocks (TSB and DSB) with FMT's results.

7 - CSD returns control to calling program.

8 - Calling Program reads task's results by accessing the Task and Detailed Status Blocks of the CSD (TSB & DSB).

The Process Flow of a File Management Task (FMT)

Glossary

Here is a glossary of abbreviations and special terms that are used often in this ERS ...

CB --- Command Buffer directory for CMSE's command buffer files
CDA --- Common Disk Area directory
CIP --- CYBER Initialization Package
CMSE --- Common Maintenance Software Executive
CSD --- Common SCSI Driver
CTI --- Common Test and Initialization directory
DCB --- Driver Control Block used by maintenance software programs to control the CSD
DCS --- Documentation Control System
DFT --- Dedicated Fault Tolerant module
differential a SCSI bus and logic structure that can be connected to another SCSI device with a cable length greater than 6 meters.
DLD --- Dedicated Load Device; which is the Wren III disk drive
DSB --- Detailed Status Block used by the CSD to inform maintenance software of any detailed error conditions resulting from the latest task issued.
DTL --- Data Transfer Length of a current data transfer to/from the calling program and to/from the File Server.
ERS --- External Reference Specification
Executive the PC Console program that controls all TPM, SCSI, and console operations that the File Server gets to perform.
FDN --- File/Directory Name's hex-ASCII byte representing one of its letters (characters).
File Server -- the I4C's PC Console and its DLD.
FMT --- File Management Task
FSEC --- File Server Error Code generated by the File Server.
FSMIB--- File Server Message Input Block
FSMOB--- File Server Message Output Block
FWA --- First Word Address of an area in a PP's memory

Glossary (con't)

GS --- General Status word given to the calling program by the CSD following the execution of a task.

IDS --- Internal Design Specification

Initiator a SCSI device that selects and sends SCSI commands to another SCSI device.

I/O --- Input/Output

MS-DOS--- the internal operating system software of the PC Console.

MSL --- Maintenance Software Library directory on the DLD

OFC --- Offset Count in bytes for the Read Offset File task, or the number of file names for the List Directory task.

PC --- Personal Computer

PC Console a Zenith personal computer that is used as a system or maintenance console for a Cyber mainframe.

PP --- Peripheral Processor

PSR --- Programming System Report

SBIC --- SCSI Bus Interface Controller chip by Western Digital - WD33C92/3.

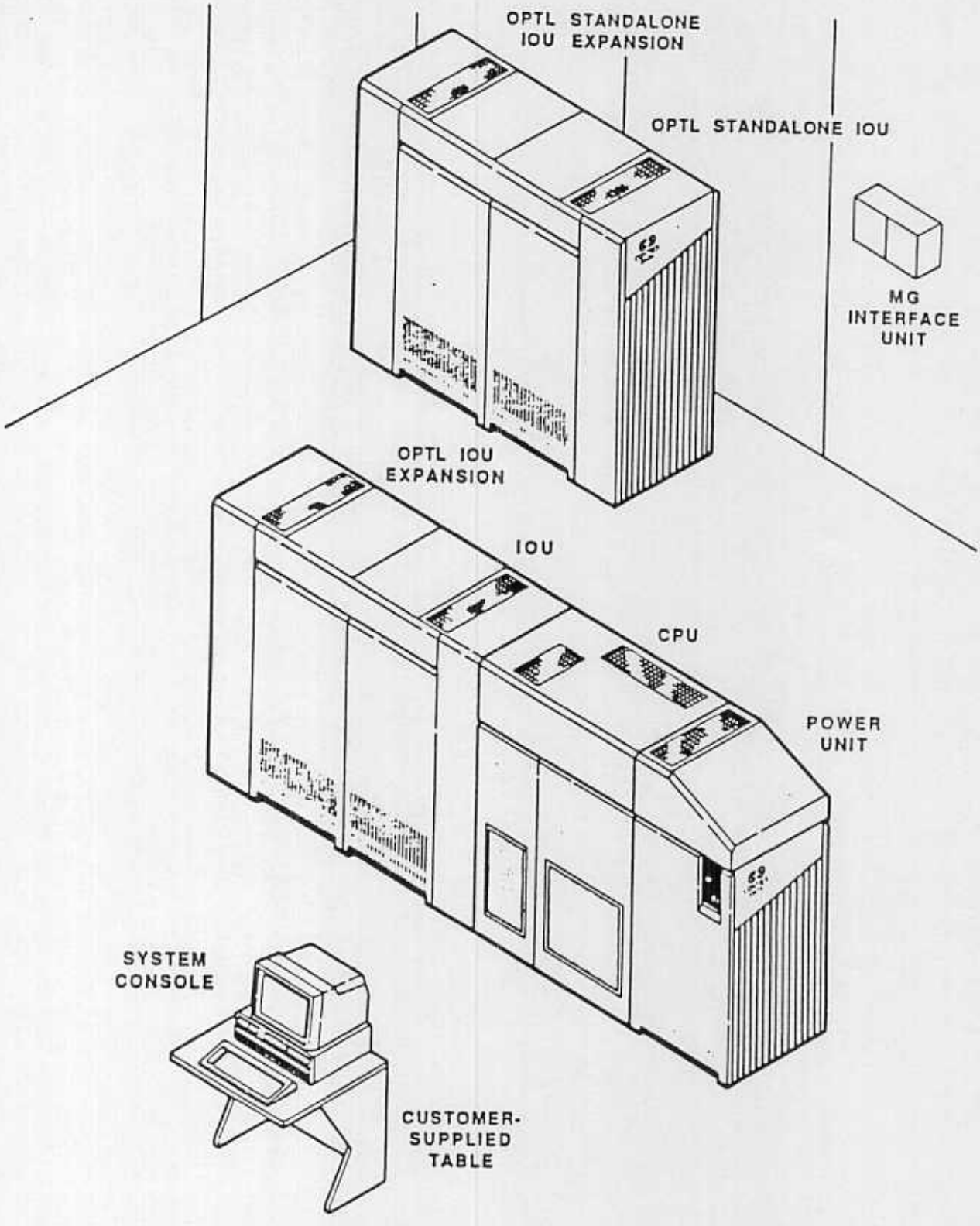
SCSI --- Small Computer Standard Interface

single-ended -- a SCSI bus and logic structure that can only be connected to another SCSI device with a cable length of 6 meters or less.

Target--- a SCSI device that receives and executes commands that are sent to it by the Initiator.

TPM --- Two-Port Multiplexer (Mux)

TSB --- Task Status Block used by the CSD to inform maintenance software of the latest task's (FMT's) condition/error status.


OPTL STANDALONE
IOU EXPANSION
OPTL STANDALONE IOU
MG
INTERFACE
UNIT
OPTL IOU
EXPANSION
IOU
CPU
POWER
UNIT
SYSTEM
CONSOLE
CUSTOMER-
SUPPLIED
TABLE

CYBER 960
SYSTEM INITIALIZATION

SYSTEM CONFIGURATION

IOU, CPU, CENTRAL MEMORY

* Minimum configuration (one each)

IOU INITIALIZATION

- Test PP memories
- Set all PP memories to all ones.
- Set all PPs to deadstart state.

MASTER CLOCK INITIALIZATION

- Read adjustment data from appropriate PROM.
- Write PROM data to associated clock array.
- Read clock array and compare clock data with data read from the associated PROM to ensure correctness.
- Rewrite the clocks to complete the initialization.

CENTRAL MEMORY INTIALIZATION

- Load central memory bank control
- Initialize central memory control maintenance registers. (enviroment control, memory bounds and error logs.)
- Initialize memory address space to all ones via a microcode routine.

CPU INITIALIZATION

- Initialize CPU maintenance registers (dependent environment control and processor test mode)
- Load CPU control memories with associated microcode files
- Initialize all registers, files, maps, and cache to contain correct parity.

HAND-OFF

- Maintenance
- NOS/VE stand-alone
- NOS or NOS/BE stand-alone and dual state

860/960 DIAGNOSTIC DIFFERENCES

- FEW DIFFERENCES

  The 960 diagnostics are an extension of the current 860 diagnostics.

- DIFFERENCES TEST/SUPPORT THE HARDWARE DIFFERENCES

  * Master clock system

    CMT3P S01, SB10-15
    MCT3P S01, SB10-15 (essentially the same as CMT3P)

  * CM Page 0 relocation

    CMT3P S24, SB05

  * First Failure Capture (bit 34 of CPU DEC)

    MCT3 S29, SB00 and SB01

  * PDM Halt (bit 43 of CPU DEC)

  * Enable Expanded Control Store Addressing
    (bit 46 of CPU DEC register)

    Tested in CST3P and elsewhere.

  * Toggle of CS Address (CY180/CY170) with VMID.
    (bit 48 of CPU DEC register)

    ICT3P S04, SB04

  * Expanded CM and CM Addressing.

    CMT3P, MAT3P, LMT3P, and others.

  * Larger PTA/PTL registers

    LMT3P S15 and greater
    (All subsections of LMT3P report as their last condition -1. the first failure capture bits, 2. the last PTA value written, and 3. the last PTL value written.)

  * Micrand Address Register bits 51 and 52

    Primarily CST3P and ICT3P

rjrassel 8-03-88

NEW DIAGNOSTICS AND PROCEDURES

- The only new diagnostics are a few new sections and subsections added to support the new logic.

  * CMT3P and MCT3 section 01 (tests master clock system)

    SB10 - Read the clock PROMs and verify the ID information.
    SB11 - Test MAC address bus and parity checkers.
    SB12 - Test write/read/data holding capability of the clock registers.
    SB13 - Write all registers. Read and verify.
    SB14 - Force clock register parity errors.
    SB15 - Force clock address parity errors.

  * CMT3P section 24, subsection 05 tests CM page zero relocation. A block of known data is written to page 0 and 1 of the memory. The page relocation control is then used to switch addressing from one page to the other. The data from each page is read and verified with the data written to the other.

  * MCT3P section 29 tests the First Failure Capture mechanism. Errors are forced to the clock subsystem and the effect on the First Failure Capture status is verified.

- The main new variation in the diagnostic system is the requirement that the system be initialized before running any of the diagnostics. The exceptions are sections 0 and 1 of CMT3P and MCT3. These sections should run even though the clock subsystem has not been initialized.

  Diagnostics do not initialize the master clock system. This must be done with the system initialization (U-I-M).

- Fault isolation is available to some extent in CMT3P and MAT3P. The method has not changed from the 860 tests. The effectiveness may increase slightly because of the reduced number of FRUs.

  A new program, PFSA, has been developed to help isolate CPU errors based on the PFS register values. This program reads the values in the registers at load time. It then uses these values to choose up to four possible failing FRUs. The program will display the FRU list or other informative messages after the analysis is complete.

  This program can be used after any failure. All that is necessary is that the error signature be in the PFS registers of the CPU. The program can be called by LT,PFSA

MARK LINE PARITY ERROR

```
08 0FFF - Possible set bits
08 00XX - CMCB or CPU-A
08 01XX - CMCB or IOU-A
08 02XX - CMCB or CPU-B
08 03XX - CMCB or IOU-B
08 0400 - CMCB
 .  .     .
08 04FF - CMCB
08 08XX - CMCB or CPU-A
08 09XX - CMCB or IOU-A
08 0AXX - CMCB or CPU-B
08 0BXX - CMCB or IOU-B
08 0C00 - CMCB
 .  .     .
08 0CFF - CMCB
```

TAG PARITY ERROR

```
0C 0700 - Possible set bits
0C 0000 - CMCB or CPU-A
0C 0100 - CMCB or IOU-A
0C 0200 - CMCB or CPU-B
0C 0300 - CMCB or IOU-B
0C 0400 - CMCB
 .  .     .
0C 04FF - CMCB
```

CMC ADDRESS PARITY ERROR

```
1C 070F  possible set bits
10 000X  CMCB or cpu-0
10 010X  CMCB or IOU
10 020X  CMCB or cpu-1

14 000X  CMCB or cpu-0
14 010X  CMCB or IOU
14 020X  CMCB or cpu-1

18 000X  CMCB or cpu-0
18 010X  CMCB or IOU
18 020X  CMCB or cpu-1

1C 000X  CMCB or cpu-0
1C 010X  CMCB or IOU
1C 020X  CMCB or cpu-1
```

Where X identifies the address byte in error.

TEST FAULT SYMPTOM CODES

FSC1 = ABBCCDD

A - FAILING TEST

1 - ACT3P etc.

2 - ANT3P F - SMT3P

BB - SECTION NUMBER

CC - SUBSECTION NUMBER

DD - ITERATION NUMBER

FSC2 = EEEEFF

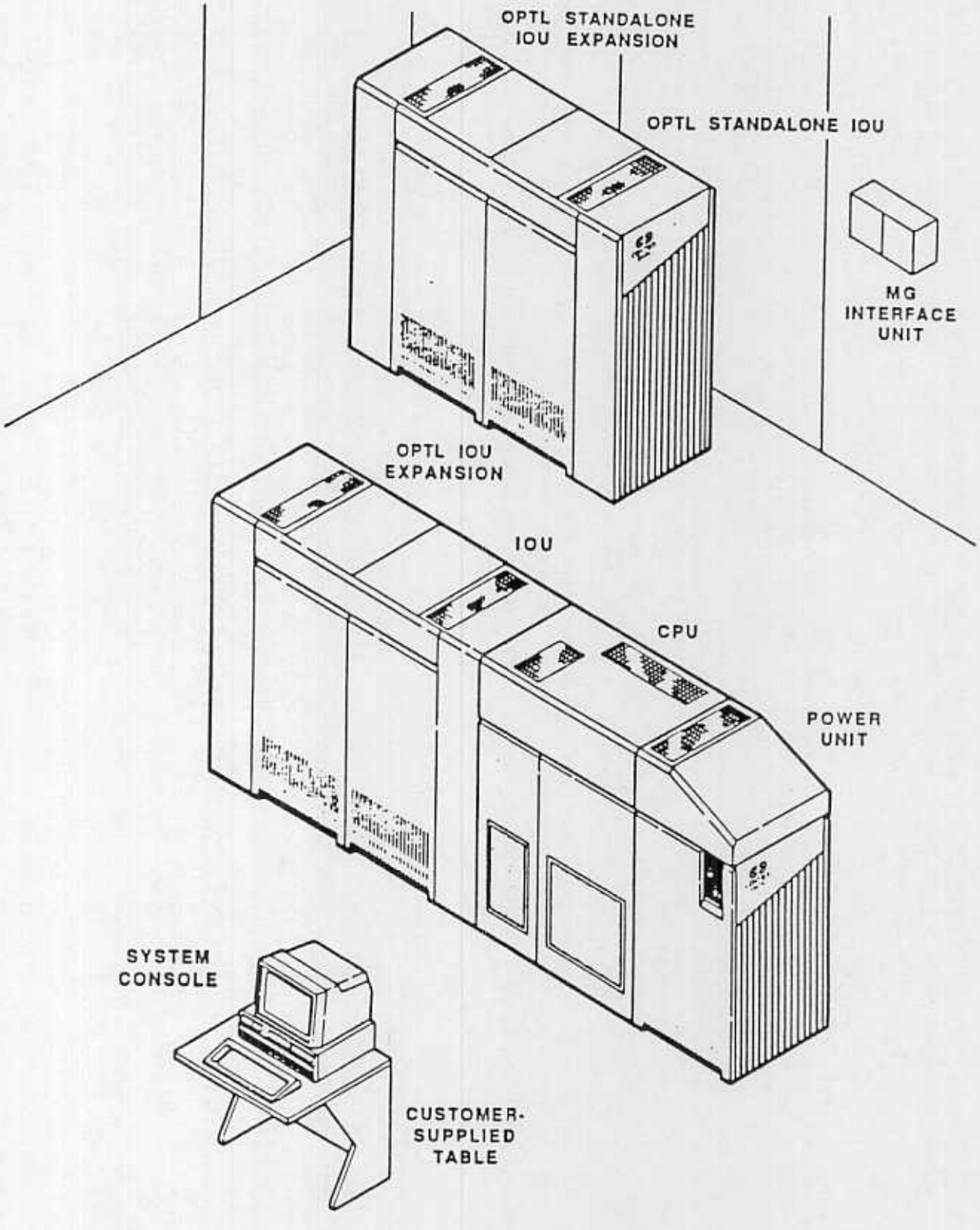
EEEE - FAILING CONDITIONS INDICATED BY BITS FOR EACH. C15-C00

FF - BYTES THAT MISCOMPARE ON THE FIRST BAD CONDITION.

```
NCH 00   01   02   03   04   05   06   07   10   11   12   13   15   17
    -00 E00 -00 F00 -    E    E    E    F    E   -10 -    -    -
NCH 20   21   22   23   24   25   26   27   30   31   32   33
    E    E    E    E    E    E    E    E    E    E    E    E

ST SS SE RB
ICT3P SE  PC0000 S0004  SB0004 C0010 I0000  VER=88/ 07 /05
EC1=1A60  EC2=0404 TE=0005    FSC1=7040400  FSC2 =030001
ITER ERR--MSYM ERROR IN CPU0  UCNT

00 EXP= 0003  0003  0003  0001 RCV= 0003  0003  0003  0001
01      0001  0003  0000  1003       0001  0003  0000  1003
02      0004  0004  0004  0002       0004  0004  0004  0002
03      0002  0004  0000  0003       0002  0004  0000  0003
04      0001  0001  0001  0001       0001  0001  0001  0001
05      0001  0001  0000  1803       0001  0001  0000  1803
06      0003  0003  0003  0003       0003  0003  0003  0003
07      0003  0003  0000  1003       0003  0003  0000  1003
08      0004  0004  0004  0004       0004  0004  0004  0000 F
09      0004  0004  0000  0003       0000  0000  0000  0047 F
10      0000  0000  0000  0004       0000  0000  0000  0004
```


OPTL STANDALONE
IOU EXPANSION
OPTL STANDALONE IOU
MG
INTERFACE
UNIT
OPTL IOU
EXPANSION
IOU
CPU
POWER
UNIT
SYSTEM
CONSOLE
CUSTOMER-
SUPPLIED
TABLE

CABLE TABS

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I4 CABLE TABS

SIGNAL	I4 ORIGIN	I4 EXT CONN/PIN	CMC EXT CONN/PIN	CMC	ROW	IODATP/IOUDAT COL/PIN/PIN
WRITE BIT 0	AO2-B56	J56-23	PO7 23/24	A	N	5/086/088
WRITE BIT 1	AO2-B41	J54-23	RO7 23/24	A	N	5/132/130
WRITE BIT 2	AO2-A41	J52-23	PO9 23/24	A	N	7/062/064
WRITE BIT 3	AO2-A42	J50-23	RO9 23/24	A	N	7/108/106
WRITE BIT 4	AO2-A43	J56-17	PO7 17/18	A	N	5/084/082
WRITE BIT 5	AO2-A45	J54-17	RO7 17/18	A	N	5/116/118
WRITE BIT 6	AO2-A46	J52-17	PO9 17/18	A	N	7/060/058
WRITE BIT 7	AO2-A47	J50-17	RO9 17/18	A	N	7/092/094
WRITE BIT 8	AO2-A49	J57-07	PO3 07/08	A	N	1/110/112
WRITE BIT 9	AO2-A50	J55-07	RO3 07/08	A	N	1/162/160
WRITE BIT 10	AO2-A51	J53-07	PO5 07/08	A	N	3/086/088
WRITE BIT 11	AO2-A52	J51-07	RO5 07/08	A	N	3/132/130
WRITE BIT 12	AO2-A53	J56-07	PO7 07/08	A	N	5/062/064
WRITE BIT 13	AO2-A55	J54-07	RO7 07/08	A	N	5/108/106
WRITE BIT 14	AO2-A56	J52-07	PO9 07/08	A	N	7/032/034
WRITE BIT 15	AO2-A57	J50-07	RO9 07/08	A	N	7/084/082
WRITE BIT 16	AO3-B56	J57-05	PO3 05/06	A	N	1/114/112
WRITE BIT 17	AO3-B41	J55-05	RO3 05/06	A	N	1/152/154
WRITE BIT 18	AO3-A41	J53-05	PO5 05/06	A	N	3/090/088
WRITE BIT 19	AO3-A42	J51-05	RO5 05/06	A	N	3/122/124
WRITE BIT 20	AO3-A43	J57-03	PO3 03/04	A	N	1/104/106
WRITE BIT 21	AO3-A45	J55-03	RO3 03/04	A	N	1/156/154
WRITE BIT 22	AO3-A46	J53-03	PO5 03/04	A	N	3/080/082
WRITE BIT 23	AO3-A47	J51-03	RO5 03/04	A	N	3/126/124
WRITE BIT 24	AO3-A49	J56-01	PO7 01/02	A	N	5/060/058
WRITE BIT 25	AO3-A50	J54-01	RO7 01/02	A	N	5/092/094
WRITE BIT 26	AO3-A51	J52-01	PO9 01/02	A	N	7/030/028
WRITE BIT 27	AO3-A52	J50-01	RO9 01/02	A	N	7/068/070
WRITE BIT 28	AO3-A53	J57-01	PO3 01/02	A	N	1/108/106
WRITE BIT 29	AO3-A55	J55-01	RO3 01/02	A	N	1/140/142
WRITE BIT 30	AO3-A56	J53-01	PO5 01/02	A	N	3/084/082
WRITE BIT 31	AO3-A57	J51-01	RO5 01/02	A	N	3/116/118
WRITE BIT 32	AO4-B56	J57-21	PO3 21/22	A	N	1/138/136
WRITE BIT 33	AO4-B41	J55-21	RO3 21/22	A	N	1/176/178
WRITE BIT 34	AO4-A41	J53-21	PO5 21/22	A	N	3/114/112
WRITE BIT 35	AO4-A42	J51-21	RO5 21/22	A	N	3/152/154
WRITE BIT 36	AO4-A43	J56-21	PO7 21/22	A	N	5/090/088
WRITE BIT 37	AO4-A45	J54-21	RO7 21/22	A	N	5/122/124
WRITE BIT 38	AO4-A46	J52-21	PO9 21/22	A	N	7/066/064
WRITE BIT 39	AO4-A47	J50-21	RO9 21/22	A	N	7/098/100
WRITE BIT 40	AO4-A49	J57-17	PO3 17/18	A	N	1/132/130
WRITE BIT 41	AO4-A50	J55-17	RO3 17/18	A	N	1/170/172
WRITE BIT 42	AO4-A51	J53-17	PO2 17/18	A	N	3/108/106
WRITE BIT 43	AO4-A52	J51-17	RO5 17/18	A	N	3/140/142
WRITE BIT 44	AO4-A53	J56-15	PO7 15/16	A	N	5/074/076
WRITE BIT 45	AO4-A55	J54-15	RO7 15/16	A	N	5/120/118
WRITE BIT 46	AO4-A56	J52-15	PO9 15/16	A	N	7/050/052
WRITE BIT 47	AO4-A57	J50-15	RO9 15/16	A	N	7/096/094
WRITE BIT 48	AO5-B56	J57-23	PO3 23/24	A	N	1/134/136
WRITE BIT 49	AO5-B41	J55-23	RO3 23/24	A	N	1/186/184
WRITE BIT 50	AO5-A41	J53-23	PO5 23/24	A	N	3/110/112
WRITE BIT 51	AO5-A42	J51-23	RO5 23/24	A	N	3/162/160
WRITE BIT 52	AO5-A43	J56-03	PO7 03/04	A	N	5/056/058
WRITE BIT 53	AO5-A45	J54-03	RO7 03/04	A	N	5/102/100
WRITE BIT 54	AO5-A46	J52-03	PO9 03/04	A	N	7/026/028
WRITE BIT 55	AO5-A47	J50-03	RO9 03/04	A	N	7/078/076
WRITE BIT 56	AO5-A49	J57-09	PO3 09/10	A	N	1/120/118
WRITE BIT 57	AO5-A50	J55-09	RO3 09/10	A	N	1/158/160
WRITE BIT 58	AO5-A51	J53-09	PO5 09/10	A	N	3/096/094
WRITE BIT 59	AO5-A52	J51-09	RO5 09/10	A	N	3/128/130
WRITE BIT 60	AO5-A53	J56-09	PO7 09/10	A	N	5/072/070
WRITE BIT 61	AO5-A55	J54-09	RO7 09/10	A	N	5/104/106
WRITE BIT 62	AO5-A56	J52-09	PO9 09/10	A	N	7/042/040
WRITE BIT 63	AO5-A57	J50-09	RO9 09/10	A	N	7/080/082
WRITE BIT 64	AO2-A48	J57-11	PO3 11/12	A	N	1/116/118
WRITE BIT 65	AO2-A58	J57-15	PO3 15/16	A	N	1/122/124
WRITE BIT 66	AO3-A48	J55-11	RO3 11/12	A	N	1/166/168
WRITE BIT 67	AO3-A58	J55-15	RO3 15/16	A	N	1/172/174
WRITE BIT 68	AO4-A48	J53-11	PO5 11/12	A	N	3/092/094
WRITE BIT 69	AO4-A58	J53-15	PO5 15/16	A	N	3/098/100
WRITE BIT 70	AO5-A48	J51-11	RO5 11/12	A	N	3/136/138
WRITE BIT 71	AO5-A58	J51-15	RO5 15/16	A	N	3/142/144

SIGNAL	I4 DEST.	I4 CONN/PIN	CMC OUT CONN/PIN	CMC	ROW	SIGNAL IORDP/IOURD COL/PIN/PIN
READ BITS						
READ BIT 0	AO2-A73	J67-03	R10 04/03	B	M	8/152/155
READ BIT 1	AO2-A84	J66-03	P10 04/03	B	M	8/126/124
READ BIT 2	AO2-A74	J67-05	R10 06/05	B	M	8/162/160
READ BIT 3	AO2-A85	J66-05	P10 06/05	B	M	8/122/125
READ BIT 4	AO2-A75	J67-07	R10 08/07	B	M	8/158/161
READ BIT 5	AO2-A86	J67-09	R10 10/09	B	M	8/168/166
READ BIT 6	AO2-A76	J67-15	R10 16/15	B	M	8/170/173
READ BIT 7	AO2-A88	J67-19	R10 20/19	B	M	8/176/179
READ BIT 8	AO2-A78	J67-13	R10 14/13	B	M	8/174/172
READ BIT 9	AO2-A89	J66-19	P10 20/19	B	M	8/156/154
READ BIT 10	AO2-A79	J67-11	R10 12/11	B	M	8/164/167
READ BIT 11	AO2-A90	J67-17	R10 18/17	B	M	8/180/178
READ BIT 12	AO2-A80	J66-15	P10 16/15	B	M	8/144/142
READ BIT 13	AO2-A91	J66-13	P10 14/13	B	M	8/134/137
READ BIT 14	AO2-A81	J66-11	P10 12/11	B	M	8/138/136
READ BIT 15	AO2-A92	J66-09	P10 10/09	B	M	8/128/131
READ BIT 16	AO3-A73	J65-03	R08 04/03	B	M	8/038/041
READ BIT 17	AO3-A84	J64-03	P08 04/03	B	M	8/018/016
READ BIT 18	AO3-A74	J65-05	R08 06/05	B	M	8/048/046
READ BIT 19	AO3-A85	J64-05	P08 06/05	B	M	8/014/017
READ BIT 20	AO3-A75	J65-07	R08 08/07	B	M	8/044/047
READ BIT 21	AO3-A86	J65-09	R08 10/09	B	M	8/054/052
READ BIT 22	AO3-A76	J65-15	R08 16/15	B	M	8/056/059
READ BIT 23	AO3-A88	J65-19	R08 20/19	B	M	8/062/065
READ BIT 24	AO3-A78	J65-13	R08 14/13	B	M	8/060/058
READ BIT 25	AO3-A89	J64-19	P08 20/19	B	M	8/042/040
READ BIT 26	AO3-A79	J65-11	R08 12/11	B	M	8/050/053
READ BIT 27	AO3-A90	J65-17	R08 18/17	B	M	8/066/064
READ BIT 28	AO3-A80	J64-15	P08 16/15	B	M	8/036/034
READ BIT 29	AO3-A91	J64-13	P08 14/13	B	M	8/026/029
READ BIT 30	AO3-A81	J64-11	P08 12/11	B	M	8/030/028
READ BIT 31	AO3-A92	J64-09	P08 10/09	B	M	8/020/023
READ BIT 32	AO4-A73	J63-03	R06 04/03	B	M	6/125/122
READ BIT 33	AO4-A84	J62-03	P06 04/03	B	M	6/102/100
READ BIT 34	AO4-A74	J63-05	R06 06/05	B	M	6/132/130
READ BIT 35	AO4-A85	J62-05	P06 06/05	B	M	6/198/100
READ BIT 36	AO4-A75	J63-07	R06 08/07	B	M	6/128/131
READ BIT 37	AO4-A86	J63-09	R06 10/09	B	M	6/138/136
READ BIT 38	AO4-A76	J63-15	R06 16/15	B	M	6/140/143
READ BIT 39	AO4-A88	J63-19	R06 20/19	B	M	6/146/149
READ BIT 40	AO4-A78	J63-13	R06 14/13	B	M	6/144/142
READ BIT 41	AO4-A89	J62-19	P06 20/19	B	M	6/126/124
READ BIT 42	AO4-A79	J63-11	R06 12/11	B	M	6/134/137
READ BIT 43	AO4-A90	J63-17	R06 18/17	B	M	6/150/148
READ BIT 44	AO4-A80	J62-15	P06 16/15	B	M	6/120/118
READ BIT 45	AO4-A91	J62-13	P06 14/13	B	M	6/110/113
READ BIT 46	AO4-A81	J62-11	P06 12/11	B	M	6/114/112
READ BIT 47	AO4-A92	J62-09	P06 10/09	B	M	6/104/107
READ BIT 48	AO5-A73	J61-03	R04 04/03	B	M	4/056/059
READ BIT 49	AO5-A84	J60-03	R04 04/03	B	M	4/036/034
READ BIT 50	AO5-A74	J61-05	R04 06/05	B	M	4/066/064
READ BIT 51	AO5-A85	J60-05	P04 06/05	B	M	4/032/035
READ BIT 52	AO5-A75	J61-07	R04 08/07	B	M	4/062/065
READ BIT 53	AO5-A86	J61-09	R04 10/09	B	M	4/072/070
READ BIT 54	AO5-A76	J61-15	R04 16/15	B	M	4/074/077
READ BIT 55	AO5-A88	J61-19	R04 20/19	B	M	4/080/083
READ BIT 56	AO5-A78	J61-13	R04 14/13	B	M	4/078/076
READ BIT 57	AO5-A89	J60-19	P04 20/19	B	M	4/060/058
READ BIT 58	AO5-A79	J61-11	R04 12/11	B	M	4/068/071
READ BIT 59	AO5-A90	J61-17	R04 18/17	B	M	4/084/082
READ BIT 60	AO5-A80	J60-15	P04 16/15	B	M	4/054/052
READ BIT 61	AO5-A91	J60-13	P04 14/13	B	M	4/044/047
READ BIT 62	AO5-A81	J60-11	P04 12/11	B	M	4/048/046
READ BIT 63	AO5-A92	J60-09	P04 10/09	B	M	4/038/041
READ BIT 64	AO2-A82	J66-17	P10 17/18	B	M	8/140/143
READ BIT 65	AO2-A83	J66-07	P10 07/08	B	M	8/132/130
READ BIT 66	AO3-A82	J64-17	P08 17/18	B	M	8/032/035
READ BIT 67	AO3-A83	J64-07	P08 07/08	B	M	8/024/022
READ BIT 68	AO4-A82	J62-17	P06 17/18	B	M	6/116/119
READ BIT 69	AO4-A83	J62-07	P06 07/08	B	M	6/106/108
READ BIT 70	AO5-A82	J60-17	P04 17/18	B	M	4/050/053
READ BIT 71	AO5-A83	J60-07	P04 07/08	B	M	4/040/042

SIGNAL	I4 ORIGIN	I4 EXT CONN/PIN	CMC EXT CONN/PIN	CMC ROW	IOADRP/IOUADR COL/PIN/PIN
ADDRESS BITS					
ADRS BIT 1	A06-A39	J64-23	P08 23/24	A N	6/036/034
ADRS BIT 2	A06-A40	J56-05	P07 05/06	A N	5/064/066
ADRS BIT 3	A06-A41	J54-05	R07 05/06	A N	5/100/098
ADRS BIT 4	A06-A42	J52-05	P09 05/06	A N	7/034/036
ADRS BIT 5	A06-A43	J50-05	R09 05/06	A N	7/076/074
ADRS BIT 6	A06-A45	J57-25	P03 25/26	A N	1/142/144
ADRS BIT 7	A06-A46	J56-13	P07 13/14	A N	5/076/078
ADRS BIT 8	A07-A39	J57-13	P03 13/14	A N	1/124/126
ADRS BIT 9	A07-A40	J56-11	P07 11/12	A N	5/070/068
ADRS BIT 10	A07-A41	J54-25	R07 25/26	A N	5/130/128
ADRS BIT 11	A07-A42	J55-25	R03 25/26	A N	1/184/182
ADRS BIT 12	A07-A43	J54-13	R07 13/14	A N	5/112/110
ADRS BIT 13	A07-A45	J55-13	R03 13/14	A N	1/166/164
ADRS BIT 14	A07-A46	J54-11	R07 11/12	A N	5/112/114
ADRS BIT 15	A07-A48	J52-25	P09 25/26	A N	7/070/072
ADRS BIT 16	A07-A49	J53-25	P05 25/26	A N	3/118/120
ADRS BIT 17	A07-A50	J52-13	P09 13/14	A N	7/052/054
ADRS BIT 18	A07-A51	J53-13	P05 13/14	A N	3/100/102
ADRS BIT 19	A07-A52	J52-11	P09 11/12	A N	7/040/038
ADRS BIT 20	A07-A55	J52-19	P09 19/20	A N	7/058/056
ADRS BIT 21	A07-A56	J53-19	P05 19/20	A N	3/106/104
ADRS BIT 22	A07-A57	J50-25	R09 25/26	A N	7/106/104
ADRS BIT 23	A07-A58	J51-25	R05 25/26	A N	3/160/158
ADRS BIT 24	A06-A48	J50-15	R09 15/16	A N	7/088/086
ADRS BIT 25	A06-A49	J51-13	R05 13/14	A N	3/136/134
ADRS BIT 26	A06-A50	J50-11	R09 11/12	A N	7/088/090
ADRS BIT 27	A06-A51	J50-19	R09 19/20	A N	7/100/102
ADRS BIT 28	A06-A52	J51-19	R05 19/20	A N	3/154/156

SIGNAL	I4 ORIGIN	I4 EXT CONN/PIN	CMC EXT CONN/PIN		CMC ROW		COL/PIN/PIN
TAG OUT BITS							
CMC to I-4 TAG OUT 0	A08-A39	J58-21	P02	21/22	B	M	2/142/144
TAG OUT 1	A08-A40	J58-19	P02	19/20	B	M	2/137/134
TAG OUT 2	A08-A41	J58-17	P02	17/18	B	M	2/136/138
TAG OUT 3	A08-A42	J58-15	P02	15/16	B	M	2/131/128
TAG OUT 4	A08-A43	J59-15	R02	15/16	B	M	2/151/152
TAG OUT 5	A08-A45	J58-13	P02	13/14	B	M	2/130/132
TAG OUT 6	A08-A46	J58-11	P02	11/12	B	M	2/125/122
TAG OUT 7	A08-A47	J59-09	R02	09/10	B	M	2/148/150
TAG OUT P	A08-A48	J58-09	P02	09/10	B	M	2/124/126
TAG IN BITS							
TAG IN 0	A08-A72	J66-25	P10	25/26	A	N	6/066/064
TAG IN 1	A08-A73	J64-25	P08	25/26	A	N	6/026/028
I-4 to CMC TAG IN 2	A08-A74	J62-25	P06	25/26	A	N	4/164/166
TAG IN 3	A08-A75	J60-25	P04	25/26	A	N	4/122/124
TAG IN 4	A08-A76	J67-25	R10	25/26	A	N	6/056/058
TAG IN 5	A08-A78	J65-25	R08	25/26	A	N	6/024/022
TAG IN 6	A08-A79	J63-25	R06	25/26	A	N	4/174/172
TAG IN 7	A08-A80	J61-25	R04	25/26	A	N	4/132/130
TAG IN P	A08-A81	J62-~~25~~ 23	P06	~~25/26~~ 23/24	A	N	4/162/160
RESPONSE	A08-A49	J59-23	R02	23/24	B	M	2/164/167
PORT BUSY	A08-A50	J59-11	R02	11/12	B	M	2/146/152
REQUEST	A08-A82	J60-23	P04	23/24	B	M	4/118/120
RESPONSE CODE							
BIT 0	A06-A83	J59-21	R02	21/22	B	M	2/168/166
BIT 1	A06-A82	J59-19	R02	19/20	B	M	2/158/161
BIT 2	A06-A81	J59-17	R02	17/18	B	M	2/162/160
BIT P	A06-A84	J59-13	R02	13/14	B	M	2/156/154
FUNCTION CODE							
BIT 0	A06-A58	J56-19	P07	19/20	A	N	5/080/082
BIT 1	A06-A57	J57-19	P03	19/20	A	N	1/128/130
BIT 2	A06-A56	J54-19	R07	19/20	A	N	5/124/126
BIT 3	A06-A55	J55-19	R03	19/20	A	N	1/178/180
BIT P	A06-A59	J56-25	P07	25/26	A	N	5/096/094
MARK BITS							
BIT 0	A02-A59	J66-21	P10	21/22	A	N	6/072/070
BIT 1	A02-A72	J67-21	R10	21/22	A	N	6/064/062
BIT 2	A03-A59	J64-21	P08	21/22	A	N	6/032/034
BIT 3	A03-A72	J65-21	R08	21/22	A	N	6/028/030
BIT 4	A04-A59	J62-21	P06	21/22	A	N	4/158/160
BIT 5	A04-A72	J63-21	R06	21/22	A	N	4/166/168
BIT 6	A05-A59	J60-21	P04	21/22	A	N	4/118/116
BIT 7	A05-A72	J61-21	R04	21/22	A	N	4/124/126
BIT P	A08-A83	J66-23	P10	23/24	A	N	6/068/070
ADDRESS PARITY							
BIT B0	A06-A47	J67-23	R10	23/24	A	N	6/060/058
BIT B1	A07-A47	J65-23	R08	23/24	A	N	6/020/022
BIT B2	A07-A53	J63-23	R06	23/24	A	N	4/170/172
BIT B3	A06-A53	J61-23	R04	23/24	A	N	4/128/130

NAME IN CMC	CMCA (ROW N) COL/PIN	EXT CONNECTOR SIB A CONN/PIN	CSU CONT BD CONN/PIN	NAME CHIP	CHIP	PIN
WRITE DATA						
TWD0	01/035	06/47	CC06 47	CSUWD0	D001	F02
TWD1	01/031	06/48	CC06 48	CSUWD1	D001	F01
TWD2	01/036	06/45	CC06 45	CSUWD2	D001	G02
TWD3	01/032	06/46	CC06 46	CSUWD3	D001	G01
TWD4	01/041	06/41	CC06 41	CSUWD4	D001	H01
TWD5	01/037	06/42	CC06 42	CSUWD0	D002	F02
TWD6	01/042	06/39	CC06 39	CSUWD1	D002	F01
TWD7	01/038	06/40	CC06 40	CSUWD2	D002	G02
TWD8	01/053	08/47	CC08 47	CSUWD3	D002	G01
TWD9	01/049	08/48	CC08 48	CSUWD4	D002	H01
TWD10	01/054	08/45	CC08 45	CSUWD0	D003	F02
TWD11	01/050	08/46	CC08 46	CSUWD1	D003	F01
TWD12	01/059	08/41	CC08 41	CSUWD2	D003	G02
TWD13	01/055	08/42	CC08 42	CSUWD3	D003	G01
TWD14	01/060	08/39	CC08 39	CSUWD4	D003	H01
TWD15	01/056	08/40	CC08 40	CSUWD0	D004	F02
TWD16	01/066	10/47	CC10 47	CSUWD1	D004	F01
TWD17	01/062	10/48	CC10 48	CSUWD2	D004	G02
TWD18	01/071	10/45	CC10 45	CSUWD3	D004	G01
TWD19	01/067	10/46	CC10 46	CSUWD4	D004	H01
TWD20	01/072	10/41	CC10 41	CSUWD0	D005	F02
TWD21	01/068	10/42	CC10 42	CSUWD1	D005	F01
TWD22	01/077	10/39	CC10 39	CSUWD2	D005	G02
TWD23	01/073	10/40	CC10 40	CSUWD3	D005	G01
TWD24	01/083	12/47	CC12 47	CSUWD4	D005	H01
TWD25	01/079	12/48	CC12 48	CSUWD0	D006	F02
TWD26	01/084	12/45	CC12 45	CSUWD1	D006	F01
TWD27	01/080	12/46	CC12 46	CSUWD2	D006	G02
TWD28	01/089	12/41	CC12 41	CSUWD3	D006	G01
TWD29	01/085	12/42	CC12 42	CSUWD4	D006	H01
TWD30	01/090	12/39	CC12 39	CSUWD5	D005	H02
TWD31	01/086	12/40	CC12 40	CSUWD5	D006	H02
TWD32	01/096	18/47	CC18 47	CSUWD0	D007	F02
TWD33	01/092	18/48	CC18 48	CSUWD1	D007	F01
TWD34	01/101	18/45	CC18 45	CSUWD2	D007	G02
TWD35	01/097	18/46	CC18 46	CSUWD3	D007	G01
TWD36	01/102	18/41	CC18 41	CSUWD4	D007	H01
TWD37	01/098	18/32	CC18 42	CSUWD0	D008	F02
TWD38	01/107	18/39	CC18 39	CSUWD1	D008	F01
TWD39	01/103	18/40	CC18 40	CSUWD2	D008	G02
TWD40	01/119	20/47	CC20 47	CSUWD3	D008	G01
TWD41	01/115	20/48	CC20 48	CSUWD4	D008	H01
TWD42	01/125	20/45	CC20 45	CSUWD0	D009	F02
TWD43	01/121	20/46	CC20 46	CSUWD1	D009	F01
TWD44	01/131	20/41	CC20 41	CSUWD2	D009	G02
TWD45	01/127	20/42	CC20 42	CSUWD3	D009	G01
TWD46	01/137	20/39	CC20 39	CSUWD4	D009	H01
TWD47	01/133	20/40	CC20 40	CSUWD0	D010	F02
TWD48	01/145	22/47	CC22 47	CSUWD1	D010	F01
TWD49	01/155	22/48	CC22 48	CSUWD2	D010	G02
TWD50	01/151	22/45	CC22 45	CSUWD3	D010	G01
TWD51	01/161	22/46	CC22 46	CSUWD4	D010	H01
TWD52	01/157	22/41	CC22 41	CSUWD0	D011	F02
TWD53	01/167	22/42	CC22 42	CSUWD1	D011	F01
TWD54	01/163	22/39	CC22 39	CSUWD2	D011	G02
TWD55	01/173	22/40	CC22 40	CSUWD3	D011	G01
TWD56	01/175	24/47	CC24 47	CSUWD4	D012	H01
TWD57	01/185	24/48	CC24 48	CSUWD0	D012	F02
TWD58	01/181	24/45	CC24 45	CSUWD1	D012	F01
TWD59	01/191	24/46	CC24 46	CSUWD2	D012	G02
TWD60	01/187	24/41	CC24 41	CSUWD3	D012	G01
TWD61	03/005	24/42	CC24 42	CSUWD4	D012	H01
TWD62	03/001	24/39	CC24 39	CSUWD5	D011	H02
TWD63	03/011	24/40	CC24 40	CSUWD5	D012	H02
TDPAR64	01/047	06/37	CC06 37	CSUWD6	D001	J01
TDPAR65	01/065	08/37	CC08 37	CSUWD6	D002	J01
TDPAR66	01/078	10/37	CC10 37	CSUWD6	D003	J01
TDPAR67	01/095	12/37	CC12 37	CSUWD6	D004	J01
TDPAR68	01/109	18/37	CC18 37	CSUWD6	D007	J01
TDPAR69	01/139	20/37	CC20 37	CSUWD6	D008	J01
TDPAR70	01/169	22/37	CC22 37	CSUWD6	D009	J01
TDPAR71	03/007	24/37	CC24 37	CSUWD6	D010	J01

NAME IN CMC	CMCB (ROW M) COL/PIN	EXT CONNECTOR SIB A CONN/PIN	CSU CONT BD CONN/PIN	NAME CHIP	CHIP	PIN
READ DATA						
RDDAT0	03/042	06/11	CC06 11	CSURD0	D001	B11
RDDAT1	03/038	06/12	CC06 12	CSURD1	D001	B10
RDDAT2	03/047	06/09	CC06 09	CSURD2	D001	H12
RDDAT3	03/048	06/10	CC06 10	CSURD3	D001	R13
RDDAT4	03/053	06/05	CC06 05	CSURD4	D001	P11
RDDAT5	03/049	06/06	CC06 06	CSURD0	D002	B11
RDDAT6	03/054	06/03	CC06 03	CSURD1	D002	B10
RDDAT7	03/050	06/04	CC06 04	CSURD2	D002	H12
RDDAT8	03/059	08/11	CC08 11	CSURD3	D002	R13
RDDAT9	03/055	08/12	CC08 12	CSURD4	D002	P11
RDDAT10	03/060	08/09	CC08 09	CSURD0	D003	B11
RDDAT11	03/056	08/10	CC08 10	CSURD1	D003	B10
RDDAT12	03/065	08/05	CC08 05	CSURD2	D003	H12
RDDAT13	03/061	08/06	CC08 06	CSURD3	D003	R13
RDDAT14	03/066	08/03	CC08 03	CSURD4	D003	P11
RDDAT15	03/062	08/04	CC08 04	CSURD0	D004	B11
RDDAT16	03/071	10/11	CC10 11	CSURD1	D004	B10
RDDAT17	03/067	10/12	CC10 12	CSURD2	D004	H12
RDDAT18	03/072	10/09	CC10 09	CSURD3	D004	R13
RDDAT19	03/068	10/10	CC10 10	CSURD4	D004	P11
RDDAT20	03/077	10/05	CC10 05	CSURD0	D005	B11
RDDAT21	03/073	10/06	CC10 06	CSURD1	D005	B10
RDDAT22	03/078	10/03	CC10 03	CSURD2	D005	H12
RDDAT23	03/074	10/04	CC10 04	CSURD3	D005	R13
RDDAT24	03/083	12/11	CC12 11	CSURD4	D005	P11
RDDAT25	03/079	12/12	CC12 12	CSURD0	D006	B11
RDDAT26	03/084	12/09	CC12 09	CSURD1	D006	B10
RDDAT27	03/080	12/10	CC12 10	CSURD2	D006	H12
RDDAT28	03/089	12/05	CC12 05	CSURD3	D006	R13
RDDAT29	03/085	12/06	CC12 06	CSURD4	D006	P11
RDDAT30	03/090	12/03	CC12 03	CSURD5	D005	R12
RDDAT31	03/086	12/04	CC12 04	CSURD5	D006	R12
RDDAT32	03/101	18/11	CC18 11	CSURD0	D007	B11
RDDAT33	03/097	18/12	CC18 12	CSURD1	D007	B10
RDDAT34	03/102	18/09	CC18 09	CSURD2	D007	H12
RDDAT35	03/098	18/10	CC18 10	CSURD3	D007	R13
RDDAT36	03/107	18/05	CC18 05	CSURD4	D007	P11
RDDAT37	03/103	18/06	CC18 06	CSURD0	D008	B11
RDDAT38	03/108	18/03	CC18 03	CSURD1	D008	B10
RDDAT39	03/104	18/04	CC18 04	CSURD2	D008	H12
RDDAT40	03/113	20/11	CC20 11	CSURD3	D008	R13
RDDAT41	03/109	20/12	CC20 12	CSURD4	D008	P11
RDDAT42	03/114	20/09	CC20 09	CSURD0	D009	B11
RDDAT43	03/110	20/10	CC20 10	CSURD1	D009	B10
RDDAT44	03/119	20/05	CC20 05	CSURD2	D009	H12
RDDAT45	03/115	20/06	CC20 06	CSURD3	D009	R13
RDDAT46	03/120	20/03	CC20 03	CSURD4	D009	P11
RDDAT47	03/116	20/04	CC20 04	CSURD0	D010	B11
RDDAT48	03/125	22/11	CC22 11	CSURD1	D010	B10
RDDAT49	03/121	22/12	CC22 12	CSURD2	D010	H12
RDDAT50	03/126	22/09	CC22 09	CSURD3	D010	R13
RDDAT51	03/122	22/10	CC22 10	CSURD4	D010	P11
RDDAT52	03/131	22/05	CC22 05	CSURD0	D011	B11
RDDAT53	03/127	22/06	CC22 06	CSURD1	D011	B10
RDDAT54	03/132	22/03	CC22 03	CSURD2	D011	H12
RDDAT55	03/128	22/04	CC22 04	CSURD3	D011	R13
RDDAT56	03/137	24/11	CC24 11	CSURD4	D011	P11
RDDAT57	03/133	24/12	CC24 12	CSURD0	D012	B11
RDDAT58	03/138	24/09	CC24 09	CSURD1	D012	B10
RDDAT59	03/134	24/10	CC24 10	CSURD2	D012	H12
RDDAT60	03/143	24/05	CC24 05	CSURD3	D012	R13
RDDAT61	03/139	24/06	CC24 06	CSURD4	D012	P11
RDDAT62	03/144	24/03	CC24 03	CSURD5	D011	R12
RDDAT63	03/140	24/04	CC24 04	CSURD5	D012	R12
RDDAT64	03/095	06/01	CC06 01	CSURD5	D001	R12
RDDAT65	03/091	08/01	CC08 01	CSURD5	D002	R12
RDDAT66	03/096	10/01	CC10 01	CSURD5	D003	R12
RDDAT67	03/092	12/01	CC12 01	CSURD5	D004	R12
RDDAT68	03/145	18/01	CC18 01	CSURD5	D007	R12
RDDAT69	03/146	20/01	CC20 01	CSURD5	D008	R12
RDDAT70	03/156	22/01	CC22 01	CSURD5	D009	R12
RDDAT71	03/152	24/01	CC24 01	CSURD5	D010	R12

NAME IN CMC	CMCB (ROW M) COL/PIN	EXT CONNECTOR SIB A CONN/PIN	CSU CONT BD CONN/PIN	NAME CHIP	CHIP	PIN
SERIAL READ DATA						
TCMWD0	01/005	06/23	CC06 23	CSUPRD0	D001	P06
TCMWD1	01/001	06/24	CC06 24	CSUPRD1	D001	P05
TCMWD2	01/006	06/21	CC06 21	CSUPRD2	D001	R03
TCMWD3	01/002	06/22	CC06 22	CSUPRD3	D001	B05
TCMWD4	01/011	06/17	CC06 17	CSUPRD4	D001	A03
TCMWD5	01/007	06/18	CC06 18	CSUPRD0	D002	P06
TCMWD6	01/012	06/15	CC06 15	CSUPRD1	D002	P05
TCMWD7	01/008	06/16	CC06 16	CSUPRD2	D002	R03
TCMWD8	01/017	08/23	CC08 23	CSUPRD3	D002	B05
TCMWD9	01/013	08/24	CC08 24	CSUPRD4	D002	A03
TCMWD10	01/018	08/21	CC08 21	CSUPRD0	D003	P06
TCMWD11	01/014	08/22	CC08 22	CSUPRD1	D003	P05
TCMWD12	01/023	08/17	CC08 17	CSUPRD2	D003	R03
TCMWD13	01/019	08/18	CC08 18	CSUPRD3	D003	B05
TCMWD14	01/024	08/15	CC08 15	CSUPRD4	D003	A03
TCMWD15	01/020	08/16	CC08 16	CSUPRD0	D004	P06
TCMWD16	01/029	10/23	CC10 23	CSUPRD1	D004	P05
TCMWD17	01/025	10/24	CC10 24	CSUPRD2	D004	R03
TCMWD18	01/030	10/21	CC10 21	CSUPRD3	D004	B05
TCMWD19	01/026	10/22	CC10 22	CSUPRD4	D004	A03
TCMWD20	01/035	10/17	CC10 17	CSUPRD0	D005	P06
TCMWD21	01/031	10/18	CC10 18	CSUPRD1	D005	P05
TCMWD22	01/036	10/15	CC10 15	CSUPRD2	D005	R03
TCMWD23	01/032	10/16	CC10 16	CSUPRD3	D005	B05
TCMWD24	01/041	12/23	CC12 23	CSUPRD4	D005	A03
TCMWD25	01/037	12/24	CC12 24	CSUPRD0	D006	P06
TCMWD26	01/042	12/21	CC12 21	CSUPRD1	D006	P05
TCMWD27	01/038	12/22	CC12 22	CSUPRD2	D006	R03
TCMWD28	01/047	12/17	CC12 17	CSUPRD3	D006	B05
TCMWD29	01/048	12/18	CC12 18	CSUPRD4	D006	A03
TCMWD30	01/053	12/15	CC12 15	CSUPRD5	D005	B04
TCMWD31	01/149	12/16	CC12 16	CSUPRD5	D006	B04
TCMWD32	01/179	18/23	CC18 23	CSUPRD0	D007	P06
TCMWD33	01/175	18/24	CC18 24	CSUPRD1	D007	P05
TCMWD34	01/180	18/21	CC18 21	CSUPRD2	D007	R03
TCMWD35	01/176	18/22	CC18 22	CSUPRD3	D007	B05
TCMWD36	01/185	18/17	CC18 17	CSUPRD4	D007	A03
TCMWD37	01/181	18/18	CC18 18	CSUPRD0	D008	P06
TCMWD38	01/186	18/15	CC18 15	CSUPRD1	D008	P05
TCMWD39	01/182	18/16	CC18 16	CSUPRD2	D008	R03
TCMWD40	01/191	20/23	CC20 23	CSUPRD3	D008	B05
TCMWD41	01/187	20/24	CC20 24	CSUPRD4	D008	A03
TCMWD42	03/005	20/21	CC20 21	CSUPRD0	D009	P06
TCMWD43	03/001	20/22	CC20 22	CSUPRD1	D009	P05
TCMWD44	03/006	20/17	CC20 17	CSUPRD2	D009	R03
TCMWD45	03/002	20/18	CC20 18	CSUPRD3	D009	B05
TCMWD46	03/011	20/15	CC20 15	CSUPRD4	D009	A03
TCMWD47	03/007	20/16	CC20 16	CSUPRD0	D010	P06
TCMWD48	03/012	22/23	CC22 23	CSUPRD1	D010	P05
TCMWD49	03/008	22/24	CC22 24	CSUPRD2	D010	R03
TCMWD50	03/017	22/21	CC22 21	CSUPRD3	D010	B05
TCMWD51	03/013	22/22	CC22 22	CSUPRD4	D010	A03
TCMWD52	03/018	22/17	CC22 17	CSUPRD0	D011	P06
TCMWD53	03/014	22/18	CC22 18	CSUPRD1	D011	P05
TCMWD54	03/023	22/15	CC22 15	CSUPRD2	D011	R03
TCMWD55	03/019	22/16	CC22 16	CSUPRD3	D011	B05
TCMWD56	03/024	24/23	CC24 23	CSUPRD4	D011	A03
TCMWD57	03/020	24/24	CC24 24	CSUPRD0	D012	P06
TCMWD58	03/029	24/21	CC24 21	CSUPRD1	D012	P05
TCMWD59	03/025	24/22	CC24 22	CSUPRD2	D012	R03
TCMWD60	03/030	24/17	CC24 17	CSUPRD3	D012	B05
TCMWD61	03/026	24/18	CC24 18	CSUPRD4	D012	A03
TCMWD62	03/035	24/15	CC24 15	CSUPRD5	D011	B04
TCMWD63	03/031	24/16	CC24 16	CSUPRD5	D012	B04
TCMWD64	01/054	06/13	CC06 13	CSUPRD5	D001	B04
TCMWD65	01/050	08/13	CC08 13	CSUPRD5	D002	B04
TCMWD66	01/059	10/13	CC10 13	CSUPRD5	D003	B04
TCMWD67	01/055	12/13	CC12 13	CSUPRD5	D004	B04
TCMWD68	03/036	18/13	CC18 13	CSUPRD5	D007	B04
TCMWD69	03/032	20/13	CC20 13	CSUPRD5	D008	B04
TCMWD70	03/041	22/13	CC22 13	CSUPRD5	D009	B04
TCMWD71	03/037	24/13	CC24 13	CSUPRD5	D010	B04

NAME IN CMC	CMCB (ROW M) COL/PIN	EXT CONNECTOR SIB A CONN/PIN	CSU CONT BD CONN/PIN	NAME CHIP	CHIP	PIN
PARTIAL WRITE DATA						
TPWD0	01/065	06/35	CC06 35	CSUPWD0	D001	D15
TPWD1	01/061	06/36	CC06 36	CSUPWD1	D001	E15
TPWD2	01/066	06/33	CC06 33	CSUPWD2	D001	F14
TPWD3	01/062	06/34	CC06 34	CSUPWD3	D001	G14
TPWD4	01/071	06/29	CC06 29	CSUPWD4	D001	F15
TPWD5	01/067	06/30	CC06 30	CSUPWD0	D002	D15
TPWD6	01/072	06/27	CC06 27	CSUPWD1	D002	E15
TPWD7	01/068	06/28	CC06 28	CSUPWD2	D002	F14
TPWD8	01/077	08/35	CC08 35	CSUPWD3	D002	G14
TPWD9	01/073	08/36	CC08 36	CSUPWD4	D002	F15
TPWD10	01/078	08/33	CC08 33	CSUPWD0	D003	D15
TPWD11	01/074	08/34	CC08 34	CSUPWD1	D003	E15
TPWD12	01/083	08/29	CC08 29	CSUPWD2	D003	F14
TPWD13	01/079	08/30	CC08 30	CSUPWD3	D003	G14
TPWD14	01/084	08/27	CC08 27	CSUPWD4	D003	F15
TPWD15	01/080	08/28	CC08 28	CSUPWD0	D004	D15
TPWD16	01/089	10/35	CC10 35	CSUPWD1	D004	E15
TPWD17	01/085	10/36	CC10 36	CSUPWD2	D004	F14
TPWD18	01/090	10/33	CC10 33	CSUPWD3	D004	G14
TPWD19	01/086	10/34	CC10 34	CSUPWD4	D004	F15
TPWD20	01/095	10/29	CC10 29	CSUPWD0	D005	D15
TPWD21	01/091	10/30	CC10 30	CSUPWD1	D005	E15
TPWD22	01/096	10/27	CC10 27	CSUPWD2	D005	F14
TPWD23	01/092	10/28	CC10 28	CSUPWD3	D005	G14
TPWD24	01/101	12/35	CC12 35	CSUPWD4	D005	F15
TPWD25	01/097	12/36	CC12 36	CSUPWD0	D006	D15
TPWD26	01/102	12/33	CC12 33	CSUPWD1	D006	E15
TPWD27	01/098	12/34	CC12 34	CSUPWD2	D006	F14
TPWD28	01/107	12/29	CC12 29	CSUPWD3	D006	G14
TPWD29	01/103	12/30	CC12 30	CSUPWD4	D006	F15
TPWD30	01/108	12/27	CC12 27	CSUPWD5	D005	G15
TPWD31	01/104	12/28	CC12 28	CSUPWD5	D006	G15
TPWD32	01/113	1835	CC18 35	CSUPWD0	D007	D15
TPWD33	01/109	18/36	CC18 36	CSUPWD1	D007	E15
TPWD34	01/114	18/33	CC18 33	CSUPWD2	D007	F14
TPWD35	01/110	18/34	CC18 34	CSUPWD3	D007	G14
TPWD36	01/119	18/29	CC18 29	CSUPWD4	D007	F15
TPWD37	01/115	18/30	CC18 30	CSUPWD0	D008	D15
TPWD38	01/120	18/27	CC18 27	CSUPWD1	D008	E15
TPWD39	01/116	18/28	CC18 28	CSUPWD2	D008	F14
TPWD40	01/125	20/35	CC20 35	CSUPWD3	D008	G14
TPWD41	01/121	20/36	CC20 36	CSUPWD4	D008	F15
TPWD42	01/126	20/33	CC20 33	CSUPWD0	D009	D15
TPWD43	01/122	20/34	CC20 34	CSUPWD1	D009	E15
TPWD44	01/131	20/29	CC20 29	CSUPWD2	D009	F14
TPWD45	01/127	20/30	CC20 30	CSUPWD3	D009	G14
TPWD46	01/132	20/27	CC20 27	CSUPWD4	D009	F15
TPWD47	01/128	20/28	CC20 28	CSUPWD0	D010	D15
TPWD48	01/137	22/35	CC22 35	CSUPWD1	D010	E15
TPWD49	01/133	22/36	CC22 36	CSUPWD2	D010	F14
TPWD50	01/138	22/33	CC22 33	CSUPWD3	D010	G14
TPWD51	01/134	22/34	CC22 34	CSUPWD4	D010	F15
TPWD52	01/143	22/29	CC22 29	CSUPWD0	D011	D15
TPWD53	01/139	22/30	CC22 30	CSUPWD1	D011	E15
TPWD54	01/144	22/27	CC22 27	CSUPWD2	D011	F14
TPWD55	01/140	22/28	CC22 28	CSUPWD3	D011	G14
TPWD56	01/145	24/35	CC24 35	CSUPWD4	D011	F15
TPWD57	01/146	24/36	CC24 36	CSUPWD0	D012	D15
TPWD58	01/155	24/33	CC24 33	CSUPWD1	D012	E15
TPWD59	01/151	24/34	CC24 34	CSUPWD2	D012	F14
TPWD60	01/156	24/29	CC24 29	CSUPWD3	D012	G14
TPWD61	01/152	24/30	CC24 30	CSUPWD4	D012	F15
TPWD62	01/161	24/27	CC24 27	CSUPWD5	D011	G15
TPWD63	01/157	24/28	CC24 28	CSUPWD5	D012	G15

** CABLE TABS **

NAME IN CMC	CMCA (ROW N) COL/PIN	EXT CONNECTOR SIB A CONN/PIN	CSU CONT BD CONN/PIN	NAME CHIP	CHIP	PIN
GO BANK						
GOBE 0	01/017	14/05	CC14 5	CMCGD B0	T001	V20
GOBE 1	01/013	14/06	CC14 6	CMCGD B1	T001	E18
GOBE 2	01/023	14/03	CC14 3	CMCGD B2	T001	U19
GOBE 3	01/019	14/04	CC14 4	CMCGD B3	T001	F18
GOBE 4	01/018	16/05	CC16 5	CMCGD B0	T002	V20
GOBE 5	01/014	16/06	CC16 6	CMCGD B1	T002	E18
GOBE 6	01/024	16/03	CC16 3	CMCGD B2	T002	U19
GOBE 7	01/020	16/04	CC16 4	CMCGD B3	T002	F18
CLEAR BANK						
CLRBP0	01/005	14/11	CC14 11	CMCCLR 0	T001	W14
CLRBP1	01/001	14/12	CC14 12	CMCCLR 1	T001	B14
CLRBP2	01/006	14/09	CC14 09	CMCCLR 2	T001	Y12
CLRBP3	01/002	14/10	CC14 10	CMCCLR 3	T001	A12
CLRBP4	01/011	16/11	CC16 11	CMCCLR 0	T002	W14
CLRBP5	01/007	16/12	CC16 12	CMCCLR 1	T002	B14
CLRBP6	01/012	16/09	CC16 09	CMCCLR 2	T002	Y12
CLRBP7	01/008	16/10	CC16 10	CMCCLR 3	T002	A12
PARTIAL WRITE DATA ECC	CMCB (ROW M)					
TPDECC 64	01/162	06/25	CC06 25	CSUPWD 5	D001	G15
TPDECC 65	01/158	08/25	CC08 25	CSUPWD 5	D002	G15
TPDECC 66	01/167	10/25	CC10 25	CSUPWD 5	D003	G15
TPDECC 67	01/163	12/25	CC12 25	CSUPWD 5	D004	G15
TPDECC 68	01/168	18/25	CC18 25	CSUPWD 5	D007	G15
TPDECC 69	01/164	20/25	CC20 25	CSUPWD 5	D008	G15
TPDECC 70	01/173	22/25	CC22 25	CSUPWD 5	D009	G15
TPDECC 71	01/169	24/25	CC24 25	CSUPWD 5	D010	G15
WRITE DATA ECC						
TDECC 64	01/026	06/50	CC06 50	CSUWD 5	D001	H2
TDECC 65	01/048	08/50	CC08 50	CSUWD 5	D002	H2
TDECC 66	01/061	10/50	CC10 50	CSUWD 5	D003	H2
TDECC 67	01/074	12/50	CC12 50	CSUWD 5	D004	H2
TDECC 68	01/091	18/50	CC18 50	CSUWD 5	D007	H2
TDECC 69	01/113	20/50	CC20 50	CSUWD 5	D008	H2
TDECC 70	01/143	22/50	CC22 50	CSUWD 5	D009	H2
TDECC 71	01/179	24/50	CC24 50	CSUWD 5	D010	H2

NAME IN CMC	BDP (ROW A) COL/PIN	EXT CONNECTOR SIB A CONN/PIN	CSU CONT BD CONN/PIN	NAME CHIP	CHIP	PIN
MAC DATA TO CSU						
POMDO0	01/002	02/47	CCO2 47	MACDIO	TOO2	J1
POMDO1	01/006	02/48	CCO2 48	MACDI1	TOO2	K3
POMDO2	01/008	02/45	CCO2 45	MACDI2	TOO2	H1
POMDO3	01/012	02/46	CCO2 46	MACDI3	TOO2	J2
POMDO4	01/014	02/41	CCO2 41	MACDI4	TOO2	G1
POMDO5	01/018	02/42	CCO2 42	MACDI5	TOO2	J3
POMDO6	01/020	02/39	CCO2 39	MACDI6	TOO2	F1
POMDO7	01/024	02/40	CCO2 40	MACDI7	TOO2	H2
POMDOP	01/026	02/35	CCO2 35	MACDI8	TOO2	H3
MAC ADDRESS TO CSU						
POMAO0	01/030	02/29	CCO2 24	MACAIO	TOO2	J2
POMAO1	01/032	02/30	CCO2 30	MACAI1	TOO2	P2
POMAO2	01/036	02/27	CCO2 27	MACAI2	TOO2	T1
POMAO3	01/038	02/28	CCO2 28	MACAI3	TOO2	N3
POMAO4	01/042	02/23	CCO2 23	MACAI4	TOO2	R2
POMAO5	01/044	02/24	CCO2 24	MACAI5	TOO2	R1
POMAO6	01/048	02/21	CCO2 21	MACAI6	TOO2	N2
POMAO7	01/050	02/22	CCO2 22	MACAI7	TOO2	P1
POMAOP	01/054	02/34	CCO2 34	MACAI8	TOO2	M3
MAC DATA OUT OF CSU	MD (ROW B)					
MDINO	01/001	04/47	CCO4 47	MACDO	TOO2	YO4
MDIN1	01/002	04/48	CCO4 48	MACD1	TOO2	VO8
MDIN2	01/005	04/45	CCO4 45	MACD2	TOO2	WO6
MDIN3	01/006	04/46	CCO4 46	MACD3	TOO2	YO5
MDIN4	01/007	04/41	CCO4 41	MACD4	TOO2	WO8
MDIN5	01/008	04/42	CCO4 42	MACD5	TOO2	YO6
MDIN6	01/011	04/39	CCO4 39	MACD6	TOO2	VO9
MDIN7	01/012	04/40	CCO4 40	MACD7	TOO2	YO7
MDINP	01/013	04/35	CCO4 35	MACD8	TOO2	YO8
MAC ADDRESS OUT OF CSU						
MADINO	01/014	04/29	CCO4 29	MACAO	TOO2	UO5
MADIN1	01/017	04/30	CCO4 30	MACA1	TOO2	YO2
MADIN2	01/018	04/27	CCO4 27	MACA2	TOO2	VO5
MADIN3	01/019	04/28	CCO4 28	MACA3	TOO2	WO4
MADIN4	01/020	04/23	CCO4 23	MACA4	TOO2	UO6
MADIN5	01/023	04/24	CCO4 24	MACA5	TOO2	VO6
MADIN6	01/024	04/21	CCO4 21	MACA6	TOO2	YO3
MADIN7	01/025	04/22	CCO4 22	MACA7	TOO2	VO7
MADINP	01/026	04/34	CCO4 34	MACA8	TOO2	WO5

NAME IN CMC	CMCA (ROW N) COL/PIN	EXT CONNECTOR SIB A CONN/PIN	CSU CONT BD CONN/PIN	NAME CHIP	CHIP	PIN
ADDRESS BITS						
ADRS1	03/097	14/21	CC14 21	CMCRMA1	AOO1	KO1
ADRS2	03/101	14/24	CC14 24	CMCRMA2	AOO1	JO1
ADRS3	03/091	14/23	CC14 23	CMCRMA3	AOO1	HO2
ADRS4	03/095	14/28	CC14 28	CMCRMA4	AOO1	HO1
ADRS5	03/085	14/27	CC14 27	CMCRMA5	AOO1	GO1
ADRS6	03/089	14/30	CC14 30	CMCRMA6	AOO1	GO2
ADRS7	03/079	14/29	CC14 29	CMCRMA7	AOO1	FO1
ADRS8	03/083	14/34	CC14 34	CMCRMA8	AOO1	L14
ADRS9	03/073	14/33	CC14 33	CMCRMA9	AOO1	L15
ADRS10	03/077	14/36	CC14 36	CMCRMA1	AOO1	G15
ADRS11	03/067	14/35	CC14 35	CMCRMA1	AOO1	F15
ADRS12	03/071	14/40	CC14 40	CMCRMA1	AOO1	G14
ADRS13	03/061	14/39	CC14 39	CMCRMA1	AOO1	F14
ADRS14	03/065	14/42	CC14 42	CMCRMA1	AOO1	E15
ADRS15	03/055	14/41	CC14 41	CMCRMA1	AOO1	D15
ADRS16	03/017	16/41	CC16 41	CMCRMA8	AOO2	L14
ADRS17	03/013	16/42	CC16 42	CMCRMA9	AOO2	L15
ADRS18	03/023	16/39	CC16 39	CMCRMA1	AOO2	G15
ADRS19	03/019	16/40	CC16 40	CMCRMA1	AOO2	F15
ADRS20	03/029	16/35	CC16 35	CMCRMA1	AOO2	G14
ADRS21	03/025	16/36	CC16 36	CMCRMA1	AOO2	F14
ADRS22	03/035	16/33	CC16 33	CMCRMA1	AOO2	E15
ADRS23	03/031	16/34	CC16 34	CMCRMA1	AOO2	D15
ADRS24	03/041	16/29	CC16 29	CMCRMA6	AOO2	GO2
ADRS25	03/037	16/30	CC16 30	CMCRMA7	AOO2	FO1
ADRS26	03/053	16/27	CC16 27	CMCRMA3	AOO2	HO2
ADRS27	03/049	16/28	CC16 28	CMCRMA4	AOO2	HO1
ADRS28	03/059	16/23	CC16 23	CMCRMA5	AOO2	GO1
ADRS32	03/113	14/17	CC14 17	CMCRMA6	AOO1	FO2
ADRS33	03/109	14/18	CC14 18	CMCRMA6	AOO1	F13
ADRS34	03/107	16/21	CC16 21	CMCRMA6	AOO2	F13
ADRS35	03/103	16/22	CC16 22	CMCRMA6	AOO2	FO2

	NAME IN CMC	CM C	ROW	COL/PIN	EXT CONNECTOR SIB A CONN/PIN	CSU CONT BD CONN/PIN	NAME CHIP	CHIP	PIN
CMCMC - MULTI BIT	MCLRC	B	M	01/181	14/16	CC14 16	FNOTI2	TOO1	F20
ERROR - CMC WRITE	MBEP	B	M	03/162	14/15	CC14 15	CMCMBE	TOO1	J20
ENABLE - CMC WRITE	CSUWTE	A	N	01/043	16/24	CC16 24	CMCWRTCNT	TOO1	H20
FUNCTION - 2ND PASS	CSUWT	A	N	01/025	16/16	CC16 16	CMCWRT	AOO2	EO1
FUNCTION -	PASS2	A	N	01/030	16/17	CC16 17	CMC2PASS	TOO1	K18
REFRESH -	RFRQ	A	N	01/029	16/15	CC16 15	CMCREFR	AOO1	LO1
LONG CYCLE -	LNGCY	B	M	03/158	16/18	CC16 18	CMCLNGCYC	TOO1	K20
	MPOIDS	MD	B	01/029	04/11	CCO4 11			
	MPOSHF	MD	B	01/030	04/12	CCO4 12			
	NCSU10	CSMC	G	01/023	02/13	CCO2 15	CLKNFO	AOO4	K14
	CSU10	CSMC	G	01/017	02/16	CCO2 16	CLKFO	AOO4	K15
	NCSU5	CSMC	G	01/011	02/15	CCO2 17	CLKNFO	AOO3	K14
	CSU5	CSMC	G	01/005	02/18	CCO2 18	CLKFO	AOO3	K15
	PFSB118					CCO4 9	MACPERR	TOO2	B09
	PFSB119					CCO4 5	MACPERR	TOO1	B09
	THERM11					CCO2 3	TS1	TOO1	M20
	THERMO1					CCO2 5	TSO	TOO1	M19
	THERM12					CCO2 4	TS1	TOO2	M20
	THERMO2					CCO2 6	TSO	TOO2	M19

J50 (R09)

Y/B		Bit
1/2	Write Data	27
3/4	Write Data	55
5/6	Address Bit	5
7/8	Write Data	15
9/10	Write Data	63
11/12	Address Bit	26
13/14	Address Bit	24
15/16	Write Data	47
17/18	Write Data	07
19/20	Address Bit	27
21/22	Write Data	39
23/24	Write Data	03
25/26	Address Bit	33

J51 (R05)

Y/B		Bit
1/2	Write Data	31
3/4	Write Data	23
5/6	Write Data	19
7/8	Write Data	11
9/10	Write Data	59
11/12	Write Data	70
13/14	Address Bit	25
15/16	Write Data	71
17/18	Write Data	43
19/20	Address Bit	28
21/22	Write Data	35
23/24	Write Data	51
25/26	Address Bit	23

J52 (P09)

Y/B		Bit
1/2	Write Data	26
3/4	Write Data	54
5/6	Address Bit	04
7/8	Write Data	14
9/10	Write Data	62
11/12	Address Bit	19
13/14	Address Bit	17
15/16	Write Data	46
17/18	Write Data	06
19/20	Address Bit	20
21/22	Write Data	38
23/24	Write Data	02
25/26	Address Bit	15

J53 (P05)

Y/B		Bit
1/2	Write Data	30
3/4	Write Data	22
5/6	Write Data	18
7/8	Write Data	10
9/10	Write Data	58
11/12	Write Data P	68
13/14	Address Bit	18
15/16	Write Data P	69
17/18	Write Data	42
19/20	Address Bit	21
21/22	Write Data	34
23/24	Write Data	50
25/26	Address Bit	16

J54 (R07)

Y/B		Bit
1/2	Write Data	25
3/4	Write Data	53
5/6	Address Bit	03
7/8	Write Data	13
9/10	Write Data	61
11/12	Address Bit	14
13/14	Address Bit	12
15/16	Write Data	45
17/18	Write Data	05
19/20	Function Bit	02
21/22	Write Data	37
23/24	Write Data	01
25/26	Address Bit	10

J55 (R03)

Y/B		Bit
1/2	Write Data	29
3/4	Write Data	21
5/6	Write Data	17
7/8	Write Data	09
9/10	Write Data	57
11/12	Write Data P	66
13/14	Address Bit	13
15/16	Write Data P	67
17/18	Write Data	41
19/20	Function Bit	03
21/22	Write Data	33
23/24	Write Data	49
25/26	Address Bit	11

J56 (P07)

Y-B		Bit
1/2	Write Data	24
3/4	Write Data	52
5/6	Address Bit	02
7/8	Write Data	12
9/10	Write Data	60
11/12	Address Bit	09
13/14	Address Bit	07
15/16	Write Data	44
17/18	Write Data	04
19/20	Function Bit	0
21/22	Write Data	36
23/24	Write Data	0
25/26	Function Par.	

J57 (P03)

Y/B		Bit
1/2	Write Data	28
3/4	Write Data	20
5/6	Write Data	16
7/8	Write Data	08
9/10	Write Data	56
11/12	Write Data P	64
13/14	Address Bit	08
15/16	Write Data P	65
17/18	Write Data	40
19/20	Function Bit	01
21/22	Write Data	32
23/24	Write Data	48
25/26	Address Bit	06

J58 (P02)

Y/B		Bit
1/2		
3/4	Half Clock	40/40 (F3)
5/6		
7/8		
9/10	Tag Out	P
11/12	Tag Out	6
13/14	Tag Out	5
15/16	Tag Out	3
17/18	Tag Out	2
19/20	Tag Out	1
21/22	Tag Out	0
23/24		
25/26		

IN/OUT FROM CMC

J59 (R02)

Y/B		Bit
1/2		
3/4	Full Clock	20/20
5/6		
7/8		
9/10	Tag Out	7
11/12	Busy	
13/14	Response Par.	
15/16	Tag Out	4
17/18	Response Bit	2
19/20	Response Bit	1
21/22	Response Bit	0
23/24	Response	
25/26		

J60 (P04)

Y/B		Bit
1/2		
3/4	Read Data	49
5/6	Read Data	51
7/8	Read Data P	71
9/10	Read Data	63
11/12	Read Data	62
13/14	Read Data	61
15/16	Read Data	60
17/18	Read Data P	70
19/20	Read Data	57
21/22	Mark Bit	6
23/24	Request	
25/26	Tag Bit In	3

J61 (R04)

Y/B		Bit
1/2		
3/4	Read Data	48
5/6	Read Data	50
7/8	Read Data	52
9/10	Read Data	53
11/12	Read Data	58
13/14	Read Data	56
15/16	Read Data	54
17/18	Read Data	59
19/20	Read Data	55
21/22	Mark Bit	7
23/24	Address P	B3
25/26	Tag Bit In	7

J62 (P06)

Y/B	Test Clock	Bit
1/2		
3/4	Read Data	33
5/6	Read Data	35
7/8	Read Data P	69
9/10	Read Data	47
11/12	Read Data	46
13/14	Read Data	45
15/16	Read Data	44
17/18	Read Data P	68
19/20	Read Data	41
21/22	Mark Bit	4
23/24	Tag Bit	P
25/26	Tag Bit In	2

J63 (R06)

Y/B		Bit
1/2		
3/4	Read Data	32
5/6	Read Data	34
7/8	Read Data	36
9/10	Read Data	37
11/12	Read Data	42
13/14	Read Data	40
15/16	Read Data	38
17/18	Read Data	43
19/20	Read Data	39
21/22	Mark Bit	5
23/24	Address P	B2
25/26	Tag Bit In	6

J64 (P08)

Y/B		Bit
1/2		
3/4	Read Data	17
5/6	Read Data	19
7/8	Read Data P	67
9/10	Read Data	31
11/12	Read Data	30
13/14	Read Data	29
15/16	Read Data	28
17/18	Read Data P	66
19/20	Read Data	25
21/22	Mark Bit	2
23/24	Address Bit	1
25/26	Tag Bit In	1

J65 (R08)

Y/B		Bit
1/2		
3/4	Read Data	16
5/6	Read Data	18
7/8	Read Data	20
9/10	Read Data	21
11/12	Read Data	26
13/14	Read Data	24
15/16	Read Data	22
17/18	Read Data	27
19/20	Read Data	23
21/22	Mark Bit	3
23/24	Address P	B1
25/26	Tag Bit In	5

J66 (P10)

Y/B		Bit
1/2		
3/4	Read Data	01
5/6	Read Data	03
7/8	Read Data P	65
9/10	Read Data	15
11/12	Read Data	14
13/14	Read Data	13
15/16	Read Data	12
17/18	Read Data P	64
19/20	Read Data	9
21/22	Mark Bit	0
23/24	Mark P	
25/26	Tag Bit In	0

J67 (R10)

Y/B		Bit
1/2		
3/4	Read Data	0
5/6	Read Data	02
7/8	Read Data	04
9/10	Read Data	05
11/12	Read Data	10
13/14	Read Data	08
15/16	Read Data	06
17/18	Read Data	11
19/20	Read Data	7
21/22	Mark Bit	1
23/24	Address P	B0
25/26	Tag Bit In	4

In/out to IOU

SIG	CABLE	I-4	W1	CSMC	NAME
JXINAI	J70 - 07/08	A23 - B030/A030	0107/0108	1020/1024	INACTIVE IN
JXXEII	J70 - 09/10	A23 - B031/A031	0109/0110	1026/1030	ERROR IN
JXSTII	J70 - 11/12	A23 - B032/A032	0111/0112	1032/1036	STATUS SUMMARY
JXEXJI	J70 - 13/14	A23 - B033/A033	0113/0114	1038/1042	EXCH. ACCEPT
JXRDYI	J70 - 15/16	A23 - B029/A029	0115/0116	1050/1054	READY IN
JROLJA	J70 - 19/20	A23 - B027/A027	0119/0120	1056/1060	ACTIVE OUT
JROLII	J70 - 21/22	A23 - B028/A028	0121/0122	1062/1066	INACTIVE OUT
JROLIF	J70 - 23/24	A23 - B025/A025	0123/0124	1068/1072	FUNCTION
JROL1R	J70 - 25/26	A23 - B026/A026	0125/0126	1074/1078	READY OUT

SIG	CABLE	I-4	W3	CSMC	NAME
JXR156	J71 - 01/02	A23 - B022/A022	0301/0302	1080/1084	DATA IN 0
JXR157	J71 - 03/04	A23 - B021/A021	0303/0304	1086/1090	DATA IN 1
JXR158	J71 - 05/06	A23 - B020/A020	0305/0306	1092/1096	DATA IN 2
JXR159	J71 - 07/08	A23 - B019/A019	0307/0308	1098/1102	DATA IN 3
JXR160	J71 - 09/10	A23 - B018/A018	0309/0310	1104/1108	DATA IN 4
JXR161	J71 - 11/12	A23 - B017/A017	0311/0312	1110/1114	DATA IN 5
JXR162	J71 - 13/14	A23 - B016/A016	0313/0314	1116/1120	DATA IN 6
JXR163	J71 - 15/16	A23 - B015/A015	0315/0316	1122/1126	DATA IN 7
JXR1P0	J71 - 17/18	A23 - B023/A023	0317/0318	1128/1132	PARITY IN

SIG	CABLE	I-4	W5	CSMC	NAME
JROL10	J72 - 01/02	A23 - B012/A012	0501/0502	1134/1138	MCH DATA OUT 0
JROL11	J72 - 03/04	A23 - B011/A011	0503/0504	1140/1144	MCH DATA OUT 1
JROL12	J72 - 05/06	A23 - B010/A010	0505/0506	1146/1150	MCH DATA OUT 2
JROL13	J72 - 07/08	A23 - B009/A009	0507/0508	1152/1156	MCH DATA OUT 3
JROL14	J72 - 09/10	A23 - B008/A008	0509/0510	1158/1162	MCH DATA OUT 4
JROL15	J72 - 11/12	A23 - B006/A006	0511/0512	1164/1168	MCH DATA OUT 5
JROL16	J72 - 13/14	A23 - B005/A005	0513/0514	1170/1174	MCH DATA OUT 6
JROL17	J72 - 15/16	A23 - B004/A004	0515/0516	1176/1180	MCH DATA OUT 7
JROL1P	J72 - 17/18	A23 - B013/A013	0517/0518	1182/1186	MCH DATA OUT P

I4 AT47B GROUND PLACEMENT LIST
(P/N 77612622)

ECO 46860

A02 - B011/C011
A02 - B049/C049
A02 - B050/C050
A02 - B051/C051
A02 - B052/C052
A02 - B053/C053
A02 - B055/C055
A02 - A068/D068
A02 - A069/D069
A02 - B069/C069
A02 - A071/D071
A02 - B074/C074
A02 - B075/C075
A02 - A099/D099
A02 - A101/D101
A02 - B101/C101
A02 - B102/C102
A02 - A120/D120
A02 - B120/C120
A02 - A128/D128

A03 - B011/C011
A03 - B049/C049
A03 - B050/C050
A03 - B051/C051
A03 - B052/C052
A03 - B053/C053
A03 - B055/C055
A03 - A068/D068
A03 - A069/D069
A03 - B069/C069
A03 - A071/D071
A03 - B074/C074
A03 - B075/C075
A03 - A099/D099
A03 - A101/D101
A03 - B101/C101
A03 - B102/C012
A03 - A120/D120
A03 - B120/C120
A03 - A128/D128

A04 - B011/C011
A04 - B049/C049
A04 - B050/C050
A04 - B051/C051
A04 - B052/C052
A04 - B053/C053
A04 - B055/C055
A04 - A068/D068
A04 - A069/D069
A04 - B069/C069
A04 - A071/D071
A04 - B074/C074
A04 - B075/C075
A04 - A099/D099
A04 - A101/D101
A04 - B101/C101
A04 - B102/C102
A04 - A120/D120
A04 - B120/C120
A04 - A128/D128

A05 - B011/C011
A05 - B049/C049
A05 - B050/C050
A05 - B051/C051
A05 - B052/C052
A05 - B053/C053
A05 - B055/C055
A05 - A068/D068
A05 - A069/D069
A05 - B069/C069
A05 - A071/D071
A05 - B074/C074
A05 - B075/C075
A05 - A099/D099
A05 - A101/D101
A05 - B101/C101
A05 - B102/C102
A05 - A120/D120
A05 - B120/C120
A05 - A128/D128

A06 - B046/C046
A06 - B053/C053
A06 - B061/C061
A06 - B069/C069
A06 - B070/C070
A06 - A070/D070
A06 - A126/D126

A07 - B046/C046
A07 - B053/C053
A07 - B061/C061
A07 - B069/C069
A07 - B070/C070
A07 - A070/D070
A07 - A126/D126

A08 - A032/D032
A08 - B032/C032
A08 - A033/D033
A08 - B033/C033
A08 - A036/D036
A08 - B036/C036
A08 - B093/C093
A08 - B099/C099
A08 - B105/C105

CLOCK ENABLE & CMI TEST MODE

A02-B103
STAND ALONE GRNDS- JHII (O1A)

A02-B068	A04-B068
A02-A098	A04-A098
A03-B068	A05-B068
A03-A098	A05-A098

SN/GNDS FOR I-4 - REMOVED ENABLES "1" FOR SERIAL NUMBER

A22-B038 - 48	A22-A038 - 56
A22-A036 - 49	A22-B036 - 57
A22-B042 - 50	A22-A042 - 58
A22-B041 - 51	A22-A040 - 59
A22-A050 - 52	A22-B051 - 60
A22-B047 - 53	A22-A046 - 61
A22-B043 - 54	A22-A041 - 62
A22-A039 - 55	A22-B40 - 63

(PN 77612622)

CIO/ISI CHANNEL CABLE CONNECTIONS

CABLE P/N 53577060

CHANNEL #	PORT	JACK #	BACKPANEL	LOCATION
CHAN 0	PORT A	J5	D09	A/B 09
	PORT B	J2	D09	A/B 92
CHAN 1	PORT A	J6	D12	A/B 09
	PORT B	J3	D12	A/B 92
CHAN 2	PORT A	J10	D15	A/B 09
	PORT B	J7	D15	A/B 92
CHAN 3	PORT A	J11	D18	A/B 09
	PORT B	J08	D18	A/B 92
CHAN 4	PORT A	J12	D21	A/B 09
	PORT B	J09	D21	A/B 92
CHAN 5	PORT A	J16	C09	A/B 09
	PORT B	J13	C09	A/B 92
CHAN 6	PORT A	J17	C12	A/B 09
	PORT B	J14	C12	A/B 92
CHAN 7	PORT A	J18	C15	A/B 09
	PORT B	J15	C15	A/B 92
CHAN 10	PORT A	J23	C18	A/B 09
	PORT B	J20	C18	A/B 92
CHAN 11	PORT A	J24	C21	A/B 09
	PORT B	J21	C21	A/B 92

NOTE: Cable connects to backpanel with pin 1 up, white side on B row and black side on A row.

Signal Name		Port A	Port B		
Interface Control	[Bus Director]	A09/B09	A92/B92	1/2	49/50
Pause	[Bus Slave]	A10/B10	A93/B93	3/4	47/48
Sync In	[Bus Slave]	A11/B11	A94/B94	5/6	43/44
Select Active	[Bus Slave]	A12/B12	A95/B95	7/8	45/46
Sync Out	[Bus Master]	A13/B13	A96/B96	9/10	35/36
Command Sequence	[Bus Master]	A15/B15	A98/B98	13/14	41/42
Select Hold	[Bus Master]	A16/B16	A99/B99	15/16	37/38
Data Bus Parity Lower	[Bidirectional]	A17/B17	A100/B100	17/18	39/40
Data Bus Bit 0	[Bidirectional]	A18/B18	A101/B101	19/20	18/34
Data Bus Bit 1	[Bidirectional]	A19/B19	A102/B102	21/22	19/20
Data Bus Bit 2	[Bidirectional]	A20/B20	A103/B103	23/24	21/22
Data Bus Bit 3	[Bidirectional]	A21/B21	A104/B104	25/26	23/24
Data Bus Bit 4	[Bidirectional]	A22/B22	A105/B105	27/28	25/26
Data Bus Bit 5	[Bidirectional]	A23/B23	A106/B106	29/30	27/28
Data Bus Bit 6	[Bidirectional]	A25/B25	A108/B108	33/34	29/30
Data Bus Bit 7	[Bidirectional]	A26/B26	A109/B109	35/36	31/32
Data Bus Parity Upper	[Bidirectional]	A27/B27	A110/B110	37/38	17/33
Data Bus Bit 8	[Bidirectional]	A28/B28	A111/B111	39/40	15/16
Data Bus Bit 9	[Bidirectional]	A29/B29	A112/B112	41/42	13/14
Data Bus Bit 10	[Bidirectional]	A30/B30	A113/B113	43/44	11/12
Data Bus Bit 11	[Bidirectional]	A31/B31	A114/B114	45/46	9/10
Data Bus Bit 12	[Bidirectional]	A32/B32	A115/B115	47/48	7/8
Data Bus Bit 13	[Bidirectional]	A33/B33	A116/B116	49/50	5/6
Data Bus Bit 14	[Bidirectional]	A35/B35	A118/B118	53/54	3/4
Data Bus Bit 15 [MSB]	[Bidirectional]	A36/B36	A119/B119	55/56	1/2

ISI Connector Pin Assignment

I/O SWITCH BOX TO B23 (JK)

		SWITCH	PIN NO.	
B23 - A016	+ PORT 1 BAUD SEL A	S1-A	7	GREEN
B017	+ PORT 1 BAUD SEL B	S1-B	7	BLUE
B016	+ PORT 1 BAUD SEL C	S1-C	7	WHITE
B012	+ PORT 0 BAUD SEL A	S2-A	7	BROWN
A012	+ PORT 0 BAUD SEL B	S2-B	7	RED
A017	+ PORT 0 BAUD SEL C	S2-C	7	ORANGE
A031	- ENABLE DIAGNOSTIC	S3	2	WHITE/BLUE
C044	GND	S3	1	WHITE/YELLOW
B013	+ PORT 1 SEL B	S4	2	WHITE/BLACK
B004	+ PORT 1 SEL C	S4	3	WHITE/RED
A004	+ PORT 1 SEL D	S4	4	WHITE/GREEN
A005	+ PORT 0 SEL B	S5	2	YELLOW
B005	+ PORT 0 SEL C	S5	3	GRAY
A013	+ PORT 0 SEL D	S5	4	VIOLET
C117	GND	S4	COM.	BLACK
S4	C	S5	C	
S5	C	S2-C	C	
S2-C	C	S2-B	C	
S2-B	C	S2-A	C	
S2-A	C	S1-C	C	
S1-C	C	S1-B	C	
S1-B	C	S1-A	C	

TPM TERMINAL CABLES

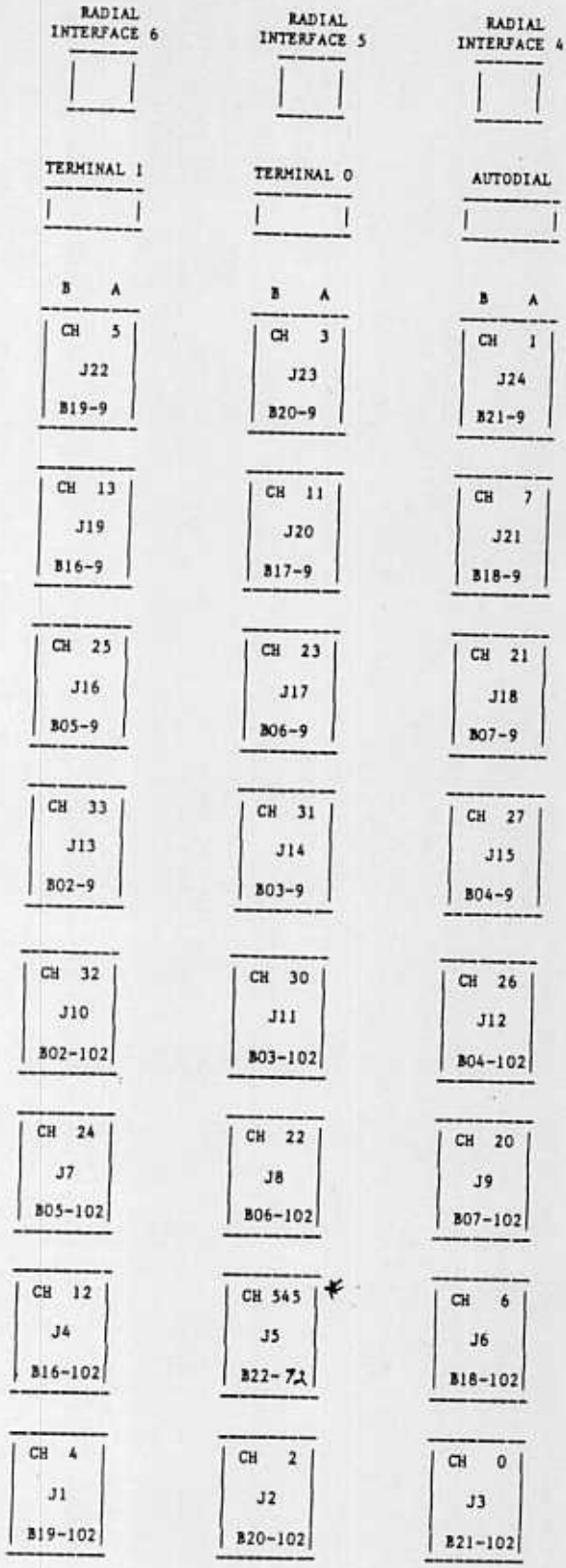
TERM. 0

J25-2	- DATA OUT	B23-A043
3	- DATA IN	B033
4	+ REQ TO SEND	B042
5	+ CLR TO SEND	B043
6	+ DATA SET READ	A041
7	GND	C054
8	+ CARRIER ON	A045
20	+ DATA TERM RDY	A042
22	+ RING INDICATOR	B041

TERM. 1

J26-2	- DATA OUT	B23-A039
3	- DATA IN	B028
4	+ REQ TO SEND	B038
5	+ CLR TO SEND	A028
6	+ DATA SET READY	B026
7	GND	D034
8	+ CARRIER ON	B027
20	+ DATA TERM RDY	A038
22	+ RING INDICATOR	A207

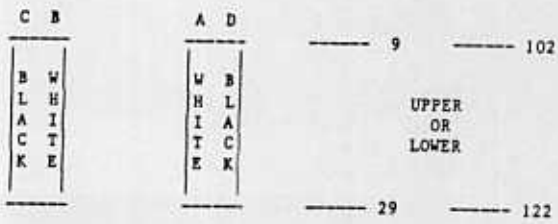
I-4 CHANNELS (REAR VIEW)

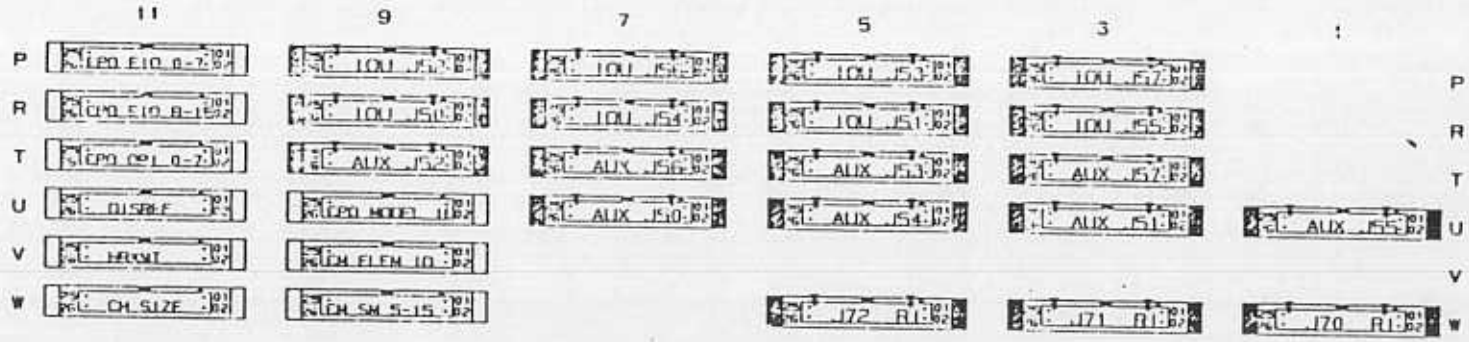


* J5 - P/N 53577044

ALL OTHER CHAN. CABLES P/N 19266534

I-4 BKPANEL



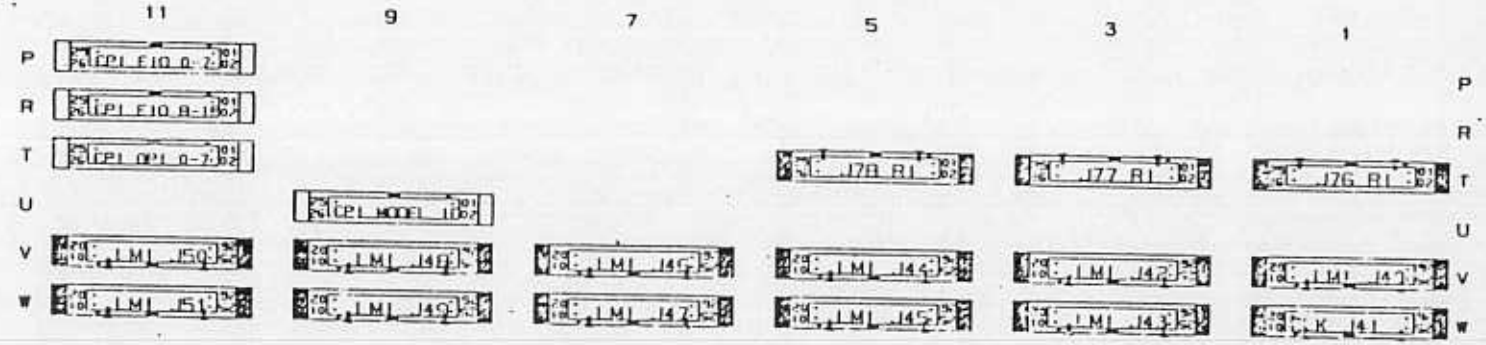


BOTTOM OF SIB A

VIEWED FROM THE PLUG IN SIDE OF SIB A HEADER

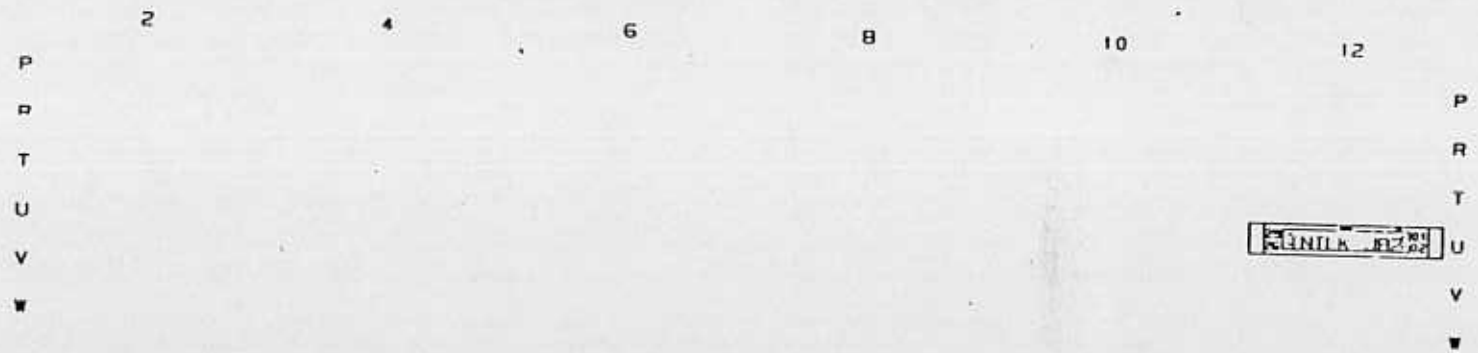
BOTTOM OF SIB B

VIEWED FROM THE PLUG IN SIDE OF SIB B HEADER



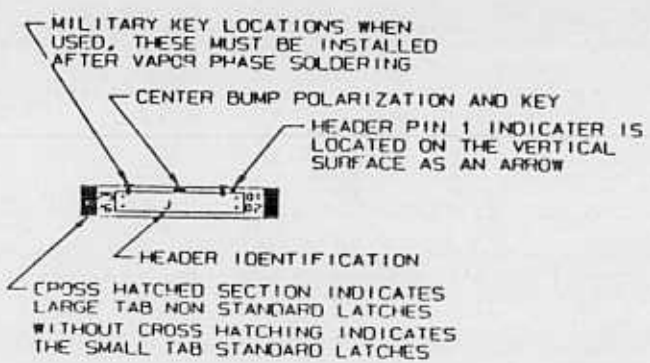
BOTTOM OF SIB C

↑ VIEWED FROM THE PLUG IN SIDE OF SIB C HEADER



BOTTOM OF SIB D

↑ VEIWED FROM THE PLUG IN SIDE OF SIB D HEADER



SIB D MAP