MAGNETIC PERIPHERALS INC.
a Control Data Company

ENGINEERING SPECIFICATION

SMALL DISK DIVISION

SPEC 64717900
CD 1
REV A
DATE 6/18/82
PAGE 1 of 60

1085A 5026S

PRODUCT SPECIFICATION

FOR THE

FIXED SMALL DISK DRIVE

(WITH SMD-0 INTERFACE)

9715-160

Approved 6-18-82

Released

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ILLUSTRATIONS

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1.0 SCOPE

This document describes the MAGNETIC PERIPHERALS INC. Fixed Small Disk (FSD) Drive and its available configurations.

2.0 APPLICABLE DOCUMENTS

DWG 93913853 - FSD Drive Mechanical Interface
PUBL 83324500 - Hardware Maintenance Manual Volume 1
PUBL 83324510 - Hardware Maintenance Manual Volume 2
PUBL 83322440 - Microcircuits Manual Volume 1
PUBL 83324440 - Microcircuits Manual Volume 2

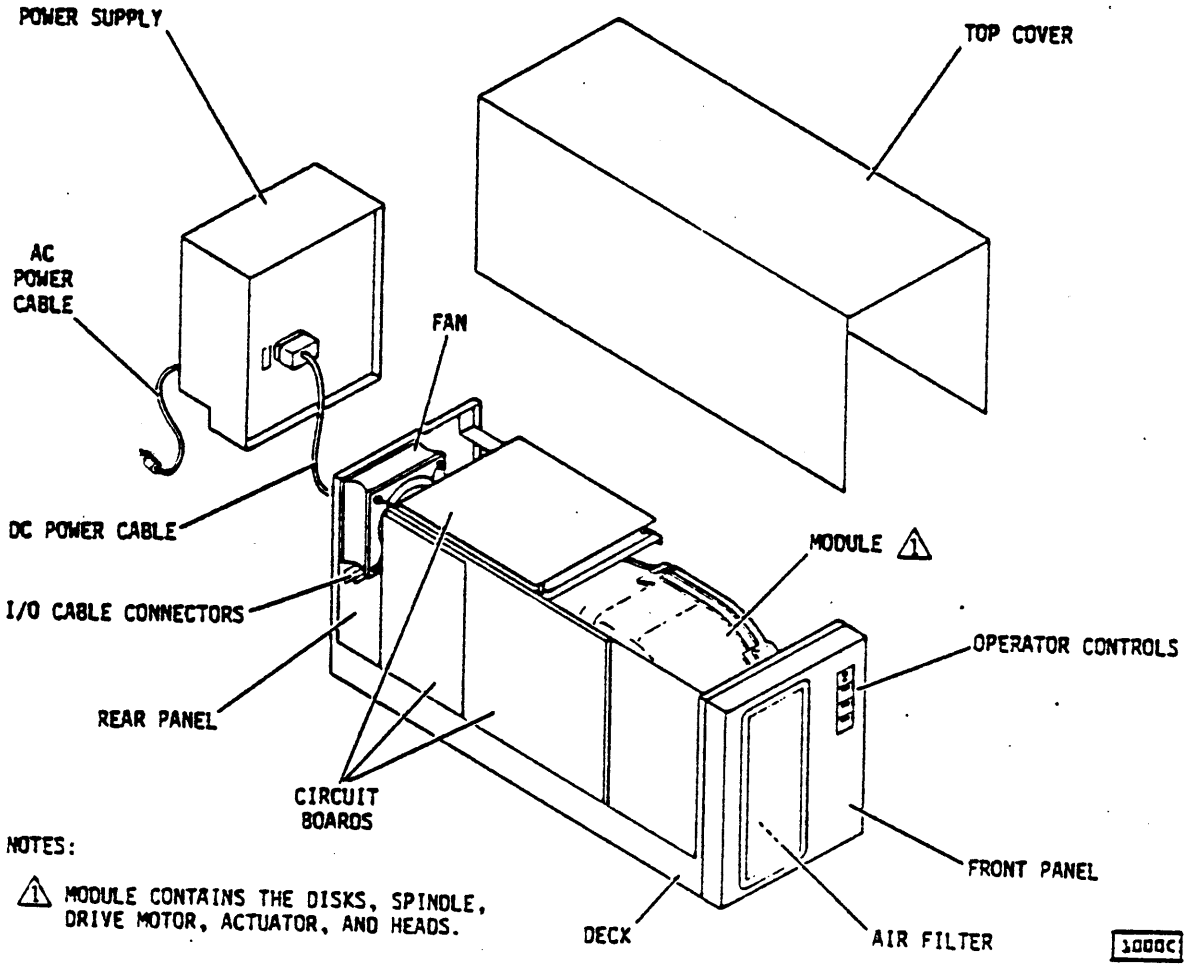
3.0 GENERAL DESCRIPTION

3.1 Equipment Definition

The FSD Drive is a 3600 rpm, 9.677 MHz data rate, random access, fixed-media flat cable disk drive consisting of a direct coupled dc brushless drive motor with digital speed control brake, detached switching type power supply, and a Disk Module incorporating Winchester type heads. The logic package utilizes both low power Schottky, I^2L and ECL technology and contains electonic printed circuit boards with extensive use of Large Scale Integration (LSI). All read/write, fault, transmitter/receiver and microprocessor controlled servo electronics are contained within this package. See Figure 1 for Major Component Placement and Figure 2 for the plan view.

The Module contains the disks, heads, rotary type actuator and air filters, all of which are sealed to minimize the effects of environmental contamination. See Figure 3 for Module Components and Air Flow.

Several features to enhance system integrity are included. They are phase-locked data separation, NRZ to 2, 7 RLL code data conversion, fixed and variable (Address Mark) sectoring and daisy-chain interface capability. The drive is designed to be rack mounted in either domestic or European enclosures.



NOTES:

1 MODULE CONTAINS THE DISKS, SPINDLE, DRIVE MOTOR, ACTUATOR, AND HEADS.

FIGURE 1. MAJOR COMPONENT PLACEMENT

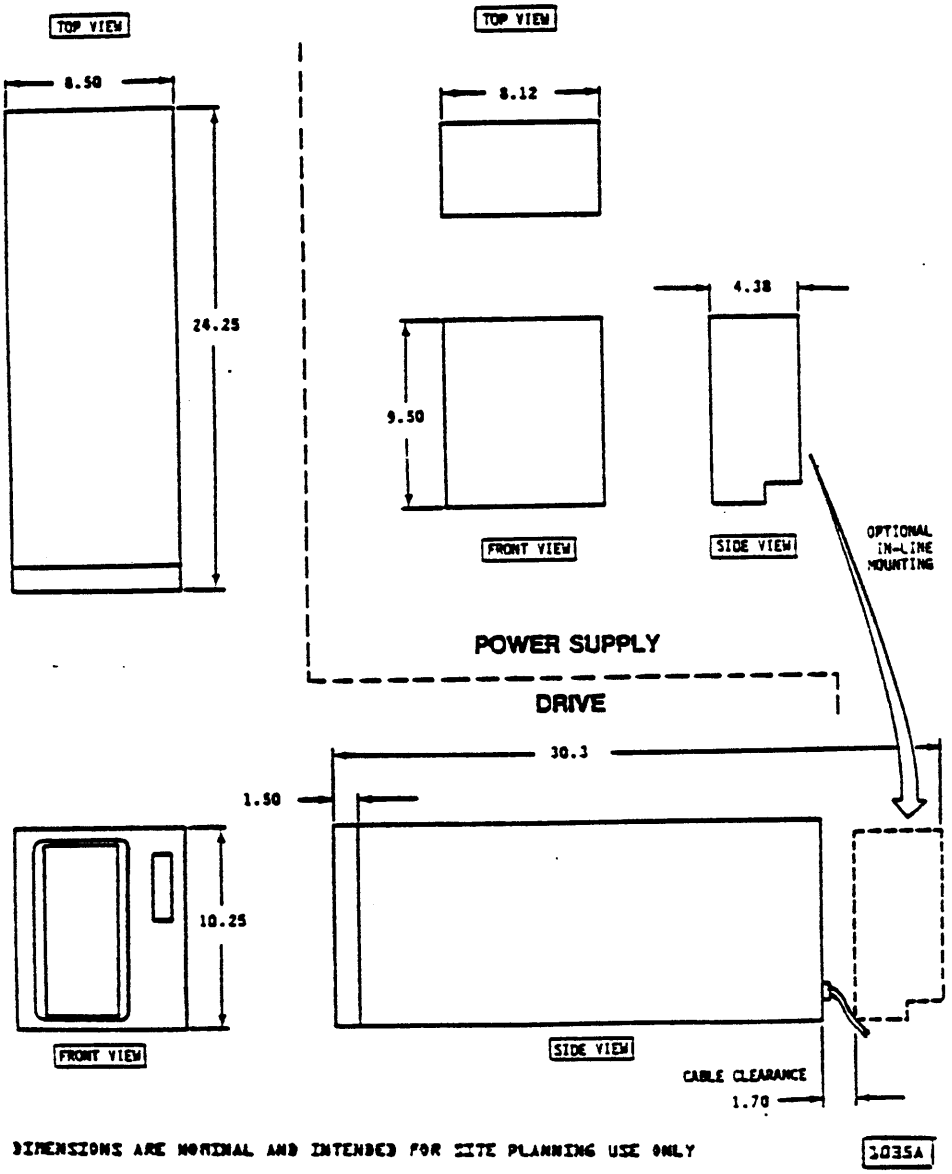


FIGURE 2. PLAN VIEW

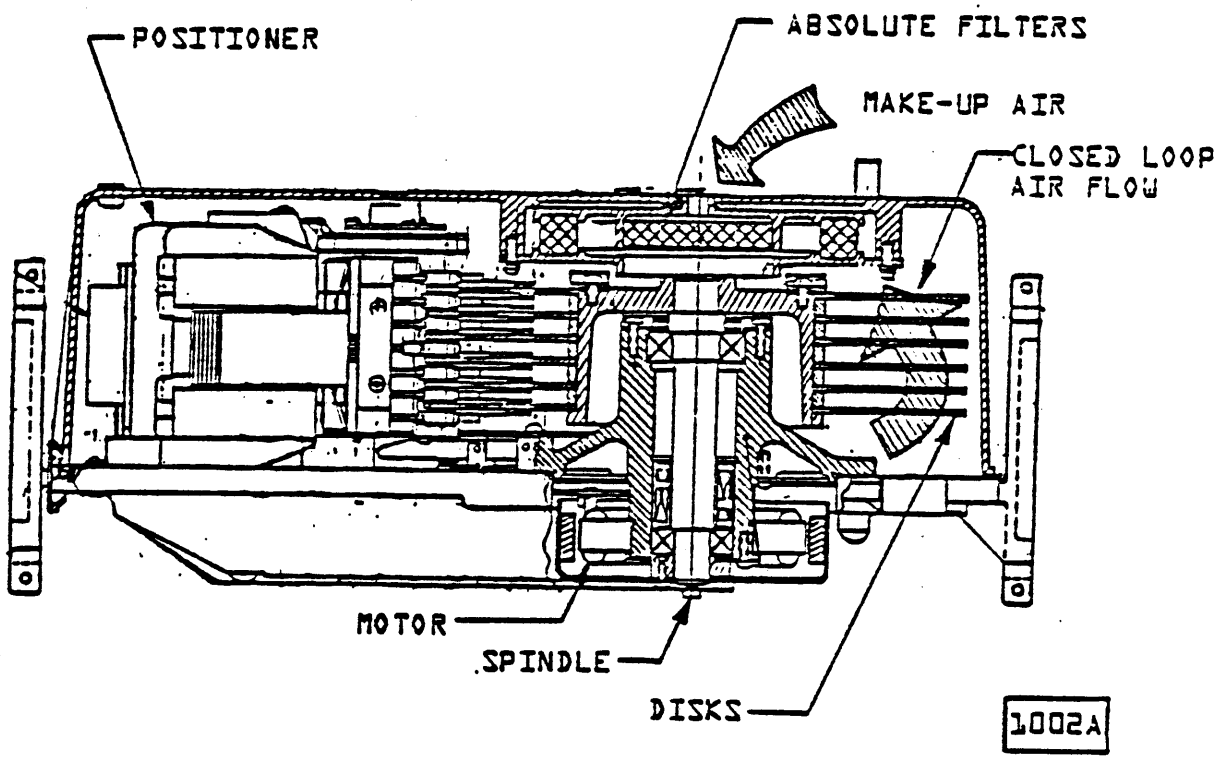


FIGURE 3. MODULAR COMPONENT PLACEMENT AND AIR FLOW

3.2 Options

3.2.1 Optional Power

The FSD Drive is available with a power supply which is switchable for the following ac voltage/frequency combinations:

120 V	50/60 Hz
220/240V	50/60 Hz

3.2.2 Index and Sector in "B" Cable Option

The drive can be modified to have index and sector in the "B" cable. This is accomplished by moving predesignated jumpers on the I/O card. See Figure 11.

3.2.3 Dual Channel Access Option

The Dual Channel option allows two controller access of the drive. This option is installable in either factory or field.

3.3 Accessory Items

Accessory items required but not included with the units must be purchased separately (see Table 1).

4.0 PERFORMANCE

4.1 Access-to-Data Characteristics

4.1.1 Positioning Times

All positioning times are measured from initiating a seek to the On Cylinder condition.

The maximum positioning time is 55 ms. This is defined as the time to move the head from track zero to track 822.

The maximum single track positioning time is 7 ms. This is defined as the time to move between any pair of adjacent tracks.

The average positioning time is no greater than 30 ms. This is defined as the time taken to make all possible moves divided by the number of all possible moves (see Figure 4).

TABLE 1. ACCESSORIES LIST

DESCRIPTION	QUANTITY REQUIRED	NOTE	PART NO
"A" Cable (Controller to drive) (Shielded)	One per drive in Star configuration one per Daisy-Chain configuration.	3, 4	925897XX
"A" Cable (drive to drive) (Shielded)	One less than total drive in the system	3, 4	925897XX
"B" Cable (Controller to drive) (Shielded)	One per drive	3	951936XX
Terminator Assembly	One per drive on Star, one per multi-spindle installation in Daisy Chain.	3	93270700
TB216-A Field Exerciser		2	82338800
Logic Plug	One per drive	1	94398817 thru 94398824
DC Power Supply Cable	One per drive	5	939918XX

NOTES:

1. Last two degits denote lens tab. Logic plugs 0 thru 3 - (tabs 17 thru 20) are provided with each FSD.
2. Quantity as required for regional maintenance.
3. In systems using the dual channel operation, twice the number of cables and terminators are required.
4. Last two digits denote cable length. (See Table 2 for I/O Cable Lengths)
5. Last two digits denote cable length. See Table 3 for cable length. Tab 02 (1 ft.) included with each drive.

TABLE 2. I/O CABLE LENGTHS AND TABS

CABLE LENGTH IN FEET	10	15	20	25	30	40	50	100
"A" CABLE TABS 925897XX	00	01	02	03	04	05	06	07
"B" CABLE TABS 951936XX	00	01	02	03	04	05	06	N/A

TABLE 3. DC POWER SUPPLY CABLE LENGTHS AND TABS

CABLE LENGTH IN FEET	5	8	1					
939918XX	00	01	02					

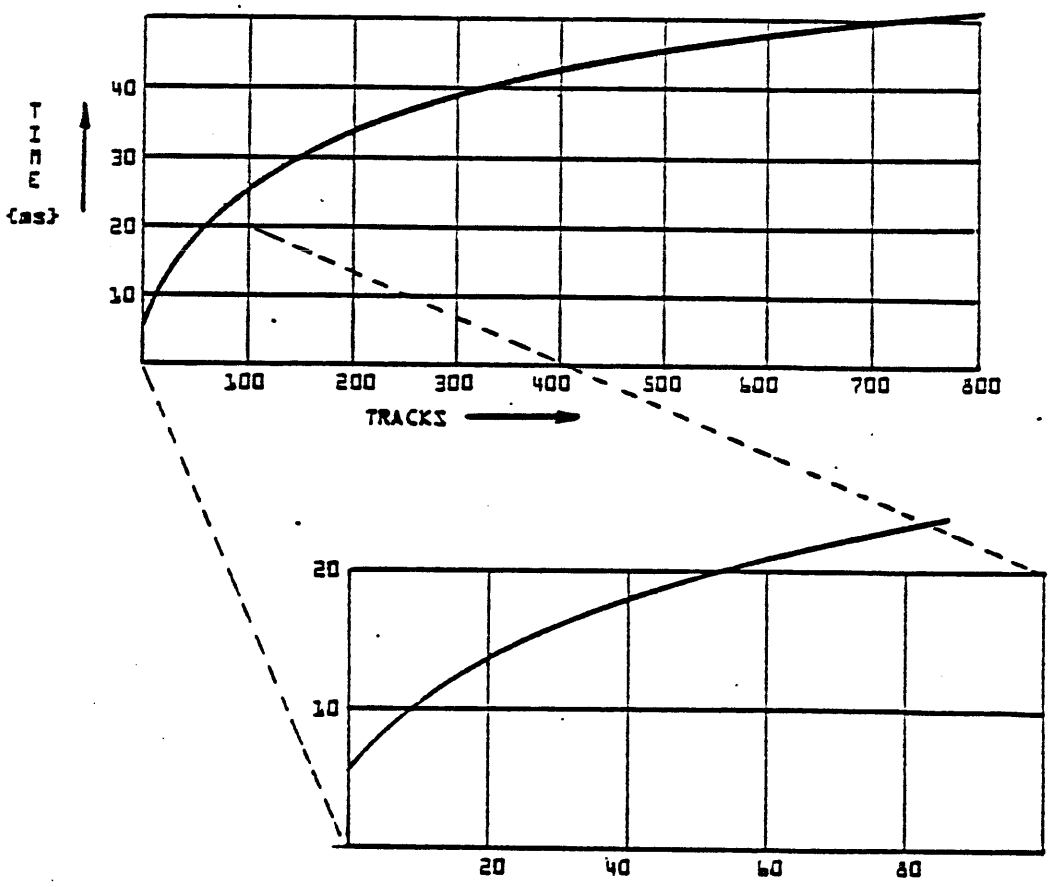


FIGURE 4. TYPICAL FSD DRIVE SEEK PROFILE

4.1.2 Latency Time

The average latency time is 8.33 ms, based on a nominal disk speed of 3600 rpm.

The maximum latency time is 16.83 ms, based on a minimum disk speed of 3564 rpm (see 5.4).

Latency time is defined as the time required to reach a particular track location after positioning is complete.

4.1.3 Read Initialization Time

Between the deselection of one head and the selection of another head, there is a 5.0 µs delay within the Drive due to circuit characteristics. The time from the initiation of a head change until data can be read with a selected head without error is 24.0 µs maximum (5.0 µs for head selection, 10.0 µs for read amplifier stabilization, and 9.0 µs for phase lock synchronization).

4.1.4 Write-to-Read Recovery Time

Assuming head selection is stabilized, the time lapse before Read Gate can be enabled after switching the Write Gate off is 10 µs, minimum. (See Figure 22(B)).

4.1.5 Read-to-Write Recovery Time

Assuming head selection is stabilized, the time lapse from dropping Read Gate to enabling Write Gate is 0.3 µs minimum (see Figure 22(B)).

4.2 Data Capacity

The data capacity specified is based on the number of eight-bit bytes that are recorded on a track. The unsectored capacity below does not include an allowance for tolerance gaps.

HEADS	10
BYTES/TRACK	20 160
BYTES/CYLINDER	201 600
BYTES/SPINDLE	165 916 800
CYLINDER/UNITS	823

4.3 Data Transfer Rate

The nominal bit rate is 9.677 MHz.

4.4 Error Rates

The following error rates assume that the Drive is being operated within its specification. Errors caused by media defects or equipment failures are excluded.

4.4.1 Read Errors

Prior to determination of a read error rate, the data will have been verified as written correctly and all media defects flagged.

1. Recoverable Error Rate = 1 in 10^{10}

   The recoverable error rate is the number of errors encountered which are recoverable within 27 retries (three retries at each data strobe and carriage offset) as a function of the number of bits transferred.

2. Unrecoverable Error Rate = 1 in 10^{12}

   An unrecoverable read error is one which cannot be read correctly within 27 retries (three retries at each combination of data strobe and carriage offset).

4.4.2 Write Errors

Write errors can occur as a result of the following: write data not being presented correctly, media defects, or equipment malfunction. As such, write errors are not predictable as a function of the number of bits passed.

For the case of an unrecoverable write error occurring because of a Drive equipment malfunction, the error is classified as a failure affecting MTBF.

Unrecoverable write errors are those which cannot be corrected within three attempts at writing the record with a read verify after each attempt.

4.4.3 Media Defects

A media defect is a physical characteristic of the media which results in a repetitive read error when a properly adjusted unit is operated within specific operating conditions. Valid data must not be written over known media defects; therefore, sector/track deallocation or skip displacement techniques must be utilized.

Media Defect Characteristics

1. The maximum number of defects for the FSD Drive is 250.

2. The maximum number of defective tracks per FSD Drive is 25.

A defective track is defined as a track having any of the following:

1. Two or more defects

2. False address marks

3. Any single defect which will cause read errors in more than one sector.

Media Defect Free Areas are defined as follows:

1. Cylinder 0, head 0 and 1

2. Any error in logging area to be extent defined in the rules 4.4.5.

4.4.4 Media Defect Logging Information

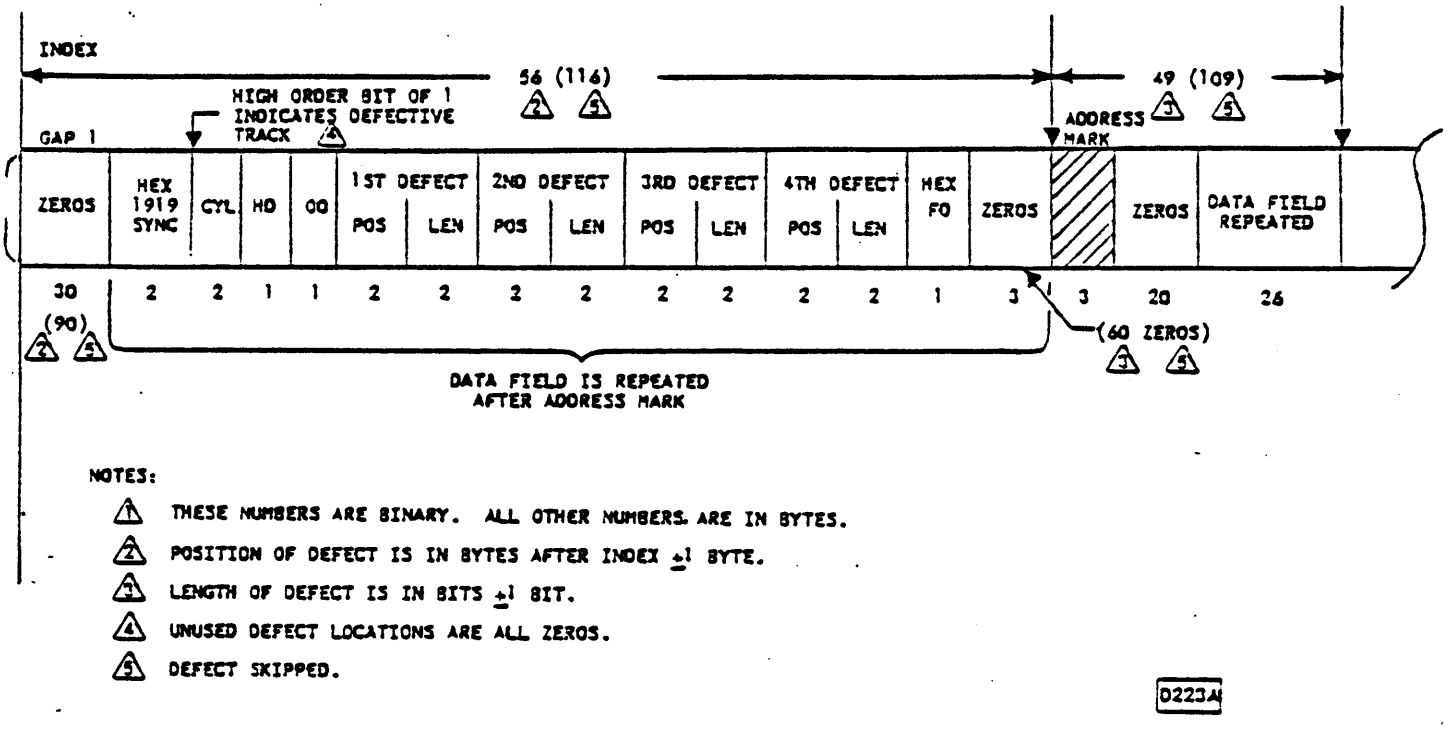
All drives will have a flaw map attached to each module which will list the following information:

1. Head
2. Cylinder
3. Location (bytes from Index)
4. Length (bits)

In addition, the drives will be formatted at the factory with standard external format (see 4.4.5 for format rules). This format is divided into 2 parts. The first part is a sectored format and is normally included in the first 56 bytes following Index. The second part is an address mark format and is normally included in the next 49 bytes following Index.

4.4.5 Format Rules (See Figure 5)

1. More than one defect on a track causes it to be flagged as a defective track (see Rule 4). The first four media flaws are logged.
2. If the beginning of a defect is located between 15 and 56 bytes after Index, 60 bytes of zeros are added to gap 1 (90 bytes total). In this case, if any part of a defect is between bytes 70 and 165, the track is flagged defective.
3. If the beginning of a defect is between 56 and 106 bytes after Index, 60 bytes of zeros are added immediately before the address mark. In this case, if any part of a defect is between bytes 116 and 155, the track is flagged defective.
4. If a defective track is established according to Rules 1, 2, or 3 above, the high order bit of the first cylinder bytes is set to 1. Remaining information may or may not be valid.
5. The media flaws for each track are encoded in a home address format.



NOTES:

1. THESE NUMBERS ARE BINARY. ALL OTHER NUMBERS ARE IN BYTES.
2. POSITION OF DEFECT IS IN BYTES AFTER INDEX ±1 BYTE.
3. LENGTH OF DEFECT IS IN BITS ±1 BIT.
4. UNUSED DEFECT LOCATIONS ARE ALL ZEROS.
5. DEFECT SKIPPED.

D223A

FIGURE 5. FSD STANDARD EXTERNAL FORMAT

4.4.6 Environmental Errors

When operating a low effective data transfer rate; e.g., random access of single short records, the effective error rate may be expected to exceed the above limits due to external environmental interference. The resulting recoverable read error rate is less than one error in eight hours of operation

4.4.7 Access Errors

There is no more than one positioning error in 10^6 seeks.

4.5 Data Security

Under normal controller I/O operation, the drive will write only that pattern present on the write data lines. Both drive Selected and On Cylinder must be true before a valid write operation can be completed. Data is protected by inhibiting Write Gate in all fault conditions including a loss of On Cylinder, Seek Error or low dc voltage. This is accomplished by switching off the voltage required to write and/or performing an emergency retract of the Read/Write heads.

4.6 Stop Time

The time to stop a disk after the START/STOP switch has been turned off is typically 6 s, 15 s maximum.

4.7 Start Time

The time for the Drive to be in the Ready state after the START/STOP switch has been depressed is typically 10 s, 30 s maximum.

5.0 RECORDING CHARACTERISTICS

5.1 Recording

Mode:	2,7 Code
Density (inner track):	9492 bpi nominal
(outer track):	6117 bpi nominal

5.2 Disk

Total number:	6
Servo surface:	1
Data surfaces:	10
Data tracks per surface:	823
Track spacing in inches:	.0018 nominal
Tracks per inch:	551 nominal

5.3 Heads

Servo head:	1
Recording heads:	10
Read/Write width in inches: (No erase gap)	.0014 nominal

5.4 Spindle

The spindle speed is 3600 ±36 rpm. These limits represent ±1% of nominal.

6.0 INTERFACE

6.1 Interface Definition

All input and output signals are digital, utilizing industry standard transmitters and receivers. When used with properly shielded cables, this provides a terminated, balanced, transmission system for long distances and/or noisy electrical environment. Figure 6 is a block diagram of the Drive interface.

The "A" cable is a 60 pin shielded, flat cable. The "B" cable is also shielded and allows mass termination without stripping. Shielding is utilized to minimize cross-talk and reduce inductive coupling due to static discharges, as well as control impedance variations regardless of cable lay.

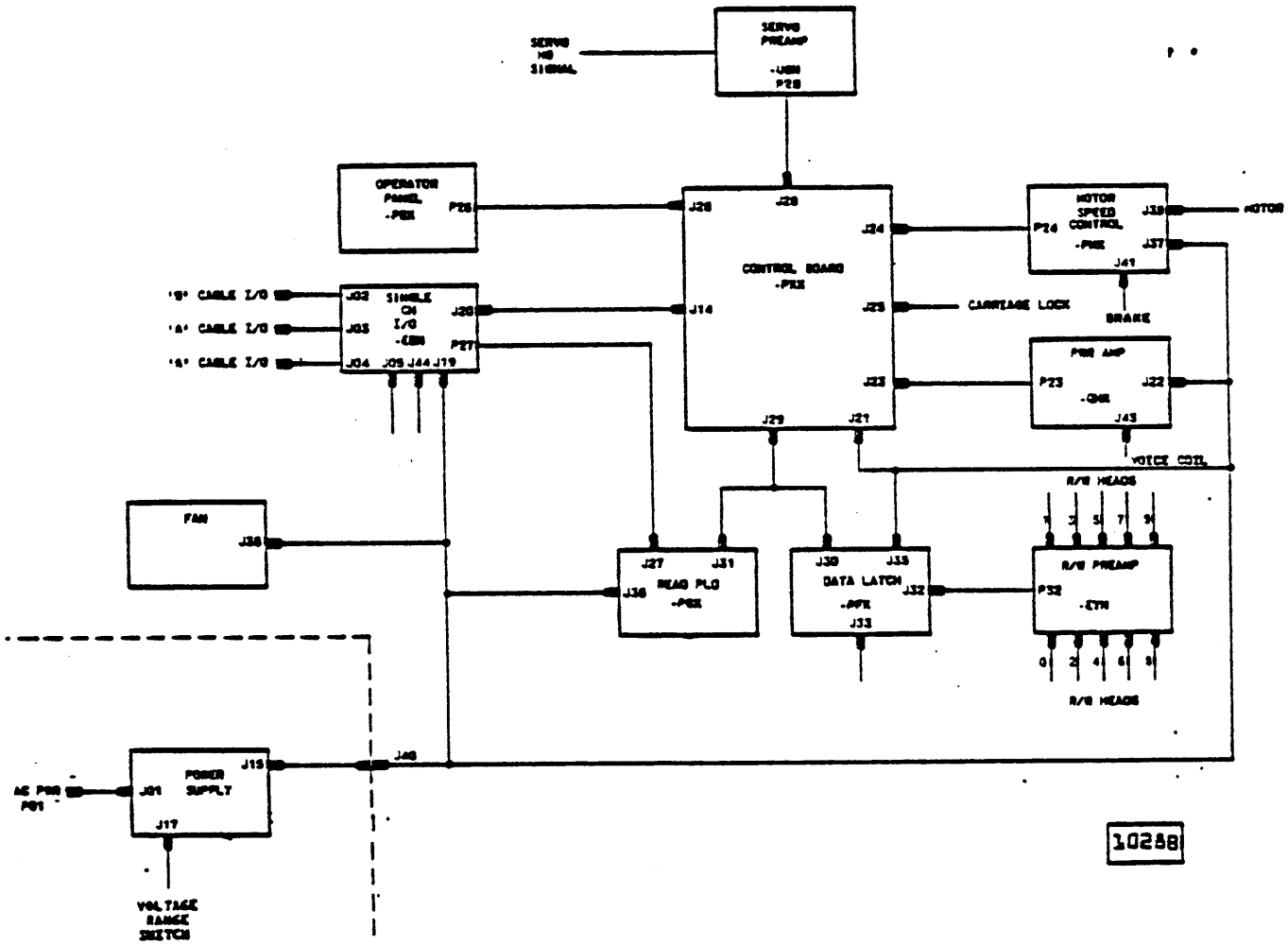


FIGURE 6. BLOCK DIAGRAM

6.1.1 Terminated, Balanced Transmission System

Transmitters and receivers of the industry standard type 75110A and MC 3450 or equivalent are used to provide a terminated, balanced transmission system (see Figure 7).

6.1.2 Line Transmitter Characteristics

The FSD Drive controller line transmitter (see Figure 8) is compatible with the CDC line receiver described in 6.1.3.

1. Output Signal Levels

"A" Cable Control Signals - See Figure 8.
"B" Cable Data Signals - See Figure 7.

2. Output Line Polarity

Control Signals - The CDC transmitter (see Figure 8) is connected to the I/O line such that the output, labeled Z, corresponds with the low order pin number of the pin assignments and in turn connect to receiver pin labeled B, except for the Unit Selected line, which is connected in the opposite manner.

When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver.

6.1.3 Input Amplifier (Receiver) Characteristics

The Drive controller input amplifier (see Figure 9) is compatible with the CDC transmitter described in 6.1.2.

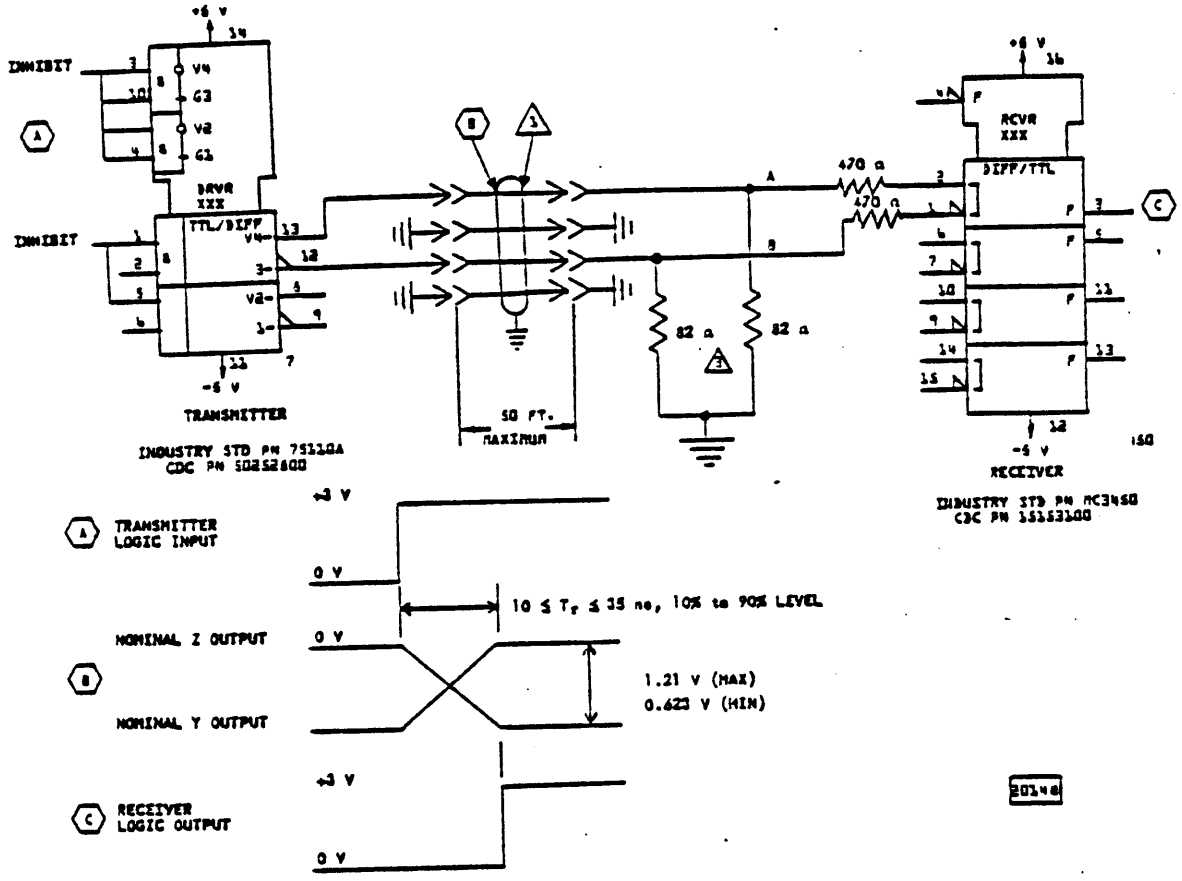
1. Receiver Propagation Delay

The receiver propagation delay is typically 19 ns in the direction of the logical 1, and 19 ns in the direction of the logical 0.

2. Receiver Input Polarity

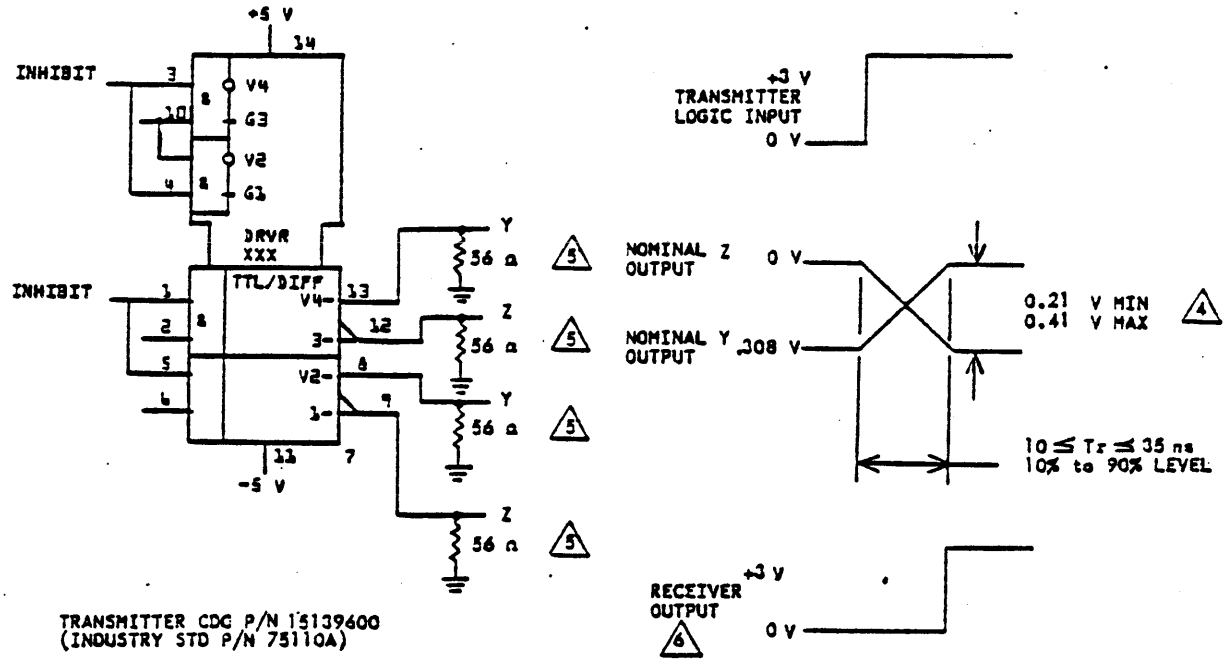
Control Signals - The input (labeled "B") of the receiver (see Figure 7) is connected to the lowest numbered pin of the pair in the cable and in turn connected to the transmitter pin labled Z.

"B" Cable Data Signals - See Figure 7.



1. CABLE IS FLAT CABLE WITH CHARACTERISTIC IMPEDANCE 130 ± 15 OHMS.
2. FOR LOGIC LEVELS AND TRUTH TABLE, REFER TO TRANSMITTER AND RECEIVER FIGURES.
3. TERMINATOR RESISTORS ARE LOCATED ON DRIVE LOGIC CARD OR IN CONTROLLER. THESE SIGNALS MUST BE STAR CABLED.

FIGURE 7. DATA TRANSMITTER AND RECEIVER



TRANSMITTER CDC P/N 75139600
(INDUSTRY STD P/N 75110A)

LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS*		OUTPUT CONDITION
1, 5	2, 6	3, 4	10	9, 12	8, 13	
1 OR 0 1 OR 0	1 OR 0 1 OR 0	0 1 OR 0	1 OR 0 0	1 1	1 1	INHIBITED
0 1 OR 0 1	1 OR 0 0 1	1 1 1	1 1 1	0 0 1	1 1 0	ACTIVE DATA STATE

* LOW OUTPUT REPRESENTS THE CURRENT ON STATE.
HIGH OUTPUT REPRESENTS THE CURRENT OFF STATE.

TRUTH TABLE

NOTES:

1. OUTPUT LEVELS - L = MOST NEGATIVE LEVEL
H = LEAST NEGATIVE LEVEL

3006A

2. INPUT LEVELS - H = MOST POSITIVE LEVEL
L = LEAST POSITIVE LEVEL

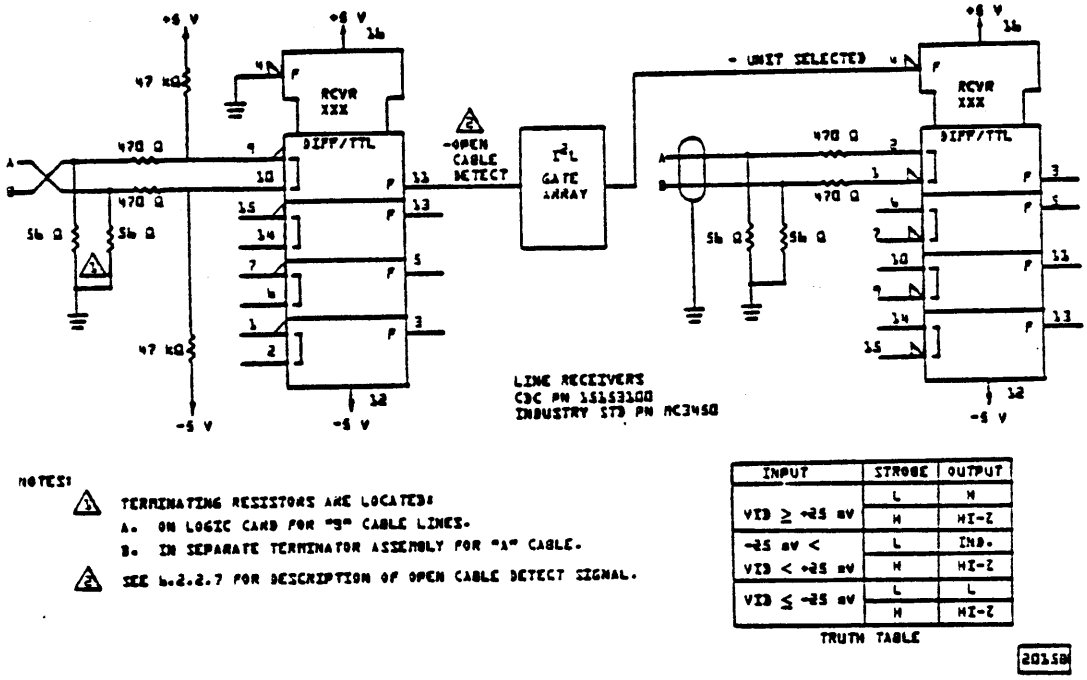
3. THIS IS AN INDETERMINATE INSTRUCTION WHEN SENSED BY AN ACTIVE (SELECTED) RECEIVER.

4. VOLTAGE RANGE INCLUDES TRANSMITTER OUTPUT SWING IN LOW STATE OF 11 ±3 mA, AND TERMINATING RESISTOR RANGE OF 56 ±5% OHMS.

5. TERMINATING RESISTORS ARE REQUIRED ON ALL "A" CABLE TRANSMITTERS. TRANSMITTERS IN THE DRIVE ARE TERMINATED BY THE TERMINATOR ASSEMBLY. REFER TO SINGLE AND DUAL CHANNEL INTERFACE ILLUSTRATION, AND THE TERMINATOR PARAGRAPH.

6. RECEIVER INPUTS A AND B ARE CONNECTED TO TRANSMITTER OUTPUTS Y AND Z RESPECTIVELY.

FIGURE 8. CONTROL LINE TRANSMITTER



NOTES:

1. TERMINATING RESISTORS ARE LOCATED:
   A. ON LOGIC CARD FOR "B" CABLE LINES.
   B. IN SEPARATE TERMINATOR ASSEMBLY FOR "A" CABLE.
2. SEE 6.2.2.7 FOR DESCRIPTION OF OPEN CABLE DETECT SIGNAL.

INPUT	STROBE	OUTPUT
VID ≥ +25 mV	L	H
	H	HI-Z
-25 mV < VID < +25 mV	L	IND.
	H	HI-Z
VID ≤ -25 mV	L	L
	H	HI-Z

TRUTH TABLE

20158

FIGURE 9. CONTROL LINE RECEIVER

6.1.4 Terminator

1. "A" Cable

A termination resistance as shown in Figures 8 and 9 is required at the transmitter and receiver end of each transmission line of the "A" cable. This resistance is provided on the unit by the terminator assembly (see Table 1 and Figure 10), which must be ordered separately.

2. "B" Cable

A termination resistance as shown in Figure 7 is required at the receiver end of each transmission line of the "B" cable. This resistance is provided at the unit's receiver logic card.

6.1.5 I/O Connectors and Cables

6.1.5.1 "A" Cable

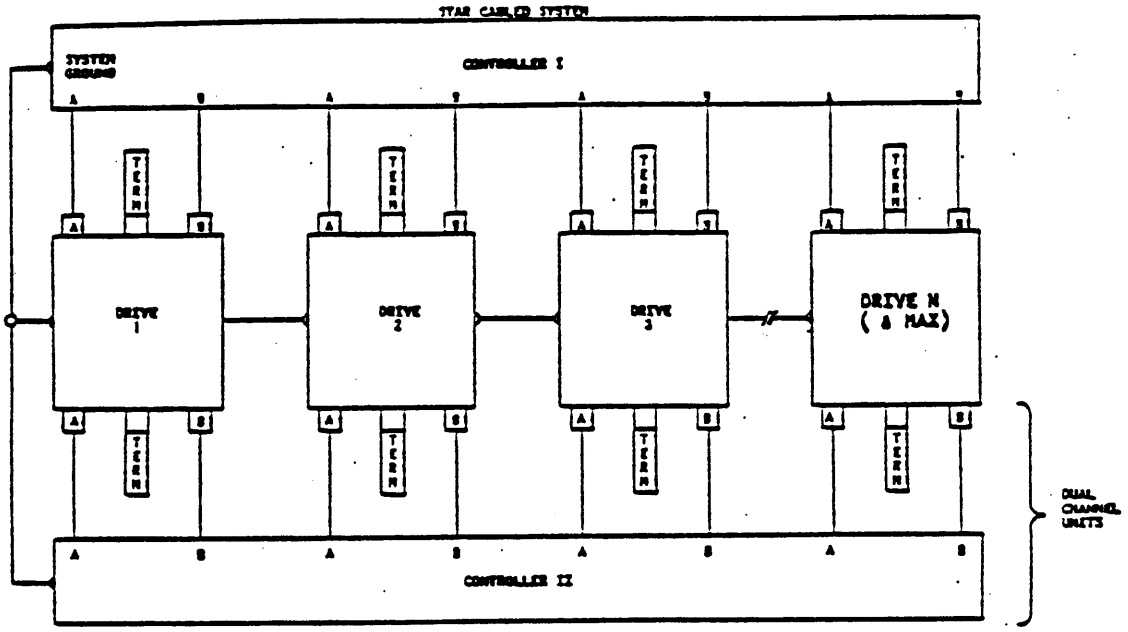
DESCRIPTION	MPI PN	3M PN
Connector (60 pos.)	10130439	3334-7060
Flat cable shielded, 60 wire, 28AWG	73157980	3638-60
Connector pull tab	92004804	3490-5

6.1.5.2 "A" Cable Mating Receptacle on Unit or Controller

DESCRIPTION	MPI PN	3M PN
60 pin, right angle header	15014076	3372-1002
60 pin vertical header	15014112	3372-2002

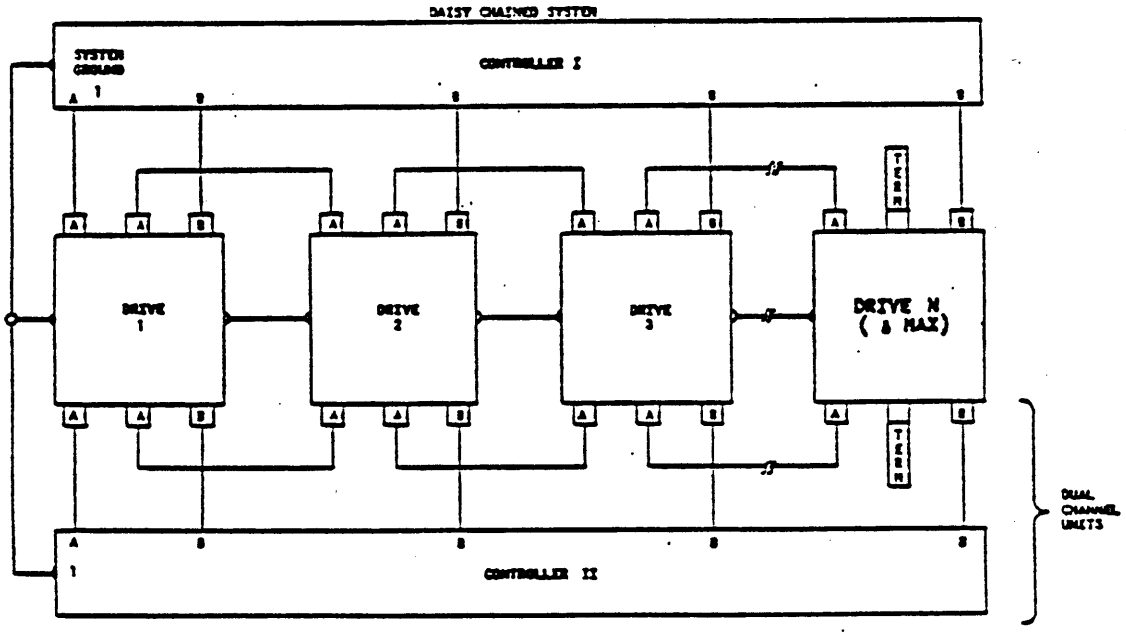
6.1.5.3 "B" Cable

DESCRIPTION	MPI PN	3M PN
Connector (26 pos.)	10130435	3399-7026
Connector pull tab	92004801	3490-2
Flat cable (26 pos.) shielded	73157982	3638-26



NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET



NOTES:

1. TERMINATION OF "A" CABLE LINES ARE REQUIRED AT CONTROLLER AND THE LAST UNIT OF THE DAISY CHAIN OR EACH UNIT IN A STAR.
2. TERMINATION OF "B" CABLE RECEIVER LINES ARE REQUIRED AT THE CONTROLLER AND ARE ON THE UNIT'S RECEIVER CARDS.
3. MAXIMUM CUMULATIVE A CABLE LENGTH PER CONTROLLER = 100 FEET.
   MAXIMUM INDIVIDUAL B CABLE LENGTH = 50 FEET.

FIGURE 10. SINGLE AND DUAL CHANNEL INTERFACE

6.1.5.4 B" Cable Mating Receptacle on Unit or Controller

DESCRIPTION	MPI PN	3M PN
26 pin, right angle header	15014072	3429-1002
26 pin, vertical header	15014108	3429-2002

6.1.6 I/O Cable Characteristics

"A" Cable

Type:	60 pin shielded, flat-cable
Impedance:	100 ±10 Ω
Wire size:	28 AWG, 7 strands
Propagation time:	1.4 to 1.6 ns/ft
Maximum cable length:	100 ft cumulative
Voltage rating:	150 V rms

"B" CABLE

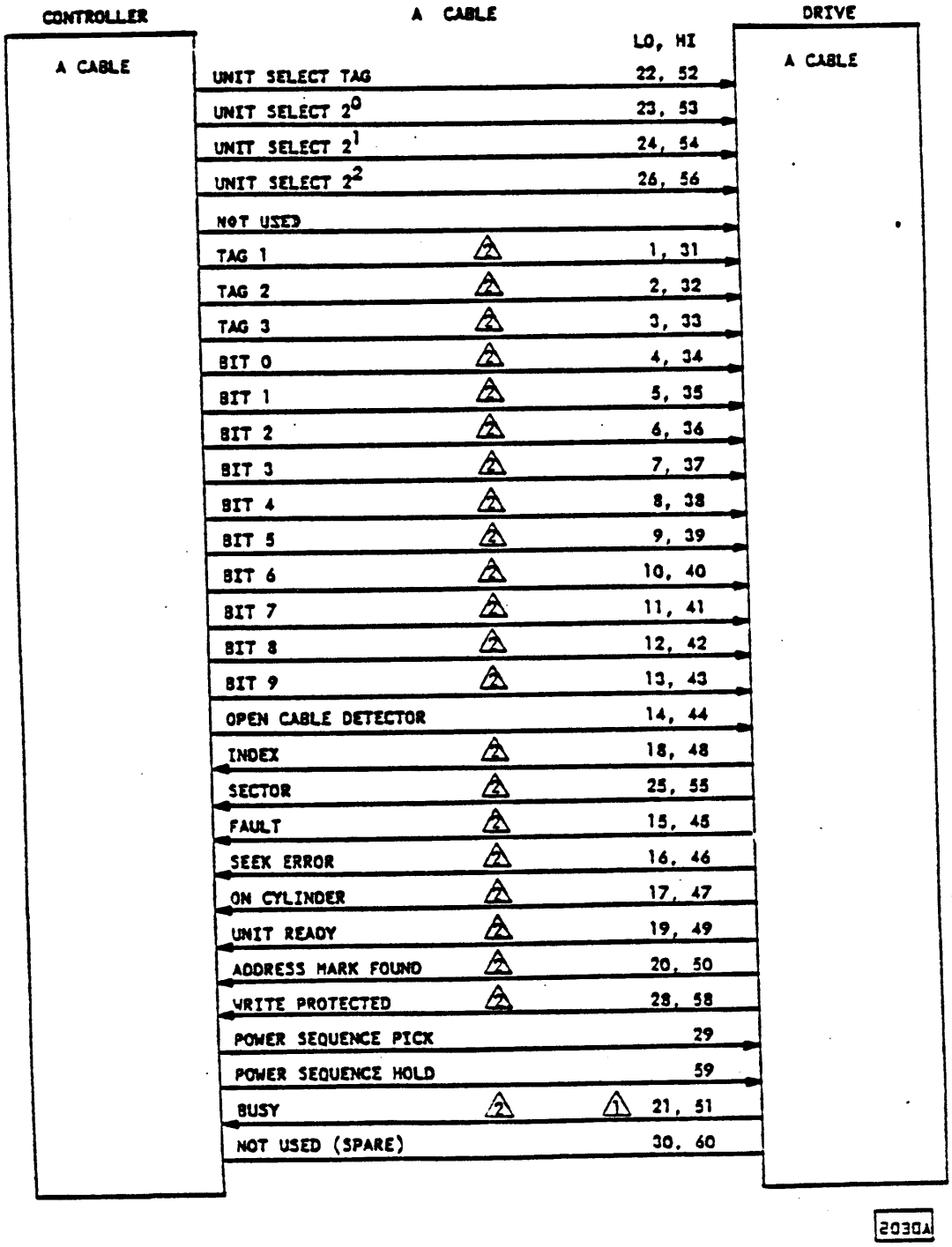
Type:	26 conductor, shielded, flat-cable
Impedance:	130 ±15 Ω
Wire size:	No. 28 AWG, 7 strands
Propagation time:	1.4 to 1.6 ns/ft
Maximum cable length:	50 ft
Voltage rating:	150 V rms

6.2 Signal Lines

See Figure 11 for the "A" (Address/Control) cable and Figure 12 for the "B" (data) cable I/O signals.

6.2.1 Address and Control Tag Functions

Address and Control functions are transferred on 10 lines. The significance of the information on these lines is indicated by one of three Tag Lines (see Figure 13). See Figure 14 for timing.

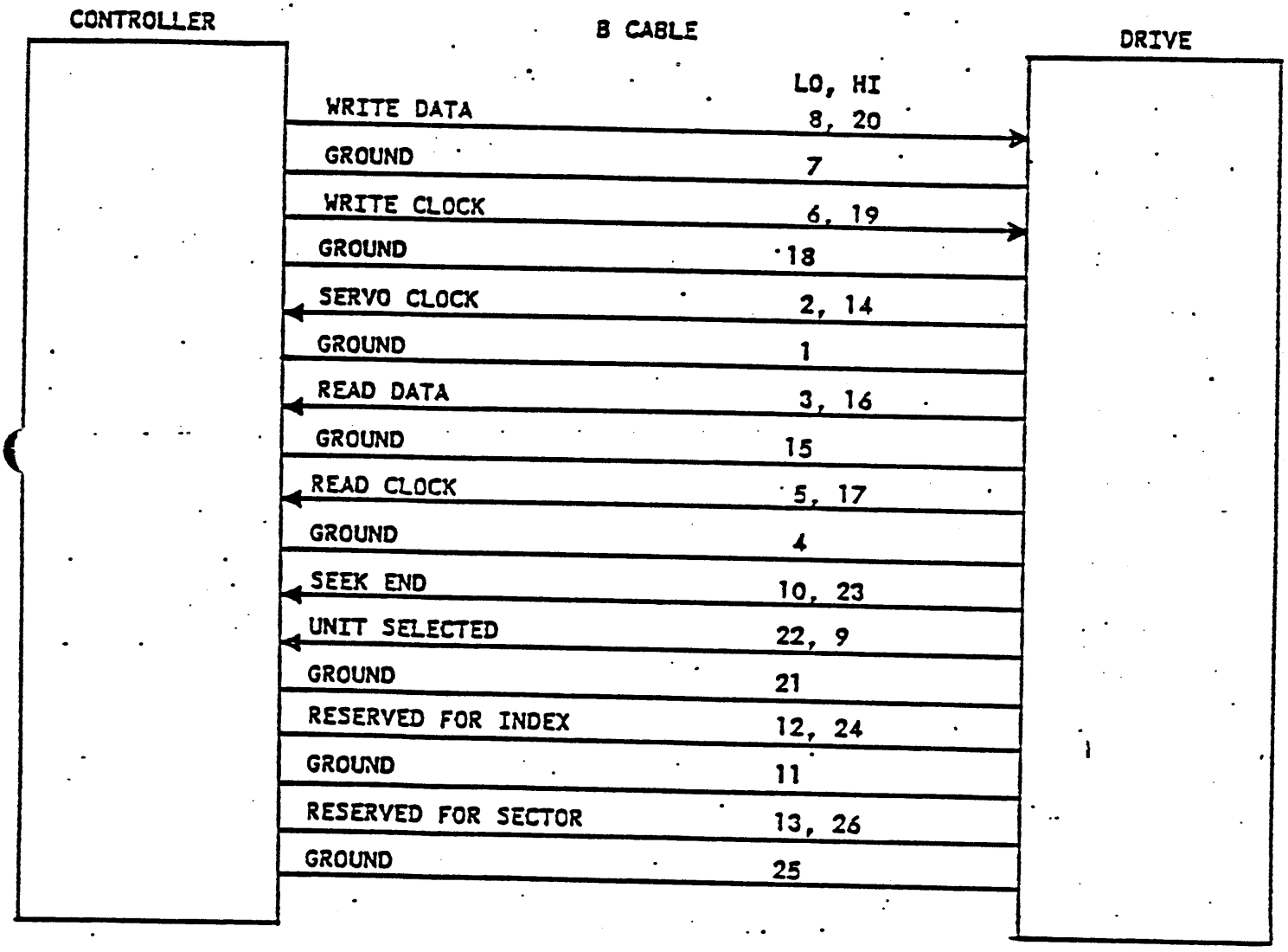


NOTE: 60 POSITION
28 AWG, STRAIGHT FLAT CABLE
MAXIMUM LENGTH = 100 FT

(1) DUAL CHANNEL UNITS ONLY.

(2) GATED BY UNIT SELECTED.

FIGURE 11. TAG BUS I/O INTERFACE



NOTES: 1. 26 CONDUCTOR, SHIELDED FLAT CABLE. MAXIMUM LENGTH: 50 FT.

2. NO SIGNALS GATED BY UNIT SELECTED

2016A

FIGURE 12. "B" CABLE INTERFACE

BUS	TAG 1 IN CYLINDER ADDRESS	TAG 2 IN HEAD SELECT	TAG 3 IN CONTROL SELECT	UNIT SELECT
Bit 0	2^0	2^0	Write Gate	
1	2^1	2^1	Read Gate	
2	2^2	2^2	Servo Offset Plus	
3	2^3		Servo Offset Minus	
4	2^4		Fault Clear	
5	2^5		AM Enable	
6	2^6		RTZ	
7	2^7		Data Strobe Early	
8	2^8		Data Strobe Late	
9	2^9		Release (1)	Priority Select (1)

(1) DUAL CHANNEL ONLY

FIGURE 13. TAG BUS DECODE

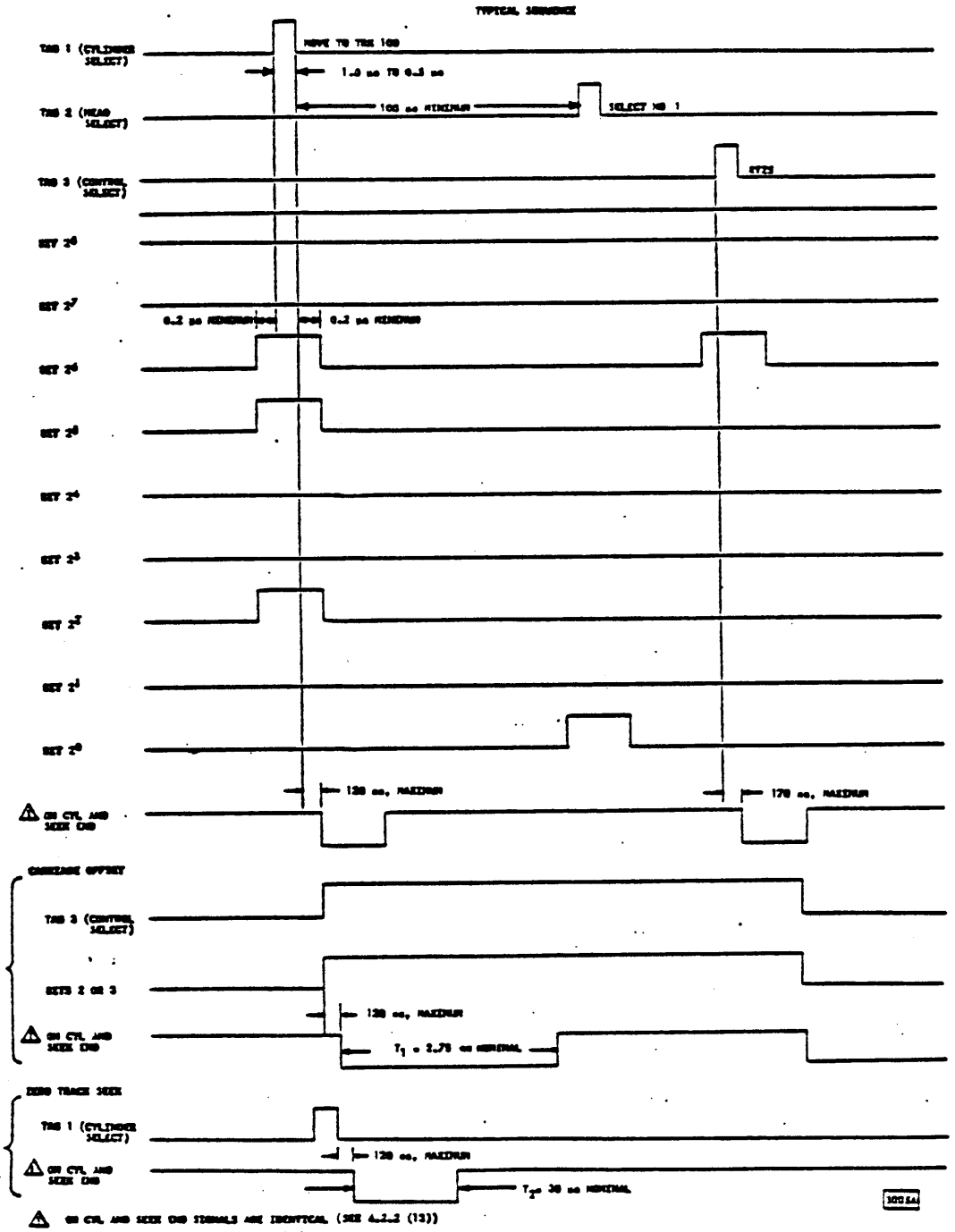


FIGURE 14. TAG AND BUS TIMING

6.2.1.1 Cylinder Address (Tag 1)

The FSD Drive is a direct addressing device, the controller need only place the new address on the bus lines and strobe the lines with Tag 1. The unit must be On Cylinder before Tag 1 is sent.

6.2.1.2 Head Select (Tag 2)

This signal is the head address that will be selected by bits 0 through 3.

6.2.1.3 Control Select (Tag 3)

This signal acts as an enable and must be true for the entire control operation.

6.2.1.3.1 Write Gate (Bit 0)

The Write Gate line enables the write driver (Figure 13).

6.2.1.3.2 Read Gate (Bit 1)

Enabling of the Read Gate (see Figure 14), enables digital read data on the transmission lines. The leading edge of Read Gate triggers the read chain to synchronize on an all zeros pattern. (See Figure 15 for Read Gate and Write Splice relationship).

6.2.1.3.3 Servo Offset Plus (Bit 2) (See Note in 6.2.1.3.9)

When this signal is true, the actuator is offset from the nominal On Cylinder position towards the spindle. On Cylinder will drop for 2.75 ms nominal.

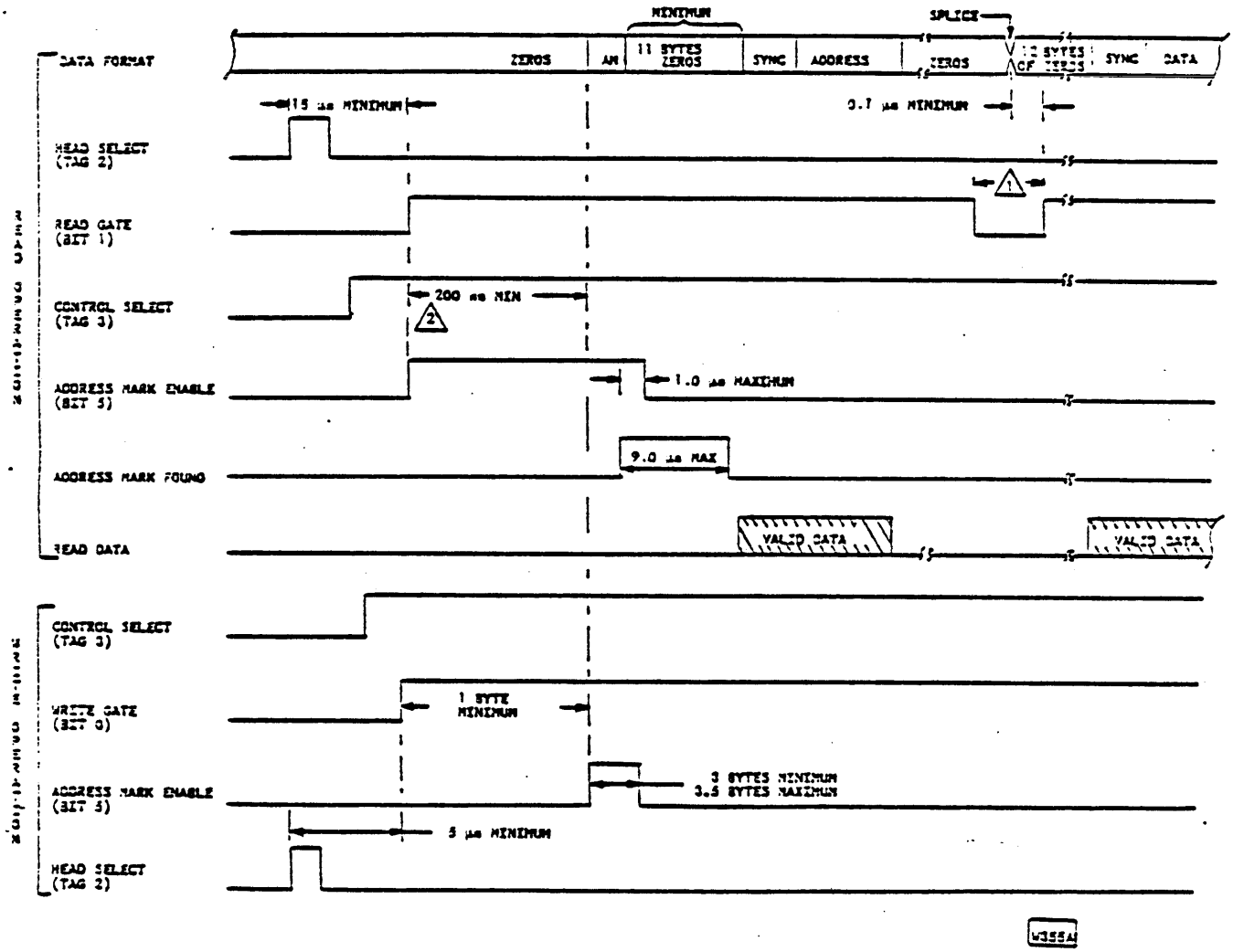
6.2.1.3.4 Servo Offset Minus (Bit 3) (See Note in 6.2.1.3.9)

When this signal is true, the actuator is offset from the nominal On Cylinder position away from the spindle. On Cylinder will drop for 2.75 ms nominal.

NOTE: When dropping Offset Plus or Minus, on cylinder will drop for 2.73 ms nominal.

6.2.1.3.5 Fault Clear (Bit 4)

A 100 ns minimum pulse sent to the FSD Drive will clear the Fault flip-flop if the fault condition no longer exists.



NOTES: ⚠1 READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 10 BYTES OF ZERO BITS REMAINING IN THE SYNC FIELD. 12 BYTE EXAMPLE CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

⚠2 ADDRESS MARK ENABLE SHOULD OCCUR SIMULTANEOUS WITH READ GATE.

FIGURE 15. TYPICAL TIMING WITH ADDRESS MARK

6.2.1.3.6 AM Enable (Bit 5) (See Note)

The AM (Address Mark) Enable line, in conjunction with Write Gate or Read Gate, allows the writing or recovering of Address Marks (Figure 15). When AM Enable is true while Write Gate is true, the writer stops toggling and erases the data, creating an Address Mark. Write fault detection in the unit is inhibited by this signal.

When AM Enable is true while Read Gate is true, an analog voltage comparator detects the absence of Read signal. If the duration of the erased area is greater than 20 but less than 36 bits, an Address Mark Found signal will be issued.

NOTE: If Address Mark is not used, Bit 5 must be held inactive during Control Select functions.

Address Mark should be 3.0 bytes in length with no transitions.

6.2.1.3.7 RTZ (Bit 6)

A 250 ns minimum, 1.0 ms maximum pulse, sent to the Drive will cause the actuator to seek track 0, reset the Head register and clear the Seek Error flip-flop.

This seek is significantly longer than a normal seek to track 0, and should only be used for recalibration, not data acquisition.

6.2.1.3.8 Data Strobe Early (Bit 7) (See Note in 6.2.1.3.9)

When this line is true, the Drive PLO Data Separator will strobe the data at a time earlier than nominal. Normal strobe timing will be returned when the line is false.

6.2.1.3.9 Data Strobe Late (Bit 8)

When this line is true, the Drive PLO Data Separator will strobe the data at a time later than nominal. Normal strobe timing will be returned when the line is false.

NOTE: The Data Strobe and Carriage Offset signals are intended to be used as an aid to recover marginal data. The carriage and data strobe position return to nominal when the respective signals go false. A carriage offset will result in loss of On Cylinder and Seek End for a period of 2.75 ms maximum (see Figure 14). The nominal time for the carriage to move from forward to reverse offset or vice versa will be 4 ms. Write gate should not be raised by the controller while in the offset mode.

6.2.1.3.10 Release (Bit 9) (Dual Channel Only)

Enabling this line will release Channel Reserve and Channel Priority Select Reserve in the Drive, making alternate channel access possible after selection by the other channel ceases. If the unit is desired to function with "Reserve Timer" feature, release will occur 500 ms (nominal) following the deselection of the Drive. If a longer or shorter time is desired, the timer may be customer altered by changing a resistor and capacitor to obtain delays from 500 ns to 10 seconds. Enabling Release will always clear Reserve and allow alternate channel access independent of the Reserve Timer feature. The Reserve Timer is enabled by means of a switch in the logic chassis. Inhibiting the Reserve Timer causes the Drive to stay reserved until specifically released by the operating channel. A unit is reserved immediately upon selection, but may be released any time after 500 ns following selection. By means of a switch on the dual channel card, it is also possible to absolutely reserve an Drive to one or the other channels.

6.2.1.4 Unit Select

Priority Select (Bit 9) (Dual Channel Only)

When this line is true during Unit Select Tag (see 6.2.2.8), the unit will be unconditionally selected and absolutely reserved by the respective channel providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the priority select function has been performed the respective channel has exclusive access to the drive. The opposite channel can gain access only after a release function has been performed on the selected channel. For timing see Figures 17 and 18.

6.2.2 Individual Lines

6.2.2.1 Sector Mark

The Sector Mark is derived from the servo track. Timing integrity is maintained throughout seek operations (see Figure 16). The number of sectors per revolution is switch selectable and is determined by counting Sector Clocks. The switches are located on the control card. Each switch represents a fixed number of Sector Clocks when closed.

Switch:	0	1	2	3	4	5	6	7	8	9	10	11
Sector Clocks:	1	2	4	8	16	32	64	128	256	512	1024	2048

To calculate the proper switch positions for the number of sectors desired, use the following formula:

$$\frac{\text{Clocks/Revolution}}{\text{No. Sectors}} - 1 = \text{Sector Clock Count/Sector}$$

Example for 8 Sectors: $\frac{13\ 440}{8} - 1 = 1679$

Close switch 10 = 1024
9 = 512
7 = 128
3 = 8
2 = 4
1 = 2
0 = 1

One Sector Clock for SM Counter Reset = $\frac{1}{1680}$

Each Sector Clock is equivalent to 12 data bits.

6.2.2.2 Fault

When this line is true, a fault condition exists in the Drive. The following types of faults may be detected by the Drive: voltage fault, MPU/first seek fault, Write fault, Write or Read while Off Cylinder, and Write Gate during a Read operation. A fault condition will immediately inhibit the writer to prevent data destruction. The dc power fault indicates a below normal voltage from the positive or negative power supplies. The Write fault indicates either low or absence of write current, absence of write data from the corresponding data head, or the absense of write clock from the controller when write gate is active.

The Fault line may be cleared by a Clear Fault command on the I/O or by depressing Fault Clear on the operator panel (providing the Fault no longer exists). As a maintenance aid, Fault indicators are provided on the control board. All Faults will be stored until powering down dc power or by depressing fault Clear on the operator panel.

6.2.2.3 Seek Error

When this line is true, a Seek Error has occurred. The error may only be cleared by performing an RTZ. This signal indicates that the unit was unable to complete a move or that the carriage has moved to a position outside the recording field, or that an address greater than 822 tracks has been selected. If an address greater than 822 tracks is selected, the Seek Error signal will go true within 250 µs max. of the Cylinder Select tag.

A Return-to-Zero Seek command will clear the Seek Error condition, return the heads to cylinder zero, and enable an On Cylinder signal to the controller.

6.2.2.4 On Cylinder

This status indicates the servo has positioned the heads over a track. The status is cleared with any seek instruction causing carriage movement, or a zero-track seek. A carriage offset will result in loss of On Cylinder for a period of 2.75 ms nominal. For a zero track seek, On Cylinder drops for 30 µs nominal.

6.2.2.5 Index

This signal occurs once per revolution, and its leading edge is considered the leading edge of the Sector Zero, typically 2.5 µs (see Figure 16). Timing integrity is retained throughout seek operations.

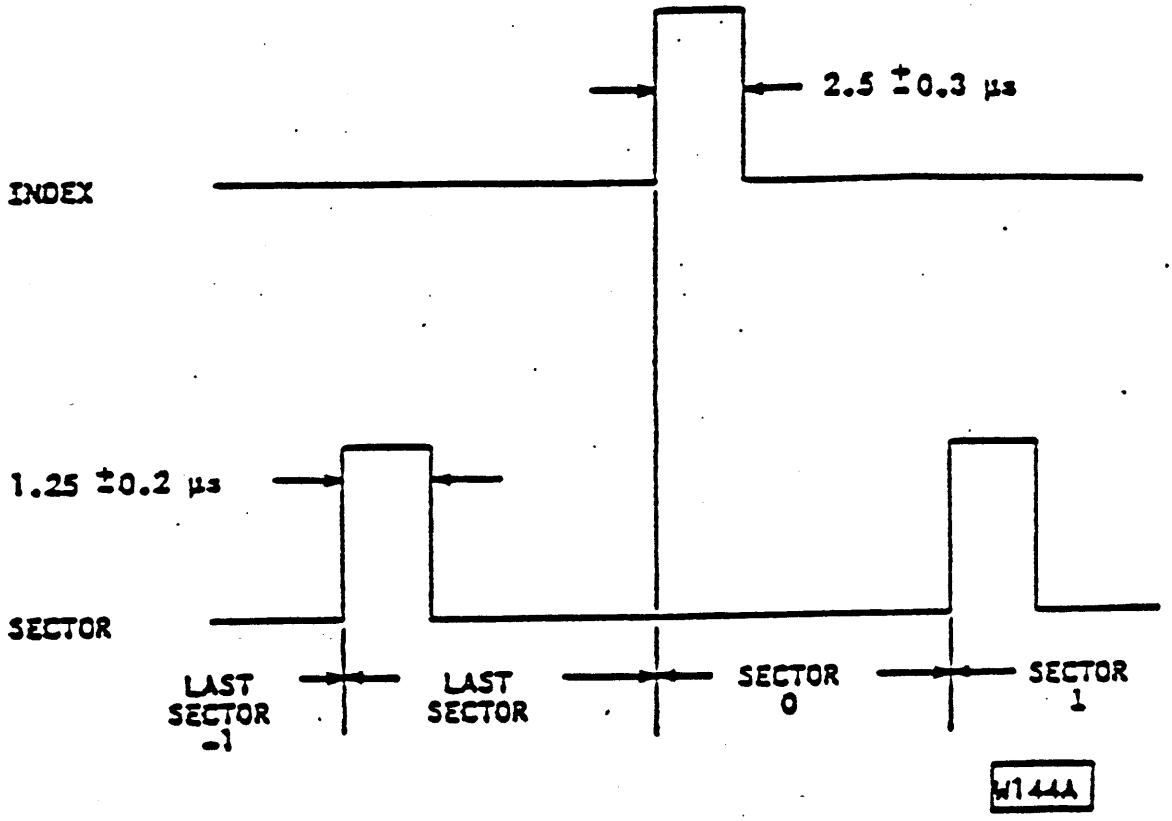


FIGURE 16. INDEX AND SECTOR TIMING

6.2.2.6 Unit Ready

When true this line indicates that the unit is up to speed and no fault condition exists within the Drive. If during a load sequence tribits are not sensed, a first seek fault will be indicated and Unit Ready will remain low.

6.2.2.7 Open Cable Detector

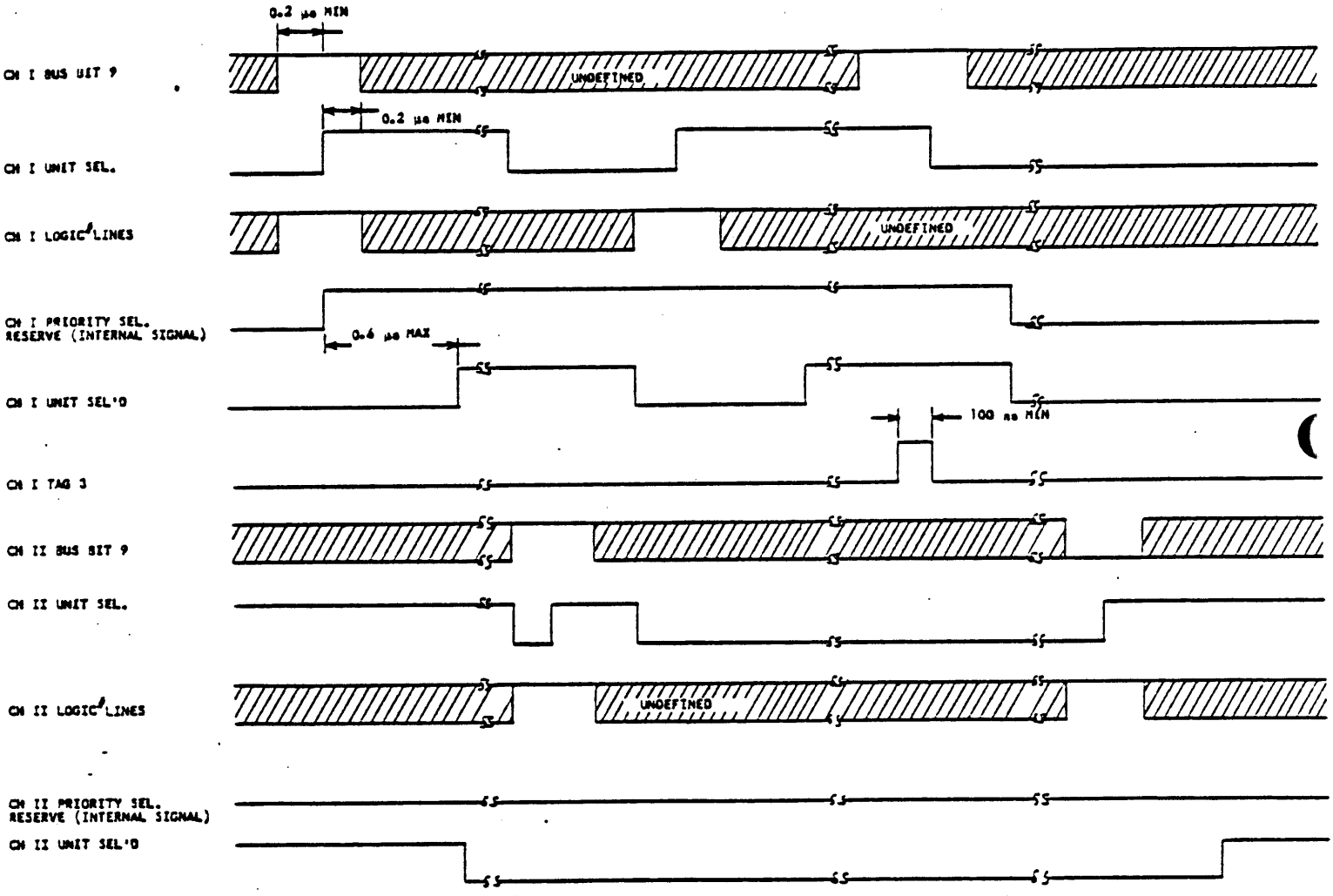
The Open Cable Detect circuit (see Figure 8) disables the interface in the event that the "A" interface cable is disconnected or controller power is lost.

It is recommended that the controller circuitry have sufficient voltage margins and interlocks to prevent operation on the Drive before the controller is ready or prior to impending controller power failure. Relay logic and passive terminations sometimes aid this requirement. If 75110A transmitters are used to drive the Open Cable Detect line from the controller, two transmitters should be paralleled, and no 56 Ω termination resistance to ground should be used at the controller end.

6.2.2.8 Unit Select Tag

This signal gates the desired logic number into the Logic Number Compare circuit. The unit will be selected internally 600 ns maximum after leading edge of this signal. For timing see Figures 17 and 18. Note that this function must be edge triggered.

In Dual-Channel units, Unit Select tag also forces the Drive to be reserved to that channel, providing selection occurs. The reserve will not be cancelled unless by Release command, Reserve Timer or dc power-down/power-up. If Bus Bit 9 and the desired logic number are present with Unit Select tag, a Priority Select will be perfomed, see 6.2.1.4. The unit will be selected internally 600 ns maximum after leading edge of Unit Select tag. For timing see Figure 18.



SEQUENCE OF EVENTS

1. CH II SELECTED
2. CH I PRIORITY SELECT
3. CH II PRIORITY SELECT
4. CH I RELEASE
5. CH II SELECT

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FIGURE 17. SAMPLE PRIORITY SELECT TIMING

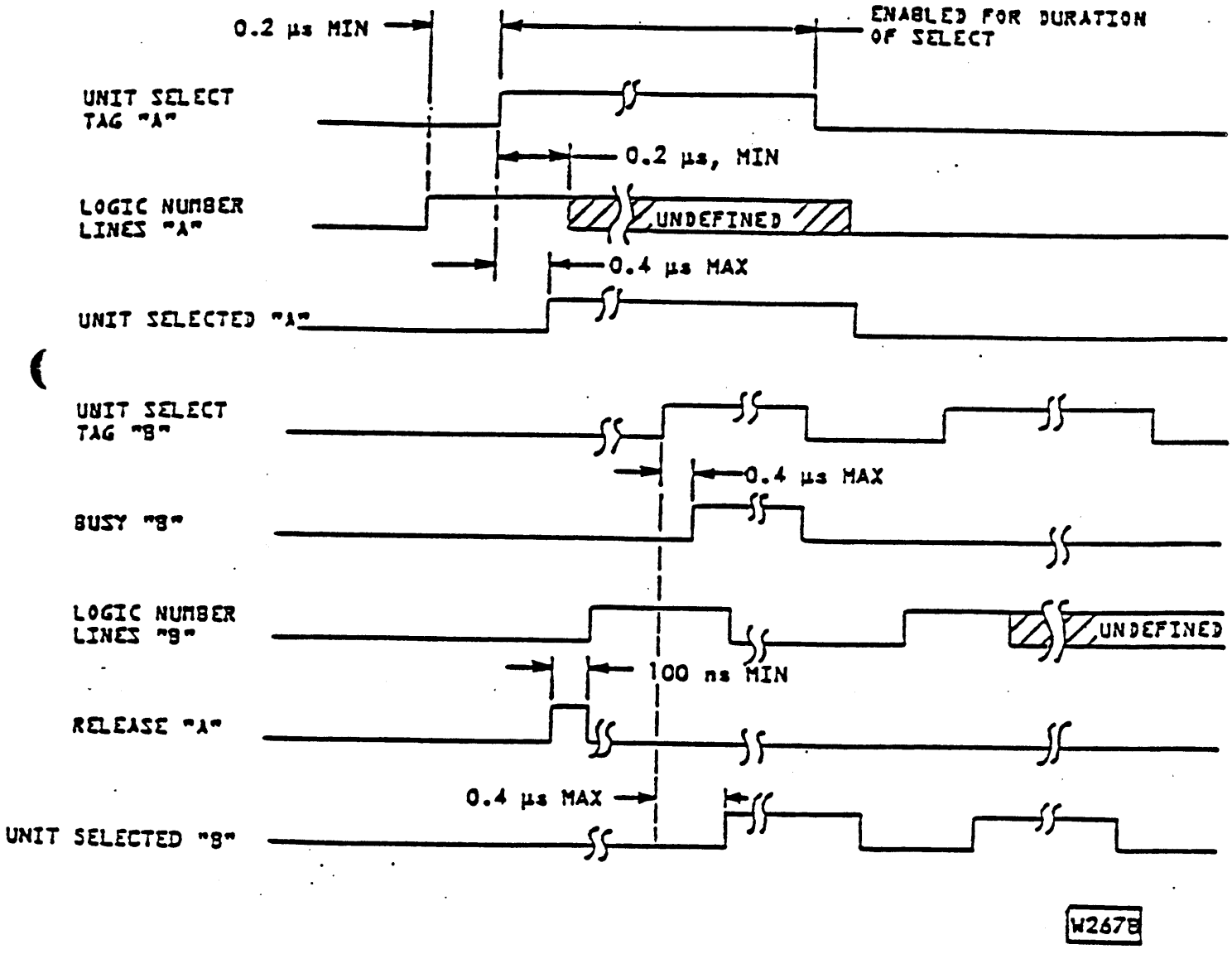


FIGURE 18. LOGIC NUMBER SELECT AND TIMING DIAGRAM

6.2.2.9 Unit Select (2^0, 2^1 and 2^2)

These three lines are binary coded to select the logical number one of eight Drives. The unit number (0 through 7) is selectable by means of a logic plug on the operator panel in each individual unit. Care should be taken to have no duplicate logic plugs in the same system. Removing the logic plug from any unit results in a logic number 7.

6.2.2.10 Address Mark Found

Address Mark Found is a 9.0 µs maximum pulse which is sent to the controller following recognition of at least 20 but less than 36 missing transitions and the first zero of the zeros pattern.

The controller must drop the Address Mark Enable line (Bit 9) upon receiving Address Mark Found (AMF) and valid data will be presented on the I/O lines following the AMF pulse. (see Figure 15).

NOTE: Under certain conditions it is possible that the Drive could issue a false Address Mark Found signal during an address mark search operation. This would occur if a media flaw existed which simulated the electrical characteristics of an Address Mark (at least 20 but less than 36 missing transitions followed by a zero).

It is recommended provisions be made in system hardware or software to allow recovery from, or avoid the possibility of detecting false AMF signals.

6.2.2.11 Unit Selected

When the three Unit Select bit lines compare with the logic plug on the control panel, and when the leading edge of Unit Select tag is received, the Unit Selected line becomes true and is transmitted to the controller on the "B" cable (see Figures 17 and 18). Multiple Unit Selected responses on a daisy chain system indicated duplicate plugs have been installed

6.2.2.12 Write Protected

Enabling the Write Protect function inhibits the writer under all conditions, illuminates a front panel LED, and sends a Write Protected signal to controller. Attempting to write while protected will cause a fault to be issued. The write protect function is enabled by a front panel switch or a switch on the control card.

6.2.2.13 Seek End

Seek End is the combination of On Cylinder or Seek Error indicating that a seek operation has terminated. In dual channel drives, the Seek End signal sent to the unselected channel will normally be a constant one. However, if while the drive is selected on a channel, and the opposite channel receives a Select, this action will be noted by circuitry within the drive. Then, when the selected channels Select and Reserve latches are cleared, the Seek End signal sent to the waiting channel will go to a zero for 30 µs. If an address greater than 823 tracks has been selected, Seek End and On Cylinder will interrupt for 30 µs nominal (see Figure 18).

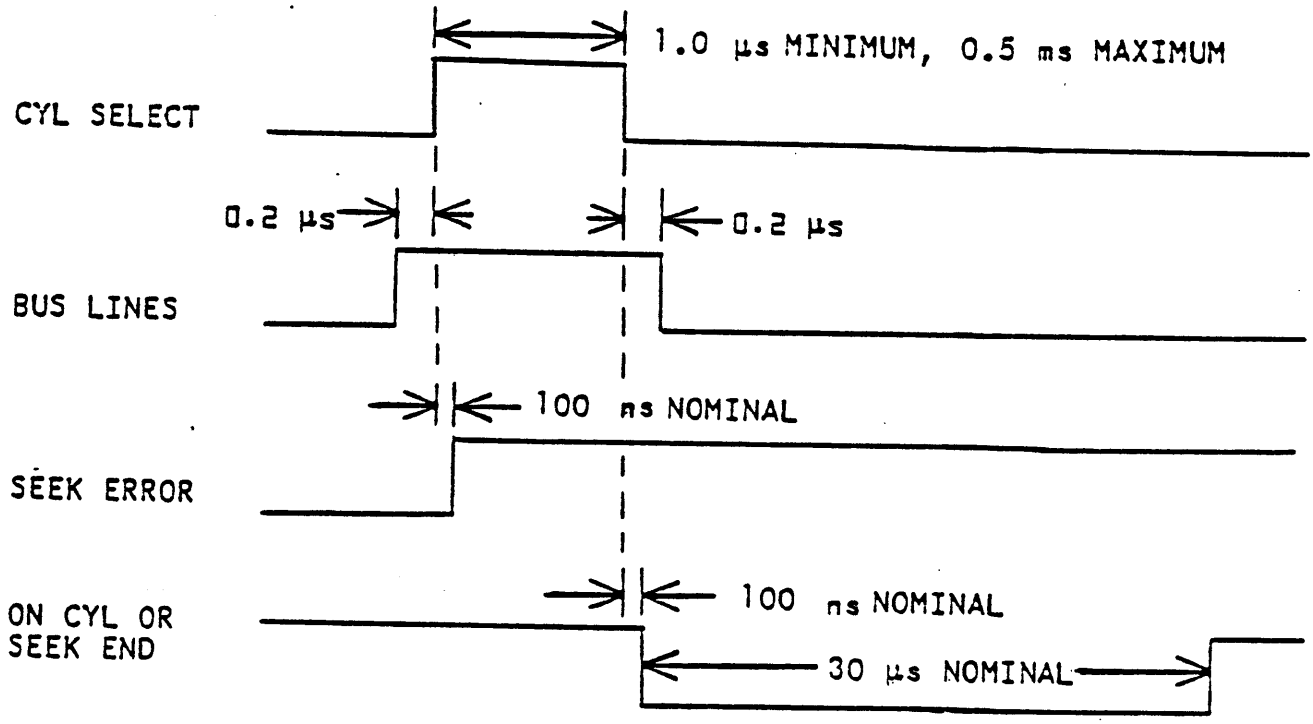


FIGURE 19. SEEK END TIMING

6.2.2.14 Power Sequencing

Power sequencing requires the ac power on, START indicator on and REMOTE SEQUENCE switch in the REMOTE position. Applying ground to the Pick and Hold lines will cause all drives logically connected to power up. Individual power up is not required because of the low power consumption of each Drive.

6.2.2.15 Busy (Dual Chanel Only)

If the Drive is already reserved and/or selected, a Busy signal will be issued to the "A" cable and Unit Selected will be issued on the "B" cable to the channel attempting the select. This Busy signal will be issued from the at its I/O connector within 600 ns following the selection attempt, and remain at this status until Unit Select tag is dropped or the unit is no longer Busy. Unit Selected should be used to enable Busy in the controller.

6.2.3 Data and Clock Lines

6.2.3.1 Write Data

This line carries data which is to be recorded on the disk.

6.2.3.2 Servo Clock

The Servo Clock is a phase-locked 9.677 MHz clock generated from the servo track tribits. (see Figure 20(A)). Servo Clock is available at all times (not gated with Unit Select).

6.2.3.3 Read Data

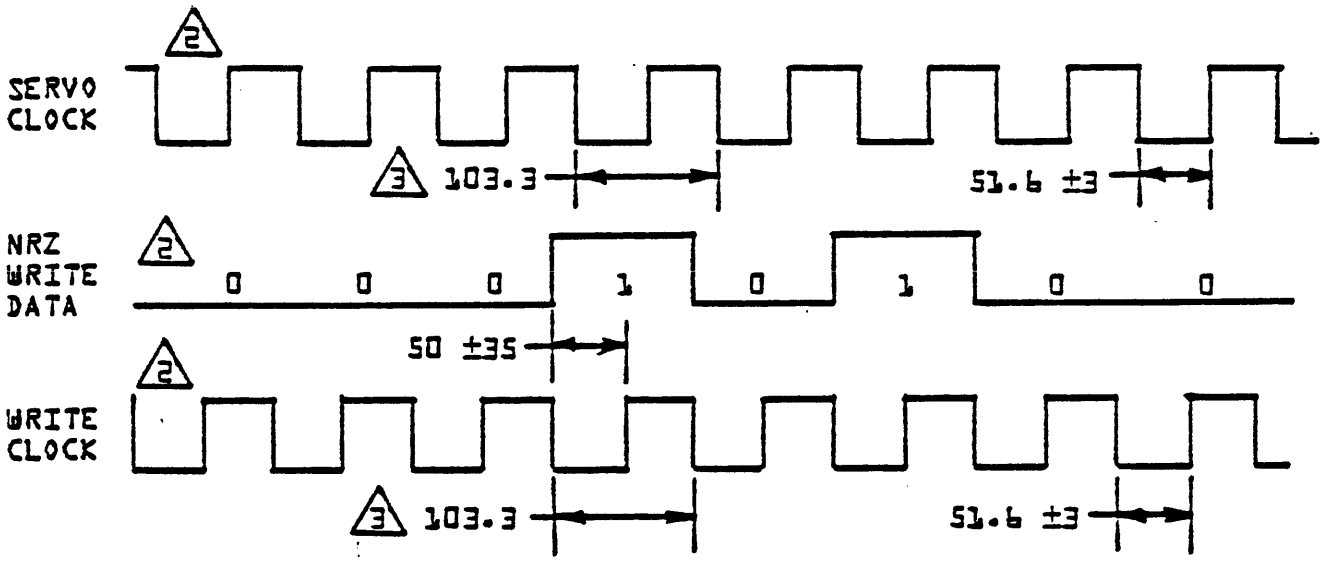
This line transmits the recovered data in the form of NRZ data (see Figure 20(B)).

6.2.3.4 Read Clock

The Read Clock defines the beginning of a data cell. It is an internally derived clock signal and is synchronous with the detected data as specified in Figure 19(B). This signal is transmitted continuously, and is in phase sync within 9 µs after Read Gate.

6.2.3.5 Write Clock

This line transmits the Write Clock signal which must be synchronized to the NRZ Data as illustrated in Figure 19(A). The Write Clock is the Servo Clock retransmitted to the Drive by the controller, during a write operation. The Write Clock need not be transmitted continuously, but must be transmitted at least 250 ns prior to Write Enable.



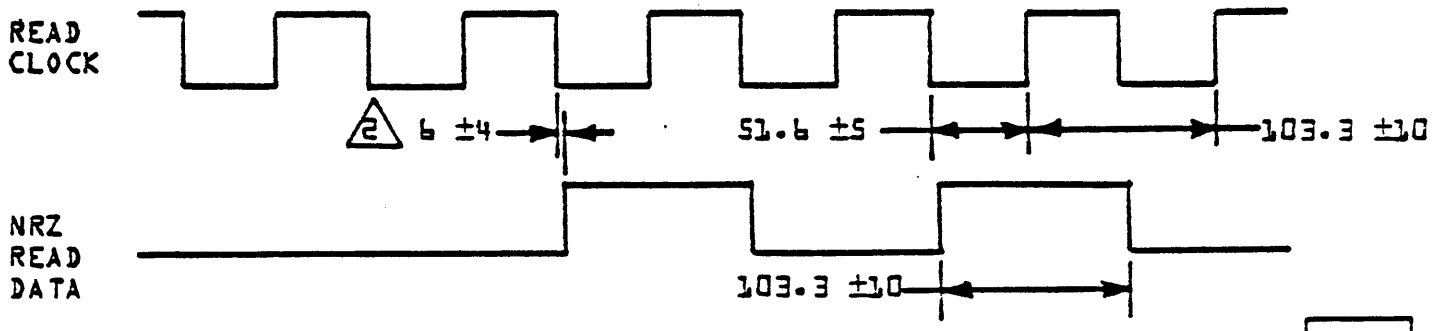
NOTES: 1. ALL TIME IN ns.

2 AT DRIVE I/O CONNECTOR.

3 SIMILAR PERIOD SYMMETRY IS ±2 ns. AT I/O CONNECTOR IN DRIVE SPEED VARIATION TOLERANCE IS ±1% CONSISTING OF:

- VARIATIONS BETWEEN INNER AND OUTER CYLINDER.
- DYNAMIC JITTER ON BYTE-TO-BYTE BASIS. APPLIES WHEN ON CYLINDER.
- TRIBIT SKEW AND DROPOUT. APPLIES DURING SEEK.

A. WRITE TIMING



NOTES: 1. ALL TIME IN ns

2 NEGATIVE EDGE OF CLOCK PRECEDES SIGNIFICANT EDGE OF DATA AT I/O CONNECTOR.

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B. READ TIMING

FIGURE 20. DATA TIMING

6.3 Data Format and Data Control Timing

The record format on the disk is under control of the controller. The Index and Sector pulses are available for use by the controller to indicate the beginning of a track or sector. Minimum formats for fixed and variable sector data records are shown in Figures 21 and 22.

Some hardware-oriented constraints must be recognized when designing a format. The following is a list of those format parameters:

1. Beginning-of-Record Tolerance

   This tolerance must be provided to allow for worst case conditions of head skew and circuit tolerances.

   This gap must be written with a minimum of 16 bytes of zeros.

2. Read PLO Synchronization

   The synchronization time needed to allow the Phase-Locked Oscillator to synchronize is 9.0 µs of zeros.

3. Sync Pattern

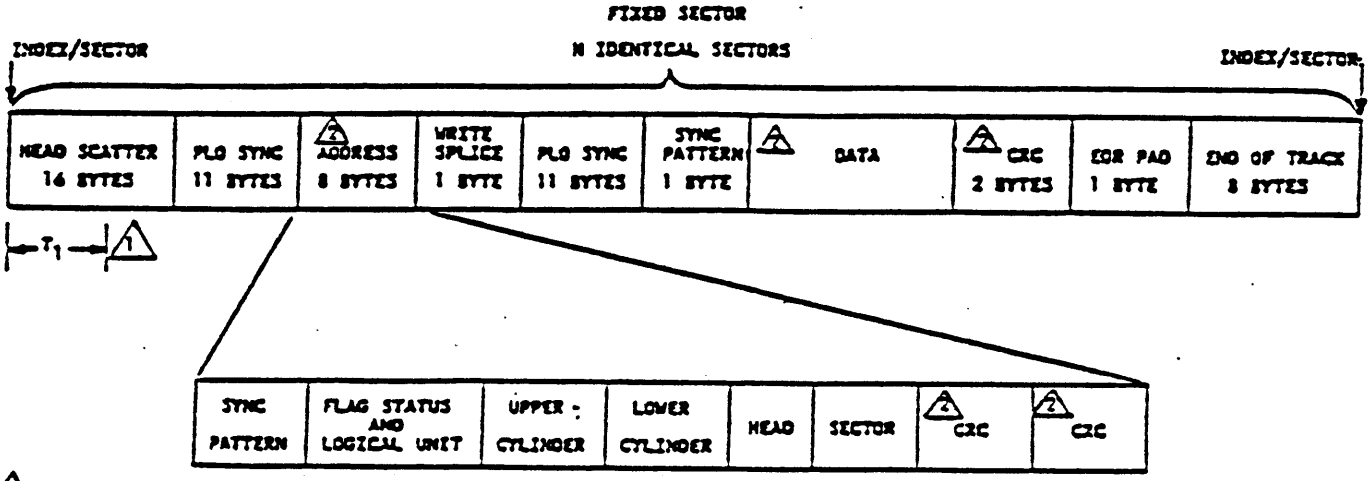
   The sync pattern consists of "one" bits indicating the beginning of the address or data area (one "one" bit is the minimum required).

4. Write Driver Turn On

   The write driver turn on time is about 0.8 µs or one byte. This time has to be accounted for in order to know where possible splice areas are located.

5. End-of-Record Tolerance

   This tolerance is an eight byte pad of zeros which eliminates the possibility of destroying the end of a record written with a late displacement head. This is accomplished by writing an adjacent succeeding sector with an early head.



1. T_1 = TIME BETWEEN LEADING EDGE OF INDEX/SECTOR AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

2. THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

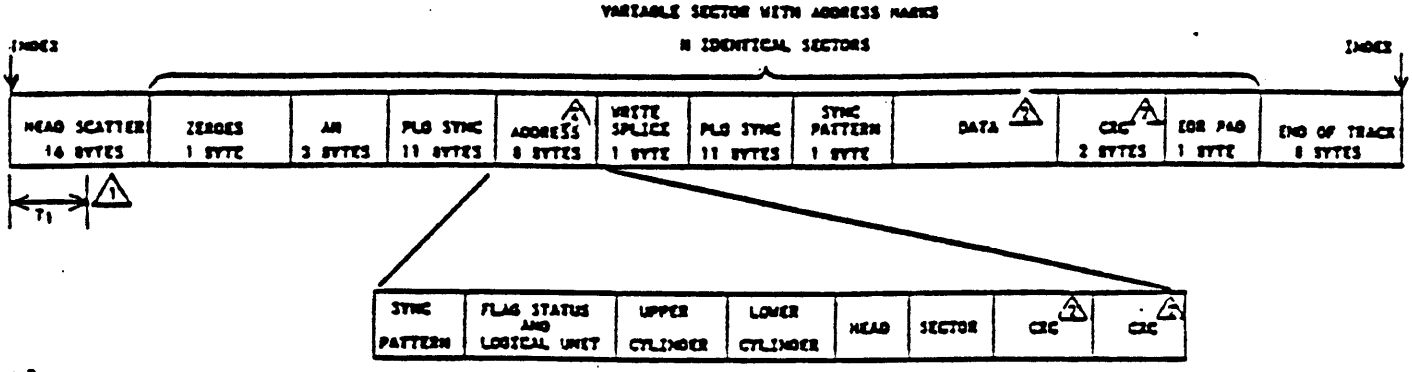
$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS})$$

$$\text{DATA FIELD} = \frac{20\,160}{64} - 59 = 256\ \frac{\text{BYTES}}{\text{SECTOR}}$$

DATA = 256 BYTES/SECTOR

$$\%\ \text{EFFICIENCY} = \frac{256 \times 64}{20\,160} \times 100 = 81\%$$

FIGURE 21. FIXED SECTOR FORMAT



1. T_1 = TIME BETWEEN LEADING EDGE OF INDEX AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

2. THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

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EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK} - \text{MECHANICAL TOLERANCES}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS AND ADDRESS})$$

$$\text{DATA FIELD} = \frac{20\,160\ \frac{\text{BYTES}}{\text{TRACK}} - 24\ \frac{\text{BYTES}}{\text{TRACK}}}{64\ \frac{\text{SECTORS}}{\text{TRACK}}} - 39\ \frac{\text{BYTES}}{\text{SECTOR}} = 275\ \frac{\text{BYTES}}{\text{SECTOR}}$$

$$\% \text{ EFFICIENCY} = \frac{275 \times 64}{20\,160} \times 100 = 87\%$$

EXAMPLE NO. 2: WHAT IS NUMBER OF SECTORS USING 256 DATA BYTES?

$$\text{N SECTORS} = \frac{20\,160 - 24}{256 + 39} = 68\ \text{SECTORS}$$

$$\% \text{ EFFICIENCY} = \frac{256 \times 68}{20\,160} \times 100 = 86\%$$

FIGURE 22. VARIABLE SECTOR FORMAT

6.3.1 Write Format

Provisions must be made within the controller to format the disk. The following is recommended for fixed sector formats:

1. Select desired unit, cylinder, head, and sector.

2. The controller must provide a 5 µs minimum delay between selecting a head and initiating a search for leading edge of sector. This delay will ensure that the unit will be ready to write when the sector leading edge is detected.

3. Search for leading edge of desired sector.

4. Detect leading edge of selected sector.

5. Immediately bring up Write Gate and start writing zeros.

6. Write all zeros for head scatter and PLO sync areas (27 bytes).

7. Write a sync pattern, the address, and the address checkword.

8. Write all zeros for write splice gap and PLO sync field (12 bytes).

9. Write a sync pattern, the data field, the two byte data field checkword, and the one byte pad at the end of the checkword. The data field should be written with all ones or preferably a worst case pattern.

10. The end tolerance gap is the only part of the format where there may be erased areas with no write data. If erased areas occur in Gap 2 there may be problems in recovering the data following this gap.

11. If the next sector of the same track is to be formatted and the head is not deselected, the Write Gate should be left on. In this case. the controller should write all zeros in the tolerance gap. If Write Gate is dropped, it should not be raised again within 2 µs.

6.3.2 Control Timing (See Figure 18)

1. Read

The control line associated with a Read command is the Read Gate line.

The leading edge of Read Gate forces the Phase Locked Oscillator to synchronize on an all zeros pattern. Read Gate also enables the output of the Data Separator onto the I/O lines after a lock-to-data internal time out. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled 60 ±4 clock counts after the leading edge of Index or Sector.

The sync pattern search may begin 88 servo clock counts after the leading edge of Read Gate.

Head switching and read amplifier stabilization (see Figure 23(B)) shows the latest acceptable time at which a head can be selected in order to read the next successive sector (with the format described in 6.3).

Data I/O lines may not have valid data until 9 µs from leading edge of Read Gate, due to phase lock synchronizing time.

Ensure that there will be no splice area after Read Gate is brought up even under worst case pack interchange conditions.

2. Write Data Field

The control line associated with a write operation is Write Gate.

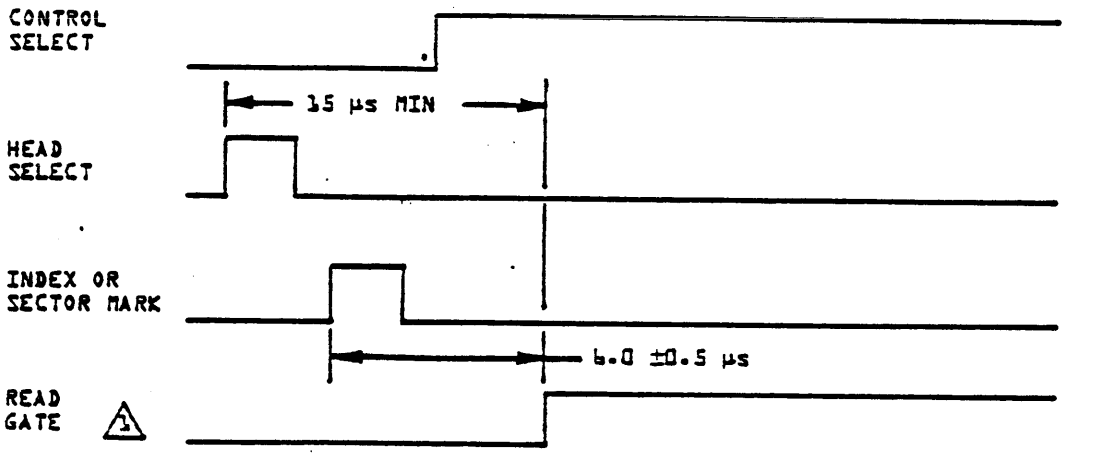
The sector address must always be read and verified prior to writing the data field, except while formatting.

Writing the data field must always be preceded by writing the PLO sync field and sync pattern.

The controller must provide a three bit internal delay (approximately 0.3 µs) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal (see Figure 23(B)). This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit.

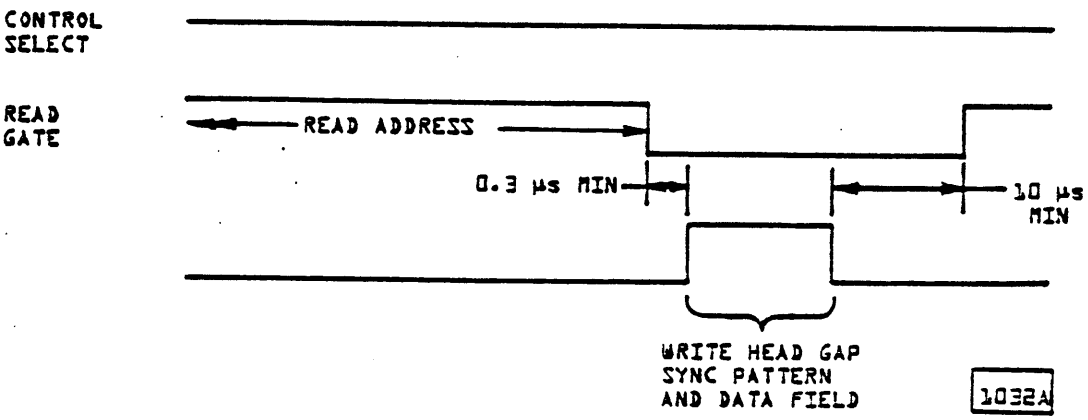
Writing the data field must always be followed by writing the checkword and at least an eight bit pad at the end of the checkword.

During formatting, Write Gate is raised immediately upon sensing Index or Sector. During a record update, Write Gate is raised within two bits of the last bit of an address.



1 IF A READ OPERATION IS TO BE PERFORMED AFTER INDEX OR SECTOR, READ GATE MUST NOT OCCUR LATER THAN 6.0 ±0.5 µs AFTER THE LEADING EDGE OF INDEX OR SECTOR.

A. TYPICAL READ CONTROL TIMING



B. TYPICAL WRITE CONTROL TIMING

FIGURE 23. CONTROL TIMING

7.0 CONTROLS AND INDICATORS

7.1 Operator Panel

The unit contains a front panel with a logic plug, a start/stop switch/indicator, a fault/clear switch/indicator, and a write protect switch/indicator.

NAME	TYPE		FUNCTION
	LIGHT	SW	
LOGIC PLUG (REMOVABLE)		X	Establishes Logical Address of the device.
START/STOP	X	X	Indicator is on when the drive is Ready. Indicator blinks when START is activated until drive is Ready. Indicator blinks when STOP is depressed until disk rotation is stopped.
FAULT/CLEAR	X	X	Indicates any Fault condition. The switch clears the Fault condition if that Fault no longer is present.
WRITE PROTECT	X	X	Indicator is on when the Drive's write circuits are disabled. Write Protect is activated by a switch located in the logic assembly or on the front panel.

7.2 Control Board Switch and Indicators

NAME	TYPE		FUNCTION
	LIGHT	SW	
WRITE	X		Indicates that a Write fault had occurred.
WRITE AND READ	X		Indicates write and read conditions existed simultaneously.
WRITE OR READ AND OFF CYL	X		Indicates write or read conditions existed during a seek operation (off cylinder).
VOLTAGE	X		Indicates a below normal voltage had existed.
MPU/FIRST SEEK FAULT	X		Indicates drive failed first seek/load attempt.
WRITE PROTECT		X	Enables write protection circuitry.

The indicators listed above are located on the control card in the logic chassis and are visible thru a hole in the top cover. See 6.2.2.2.

7.3 Channel Select and Reserve Switches and Indicators (Dual Channel Only)

NAME	TYPE		FUNCTION
	LIGHT	SW	
DI/NRM		X	Switch will disable Channel I or allow Channel I to be selected.
DII/NRM		X	Switch will disable Channel II or allow Channel II to be selected.
ABR/RTM		X	In ABR position once drive is selected it must be released in order for Reserve to drop. In RTM position once drive is deselected, Reserve will drop after 500 ms.
CH. I SEL	X		Indicates Channel I is selected.
CH I RES	X		Indicates Channel I is reserved
CH. II SEL	X		Indicates Channel II is selected.
CH. II RES	X		Indicates Channel II is reserved.

8.0 PHYSICAL SPECIFICATIONS

Nominal dimensions of the FSD Drive and Power Supply are shown on the plan view of Figure 2.

The drive weight is approximately 60 lbs.

The power supply weight is approximately 12 lbs.

9.0 RELIABILITY AND SERVICE GOALS

9.1 Mean Time Between Failure

Following an initial period of 200 hours, the Mean Time Between Failure exceeds 7,000 hours for units manufactured in the first year of production and 9,000 hours for units manufactured in the second year. For units manufactured after the second year, the MTBF exceeds 10,000 hours. The following expression defines MTBF:

$$\text{MTBF} = \frac{\text{Estimated Operating Hours}}{\text{No. of Equipment Failures}}$$

Operating hours means total hours less any maintenance time. Equipment failures mean any stoppage or substandard performance of the equipment because of equipment malfunction, excluding stoppages or substandard performance caused by operator error, adverse environment, power failure, controller failure, cable failure, or other failure not caused by the equipment. To establish a meaningful MTBF, operating hours must be statistically significant and must include field performance data from all field sites.

For the purpose of this specification, equipment failures are defined as those failures necessitating repairs, adjustments or replacements on an unscheduled basis. Essentially, the term equipment failure implies that emergency maintenance is required because of hardware failure or substandard performance.

9.2 Mean Time to Repair

The mean time to repair does not exceed 1.0 hours; it is defined as the time for an adequately trained and competent serviceman to diagnose and correct a malfunction.

9.3 Preventive Maintenance Time

No scheduled maintenance is required other than coarse filter cleaning by the operator.

9.4 Service Life

The FSD Drive is designed and constructed to provide a useful life of five years before factory overhaul or replacement is required. Repair or replacement of major parts will be permitted during the lifetime.

10.0 INSTALLATION AND MAINTENANCE

Required connections to the device are power (dependent upon variation selected), signal cables and a system ground consistent with CDC STD 1.30.023. The only physical requirement is adequate clearances for maintenance and air intake/exhaust. Detailed instructions are found in the equipment maintenance manuals.

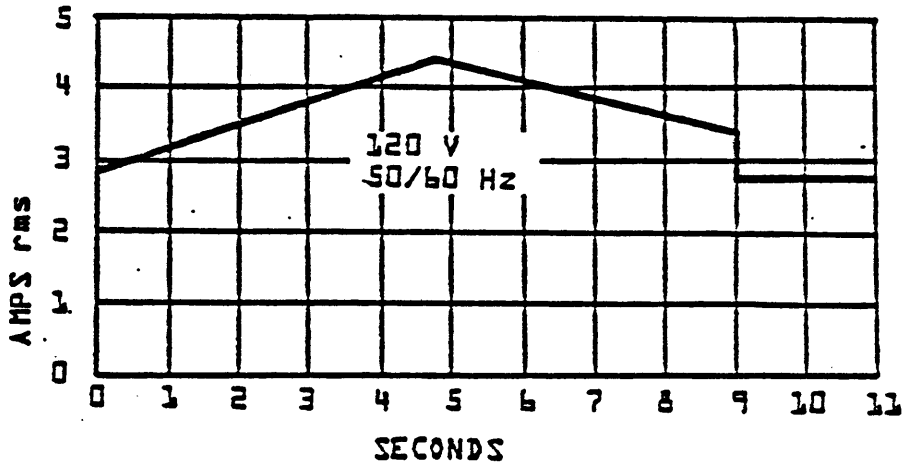
10.1 Power Requirements

10.1.1 Primary Power Requirements

The typical primary voltage, frequency, and power requirements are shown in Table 4. Start up current is shown in Figure 24.

TABLE 4. PRIMARY FREQUENCY, VOLTAGE, AND POWER REQUIREMENTS

FREQUENCY			VOLTAGE			DISKS AND CARRIAGE IN MOTION			
						LINE CURRENT	ENERGY CONSUMPTION	HEAT DISSIPATION	POWER FACTOR
NOM	MAX	MIN	NOM	MAX	MIN	AMPS	KW	BTU/H	
60	60.6	59.0	120	128	104	2.8	.244	832	.726
60	60.6	59.0	220	235	191	1.6	.242	825	.687
60	60.6	59.0	240	254	212	1.5	.242	832	.684
50	50.5	49.0	120	128	102	2.8	.244	832	.723
50	50.5	49.0	220	235	191	1.6	.236	805	.688
50	50.5	49.0	240	256	208	1.5	.243	829	.672



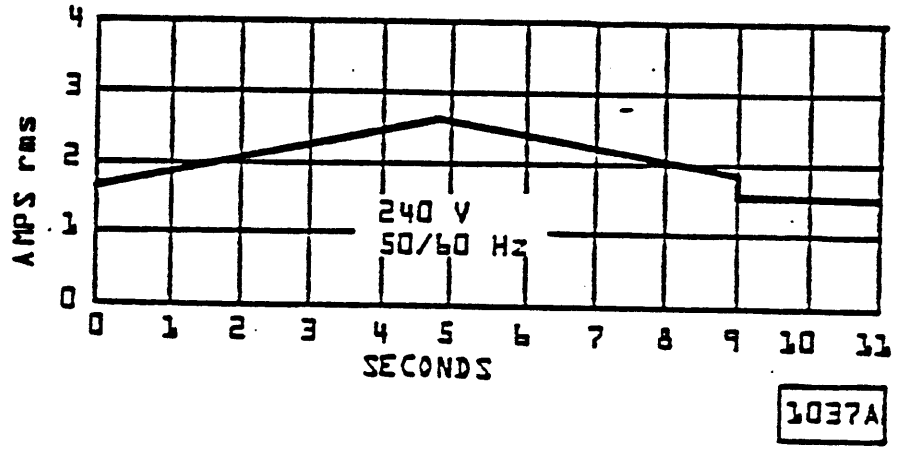
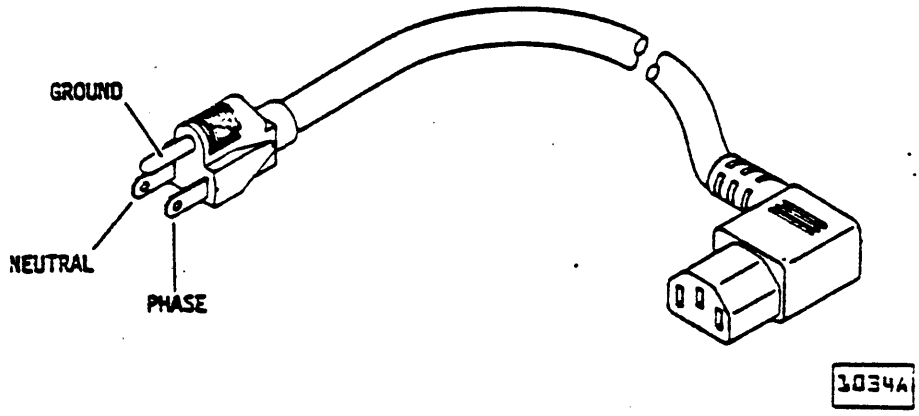


FIGURE 24. LINE CURRENT VERSUS START-UP TIME

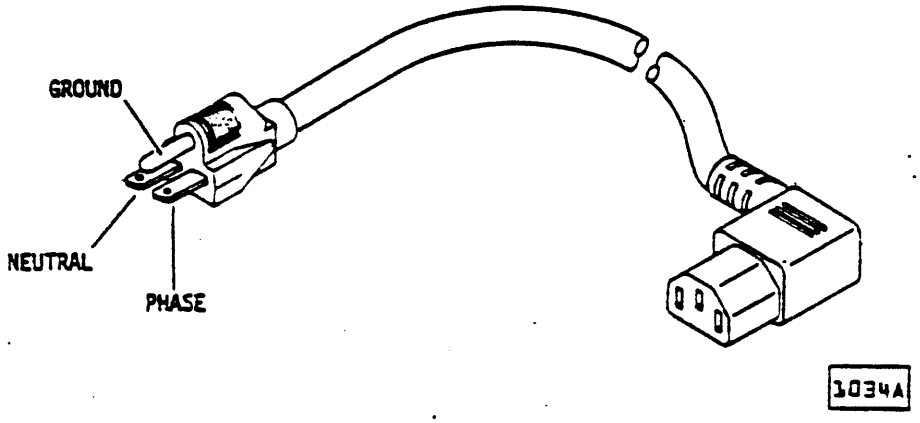
10.1.2 AC Power Connector

10.1.2.1 60 Hz

A connector/cord assembly is furnished with each 60 Hz FSD drive in the configuration of Figure 25.



A. 120 V POWER CORD



B. 220 V, 240 V POWER CORD

FIGURE 25. 60 HZ POWER CONNECTORS

10.1.2.2 50 Hz

A connector/cord assembly is furnished with each 50 Hz FSD drive in the configuration of Figure 24.

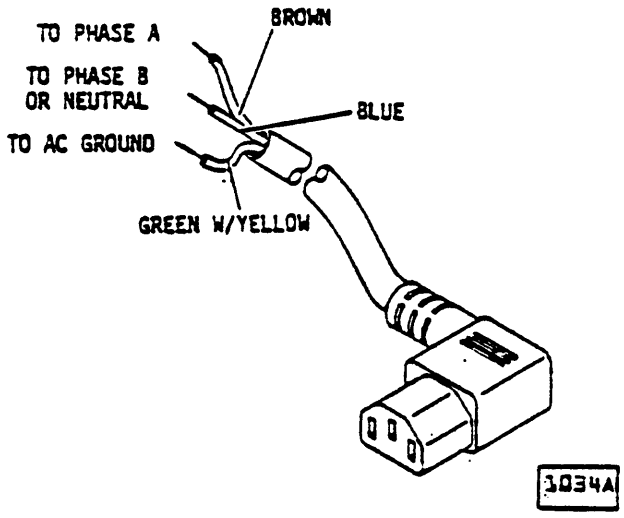


FIGURE 24. 50 HZ POWER CONNECTOR

10.2 Grounding

Installation requirements are ac power grounding, and signal cable connections to the Drive. Since the drive is isolated from ac ground, a ground strap must be connected between the dc grounds of the controller and Drives. The drive Power Supply will be connected to frame (ac) ground. Detailed instructions are in Volume 1 of the hardware maintenance manual.

10.3 Environmental Limits

The FSD drive will comply with VDE and FCC Class A emissions when mounted in an appropriate cabinet representative of end use.

Compliance to VDE and FCC will be demonstrated by testing in a cabinet similar to Figure 27. Appropriate shielded I/O cables, (see Table 1) and a means to terminate the I/O cable shield at the entrance into the cabinet are required. A power distribution box in the cabinet is optional but not required.

ENVIRONMENT	STORAGE	TRANSIT	OPERATING IN AN OFFICE ENVIRONMENT
TEMPERATURE	For 90 days max 14°F to 122°F -10°C to 50°C Max change: 27°F per hour 15°C per hour	For 7 days max -40°F to 140°F -40°C to 60°C Max change: 36°F per hour 20°C per hour	 50°F to 114°F 10°C to 45°C Max change: 18°F per hour 10°C per hour Gradient: 18°F, 10°C
HUMIDITY	10% to 90% relative For 90 days max	5% to 95% relative For 7 days max	20% to 80% relative Max change: 10% per hour
BAROMETRIC PRESSURE	105 kPa to 74 kPa (-300 m to 2500 m) (-983 ft to 8200 ft)	105 kPa to 74 kPa (-300 m to 2500 m) (-983 ft to 8200 ft)	105 kPa to 79.5 kPa (-300 m to 2000 m) (-983 ft to 6560 ft)

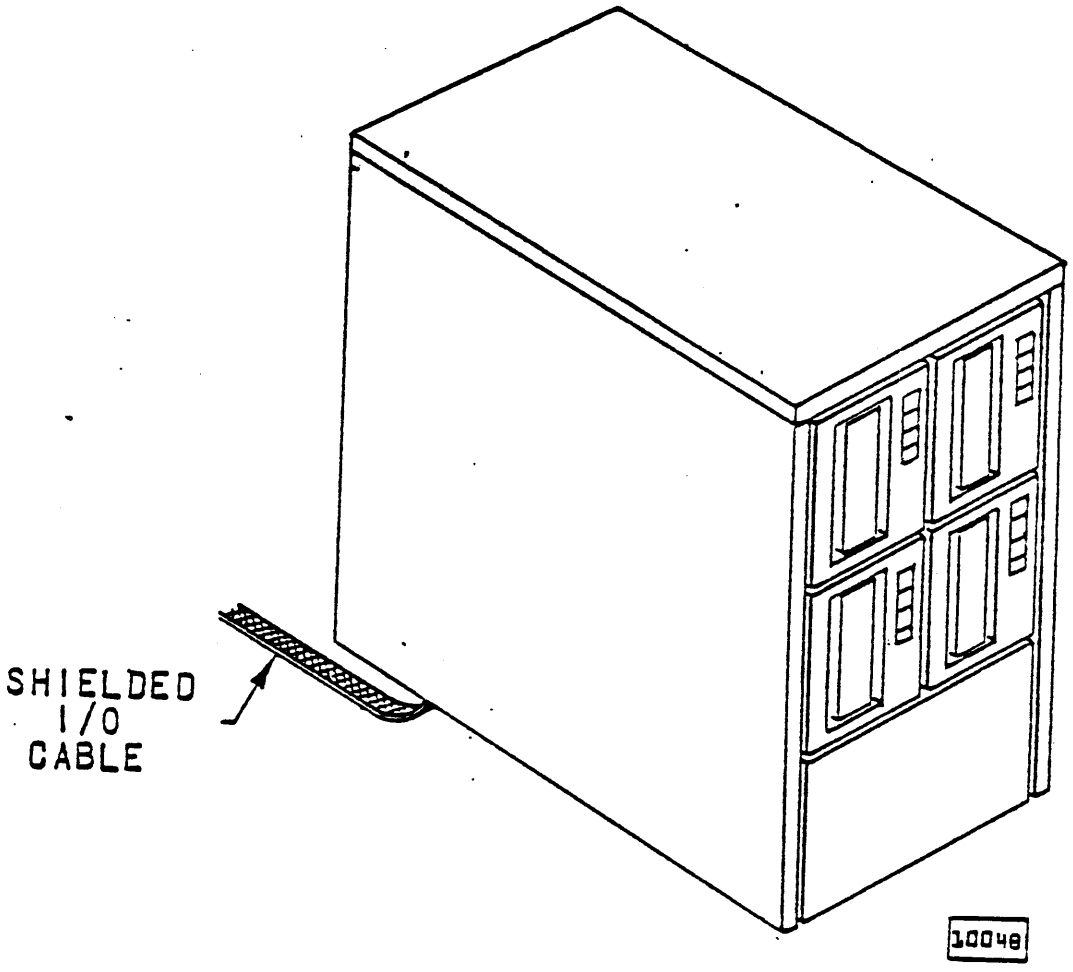


FIGURE 27. TYPICAL CABINET CONFIGURATION

10.4 Air Flow

The enclosure must provide an exhaust opening for the fan air flow across the electronics, motor, and power supply.

An open inlet and exhaust area of 30 sq. inches for each module can be used as a nominal design figure for the enclosure. The ideal location for the exhaust opening is a rear position on the top panel, the second choice would be a top position on the rear panel. The openings, especially if on the top panel, should be louvered, baffled or screened to prevent debris from being dropped into the unit.

An open bottom on the enclosure which allows air to enter around the base and be exhausted at the top of the cabinet will promote a natural air flow through the cabinet which will aid the air flow from the fan.