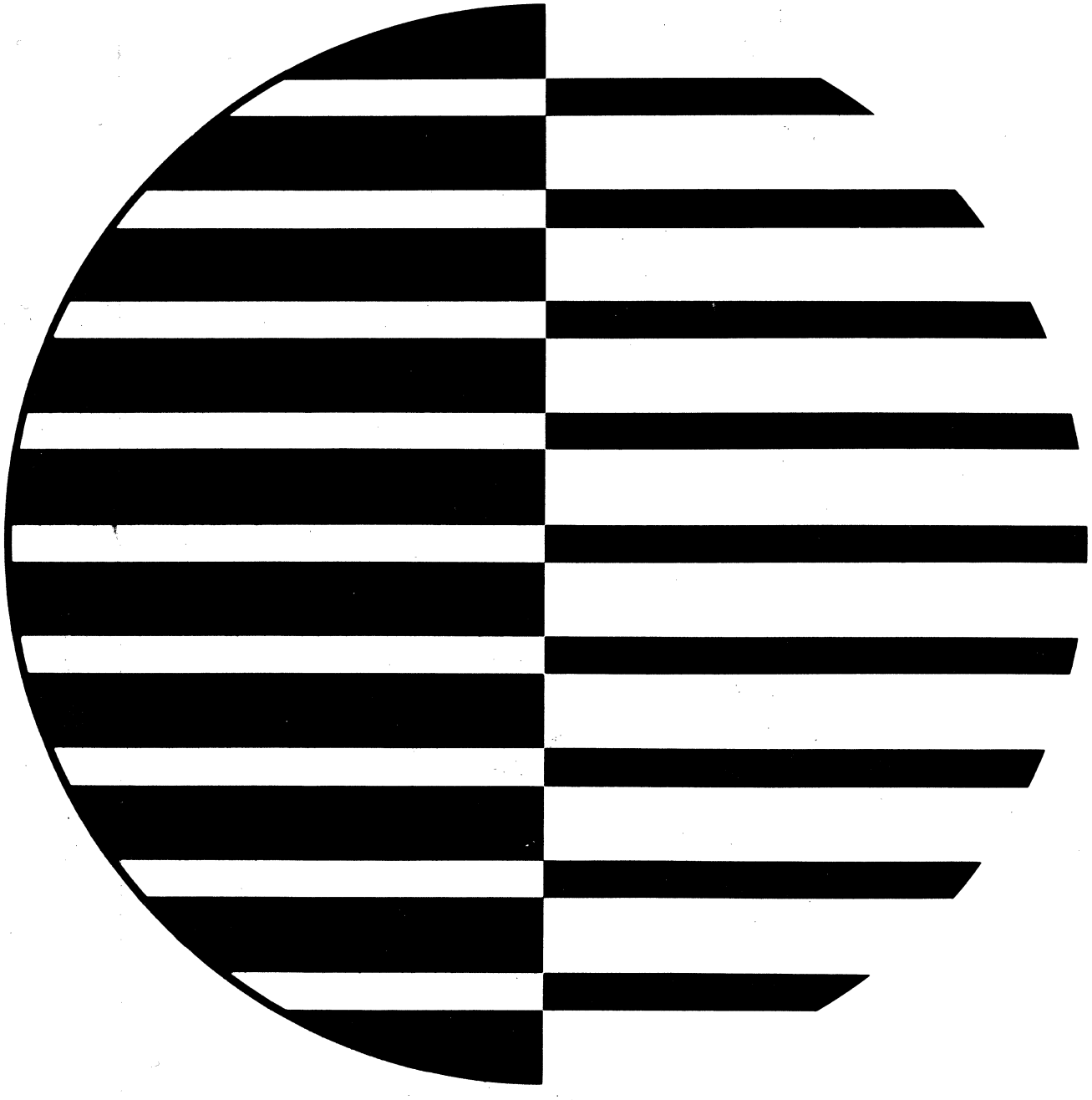
CONTROL DATA INSTITUT

CONTROL DATA



LOGIC DIAGRAMS

Magnetbandeinheiten

Control delays may have multiple inputs and/or multiple outputs. When a control delay has multiple output terms (i.e., more than one V, Y, or N term), each output term may have a separate conditioning input.

Capacitive Delays

A capacitive delay is used to delay the "1" input to a logic element. ("0" inputs are not affected by the delay.) Capacitive delays may be active or passive, depending upon whether or not transistors are used as part of the delaying circuit. Delay periods are checked by using a dual-trace scope connected to the input and output of the delay producing element. The actual connection points for the scope and probes vary for different cards and should be determined by referring to the Printed Circuit Manual.

Active delays may be recognized by the circuit letter always present as part of the card location. Pin numbers are also shown when external wiring is needed to connect the proper capacitance. In Figure 9, the pluggable delay uses this wiring to connect to capacitors on the same card. In the third example, this wiring connects to capacitors located on two separate capacitor cards.

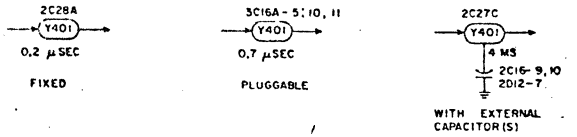


Figure 9. Active Capacitive Delays

All passive capacitive delays (Figure 10) are formed by wiring grounded capacitors, located on one or more capacitor cards, as an AND input to the affected logic element. For this reason, all passive delays show pin numbers to provide this external wiring data.

Figure 10. Passive Capacitive Delays

Capacitive delays may be adjustable or nonadjustable, depending on the card type and/or the external wiring connections on the card. When it is necessary to adjust the delay period in order to obtain specified circuit operation (usually done by varying a potentiometer in the RC network), a diagonal arrow is added to the delay symbol as shown in Figure 11.

Figure 11. Adjustable Capacitive Delays

Inductive Delays

An inductive delay is used to delay either the "1" or "0" input to a logic element or as a tapped delay line for timing of operations. The symbol for this delay is an elongated oval with a double vertical line just within the input end of the oval. When used as a tapped delay line, the inductive delay is terminated in its characteristic impedance. Inductive delays are identified in the same manner as capacitive delays (except for the vertical lines) unless they are used as delay lines. On multi-section cards where no identifying circuit letters are present, pin numbers are shown adjacent to the input and output arrows. Figure 12 shows both kinds of inductive delays.

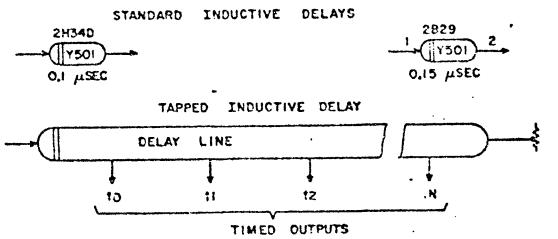


Figure 12. Inductive Delays

Line Drivers/Receivers

Voltage levels used to represent "1's" and "0's" on cables are different from those used for internal logic. The level shift to and from internal logic is made by line drivers and line receivers. These cards may be considered as inverting the signal electrically, but not logically. The letters commonly associated with these cards are L & M (1604) and R & T (3000 Series). A 3000 Series Receiver may also be used to perform a logical inversion by swapping the twisted pair wires. This usage is indicated by a circle on the input side of the symbol. In Figure 13, "1's" and "0's" have been added to clarify the logic states; they are not part of the symbol.

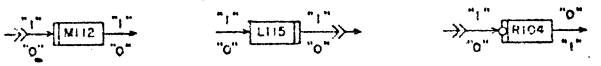


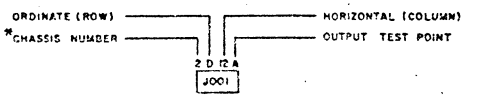
Figure 13. Typical Line Driver/Receiver Symbols

NON-LOGIC CONVENTION

The use of the double vertical bar, as shown in Figure 13, denotes a shift in signal voltage level from that used in internal logic. The double bar appears on the input or output side of the symbol, depending on which side connects to the non-logic-level signal. No particular voltage level is implied by the double bar - only that it is non-logic.

JACK ASSIGNMENTS

Each numbered term in the logic diagrams contains a jack assignment showing the physical location of that hardware element and the test point (circuit section) associated with it. For some card types, the test point letter is replaced by a pin number. For these cases, a card extender must be used in order to test that section of the card. Also, some symbols show no test point. This is because the entire card is used for one purpose (e.g. a single inverter, FF, or control delay). Figure 14 illustrates the inverter J001, with 2D12A representing its jack assignment.



*When most or all jack assignments are located on one chassis, the chassis numbers for that chassis are omitted. All multi-chassis devices include a chassis number as part of each jack assignment.

Figure 14. Jack Assignment Scheme

CABLE IDENTIFICATION

Cable connections are represented by the MIL-STD-15 symbol and identified as to connector location and pins used, as shown in Figure 15.

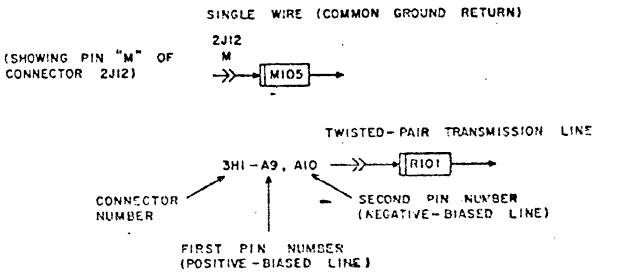


Figure 15. Cable Connections

SPECIAL LOGIC SYMBOLS

Nonstandard elements (special logic and/or non-logic elements) are represented by a special circuit symbol (generally a rectangle as shown in Figure 16). The special circuit symbol always shows the symbol designation, jack location, and the card type. Supplemental information may also be shown such as in the case of special delay cards which indicate the delay period. For detailed information refer to the specific card type in the appropriate Printed Circuit or Logic Module Manual.

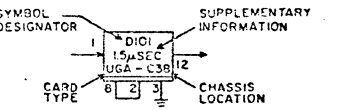


Figure 16. Symbol for Special Circuits

INPUT/OUTPUT DESIGNATIONS

Where several pages of logic are involved, a symbol index and term list (side cars) are incorporated within the manual. Also in certain instances such as special card types or on equipments for which no equation summary exists (as for peripheral devices) input and output pin numbers are indicated on each logic element as are the output destinations of the elements (Figure 17).

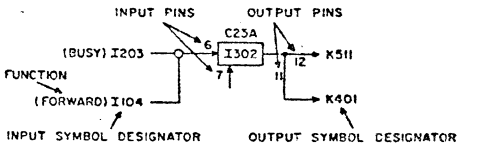


Figure 17. Input/Output Designations

SYMBOL INDEX

SYMBOL INDEX

READ DATA

The seven read data circuits detect, convert, and route information from the tape to the external equipment.

During a read operation, tape data are detected by the read heads, amplified by preamplifier cards, and rectified and detected by level and peak detectors. The information bits are then placed in rank I of the 7-bit Read register. The lower order six tracks of the register receive the information character; the highest order track receives the parity bit. After the information is placed in rank I, the bits are delayed to compensate for electrical and mechanical skewing. They are then gated to ranks II and III. The information remains in rank II from 4 to 12 μsec (depending upon read density) before it is cleared in coincidence with the leading edge of the sprocket pulse from the read gate circuit. Information is sampled by the TCU during the 2 μsec sprocket pulse. Rank III is cleared by the trailing edge of the 2 μsec sprocket pulse.

LEVEL SHIFT NETWORK

The level shift network is an emitter follower with a variable output attenuator. A 2.8 vdc bias is supplied to the base by a zener voltage regulator in the read preamplifier. By adjusting the output resistance, the output level is controlled. The reduced level is supplied to the read level detector to set the bias (and consequently the sensitivity) of the read level detector. If the bias is lower than the detected bits, the bit is coupled; if not, the bit is blocked. Random noise is excluded by reducing the level detector sensitivity.

READ GATE

The read gate circuit controls the coupling of information through the read data circuit to the output lines.

The delay of bits in rank II is determined by the density selected and whether a read or write operation is being performed. These delays are the following:

800 bpi - 4.0 μs (read) 2.8 μs (write)
556 bpi - 5.8 μs (read) 4.0 μs (write)
200 bpi - 12.0 μs (read) 5.8 μs (write)

The delays are controlled by the inputs to delay card Y527. After Y527 times out, its output changes to "0" for 0.1 μsec. This causes the Sprocket FF to be set while rank II is cleared. Setting the Sprocket FF sends a sprocket signal to the TCU indicating that information is on the output lines. After a 2 μsec delay (Y547), the FF is cleared, clearing rank III.

If neither a read nor a write operation is selected, the "1" output from Y531 results in a continuous "1" output from I508 and I511. Rank II of the read register is held in the clear state and a read operation is disabled. When a read or write operation is initially selected, I508 and I511 continue to produce a "1" output to hold rank II cleared for 2 msec. (because of the Y543 delay). This precaution eliminates the possibility of transient noises being read as information while tape is brought up to speed.

L O G I C D I A G R A M S

Magnetbandgerät CDC 607

Controller CDC 3228

Herausgeber: Control Data Institut Frankfurt/M.
Control Data GmbH Frankfurt/M. 1976

DEVELOPED & PRINTED BY CDI FRANKFURT

Printed in Germany

CDI-CT-PHIV-19-02/65

INHALTSVERZEICHNIS

KEY TO LOGIC SYMBOLS

(STANDARD 1604 OR 3600 CARD TYPES)

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In CONTROL DATA® Corporation logic, two signals, a logical "0" and a logical "1", are the possible input or output conditions of a circuit. A circuit with an output of "1" is "up" and a circuit with an output of "0" is "down". Detailed descriptions of logic symbols and their associated building block circuit cards are contained in the Printed Circuit Manual (Pub. No. 60042900, Vols. 1 and 2).

STANDARD LOGIC SYMBOLS

Standard logic diagram symbols for Control Data equipment using 1604- or 3600-type cards are inverters, flip-flops, control delays, and capacitive and inductive delays.

Inverters

An inverter is a logic element which provides an output that is an inversion of its input. When more than one input is provided to an inverter, "1's" take precedence over "0's" and drive the output of the inverter to "0". Because any "1" input of several inputs drives the output to a "0", an inverter may be considered an inverting OR (or NOR) gate when more than one input is present.

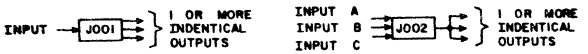


Figure 1. Inverter Symbols

Acceptable conventions for showing multiple OR inputs are given in Figure 2.

Figure 2. OR Circuit Conventions

Flip-Flops (FF)

The flip-flop (FF) is a storage device with two stable states - designated as Set and Clear - and is composed of two or more inverters. The logic symbols (Figure 3) are formed by the combination of inverter symbols. By convention, Set inputs and outputs are shown in the upper part of the symbol and Clear inputs and outputs are shown in the lower part of the symbol.

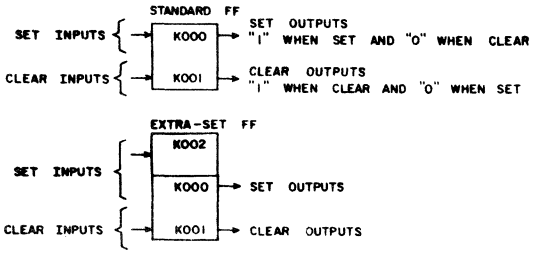


Figure 3. Flip-Flop Symbols

Figure 4 illustrates the interconnection of inverter symbols to form a flip-flop symbol. The term numbers assigned to each flip-flop are the term numbers of the internal inverters as seen by comparing the terms in Figure 3 with those in Figure 4. Notice that the Set output is the output of inverter K001, and the Clear output is the output of inverters K000 and K002.

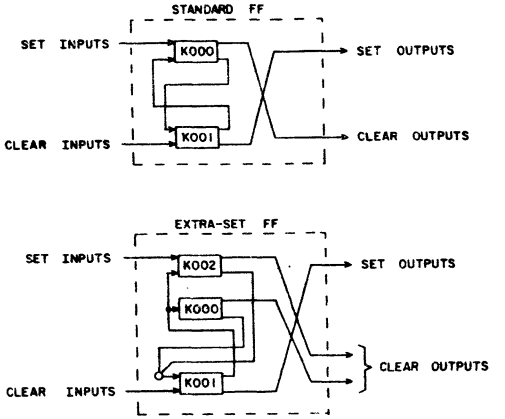


Figure 4. Internal Inverter Connections for a Flip-Flop

AND Gate

An AND gate requires that all its inputs be "1's" in order that its output be a "1". If one or more of the inputs to an AND gate are "0", the output is a "0". Figure 5 illustrates conventions for showing AND gates feeding an inverter.

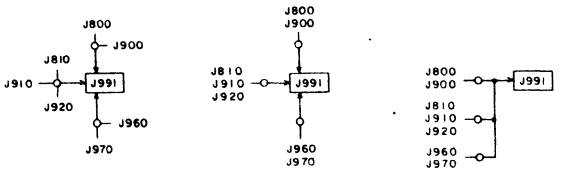


Figure 5. AND Circuit Conventions

Control Delay

A control delay is a timing device consisting of an H term which receives the input and one or more V, Y, or N terms to provide the outputs. The H term is essentially a flip-flop with controlled feedback and occupies an entire printed circuit card. The output term(s) are inverter(s) located elsewhere on the logic chassis. The "1" outputs from a control delay are clocked pulses which are delayed one phase time from the "1" inputs. Clock inputs are not shown on the logic diagrams for any H, V, Y, or N terms; these terms, which control the start and duration of the delayed output pulses, may be found in the Equation Summary. Figure 6 illustrates two representative forms of the control delay symbol, with possible inputs and outputs labelled. Figure 7 shows the electrical connections for the two forms.

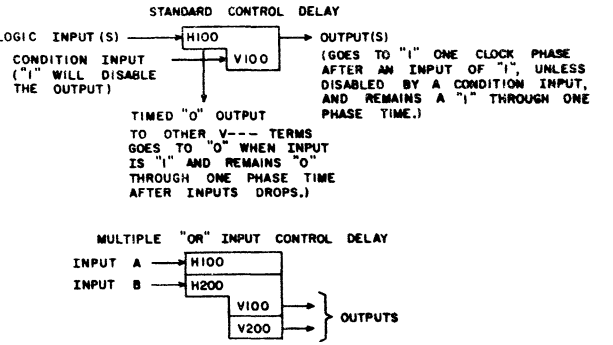


Figure 6. Control Delay Symbols

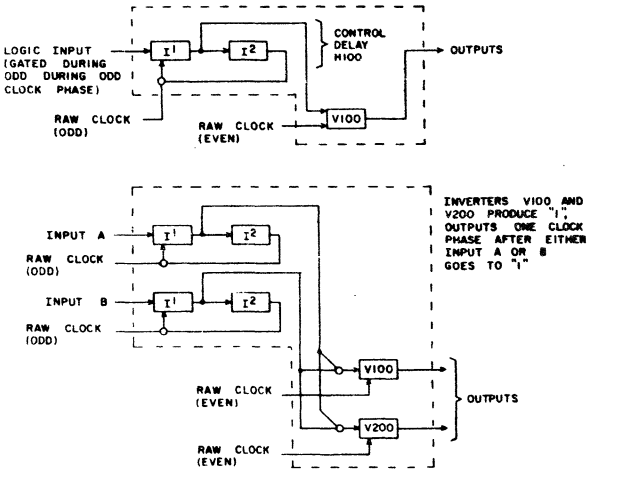


Figure 7. Electrical Connections for Control Delay

R

Rang 1

100ns nachdem

Rang 2 gesetzt

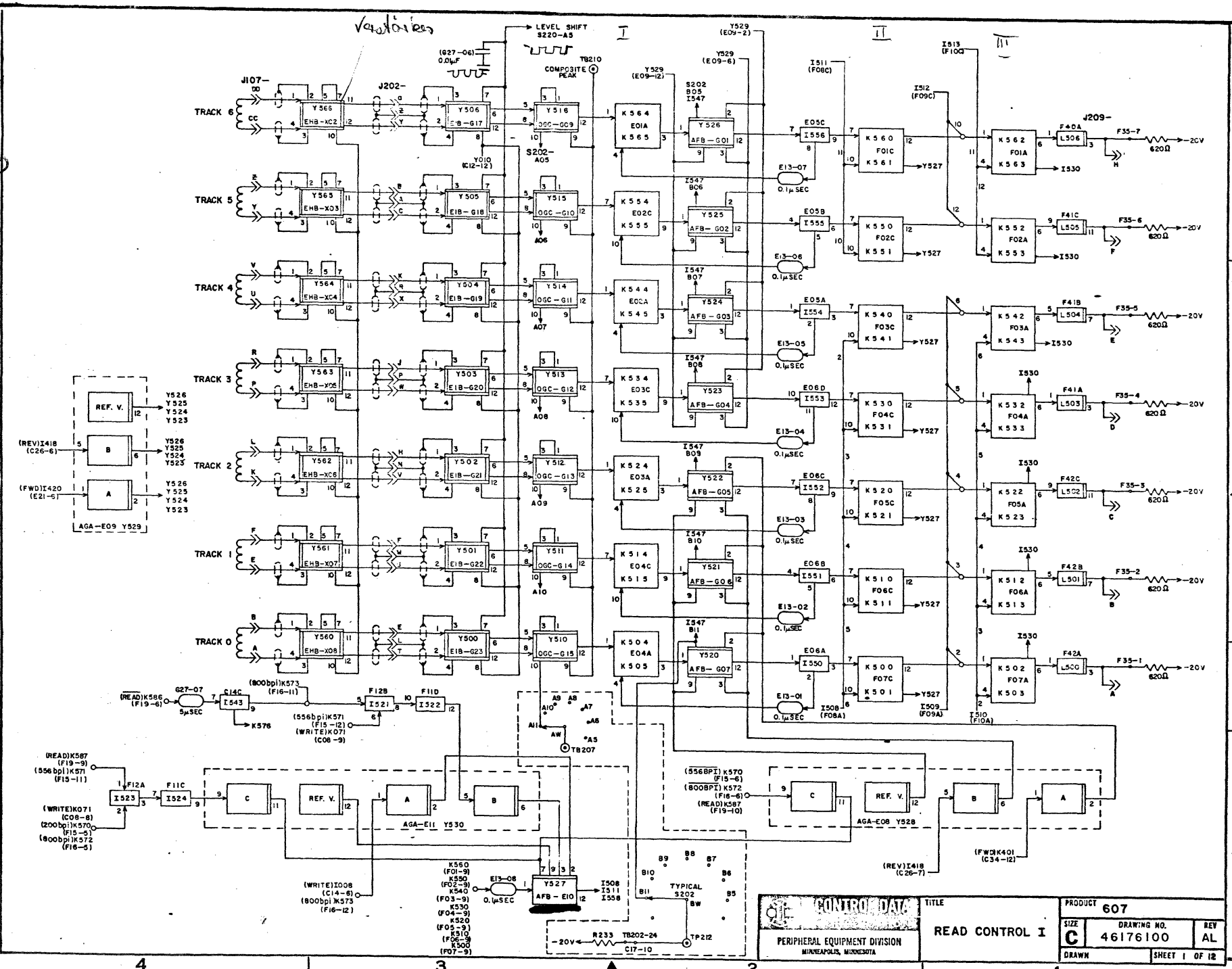
Rang 2 4 µs

bei 800 BPI READ

Rank 3 7.8 µs

(800 BPI WRITE)

Rang 1 100ns nach



FILE MARK STOP

The file mark stop circuit controls the stopping of tape during a read operation. It also notifies the TCU when a complete record has been read, or a file mark (octal 17) or load point has been detected.

If the TCU has not selected a stop on file mark, the circuit will supply an end of operation pulse under the following conditions:

1. End of record. End of record occurs if new information is not loaded into rank II of the read register within 200 microseconds after rank II was cleared. After the 200-microsecond delay, a 10 μsec end of operation pulse is sent to TCU. At the end of the 10-microsecond pulse, the motion flip flop is cleared to stop tape.
2. Load point marker detected.
3. File mark is detected. The circuit supplies both a file mark pulse and an end of record pulse. Motion stops.

If the TCU selects stop on file mark, motion stops only if a file mark or load point marker is detected. An end of operation pulse is not provided between records.

Refer to the file mark stop circuit in the Flow Charts and Timing Diagrams section of the manual for an explanation of circuit operation.

SELECT DENSITY

The select density circuit specifies the rate at which information will be transferred from the TCU. The selection may be made by the TCU or under local control.

Density is a function of the status of flip-flops K570/K571 and K572/K573.

Density	K570/K571	K572/K573
200 bpi	Clear	Clear
556 bpi	Set	Clear
800 bpi	Clear	Set

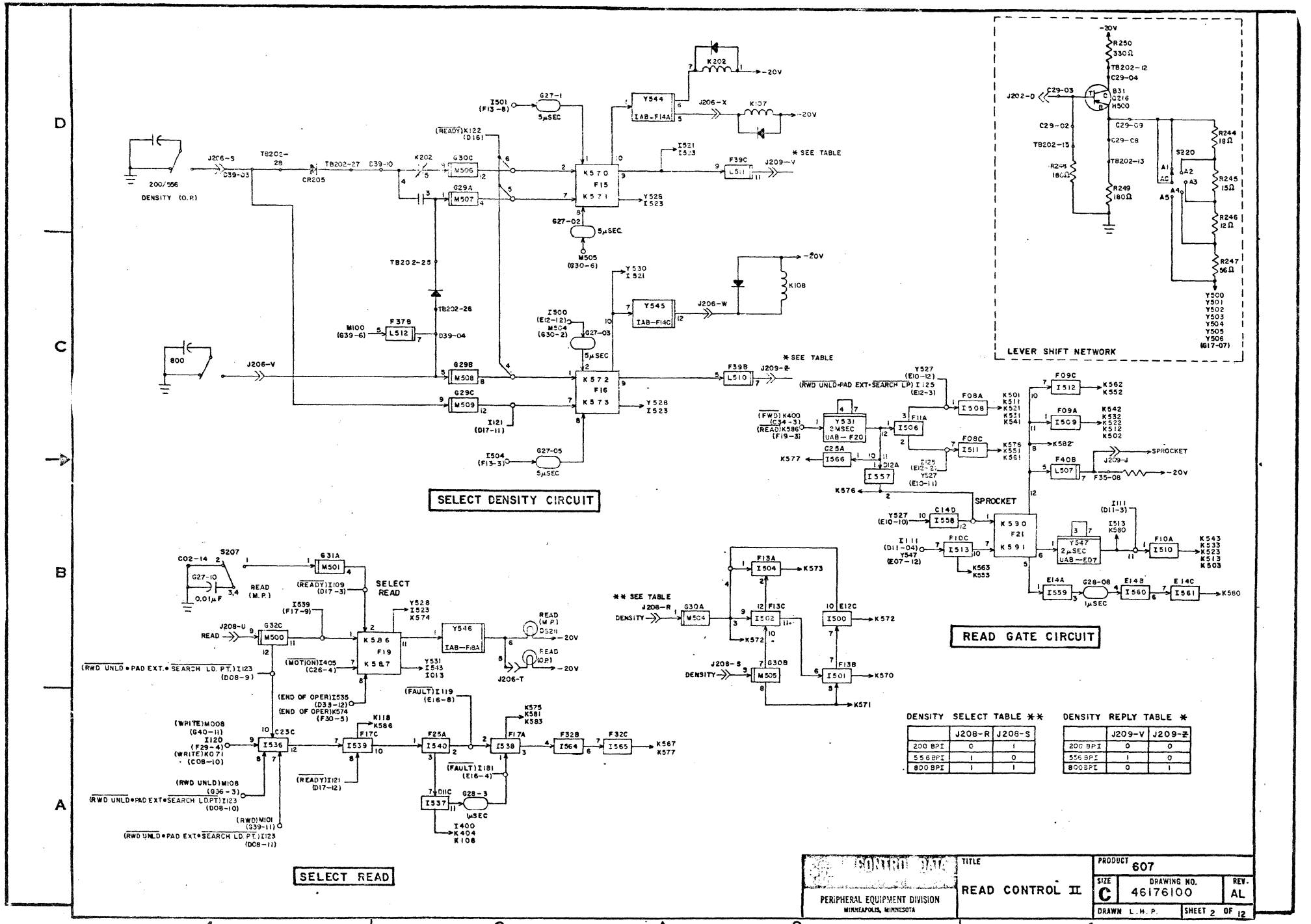
SELECT READ

The select read circuit enables the read circuit and the motion operations either by local selection or by programmed select read. This circuit also provides an indication of the read operation.

When the Select Read FF is cleared, the read operation is disabled by holding read register rank II in the clear condition. A read select signal from the TCU or from the maintenance panel read switch sets the Select Read FF, enabling the read circuit and causing the read indicators to illuminate.

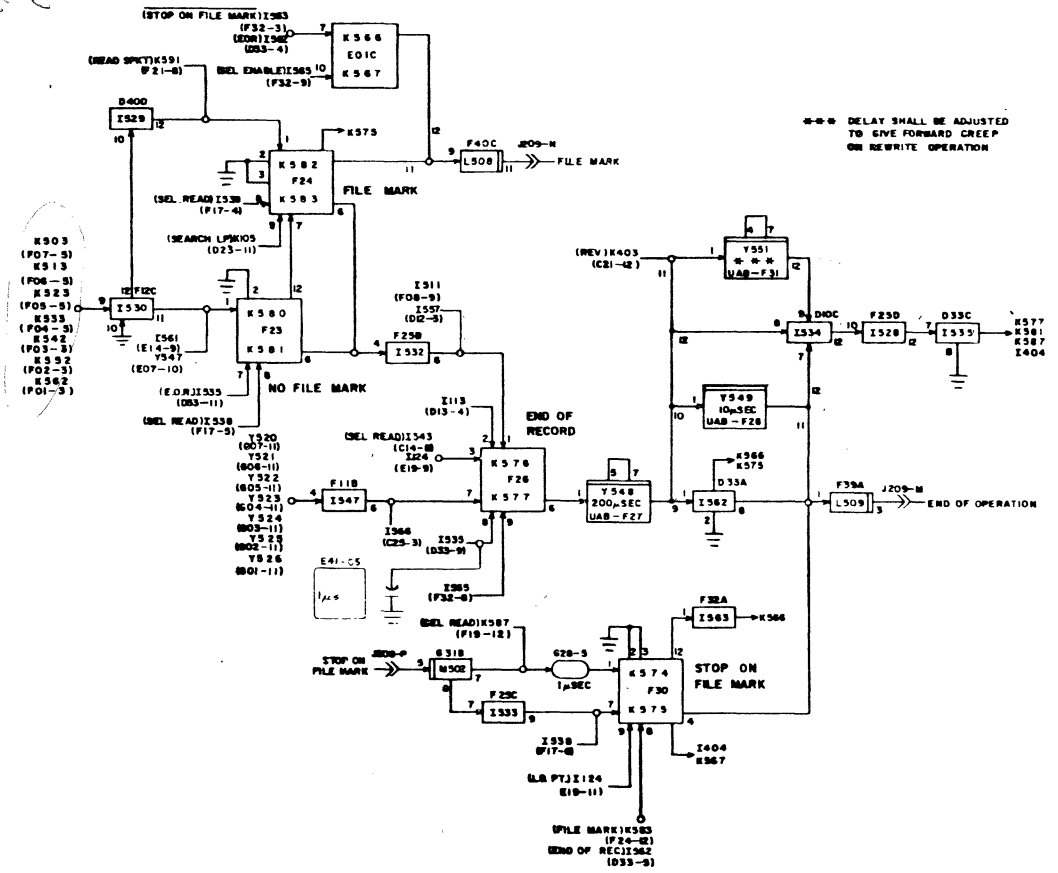
The Select Read FF is cleared when forward or reverse tape motion is terminated or when an end of operation signal is produced by the file mark stop circuit. Consequently, the read operation must be reselected to initiate read.

A forward or reverse motion operation cannot be initiated by the TCU until a read or write operation is selected. Also a rewind or rewind unload operation cannot be initiated until a previously selected rewind or unload operation is completed. However, a rewind or rewind unload operation can be initiated while a read or a write operation is in progress.



DENSITY SELECT TABLE **	J208-R	J208-S
200 BPI	0	1
556 BPI	1	0
800 BPI	1	1

DENSITY REPLY TABLE *	J209-V	J209-Z
200 BPI	0	0
556 BPI	1	0
800 BPI	0	1



FILE MARK STOP CIRCUIT

CONTROL DATA CORPORATION PERIPHERAL EQUIPMENT DIVISION MINNEAPOLIS, MINNESOTA	TITLE READ CONTROL III	PRODUCT 607	
		SIZE C	DRAWING NO. 46176100 REV AN
		DRAWN L H P	SHEET 3 OF 12

46176100

WRITE CONTROL

A write operation is selected only by a write signal from the TCU. Once selected, the Write FF remains set until another operation is selected or a fault occurs. However, before the actual write operation is performed a number of enable conditions must first be satisfied.

The file protect relay puller receives a "1" input (enable) only if the tape is not in the unload condition and the tape supply reel contains a file protect ring (File Protect switch is closed). This enable input produces a ground output of the relay puller which:

1. Returns a write ready signal to the TCU, indicating that the reel contains a file protection ring and is loaded.
2. Pulls in the File Protect switch plunger by means of the File Protect solenoid. Holding the plunger in its retracted position prevents it from scoring the file protect ring during operation.
3. Selects the Write Enable relay which turns on the overhead lights. These lights are turned on only when the file protect ring is installed.

The write command from the TCU enables the write control circuit only when the AND input circuit requirements have been satisfied. If all conditions exist the Write FF is set. This energizes the indicator relay pullers which:

1. Light the Write indicators on the operator and maintenance panels.
2. Allow current to flow through the erase head while applying potential to the write drivers.

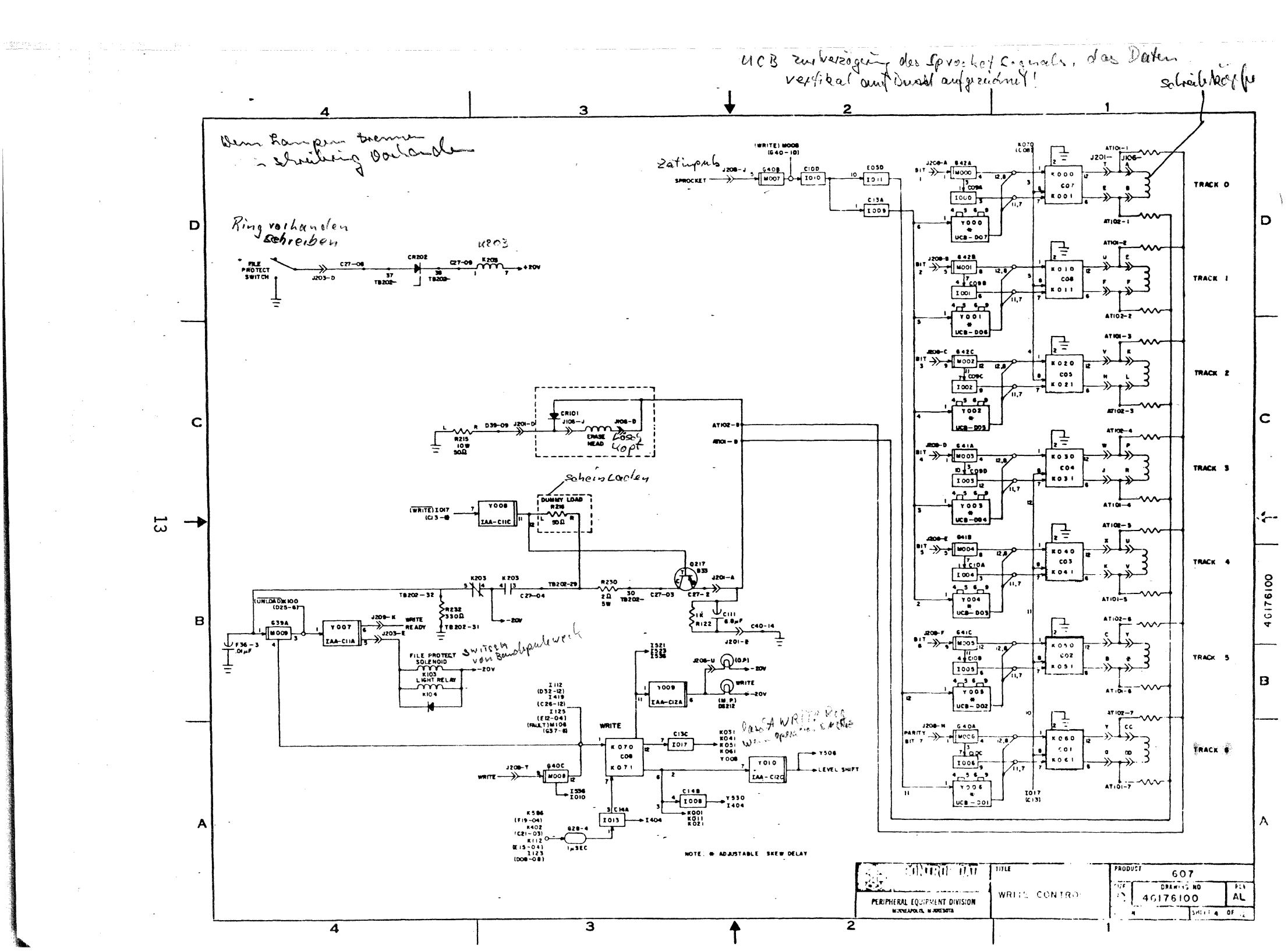
If a write operation is both selected and enabled, the Write FF is in a state which causes flux in the same direction as the erase head. Thus, tape particles are initially aligned in the same direction as they are when tape is erased. This procedure eliminates the possibility of "1" bits being recorded on the tape when a write operation is first selected.

If a write operation is not selected or enabled, the Write FF is cleared. This holds the Write register in a clear state. Erase head current is cut off since the base of Q217 is grounded. During non-write operations, dummy load current flows through the external load resistors. This feature is provided to maintain an approximately constant power supply load both writing and non-writing conditions.

The write data circuits accept information from the TCU in the form of 7-bit characters and route the data via the Write register to the write heads for recording.

A sprocket signal indicates that a 7-bit character is on the input line and may be sampled and routed to the Write register. The presence of a write sprocket signal results in a "1" input to the pulse delay cards. The delay cards are individually adjustable so that each bit can be gated into the register at the time necessary to vertically align all bits on the tape.

The individual Write Register FF changes state each time a "1" is to be written on that particular track: the FF remains unchanged if a "0" is to be recorded. The TCU, in other words, must supply NRZ1 input data to the tape transport.


UCB zur Verzögerung des Sprocket Signals, das Daten vertikal auf Band aufzeichnet!
Schreibköpfe
Beim Lampen trennen - Schreiben Vorlauf
Ring vorhanden Schreiben
+20V
FILE PROTECT SWITCH
WRITE READY
FILE PROTECT SOLENOID
LIGHT RELAY
SWITCH vom Bandspulenwerk
WRITE
LEVEL SHIFT
ERASE HEAD
DUMMY LOAD
TRACK 0
TRACK 1
TRACK 2
TRACK 3
TRACK 4
TRACK 5
TRACK 6
NOTE: * ADJUSTABLE SKEW DELAY
PERIPHERAL EQUIPMENT DIVISION
WRITE CONTRO
PRODUCT 607
DRAWING NO 46176100
REV AL
SHEET 4 OF

MOTION CONTROL

Tape direction is determined by the Forward and Reverse FF's. Because the forward and reverse circuits are similar in design and function, only the forward circuit is discussed.

The Forward FF is set when:

1. Forward operation is selected from TCU.
2. Forward operation is selected by pressing the Forward switch on operator or maintenance panels.
3. It is necessary to search for load point by moving tape forward. This occurs when a rewind operation is terminated or during a load tape operation.

The following actions occur when the Forward FF is set:

1. Forward indicators (MP and OP) are turned on.
2. A 2 msec "0" output is applied to Y402 in the forward capstan drive circuit. This allows 2 amperes current to flow in the new direction for 2 msec to reduce actuation time of the pneumatic valve coil.
3. Set output from the Forward FF is sent to emitter follower (EF) cards in the capstan drive circuit. The capstan drive circuit applies vacuum to the forward capstan. Tape is therefore moved in the forward direction.
4. A busy signal is returned to the TCU indicating that tape motion is in progress. This signal stays up approximately 5 msec after the Motion FF clears (allowing time for tape motion to stop).

The Motion FF's are cleared if any of the following conditions exist:

1. Forward command from TCU is dropped while the write operation is still enabled.
2. Operation is under manual control (not ready), and end of tape is detected while tape is moving forward.
3. Load point is sensed or a fault detected.
4. File mark stop circuit produces a stop signal.

When the Motion FF's are cleared, the Select Read FF is also cleared. Therefore, a new select read signal must accompany or precede every new motion signal from the TCU.

When cleared, the Motion FF's:

1. Turn off Motion indicator on the operator and maintenance panels.
2. Stop tape motion by removing vacuum to capstan and applying vacuum to brake port and motion capstan.
3. Drop busy signal to TCU after a 5 msec delay.

Reverse Read Memory FF K404/K405 is used if the TCU commands a forward read, then reverse read immediately after a high speed rewind. Under these conditions, the reverse capstan may not have slowed sufficiently to drive tape in reverse at the proper speed. The ANDed input to I401 from Y117 in the pad extend circuit prevents the Reverse FF from setting for 1.5 seconds after the Hi Speed FF clears. The output from K404 forces a busy signal return to the TCU to notify it that the transport has accepted the command, even though tape motion has not started yet. After Y117 has timed out, the Reverse FF K402 is set in its normal sequence.

CAPSTAN AND BRAKE CONTROL

These circuits control the venting of vacuum and pressure to the capstans and the brake port.

A forward command causes vacuum to be applied to the forward capstan and pressure to the reverse capstan. A reverse command has the opposite effect. The tape brake is vented to the atmosphere.

Lack of a motion command applies vacuum to the brake port. If forward motion is dropped, a pulse from Y410 applies vacuum to the reverse capstan for 1.5 msec to help reduce stop time. The opposite is true when the Reverse FF is cleared.

SERVO DRIVE CONTROL

The servo drive control circuits monitor and control the length of the tape loop in each of the vacuum columns. The output from this circuit is applied to the reel motor drive circuit, which provides the output power necessary to operate the motors and brakes.

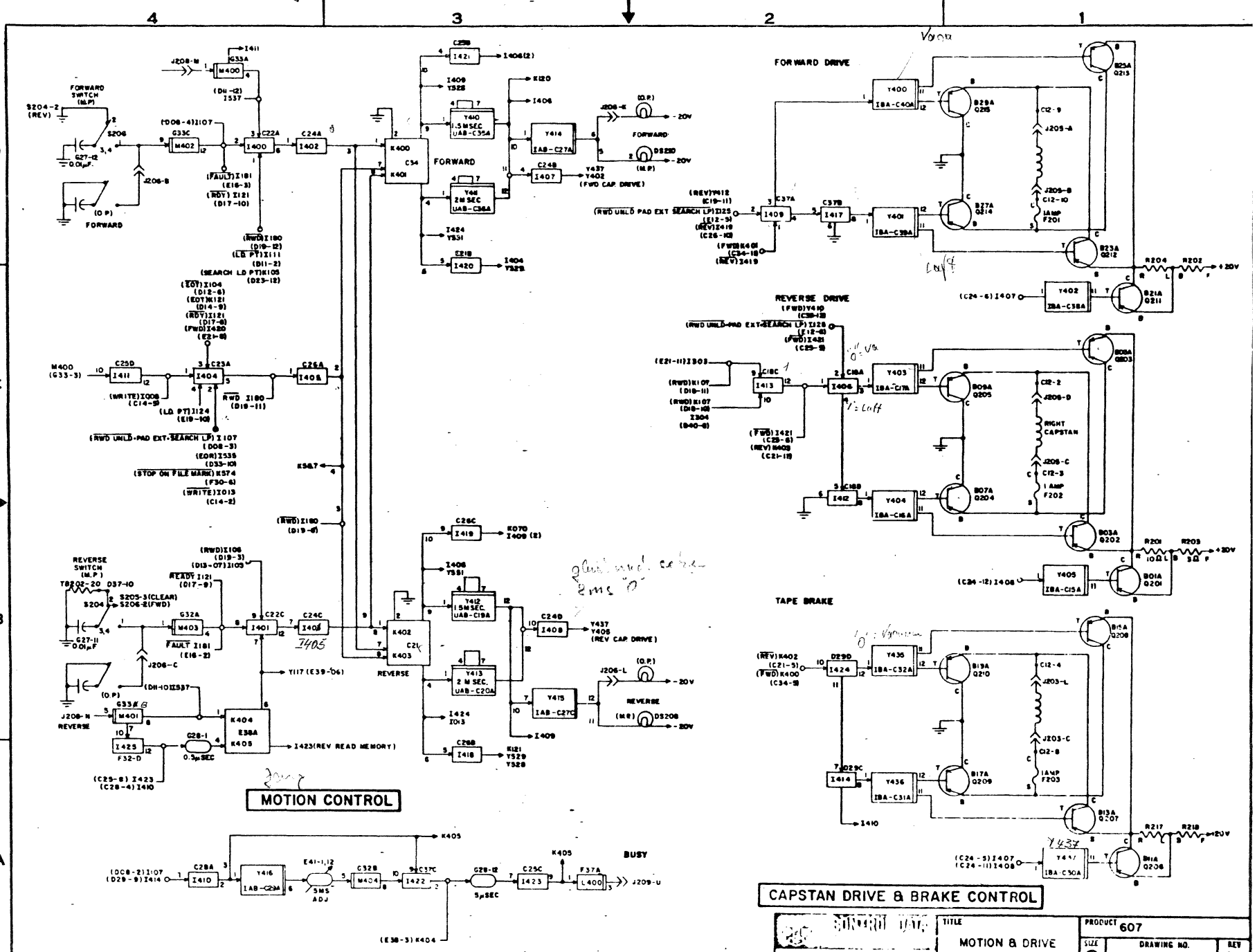
The servo drive control logic is divided into photosense and tachometer circuits.

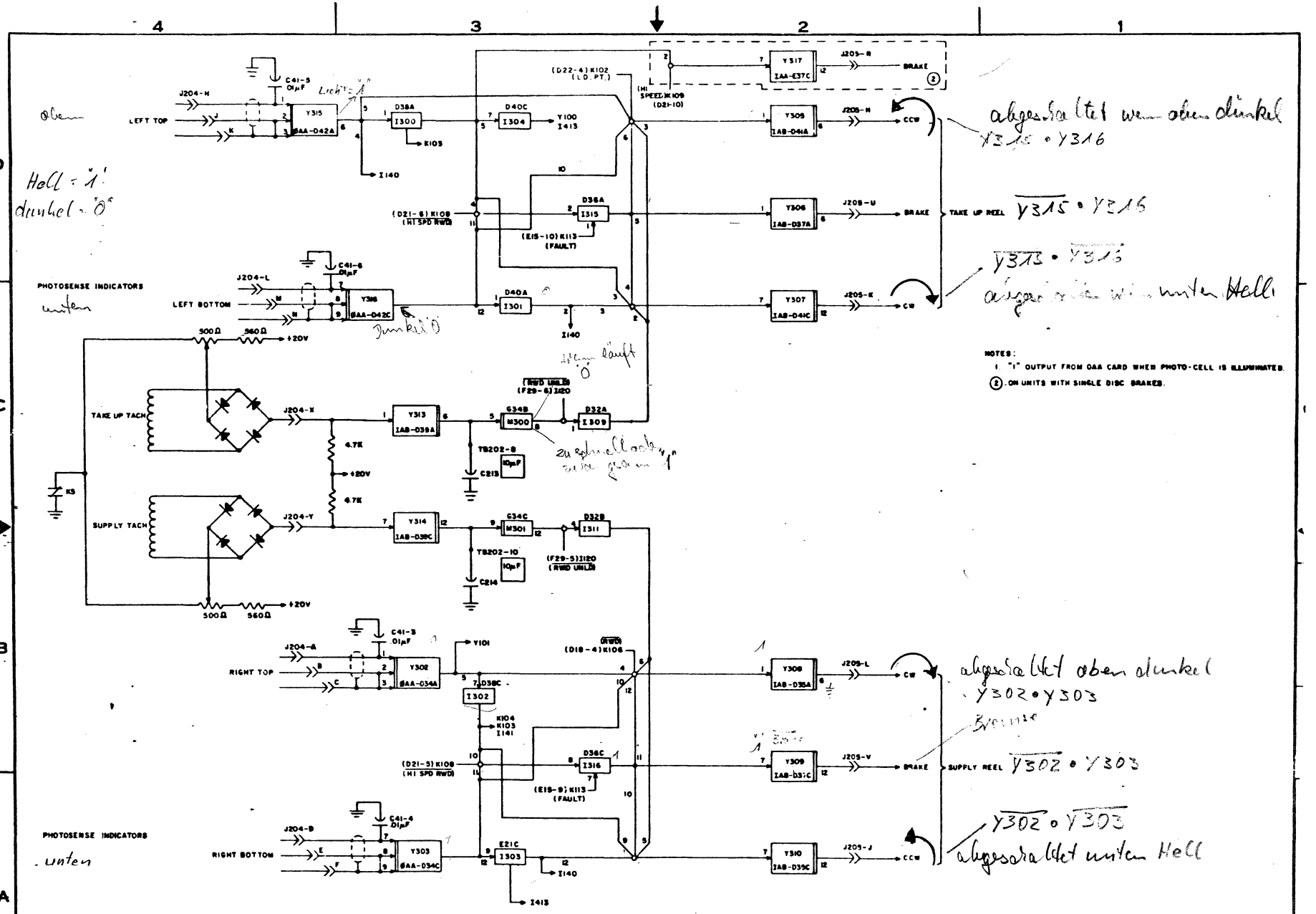
The photosense circuits detect the position of tape in the vacuum storage columns and, based upon this information, specify which reel is to be braked or the direction it is to be driven.

The tachometer circuits compare the tape speed with a preset value. If the tape speed becomes excessive, the tachometer voltage is sufficient to temporarily deenergize the reel drive until the speed returns to normal. These circuits are deactivated during high speed rewind.

Tape Brake Vacuum: Forward à Reverse gelöscht

K400/401 CLR sofort und Luft 2 Forward Capstan u Vakuum 2. Brake Pair gelöscht





CONTROL DATA — PERIPHERAL EQUIPMENT DIVISION	TITLE: REEL DRIVE CONTROL	PRODUCT 607	
		SIZE C	DRAWING NO 46176100
		DRAWN K P	SHEET 6 OF 12

READY

The Ready FF, when set, indicates that the tape is under external control (ready). A not-ready condition (Ready FF cleared) indicates that the tape unit is under manual control and cannot communicate with the TCU.

The Ready FF is set by pressing the Ready switch on the operator panel. When set, the following actions occur:

1. Ready indicators on operator and maintenance panels illuminate.
2. A ready signal is sent to the TCU. This indicates that the tape transport is under control of the TCU and no fault is present. If a power failure occurs, the relay K201 is deenergized, allowing a not ready signal to be sent to the TCU.

The tape transport is returned to the not ready status (Ready FF cleared) at the end of a unload operation. A not ready status also exists when the unit is locally master cleared and when the power is initially turned on. Note that a master clear from the computer does not clear the Ready FF. The ready line to the TCU is disabled whenever a fault occurs.

SENSE END OF TAPE EOT

Detecting the end of tape reflective marker, when tape is moving forward, sets the End of Tape FF. When set, the End of Tape FF initiates the following:

1. Turns on the EOT indicator on the maintenance panel.
2. Returns an end of tape signal to the TCU indicating that the reflective marker has been located.
3. Stops tape motion by clearing the Motion FF's--if the unit is under manual control. If the unit is under external control, motion continues until stopped by either a load point marker, fault, stop signal from file mark stop circuit, or by dropping the forward select while a write operation is still selected.

The End of Tape FF, once set, remains set until the EOT marker is sensed in the reverse direction or a load point marker is detected. Therefore, if the EOT marker is sensed when under external control, the unit need not be stopped immediately.

The End of Tape FF can only be cleared by sensing the EOT marker in the reverse direction or by sensing a load point marker. This could occur if more than one load point is used on a reel of tape. Note that tape motion is not stopped if an EOT marker is detected during reverse tape motion.

FAULT

The fault circuit stops operation when any one of a number of fault conditions is detected.

The Fault FF is set if:

1. The Pneumatic switches are open (indicating that tape has been removed from the vacuum column). The Loops Ready light on the maintenance panel is turned off when either switch is opened.
2. Fault switch on maintenance panel is depressed.
3. The -20 vdc power supply output is not present.
4. There is an external or local master clear. The Fault FF is cleared by a pulse when the master clear is removed.

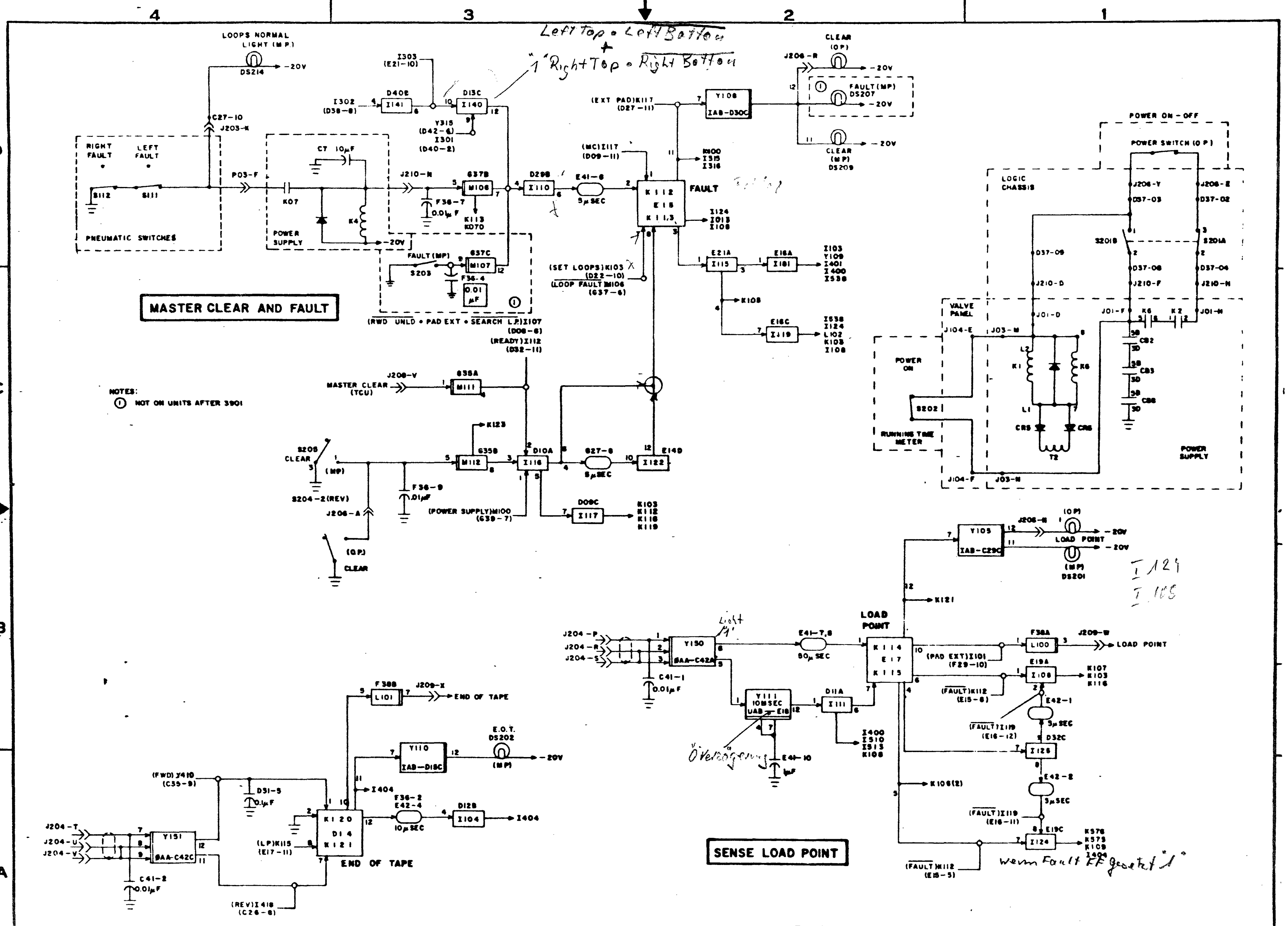
The Fault FF, when set, initiates the following actions:

1. Lights the Fault and Clear lights on the maintenance panel and the Clear light on the operator panel.
2. Stops tape motion by clearing the Motion FF's.
3. Stops reel servo drive and energizes reel servo brakes.

Note that the Fault FF is cleared when a load tape operation is initiated. Therefore, it is not necessary to remove the fault indication by master clearing the unit before pressing the Forward or Reverse switches.

SENSE LOAD POINT

The sense load point circuit stops tape motion when the load point marker is positioned over the photocell by applying a 5 μsec clear pulse to the motion FF's. The Load Point FF is cleared 10 msec after the tape moves off the load point marker.



19

CONTROL DATA
PERIPHERAL EQUIPMENT DIVISION
MINNEAPOLIS, MINNESOTA

TITLE	PRODUCT		
LOCAL CONTROL I	607		
	SIZE C	DRAWING NO 46176100	REV AL
	DRAWN B H M	SHEET 7 OF 12	

PAD EXTEND

The pad extend circuit extends the pressure pad prior to low speed (150 ips) operation, and retracts the pressure pad prior to high speed operation. The tape cleaners are turned on when the pad is extended and turned off when retracted. The pad extend circuit also senses the state of the pressure pad.

The Pad Extend FF is set by:

1. Local or external master clear.
2. Tape at load point.

The Pad Extend FF, when set, allows:

1. Ground output from extend pad relay puller to extend the pad and enable a write operation.
2. -20v output from the scraper off relay puller to allow a vacuum to be applied to cleaning ports.

While the pressure pad is in the process of extending, the pad switch is closed. After a delay of approximately 400 msec, the output from I101 changes from "0" to "1". This indicates that the pressure pad is fully extended and a read or write operation may be performed.

Delay Y117 prevents the Reverse FF K406/K403 from being set until the pad has been extended for 1.5 seconds after a high speed rewind. (See Motion Control Discussion.)

The Extend Pad FF is cleared when:

1. Rewind operation is selected.
2. Tape is in unload status.

When the Extend Pad FF is cleared, the pad is retracted and the vacuum is removed from the cleaning ports. Once the pad retracts sufficiently to open the pad switch, a 50 μsec pulse from I105 is supplied to the rewind circuit to permit high speed operation.

LOAD TAPE

The load tape circuit, when energized, provides the logic to enable the fault bypass solenoids and progress the tape transport from the unload status to the tape loaded status.

When the Load Point switch on the operator panel is depressed, the Set Loops FF is set, causing the left and right fault bypass solenoids to be energized. The output of the Set Loops FF also clears the Unload FF. This results in the energizing of power supply relays which start the vacuum pump and capstan motors. The photocell circuits allow the supply reel to drive tape into its loop box. Once the supply loop is set, the Search Load Point FF is set, starting tape motion into the other loop box. When both loops are set, the Set Loops FF is cleared and the fault by pass solenoid is deenergized when the load point marker is sensed, the Load Point FF is set to stop forward motion and the Pad Extend FF is set. The Search Load Point FF is cleared after the pad switch closes.

REWIND UNLOAD AND UNLOAD

The rewind unload circuit rewinds tape at high speed from the take-up reel to the supply reel. A rewind unload operation is selected by depressing the Unload switch on the operator panel or when a rewind command is received from the TCU. Either command input sets the Rewind and Rewind Unload FF's.

The rewind operation continues until the load point marker is sensed. The High Speed FF is then cleared; tape continues to be rewound at slow speed until it is completely removed from the take-up reel. At that time, Fault FF sets the Unload FF. With the Unload FF set, the Unload lamps illuminate and power is removed from the capstan motors and loop vacuum pump. The Unload FF remains set until the tape load procedure is executed. Note that the Unload FF is also set by the input to M100 from the power supply whenever the unit is turned on.

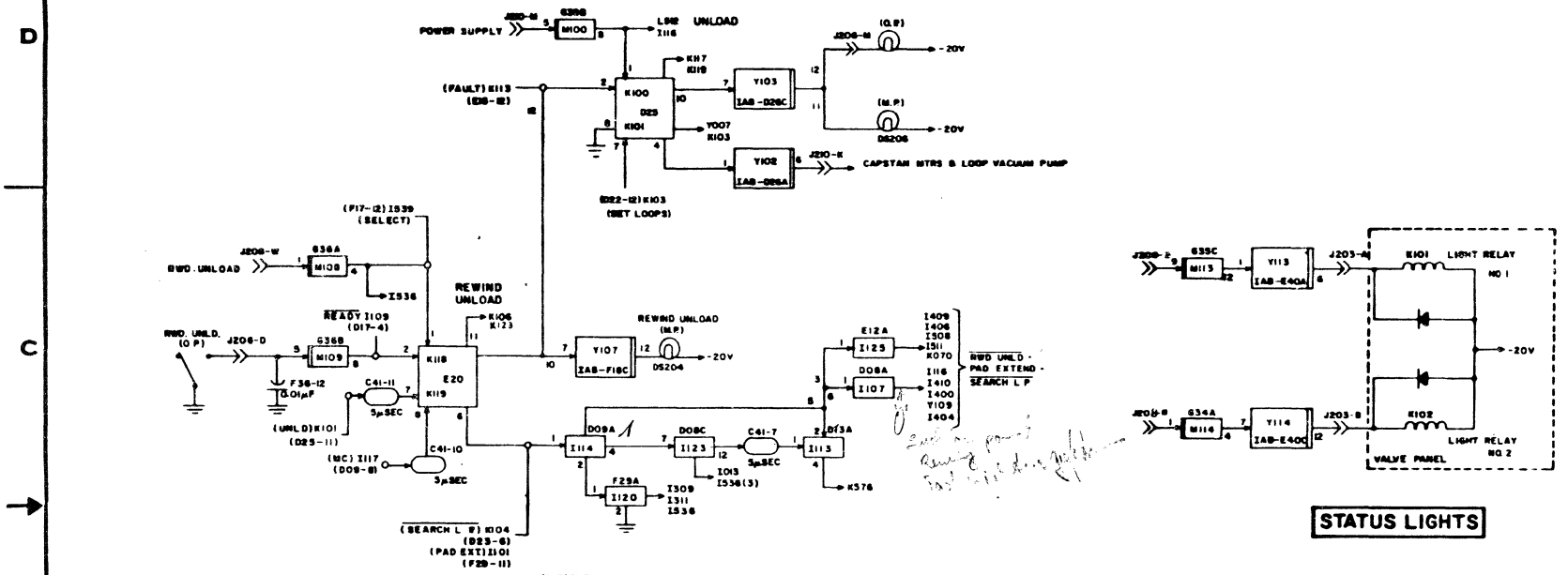
REWIND

The Rewind FF is set when a manual or programmed command causing the tape to be rewound from the take-up reel to the supply reel at the rate of more than 350 ips. Motion stops when a load point is reached.

When a rewind command is applied to the circuit, the Rewind FF is set, causing the Rewind lamps to illuminate and the Pad Extend FF to be cleared. The head pad is then retracted and the vacuum is removed from the tape cleaners.

When the head pad is retracted the Reverse FF is set, enabling the tape to be moved in reverse. The High Speed FF is also set, if the tape is not at a load point, energizing a power supply relay that applies power to the high speed capstan windings. The Search Load Point FF is also set during rewind.

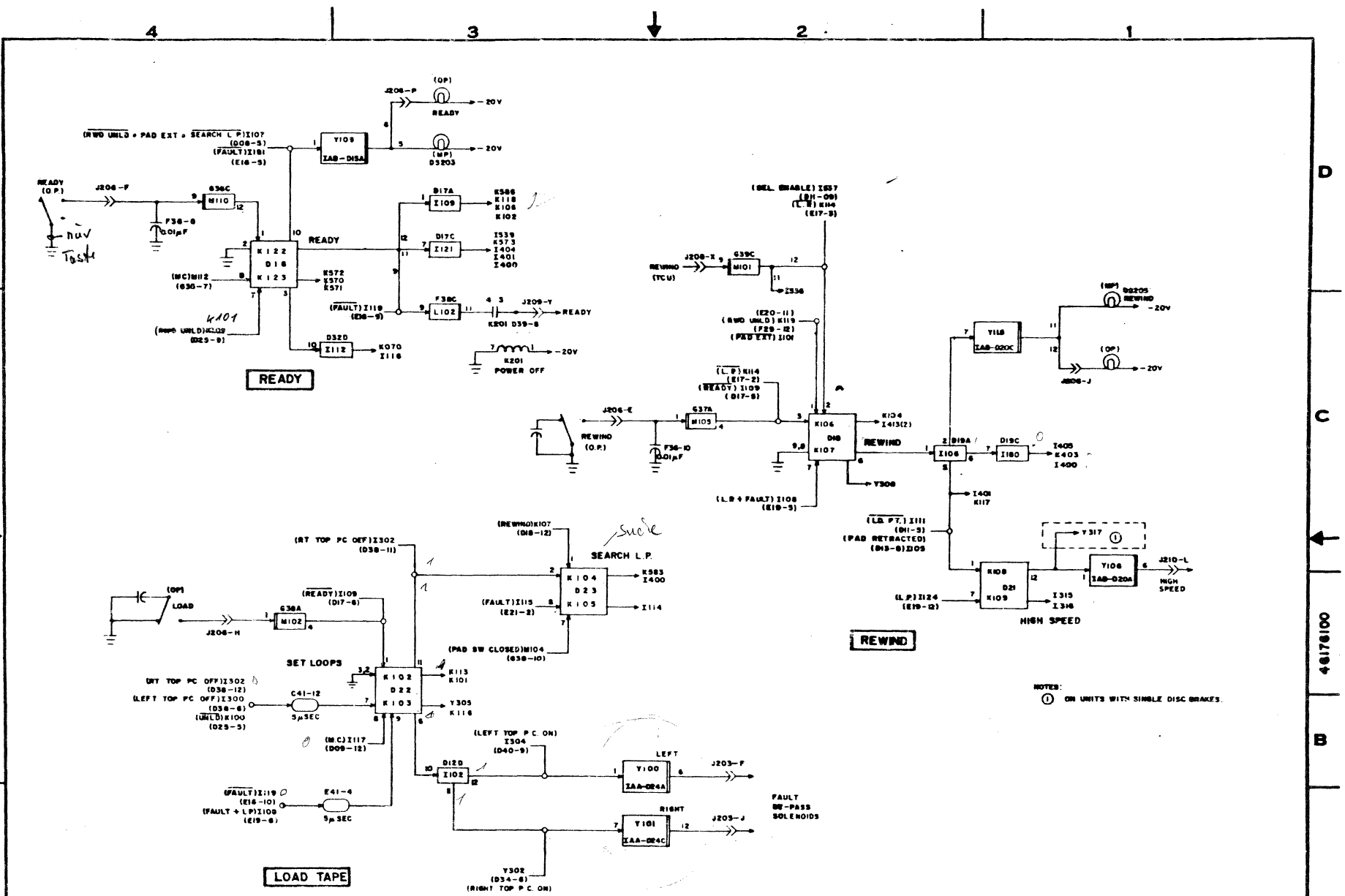
As the rewind operation continues, the tape is scanned for a load point. When a load point marker is detected, the Load Point FF is set, tape motion is stopped, and the Pad Extend FF is set.



CONTROL DATA CORPORATION PERIPHERAL EQUIPMENT DIVISION	TITLE LOCAL CONTROL II	PRODUCT 607	
		SIZE C	DRAWING NO. 46176100
		REV AN	
		DRAWN K P	SHEET 8 OF 12

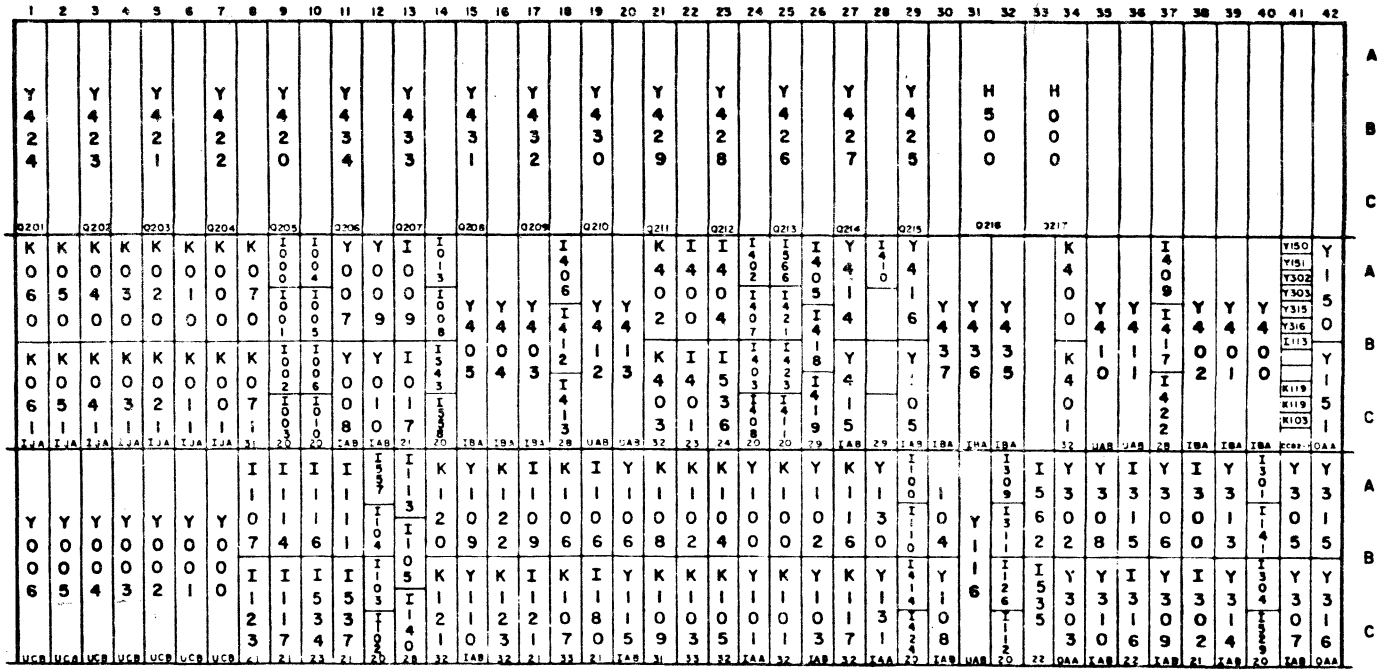
46176100

I 180 ständig 0° Reverse nicht gelassen
Forward nicht gesetzt

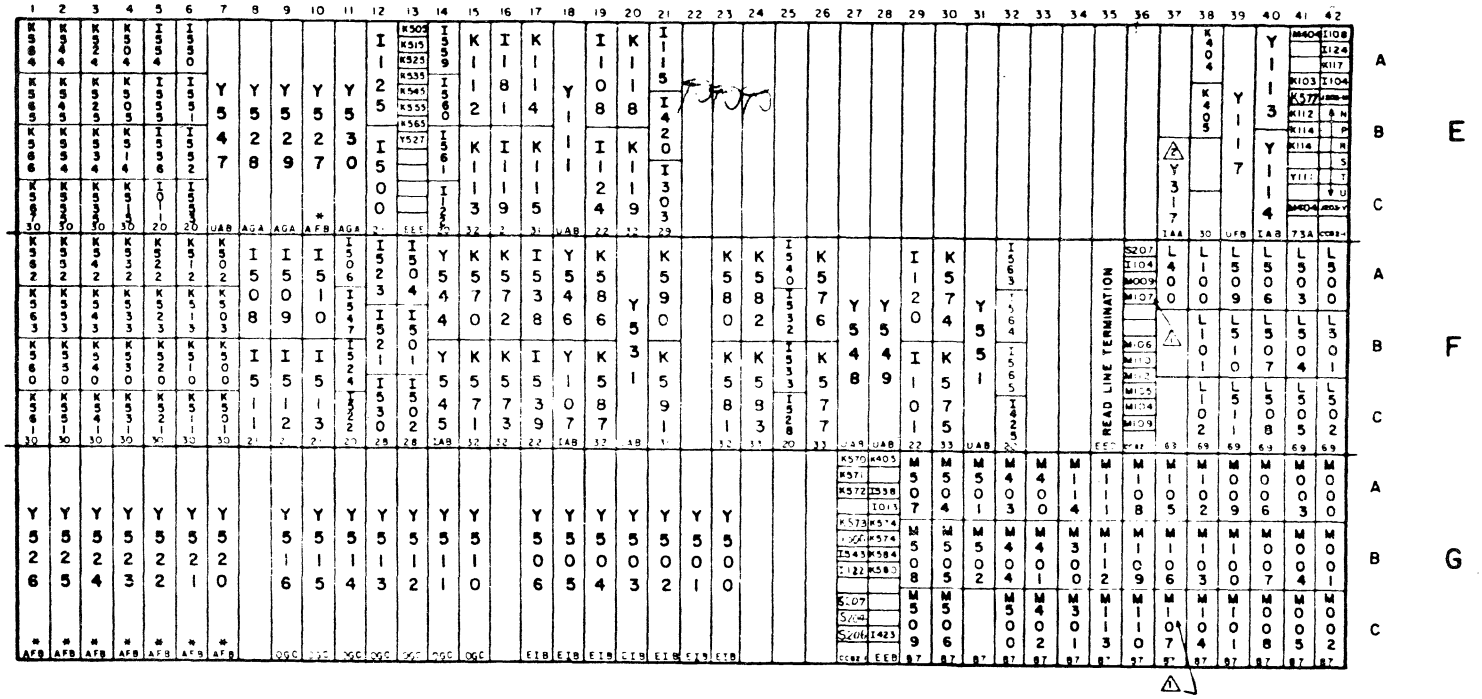


CONTROL DATA CORPORATION, PERIPHERAL EQUIPMENT DIVISION	TITLE: LOCAL CONTROL III	PROJECT 607	
		SIZE C	DRAWING NO. 46176100 REV AN
		DRAWN B H M	SHEET 9 OF 12

46176100

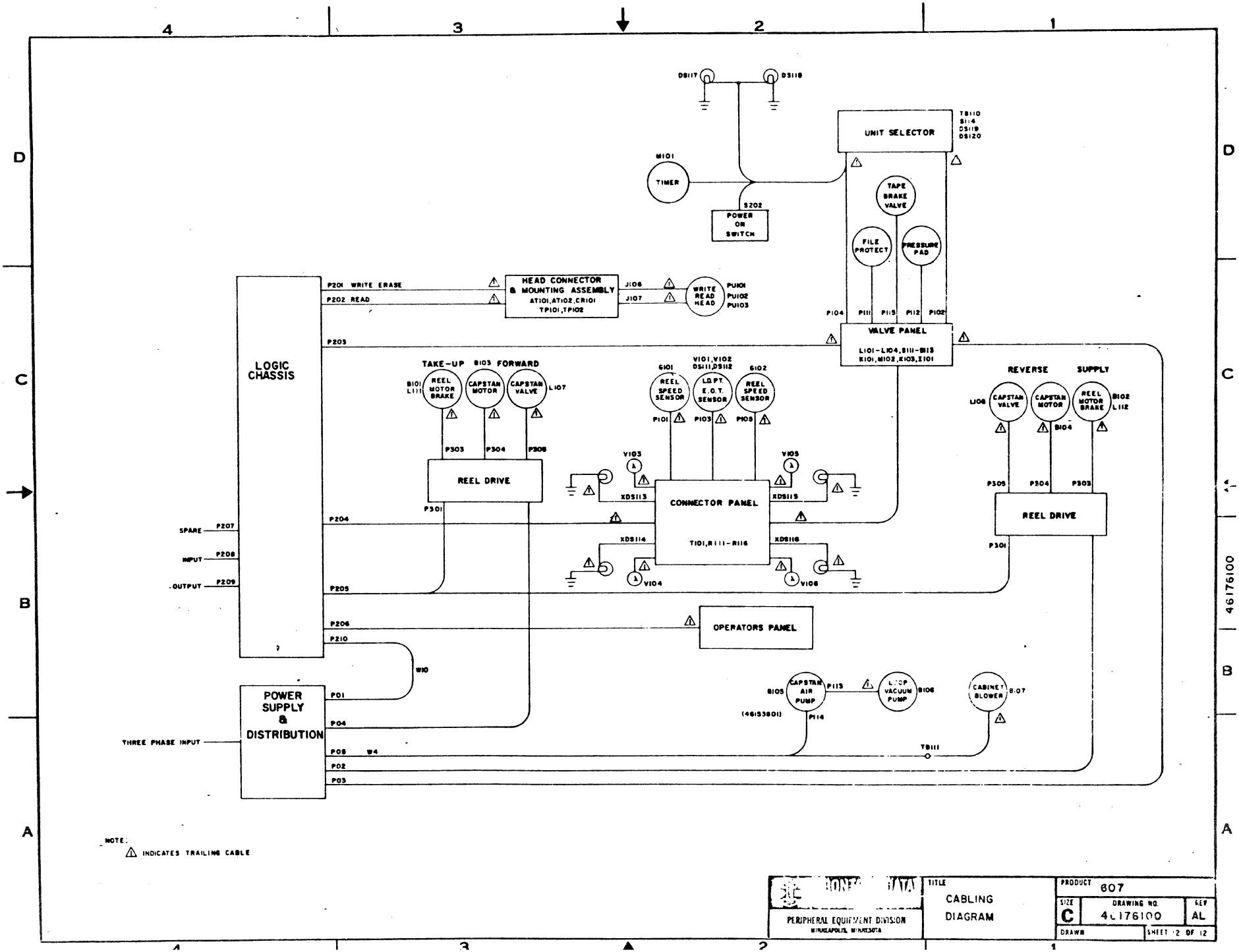


CONTROL DATA CORPORATION	TITLE: CARD PLACEMENT (PART 1)	PRODUCT: 607
DEVELOPMENT DIVISION		SIZE: C · DRAWING NO: 46176100 · REV: AN
		SHEET: 10 OF 12 · PAGE



NOTE: * AFA CARD MAY BE USED IN THIS POSITION

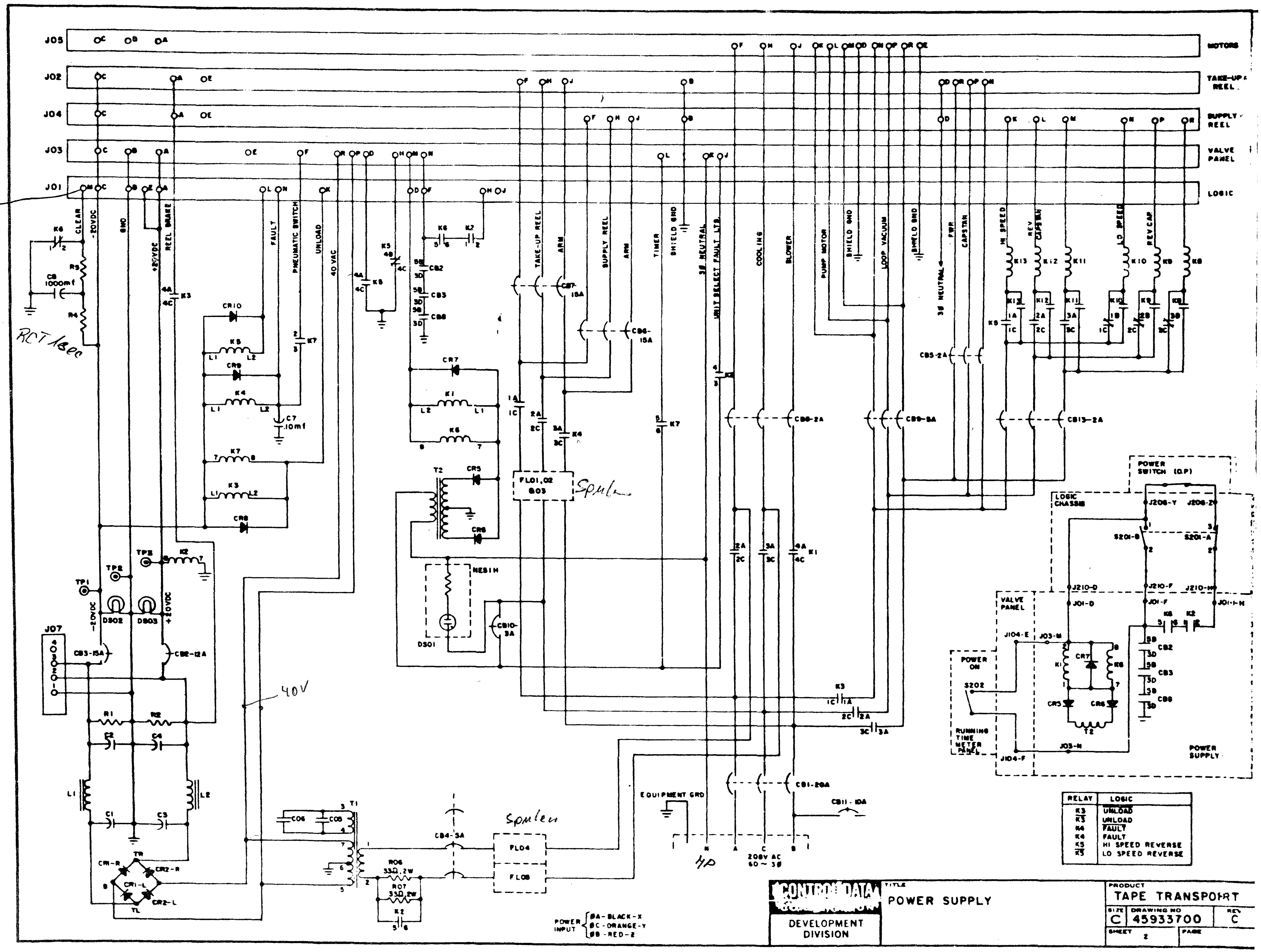
CONTROLDATA CORPORATION DEVELOPMENT DIVISION	TITLE CARD PLACEMENT (PART 2)	PRODUCT 607		
		SIZE C	DRAWING NO 46176100	REV AN
		SHEET 11 OF 12	PAGE	


DS117
DS118
UNIT SELECTOR
TB110
S114
DS119
DS120
M101
TIMER
S202
POWER ON SWITCH
TAPE BRAKE VALVE
FILE PROTECT
PRESSURE PAD
P104
P111
P115
P112
P102
VALVE PANEL
L101-L104, B111-B113
K101, M102, K103, Z101
HEAD CONNECTOR & MOUNTING ASSEMBLY
AT101, AT102, CR101
TP101, TP102
J106
J107
WRITE READ HEAD
PU101
PU102
PU103
P201 WRITE ERASE
P202 READ
P203
LOGIC CHASSIS
TAKE-UP
B103 FORWARD
B101
L111
REEL MOTOR BRAKE
CAPSTAN MOTOR
CAPSTAN VALVE
L107
P303
P304
P306
REEL DRIVE
P301
G101
REEL SPEED SENSOR
LD.P.T. E.O.T. SENSOR
V101, V102
DS111, DS112
G102
REEL SPEED SENSOR
P101
P103
P105
V103
V105
XDS113
XDS115
CONNECTOR PANEL
T101, R111-R116
XDS114
XDS116
V104
V106
REVERSE
SUPPLY
L108
CAPSTAN VALVE
CAPSTAN MOTOR
REEL MOTOR BRAKE
B102
L112
B104
P305
P304
P303
REEL DRIVE
P301
P204
P205
SPARE P207
INPUT P208
OUTPUT P209
P206
P210
OPERATORS PANEL
W10
POWER SUPPLY & DISTRIBUTION
P01
P04
P08
W4
P02
P03
THREE PHASE INPUT
B105
CAPSTAN AIR PUMP
(46153801)
P113
P114
LOOP VACUUM PUMP
B106
CABINET BLOWER
B107
TB111
NOTE:
INDICATES TRAILING CABLE
PERIPHERAL EQUIPMENT DIVISION
MINNEAPOLIS, MINNESOTA
TITLE
CABLING DIAGRAM
PRODUCT 607
SIZE C
DRAWING NO. 46176100
REV AL
DRAWN
SHEET 12 OF 12
46176100

POWER SUPPLY

The primary power is converted to ac and dc for control and operation of the magnetic transport. The distribution of power throughout the transport is in a logical sequence.

1. 208 vac, 3Ø 60/50 cps is applied to the power supply chassis.
2. Main Power circuit is ON causing neon lamp DS01 to illuminate.
3. Relay Power circuit breaker CB10 is ON, and the momentary close Power On switch on the maintenance panel is held on for 2 seconds, power is applied through transformer T2 to energize K1 and K6. The power is then:
   a. Applied through the closed contacts of K1 and Cooling Motors circuit breaker CB8 so that power is applied to the blowers.
   b. Applied through the closed contacts of K1 so that when Primary DC Power circuit breaker CB4 is closed, power is applied to the primary of transformer T1. Refer to the power on sequence diagram (A) in the Flow Charts and Timing Diagrams Section. The secondary voltage is:
      1. Supplied as 40 vac, through the valve panel to energize the photocell lamp in the tape loop boxes, and the load point/end of tape lamps on the tape deck.
      2. Rectified in a full wave bridge network. The ±20 vdc outputs are applied to their respective circuit breakers.
         a. The -20 vdc is applied through -20 VDC Power circuit breaker CB3 to:
            (1) The reel drive motor brake as field supply.
            (2) One side of relays K5, K4, K7, and K3.
            (3) To Light 1, Light 2, and File Protect solenoids and to the Loop Fault Bypass, Pad Extend, and Tape Scraper as power in the valve panel.
            (4) The logic circuit as power.
            (5) A capacitive charging network which provides a 1 second clear pulse to clear the Ready FF, the Rewind Unload FF, the Set Loops FF and to set the Unload FF. Refer to the power on sequence diagram (B) in the Flow Charts and Timing Diagrams Section.
            (a) Setting the Unload FF provides power to illuminate the Unload lamp.
            (b) Setting the Set Loops FF activates the fault bypass solenoids and energizes relay K4 when a load sequence is in process. Consequently, power is applied through closed Take-up Reel Armature circuit breaker CB7 and Supply Reel Armature CB6 to their respective drive motors.
         b. When +20 VDC Power circuit breaker CB2 is closed, power is applied to:
            (1) Energize relay K2 to provide holding power to provide a hold for K1 and K6 and make available the power to illuminate Light #1/Light #2 (on computer command) and the File Protect light when the file protect ring is installed. Refer to the power on sequence diagram (C) in the Flow Charts and Timing Diagrams Section.
            (2) The Capstan air pump and cabinet blower as power.
            (3) The logic circuit as power.


J05
J02
J04
J03
J01
J07
MOTORS
TAKE-UP REEL
SUPPLY REEL
VALVE PANEL
LOGIC
CLEAR
-20VDC
GND
+20VDC
REEL BRAKE
FAULT
PNEUMATIC SWITCH
UNLOAD
40 VAC
TAKE-UP REEL
ARM
SUPPLY REEL
TIMER
SHIELD GND
3Ø NEUTRAL
UNIT SELECT FAULT LTS.
COOLING
BLOWER
PUMP MOTOR
LOOP VACUUM
FWR
CAPSTAN
HI SPEED
REV CAPSTAN
LO SPEED
REV CAP
POWER SWITCH (O.P)
LOGIC CHASSIS
VALVE PANEL
POWER ON
RUNNING TIME METER PANEL
POWER SUPPLY
EQUIPMENT GRD
208V AC 60 ~ 3Ø
POWER INPUT
ØA - BLACK - X
ØC - ORANGE - Y
ØB - RED - Z
RELAY
LOGIC
K3 UNLOAD
K3 UNLOAD
K4 FAULT
K4 FAULT
K5 HI SPEED REVERSE
K5 LO SPEED REVERSE
CONTROL DATA
DEVELOPMENT DIVISION
TITLE
POWER SUPPLY
PRODUCT
TAPE TRANSPORT
SIZE C
DRAWING NO 45933700
REV C
SHEET 2
PAGE
S21
M100
Zöffner
RCT 18ec
40V
Spulen
HP

REEL MOTOR DRIVE

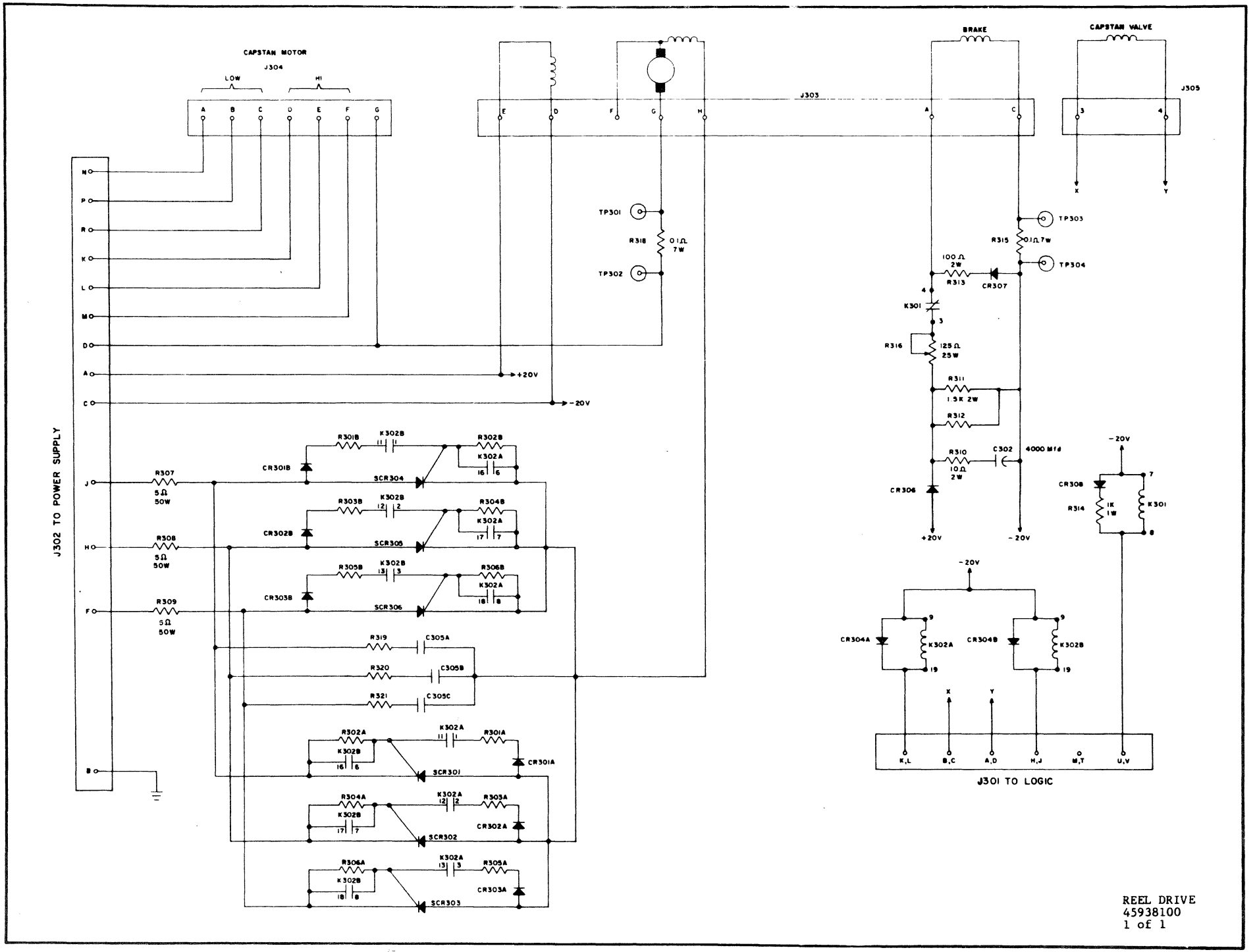
The reel motor drive circuit controls the braking and direction of the shunt-wound dc reel motor rotation. The direction of current flow through the armature establishes the direction of motor rotation and is controlled by the silicon controlled rectifiers (SCR's) selected. Operation of the supply and take-up reel drive circuits are similar. Therefore, only the take-up reel operation is presented.

If the take-up reel motor is to be driven counterclockwise, relays K302B and K301 are energized (K302A is not energized). During the positive half of the applied 3-phase line voltage, the voltage dividers paralleling SCR304, SCR305, and SCR306 develop the forward bias that is applied to the respective SCR gates. This causes the SCR circuits to be alternately gated on as the applied anode voltage goes positive. The SCR circuits are gated off when the applied anode voltage goes negative. The SCR's produce a 115 vdc output which drives the reel motor CCW. Parallel SCR301, SCR302, SCR303 are not energized since, with K302B energized, their respective cathode to gate circuits are shorted to disable the circuits.

For clockwise rotation, relay K302A is energized and K302B is not energized. K301 prevents the brake from being applied. SCR301, SCR302, and SCR303 are forward biased, causing current to flow through the armature in the opposite direction (i.e., 115 vdc is developed at the anodes of the SCR circuits). The remainder of the circuit operation is parallel to the CCW motion described above.

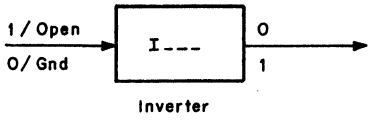
If the take-up reel motor is to be braked, the servo drive take-up relay pullers receive "0" inputs. Relays K301, K302A and K302B de-energize. Line current through the armature is turned off. With K301 de-energized, the normally closed contacts of K301 permit current through the brake winding to provide the braking action. The stored energy in C302 is sufficient to brake the motor if power is interrupted during operation.

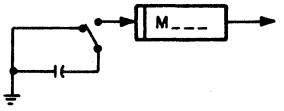
If the take-up reel motor is to be partially braked (during high speed rewind), one side of the brake winding is grounded. This allows a small amount of current to flow through the winding and partially brakes the motor.

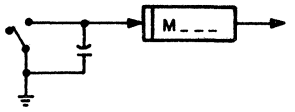


REEL DRIVE
45938100
1 of 1

M cards are not restricted to I/O functions alone. Using a switch to ground or open the input of an M card results in a forced output of 1 or 0 respectfully. Inclusion of a capacitor can provide a pulse or noise filtering.

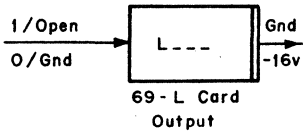


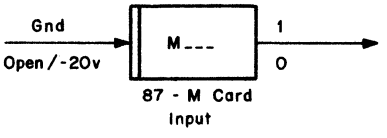


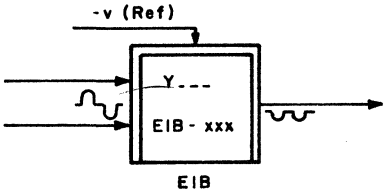


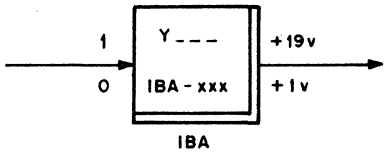
Closing of the switch results in the discharged capacitor being connected between the M card input voltage divider and ground. While the capacitor is charging, the input appears as ground and the output is a 1; but as the capacitor charges towards -20v the threshold will be reached, the output will go back to a-0. The switch must be released before the capacitor is again discharged, thus the output of the M card will be a short pulse once for each closure of the switch.

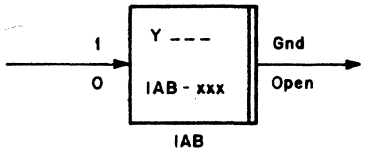
The capacitor provides noise filtering through it's properity of not begin able to change it's charge instantaneously.

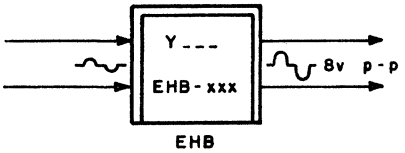


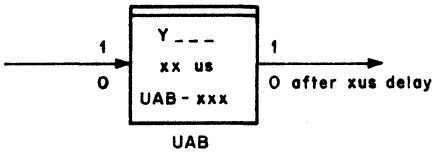


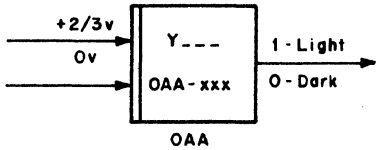


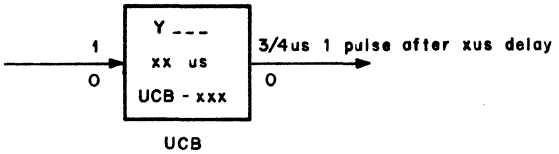


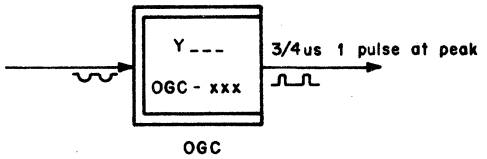


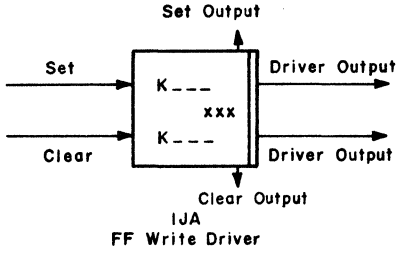


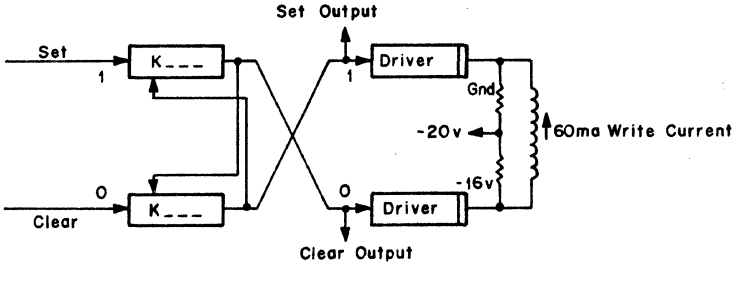












3229 Controller

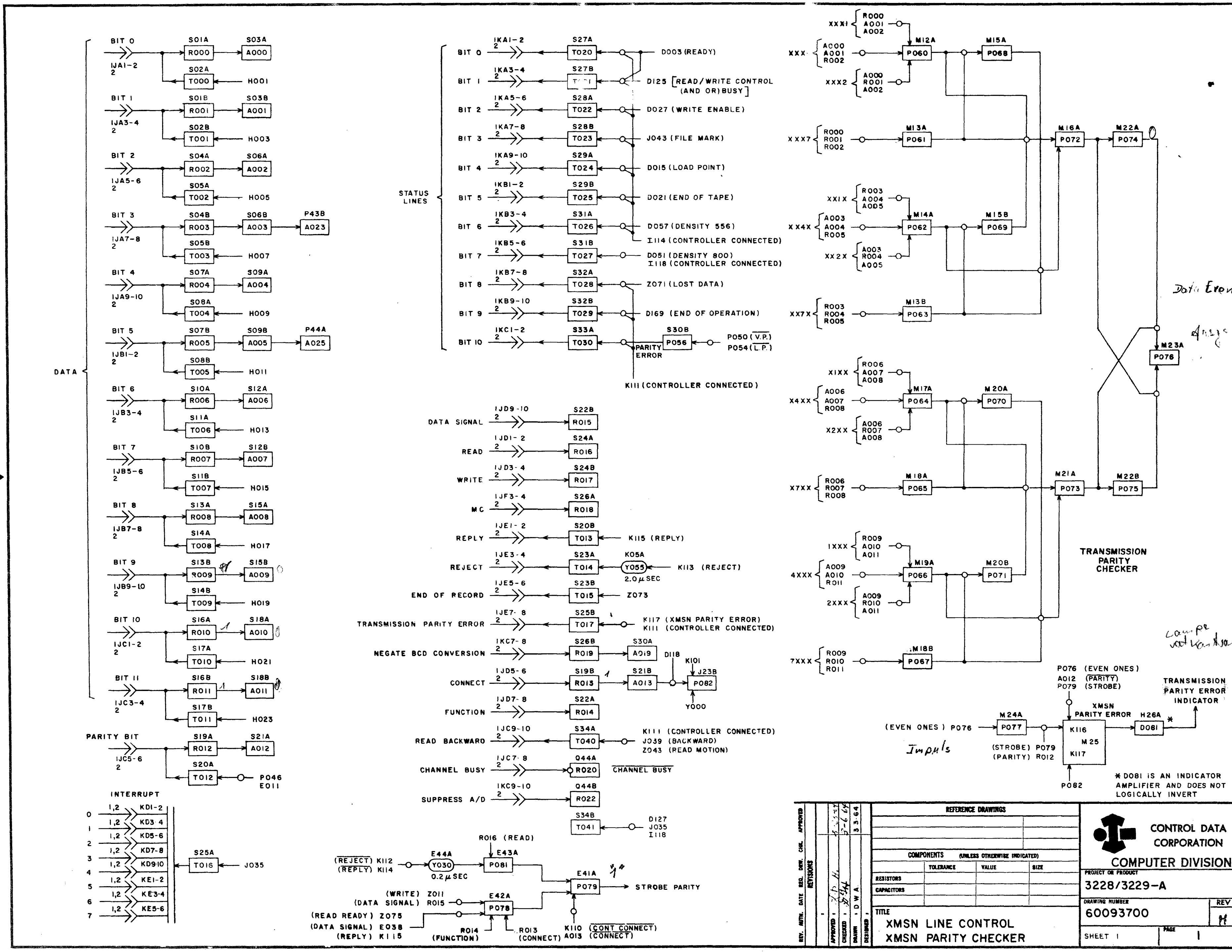
NOTE: All terms are not in alphanumerical order

TERM	LOCATION	PAGE	DEFINITION
D003	I26A	6	
D015	I28A	6	
D021	I29A	6	
D027	I30A	6	
D051	G29B	7	
D057	I42A	7	
D118	E17B	3	
D125	D43B	3	
D169	L07B	3	
E011	D29A	11	
E038	C13B	2	
D127	E17A	3	
H001	K20	12	
H003	K21	12	
H005	K22	12	
H007	K23	12	
H009	K24	12	
H011	K25	12	
H013	K26	12	
H015	K27	12	
H017	K28	12	
H019	K29	12	
H021	K30	12	
H023	K31	12	
I114	C06A	2	
I118	D13A	2	
J035	D07A	3	
J039	C41	3	
J043	I37	6	
K101	C08	2	
K110	C05	2	
K111	C05	2	
K112	C17A	2	
K113	C18A	2	
K114	C16	2	
K115	C16	2	
P046	'144 B	12	
P050	E39A	12	
P054	J18	14	
Y000	C07A	2	
Z011	F30	8	
Z043	D31A	11	
Z071	C03	8	
Z073	D25	11	
Z075	D26	11	

FORM 510

ITL-1
Rev. J

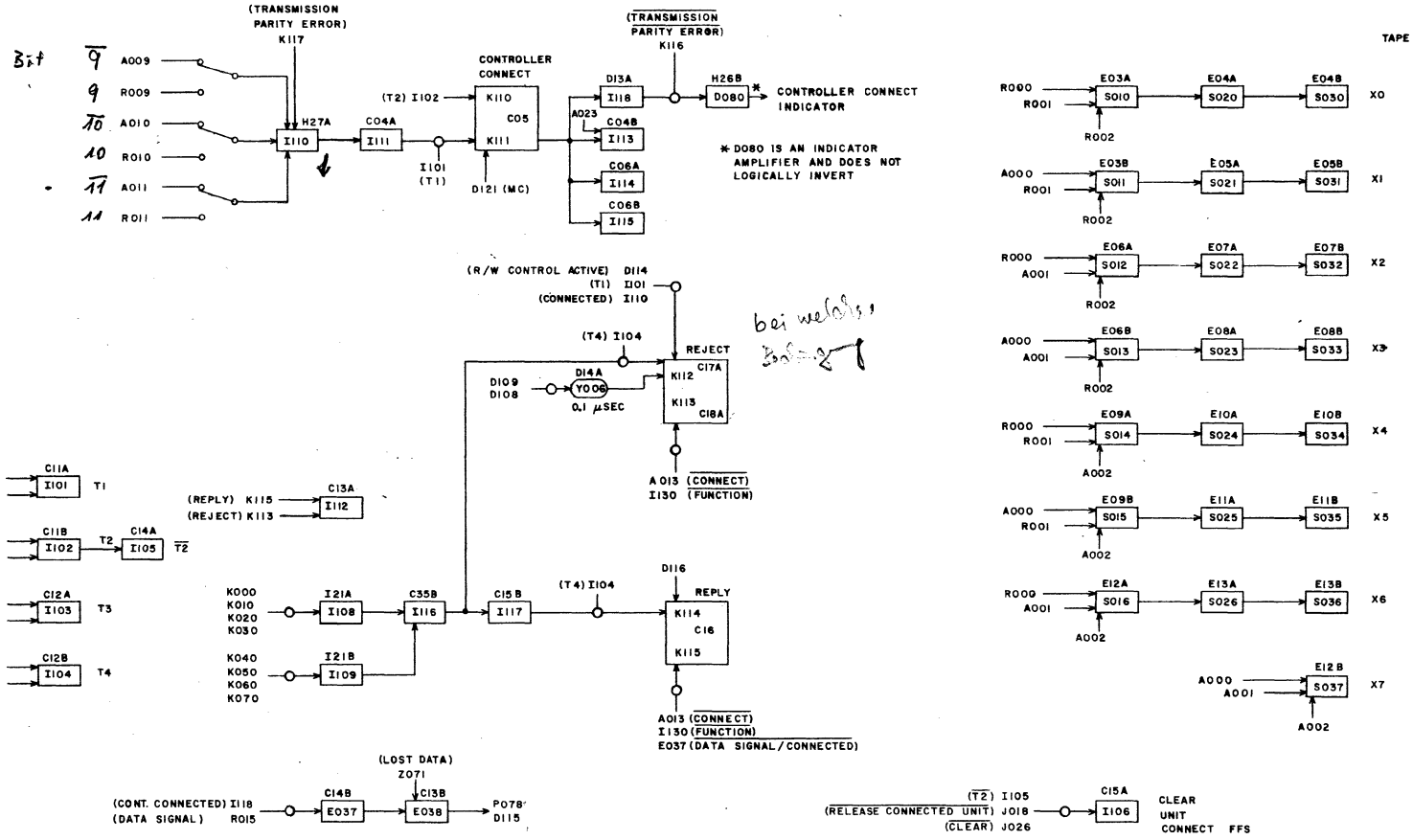
35



DATA
BIT 0 … BIT 11
PARITY BIT
INTERRUPT
STATUS LINES
BIT 0 D003 (READY)
BIT 1 D125 [READ/WRITE CONTROL (AND OR) BUSY]
BIT 2 D027 (WRITE ENABLE)
BIT 3 J043 (FILE MARK)
BIT 4 D015 (LOAD POINT)
BIT 5 D021 (END OF TAPE)
BIT 6 D057 (DENSITY 556)
I114 (CONTROLLER CONNECTED)
BIT 7 D051 (DENSITY 800)
I118 (CONTROLLER CONNECTED)
BIT 8 Z071 (LOST DATA)
BIT 9 D169 (END OF OPERATION)
BIT 10 PARITY ERROR
P050 (V.P.)
P054 (L.P.)
K111 (CONTROLLER CONNECTED)
DATA SIGNAL
READ
WRITE
MC
REPLY K115 (REPLY)
REJECT K113 (REJECT) 2.0 μSEC
END OF RECORD Z073
TRANSMISSION PARITY ERROR K117 (XMSN PARITY ERROR) K111 (CONTROLLER CONNECTED)
NEGATE BCD CONVERSION
CONNECT
FUNCTION
READ BACKWARD K111 (CONTROLLER CONNECTED) J039 (BACKWARD) Z043 (READ MOTION)
CHANNEL BUSY
SUPPRESS A/D
(REJECT) K112
(REPLY) K114
0.2 μSEC
R016 (READ)
STROBE PARITY
(WRITE) Z011
(DATA SIGNAL) R015
(READ READY) Z075
(DATA SIGNAL) E038
(REPLY) K115
R014 (FUNCTION)
R013 (CONNECT)
K110 A013
(CONT CONNECT) (CONNECT)
TRANSMISSION PARITY CHECKER
P076 (EVEN ONES)
A012 (PARITY)
P079 (STROBE)
XMSN PARITY ERROR
TRANSMISSION PARITY ERROR INDICATOR
(EVEN ONES) P076
(STROBE) P079
(PARITY) R012
P082
* D081 IS AN INDICATOR AMPLIFIER AND DOES NOT LOGICALLY INVERT
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE
VALUE
SIZE
RESISTORS
CAPACITORS
REVISIONS
CONTROL DATA CORPORATION
COMPUTER DIVISION
PROJECT OR PRODUCT
3228/3229-A
DRAWING NUMBER
60093700
REV
TITLE
XMSN LINE CONTROL
XMSN PARITY CHECKER
SHEET 1
PAGE 1

TERM	LOCATION	PAGE	DEFINITION
A000	S03A	1	
A001	S03B	1	
A002	S06A	1	
A009	S15B	1	
A010	S18A	1	
A011	S18B	1	
A013	S21B	1	
A023	P43B	1	
D108	C22A	3	
D109	D37A	3	
D114	D43A	3	
D115	D39A	3	
D116	D40A	3	
D121	D05B	3	
I130	C32B	3	
J018	C33	3	
J026	C40	3	
K000	I01	4	
K010	I05	4	
K020	I06	4	
K030	I10	4	
K040	I11	4	
K050	I15	4	
K060	I16	4	
K070	I19	4	
K116	M25	1	
K117	M25	1	
P078	E42A	1	
R000	S01A	1	
R001	S01B	1	
R002	S04A	1	
R009	S13B	1	
R010	S16A	1	
R011	S16B	1	
R013	S19B	1	
R015	S22B	1	
Z071	C03	8	

FORM 510



Connect Timing

REV.	APPR.	DATE	REGD.	ENGR.	CHK.	APPROVED
						2-27-64

REVISIONS

APPROVED
CHECKED
DRAWN
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
UNIT CONNECTION

CONTROL DATA CORPORATION
COMPUTER DIVISION

PROJECT OR PRODUCT
3228/3229-A

DRAWING NUMBER
60093700

REV
F

SHEET 2

PAGE
2

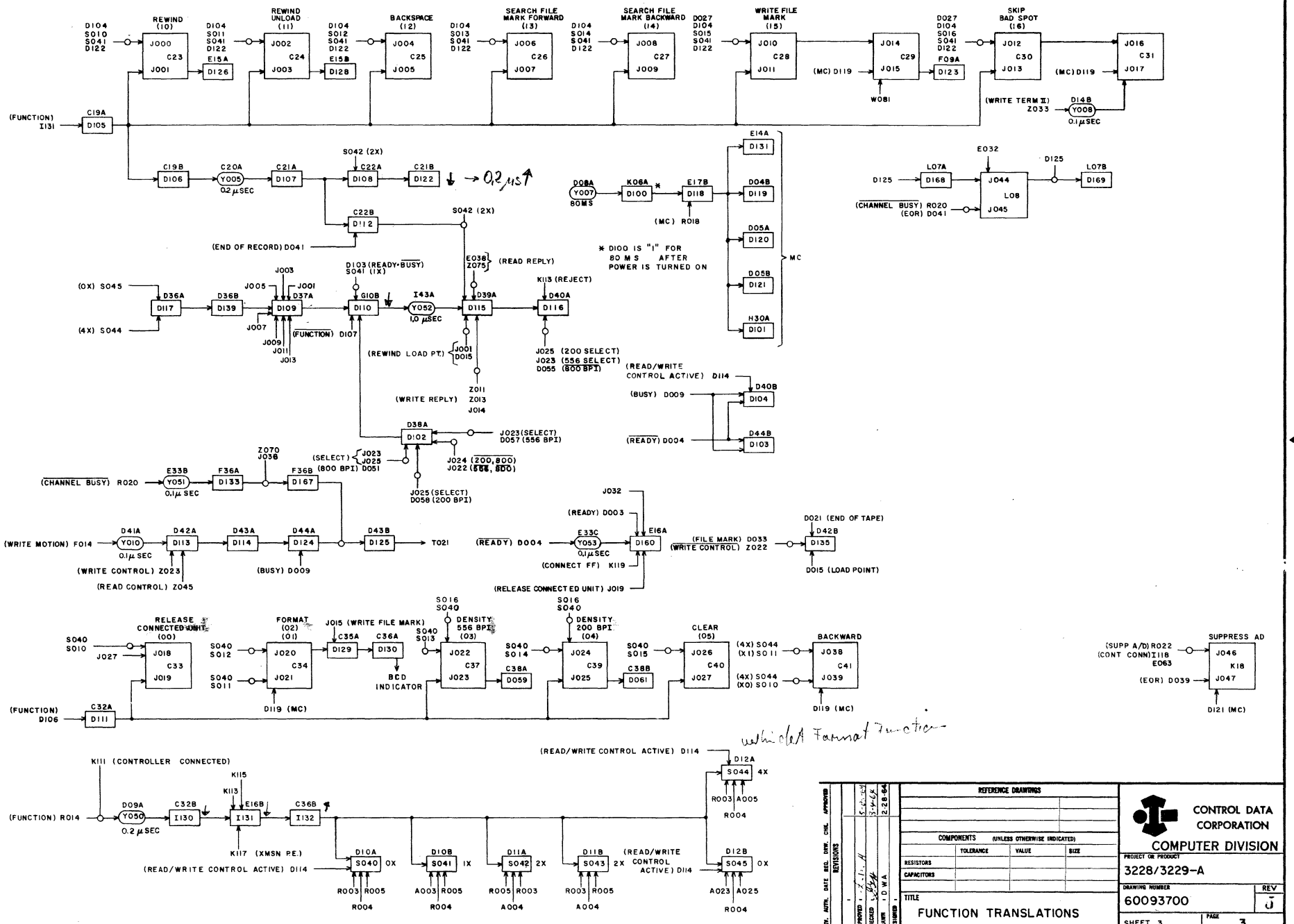
TERM	LOCATION	PAGE	DEFINITION
A003	S06B	1	
A004	S09A	1	
A005	S09B	1	
A023	P43B	1	
A025	P44A	1	
D003	I26A	6	
D004	I26B	6	
D009	I27A	6	
D015	I28A	6	
D021	I29A	6	
D027	I30A	6	
D033	I31A	6	
D041	I34A	7	
D051	G29B	7	
D055	I27B	7	
D057	I42A	7	
D058	I42B	7	
E032	J22B	14	
E038	C13B	2	
E063	H30B	14	
F011	F17B	8	
F014	F38A	8	
K111	C05	2	
K113	C18A	2	
K115	C16	2	
K117	M25	1	
K119	G24	2	
P050	E39A	12	
P054	J18	14	

FORM CA 210

TERM	LOCATION	PAGE	DEFINITION
R003	S04B	1	
R004	S07A	1	
R005	S07B	1	
R014	S22A	1	
R018	S26A	1	
R020	Q44B	1	
S010	E03A	2	
S011	E03B	2	
S012	E06A	2	
S013	E06B	2	
S014	E09A	2	
S015	E09B	2	
S016	E12A	2	
T021	S27B	1	
W081	G35B	8	
Z011	F30	8	
Z013	F32	8	
Z022	F27	8	
Z023	F27	8	
Z033	F42	8	
Z045	D34	11	
Z070	C03	8	
Z075	D26	11	
R022	Q44B	1	
I118	P13A	2	
D039	I32A	7	
E032	J22B	14	

FORM CA 210

Format Set 02 BCD INT (Binary)
CLR 01 BCD EXT (Coded)



which of Format Function

REV.	AUTH.	DATE	REQ.	DRW.	CHK.	APPROVED
REVISIONS						
-						

APPROVED
CHECKED
DRAWN I. D. W. A.
DESIGNED - 2-28-64

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

CONTROL DATA CORPORATION
COMPUTER DIVISION

PROJECT OR PRODUCT: 3228/3229-A

DRAWING NUMBER: 60093700 REV J

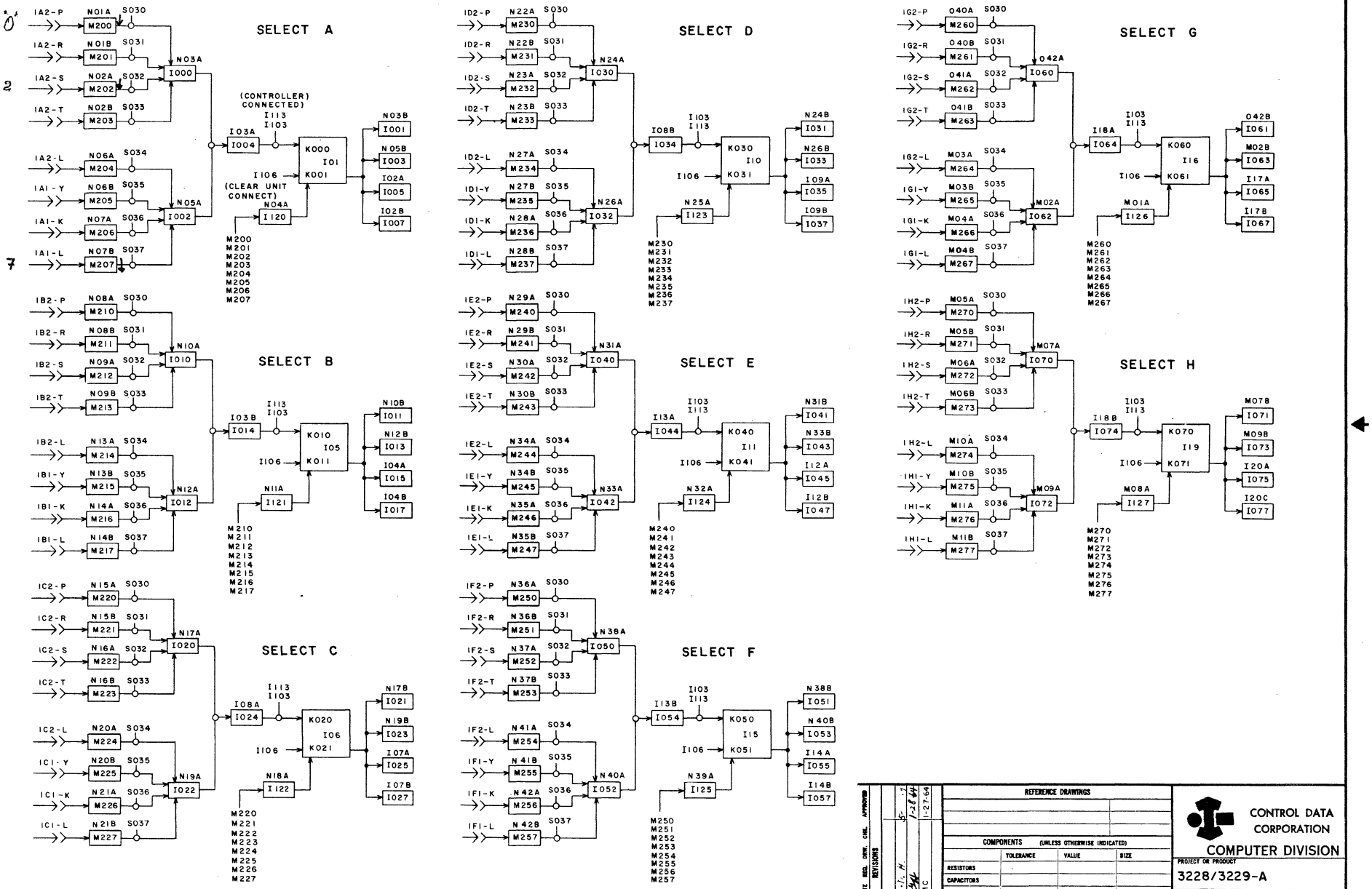
TITLE: FUNCTION TRANSLATIONS

SHEET 3 PAGE 3

TERM	LOCATION	PAGE	DEFINITION
I103	C12A	2	
I106	C15A	2	
I113	C04B	2	
S030	E04B	2	
S031	E05B	2	
S032	E07B	2	
S033	E08B	2	
S034	E10B	2	
S035	E11B	2	
S036	E13B	2	
S037	E14B	2	

FORM 510

Unit Select switch



REFERENCE DRAWINGS			

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

REV.	AUTH.	DATE	REGD.	DWN.	CHK.	APPROVED
REVISIONS						

APPROVED - 1-28-64
CHECKED - 1-27-64
DRAWN - E.M.C.
DESIGNED -

CONTROL DATA CORPORATION
COMPUTER DIVISION

PROJECT OR PRODUCT: 3228/3229-A

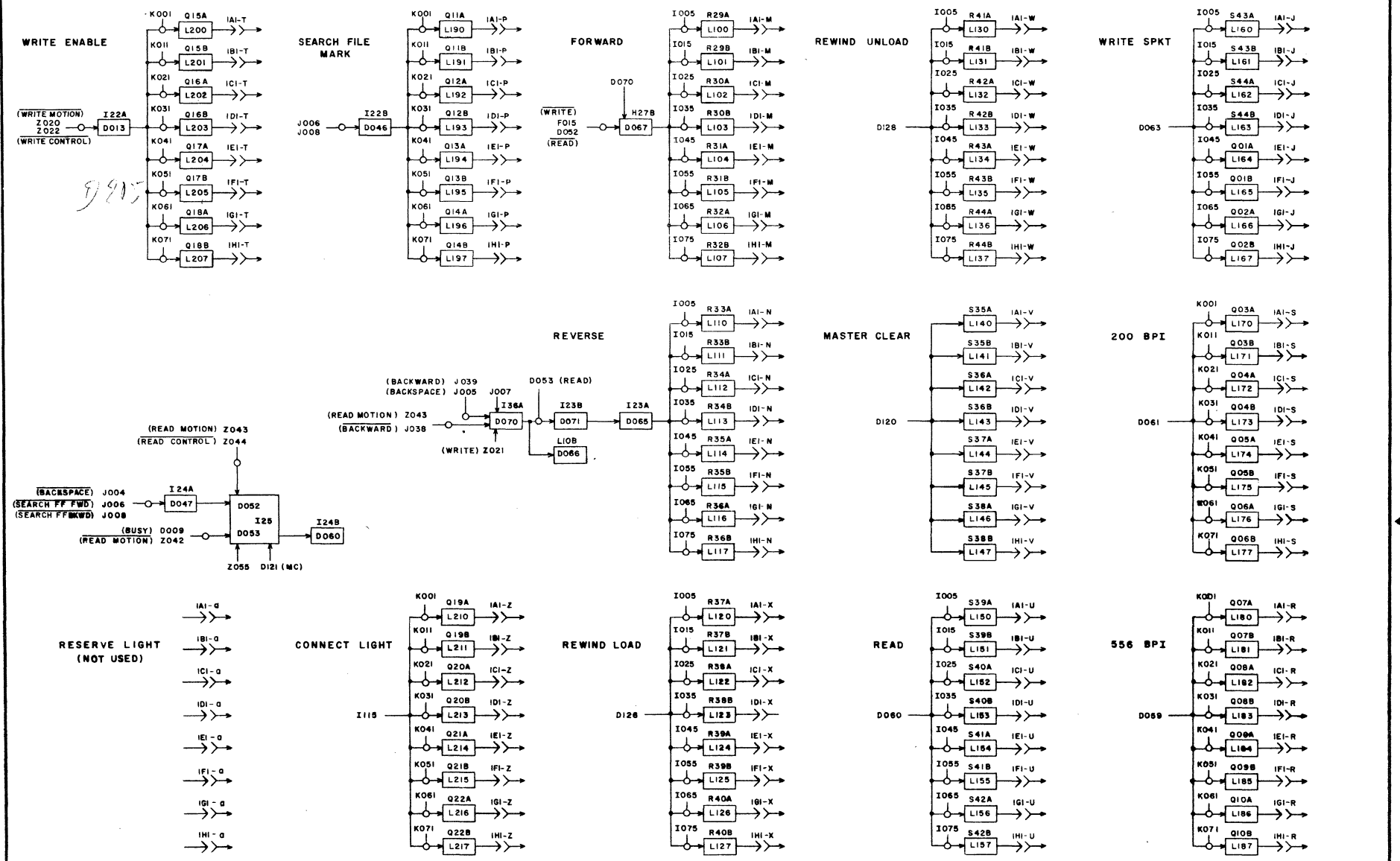
TITLE: UNIT SELECT

DRAWING NUMBER: 60093700 REV: F

SHEET 4 PAGE 4

TERM	LOCATION	PAGE	DEFINITION
D009	I27A	6	
D059	C38A	3	
D061	C38B	3	
D063	H43B	8	
D120	D05A	3	
D121	D05B	3	
D126	E15A	3	
D128	E15B	3	
F015	F16A	8	
I005	I02A	4	
I015	I04A	4	
I025	I07A	4	
I035	I09A	4	
I045	I12A	4	
I055	I14A	4	
I065	I17A	4	
I075	I20A	4	
I115	C06B	2	
J004	C25	3	
J005	C25	3	
J006	C26	3	
J007	C26	3	
J008	C27	3	
J038	C41	3	
J039	C41	3	
K001	I01	4	
K011	I05	4	
K021	I06	4	
K031	I10	4	
K041	I11	4	
K051	I15	4	
K061	I16	4	
K071	I19	4	
Z020	F19A	8	
Z021	F20A	8	
Z022	F27	8	
Z042	D30A	11	
Z043	D31A	11	
Z044	D34	11	
Z055	E30A	11	

FORM 510



REV.	APPROVED	DATE	DESCRIPTION
			REVISIONS

APPROVED - [illegible]
CHECKED - [illegible]
DRAWN - D.W.A. 3-2-64
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
UNIT REQUESTS

CONTROL DATA CORPORATION
COMPUTER DIVISION

PROJECT OR PRODUCT
3228/3229-A

DRAWING NUMBER
60093700

REV
F

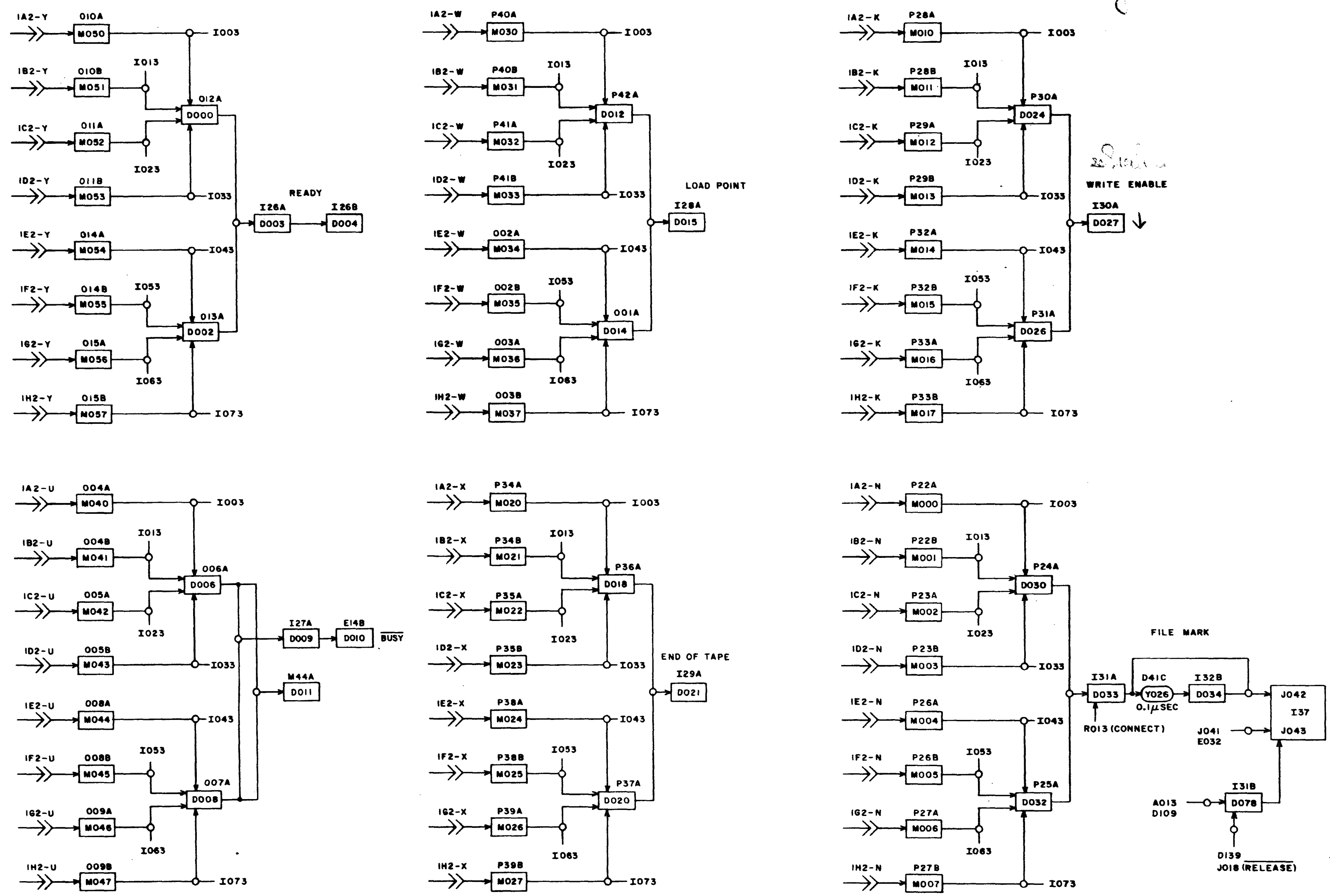
SHEET 5

PAGE 5

TERM	LOCATION	PAGE	DEFINITION
A013	S21B	1	
D109	D37A	3	
D139	D36B	3	
E032	J22B	14	
I003	N05B	4	
I013	N12B	4	
I023	N19B	4	
I033	N26B	4	
I043	N33B	4	
I053	N40B	4	
I063	M02B	4	
I073	M09B	4	
J018	C33	3	
J041	E18	3	
R013	S19B	1	

FORM 510

45



CONTROL DATA CORPORATION
COMPUTER DIVISION

3228 / 3229-A

REPLIES FROM 60X (PART 1 OF 2)

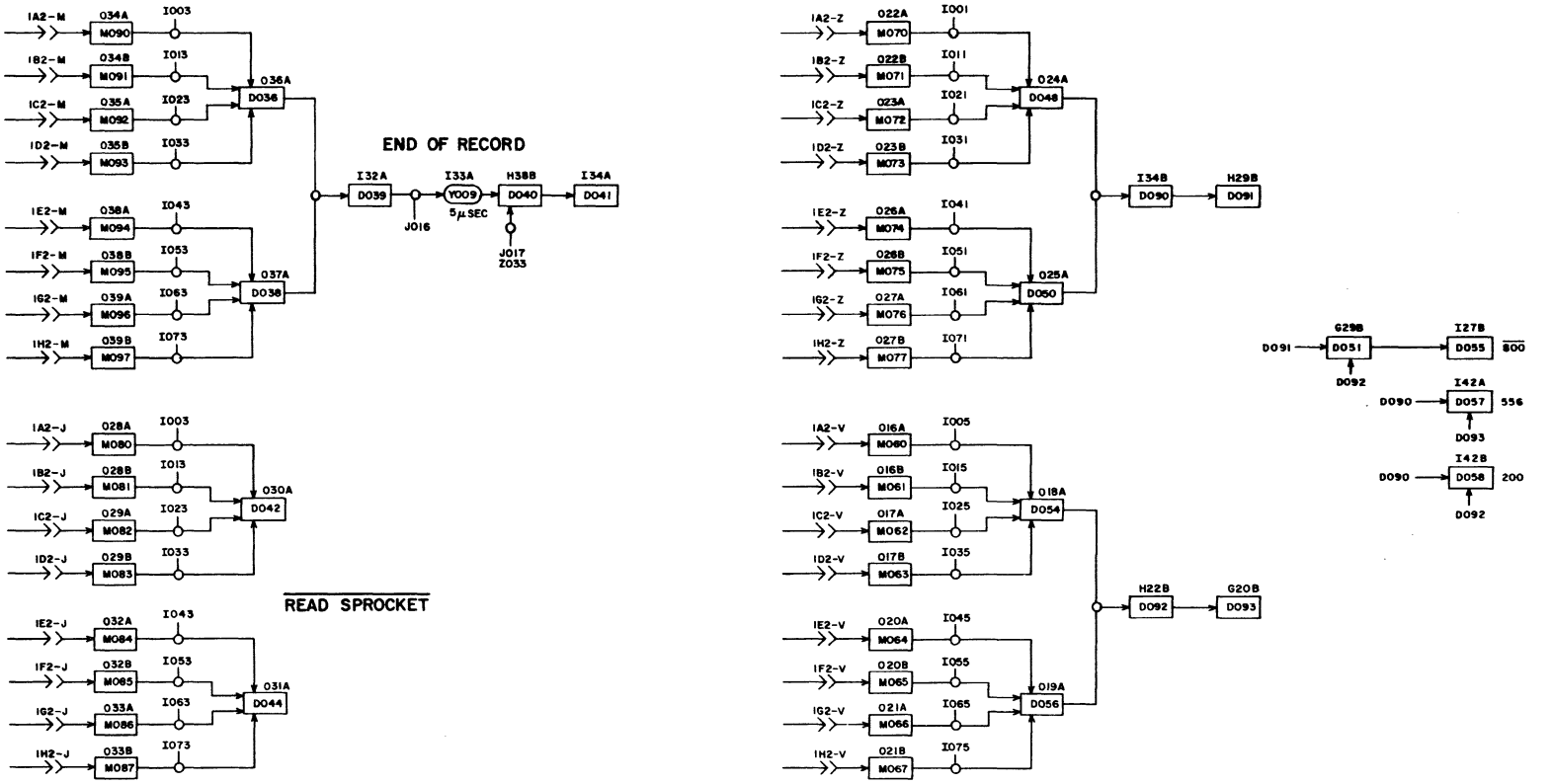
60093700 | REV F

SHEET 6 | PAGE 6

TERM	LOCATION	PAGE	DEFINITION
I001	N03B	4	
I003	N05B	4	
I005	I02A	4	
I011	N10B	4	
I013	N12B	4	
I015	I04A	4	
I021	N17B	4	
I023	N19B	4	
I025	I07A	4	
I031	N24B	4	
I033	N26B	4	
I035	I09A	4	
I041	N13B	4	
I043	N33B	4	
I045	I12A	4	
I051	N38B	4	
I053	N40B	4	
I055	I14A	4	
I061	O42B	4	
I063	M02B	4	
I065	I17A	4	
I071	M07B	4	
I073	M09B	4	
I075	I20A	4	
J016	C31	3	
J017	C31	3	
Z033	F42	8	

FORM 510

ITL-7
Rev. F



47

DES. APPROVED						
REVISIONS						
DATE	-	-	-	-	-	1-23-64
APPROVED	-	-	-	-	-	
CHKD	-	-	-	-	-	
DRAWN	-	-	-	-	-	RDS

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE: REPLIES FROM 60X (PART 2 OF 2)

CONTROL DATA CORPORATION
COMPUTER DIVISION

PROJECT OR PRODUCT: 3228/3229-A

DRAWING NUMBER: 60093700 REV: F

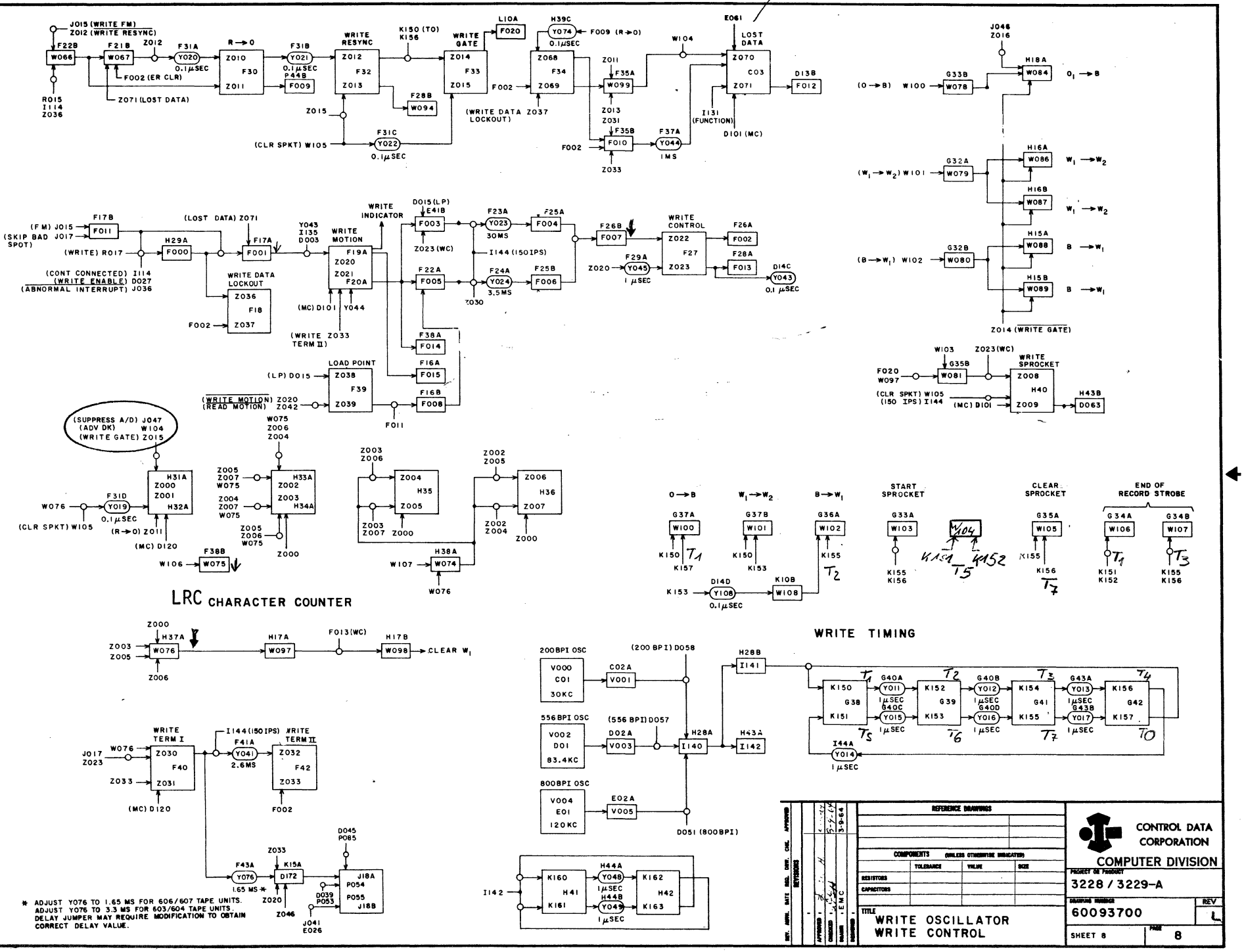
SHEET 7 PAGE 7

Note: All Terms Set in Alphanumeric Order

TERM	LOCATION	PAGE	DEFINITION
A022	P43A	1	
D003	I26A	6	
D015	I28A	6	
D027	I30A	6	
D045	D15B	11	
D051	G29B	7	
D057	I42A	7	
D058	I42B	7	
D101	H30A	3	
D118	E17B	3	
D120	D05A	3	
D124	D44A	3	
I101	C11A	2	
I114	C06A	2	
I131	E16B	3	
I143	K07A	11	
I144	K06B	11	
J015	C29	3	
J017	C31	3	
J036	D04A	3	
R015	S22B	1	
R017	S24B	1	
R022	Q44B	1	
Z042	D30A	11	
Z075	D26	11	
E061	L12A	11	
I143	K07A	11	
I144	K07B	11	
I135	E21B	9	
J046	K18A	3	
J047	K18C	3	
Z046	D18A	11	

FORM 510

ITL-8
Rev. K

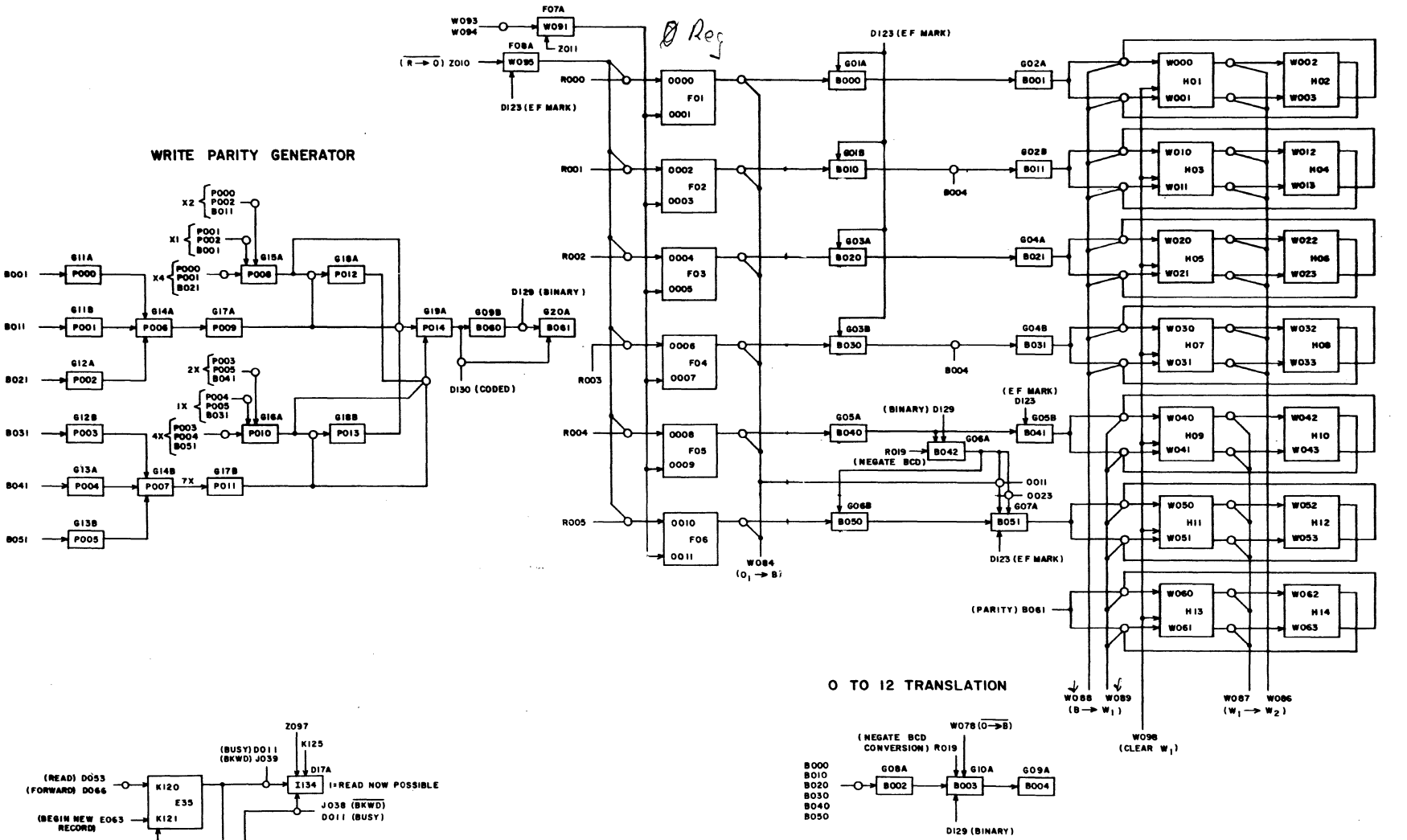

LRC CHARACTER COUNTER
WRITE TIMING
* ADJUST Y076 TO 1.65 MS FOR 606/607 TAPE UNITS. ADJUST Y076 TO 3.3 MS FOR 603/604 TAPE UNITS. DELAY JUMPER MAY REQUIRE MODIFICATION TO OBTAIN CORRECT DELAY VALUE.
CONTROL DATA CORPORATION
COMPUTER DIVISION
3228 / 3229-A
60093700
WRITE OSCILLATOR
WRITE CONTROL
SHEET 8
8

TERM	LOCATION	PAGE	DEFINITION
D010	E14B	6	
D011	M44A	6	
D047	I24A	5	
D053	I25	5	
D066	L10B	5	
D070	I36A	5	
D101	H30A	3	
D119	D04B	3	
D121	D05B	3	
D123	F09A	3	
D129	C35A	3	
D130	C36A	3	
D131	E14A	3	
E063	H30B	14	
F014	F38A	8	
I104	C12B	2	
J001	C23	3	
J038	C41	3	
J039	C41	3	
R000	S01A	1	
R001	S01B	1	
R002	S04A	1	
R003	S04B	1	

FORM CA 210

TERM	LOCATION	PAGE	DEFINITION
R004	S07A	1	
R005	S07B	1	
R006	S10A	1	
R007	S10B	1	
R008	S13A	1	
R009	S13B	1	
R010	S16A	1	
R011	S16B	1	
R019	S26B	1	
W078	G33B	8	
W084	H18A	8	
W085	H18B	8	
W086	H16A	8	
W087	H16B	8	
W088	H15A	8	
W089	H15B	8	
W094	F28B	8	
W098	H17B	8	
W104	G36B	8	
Z010	F30	8	
Z011	F30	8	
Z015	F33	8	
Z019	G31	8	

FORM CA 210



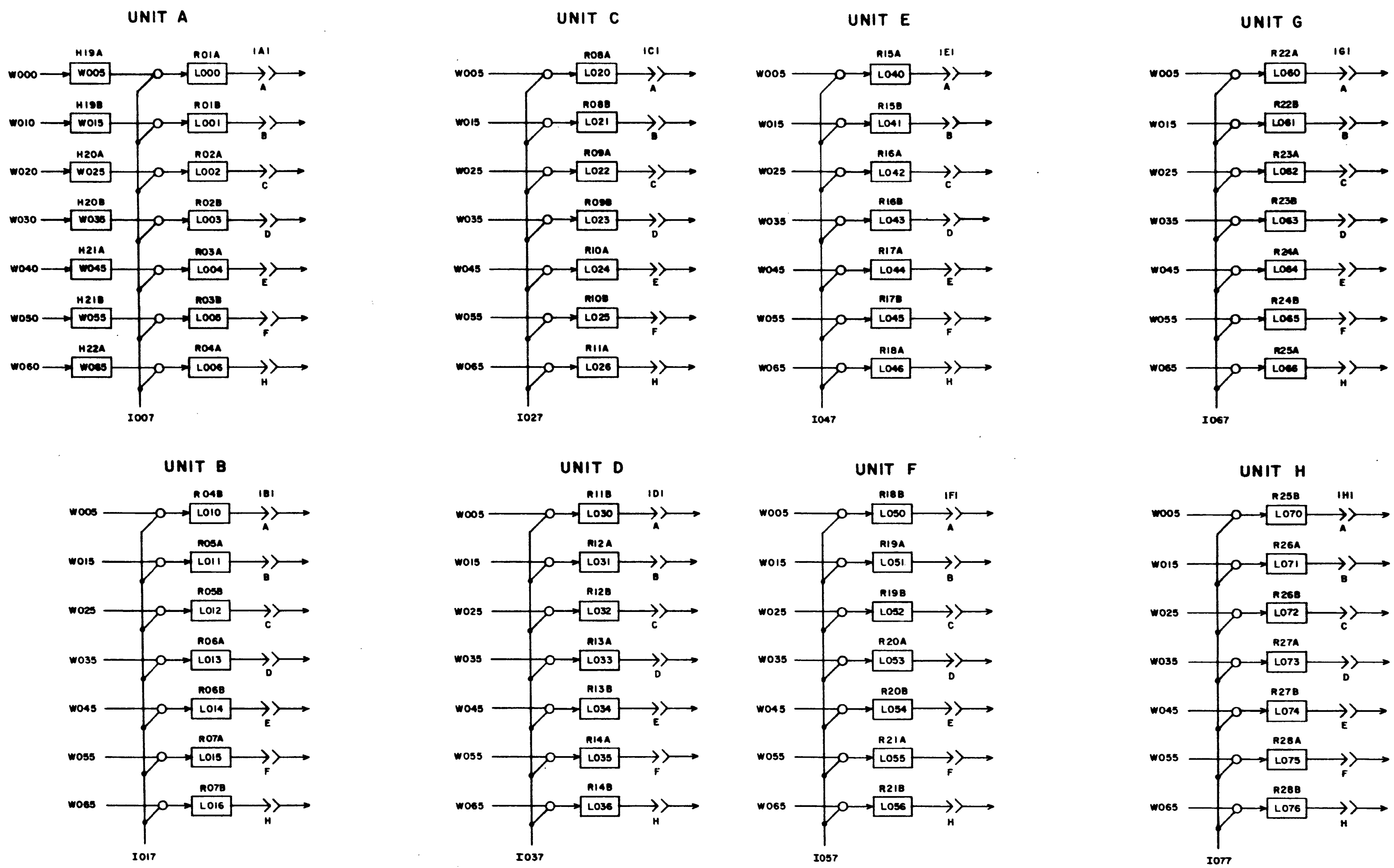
			CONTROL DATA CORPORATION
			COMPUTER DIVISION
			3228/3229-A
			60093700 REV F
			SHEET 9 PAGE 9

TITLE: WRITE REGISTER

51

TERM	LOCATION	PAGE	DEFINITION
I007	I02B	4	
I017	I04B	4	
I027	I07B	4	
I037	I09B	4	
I047	I12B	4	
I057	I14B	4	
I067	I17B	4	
I077	I20C	4	
W000	H01	9	
W010	H03	9	
W020	H05	9	
W030	H07	9	
W040	H09	9	
W050	H11	9	
W060	H13	9	

FORM 510



CONTROL DATA CORPORATION
COMPUTER DIVISION

PROJECT OR PRODUCT: 3228/3229-A

DRAWING NUMBER: 60093700

REV: F

TITLE: DATA OUTPUT

DRAWN: L. KOELLEN

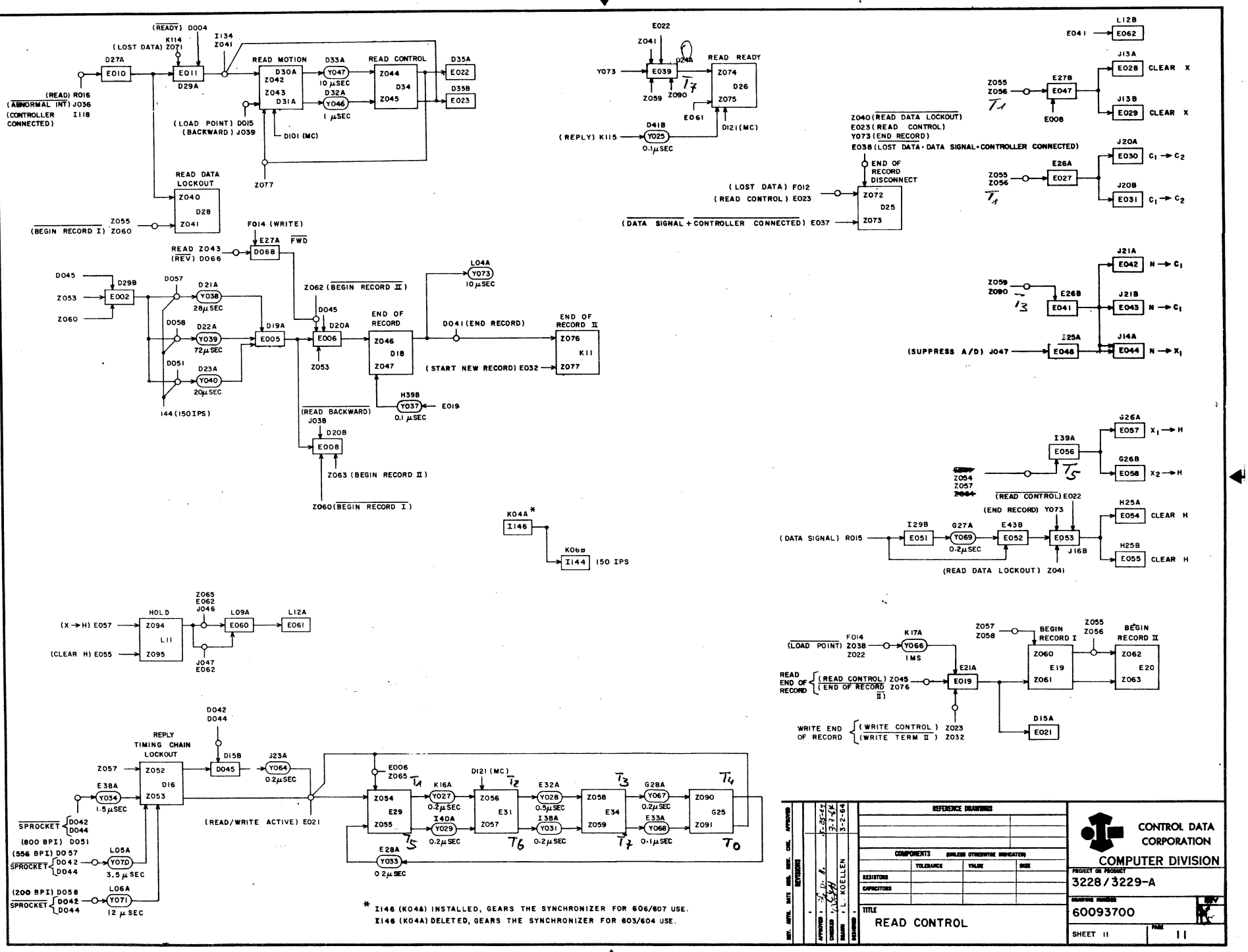
SHEET 10 PAGE 10

Note: All terms set in Alphanumeric order

TERM	LOCATION	PAGE	DEFINITION
D001	I26B	6	
D015	I28A	6	
D039	I32A	7	
D042	O30A	7	
D044	O31A	7	
D051	G29B	7	
D057	I42A	7	
D058	I42B	7	
D066	L10B	5	
D101	H30A	3	
D120	D05A	3	
D121	D05B	3	
D124	D44A	3	
D131	E14A	3	
E032	J22B	14	
E037	C14B	2	
E038	C13B	2	
F012	D13B	8	
F014	F38A	8	
I118	D13A	2	
J036	D04A	3	
J038	C41	3	
J039	C41	3	
K114	C16	2	
K115	C16	2	
R015	S22B	1	
R016	S24A	1	
Z022	F27	8	
Z023	F27	8	
Z034	F44	8	
Z038	F39	8	
Z070	C03	8	
Z071	C03	8	
J046	K18A	5	
J047	K18C	5	
I134	D17A	9	
Z032	F42	8	
D041	I34A	7	

FORM 510

ITL-11
Rev. K


(READY) D004
K114
(LOST DATA) Z071
I134
Z041
D27A
E010
E011
D29A
READ MOTION
D30A
Z042
Z043
D31A
D33A
Y047
10 μSEC
D32A
Y046
1 μSEC
READ CONTROL
Z044
D34
Z045
D35A
E022
D35B
E023
(READ) R016
(ABNORMAL INT) J036
(CONTROLLER CONNECTED) I118
(LOAD POINT) D015
(BACKWARD) J039
D101 (MC)
Z077
READ DATA LOCKOUT
Z040
D28
Z041
Z055
(BEGIN RECORD I) Z060
F014 (WRITE)
E27A
FWD
D068
READ Z043
(REV) D066
D045
Z053
Z060
D29B
E002
D057
D21A
Y038
28μSEC
D058
D22A
Y039
72μSEC
D051
D23A
Y040
20μSEC
144 (150IPS)
D19A
E005
D20A
E006
Z053
Z062 (BEGIN RECORD II)
END OF RECORD
Z046
D18
Z047
L04A
Y073
10μSEC
D041 (END RECORD)
END OF RECORD II
Z076
K11
Z077
(START NEW RECORD) E032
H39B
Y037
0.1 μSEC
E019
(READ BACKWARD) J038
D20B
E008
Z063 (BEGIN RECORD II)
Z060 (BEGIN RECORD I)
K04A *
I146
K06B
I144
150 IPS
E022
Z041
Y073
E039
D24A
READ READY
Z074
D26
Z075
Z059
Z090
E061
D121 (MC)
(REPLY) K115
D41B
Y025
0.1μSEC
E041
L12B
E062
J13A
E028
CLEAR X
J13B
E029
CLEAR X
Z055
Z056
E27B
E047
E008
Z040 (READ DATA LOCKOUT)
E023 (READ CONTROL)
Y073 (END RECORD)
E038 (LOST DATA · DATA SIGNAL · CONTROLLER CONNECTED)
END OF RECORD DISCONNECT
(LOST DATA) F012
(READ CONTROL) E023
(DATA SIGNAL + CONTROLLER CONNECTED) E037
Z072
D25
Z073
J20A
E030
C1 → C2
J20B
E031
C1 → C2
E26A
E027
Z059
Z090
E26B
E041
J21A
E042
N → C1
J21B
E043
N → C1
E25A
E048
J14A
E044
N → X1
(SUPPRESS A/D) J047
I39A
E056
G26A
E057
X1 → H
G26B
E058
X2 → H
Z054
Z057
(READ CONTROL) E022
(END RECORD) Y073
H25A
E054
CLEAR H
H25B
E055
CLEAR H
J16B
(DATA SIGNAL) R015
I29B
E051
G27A
Y069
0.2μSEC
E43B
E052
E053
(READ DATA LOCKOUT) Z041
(X → H) E057
(CLEAR H) E055
HOLD
Z094
L11
Z095
Z065
E062
J046
J047
E062
L09A
E060
L12A
E061
(LOAD POINT) F014
Z038
Z022
K17A
Y066
1MS
READ END OF RECORD
(READ CONTROL) Z045
(END OF RECORD II) Z076
E21A
E019
Z057
Z058
BEGIN RECORD I
Z060
E19
Z061
Z055
Z056
BEGIN RECORD II
Z062
E20
Z063
WRITE END OF RECORD
(WRITE CONTROL) Z023
(WRITE TERM II) Z032
D15A
E021
D042
D044
REPLY TIMING CHAIN LOCKOUT
Z052
D16
Z053
D15B
D045
J23A
Y064
0.2μSEC
Z057
E38A
Y034
1.5μSEC
SPROCKET
D042
D044
(800 BPI) D051
(556 BPI) D057
SPROCKET
D042
D044
L05A
Y070
3.5 μSEC
(200 BPI) D058
SPROCKET
D042
D044
L06A
Y071
12 μSEC
(READ/WRITE ACTIVE) E021
E006
Z065
T1
Z054
E29
Z055
K16A
Y027
0.2μSEC
I40A
Y029
0.2μSEC
D121 (MC)
T2
Z056
E31
Z057
E32A
Y028
0.5μSEC
I38A
Y031
0.2μSEC
T3
Z058
E34
Z059
G28A
Y067
0.2μSEC
E33A
Y068
0.1μSEC
T4
Z090
G25
Z091
T0
E28A
Y033
0.2μSEC
T5
T6
T7
* I146 (K04A) INSTALLED, GEARS THE SYNCHRONIZER FOR 606/607 USE.
I146 (K04A) DELETED, GEARS THE SYNCHRONIZER FOR 603/604 USE.
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE
VALUE
SIZE
RESISTORS
CAPACITORS
APPROVED
CHECKED
DRAWN
DESIGNED
J. L. KOELLEN
3-2-64
TITLE
READ CONTROL
CONTROL DATA CORPORATION
COMPUTER DIVISION
PROJECT OR PRODUCT
3228/3229-A
DRAWING NUMBER
60093700
REV
SHEET 11
PAGE 11

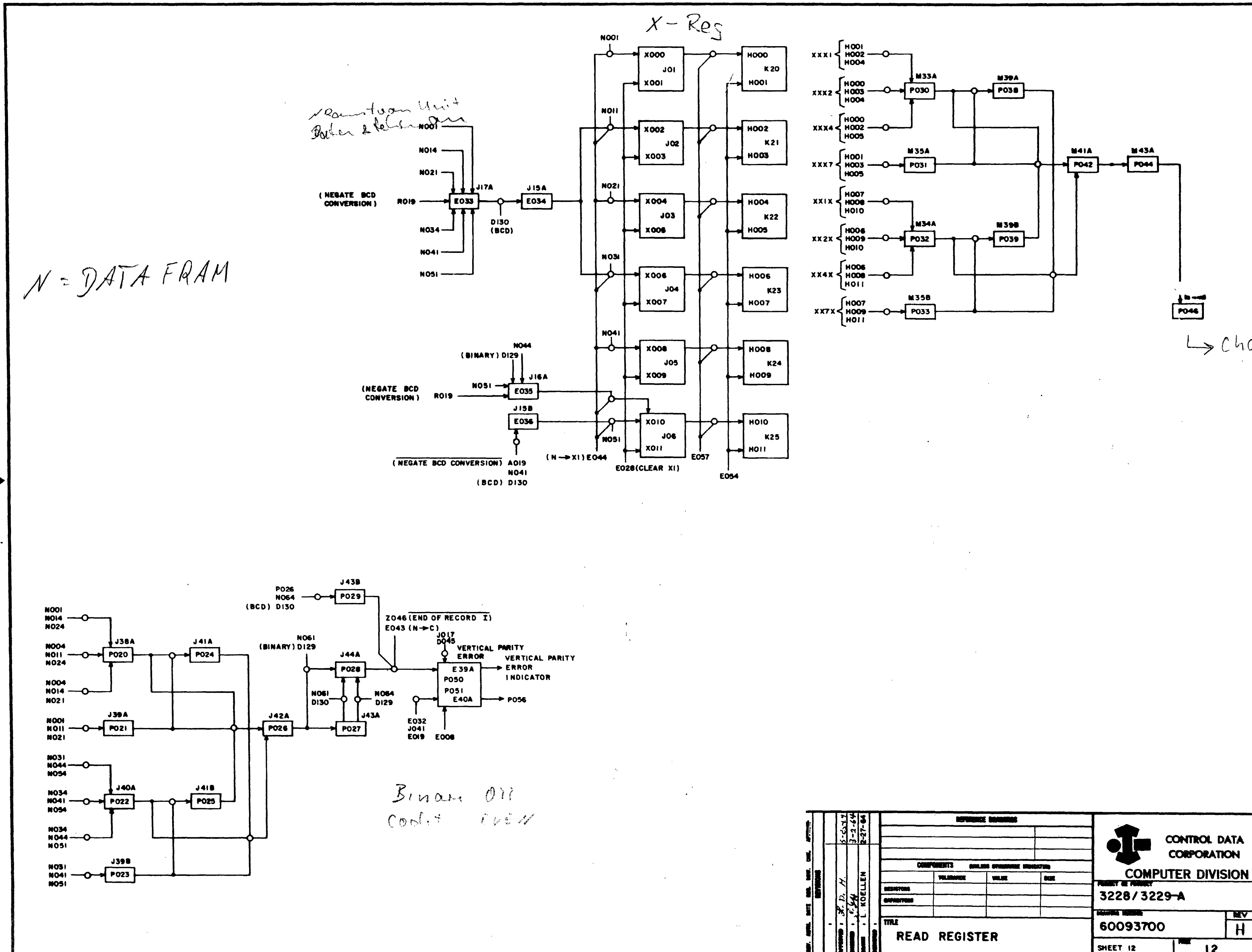
Note: All Terms Not in Alphanumeric Order

TERM	LOCATION	PAGE	DEFINITION
A019	S30A	1	
D045	D15B	11	
D129	C35A	5	
D130	C36A	5	
E008	J20B	11	
E029	J13B	11	
E032	J22B	11	
E043	J21B	11	
E046	J14B	11	
E054	H25A	11	
E055	H25B	11	
E057	G26A	11	
E058	G26B	11	
J041	E18	3	
N001	M26A	13	
N011	M27A	13	
N014	M27B	13	
N021	M28A	13	
N031	M29A	13	
N034	M29B	13	
N041	M30A	13	
N044	M30B	13	
N051	M31A	13	
N053	I35B	13	
N061	M32A	13	
N064	M32B	13	
P056	S30B	1	
R019	S26B	1	
Z046	D18	11	
E019	E21A	11	
J017	C31	3	

FORM 510

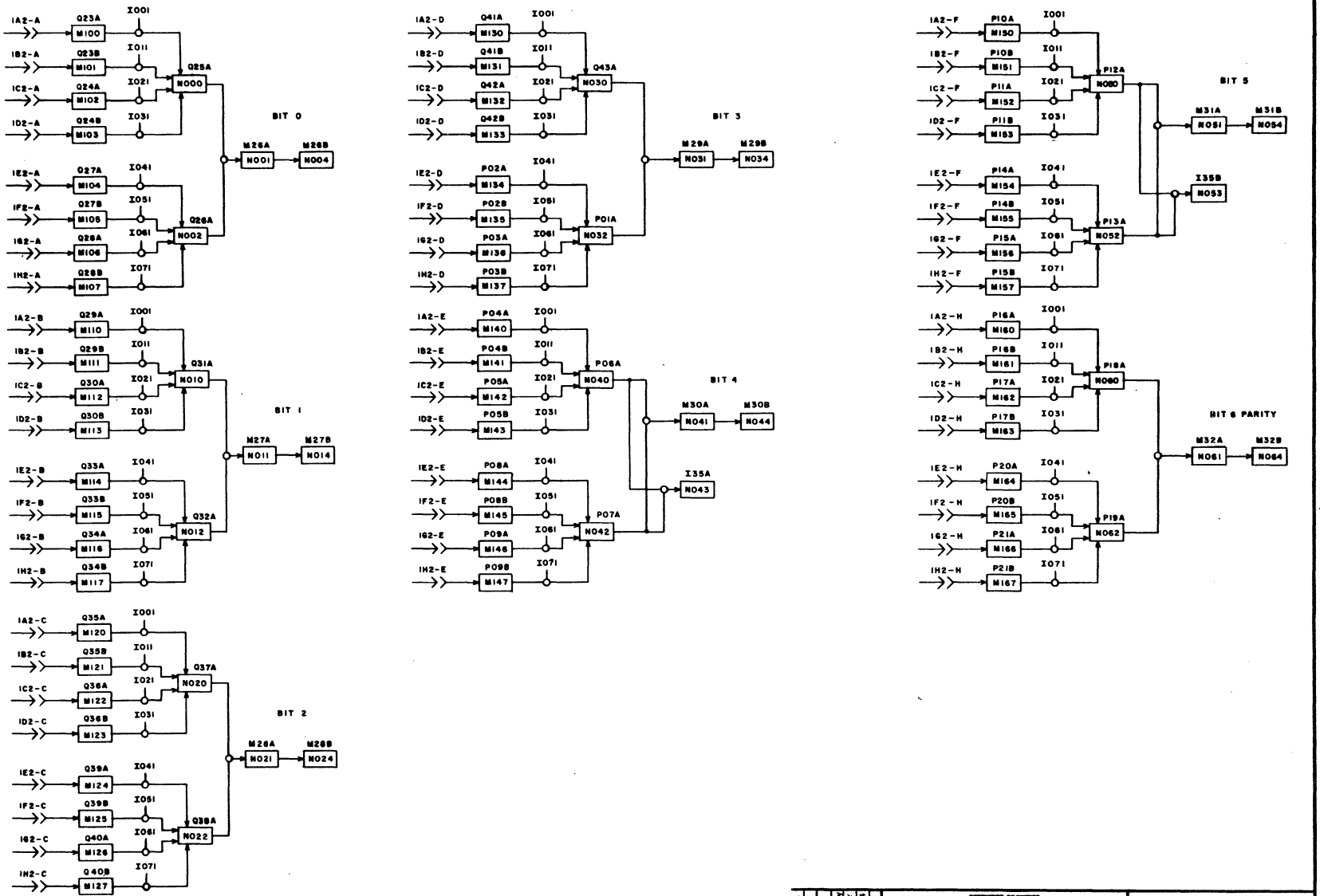
ITL-12
Rev. H

57


X-Res
N = DATA FRAM
(NEGATE BCD CONVERSION)
R019
E033
J17A
J15A
E034
D130 (BCD)
N001
N014
N021
N034
N041
N051
N011
N031
X000 J01 X001
X002 J02 X003
X004 J03 X005
X006 J04 X007
X008 J05 X009
X010 J06 X011
H000 K20 H001
H002 K21 H003
H004 K22 H005
H006 K23 H007
H008 K24 H009
H010 K25 H011
(BINARY) D129
N044
J16A
E035
J15B
E036
(NEGATE BCD CONVERSION) A019
(BCD) D130
(N→X1) E044
E028 (CLEAR X1)
E057
E054
XXX1
XXX2
XXX4
XXX7
XX1X
XX2X
XX4X
XX7X
M33A
P030
M39A
P038
M35A
P031
M41A
P042
M43A
P044
M34A
P032
M39B
P039
M35B
P033
P046
Chanel
J38A
P020
J41A
P024
J39A
P021
J42A
P026
J40A
P022
J41B
P025
J39B
P023
J43B
P029
J44A
P028
J43A
P027
(BINARY) D129
N061
N064
Z046 (END OF RECORD I)
E043 (N→C)
J017
D045
VERTICAL PARITY ERROR
E39A
P050
P051
E40A
VERTICAL PARITY ERROR INDICATOR
P056
E032
J041
E019
E008
CONTROL DATA CORPORATION
COMPUTER DIVISION
3228/3229-A
60093700
H
READ REGISTER
SHEET 12
12
L. KOELLEN

TERM	LOCATION	PAGE	DEFINITION
I001	N03B	4	
I011	N10B	4	
I021	N17B	4	
I031	N24B	4	
I041	N13B	4	
I051	N38B	4	
I061	O42B	4	
I071	N07B	4	

FORM 510



DRT.				
APPROVED				
CHECKED				
ISSUED				
DESIGNED				

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	USE
RESISTORS			
CAPACITORS			

TITLE

READ REPLIES FROM 606

CONTROL DATA CORPORATION
COMPUTER DIVISION

PROJECT OR PRODUCT
3228/3229-A

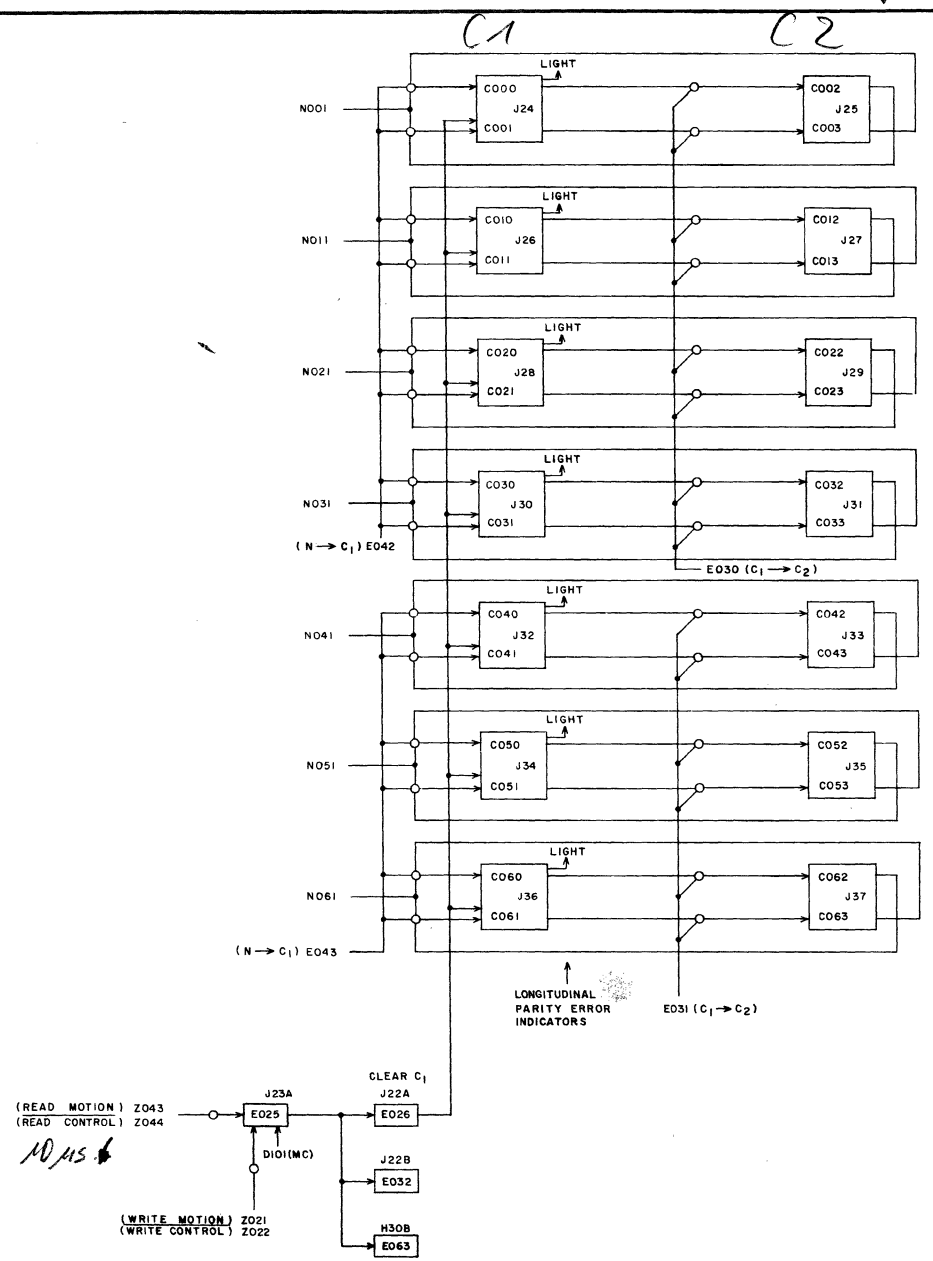
DRAWING NUMBER
60093700

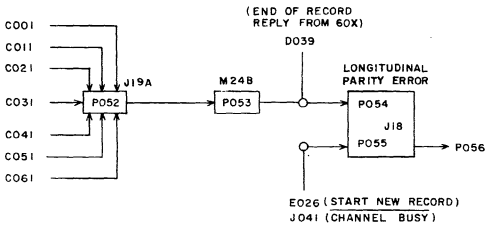
REV
F

SHEET 13

PAGE
13

TERM	LOCATION	PAGE	DEFINITION
D039	I32A	7	
D101	H30A	3	
E030	J20A	11	
E031	J20B	11	
E042	J21A	11	
E043	J21B	11	
J041	E18	3	
N001	M26A	13	
N011	M27A	13	
N021	M28A	13	
N031	M29A	13	
N041	M30A	13	
N051	M31A	13	
N061	M32A	13	
P056	S30B	1	
Z021	F20A	8	
Z022	F27	8	
Z043	D31A	11	
Z044	D34	11	





LONGITUDINAL PARITY CHECKER

61

REFERENCE DRAWINGS				
COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE	
RESISTORS				
CAPACITORS				

TITLE: LONGITUDINAL PARITY CHECKER

CONTROL DATA CORPORATION
COMPUTER DIVISION

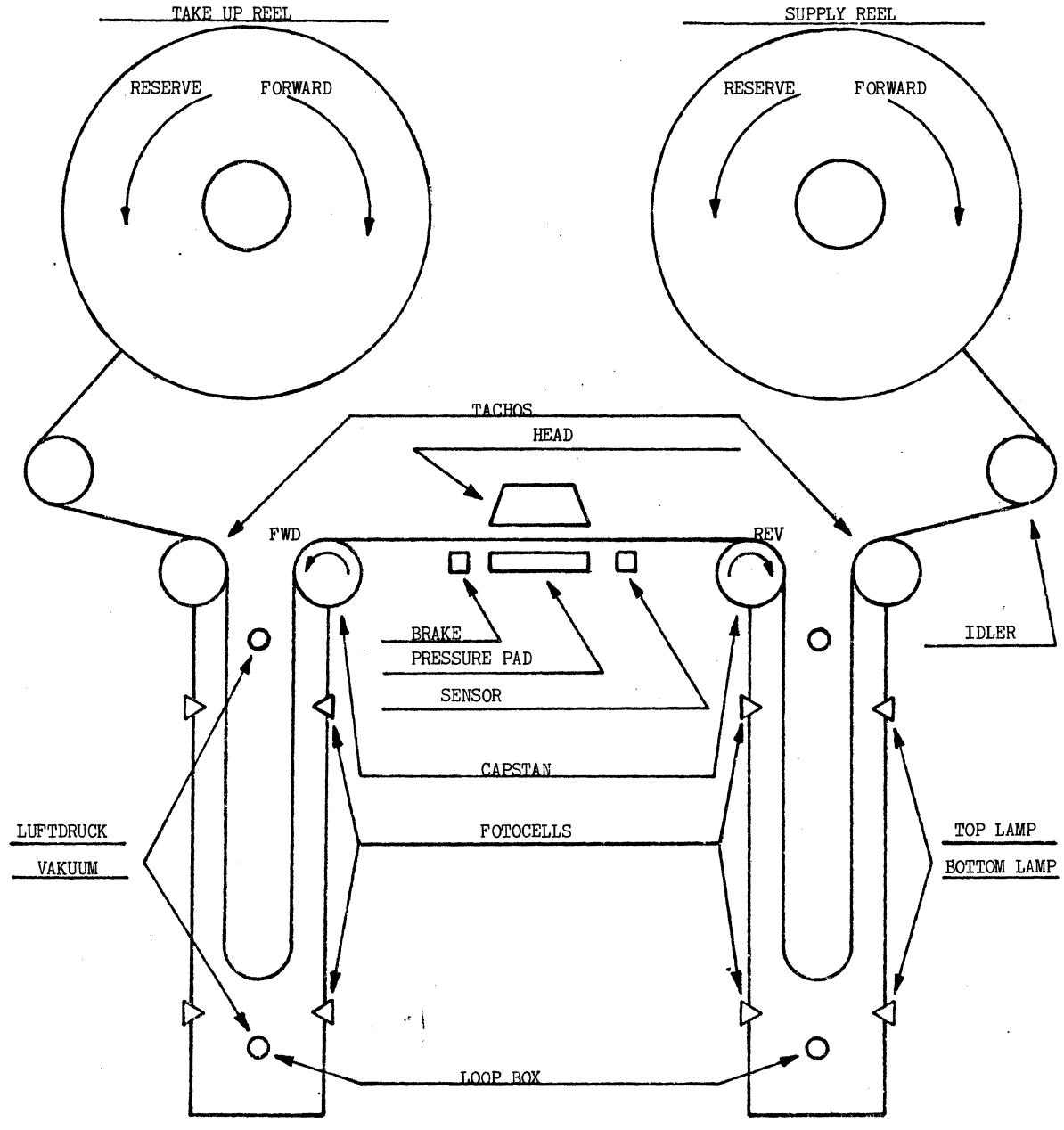
PROJECT OR PRODUCT: 3228/3229-A

DRAWING NUMBER: 60093700 REV J

SHEET 14 PAGE 14

DRAWN: L. KOELLEN 2-27-64
APPROVED: 5-5-64
CHECKED: 5-6-64

1A. TAPE MOVEMENT



1B. MAGNETIC TAPE FORMAT