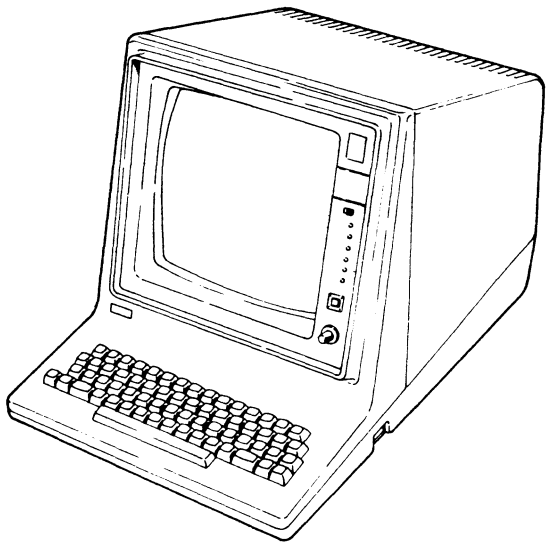
82100083

CONTROL DATA CORPORATION

CDC® INFORMATION SYSTEMS TERMINAL II



HARDWARE MAINTENANCE MANUAL (SITE AND SUPPORT INFORMATION)

CAUTION

BEFORE READING THIS MANUAL, REVIEW FEDERAL COMMUNICATIONS COMMISSION REGULATIONS FOUND IN APPENDIX A. ALSO, ONLY TRAINED CDC PERSONNEL ARE AUTHORIZED TO MAKE REPAIRS TO THIS TERMINAL.

REVISION RECORD

REVISION	DESCRIPTION
A (09-10-79)	Final release; includes ECOs 13578, 13614, 13632, and 13656.
B (09-27-79)	Manual revised to reflect technical corrections.
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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCO'S	COMMENTS
FC816-A	01		
FC816-B	01		
XA243-A	01		

01987-2

MANUAL TO EQUIPMENT LEVEL CORRELATION (CONTD)

EQUIPMENT TYPE	SERIES	WITH FCO'S	COMMENTS
XA244-A	01		
XA247-A	01		

01987-3

LIST OF EFFECTIVE PAGES

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PREFACE

The CDC® Information Systems Terminal II Hardware Maintenance Manual contains site and support information. Sections contained in this manual are:

- General Description
- Operation
- Installation and Checkout
- Theory of Operation
- Diagrams
- Maintenance
- Parts Data
- Wire Lists

Appendix A contains the Federal Communications Commission Regulations.

Additional reference and hardware maintenance information applicable to the terminal is provided in the following publications.

Title	Publication Number
PLATO Terminal User's Guide	97404800
+5-Volt Regulator Hardware Maintenance Manual	62960700
Processor Module Hardware Maintenance Manual	62960000
Key to Logic Symbology for Terminal Equipment Manual	82172400

This manual and the previously listed manuals may be ordered from:

Control Data Corporation
Literature and Distribution Services
304 North Dale Street
St. Paul, Minnesota 55103

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4. THEORY OF OPERATION

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7. PARTS DATA

The basic terminal is a stand-alone device that operates in the CDC® PLATO Education Network.* This section discusses the terminal configuration, controller, internal modem, communication line interfaces, and terminal characteristics.

TERMINAL CONFIGURATION

An illustration of the terminal is shown in figure 1-1. The following paragraphs discuss the display, operator's panel, touchpanel, keyboard, and the enclosure.

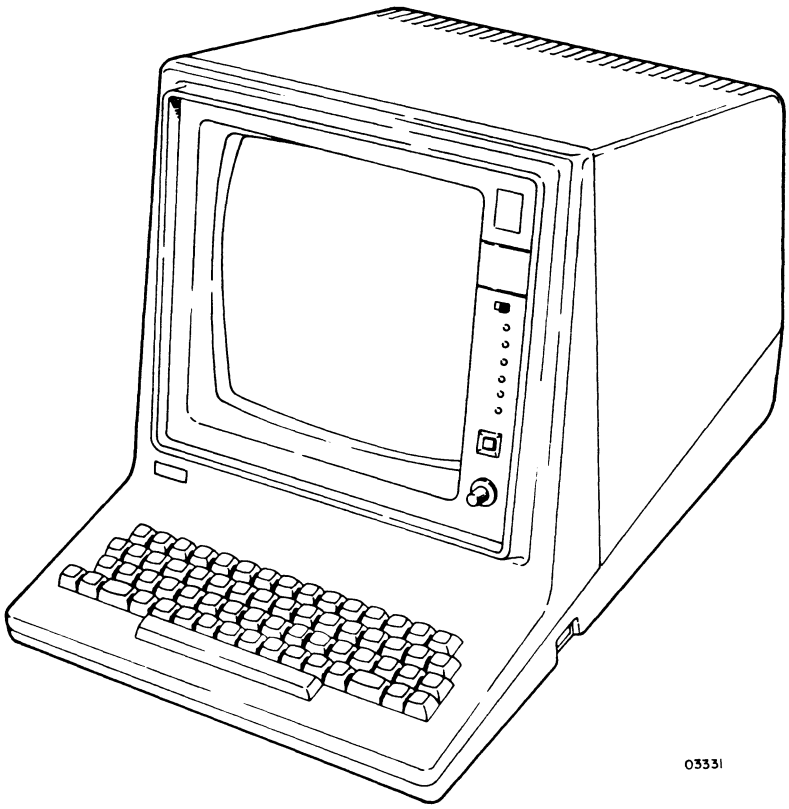


Figure 1-1. Terminal

*PLATO is an acronym for Programmed Logic for Automated Teaching Operations.

DISPLAY

The display is a noncomposite video display which receives vertical and horizontal sync pulses to deflect an electron beam in the cathode-ray tube (crt). The video information received is used to unblank the crt at proper times to present data on the screen. The display consists of electronics, yoke, flyback transformer, brightness potentiometer, high-voltage rectifier, and a crt.

The active display area is a raster of 512 by 512 picture elements which is refreshed in the noninterlaced mode. These 262,144 picture elements are individually programmable (ON or OFF). The active display area is approximately 8.5 in by 8.5 in (216 mm by 216 mm).

OPERATOR'S PANEL

This panel, located on the right of the bezel, contains all of the external indicators and controls, except for the POWER ON/OFF switch. These indicators and controls are described in section 2.

TOUCHPANEL

The touchpanel forms a 16 by 16 matrix of 0.5 in by 0.5 in (13 mm by 13 mm) square touch-sensitive areas, overlaid on the display screen. Pressure applied to the touchpanel/display surface interrupts the x and y scanning mechanism. When a touch is detected, the interface logic captures the intersecting X/Y coordinates for further processing, and an audible tone is produced.

KEYBOARD

The terminal keyboard provides for operator entry of specific symbol and control codes. When a key is pressed, a 7-bit code is sent to the control section of the terminal. It thus passes to the central computer for interpretation before data returns to the terminal for display.

Interpretation of the code by the central computer allows the code to be redefined before display. When used in conjunction with the computer software, the keyboard can communicate a limitless number of characters, lines, and symbols.

ENCLOSURE

The terminal is housed in a four-part integral housing consisting of the base, hood, bezel/keyboard cover, and display/touchpanel mask.

All the components, except the touchpanel brightness control, and operator's panel, fasten to the base. The removable hood gives access to all the modules of the terminal, except for the keyboard, touchpanel, and operator's panel.

CONTROLLER

The controller portion consists of two printed-circuit logic boards: the controller board and the video board.

CONTROLLER BOARD

The controller board provides the control function and processing capability required to support the input and output operations and to manage their interactions. Examples of control functions are:

a. Character generation
b. Line generation
c. Instruction decoding and execution
d. Routing of messages for peripheral devices
e. Interrupt recognition and processing

The processor inputs data from, or outputs data to, the devices/interfaces listed in table 1-1.

TABLE 1-1. DEVICE INPUTS AND OUTPUTS

DEVICE	MICROPROCESSOR INPUT/OUTPUT
Memory	Both
Keyboard	Input
PLATO communication interface	Both
Serial channel	Both
Maintenance LEDs	Output
Switches	Input
ID code setting	Input
Touchpanel	Input
Parallel channel	Both
Interrupt mask	Output

VIDEO BOARD

The video board provides timing and memory to support the controller board and the display module. Features are:

a. 32K 8-bit words of RAM for crt refresh

b. 16K 8-bit words of RAM for programs (basic memory)

c. Provision for 16K 8-bit words of RAM expansion

d. 2K 8-bit words of ROM/EROM for terminal diagnostic and loader program

e. Timing generation for the display, memory, and controller board

f. Composite video output for external devices

The video board has in it the supporting logic for the memory expansion, including sockets where the memory chips are inserted. This feature expands the basic 48K-word RAM to 64K words (8-bit words). This increases the capacity of the random-access memory dedicated for programs from 16K to 32K 8-bit words. This memory expansion feature consists of the addition of eight memory chips.

INTERNAL MODEM

The internal modem PC board is a FSK (Frequency Shift Key) data modem designed for asynchronous operation on a voice-grade telephone line. Features are:

- RS-232-C interface to the terminal for transmitted and received data
- Forward (receive) channel 1300-Hz mark, 2100-Hz space binary, FSK modulated signal
- Reverse (transmit) channel 390-Hz mark, 490-Hz space binary FSK modulated signal.
- Receive data rate up to 1200 bps on unconditioned dial-up line
- Transmit data rate 0 to 150 bps
- Line impedance is 600 ohms balanced
- Operation is full duplex on a two-wire, dial-up line
- Transmitter output level is -9 dBm (+0, -4 dBm)
- Receiver input level is from -10 dBm to -43 dBm

POWER SUPPLY

The basic power supply is designed for 120-V ac, 50/60-Hz, or 220/240-V ac, 50/60-Hz input. However, the 220/240-volt operation requires a different ac entry panel. Regulated output voltages generated are:

- +55 volts
- +12 volts
- +5 volts
- -5 volts
- -12 volts

INTERFACES

Three interfaces are bidirectional: - serial channel, PLATO communication, and parallel channel. The terminal can be configured into several systems or communication networks.

SERIAL CHANNEL INTERFACE

The serial channel interface provides the terminal processor with an asynchronous, full duplex, bit-serial/ word-serial interface that meets the RS-232-C standard.

The transmitter voltage levels are:

$$-12.0\ V \leq \text{Mark or OFF} < -3.0\ V$$
$$+3.0\ V < \text{Space or ON} \leq +12.0\ V$$

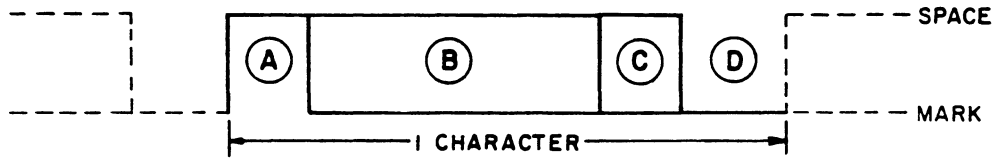
Slew rate is 30 V per microsecond or less.

The receiver voltage levels are:

$$-22.0\ V \leq \text{Mark or OFF} < +0.8\ V$$
$$+0.8\ V \leq \text{Undefined} \leq +2.0\ V$$
$$+2.0\ V < \text{Space or ON} \leq +22.0\ V$$

Open input gives a mark or OFF state (fail-safe condition).

The send-data and receive-data serial information is asynchronous having the format shown in figure 1-2.



(A) 1 START BIT (SPACE OR HIGH)
(B) 5, 6, 7, OR 8 DATA BITS (1=MARK OR LOW, 0=SPACE OR HIGH)
(C) 1 OR NO PARITY BIT (EVEN OR ODD)
(D) 1, 1.5, OR 2 STOP BITS (MARK OR LOW)

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Figure 1-2. Serial Word Format

The transmitter idles in the mark state.

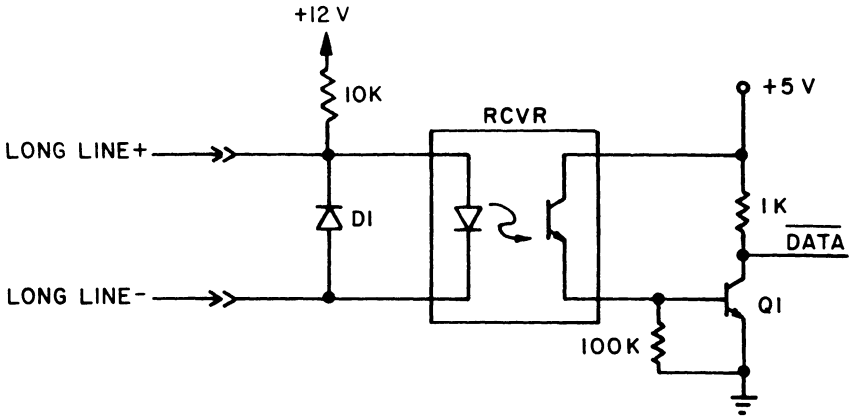
Both the receive and send portions must operate with the same format (number of data bits, parity) and baud rates.

PLATO COMMUNICATION INTERFACE

This PLATO network-compatible communication interface allows asynchronous reception of 21-bit words at a nominal 1200 bps, and asynchronous transmission of 12-bit words at a nominal 75, 120, or 1200 bps (switch selectable) via RS-232-C or optically-coupled long line interface circuits.

This long line receiver is basically a light-emitting diode/phototransistor circuit. The sending device should provide enough current to drive the LED to the on state to transmit a logical 1, and turn the current off to transmit a logical 0. Figure 1-3 shows the typical long line receiver circuit.

The long line receiver data is ORed with the RS-232-C data. An internal switch determines which of the two signal inputs is to be used by the terminal.



RCVR = MCT2F, CDC PART NUMBER 95791300
Q1 = TRANSISTOR NPN, CDC PART NUMBER 51003059
D1 = DIODE IN4148, CDC PART NUMBER 51007385

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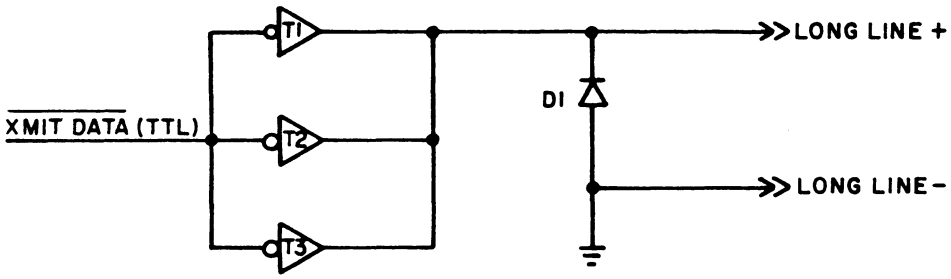
Figure 1-3. Long Line Receiver

When long line transmitter is more positive than long line receiver, the LED will conduct and emit light, causing the NPN phototransistor in the receiver to conduct. This, in turn, will increase the voltage at the base of Q1, turning Q1 on and lowering the output (collector) to a TTL low. When long line transmitter is equal to or lower than long line receiver, the LED will be off and the output of Q1 high.

Therefore, the data is inverted by the receiver. The diode across the input lines prevents the LED from being reverse biased.

The long line driver lines, when enabled, provide the source and sink current required to match the long line receivers. Figure 1-4 shows the typical long line driver circuit.



T1, T2, AND T3 = RS-232-C DRIVERS (MC1488), CDC PART NUMBER 36186400

DI = DIODE 1N4148, CDC PART NUMBER 51007385

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Figure 1-4. Long Line Driver

These three drivers connected in parallel can drive a long line receiver (figure 1-4) 10 000 feet (3000 metres) when using the proper cable.

The diode prevents the long line transmitter from going more negative than the diode forward bias drop (0.6 V), thus protecting the receiving LED from large reverse bias voltage.

A low TTL input to the driver will switch long line transmitter to a positive voltage, driving current through the load (receiver). This is the on state.

PARALLEL CHANNEL INTERFACE

The parallel channel interface provides a means for the terminal to communicate and exchange information with 16 addressable, external devices. Data is exchanged in bit-parallel/byte-serial mode, with the terminal processor controlling the interface.

All voltage levels on the parallel channel are TTL compatible, defined as follows:

Terminal output

	Data Lines	Others
High	+2.0 V ≤ High ≤ +5.25 V	+2.4 ≤ High ≤ +5.25 V
Low	+0.0 V ≤ Low ≤ +0.4 V	+0.0 ≤ Low ≤ +0.4 V

Terminal input

	Data Lines	Others
High	+2.0 V ≤ High ≤ +5.25 V	+2.4 V ≤ High ≤ +5.25 V
Low	-0.25 V ≤ Low ≤ +0.8 V	+0.25 V ≤ Low ≤ +0.5 V

TERMINAL CHARACTERISTICS

The following are physical, electrical, environmental, performance characteristics, as well as I/O signal cables and grounding requirements of the terminal.

PHYSICAL CHARACTERISTICS

The terminal has the following dimensions and weights:

Width:	15.75 in (400 mm)
Height:	16.5 in (419 mm)
Depth:	23.75 in (603 mm)
Weight:	45 lb (20.5 kg), 60 Hz
	53 lb (24.0 kg), 50 Hz
	120-V ac = 45 lbs (20.5 kg)
	220/240-V ac = 53 lbs (24.1 kg)

ELECTRICAL CHARACTERISTICS

The electrical power requirements for the domestic terminal, are listed below. The electrical power requirements for the international unit, are listed within parentheses in the cases where they differ from the domestic unit.

Voltage: 120 V ac (220/240 V ac)
Phase: Single
Frequency: 60 Hz (50 Hz)
Current: 1.4 A (0.7 A)
Power Consumption: 0.154 kVA

ENVIRONMENTAL CHARACTERISTICS

The terminal has the following environmental characteristics:

Operating Temperature: 50°F to 105°F (10°C to 40°C)

Recommended Operating Temperature: 75°F (24°C)

Storage Temperature: -40°F to 158°F (-40°C to 70°C)

Maximum Temperature Gradient: 18°F/h (10°C/h)

Operating Relative Humidity: 10% to 90% (no condensation)

Storage Relative Humidity: 0% to 100% (no condensation)

Humidity Gradient: 10%/h

Maximum Operating Altitude: 9850 ft (3000 m)

Heat Dissipation: 278 W (400 Btu/h)

Cooling: Natural Convection

PERFORMANCE CHARACTERISTICS

The Plato Interface has the following maximum performance characteristics.

Input Data Rate: 1200 bps
Output Data Rate: 1200 bps
Characters per Second: 171
Lines per Second: 57
Point Plots per Second: 57

I/O SIGNAL CABLES

The following list details the signal cables used by the terminal.

Connects Between	Number of Pins	Standard Length	Maximum Length	Mating Connector
Terminal (RJ1) and Communications Network	25		10,000 ft (3000 m)	CDC 53397814
Terminal and Supplemental Equipment				
Parallel Channel (RJ2)	25		5 ft (1.5 m)	CDC 53397914
Serial Channel RS232C(RJ3)	25		50 ft (15 m)	CDC 53397814
Composite Video BNC Connector			500 ft (150 m)	Standard BNC Plug
Telephone Connector		14 ft (4.3 m)		51917911

GROUNDING

No special grounding requirements are necessary for this terminal. A safety ground is provided through the three-pin ac power plug when connected to a properly grounded site outlet.

This section describes the location and function of all external controls, indicators and connectors, and all internal controls and indicators of the terminal. Terminal operating procedures are described in the Control Data PLATO Terminal User's Guide (refer to the preface of this manual for the publication number). Use of these controls and indicators for maintenance purposes is described in section 6 of this manual.

EXTERNAL CONTROLS, INDICATORS, AND CONNECTORS

The following paragraphs describe the function of the external controls, indicators, and connectors.

EXTERNAL CONTROLS

The locations of the external controls and indicators are illustrated in figure 2-1. They are:

- Alphanumeric keyboard
- Power ON/OFF switch
- Brightness Control
- RESET switch
- DATA/TALK switch
- Parameter/Mode switches

Alphanumeric Keyboard

The terminal keyboard, figure 2-2, is discussed in the PLATO Terminal User's Guide. Input codes are discussed in section 4 of this manual.

Power ON/OFF Switch

This is a horizontal rocker switch serving as both a circuit breaker and power switch.

Since this switch disconnects all power from the terminal, the user must wait approximately 45 seconds after applying power to allow the crt filament to warm up. Following the application of ac power, the terminal automatically clears and all logical elements set to their initial status.

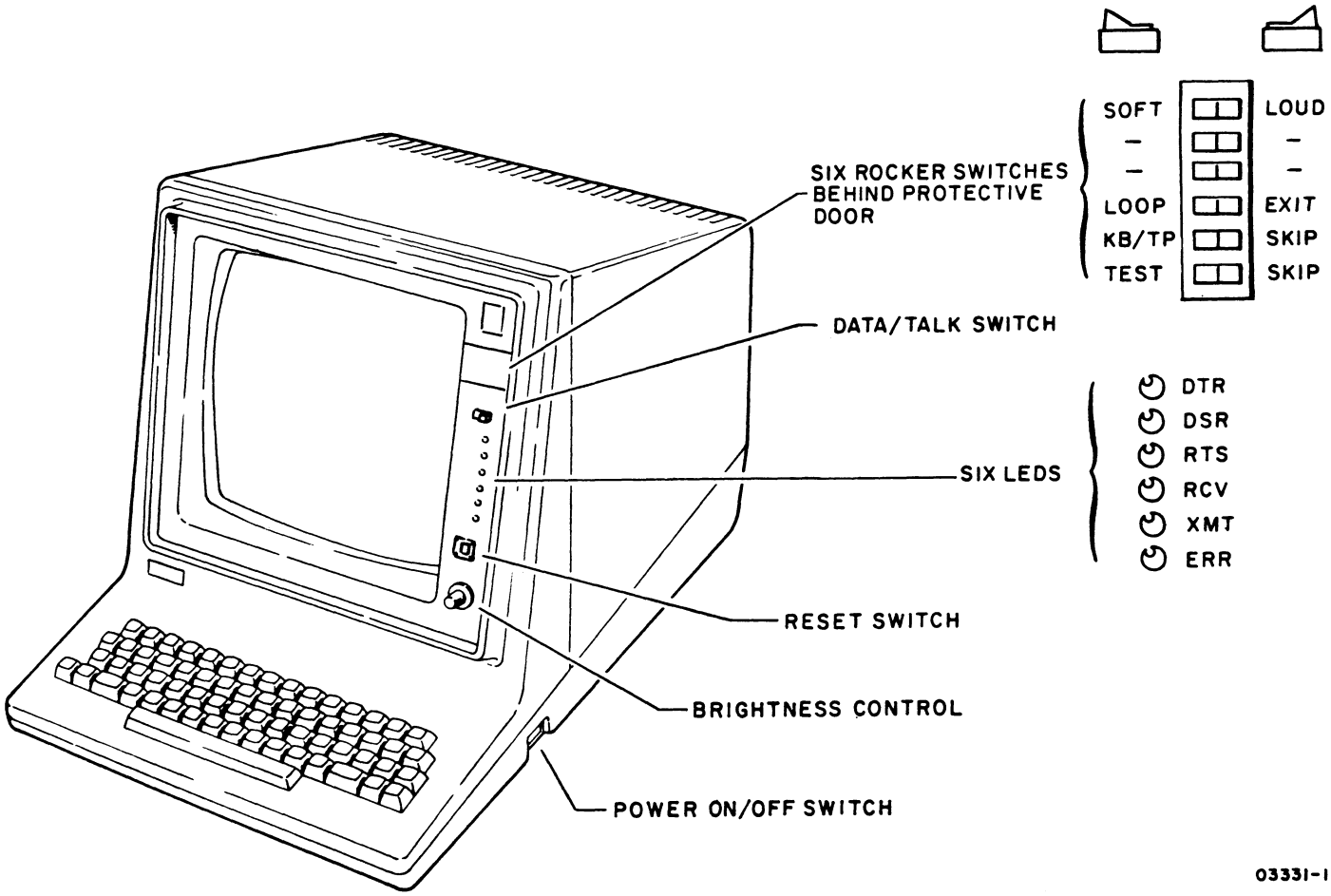


Figure 2-1. External Controls and Indicators

Brightness Control

This control adjusts video brightness.

CAUTION

If the brightness control is set too high, the display will be out of focus, and the life of the crt will be unnecessarily shortened.

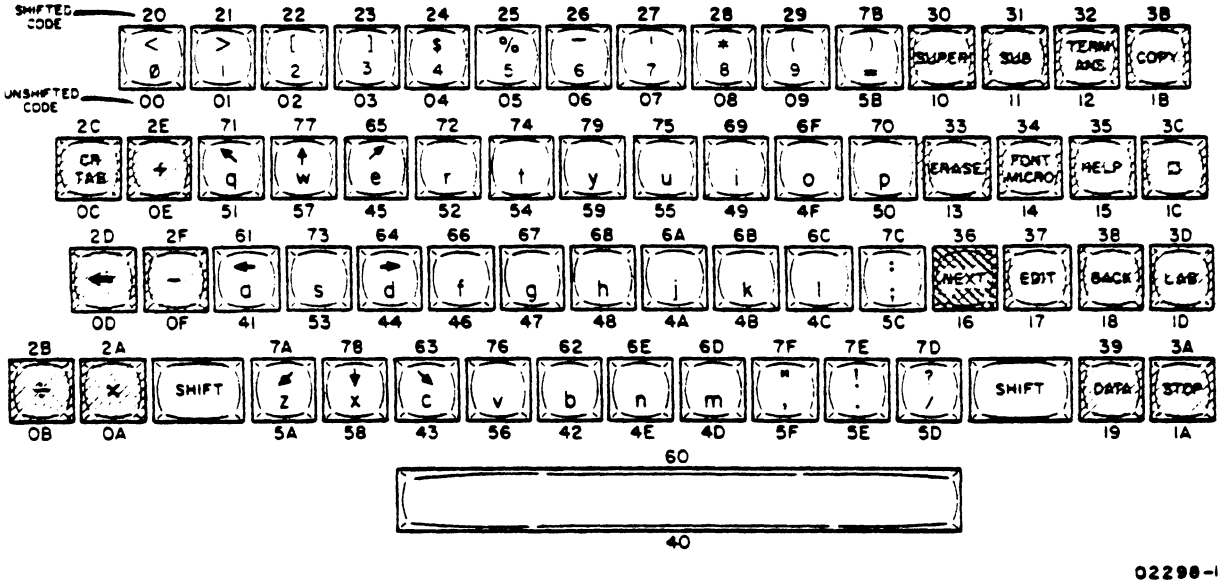


Figure 2-2. Alphanumeric Keyboard

RESET Switch

Pressing the RESET switch momentarily initializes the terminal logic and causes a check sum test of each major controlware block. Controlware blocks found to be in error reload automatically. Pressing the RESET switch and holding it down for longer than 3 seconds initializes the terminal logic, initiates the terminal resident diagnostics (as selected by front panel switches), and causes a full autoload of the terminal's controlware from the PLATO system.

Terminal logic is initialized as follows:

1. ROM and test mode selected
2. Next instruction fetch from address 0000
3. Interrupts disabled
4. Interrupt mask reset
5. I/O interfaces reset; ready to start new cycle
6. External indicators illuminated
7. Keyboard data not ready
8. PLATO communication character request set (transmission aborted)
9. PLATO communication character ready; not changed from previous state

10. Serial port

    a. Selects 150 bps clock

    b. Resets character request and ready interrupts

    c. Aborts transmission and sets character request

    d. Resets character ready status

11. Touchpanel data not ready

DATA/TALK Switch

This slide switch routes the signals from the telephone network to either a telephone set plugged into the terminal (TALK position) or to the internal modem (DATA position). This switch is only operational if the internal modem is installed.

Parameter/Mode Switches

These six rocker switches are behind a protective door on the front of the terminal. Each is labeled according to its function. Several have not been assigned, and their settings do not affect terminal performance. The following paragraphs describe the remaining four switches: SOFT/LOUD, LOOP/EXIT, KB-TP/SKIP, and TEST/SKIP.

CAUTION

Do not use a "lead" pencil to set rocker switches. Graphite dust from the pencil can cause a switch malfunction.

NOTE

Pressing RESET switch for more than 3 seconds is necessary to initiate terminal resident diagnostics.

SOFT/LOUD

This switch permits the operator to select between two alarm volume levels.

LOOP/EXIT

In the LOOP position, the terminal keeps repeating the internal diagnostic tests. In the EXIT position, it runs one pass of the internal diagnostic tests and exits. This switch functions only if TEST/SKIP switch is set to TEST.

KB-TP/SKIP

In the KB-TP, position the operator may perform the keyboard/touchpanel test. In the SKIP position, this portion of the internal diagnostic test is bypassed.

TEST/SKIP

In the TEST position, the terminal runs the internal diagnostic. In the SKIP, position it bypasses all tests and procedes with the autoload of the terminal controlware. This switch should be used in conjunction with the LOOP/EXIT switch.

EXTERNAL INDICATORS

These indicators consist of six red light-emitting diodes (LEDs). The LEDs are set slightly off-center within their sockets so as not to interfere with the operator's line of sight during normal operation.

The LED indicators serve two purposes: 1) to indicate the status of the terminal when running the resident diagnostic program and, if an error is detected, the area where the program failed (see section 6 for a description of these error codes); and 2) during normal terminal operation to monitor the signals described by the labels explained in the following paragraphs. All the LED indicators may be forced to the ON state by pressing the RESET switch and holding it depressed.

DTR

The Data Terminal Ready indicator is normally lit when the terminal is on.

DSR

The data set ready (DSR) indicator follows the state of the DSR signal as provided at the terminal's PLATO interface connector or as provided by the internal modem. This indicator will be lit when using the internal modem or when connected to a functioning external modem. It will always be lit when using the interface identified in table 3-1.

RTS

The Request to Send indicator is always lit when not in test mode.

RCV

The Received Data indicator monitors the Received Data line after being ANDed with the Carrier Detect and Data Set Ready (when the RS-232 interface is used) or the long line receiver (when the long line interface is used).

The indicator is lit when the input signal is in the space (logical 0) condition, and off in the mark (logical 1) condition.

XMT

The Transmitted Data indicator monitors the output of the transmit shift register before the signal gets to the RS-232-C or long line drivers. It is lit in the space (logical 0) condition and off in the mark (logical 1) condition.

ERR

The Error indicator indicates to the user that some kind of error condition has been detected by the controller. See section 6 in this manual for error codes and their definitions.

EXTERNAL CONNECTORS

Figure 2-3 shows the external connectors. Which are:

- PLATO Communication
- Parallel Channel
- Serial Channel
- Telephone
- Composite Video

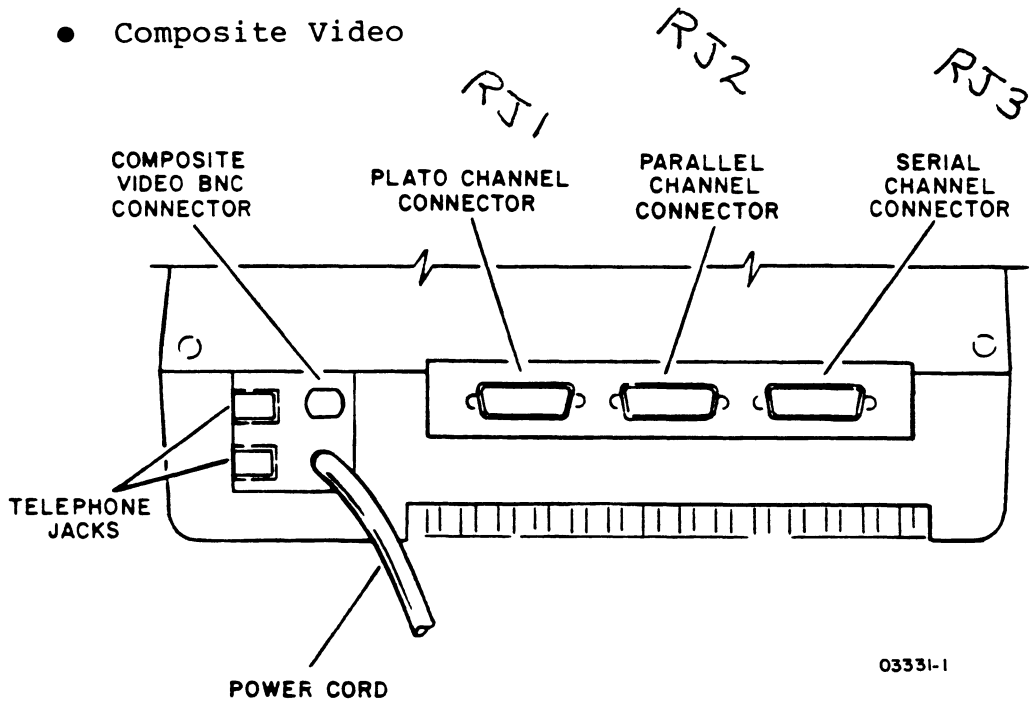


Figure 2-3. External Connectors

PLATO Communication Connector

This connector is on the lower rear panel of the terminal.

The pin assignments for the connector are listed in table 2-1. The RS-232-C interface is restricted to a shielded cable not to exceed 50 ft (15 m) in length. The long line interface is restricted to a twisted pair cable for each set of receive and transmit signals, not to exceed 10,000 ft (3048 m) in length.

TABLE 2-1. PLATO COMMUNICATION CONNECTOR PIN ASSIGNMENTS

PIN NUMBER	DESCRIPTION	NOTES
RJ1-1	Protective Ground	Green wire (Ground)
RJ1-2	Forward Channel Transmit	1 and 2
RJ1-3	Forward Channel Receive	2
RJ1-4	Forward Channel RTS	Always on
RJ1-5	Not Used	Open
RJ1-6	DSR	Must be on to RCV
RJ1-7	Logic Ground	Open
RJ1-8	Forward Carrier Detect	2; must be on to RCV
RJ1-9	-	3
RJ1-10	-	3
RJ1-11	-	3
RJ1-12	Not Used	Open
RJ1-13	Not Used	Open
RJ1-14	Reverse Channel XMT	1
RJ1-15	XMT Clock	4
RJ1-16	Not Used	Open
RJ1-17	Not Used	Open
RJ1-18	-	3
RJ1-19	Reverse Channel RTS	Always on
RJ1-20	DTR	Programmable
RJ1-21	Long Line Transmit	2
RJ1-22	Long Line Transmit Return	2
RJ1-23	Long Line Receive	2
RJ1-24	Long Line Receive Return	2
RJ1-25	Not Used	2

Notes:

1. Forward/reverse channel switch selectable.

2. RS-232-C/long line interfaces switch selectable.

3. These four lines go directly to module connector.

4. Internal/external clock switch selectable.

PARALLEL CHANNEL CONNECTOR

This interface provides a means for the terminal to communicate and exchange information with 16 addressable, external devices. Data is exchanged in bit-parallel/byte-serial mode with the terminal processor controlling the interface. Table 2-2 shows the pin assignments of this interface.

TABLE 2-2. PARALLEL CHANNEL CONNECTOR PIN ASSIGNMENTS

PIN NUMBER	SIGNAL	ACTIVE LEVEL	IN/OUT
RJ2-15	Data line 0	High	Both
RJ2-16	Data line 1	High	Both
RJ2-17	Data line 2	High	Both
RJ2-18	Data line 3	High	Both
RJ2-21	Data line 4	High	Both
RJ2-22	Data line 5	High	Both
RJ2-23	Data line 6	High	Both
RJ2-24	Data line 7	High	Both
RJ2-2	Address line 0	High	Out
RJ2-3	Address line 1	High	Out
RJ2-4	Address line 2	High	Out
RJ2-5	Address line 3	High	Out
RJ2-6	Address line 4	High	Out
RJ2-7	Address line 5	High	Out
RJ2-8	External write	Low	Out
RJ2-9	External output	Low	Out
RJ2-10	External read	Low	Out
RJ2-12	Interrupt	Low	In
RJ2-11	External ready	High	In

Note: Pins RJ2-1, -14, -19, -20, and -25 are grounded. Pin RJ2-13 is open.

A 25-conductor shielded cable not exceeding 5 ft (1.5 m) in total length is recommended. The shield must be properly terminated to safety ground (the connector metal case).

Serial Channel Connector

The serial channel interface provides the terminal processor with an asynchronous full duplex, bit-serial/byte-serial interface.

A shielded cable not to exceed 50 ft (15 m) in length should be used. Table 2-3 shows the pin assignments.

TABLE 2-3. SERIAL CHANNEL CONNECTOR PIN ASSIGNMENTS

PIN NUMBER	SIGNAL
RJ3-1	Safety Ground
RJ3-2	Send Data
RJ3-3	Received Data
RJ3-4	Request to Send
RJ3-5	Clear to Send
RJ3-6	Data Set Ready
RJ3-7	Signal Ground
RJ3-8	Carrier Detect
RJ3-20	Data Terminal Ready

Note: All unlisted (unused) pins of connector RJ3 are open.

Composite Video Connector

This BNC connector supplies a composite video signal of the display picture that meets the RS-170 standard.

A 75-ohm coaxial cable is recommended.

Flood Screen Switch

This is a three-position switch that forces the video output to the active (white) state, thus illuminating the entire screen. The purpose of this switch is to enable maintenance personnel to separate logic from display problems. The switch is normally in the OFF position and is activated while pressed to either side. Operation of this switch does not alter the contents of memory or stop the activity of the microprocessor.

Configuration/Mode Selection Switches

These switches are on the controller board and are labeled S2-1 through S2-10. Switch polarity is shown in figure 2-5. The following paragraphs describe their function.

CAUTION

Do not use a "lead" pencil to set rocker switches. Graphite dust from the pencil can cause a switch malfunction.

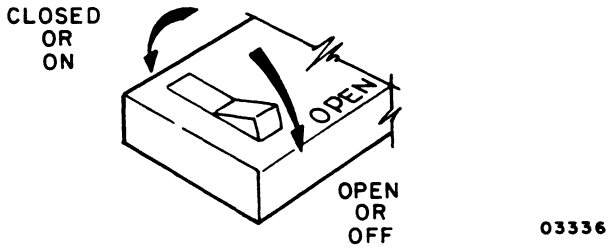


Figure 2-5. Configuration/Mode Selection Switch Polarity

S2-10 - Program Memory

This switch should be set to the ON (closed) position for 16K program memory; or to the OFF (open) position for 32K program memory.

S2-9 - Touchpanel

This switch should be set to the ON (closed) position if the touchpanel is not present; or to the OFF (open) position if the touchpanel is present.

S2-8 - Serial Channel Stop Bits Select

This switch selects the number of Stop bits to be transmitted after the Parity bit (or following the last data bit if parity is inhibited) on the serial channel interface. This switch on (closed) selects 1 Stop bit. This switch Off (open) selects 2 Stop bits when a 6-, 7-, or 8-bit word length is selected or 1.5 Stop bits when a 5-bit word is selected. The switch itself provides an input-high or input-low to the serial channel interface and a load serial control function must be executed in order for the serial channel to accept this new mode.

S2-7 - Forward/Reverse Channel

This switch selects the RS-232-C channel through which the terminal will transmit data to the central computer. In the OFF (open) position, the forward or primary channel is selected; in the ON (closed), position the reverse, low-speed channel is selected.

NOTE

To select either the forward or reverse channel, the S2-2 switch must be in the OFF (RS-232-C enabled) position.

Table 2-4 shows the outputs of the RS-232-C interface as controlled by this switch.

S2-6 - Serial Channel Parity Inhibit

This switch in the ON (closed) position, enables the insertion of the parity bit on transmissions, and parity checking on receptions of the serial channel interface. In the OFF (open) position, it disables the insertion and checking of parity bits.

TABLE 2-4. RS-232-C INTERFACE FORWARD/REVERSE CHANNEL SELECTION

PIN	SIGNAL	FORWARD SELECTED	REVERSE SELECTED
RJ1-2	Forward XMT	Dynamic	Mark
RJ1-14	Reverse XMT	Mark	Dynamic
RJ1-4	Forward RTS	ON	ON
RJ1-19	Reverse RTS	ON	ON
RJ1-20	DTR*	ON	ON

*Programmable, normally ON.

Once the parity generation/checking capability is enabled, the processor can control whether this parity is even or odd. See section 4, subsection Programming, for a further explanation of the function of this switch.

S2-3, S2-4, and S2-5 - Baud Rate Selection

These three switches control the PLATO transmitter baud rate. The settings for these switches are described in table 2-5.

TABLE 2-5. PLATO CHANNEL BAUD RATE SWITCH SELECTIONS

S2-3	S2-4	S2-5	FREQUENCY
ON	X*	ON	75 bps
ON	X*	OFF	120 bps
OFF	ON	X*	1200 bps
OFF	OFF	X*	External clock**

* X means that the position of that switch is irrelevant.

** The external clock is brought in through RJ1-15 (RS-232-C transmitter signal element timing).

S2-2 - RS-232-C/Long Line Selection

This switch selects whether the RS-232-C or long line drivers or receivers will be enabled to transmit and receive data to and from the central computer.

In the ON (closed), position, the RS-232-C option is enabled; in the OFF (open) position the long line option is enabled.

S2-1-Clear to Send

In the ON (closed) position, this switch forces a constant Clear to Send signal, thus enabling transmission without the external CTS (no modem). In the OFF (open) position, an external signal active is required.

Video Controls Adjustments

The video controls are on the video monitor board. Access to these controls, as well as function, is described in section 6.

Power Supply Controls

These potentiometers are on the power supply board. Access to these controls, as well as their function, is described in section 6.

INTERNAL INDICATORS

The the video LED and power supply LEDs, are discussed in the following paragraphs.

Video LED

This red light-emitting diode (LED) indicates power is present on the video board; it is discussed in section 6.

Power Supply LEDs

There are five red LED indicators on the power supply board. Access to them, as well as their purpose, is described in section 6.

This section describes the crating, uncrating, installation, checkout procedures, memory expansion installation, and optional modem installation for the terminal as well as instructions for connecting the terminal to the PLATO system.

CRATING

Figure 3-1 details the crating procedures to be followed when preparing the terminal for shipment. Use only approved materials to protect against shipping damage. Ship only by van or air. Do not ship via truck or ocean vessel. Approximate shipping weight of the packaged terminal is 45 lb (21 kg) for the domestic unit, and 53 lb (24 kg) for the international unit.

To protect against shipping damage, always prepare the terminal for shipment using only approved procedures and materials. To obtain proper procedures and materials, contact the nearest CDC representative or:

Control Data Corporation
Corporate Traffic
8100 34th Avenue South
Minneapolis, Minnesota 55440

UNCRATING

The following instructions describe the uncrating procedures for the terminal. Refer to figure 3-1 to remove the terminal from the exterior container.

1) Open top of exterior container.

2) Lift terminal with end frames attached from exterior container. Remove end frames.

3) Inspect terminal for shipping damage.

NOTE: PERFORM THE FOLLOWING STEPS IN ORDER.

1. INTERLOCK FOAM BASE LEGS WITH END FRAMES.
2. PLACE END FRAMES WITH BASE LEGS ON DISPLAY STATION.
3. PLACE DISPLAY STATION WITH END FRAME CUSHIONING INTO EXTERIOR CONTAINER.
4. LOCK "L" BLOCKS IN POSITION.
5. SECURE POWER CABLE IN SLITS OF END FRAMES. (DONT LET PLUG DANGLE).
6. CLOSE AND SEAL EXTERIOR CONTAINER WITH 3-in REINFORCED BOX SEALING TAPE.

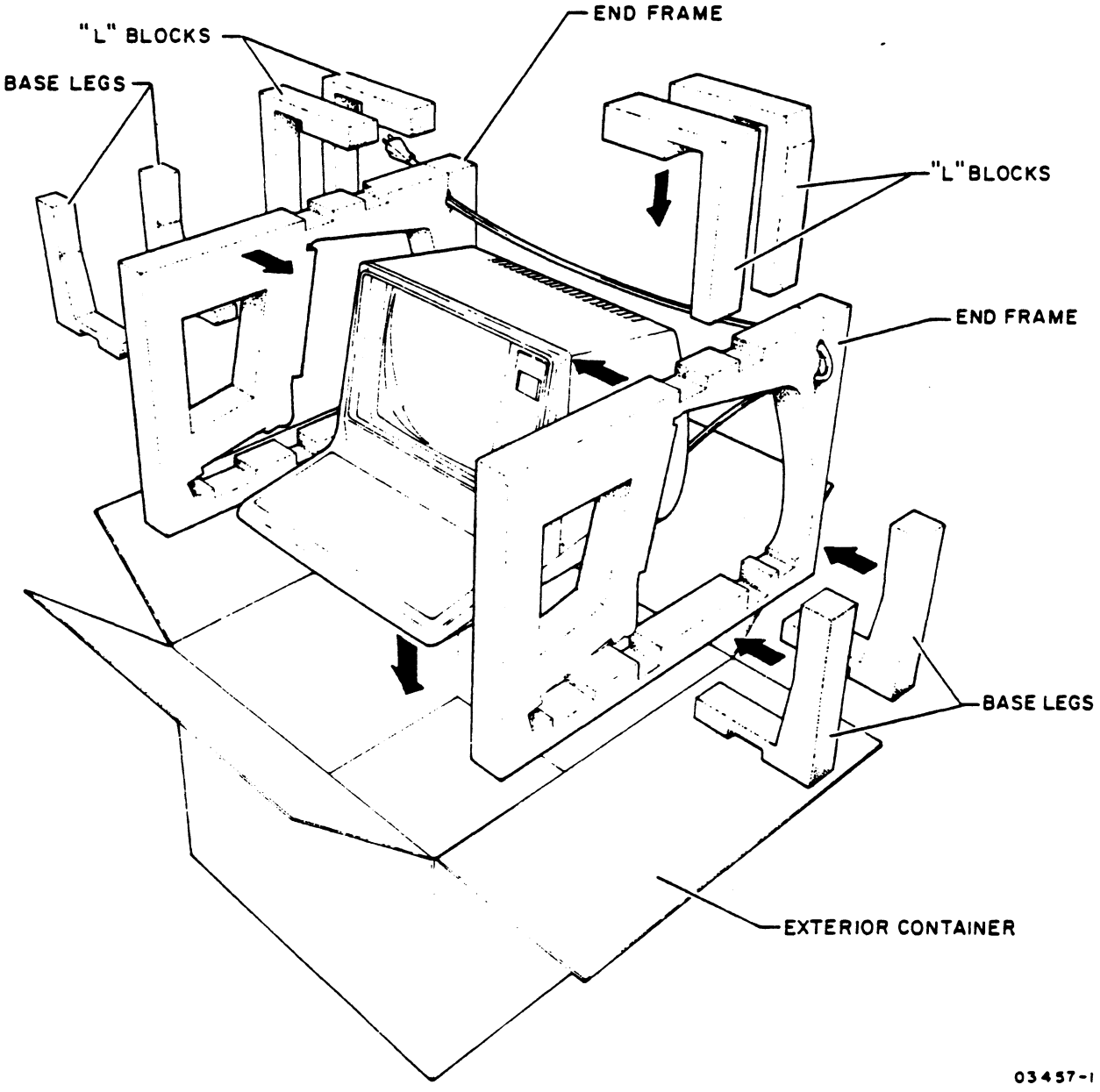


Figure 3-1. Terminal Packaging

INSTALLATION

The following paragraphs define the installation instructions for the terminal. All procedures referenced in the instructions are contained in section 6 of this manual. An index is provided at the end of section 6 that lists the page numbers for the various procedures.

1) Set terminal on flat surface in area in which it is to be used. The terminal uses natural convection for its ventilation; allow a 4-in (101.6 mm) clearance around the terminal.

2) Set terminal power ON/OFF switch to OFF (procedure 1).

3) If internal modem is being employed, unplug the telephone set from the wall jack and plug it into the terminal jack labeled PHONE. Using the telephone cable supplied with the terminal, connect the terminal to the telephone line by plugging one end of this cable into the terminal jack labeled LINE and the other end into the wall jack (figure 3-2).

NOTE

If PLATO interface (RS-232 or long long driver) is to be used (no internal modem), see steps 4 through 6 for assembly instructions.

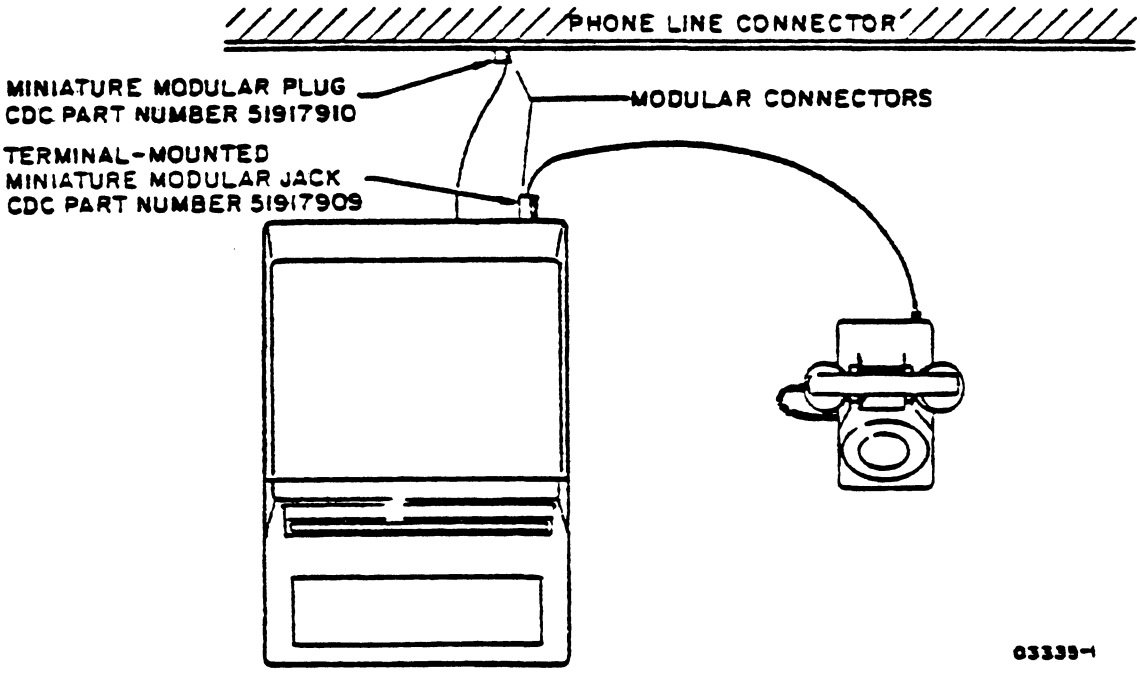


Figure 3-2. Terminal/Telephone Connection

4) If PLATO interface (RS-232 or long line driver) is being used, assemble interface cable kit as required for communication interface used by terminal.

NOTE

To use this interface when an internal modem is installed, connector AJ5 on the controller board must be disconnected.

a) Connect applicable color-coded wires to connector according to table 3-1 and figure 3-3.

- Do not connect more than one interface selection to connector.

- Use Cannon CIET-20-HDB pin extractor for pin removal (CDC Part Number 95363200).

b) Tape unused wires on both sides of cable back against cable jacket. Do not cut off as interface configuration of terminal may change in future.

c) Place connector in mounting slot of connector hood and fasten cable tie strap as shown in figure 3-3.

d) Close connector hood and fasten it together with two screws provided.

5) Install interface cable to PLATO I/F connector at rear of controller unit. Screw on locking devices to provide mechanical retention and good safety ground.

6) Connect respective color-coded wires of interface cable to site data access equipment terminals.

7) Remove terminal hood (procedure 4) and set configuration/mode switches on controller board to applicable settings: (see figure 6-16 for switch location).

- S2-1 - In the On (closed) position enables a constant Clear to Send signal and enables external clear to send. In the Off (open) position disables the constant Clear to Send.

- S2-2 - In Off (open) position enables long line interface. In On (closed) position enables RS-232-C interface.

- S2-3, S2-4, S2-5 - These switches must be set to the correct transmitter baud rate. Check with PLATO Site Director to determine transmission rate (normally set at 120 baud). Refer to table 3-2 for correct switch settings.

- S2-6 - In the On (closed) position enables the inserting of a parity bit on transmitted data and parity checking on received data on the serial channel interface. In the Off (open) position disables the inserting and checking of parity bits.

- S2-7 - In the Off (open) position selects the primary (forward) channel. In the On (closed) position selects the low-speed (reverse) channel. To select either the primary or low-speed channel, switch S2-2 must be in the On position.

- S2-8 - In the On (closed) position selects 1 stop bit. In the Off (open) position selects 2 stop bits for 6-, 7-, or 8-bit words or 1.5 stop bits for a 5-bit word.

- S2-9 - In the On (closed) position selects touchpanel not present. In the Off (open) position selects touchpanel present.

- S2-10 - In the On (closed) position selects 16K memory. In the Off (open) position selects 32K memory.

8) Verify that power ON/OFF switch is in OFF position. Plug ac power cord into site outlet. Replace hood (procedure 4) and proceed with checkout procecure.

TABLE 3-1. PLATO INTERFACE SELECTIONS

PIN NO.	SIGNAL	PLATO Long Line	PLATO RS-232-C*
1	Protective Ground	Bare	Bare
2	Forward Channel Transmit	-	-
3	Receive	-	Red
4	Forward Channel Request to Send	-	-
5	Not used	-	-
6	Data Set Ready	Yellow Jumper***	Yellow Jumper***
7	Logic Ground	-	Black
8	Forward Channel Carrier Detect	Orange Jumper***	Orange Jumper***
9	Reserved	-	-
10	Reserved	-	-
11	Reserved	-	-
12	Not used	-	-
13	Not used	-	-
14	Receive Channel Transmit	-	White
15	Transmit Clock	-	Green**
16	Not used	-	-
17	Not used	-	-
18	Reserved	-	-
19	Receive Channel Request to Send	Orange Jumper***	Orange Jumper***
20	Data Terminal Ready	Yellow Jumper***	Yellow Jumper***
21	Long Line Transmit	White	-
22	Long Line Transmit Return	Green	-
23	Long Line Receive	Red	-
24	Long Line Receive Return	Black	-
25	Not used	-	-

*If internal modem is installed, disconnect internal modem flat ribbon cable from controller board (AJ5 connector).

**This pin is assigned for an externally supplied transmit clock signal and is only used in special installations.

***Pins 6 and 20 and pins 8 and 19 are jumpered together.

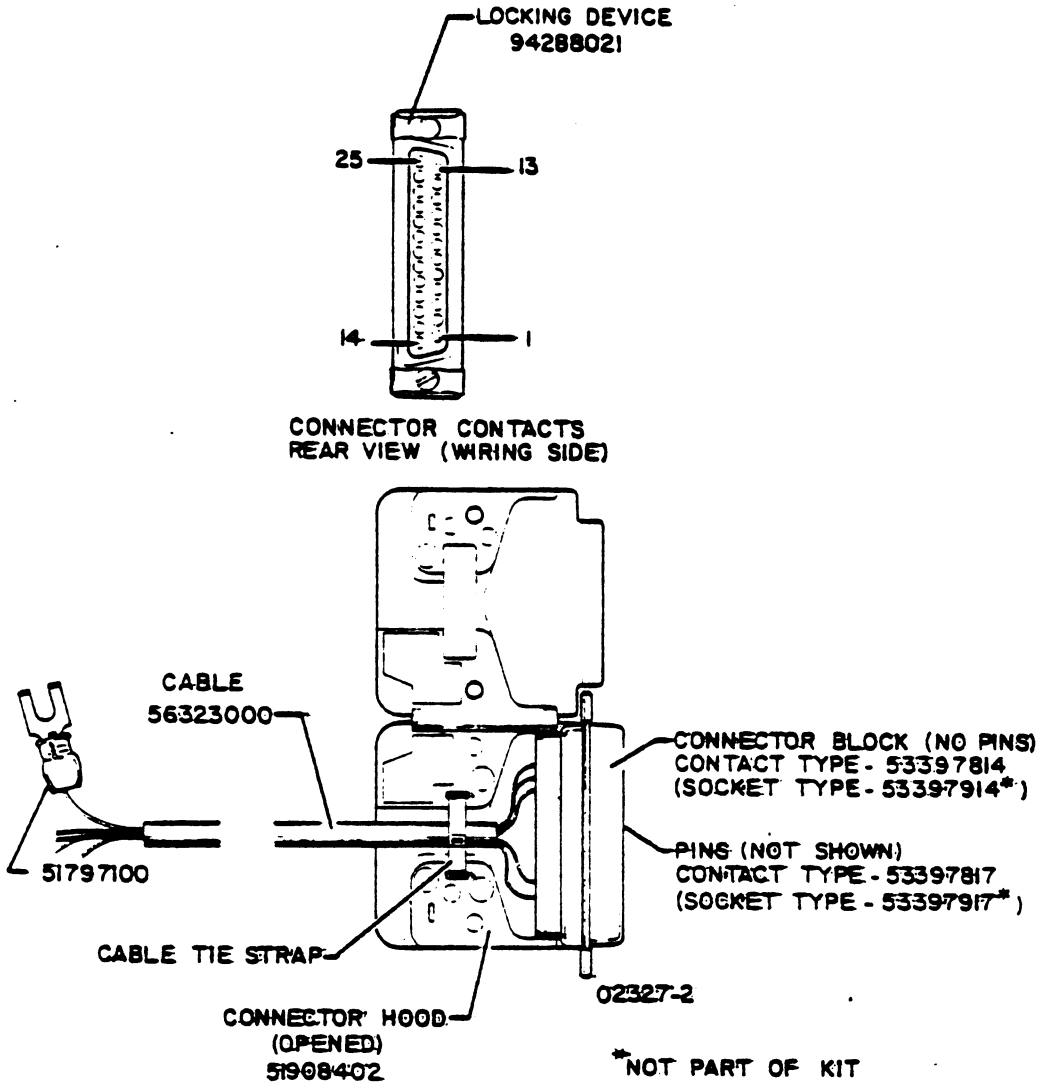


Figure 3-3. Interface Cable Kit

TABLE 3-2. BAUD RATE SWITCH SELECTIONS

S2-5	S2-4	S2-3	FREQUENCY
ON	X*	ON	75 bps
OFF	X*	ON	120 bps
X*	ON	OFF	1200 bps
X*	OFF	OFF	External clock**

* The switch position is irrelevant.
** The external clock is brought in through RJ1-15 (RS-232-C transmit clock).
On = closed; Off = open.

CHECKOUT

Perform the following steps for operational checkout of the terminal. Procedures and sections referred to in the checkout steps are defined in section 6 of this manual unless otherwise stated. Also, refer to section 6 if any difficulties are encountered.

1) Turn terminal power on per procedure 1.

2) Run resident diagnostics as per procedure 2.

3) Check for correct alignment and acceptable display quality (refer to procedure 23). When checks are complete, return switches on operators panel to bypass internal diagnostic checks.

4) Perform a basic systems check of terminal by executing quicklook portion of PLATO system diagnostic (DIAG) per procedure 3.

MEMORY EXPANSION INSTALLATION

The memory expansion consists of eight MOS type memory IC (integrated circuit) chips that plug into the terminal video board. The video board has all the sockets to accept the eight IC's and also the support logic for the operation of the memory expansion. Observe the following caution when installing the memory expansion IC's.

CAUTION

Follow precautionary rules for handling MOS type circuits as described in Section 6.

To install memory expansion reference figure 3-4 and do the following:

1. Turn terminal power off per procedure 1.

2. Remove video board from terminal per procedure 7.

3. Observe correct pin alignment and insert the eight memory IC's into C10 through C17 locations on video board. Dot or indentation on the IC's must be aligned with notched side of IC sockets.

4. Reinstall video board in terminal per procedure 7.

5. Set configurator/mode switch S2-10 on controller board to the OFF (open) position to indicate the presence of the memory expansion.

6. Apply power and test terminal per procedure 2.

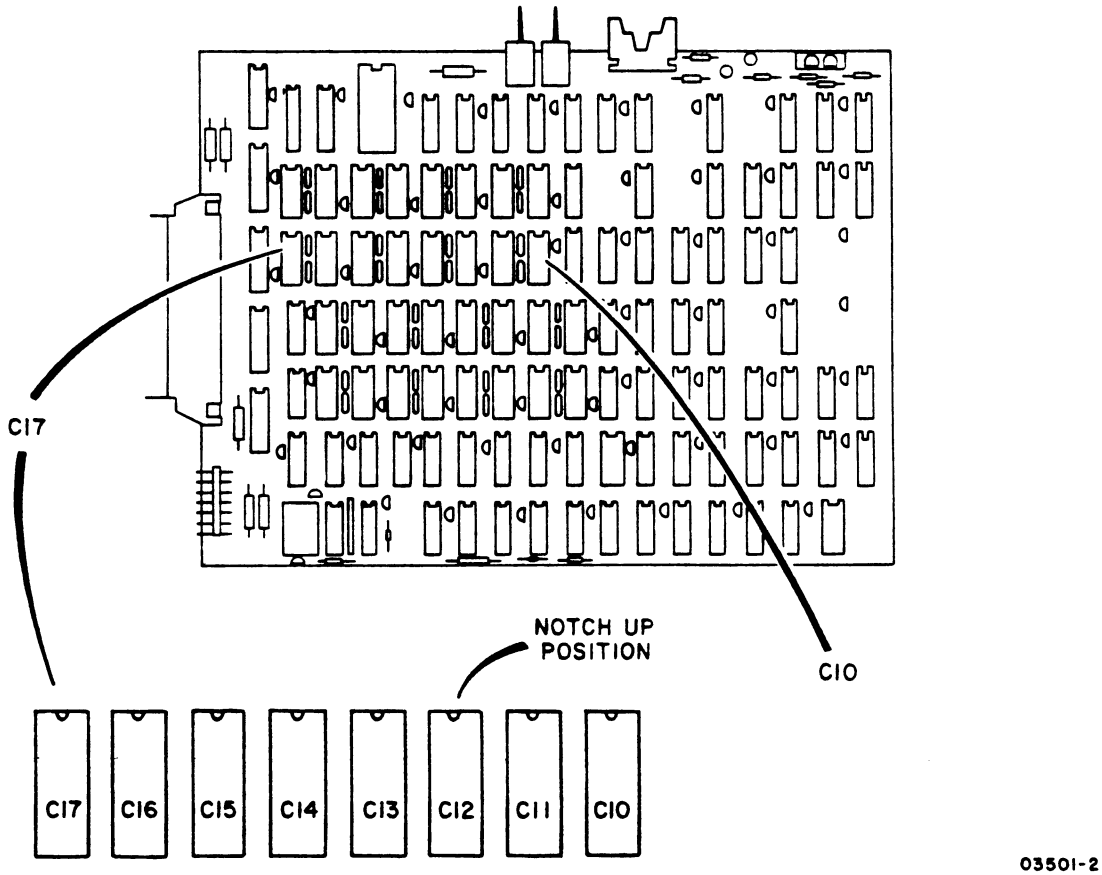


Figure 3-4. Video Board IC Locations for Memory Expansion

INSTALLATION INSTRUCTIONS FOR OPTIONAL MODEM (XA247-A)

To install the optional modem do the following:

1) Power off terminal per procedure 1.

2) Unplug ac power cord from site outlet.

3) Remove terminal hood per procedure 4.

4) Remove ac entry panel per procedure 11 and discard the ac entry cover plate. Install two telephone jack connectors and reinstall ac entry panel.

5) Remove three standoffs (if present) from monitor assembly and discard. See figure 3-6 for location of existing standoffs.

6) Remove operators panel cable clamp and discard.

7) Fasten a ground wire to monitor chassis mounting screw shown in figure 3-5. the other end will be connected in step 12.

8) Position shield as shown in figures 3-5 and 3-6 and insert three new standoffs (these are provided) through the shield and attach it to the monitor chassis.

9) Run the operators panel cable along the outside of the shield so it will fit between it and the modem printed circuit board after the board is installed.

10) Insert the remaining new standoff through the upper right hand corner of the modem printed circuit board (this is for proper spacing between the shield and modem board).

11) To install modem printed circuit board, do the following:

    a) Position the board in the location shown in figure 3-6.

    b) Make sure the operator panel cable is between the shield and board as shown in figure 3-6.

    c) Align the board so its three mounting holes line up with the three standoffs on the shield.

    d) Press the board into place by pushing it over the three standoffs until it is in the mounting position. The 4th standoff (this was installed in step 10) protrudes through a clearance hole in the shield.

    e) Attach a tie wrap through the opening in the end of the three standoffs (leave tie wrap off the fourth standoff) and lock each tie wrap. Installing the tie wraps ensures a locking action to prevent the board from becoming detached from the shield and falling inside the monitor.

    f) Connect modem printed circuit board cable to location AJ5 of controller board.

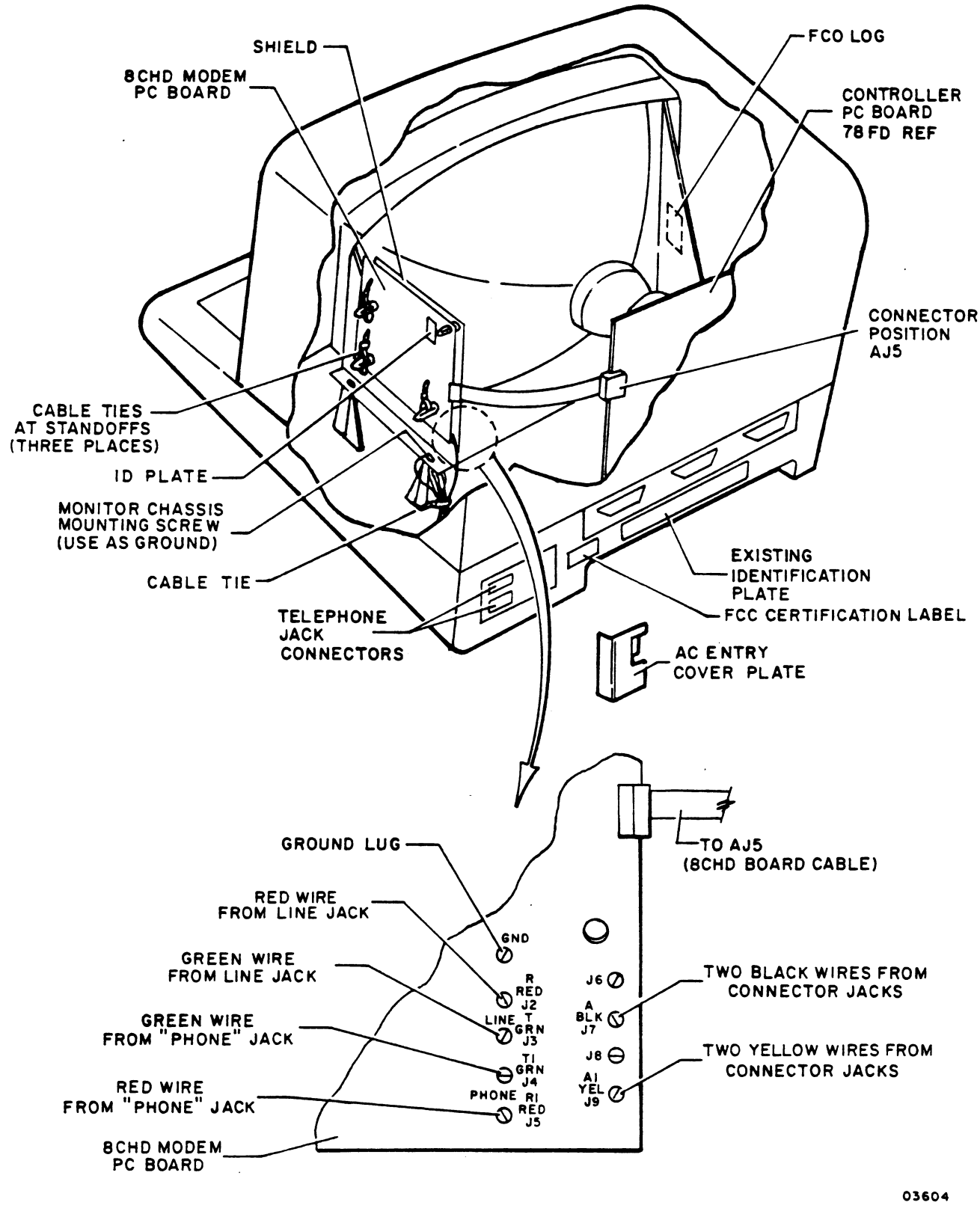


Figure 3-5. Optional Modem Installation

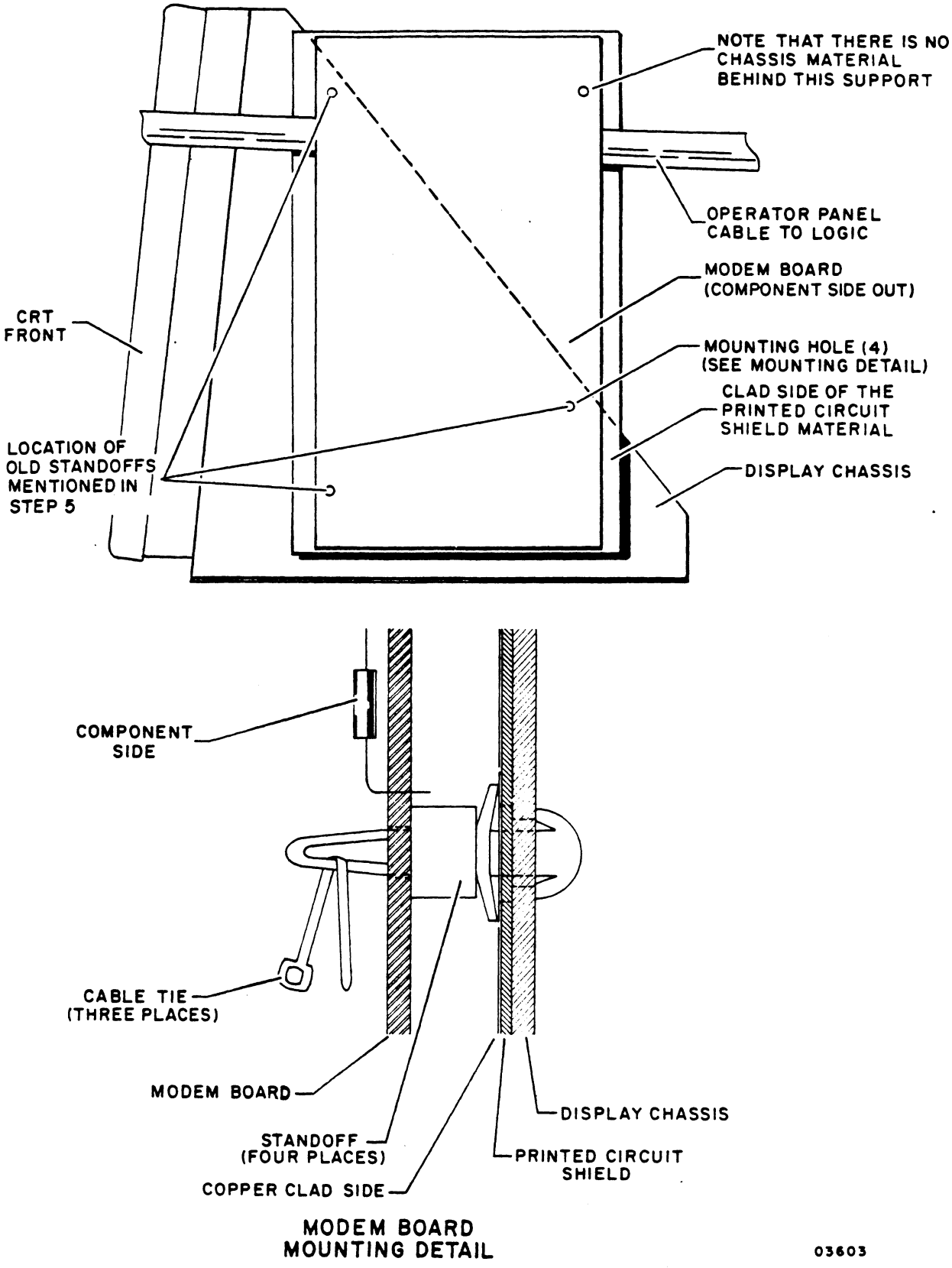


Figure 3-6. Modem Shield and Printed Circuit Board Installation

12) Fasten other end of ground wire installed in step 7 to ground (GND) lug on modem printed circuit board (figure 3-5).

13) Attach red wire from connector jack marked PHONE to terminal J5 and green wire to terminal J4 of modem printed circuit board (figure 3-5).

14) Fasten the red wire from connector jack marked LINE to terminal J2 and the green wire to terminal J3 of modem printed circuit board (figure 3-5).

15) Attach the two black wires from both connector jacks to terminal J7 of modem printed circuit board (figure 3-5).

16) Fasten the two yellow wires from both connector jacks to terminal J9 of modem printed circuit board (figure 3-5).

17) Install the remaining tie wrap around the wires going to the board mentioned in steps 13 through 16.

18) Install a identification plate on the modem printed circuit board in a approximate location shown in figure 3-5.

19) Update equipment identification log showing modem is installed.

20) Install FCC (Federal Communications Commision) certification tag as shown in figure 3-5.

21) Install FCO log per figure 3-5.

22) Replace hood per procedure 4.

CONNECTING TERMINAL TO PLATO SYSTEM

The following defines the instructions for connecting the terminal to the PLATO system. The procedure contains instructions for the direct connected terminal (RS-232 or long line driver interface) and the dial-in connected terminal (internal modem). To make the connections between the terminal and the PLATO system do the following:

1) Set terminal power ON/OFF switch to ON (procedure 1).

2) Set rocker switches for normal operating mode.

a) LOOP/EXIT switch to EXIT position.

b) KB/TP/SKIP switch to SKIP position.

c) TEST/SKIP switch to SKIP position.

3) Direct connected terminal (RS-232 or long line driver interfaces).

a. The terminal must load its controlware from the PLATO system. This process takes about 1-1/2 minutes.

NOP

No operation. Indicates that the communication link between the terminal and the PLATO system is down. Refer to section 6.

NO REPLY

Indicates that the terminal has received no response from the PLATO system. The terminal continues to solicit a response from the PLATO system approximately every 4 seconds until a reply is received.

LOADING FAILURE

Indicates that the loading process was unsuccessful and the program has aborted. Refer to section 6.

LOADING XX

Indicates a successful loading process. XX signifies the block being loaded. This message is followed by the Begin Display.

b) Proceed with sign-on sequence.

4) Dial-in connected terminal (internal modem).

a) Set the DATA/TALK switch to TALK.

b) Dial telephone number that connects computer, and listen for the computer telephone to ring, followed by a period of no sound, and then a high-pitched answer tone which indicates connection to the computer.

c) Set DATA/TALK switch to DATA, and hang up telephone.

d) The terminal must be loaded with its controlware from the PLATO system. This process takes about 1-1/2 minutes.

During this loading process, the terminal displays one of the following messages:

NOP

No operation. Indicates that the communication link between the terminal and the PLATO system is down. Refer to section 6.

NO REPLY

Indicates that the terminal has received no response from the PLATO system. The terminal continues to solicit a response from the PLATO system approximately every 4 seconds until a reply is received.

LOADING FAILURE

Indicates that the loading process was unsuccessful and the program has aborted. Refer to section 6.

LOADING XX

Indicates a successful loading process. XX signifies the block being loaded. This message is followed by the Begin Display.

e) Proceed with sign-on sequence.

5) To disconnect the terminal from the PLATO system, sign off system, hang up telephone handset, and set the DATA/TALK switch to TALK.

6) Turn off terminal by setting power ON/OFF switch to OFF.

The maintenance philosophy for the terminal calls for troubleshooting and parts replacement down to the chip level in some cases. A block diagram of the terminal is presented in figure 4-1. This section describes the basic functional modules and chips that are replaceable in the terminal without a detailed analysis of their internal operation. The information is presented in the following order:

- Controller
- Communication Interface/Internal Modem
- Operators Panel
- Touchpanel
- Power Supply
- Video Monitor
- Keyboard

CONTROLLER

The controller portion of the terminal consists of two printed-circuit logic boards (PCBs): the controller board and the video board. The following paragraphs describe some of their features and capabilities.

CONTROLLER BOARD

This board provides the control function and processing capability required to support the input and output operations as well as to manage their interactions.

Examples of control functions are:

- Character generation
- Line generation
- Instruction decoding and execution

- Routing of messages for peripheral devices
- Interrupt recognition and process

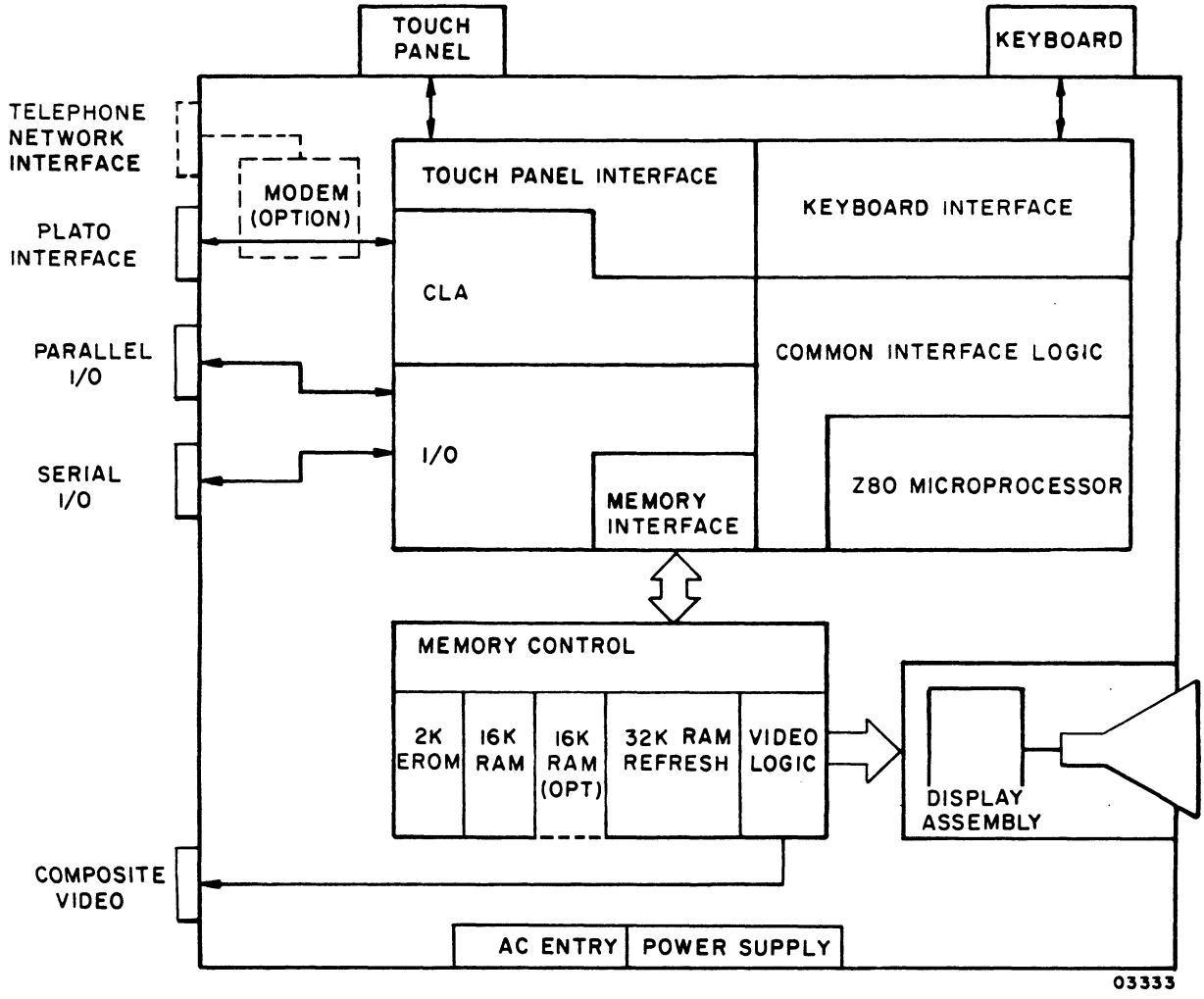


Figure 4-1. IST-II Terminal Block Diagram

The Z80A microprocessor, on the controller board, inputs data from or outputs data to the devices and interfaces listed in table 4-1. A block diagram of the controller board is illustrated in figure 4-2.

TABLE 4-1. DEVICE INPUTS AND OUTPUTS

DEVICE	MICROPROCESSOR INPUT/OUTPUT
Memory	Both
Keyboard	Input
PLATO communication interface	Both
Serial channel	Both
Maintenance LEDs	Output
Switches	Input
Identification code setting	Input
Touchpanel	Input
Parallel channel	Both
Interrupt mask	Output

The following paragraphs discuss the execution times, PLATO communications interface, serial channel interface, parallel channel interface, terminal identification, and programming.

Execution Times

The state time is fixed at 250 nanoseconds. The program memory addresses 0000_{16} through $7FFF_{16}$ are dedicated exclusively for program storage. The controller is the only user of this memory. The refresh memory addresses 8000_{16} through $FFFF_{16}$ contain the information to be displayed on the screen, and both the display logic (read) and the controller (read/write) have access to this memory, with the display having top priority. The fact that whatever information stored in the refresh memory is displayed on the screen does not preclude the possibility for storing and executing programs in it.

The following rules must be followed when calculating execution times:

- Add one state time (WAIT state) to each instruction (whether it is a 1-, 2-, 3-, or 4-byte instruction) if it is stored in the program memory.

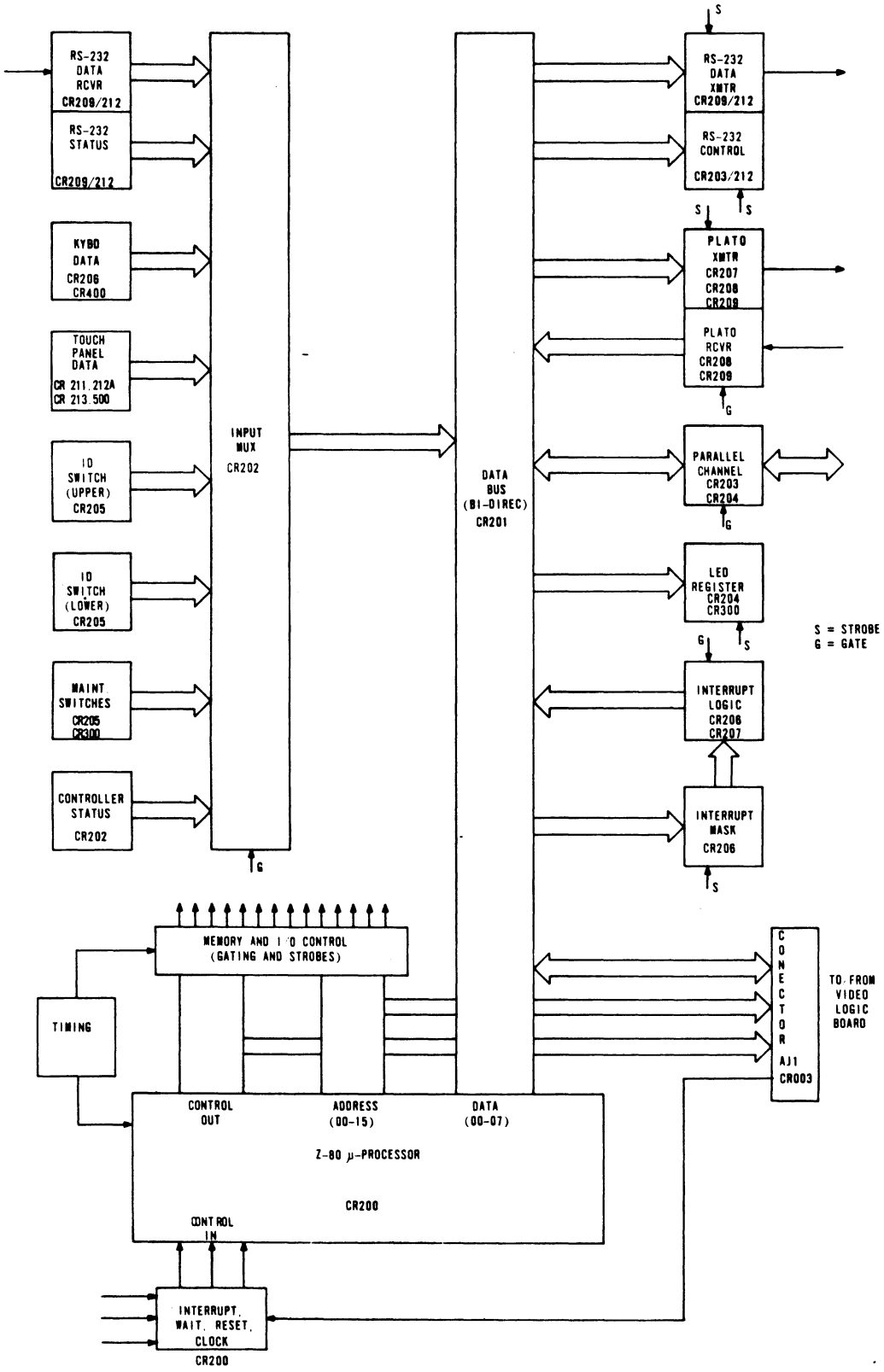


Figure 4-2. Controller Board Block Diagram

- Add three state times (WAIT states) to each memory reference to the refresh memory.

For example, the instruction LD (nn), A stores the contents of the A register in address nn. It is a 3-byte instruction with four memory references (read operations code, read lower 8 bits of address, read upper 8 bits of address, and write the contents of the A register into that address).

Here are four typical cases:

Case	Address (Hex Code)	Code	Description
1	1000	32 00 70	A(7000)
2	1000	32 00 80	A(8000)
3	9000	32 00 70	A(7000)
4	9000	32 00 80	A(8000)

Case 1 - All addresses in program memory

```
Execution time = 13 states   (basic)
                  1 wait     (program memory)
                 14 states = 3.5 microseconds
```

Case 2 - Program in program memory, write into refresh memory

```
Execution time = 13 states = (basic)
                  1 wait     (program memory)
                  3 wait     (write in refresh memory)
                 17 states = 4.25 microseconds
```

Case 3 - Program is refresh memory, write into program memory

```
Execution time = 13 states   (basic)
                  9 wait     (three refresh memory reads)
                 22 states = 5.5 microseconds
```

Case 4 - All addresses in refresh memory

```
Execution time = 13 states   (basic)
                 12 wait     (four refresh memory references)
                 25 states = 6.25 microseconds
```

PLATO Communications Interface

This interface enables the terminal logic to communicate with the PLATO system and discussion here centers on the signals, pinouts, parameter selection, and operation of the PLATO Receiver and PLATO Transmitter.

PLATO Receiver

Important aspects of the PLATO Receiver are word format, word polarity, word parity, data rate, and data assembly/ transfer.

Word Format - The asynchronous PLATO receiver receives 21 bits of serial data after detection of a Start bit (including the Start bit). After reception of the 21 bits it searches for another Start bit. If the bit following a 21-bit word is a logical 1, it is interpreted as a Start bit and 21 more bits are clocked in. If after 21 bits, the incoming data is a logical 0, the receiver stops in Search mode until the incoming data line switches from 0 to 1, at which point the receiver resumes its activity. Figure 4-3 shows the receiver word format.

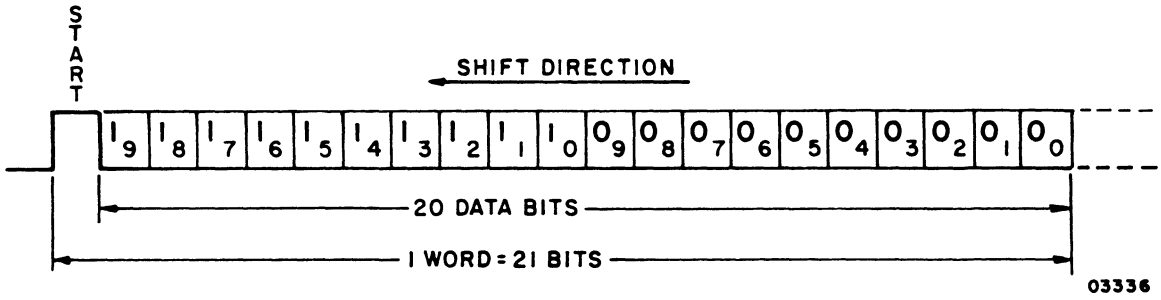


Figure 4-3. Receiver Word Format

Word Polarity - The Start bit must be a logical 1 to trigger receiver activity. A logical 1 is received when the RS-232-C receiver (RJ1-3) is in the space condition or the interface receiver (AJ5-7) is in the space or TTL high condition (both interfaces require that the long line interface not be enabled), or the long line receiver on and the long line interface enabled.

The data following the Start bit is assembled and passed on to the microprocessor as a logical 1 if it has the same polarity as the Start bit; otherwise, it is assembled and passed on as a logical 0.

Word Parity - The receive logic does not have parity check circuits. Received word parity checking is accomplished by the terminal controlware program.

Data Rate - The receiver nominal data rate is 1200 bps.

When measured at the receiver inputs, the combination of frequency differential between receiver and transmitter, plus network distortion should not make the data string:

- Have the rising and falling edges more than 40 percent away from the 1200 bps nominal positioning. This 40 percent applies to any edge of any bit within the 21-bit word. Timing is resynchronized upon detection of the next Start bit, so the error is noncumulative.
- Contain bit times whose levels are stretched or shortened by more than 40 percent of the nominal 833-microsecond bit duration (1167- to 500-microsecond duration).

Data Assembly/Transfer - Upon detection of the Start bit, the receiver logic starts clocking the incoming serial data into a 7-bit shift register. When the register is full, its contents are parallel-transferred to a holding register and the communication ready status/interrupt set. The shift register is available to receive the next 7 bits. The data in the holding register must be removed before the second byte of 7 bits is received to avoid losing data. The time available between the communication ready and the lost data condition is:

7 bits at 0.833 millisecond/bit = 5.83 milliseconds

The second assembled byte loads into the holding register and the process repeats for the last 7 bits of the 21-bit word.

Figure 4-4 shows the 21-bit incoming serial word and the way it passes on to the processor in 3 bytes.

Bit 7 of the 8-bit byte received by the processor sets when the first byte transfers and resets for bytes 2 and 3.

The Start bit, labeled S, is always a logical 1.

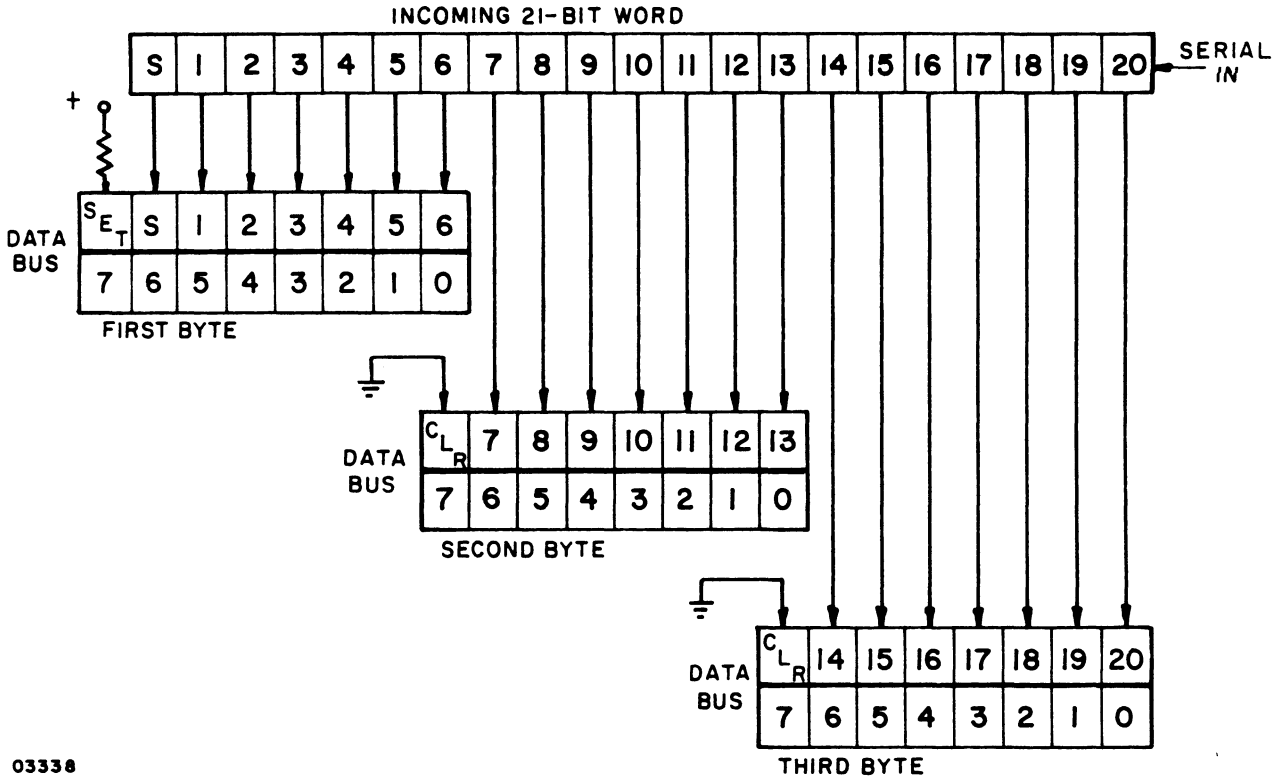


Figure 4-4. Receiver Data Transfer

PLATO Transmitter

The following paragraphs describe the PLATO Transmitter word format, word polarity, word parity, data rate, data transfer/disassembly, signals, and long line receiver, and driver.

Word Format - The PLATO transmitter transmits a Start bit plus 11 Data bits. A Stop bit adds at the end of the Data bits to generate a gap between characters. Figure 4-5 shows the transmitter word format.

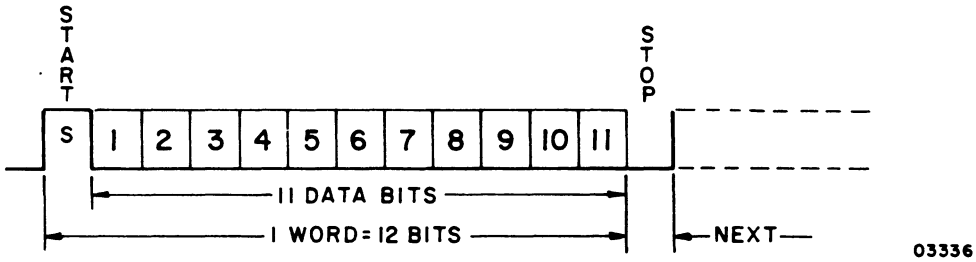


Figure 4-5. Transmitter Word Format

Word Polarity - The transmitter output is in the TTL high state during the idle (inactive) state. The Start bit is a logical 0. The data is inverted; that is, if bit 4 output from the processor was a logical 1, it goes out of the transmitter as a logical 0.

These TTL levels show at the connectors as follows:

TTL 0	RJ1-2, RJ1-14 (RS-232-C)	= Space
	AJ5-6 (TTL)	= TTL high
TTL 1	RJ1-2, RJ1-14 (RS-232-C)	= Mark
	AJ5-6 (TTL)	= TTL low

Word Parity - The transmitter logic does not generate parity.

Data Rate - The transmitter can transmit at 75, 120, and 1200 bps.

Data Transfer/Disassembly - When the transmit data has been correctly loaded, the two output bytes shift out as shown in figure 4-6.

Bits 0, 1, and 2 of the load low bits output are not used (they can have any value). Bits 3 through 7 hold Transmitter Data bits 11 through 07, respectively. Bits 0 through 5 of the load upper bits output contain bits 06 through 01 of the Transmitter data word. Bits 6 and 7 are ignored and the transmit logic inserts the Start bit.

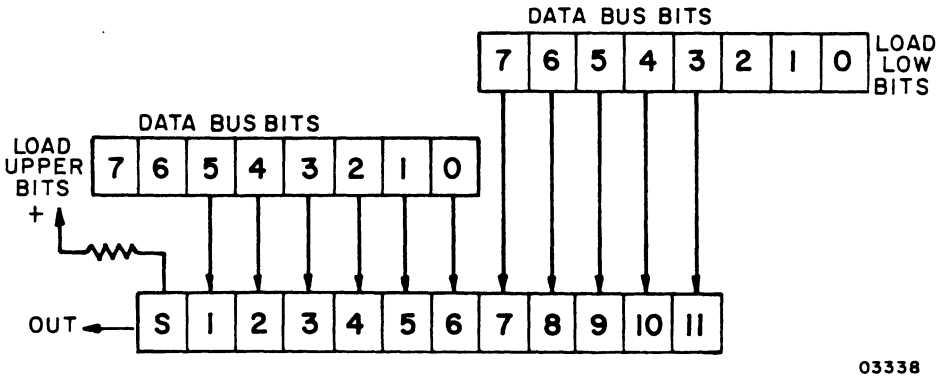


Figure 4-6. Transmit Data Transfer

Signals - The following paragraphs describe the Data Set Ready, Carrier Detect, Request to Send, Data Terminal Ready, and Transmit Clock.

- Data Set Ready - This signal in the true state is required to enable the receiver to accept data. This condition is met when the RS-232-C input (RJ1-6) is in the on state or when the board connector AJ5-8 is a RS-232-C On or a TTL high.

- Carrier Detect - This signal has the same use as Data Set Ready. The condition is met when the RS-232-C input (RJ1-8) is On or when the board connector AJ5-9 is a RS-232-C On or a TTL high.

- Request to Send - Both the forward channel RTS (RJ1-4) and reverse channel RTS (RJ1-19) are always in the RS-232-C on state as long as the terminal is powered up.

- Data Terminal Ready - This signal is programmable and comes up set upon power on, but its state can be controlled via software. This signal set means the RS-232-C output (RJ1-20) is in the space condition.

- Transmit Clock - This signal brings a timing clock from an external source (that is, modem) to control the transmitter shift rate. The selection of the internal clocks or external clock is performed via switches.

Long Line Receiver - The receiver is basically a light-emitting diode/phototransistor circuit. Figure 4-7 shows the typical long line receiver circuit.

Request to Send (RTS), CA - This signal from the terminal to a data set (modem) indicates that data to be transmitted is available and the modem should condition the lines.

It is activated automatically. The interface, after receiving data from the processor, holds the data and activates the RTS line. It keeps it activated until the last bit of data has been clocked out.

Clear to Send (CTS), CB - This signal from the data set must be active to enable the interface to transmit data. It must follow the RTS signal.

Data Terminal Ready (DTR), CD - This signal is active as long as the terminal is powered up.

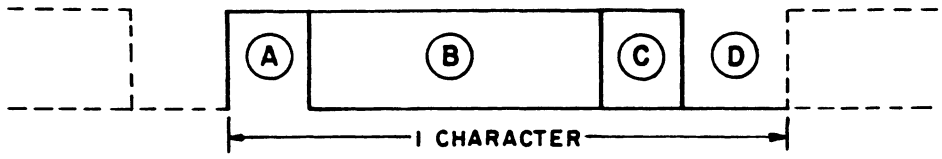
Data Set Ready, CC - This signal from the data set is passed on to the processor as a Status bit.

Carrier Detect - This signal from the data set is passed on to the processor as a status bit.

Data Format

The send data and receive data serial information is asynchronous. Figure 4-9 shows the serial data format. Both the receive and send portions must operate with the same format (number of data bits, stop bits, odd/even/no parity, and baud rates). The Least Significant Bit (LSB) of the character transmits first (after the start bit) and the Most Significant Bit (MSB) last. The receiver takes the first serial data bit as the LSB and the last one as the MSB. The transmitter idles in the mark state.

The number of data bits is selectable by program control. Parity or no parity is switch selectable (S2-5). If parity is enabled, the even or odd selection is performed under program control. The number of stop bits is switch selectable.



(A) 1 START BIT (SPACE OR HIGH)

(B) 5, 6, 7, OR 8 DATA BITS (1=MARK OR LOW, 0=SPACE OR HIGH)

(C) 1 OR NO PARITY BIT (EVEN OR ODD)

(D) 1 STOP BIT (MARK OR LOW)

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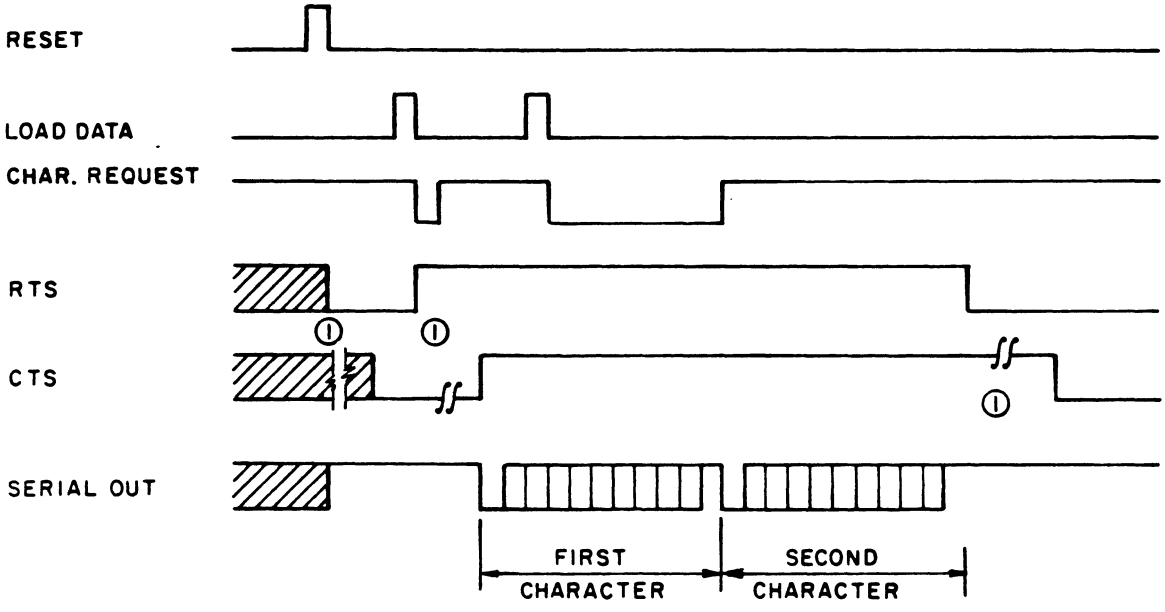
Figure 4-9. Serial Word Format

Timing

Figures 4-10 and 4-11 show the serial transmit and receive timing respectively.



(1) RTS→CTS DELAY CONTROLLED BY DATA SET

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Figure 4-10. Serial Transmit Timing

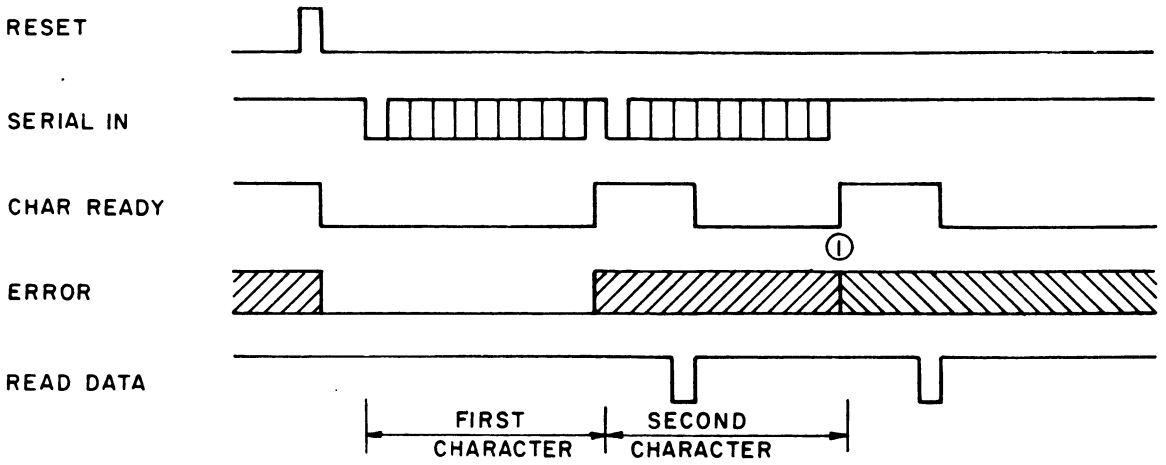


Figure 4-11. Serial Receive Timing

Switches

The Clear to Send and Parity Enable/Inhibit switches are available to select operating modes.

Clear to Send (CTS) - Switch S2-1 in the On (closed) position forces a constant CTS signal enabling transmission without the external CTS (without the modem). An active external signal is required when the switch is in the Off (open) position.

Parity Enable/Inhibit - Switch S2-6 in the On (closed) position enables the insertion of the Parity bit during transmissions and parity check during receptions. A load serial control function must be executed before a mode change is accepted. The even or odd selection is done under program control. This switch in the Off (open) position disables the parity circuits. The Stop bit must follow the last Data bit on transmission (receptions).

The processor can, by means of I/O instructions, transfer information between itself and the serial channel interface as summarized in table 4-2 and discussed in the following paragraphs.

TABLE 4-2. SERIAL CHANNEL I/O INSTRUCTIONS

NAME	ADDRESS	DESCRIPTION
Load Serial Data	Output 06	Data to be transmitted
Load Serial Control	Output 07	Control parameters
Read Serial Data	Input 05	Data received
Read Serial Status	Input 06	Status information

Load Serial Data (Output 06) - Upon reception of this function, the module transfers the contents of the data bus into the serial transmitter. If the transmitter is conditioned to transmit less than 8 data bits, it discards the excess most significant bits of the 8-bit-wide data bus; that is, the data bits to be transmitted have to be right-justified.

Before trying this command, the processor, or the system, must ensure the character-request signal is active (the transmit-holding register is empty); otherwise, data may be lost.

Upon loading of a character, the module activates the RTS signal and waits until the CTS becomes active before clocking the serial data out.

The module generates the Start, Parity, and Stop bits (according to the features previously selected) and inserts them in the corresponding bit slots.

Load Serial Control (Output 07) - The module loads the contents of the data bus into the control register. The information of the data bus is interpreted as follows:

- Data Bus Line 0 (Enable CREQ Interrupt) - If this line is a 1, it enables the character request interrupt; if a 0, it disables it. An interrupt is

generated when both the enable and the character request condition are true simultaneously (character request means the transmitter can accept one character of data to send).

- Data Bus Line 1 (Enable CRDY Interrupt) - The character-ready interrupt is enabled if this line is a 1 and disabled if it is a 0. An interrupt is generated when both the enable and the character-ready condition are true simultaneously (character-ready means the receiver has received a full character and the processor can take it). It does not mean that the character has no errors in it. The software should check the status word to verify the quality of the data.

- Data Bus Lines 2 and 3 (Select Word Length) - These 2 bits select how many Data bits are transmitted in each serial character or expected in each serial character received. Table 4-3 shows how the selection is performed.

TABLE 4-3. SERIAL CHANNEL WORD LENGTH SELECTION

DATA LINE 3	DATA LINE 2	NUMBER OF DATA BITS
0	0	5
0	1	6
1	0	7
1	1	8

- Data Bus Line 4 (Even/Odd Parity) - This line high conditions the module to generate and check for an even Parity bit. This line on low conditions the module to generate and check for an odd Parity bit. This circuit is disabled if parity is inhibited.

  Even parity means that the number of logical 1s in the data is even, while odd parity means that the number of logical 1s in the data is odd. The Start and Stop bits are excluded in the calculation.

- Data Bus Lines 5, 6, and 7 (Baud Rate Select) - The module generates some of the commonly used baud rates. Their selection is performed by these 3 bits shown in table 4-4.

TABLE 4-4. SERIAL CHANNEL BAUD RATE SELECTION

DATA LINE 7	DATA LINE 6	DATA LINE 5	BAUD RATE
0	0	0	150
0	0	1	300
0	1	0	600
0	1	1	1200
1	0	0	2400
1	0	1	4800
1	1	0	9600
1	1	1	19200

Read Serial Data (Input 05) - This function transfers data from the serial receiver to the processor. The data is valid only when the serial character ready status is set.

If the receiver is set to receive words with less than 8 bits, the data is right-justified within the 8-bit transfer.

Read Serial Status (Input 06) - This function transfers status information from the serial interface to the processor. The status word is as shown in figure 4-12.

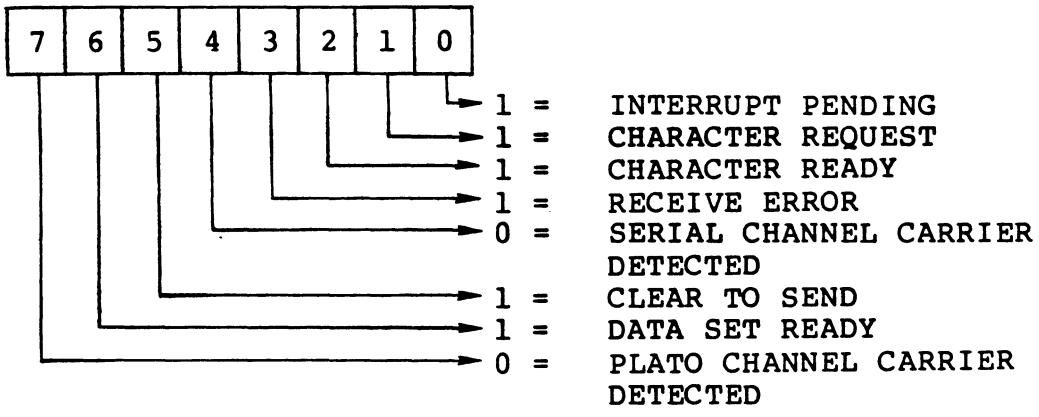


Figure 4-12. Serial Channel Status Word

The following paragraphs explain the meaning and use of these Status bits:

- Status Bit 0, Interrupt Pending - This bit is sent when an interrupt has been generated by either character request or character ready and remains set until the processor services it.

- Status Bit 1, Character Request - Character request means that the Transmitter Holding register is empty and a new character can be accepted. Loading data into it drops the character-request condition until the register is again empty.

- Status Bit 2, Character Ready - Character ready means that the Receiver Holding register has a character in it that can be removed by the processor. If the character is not removed within a character time, the following character received is transferred into the holding register, thus destroying the character (lost data).

  The character ready status is dropped by executing a read data function.

- Status Bit 3, Receive Error - The receive error condition can be generated by:

  - Parity Error - The Parity bit received in the character does not match the one generated by the receiver.

  - Framing Error - No Stop bit was detected in the Stop bit slot of the character.

  - Lost Data - A new character was received and transferred into the Receiver Holding register before the processor removed the previous one.

  The Status bit does not indicate which of the possible causes actually forced the error condition. Software should be prepared to recover from this mode of failure (request retransmission). The error condition is cleared automatically by reception of a new character containing no errors, provided that the character-ready condition does not exist when this happens.

- Status Bit 4, Serial Channel Carrier Detected - This bit, active low, indicates that the data set Carrier Detect signal is active at the serial channel interface.

- Status Bit 5, Clear to Send - This bit indicates that the data set Clear to Send signal is active.

- Status Bit 6, Data Set Ready - This bit indicates that the data set connected to this interface is ready.

- Status Bit 7, PLATO Channel Carrier Detected - This bit, active low, indicates that the Carrier Detect signal line is active at the PLATO communication interface connector (RJ1-8) or that the board connector signal AJ5-9 is an RS-232-C On or a TTL high.

Parallel Channel Interface

The parallel channel interface provides a means for the terminal to communicate and exchange information with 16 addressable, external devices. Data is exchanged in bit-parallel/byte-serial mode, with the terminal processor controlling the interface. The discussion here focuses on the signals and timing.

Signals

All voltage levels on the parallel channel are TTL compatible and defined as follows:

- Terminal output

Data Lines	Others
+2.0 V to +5.25 V = High	+2.4 V to +5.25 V = High
+0.0 V to +0.5 V = Low	+0.0 V to 0.4 V = Low

- Terminal input

Data Lines	Others
+2.0 V to +5.25 V = High	+2.4 V to 5.25 V = High
-0.25 V to +0.8 V = Low	-0.25 V to +0.8 V = Low

The signal definitions for the parallel channel interface are as follows:

- Data Line 0 through Data line 7 - These eight bidirectional lines carry the information from the terminal to the external devices or vice versa, depending on the setting of the control signals external write and external read. The kind of information carried is defined by the setting of the five address lines which determine the device being communicated with and the function taking place.

- These eight lines are driven by the terminal during module outputs (external write active) and by the device during terminal inputs (external read active).

NOTE

Unless a device is requested to place data on the data lines, its data line drivers must be in the high impedance state.

- Address Line 0 through Address Line 5 - These six output lines, driven by the terminal, determine the device to receive or send data and the kind of function to be performed on the data.

- External Write - When active, this control signal, driven by the terminal, indicates that the information on the data bus goes from the terminal to the device defined by the address bus. The device should get ready to receive data.

- External Output - This control signal, driven by the terminal, complements the External Write signal. External Write defines the direction of the flow of data; External Output active indicates that the data is on the data lines and stable; and the device defined by the address lines is to act on it.

- External Read - When active, this control signal, driven by the terminal, indicates that the device defined by the address lines is to place the requested information on the data lines. Only at this time can the device turn on its data line drivers.

- External Ready - When active, this signal, driven by the addressed device, indicates that the I/O cycle initiated by the terminal has been completed by the device (data was taken by the device during terminal outputs or placed on the data lines by the device during terminal inputs).

- Interrupt Line - This line is common to all devices on the parallel channel and any of them can activate it at any time. Its purpose is to tell the processor to process data over the parallel channel, since all the activities on this channel are initiated by the processor. When the processor has acknowledged and serviced the interrupting device, it must deactivate this line.

Figures 4-13, 4-14, and 4-15 show the three possible cases of interface timing for input and output cycles. The processor in the three cases starts the sequence in the same fashion; the difference between cases depends exclusively on the device response. All timing is referenced to the parallel channel connector RJ2 at the terminal.

The three cases described for the output cycle (no extra wait states, extra wait states, and timeout) also apply to the input instruction, the only difference in requirements being that in input cycles the device must have the requested data on the bus before 750 nanoseconds for the no extra wait state case or before the external ready goes high for the extra wait states case.

Output Cycle - The processor places the address and data on the bus (shown by the drivers going from tristate floating to bipolar state). Fifty nanoseconds later the External Write goes active (low). At this time, the devices on the bus can start sampling the address code, and the device that matches it can start conditioning the external ready line.

The External Output signal goes active (low) 250 nanoseconds after the External Write. The data is perfectly stable at this time, and the addressed device can use this strobe to latch the data. The processor timing stops and the sequence is restarted by the External Ready Signal.

The processor samples the external ready line continuously, starting 750 nanoseconds after the External Write was issued. To allow for gate delays, cable length, and a safety margin, the device should condition the external ready line within 625 nanoseconds after the External Write is received. It should be in the high state (ready) if the data on the data bus was taken or processed; pulled down (not ready) otherwise.

- Output with no extra wait states (figure 4-13) - If the external ready line is high and stable 750 nanoseconds after the External Write, the processor assumes that the data was successfully transferred and terminates the output cycle by turning all the drivers off and executing the next program instruction.

- Output with extra wait states (figure 4-14) - If the external ready line is low 750 nanoseconds after the External Write, the processor goes into Wait mode until it sees the external ready line go high. At this point, the sequence continues as described in the previous paragraph. Notice that in the Wait mode the processor could not execute the program; therefore, the processor overall throughput is decreased.

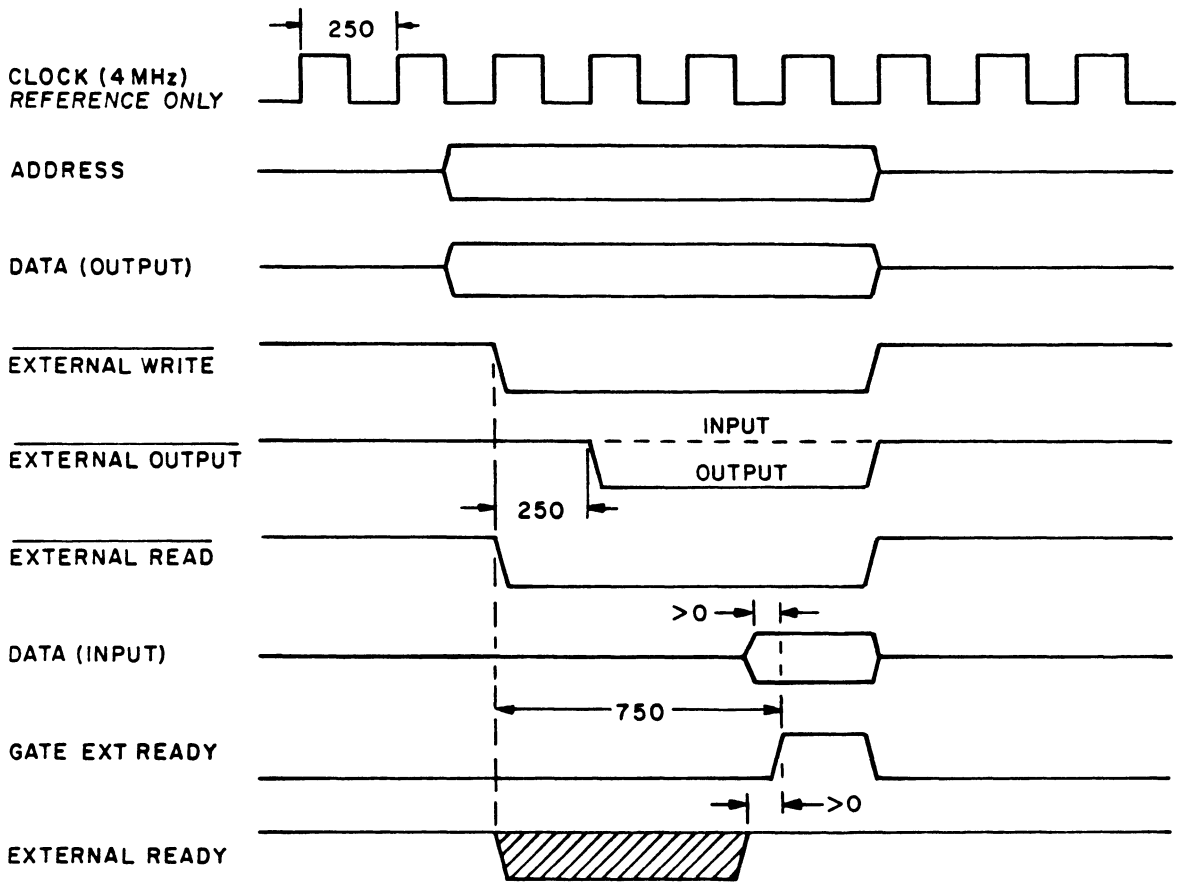
- Output with timeout (figure 4-15) - If the external ready line is low 750 nanoseconds after the External Write and remains low for the next 64 microseconds (+20 percent), the interface terminates the output cycle by simulating an External Ready and setting a timeout status bit. Note that:

  - The timeout condition is guaranteed not to occur if the external ready line is high and stable within 43.2 microseconds after the External Write signal.

  - Since the processor does not know whether the completion of the cycle was due to a device-activated External Ready or a timeout condition, the driver routine for this interface should have a check of the status bit immediately after the output instruction.

  - While in the Wait mode, the processor is not refreshing the program memory. The processor must perform 128 refresh cycles during every 2-millisecond period in order to maintain the program memory contents. These refresh cycles are performed automatically by the processor, one after each fetch instruction operation. Given the worst case practical condition of executing block move instructions located in the display memory space with all memory references also within the display memory space, there is 752 microseconds to spare during any 2-millisecond period while still satisfying the refresh requirements. To ensure that program memory refresh requirements are met under all conditions, the program prevents the occurrence of more than 11 timeout conditions during any 2-millisecond period.

  The timeout status is automatically reset at the beginning of an I/O cycle.



NOTE: ALL TIMES IN NANOSECONDS.

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Figure 4-13. External Input or Output Timing (No Extra Wait States)

Input Cycle - The processor places the address on the bus (shown by drivers going from tristate floating to bipolar state). Fifty nanoseconds later the External Read signal goes active (low). At this time, the devices can start sampling the address bus and the device that matches the address code can start conditioning the external ready line and turn the data drivers on (shown by the drivers going from tristate floating to bipolar state).

The processor timing stops and the sequence is resumed by the External Ready signal.

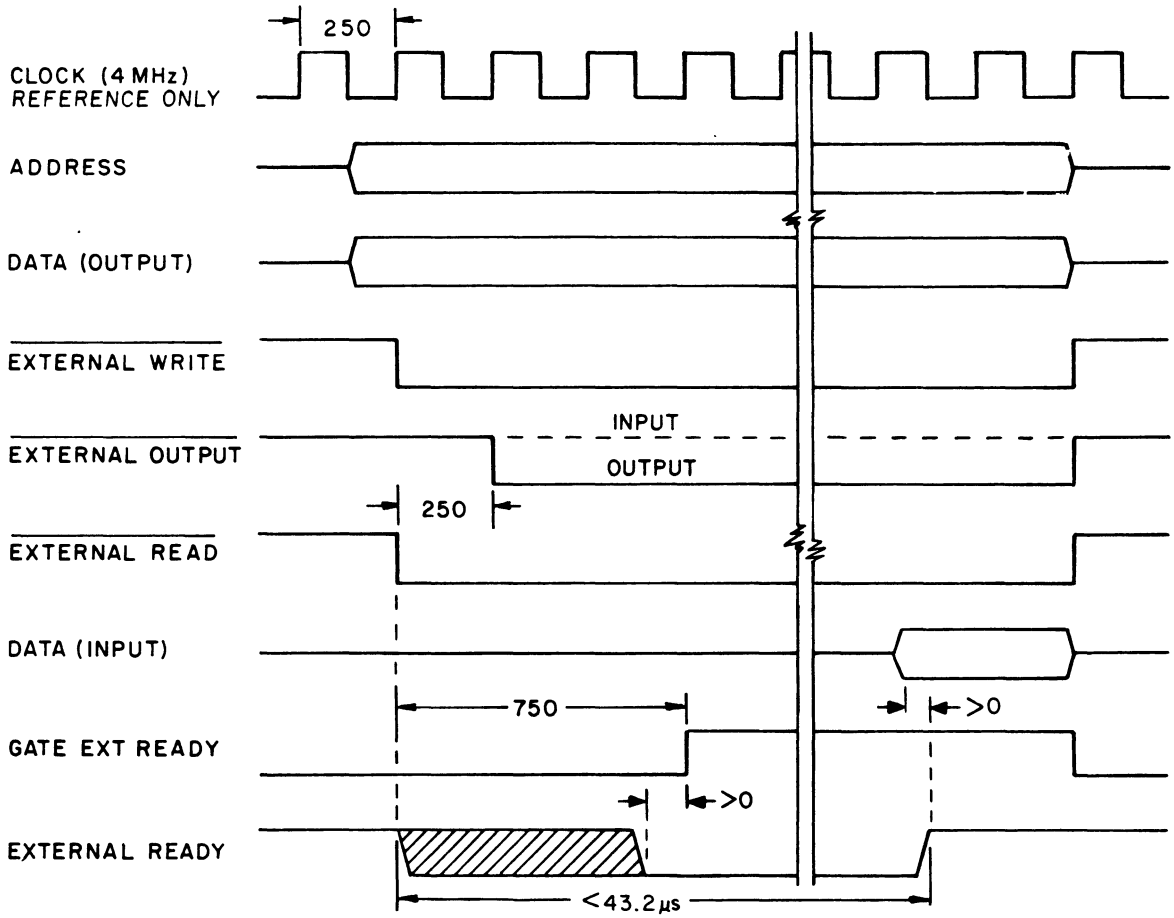


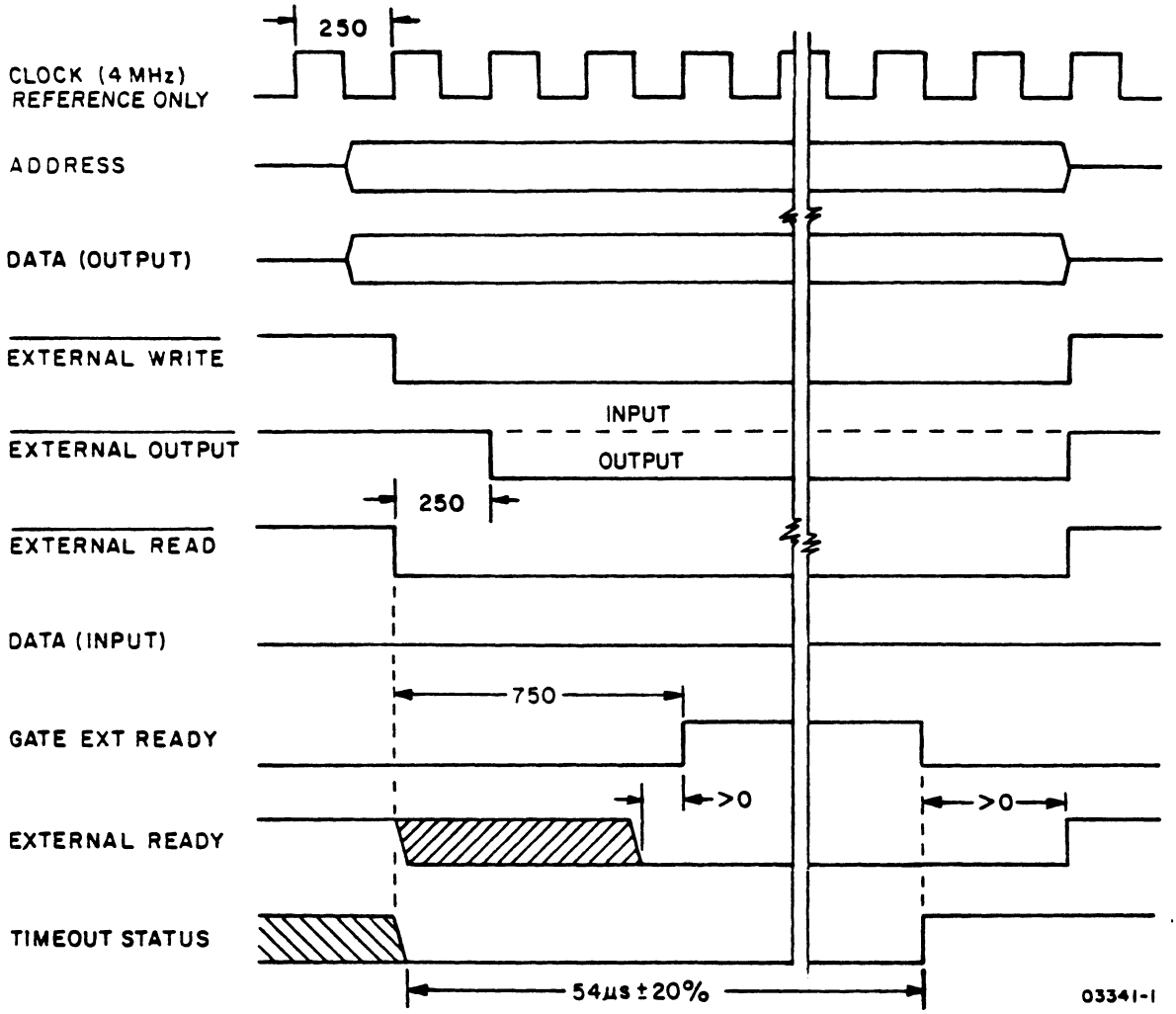
Figure 4-14. External Input or Output Timing (With Extra Wait States)

Terminal Identification

There are 16 selection jumpers on the controller board that have been individually opened or left shunted, as required, to establish a unique 16-bit terminal identification (ID) code. Under program control, this ID code can be read and transmitted to the host. This ID code is factory set only.

Programming

All the I/O instructions whose address have bit 2^5 set route through the parallel channel interface. The actual addressing/function codes (lower 5 bits of address code), as well as the meaning of the information transferred is device dependent.



NOTE: ALL TIMES IN NANOSECONDS UNLESS STATED OTHERWISE.

Figure 4-15. External Input or Output Timing (Timeout Condition)

VIDEO BOARD

The video board provides timing and memory capabilities to support the controller board and the display module. A block diagram of the video board is illustrated in figure 4-16. The following is a list of some of the features provided by the video board:

- 32K 8-bit words of RAM for crt refresh
- 16K 8-bit words of RAM for programs (basic memory)
- Provision for 16K 8-bit words of RAM expansion

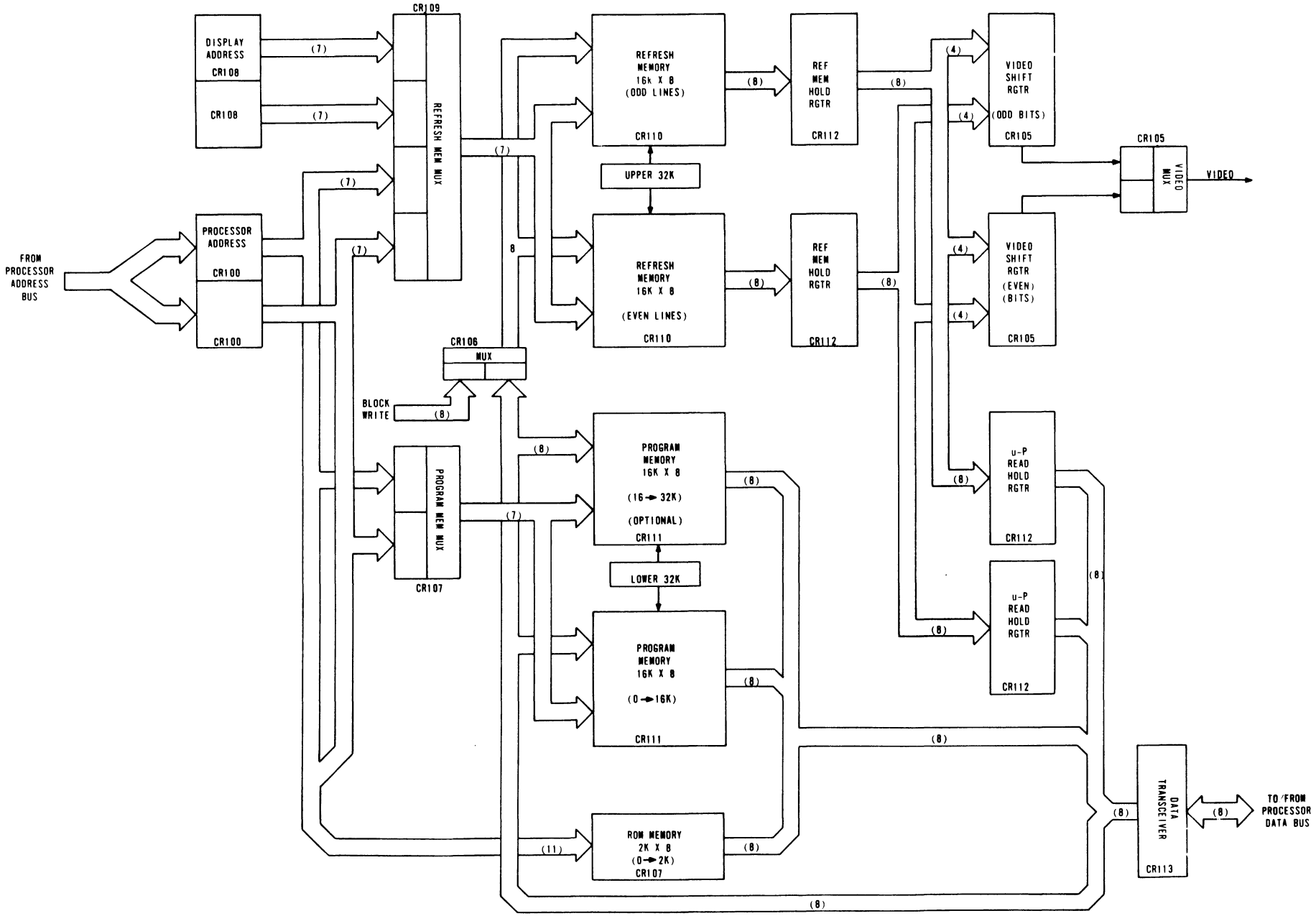


Figure 4-16. Video Board Block Diagram

- 2K 8-bit words of ROM/EROM for terminal diagnostic and loader program
- Timing generation for the display, memory, and controller board
- Composite video output for external devices

Memory Expansion

The memory expansion consists of 16K 8-bit words. The module consists of 8 ICs which are to be plugged into the Video PCB. The board already has all the sockets to accept the ICs and support logic to integrate them into the terminal. Switch S2-10 on the Controller Board must be placed in the Off position (open).

Programming

All functions and capabilities of the terminal are controlled by a program residing in memory and executed by a Z80 microprocessor LSI chip. State time is set at 250 nanoseconds. The following paragraphs discuss the memory structure.

Memory Structure

Figure 4-17 shows the memory breakdown and addressing. The following paragraphs discuss:

- Read-Only Memory
- Program RAM
- Display Refresh Memory
- Control of Peripherals
- I/O Peripheral Devices
- Read Configuration Switches
- Load Maintenance Register
- Read Keyboard Data
- Load Transmitter Lower Bits
- Read Touchpanel Data
- Load Transmitter Upper Bits
- Read Lower ID
- Bulk Write/Erase
- Read Upper ID
- Load Interrupt Mask
- Read Serial Data
- Miscellaneous Control
- Read Serial Status
- Load Serial Data
- Read Controller Status
- Load Serial Control
- Read Communication Line
- Input Parallel Channel
- Output Parallel Channel

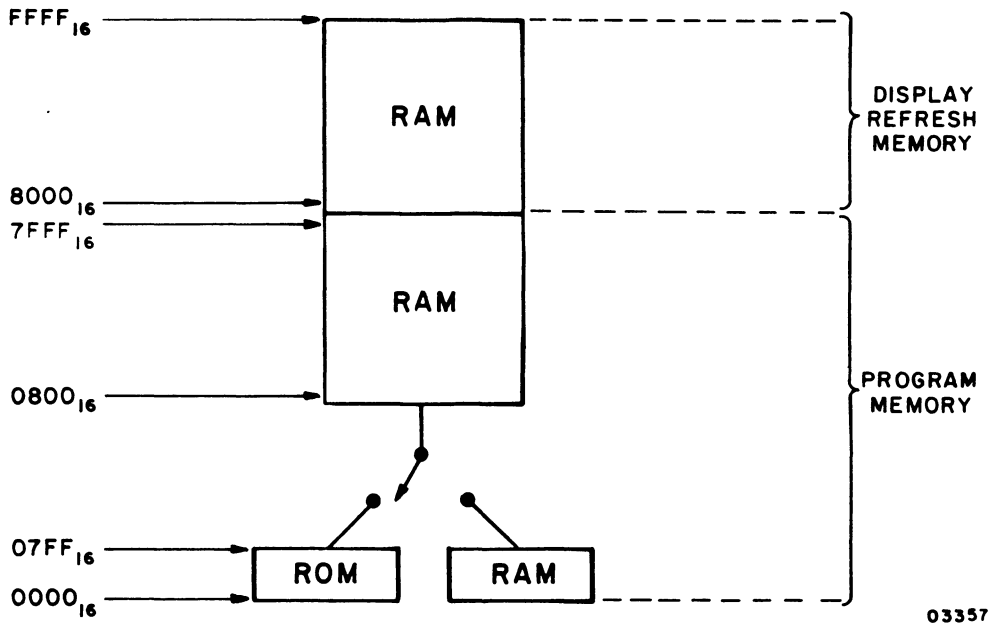


Figure 4-17. Memory Assignment

Read-Only Memory - There are 2K by 8 words of ROM in the terminal. Starting address is 0000_{16} and final address is $07FF_{16}$. Access time of this memory is 350 nanoseconds.

Program RAM - The terminal has a minimum of 16K 8-bit words of RAM. A memory expansion can be added to obtain a total of 32K 8-bit words of RAM.

Starting address for the basic program memory is 0000_{16} and final address is $3FFF_{16}$. The first address of the memory expansion is 4000_{16} and the final address is $7FFF_{16}$. Access time is 300 nanoseconds.

NOTE

The set of addresses between 0000_{16} and $07FF_{16}$ define both ROM and RAM. Upon power on or activation of the RESET switch, this range of addresses selects the ROM, and remains in this mode until the program instructs the hardware to deselect the ROM and select the RAM (or vice versa).

Display Refresh Memory - These 32K 8-bit words of memory (262 144 bits) are part of the processor memory and contain all the information to be displayed on a 512 by 512 (262 144 dots) matrix crt screen. Each bit of information in this memory represents a dot on the screen. A logical 1 (0) in memory equals a white (black) dot on this screen. The starting address is 8000_{16} and the final address is $FFFF_{16}$ (Address Bit 2^{15} is always set when referencing this memory).

Both the processor and the display have access to this memory, with the display having a higher priority, which means that, on the average, the processor has to wait to gain access to this memory.

Control of the Peripherals - A peripheral device is any device, interface, or function that performs a task when commanded to do so by the processor. The peripherals may be internal or external, and their complexity may vary from simple holding registers to sophisticated LSI functions. Their operation and responses are described in the following paragraphs.

- Display - As seen by the processor, the display is nothing more than a portion of the terminal memory (the refresh memory). Data is displayed on the screen by executing write instructions into this memory.

  Each bit of information written on this memory represents a dot on the screen (as opposed to alphanumeric terminals, where a 7-bit code in memory represents, for example, a 7- by 9-dot matrix symbol).

- Refresh Address/Display Portion - There is a one-to-one relationship between the address of the refresh memory where data is written and the X/Y coordinate where this data is displayed. The correspondence is as follows:

  - Each refresh memory address contains 8 bits (dots) of information. These 8 bits are positioned on the screen in the horizontal direction, with the data bit 0 at the left and data bit 7 at the right.

  - The lowest refresh memory address (8000_{16}) corresponds to the upper left corner of the display (the corner dot plus the seven dots to the right of it).

- Increasing the address by one is equivalent to moving one dot to the bottom on the screen (still controlling eight horizontal dots).

- There are 512 horizontal lines within a column. The lower 9 bits of the 16-bit refresh memory address determine 1 of the possible 512 lines.

- The next 6 bits (A09-A14) of the refresh memory address select 1 of the 64 vertical columns (each column is 8 bits, or dots, wide). Increasing the column address by one is equivalent to selecting the next column to the right.

Each address uniquely selects a group or set of 8 bits (dots). Selection of a bit or bits within this group is accomplished by data manipulation.

For example, write a 1 and then a 0 in the screen position located 21 dots to the right and 9 dots below the upper left corner dot (figure 4-18). Do not modify any other data on the screen.

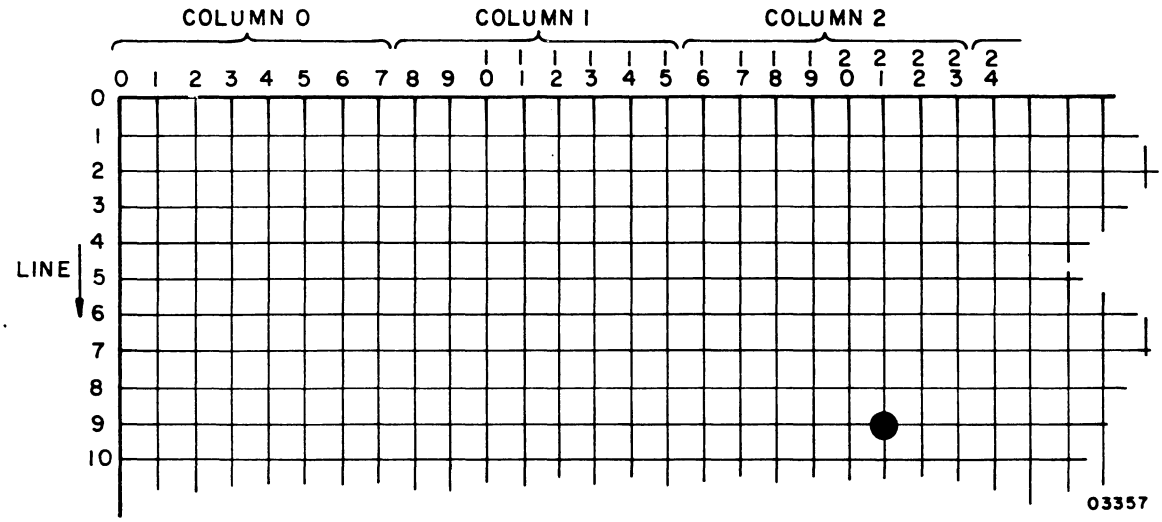


Figure 4-18. Address 8409_{16}

The addressing is formed as follows:

- The lower 9 bits define the line position, with 0 0000 0000 at the top. The desired location is 9 dots away from the top the line address is:

  $$A_8 - A_0 = 0\ 0000\ 1001$$

- The column address defines groups of 8 bits in the horizontal direction, with 00 0000 on the extreme left. The desired location is 21 dots away from the left, the column address is:

  $$A_{14} - A_{09} = 21/8 = 2 \text{ (Remainder = 5)}$$

  $$A_{14} - A_{09} = 00\ 0010 \text{ (Data Bit 5)}$$

  By dividing the X coordinate by 8 it can be seen that the integer result defines the column and the remainder defines the Data Bit to be used in the manipulation.

- Address Bit 15 must be set to select the refresh memory address.

  The complete address is:

  $$\begin{aligned}\text{Address} &= 1\ 000010\ 00000\ 1001 \\ &= 1000\ 0100\ 0000\ 1001 \\ &= 8409_{16}\end{aligned}$$

The Read/Write instruction affects 8 bits at the time. Only the Data Bit 5 must be altered, the following masks are generated.

$$\text{Write Mask} = 0010\ 0000 \text{ (DB5 set)} = 20_{16}$$

$$\text{Erase Mask} = 1101\ 1111 \text{ (DB5 clear)} = DF_{16}$$

The program is:

LD	A, (8409H)	Load A register with 8-bit word from location 8409H
OR	A, 20H	OR data in A register with write mask. This sets bit 5 of the data without modifying the other 7 bits.
LD	(8409), A	Store contents of A register in location 8409H. The desired dot on the screen is now illuminated.
AND	A, ODFH	The data just stored in memory and still in the A register is ANDed with the erase mask. Bit 5 is reset without modifying the other 7 bits.
LD	(8409), A	Store the A register in location 8409H. The desired dot on the screen is now dark.

I/O Peripheral Devices - All the peripheral devices except the display are controlled by the processor by means of I/O instructions. These instructions perform functions, such as transfer data, control parameters, and status information. The secondary byte of the I/O instruction defines the device/function with which the processor exchanges data. Table 4-5 is a complete list of all the defined device/functions of the terminal.

Read Configuration Switches (Input 00) - This command reads the setting of eight switches, five of them external, the rest on the controller board.

Load Maintenance Register (Output 00) - This instruction transfers the data output by the processor into an 8-bit holding register. Each bit of this register has a function, as follows:

- Data Bit 0, ERR LED - This maintenance register output drives an LED labeled ERR (error). Loading a 0 in the register turns the light on (1 equals off). This output is a 0 upon power on or reset.

- Data Bit 1, XMT LED - If the terminal is in Test mode the output of this register drives an LED labeled XMT (transmitted data). A 0 turns the light on and a 1 turns it off. It is a 0 upon power on or reset.

- Data Bit 2, RCV LED - The same description as Data Bit 1 but to the LED labeled RCV (Received Data).

- Data Bit 3, RTS, LED - The same description as Data Bit 1 but to the LED labeled RTS (Request to Send).

- Data Bit 4, DSR LED - The same description as Data Bit 1 but to the LED labeled DSR (Data Set Ready).

- Data Bit 5, DTR LED - The same description as Data Bit 0 but to the LED labeled DTR (Data Terminal Ready).

- Data Bit 6, Test Mode - This bit controls the hardware maintenance features of the terminal. It places the PLATO communication interface and the serial channel interface in loopback mode (the transmitters connected to their respective receivers) and disconnects the external drivers. Data output by the processor under these conditions is received by the same processor that is now able to compare the data integrity. It also controls the source signals to drive the front panel LEDs. In Test mode, the processor has control of these six indicators. When not in Test mode, only the ERR and DTR indicators remain under processor control; the others are driven by the modem or terminal hardware.

  A 0 loaded in this bit position puts the terminal in Test mode, and a 1 puts it in Normal mode. The terminal goes into Test mode automatically upon power up or activation of the RESET switch.

- Data Bit 7, ROM Enable - This bit controls the ROM/RAM overlap. Both ROM and RAM can be referenced in the address range from 0000_{16} through $07FF_{16}$, and the memory selection itself is done by this bit. ROM is selected when this bit is a 0, and RAM will be selected when it is a 1. This bit is a 0 (ROM selected) upon power up or when the RESET switch is pressed.

NOTE

RAM addresses 0000_{16} through $07FF_{16}$ are not available when executing programs in ROM, and ROM is not available when running programs in 0000_{16} through $07FF_{16}$ in RAM.

TABLE 4-5. INPUT AND OUTPUT FUNCTIONS

ADDRESS*								NORMALIZED (HEX)**	I/O	DESCRIPTION
7	6	5	4	3	2	1	0			
X	X	0	X	0	0	0	0	00	I	Read configuration switches
X	X	0	X	0	0	0	0	00	O	Load maintenance register
X	X	0	X	0	0	0	1	01	I	Read keyboard data
X	X	0	X	0	0	0	1	01	O	Load transmitter lower bits
X	X	0	X	0	0	1	0	02	I	Read touchpanel data
X	X	0	X	0	0	1	0	02	O	Load transmitter upper bits
X	X	0	X	0	0	1	1	03	I	Read lower ID
X	X	0	X	0	0	1	1	03	O	Bulk write/erase - video enable
X	X	0	X	0	1	0	0	04	I	Read upper ID
X	X	0	X	0	1	0	0	04	O	Load interrupt mask
X	X	0	X	0	1	0	1	05	I	Read serial data
X	X	0	X	0	1	0	1	05	O	Miscellaneous control
X	X	0	X	0	1	1	0	06	I	Read serial status
X	X	0	X	0	1	1	0	06	O	Load serial data
X	X	0	X	0	1	1	1	07	I	Read controller status
X	X	0	X	0	1	1	1	07	O	Load serial control
X	X	0	X	1	X	X	X	08	I	Read communication line
X	X	1	Y	Y	Y	Y	Y	2Y,3Y	I	Input - parallel channel
X	X	1	Y	Y	Y	Y	Y	2Y,3Y	O	Output - parallel channel

*X = 0 or 1 irrelevant. Y = External device address.

**The normalized hexadecimal code is obtained by making X = 0.

Read Keyboard Data (Input 01) - This function transfers data from the keyboard interface to the processor. This data is valid only when the keyboard ready status is present or after receiving a keyboard interrupt.

Load Transmitter Lower Bits (Output 01) - This function transfers 8 bits of data from the processor to the 12-bit shift register, which serializes the data to be sent to the PLATO system. Data should be transferred only when the transmitter is not active, that is, communication line request status is present, to avoid losing or destroying data. This function loads part of the transmit shift register; it does not initiate transmission or modify the status of the interface.

Read Touchpanel Data (Input 02) - This function transfers data from the touchpanel interface to the processor. This data is valid only when the touchpanel ready status is present or after receiving a touchpanel interrupt.

The data format is as follows: This word defines 1 of 16 X columns and 1 of 16 Y rows (1 of 256 locations). The origin X equals 0, Y equals 0 is the lower left corner of the screen.

Load Transmitter Upper Bits (Output 02) - This function transfers 8 bits of data from the processor to the 12-bit shift register, which serializes the data to be sent to the PLATO system . Data should be transferred only when the transmitter is not active, that is, communication line request status is present, to avoid losing or destroying data. In addition, this function loads data into the transmit register, initiates the transmission, and drops the request status condition.

Read Lower ID (Input 03) - This function transfers the setting of the lower 8 bits of the ID switches to the processor. The 16 ID switches are set to a unique code for each terminal and sealed at the factory.

Bulk Write/Erase (Video Enable/Disable, Output 03) - The operation of this function is dependent on Data Bits 0, 1, and 2 as summarized in table 4-6.

TABLE 4-6. BULK WRITE/ERASE - VIDEO ENABLE FUNCTION

DATA BITS			OPERATION
2	1	0	
0	0	X	Disable video
0	1	X	Enable video
1	0	0	Bulk erase and Disable video
1	0	1	Bulk write and Disable video
1	1	0	Bulk erase and Enable video
1	1	1	Bulk write and Enable video

X = 0 or 1 irrelevant.

This function with Data Bits 1 and 2 equals 0 places the terminal in nondisplay mode without affecting the display memory contents. In this nondisplay mode, the video signal to the monitor and to the composite video interface is forced to the blanking state. The intended use of this nondisplay mode is to allow blanking the display, if desired, while the display memory space is being used as extended program memory.

This function with Data Bit 2 equals 0 and Data Bit 1 equals 1 reenables the video to the monitor and to the composite video interface (if previously disabled) without affecting the display memory contents.

This function with Data Bit 2 equal to 1 initiates a hardware write or erase of the complete refresh (display) memory. The state of Data Bit 0 determines whether all 1s (Data Bit 0 equals 1) are written, giving a completely illuminated display, or all Os (Data Bit 0 equals 0), producing a totally blank (black) display. Either the bulk write or bulk erase operation, when completed, also reenables the video to the monitor and to the composite video interface (if previously disabled). The full refresh memory bulk write or erase takes about 14 milliseconds, and writing data to the refresh memory should not be attempted during this time as it may be destroyed. The Bulk Busy status bit monitors this activity. Data Bits 2 through 7 are ignored during this output function as indicated in table 4-6.

Read Upper ID (Input 04) - This function is the same as Read Lower ID; but, transfers the remaining 8 bits.

Load Interrupt Mask (Output 04) - This function transfers 8 bits of data from the processor to the Interrupt Mask register, whose outputs control the interrupt traffic to the processor. Each of the eight interrupt levels of the terminal has an associated bit in the Mask register. If the bit in the mask is a 1, the incoming interrupt is allowed to pass and reach the processor, otherwise it is blocked off.

Each interrupt level that reaches the processor generates an interrupt vector uniquely defining its level (interrupt trap address). If more than one interrupt level is active at the same time, the hardware blocks all except the one that has the highest priority. Table 4-7 shows the data bit assignments, priorities, interrupt sources, and interrupt vectors.

TABLE 4-7. INTERRUPT DESCRIPTION

PRIORITY	SOURCE	INTERRUPT MASK (DATA BIT)	INTERRUPT VECTOR (HEX CODE)
0*	Serial channel	0	00
1	Communication line ready	7	02
2	Communication line request	4	04
3	Keyboard data ready	6	06
4	Touchpanel data ready	5	08
5	Short interval	1	0A
6	External interrupt	3	0C
7**	Long interval	2	0E

*Highest order bit.
**Lowest order bit.

The interrupt sources are:

- Serial Channel - Either character request or character ready.
- Communication Line Ready - The PLATO receiver has a byte ready to be transferred to the processor.
- Communication Line Request - The PLATO transmitter is inactive and can accept data from the processor.

- Keyboard Data Ready - The keyboard interface has detected the depression of a key and is saving the data for the processor.

- Touchpanel Data Ready - The touchpanel interface has detected a touch and is saving the X/Y data for the processor.

- Short Interval - This interrupt is generated by a flip-flop that is switched to the set state every 104 microseconds. The only way to clear this flip-flop is to make its associated mask bit a 0 (if more interrupts are needed, the mask should then be reenabled).

NOTE

This interrupt guarantees only that a 104-microsecond interval occurs between interrupts.

- External Interrupt - This interrupt is generated by devices external to the terminal and connected to it by the parallel channel.

- Long Interval - Analogous in operation to the short interval, but the time between interrupts is set to 833.3 microseconds.

The interrupt vector forms the lower 8 bits of the interrupt trap address. The processor must execute programs in Interrupt Mode 2 and preset the upper 8 bits of the address in the I register. The mask is reset to all Os - all interrupts disabled - upon power on or reset.

Read Serial Data (Input 05) - This function transfers 8 bits of data from the serial channel receiver to the processor.

Miscellaneous Control (Output 05) - This function transfers data from the processor to a control register to implement the features shown in table 4-8 and further explained in the following paragraphs.

TABLE 4-8. MISCELLANEOUS CONTROL

Data Bit	Control Feature
0	1 = Sound alarm
	0 = No operation
1	0 = DTR ON
	1 = DTR OFF
2	0 = Reset flag
	1 = Set flag

- Data Bit 0, Alarm - The output function with bit 0 set to 1 triggers an 80-millisecond audible tone. If bit 0 is not set, the alarm does not sound. The alarm timer is retriggerable; therefore, the programmer can repeat this output function and keep the alarm sounding. The alarm keeps sounding for 100 milliseconds after the last function is received.

- Data Bit 1, Programmable DTR - The processor has control of the DTR signal. It is forced to the ON state by power on or the RESET switch, and then it can be software controlled. Data Bit 1 set to 0 turns the signal on and Data Bit 1 set to 1 turns it off.

- Data Bit 2, Hardware Flag - This bit controls the state of a flip-flop that can be read by the processor. A 1 sets the flip-flop and a 0 clears it.

  A unique feature of this flip-flop is that it comes up set upon power on, but it is not modified by the RESET switch. These two conditions force the processor to start executing at address 0000, this flip-flop can inform the processor as to which of the conditions actually occurred. (The program should check the state and reset it immediately.)

- Data Bits 3 through 7 (Not assigned) - These five bits are ignored by the terminal.

Read Serial Status (Input 06) - This function transfers status information from the serial channel interface to the processor.

Load Serial Data (Output 06) - This function transfers data from the processor to the serial channel.

Read Controller Status (Input 07) - This function transfers status information from different interfaces of the terminal to the processor. Figure 4-19 shows the configuration of the status word and the following paragraphs explain their meaning.

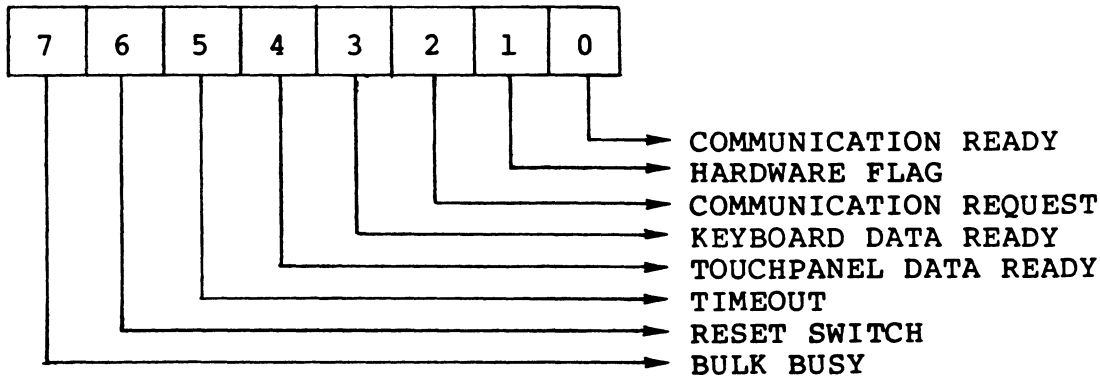


Figure 4-19. Controller Status Word Format

- Data Bit 0, Communication Ready - This bit set indicates that the PLATO receiver has clocked in 7 bits of serial data and that it is ready to transfer them to the processor. The processor should remove this byte by executing a read communication line function, which transfers the data and reset the status bit. This signal also generates the comm line ready interrupt.

- Data Bit 1, Hardware Flag - This bit is the output of the hardware flag flip-flop, which is controlled by the processor or the power-on sequence.

- Data Bit 2, Communication Request - This bit set indicates that the PLATO transmitter is inactive and can accept data to transmit. A load transmitter lower bits and load transmitter upper bits should be executed to load data, initiate the transmission, and reset this status bit. This signal also generates the communication request interrupt.

- Data Bit 3, Keyboard Data Ready - This bit set indicates that the keyboard interface has detected a key depression and is holding the code to transfer it to

the processor. A read keyboard data function transfers the data and resets this status bit. This signal also generates the keyboard data ready interrupt.

- Data Bit 4, Touchpanel Data Ready - This bit set indicates that the touchpanel interface has detected a touch and is saving the X/Y information. A ready touchpanel data function should be executed to transfer the data and reset this status bit. This signal also generates the touchpanel data ready interrupt.

- Data Bit 5, Timeout - This bit set indicates that an I/O cycle to an external device on the parallel channel was not completed in the allotted time. The hardware aborts the I/O cycle and sets this status bit. The program should, after every I/O cycle to external devices, check this bit to know whether the completion of the I/O was due to normal or abnormal circumstances.

  This bit clears automatically at the beginning of the next external I/O cycle (and sets again if it fails).

- Data Bit 6, RESET Switch - This bit carries information on the status of the RESET switch: a 0 when it is being held down and a 1 under normal conditions. (The reset pulse acting on the hardware is independent of the duration of the switch depression, therefore, the terminal could be running while this switch is down.)

- Data Bit 7, Bulk Busy - This bit monitors the activity of the hardware Bulk Write/Erase circuit. It is a 1 only while the hardware Bulk Write /Erase is taking place.

Load Serial Control (Output 07) - This function transfers control parameters from the processor or the serial channel interface.

Read Communication Line (Input 08) - This function transfers 8 bits of information from the PLATO receiver to the processor. This data is valid only when the Communication Ready status bit or interrupt is set. This status/ interrupt condition is removed automatically at completion of the transfer cycle.

Input Parallel Channel (Input 2Y, 3Y) - Any input instruction whose address has bit 2^5 set indicates a transfer of data from external devices to the processor.

Output Parallel Channel (Output 2X, 3X) - Any output instruction whose address has bit 2^5 set indicates a transfer of data from the processor to an external device.

Composite Video Interface

The composite video interface generates and supplies a noninterlaced, composite video signal equivalent to and in synchronous with the picture being displayed on the terminal screen. The output signals consist of three voltage levels:

V_{out} = 0.0 to 0.2 V sync level

V_{out} = 0.5 to 0.7 V black level

V_{out} = 1.5 to 1.7 V white level

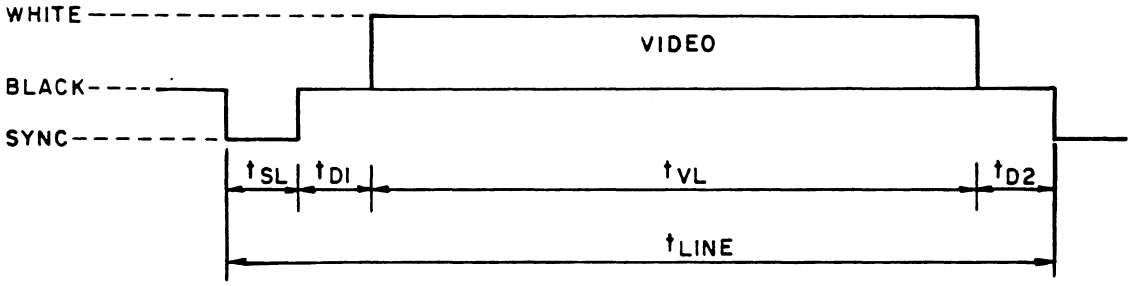
The video information is digital, black or white, with no intermediate gray levels.

The maximum data rate supplied by this interface is 12.048 mHz (41.5 nanoseconds, white; 41.5 nanoseconds, black).

The timing of the signals is nonstandard. Figures 4-20 and 4-21 show the 60-Hz and 50-Hz timing for the line and frame portion of the signals.

A display monitor connected to this interface duplicates the image of the terminal display when:

- Line scanning (34.23 kHz rate) is performed horizontally, from left to right of the screen (retrace from right to left)
- Frame scanning (50 or 60 Hz) is performed vertically, from top to bottom (retrace from bottom to top).



t_{SL} = SYNC WIDTH = 2.998 uSEC

t_{DI} = SYNC/VIDEO DELAY = 2.998 uSEC

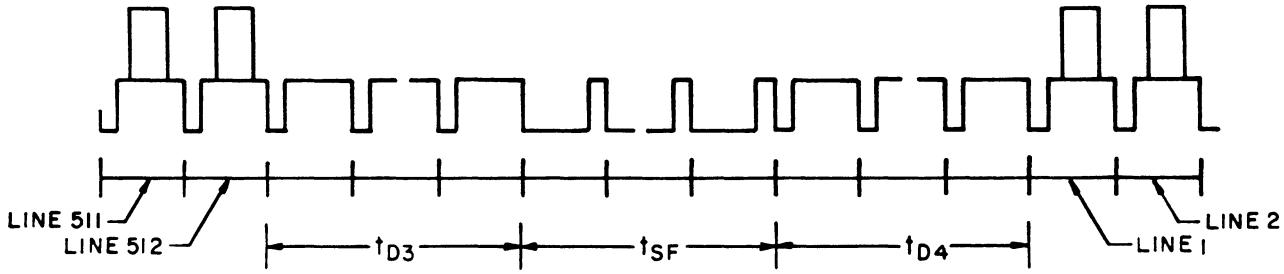
t_{VL} = VIDEO FIELD = 21.248 uSEC

t_{D2} = VIDEO/SYNC DELAY = 1.972 uSEC

t_{LINE} = 29.216 uSEC (34.23 KHZ)

03358

Figure 4-20. Scan Line Timing (50/60 Hz)



		60 HZ		50 HZ	
		(LINES)	(m SEC)	(LINES)	(m SEC)
	VIDEO WIDTH	512	14.959	512	14.959
t_{D3}	VIDEO/SYNC DELAY	19	0.555	73	2.133
t_{SF}	FRAME SYNC	4	0.117	4	0.117
t_{D4}	SYNC/VIDEO DELAY	25	0.730	96	2.805
	FRAME TIME	570	16.653	685	20.013

03358

VIDEO/SYNC DELAY 16.653

Figure 4-21. Frame Timing (50/60 Hz)

COMMUNICATION INTERFACE/INTERNAL MODEM

This expansion module interface connects the terminal processor to a communication adapter module (modem). The interface connector is a PC-mounted, 20-pin flat ribbon cable, CDC #51847500; the mating connector is CDC #65853405. Table 4-9 describes the pin assignments of the internal interface. Figure 4-22 shows the actual wiring of the PLATO interface signals and expansion module signals. The signal descriptions are as follows:

- Power and Ground - Power available for the optional adapter board is:

  +5 V - 250 mA (1.25 W)
  +12 V - 100 mA (1.2W)
  -5 V - 150 mA (0.75 W)
  -12 V - 100 mA (1.2 W)

- DATA/TALK Switch - This switch is on the front panel of the terminal. Set to TALK, the contacts are open, and set to DATA, the contacts are closed. This switch simulates the exclusion key of some telephone sets.

TABLE 4-9. EXPANSION MODULE PIN ASSIGNMENTS

PIN (RJ5)	SIGNAL	ORIGIN	DESTINATION
1	Logic Ground	-	-
2	-12 V	-	-
3	Logic Ground	-	-
4	-5 V	-	-
5	DATA/TALK Switch	Front panel	
6	Transmitted Data	Controller	
7	Received Data	*	Controller
8	Data Set Ready*	**	Controller
9	Carrier Detect**	***	Controller
10	Logic Ground	-	-
11	+12 V	-	-
12	Logic Ground	-	-
13	+5 V	-	-
14	Logic Ground	-	-
15	Undefined	RJ1-9	RJ1-9
16	Undefined	RJ1-10	RJ1-10
17	Undefined	RJ1-11	RJ1-11
18	Undefined	RJ1-18	RJ1-18
19	Logic Ground	-	-
20	4-mHz Clock	Controller	Option

* Wired OR with RJ1-3 (Received Data)
** Wired OR with RJ1-6 (Data Set Ready)
*** Wired OR with RJ1-8 (Carrier Detect)

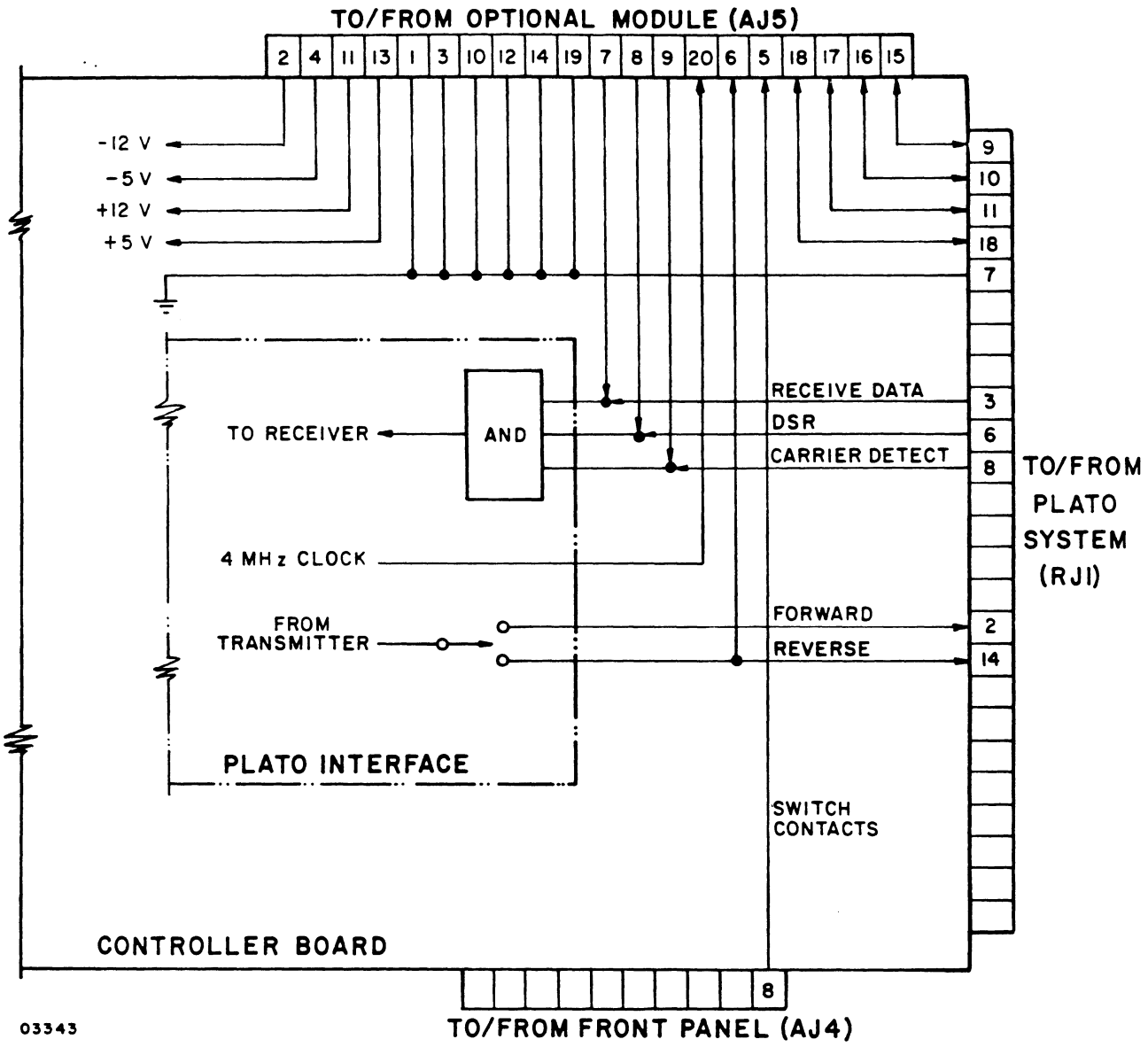


Figure 4-22. Expansion Module/PLATO Interface Signal Routing

- Transmitted Data - This signal is the output of the PLATO interface shift register. Levels are TTL compatible. The signal is a TTL high when idle (marking state). Data rates are switch selectable at 1200, 120, and 75 bps.

- Received Data - This signal carries information to the PLATO interface receiver. Voltage levels can be TTL or RS-232-C. The marking state is defined as either a TTL or RS-232-C off (V_{in} = +0.8 V). The data rate of this signal must be 1200 bps.

- Data Set Ready - This input to the PLATO interface is wired ORed with the RS-232-C DSR signal. It must be a TTL high or RS-232-C ON to enable the receiver logic.

- Carrier Detect - This input to the PLATO interface is wired ORed with the RS-232-C Carrier Detect signal. It must be a TTL high or RS-232-C ON to enable the receiver logic.

- Undefined Signals - These four signals bypass the PLATO interface logic and go directly to connector RJ1. This allows the internal optional board to have direct communications with external devices.

- 4-MHz Clock - This signal carries a symmetrical squarewave (50-percent duty cycle ±20 percent) at TTL levels.

INTERNAL MODEM

This module is a 1200-bps Receive/150-bps Transmit PCB modem and data access arrangement (DAA). The module contains a digital interface for communications with the terminal processor and an analog interface for two-wire full duplex data communications via the telephone network.

A terminal with the modem installed and connected to the telephone network has the following general capabilities:

- Asynchronous, serial, binary data

- Phase-coherent FSK modulation

- Operates full duplex with a two-wire local or long-distance unconditioned dial-up line

- Receiver data rate is 1200 bps

- Transmitter data rate selectable at 75 bps or 120 bps via switches on controller board.

OPERATORS PANEL

This panel consists of 2 PCB attached to the bezel/keyboard cover. Attached to it are: the tone generator (alarm), reset switch, six LEDs, DATA/TALK switch, and six rocker switches. The brightness control potentiometer also attaches to the bezel/keyboard cover, but is not part of the operator's panel PCB.

TOUCHPANEL

The touchpanel assembly consists of the touchpanel and connectors. The scanning and touch detection logic is part of the basic unit and is in the controller PCB.

It consists of a 16 by 16 matrix of touch-sensitive areas installed adjacent to the display surface. Pressure applied to the touchpanel/display surface interrupts the X and Y scanning mechanism. When a touch is detected, the interface logic captures the intersecting X/Y coordinates for further processing.

The touchpanel interface, as present at the internal controller board connector AJ3, consists of the signals listed in table 4-10. The 16 Y signal lines are connected to the 16 touchpanel rows (on the mylar of the touchpanel assembly). The 16 X signal lines are connected to the 16 touchpanel columns (on the glass of the touchpanel assembly). The characteristics of the touchpanel are such that if pressure is applied to a particular cell, the intersecting column signal line and row signal line are effectively shorted together. The touchpanel interface logic on the controller board operates basically as follows. The upper 4 outputs of an initially free-running 8-bit counter are fed into a 1-of-16 decoder, which then sequentially drives each column signal line to a logical low while leaving the others high. During the excitation of each column signal line, the lower 4 outputs of the counter are employed, via a 16-input multiplexer, to sequentially select each row signal line for sampling. Upon detection of a logical low row signal line, the controller logic:

1. Delays (debounces) the signal
2. Stops the counter
3. Sets the Touchpanel Data Ready status/interrupt

4. Passes the current counter outputs (X-Y coordinate) to the processor program upon request

5. Enables the counter to continue scanning after being statused by the processor.

TABLE 4-10. TOUCHPANEL CONNECTOR AJ3 (INTERNAL)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
AJ3-1	Y15	AJ3-2	X15
AJ3-3	Y14	AJ3-4	X14
AJ3-5	Y13	AJ3-6	X13
AJ3-7	Y12	AJ3-8	X12
AJ3-9	Y11	AJ3-10	X11
AJ3-11	Y10	AJ3-12	X10
AJ3-13	Y9	AJ3-14	X9
AJ3-15	Y8	AJ3-16	X8
AJ3-17	Y7	AJ3-18	X7
AJ3-19	Y6	AJ3-20	X6
AJ3-21	Y5	AJ3-22	X5
AJ3-23	Y4	AJ3-24	X4
AJ3-25	Y3	AJ3-26	X3
AJ3-27	Y2	AJ3-28	X2
AJ3-29	Y1	AJ3-30	X1
AJ3-31	Y0	AJ3-32	X0
AJ3-33	Not used	AJ3-34	Not used

POWER SUPPLY

The basic power supply is designed for 110-V ac, 50/60-Hz input power. For 220/240-V ac operation a transformer is placed between the ac entry and the basic power supply to allow for commonality of parts. Input power is applied from the ON/OFF switch on the lower right side of the terminal. The ac entry for the 110-V ac unit consists of a three-wire power card, line filter (RF filter), remote circuit breaker with auxiliary tripout (this is the ON/OFF switch), and a surge-limiting thermistor. The ac entry for the 220/240-V ac units is similar to the 110-V ac unit except for power cord plug, wiring harness, and the addition of a stepdown transformer.

The power supply converts the input ac power to five dc-regulated output voltages: +55 V, +12 V, +5 V, -5 V, and -12 V. The power supply adjustments and indicators are described as follows:

- +5-V Adjustment - This potentiometer, in the power supply, allows for the adjustment of the +5-V output of the power supply. The voltage should be measured at the PCB level when this adjustment is being made.

- +5-V Indicator - This red LED indicator, in the power supply, indicates, when lit, that the +5-V output of the power supply is energized. A voltmeter should be used to measure the actual voltage.

- +55-V Adjustment - This potentiometer, in the power supply, permits the adjustment of the +55-V output of the power supply. The voltage should be measured at the monitor PCB when this adjustment is being made.

- +55-V Indicator - This red LED indicator, in the power supply, indicates, when lit, that the 55-V output is energized. A voltmeter should be used to measure the actual voltage.

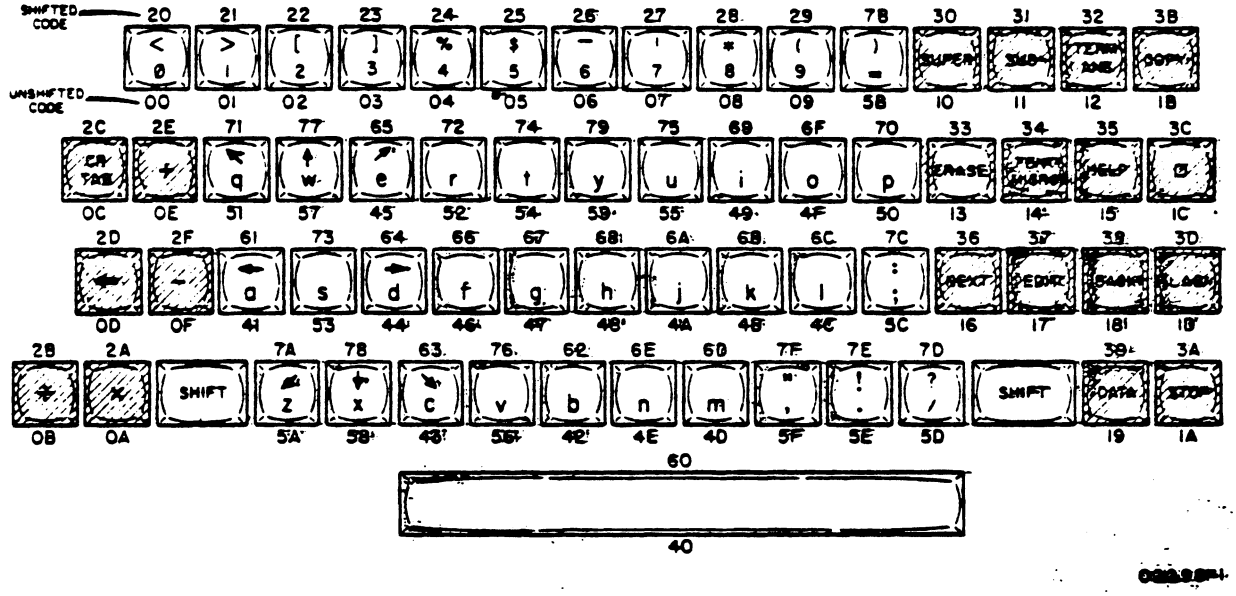
- +12-, -12-, and -5-V Indicators - These three red LED indicators, in the power supply, show the condition of the +12-, -12-, and -5-V outputs of the power supply, lit when energized, off otherwise. These outputs are not adjustable. They are supplied by solid state voltage regulators.

VIDEO MONITOR

The display is a noncomposite raster scan display that utilizes standard TTL/DTL logic level inputs. The display inputs are horizontal sync, vertical sync, and video information. DC power is provided for the display circuits. The display consists of deflection electronics, high voltage, video electronics, cathode-ray tube (crt) and necessary mechanical support components. Adjustments are provided for size, centering, focus, contrast, brightness, and linearity. All adjustments except brightness are factory set, but may be adjusted by maintenance personnel. The high frequency line scan is from left to right and the low frequency field scan is from top to bottom (facing the screen).

KEYBOARD

The terminal keyboard provides for operator entry of specific symbol and control codes. The codes generated by the keyboard are illustrated in figure 4-23. The function of the keys is not defined because every key pressed at the terminal becomes a 7-bit code, processed by the application program being executed; therefore, this code can take the form of displayable data, control commands, and/or information to be passed on to the central computer.



NOTES:

1) Each key has two different inputs. The hexadecimal number below the box is the input when a key is pressed singly, and the number above the box is the input when the SHIFT key is held down as a key is pressed. The SHIFT key alone does not initiate input data transfer, but merely causes an addition of 020 (Hex) to the normal input.

2) There are a total of 124 different inputs. Input codes of 1E, 1F, 3E, 3F are not used.

3) Shaded areas indicate difference in keycap colors.

Figure 4-23. Keyboard Codes and Legends

The keyboard interface, as presented at the internal controller board connector AJ2, consists of the signals listed in table 4-11.

TABLE 4-11. KEYBOARD CONNECTOR AJ2 (INTERNAL)

PIN NO.	SIGNAL
AJ2-1	Ground
AJ2-2	-Strobe
AJ2-3	+KBD 00
AJ2-4	01
AJ2-5	02
AJ2-6	03
AJ2-7	04
AJ2-8	+KBD 06
AJ2-9	-Shift
AJ2-10	+5 V dc

The signals +KBD XX are the outputs of a counter residing on the controller board. The keyboard decodes these 6 signed lines to select one of the 64 keys. The keyboard passes the state of the selected key back to the controller via the Strobe signal: logical high when at rest; logical low when depressed. If a particular selection (count) results in an active Strobe reply (logical low), then the controller logic

1. Delays (debounces) the signal
2. Stops the counter
3. Sets the Keyboard Data Ready status/interrupt
4. Passes the current counter outputs to the processor (program) upon request
5. Enables the counter to continue scanning after being statused by the processor.

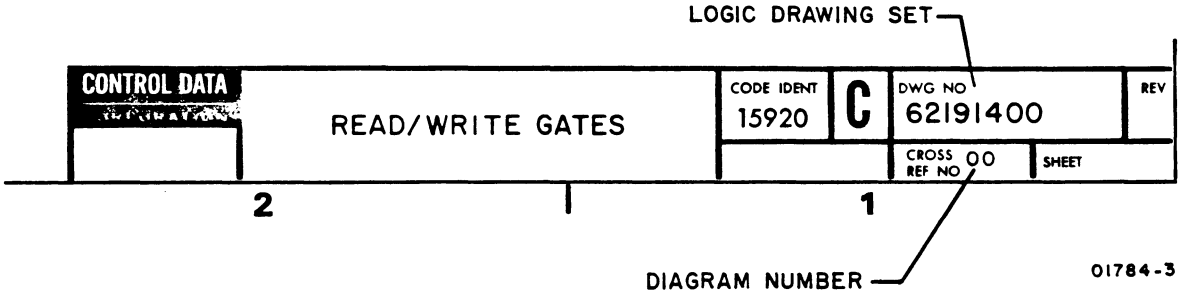
NOTE

The design/layout of the keyboard is such that the output of the counter to select a particular key is equal to the code assigned to that key. This means that the keyboard does not send the keycode to the controller, only the state of the selected key.

The SHIFT key is just a modifier to the 6-bit code generated by the counter. This key is connected directly to the interface and passed to the processor as a seventh bit.

Section 5 contains logic diagrams for the terminal. Information on how to interpret the logic diagrams precedes, and is part of, the logic diagram set. Information on the operation of individual logic chips may be found in the Key to Logic Symbology for Terminal Equipment Manual (see preface).

The title block of each logic diagram contains the following information:



In the diagrams that follow, the logic drawing set number refers to the entire set of diagrams while the diagram cross-reference number identifies the specific diagram. The cross-reference number is the only reference term that can appear on the inputs and outputs of the circuitry to indicate that the source or destination of the signal is found internally on another diagram of this logic set. Lack of a cross-reference number on an input or an output line indicates that this line comes from or goes to an external location (one that is not part of this logic set).

SHEET NO	CROSS REFERENCE NUMBER	MODULE LOCATION	REV	LOGIC DIAGRAM TITLE
1			A	LOGIC DIAGRAM SET CONTENTS SHEET
1A			A	LOGIC DIAGRAM SET CONTENTS SHEET (CONTINUED)
2			A	KEY TO DIAGRAMS-PHYSICAL LOCATION CODES
3			A	KEY TO SYMBOLS
4	000		A	CABLING AND INTERCONNECTION DIAGRAM
5	001		A	SCHEMATIC DIAGRAM 8A6D POWER SUPPLY 1
6	002		A	SCHEMATIC DIAGRAM 8A6D POWER SUPPLY 2
7	003		A	VIDEO CONTROLLER (7BGD) EXTERNAL CONNECTIONS
8	004		A	SCHEMATIC, DISPLAY LOGIC CABLE
9	005		A	DISPLAY SCHEMATIC
10	006		A	CONTROLLER MODULE (7BFD) EXTERNAL CONNECTIONS
11			A	VIDEO, CONTROLLER (7BGD) BLOCK DIAGRAM
12			A	CONTROLLER MODULE (7BFD) BLOCK DIAGRAM
13	100		A	OSCILLATOR,CPU INTERFACE
14	101		A	DOT TIMING CHAIN
15	102		A	VERTICAL TIMING
16	103		A	HORIZONTAL TIMING, MEMORY WINDOW TIMING
17	104		A	MEMORY WINDOW TIMING
18	105		A	VIDEO SHIFT REGTR,MUX,DISPLAY DRIVE LOGIC
19	106		A	BULK WRITE/ERASE, VIDEO DISABLE
20	107		A	PROGRAMMED EROM,PROCESSOR MEMORY TIMING
21	108		A	DISPLAY ADDRESS REGISTER, DISPLAY MEMORY TIMING
22	109		A	DISPLAY MEMORY ADDRESS MUX
23	110		A	DISPLAY MEMORY
24	111		A	PROCESSOR MEMORY
25	112		A	MEMORY OUTPUT BUFFERS
26	113		A	DATA BUS TRANSCEIVER, COMPOSITE VIDEO
26A	114		A	VIDEO CONTROLLER MODULE (7BGD), POWER, GROUND,& DECOUPLING
27			A	VIDEO DOT TIMING,CHARACTER TIMING & MEMORY WINDOWS
28			A	LINE TIMING FIELD (50 60 HZ) TIMING
29			A	DISPLAY MEMORY TIMING
30	200		A	Z80 MICROPROCESSOR, RESET LOGIC
31	201		A	uP SIGNAL BUFFERS
32	202		A	INPUT MUX
33	203		A	I/O CONTROL
34	204		A	I/O CONTROL, OP PANEL LED RGTR AND DRVRS
35	205		A	FEATURE SELECT SWITCHES, IO CODE SHUNTS

NOTES
1. FOR LOGIC CHIP INFORMATION SEE DWG. 82297000 (KEY TO SYMBOLS).

REVISION RECORD

REV	CO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	156533	RELEASED CLASS A		8-28-79		

SHEET REVISION STATUS

TITLE: LOGIC DIAGRAM SET CONTENTS SHEET

CONTROL DATA

FIRST USED ON: FC816A,FC816B

DWN	Mary Dietz	8-17-79
CHKD		
ENGR		
MFG		
APPR		

REFERENCE DRAWING

COMPONENTS EXCEPT AS NOTED: TOLERANCE, VALUE, RATING; RES, CAP

CODE IDENT 15920 | SCALE | DRAWING NO C 62201041 | CROSS REF NO | SHEET 1 OF 52

SHEET NO	CROSS REFERENCE NUMBER	REV	LOGIC DIAGRAM TITLE
36	206	A	KEYBOARD SCANNER AND CONTACT DETECTION LOGIC, INTERRUPT MASK RGTR AND ENCODER
37	207	A	PLATO XMT SHIFT REGISTER, SERIAL BAUD RATE GENERATION, INTERVAL TIMES
38	208	A	PLATO COMMUNICATIONS CONTROL
39	209	-	LONG LINE RECEIVER, RS232 DRIVERS AND RECEIVERS
40	210	-	PLATO RECEIVER LOGIC
41	211	A	SERIAL BAUD RATE MUX, TOUCHPANEL CONTACT DETECT
42	212	A	SERIAL CHANNEL UART, LONG LINE DRIVER
42A	212A	-	TOUCH PANEL LOGIC X SCANNER
43	213	A	TOUGH PANEL LOGIC Y-SCANNER
43A	214	-	CONTROLLER MODULE (7BFD); POWER, GROUND, AND DECOUPLING
44		-	PROCESSOR MEMORY CYCLES
45		-	PLATO RECEIVER TIMING
46		-	PLATO TRANSMITTER TIMING
47	300	-	OPERATOR'S PANEL (7BYD)
48	400	-	KEYBOARD
49	500	-	LOGIC DIAGRAM, TOUCH PANEL (OPTIONAL)
50	600	-	MODEM OPTION, TRANSMITTER AND DAA
51	601	-	MODEM OPTION, RECEIVER
52	602	-	MODEM OPTION; POWER, GROUND, AND DECOUPLING

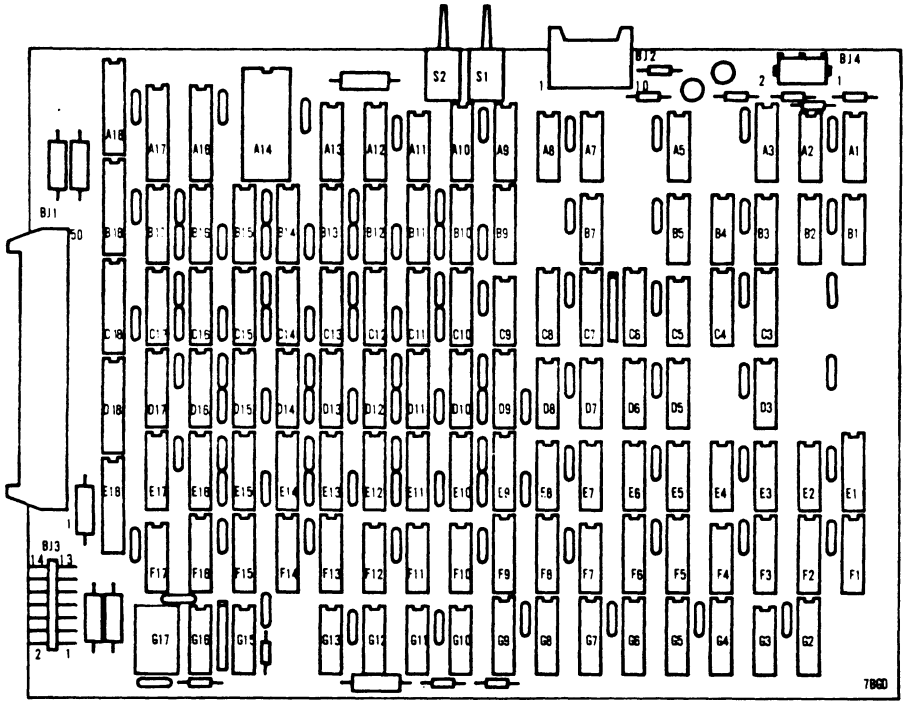
SHEET NO.	CROSS REFERENCE NUMBER	REV	LOGIC DIAGRAM TITLE

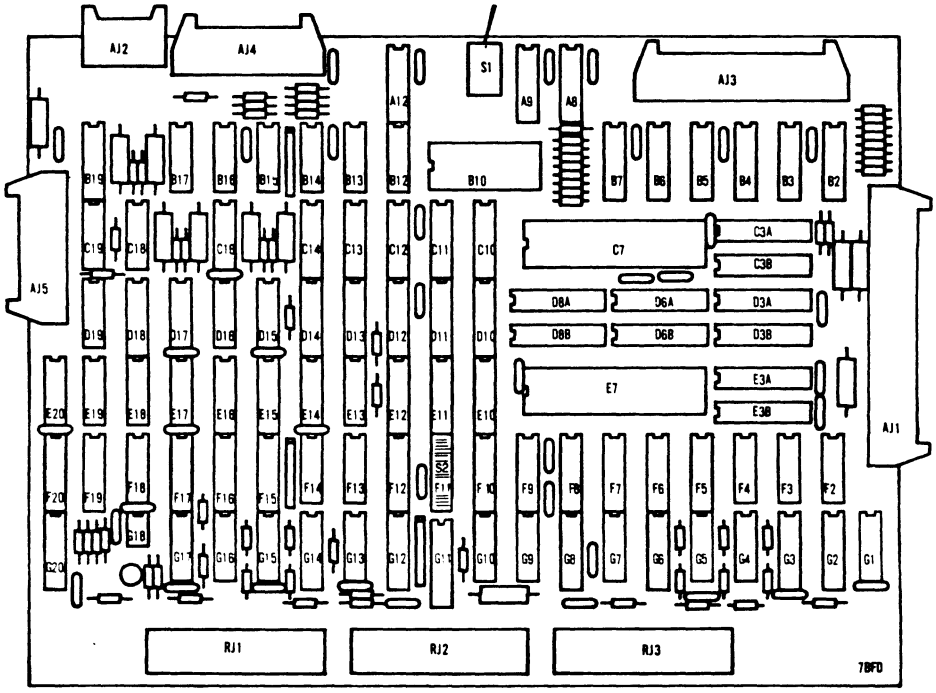
CONTROL DATA

LOGIC DIAGRAM
CONTENTS SHEET (CONTINUED)

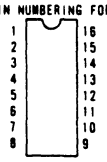
CODE IDENT 15920 | C | DWG NO 62201041 | REV A

CROSS REF NO | SHEET 1A





TYPICAL PIN
PIN NUMBERING FOR IC



PHYSICAL LOCATION CODES

CIRCUIT MODULE LAYOUT THESE DRAWINGS DEPICT THE COMPONENT SIDE ASSEMBLY OF THE TWO LOGIC MODULES DIAGRAMMED IN THIS LOGIC SET THE ALPHANUMERIC CODES AR THE BOTTOM OF THE SYMBOLS ARE THE PHYSICAL LOCATION CODES THESE NUMBERS CORRESPOND TO THOSE SHOWN INSIDE THE LOGIC SYMBOL OUTLINES ON THE DIAGRAM SHEETS.

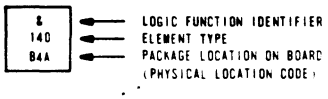
KEY TO DIAGRAMS
PHYSICAL LOCATION CODES

CODE IDENT 15920
DWG NO 62201041
REV K
SHEET 2
CROSS REF NO

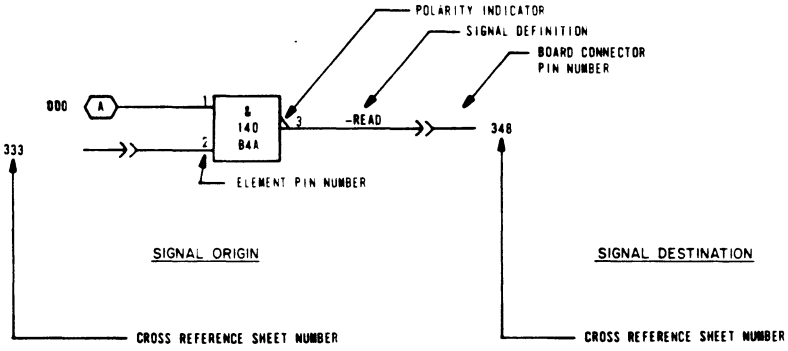
LOC
CROSS REF NO

GENERAL LOGIC SYMBOL INFORMATION

INTEGRATED CIRCUIT LOGIC SYMBOL



TAGGING INFORMATION



GENERAL P.C. BOARD INFORMATION

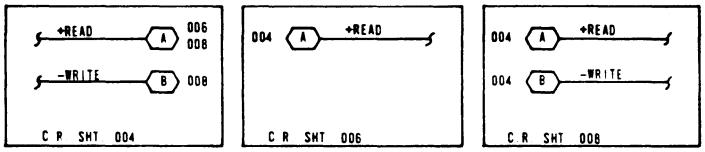
EACH PRINTED CIRCUIT BOARD UNDER IDEAL CONDITIONS WOULD BE REPRESENTED ON ONE SHEET HOWEVER, DUE TO THE LARGE NUMBER OF CIRCUITS LOCATED ON SOME BOARDS, MULTIPLE SHEETS MAY BE REQUIRED. THE BOARD TYPE IS LISTED AT THE BOTTOM OF EACH DIAGRAM SHEET. THE BOARD LOCATION WITHIN THE LOGIC CHASSIS MAY ALSO ACCOMPANY THE BOARD TYPE. EACH SYMBOL ON THE DIAGRAM REPRESENTS A PORTION OF AN INTEGRATED CIRCUIT, THE ENTIRE INTEGRATED CIRCUIT OR A DISCRETE COMPONENT. EACH SYMBOL REFLECTS THE LOGIC FUNCTION IDENTIFIER, ELEMENT OR COMPONENT TYPE, AND THE ELEMENT OR COMPONENT LOCATION ON THE BOARD. COMPONENT LOCATION IS DEFINED BY AN ALPHANUMERIC MATRIX DEPENDING ON THE TYPE OF PRINTED CIRCUIT BOARD USED. FOR INFORMATION ON THE COMPONENT OR ELEMENT TYPES USED IN THIS LOGIC SET, REFER TO KEY TO LOGIC SYMBOLOGY MANUAL, CDC PUBLICATION NUMBER 82172400

QUALIFYING SYMBOLS

& = AND
1 = OR
1 = INVERTER
X→Y = X(INPUTS) DECODED OR ENCODED TO Y(OUTPUTS)
X/Y = X(INPUT LEVEL) CONVERTED TO Y(OUTPUT LEVEL)

ON BOARD, OFF SHEET TAGGING

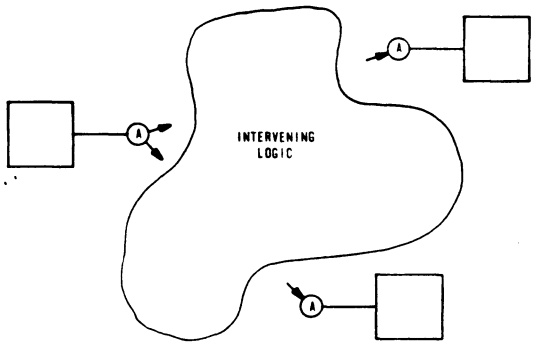
IN A LOGIC DIAGRAM SET HAVING MORE THAN ONE SHEET, A HEXAGON IS USED TO INDICATE THAT THE SIGNAL IS COMING FROM, OR GOING TO, ANOTHER SHEET OF THE SAME BOARD. (NOTE: EACH SIGNAL NAME IN THIS LOGIC SET HAS BEEN PRECEDED BY A "+" (INDICATING AN ACTIVE HI) OR A "-" (INDICATING AN ACTIVE LO))



NON-STANDARD ABBREVIATIONS

ON SHEET TAGGING

THE SMALL CIRCLES WITH ALPHA CHARACTERS INSIDE ARE USED TO SHOW A SIGNAL PATH WITHOUT ACTUALLY RUNNING A LINE FROM ONE POINT TO ANOTHER. A CIRCLE WITH AN ARROW POINTING AWAY FROM IT IS THE SIGNAL ORIGIN. IN DIRECT LINE WITH THE ORIGIN ARROW, ANOTHER CIRCLE IS DRAWN WITH AN ARROW POINTING TOWARD IT. THIS IS THE SIGNAL DESTINATION



VOLTAGE LEVELS

1. ANALOG OR NON-LOGIC LEVELS

2. NON-STANDARD LOGIC LEVEL

3. LOGIC LEVELS

DTL LOGIC OPERATION

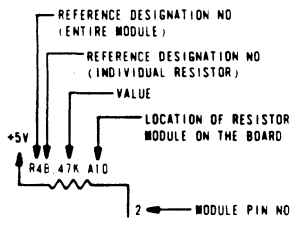
HIGH (LOGICAL 1) = +2.6 TO +5.0 VOLTS
LOW (LOGICAL 0) = 0.0 TO +0.45 VOLTS
SWITCHING POINT = +1.1 TO +1.9 VOLTS

TTL LOGIC OPERATION

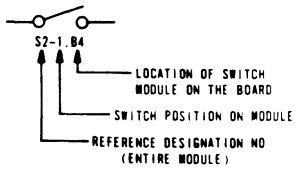
HIGH (LOGICAL 1) = +2.8 TO +5.0 VOLTS
LOW (LOGICAL 0) = 0.0V TO +0.45 VOLTS
SWITCHING POINT = +.85V TO +1.9 VOLTS

MISCELLANEOUS INDICATORS

RESISTOR MODULES

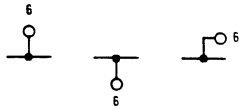


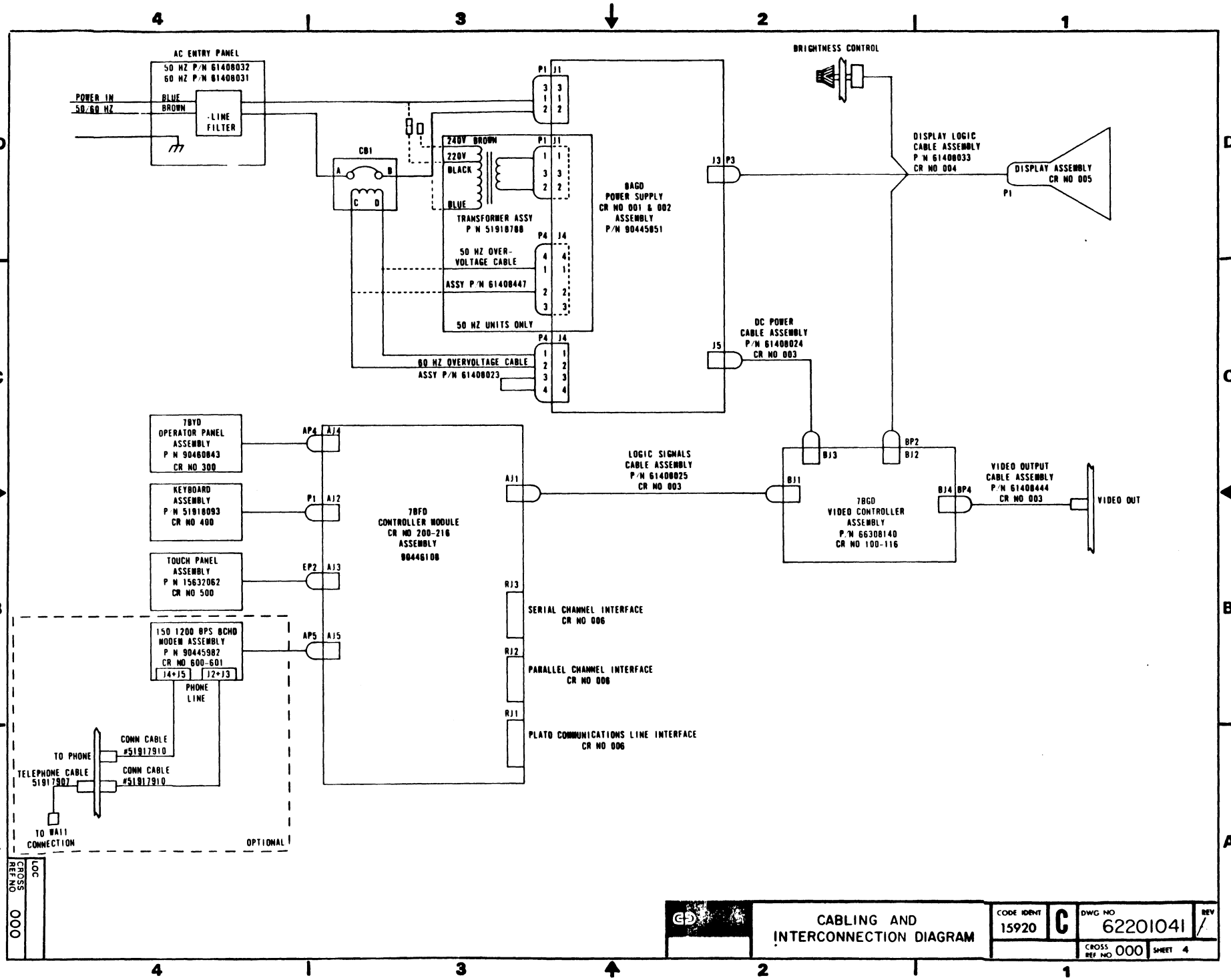
SWITCH MODULES



TEST POINTS

THE CLASS DESIGNATION LETTERS "TP" HAVE NOT BEEN SHOWN ON THIS LOGIC SET. THEREFORE, THE TEST POINTS APPEAR AS FOLLOWS





CROSS REF NO 000 LOC

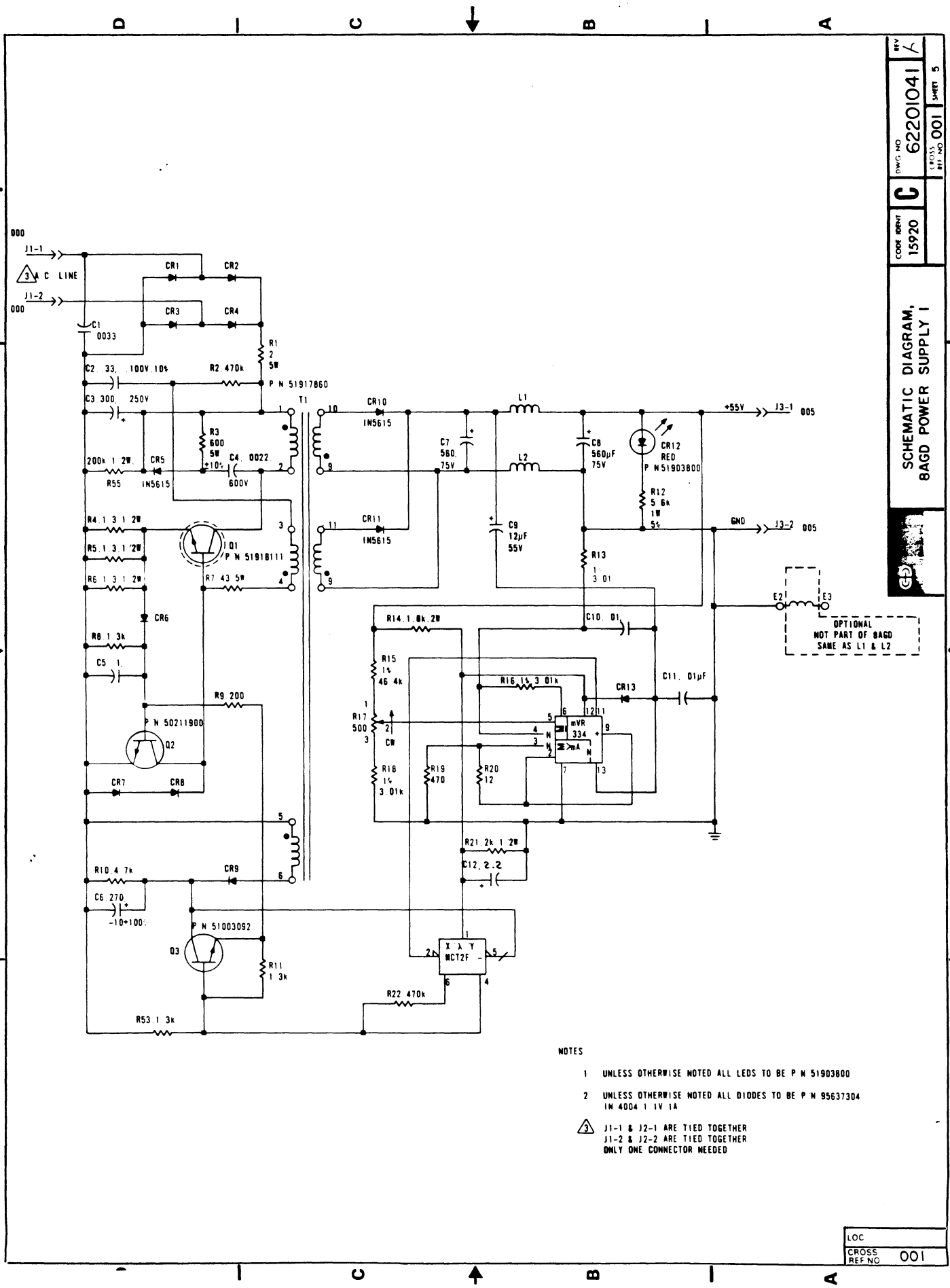
CABLING AND INTERCONNECTION DIAGRAM

CODE IDENT 15920 | C | DWG NO 62201041 | REV /

CROSS REF NO 000 | SHEET 4

5-6

82100083



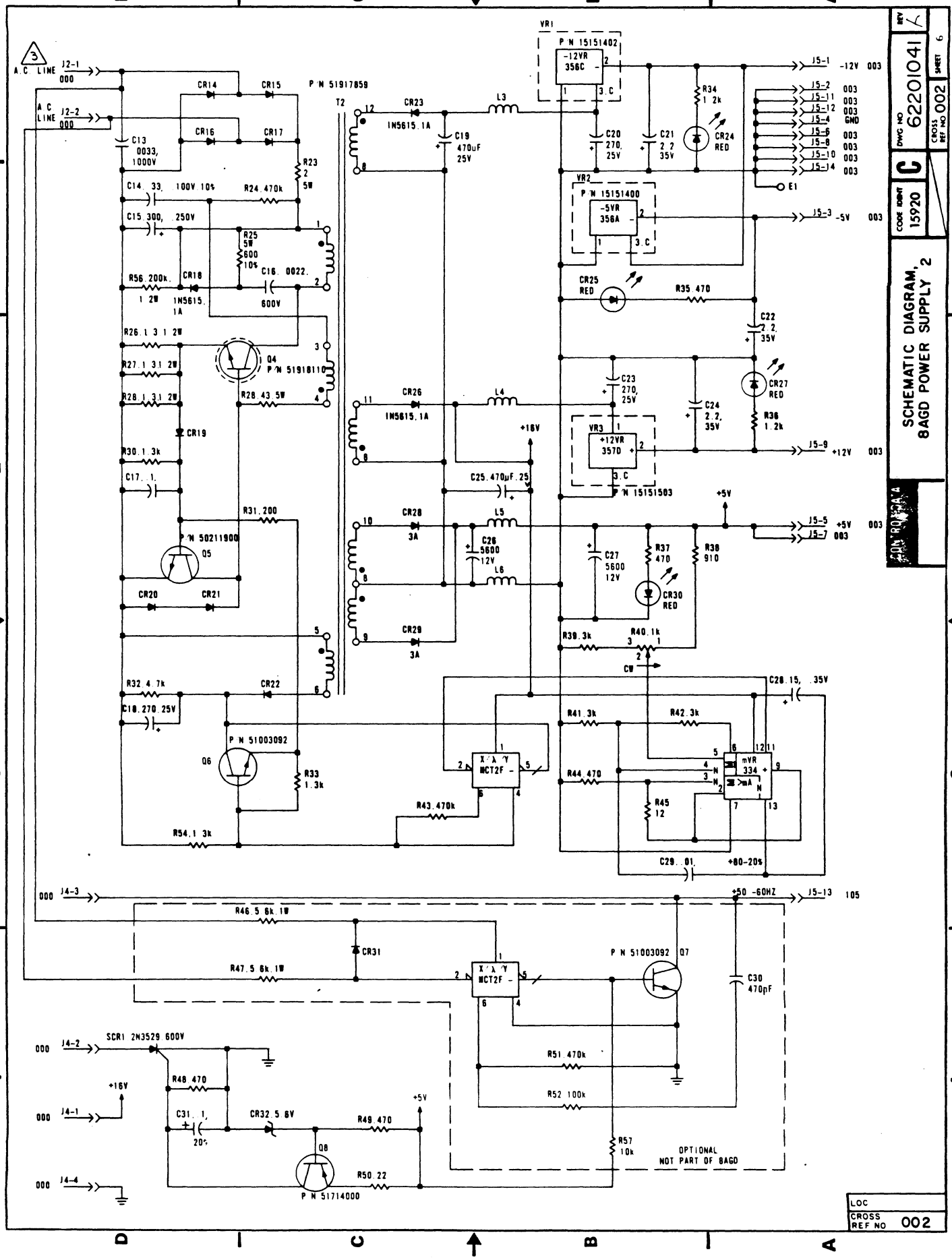
NOTES

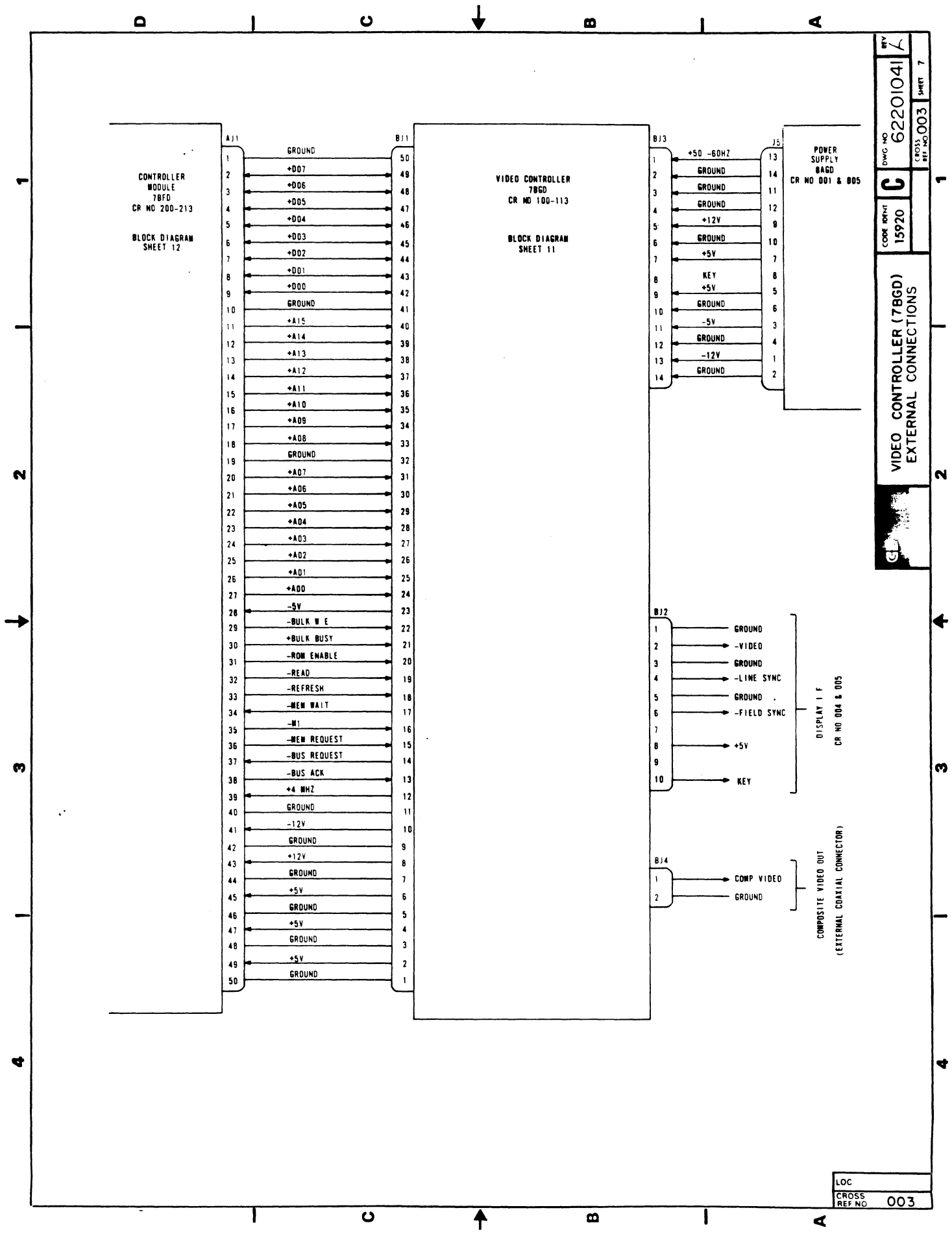
1 UNLESS OTHERWISE NOTED ALL LEDS TO BE P N 51903800

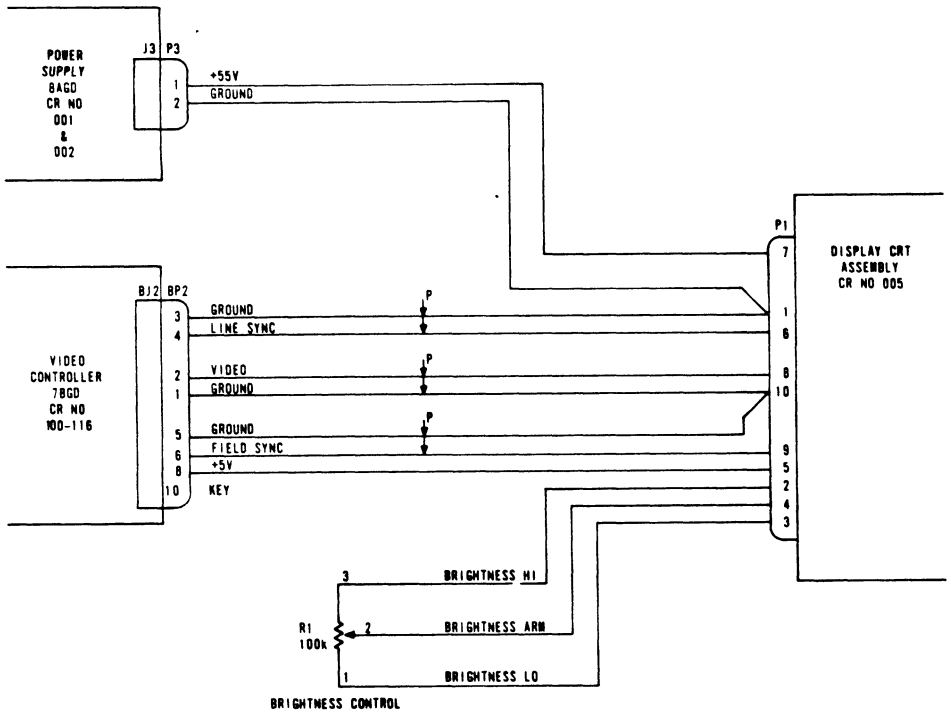
2 UNLESS OTHERWISE NOTED ALL DIODES TO BE P N 95637304 IN 4004 1 1V 1A

3 J1-1 & J2-1 ARE TIED TOGETHER
J1-2 & J2-2 ARE TIED TOGETHER
ONLY ONE CONNECTOR NEEDED

LOC
CROSS REF NO 001


SCHEMATIC DIAGRAM, 8AGD POWER SUPPLY 2
DWG NO 62201041
REV J
SHEET 6
CROSS REF NO 002
CODE IDENT 15920
C
A.C. LINE
J2-1
J2-2
000
CR14
CR15
CR16
CR17
P/N 51917859
T2
C13 .0033, 1000V
R23 2 5W
C14 .33, 100V 10%
R24 470k
C15 300, 250V
R25 5W 600 10%
C16 .0022, 600V
R56 200k 1 2W
CR18 1N5615, 1A
R26 1 3 1 2W
R27 1 3 1 2W
R28 1 3 1 2W
Q4 P/N 51918110
R28 43 5W
CR19
R30 1 3k
C17 .1
R31 200
P/N 50211900
Q5
CR20
CR21
R32 4 7k
CR22
C18 270 25V
P/N 51003092
Q6
R33 1 3k
R54 1 3k
R43 470k
X/λ/Y MCT2F
VR1
P/N 15151402
-12VR 356C
3.C
VR2
P/N 15151400
-5VR 356A
VR3
+12VR 357D
P/N 15151503
CR23 1N5615, 1A
L3
C19 470uF 25V
C20 270, 25V
C21 2 2 35V
R34 1 2k
CR24 RED
E1
CR25 RED
R35 470
C22 2 2, 35V
CR26 1N5615, 1A
L4
C23 270, 25V
C24 2 2, 35V
CR27 RED
R36 1 2k
+16V
C25 470µF 25
CR28 3A
L5
C26 5600 12V
L6
CR29 3A
C27 5600 12V
R37 470
R38 910
CR30 RED
+5V
R39 3k
R40 1k
CW
C28 15, 35V
R41 3k
R42 3k
R44 470
R45 12
mVR 334
>mA
C29 .01 +80-20%
J5-1 -12V 003
J5-2 003
J5-11 003
J5-12 003
J5-4 GND
J5-6 003
J5-8 003
J5-10 003
J5-14 003
J5-3 -5V 003
J5-9 +12V 003
J5-5 +5V 003
J5-7 003
J4-3
+50 -60HZ
J5-13 105
R46 5 6k 1W
CR31
R47 5 6k 1W
P/N 51003092 Q7
C30 470pF
J4-2
SCR1 2N3529 600V
R48 470
J4-1
C31 .1, 20%
CR32 5 6V
R49 470
Q8
P/N 51714000
R50 22
R51 470k
R52 100k
R57 10k
OPTIONAL NOT PART OF 8AGD
J4-4
LOC
CROSS REF NO 002


CONTROLLER MODULE 78FD CR NO 200-213
BLOCK DIAGRAM SHEET 12
AJ1
BJ1
GROUND
+D07
+D06
+D05
+D04
+D03
+D02
+D01
+D00
GROUND
+A15
+A14
+A13
+A12
+A11
+A10
+A09
+A08
GROUND
+A07
+A06
+A05
+A04
+A03
+A02
+A01
+A00
-5V
-BULK W E
+BULK BUSY
-ROM ENABLE
-READ
-REFRESH
-MEM WAIT
-M1
-MEM REQUEST
-BUS REQUEST
-BUS ACK
+4 MHZ
GROUND
-12V
GROUND
+12V
GROUND
+5V
GROUND
+5V
GROUND
+5V
GROUND
VIDEO CONTROLLER 78GD CR NO 100-113
BLOCK DIAGRAM SHEET 11
BJ3
J5
+50 -60HZ
GROUND
GROUND
GROUND
+12V
GROUND
+5V
KEY
+5V
GROUND
-5V
GROUND
-12V
GROUND
POWER SUPPLY 8AGD CR NO 001 & 005
BJ2
GROUND
-VIDEO
GROUND
-LINE SYNC
GROUND
-FIELD SYNC
+5V
KEY
DISPLAY I F CR NO 004 & 005
BJ4
COMP VIDEO
GROUND
COMPOSITE VIDEO OUT (EXTERNAL COAXIAL CONNECTOR)
VIDEO CONTROLLER (78GD) EXTERNAL CONNECTIONS
CODE IDENT 15920
DWG NO 62201041
REV
SHEET 7
CROSS REF NO 003
LOC
CROSS REF NO 003



CABLE ASSEMBLY PART NO 61400833

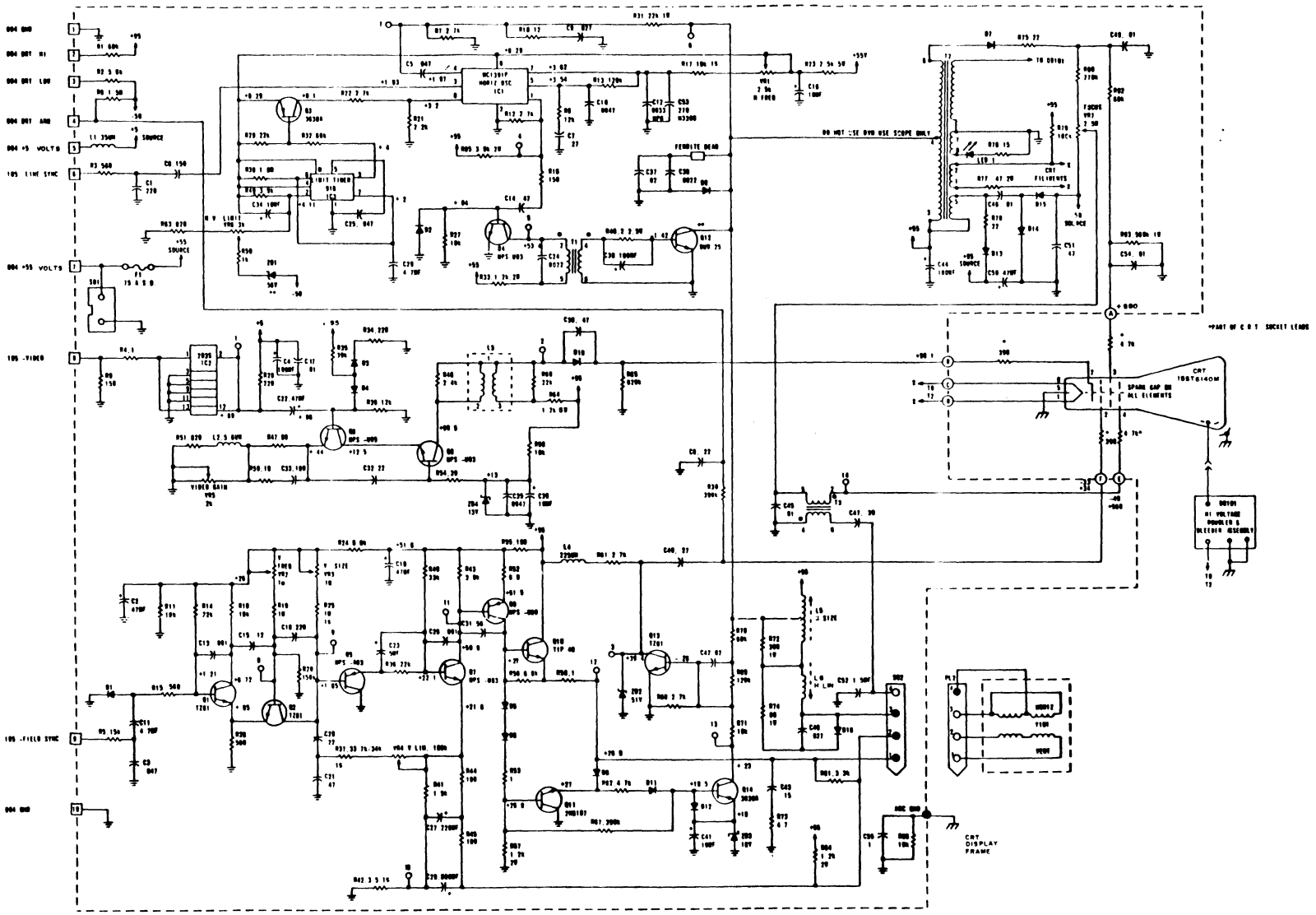
SCHEMATIC, DISPLAY LOGIC CABLE

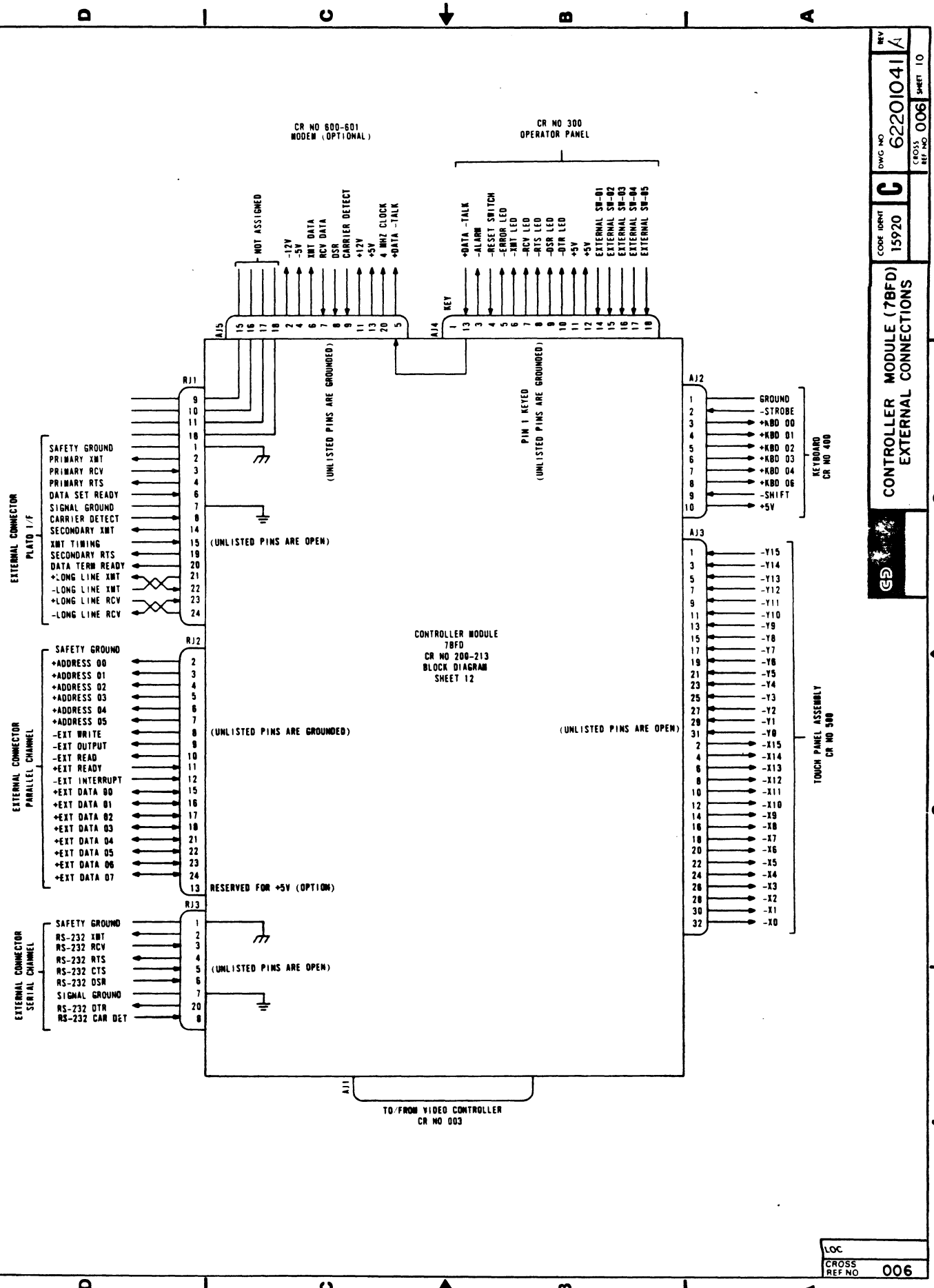
CODE IDENT 15920 | C | DWG NO 62201041 | REV /

CROSS REF NO 004 | SHEET 8

LOC

CROSS REF NO 004

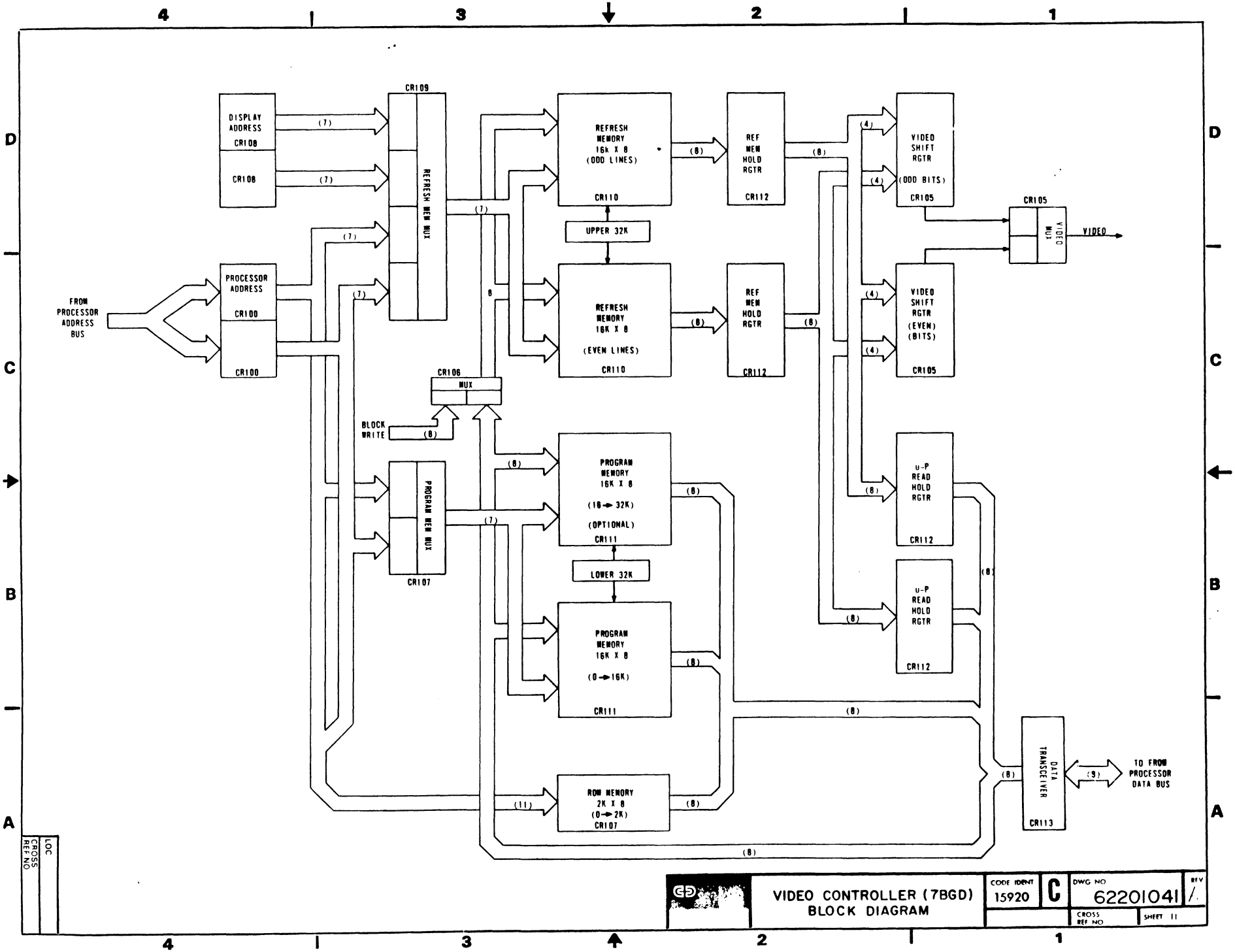

DISPLAY SCHEMATIC
CODE IDENT 15920
C
DWG NO 62201041
REV A
CROSS REF NO 005
SHEET 9
LOC CROSS REF NO 005

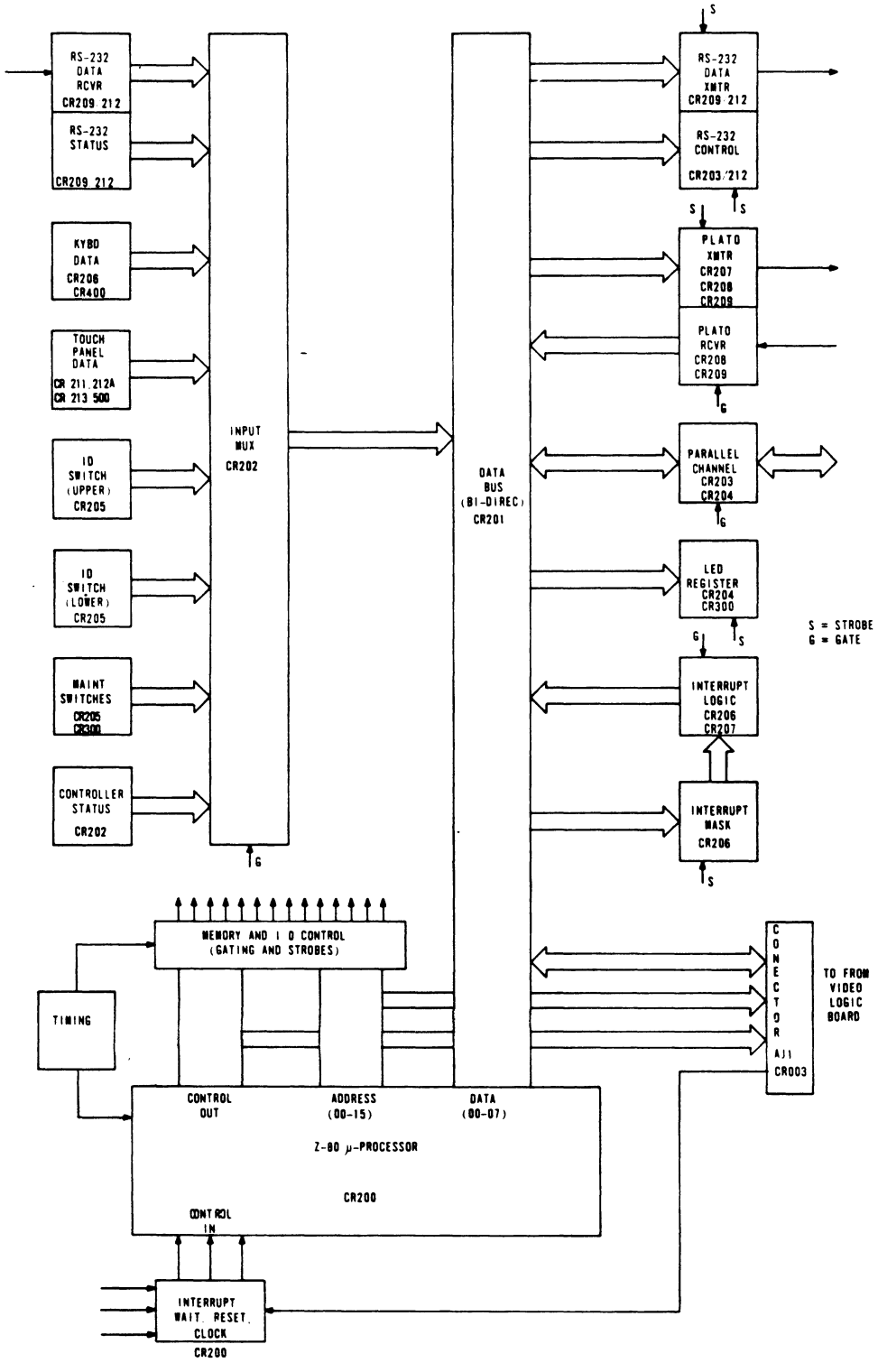


CONTROLLER MODULE (78FD)
EXTERNAL CONNECTIONS

CODE IDENT 15920 | DWG NO 62201041 | REV A | SHEET 10 | CROSS REF NO 006

LOC
CROSS REF NO 006

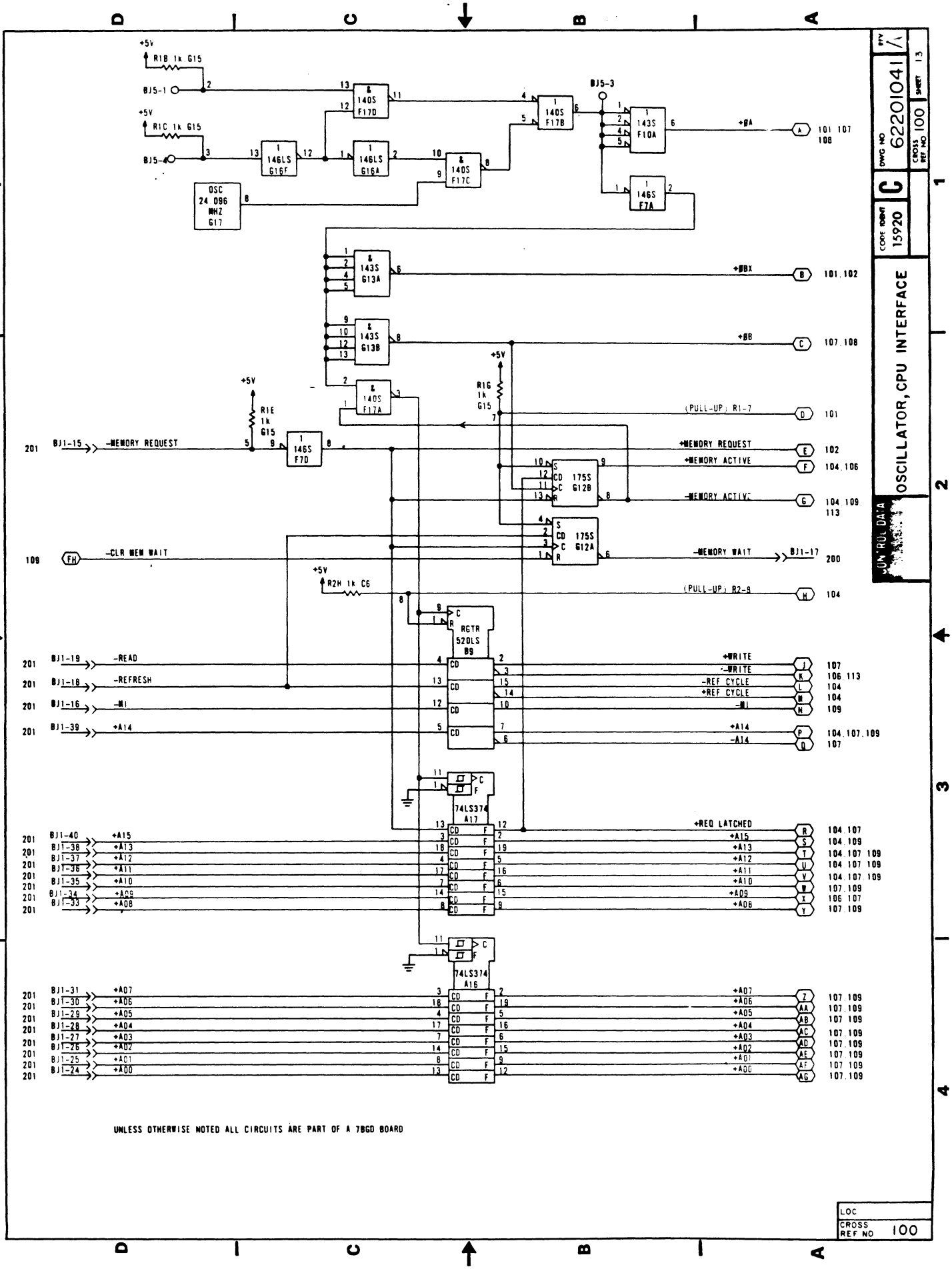

DISPLAY ADDRESS
CR108
CR108
PROCESSOR ADDRESS
CR100
CR100
FROM PROCESSOR ADDRESS BUS
CR109
REFRESH MEM MUX
REFRESH MEMORY 16k X 8 (ODD LINES)
CR110
REFRESH MEMORY 16K X 8 (EVEN LINES)
CR110
UPPER 32K
REF MEM HOLD RGTR
CR112
REF MEM HOLD RGTR
CR112
VIDEO SHIFT RGTR (ODD BITS)
CR105
VIDEO SHIFT RGTR (EVEN) (BITS)
CR105
CR105
VIDEO MUX
VIDEO
CR106
MUX
BLOCK WRITE
PROGRAM MEM MUX
CR107
PROGRAM MEMORY 16K X 8 (16→32K) (OPTIONAL)
CR111
LOWER 32K
PROGRAM MEMORY 16K X 8 (0→16K)
CR111
u-P READ HOLD RGTR
CR112
u-P READ HOLD RGTR
CR112
ROM MEMORY 2K X 8 (0→2K)
CR107
DATA TRANSCEIVER
CR113
TO FROM PROCESSOR DATA BUS
LOC
CROSS REF NO
VIDEO CONTROLLER (7BGD) BLOCK DIAGRAM
CODE IDENT 15920
C
DWG NO 62201041
REV /.
CROSS REF NO
SHEET 11

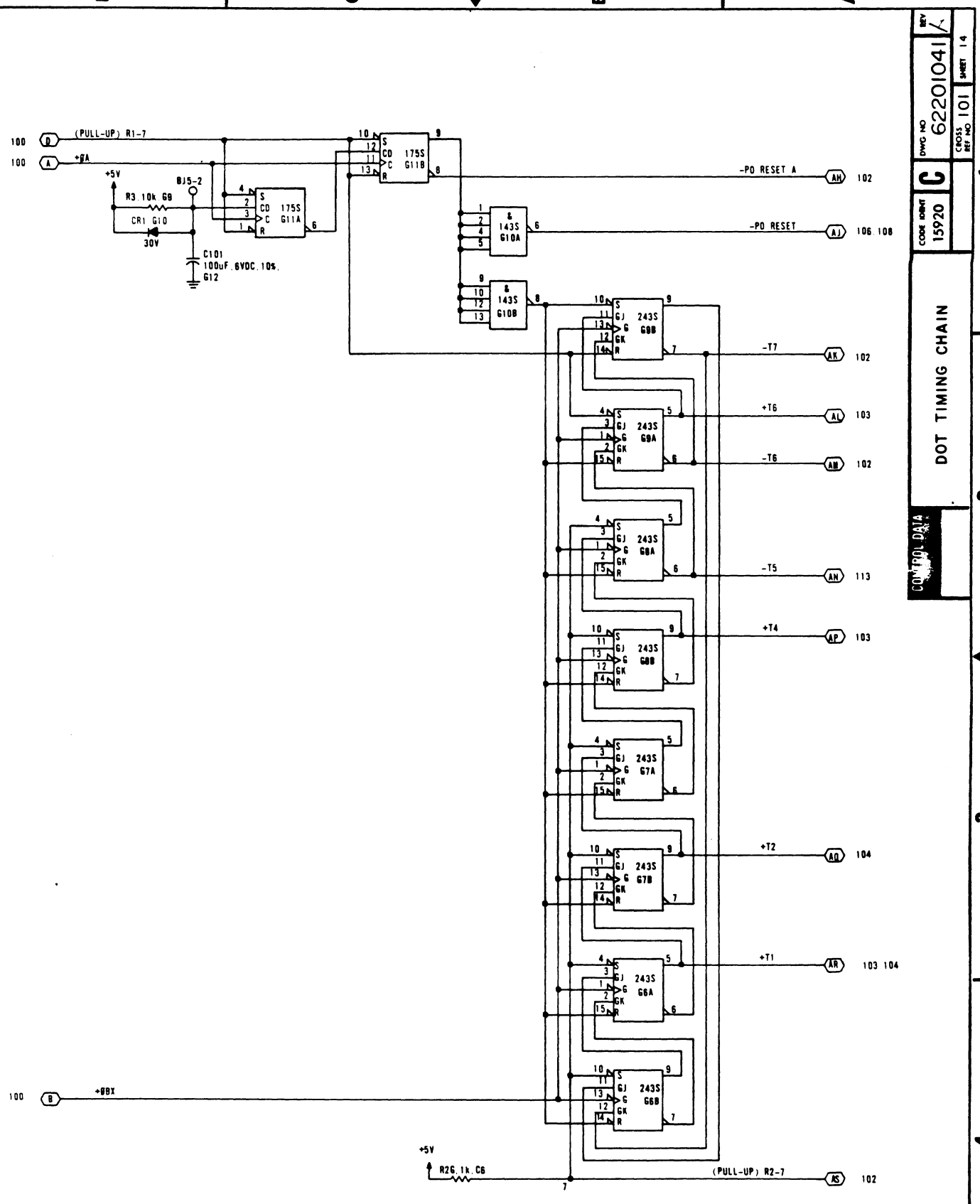


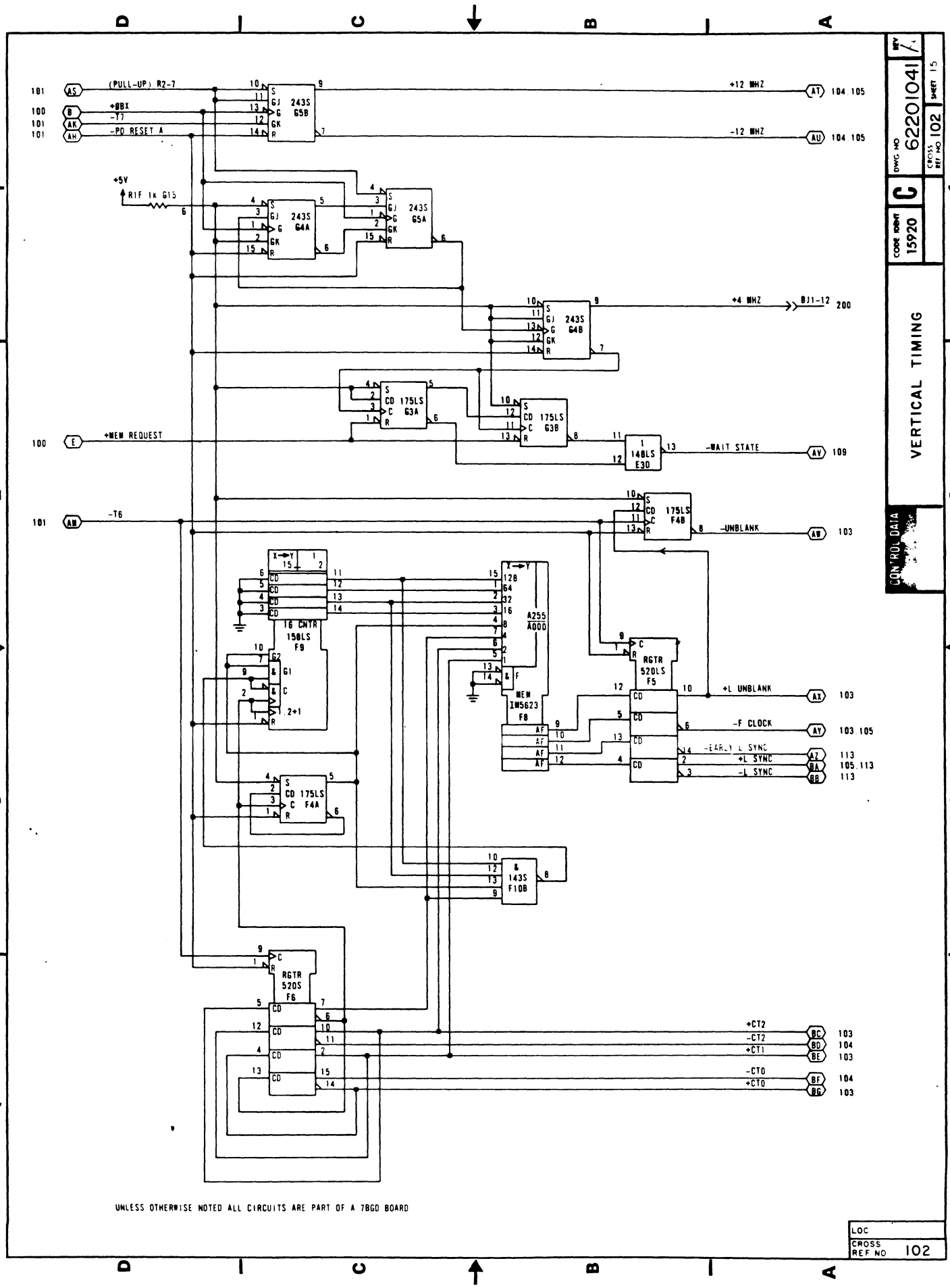
CONTROLLER MODULE (7BFD) BLOCK DIAGRAM

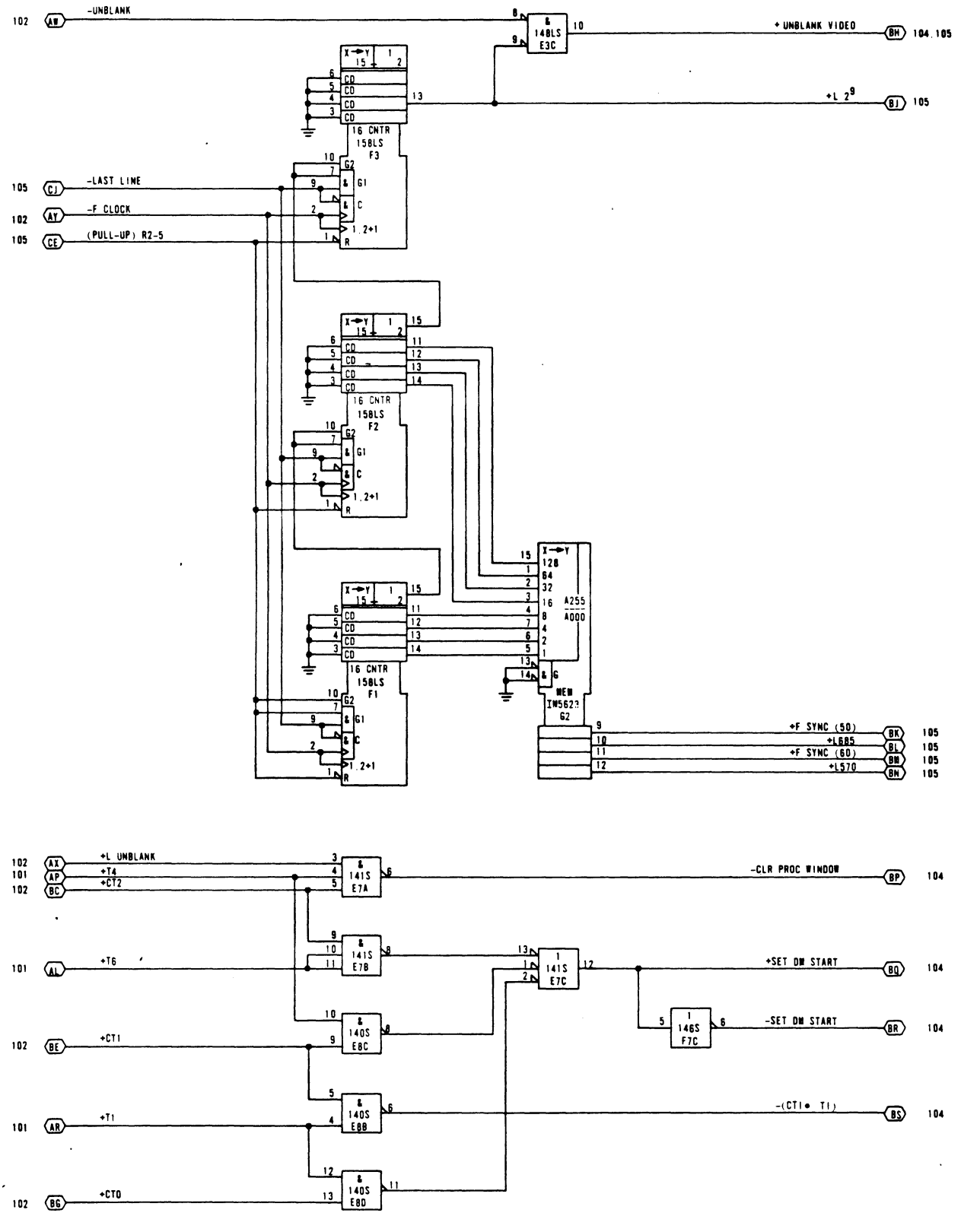
DWG NO 6220104 | REV A | SHEET 12 | CODE IDENT 15920 | C | CROSS REF NO

LOC | CROSS REF NO


OSCILLATOR, CPU INTERFACE
DWG NO 6220104
REV A
SHEET 13
CROSS REF NO 100
CODE IDENT 15920
SIZE C
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78GD BOARD
LOC
CROSS REF NO 100


DOT TIMING CHAIN
CONTROL DATA
DWG NO 6220104
REV C
CODE IDENT 15920
CROSS REF NO 101
SHEET 14
(PULL-UP) R1-7
+9A
+5V
BJ5-2
R3 10k G9
CR1 G10
30V
C101
100uF 6VDC 10%
G12
175S G11A
175S G11B
143S G10A
143S G10B
-PO RESET A
-PO RESET
-T7
+T6
-T6
-T5
+T4
+T2
+T1
243S G9B
243S G9A
243S G8A
243S G8B
243S G7A
243S G7B
243S G6A
243S G6B
+9BX
R26 1k C6
(PULL-UP) R2-7
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78GD BOARD
LOC
CROSS REF NO 101


VERTICAL TIMING
CONTROL DATA
DWG NO 6220104
REV
SHEET 15
CROSS REF NO 102
CODE IDENT 15920
(PULL-UP) R2-7
+BBX
-T7
-PD RESET A
+5V
R1F 1K G13
+12 MHZ
-12 MHZ
+4 MHZ
+MEM REQUEST
-WAIT STATE
-T6
-UNBLANK
+L UNBLANK
-F CLOCK
-EARLY L SYNC
+L SYNC
-L SYNC
+CT2
-CT2
+CT1
-CT0
+CT0
16 CNTR 158LS F9
MEM IM5623 F8
RGTR 520LS F5
RGTR 520S F6
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BGD BOARD
LOC
CROSS REF NO 102

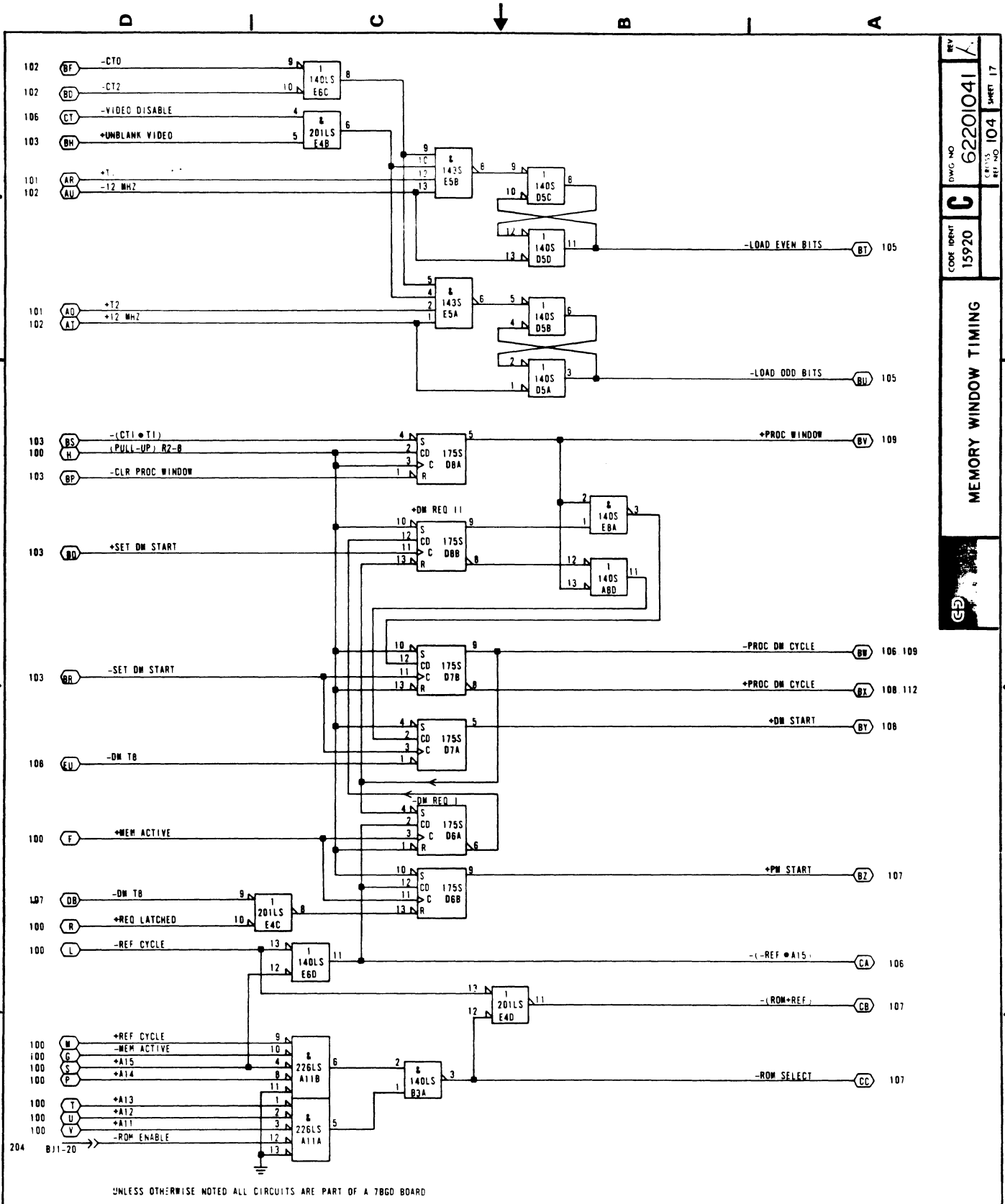


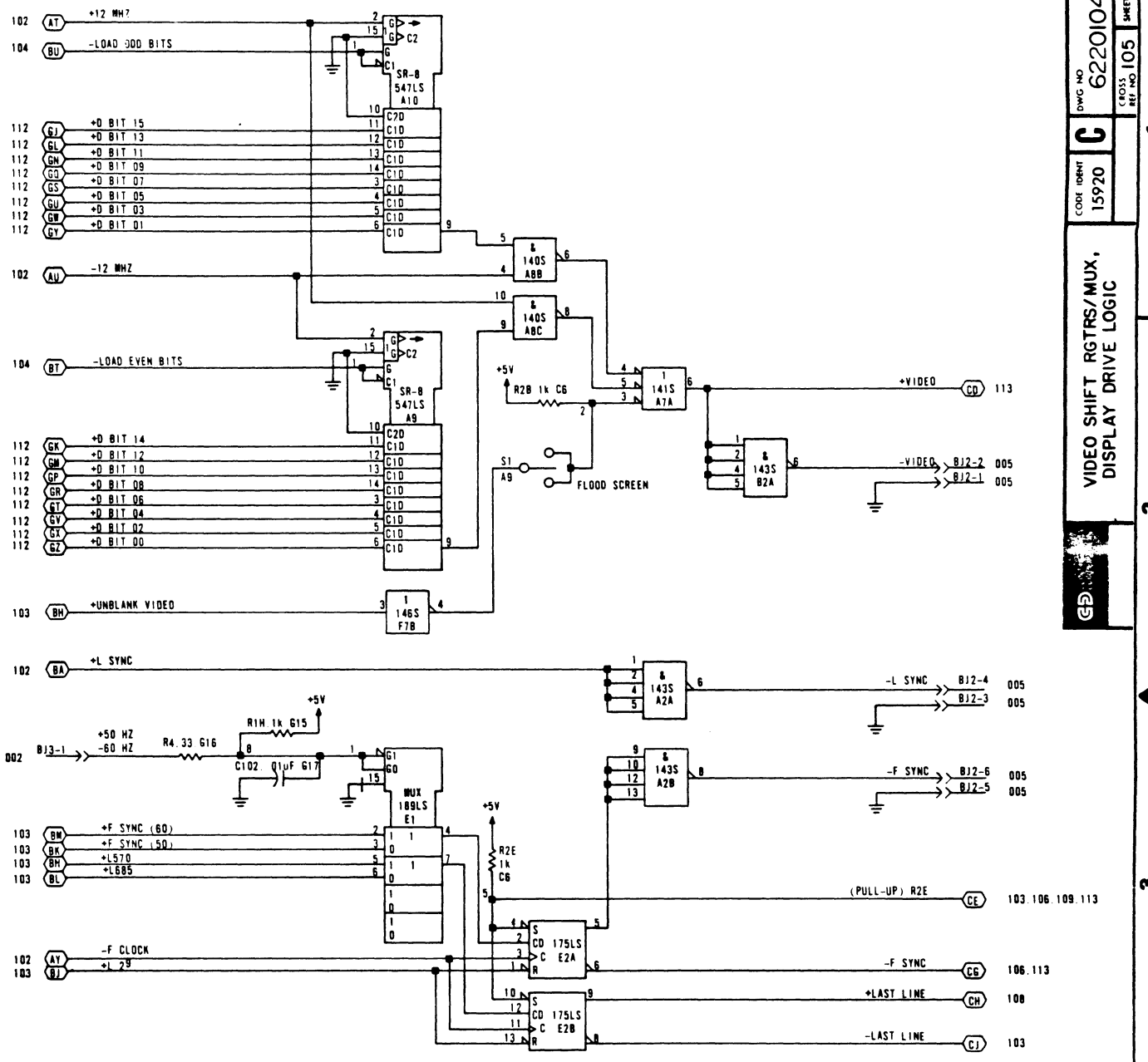
CONTROL DATA

HORIZONTAL TIMING, · MEMORY WINDOW TIMING

CODE IDENT 15920 | C | DWG NO 62201041 | REV | SHEET 16 | CROSS REF NO 103

LOC
CROSS REF NO 103


MEMORY WINDOW TIMING
DWG NO 6220104
CODE IDENT 15920
SHEET 17
CROSS REF NO 104
-CT0
-CT2
-VIDEO DISABLE
+UNBLANK VIDEO
+T1
-12 MHZ
+T2
+12 MHZ
-LOAD EVEN BITS
-LOAD ODD BITS
-(CT1 • T1)
(PULL-UP) R2-8
-CLR PROC WINDOW
+PROC WINDOW
+DM REQ 11
+SET DM START
-PROC DM CYCLE
-SET DM START
+PROC DM CYCLE
+DM START
-DM T8
-DM REQ 1
+MEM ACTIVE
+PM START
-DM T8
+REQ LATCHED
-REF CYCLE
-(-REF • A15)
-(ROM+REF)
+REF CYCLE
-MEM ACTIVE
+A15
+A14
+A13
+A12
+A11
-ROM ENABLE
-ROM SELECT
BJ1-20
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78GD BOARD
LOC
CROSS REF NO 104

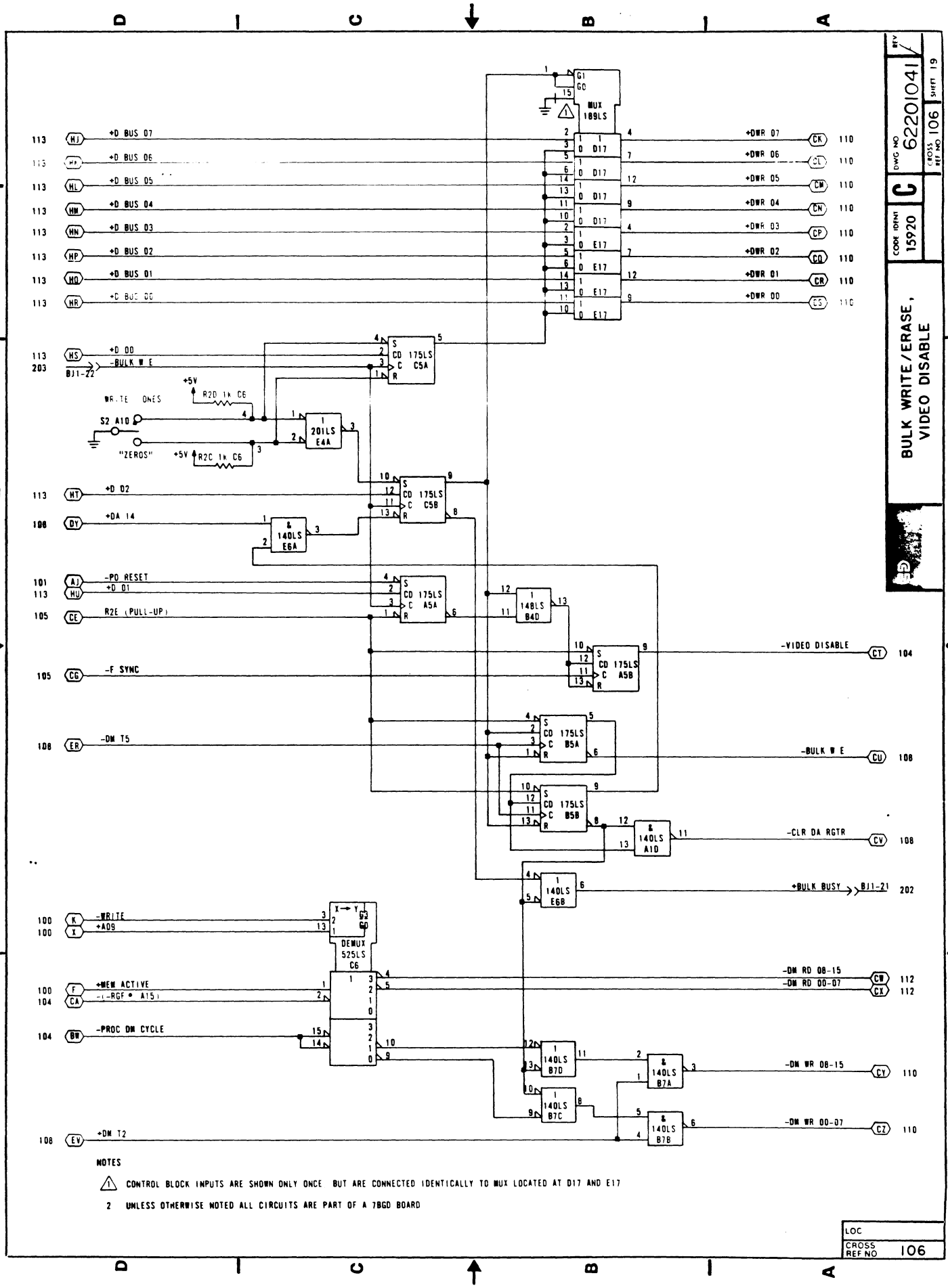


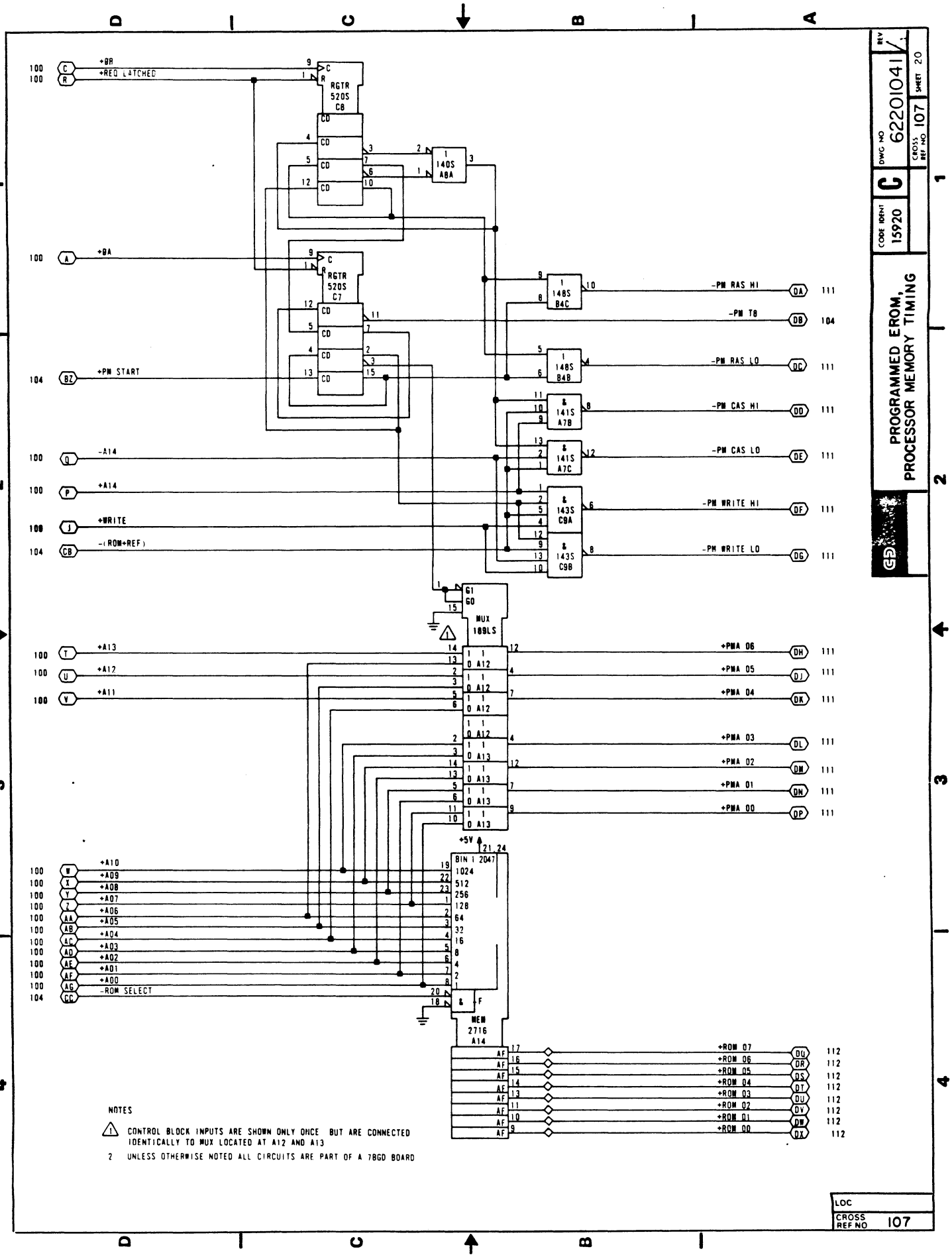
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78GD BOARD

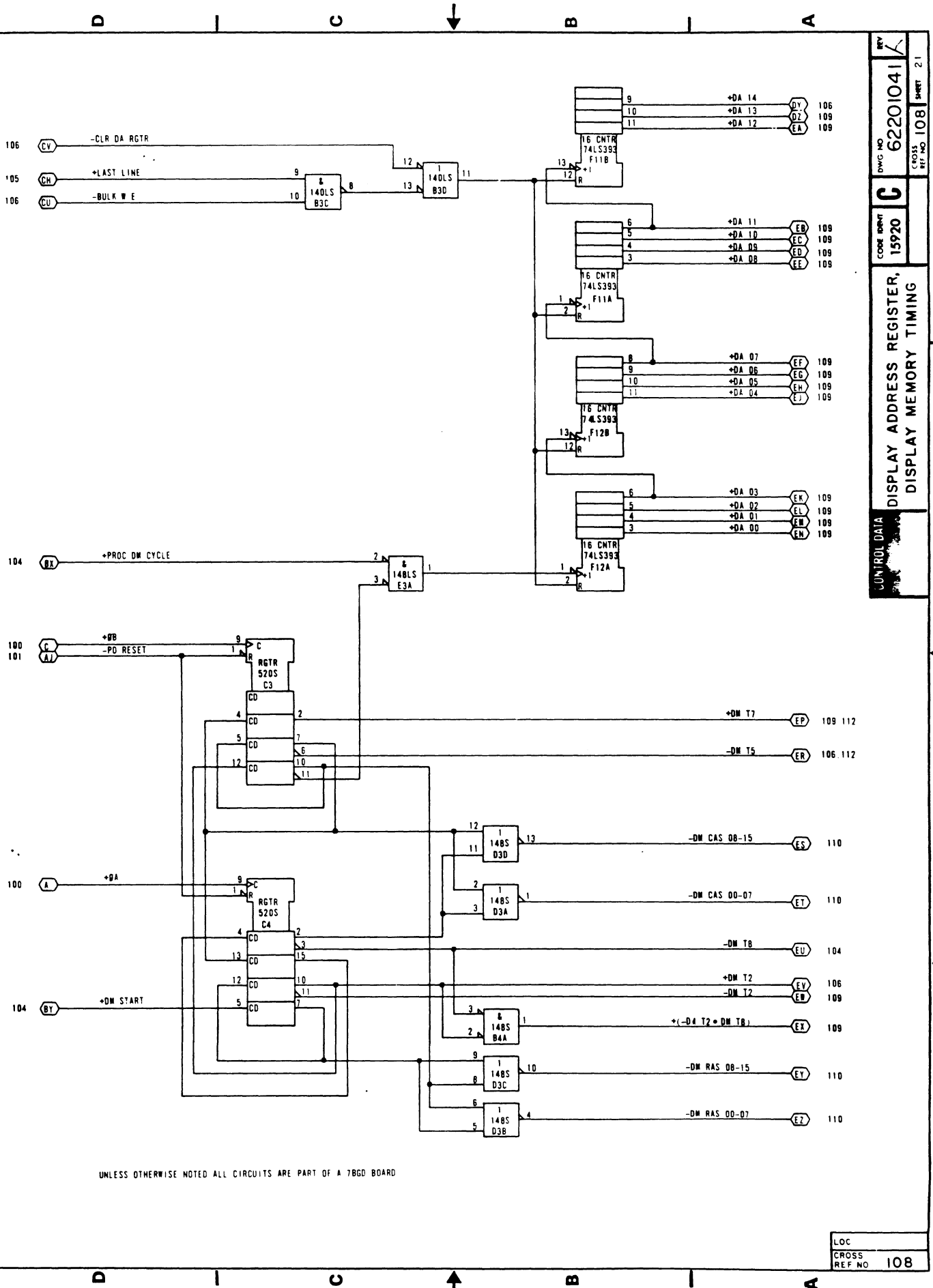
VIDEO SHIFT RGTRS/MUX, DISPLAY DRIVE LOGIC

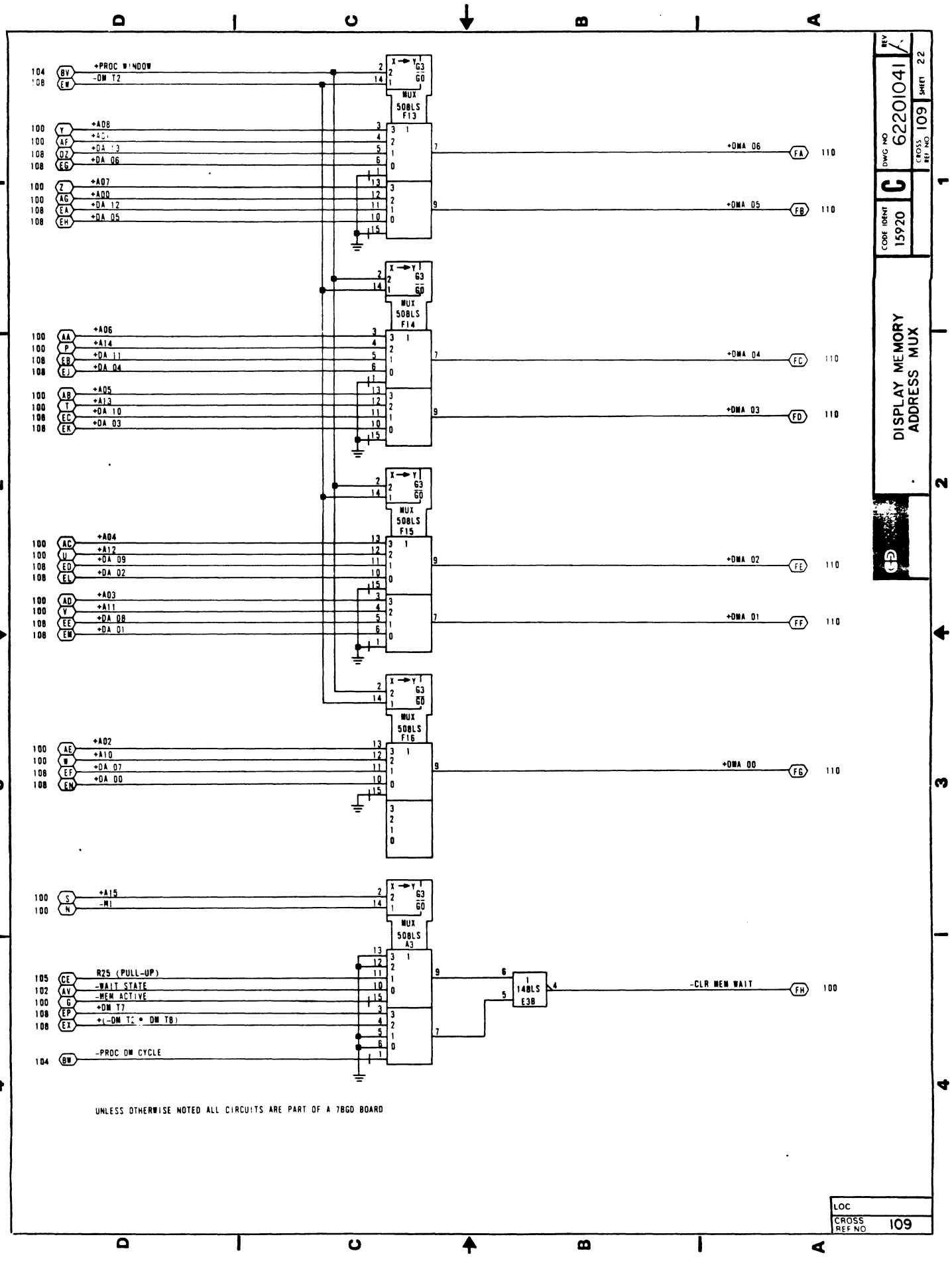
CODE IDENT 15920 | C | DWG NO 62201041 | REV L | CROSS REF NO 105 | SHEET 18

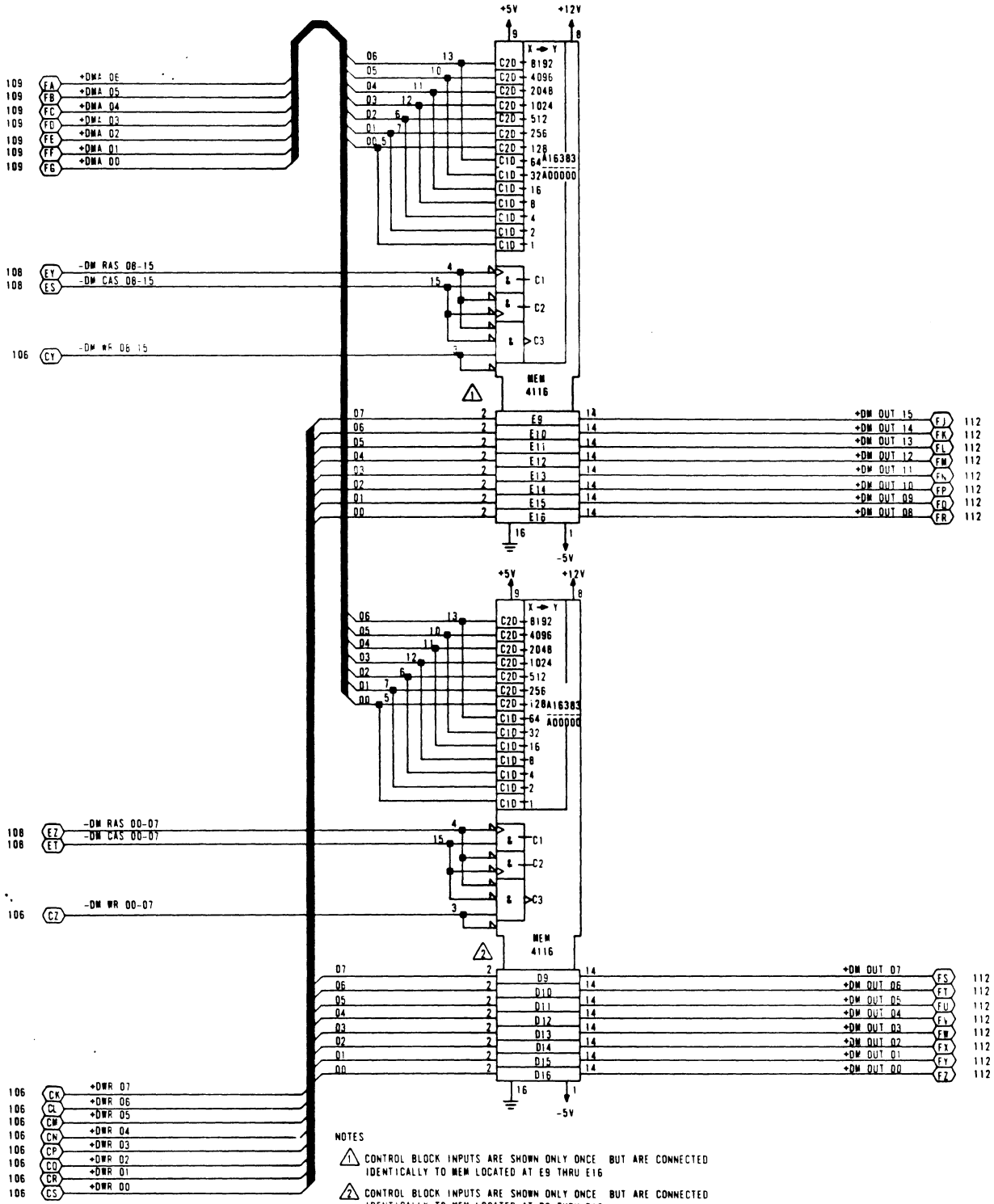
LOC
CROSS REF NO 105

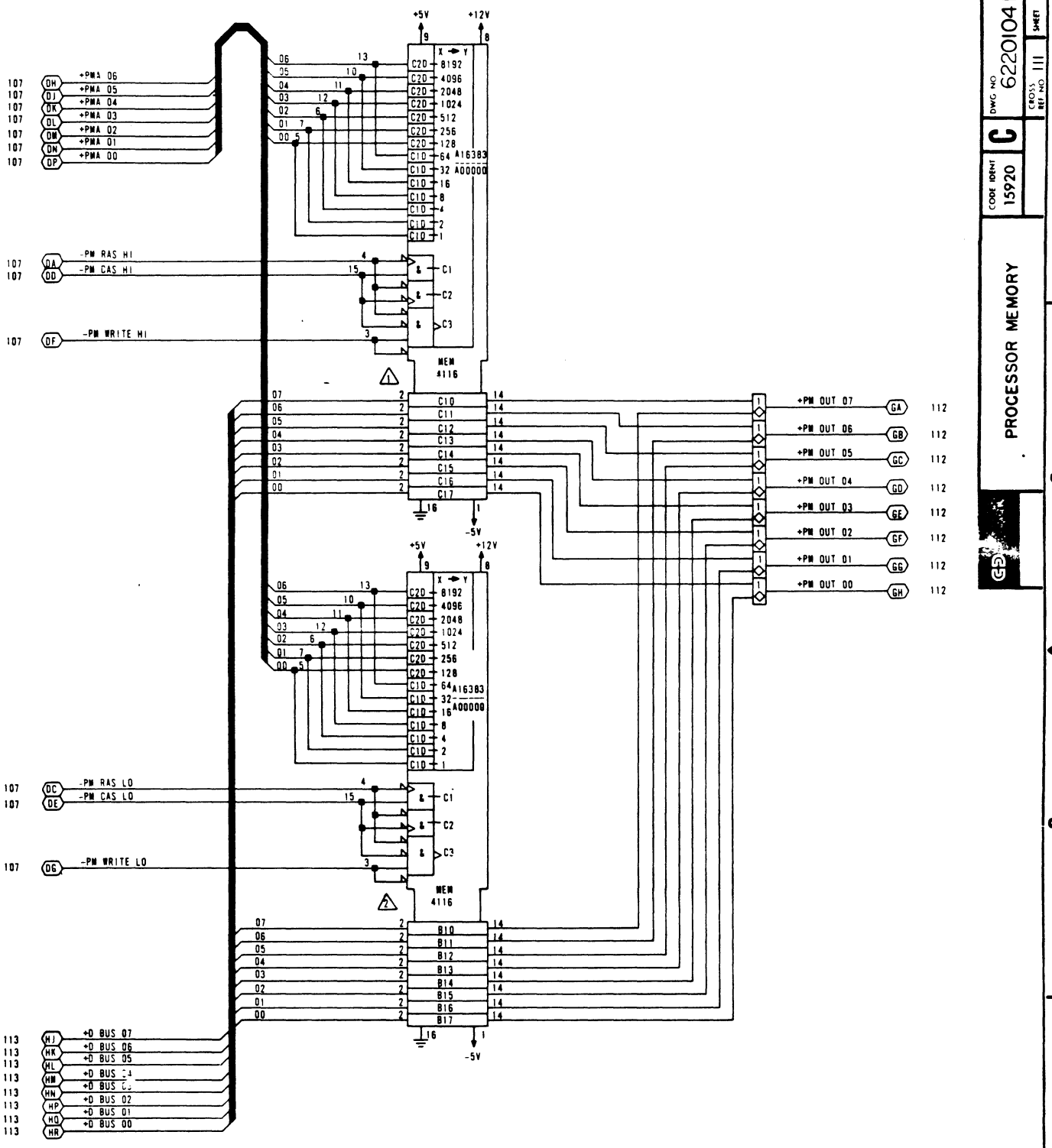

BULK WRITE/ERASE, VIDEO DISABLE
DWG NO 6220104
REV C
CODE IDENT 15920
CROSS REF NO 106
SHEET 19
MUX 189LS
+D BUS 07
+D BUS 06
+D BUS 05
+D BUS 04
+D BUS 03
+D BUS 02
+D BUS 01
+D BUS 00
+DWR 07
+DWR 06
+DWR 05
+DWR 04
+DWR 03
+DWR 02
+DWR 01
+DWR 00
+D 00
-BULK W E
WRITE ONES
S2 A10
"ZEROS"
+5V
R2D 1k C6
R2C 1k C6
+D 02
+DA 14
-PO RESET
+D 01
R2E (PULL-UP)
-F SYNC
-VIDEO DISABLE
-DM T5
-BULK W E
-CLR DA RGTR
+BULK BUSY
-WRITE
+A09
DEMUX 525LS C6
+MEM ACTIVE
-PROC DM CYCLE
-DM RD 08-15
-DM RD 00-07
-DM WR 08-15
-DM WR 00-07
+DM T2
NOTES
1 CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE BUT ARE CONNECTED IDENTICALLY TO MUX LOCATED AT D17 AND E17
2 UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BGD BOARD
LOC
CROSS REF NO 106


PROGRAMMED EROM, PROCESSOR MEMORY TIMING
CODE IDENT 15920
DWG NO 6220104
REV
SHEET 20
CROSS REF NO 107
+BR
+REQ LATCHED
RGTR 520S C8
RGTR 520S C7
+BA
+PM START
-A14
+A14
+WRITE
-(ROM+REF)
-PM RAS HI
-PM T8
-PM RAS LO
-PM CAS HI
-PM CAS LO
-PM WRITE HI
-PM WRITE LO
MUX 189LS
+A13
+A12
+A11
+PMA 06
+PMA 05
+PMA 04
+PMA 03
+PMA 02
+PMA 01
+PMA 00
+5V
BIN 1 2047
1024
512
256
128
64
32
16
8
4
2
1
+A10
+A09
+A08
+A07
+A06
+A05
+A04
+A03
+A02
+A01
+A00
-ROM SELECT
MEM 2716 A14
+ROM 07
+ROM 06
+ROM 05
+ROM 04
+ROM 03
+ROM 02
+ROM 01
+ROM 00
NOTES
1 CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE BUT ARE CONNECTED IDENTICALLY TO MUX LOCATED AT A12 AND A13
2 UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78GD BOARD
LOC
CROSS REF NO 107


DISPLAY ADDRESS REGISTER, DISPLAY MEMORY TIMING
CONTROL DATA
DWG NO 6220104 REV K
CODE IDENT 15920 C
CROSS REF NO 108 SHEET 21
106 CV -CLR DA RGTR
105 CH +LAST LINE
106 CU -BULK W E
140LS B3C
140LS B3D
16 CNTR 74LS393 F11B
16 CNTR 74LS393 F11A
16 CNTR 74LS393 F12B
16 CNTR 74LS393 F12A
+DA 14 DY 106
+DA 13 DZ 109
+DA 12 EA 109
+DA 11 EB 109
+DA 10 EC 109
+DA 09 ED 109
+DA 08 EE 109
+DA 07 EF 109
+DA 06 EG 109
+DA 05 EH 109
+DA 04 EJ 109
+DA 03 EK 109
+DA 02 EL 109
+DA 01 EM 109
+DA 00 EN 109
104 BX +PROC DM CYCLE
148LS E3A
100 C +ØB
101 AJ -PD RESET
RGTR 520S C3
RGTR 520S C4
100 A +ØA
104 BY +DM START
+DM T7 EP 109 112
-DM T5 ER 106 112
148S D3D
148S D3A
148S B4A
148S D3C
148S D3B
-DM CAS 08-15 ES 110
-DM CAS 00-07 ET 110
-DM T8 EU 104
+DM T2 EV 106
-DM T2 EW 109
+(-D4 T2 • DM T8) EX 109
-DM RAS 08-15 EY 110
-DM RAS 00-07 EZ 110
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BGD BOARD
LOC
CROSS REF NO 108


DISPLAY MEMORY ADDRESS MUX
CODE IDENT 15920
DWG NO 62201041
REV C
SHEET 22
CROSS REF NO 109
+PROC WINDOW
-DM T2
MUX 508LS F13
MUX 508LS F14
MUX 508LS F15
MUX 508LS F16
MUX 508LS A3
+DMA 06
+DMA 05
+DMA 04
+DMA 03
+DMA 02
+DMA 01
+DMA 00
-CLR MEM WAIT
R25 (PULL-UP)
-WAIT STATE
-MEM ACTIVE
-PROC DM CYCLE
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78GD BOARD
LOC
CROSS REF NO 109

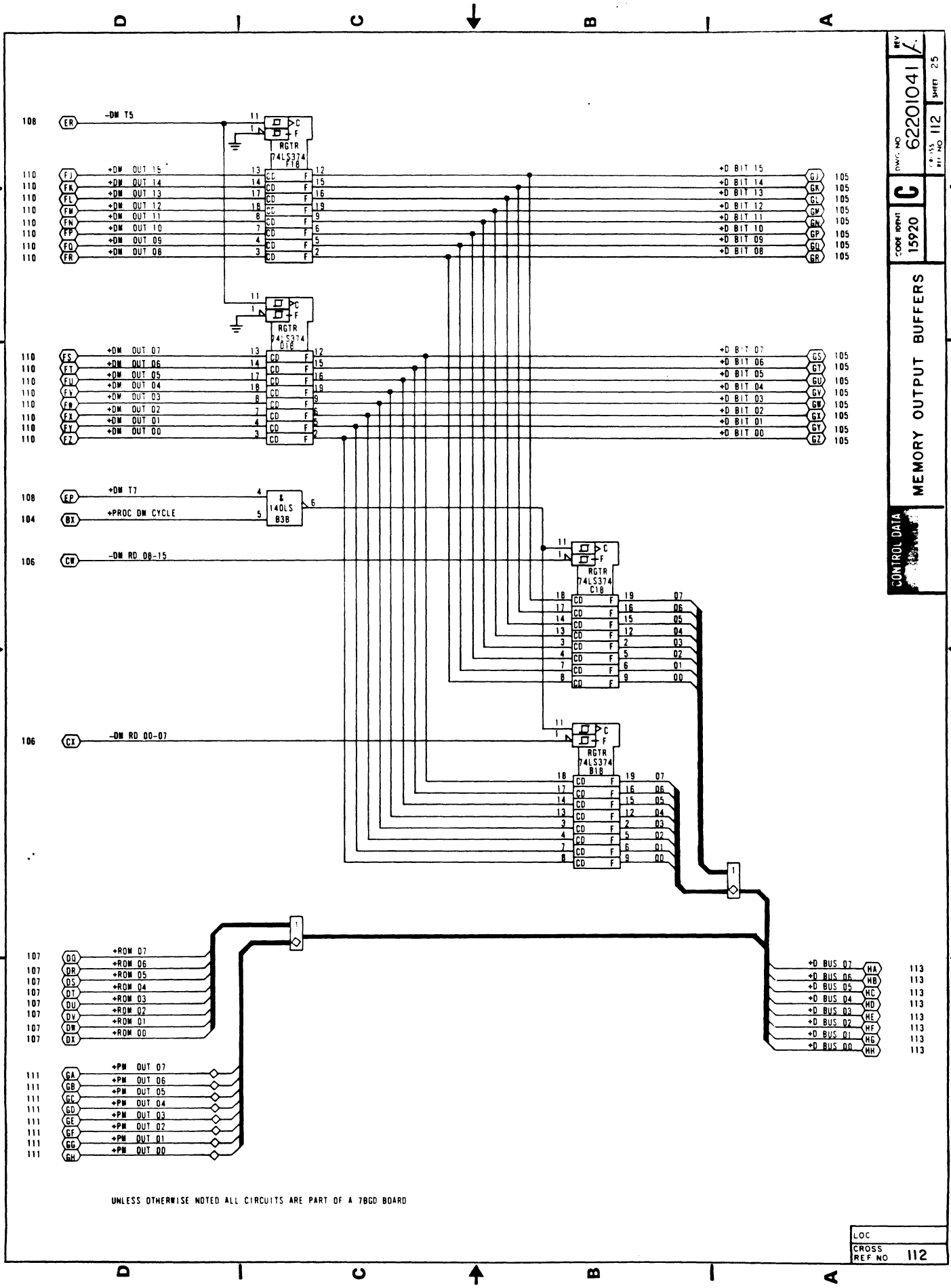

DISPLAY MEMORY
DWG NO 62201041
REV C
CODE IDENT 15920
SHEET 23
CROSS REF NO 110
+5V
+12V
-5V
MEM 4116
-DM RAS 08-15
-DM CAS 08-15
-DM WR 08-15
-DM RAS 00-07
-DM CAS 00-07
-DM WR 00-07
+DMA 00
+DMA 01
+DMA 02
+DMA 03
+DMA 04
+DMA 05
+DMA 06
+DMA 07
+DM OUT 15
+DM OUT 14
+DM OUT 13
+DM OUT 12
+DM OUT 11
+DM OUT 10
+DM OUT 09
+DM OUT 08
+DM OUT 07
+DM OUT 06
+DM OUT 05
+DM OUT 04
+DM OUT 03
+DM OUT 02
+DM OUT 01
+DM OUT 00
+DWR 07
+DWR 06
+DWR 05
+DWR 04
+DWR 03
+DWR 02
+DWR 01
+DWR 00
NOTES
1 CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE BUT ARE CONNECTED IDENTICALLY TO MEM LOCATED AT E9 THRU E16
2 CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE BUT ARE CONNECTED IDENTICALLY TO MEM LOCATED AT D9 THRU D16
3 UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BGD BOARD
LOC
CROSS REF NO 110

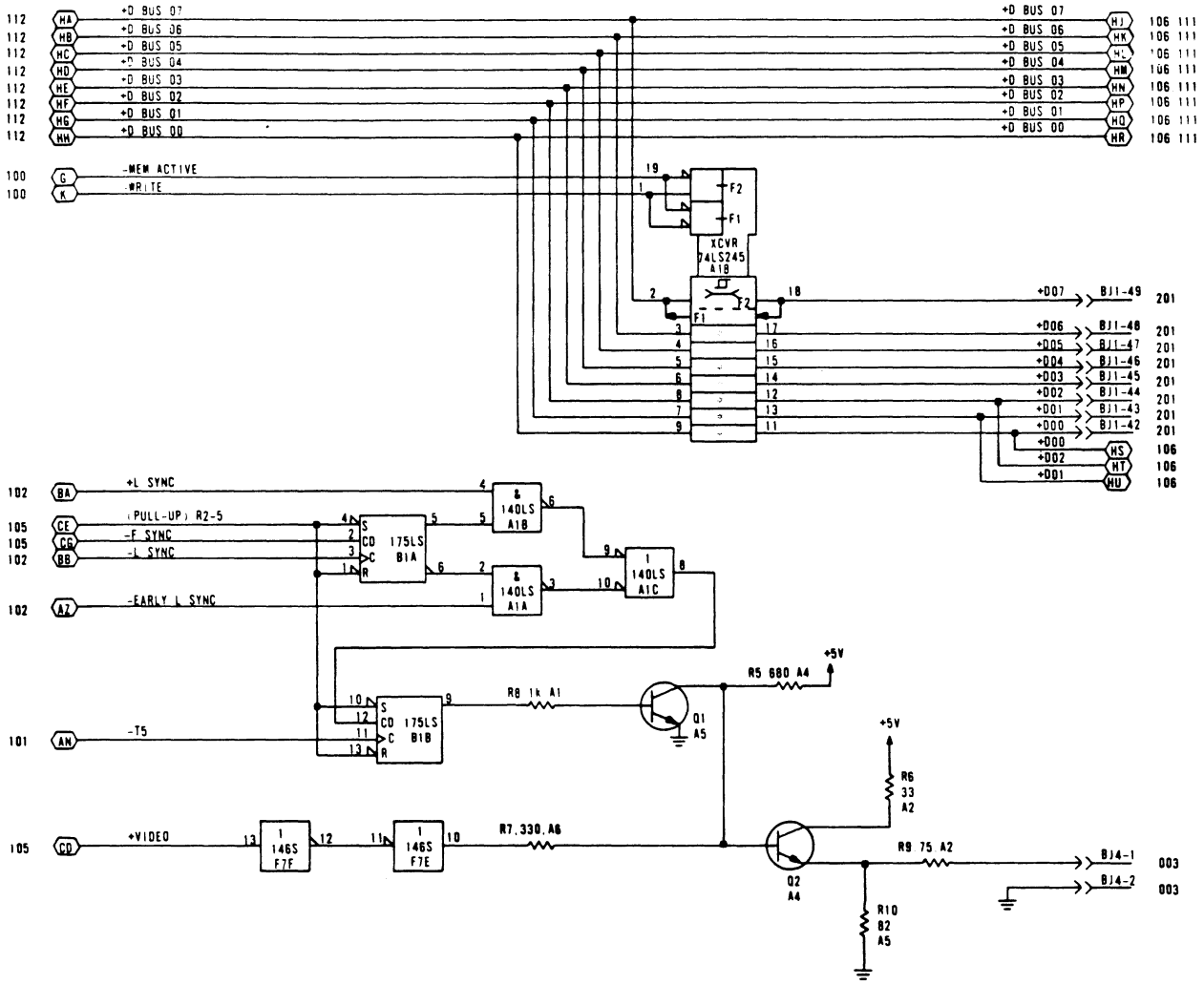


NOTES

1. CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE BUT ARE CONNECTED IDENTICALLY TO MEM LOCATED AT C10 THRU C17
2. CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE BUT ARE CONNECTED IDENTICALLY TO MEM LOCATED AT B10 THRU B17
3. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BGD BOARD
4. MEMORY C10 THRU C17 IS OPTIONAL

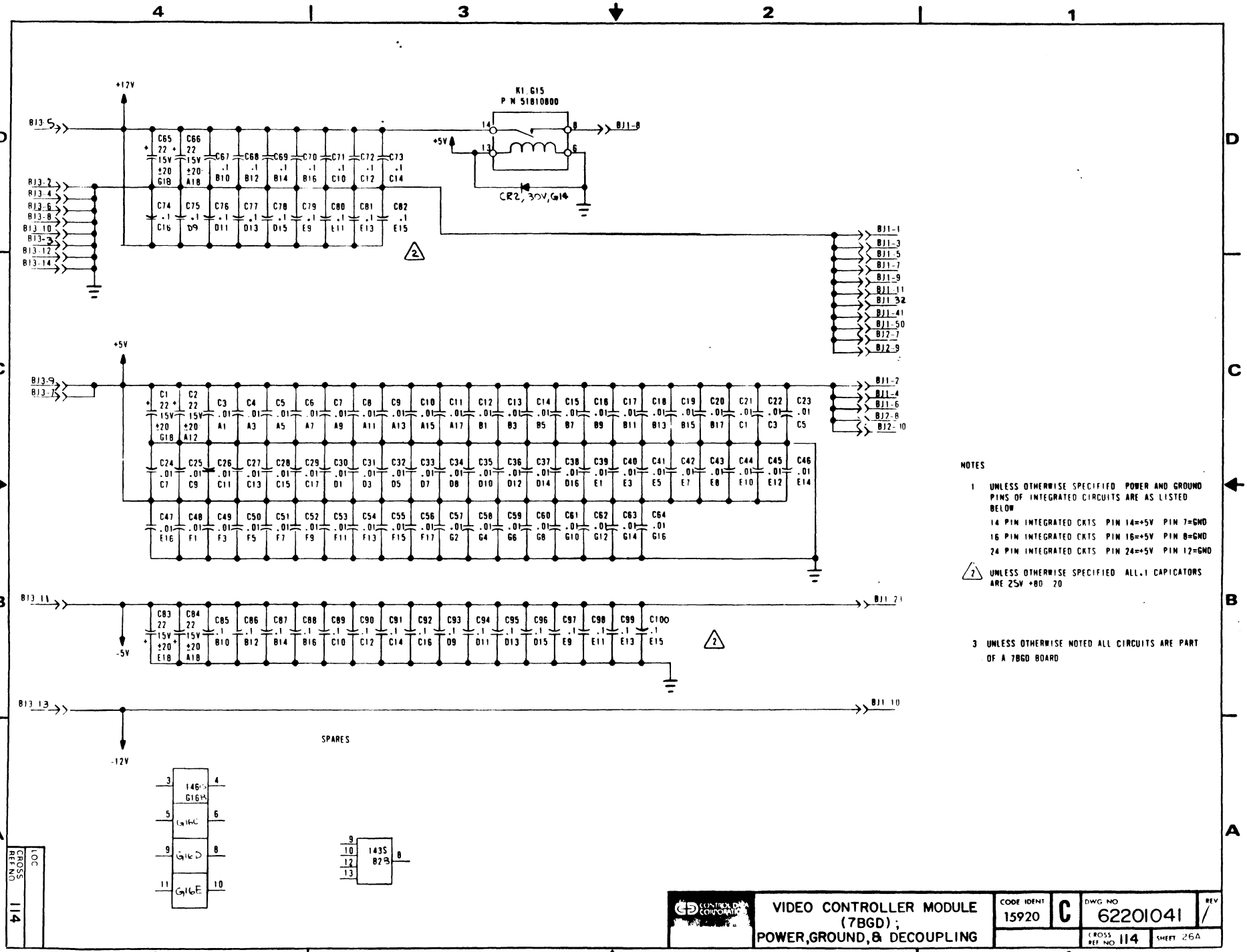
LOC
CROSS REF NO 111


MEMORY OUTPUT BUFFERS
CONTROL DATA
CODE IDENT 15920
DWG NO 62201041
REV
SHEET 25
-DM T5
RGTR 74LS374 F18
+DM OUT 15
+DM OUT 14
+DM OUT 13
+DM OUT 12
+DM OUT 11
+DM OUT 10
+DM OUT 09
+DM OUT 08
+D BIT 15
+D BIT 14
+D BIT 13
+D BIT 12
+D BIT 11
+D BIT 10
+D BIT 09
+D BIT 08
RGTR 74LS374 D18
+DM OUT 07
+DM OUT 06
+DM OUT 05
+DM OUT 04
+DM OUT 03
+DM OUT 02
+DM OUT 01
+DM OUT 00
+D BIT 07
+D BIT 06
+D BIT 05
+D BIT 04
+D BIT 03
+D BIT 02
+D BIT 01
+D BIT 00
+DM T7
& 14LS B3B
+PROC DM CYCLE
-DM RD 08-15
RGTR 74LS374 C18
-DM RD 00-07
RGTR 74LS374 B18
+ROM 07
+ROM 06
+ROM 05
+ROM 04
+ROM 03
+ROM 02
+ROM 01
+ROM 00
+PM OUT 07
+PM OUT 06
+PM OUT 05
+PM OUT 04
+PM OUT 03
+PM OUT 02
+PM OUT 01
+PM OUT 00
+D BUS 07
+D BUS 06
+D BUS 05
+D BUS 04
+D BUS 03
+D BUS 02
+D BUS 01
+D BUS 00
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78GD BOARD
LOC
CROSS REF NO 112



UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BGD BOARD

LOC
CROSS REF NO 113



NOTES

1 UNLESS OTHERWISE SPECIFIED POWER AND GROUND PINS OF INTEGRATED CIRCUITS ARE AS LISTED BELOW

14 PIN INTEGRATED CKTS PIN 14=+5V PIN 7=GND

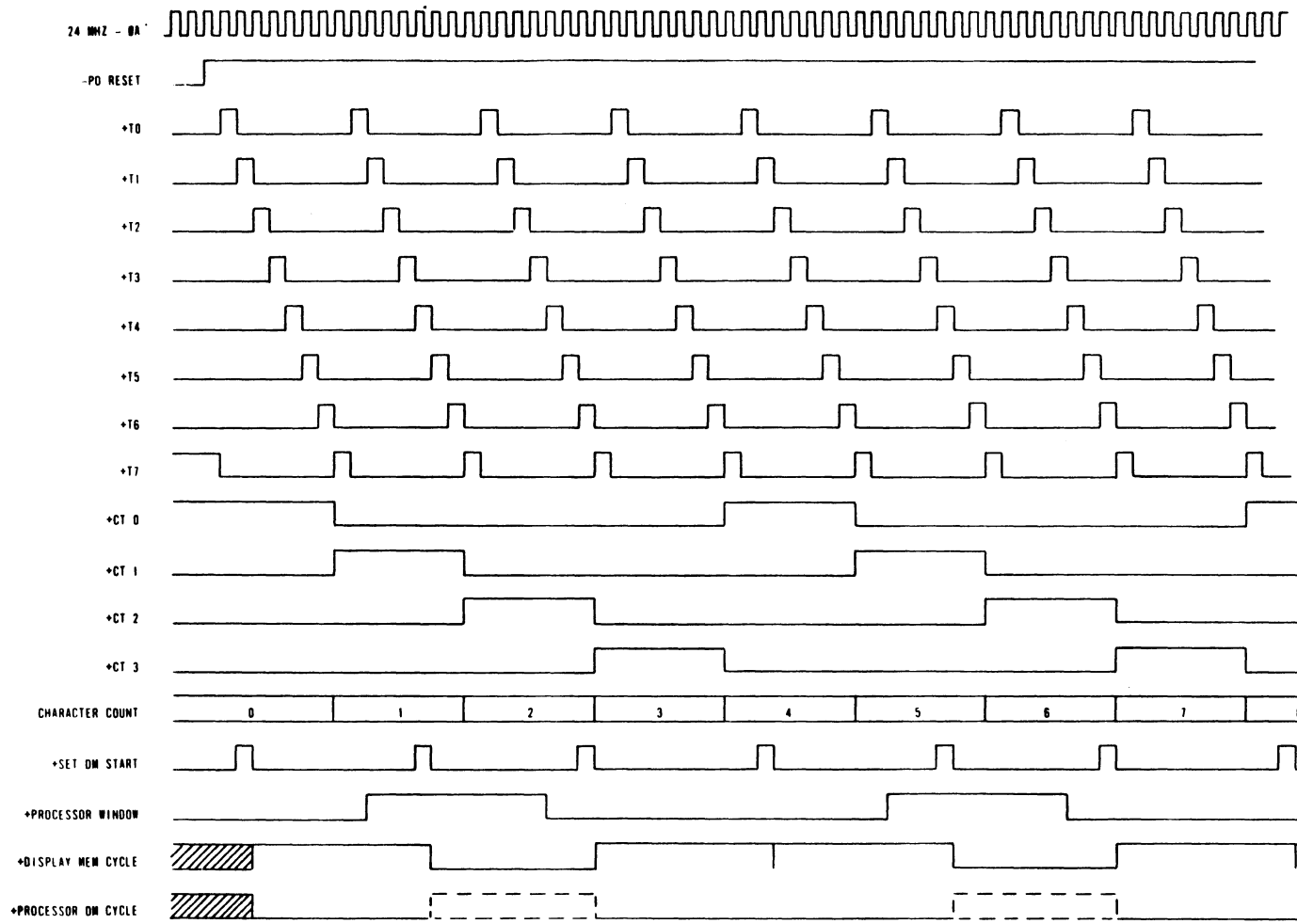
16 PIN INTEGRATED CKTS PIN 16=+5V PIN 8=GND

24 PIN INTEGRATED CKTS PIN 24=+5V PIN 12=GND

2 UNLESS OTHERWISE SPECIFIED ALL.1 CAPICATORS ARE 25V ±80 -20

3 UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BGD BOARD

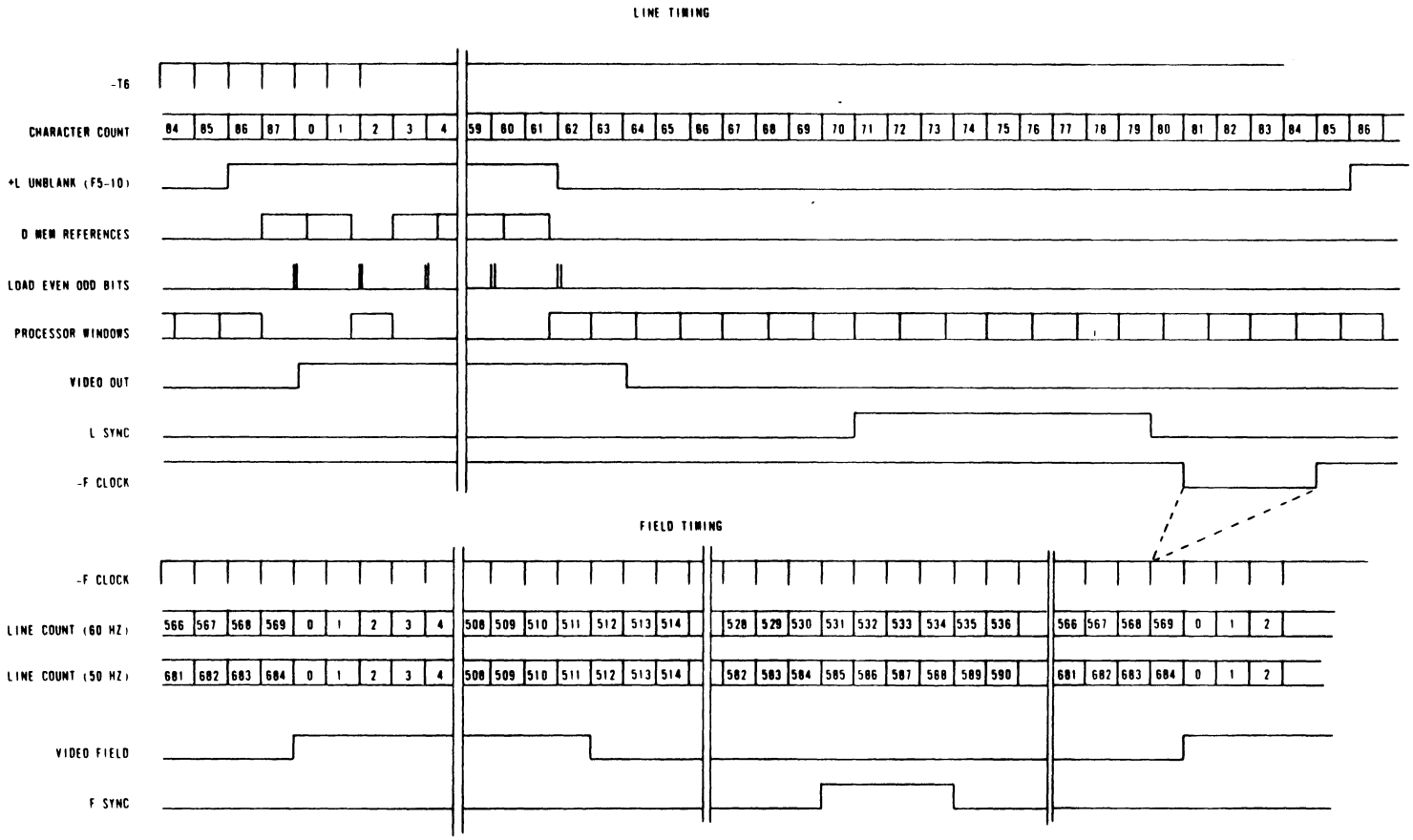
CONTROL DATA CORPORATION	VIDEO CONTROLLER MODULE (7BGD); POWER, GROUND, & DECOUPLING	CODE IDENT 15920	C	DWG NO 62201041 REV /
				CROSS REF NO 114 SHEET 26A



LOC
CROSS REF NO

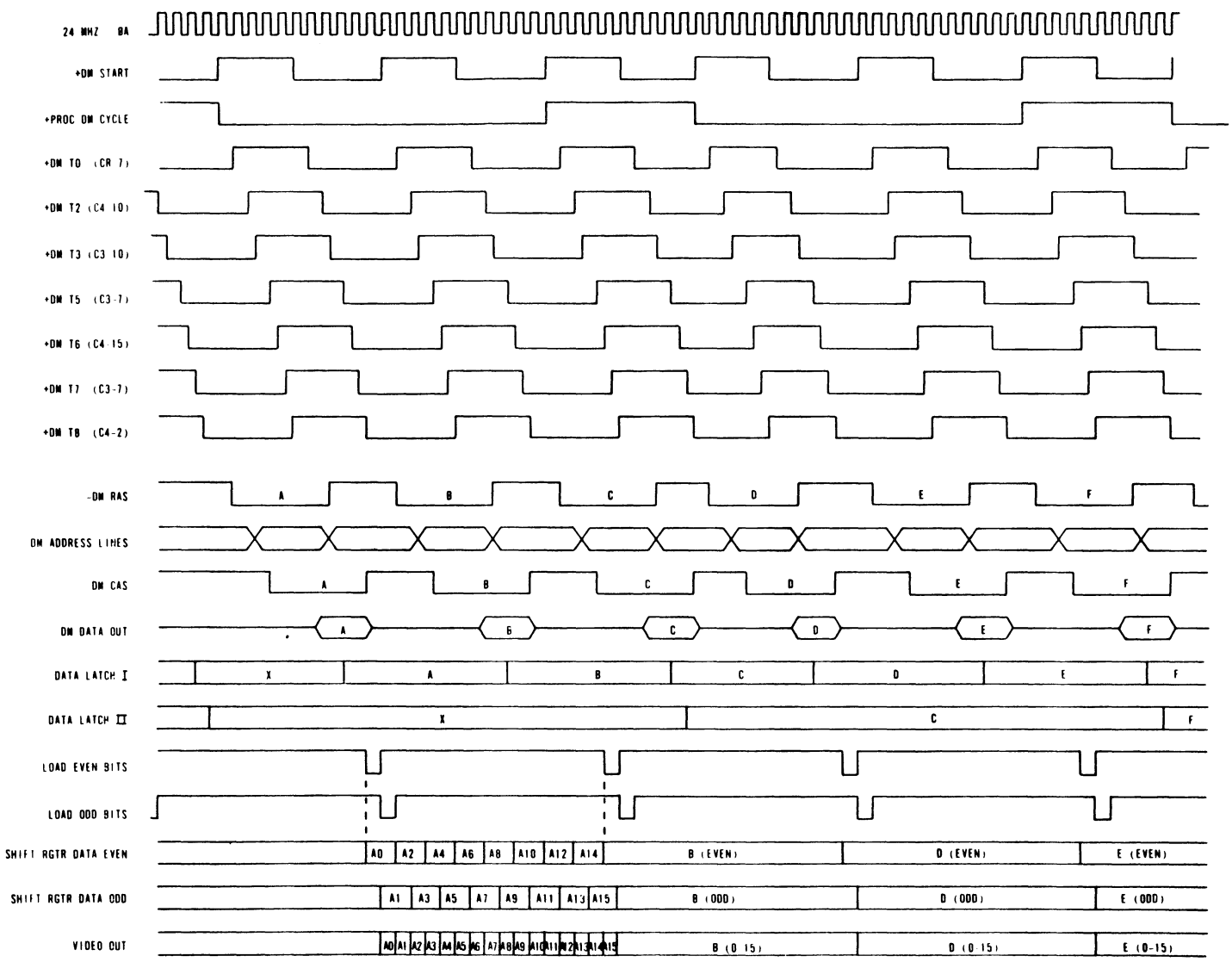
VIDEO DOT TIMING, CHARACTER TIMING AND MEMORY WINDOWS

CODE IDENT		DWG NO	REV
15920	C	6220104	A
		CROSS REF NO	SHEET 27



LOC
CROSS REF NO

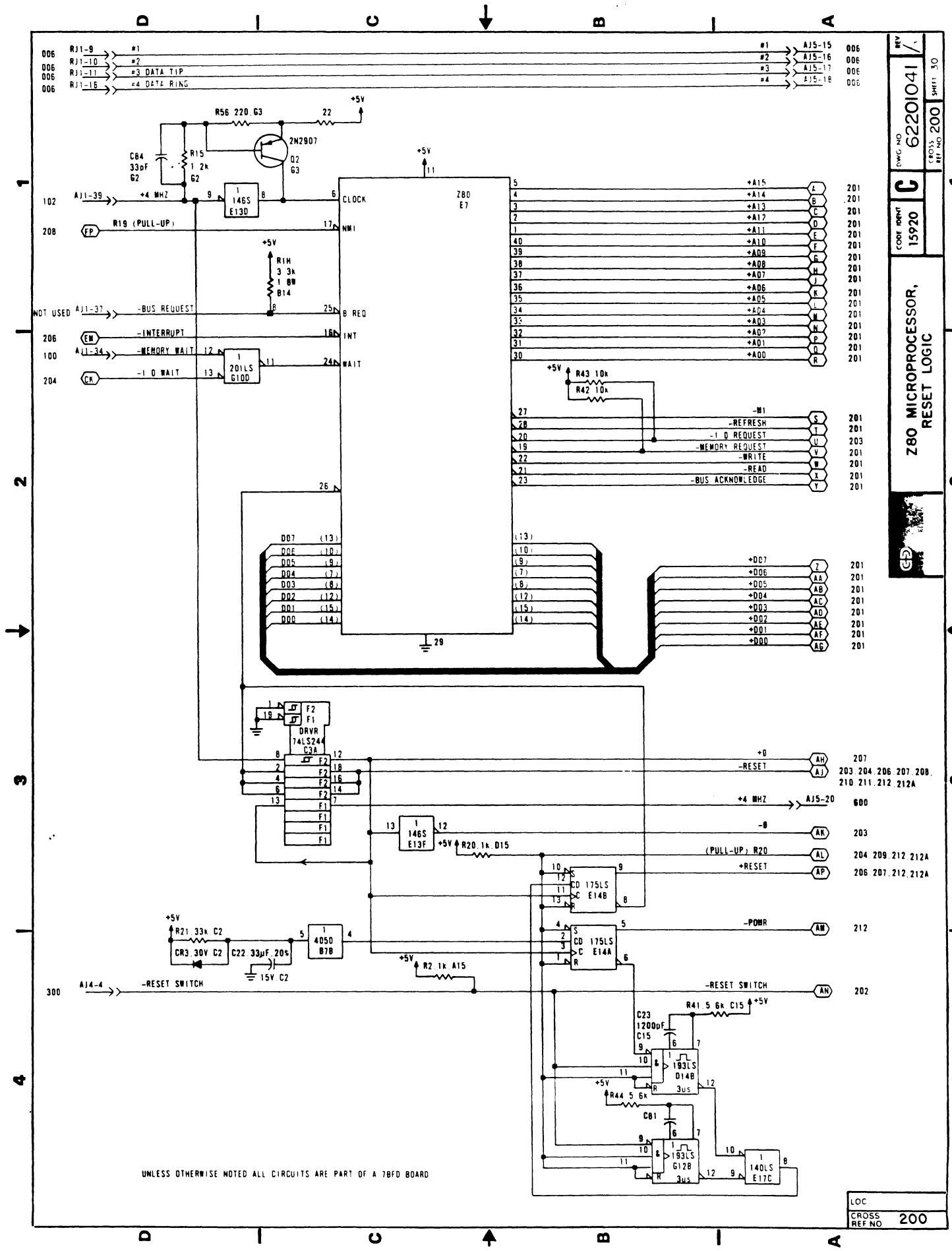
LINE TIMING FIELD (50/60 HZ) TIMING	CODE IDENT 15920	C	DWG NO 62201041	REV A
			CROSS REF NO	SHEET 28

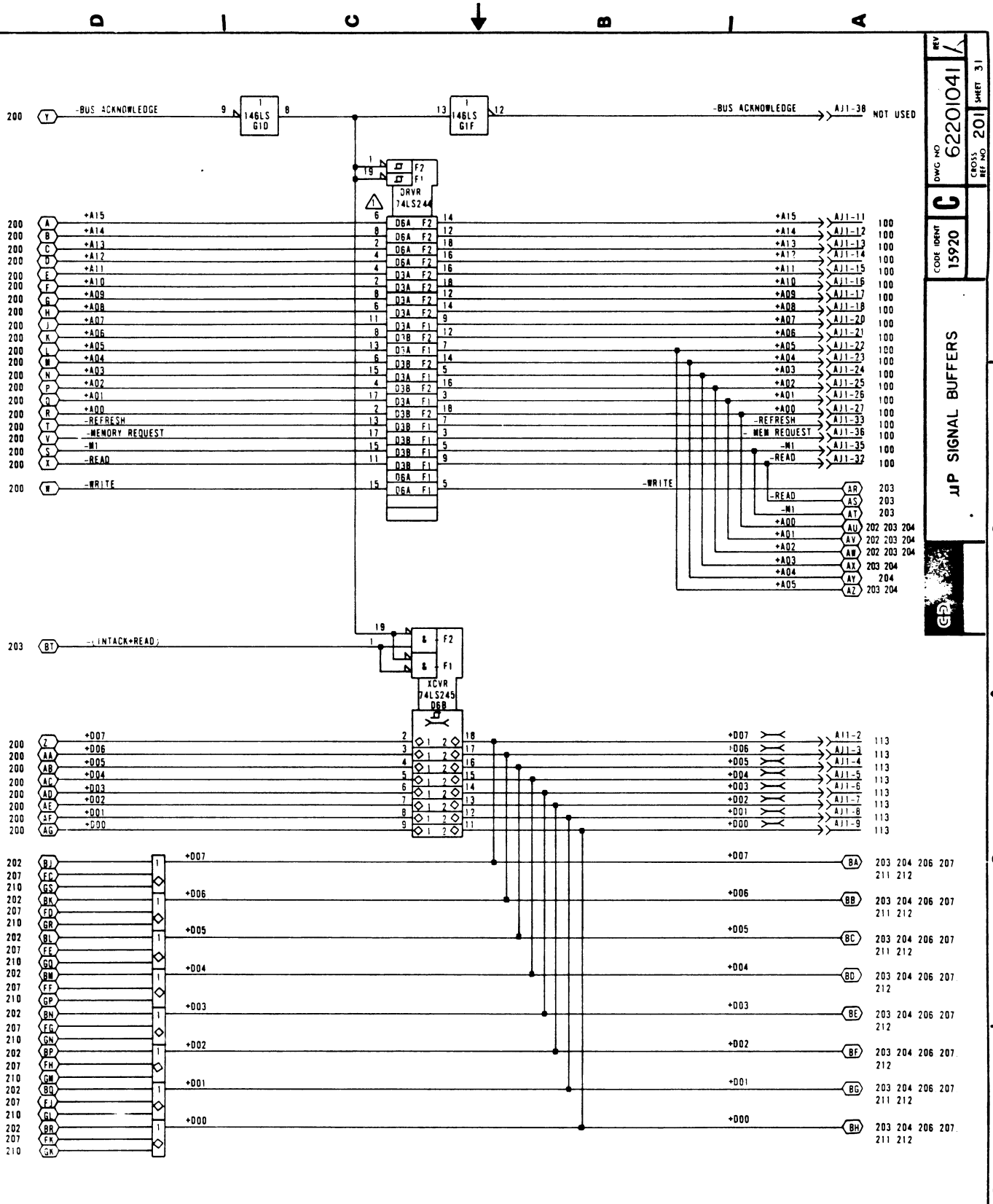


LOC
CROSS REF NO

DISPLAY MEMORY TIMING

CODE IDENT		DWG NO	REV
15920	C	62201041	A
		CROSS REF NO	SHEET 29

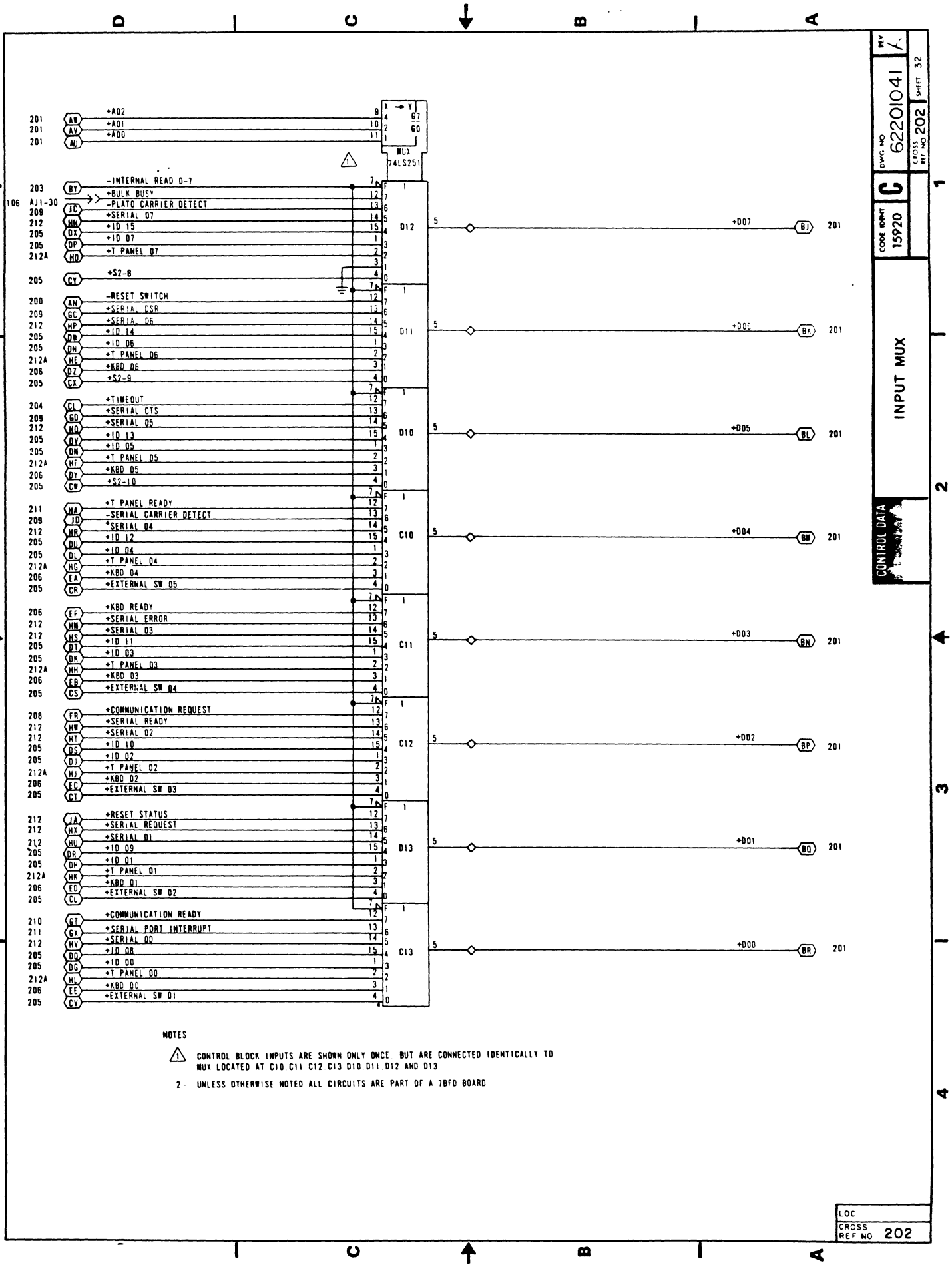

Z80 MICROPROCESSOR, RESET LOGIC
DWG NO 6220104 1
REV A
CODE IDENT 15920
C
CROSS REF NO 200
SHEET 30
Z80 E7
CLOCK
NMI
B REQ
INT
WAIT
+4 MHZ
R19 (PULL-UP)
-BUS REQUEST
-INTERRUPT
-MEMORY WAIT
-I O WAIT
-M1
-REFRESH
-I O REQUEST
-MEMORY REQUEST
-WRITE
-READ
-BUS ACKNOWLEDGE
+A15
+A14
+A13
+A12
+A11
+A10
+A09
+A08
+A07
+A06
+A05
+A04
+A03
+A02
+A01
+A00
+D07
+D06
+D05
+D04
+D03
+D02
+D01
+D00
DRVR 74LS244 C3A
-RESET
-PWR
-RESET SWITCH
+4 MHZ
(PULL-UP) R20
+RESET
R56 220 G3
2N2907
Q2 G3
C84 33pF G2
R15 1 2k G2
R1H 3 3k 1 8W B14
R43 10k
R42 10k
R20 1k D15
R21 33k C2
CR3 30V C2
C22 33µF 20% 15V C2
R2 1k A15
R41 5 6k C15
C23 1200pF C15
R44 5 6k
C81
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD
LOC
CROSS REF NO 200



NOTES

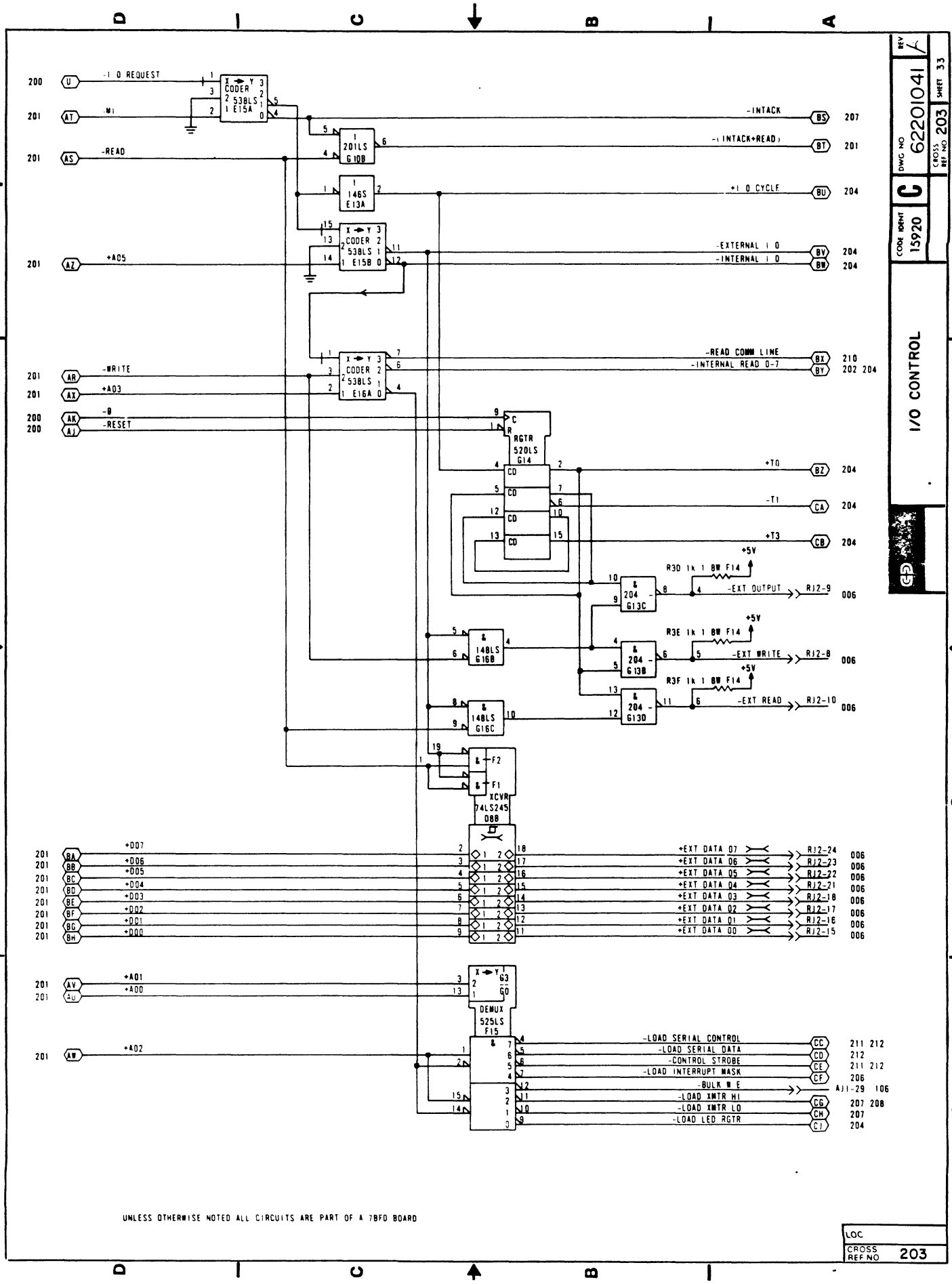
1. CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE BUT ARE CONNECTED IDENTICALLY TO DRVR LOCATED AT D3A, D3B AND D6A
2. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78FD BOARD

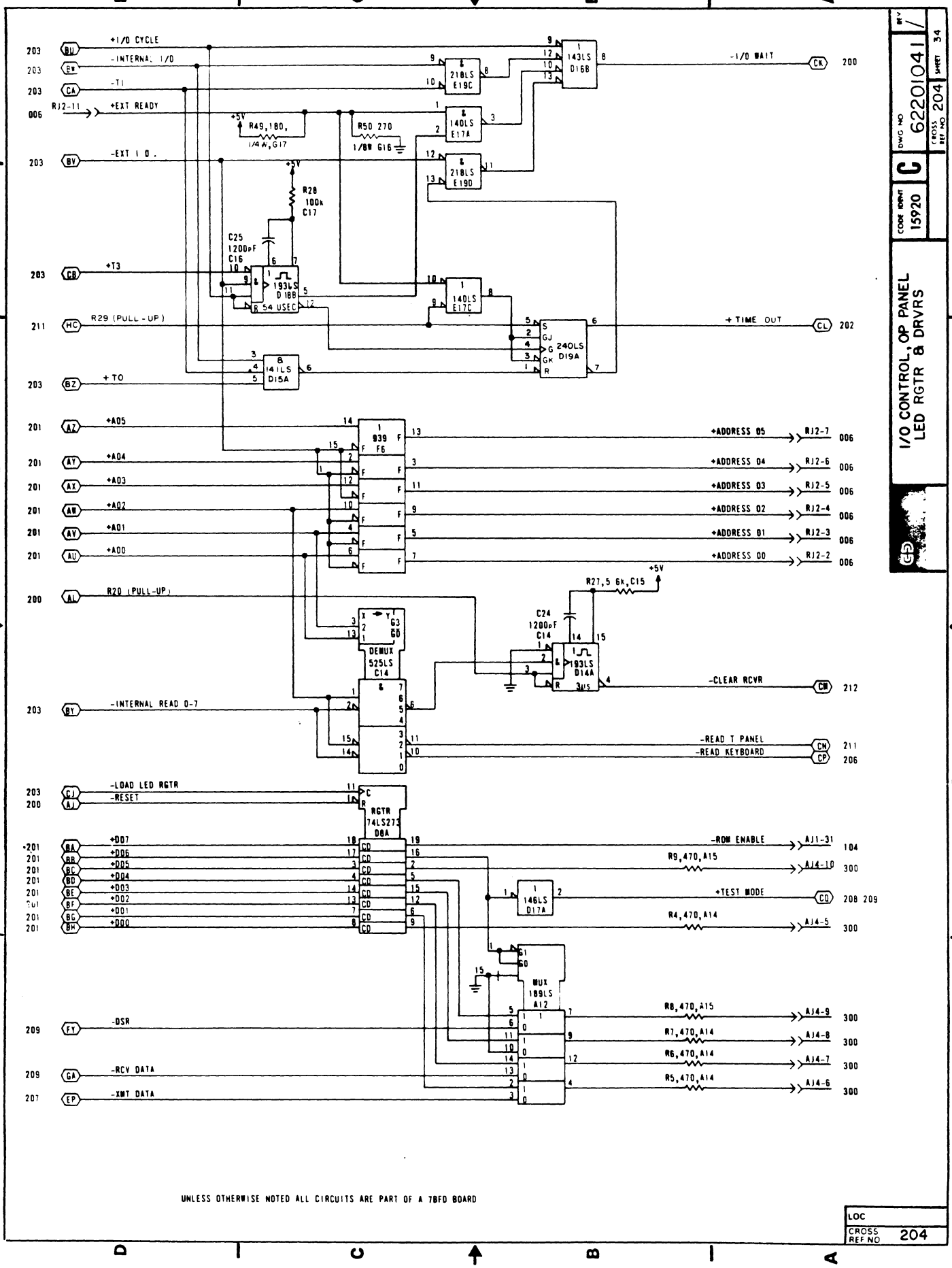
LOC
CROSS REF NO 201



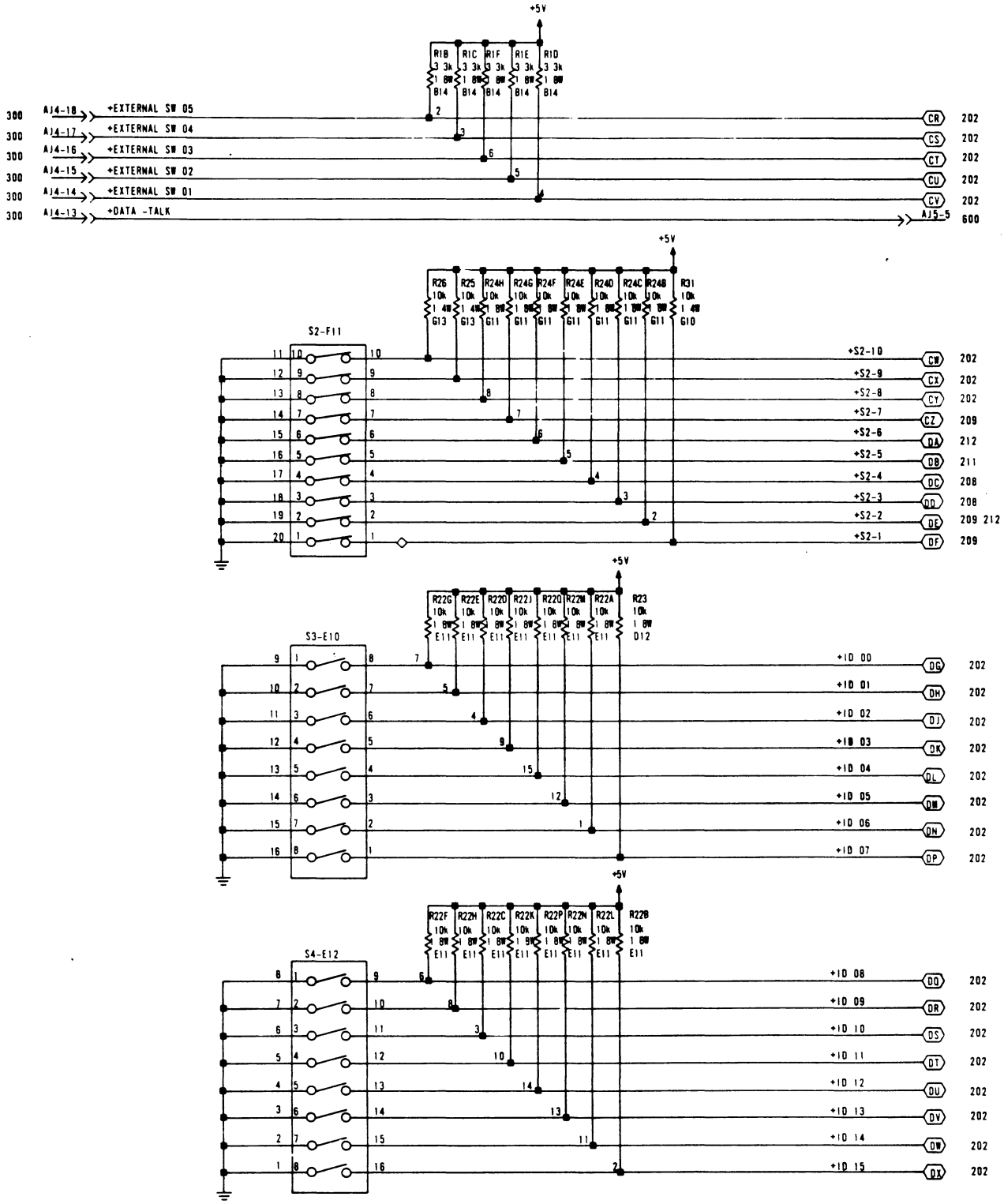
NOTES

1. CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE BUT ARE CONNECTED IDENTICALLY TO MUX LOCATED AT C10 C11 C12 C13 D10 D11 D12 AND D13
2. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD


I/O CONTROL
DWG NO 62201041
REV C
SHEET 33
CROSS REF NO 203
CODE IDENT 15920
-I O REQUEST
-MI
-READ
+AD5
-WRITE
+AD3
-0
-RESET
-INTACK
-(INTACK+READ)
+I O CYCLE
-EXTERNAL I O
-INTERNAL I O
-READ COMM LINE
-INTERNAL READ 0-7
+T0
-T1
+T3
+5V
R3D 1k 1 BW F14
R3E 1k 1 BW F14
R3F 1k 1 BW F14
-EXT OUTPUT
-EXT WRITE
-EXT READ
RJ2-9
RJ2-8
RJ2-10
+D07
+D06
+D05
+D04
+D03
+D02
+D01
+D00
+EXT DATA 07
+EXT DATA 06
+EXT DATA 05
+EXT DATA 04
+EXT DATA 03
+EXT DATA 02
+EXT DATA 01
+EXT DATA 00
RJ2-24
RJ2-23
RJ2-22
RJ2-21
RJ2-18
RJ2-17
RJ2-16
RJ2-15
+A01
+A00
+A02
-LOAD SERIAL CONTROL
-LOAD SERIAL DATA
-CONTROL STROBE
-LOAD INTERRUPT MASK
-BULK M E
-LOAD XMTR HI
-LOAD XMTR LO
-LOAD LED RGTR
AJ1-29
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD
LOC
CROSS REF NO 203



UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD

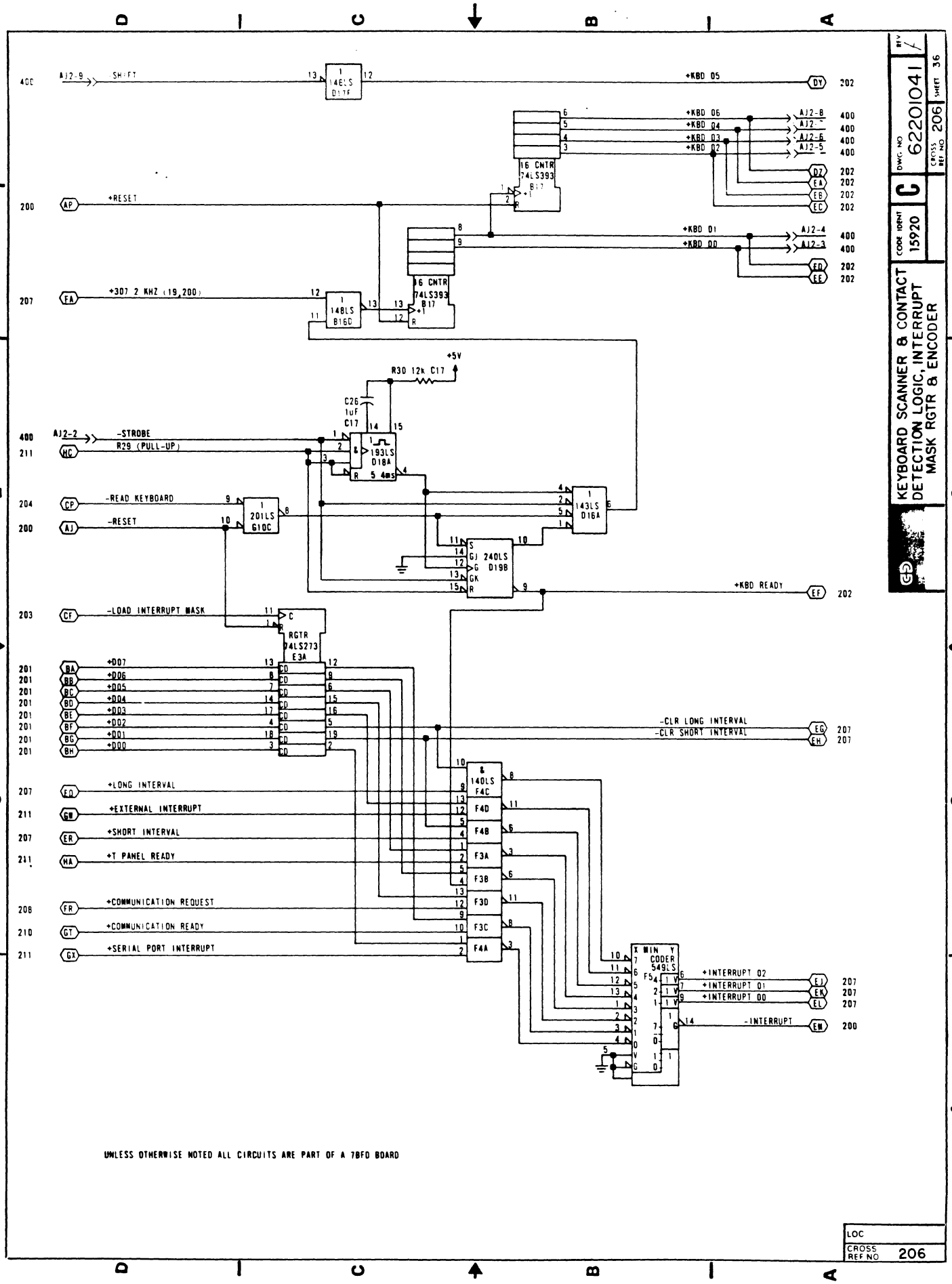


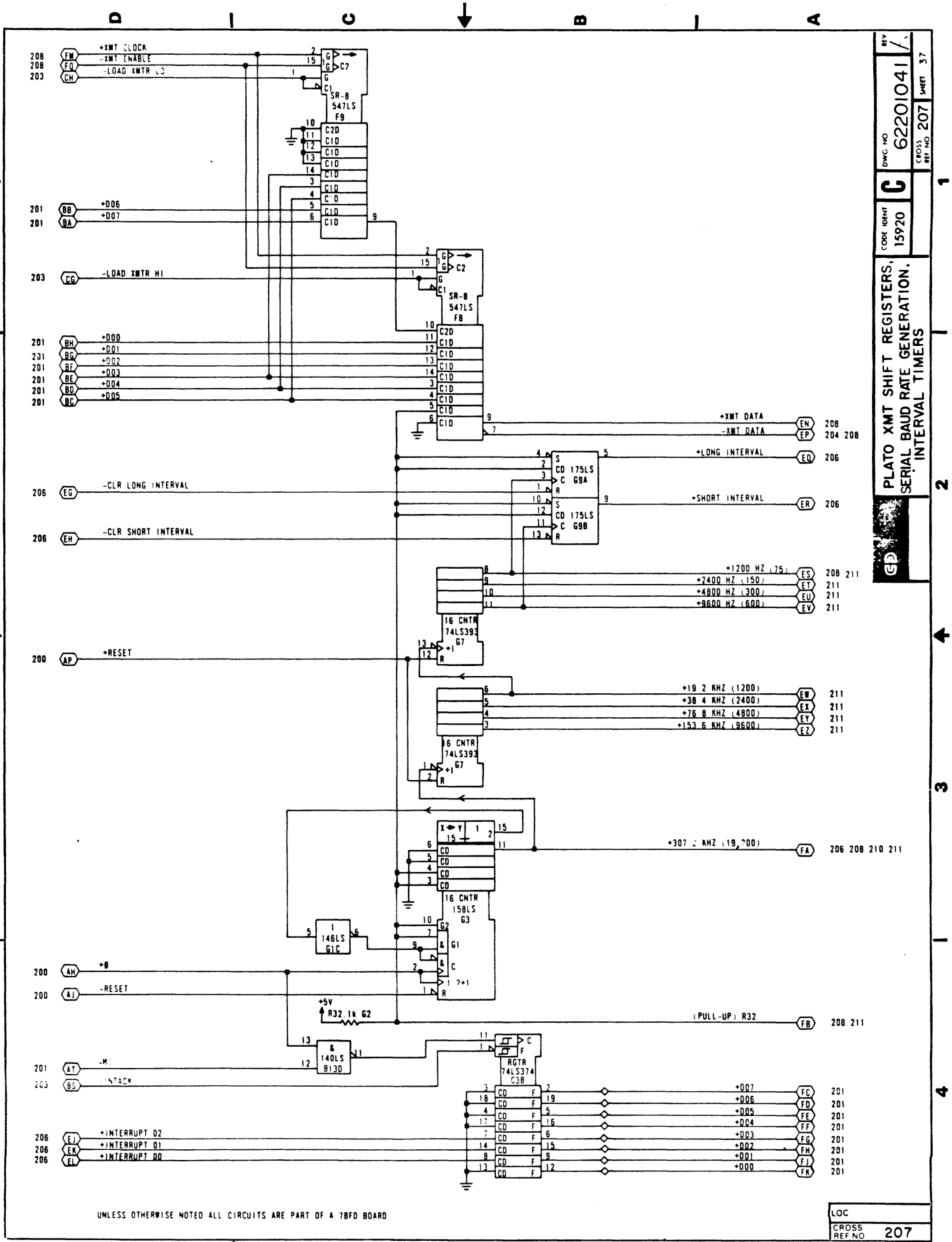
FEATURE SELECT SWITCHES, I.D. CODE SHUNTS

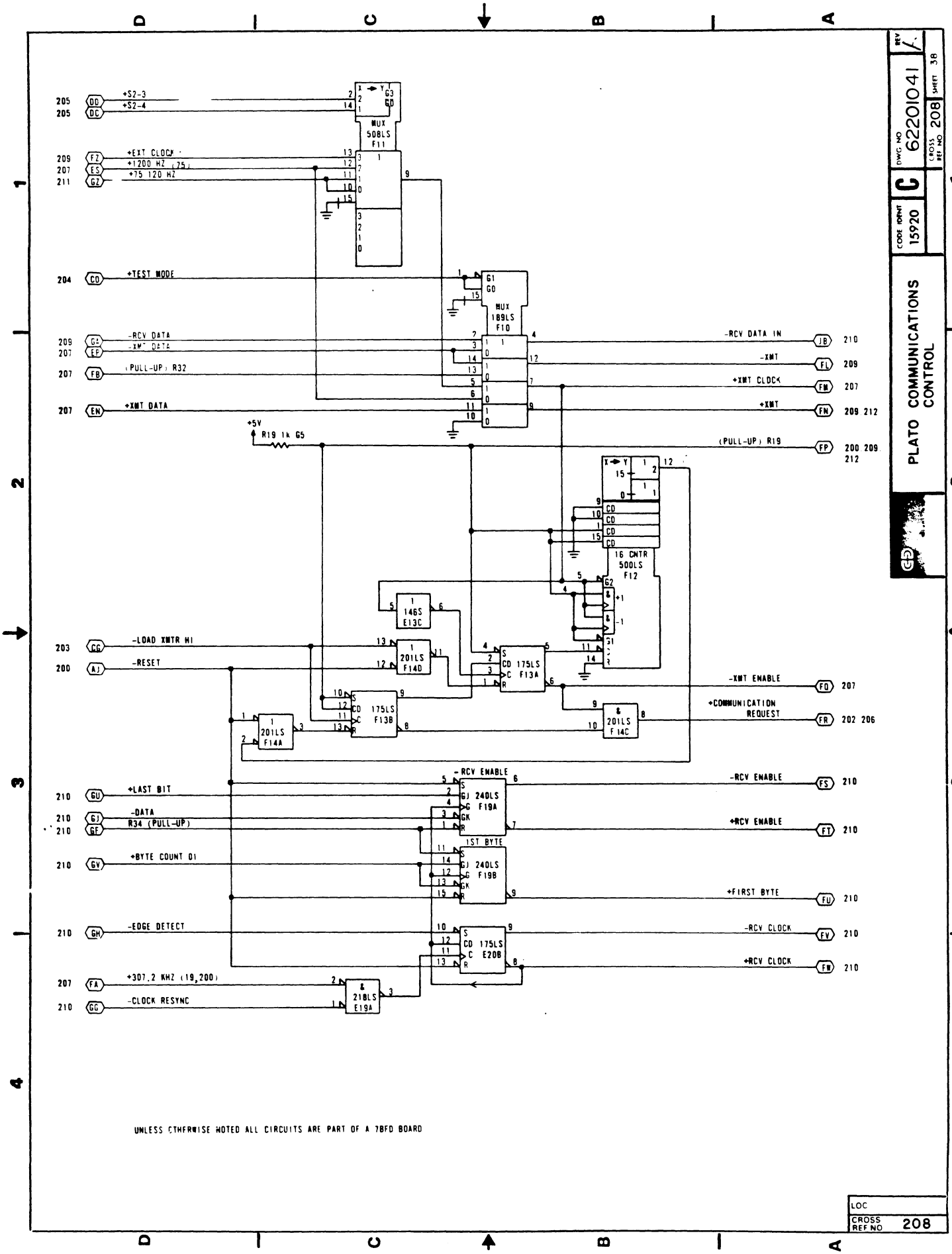
CODE IDENT 15920 | C | DWG NO 62201041 | REV K | SHEET 35 | CROSS REF NO 205

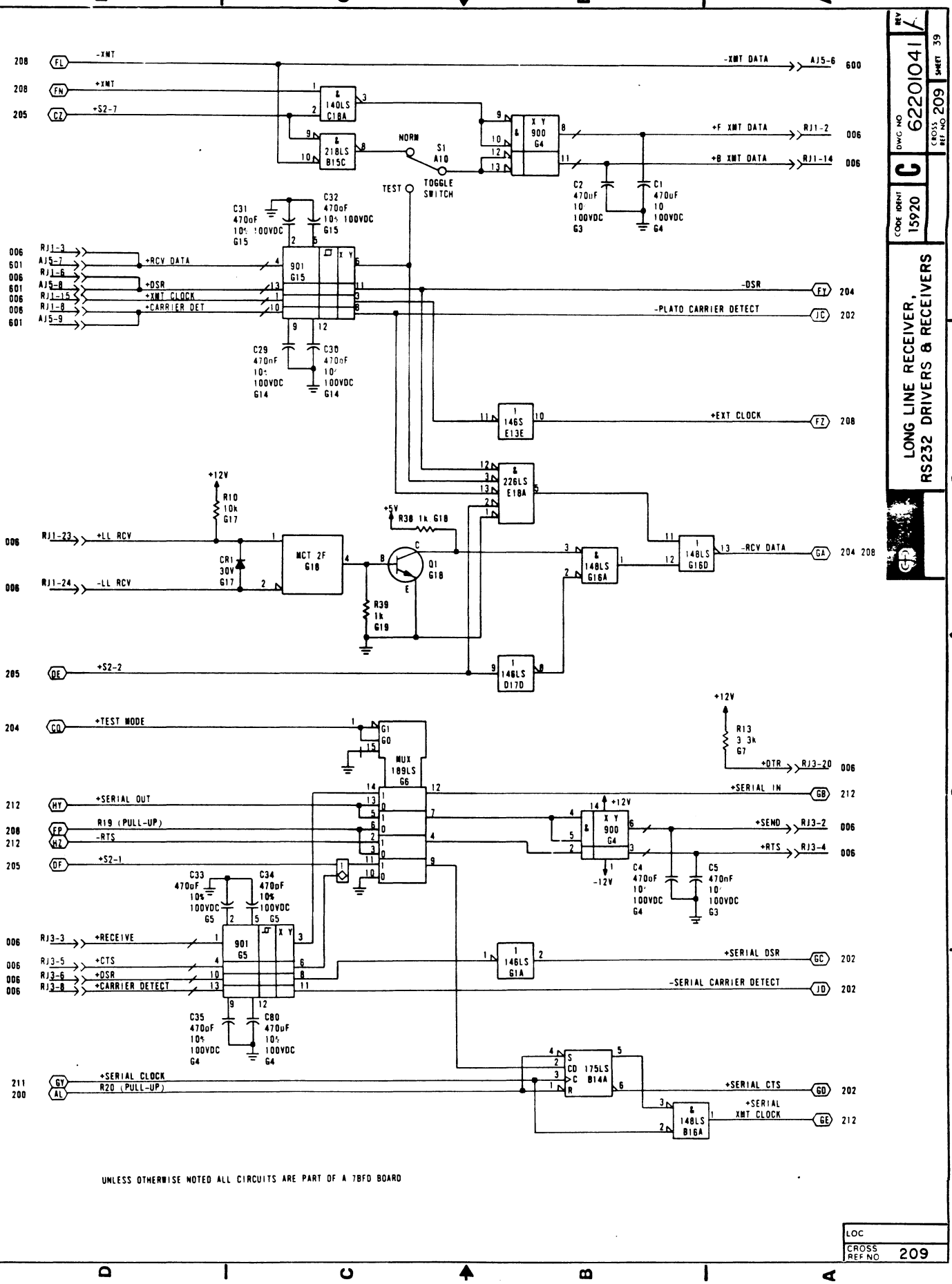
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD

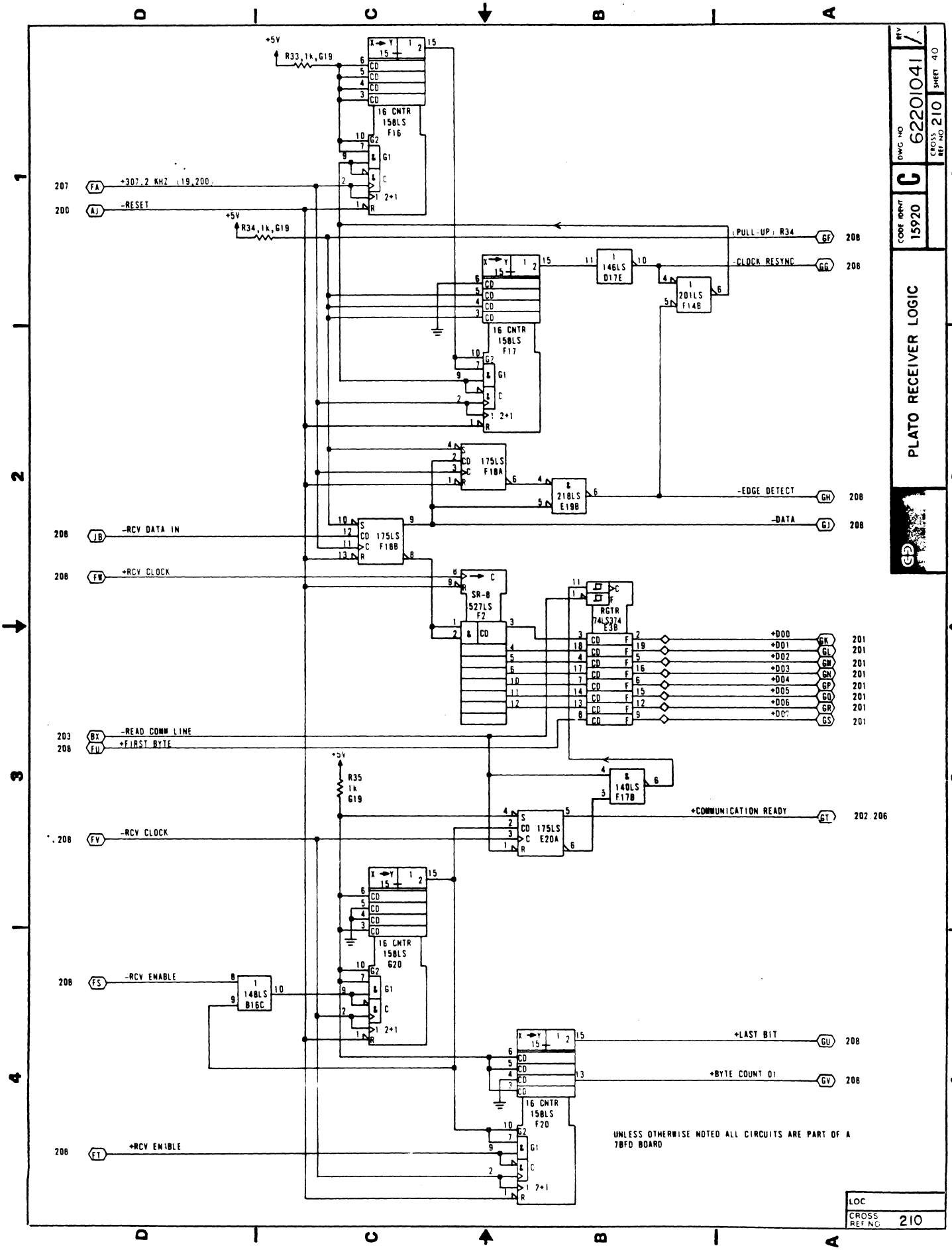
LOC
CROSS REF NO 205

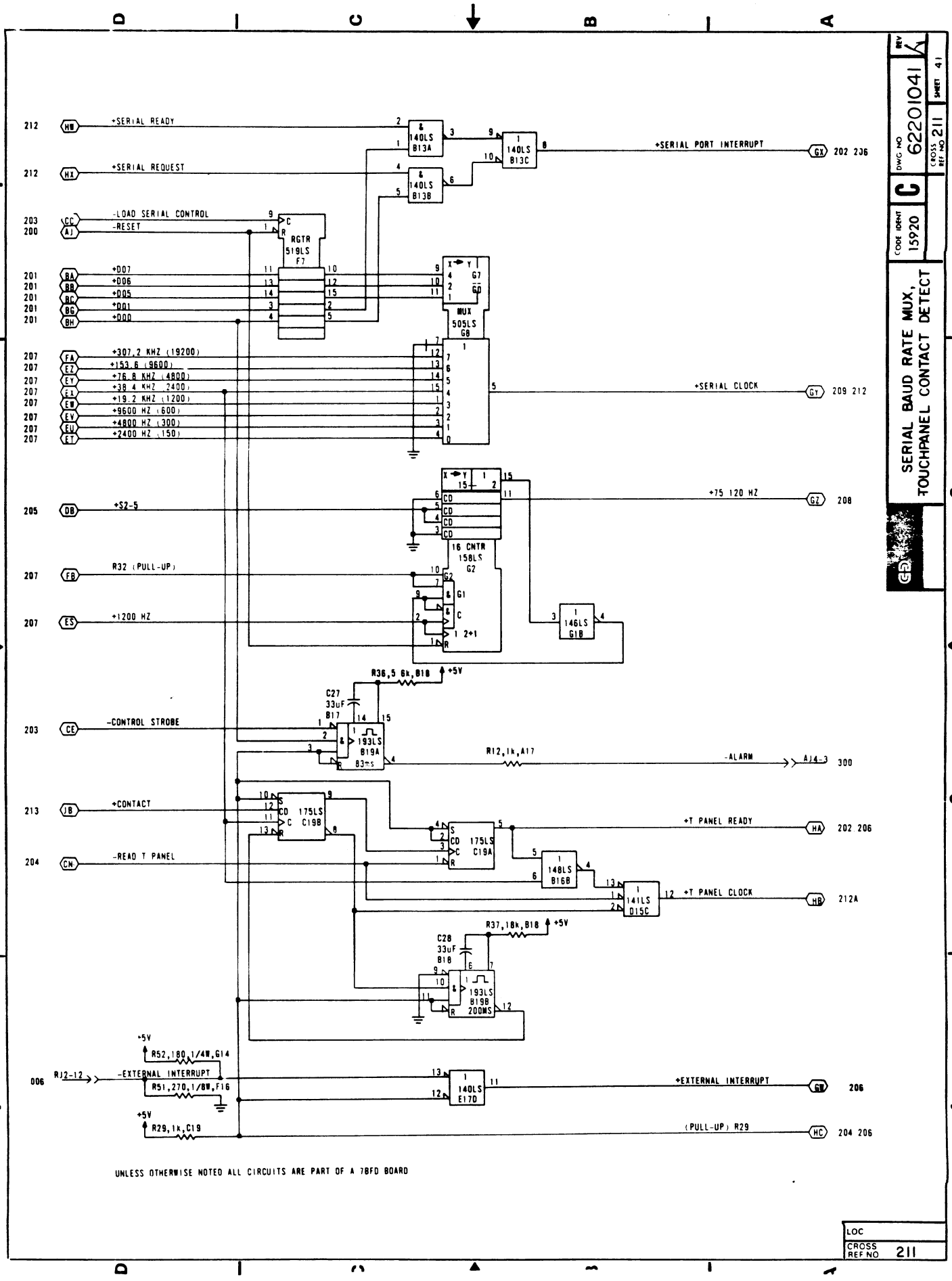

KEYBOARD SCANNER & CONTACT DETECTION LOGIC, INTERRUPT MASK RGTR & ENCODER
DWG. NO 62201041
REV F
CODE IDENT 15920
C
CROSS REF NO 206
SHEET 36
+KBD D5
+KBD D6
+KBD D4
+KBD D3
+KBD D2
+KBD D1
+KBD D0
16 CNTR 74LS393 B17
+RESET
+307.2 KHZ (19,200)
+5V
R30 12k C17
C26 1uF C17
-STROBE
R29 (PULL-UP)
193LS D18A
5.4ms
-READ KEYBOARD
-RESET
201LS G10C
143LS D16A
240LS D19B
+KBD READY
-LOAD INTERRUPT MASK
RGTR 74LS273 E3A
+D07
+D06
+D05
+D04
+D03
+D02
+D01
+D00
-CLR LONG INTERVAL
-CLR SHORT INTERVAL
140LS F4C
F4D
F4B
F3A
F3B
F3D
F3C
F4A
+LONG INTERVAL
+EXTERNAL INTERRUPT
+SHORT INTERVAL
+T PANEL READY
+COMMUNICATION REQUEST
+COMMUNICATION READY
+SERIAL PORT INTERRUPT
X MIN Y CODER 549LS
+INTERRUPT D2
+INTERRUPT D1
+INTERRUPT D0
-INTERRUPT
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78FD BOARD
LOC
CROSS REF NO 206

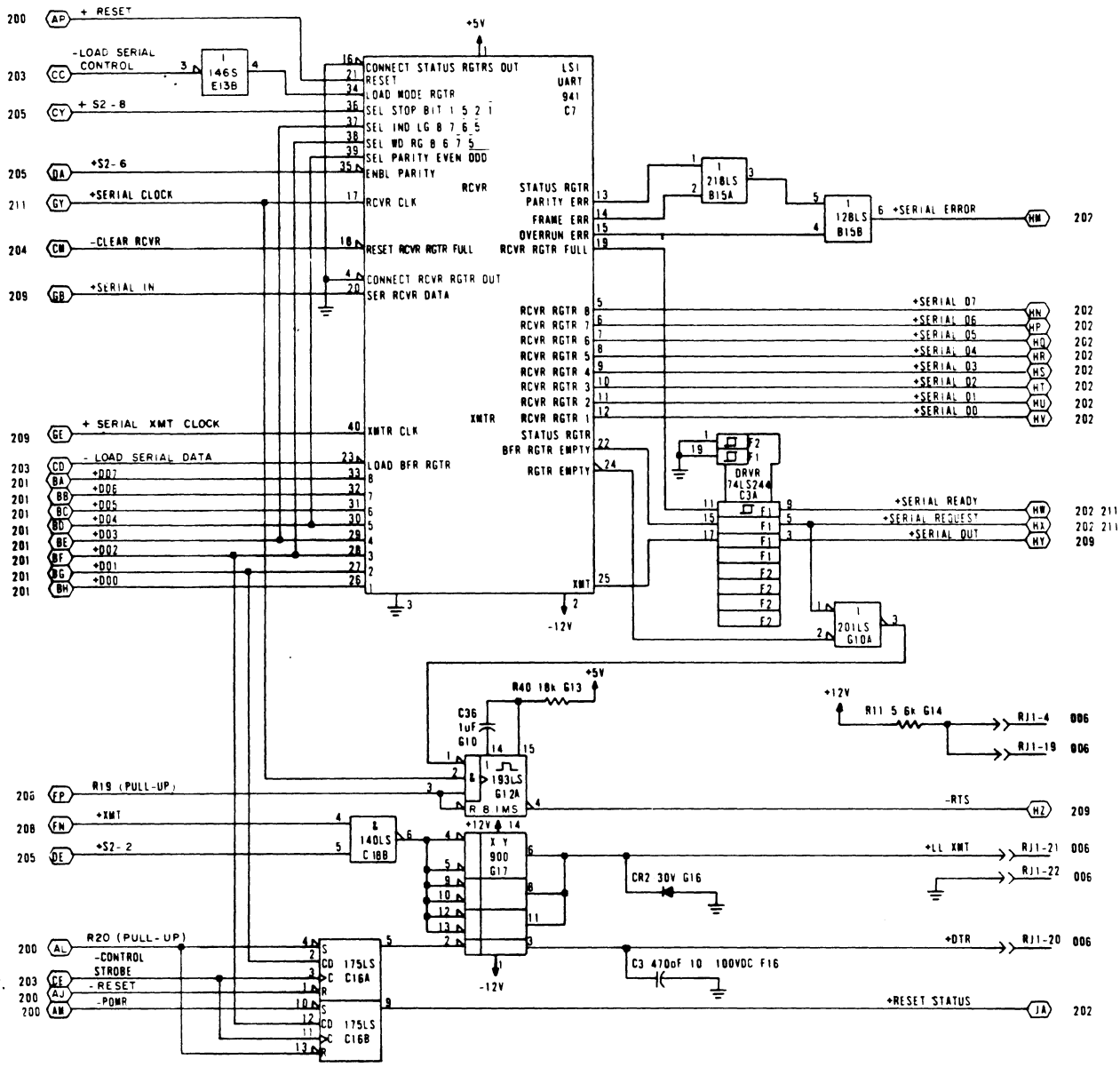

PLATO XMT SHIFT REGISTERS, SERIAL BAUD RATE GENERATION, INTERVAL TIMERS
CODE IDENT 15920
DWG NO 6220104
REV
SHEET 37
CROSS REF NO 207
+XMT CLOCK
-XMT ENABLE
-LOAD XMTR LO
SR-8 547LS F9
+D06
+D07
-LOAD XMTR HI
SR-8 547LS F8
+D00
+D01
+D02
+D03
+D04
+D05
+XMT DATA
-XMT DATA
+LONG INTERVAL
-CLR LONG INTERVAL
+SHORT INTERVAL
-CLR SHORT INTERVAL
CD 175LS C 69A
CD 175LS C 69B
+1200 HZ (75)
+2400 HZ (150)
+4800 HZ (300)
+9600 HZ (600)
16 CNTR 74LS393 G7
+RESET
+19.2 KHZ (1200)
+38.4 KHZ (2400)
+76.8 KHZ (4800)
+153.6 KHZ (9600)
16 CNTR 74LS393 G7
+307.2 KHZ (19,200)
16 CNTR 158LS G3
1 146LS G1C
+0
-RESET
+5V
R32 1k G2
(PULL-UP) R32
& 140LS B13D
-M1
-INTACK
RGTR 74LS374 C3B
+D07
+D06
+D05
+D04
+D03
+D02
+D01
+D00
+INTERRUPT 02
+INTERRUPT 01
+INTERRUPT 00
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78FD BOARD
LOC
CROSS REF NO 207

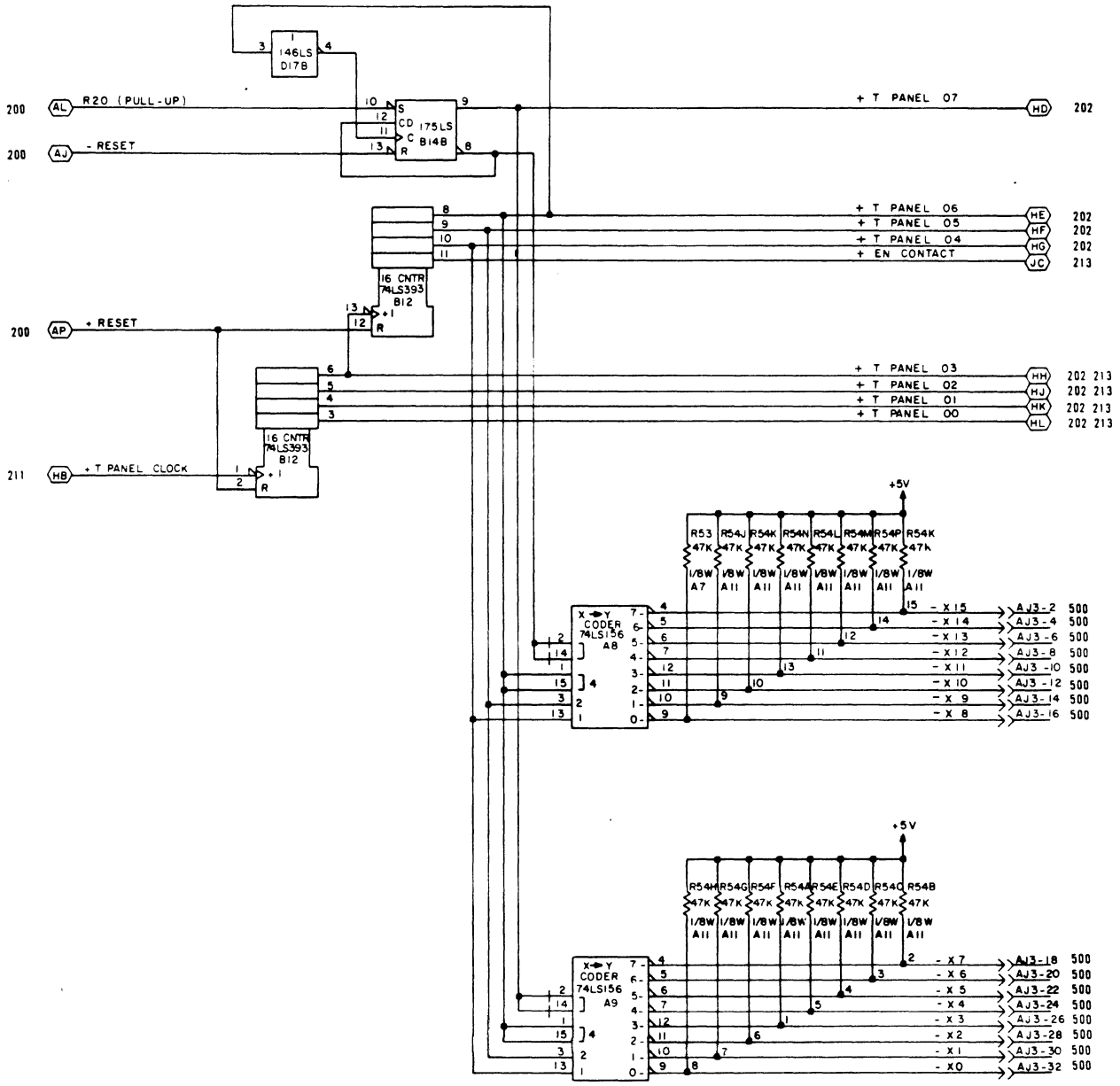

PLATO COMMUNICATIONS CONTROL
DWG NO 6220104 1
REV
SHEET 38
CROSS REF NO 208
CODE IDENT 15920
C
+S2-3
+S2-4
MUX 508LS F11
+EXT CLOCK
+1200 HZ (75)
+75 120 HZ
+TEST MODE
MUX 189LS F10
-RCV DATA
-XMT DATA
(PULL-UP) R32
+XMT DATA
-RCV DATA IN
-XMT
+XMT CLOCK
+XMT
+5V
R19 1k G5
(PULL-UP) R19
16 CNTR 500LS F12
-LOAD XMTR HI
-RESET
146S E13C
201LS F14D
CD 175LS F13A
CD 175LS F13B
201LS F14A
201LS F14C
-XMT ENABLE
+COMMUNICATION REQUEST
-RCV ENABLE
+LAST BIT
-DATA
R34 (PULL-UP)
+BYTE COUNT 01
1ST BYTE
GJ 240LS F19A
GJ 240LS F19B
+FIRST BYTE
-EDGE DETECT
CD 175LS E20B
-RCV CLOCK
+RCV CLOCK
+307.2 KHZ (19,200)
-CLOCK RESYNC
218LS E19A
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD
LOC
CROSS REF NO 208


LONG LINE RECEIVER, RS232 DRIVERS & RECEIVERS
DWG NO 6220104
REV
SHEET 39
CROSS REF NO 209
CODE IDENT 15920
-XMT
+XMT
+S2-7
-XMT DATA
+F XMT DATA
+B XMT DATA
NORM
TOGGLE SWITCH
TEST
+RCV DATA
+DSR
+XMT CLOCK
+CARRIER DET
-DSR
-PLATO CARRIER DETECT
+EXT CLOCK
+LL RCV
-LL RCV
-RCV DATA
+S2-2
+TEST MODE
+SERIAL OUT
R19 (PULL-UP)
-RTS
+S2-1
+RECEIVE
+CTS
+CARRIER DETECT
+SERIAL IN
+SEND
+RTS
+DTR
+SERIAL DSR
-SERIAL CARRIER DETECT
+SERIAL CLOCK
R20 (PULL-UP)
+SERIAL CTS
+SERIAL XMT CLOCK
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD
LOC
CROSS REF NO 209


PLATO RECEIVER LOGIC
DWG NO 6220104
REV
SHEET 40
CROSS REF NO 210
CODE IDENT 15920
+5V
R33,1k,G19
16 CNTR 158LS F16
207 FA +307.2 KHZ (19,200)
200 AJ -RESET
R34,1k,G19
(PULL-UP) R34 GF 208
-CLOCK RESYNC GG 208
146LS D17E
201LS F14B
16 CNTR 158LS F17
175LS F18A
218LS E19B
-EDGE DETECT GH 208
-DATA GJ 208
208 JB -RCV DATA IN
175LS F18B
208 FW +RCV CLOCK
SR-8 527LS F2
RGTR 74LS374 E3B
+D00 GK 201
+D01 GL 201
+D02 GM 201
+D03 GN 201
+D04 GP 201
+D05 GQ 201
+D06 GR 201
+D07 GS 201
203 BY -READ COMM LINE
208 FU +FIRST BYTE
R35 1k G19
140LS F17B
+COMMUNICATION READY GT 202,206
208 FV -RCV CLOCK
175LS E20A
16 CNTR 158LS G20
208 FS -RCV ENABLE
148LS B16C
+LAST BIT GU 208
+BYTE COUNT 01 GV 208
16 CNTR 158LS F20
208 FT +RCV ENABLE
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78FD BOARD
LOC
CROSS REF NO 210


SERIAL BAUD RATE MUX, TOUCHPANEL CONTACT DETECT
CODE IDENT 15920
DWG NO 62201041
REV K
SHEET 41
CROSS REF NO 211
+SERIAL READY
+SERIAL REQUEST
+SERIAL PORT INTERRUPT
-LOAD SERIAL CONTROL
-RESET
RGTR 519LS F7
+D07
+D06
+D05
+D01
+D00
MUX 505LS G8
+307.2 KHZ (19200)
+153.6 (9600)
+76.8 KHZ (4800)
+38.4 KHZ (2400)
+19.2 KHZ (1200)
+9600 HZ (600)
+4800 HZ (300)
+2400 HZ (150)
+SERIAL CLOCK
+S2-5
+75 120 HZ
16 CNTR 158LS G2
R32 (PULL-UP)
+1200 HZ
R36,5 6k,B18
+5V
C27 33uF B17
-CONTROL STROBE
193LS B19A 83ms
R12,1k,A17
-ALARM
+CONTACT
175LS C19B
175LS C19A
+T PANEL READY
-READ T PANEL
148LS B16B
141LS D15C
+T PANEL CLOCK
R37,18k,B18
C28 33uF B18
193LS B19B 200MS
R52,180,1/4W,G14
-EXTERNAL INTERRUPT
R51,270,1/8W,F16
140LS E17D
+EXTERNAL INTERRUPT
R29,1k,C19
(PULL-UP) R29
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78FD BOARD
LOC
CROSS REF NO 211

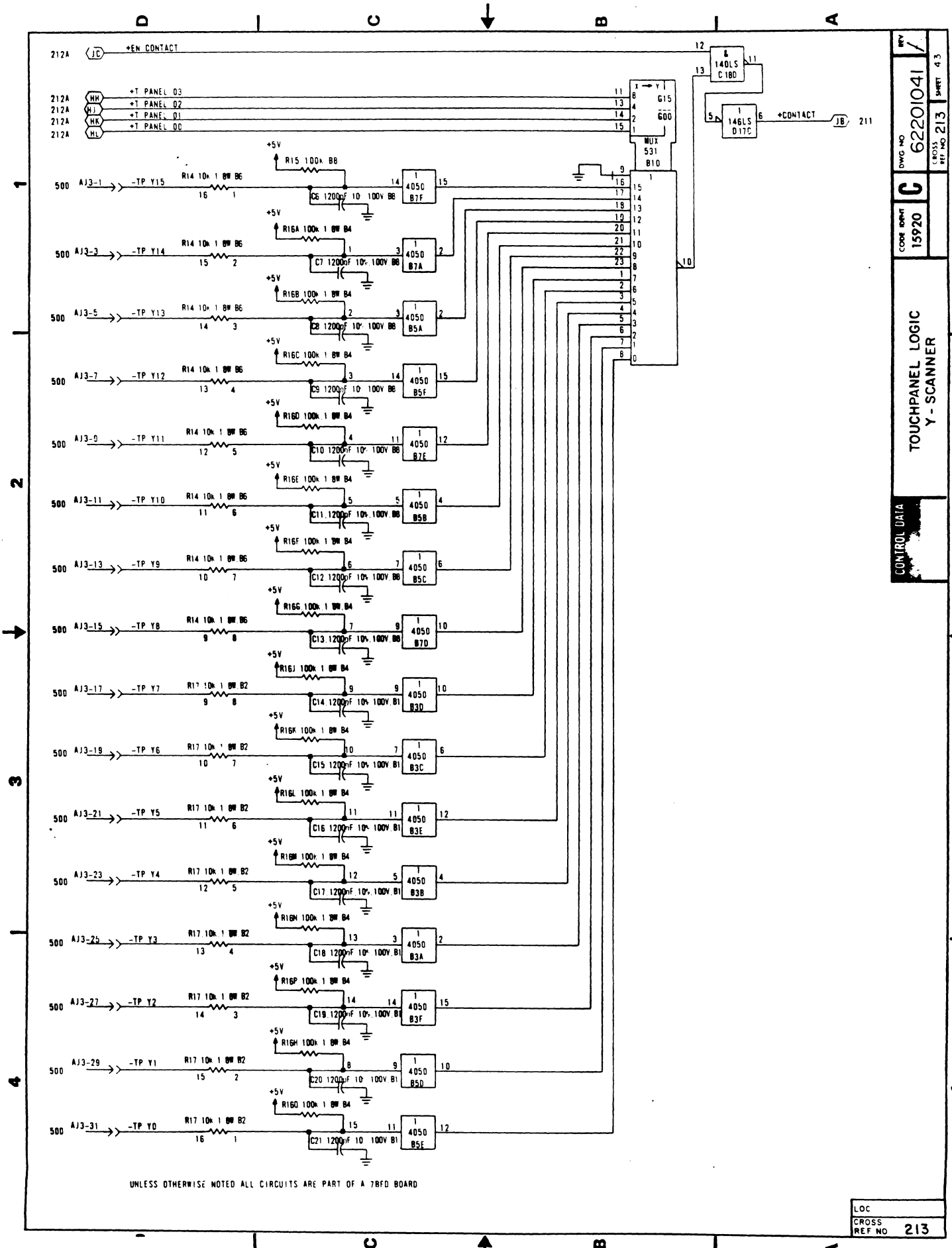

SERIAL CHANNEL UART, LONG LINE DRIVER
DWG NO 6220104 1
REV
SHEET 42
CROSS REF NO 212
CODE IDENT 15920
C
+ RESET
-LOAD SERIAL CONTROL
+ S2 - 8
+S2- 6
+SERIAL CLOCK
-CLEAR RCVR
+SERIAL IN
+ SERIAL XMT CLOCK
- LOAD SERIAL DATA
+DD7
+DD6
+DD5
+DD4
+DD3
+DD2
+DD1
+DD0
CONNECT STATUS RGTRS OUT
RESET
LOAD MODE RGTR
SEL STOP BIT 1 5 2 1
SEL IND LG 8 7 6 5
SEL WD RG 8 6 7 5
SEL PARITY EVEN ODD
ENBL PARITY
RCVR CLK
RESET RCVR RGTR FULL
CONNECT RCVR RGTR OUT
SER RCVR DATA
XMTR CLK
LOAD BFR RGTR
LSI UART 941 C7
RCVR
XMTR
STATUS RGTR PARITY ERR
FRAME ERR
OVERRUN ERR
RCVR RGTR FULL
RCVR RGTR 8
RCVR RGTR 7
RCVR RGTR 6
RCVR RGTR 5
RCVR RGTR 4
RCVR RGTR 3
RCVR RGTR 2
RCVR RGTR 1
STATUS RGTR
BFR RGTR EMPTY
RGTR EMPTY
XMT
+5V
-12V
+SERIAL ERROR
+SERIAL D7
+SERIAL D6
+SERIAL D5
+SERIAL D4
+SERIAL D3
+SERIAL D2
+SERIAL D1
+SERIAL D0
+SERIAL READY
+SERIAL REQUEST
+SERIAL OUT
DRVR 74LS244 C3A
R40 10k G13
C36 1uF G10
R19 (PULL-UP)
+XMT
+S2- 2
R20 (PULL-UP)
-CONTROL STROBE
- RESET
-PWR
R11 5.6k G14
-RTS
+LL XMT
CR2 30V G16
+DTR
C3 470pF 10 100VDC F16
+RESET STATUS
RJ11-4
RJ11-19
RJ11-21
RJ11-22
RJ11-20
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78FD BOARD
LOC
CROSS REF NO 212

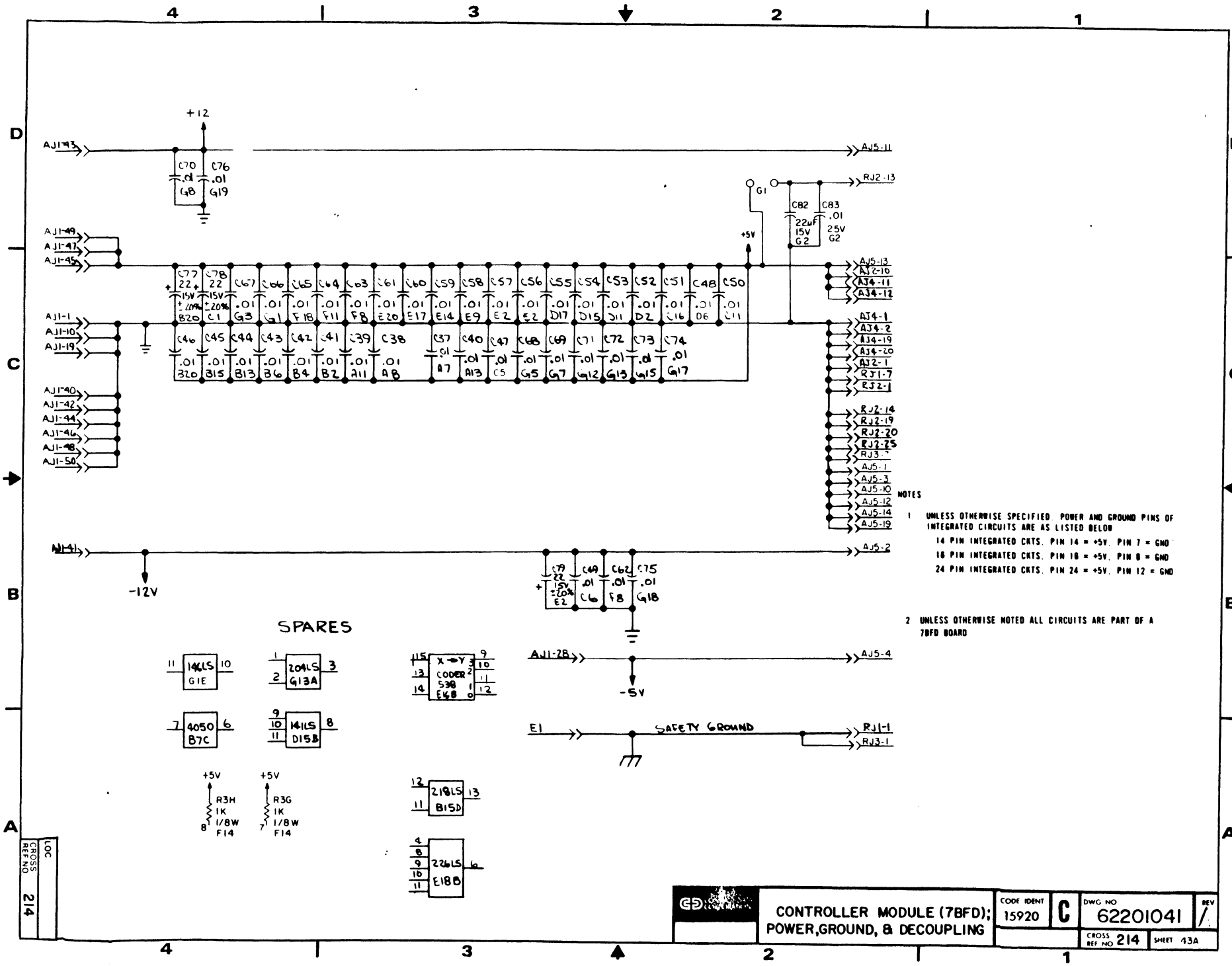


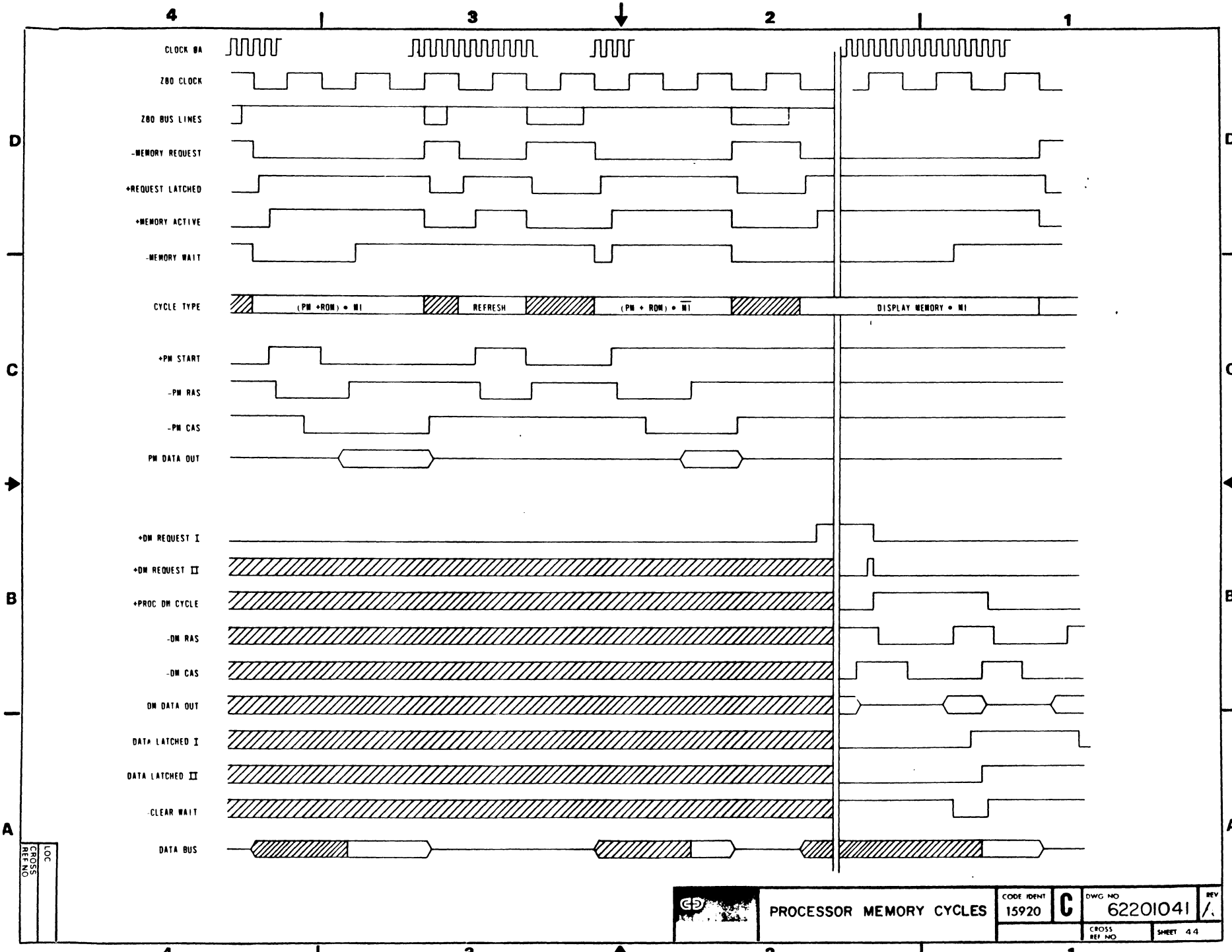
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 78FD BOARD

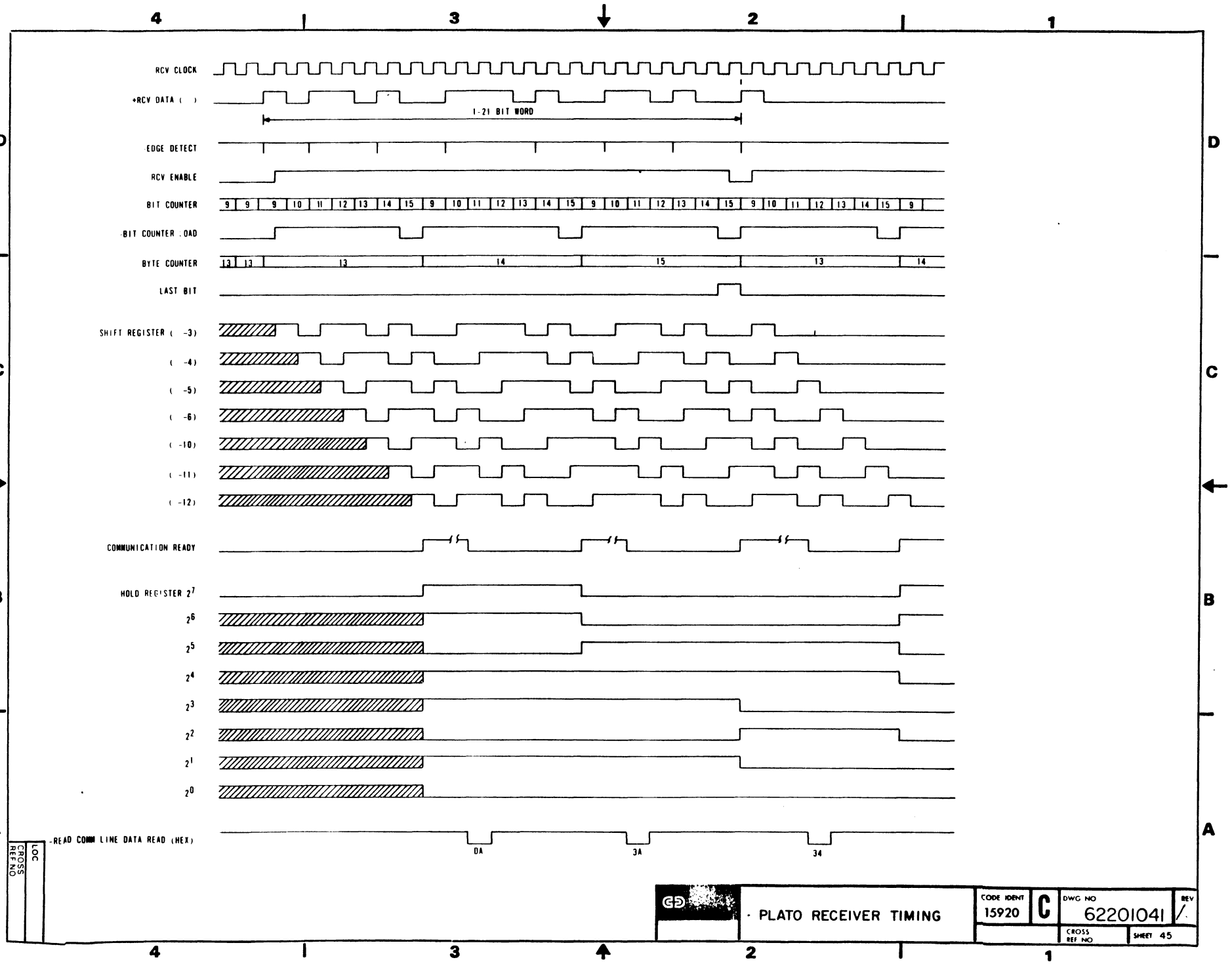
REV /
DWG NO 62201041
SHEET 42A
CROSS REF NO 212A
CODE IDENT 15920
C
TOUCHPANEL LOGIC
X - SCANNER

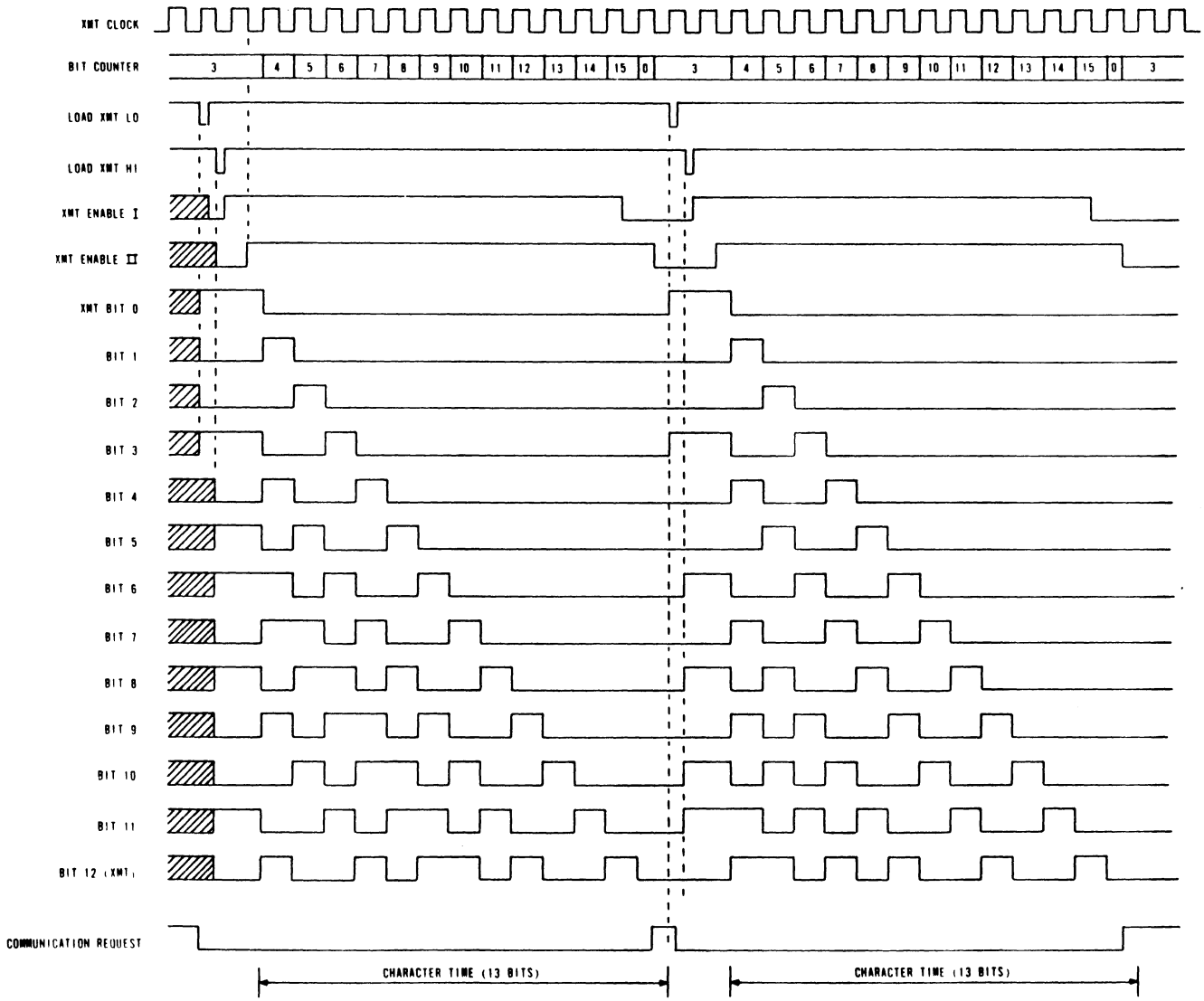
LOC
CROSS REF NO 212A


+EN CONTACT
+T PANEL 03
+T PANEL 02
+T PANEL 01
+T PANEL 00
+CONTACT
MUX 531 B10
TOUCHPANEL LOGIC Y-SCANNER
CONTROL DATA
DWG NO 62201041
CODE IDENT 15920
CROSS REF NO 213
SHEET 4.3
REV
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD
LOC
CROSS REF NO 213


+12
AJ1-43
C70 .01 G8
C76 .01 G19
AJ5-11
RJ2-13
G1
C82 22uF 15V G2
C83 .01 25V G2
+5V
AJ1-49
AJ1-47
AJ1-45
C77 22 15V ±20% B20
C78 22 15V ±20% C1
C67 .01 G3
C66 .01 G1
C65 .01 F18
C64 .01 F11
C63 .01 F8
C61 .01 E20
C60 .01 E17
C59 .01 E14
C58 .01 E9
C57 .01 E2
C56 .01 E2
C55 .01 D17
C54 .01 D15
C53 .01 D11
C52 .01 D2
C51 .01 C16
C48 .01 D6
C50 .01 C11
AJ5-13
AJ2-10
AJ4-11
AJ4-12
AJ1-1
AJ1-10
AJ1-19
C46 .01 B20
C45 .01 B15
C44 .01 B13
C43 .01 B6
C42 .01 B4
C41 .01 B2
C39 .01 A11
C38 .01 A8
C37 .01 A7
C40 .01 A13
C47 .01 C5
C68 .01 G5
C69 .01 G7
C71 .01 G12
C72 .01 G13
C73 .01 G15
C74 .01 G17
AJ4-1
AJ4-2
AJ4-19
AJ4-20
AJ2-1
RJ1-7
RJ2-1
AJ1-40
AJ1-42
AJ1-44
AJ1-46
AJ1-48
AJ1-50
RJ2-14
RJ2-19
RJ2-20
RJ2-25
RJ3-7
AJ5-1
AJ5-3
AJ5-10
AJ5-12
AJ5-14
AJ5-19
NOTES
1 UNLESS OTHERWISE SPECIFIED. POWER AND GROUND PINS OF INTEGRATED CIRCUITS ARE AS LISTED BELOW
14 PIN INTEGRATED CKTS. PIN 14 = +5V. PIN 7 = GND
16 PIN INTEGRATED CKTS. PIN 16 = +5V. PIN 8 = GND
24 PIN INTEGRATED CKTS. PIN 24 = +5V. PIN 12 = GND
2 UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BFD BOARD
AJ1-91
-12V
AJ5-2
C79 22 15V ±20% E2
C49 .01 C6
C62 .01 F8
C75 .01 G18
SPARES
14LS G1E
204LS G13A
X→Y CODER 538 E4B
AJ1-28
AJ5-4
-5V
4050 B7C
14LS D15B
E1
SAFETY GROUND
RJ1-1
RJ3-1
+5V
R3H 1K 1/8W F14
+5V
R3G 1K 1/8W F14
219LS B15D
226LS E18B
LOC
CROSS REF NO
214
5-48
82100083
CONTROLLER MODULE (7BFD); POWER, GROUND, & DECOUPLING
CODE IDENT 15920
C
DWG NO 62201041
REV /
CROSS REF NO 214
SHEET 43A

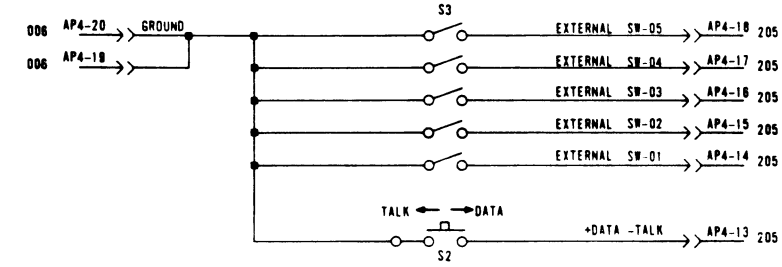

4
3
2
1
CLOCK 8A
Z80 CLOCK
Z80 BUS LINES
-MEMORY REQUEST
+REQUEST LATCHED
+MEMORY ACTIVE
-MEMORY WAIT
CYCLE TYPE
(PM +ROM) • MI
REFRESH
(PM + ROM) • MI
DISPLAY MEMORY • MI
+PM START
-PM RAS
-PM CAS
PM DATA OUT
+DM REQUEST I
+DM REQUEST II
+PROC DM CYCLE
-DM RAS
-DM CAS
DM DATA OUT
DATA LATCHED I
DATA LATCHED II
-CLEAR WAIT
DATA BUS
D
C
B
A
LOC
CROSS REF NO.
PROCESSOR MEMORY CYCLES
CODE IDENT 15920
C
DWG NO 62201041
REV /.
CROSS REF NO
SHEET 44

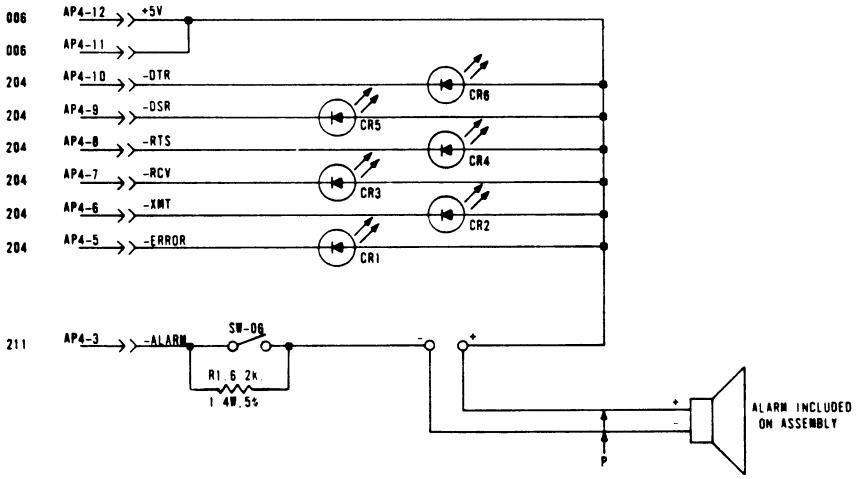

RCV CLOCK
+RCV DATA ( )
1-21 BIT WORD
EDGE DETECT
RCV ENABLE
BIT COUNTER
BIT COUNTER LOAD
BYTE COUNTER
LAST BIT
SHIFT REGISTER (-3)
(-4)
(-5)
(-6)
(-10)
(-11)
(-12)
COMMUNICATION READY
HOLD REGISTER 2^7
2^6
2^5
2^4
2^3
2^2
2^1
2^0
-READ COMM LINE DATA READ (HEX)
DA
3A
34
CROSS REF NO
LOC
PLATO RECEIVER TIMING
CODE IDENT 15920
C
DWG NO 62201041
REV
CROSS REF NO
SHEET 45

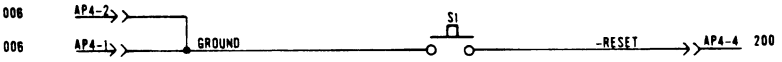


LOC
CROSS REF NO.

	PLATO TRANSMITTER TIMING	CODE IDENT 15920	C	DWG NO 62201041 / REV
		CROSS REF NO		SHEET 46





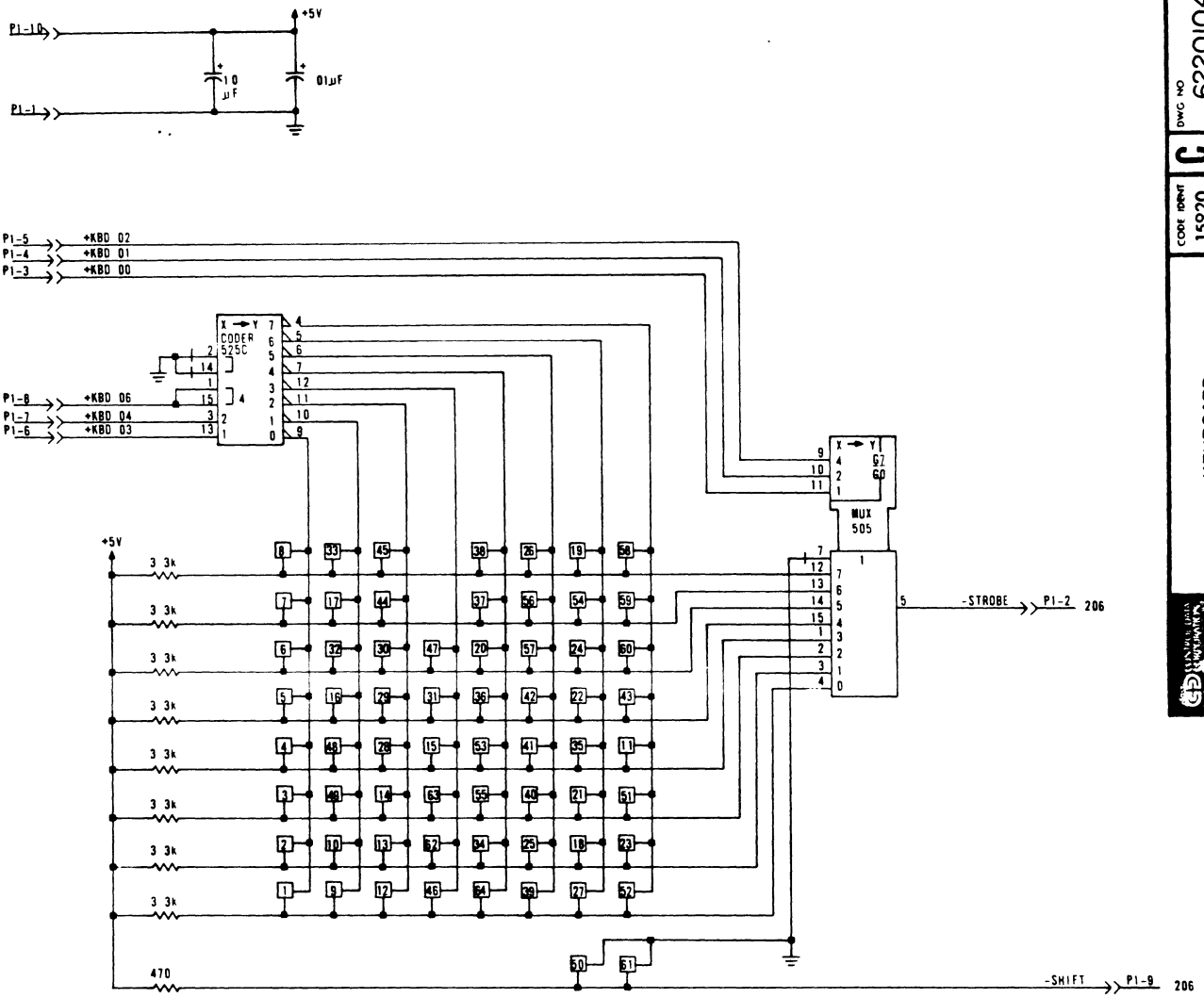


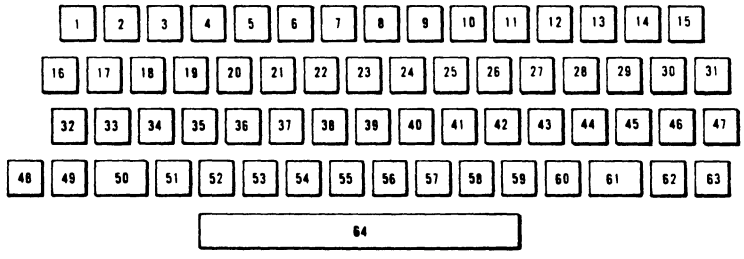
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 7BVD BOARD

OPERATOR'S PANEL (7BVD)

CODE IDENT 15920 | C | DWG NO 62201041 | REV | CROSS REF NO 300 | SHEET 47

LOC
CROSS REF NO 300





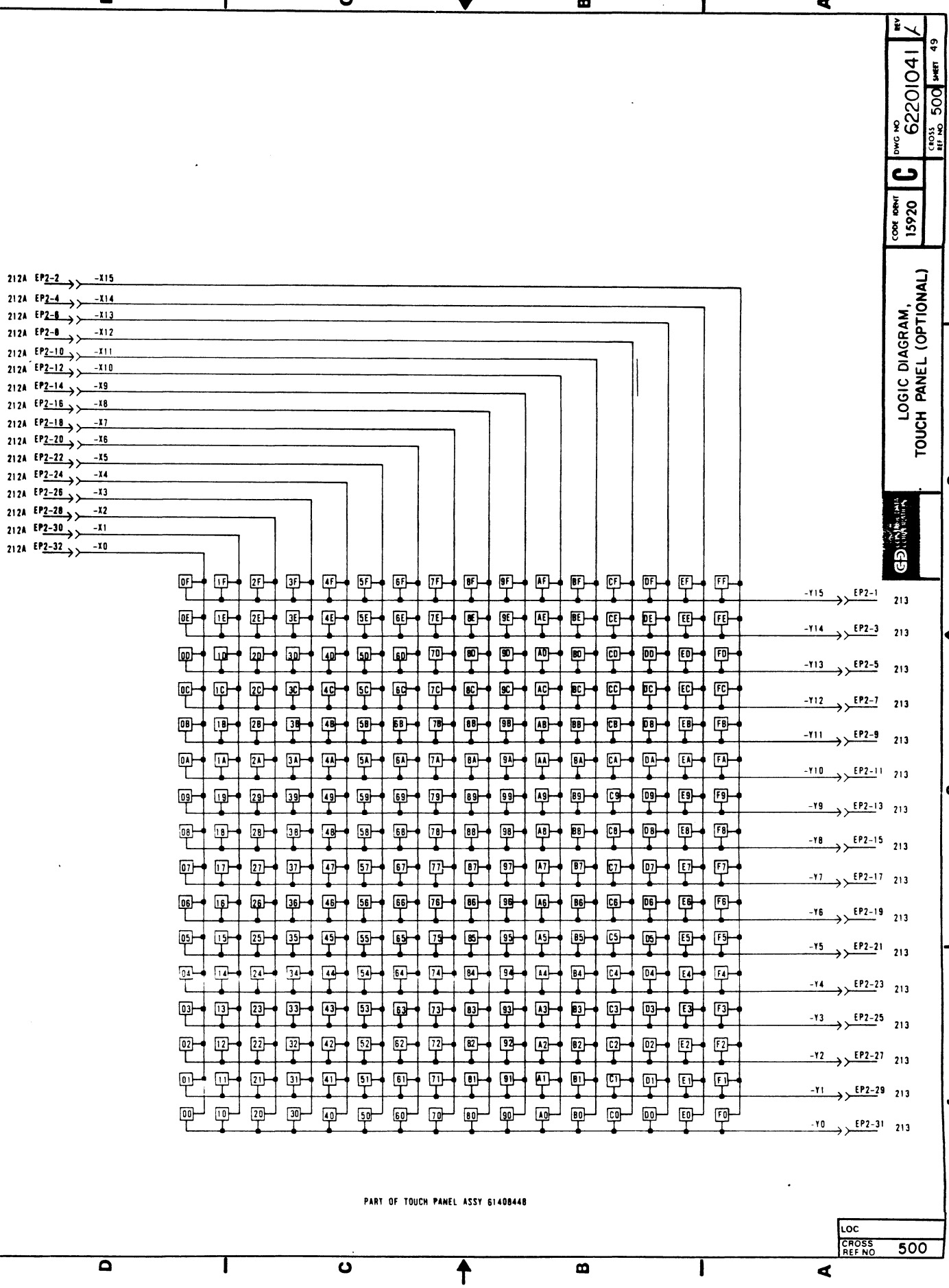
KEY NUMBER ASSIGNMENT

PART OF KEYBOARD ASSY 51918093

CODE IDENT 15920 | DWG NO 62201041 | REV / | SHEET 48 | CROSS REF NO 400

KEYBOARD

LOC
CROSS REF NO 400

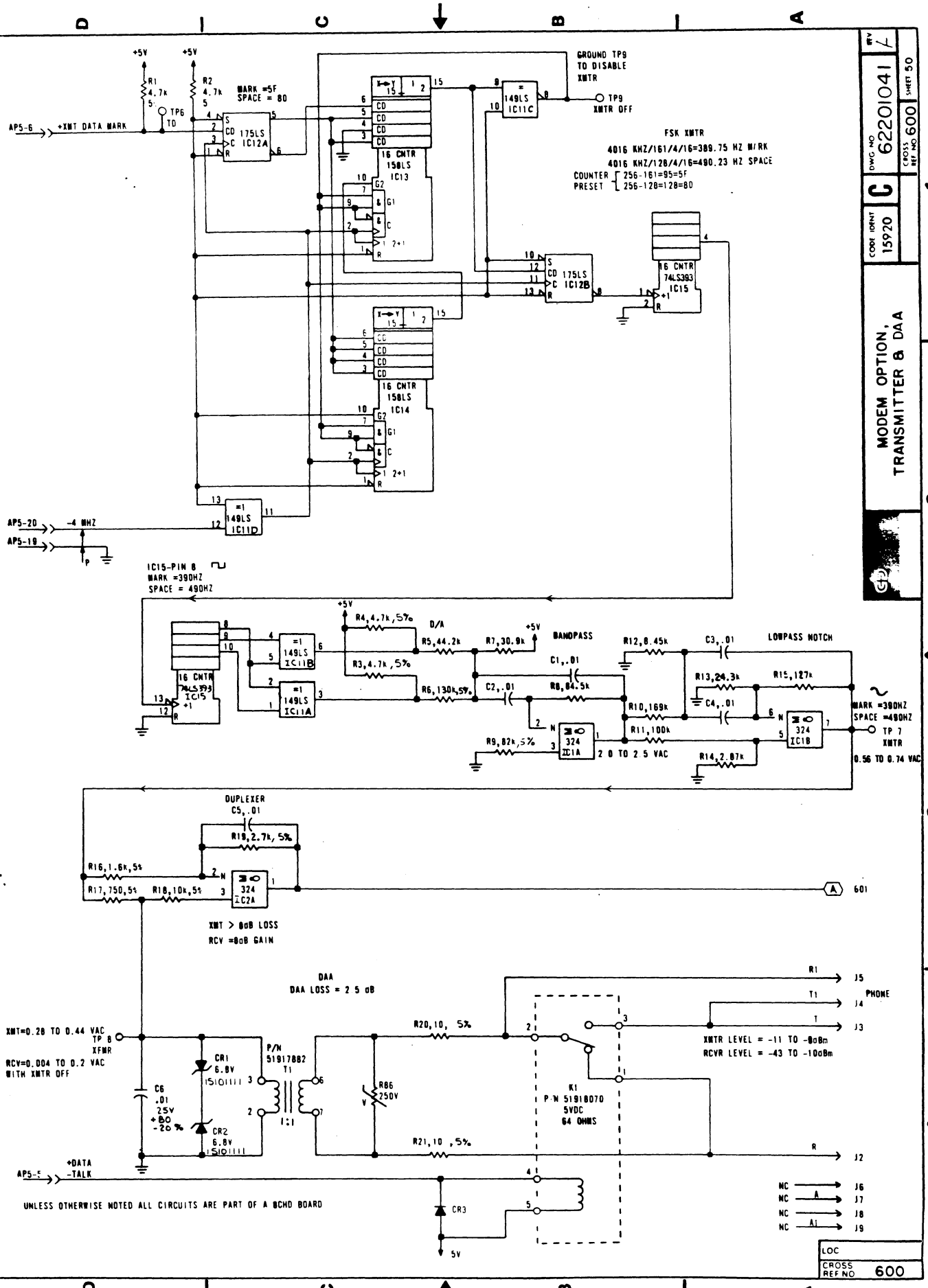


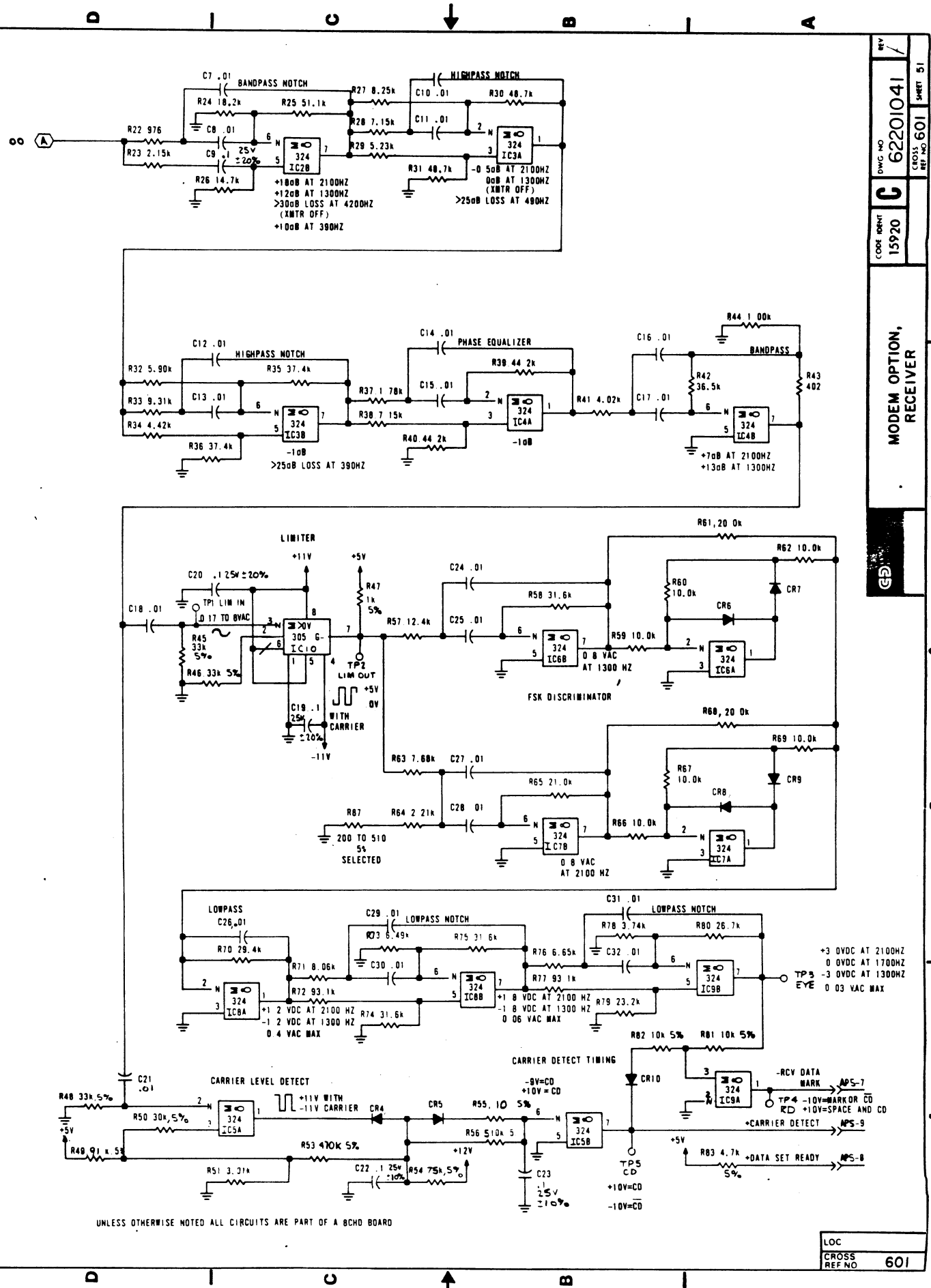
CODE IDENT 15920 | C | DWG NO 62201041 | REV L | CROSS REF NO 500 | SHEET 49

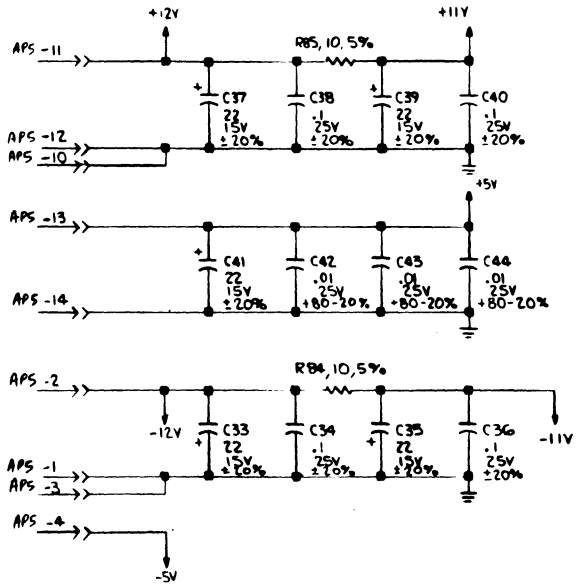
LOGIC DIAGRAM, TOUCH PANEL (OPTIONAL)

PART OF TOUCH PANEL ASSY 61408448

LOC
CROSS REF NO 500


MODEM OPTION, TRANSMITTER & DAA
CODE IDENT 15920
DWG NO 62201041
REV C
SHEET 50
CROSS REF NO 600
FSK XMTR
4016 KHZ/16/4/16=389.75 HZ MRK
4016 KHZ/128/4/16=490.23 HZ SPACE
COUNTER PRESET 256-161=95=5F
256-128=128=80
MARK =5F
SPACE = 80
GROUND TP9 TO DISABLE XMTR
TP9 XMTR OFF
AP5-6 +XMT DATA MARK
AP5-20 4 MHZ
AP5-19
IC15-PIN 8
MARK =390HZ
SPACE = 490HZ
BANDPASS
LOWPASS NOTCH
MARK =390HZ
SPACE =490HZ
TP 7 XMTR
0.56 TO 0.74 VAC
2.0 TO 2.5 VAC
DUPLEXER
XMT > 8dB LOSS
RCV =8dB GAIN
DAA
DAA LOSS = 2.5 dB
XMT=0.28 TO 0.44 VAC
TP 8 XFMR
RCV=0.004 TO 0.2 VAC WITH XMTR OFF
P/N 51917882 T1
K1 P/N 51918070 5VDC 64 OHMS
XMTR LEVEL = -11 TO -8dBm
RCVR LEVEL = -43 TO -10dBm
PHONE
+DATA -TALK
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 8CHD BOARD
LOC
CROSS REF NO 600


MODEM OPTION, RECEIVER
DWG NO 62201041
CODE IDENT 15920
CROSS REF NO 601
SHEET 51
REV
BANDPASS NOTCH
HIGHPASS NOTCH
PHASE EQUALIZER
BANDPASS
LIMITER
FSK DISCRIMINATOR
LOWPASS
LOWPASS NOTCH
CARRIER LEVEL DETECT
CARRIER DETECT TIMING
+18dB AT 2100HZ
+12dB AT 1300HZ
>30dB LOSS AT 4200HZ
(XMTR OFF)
+10dB AT 390HZ
-0 5dB AT 2100HZ
0dB AT 1300HZ
(XMTR OFF)
>25dB LOSS AT 490HZ
-1dB
>25dB LOSS AT 390HZ
+7dB AT 2100HZ
+13dB AT 1300HZ
0 8 VAC AT 1300 HZ
0 8 VAC AT 2100 HZ
200 TO 510 5% SELECTED
+1 2 VDC AT 2100 HZ
-1 2 VDC AT 1300 HZ
0 4 VAC MAX
+1 8 VDC AT 2100 HZ
-1 8 VDC AT 1300 HZ
0 06 VAC MAX
+3 0VDC AT 2100HZ
0 0VDC AT 1700HZ
-3 0VDC AT 1300HZ
0 03 VAC MAX
+11V WITH -11V CARRIER
-9V=CD +10V=CD
+10V=CD
-10V=CD
-RCV DATA MARK
+CARRIER DETECT
+DATA SET READY
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 8CHD BOARD
LOC
CROSS REF NO 601



NOTES

1. UNLESS OTHERWISE SPECIFIED, POWER AND GROUND PINS OF INTEGRATED CIRCUITS ARE AS LISTED BELOW
   - 14 PIN INTEGRATED CKTS. PIN 14 = +5V, PIN 7 = GND
   - 16 PIN INTEGRATED CKTS. PIN 16 = +5V, PIN 8 = GND
   - 8 PIN INTEGRATED CKTS. PIN 8 = +5V, PIN 4 = GND
2. UNLESS OTHERWISE NOTED ALL DIODES TO BE P/N S100385.
3. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A BCHP BOARD

	MODEM OPTION; POWER, GROUND, & DECOUPLING	CODE IDENT 15920	C	DWG NO 62201041	REV /
				CROSS REF NO 602	SHEET 52

LOC CROSS REF NO 602

This section provides information necessary to perform field maintenance on the terminal subsystem. Information is organized under the following major headings:

- Suggested Emergency Maintenance Procedure -- describes a suggested approach to emergency maintenance (field maintenance).
- Maintenance Aids -- describes the diagnostics available to troubleshoot the terminal.
- Preventive Maintenance -- describes minor preventive maintenance tasks and related procedures.
- Special Tools and Test Equipment -- describes special items required for terminal maintenance.
- MOS Circuit Handling Precautions -- describes special procedures to be used when replacing MOS circuits.
- Diagnostic and Corrective Maintenance Procedures -- describes procedures to be used to diagnose and correct a malfunction.

Diagnostic decision logic tables (DDLTs) are used to identify malfunctions in the terminal subsystem. These tables use a logical process of elimination to trace a malfunction to a field replaceable part, and the part is then replaced. This type of table is described in greater detail later in this section.

SUGGESTED EMERGENCY MAINTENANCE PROCEDURE

The following procedure provides suggested steps for the customer engineer (CE) to follow when responding to a customer request for maintenance on the terminal.

BEFORE LEAVING FOR CUSTOMER SITE

Before leaving for the customer site, the CE should call the customer and talk to the person operating the terminal at the time the malfunction occurred, then:

1. Determine the following:

   a. Specific configuration of terminal; for example, does terminal use a touchpanel and/or an internal modem.

   b. Type of symptoms terminal exhibited to indicate that a malfunction occurred.

   c. Whether terminal is operating and what symptoms, if any, are present when an attempt is made to operate.

2. Decide course of action to take, for example:

   a. Go to customer site and begin troubleshooting.

   b. Deduce that terminal itself is probably not at fault and most likely cause of problem is either communication lines or a power reduction or loss. In either case, CE can notify responsible party (common carrier or customer) of problem.

   c. Decide that an error in operating procedure rather then equipment failure is probably cause of malfunction, and notify customer of correct operating procedure.

3. If a site maintenance trip is required, CE should try to determine a probable cause for failure and gather necessary tools, manuals, and spare parts that may be needed.

UPON ARRIVING AT CUSTOMER SITE

Upon arriving at the customer site, the CE should locate the appropriate supervisory personnel and again talk to the terminal operator concerning the malfunction, then:

1. Visually inspect terminal to ensure that correct input/output and power cable connections exist.

2. Verify that a malfunction does exist, and then begin to troubleshoot terminal.

3. After source of malfunction is corrected, CE should:

   a. Run terminal diagnostics explained later in this section to ensure that terminal is operational.

b. Perform preventive maintenance tasks listed in this section.

c. Demonstrate to customer that terminal is now operating properly within system.

MAINTENANCE AIDS

Resident diagnostics provide error indications of basic hardware faults. A system diagnostic lesson (DIAG) provides additional tests.

RESIDENT DIAGNOSTICS

To run the terminal resident diagnostics, the TEST/SKIP, KB/TP/SKIP, and/or LOOP/EXIT rocker switches must be used. These switches are behind the protective door on the front of the terminal. See section 2 for definitions of each switch. Procedure 2 describes how to run these diagnostics.

As the RAM test is run, the terminal displays a pattern of white vertical lines written from right to left across the crt. If the crt alignment/keyboard touchpanel test is selected, the test concludes with the alignment pattern being displayed.

The terminal resident diagnostic program consists of three sections. These sections test the random access memory (RAM), the PLATO serial interface, the external serial interface, the crt alignment, keyboard, and the touchpanel.

RAM Memory Test

This test includes writing, reading, and verifying the following data patterns:

- Write/read 55 hexadecimal code in all memory locations above $08FF_{16}$.
- Write/read AA hexadecimal code in all memory locations above $08FF_{16}$.
- Clear all memory locations above $08FF_{16}$. Write a data pattern into a test address, and read all

memory to ensure that it was written into the desired address only.

Serial Interface Tests

These tests check the PLATO and external serial interfaces.

PLATO Serial Interface Test

This test checks that the status and control lines of the PLATO interface are functioning properly and checks that data is transmitted and received correctly. The following conditions are tested:

- Character request status is present.
- Character request status does not drop after low order bits are output to the interface.
- Character request status drops after the high order bits are output to the interface.
- First byte flag is set.
- Start bit is present.
- Character ready status is present.

External Serial Interface Test

This test checks that the control and status lines of the external serial interface are functioning properly and checks that data is transmitted and received correctly at 9600 bps, using the internal loopback feature. The following conditions are tested:

- Character request status present.
- Character read status present.

CRT Alignment, Touchpanel, and Keyboard Tests

This section consists of three test segments. These are an alignment pattern, a touchpanel test, and a keyboard test.

The alignment pattern consists of four lines outlining the screen border with two diagonal lines intersecting at screen center. Pattern is used to check for correct crt alignment and touchpanel installation.

The touchpanel has 256 touch sensitive areas. Touching any one of these areas causes the crt pattern of that area to be displayed in inverse video. Repeated touches cause repeated inversions.

The keyboard portion of this test displays upon the screen a binary representation of the hexadecimal code received from the keyboard. These keyboard codes are defined in the IST-II Hardware Maintenance Manual. This binary representation is made up of long bars (binary 1s) and short bars (binary 0s) with the bottom bar being the lowest order bit. Refer to procedure 2 later in this section for additional information.

Diagnostic Error Indication

When an error is detected, the alarm sounds and an error code displays in the LED indicators on the front panel of the terminal. The following octal error codes display, where the ERR LED represents the 2^0 bit:

Code	Cause of Error
01	Memory error writing/reading 55_{16} pattern
02	Memory error writing/reading AA_{16} pattern
03	Memory error due to addressing problem
04	PLATO serial interface error
05	External serial interface error
06	Keyboard/touchpanel test in progress

For error codes 01 and 02, pressing any key provides a second level LED indication. The second level is the chip number where the error was first detected (figure 6-1).

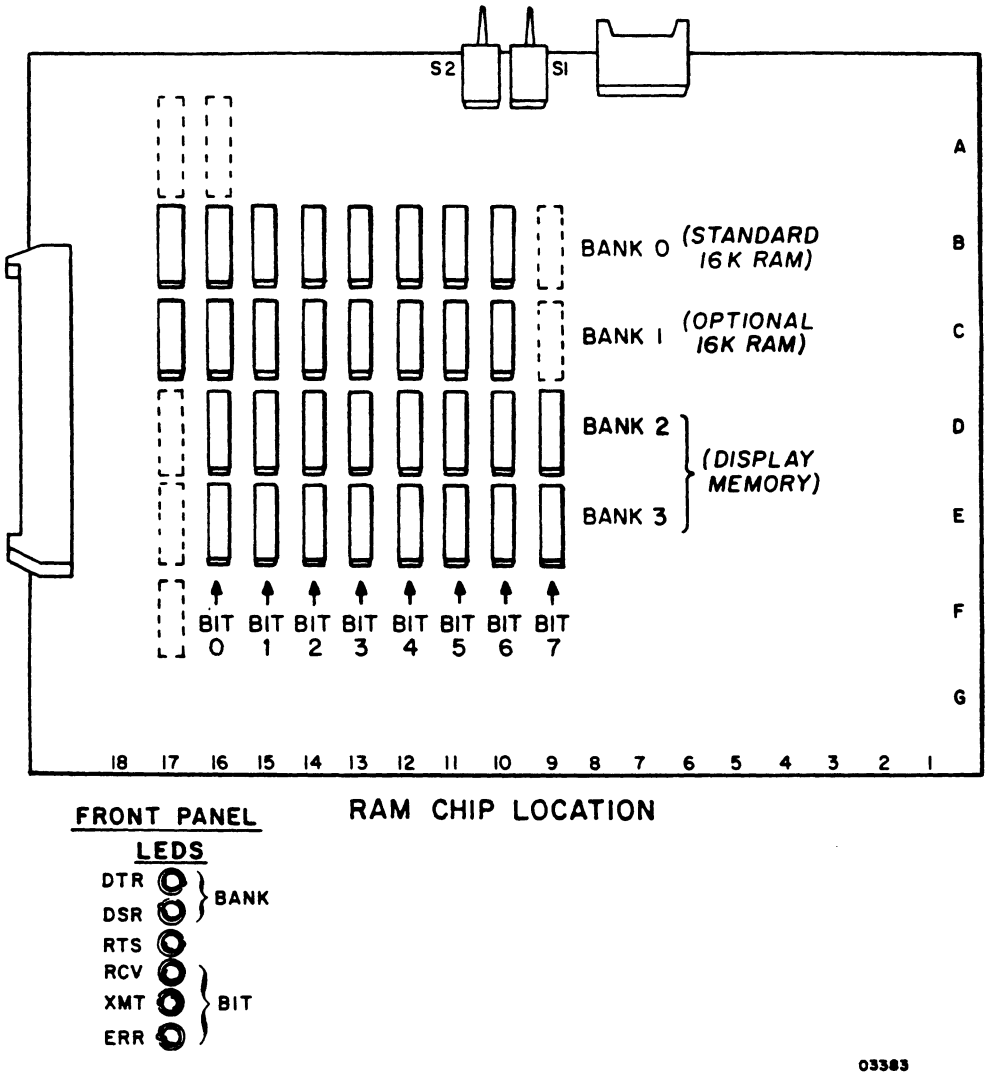


Figure 6-1. RAM Chip Locations

For error codes 04 and 05, pressing any key provides a second level of indication. The second level for an 04 error is as follows:

Code	Description
01	No character request status

02	Character request dropped after output of lower bits
03	Character request active after output of upper bits
04	First byte flag not set
05	Start bit not received
06	No character ready status
07	Data error

The second level for an 05 error (serial transmission error) is as follows:

Code	Description
01	No character request
02	No character ready
03	Data error

SYSTEM DIAGNOSTIC LESSON (DIAG)

The system diagnostic lesson DIAG can be used to troubleshoot a faulty terminal. DIAG provides diagnostics to exercise the PLATO terminal. Some of the available options are a pattern test, character tests, and a keyboard/touchpanel test. DIAG can be used with any terminal.

The user can access lesson DIAG by typing the word diag on the welcome page, pressing the NEXT key, typing m on the group name page, and pressing the SHIFT and STOP keys simultaneously. A list of the available tests will be displayed at the beginning of the lesson.

PREVENTIVE MAINTENANCE

Preventive maintenance should be performed immediately following and as a part of an emergency maintenance call. The following suggested preventive maintenance steps help to minimize maintenance calls by verifying correct crt

alignment and related operations of the terminal. General inspection of the terminal, including proper seating of cable connectors, should also be made. Procedures referred to in text are found after the DDLTs in this section.

Remove power from terminal (procedure 1) and clean as follows:

CAUTION

Do not use solvents to clean keyboard. Solvent can cause defective keyswitch operation.

1. Dust keyboard with soft-bristled brush.
2. Clean touchpanel in front of crt screen using a soft cloth dampened with a mild soap and water solution. Apply cleaning agent to cloth (avoid splashing on crt screen or keyboard) to prevent the cleaning agent from entering behind the bezel.
3. Wipe exterior of the terminal cabinets using a damp lint-free cloth.

Reapply terminal power (procedure 1) and verify correct crt alignment as follows:

4. Set KB-TP/SKIP rocker switch on operator panel to KB-TP. Set TEST/SKIP switch to TEST. Press RESET switch.
5. Check for correct alignment and acceptable display quality (refer to procedure 23). If required perform related adjustments per procedure 5.
6. Return KB-TP/SKIP and TEST/SKIP rocker switches to SKIP.

SPECIAL TOOLS AND TEST EQUIPMENT

In addition to the normal complement of hand tools and test equipment carried by the field CE, maintenance of this terminal requires a special tuning wand tool (CDC Part Number 12263476) when performing adjustments on the power supply and display boards. A plastic keyswitch insertion tool (CDC Part Number 51919702) is required for work on the

keyboards. Also, a chip removal tool (CDC Part Number 87365900) is required. To perform adjustments on the monitor board use a hex adjustment tool (Part Number 12263299) and the special tuning wand previously mentioned. It is recommended that the hook be snipped off the hex tool prior to its use to prevent it from locking into the inductor slug.

MOS CIRCUIT HANDLING PRECAUTIONS

The control and video boards contain a number of MOS (metal-oxide semiconductor) integrated circuits. The MOS circuits are susceptible to irreparable damage if they are exposed to excessive static electricity and thus require special handling. Follow the precautions listed here at all times when handling the PC board.

- Never insert, remove, or otherwise connect/disconnect any circuit(s) while primary power is applied.

WARNING

To prevent accidental shock when observing static-grounding precautions, do not touch powered-on electrical equipment and chassis frame at the same time.

- Before touching (with hands and/or tool) or handling any circuit, connector cable, or logic backpanel, always touch hand(s) (and/or tool) to an exposed portion of the associated chassis frame to discharge any buildup of static electricity.

- Especially in dry ambient air, any movement may cause static electricity buildup due to friction. In the case of shuffling one's feet across a dry carpet, such static buildup may be quite high and may easily jump from a cable connector being held onto the pins being mated to. This could damage the MOS circuits within the equipment. Thus, the chassis frame must always be touched immediately before connecting any cable to it.

- When removing, replacing, or otherwise handling any assembly/module that contains MOS circuits, do not touch circuit paths or conductors if at all possible. Do not carry a MOS circuit assembly across a room while touching its circuits.

- When a module is removed from its chassis and placed where it may be touched, carried to some other

location, or if it is to be shipped, wrap the module in static protective material, such as aluminum foil or conductive foam.

DIAGNOSTIC AND CORRECTIVE MAINTENANCE PROCEDURES

This portion of the text concentrates on diagnostic and corrective maintenance. Diagnostic maintenance provides an organized means of diagnosing a malfunction and of identifying its source. Corrective maintenance consists of the procedures for correcting a diagnosed malfunction and of those procedures used to verify that the malfunction has been corrected. It uses the diagnostic decision logic tables and the procedures in this section to efficiently diagnose and correct a malfunction.

DIAGNOSTIC DECISION LOGIC TABLES

The key to isolating a terminal malfunction to its probable cause is proper use of the diagnostic tables that follow. These tables, termed diagnostic decision logic tables (DDLTs), or decision tables, identify and isolate a malfunction in an equipment to a replaceable module; or where equipment design does not permit this approach, to a replaceable part or component. The tables present test setup and resulting symptom information in a logical, organized manner; and where necessary, they refer to procedures for testing, adjusting, or replacing a suspected component. References to procedures are also made in a sequenced manner so they refer to the most likely cause first or easiest procedure and progress to the least likely cause, or most difficult procedure.

The following paragraphs describe the decision tables in greater detail. Anyone not familiar with the format and structure of diagnostic decision logic tables should read the following paragraphs and study the sample table in figure 6-2 carefully before attempting to use the decision tables later in this section. Also, anyone using decision tables for the first time should always start at the beginning of the tables and continue through to the end.

The diagnostic decision logic table is a specialized format for displaying logic in a way that is superior to the conventional logic flowchart because the logic is more visible. The DDLT analyzes a situation down to a set of

specific conditions and then directs the customer engineer to those actions that will correct the situation. Basically, the table is arranged in four sections, or quadrants: conditions, situations, sequence, and actions. Figure 6-2 illustrates the layout of a diagnostic decision logic table; the sample table is for illustration purposes only and is not a table for this terminal.

Conditions Quadrant

The conditions quadrant of a DDLT contains test conditions and questions that can be answered with either a yes or no. The CE should read and answer all of the questions in the conditions quadrant and write the answers to each question (Y or N) in a vertical column before proceeding to the situations column.

Situations Quadrant

The situations quadrant of the example table contains 10 vertical columns of Ys and/or Ns, and one column with the word Other in it. Each of the first 10 columns represents a unique set of answers to the questions asked in the conditions quadrant. A hyphen (-) in a column indicates that the answer to the associated condition is irrelevant; that is, the answer may be either a yes or a no without affecting the result. In using the tables, the CE should look for a match between the Y and N column written down while answering the questions posed in the conditions quadrant and the Y and N answers listed in a column of the situations quadrant.

As an example, refer to the shaded area of the sample figure and assume that each question in the conditions quadrant was answered no (N) as it was tested. The full column of N answers to the conditions questions would actually match situations column 2 even though situations column 2 contains three hyphens. This is true because the hyphens indicate that their respective conditions questions are irrelevant. As can be seen by examining the conditions questions, it is indeed irrelevant to ask which indicators light or which motors run if it is already known that no indicators light and no motors run.
When using the tables, look for a match between the answers to the conditions and the situations columns starting from the left situation column and moving toward the right one. Do this because overriding situations are normally listed

VISUAL CHECKS

ASSUME

Card-reader power cord is connected to ac outlet. Power is on. If power is not on, see procedure 1.

CONDITIONS	SITUATIONS										
	1	2	3	4	5	6	7	8	9	10	11
Is POWER ON indicator illuminated?	Y	N	N	N	Y	Y	Y	Y	Y	Y	OTHER
Cycle rear-panel toggle switch S1. Press READ CHECK indicator/switch. Do all other indicators illuminate?	Y	N	N	Y	N	N	Y	Y	Y	Y	
Do any indicators illuminate?	-	N	N	-	N	Y	-	-	-	-	
Press and release RESET indicator/switch. Is RESET indicator illuminated?	Y	-	-	-	-	-	N	Y	Y	Y	
Do all three motors start when RESET indicator/switch is pressed (observe card-feed drum and coils of stacker motors)?	Y	-	-	-	-	-	-	N	N	Y	
Do any motors start?	-	N	Y	-	-	-	-	Y	N	-	
Did motor power drop within 10 to 30 seconds after releasing RESET indicator/switch?	Y	-	-	-	-	-	-	-	-	N	

ACTIONS	SEQUENCE										
Go to sheet 2, Electromechanical Checks.	X	-	-	-	-	-	-	-	-	-	-
Check that toggle switch S1 (rear panel) is up.	-	1	-	-	-	-	-	-	-	-	-
Check that removable power cord is connected securely to card reader.	-	2	-	-	-	-	-	-	-	-	-
Check fuses (rear panel).	-	3	-	-	-	-	-	-	-	-	-
Check switch board and associated cabling (procedure 40). Replace, if required (procedure 41).	-	4	-	2	2	2	3	-	-	-	-
Refer to CB10X manual.	-	5	4	4	3	4	5	3	3	3	-
Check +17-volt power supply (procedure 36).	-	-	1	-	-	-	-	-	-	-	-
Check for +17-V dc between ground and control-board connector P2, pins 2 and 3 and between ground and switch board connector, pins 2 and 3 (two pins joined by foil).	-	-	2	-	-	-	-	-	-	-	-
Check cable between control board and switch board.	-	-	3	-	-	-	-	-	-	-	-
Replace lamp in failing indicator (procedure 41).	-	-	-	1	-	1	-	-	-	-	-
Check failing indicator and/or switch (procedure 40) and replace, if required (procedure 41).	-	-	-	3	-	3	-	-	-	-	-
Check READ CHECK indicator/switch (procedure 40) and replace, if required (procedure 41).	-	-	-	-	1	-	-	-	-	-	-
Check +5-volt power supply (procedure 35).	-	-	-	-	-	-	1	-	-	-	-
Check RESET indicator/switch (procedure 40) and replace, if required (procedure 41).	-	-	-	-	-	-	2	-	-	-	-
Replace control board (procedure 44).	-	-	-	-	-	-	4	-	2	2	-
Check for ac power at motor connectors (procedure 37).	-	-	-	-	-	-	-	1	-	-	-
Check failing motor. Replace motor, if required (procedure 46 for card-feed motor, or procedure 47 for card-stacker motor).	-	-	-	-	-	-	-	2	-	-	-
Check common cable connections to motors.	-	-	-	-	-	-	-	-	1	-	-
Check that T0 switch (control board) has labeled side, T0, up.	-	-	-	-	-	-	-	-	-	1	-
Call for assistance.	-	-	-	-	-	-	-	-	-	-	X

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Figure 6-2. Example of a Diagnostic Decision Logic Table

first (on the left) within the situations quadrant. Overriding situations are those that move the user out of the table and onto the next test, table, or action.

Sequence Quadrant

The sequence quadrant contains numbers that indicate the sequence in which corrective actions are to be taken. The sequence of actions for a particular set of conditions appears in the same vertical column as the situations column that matches the conditions. For example, the sample figure shows the sequence 1, 2, 3, 4, and 5 directly under the situations column. These sequence numbers indicate that the first action to be taken is check that toggle switch S1 (rear panel) is up; the next action to be taken is, check that removable power cord is connected securely to card reader; and the last action to be taken (5) is, refer to CB10X manual. The sequence of actions normally selects either the easiest procedure or most likely cause first and progresses to the most difficult procedure or least likely cause.

In the figure 6-2, also notice that some of the sequence columns contain only an X. The X indicates that there is only one possible action to take. As an example, the X in the situation 11, or Other column of the sample table, indicates that the only action available is to call for assistance. The Other term in the situation 11 column indicates that none of the previous situations match the answer written down for the conditions questions.

Actions Quadrant

The actions quadrant lists specific actions that the CE is to take in the process of troubleshooting an equipment. The actions listed are taken in the order listed in the sequence quadrant.

Notice that either the conditions or the actions quadrants can direct the CE to perform specific procedures. A condition, for example could direct the CE to run a particular checkout procedure before asking a question about the results (yes or no answer) of the checkout procedure. An action, on the other hand, could direct a CE to perform a checkout procedure, perform an adjustment or remove-and-replace procedure, exit this table and go to another table, or to call for assistance in troubleshooting the malfunction.

To facilitate locating the corrective action procedures that are part of this section, an index at the end of this section lists all of the corrective action procedures and their respective page numbers.

ARRANGEMENT OF DIAGNOSTIC AND CORRECTIVE MAINTENANCE INFORMATION

The arrangement of the diagnostic and corrective maintenance information is shown in figure 6-3.

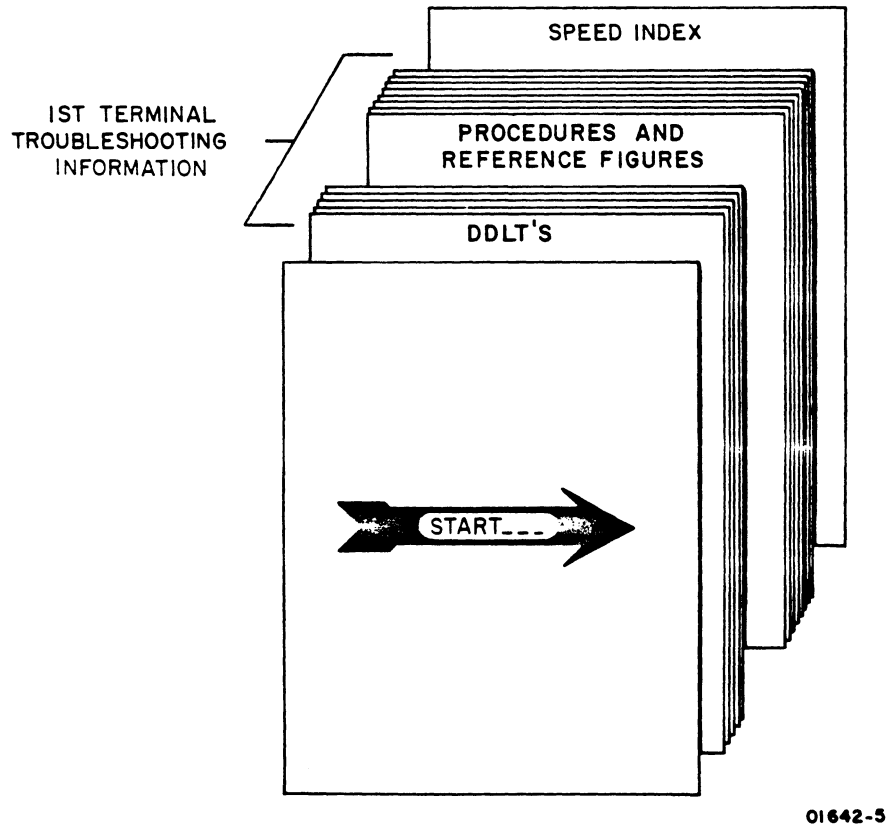


Figure 6-3. Arrangement of Diagnostic and Corrective Maintenance Information

WARNING

LETHAL VOLTAGES EXIST IN THE CRT ASSEMBLY. USE EXTREME CAUTION WHEN PERFORMING INTERNAL ADJUSTMENTS OR SEVERE PERSONAL INJURY OR LOSS OF LIFE MAY RESULT.

NOTE

If you are unfamiliar with DDLTs, read the explanation of their use described earlier in this section. Then, start at the beginning of the tables and work through to the end of the section, ensuring that all malfunctions detected are corrected. If a table pertains to equipments or functions not present in a particular terminal configuration, skip to the following table or tables and continue in this manner until all applicable tables are completed.

CAUTION

Because many of the circuits used in this system are of the MOS integrated circuit type, always observe the rules for handling MOS type circuits as described earlier in this section. Failure to do so can result in these circuits being destroyed by an excessive discharge of static electricity.

TABLE CRT1. DDLT FOR DISPLAY TERMINAL

POWER FAULTS

ASSUME

Power applied per procedure 1.

Note - LED's will light with voltage present, however the voltage may not be correct. Refer to procedure 9 to check/adjust voltages.

CONDITIONS	SITUATIONS 1	2	3	4	5	6
Does ON/OFF switch trip when set to ON?	Y	N	N	N	N	OTHER
Is there complete absence of power on J1-2 of the power supply?	-	Y	N	N	N	
Are any (or all) power supply board LEDs unlit?	-	-	Y	N	N	
Does video or raster fail to display on crt?	-	-	-	-	Y	

ACTIONS	SEQUENCE					
Check ac power cord and whether site power is available.	-	1	-	-	-	-
Replace ac entry assembly (procedure 11) if line filter pin 4 has no voltage.	-	3	-	-	-	-
Replace power supply board (procedure 10)	2	-	2	-	-	-
Replace power ON/OFF switch (procedure 12)	3	4	-	-	-	-
Check internal cable connections for shorts and/or damage.	1	2	1	-	-	-
Go to table CRT2 and do No Video, No Raster checks.	-	-	-	-	X	-
Problem not covered in manual. Call for assistance.	-	-	-	-	-	X
Perform power supply voltage check/adjust (procedure 9). Replace power supply board (procedure 10) if unable to adjust or if voltages are incorrect.	-	-	-	X	-	-

TABLE CRT2. DDLT FOR DISPLAY TERMINAL

NO VIDEO, NO RASTER

ASSUME

Terminal power on (and present) per procedure 1 and BRIGHTNESS control turned to maximum and no raster.

CONDITIONS	SITUATIONS 1	2	3	4	5	6	7
Is +55-V indicator lit on power supply?	N	Y	Y	Y	Y	Y	O
Is fuse okay on display PC board?	-	N	Y	Y	Y	Y	T
Is LED lit on display PC board?	-	-	N	Y	Y	Y	H
Is crt filament lit?	-	-	-	N	Y	Y	E
Is +55 V present on display board (procedure 9)?	-	-	-	-	N	Y	R
ACTIONS	**SEQUENCE**						
Check display PC board connector, connector to power supply board, and yoke connector.	-	-	1	1	1	-	-
Check +55 V on display board (procedure 9). If measurement is less than +55 V, replace power supply board (procedure 10).	-	-	2	2	-	-	-
Replace Doubler/Bleeder assembly (procedure 19).	-	-	-	-	-	1	-
Replace power supply board (procedure 10) only if other LEDs on power supply are lit. If none are lit, go to table CRT1 (power faults).	X	-	-	-	2	-	-
Replace display PC board (procedure 18).	-	2	3	3	-	2	-
Replace crt/yoke (procedure 18).	-	-	-	4	-	3	-
Replace fuse.	-	1	-	-	-	-	-
Problem not covered in manual. Call for assistance.	-	-	-	-	-	-	X

TABLE CRT3. DDLT FOR DISPLAY TERMINAL

VIDEO AND RASTER PROBLEMS (GENERAL)

ASSUME

Terminal power on per procedure 1. Resident diagnostics ran without error.

CONDITIONS	SITUATIONS 1	2	3	4	5	6	7	8
Did resident diagnostics run OK?	N	Y	Y	Y	Y	Y	Y	OTHER
Adjust BRIGHTNESS control. Is alignment pattern present?	-	N	Y	N	N	N	N	
Is alignment pattern distorted or incorrect?	-	-	Y	-	-	-	-	
Turn BRIGHTNESS control to maximum. Is raster present?	-	N	-	Y	Y	Y	Y	
Is video present?	-	-	-	N	Y	Y	Y	
Force video output to white state with Flood Screen switch (procedure 22). Is entire screen illuminated?	-	-	-	-	N	Y	Y	
Load memory with ones and zeros (procedure 22). Does crt respond?	-	-	-	-	-	Y	N	
Are ones and zero displayed correctly? (No picked or dropped bits.)	-	-	-	-	-	N	-	

ACTIONS	SEQUENCE							
Go to table CRT4.	X	-	-	-	-	-	-	-
Perform crt alignment checks and adjustments if necessary (procedure 5).	-	-	1	-	-	-	-	-
Check internal connectors.	-	-	-	1	1	1	1	-
Replace chip 74S05 on display board (procedure 8).	-	-	-	2		-	-	-
Replace video board (procedure 7).	-	-	3	3	2	3	2	-
Go to table CRT2 and do No Video, No Raster checks.	-	X	-	-	3	-	-	-
Run internal diagnostics (procedure 2) and replace bad RAM chip (procedure 8).	-	-	-	-	-	2	-	-
Replace display board (procedure 18).	-	-	2	4	-	-	-	-
Problem not covered in manual. Call for assistance.	-	-	-	-	-	-	-	X

TABLE CRT 4. DDLT FOR DISPLAY TERMINAL

RESIDENT DIAGNOSTIC ERRORS

ASSUME

Internal configuration/mode switches set correctly (see section 2 of this manual). Resident diagnostics executed per procedure 2 and an error condition occurs. All voltage LEDs lit. Error codes are displayed on operator panel.

CONDITIONS	SITUATIONS										
	1	2	3	4	5	6	7	8	9	10	11
Error code 01 or 02 with beep?	Y	N	N	N	N	N	N	N	-	N	
Error code 03 with beep?	-	Y	N	N	N	N	N	N	-	N	
Error code 04 with beep?	-	-	Y	N	N	N	N	N	-	N	O
Error code 05 with beep?	-	-	-	Y	N	N	N	N	-	N	T
No error code, invalid error code, error code with no beep, or diagnostics will not start?	-	-	-	-	Y	Y	N	N	N	N	H
Are any power supply LEDs unlit?	-	-	-	-	Y	N	N	N	N	N	E
Code 06 (keyboard/touchpanel test)?	-	-	-	-	-	-	Y	Y	Y	N	R
Keyboard code incorrect or no response?*	-	-	-	-	-	-	Y	N	N	N	
Touchpanel test does not cause crt patterns to invert or no response?**	-	-	-	-	-	-	-	Y	N	N	

ACTIONS	SEQUENCE										
Press any keyboard key to get second level indication (procedure 2)	1	1	1	1	-	-	-	-	-	-	-
Replace RAM chip on video board as indicated by diagnostics (procedure 8).	2	-	-	-	-	-	-	-	-	-	-
Replace TR1602A UART chip on controller board (procedure 8).	-	-	-	3	-	-	-	-	-	-	-
Replace video board (procedure 7).	3	2	-	-	-	3	-	-	-	-	-
Replace controller board (procedure 7).	4	3	3	4	-	2	3	2	-	-	-
Replace keyboard assembly or faulty keyswitch (procedure 13).	-	-	-	-	-	-	2	-	-	-	-
Replace touchpanel (procedure 20).	-	-	-	-	-	-	-	3	-	-	-
Check all internal and external connectors for loose connections, shorts, opens or reversed cables.	-	-	2	2	-	1	1	1	-	-	-
Keyboard/touchpanel tests are OK.	-	-	-	-	-	-	-	-	X	-	-
Resident diagnostics ran OK.	-	-	-	-	-	-	-	-	-	X	-
Go to CRT1 and do power fault checks.	-	-	-	-	X	-	-	-	-	-	-
Problem not covered in manual. Call for assistance.	-	-	-	-	-	-	-	-	-	-	X

*To check for a shorted keyswitch, hold "0" key depressed and reset or power on terminal. Wait for keyboard/touchpanel to display, then release "0" key. Keycode of shorted switch displays on crt.

**A shorted touchpanel beeps and displays the shorted spot during power up and a long reset. A short reset indicates the touchpanel pattern only and not the shorted area.

TABLE CRT5. DDLT FOR DISPLAY TERMINAL

UNABLE TO ESTABLISH COMMUNICATION WITH CENTRAL SITE					
ASSUME Internal and external configuration/mode switches set correctly (see section 2 of this manual). Resident diagnostics ran without error. Central computer is in operation.					
CONDITIONS	SITUATIONS 1	2	3	4	5
"NOP" message displayed?	Y	-	-	-	OTHER
"NO REPLY" message displayed?	-	Y	Y	-	
Transmit indicator flashes every few seconds?	-	Y	N	-	
"LOADING FAILURE" message displayed.	-	-	-	Y	
ACTIONS	SEQUENCE				
Press RESET switch three seconds or longer and check that all LEDs on operator's panel light. If not, replace operator panel (procedure 13). Terminal tries to autoload.	1	1	1	1	-
Check communication cable hookup.	5	-	-	-	-
Check internal connectors	6	-	2	-	-
If internal modem used: 1) Check setting of DATA/TALK switch. 2) Check hookup (procedure 21).	3	-	-	-	-
Replace controller board (procedure 7).	8	5	4	4	-
Replace internal modem, if used (procedure 21).	7	4	3	-	-
Check external communication device(s).	4	3	-	2	-
System is down. Wait a few minutes and try again.	-	-	-	-	-
Verify that terminal is being dialed to an active (connected) system	2	-	-	-	-
Replace video board (procedure 7).	-	-	-	3	-
Verify that PLATO system is operational.	-	2	-	-	-
Problem not covered in manual. Call for assistance.	-	-	-	-	X

Procedure 1 - Turning On/Off Terminal

To apply input ac power to the terminal:

1. Verify that power cord is plugged into site outlet.
2. Press ON side of Power ON/OFF rocker switch. See figure 6-10 for location of switch.
3. Adjust BRIGHTNESS control for desired viewing intensity.

To remove power from the terminal:

1. Press the OFF side of the Power ON/OFF rocker switch.
2. To remove all power from the terminal, disconnect power cord from site outlet.

Procedure 2 - Executing Resident Diagnostics

To run resident diagnostics:

1. Set rocker switches on operator's panel as follows:

   TEST/SKIP (S1) - Set to TEST to execute any of the terminal diagnostic routines. In SKIP position, all terminal diagnostics are bypassed.

   KB/TP/SKIP (S2) - Set to KB/TP to run keyboard/touchpanel test. In SKIP position this test does not execute.

   LOOP/EXIT (S3) - Set to LOOP position to repeat diagnostic tests. In EXIT position, diagnostic test runs only once.

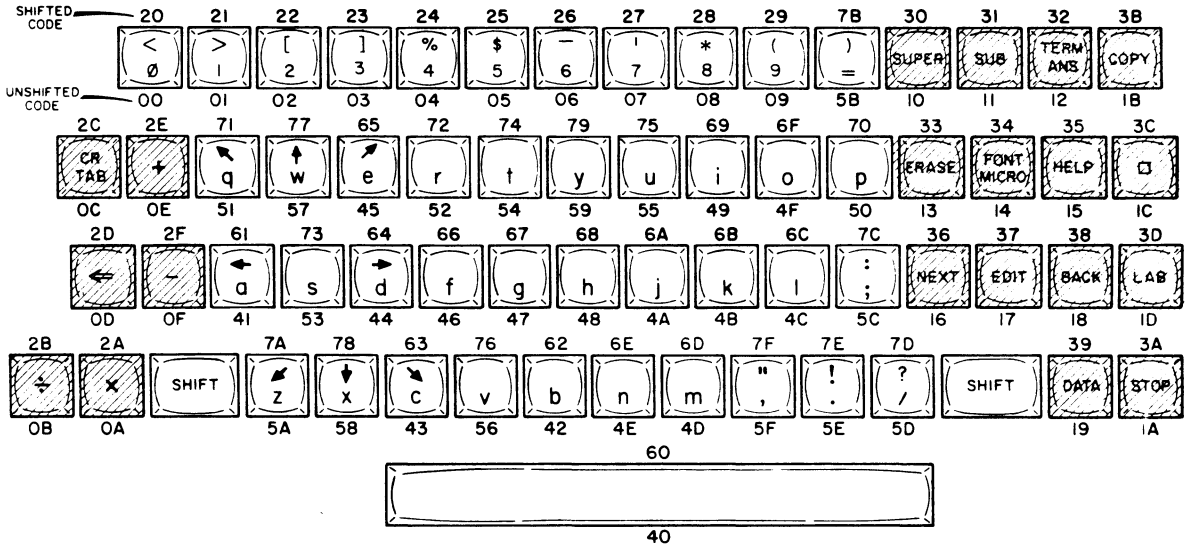
2. Press RESET switch to initialize diagnostic tests. Terminal diagnostics run RAM Memory and Serial Interface tests. If keyboard/touchpanel test is selected, it runs last. Alignment pattern consists of four lines outlining the screen border with two diagnonal lines intersecting at screen center.

3. Touchpanel has 256 touch sensitive areas. Touching any one of these areas causes crt pattern of that area to invert. Repeated touches cause repeated inversions.

   Keyboard portion of this test displays on screen a binary representation of hexadecimal code received from keyboard. These keyboard codes are defined in figure 6-4. This binary representation is made up of long bars (binary 1s) and short bars (binary 0s) with the bottom bar being the lowest order bit.

   Example: Binary representation of w keyboard code, 57_{16}.

   Bit 6 ---
   Bit 5 -
   Bit 4 ---
   Bit 3 - $= 1010111_2 = 57_{16}$
   Bit 2 ---
   Bit 1 ---
   Bit 0 ---



NOTES:

1) Each key has two different inputs. The hexadecimal number below the box is the input when a key is pressed singly, and the number above the box is the input when the SHIFT key is held down as a key is pressed. The SHIFT key alone does not initiate input data transfer, but merely causes an addition of 020 (Hex) to the normal input.
2) There are a total of 124 different inputs. Input codes of 1E, 1F, 3E, 3F are not used.
3) Shaded areas indicate difference in keycap colors.

Figure 6-4. Keyboard Codes and Legends

Error Indications

When an error is detected, the alarm sounds and an error code is displayed in the LED indicators on the front panel of the terminal. The following error codes are displayed where the ERR LED represents the lowest order bit. To isolate error conditions, refer to DDLTs in this section.

Code	Cause of Error
01	Memory error writing/reading 55_{16} pattern
02	Memory error writing/reading AA_{16} pattern
03	Memory error due to addressing problem
04	PLATO serial interface error
05	External serial interface error
06	Keyboard/touchpanel test in progress

For error codes 01 and 02 a second level of LED indication is provided by pressing any keyboard key. The second level is the chip number where the error was first detected. (See figure 6-5).

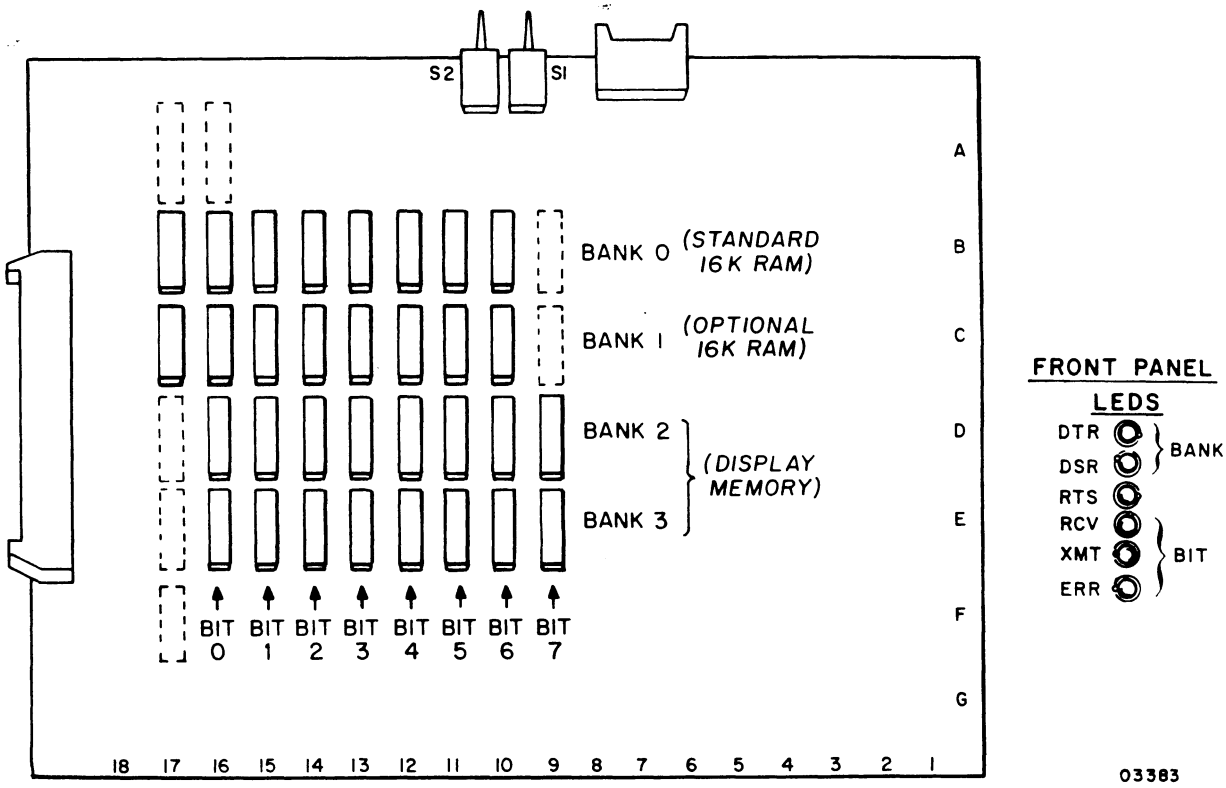


Figure 6-5. RAM Chip Location

For error codes 04 and 05 a second level of indication is provided by depressing any keyboard key. The second level for an 04 error is as follows:

Code	Description
01	No character request status
02	Character request dropped after lower bits output
03	Character request active after upper bits output
04	First byte flag not set
05	Start bit not received
06	No Character ready status
07	Data error

The second level for an 05 error (serial transmission error) is as follows:

Code	Description
01	No character request
02	No character ready
03	Data error

4. With S2 (KB/TP) not set and the diagnostics run successfully, testing stops with a 70 code and a "NOP" displayed on the screen.

Procedure 3 - Executing System Diagnostic (DIAG)

This procedure describes how to access the PLATO system to execute the system diagnostics. The expected display is shown for the log-in portion of the sequence. The diagnostic display provides instructions for test execution (figures 6-6 and 6-7).

1. Turn terminal power on (procedure 1)

2. Ensure that the TEST/SKIP rocker switch is set to SKIP.

3. Dial into system, if applicable

4. When dialing in, DATA/TALK switch on terminal front panel must be in TALK position. When tone is heard, switch to DATA position, and hang up phone.

5. Terminal then initiates a downline load. This takes two to three minutes to perform and is indicated by an incrementing visual display of the data block being loaded (00 to 1C).

NOTE

If terminal displays a NOP, No Reply, or Loading Failure, refer to DDLT CRT5 for corrective action

6. When loading is complete, Welcome Page is then displayed as shown in figure 6-6. Type the word "diag" and press NEXT key as instructed.

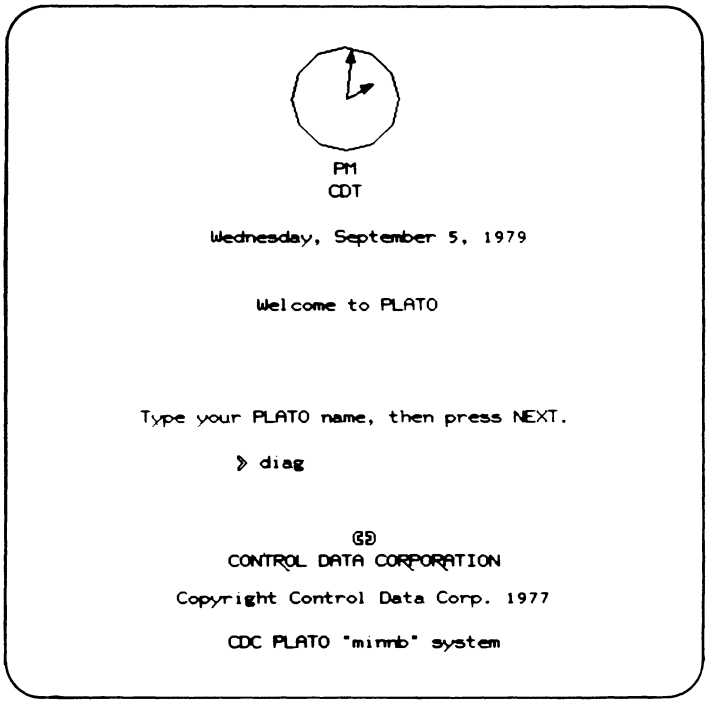


Figure 6-6. Welcome Page Display

7. Group name page is displayed next as shown in figure 6-7. Type "m" and press SHIFT and STOP keys as directed to access DIAG.

6. Follow DIAG instructions for test desired.

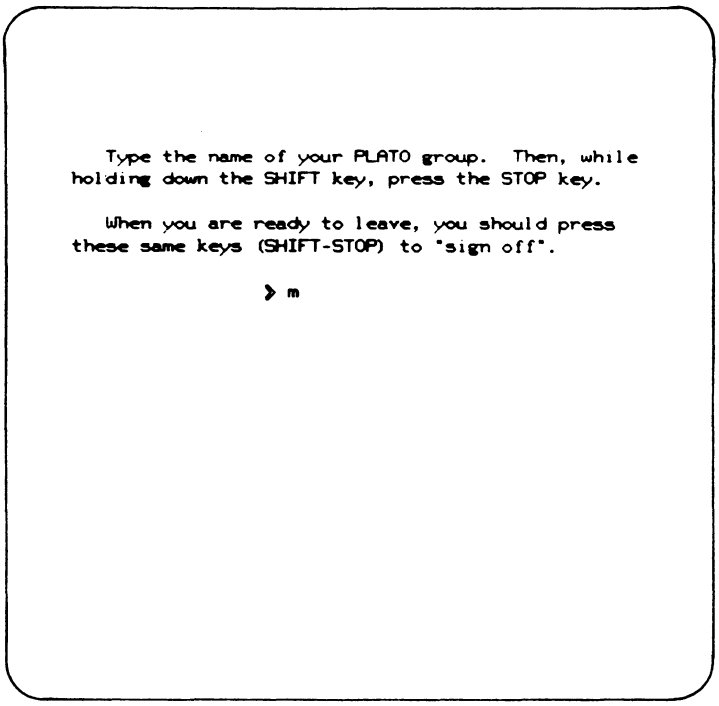


Figure 6-7. Group Name Page Display

Procedure 4 - Removing Hood and Bezel

To remove hood:

1. Remove two bolts at rear of display unit (figure 6-8). lift rear slightly and slide hood toward rear to remove.

2. To reinstall, perform reverse of step 1.

NOTE

When reinstalling hood, be sure connector panel is in slot at rear of hood

To remove bezel:

1. Remove power from terminal per procedure 1.

2. Lay terminal on its side and remove two screws at bottom of terminal, (figure 6-9).

3. Set terminal upright, and remove hood as per preceding instructions.

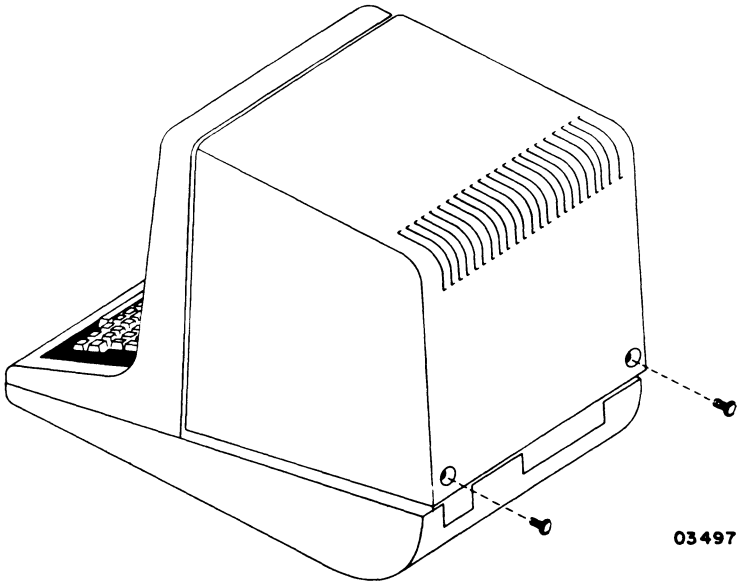


Figure 6-8. Hood Removal

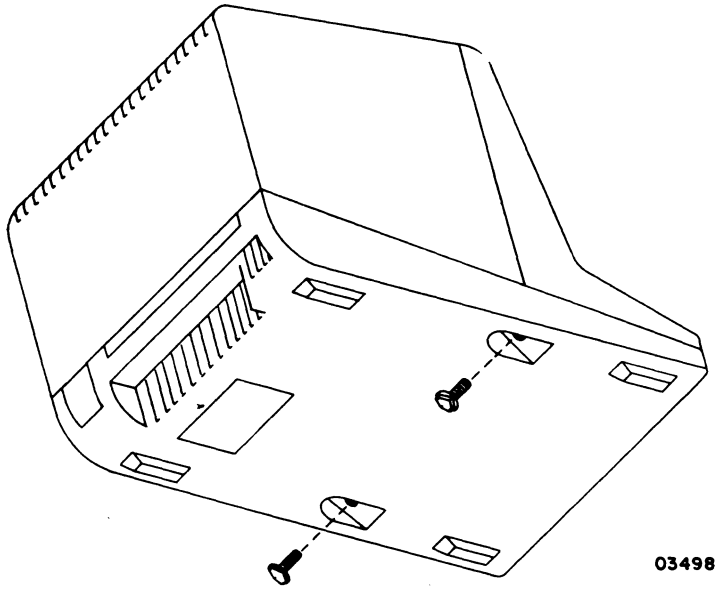


Figure 6-9. Bottom of Terminal

4. Refer to figure 6-10 and remove two bracket bolts as indicated.

5. Disconnect touchpanel and operator panel flat ribbon cables from controller board. Operator panel cable is routed behind modem board, therefore tiewrap must be cut and top of modem board must be loosened to remove cable.

6. If adequate space is available, bezel can be removed and placed to right of terminal while leaving brightness cable and ground cable attached. If space is not available and bezel must be removed completely, continue with the following steps.

NOTE

Before bezel is replaced, it is suggested that face of crt be cleaned with a suitable glass cleaning agent.

7. Remove knob from BRIGHTNESS control by pulling knob straight off.

8. Remove hex nut and washer from BRIGHTNESS control.

9. Loosen touchpanel retainer clip above BRIGHTNESS control and carefully work control out around touchpanel. Retighten touchpanel retainer clip.

10. Remove ground wire at upper left by removing touchpanel retainer clip. Retighten retainer clip.

11. Replace bezel by reversing procedure of preceding steps.

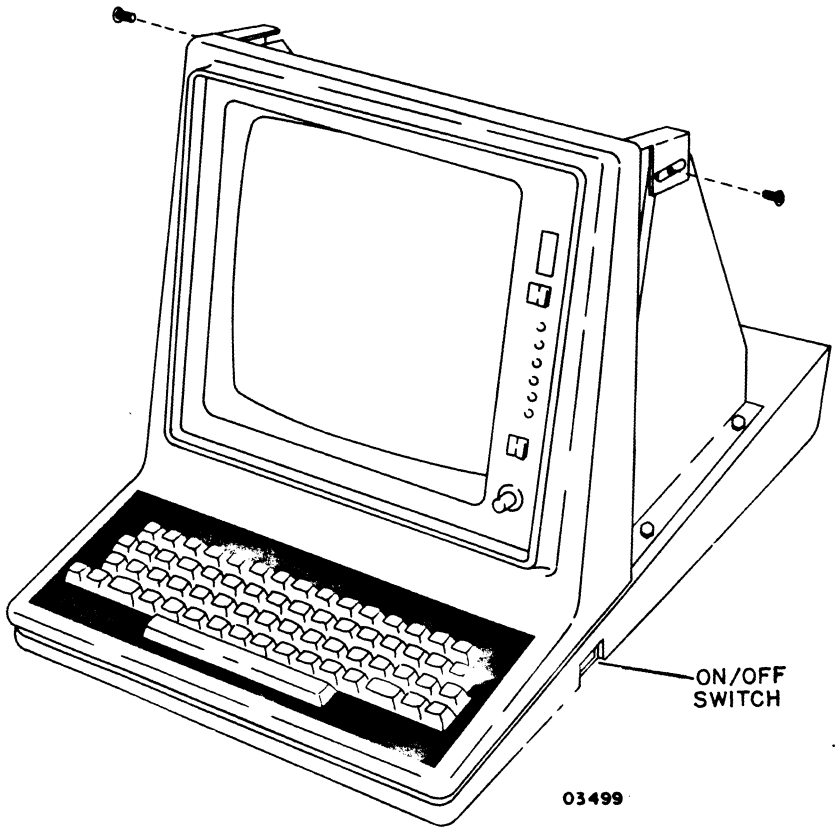


Figure 6-10. Bracket Screws Removal

Procedure 5 - Aligning and Adjusting CRT

To align and adjust crt:

1. Power terminal on per procedure 1.

2. Select alignment pattern by:

   a. Placing KB-TP/SKIP rocker switch to KB-TP.
   b. Placing TEST/SKIP rocker switch to TEST.
   c. Pressing RESET switch.

3. Adjust BRIGHTNESS control for sharpest video and carefully observe the alignment pattern for a symmetrical display and correct alignment with touchpanel etched pattern at sides, top, and bottom of display screen. Refer to procedure 23 for acceptable display quality definitions.

NOTE

Allow a warm-up period of 15 to 30 minutes before performing adjustments.

Minor adjustments may be performed by the use of the Horizontal Linearity. Horizontal Width, Horizontal Frequency, Vertical Linearity, Vertical Height, Vertical Frequency, Video Gain and Focus adjustments. To perform these internal adjustments, remove the terminal hood (procedure 4) and refer to figure 6-11 for location of internal controls.

WARNING

Lethal voltages exist in the crt assembly. Use extreme caution when performing adjustments or severe personal injury or loss of life may result.

4. Adjust Focus control such that top center and extreme right center focus are of equal display quality.

5. Adjust BRIGHTNESS control on front of terminal so that scan lines are visible in background of display.

6. Adjust Horizontal Frequency control to center display horizontally until margins on right and left are of equal distance.

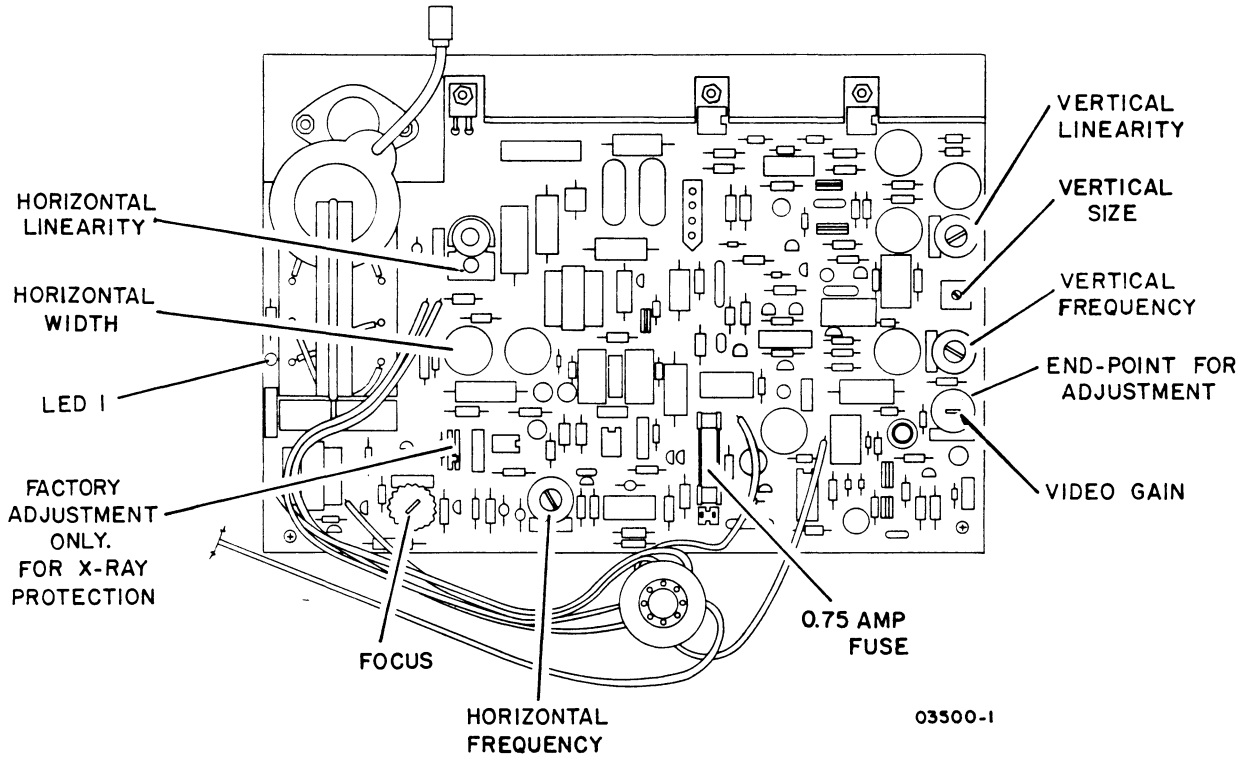


Figure 6-11. Display PC Board

7. Adjust BRIGHTNESS control until background scan lines are no longer visible.

8. Adjust Horizontal Linearity control until diagonal lines of touchpanel test display are an equal distance from right and left sides.

9. Adjust Vertical Linearity control until diagonal lines of touchpanel test display are an equal distance from top and bottom.

10. To adjust Vertical Frequency control, first turn potentiometer 90° in each direction, then adjust so that potentiometer is in middle of range where display is not moving vertically.

11. Use Horizontal Width and Vertical Height controls to adjust picture size to 8.5 in by 8.5 in (216 mm by 216 mm). Use plastic ruler or a piece of 8 1/2 by 11 inch paper to measure display size.

12. Adjust video contrast using Video Gain control. Turn Video Gain control in a counterclockwise direction until saturation just occurs, then back off the control 30 degrees clockwise.

NOTE

Video gain is increased by adjusting the potentiometer in a counterclockwise direction. Over adjustment results in saturation of the video amplifier. This is indicated by the end-points on the right of the display overshooting.

Procedure 6 - Adjustment of Yoke Centering Rings

NOTE

Perform this procedure only after procedure 5 has been completed.

If after having followed procedure 5, the display is not centered, or if portions of the display are missing, see figure 6-12 and do the following:

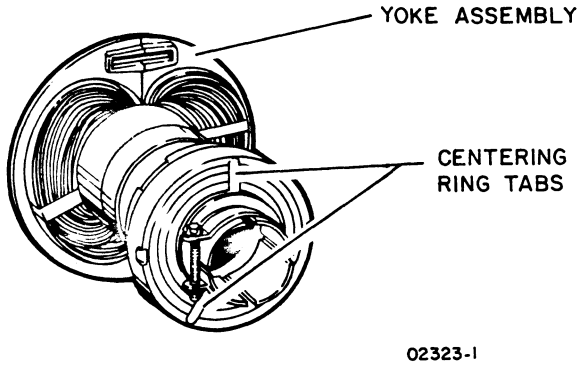


Figure 6-12. CRT Centering Rings

1. Remove power from terminal per procedure 1.
2. Remove terminal hood per procedure 4.
3. Break glue on centering rings by turning each approximately one-quarter turn each way.

4. Ensure that yoke is snug against crt neck.

5. Power on terminal per procedure 1.

WARNING

Lethal voltages exist in the crt assembly. Use extreme caution when performing adjustments or severe personal injury or loss of life may result.

6. Run keyboard/touchpanel resident diagnostic per procedure 2 to display alignment pattern.

7. Adjust centering rings to ensure display pattern is centered. Distance between each side and center should be 4.25 in (108 mm).

8. After picture is centered:

   a. Power off terminal and disconnect ac power cord from site outlet.

   b. Wait 60 seconds to permit crt to bleed off power.

   c. Reglue centering rings. Use torque seal glue or equivalent.

   d. Reapply power to terminal and verify that centering rings did not move while being glued.

9. Replace hood per procedure 4.

10. Go back and repeat procedure 5.

Procedure 7 - Replacing Video or Controller Printed Circuit Boards

To replace the video or controller boards perform the following steps as applicable:

1. Remove terminal power per procedure 1.

2. Remove terminal hood per procedure 4.

3. Refer to figure 6-13 for board locations.

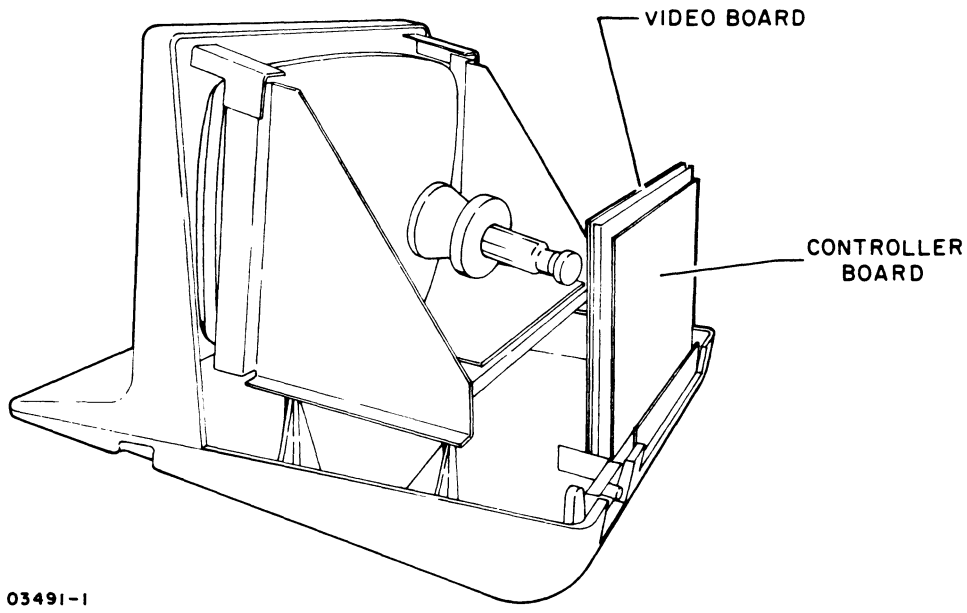


Figure 6-13. Video and Controller Board Locations

4. To replace video board:

   a. Disconnect cables from board taking care not to bend pins.

   b. Unlock board from each retainer clip by holding retainer between thumb and forefinger (figure 6-14) and use thumbnail to press on protruding portion of retainer. Gently pull board out about 0.25 in (6 mm) and remove board.

   c. Place replacement board over retainer clips and press to snap into position.

   d. Reconnect cables to board. Refer to figure 6-15 for correct cable connections/pin alignment.

5. To replace controller board:

   a. Disconnect I/O cables from connectors at rear of terminal.

   b. Disconnect cables from board taking care not to bend pins.

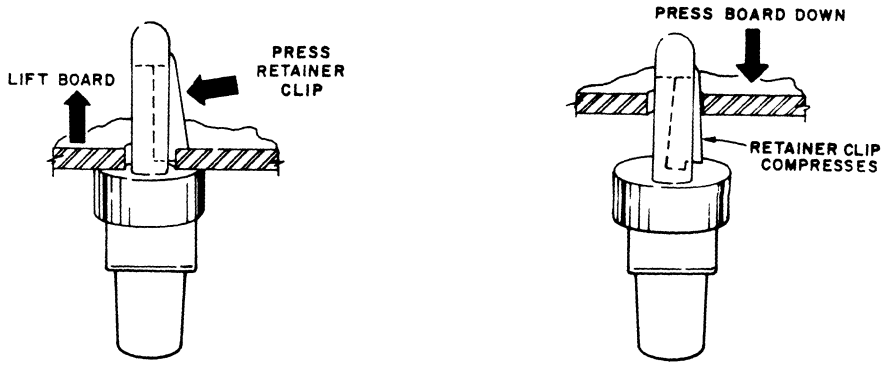


Figure 6-14. Board Retainer Clips

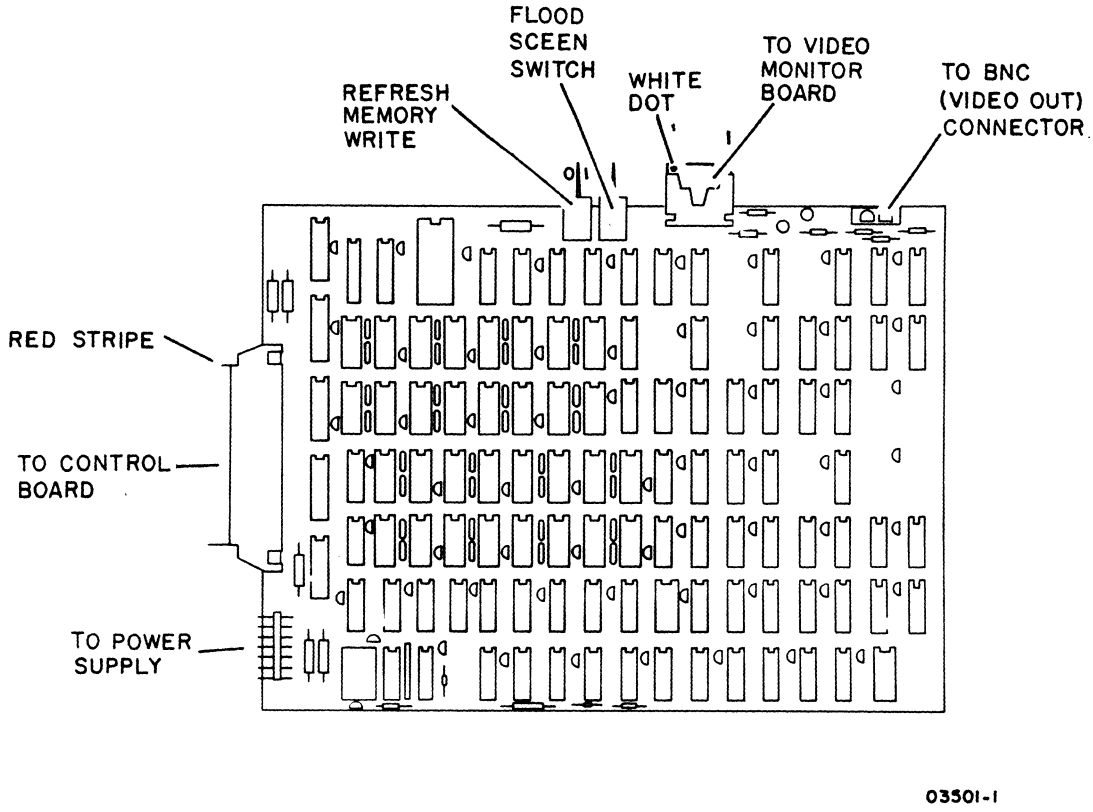


Figure 6-15. Video Board

c. Unlock board from each retainer clip by holding retainer between thumb and forefinger (figure 6-14) and use thumbnail to press on protruding portion of retainer. Gently pull board out about 0.25 in (6 mm) and remove board.

d. Disconnect ground lead from board mounting frame.

e. Connect ground lead to replacement board mounting frame.

f. Place replacement board over retainer clips and press to snap into position.

g. Reconnect cables to board. Refer to figure 6-16 for correct cable connections/pin alignment.

h. Reconnect I/O cables to connector panel.

i. Verify that configuraion/mode switches on board are set correctly (see Installation, section 3 of this manual).

6. Apply power and test terminal (procedure 2) with new board installed before replacing hood.

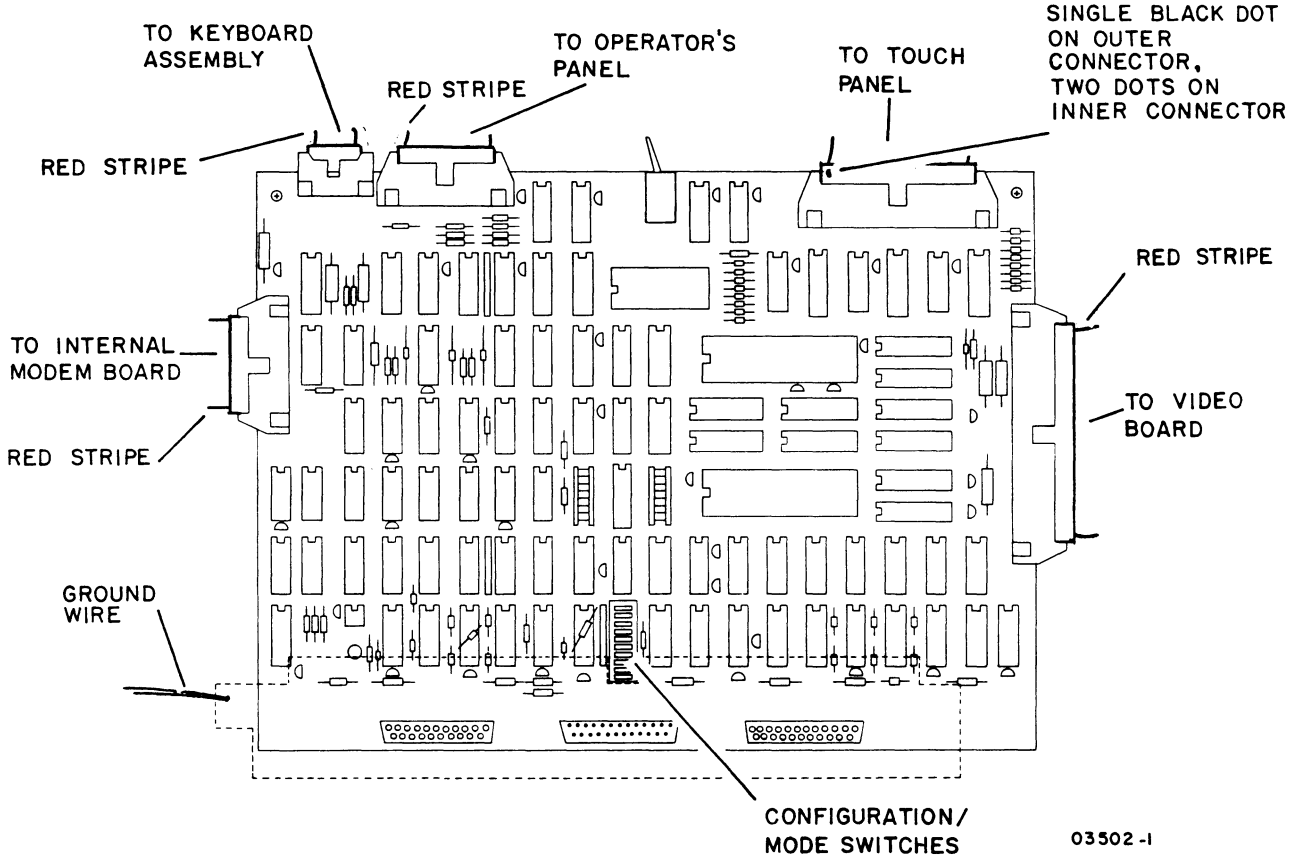


Figure 6-16. Controller Board

Procedure 8 - Replacing IC Chips

Observe the following caution when replacing IC chips:

CAUTION

Follow precautionary rules for handling MOS type circuits as described earlier in this section.

The following plugable chips can be removed on site:

- Z80A Processor IC on controller board (figure 6-17)
- TR1602A UART IC on controller board (figure 6-17)
- All 32 RAM ICs on video board (figure 6-18)
- One EROM IC on video board (figure 6-18)
- One 14-pin IC (IC2) on crt monitor display board (figure 6-19)

1. Turn terminal power off per procedure 1.
2. Remove controller board or video board from terminal as applicable per procedure 7.
3. Use chip remover tool (CDC part number 87365900 or equivalent) for 14 and 16-pin ICs, or use a small screwdriver for larger ICs, and lift IC straight out to avoid bending pins.
4. Observe correct pin alignment when installing replacement IC. Dot or indentation on IC must be aligned with notched side of IC socket.
5. Apply power and test terminal per procedure 2 after replacing any IC.

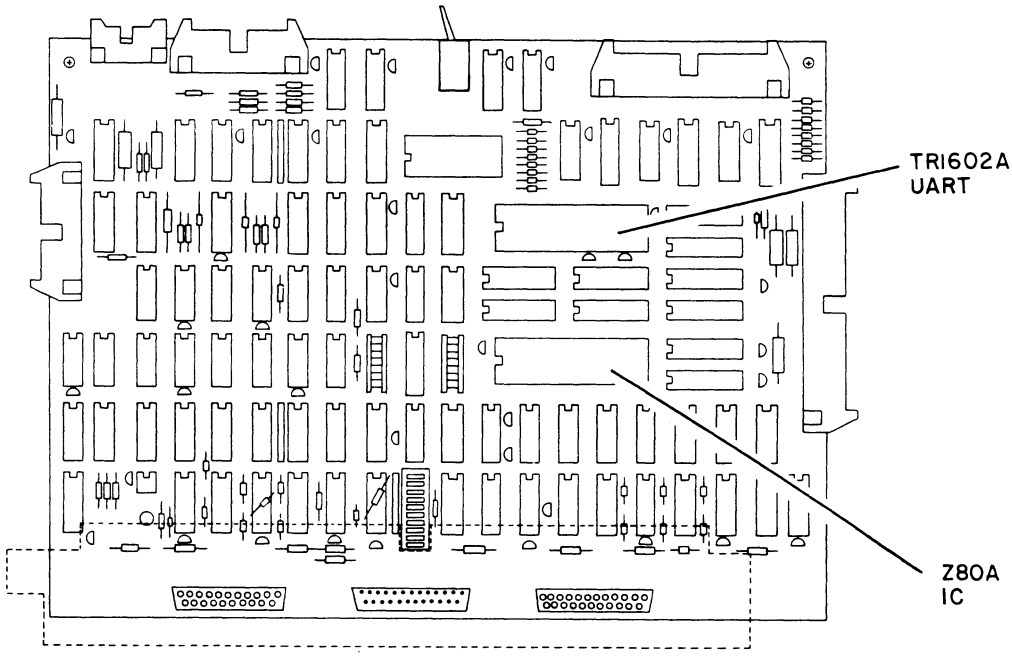


Figure 6-17. IC Locations on Controller Board

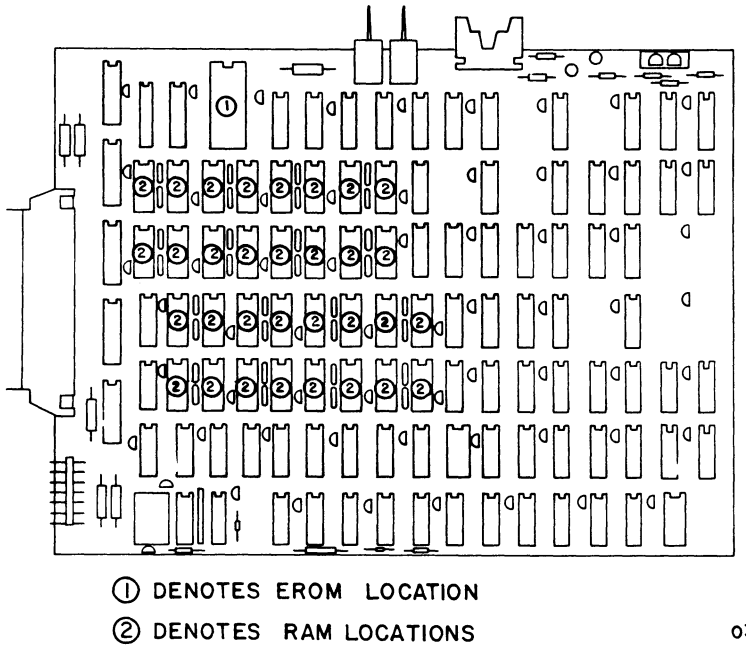


Figure 6-18. IC Locations on Video Board

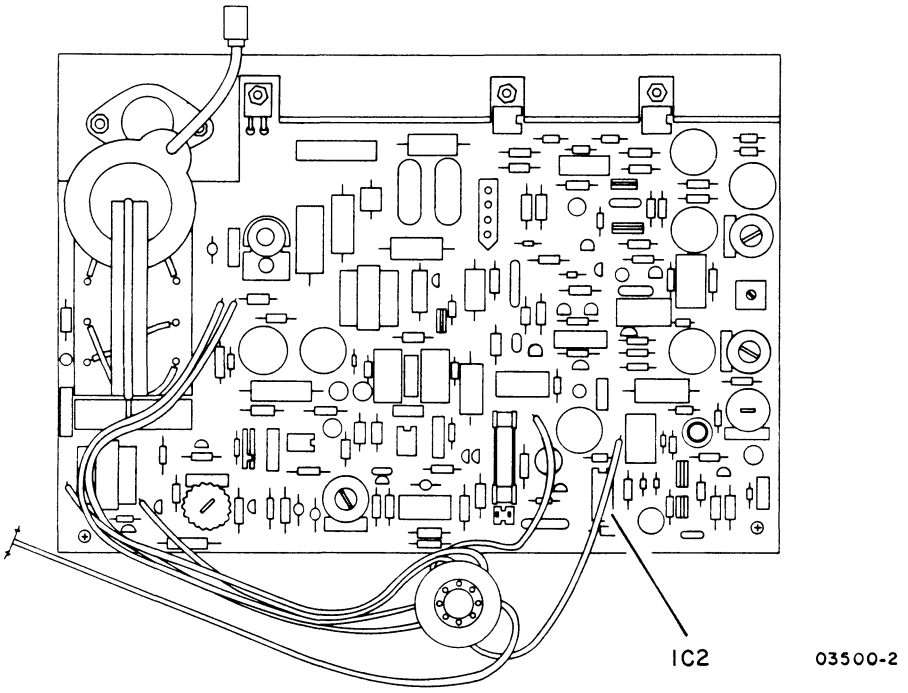


Figure 6-19. IC Location on CRT Monitor Display Board

Procedure 9 - Adjusting Power Supply

To adjust the output voltages of the power supply regulator assembly:

1. Remove terminal hood per procedure 4.
2. Apply terminal power per procedure 1.
3. Verify that five LEDs on power supply board are lit (figure 6-20)

NOTE

A lit LED does not necessarily mean that the correct voltage is present. An LED will light whenever a voltage having the proper polarity and of a sufficient level to light the indicator is present.

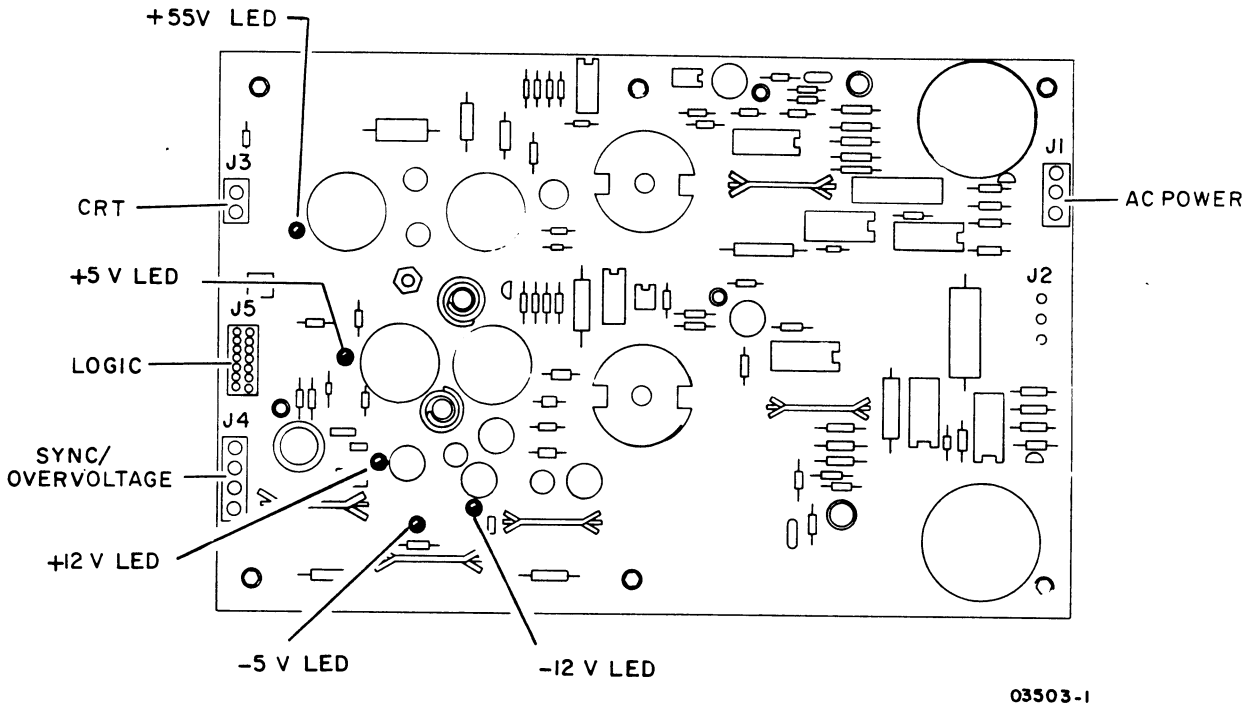


Figure 6-20. Power Supply Board

4. Measure +5 V at controller board, see figure 6-21.

NOTE

Voltage measurements are made on the controller PC board rather than the power supply because a voltage drop occurs over the cables.

5. Measure +55 V at display board of crt monitor assembly, see figure 6-22.

6. To adjust voltages use special tuning wand tool (CDC part number 12263476). Access to the adjustment pots is through holes in the monitor chassis. Each of the two holes is labeled with the corresponding voltage of the pot. See figure 6-23.

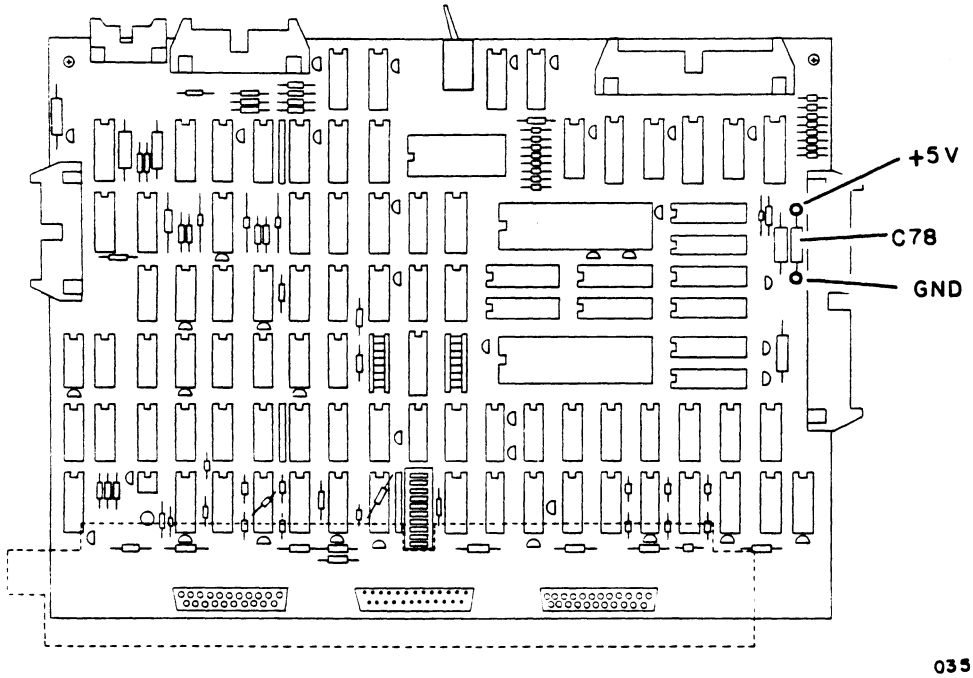


Figure 6-21. Test Points for +5 V on Controller Board

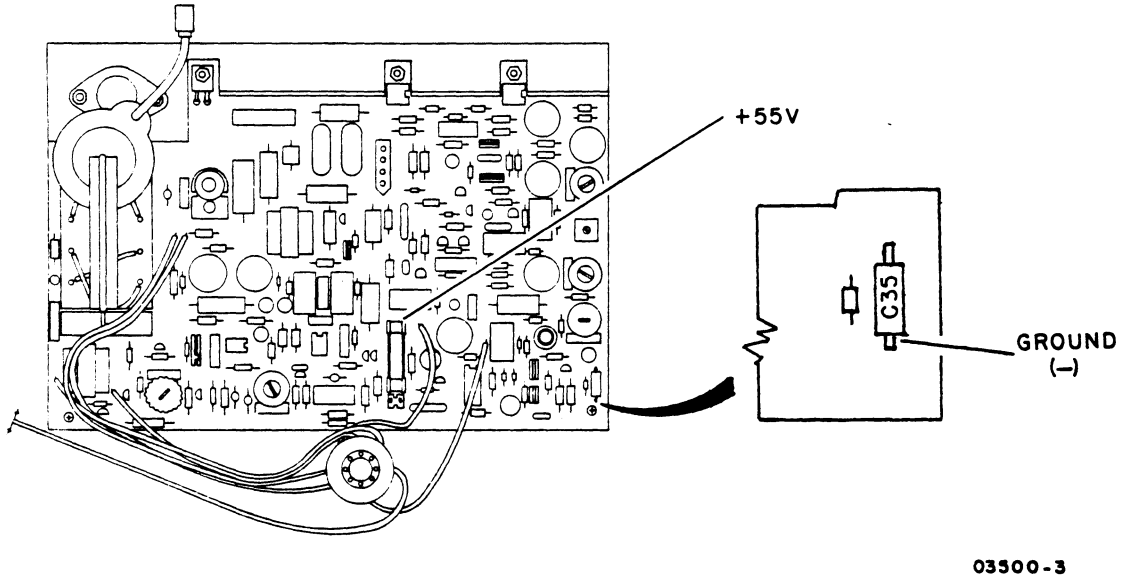


Figure 6-22. Test Points for +55 V on Display PC Board

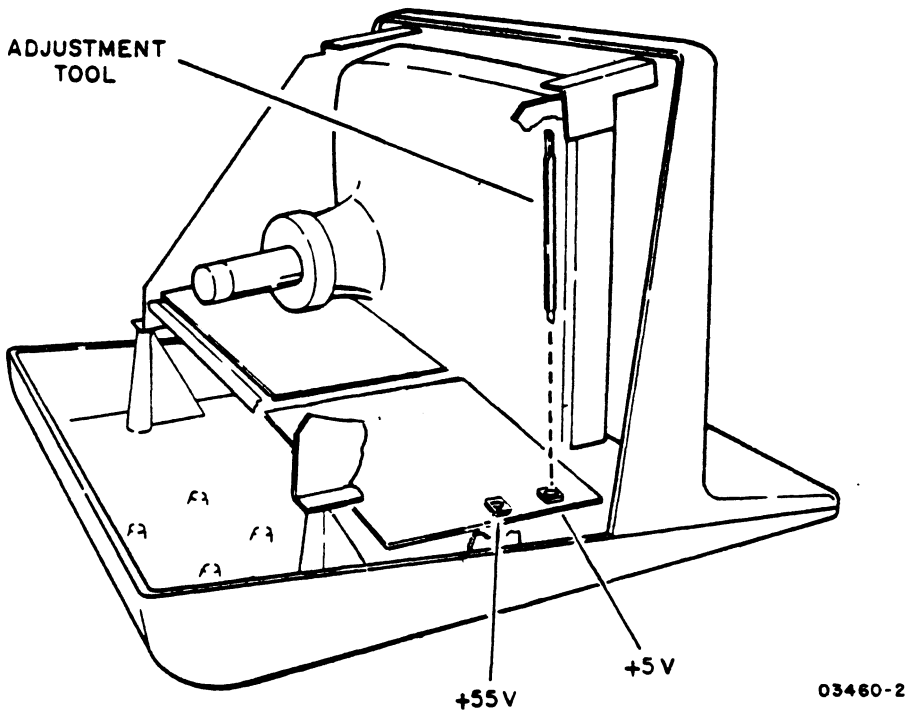


Figure 6-23. Power Supply Adjustments

Procedure 10 - Replacing Power Supply

To replace the power supply:

1. Turn terminal power off (procedure 1).
2. Unplug ac input power cord from site power outlet.
3. Remove terminal hood per procedure 4.
4. Disconnect the following cables:
   - Keyboard cable at controller board (see figure 6-16)
   - Touchpanel cable at controller board (see figure 6-16)
   - Operator panel cable at controller board (see figure 6-16)

5. Remove internal modem board from chassis (procedure 21).

CAUTION

When removing and installing crt chassis, use care so that crt yoke is not bumped against video PC board. TILT CHASSIS SO THAT YOKE IS DOWN. Also when installing crt chassis use care to prevent pinching the touchpanel cable.

6. Remove six crt chassis mounting bolts (figure 6-24) and carefully lift crt chassis and place on a firm surface.

7. Disconnect four cables and ground wire from power supply board (see figure 6-20).

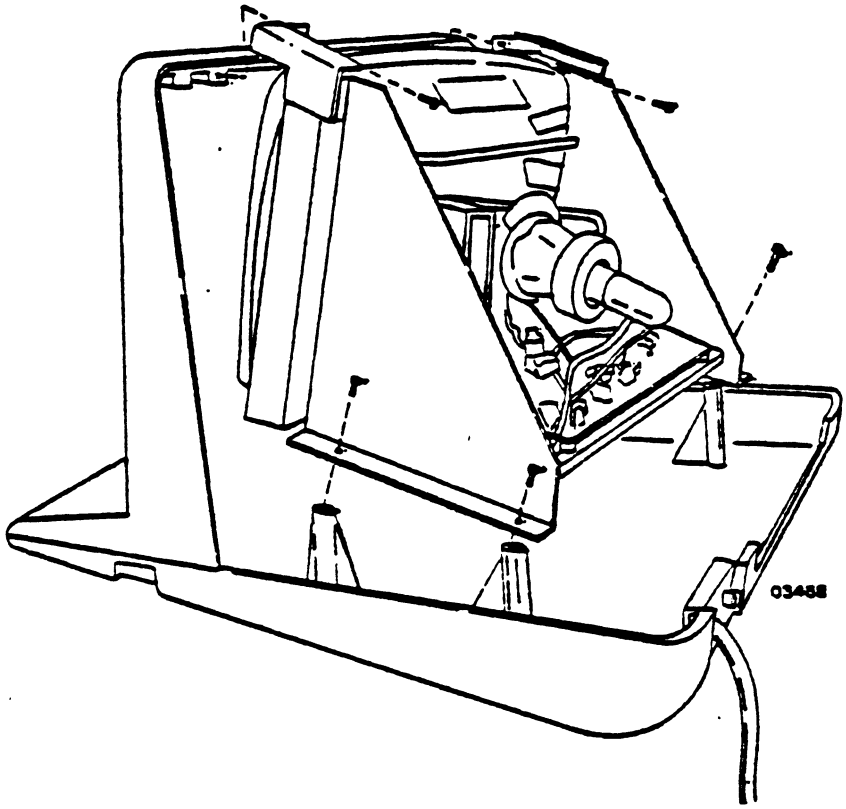


Figure 6-24. CRT Chassis Removal

8. Remove power supply board by removing six mounting screws as shown in figure 6-25.

9. To replace power supply board reverse procedure of preceding steps.

10. Perform power supply adjustments per procedure 9.

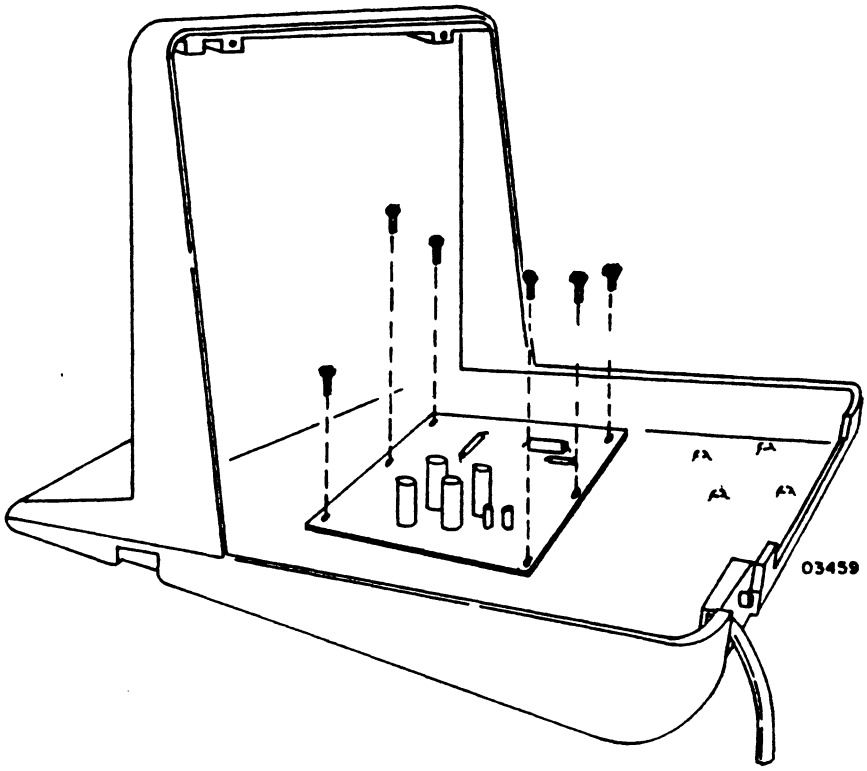


Figure 6-25. Power Supply Removal

Procedure 11 - Replacing 60 Hz or 50 Hz AC Entry Panel, and 50 Hz Transformer

To replace 110 V, 60 Hz ac entry panel, reference 60-Hz ac entry panel assembly drawing in Section 7 (Parts Data Section) and do the following:

1. Power off terminal per procedure 1.

2. Unplug ac power cord from site outlet.

3. Remove terminal hood and bezel per procedure 4.

4. Disconnect cable at connector J1 from power supply board (reference figure 6-20).

5. Disconnect Video Out BNC connector from video board.

6. Disconnect Fastons from terminals A and B (yellow wires) of ON/OFF switch (reference figure 6-26).

power cord).

8. Remove two bolts that mount ac entry panel to terminal base (see figure 6-).

9. Lift ac entry assembly out of unit. Remove telephone connectors (if used) from panel by pressing latching mechanism and sliding them out.

10. Unscrew BNC connector from panel.

11. To install replacement ac entry panel, perform reverse of preceding steps.

To replace 220/240-V, 50-Hz ac entry panel, reference 50-Hz ac entry panel assembly drawing in Section 7 (Parts Data Section) and do the following:

1. Power off terminal per procedure 1.

2. Unplug ac power cord from site outlet.

3. Remove terminal hood and bezel per procedure 4.

4. Disconnect Video Out BNC connector from video board.

5. Disconnect Faston from terminal B (yellow wire) of ON/OFF switch (see figure 6-26).

6. Disconnect other yellow wire of ac entry panel that connects to either the 220 V or 240 V input lead of power transformer. Make note of which input power lead wire was connected to. (From transformer 220-V wire is black and 240-V wire is brown.)

7. Disconnect four ground wires from ac entry panel mounting frame.

8. Remove two bolts that mount ac entry panel to terminal base (see figure 6-).

9. Lift ac entry assembly out of unit. Remove telephone connectors (if used) from panel by pressing latching mechanism and sliding them out.

10. Unscrew BNC connector from panel.

11. To install replacement ac entry panel, perform reverse of preceding steps.

To replace 220/240-V, 50-Hz input power transformer:

1. Power off terminal per procedure 1.
2. Unplug ac power cord from site outlet.
3. Remove terminal hood and bezel per procedure 4.
4. Remove crt chassis per procedure 10, steps 4 thru 7.
5. Disconnect Faston from terminal A (blue wire) of ON/OFF switch (reference figure 6-26).
6. Disconnect J1 from power supply board (reference 6-20).
7. Disconnect ground wire from side of transformer.
8. Remove four mounting screws and lift transformer from unit (reference figure 6-25.1).
9. To install replacement transformer, perform reverse of preceding steps.

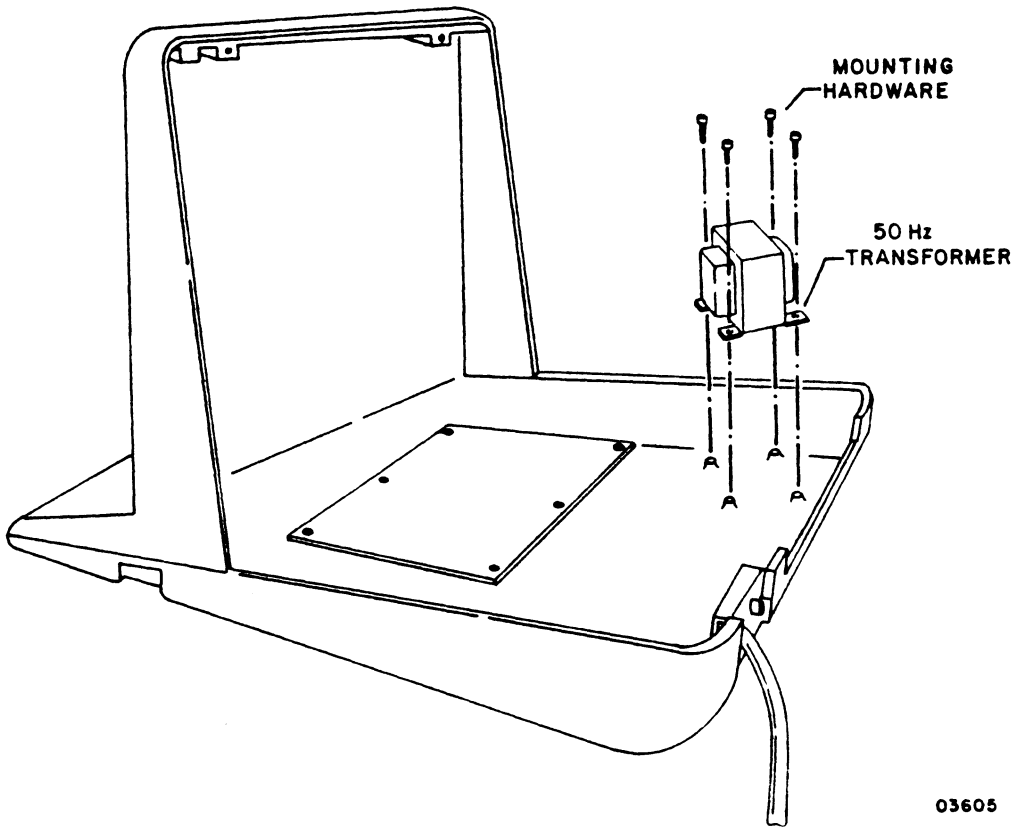


Figure 6-25.1. 50 Hz Transformer Removal

Procedure 12 - Replacing Power ON/OFF switch/circuit breaker:

1. Power off terminal per procedure 1.
2. Unplug ac power cord from site outlet.
3. Remove terminal hood and bezel per procedure 4.
4. Position new switch above bad switch with ON/OFF label orientated correctly. Remove each wire one at a time from bad switch and connect to corresponding terminal of new switch. Figure 6-26 shows the ON/OFF switch wire connection on the 60-Hz and the 50-Hz units.
5. Remove faulty switch by removing two bolts as shown in figure 6-26.
6. Install new switch and secure with two mounting bolts removed in step 5.
7. Replace bezel and hood per procedure 4.

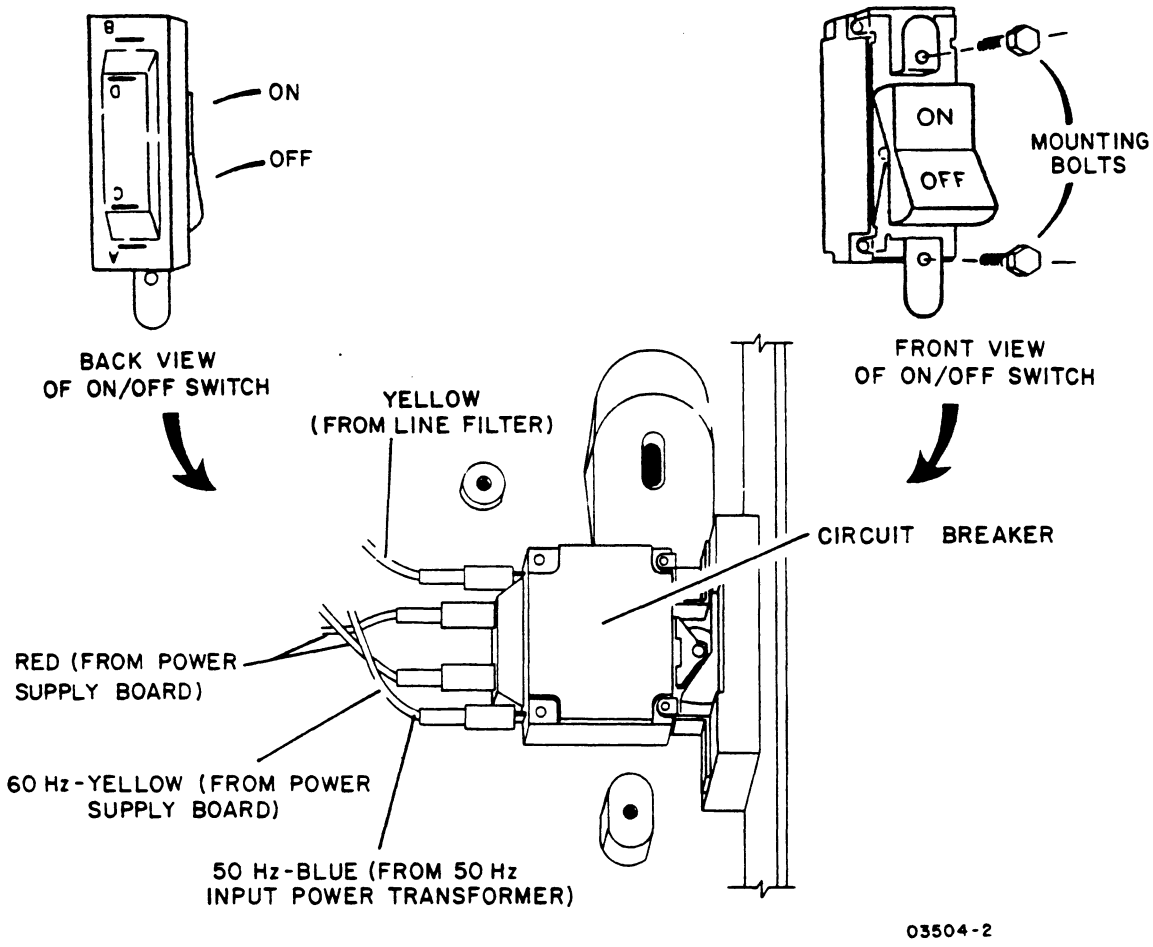


Figure 6-26. Power Switch Replacement

To replace the keycaps, keyboard, space bar, or keyswitches perform the following steps as applicable:

To Replace Keycap:

1. Turn terminal power off (procedure 1).
2. Remove keycap by using chip removal tool (CDC part number 87365900).
3. Install new keycap by pressing down on new keycap until it seats firmly.

To Replace Spacebar:

1. Place a finger under each end of spacebar and pull up to release. Move spacebar to one side and carefully pull wire from bracket (see figure 6-27).
2. Install replacement spacebar in a reverse manner.

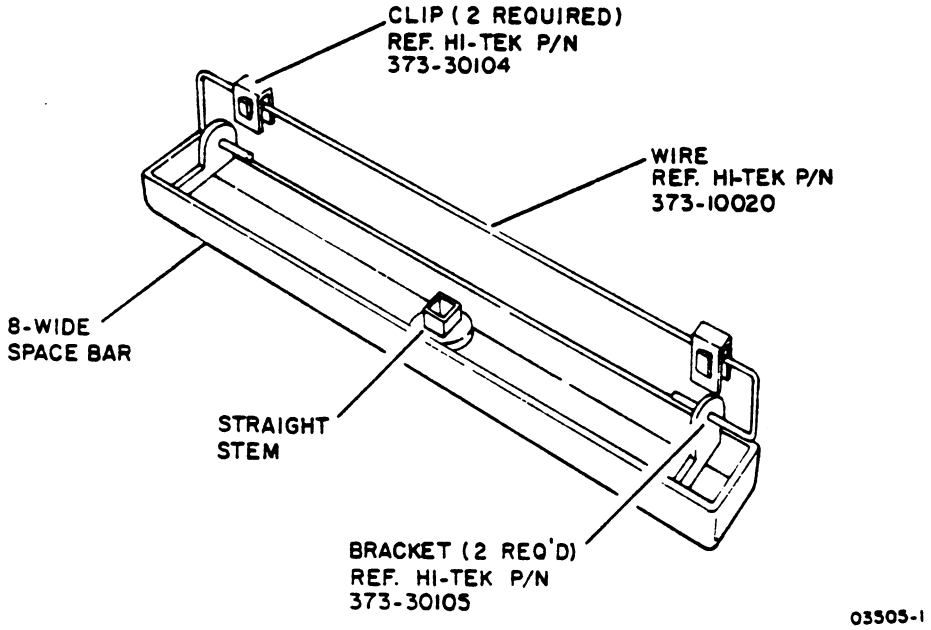


Figure 6-27. Space Bar Removal

To Replace Keyboard:

1. Turn terminal power off (procedure 1) and disconnect ac power input cord from site outlet.

2. Remove terminal hood and bezel (procedure 4).

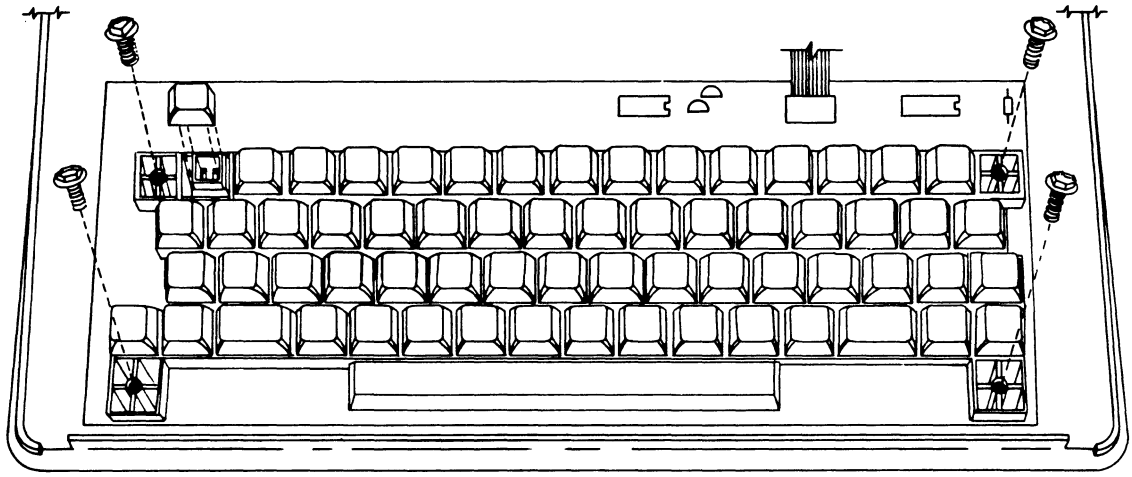
3. Disconnect keyboard cable.

4. Refer to figure 6-28 and remove four bolts mounting keyboard assembly to terminal base.

5. Install new keyboard assembly by reversing preceding steps. When reconnecting keyboard cable to controller board, make sure that red stripe on cable is correctly lined up (refer to figure 6-16).

NOTE

Check that bezel does not bind key caps on top or sides before tightening down. If binding occurs, remove bezel, loosen keyboard and reposition slightly.



03506-1

Figure 6-28. Keyboard Assembly Removal

To Replace Keyswitch:

1. Turn terminal power off (procedure 1) and remove keyboard assembly as previously described in this procedure.

2. Remove keycap as described earlier in this procedure.

CAUTION

The black plunger housings for the entire keyboard are molded in one piece. Do not pry against housing as it is subject to breakage and would require complete keyboard replacement.

3. Grasp white plunger firmly with a long nose plier and pull straight up. Remove spring.

CAUTION

Use a low wattage soldering iron to prevent damage to the PC board. A vacuum action desoldering tool or solder wick is suggested when unsoldering the switch.

4. Unsolder switch contacts and remove them by pulling straight up using a long nose plier. Do not pry against plunger housing.

5. Insert new switch contacts into keyswitch insertion tool (CDC part number 51919702). Refer to figure 6-29 for proper loading of tool. Be sure to use one bifurcated and one solid contact.

6. Place insertion tool into plunger housing with switch contacts facing right and left of keyboard (not up and down). Press insertion tool plunger firmly down until it stops. Check that solder tabs are exposed on back of PC board.

7. Solder each solder tab of switch.

8. Place spring over switch contacts (figure 6-29) and carefully snap plunger down over spring. Be sure that divider bar inside plunger goes between contacts.

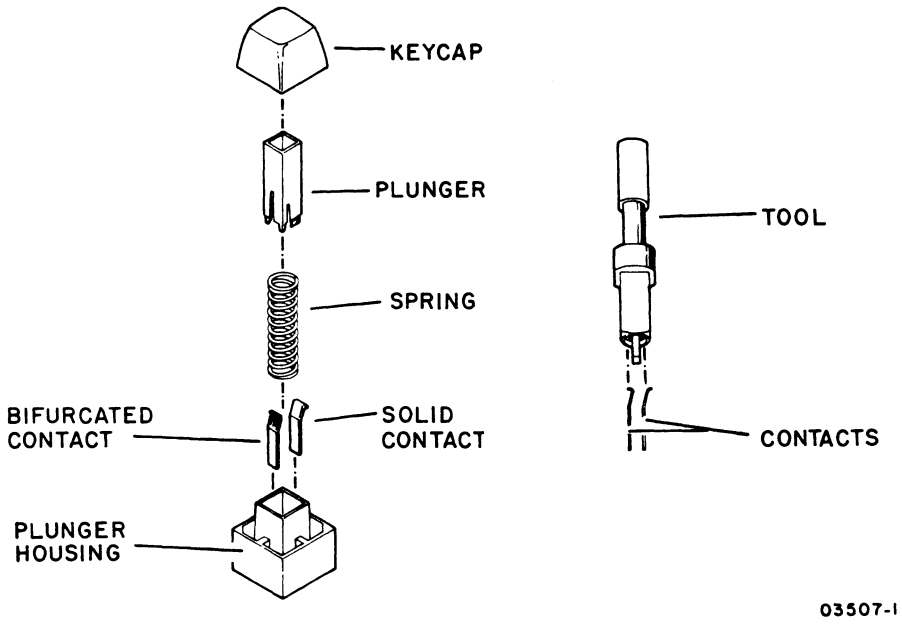


Figure 6-29. Keyswitch Replacement

9. Replace keycap and reinstall keyboard.

NOTE

Spacebar keyswitch replacement is performed in the same manner described in the preceding procedure. However, note that the spacebar has a 3-ounce spring rather than the 2-ounce springs used for the remaining switches.

Procedure 14 - Replacing Operator Panel

To replace operator panel:

1. Power off terminal per procedure 1.
2. Remove hood and bezel per procedure 4.
3. Remove touchpanel per procedure 20.
4. Remove bolt holding alarm, see figure 6-30.

5. Remove three bolts holding operator panel, see figure 6-30.

6. Disconnect flat ribbon cable from controller board.

7. To replace operator panel, perform reverse of preceding steps.

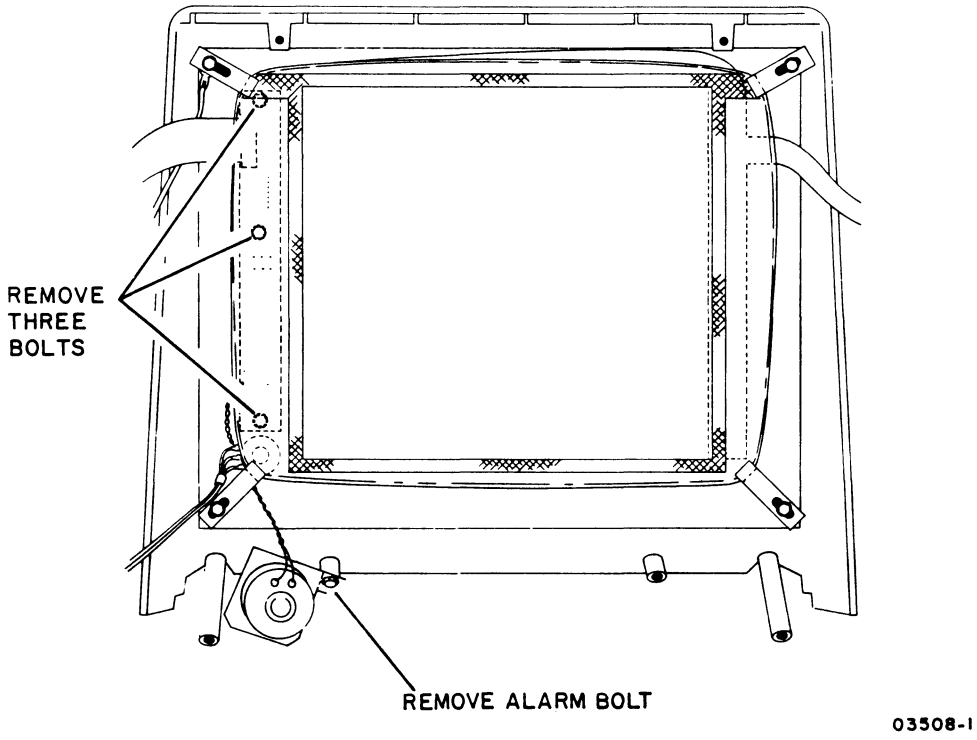


Figure 6-30. Operator Panel Removal

Procedure 15 - Replacing Operator Panel LEDs

To replace the LED indicators on the operator panel, perform the following:

1. Turn terminal power off (procedure 1) and unplug ac power cord from site outlet.

2. Remove operator panel per procedure 14.

CAUTION

Use a low wattage soldering iron to prevent damage to PC board. A vacuum action desoldering tool or solder wick is suggested when unsoldering the LED.

3. Unsolder faulty LED from operator panel.

4. Install new LED making sure that it is configured as shown in figure 6-31, then solder to PC board.

5. Reinstall operator panel (refer to procedure 14).

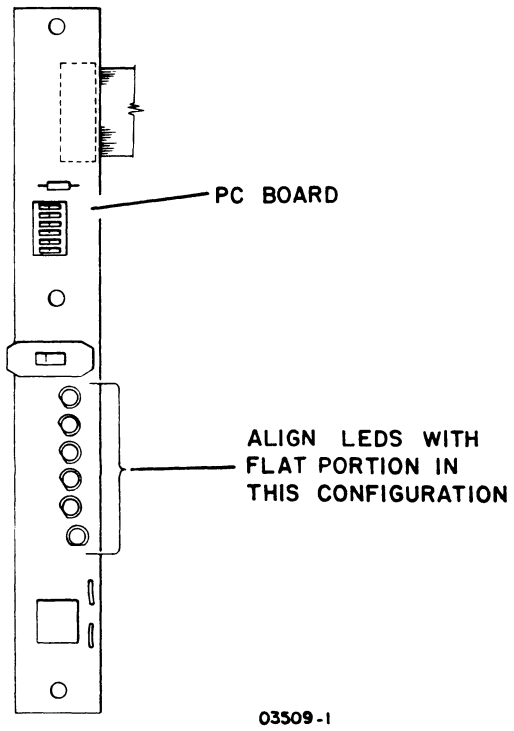


Figure 6-31. Operator Panel

Procedure 16 - Replacing BRIGHTNESS Control

To replace BRIGHTNESS control:

1. Power off terminal per procedure 1, unplug ac power cord from site outlet.

2. Remove hood and bezel per procedure 4 (steps 1 through 6).

3. Pull BRIGHTNESS knob off and remove hex nut and washer from front of BRIGHTNESS control.

4. Loosen touchpanel mounting clip above potentiometer and move clip to one side.

5. Remove BRIGHTNESS control by carefully working it around touchpanel and touchpanel mounting clip.

CAUTION

Use a low wattage soldering iron. A vacuum action desoldering tool or solder wick is suggested to unsolder wires from potentiometer.

6. Place replacement potentiometer next to bad one. Unsolder wires one at a time and resolder to corresponding lug of replacement potentiiometer.

7. Carefully install potentiometer in bezel by working it around touchpanel. Insert potentiometer in bezel opening with key positioned properly.

8. Attach nut and washer to front of potentiometer and replace bezel and hood per procedure 4.

Procedure 17 - Replacing Access Door

To replace access door on operator panel, perform the following:

1. Power off terminal per procedure 1.

2. Remove hood and bezel per procedure 4.

3. Remove black bezel insert by breaking two metal keepers that hold both bezel pieces together.

4. Insert new access door and fasten both bezel pieces back together using two new keepers.

5. Reinstall bezel and hood per procedure 4.

Procedure 18 - Replacing CRT or Display Board

To replace the crt or display board, the crt monitor chassis must be removed.

1. Turn terminal power off, per procedure 1, and disconnect ac power cord from site outlet.

2. Remove terminal hood per procedure 4.

3. Disconnect touchpanel, operator panel, modem, and keyboard cables from controller board (see figure 6-16).

4. Disconnect display board connector, see figure 6-32.

CAUTION

When removing chassis from terminal, use care so that crt neck is not bumped against video PC board. Do not handle crt by its neck. Tilt the chasis so that the neck is down.

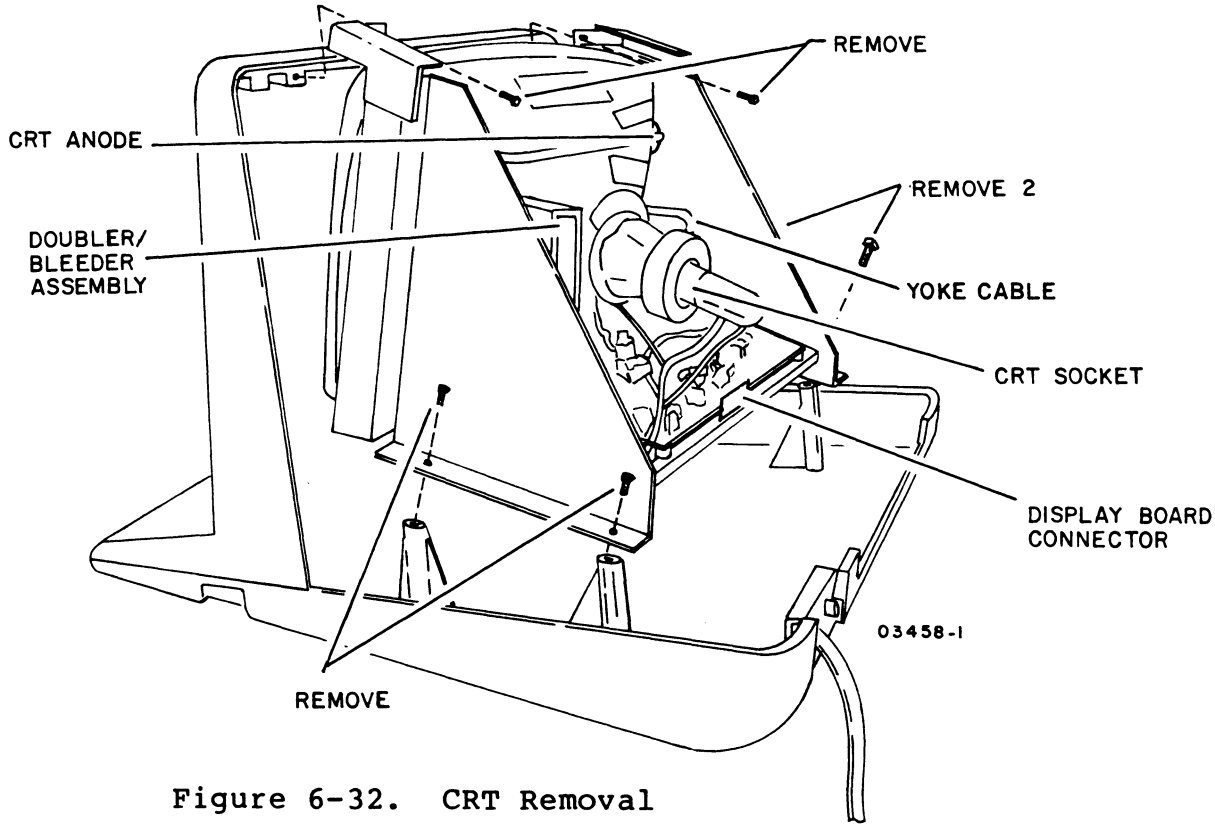


Figure 6-32. CRT Removal

5. Remove six screws as shown in figure 6-32, and lift chassis out of terminal. Set on firm surface to work on.

WARNING

Use care when handling crt as rough handling, nicks, or scratches can cause crt to implode. Wear heavy gloves and safety goggles.

6. To remove crt, see figure 6-32 and 6-33, and disconnect the following cables:

   - CRT socket
   - Yoke cable
   - CRT anode (fold back suction cup on two sides and squeeze to remove).

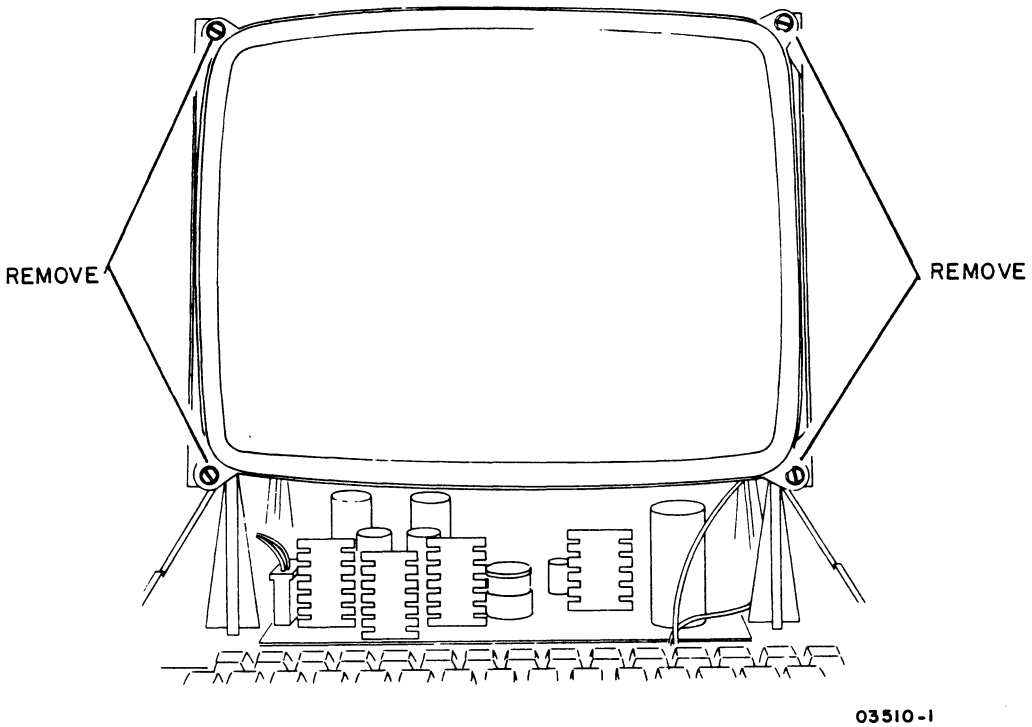


Figure 6-33. Front Chassis View

7. Remove four screws on front of chassis and lift crt up and out.

8. To install new crt, reverse above steps. Perform crt alignment checks according to procedure 5.

To remove display board assembly:

9. Disconnect display board connector, yoke connector plug, high voltage lead, and ground wire from display board.

10. Remove two screws and remove board.

11. To replace board reverse above steps. Care must be taken when replacing display board; align tongue on board with slot on chassis. Perform crt alignment checks per procedure 5.

Procedure 19 - Replacing Voltage Doubler/Bleeder Assembly.

To replace the voltage doubler/bleeder assembly, refer to figure 6-32 and perform the following:

1. Turn terminal power off per procedure 1.

2. Remove hood per procedure 4.

3. Disconnect anode lead from crt (to remove, fold back suction cup and squeeze).

4. Disconnect input lead from flyback transformer.

5. Remove doubler/bleeder assembly from panel by loosening bottom screw and removing top one. If proper length screwdriver is not available, it is necessary to remove crt first (procedure 18) before screws are accessable.

6. Replace assembly by reversing preceding procedure steps. Be sure both ground wires are reattached to top mounting screw.

Procedure 20 - Replacing Touchpanel

To replace the touchpanel refer to figure 6-34 and perform the following

1. Turn terminal power off (procedure 1) and pull ac power cord from site outlet.

2. Remove terminal bezel and hood per procedure 4.

3. Disconnect touchpanel connectors from controller board.

4. Remove touchpanel by loosening four mounting bracket screws holding touchpanel to bezel.

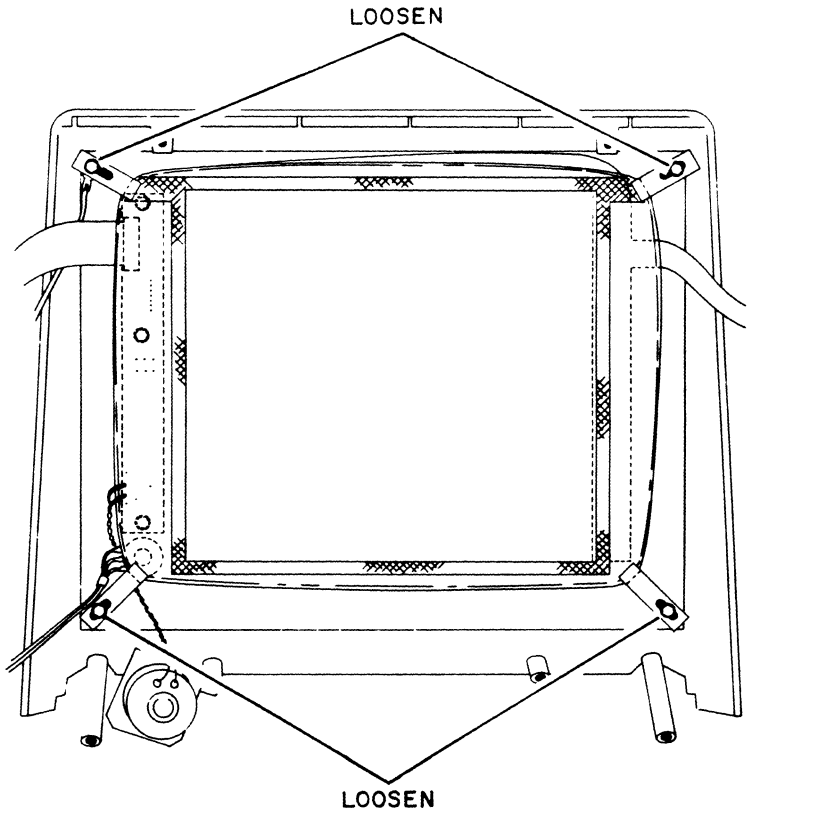


Figure 6-34. Touchpanel Removal

To install replacement touchpanel:

5. Place touchpanel in bezel opening with ribbon cable on top of bezel.

6. Align touchpanel so that etched alignment marks on panel (figure 6-35) are lined up with marks on bezel. Alignment marks on bezel are hard to see. Use a lead pencil to highlight them.

7. Carefully tighten four brackets while holding touchpanel to bezel. Check that touchpanel remains correctly aligned.

8. Check front of touchpanel for dimples in the mylar. Any dimples caused by tightening touchpanel down too tight may cause errors.

8. Reinstall bezel and hood per procedure 4.

9. Connect touchpanel connectors to controller board (see figure 6-16).

10. Perform touchpanel alignment according to procedure 5.

11. Place the defective touch panel in the shipping carton the replacement panel came in, the curved side goes down for protection.

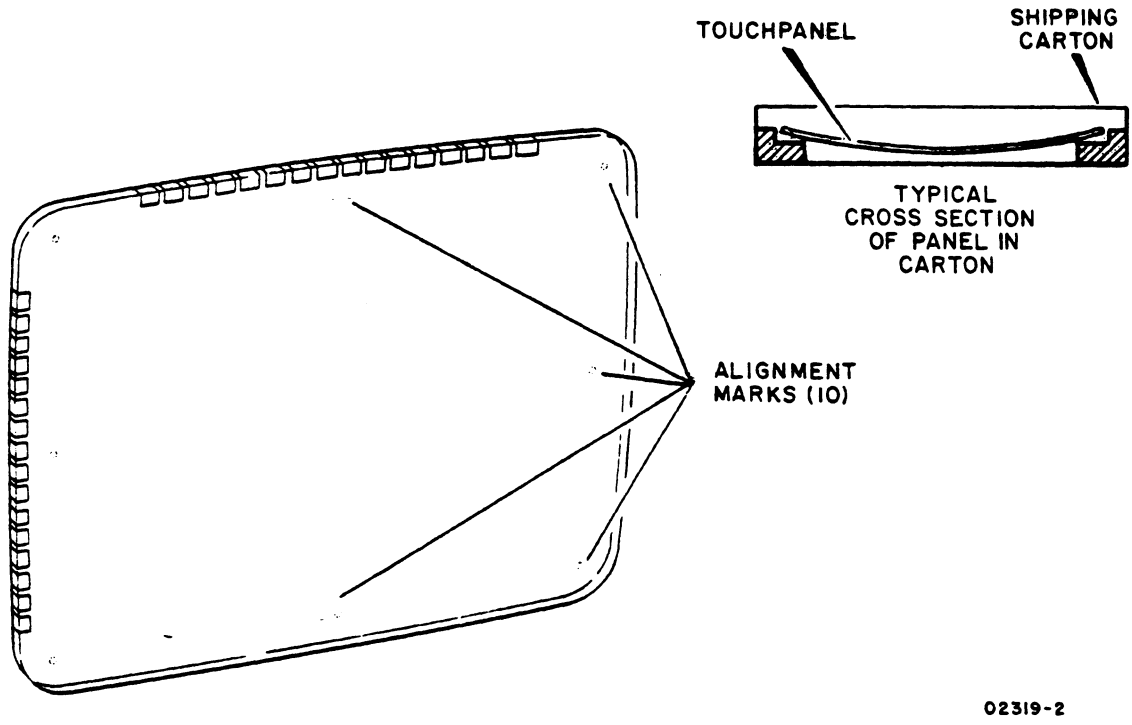


Figure 6-35. Touchpanel Alignment Marks

Procedure 21 - Replacing Internal Modem

To replace internal modem:

1. Power off terminal, remove ac power cord from site outlet.

2. Remove hood per procedure 4.

3. Disconnect telephone cables.

4. Disconnect modem cable from controller board (see figure 6-16).

5. Remove modem board by cutting tie-wraps and pulling board out.

6. Install new modem board by pressing into retainers and installing new tie-wraps.

7. Reconnect wires from telephone cable as follows:

   a. Attach red wire from connector jack marked PHONE to terminal J4 and green wire to terminal J5 of modem board.

   b. Attach red wire from connector jack marked LINE to terminal J2 and green wire to terminal J3 of modem board.

   c. Attach two black wires from both connector jacks to terminal J9 of modem board.

   d. Attach two yellow wires from both connector jacks to terminal J7 of modem board.

8. Reconnect modem cable to controller board.

9. Replace hood per procedure 4.

Procedure 22 - Checking Video Offline

Perform the following steps to check the basic function of the video board.

1. Remove terminal hood (procedure 4) and apply terminal power (procedure 1).

2. Activate the Flood Screen Switch (located on video board, see figure 6-15) to force video output to active (white) state. Entire display should appear completely white. If display is not complete, refer to CRT-3.

NOTE

Operation of the Refresh Memory Write Switch changes the contents of the refresh memory.

3. Write and display contents of refresh memory by placing Refresh Memory Write Switch (located on

video board, see figure 6-15) to the right to write all ones (white) or to the left to write all zeroes (black).

4. Examine display for any missing bits when writing all ones, and for any picked bits when writing zeroes. If bit errors are observed, perform specified actions listed in CRT-3.

Procedure 23 - Defining Acceptable Display Quality

This information is listed for reference whenever definitions of acceptable display quality are required.

Brightness -- The retrace and nonintensified scan lines should not be visible. The intensity should be set high enough for the display to be read by the user from at least 3 feet away, but not so high that the displayed data changes in size and symbols appear defocused.

Focus -- Focus is to be adjusted so that the focus at top center and extreme right center of screen is the same.

Orthogonality and Linearity -- With the line mode test pattern displayed (square with crossing diagonal lines), the pattern should appear square and coincide with the outer edges of the touchpanel grid. The point where the diagonals intersect should be equidistant from each edge of the square.

INDEX

This section contains parts data information necessary to maintain the terminal, touchpanel, modem and memory expansion. The spare parts lists are included at the beginning of this section. Table 7-1 explains the column headings of computer-generated assembly parts lists.

TABLE 7-1. EXPLANATION OF COLUMN HEADINGS OF COMPUTER-GENERATED ASSEMBLY PARTS LISTS

COLUMN HEADING	EXPLANATION
FIND NO.	Identifies an electrical or mechanical part on an assembly drawing. If more than one listing appears for a find number, refer to LI, WK IN, and WK OUT.
LI (Line Item)	Gives a chronological or historical record of the addition of a new part to a find number. For example, 01 indicates that the part was the first one used, and 02 indicates the second, etc. See also WK IN and WK OUT.
PART NUMBER	Gives the Control Data Corporation part identification. Use this number when ordering replacements.
CD (Check Digit)	Gives the information-control system a means of cross-checking the correctness of a part number.
QUANTITY	Lists the total number of a part required to complete an assembly. The vertical line near the center of the column acts as a decimal point. Numbers to the left of the line are whole numbers. Those to the right of the line are tenths, hundredths, and thousandths.
U/M (Unit of Measure)	Indicates how the information-control system counts or supplies a part.
PART DESCRIPTION	Describes the physical appearance, type, or name of a part.
MC (Material Code)	Supplies additional descriptive data to the information-control system.
YLD (Yield)	A 2-digit number that indicates the usable portion of any quantity of parts expressed as a percentage.
ECO NO. IN	Engineering Change Order that adds a new part to an assembly. See also WK IN.
ECO NO. OUT	Engineering Change Order that deletes a part from an assembly. See also WK OUT.
S/N (Serial Number)	Used to specify an ECO's effectivity by serial number.
WK IN (Week In)	Lists the date when manufacturing begins using a new part and when it is available for parts replacement. For example, 7222 means a part is available of the 22nd week of 1972.
WK OUT (Week Out)	Lists the date when manufacturing no longer uses a part in building an assembly. See also WK IN. Do not order a part after its week-out date.

0643-2A

DWN	R. Trautman	4/79
CHKD	R. Trautman	5-1-79
ENG	[signature]	5-21-79
MFG	[signature]	6-26-79
APPR	E. H. Hu	6-27-79
ES	[signature]	6/29/79

CONTROL DATA CORPORATION

CODE IDENT 15920

TITLE: SPARE PARTS LIST
IST-II BASIC TERMINAL

FIRST USED ON: FC816A/B

PREFIX	DOCUMENT NO	REV
SPL	66308093	B

SHEET 1 of 4

SHEET REVISION STATUS

4	3	2	1
—	—	—	—
01	—	—	01
02	—	02	02
A	A	A	A
A	B	A	B

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
—	50003-10	RELEASED CLASS B	—	5/21/79	[signature]
01	50702	ADD P/N 33	WJS 6-19-79		[signature]
02	50715	ADD P/N 34 & NOTE 12	RG		[signature]
A	12759-52	RELEASED CLASS "A"	/	6/27/79	[signature]
B	13635	P/N 15 WAS 51919716	WJU 8-30-79		[signature]

NOTES

1. Quantity shown is that used per equipment. Quantities for FC816A are listed under heading "A". Quantities for FC816B are listed under heading "B".

2. EQUIPMENT CONFIGURATOR-15631279 for FC816A and 15632064 for FC816B.
TOP LEVEL ASSEMBLY-15631280 for FC816A and 15632065 for FC816B.

DETACHED LISTS

AA3180 REV. 8-71

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ENTRY DATA		CODE IDENT 15920	SHEET 2	SPL	DOCUMENT NO. 66308093	REV A

3. Individual keycaps are documented in drawing 51919625 as CDC part number 51920001 thru 51920063.

4. Indicated parts are included as part of Keyboard Assy 51918093.

5. Either tool can be used. Plastic version less expensive than metal.

6. Indicated part is included as part of display PC Assy 51919715.

7. Indicated parts are included as part of 7BGD PC Assy 66308140.

8. Indicated parts are included as part of 7BFD PC Assy 90446108.

9. Only one AC Entry Assy per equipment; 61408031 for FC816A,61408032 for FC816B.

10. Xformer required for FC816B only. Not used on FC816A.

11. Other Applicable / Reference Documents,

66308604 - CDC P/N to vendor P/N cross Ref PL for Display Assy.

66308094 - SPL for Touch Panel Option (XA244-A).

66308095 - SPL for Internal Modem Option (XA247-A).

66308096 - SPL for Memory Expansion Option (XA243-A).

12. Indicated part is included as part of 7BVD PC Assy 90460843.

CONTROL DATA

CODE IDENT	SHEET	SPL	DOCUMENT NO.	REV.
15920	3		66308093	B

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED A	QUANTITY REQUIRED B	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	51918093	1	1		Keyboard Assy	
2	51919625	1	1		Keycap Set	Notes 3 & 4
3	51919695	1	1		Space Bar Mechanism	Note 4
4	51919696	64	64		Plunger	Note 4
5	51919697	64	64		Contact, Solid	Note 4
6	51919698	64	64		Contact, Quad	Note 4
7	51919699	63	63		Spring, 2 oz	Note 4
8	51919700	1	1		Spring, 3 oz	Note 4
9	51919701	1	1		64 Position Switch Housing	Note 4
10	51919702	0	0		Contact Insertion Tool, Plastic	Note 5
11	51919703	0	0		Contact Insertion Tool, Metal	Note 5
12	51919711	1	1		CRT/Yoke (Matched)	
13	51919714	1	1		Doubler/Bleeder Assy	
14	51919715	1	1		Display PC Assy	
15	51650215	1	1		Fuse .75 AMP S.B.	Note 6
16	66308140	1	1		Populated 7BGD PC Assy	
17	66308141	1	1		Programmed EROM	Note 7
18	15153821	24	24		4116 RAM (16K)	Note 7
19	90446108	1	1		7BFD PC Assy	
20	15163201	1	1		Z80A Processor	Note 8

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CONTROL DATA

CODE IDENT	SHEET	SPL	DOCUMENT NO.	REV.
15920	4		66308093	A

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED A	QUANTITY REQUIRED B	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
21	15125700	1	1		TR1602A UART	Note 8
22	90445851	1	1		8AGD PC Assy	
23	90460843	1	1		7BVD PC Assy	
24	51907757	1	1		CRT BKR/Trip Coil	
25	51911801	1	1		Brightness Pot	
26	51915101	1	1		Brightness Knob	
27	61408444	1	1		Cable Assy (COAX/BNC)	
28	61408025	1	1		Cable Assy (RIBBON)	
29	71492795	1	1		Access Door	
30	61408031	1	0		AC Entry (110 VAC)	Note 9
31	61408032	0	1		AC Entry (220 VAC)	Note 9
32	51918788	0	1		Stepdown Xformer	Note 10
33	88914700	1	1		IC 74S05	Note 6
34	51903800	6	6		LED	Note 12

AA8181 REV. 8/71

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DWN	R. Trautman	4/79	CONTROL DATA CORPORATION	TITLE SPARE PARTS LIST TOUCH PANEL OPTION	PREFIX SPL	DOCUMENT NO. 66308094	REV A
CHKD	R. Trautman	5-1-79					
ENG	[illegible]	5-24-79					
MFG	[illegible]	6-4-79					
APPR	[illegible]	6-27-79	CODE IDENT 15920	FIRST USED ON FC816A/B		SHEET 1 of 2	

SHEET REVISION STATUS

2	1
–	–
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
–	60003.10	RELEASED CLASS B	–	5/21/79	[illegible]
A	127545	RELEASED CLASS "A"	/	6/27/79	[illegible]

NOTES

1. Quantity shown is that used per equipment

2. EQUIPMENT CONFIGURATOR---------15632062
   TOP LEVEL ASSEMBLY-------------15632146

DETACHED LISTS

AA3180 REV. 8 71

PRINTED IN U.S.A.

[redacted]		CODE IDENT 15920	SHEET 2	SPL	DOCUMENT NO. 66308094	REV. A

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	61408448	1		Touch Panel And Gasket Assy	

AA3181 REV. 8/71

PRINTED IN U.S.A.

DWN	R. Trautman	4/25	CONTROL DATA CORPORATION	TITLE	PREFIX	DOCUMENT NO	REV
CHKD	R. Trautman	5-1-79		SPARE PARTS LIST INTERNAL MODEM OPTION	SPL	66308095	B
ENG	[illegible]	5-21-79					
MFG	[illegible]	6-26-9		FIRST USED ON		SHEET	
APPR	[illegible]	5-27-79	CODE IDENT 15920	FC816A/B		1 of 2	
QS	[illegible]	[illegible]					

SHEET REVISION STATUS

2	1
–	–
A	A
B	B

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
–	60003-10	RELEASED CLASS B	–	5/21/79	[illegible]
A	12754-52	RELEASED CLASS A"	/	5/27/79	Mch
B	13635	REVISED PER ECO	[illegible] 6-20-79		6/28

NOTES
1. Quantity shown is that used per equipment.
2. EQUIPMENT CONFIGURATOR--------15632110
   TOP LEVEL ASSEMBLY------------15632145

DETACHED LISTS

AA3180 REV. 8/71 PRINTED IN U.S.A.

[redacted]

CODE IDENT	SHEET		DOCUMENT NO	REV.
15920	2	SPL	66308095	B

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	90445982	1			8CHD PC Assy	
2	51917910	2			Cable Assy	
3	51917907	1			Cable Assy	(To Wall Jack)
4	51777315	3			Support Ckt Bd	

AA3181 REV. 8/71 PRINTED IN U.S.A.

DWN	R. Trautman	4/79
CHKD		5-1-79
ENG		5/4/79
MFG		6-26-79
APPR		6-27-79
CB		

CONTROL DATA CORPORATION

CODE IDENT 15920

TITLE: SPARE PARTS LIST
MEMORY EXPANSION OPTION

FIRST USED ON: FC816A/B

PREFIX	DOCUMENT NO	REV
SPL	66308096	A

SHEET 1 of 2

SHEET REVISION STATUS

2	1
-	-
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
-	60003-10	RELEASED CLASS B	-	5/4/79	
A	132543-58	RELEASED CLASS "A"	/	6/27/79	

NOTES
1. Quantity shown is that used per equipment.
2. EQUIPMENT CONFIGURATOR--------15632060
   TOP LEVEL ASSEMBLY ----------15632061

DETACHED LISTS

AA3180 REV. 8/71 PRINTED IN U.S.A.

[redacted]

CODE IDENT	SHEET	SPL	DOCUMENT NO.	REV.
15920	2	SPL	66308096	A

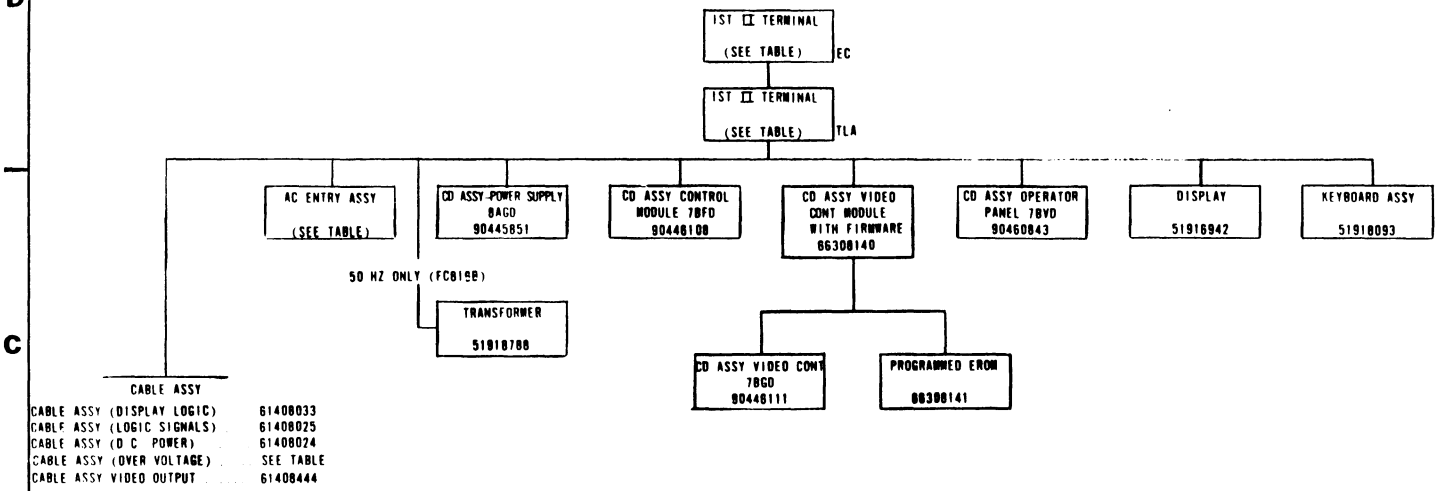
FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	15153821	8	PC		4116 RAM (16K)	

AA3181 REV. 8/71 PRINTED IN U.S.A.

	60 HZ	50 HZ
EC	15631279	15632064
TLA	15631280	15632065
A C ENTRY ASSY	61408031	61408032
CABLE ASSY (OVER VOLTAGE)	61408023	61408447

SHEET REVISION STATUS

REVISION RECORD						
REV	CO	DESCRIPTION	DRFT	DATE	CHKD	APP
-	50002-59	RELEASED CLASS B	-	1/19/79	-	
C1	50572	DELETED OPTIONS FROM UNITS/REPAIR AND ADDED TO	RL	3-21-79	RL	
02	50649	ADD SPARE PARTS LIST	WJG	5-10-79	WJ	
03	50698	REVISE PER ECO	WJG	6-18-79	WJ	
A	11565-53	RELEA. EC [illegible]		8/6/79	/	



CABLE ASSY

CABLE ASSY (DISPLAY LOGIC)	61408033
CABLE ASSY (LOGIC SIGNALS)	61408025
CABLE ASSY (D C POWER)	61408024
CABLE ASSY (OVER VOLTAGE)	SEE TABLE
CABLE ASSY VIDEO OUTPUT	61408444

REFERENCE DOCUMENTS

EC TOUCH PANEL OPTION KIT	15632062
EC MODEM OPTION KIT	15632110
EC MEMORY EXPANSION OPTION KIT	15632060
ENGINEERING SPEC	16042809
LOGIC SET	62201041
ON SITE REPAIR CENTER HARDWARE MAINTENANCE MANUAL	82100083
SPARE PART LISTS FC816A,B	66308093
TOUCH PNL OPTION	66308094
MODEM OPTION	66308095
MEMORY EXP	66308096
RELIABILITY TEST PLAN REPORT	66308546
DESIGN VERIFICATION TEST PLAN/REPORT	66306660
PRODUCT VERIFICATION TEST PLAN REPORT	66308906

WRITER'S NOTE

REFER TO FIGURES IN SECTION 6 FOR LOCATION OF TERMINAL ASSEMBLIES.

REFERENCE DRAWING	CONTROL DATA		
	FIRST USED ON	FC816A&B	
	DWN	WJ Blasen	1-9-79
	CHKD	[illegible]	1-17-79
	ENGR	[illegible]	1-16-79
	MFG	[illegible]	8-01-79
	APPR	[illegible]	8-8-79

COMPONENTS, EXCEPT AS NOTED

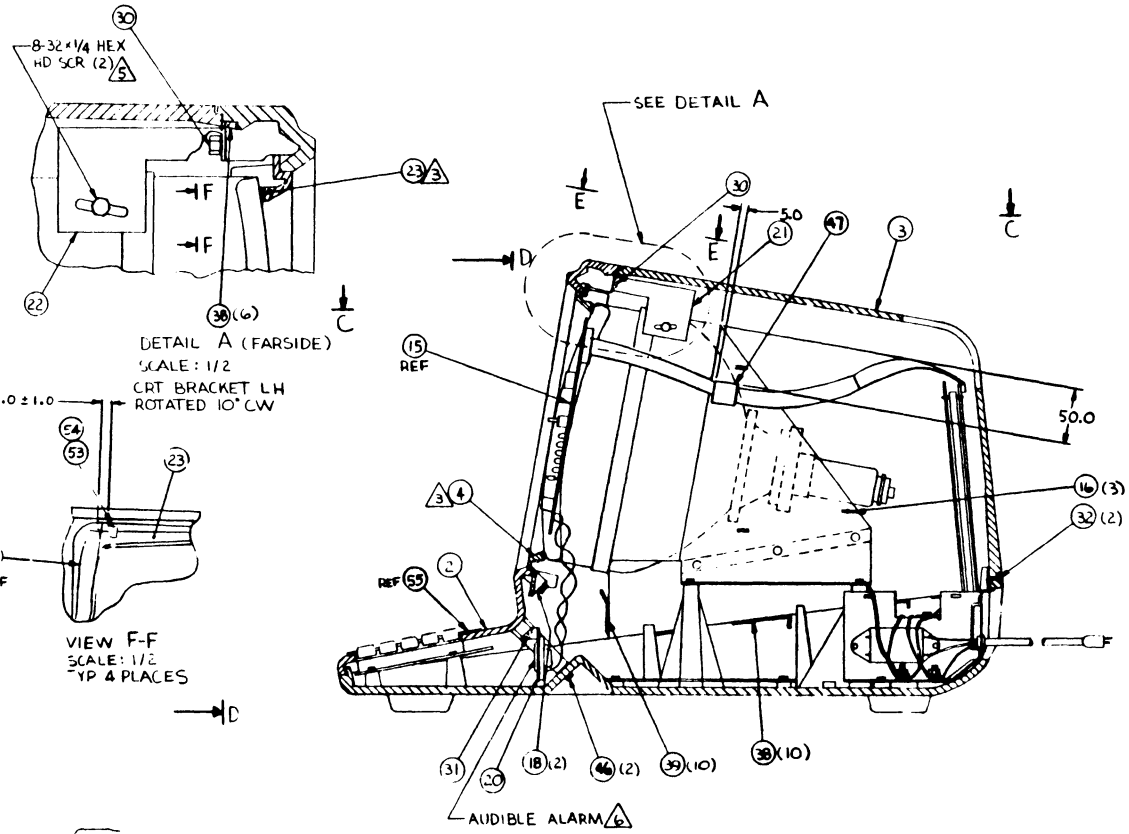
	TOLERANCE	VALUE	RATING
RES			
CAP			

TITLE: GENEALOGY
IST-II 50/60 HZ

CODE IDENT 15920 | C | DRAWING NO 66304578

SCALE | CROSS REF NO | SHEET 1 OF 1

66304578



REVISION RECORD								
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
–	2000E-52	RELEASED CLASS B				
01	50480	PL CHGS ONLY				
02	50632	ADD D SIZE PLUGS, PL CHGS				
03	50662	ADD CABLES, PL CHGS				
04	50682	PL CHGS				
05	50687	DELETE F/N'S				
CD	50739	NOTE 3: F/N 35, F/N 41 WAS [illegible], F/N [illegible] WAS 5900370, F/N [illegible] WAS 7149970				
07	50749	ADD F/N 53,56,57 F/N 34 WAS NO 7				
A	13656	APL CHANGE ONLY				
B	13666	REVISED PER ECO				

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS (MM) UNLESS OTHERWISE SPECIFIED.
2. MARK "ASSY 15632065" IN AREA SHOWN PER CDC SPEC 10121508.
3. F/N 23 IS APPLIED ACROSS THE TOP, BOTTOM, & UP RIGHT SIDE OF OPENING IN F/N 4.
4. F/N 24 IS APPLIED UP LEFT SIDE OF OPENING IN F/N 4. MUST NOT EXTEND INTO OPENING.
5. FURNISHED AS PART OF F/N 8.
6. FURNISHED AS PART OF F/N 15.
7. TERMINALS INTERCHANGEABLE.
8. DISCARD FIBER GASKET FROM F/N 37.
9. FURNISHED AS PART OF F/N 14

METRIC

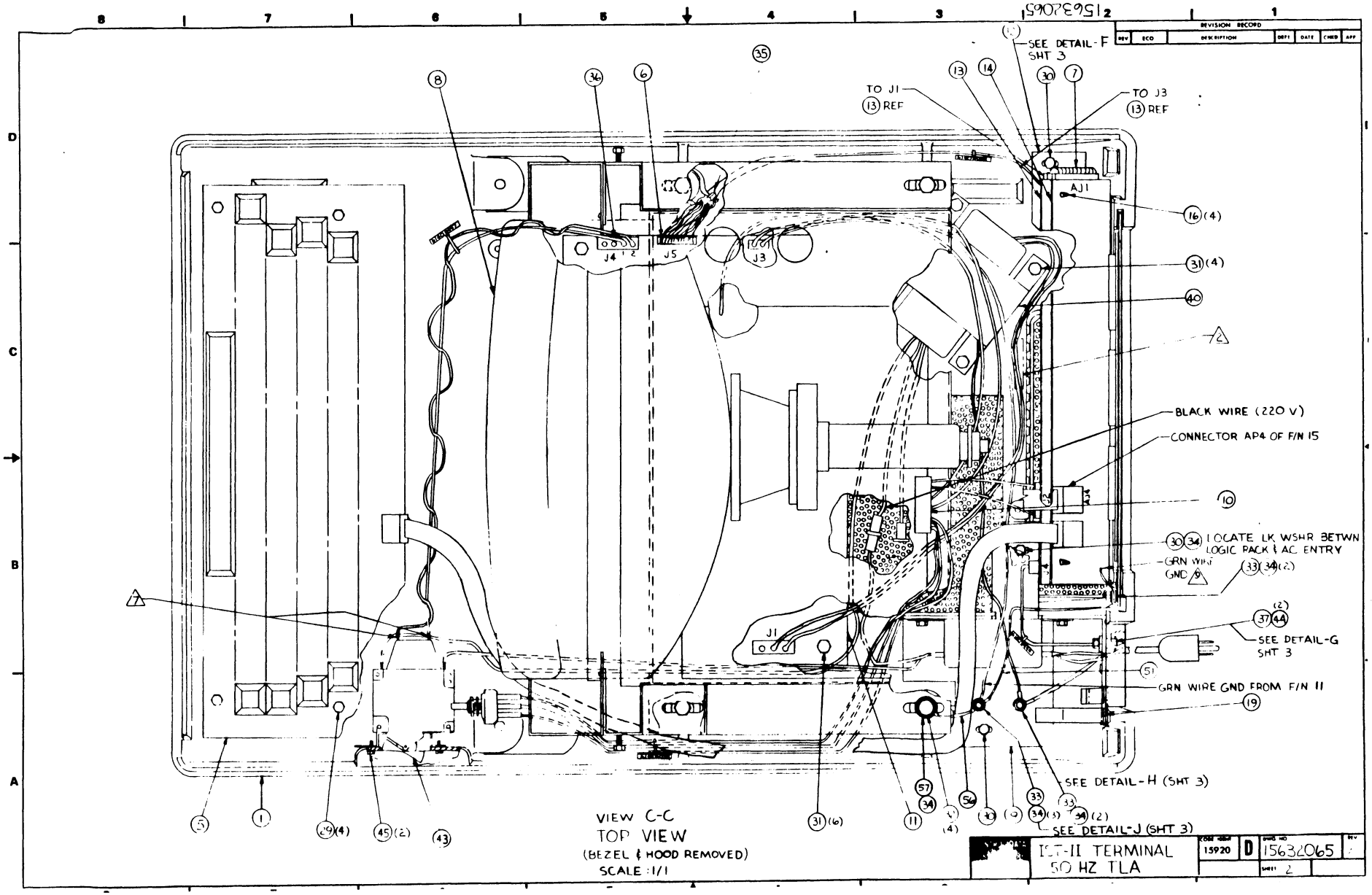
APL 15632065

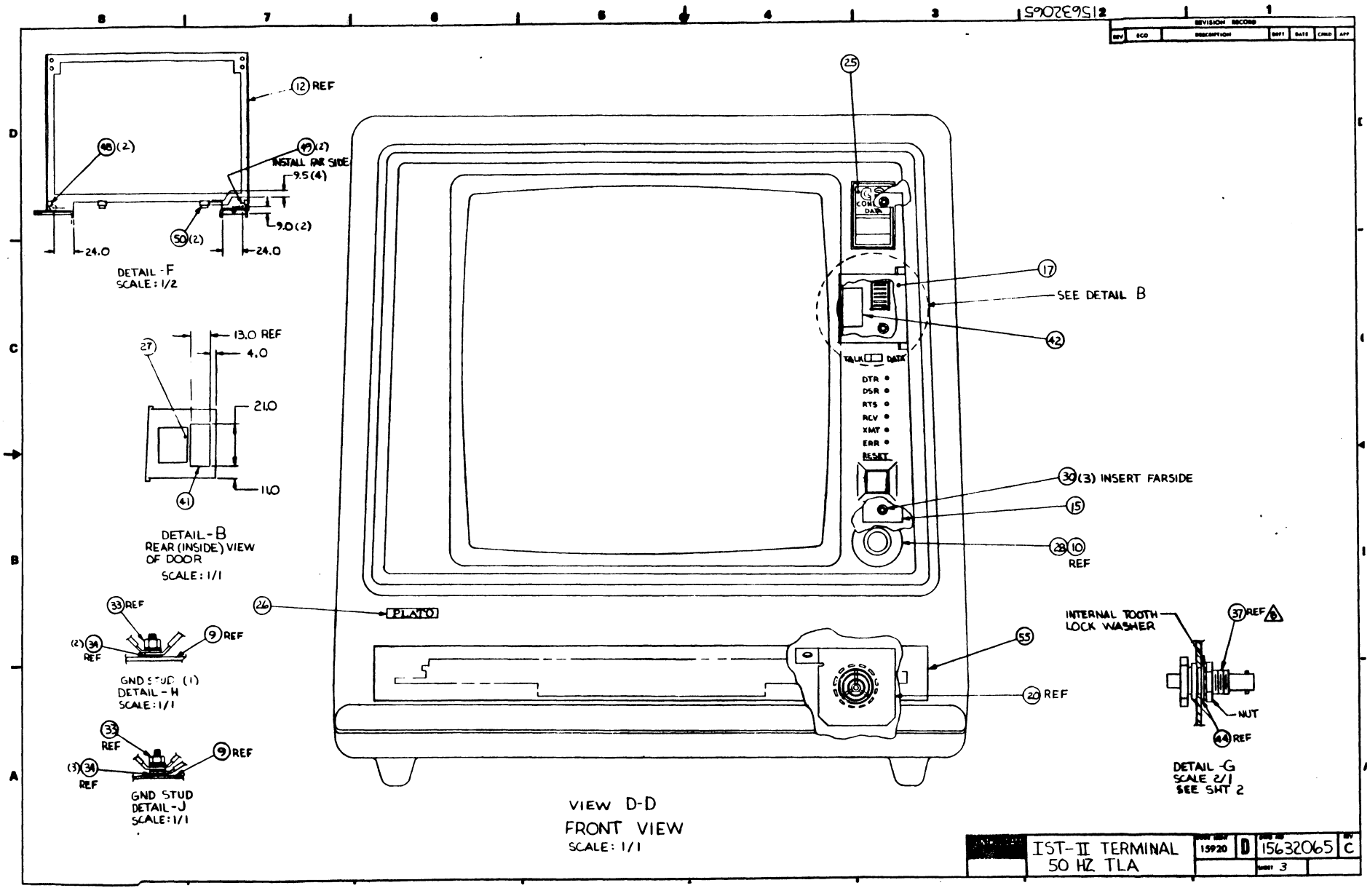
DO NOT SCALE DRAWING

TITLE: IST-II TERMINAL 50 HZ TLA

FSCM NO. 15920 | SIZE D | DRAWING NO 15632065

SCALE 1/2 | NEXT ASSY 15632064 | SHEET 1 OF 3


SEE DETAIL-F SHT 3
TO J1 (13) REF
TO J3 (13) REF
BLACK WIRE (220 V)
CONNECTOR AP4 OF F/N 15
LOCATE LK WSHR BETWN LOGIC PACK & AC ENTRY
GRN WIRE GND
SEE DETAIL-G SHT 3
GRN WIRE GND FROM F/N 11
SEE DETAIL-H (SHT 3)
SEE DETAIL-J (SHT 3)
VIEW C-C
TOP VIEW
(BEZEL & HOOD REMOVED)
SCALE: 1/1
IST-II TERMINAL
50 HZ TLA
15920
D
15632065


REVISION RECORD
12 REF
48 (2)
49 (2) INSTALL PAR SIDE
9.5 (4)
9.0 (2)
50 (2)
24.0
24.0
DETAIL - F
SCALE: 1/2
13.0 REF
4.0
21.0
11.0
27
41
DETAIL - B
REAR (INSIDE) VIEW
OF DOOR
SCALE: 1/1
33 REF
(2) 34 REF
9 REF
GND STUD (1)
DETAIL - H
SCALE: 1/1
33 REF
(3) 34 REF
9 REF
GND STUD
DETAIL - J
SCALE: 1/1
25
17
SEE DETAIL B
42
TALK DATA
DTR
DSR
RTS
RCV
XMT
ERR
RESET
39 (3) INSERT FARSIDE
15
28 10 REF
26
PLATO
55
20 REF
VIEW D-D
FRONT VIEW
SCALE: 1/1
INTERNAL TOOTH LOCK WASHER
37 REF
NUT
44 REF
DETAIL - G
SCALE 2/1
SEE SHT 2
IST-II TERMINAL
50 HZ TLA
15920
D
15632065
C
SHEET 3

BUILD ARC 440

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
09-10-79	1	00013666

DIV	ASSEMBLY NUMBER	CD	REV	DWG	DESCRIPTION	ARC	STATUS	STATUS DATE	ENG. RESP	FILE DATE
0860	15632065	7	C	D	TERM, IST-II C/D/K 50HZ (TA)	N	REL	08-09-79	FC816B	09-10-79

T	FIND NO	LI	PART NUMBER	CD	RA	QUANTITY		U/M	PART DESCRIPTION	ARC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	001	01	71492480	0		1		PC	BASE, PAINTED W/SHLD (WHT)	P						
	002	01	71492748	2		1		PC	BEZEL, PAINTED W/SHLD (WHT)	P						
	003	01	71492483	4		1		PC	HOOD, PAINTED W/SHLD (WHT)	P						
	004	01	71492753	3		1		PC	BEZEL INSERT	P						
	005	01	51918093	9		1		PC	KYBD MODULE 64KEY	P						
	006	01	61408024	0		1		PC	CABLE ASSY, LOGIC DC	A						
	007	01	61408025	7		1		PC	CABLE ASSY, BRD INTC	A						
	008	01	51916942	9		1		PC	CRT, 15IN PH/P4 W-RSLTN SHORT	P						
	009	01	61408032	3		1		PC	AC ENTRY ASSY (50HZ 220V)	A						
	010	01	61408033	1		1		PC	CABLE ASSY, DISPLAY LOGIC	A						
	011	01	90445851	0		1		PC	PWR SUPPLY 8AGD	A						
	012	01	71492484	2		1		PC	BRACKET, PCB	P						
	013	01	66308140	4		1		PC	MODULE W/FIRMWARE	N						
	014	01	90446108	4		1		PC	PC CD ASSY 7BFD	S						
	015	01	90460843	7		1		PC	CD ASSY 7BVD OP PANEL	A						
	016	01	51777315	6		7		PC	SUPPORT CKT BD	P						
	017	01	71492795	1		1		PC	DOOR	P						
	018	01	93539009	6		2		PC	FASTENER PUSH ON TYPE C	P						
	019	01	71492804	1		1		PC	PLATE AC ENTRY	P						
	020	01	71492749	8		1		PC	ALARM BRACKET	P						
	021	01	71492750	6		1		PC	CRT BRACKET RH	P						

BUILD ARC 440

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
09-10-79	2	00013666

DIV	ASSEMBLY NUMBER	CD	REV	DWG	DESCRIPTION	ARC	STATUS	STATUS DATE	ENG. RESP	FILE DATE
0860	15632065	7	C	D	TERM, IST-II C/D/K 50HZ (TA)	N	REL	08-09-79	FC816B	09-10-79

T	FIND NO	LI	PART NUMBER	CD	RA	QUANTITY		U/M	PART DESCRIPTION	ARC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	022	01	71492751	4		1		PC	CRT BRACKET LH	P						
	023	01	51803904	5		2	250	FT	TAPE, NEO SELF-ADH 1/4WX1/8T	B						
	024	01	95670603	0			850	FT	TAPE MYLAR	B						
	025	01	71492817	3		1		PC	NAME PLATE ALUM	P						
	026	01	71492805	8		1		PC	LABEL	P						
	027	01	66307647	9		1		PC	LABEL SWITCH SETTING	P						
	028	01	51915101	3		1		PC	KNOB, P-O SKIRTED/INSERT PLN	P						
	029	01	15164916	7		4		PC	MSCR HEX-LK PLN M4X22MM STL Z	B						
	030	01	15164911	8		8		PC	MSCR HEX-LK PLN M4X8MM STL ZP	B						
	031	01	15165013	2		11		PC	SCR TPG HEX PLN M4.5X13MM STL	B						
	032	01	15164919	1		8		PC	MSCR HEX-LK PLN M5X13MM STL Z	B			13666			7947
	032	02	15164919	1		6		PC	MSCR HEX-LK PLN M5X13MM STL Z	B		13666			7947	
	033	01	91975724	5		2		PC	NUT HEXAGON SZ 5MM	B						
	034	01	91975671	8		9		PC	WASHER EX TOOTH SZ 5	B						
	035	01	94277411	8		1		PC	STRAP, CBL TIE TYP 1 TO 1-1/8	B						
	036	01	61408447	3		1		PC	CABLE ASSY OVERVOLTAGE	A						
	037	01	61408444	0		1		PC	CABLE ASSY-VIDEO OUTPUT	A						
	038	01	51918752	0		18		PC	SPRING FINGER FIG 2	P			13666			7947
	038	02	51918752	0		16		PC	SPRING FINGER FIG 2	P		13666			7947	
	039	01	51918753	8		10		PC	SPRING FINGER FIG 3	P						
	040	01	51918788	4		1		PC	XFMR STEP-DOWN	P						
	041	01	51940554	2			070	FT	TAPE MAGNETIC FLEXIBLE	B			13656			7934

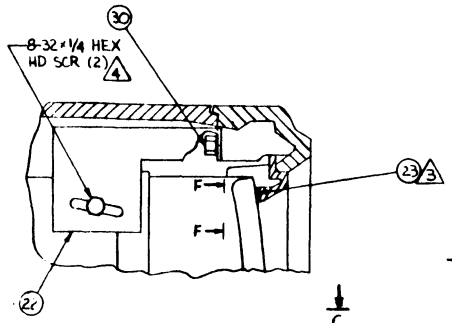
BUILD ARC 440

ASSEMBLY PARTS LIST

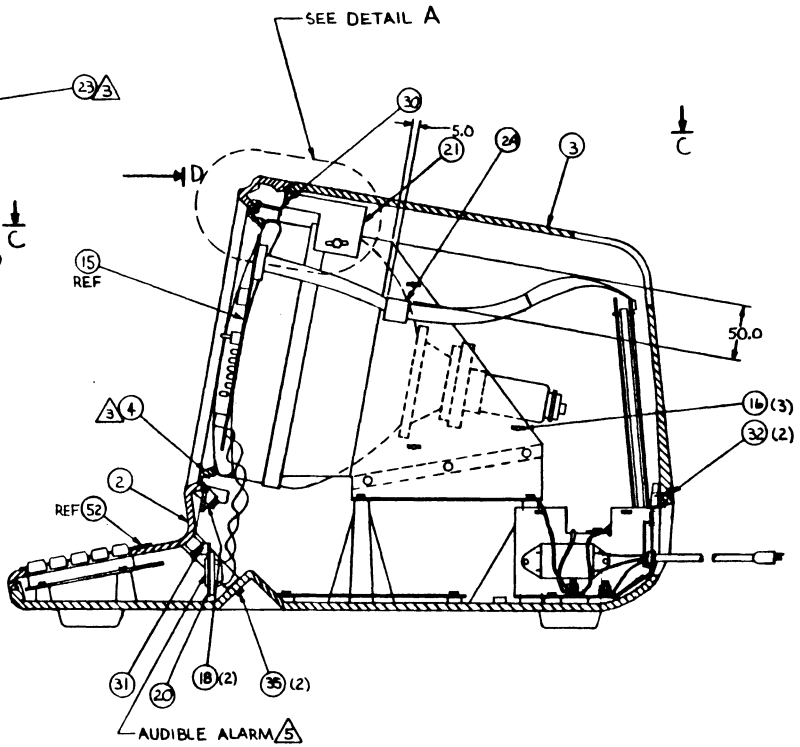
PRINT DATE	PAGE	FILE CYCLE NO.
09-10-79	3	00013666

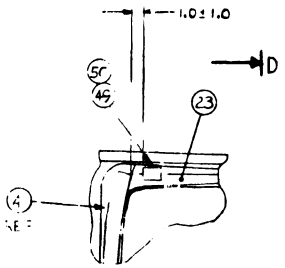
DIV	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	MC	STATUS	STATUS DATE	ENG. RESP.	FILE DATE
0860	15632065	7	C	D	TERM, IST-II C/D/K 50HZ (TA)	N	REL	08-09-79	FC816B	09-10-79

T	FIND NO	LI	PART NUMBER	CD	QUANTITY	U/M	PART DESCRIPTION	MC	YLD	ECO NO. IN	ECO NO. OUT	S/N	WK IN	WK OUT
	041	02	51940544	3	070	FT	TAPE MAG .500 WIDTH .036THICK	B		13656			7934	
	042	01	71492926	2	1	PC	PLATE STRIKER	P						
	043	01	51907757	2	1	PC	CB W/TRIP COIL 1/6 2.5A 250V	P						
	044	01	51589600	9	2	PC	BUSHING INSU	P						
	045	01	00860303	7	2	PC	MSCR HEX-LK PLN 6-32X3/8 STL	B						
	046	01	15164920	9	2	PC	SCR MET HEX M5	B		13666			7947	
	047	01	94241017	6	1	PC	CLIP CABLE ADH BACK TYPE VII	W						
	048	01	24534709	1	060	FT	SLVG, 1/4 HT/SHRINK BLK UL	B		13666			7947	
	049	01	51805700	5	2	PC	BUMPER SELF STICKING	P						
	050	01	24534712	5	125	FT	SLVG, 1/2 HT/SHRINK BLK UL	B			13666			7947
	050	02	24534710	9	060	FT	SLVG, 3/8 HT/SHRINK BLK UL	B		13666			7947	
	051	01	61391105	6	1	PC	GND WIRE ASSY (7.5IN 16AWG)	A						
	053	01	71492970	0	4	PC	BUMPER, TOUCH PANEL	P						
	054	01	00817600	0	005	OZ	ADH, RUB BASED (3M EC-1099)	B			13666			7947
	054	02	94850711	6	005	OZ	SEAL, EASTMAN CLR (910)	B		13666			7947	
	055	01	71492925	4	1	PC	MASK KYBD IST 2	P						
	056	01	61391116	3	1	PC	GND WIRE ASSY (5.5IN 16AWG)	A						
	057	01	91975617	1	1	PC	WASHER METRIC FLAT SCR SZ 5	B						
							0061 TOTAL LINES							



DETAIL A (FARSIDE)
SCALE: 1/2
CRT BRACKET LH
ROTATED 10° CW





VIEW F-F
SCALE: 1/2
TYP 4 PLACES

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS (MM) UNLESS OTHERWISE SPECIFIED.
2. MARK "ASSY 15631280" IN AREA SHOWN PER CDC SPEC 10121508.
3. F/N 23 IS APPLIED ACROSS THE TOP, BOTTOM, & UP RIGHT SIDE OF OPENING IN F/N 4.
4. FURNISHED AS PART OF F/N 8.
5. FURNISHED AS PART OF F/N 15.
6. TERMINALS INTERCHANGEABLE
7. DISCARD FIBER GASKET FROM F/N 37.
8. FURNISHED AS PART OF F/N 14

SHEET REVISION STATUS 3 2 1	REV	ECO	DESCRIPTION	BRKT	DATE	CHKD	APP
	-	70008-42	RELEASED CLASS B	-	10-3-79	-	-
	01	50446	P.L CHGS ONLY	W/G	10-7-79	WJ	
	02	50619	ADD 2 SHT NOTES P.L CHGS	W/G	10-17-79	WJ	
	03	50624	P.L CHGS ONLY	W/G	10-17-79	WJ	
	04	50649	ADD △6 DETAIL E	W/G	11-7-79	WJ	
	05	50662	ADD DTL F / P.L CHGS	W/G	11-27-79	WJ	
	06	50682	P.L CHGS	W/G	12-7-79	WJ	
	07	50687	DELETE P/NS 41,44,45,47	W/G	12-7-79	WJ	
	08	50738	ADD NOTE 8, F/N 38 WAS 5194054-4, F/N 19 WAS 7149076, F/N 41 WAS 9427741, F/N 49 WAS 7149287Q	W/G	1-7-79	WJ	
	09	50749	ADD P/NS 52,53,54 P/N 34 CHANGED WAS 7	W/G	2-2-79	WJ	
A	A	A	11565-52 RELEASED CLASS B	/	4/19/79	/	
B	B	B	13656 APL CHANGE ONLY	W/G	8-31-79	WJ	
C	C	C	13666 REVISED PER ECO	W/G	9-12-79	WJ	

METRIC

APL 15631280

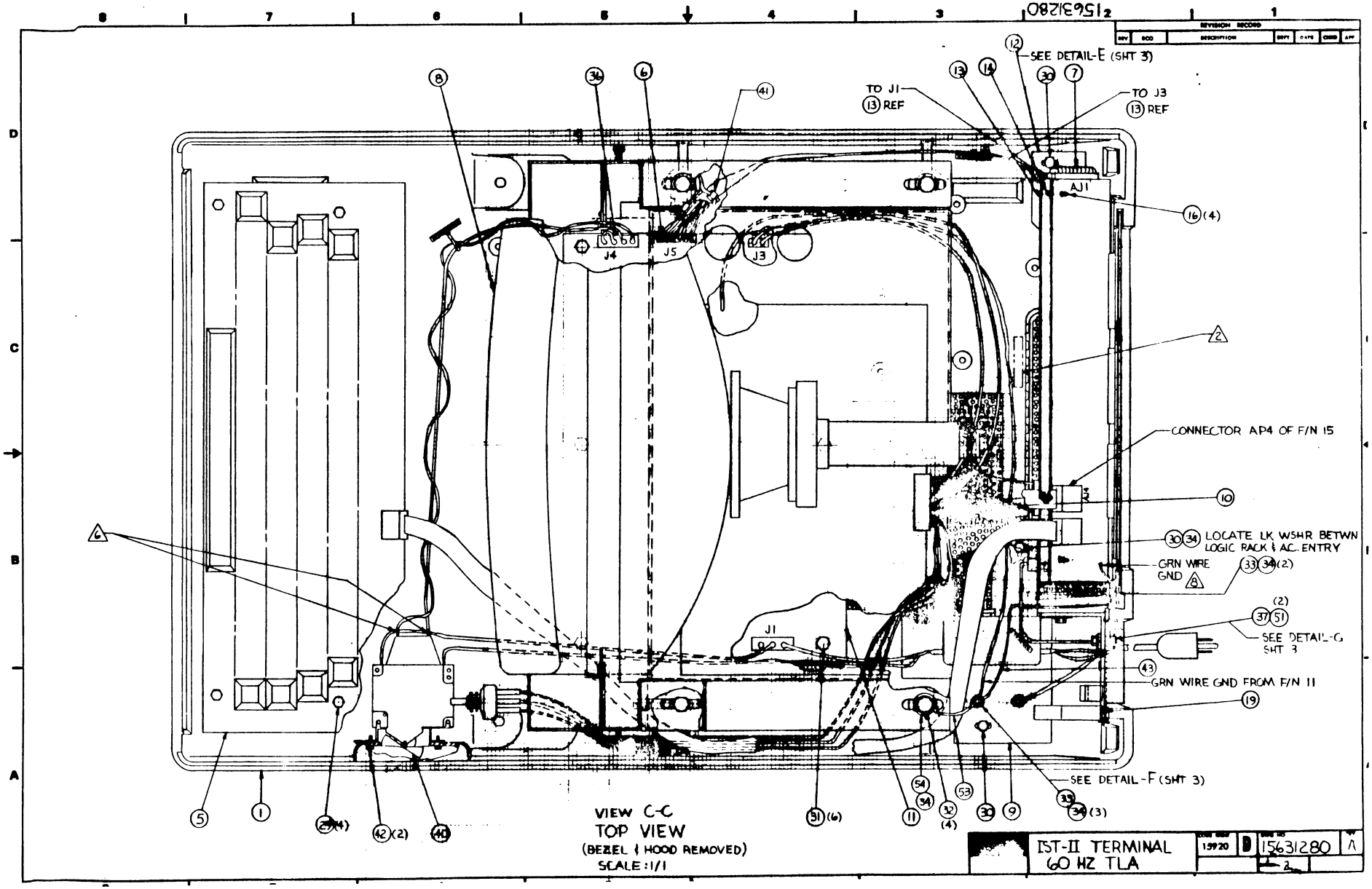
DO NOT SCALE DRAWING

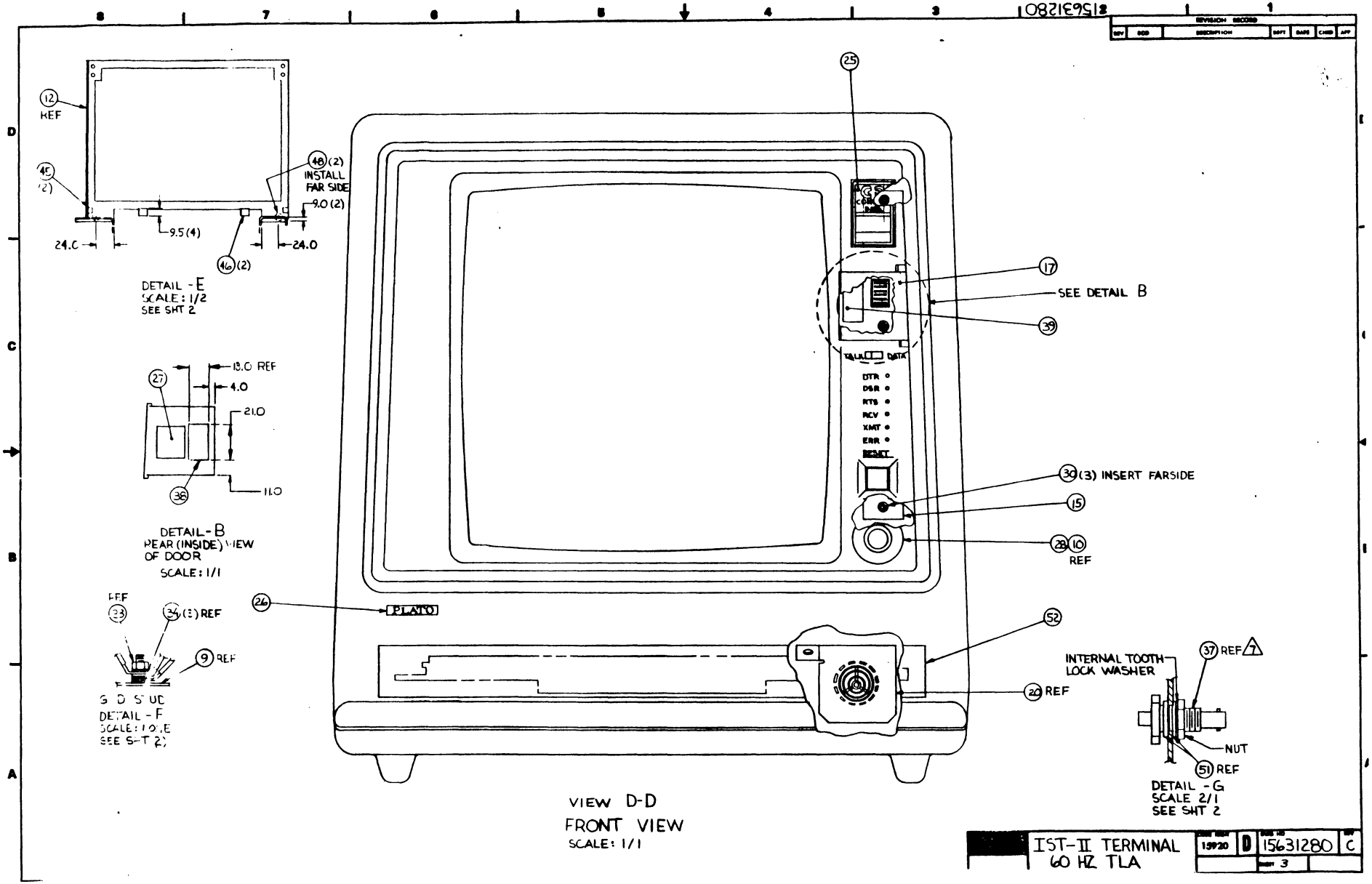
FC816A

IST-II TERMINAL
60 HZ TLA

15920 D 15631280

1/2 15631279 1 OF 3


15631280
SEE DETAIL-E (SHT 3)
TO J1
13 REF
TO J3
13 REF
J4
J5
J3
J1
AJ1
16 (4)
2
CONNECTOR AP4 OF F/N 15
10
30 34 LOCATE LK WSHR BETWN LOGIC RACK & AC. ENTRY
GRN WIRE GND
33 34 (2)
37 51 (2)
SEE DETAIL-G SHT 3
43
GRN WIRE GND FROM F/N 11
19
SEE DETAIL-F (SHT 3)
VIEW C-C
TOP VIEW
(BEZEL & HOOD REMOVED)
SCALE: 1/1
IST-II TERMINAL
60 HZ TLA
15920
15631280


12 REF
45 (2)
48 (2) INSTALL FAR SIDE
9.0 (2)
9.5 (4)
24.0
24.0
46 (2)
DETAIL - E
SCALE: 1/2
SEE SHT 2
25
17
SEE DETAIL B
39
TALK DATA
DTR
DSR
RTS
RCV
XMT
ERR
RESET
30 (3) INSERT FARSIDE
15
28
10
REF
18.0 REF
4.0
21.0
11.0
27
38
DETAIL - B
REAR (INSIDE) VIEW
OF DOOR
SCALE: 1/1
26
PLATO
52
20 REF
REF
33
34 (3) REF
9 REF
DETAIL - F
SCALE: 10/1
SEE SHT 2
INTERNAL TOOTH
LOCK WASHER
37 REF 7
NUT
51 REF
DETAIL - G
SCALE 2/1
SEE SHT 2
VIEW D-D
FRONT VIEW
SCALE: 1/1
IST-II TERMINAL
60 HZ TLA
15631280
C
SHEET 3

BUILD ARC 440

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
09-10-79	1	00013666

DIV.	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	MC	STATUS	STATUS DATE	ENG. RESP.	FILE DATE
0860	15631280	3	C	D	TERM, IST-II C/D/K 60HZ (TA)	N	REL	08-09-79	FC816A	09-10-79

T	FIND NO	LI	PART NUMBER	CD	ML	QUANTITY		U/M	PART DESCRIPTION	MC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	001	01	71492479	2		1		PC	BASE, PAINTED W/O SHLD (WHT)	P						
	002	01	71492747	2		1		PC	BEZEL, PAINTED W/O SHLD (WHT)	P						
	003	01	71492482	6		1		PC	HOOD, PAINTED W/O SHLD (WHT)	P						
	004	01	71492752	2		1		PC	BEZEL INSERT	P						
	005	01	51918093	9		1		PC	KYBD MODULE 64KEY	P						
	006	01	61408024	0		1		PC	CABLE ASSY, LOGIC DC	A						
	007	01	61408025	7		1		PC	CABLE ASSY, BRD INTC	A						
	008	01	51916942	9		1		PC	CRT, 15IN PH/P4 H-RSLTN SHORT	P						
	009	01	61408031	5		1		PC	PANEL ASSY (AC ENTRY)	A						
	010	01	61408033	1		1		PC	CABLE ASSY, DISPLAY LOGIC	A						
	011	01	90445851	6		1		PC	PWR SUPPLY 8AGD	A						
	012	01	71492484	2		1		PC	BRACKET, PCB	P						
	013	01	66308140	4		1		PC	MODULE W/FIRMWARE	N						
	014	01	90446108	4		1		PC	PC CD ASSY 7BFD	S						
	015	01	90460843	7		1		PC	CD ASSY 7BVD OP PANEL	A						
	016	01	51777315	6		7		PC	SUPPORT CKT BD	P						
	017	01	71492795	1		1		PC	DOOR	P						
	018	01	93539009	6		2		PC	FASTENER PUSH ON TYPE C	P						
	019	01	71492804	1		1		PC	PLATE AC ENTRY	P						
	020	01	71492749	8		1		PC	ALARM BRACKET	P						
	021	01	71492750	6		1		PC	CRT BRACKET RH	P						

BUILD ARC 440

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
09-10-79	2	00013666

DIV.	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	MC	STATUS	STATUS DATE	ENG. RESP.	FILE DATE
0860	15631280	3	C	D	TERM, IST-II C/D/K 60HZ (TA)	N	REL	08-09-79	FC816A	09-10-79

T	FIND NO	LI	PART NUMBER	CD	ML	QUANTITY		U/M	PART DESCRIPTION	MC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	022	01	71492751	4		1		PC	CRT BRACKET LH	P						
	023	01	51803904	5		2	250	FT	TAPE, NEO SELF-ADH 1/4"X1/8T	B						
	024	01	94241017	6		1		PC	CLIP CABLE ADH BACK TYPE VII	W						
	025	01	71492817	3		1		PC	NAME PLATE ALUM	P						
	026	01	71492805	8		1		PC	LABEL	P						
	027	01	66307647	9		1		PC	LABEL SWITCH SETTING	P						
	028	01	51915101	3		1		PC	KNOB, P-O SKIRTED/INSERT PLN	P						
	029	01	15164916	7		4		PC	MSCR HEX-LK PLN M4X22MM STL Z	B						
	030	01	15164911	8		8		PC	MSCR HEX-LK PLN M4X8MM STL ZP	B						
	031	01	15165013	2		7		PC	SCR TPG HEX PLN M4.5X13MM STL	B						
	032	01	15164919	1		8		PC	MSCR HEX-LK PLN M5X13MM STL Z	B			13666			7947
	032	02	15164919	1		6		PC	MSCR HEX-LK PLN M5X13MM STL Z	B		13666			7947	
	033	01	91975724	5		2		PC	NUT HEXAGON SZ 5MM	B						
	034	01	91975671	8		9		PC	WASHER EX TOOTH SZ 5	B						
	035	01	15164920	9		2		PC	SCR MET HEX M5	B		13666			7947	
	036	01	61408023	2		1		PC	CABLE ASSY OVER-VOLTAGE	A						
	037	01	61408444	0		1		PC	CABLE ASSY-VIDEO OUTPUT	A						
	038	01	51940554	2			070	FT	TAPE MAGNETIC FLEXIBLE	B			13656			7934
	038	02	51940544	3			070	FT	TAPE MAG .500 WIDTH .036THICK	B		13656			7934	
	039	01	71492926	2		1		PC	PLATE STRIKER	P						
	040	01	51907757	2		1		PC	CB W/TRIP COIL 1/6 2.5A 250V	P						
	041	01	94277411	8		1		PC	STRAP, CBL TIE TYP 1 TO 1-1/8	B						

BUILD ARC 440

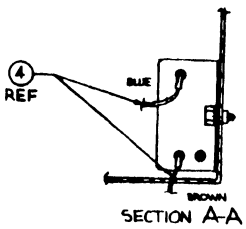
ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
09-10-79	3	000.3666

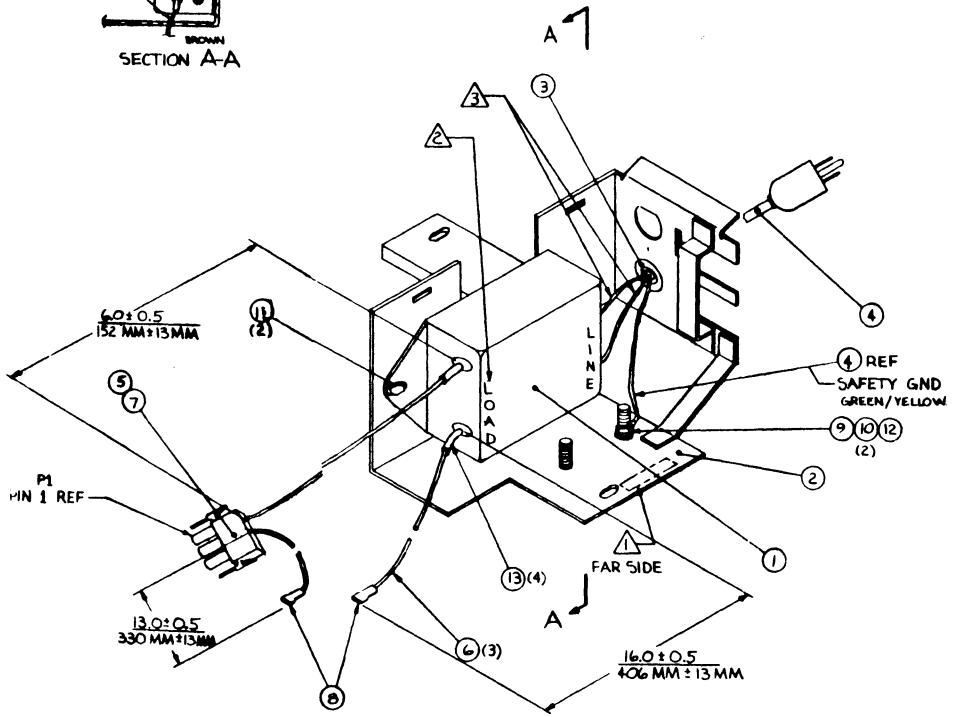
DIV.	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	INC	STATUS	STATUS DATE	ENG. RESP.	FILE DATE
0860	15631280	3	C	D	TERM, IST-II C/D/K 60HZ (TA)	N	REL	08-09-79	FC816A	09-10-79

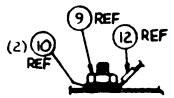
T	FIND NO	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	INC	YLD	ECO NO IN	ECO NO OUT	S/N	WK IN	WK OUT
	042	01	00860303	7	2		PC	MSCR HEX-LK PLN 6-32X3/8 STL	B						
	043	01	61391105	6	1		PC	GND WIRE ASSY (7.5IN 16AWG)	A						
	045	01	24534709	1		060	FT	SLVG, 1/4 HT/SHRINK BLK UL	B		13666			7947	
	046	01	24534712	5		125	FT	SLVG, 1/2 HT/SHRINK BLK UL	B			13666			7947
	046	02	24534710	9		060	FT	SLVG, 3/8 HT/SHRINK BLK UL	B		13666			7947	
	048	01	51805700	5	2		PC	BUMPER SELF STICKING	P						
	049	01	71492970	0	4		PC	BUMPER,TOUCH PANEL	P						
	050	01	00817600	0		050	OZ	ADH, RUB BASED (3M EC-1099)	B			13666			7947
	050	02	94850711	6		050	OZ	SEAL, EASTMAN CLR (910)	B		13666			7947	
	051	01	51589600	9	2		PC	BUSHING INSU	P						
	052	01	71492925	4	1		PC	MASK KYBD IST 2	P						
	053	01	61391116	3	1		PC	GND WIRE ASSY (5.5IN 16AWG)	A						
	054	01	91975617	1	1		PC	WASHER METRIC FLAT SCR SZ 5	B						
								0056 TOTAL LINES							

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
/	Comp 42	RELEASED CLASS B	--	1/4/77		
01	30869	P/N 13 WAS 45554301	WJG	3-30-77		
02	50606	CHG CABLE LENGTHS	WJG	4-4-77		
03	50623	[illegible]	WJG	4-21-77		
04	50660	P/N 4 WAS 51695900	WJG	6-16-77		
05	50687	PL DWG CHGS ADD WIRE 3	WJG	6-14-77		
06	50722	ADD PIN 1	WJG	7-27-79		
A	11345-52	RELEASED CLASS A		9-7-79		



SECTION A-A





GND STUD DETAIL

NOTES:

1. MARK "ASSY 61408031" IN AREA SHOWN PER CDC SPEC 1012150B.
2. REFERANCE ONLY AND MAY NOT APPEAR ON PART.
3. KEEP WIRES AS SHORT & STRAIGHT AS POSSIBLE.

APL 61408031

DO NOT SCALE DRAWING

FC 816A

A C ENTRY ASSY

15920 D 61408031

SCALE NHA 15631280

BUILD ARC 230

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
08-09-79	1	11563-32

DIV	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	SRC	STATUS	STATUS DATE	ENG. RESP	FILE DATE
0860	61408031	5	A	D	PANEL ASSY (AC ENTRY)	A	REL	08-09-79	FC816A	08-09-79

T	FIND NO	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	SRC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	001	01	44671665	6	1		PC	POWER LINE FILTER	P						
	002	01	71492604	5	1		PC	PANEL, AC ENTRY	P						
	003	01	36158909	6	1		PC	BSHG, STRAIN-REL .630/.125 IN	B						
	004	01	51918296	8	1		PC	CORD, 8FT 3-CNDCT IEC 125V 1	P						
	005	01	51906200	4	2		PC	CONT, SKT 20-14GA .130IT STR	P						
	006	01	15003304	1	3		FT	WIR 18GA STRD YEL 300V UL PVC	W						
	007	01	51906001	6	1		PC	CONN, 3 SKT PLUG FIG 1 NYLON	P						
	008	01	95643231	4	2		PC	LUG, Q-CONN 22-18AWG FIG 5	P						
	009	01	91975724	5	1		PC	NUT HEXAGON SZ 5MM	B						
	010	01	91975671	8	2		PC	WASHER EX TOOTH SZ 5	B						
	011	01	15164911	8	2		PC	MSCR HEX-LK PLN M4X8MM STL ZP	B						
	012	01	51797236	0	1		PC	LUG, NO.10 CRMP-R 16-14AWG	B						
	013	01	24534709	1		333	FT	SLVG, 1/4 HT/SHRINK BLK UL	B						
								0013 TOTAL LINES							

7-22

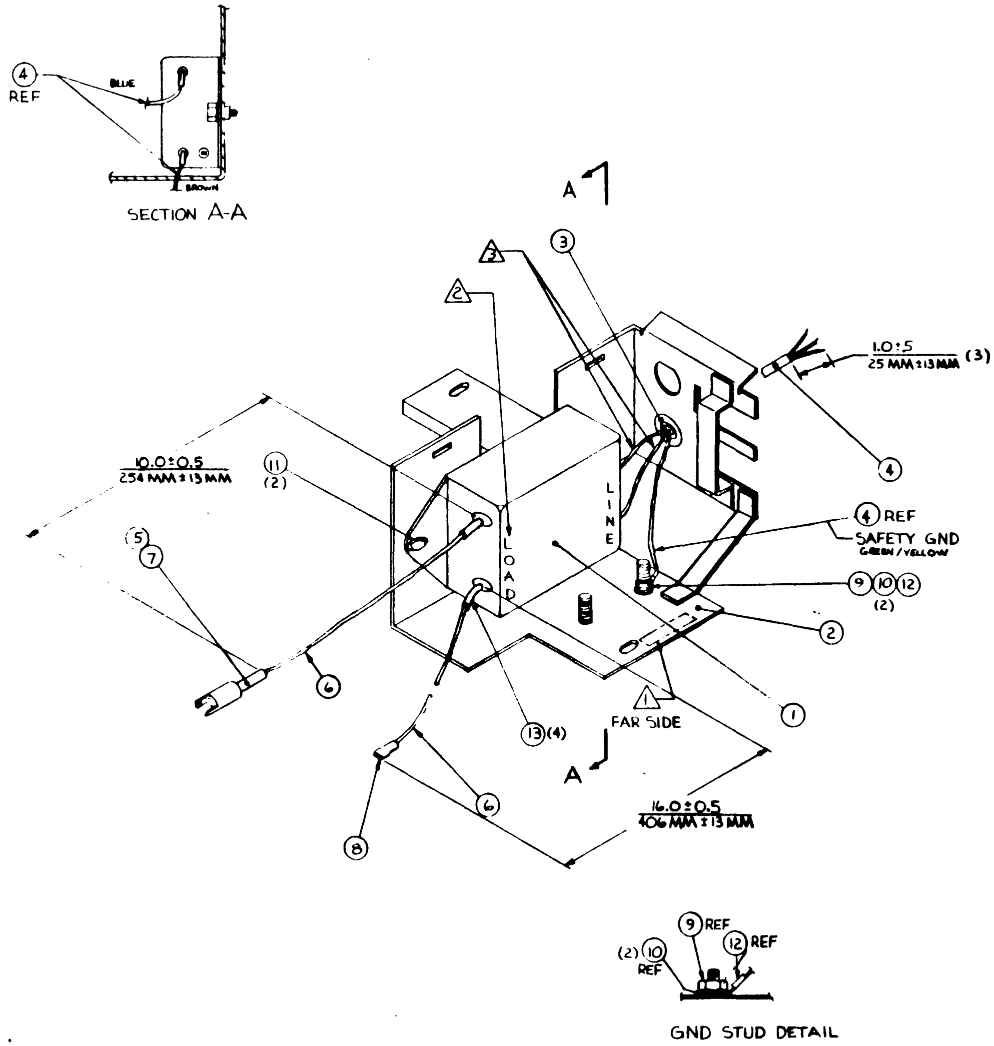
82100083

61408032

SHEET REVISION STATUS								

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
-	Same 59	RELEASED CLASS B		1/9/79	-	[illegible]
01	50569	F/N 13 WAS [illegible], F/N 4 WAS [illegible]	WJG	3-20-79	[illegible]	[illegible]
02	50606	CHG CABLE LENGTHS	WJG	4-4-79	[illegible]	[illegible]
03	50612	ADD WIRE COLOR	WJG	4-10-79	[illegible]	[illegible]
04	50687	PL [illegible] DWG CHGS, ADD NOTE 3	WJG	[illegible] 79	WJG	[illegible]
05	50722	ADD F/N 1	WJG	7 [illegible] 79	WJG	[illegible]
A	15565-52	RELEASED CLASS X		[illegible] 79		[illegible]



NOTES:

1. MARK "ASSY 61408032" IN AREA SHOWN PER CDC SPEC 10121508.
2. REFERANCE ONLY AND MAY NOT APPEAR ON PART.
3. KEEP WIRES AS SHORT & STRAIGHT AS POSSIBLE.

APL 61408032	DETACHED LISTS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: 2 PLACE ± / 3 PLACE ± / ANGLES ± /	CONTROL DATA
			FIRST USED ON: FC 816B
		DO NOT SCALE DRAWING	DRAWN BY: WJG [illegible] 1-12-79
		MATERIAL	CHECKED BY: [illegible] 1-12-79
			ENGINEER: [illegible]
		FINISH	MFG: [illegible]
			APPROVED: [illegible]

TITLE: A C ENTRY ASSY
50 HZ 220V

CODE IDENT	SIZE	DRAWING NO
15920	D	61408032

SCALE | NNA 15632065 | SHEET 1 OF 1

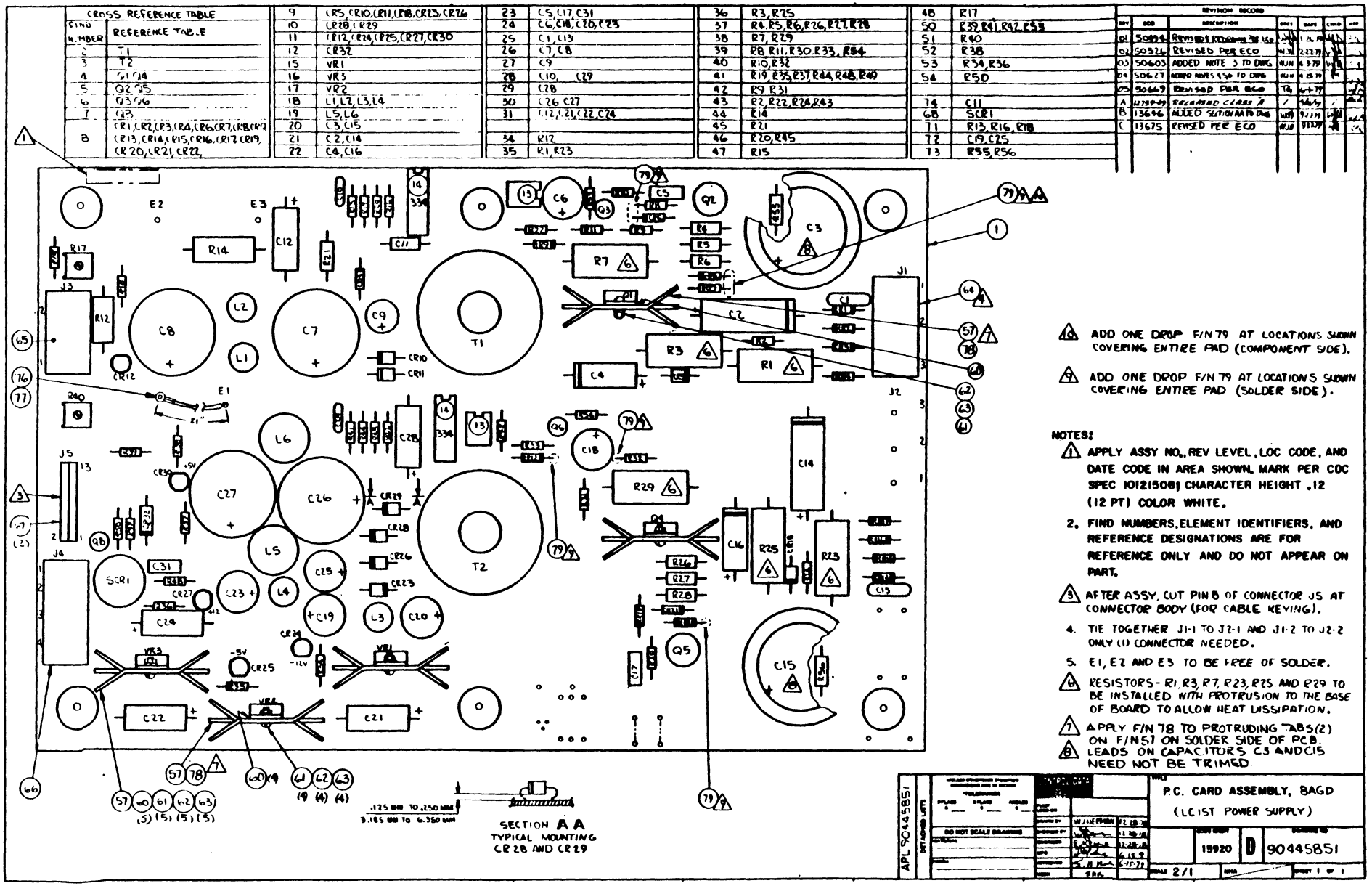
BUILD ARC 230

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO.
10-04-79	1	115532

DIV	ASSEMBLY NUMBER	CO	REV	MODEL	DESCRIPTION	EC	STATUS	STATUS DATE	MODEL GROUP	FILE DATE
8868	A1A8A832 3		A	D	AC ENTRY ASSY (50HZ 220V)	A	REL	AE-08-79	FC8168	AE-08-79

ITEM NO.	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	EC	VLD	ECO NO. IN	ECO NO. OUT	S/N	USE IN	USE OUT
001	01	44671665	6	1		PC	POWER LINE FILTER	P						
002	01	71498604	5	1		PC	PANEL, AC ENTRY	P						
003	01	36150909	6	1		PC	BSHG, STRAIN-REL .630/.125 IN	B						
004	01	51918298	4	9		FT	CORDAGE, RAW 3-CNDCT IEC 250V	W						
005	01	42821406	4	1		PC	CONT, PIN 10-14AWG B/TIN S	P						
006	01	15863304	1	2	500	FT	WIR 18GA STRD YEL 300V UL PVC	W						
007	01	93948089	1	1		PC	CONNECTOR 1 PIN HOUSING	P						
008	01	95443231	4	1		PC	LUG, 8-CONN 22-18AWG FIB S	P						
009	01	91975724	5	1		PC	NUT HEXAGON SZ 5MM	B						
010	01	91975671	8	2		PC	WASHER EX TOOTH SZ 5	B						
011	01	15164911	8	2		PC	MSCR HEX-LK PLN M4X8MM STL ZP	B						
012	01	51797219	4	1		PC	LUG, NO.18 CRMP-R 22-18AWG	B						
013	01	24534709	1		333	FT	SLVG, 1/4 HT/SHRINK BLK UL	B						
							0013 TOTAL LINES							



CROSS REFERENCE TABLE

FIND NUMBER	REFERENCE TABLE
1	T1
3	T2
4	Q1,Q4
5	Q2,Q5
6	Q3,Q6
7	Q3
8	CR1,CR2,CR3,CR4,CR6,CR7,CR8,CR9, CR13,CR14,CR15,CR16,CR17,CR19, CR20,CR21,CR22,
9	CR5,CR10,CR11,CR18,CR23,CR26
10	CR28,CR29
11	CR12,CR24,CR25,CR27,CR30
12	CR32
15	VR1
16	VR3
17	VR2
18	L1,L2,L3,L4
19	L5,L6
20	C3,C15
21	C2,C14
22	C4,C16
23	C5,C17,C31
24	C6,C18,C20,C23
25	C1,C13
26	C7,C8
27	C9
28	C10, C29
29	C28
30	C26 C27
31	C12,C21,C22,C24
34	R17
35	R1,R23
36	R3,R25
37	R4,R5,R6,R26,R27,R28
38	R7,R29
39	R8,R11,R30,R33, R34
40	R10,R32
41	R19,R35,R37,R44,R48,R49
42	R9,R31
43	R2,R22,R24,R43
44	R14
45	R21
46	R20,R45
47	R15
48	R17
50	R39,R41,R42,R53
51	R40
52	R38
53	R34,R36
54	R50
74	C11
68	SCR1
71	R13,R16,R18
72	C19,C25
73	R55,R56

REVISION RECORD

REV	ECO	DESCRIPTION	BY	DATE	CHKD	APP
01	50494	REVISED PER ECO	[illegible]	[illegible]	[illegible]	[illegible]
02	50526	REVISED PER ECO	WJH	2-27-73	[illegible]	[illegible]
03	50603	ADDED NOTE 3 TO DWG.	WJH	3-7-73	[illegible]	[illegible]
04	50627	ADDED NOTES 4 & 5 TO DWG	WJH	3-15-73	RH	[illegible]
05	50669	REVISED PER ECO	TH	4-4-73	[illegible]	[illegible]
A	12799-99	RELEASED CLASS A	/	5-16-74	/	[illegible]
B	13696	ADDED SECTION AA TO DWG	WJH	9-11-74	[illegible]	[illegible]
C	13675	REVISED PER ECO	WJH	9-11-74	[illegible]	[illegible]

⚠6 ADD ONE DROP F/N 79 AT LOCATIONS SHOWN COVERING ENTIRE PAD (COMPONENT SIDE).

⚠9 ADD ONE DROP F/N 79 AT LOCATIONS SHOWN COVERING ENTIRE PAD (SOLDER SIDE).

NOTES:

⚠1 APPLY ASSY NO., REV LEVEL, LOC CODE, AND DATE CODE IN AREA SHOWN, MARK PER CDC SPEC 10121508; CHARACTER HEIGHT .12 (12 PT) COLOR WHITE.

2. FIND NUMBERS, ELEMENT IDENTIFIERS, AND REFERENCE DESIGNATIONS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON PART.

⚠3 AFTER ASSY, CUT PIN 8 OF CONNECTOR J5 AT CONNECTOR BODY (FOR CABLE KEYING).

4. TIE TOGETHER J1-1 TO J2-1 AND J1-2 TO J2-2 ONLY (1) CONNECTOR NEEDED.

5. E1, E2 AND E3 TO BE FREE OF SOLDER.

⚠6 RESISTORS - R1, R3, R7, R23, R25, AND R29 TO BE INSTALLED WITH PROTRUSION TO THE BASE OF BOARD TO ALLOW HEAT DISSIPATION.

⚠7 APPLY F/N 78 TO PROTRUDING TABS(2) ON F/N 57 ON SOLDER SIDE OF PCB.

⚠8 LEADS ON CAPACITORS C5 AND C15 NEED NOT BE TRIMED.

.125 MM TO .250 MM
3.185 MM TO 6.350 MM

SECTION AA
TYPICAL MOUNTING
CR28 AND CR29

APL 90445851

P.C. CARD ASSEMBLY, BAGD
(LCIST POWER SUPPLY)

CODE IDENT	SIZE	DRAWING NO.
19920	D	90445851

SCALE 2/1

BUILD ARC 210

ASSEMBLY PARTS LIST

PRINT DATE 09-10-79 | PAGE 1 | FILE CHANGE NO 00013675

DIV	ASSEMBLY NUMBER	CD	REV	DWG	DESCRIPTION	SEC	STATUS	STATUS DATE	DWG GRP	FILE DATE
0860	90445851		C	D	PWR SUPPLY BASD	A	REL	06-18-79	FC816A	09-10-79

TYP	FIND NO	LI	PART NUMBER	CD	QUANTITY	U/M	PART DESCRIPTION	SEC	VLD	DCO IND IN	DCO IND OUT	S/N	USE IN	USE OUT
	001	01	90445850	2	1	PC	PW BD BASD PWR SUPPLY	P						
	002	01	51917860	2	1	PC	XFMR FLYBACK MULTI O/P	P						
	003	01	51917859	4	1	PC	XFMR FLYBACK MULTI O/P	P						
	004	01	51918111	9	2	PC	XSTR NPN 400V 8A TO 220	P						
	005	01	51681100	7	2	PC	XSTR 2N5189 NPN SIL	P						
	006	01	51003092	7	2	PC	XSTR 2N2222 HI SPEED NPN SIL	P						
	007	01	51714000	0	1	PC	XSTR 2N2907 PNP SIL	P						
	008	01	95637304	7	17	PC	DIO IN4004 400PIV SIL 1.1V/1A	P						
	009	01	95691500	3	6	PC	RECT, 1N5615 F=R SIL 1 AMP	P						
	010	01	95691506	0	2	PC	RECT, 1N5416 F=R SIL 3 AMP	P						
	011	01	51903800	4	5	PC	LED, S=S GAP RED 1.0MCD 100MW	P						
	012	01	15101109	5	1	PC	DIO 1N752A 400MW ZEN VR 5.6V	P						
	013	01	95791300	7	2	PC	IC 4N26 OPT COUPLED ISOLATOR	P						
	014	01	51718400	8	2	PC	IC 723C 33A VOLTAGE REGULATOR	P						
	015	01	15151402	3	1	PC	IC UA7900-12 350C NEG V REGLTR	P						
	016	01	15151503	8	1	PC	IC UA7800-12 357C POS V REGLTR	P						
	017	01	15151400	7	1	PC	IC UA7900-5 356A NEG V REGLTR	P						
	018	01	51918616	7	4	PC	INDUCTOR	P						
	019	01	51918617	5	2	PC	INDUCTOR	P						
	020	01	51918627	4	2	PC	CAP ALUM ELECT 300UF 250V 15P	P						
	021	01	24506816	8	2	PC	CAP FXD MYL .33UF 10P 100VDC=	P						

BUILD ARC 210

ASSEMBLY PARTS LIST

PRINT DATE 09-10-79 | PAGE 2 | FILE CHANGE NO 00013675

DIV	ASSEMBLY NUMBER	CD	REV	DWG	DESCRIPTION	SEC	STATUS	STATUS DATE	DWG GRP	FILE DATE
0860	90445851		C	D	PWR SUPPLY BASD	A	REL	06-18-79	FC816A	09-10-79

TYP	FIND NO	LI	PART NUMBER	CD	QUANTITY	U/M	PART DESCRIPTION	SEC	VLD	DCO IND IN	DCO IND OUT	S/N	USE IN	USE OUT
	022	01	3618[illegible]754	8	2	PC	CAP FXD MYL 0.0022MFD 400V	P						
	023	01	51000989	7	3	PC	CAP FXD CER .1UF 20P 25VDC=	P						
	024	01	95691133	3	4	PC	CAP ELEC 270UF -10+100P 25VDC	P						
	025	01	94842168	0	2	PC	CAP FXD CER .0033UF 6KV 1000V	P						
	026	01	94397117	6	2	PC	CAP AL ELLC 560UF 75V 1P	P						
	027	01	95691150	7	1	PC	CAP ELECT 12UF -10+100P 60VDC	P						
	028	01	51001119	0	2	PC	CAP CER F=1 .01UF +80-20P 25V	P						
	029	01	24504343	5	1	PC	CAP FXD TANT 15UF 20P 35VDC=	P						
	030	01	94397159	8	2	PC	CAP AL ELECT 5600 UF 12V	P						
	031	01	24504333	6	4	PC	CAP FXD TANT 2.2UF 20P 35VDC=	P						
	034	01	24507181	6	1	PC	RES FXD COMP 5600 OHM 5P 1=	P						
	035	01	95596501	7	2	PC	RES FXD WW 2.0 OHM 10P 5WATT	P						
	036	01	95596520	7	2	PC	RES FXD WW 600 OHM 10P 5WATT	P						
	037	01	65019518	3	6	PC	RES CARB COMP 1/2= 1.3 OHMS	P						
	038	01	95596511	6	2	PC	RES FXD WW 43 OHM 10P 5WATT	P						
	039	01	24500066	6	5	PC	RES FXD COMP 1300 OHM 5P 1/4W	P						
	040	01	24500079	9	2	PC	RES FXD COMP 4700 OHM 5P 1/4W	P						
	041	01	24500055	9	6	PC	RES FXD COMP 470 OHM 5P 1/4W	P						
	042	01	24500046	8	2	PC	RES FXD COMP 200 OHM 5P 1/4W	P						
	043	01	17705928	4	4	PC	RES FXD COMP 470K OHM 5P 1/4W	P						
	044	01	24504869	9	1	PC	RES FXD COMP 1.8K OHM 5P 2.	P						

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ASSEMBLY PARTS LIST

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DIV	ASSEMBLY NUMBER	CD	REV	SUPS	DESCRIPTION	SIC	STATUS	STATUS DATE	SUPC REP	FILE DATE
0860	9L445851		C	D	P&R SUPPLY BAGD	A	REL	06-18-79	FC816A	09-10-79

T	FIND NO	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	SIC	VLD	DCO IND IN	DCO IND OUT	S/N	WK IN	WK OUT
	045	01	24500178	0	1		PC	RES FXD COMP 2000 OHM 5P 1/2W	P						
	046	01	24500017	9	2		PC	RES FXD COMP 12 OHM 5P 1/4W	P						
	047	01	94360464	5	1		PC	RES FXD FM 46.4K OHM 1P 1/4W	P						
	048	01	51918875	9	1		PC	RES VAR CER 500 OHM 20P 1/2W	P						
	050	01	24500074	0	4		PC	RES FXD COMP 3000 OHM 5P 1/4W	P						
	051	01	51918876	7	1		PC	RES VAR CER 1K OHM 20P 1/2W	P						
	052	01	24500062	5	1		PC	RES FXD COMP 910 OHM 5P 1/4W	P						
	053	01	24500065	8	2		PC	RES FXD COMP 1200 OHM 5P 1/4W	P						
	054	01	24500023	7	1		PC	RES FXD COMP 22 OHM 5P 1/4W	P						
	057	01	51906001	3	5		PC	HT SINK, SEMI FIG 3 ALUM BLK	P						
	060	01	51903962	1		001	OZ	PASTE, HEAT XFR CMPD NON-COND	B						
	061	01	10127103	9	5		PC	MSCR PAN PHL 4-40X.312 STL ZP	B						
	062	01	10126400	6	5		PC	WSHR, NO.4 EXT/T LK STL ZP	B						
	063	01	10125103	1	5		PC	NUT, HEX 4-40 MSCR STL ZP	B						
	064	01	51906111	4	1		PC	CONN, 3 PIN PC MTD TIN FIG 1	P						
	065	01	51906100	0	1		PC	CONN, 2 PIN PC MTD TIN FIG 1	P						
	066	01	51906102	2	1		PC	CONN, 4 PIN PC MTD TIN FIG 2	P						
	067	01	51917631	9	2		PC	CONN, 7 PIN STRAIGHT PC FIG 1	P						
	068	01	51596000	3	1		PC	RECT, 2N3529 SIL CONT 600V	P						
	069	01	14006500	9	REF		PC	FABRICATION SPECIFICATION	D						
	071	01	94364346	4	3		PC	RES FXD FM 3010 OHM 1P 1/4W	P						

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ASSEMBLY PARTS LIST

PRINT DATE 09-10-79 | PAGE 4 | FILE CHANGE NO 00013675

DIV	ASSEMBLY NUMBER	CD	REV	SUPS	DESCRIPTION	SIC	STATUS	STATUS DATE	SUPC REP	FILE DATE
0860	9L445851		C	D	P&R SUPPLY BAGD	A	REL	06-18-79	FC816A	09-10-79

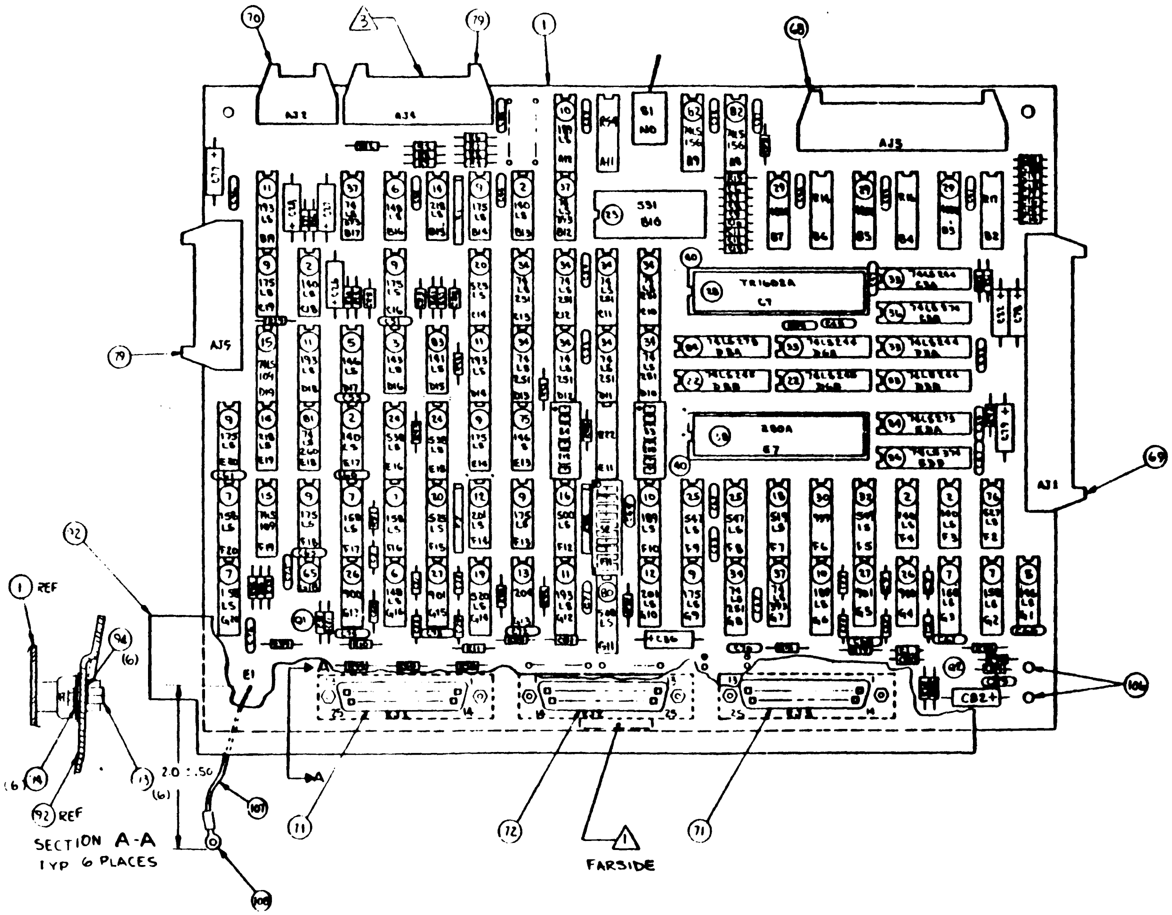
T	FIND NO	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	SIC	VLD	DCO IND IN	DCO IND OUT	S/N	WK IN	WK OUT
	072	01	95691135	8	2		PC	CAP ELEC 470UF -10+100P 25VDC	P						
	073	01	1772[illegible]519	2	2		PC	RES FXD COMP [illegible]2MEG .5% 5P	P						
	074	01	51839136	2	1		PC	CAP FXD CER .0010UF 10P 100VDC	P						
	075	01	9[illegible]445849	4	REF		PC	SCH DIA BAGD	D						
	076	01	51797230	0	1		PC	LUG, NO.10 CRMP-R 16-14AWG	B						
	077	01	52810[illegible]15	9	1	75	FT	WIR 166A STRD GRN 600V UL PVC	B						
	078	01	94857716	5		054	OZ	SEAL, 3M (4480)	B						
	079	01	51804063	7		021	OZ	ADHESIVE, SEALANT SIL RUBBER	B		13675			7935	
								0071 TOTAL LINES							

CROSS REFERENCE TABLE FIND NUMBER	REFERENCE DESIGNATION						
		51	R15, R28, R39	78	R24	103	R53
		53	R14, R17			104	R49, R52
		54	R10, R23, R25, R26, R31 [illegible]	86	R13	105	R50, R51
39	82	56	C22, C27, C28	87	R21		
42	R3	57	C6, C7, C8, C9 THRU C21, C23, C24, C25, C81				
43	R2, R12, R19, R20, R29, R32, THRU R35, R38			89	R1		
		59	[illegible]	90	R22		
44	R4, R5, R6, R7, R8, R9	60	C77, C78, C79, C82	71	S3 (WHITE DOT), S4 (RED DOT) ⚠4		
45	R37, R40	61	C1 THRU C5, C29 THRU C35, C80	96	Q2		
		62	C26, C36	97	C84		
		63	CR1, CR2, CR3	98	R55		
		66	S1	99	R56		
49	R16	73	Q1	100	R18		
50	R30	17	R11, R27, R36, R41, R44	102	R54		

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	[illegible]	DATE	CHKD	APP
-	[illegible]	RELEASED CLASS "B"	-	[illegible]	-	[illegible]
A	[illegible]	RELEASED CLASS "[illegible]"	-	[illegible]		[illegible]
B	13578	REVISED PER ECO	WJR	[illegible]		
C	13614	REVISED PER ECO	WJH	[illegible]		
D	13627	REVISED PER ECO	WJH	[illegible]		
E	13672	REVISED PER ECO	WJD	[illegible]		
F	13718	REVISED PER ECO	WJH	[illegible]		



NOTES:

1. ⚠ APPLY ASSY NO., REV LEVEL, LOC CODE, AND DATE CODE IN AREA SHOWN. MARK PER CDC SPEC 10121508; CHARACTER HEIGHT .12 (12PT) COLOR WHITE.
2. FIND NUMBERS, ELEMENT IDENTIFIERS, AND REFERENCE DESIGNATIONS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON PART.
3. ⚠ CUT PIN 1 FROM CONNECTOR AJ4 FOR KEYING PURPOSES.
4. ⚠ MARKING IS OPTIONAL WHEN SHUNT DIP IS INSTALLED BEFORE CODING.

APL 90446108

DO NOT SCALE DRAWING

FCBI6-A

P.C. CARD ASSEMBLY, 7BFD (CONTROL MODULE)

15920 | D | 90446108

SCALE NONE | SHEET 1 OF 1

BUILD ARC 214

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
10-03-79	1	00013718

DIV	ASSEMBLY NUMBER	CD	REV	DOCS	DESCRIPTION	SEC	STATUS	STATUS DATE	DOCS DISP	FILE DATE
0860	98446108	4	F	D	PC CD ASSY 7BFD	S	REL	06-07-79	FC816A	10-03-79

TYP	ASSY NO	LI	PART NUMBER	CD	SEC	QUANTITY	U/M	PART DESCRIPTION	SEC	VLD	DCO IND IN	DCO IND OUT	S/N	WS IN	WS OUT
	001	01	98446107	6		1	PC	PW BD 7BFD (CONTROL MODULE)	P						
	002	01	15144988	6		4	PC	IC 74LS00 14DLS QUAD 2-INP	P			13672			7935
	002	02	15144988	6		5	PC	IC 74LS00 14DLS QUAD 2-INP	P		13672			7935	
	003	01	15163416	9		1	PC	IC 74LS40 DUAL 4 I/P NAND BUF	P						
	005	01	15145188	2		2	PC	IC 74LS04 14DLS TTL HEX INV	P						
	006	01	15145088	4		2	PC	IC 74LS02 14DLS 02INP NOR	P						
	007	01	15146888	6		6	PC	IC 74LS161 15DLS 4BIT COUNTER	P						
	009	01	15146388	7		8	PC	IC 74LS74 17SLS F/F DUAL D	P						
	010	01	15146788	8		3	PC	IC 74LS157 18DLS TTL QD MPX	P						
	011	01	15163422	7		4	PC	IC 74LS123 DUAL MULTIVIBRATOR	P						
	012	01	15145488	6		2	PC	IC 74LS08 20ILS 02INP AND	P						
	013	01	15158388	2		1	PC	IC 7438 204 TTL QD 2IN ND BFR	P						
	014	01	15146288	9		2	PC	IC 74LS32 218LS 02INP OR	P						
	015	01	15148888	1		2	PC	I C 74LS109 TTL JKFF DUAL	P						
	016	01	15147088	2		1	PC	IC 74LS193 COUNTER TTL 4 BIT	P						
	018	01	15147588	1		1	PC	IC 74LS174 TTL 6 BIT 16 PIN	P						
	019	01	15146988	4		1	PC	IC 74LS175 S28LS LATCH 4 BIT	P						
	020	01	15163413	6		2	PC	IC 74LS155 DUAL 2 TO 4 DECODE	P						
	022	01	15163324	5		2	PC	IC 74LS245 OCTAL BUS XCEIVER	P						
	023	01	17183508	2		1	PC	IC 74150 531 TTL DATA SEL MPX	P						
	024	01	15146688	8		2	PC	IC 74LS139 538LS DECODER 10P4	P						

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ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
10-03-79	2	00013718

DIV	ASSEMBLY NUMBER	CD	REV	DOCS	DESCRIPTION	SEC	STATUS	STATUS DATE	DOCS DISP	FILE DATE
0860	98446108	4	F	D	PC CD ASSY 7BFD	S	REL	06-07-79	FC816A	10-03-79

TYP	ASSY NO	LI	PART NUMBER	CD	SEC	QUANTITY	U/M	PART DESCRIPTION	SEC	VLD	DCO IND IN	DCO IND OUT	S/N	WS IN	WS OUT
	025	01	15163415	1		2	PC	IC 74LS165 8B SHIFT REGISTER	P						
	026	01	36186488	2		2	PC	IC MC1488 900 DTL QD LN DRVR	P						
	027	01	36186588	9		2	PC	IC MC1489 901 DTL QD LN RCVR	P						
	028	01	15125788	3		1	PC	IC TR1602A 941 MOS ASYN XCVR	P						
	029	01	15136888	8		3	PC	IC 4050 CMOS HEX BFR NON-INV	P						
	030	01	15140488	1		1	PC	IC 8097 939 TTL TS HEX DRIVER	P						
	032	01	15163418	5		1	PC	IC 74LS148 ENCODER 8-3LINE PR	P						
	033	01	15163416	4		4	PC	IC 74LS244 OCTAL BFR 3-S OP	P						
	034	01	15163421	9		9	PC	IC 74LS251 DATA SELECT MPLXR	P						
	036	01	15163404	5		2	PC	IC 74LS374 OCTAL D-EDGE F-F	P						
	037	01	15163419	3		3	PC	IC 74LS393 DL 4B BIN COUNTER	P						
	038	01	15163201	5		1	PC	IC Z80A MOS 8BIT MROCESSOR	P						
	039	01	51862508	6		1	PC	SW, PC BD TGL 10 IN-LINE SPST	P						
	040	01	51848408	8		2	PC	SOCKET, IC 40 POS D-I-L TIN	P						
	042	01	94375109	9		1	PC	RES 8SIP NTWK 1000 R 3P 1.0W	P						
	043	01	24500063	3		11	PC	RES FXD COMP 1000 OHM 5P 1/4W	P			13627			7933
	043	02	24500063	3		10	PC	RES FXD COMP 1000 OHM 5P 1/4W	P		13627			7933	
	044	01	24500055	9		6	PC	RES FXD COMP 470 OHM 5P 1/4W	P						
	045	01	24500093	0		2	PC	RES FXD COMP 10K OHM 5P 1/4W	P						
	049	01	62012926	2		1	PC	RES 16PIN NTWK 100K 5P 125MW	P						
	050	01	24500089	8		1	PC	RES FXD COMP 12K OHM 5P 1/4W	P						

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ASSEMBLY PARTS LIST

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DIV	ASSEMBLY NUMBER	CD	REV	DRWG	DESCRIPTION	SEC	STATUS	STATUS DATE	DRWG RESP	FILE DATE
0860	90446108	4	F	D	PC CD ASSY 78FD	S	REL	06-07-79	FCB16A	10-03-79

TYP	FIND NO	LI	PART NUMBER	CD	SM	QUANTITY	U/M	PART DESCRIPTION	SEC	YLD	DCO IND IN	DCO IND OUT	S/N	IND IN	IND OUT
	051	01	17785912	8		2	PC	RES FXD COMP 100K OHM 5P 1/4W	P			13627			7933
	051	02	17785912	8		3	PC	RES FXD COMP 100K OHM 5P 1/4W	P		13627			7933	
	053	01	62012932	0		2	PC	RES 16PIN NTWK 10K 5P 125MW	P						
	054	01	24500087	2		7	PC	RES FXD COMP 10K OHM 5P 1/4W	P						
	056	01	51786437	7		3	PC	CAP SOLID TANT 33UF 20P 15V	P						
	057	01	51839125	5		28	PC	CAP FXD CER 1200PF 10P 100VDC	P						
	059	02	51001119	0		38	PC	CAP CER F=1 .01UF +80-20P 25V	P		13614	13718		7934	8010
	059	03	51001120	8		38	PC	CAP CER F=2 .01UF +80-20P 25V	P		13718			8010	
	060	01	24504371	6		4	PC	CAP FXD TANT 22UF 20P 15VDCW	P						
	061	01	51839120	6		13	PC	CAP FXD CER 470PF 10P 100VDC	P						
	062	01	24504329	4		2	PC	CAP FXD TANT 1.0UF 20P 35VDCW	P						
	063	01	51807385	1		3	PC	DIO IN4148 10MA MICRO SIL 30V	P						
	065	01	95791300	7		1	PC	IC 4N26 OPT COUPLED ISOLATOR	P						
	066	01	41347800	9		1	PC	SW, PC BD TGL 2POS ON-ON	P						
	068	01	51847502	5		1	PC	CONN, PCB 34POS 2RX17P FIG 1	P						
	069	01	51847504	1		1	PC	CONN, PCB 50POS 2RX25P FIG 1	P						
	070	01	51847511	6		1	PC	CONN, PCB 10POS 2RX5P FIG 3	P						
	071	01	83434804	7		2	PC	CONN 25 PIN	P						
	072	01	83434704	9		1	PC	CONN 25 PIN	P						
	073	01	51803859	6		1	PC	XSTR DD1 106 EPITAX NPN SIL	P						
	074	01	16033200	3		REF	PC	FABRICATION SPEC 70 PAK	D						
	075	01	90446106	8		REF	PC	SCH DIAG 78FD (CONTROL MOD)	D						

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ASSEMBLY PARTS LIST

PRINT DATE 10-03-79 | PAGE 4 | FILE CHANGE NO 00013718

DIV	ASSEMBLY NUMBER	CD	REV	DRWG	DESCRIPTION	SEC	STATUS	STATUS DATE	DRWG RESP	FILE DATE
0860	90446108	4	F	D	PC CD ASSY 78FD	S	REL	06-07-79	FCB16A	10-03-79

TYP	FIND NO	LI	PART NUMBER	CD	SM	QUANTITY	U/M	PART DESCRIPTION	SEC	YLD	DCO IND IN	DCO IND OUT	S/N	IND IN	IND OUT
	076	01	15163303	9		1	PC	IC 74LS164 S2TLS TTL 8B RGTR	P						
	077	01	24500081	5		5	PC	RES FXD COMP 5600 OHM 5P 1/4W	P						
	078	01	94375105	7		1	PC	RES 8SIP NTWK 10000 R 3P 1.0W	P						
	079	01	51847500	9		2	PC	CONN, PCB 20POS 2RX10P FIG 1	P						
	080	01	15148700	6		1	PC	IC 74LS153 TTL DUAL 4I/P	P						
	081	01	15148600	8		1	PC	IC 74LS260 TTL DUAL 5I/P NOR	P						
	082	01	15163440	9		2	PC	IC 74LS156	P						
	083	01	15145600	1		1	PC	IC 74LS10 14ILS TTL 3I/P NAND	P						
	084	01	15163420	1		2	PC	IC 74LS273 OCTAL D FLIP FLOP	P						
	086	01	24500075	7		1	PC	RES FXD COMP 3300 OHM 5P 1/4W	P						
	087	01	24500099	7		1	PC	RES FXD COMP 33K OHM 5P 1/4W	P						
	089	01	94375102	4		1	PC	RES 8SIP NTWK 3300 R 3P 1.0W	P						
	090	01	62012902	3		1	PC	RES MOD DUAL 10K OHMS 125MW	P						
	091	01	66308144	6		1	PC	SHUNT SET CODED	S						
	092	01	71492485	9		1	PC	PLATE MTG	P						
	093	01	94288024	6		6	PC	LKG DEVICE, CONN TYP 4 W/TYP3	P						
	094	01	19126400	8		12	PC	WSHR, NO.4 EXT/T LK STL ZP	B						
	095	01	88883700	2		1	PC	IC 74S04 14GS TTL HEX INVTR	P						
	096	01	51714000	0		1	PC	XSTR 2N2907 PNP SIL	P						
	097	01	51839106	5		1	PC	CAP FXD CER 33 PF 10P 100VDC	P						
	098	01	24500065	8		1	PC	RES FXD COMP 1200 OHM 5P 1/4W	P						

BUILD ARC 214

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
10-03-79	5	00013718

DIV	ASSEMBLY NUMBER	CD	REV	DWG	DESCRIPTION	SIC	STATUS	STATUS DATE	DWG DISP	FILE DATE
0060	90446108	4	F	D	PC CD ASSY TBFD	S	REL	06-07-79	FC010A	10-03-79

TYP	ASSY SEQ NO	LI	PART NUMBER	CD	QUANTITY	U/M	PART DESCRIPTION	SIC	VLD	ECO IND IN	ECO IND OUT	S/N	SEQ IN	SEQ OUT
	099	01	24500047	6	1	PC	RES FXD COMP 220 OHM 5P 1/4W	P						
	100	01	24500023	7	1	PC	RES FXD COMP 22 OHM 5P 1/4W	P						
	101	01	15161700	8	1	PC	IC 74LS132 TTL QUAD 2-IN NAND	P			13672			7935
	102	01	62012910	6	1	PC	RES NOD DUAL 47K OHMS 125MW	P						
	103	01	24563054	6	1	PC	RES FXD COMP 47K OHM 5P 1/8W	P						
	104	01	24500043	5	2	PC	RES FXD COMP 150 OHM 5P 1/4W	P			13578			7928
	104	02	24500045	0	2	PC	RES FXD COMP 180 OHM 5P 1/4W	P		13578			7928	
	105	01	24563074	4	2	PC	RES FXD COMP 300 OHM 5P 1/8W	P			13578			7928
	105	02	24563024	9	2	PC	RES FXD COMP 270 OHM 5P 1/8W	P		13578			7928	
	106	01	65832103	9	2	PC	SOCKET SPRING TIN	P						
	107	01	52810015	9	166	FT	WIR 16GA STRD GRN 600V UL PVC	W			13578			7928
	107	02	52810015	9	200	FT	WIR 16GA STRD GRN 600V UL PVC	W		13578	13614		7928	7934
	107	03	52810005	8	200	FT	WIR 18GA STRD GRN 600V UL PVC	W		13614			7934	
	108	01	51797236	0	1	PC	LUG, NO.10 CRMP-R 16-14AWG	B			13614			7934
	108	02	51797217	0	1	PC	LUG, NO.10 CRMP-R 22-18AWG	B		13614			7934	
							0100 TOTAL LINES							

DWN	R Trautman	4-79	CONTROL DATA	TITLE: MODULE W/FIRMWARE	PREFIX: A	DOCUMENT NO: 66308140	REV: A
CHKD	[signature]	4-30-79					
ENG	[signature]	5-31-79					
MFG	[signature]	6-7-79	CODE IDENT: 15920	FIRST USED ON: FC816A	NHA: 15631280	SHEET: 1 of 2	
APPR	[signature]	6-15-79					

SHEET REVISION STATUS

2	1
A	A

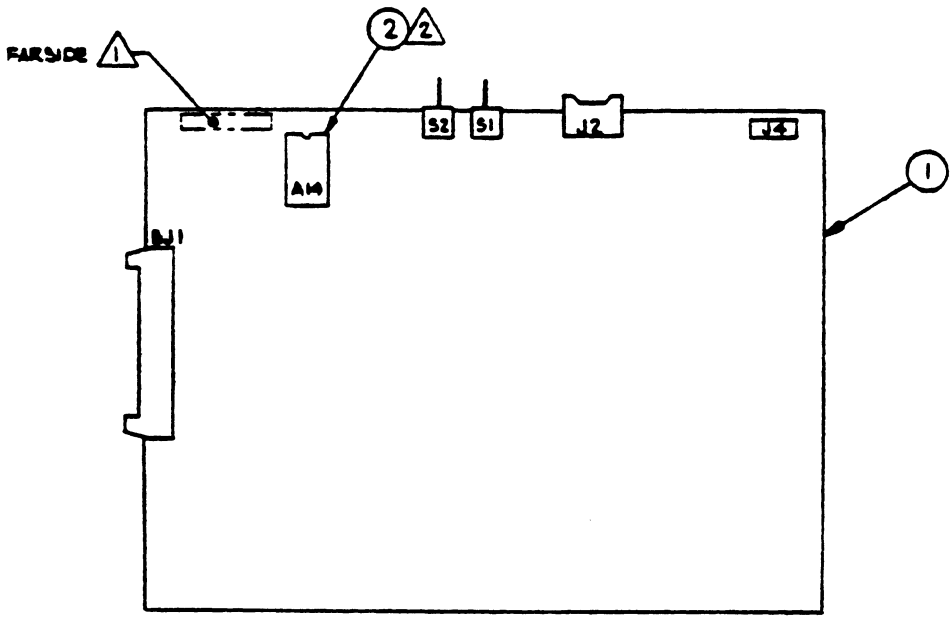
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	12259-99	Released Class "A"		6-8-79	[signature]

NOTES:
1. Mark "Assy 66308140" in area shown per CDC spec 10121508.
2. Mount find no. 2 in socket on find no. 1.

APL 66308140
DETACHED LISTS

CONTROL DATA | CODE IDENT 15920 | SHEET 2 | A | DOCUMENT NO 66308140 | REV A



BUILD ARC 440

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
06-19-79	1	12754-49

BOA	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	MC	STATUS	STATUS DATE	DWG. RESP.	FILE DATE
0860	66308141	2	A	A	IC PROGRAMMED EROM IST II	N	REL	06-18-79	FC816A	06-19-79

T	FIND NO.	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	MC	VLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	001	01	15135300	0	1		PC	IC 2716 MOS 2KX8 163848 EROM	P						
	002	01	66308142	0	REF		PC	FIRMWARE LOADER/DIAG IST II	D						
								0002 TOTAL LINES							

DWN	W GLASER	12-78	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD	R. Frantom	12-28-78		CABLE ASSY- OVER VOLTAGE	A	61408023	A
ENG	J Langdon	1/26/79					
MFG	J.D. Long	4/24/79		FIRST USED ON	NHA	SHEET	
APPR	E M Hoe	5-27-79	CODE IDENT 15920	FC816A	15631280	1 of 2	

SHEET REVISION STATUS

2	1
-	-
01	01
01	02
03	03
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
-	50002-52	Released Class B	-	1/3/79	JLH
01	50606	REVISED PER ECO	WJW	1/15/79	JLH
02	50623	F/N 2 WAS 51906201	WJG 4-21-79	4-23-79	JLH
03	50655	CABLE LENGTH WAS 16.0	WJG 5-11-79	5-11-79	JLH
A	12754-52	RELEASED CLASS A	/	6/27/79	Mech

NOTES:

1. Apply label to cable per CDC drawing 82191061, Method b. Mark as shown.

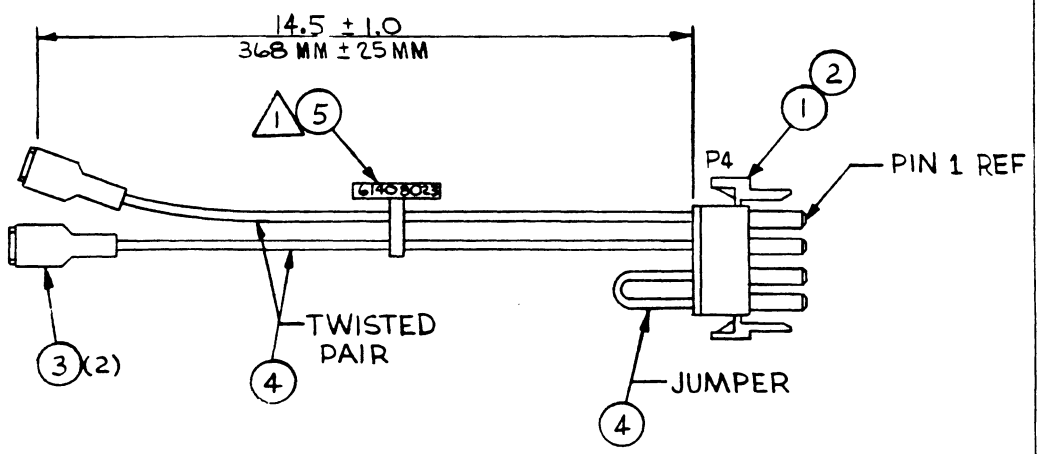
APL 61408023

DETACHED LISTS

AA3180 REV. 8/71

PRINTED IN U.S.A.

CONTROL DATA	CODE IDENT	SHEET		DOCUMENT NO.	REV
	15920	2	A	61408023	A



AA3185

PRINTED IN U.S.A.

BUILD ARC 104

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
06-28-79	1	12754-51

DIV.	ASSEMBLY NUMBER	CD	REV.	ENGR.	DESCRIPTION	SEC	STATUS	STATUS DATE	ENGR. RESP.	FILE DATE
0860	61A08023	2	A	A	CABLE ASSY OVER-VOLTAGE	A	REL	06-27-79	FC816A	06-28-79

T	FIND NO.	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	SEC	YLD	ECO. IND. IN	ECO. IND. OUT	S/N	QTY IN	QTY OUT
	001	01	51906002	4	1		PC	CONN, 4 SKT PLUG FIG 1 NYLON	P						
	002	01	51906200	4	4		PC	CONT, SKT 20-14GA .130IT STR	P						
	003	01	95643231	4	2		PC	LUG, Q-CONN 22-18AWG FIG 5	P						
	004	01	15003302	5	3		FT	WIR 18GA STRD RED 300V UL PVC	W						
	005	01	94277409	2	1		PC	STRAP, CBL TIE TYP 5 TO 5/8	B						
								0005 TOTAL LINES							

DWN	W GLASER	1-79	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV.
CHKD	W Glaser	1-79		CABLE ASSY -OVER VOLTAGE (50 HZ)	A	61408447	A
ENG	[illegible]	1-18-79					
MFG	[illegible]	1-26-79		FIRST USED ON	NHA	SHEET	
APPR	E. M. Roe	6-27-79	CODE IDENT 15920	FC816B	15632065	1 of 2	

SHEET REVISION STATUS

2	1
-	-
01	01
01	02
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
-	50002-59	Released Class B	-	4/19/79	Jeff
01	50606	CABLE LENGTH CHANGE	WJG 9-5-79	9/5/79	BEL
02	50623	F/N 2 WAS 51906200	WJG 9-21-79	9/21/79	[illegible]
A	12759-53	RELEASED CLASS A	/	6/27/79	Mch

NOTES:

1. Apply label to cable per CDC drawing 82191061, Method b. Mark as shown.

APL 61408447

DETACHED LISTS

AA3180 REV. 8 71

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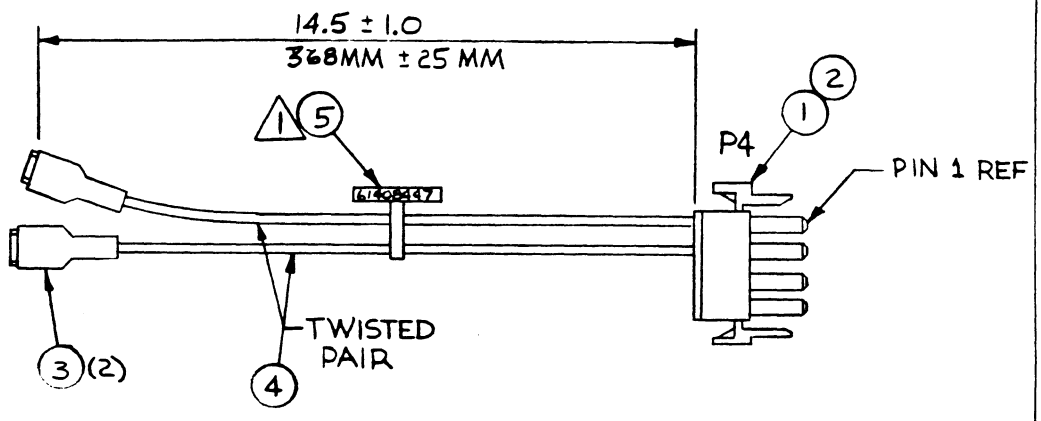
CONTROL DATA		CODE IDENT	SHEET		DOCUMENT NO.	REV.
		15920	2	A	61408447	A



AA3180

PRINTED IN U.S.A.

BUILD ARC 104

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO.
06-28-79	1	12754-51

DIV.	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	SEC	STATUS	STATUS DATE	ENG. RESP.	FILE DATE
0860	61408447	3	A	A	CABLE ASSY OVERVOLTAGE	A	REL	06-27-79	FC816B	06-28-79

T	FIND NO.	LI	PART NUMBER	CD	QUANTITY	U/M	PART DESCRIPTION	SEC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	EFF IN	EFF OUT
	001	01	51906002	4	1	PC	CONN, 4 SKT PLUG FIG 1 NYLON	P						
	002	01	51906200	4	2	PC	CONT, SKT 20-14GA .130IT STR	P						
	003	01	95643231	4	2	PC	LUG, O-CONN 22-18AWG FIG 5	P						
	004	01	15003302	5	3	FT	WIR 18GA STRD RED 300V UL PVC	W						
	005	01	94277409	2	1	PC	STRAP, CBL TIE TYP 5 TO 5/8	B						
							0005 TOTAL LINES							

DWN	W GLASER	12-7	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD		12-8-78		CABLE, DISPLAY LOGIC	A	61408033	A
ENG		6/6/78					
MFG		6-26-79		FIRST USED ON	NHA	SHEET	
APPR		6-27-79	CODE IDENT 15920	FC816A	15631280	1 of 3	

SHEET REVISION STATUS

3	2	1
-	-	-
-	01	01
02	02	02
02	03	03
A	A	A

REVISION RECORD

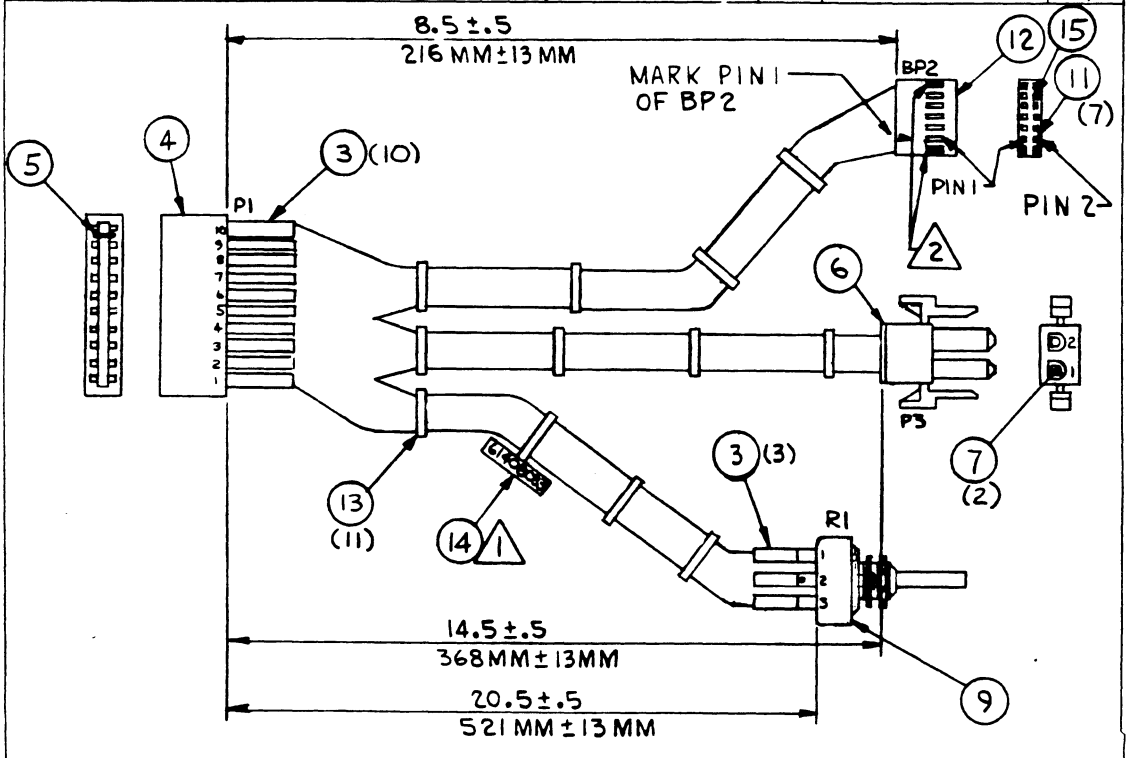
REV	ECO	DESCRIPTION	DRFT	DATE	APP
-	S0002-52	Released Class B	-	1/3/79	JBS
01	50486	P.L. CHG	WJG 1-19-79	1-19-79	gcd
02	50606	REVISED PER ECO	WJH	4-5-79	gcd
03	50655	ADD F/N 15	WJG 5-11-79	5-11-79	gcd
A	12754-52	RELEASED CLASS A	/	6/27/79	mch

NOTES:
1. Apply label to cable per CDC drawing 82191061, Method b. Mark as shown.
2. Two cavities at each end are not counted or used. For mating only.

APL 61408033
DETACHED LISTS

AA3180 REV. 8/71 PRINTED IN U.S.A.

CONTROL DATA | CODE IDENT 15920 | SHEET 2 | A | DOCUMENT NO. 61408033 | REV A



AA3180 PRINTED IN U.S.A.

CONTROL DATA

CODE IDENT	SHEET	WL	DOCUMENT NO	REV
15920	3		61408033	02

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	10	18	2	16	P1	7		P3	1	7	+55V
2	10	18	2	16	P1	1		P3	2	7	GROUND
3	1	24	0	10	P1	1		BP2	3	11	GROUND (TWP)
4	2	24	2	10	P1	6		BP2	4	11	LINE SYNC (TWP)
5	2	24	2	22	P1	2		R1	3		HIGH SIDE BRIGHTNESS
6	2	24	2	22	P1	3		R1	1		LOW SIDE BRIGHTNESS
7	1	24	0	22	P1	4		R1	2		WIPER BRIGHTNESS
8	2	24	2	10	P1	5		BP2	8	11	+5V
9	2	24	2	10	P1	8		BP2	2	11	VIDEO (TWP)
10	1	24	0	10	P1	10		BP2	1	11	GROUND (TWP)
11	1	24	0	10	P1	10		BP2	5	11	GROUND (TWP)
12	2	24	2	10	P1	9		BP2	6	11	FIELD SYNC (TWP)

AA3183 REV. 8/71 PRINTED IN U.S.A.

ASSEMBLY PARTS LIST

BUILD ARC 104

PRINT DATE	PAGE	FILE CHANGE NO.
06-28-79	1	12754-51

DIV.	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	MC	STATUS	STATUS DATE	DWG. RESP.	FILE DATE
0860	61408033	1	A	A	CABLE ASSY, DISPLAY LOGIC	A	REL	06-27-79	FC816A	06-28-79

T	FIND NO	LI	PART NUMBER	CD	QUANTITY	U/M	PART DESCRIPTION	MC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	001	01	24548301	1	4 300	FT	WIR 24GA STRD BLK 300V UL PVC	W						
	002	01	24548303	7	7	FT	WIR 24GA STRD RED 300V UL PVC	W						
	003	01	24552336	0	13	PC	SLEEVE, 5/8LG INS CLR 10GA UL	B						
	004	01	38905301	8	1	PC	CONN, 10 PIN PWB MTG GOLD	P						
	005	01	51832900	8	1	PC	KEY POARIZING	P						
	006	01	51906000	8	1	PC	CONN, 2 SKT PLUG FIG 1 NYLON	P						
	007	01	51906201	2	2	PC	CONT, SKT 20-14GA .2001 T STR	P						
	009	01	51911801	2	1	PC	RES VAR COMP 100K W/O SWITCH	P						
	010	01	15003302	5	2 700	FT	WIR 18GA STRD RED 300V UL PVC	W						
	011	01	94245602	1	7	PC	CONT, SKT 22-26GA 7 W/F STRIP	P						
	012	01	94361107	9	1	PC	CONN HSG, 14 CAV 2RX7SKT BLK	P						
	013	01	94277400	1	11	PC	STRAP, CBL TIE TYP 1 TO 5/8	B						
	014	01	94277409	2	1	PC	STRAP, CBL TIE TYP 5 TO 5/8	B						
	015	01	51870337	6	1	PC	PLUG, PLZG NYLON 10/STRIP	P						
							0014 TOTAL LINES							

DWN	W GLASER	12-7	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO	REV
CHKD				CABLE ASSY- LOGIC SIGNALS	A	61408025	A
ENG				FIRST USED ON	NHA	SHEET	
MFG				FC816A	15631280	1 of 2	
APPR		6-27-79	CODE IDENT 15920				

SHEET REVISION STATUS

2	1
-	-
01	01
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
-	50002-52	Released Class 8	-	1/3/79	
01	50606	REVISED PER ECO	WJH	1/15/79	
A	12754-52	RELEASED CLASS "A"	/	4/27/79	

NOTES:

1. Mark with CDC part number per CDC Spec 10121508.

APL 61408025
DETACHED LISTS

AA318 REV. 8/71

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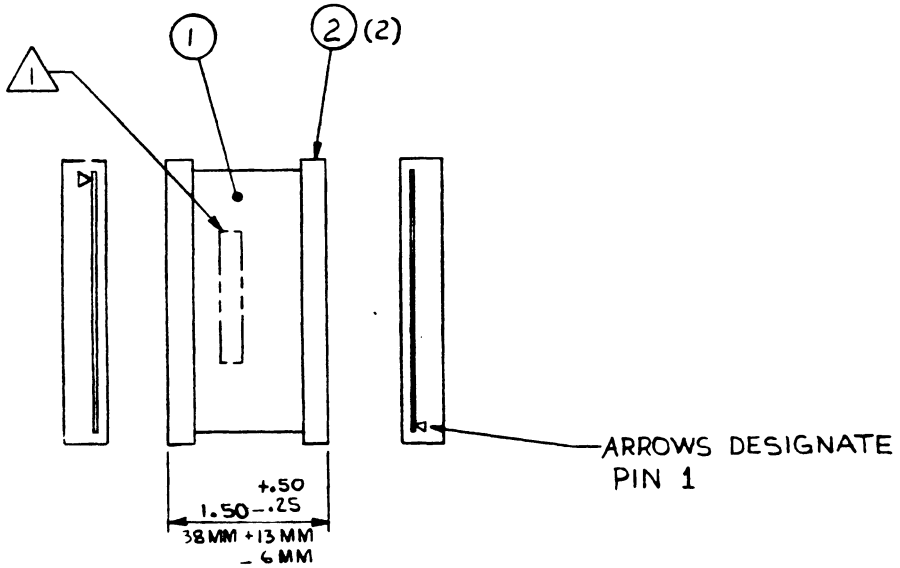
CONTROL DATA	CODE IDENT	SHEET		DOCUMENT NO.	REV
	15920	2	A	61408025	A



AA3185

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BUILD ARC 104

ASSEMBLY PARTS LIST

PRINT DATE 09-26-79 | PAGE 1 | FILE CHANGES NO 00013700

DIV	ASSEMBLY NUMBER	CD	REV	DRWG	DESCRIPTION	SEC	STATUS	STATUS DATE	DRWG GROUP	FILE DATE
0060	61400624	0	B	A	CABLE ASSY, LOGIC DC	A	REL	06-27-79	FC016A	09-26-79

T	FIND NO	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	SEC	TAG	DCO IMP IN	DCO IMP OUT	S/N	USE IN	USE OUT
	001	01	SI870337	6	2		PC	PLUG, PLZ8 NYLON 10/STRIP	P						
	002	01	15003302	5	16	500	FT	WIR 18GA STRD RED 300V UL PVC	W			13700			7940
	002	02	15003402	3	16	500	FT	WIR 20GA STRD RED 300V UL PVC	W		13700			7940	
	003	01	94245607	6	26		PC	CONT, SKT 18-20GA 2 W/F STRIP	P						
	004	01	SI020465	5	4		PC	CONNECTOR HOUSING	P			13700			7940
	004	02	94261806	7	2		PC	CONN HSG, 14 SKT 2MXTSKT BLK	P		13700			7940	
	005	01	94277409	2	1		PC	STRAP, CBL TIE TYP 5 TO 5/8	B						
	006	01	94277401	9	2		PC	STRAP, CBL TIE TYP 1 TO 1-3/4	B						
								0008 TOTAL LINES							

DWN	W GLASER	12-7-78	CONTRACT NO.	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD		12-8-78		CABLE ASSY- D C POWER	A	61408024	B
ENG		12-8-78					
MFG		6-8-79		FIRST USED ON	NHA	SHEET	
APPR	E M	6-27-79	CODE IDENT 15920	FC816A	15631280	1 of 2	

SHEET REVISION STATUS

2	1
-	-
01	01
02	02
02	03
A	A
B	B

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
-	50002-52	Released Class B	-	4/4/79	JEL
01	50592	ADD NOTE 2 & F/N 6	WJG 3-28-79	3/30/79	JEL
02	50672	ADD NOTE 3 & PL CHG'S	WJG 5-23-79	5-23-79	GWL
03	50701	ADD F/N 7	WJG 6-19-79		GLB
A	12758-52	RELEASED CLASS 'A'	/	6/27/79	MAL
B	13700	DELETED NOTES & REVISED D/L PER ECO	WJG 10-2-79	10-2-79	GWL

NOTES:

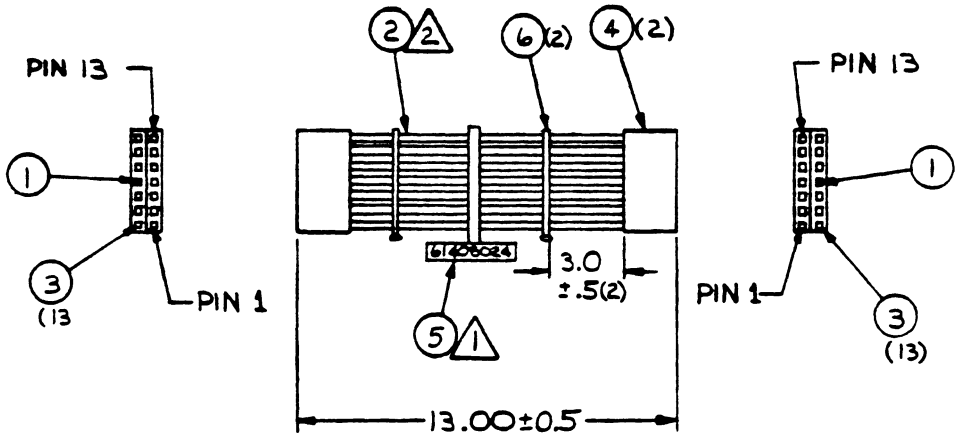
2 Apply label to cable per CDC drawing 82191061, Method b. Mark as shown.

3 Wiring to be point to point.

[illegible] Connector's) with [illegible] Adhesive [illegible]

APL 61408024
DETACHED LISTS

	CODE IDENT	SHEET		DOCUMENT NO	REV
[illegible]	15920	2	A	61408024	B



BUILD ARC 104

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO
06-28-79	1	12754-51

DIV.	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	SIC	STATUS	STATUS DATE	ENGR. RESP.	FILE DATE
0860	61A0802A	0	A	A	CABLE ASSY, LOGIC DC	A	REL	06-27-79	FCB16A	06-28-79

TYPE	FIND NO.	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	SIC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	001	01	51870337	6	2		PC	PLUG, PLZG NYLON 10/STRIP	P						
	002	01	15003302	5	16	500	FT	WIR 18GA STRD RED 300V UL PVC	W						
	003	01	94245607	0	26		PC	CONT, SKT 18-20GA 2 W/F STRIP	P						
	004	01	51920465	5	4		PC	CONNECTOR HOUSING	P						
	005	01	94277409	2	1		PC	STRAP, CBL TIE TYP 5 TO 5/8	B						
	006	01	94277401	9	2		PC	STRAP, CBL TIE TYP 1 TO 1-3/4	B						
	007	01	94850711	6		001	OZ	SEAL, EASTMAN CLR (910)	B						
								0007 TOTAL LINES							

DWN		12-78	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHK		12-8-78		CABLE ASSY-VIDEO OUTPUT	A	61408444	A
ENG		06 DEC 78					
MFG		6-14-79	CODE IDENT 15920	FIRST USED ON FC816A	NHA 15631280	SHEET 1 of 2	
APPR		6-27-79					

SHEET REVISION STATUS

2	1
-	-
01	01
02	02
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
-	50002-52	Released Class B	-	4/3/79	
01	50486	PL CHG	WJG 1-19-79	1-19-79	
02	50606	REVISED PER ECO	WJH	4-5-79	
A	12754-52	RELEASED CLASS "A"	1	6/27/79	

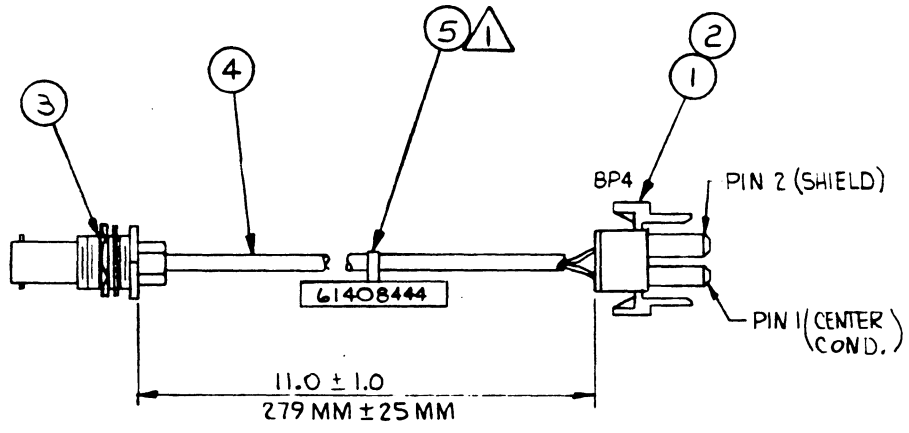
NOTES:

1. Apply label to cable per CDC drawing 82191061, Method 6. Mark as shown.

APL 61408444
DETACHED LISTS

AA1 40 REV. 8 71 PRINTED IN U.S.A.

CONTROL DATA	CODE IDENT	SHEET		DOCUMENT NO.	REV
	15920	2	A	61408444	A



AA3 85 PRINTED IN U.S.A.

BUILD ARC 104

ASSEMBLY PARTS LIST

PRINT DATE	PAGE	FILE CHANGE NO.
06-28-79	1	12754-51

DIV.	ASSEMBLY NUMBER	CD	REV.	DWG.	DESCRIPTION	ASC	STATUS	STATUS DATE	DWG. RESP.	FILE DATE
0860	6140844A	J	A	A	CABLE ASSY-VIDEO OUTPUT	A	RFL	06-27-79	FC816A	06-28-79

T	FIND NO.	LI	PART NUMBER	CD	QUANTITY		U/M	PART DESCRIPTION	ASC	YLD	ECO. NO. IN	ECO. NO. OUT	S/N	WK IN	WK OUT
	001	01	51906207	9	2		PC	CONT, SKT 24-18GA .100I T STR	P						
	002	01	51906000	8	1		PC	CONN, 2 SKT PLUG FIG 1 NYLON	P						
	003	01	51589702	3	1		PC	CONN RECPT COAX 1 PIN	P						
	004	01	17649400	3	1	100	FT	CABLE R.F. 1 COND COAX STRD	W						
	005	01	94277409	2	1		PC	STRAP, CBL TIE TYP 5 TO 5/8	B						
								0005 TOTAL LINES							

This section title page is included to maintain format compatibility with other existing manuals.

CAUTION

Important Instructions

The Information Systems Terminal II (IST-II) has been approved by the Federal Communications Commission (FCC) as not being harmful to the telephone network when connected directly to the telephone lines. In order to fully comply with Part 68, FCC Docket 19528, the following should be read carefully and followed completely where applicable:

- The FCC rules require that all direct connection to the telephone lines must be made through standard plugs and jacks as supplied with IST-II terminals equipped with internal modems. No connection can be made to party lines or coin lines. Prior to connecting the device to the lines, you must inform the local telephone company of the installation required. You must also:

  - Call the local telephone company and inform them that you have an FCC registered device which you wish to connect to their lines. Give them the 14-digit FCC Registration Number and Ringer Equivalence Number, both of which are on the label located on the back of the terminal.

  - Inform the telephone company of the jack (connector) required for the device. Recently installed telephones are provided with the required jack.

- After the telephone company has installed the required jack, connect the terminal in the manner described in this manual.

- All repairs must be accomplish as described in the IST-II Hardware Maintenance Manual.

- If it appears that the terminal is malfunctioning, it should be disconnected from the telephone line until it can be determined if the equipment or the telephone line is the source of the trouble. If the equipment needs repair, it should not be reconnected until such repairs are made.

- The terminal has been designed to prevent harm to the public network. If, in the case of malfunction, out of limit parameters are noted by your telephone company, service may be temporarily discontinued.

- The telephone company may make changes in its communication facilities, equipment, operations, or procedures, where such action is reasonably required in the operation of its business and is not inconsistent with the Rules and Regulations of the FCC. If such changes can be reasonably expected to render any customer's terminal equipment incompatible with the telephone company communications facilities, or require modification or alteration of such terminal equipment, or otherwise materially affect its use or performance, adequate notice will be given to allow you an opportunity to maintain uninterrupted service.

Service Requirements

In the event of equipment malfunction, check with your Control Data Corporation Sales Representative on the type of service warranty you have. Under FCC Rules, Part 68, users are not authorized to maintain their own terminals. Terminals must be maintained by Control Data maintenance personnel.

Faulty terminals should be reported to the nearest Control Data Service Center.

COMMENT SHEET

MANUAL TITLE: Information Systems Terminal II Hardware Maintenance Manual

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