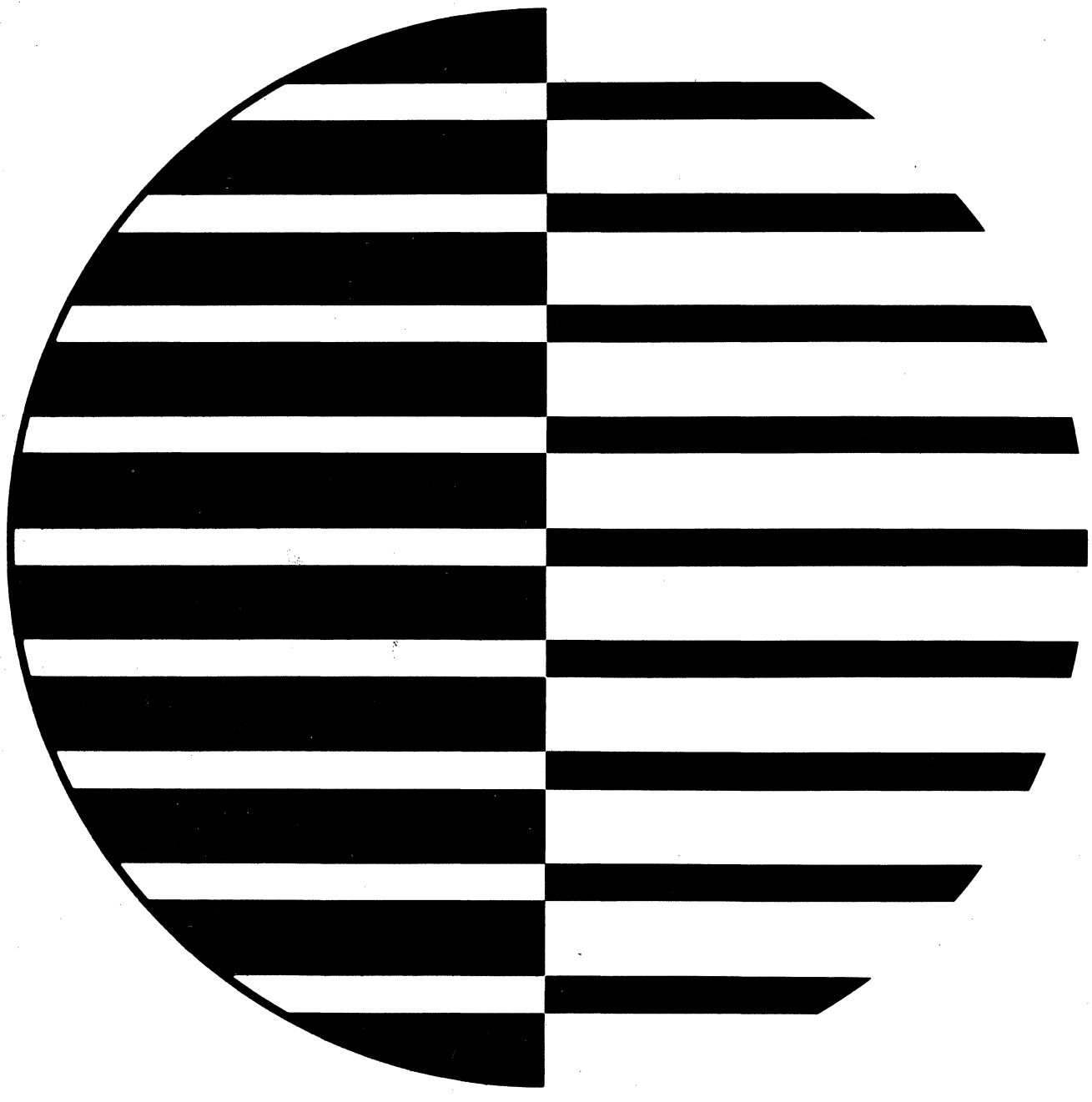
CONTROL DATA INSTITUT

CONTROL DATA



PHASE IV

LOGIC DIAGRAMS

DISPLAY

L O G I C D I A G R A M S

D I S P L A Y

Herausgeber: Control Data Institut Frankfurt/M.
Control Data GmbH Frankfurt/M. 1977

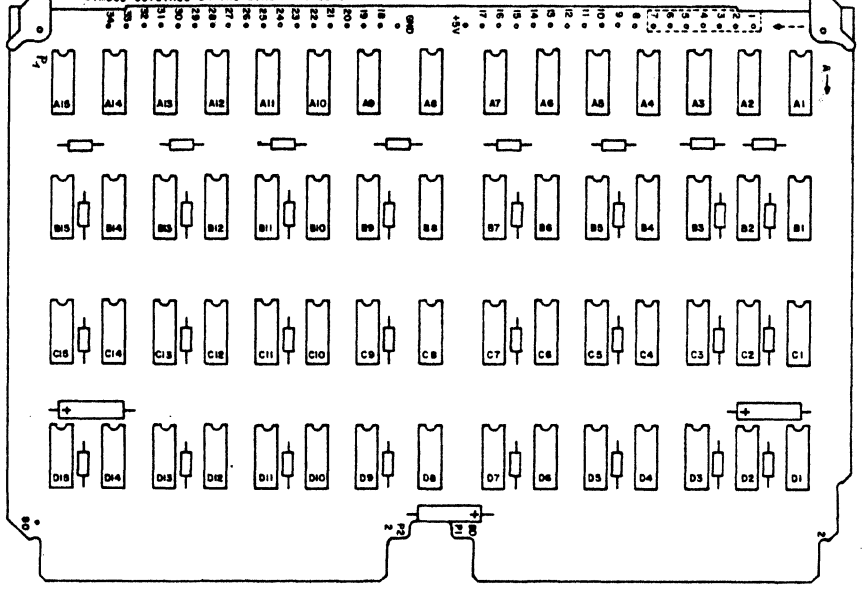
DEVELOPED & PRINTED BY CDI FRANKFURT

Printed in Germany
CDI-CT-PHIV-21-01/100

I N H A L T S V E R Z E I C H N I S

PHYSICAL LOCATION CODES

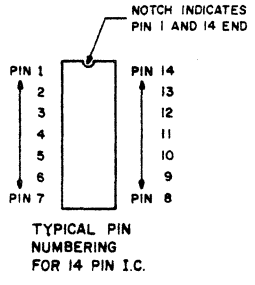
CIRCUIT MODULE LAYOUT - THE DRAWING BELOW DEPICTS A TYPICAL EXAMPLE OF THE COMPONENT SIDE ASSEMBLY OF THE 60 PAK BOARDS DIAGRAMMED IN THIS LOGIC SET. THE ALPHANUMERIC NUMBERS AT THE BOTTOM OF THE SYMBOLS ARE THE PHYSICAL LOCATION CODES. THESE NUMBERS CORRESPOND TO THOSE SHOWN INSIDE THE LOGIC SYMBOL OUTLINES ON THE DIAGRAM SHEETS.



60 PACKAGE MODULE

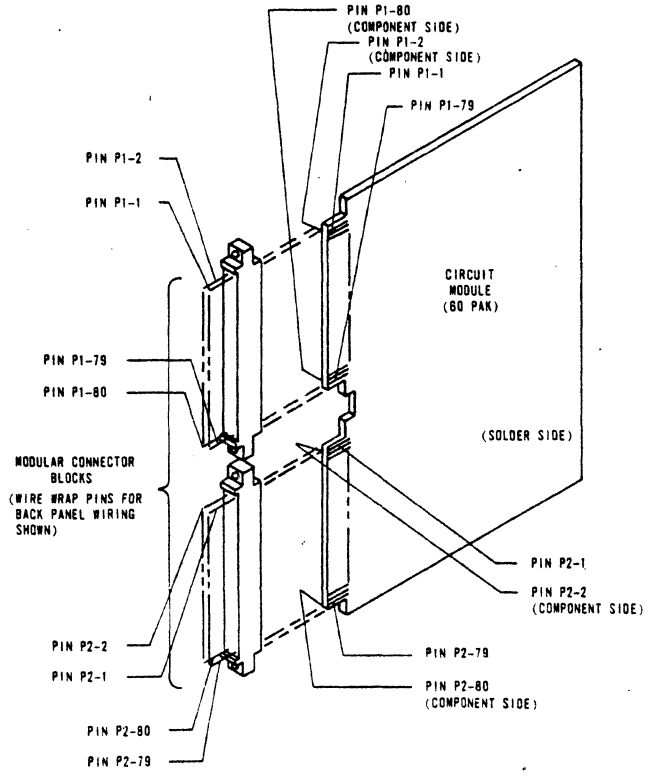
STANDARD POWER & GROUND PINS

+5V PINS P1 & P2 - 1,2,3 & 4
+18V PINS P1 & P2 - 71 & 72
-18V PINS P1 & P2 - 75 & 76
GND PINS P1 & P2 - 77,78,79 & 80



TYPICAL PIN NUMBERING FOR 14 PIN I.C.

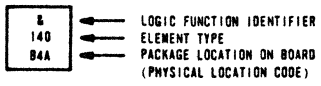
CIRCUIT MODULE & MODULAR CONNECTOR BLOCK



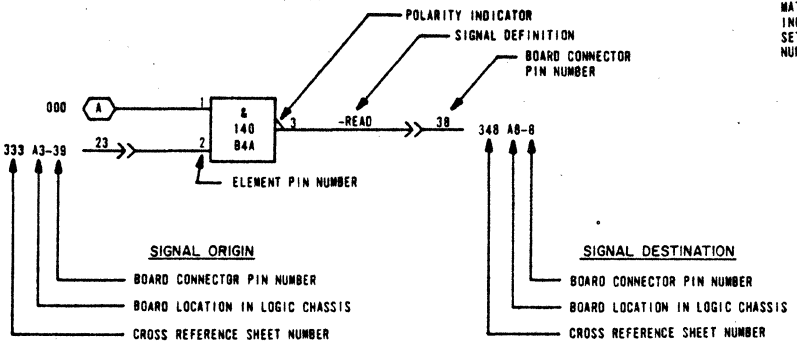
CONTROL DATA | KEY TO DIAGRAMS PHYSICAL LOCATION CODES | CODE IDENT 15920 | DWG NO 62193300 | REV A | SHEET 2 | CROSS REF NO

GENERAL LOGIC SYMBOL INFORMATION

INTEGRATED CIRCUIT LOGIC SYMBOL



TAGGING INFORMATION



GENERAL P.C. BOARD INFORMATION

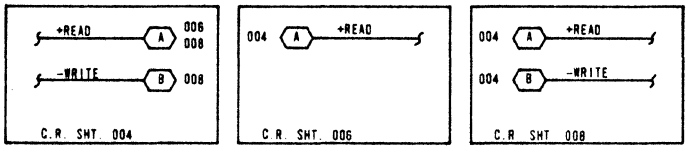
EACH PRINTED CIRCUIT BOARD, UNDER IDEAL CONDITIONS, WOULD BE REPRESENTED ON ONE SHEET. HOWEVER, DUE TO THE LARGE NUMBER OF CIRCUITS LOCATED ON SOME BOARDS, MULTIPLE SHEETS MAY BE REQUIRED. THE BOARD TYPE IS LISTED AT THE BOTTOM OF EACH DIAGRAM SHEET. THE BOARD LOCATION WITHIN THE LOGIC CHASSIS MAY ALSO ACCOMPANY THE BOARD TYPE. EACH SYMBOL ON THE DIAGRAM REPRESENTS A PORTION OF AN INTEGRATED CIRCUIT, THE ENTIRE INTEGRATED CIRCUIT OR A DISCRETE COMPONENT. EACH SYMBOL REFLECTS THE LOGIC FUNCTION IDENTIFIER, ELEMENT OR COMPONENT TYPE, AND THE ELEMENT OR COMPONENT LOCATION ON THE BOARD. COMPONENT LOCATION IS DEFINED BY AN ALPHANUMERIC MATRIX DEPENDING ON THE TYPE OF PRINTED CIRCUIT BOARD USED. FOR INFORMATION ON THE COMPONENT OR ELEMENT TYPES USED IN THIS LOGIC SET, REFER TO KEY TO LOGIC SYMBOLOGY MANUAL, CDC PUBLICATION NUMBER 62172400.

QUALIFYING SYMBOLS

& = AND
1 = OR
1 = INVERTER
X→Y = X(INPUTS) DECODED OR ENCODED TO Y(OUTPUTS)
X/Y = X(INPUT LEVEL) CONVERTED TO Y(OUTPUT LEVEL)
1 = ONE-SHOT MULTIVIBRATOR
= SCHMITT TRIGGER WITH LEAST POSITIVE TRIGGER POINT ADJUSTABLE

ON BOARD, OFF SHEET TAGGING

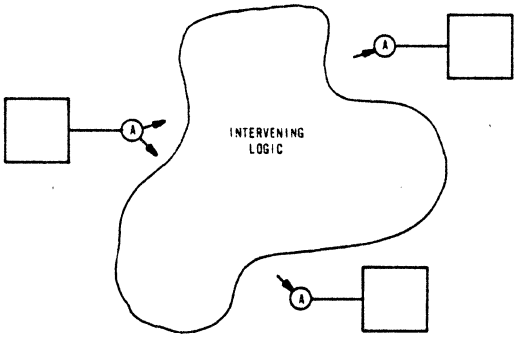
IN A LOGIC DIAGRAM SET HAVING MORE THAN ONE SHEET, A HEXAGON IS USED TO INDICATE THAT THE SIGNAL IS COMING FROM, OR GOING TO, ANOTHER SHEET OF THE SAME BOARD. (NOTE: EACH SIGNAL NAME IN THIS LOGIC SET HAS BEEN PRECEDED BY A "+" (INDICATING AN ACTIVE HI) OR A "-" (INDICATING AN ACTIVE LO)).



NON-STANDARD ABBREVIATIONS

ON SHEET TAGGING

THE SMALL CIRCLES WITH ALPHA CHARACTERS INSIDE ARE USED TO SHOW A SIGNAL PATH WITHOUT ACTUALLY RUNNING A LINE FROM ONE POINT TO ANOTHER. A CIRCLE WITH AN ARROW POINTING AWAY FROM IT IS THE SIGNAL ORIGIN. IN DIRECT LINE WITH THE ORIGIN ARROW, ANOTHER CIRCLE IS DRAWN WITH AN ARROW POINTING TOWARD IT. THIS IS THE SIGNAL DESTINATION.



VOLTAGE LEVELS

1 ANALOG OR NON-LOGIC LEVELS

2 NON-STANDARD LOGIC LEVEL

3. LOGIC LEVELS

DTL LOGIC OPERATION

HIGH (LOGICAL 1) = +2.6 TO +5.0 VOLTS
LOW (LOGICAL 0) = 0.0 TO +0.45 VOLTS
SWITCHING POINT = +1.1 TO +1.9 VOLTS

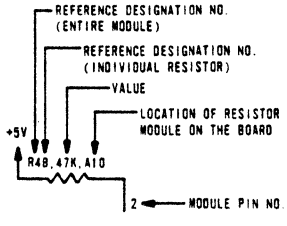
TTL LOGIC OPERATION

HIGH (LOGICAL 1) = +2.8 TO +5.0 VOLTS
LOW (LOGICAL 0) = 0.0V TO +0.45 VOLTS
SWITCHING POINT = + 85V TO +1.9 VOLTS

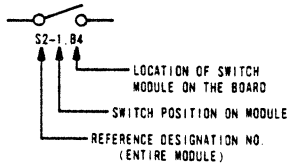
MISCELLANEOUS INDICATORS

= WIRED FUNCTION SOMEWHERE ALONG SIGNAL PATH
= BI-DIRECTIONAL LINE

RESISTOR MODULES

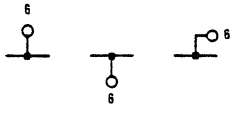


SWITCH MODULES



TEST POINTS

THE CLASS DESIGNATION LETTERS "TP" HAVE NOT BEEN SHOWN ON THIS LOGIC SET. THEREFORE, THE TEST POINTS APPEAR AS FOLLOWS:



RAM/E-ROM CARD LOGIC DIAGRAMS

Following pages contain the logic circuit diagrams which apply for the RAM/E-ROM card used in the basic logic module. Card 5ACD-X uses the full E-ROM capability of 4K words (used for full edit capability in a terminal); other versions may use less E-ROM. The backup page descriptions which accompany the E-ROM logic circuit diagrams apply to any amount of E-ROM up to the 4K words maximum (16 E-ROM chips being present on the card provide the 4K and each E-ROM chip being absent drops the total available words by 256 words).

DIAGRAM 000
SPECIAL FUNCTION SWITCHES
AND LED DRIVERS

This diagram shows I/O control circuits, LED register/driver circuits, and special function input switches/multiplexers/drivers. Additional special function switches/multiplexers appear on diagram 001.

I/O CONTROL (gates 141D13C, 140B15A, etc.) — NAND gate 140B15A issues an active low strobe pulse when +Address Bus $2^{15} - 2^{13}$ lines (P2-30, 29, and 28 from the shared bus) = 110_2 and +Output Strobe signal (P2-37 from the processor) pulses active high. This condition specifies that the processor is issuing an Output Operator Indicators function (see Programming in Section 2). The strobe pulse from NAND 140B15A loads register 520A10 and 520A14 (see LED Register/Driver Circuits description following). NAND gate 140B15B issues an active low strobe pulse when +Address Bus $2^{15} - 2^{13}$ lines (P2-30, 29, and 28) from the shared bus) = 110_2 and +Input Strobe signal (P2-38 from the processor) pulses active high. This condition specifies that the processor is issuing one of several possible Input Switches functions (see Programming in Section 2). The strobe pulse from NAND 140B15B enables drivers 939B10 and 939B14 (see Special Function Input Switches Data Drivers description following). Note that +Address Bus $2^{15} - 2^{13}$ lines continue on diagram 001 for use by the memory control circuits.

LED REGISTER/DRIVER CIRCUITS (520A10, 520A14, 200A9A - 200A9F, 200D10A, and 200D10C) — The quad, D-type, edge-triggered, flip-flop LED register (520A10 and 520A14) loads with the present +Data Bus $2^7 - 2^0$ contents when +Address Bus $2^{15} - 2^{13} = 110_2$ and an active +Output Strobe occurs (see I/O Control description preceding). This allows the processor to issue (via the +Data Bus $2^7 - 2^0$ lines) signals to indicators (LEDs) on an external operator's panel. Such signals/indicators show various operating mode conditions (see Programming in Section 2 for definition of these various conditions). An active low -Master Reset signal (diagram 001 from the processor) clears the LED register.

SPECIAL FUNCTION SWITCHES (S1-2 through S1-7, S2-1, and S2-7, on diagram 000. Also S2-2 through S2-5 on diagram 001.) These switches allow manually setting/selecting the firmware functions named by the switches. Such functions are received by the processor by several Input Switches functions described in Section 2. Any of these switches being open places a logic high active (logical 1), for the switch's named function, on the connected Special Function Input Multiplexer (see description following). Any of these switches being closed disables its named function by placing a logic low (logical 0) on the connected multiplexer input.

SPECIAL FUNCTION INPUT MULTIPLEXERS (508A11, 508A12, and 508A13 on diagram 000. Also 508A15 on diagram 001) — These multiplexers select an 8-bit, Input function, data word for transmission to the processor via the Special Function Input Data Drivers (see description following). Which word selected from the multiplexer data inputs depends on the binary value of the multiplexer select inputs. These select inputs are +Address Bus $2^2 - 2^0$ which specify the type of Input function being requested by the processor (see Programming in Section 2). Many of the multiplexer inputs come from other circuit cards on the shared bus or from an operator panel. The multiplexers select Input function code bits and transmit them to the processor for each function as follows.

MUX Select Inputs		Function On MUX Output for Each Data Bus Line Driver $2^7 - 2^0$ (from MUX's shown on diagrams 000 and 001)							
A 2^1	A 2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	+On Line	+Keylock	+Keyboard Locked LED	-Search Memory (Edit)	-Printer Present	+Full Duplex	+Char, Line, Block Mode (S2-1)	+Char, Line, Block Mode (S2-3)
0	1	+Null Background Char	+Enable Circuit Assurance	-1920 Char	-Answer back Present	-Multidrop Present	+Batch Mode	+Enable Scroll	+Constant Req to Send
1	0	+Enable Termination Code X'mit	+Enable Protected Field X'mit	+Enable X-Y Positioning	+Constant DTR	-Maintenance Mode	+Enable EOT Disconnect	+Enable EOT Termination	+Enable ETX Termination
1	1	+Enable Auto Print	-Cassette Present	(Tied 0)	(Tied 0)	(Tied 0)	+Test Mode	+Print Local	+Print On Line

SPECIAL FUNCTION INPUT DATA DRIVERS (939B10 and 939B14) — With any Input Special Function switch function active from the processor (P2-28, P2-29, P2-30, and P2-38 — See Programming in Section 2), I/O control gate 140B15B enables these drivers. The drivers send the 8-bit, special function, input data word selected by the multiplexers (see description preceding) to the processor via the shared Data Bus $2^7 - 2^0$ lines (diagram 002).

S2-6 SWITCH — When open, S2-6 issues an active high +60 Hz output signal for refresh circuit use.

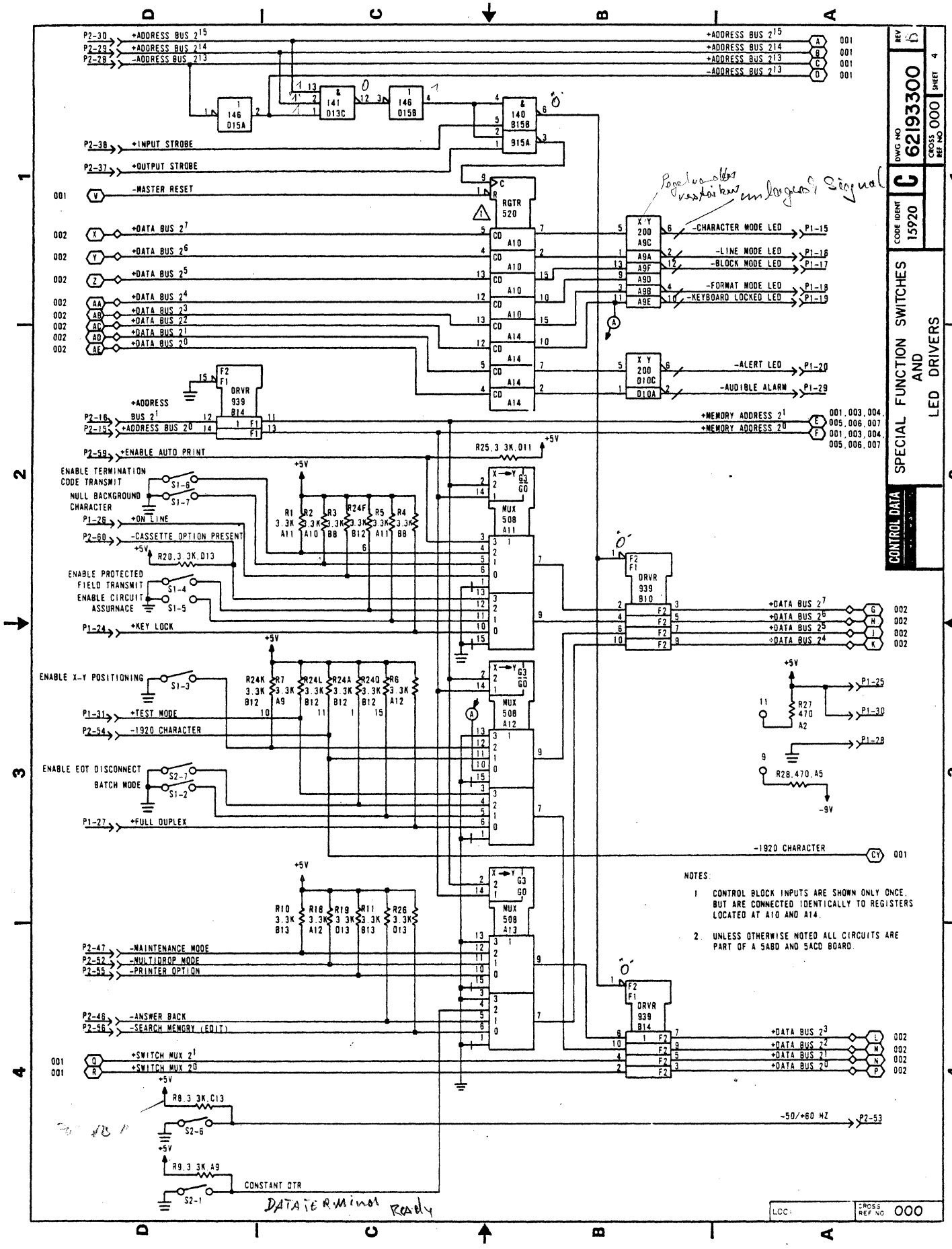

SPECIAL FUNCTION SWITCHES AND LED DRIVERS
CONTROL DATA
DWG NO 62193300
CODE IDENT 15920
CROSS REF NO 000
SHEET 4
REV B
+ADDRESS BUS 2^15
+ADDRESS BUS 2^14
+ADDRESS BUS 2^13
-ADDRESS BUS 2^13
+INPUT STROBE
+OUTPUT STROBE
-MASTER RESET
+DATA BUS 2^7
+DATA BUS 2^6
+DATA BUS 2^5
+DATA BUS 2^4
+DATA BUS 2^3
+DATA BUS 2^2
+DATA BUS 2^1
+DATA BUS 2^0
-CHARACTER MODE LED
-LINE MODE LED
-BLOCK MODE LED
-FORMAT MODE LED
-KEYBOARD LOCKED LED
-ALERT LED
-AUDIBLE ALARM
+MEMORY ADDRESS 2^1
+MEMORY ADDRESS 2^0
+ENABLE AUTO PRINT
ENABLE TERMINATION CODE TRANSMIT
NULL BACKGROUND CHARACTER
+ON LINE
-CASSETTE OPTION PRESENT
ENABLE PROTECTED FIELD TRANSMIT
ENABLE CIRCUIT ASSURNACE
+KEY LOCK
ENABLE X-Y POSITIONING
+TEST MODE
-1920 CHARACTER
ENABLE EOT DISCONNECT
BATCH MODE
+FULL DUPLEX
-MAINTENANCE MODE
-MULTIDROP MODE
-PRINTER OPTION
-ANSWER BACK
-SEARCH MEMORY (EDIT)
+SWITCH MUX 2^1
+SWITCH MUX 2^0
-50/+60 HZ
CONSTANT OTR
DATA TERMINAL READY
NOTES:
1 CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE. BUT ARE CONNECTED IDENTICALLY TO REGISTERS LOCATED AT A10 AND A14.
2. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 5ABD AND 5ACD BOARD.

DIAGRAM 001
MEMORY CONTROL CIRCUITS AND SPECIAL FUNCTION SWITCHES

These circuits consist of various memory control circuits and a portion of the Special Function Input Multiplexers.

SPECIAL FUNCTION INPUT MULTIPLEXERS (508A15) — See description for diagram 000.

MEMORY CONTROL CIRCUITS (various gates, etc.) — Following paragraphs describe the various memory control circuits/signals shown on the lower half of this diagram.

-RAM Enable signal is active low to allow I/O operation in the 1024-word refresh RAM contained in this card's circuits (diagram 003). This signal becomes active if any address in the range of addresses assigned to this RAM is received via the shared Address bus lines. This RAM's addresses assigned are from 2000_{16} through $23FF_{16}$ for basic display refresh (12 lines of 80 characters each). Addresses 2400_{16} through $277F_{16}$ for extended display refresh (12 additional lines of 80 characters each) are provided by a RAM in the extended memory option card which may be on the shared bus. Specifically, -RAM Enable signal is active low, with extended memory present (-1920 Character signal from diagram 000 being active low), only if Address 2^{15} - 2^{10} bits received (diagrams 000 and 003) are $0010\ 00_2$. This specifies RAM I/O operation for the address range 2000_{16} through $23FF_{16}$ of this card's RAM. If extended memory is not present (-1920 Character signal from diagram 00 being inactive high), -RAM Enable signal will be active low for Address 2^{15} - 2^{10} bits received being $0010\ 0X_2$. This allows RAM I/O operation in this card's RAM for the address range 2000_{16} through $27FF_{16}$.

-ROM Enable signal is active low to allow output from the firmware-storage ROM contained in this card's circuits (diagram 004 through 007). This signal becomes active if any address in the range of addresses assigned to this ROM is received via the shared Address bus lines. The ROM addresses assigned are from 0000_{16} through $1FFF_{16}$ depending on the amount of control firmware prestored in ROM chips on the card. Specifically, -ROM Enable signal is active low if Address 2^{15} - 2^{12} bits received (diagram 000 and this diagram) are 0000_2. This specifies a ROM read operation for the address range 0000_2 through $0FFF_2$ of this card's ROM.

-Enable Data Bus signal is active low to enable the Data bus drivers (diagram 002) to place either data read from RAM or data read from ROM on the shared Data bus. Specifically, -Enable Data Bus signal is active for any one of the following four sets of conditions:

- -CPU Memory Read signal (P2-33 from processor via shared bus) active low and a valid RAM address on the Address bus lines (-RAM Enable signal active low).
- -CPU Memory Read signal active low and a valid ROM address on the Address bus lines (-ROM Enable signal active low).
- -Memory Read signal (P2-35 from shared bus) active low and a valid RAM address on the Address bus lines (-RAM enable signal active low).
- -Memory Read signal active low and a valid ROM address on the Address bus lines (-ROM Enable signal active low).

-Master Reset signal (P2-31 from processor via receiver/driver 939B9) clears -Write Strobe and -Ready signals (see descriptions following). Active -Master Reset signal also clears the LED register (diagram 000).

-Write Strobe signal is active low to allow writing into RAM (diagram 003). When no Memory Write is active (P2-34 or P2-36), the inactive high output from NAND 140D11D results in a logic high on flip-flop 240A8A input pin 3. Since input pin 2 is tied permanent high, the highgoing, Ø2 clock input on input pin 4 makes output pin 7 low. This is the nonstrobe condition. If either -CPU Memory Write signal or -Memory Write signal (P2-34 or P2-36) is active low, and addressing is valid, the active high output from NAND 140D11D results in a logic low on flip-flop 240A8A input pin 3. Since input pin 2 is tied permanent high, the highgoing +Ø2 clock input on input pin 4 makes output pin 7 toggle high. This makes -Write Strobe signal active low. At the end of +Ø2, its complement (-Ø2) goes inactive high and loads the high from flip-flop 240A8A into flip-flop 175B8. The resulting high output from 175B8 pin 5 keeps -Write Strobe signal active until flip-flop 175B8 clears. Once activated, except for overriding -Master Reset (P2-31 from the processor), -Write Strobe clears as follows. The highgoing +Ø2 clock pulse following the one which activated -Write Strobe toggles flip-flop 240A8A so output pin 7 goes low. At this time, the Memory Write signal received from the shared bus (P2-34 or P2-36) should go inactive to end the present Write Strobe function. At the end of +Ø2, its complement (-Ø2) goes inactive high and loads the low from flip-flop 240A8A into flip-flop 175B8. The resulting low output from 175B8 pin 5 and the low output from 240A8A pin 7 ends the active -Write Strobe signal.

-Ready signal is active low to notify the shared bus circuits that these memory card circuits have either: 1) accepted a Write operation to RAM or 2) performed a requested Read operation from RAM or ROM. -Ready signal is active only while flip-flop 175B8 is set. This flip-flop sets at highgoing +Ø2 when either of the following conditions are present.

- AND gate 140D11D issuing active low for a Write to RAM function.
- AND gate 140D11A issuing active low for a Read from RAM or ROM function.

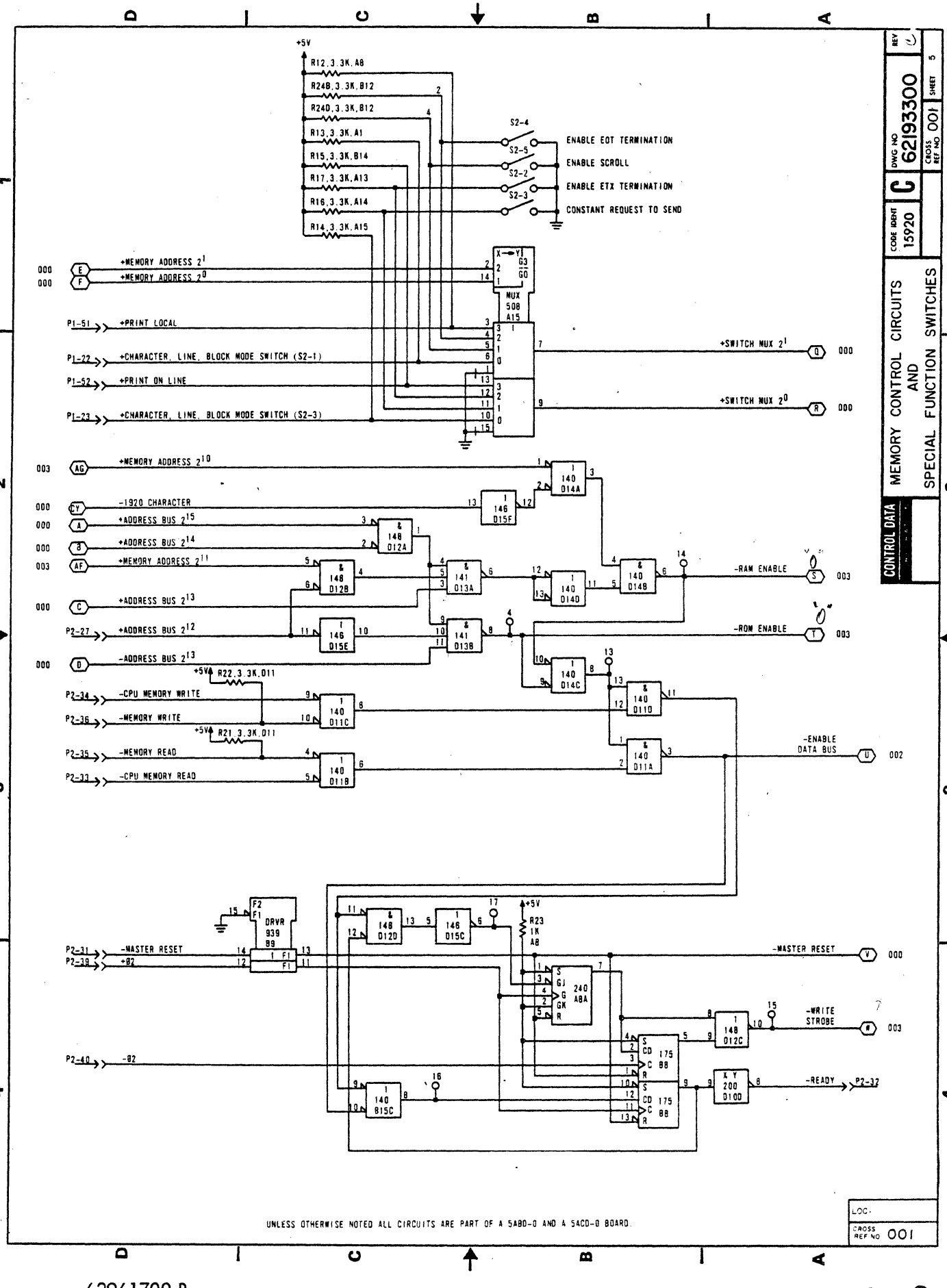

CONTROL DATA
MEMORY CONTROL CIRCUITS AND SPECIAL FUNCTION SWITCHES
DWG NO 62193300
REV J
SHEET 5
CODE IDENT 15920
C
CROSS REF NO 001
+5V
R12,3.3K,A8
R24B,3.3K,B12
R24D,3.3K,B12
R13,3.3K,A1
R15,3.3K,B14
R17,3.3K,A13
R16,3.3K,A14
R14,3.3K,A15
S2-4
S2-5
S2-2
S2-3
ENABLE EOT TERMINATION
ENABLE SCROLL
ENABLE ETX TERMINATION
CONSTANT REQUEST TO SEND
+MEMORY ADDRESS 2^1
+MEMORY ADDRESS 2^0
P1-51 +PRINT LOCAL
P1-22 +CHARACTER, LINE, BLOCK MODE SWITCH (S2-1)
P1-52 +PRINT ON LINE
P1-23 +CHARACTER, LINE, BLOCK MODE SWITCH (S2-3)
MUX 508 A15
+SWITCH MUX 2^1
+SWITCH MUX 2^0
+MEMORY ADDRESS 2^10
-1920 CHARACTER
+ADDRESS BUS 2^15
+ADDRESS BUS 2^14
+MEMORY ADDRESS 2^11
+ADDRESS BUS 2^13
P2-27 +ADDRESS BUS 2^12
-ADDRESS BUS 2^13
-RAM ENABLE
-ROM ENABLE
R22,3.3K,D11
R21,3.3K,D11
P2-34 -CPU MEMORY WRITE
P2-36 -MEMORY WRITE
P2-35 -MEMORY READ
P2-33 -CPU MEMORY READ
-ENABLE DATA BUS
DRVR 939 B9
P2-31 -MASTER RESET
P2-39 +B2
R23 1K A8
-MASTER RESET
-WRITE STROBE
P2-40 -B2
-READY P2-37
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 5ABD-0 AND A 5ACD-0 BOARD.
LOC.
CROSS REF NO 001

DIAGRAM 002
DATA BUS DRIVERS

Output from these circuits consists of an 8-bit word read from RAM or ROM and placed on the shared +Data bus lines. Also, the LED register (diagram 000) latches the +Data bus contents during an Output Operator Indicators function from the processor. In addition, the +Data bus contents are input to an 8-bit word location in RAM (diagram 003) during an active Write to RAM operation.

When -Enable Memory Data Bus signal (diagram 001) is active low, the TTL driver circuits (939B11 and 939B13) place on the shared +Data bus lines either: 1) an 8-bit word read from an E-ROM address (+ROM Memory bit $2^7 - 2^0$, diagrams 004 through 007) or 2) an 8-bit word read from a RAM address (+Memory bit $2^7 - 2^0$, diagram 003).

Other 939 type Data bus drivers exist, in circuits shown on diagram 000, which issue +Data Bus $2^7 - 2^0$ signals that bypass the drivers on diagram 002 and pass (via wired ORs) directly to the I/O +Data bus lines. Such data consists of special function switch input information requested by the processor by one of the several possible Input Switches functions (see description for diagram 000).

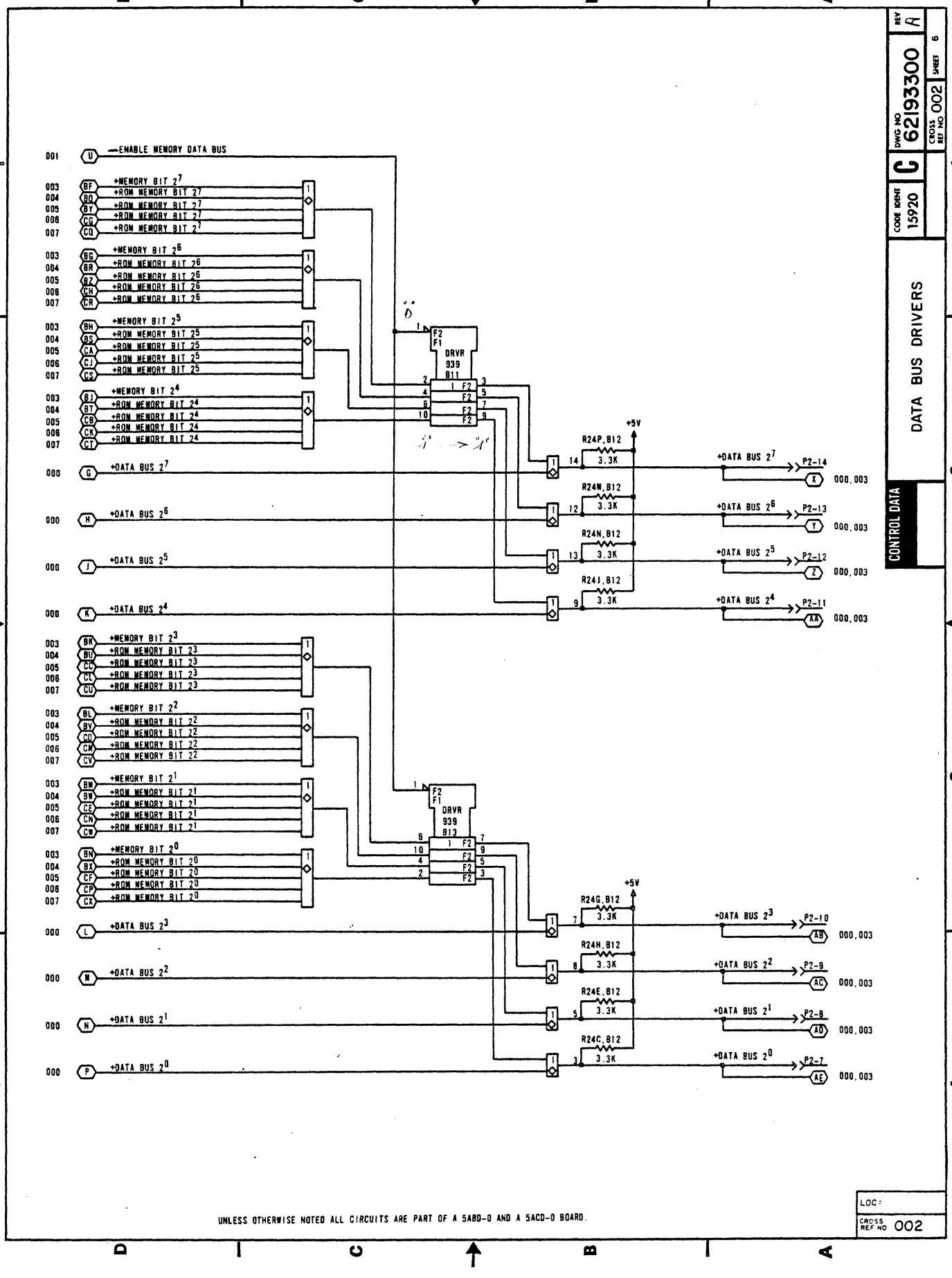

DATA BUS DRIVERS
CONTROL DATA
DWG NO 62193300
REV A
SHEET 6
CODE IDENT 15920
CROSS REF NO 002
001 U —ENABLE MEMORY DATA BUS
+MEMORY BIT 2^7
+ROM MEMORY BIT 2^7
+MEMORY BIT 2^6
+ROM MEMORY BIT 2^6
+MEMORY BIT 2^5
+ROM MEMORY BIT 2^5
+MEMORY BIT 2^4
+ROM MEMORY BIT 2^4
+DATA BUS 2^7
+DATA BUS 2^6
+DATA BUS 2^5
+DATA BUS 2^4
+MEMORY BIT 2^3
+ROM MEMORY BIT 2^3
+MEMORY BIT 2^2
+ROM MEMORY BIT 2^2
+MEMORY BIT 2^1
+ROM MEMORY BIT 2^1
+MEMORY BIT 2^0
+ROM MEMORY BIT 2^0
+DATA BUS 2^3
+DATA BUS 2^2
+DATA BUS 2^1
+DATA BUS 2^0
DRVR 939 B11
DRVR 939 B13
F2
F1
+5V
R24P,B12 3.3K
R24M,B12 3.3K
R24N,B12 3.3K
R24J,B12 3.3K
R24G,B12 3.3K
R24H,B12 3.3K
R24E,B12 3.3K
R24C,B12 3.3K
P2-14 X
P2-13 Y
P2-12 Z
P2-11 AA
P2-10 AB
P2-9 AC
P2-8 AD
P2-7 AE
000,003
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 5ABD-0 AND A 5ACD-0 BOARD.
LOC:
CROSS REF NO 002

DIAGRAM 003
RAM MEMORY AND ROM SELECTION CIRCUITS

These circuits include a ROM chip selector and a 1K RAM chip.

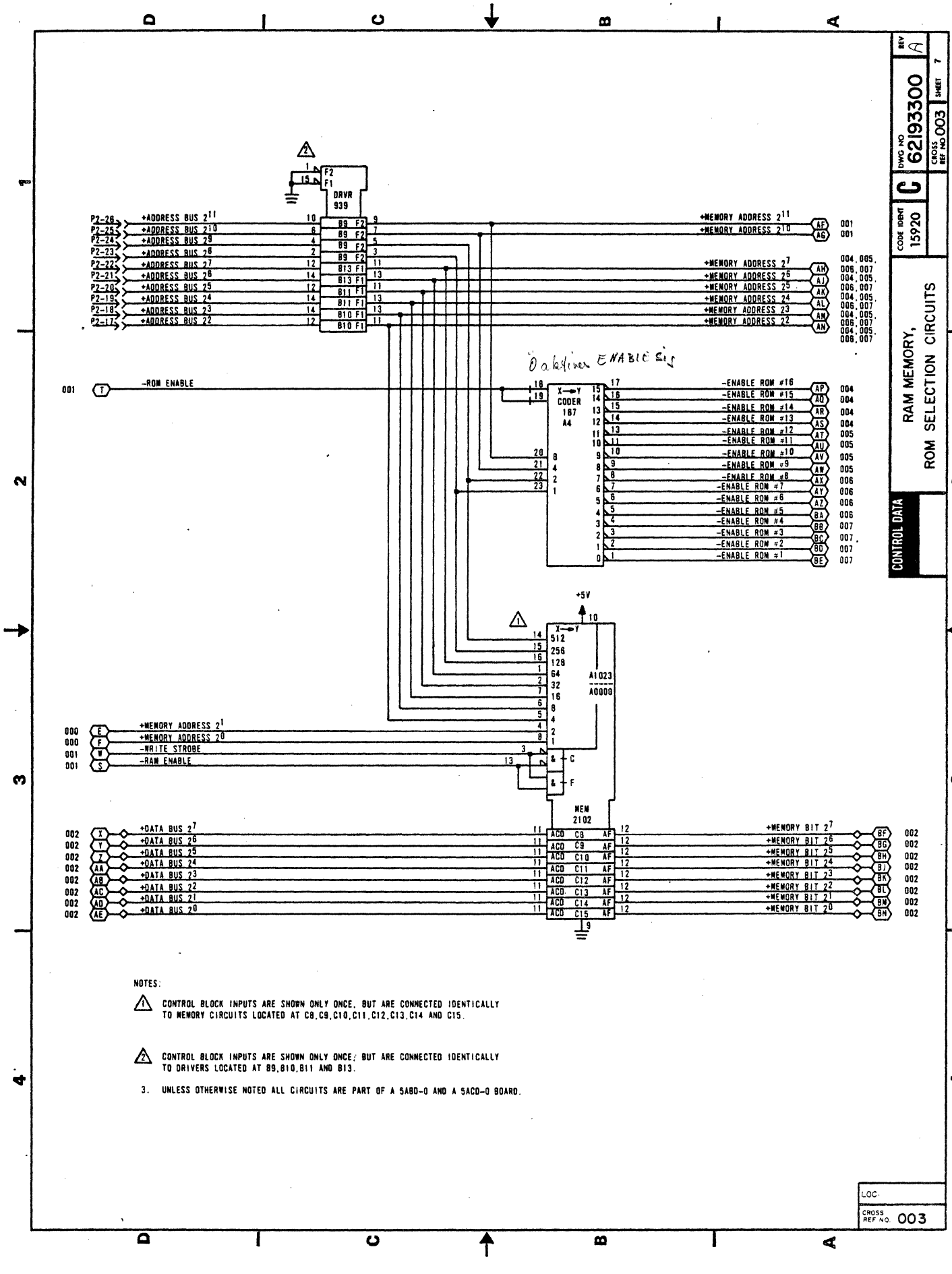
ROM CHIP SELECTOR (167A4) — The -Address Bus $2^{11} - 2^{8}$ lines from the processor (boosted by constantly enabled receiver/drivers 939B9, 939B10, 939B11, and 939B13) are the ROM chip select value. When -ROM Enable signal (diagram 001) is active low, one-of-sixteen decoder 167A4 translates this 4-bit, chip address value (range of $0000_2 - 1111_2$) and issues an active low -Enable ROM signal which selects the addressed ROM chip. This allows addressing up to 16 ROM chips (diagrams 004 through 007).

The +Address Bus $2^{7} - 2^{2}$ lines from the processor (boosted by constantly active receiver/drivers 939B10, 939B11, and 939B13) are six of the eight bits which specify the word address within any ROM chip (one of 256 words maximum). These six bits go to all ROM chips present on the card (diagrams 004 through 007). The other two bits (2^{1} and 2^{0}) required to address a word within a ROM chip go from diagram 000 to the ROM chips.

RAM (772AC8 through 772AC15) — These eight integrated circuits are each a non-destructive-read, TTL-compatible, random-access memory containing 1024, 1-bit word locations. Together, they provide read/write storage for up to 1024, 8-bit words. When -RAM Enable signal (diagram 001) is active low, either a Write or Read operation occurs for a RAM word location as addressed by +Memory Address $2^{9} - 2^{0}$ from the processor.

During a write mode, -Write Strobe signal (diagram 001) must pulse active low. This allows +Data Bus $2^{7} - 2^{0}$ (diagram 002) to enter all eight $2^{7} - 2^{0}$ RAM chips which are selected concurrently by an active low -RAM Enable signal. The data enters at the word address (range of 0 through 1023_{10}) specified by +Memory Address $2^{9} - 2^{0}$ value.

During a read mode, -Write Strobe signal (diagram 001) must be high. The word addressed by +Memory Address $2^{9} - 2^{0}$ appears on +Memory bit $2^{7} - 2^{0}$ lines. This word passes to the Data bus drivers (diagram 002). Access time for this RAM is 1000 nsec.



NOTES:

1. CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE, BUT ARE CONNECTED IDENTICALLY TO MEMORY CIRCUITS LOCATED AT C8,C9,C10,C11,C12,C13,C14 AND C15.

2. CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE, BUT ARE CONNECTED IDENTICALLY TO DRIVERS LOCATED AT B9,B10,B11 AND B13.

3. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 5A80-0 AND A 5AC0-0 BOARD.

LOC.
CROSS REF NO. 003

DIAGRAM 004
E-ROM WORD ADDRESS 3072 TO ADDRESS 4095

This diagram shows the fourth set of four E-ROM chips which may be present on the card. Each 771 type chip (Intel 1702A type, or equivalent) is programmable with up to 256, 8-bit, read-only words. Programming is a special manufacturing procedure requiring special burn-in equipment. Once programmed (burned-in) data is nonvolatile and can be erased to all zero bits by exposure to ultra-violet light. Since programming requires special manufacturing equipment and unique word bit patterns for various customer requirements, such information is not included in this text (see Foreword).

ROM ADDRESSING - The eight address inputs common to each E-ROM (+Memory Address $2^7 - 2^0$, from diagrams 000 and 003) allow selecting up to 256, 8-bit, word locations in each E-ROM. When an address is present and: 1) the - Enable ROM #n input to a particular E-ROM is active low (diagram 003), 2) the Program select input signal (pin 13) is +5 volts, 3) input pins 12 and 15 are +5 volts, and 4) pins 16 and 24 are -9 volts — then the 8-bit word stored at that address within the E-ROM appears on the eight, common + ROM Memory bit $2^7 - 2^0$ output lines. In read mode, these eight lines enter the Data bus driver circuit on diagram 002.

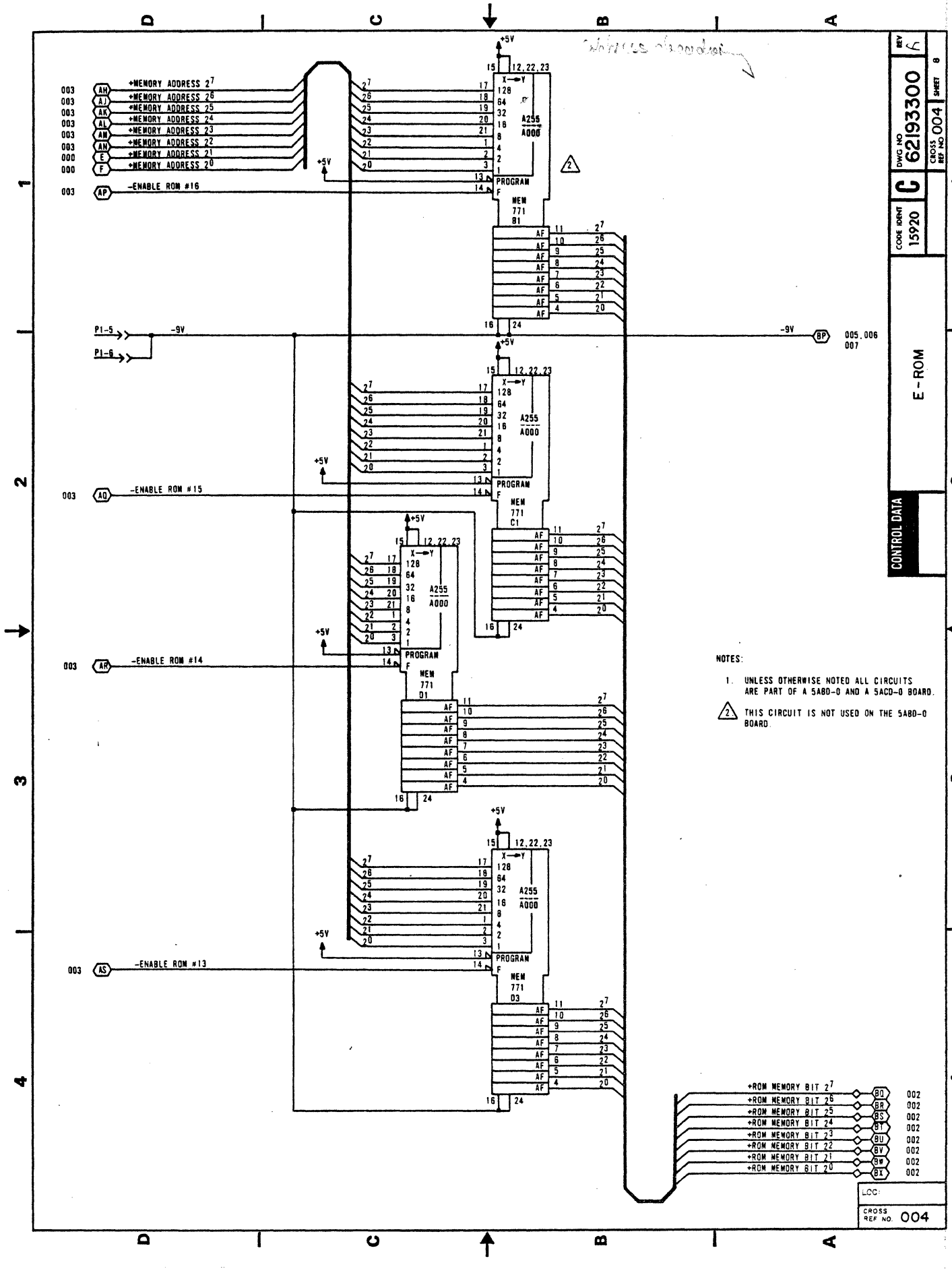

+MEMORY ADDRESS 27
+MEMORY ADDRESS 26
+MEMORY ADDRESS 25
+MEMORY ADDRESS 24
+MEMORY ADDRESS 23
+MEMORY ADDRESS 22
+MEMORY ADDRESS 21
+MEMORY ADDRESS 20
-ENABLE ROM #16
-ENABLE ROM #15
-ENABLE ROM #14
-ENABLE ROM #13
+5V
-9V
PROGRAM MEM 771 B1
PROGRAM MEM 771 C1
PROGRAM MEM 771 D1
PROGRAM MEM 771 D3
A255 A000
12,22,23
+ROM MEMORY BIT 27
+ROM MEMORY BIT 26
+ROM MEMORY BIT 25
+ROM MEMORY BIT 24
+ROM MEMORY BIT 23
+ROM MEMORY BIT 22
+ROM MEMORY BIT 21
+ROM MEMORY BIT 20
NOTES:
1. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 5A80-0 AND A 5AC0-0 BOARD.
2. THIS CIRCUIT IS NOT USED ON THE 5A80-0 BOARD.
CONTROL DATA
E-ROM
DWG NO 62193300
CODE IDENT 15920
CROSS REF NO 004
LOC:
CROSS REF NO. 004

DIAGRAM 005
E-ROM WORD ADDRESS 2048 TO ADDRESS 3071

This diagram shows the third set of four E-ROM chips which may be present on the card. The chips are the same type as described by the backup page for diagram 004. They share the same Memory Address input lines (diagram 000 and 003) and the same Data bus drivers (diagram 002). However, each E-ROM chip has its unique -Enable ROM #n input signal (diagram 003).

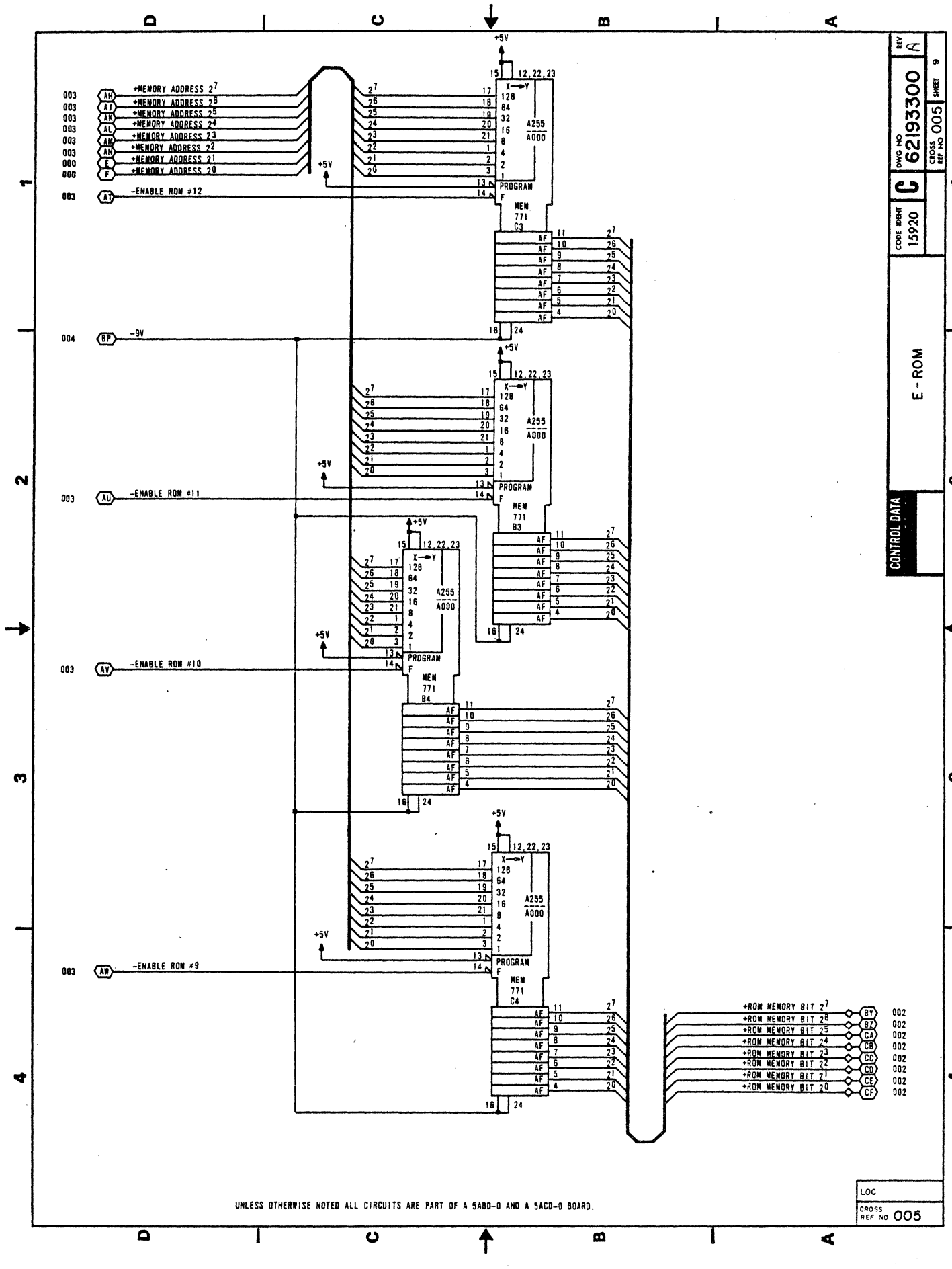

+MEMORY ADDRESS 27
+MEMORY ADDRESS 26
+MEMORY ADDRESS 25
+MEMORY ADDRESS 24
+MEMORY ADDRESS 23
+MEMORY ADDRESS 22
+MEMORY ADDRESS 21
+MEMORY ADDRESS 20
-ENABLE ROM #12
-ENABLE ROM #11
-ENABLE ROM #10
-ENABLE ROM #9
-9V
+5V
A255
A000
PROGRAM
MEM
771
C3
B3
B4
C4
+ROM MEMORY BIT 27
+ROM MEMORY BIT 26
+ROM MEMORY BIT 25
+ROM MEMORY BIT 24
+ROM MEMORY BIT 23
+ROM MEMORY BIT 22
+ROM MEMORY BIT 21
+ROM MEMORY BIT 20
REV A
DWG NO 62193300
SHEET 9
CODE IDENT 15920
C
CROSS REF NO 005
E - ROM
CONTROL DATA
LOC
CROSS REF NO 005
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 5ABD-0 AND A 5ACD-0 BOARD.

DIAGRAM 006
E-ROM WORD ADDRESS 1024 TO ADDRESS 2047

This diagram shows the second set of four E-ROM chips which may be present on the card. The chips are the same type as described by the backup page for diagram 004. They share the same Memory Address input lines (diagram 000 and 003) and the same Data bus drivers (diagram 002). However, each E-ROM chip has its unique -Enable ROM #n input signal (diagram 003).

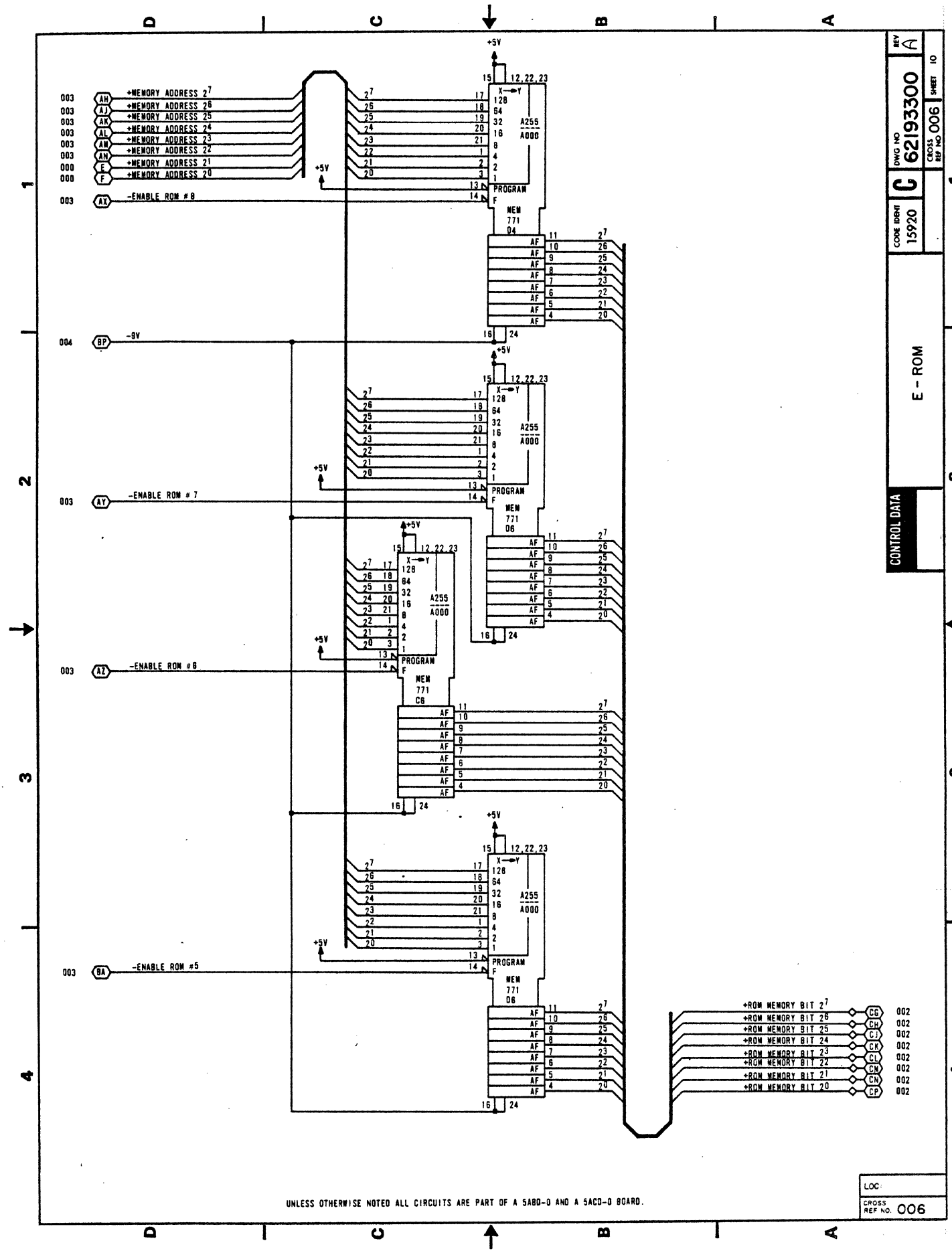
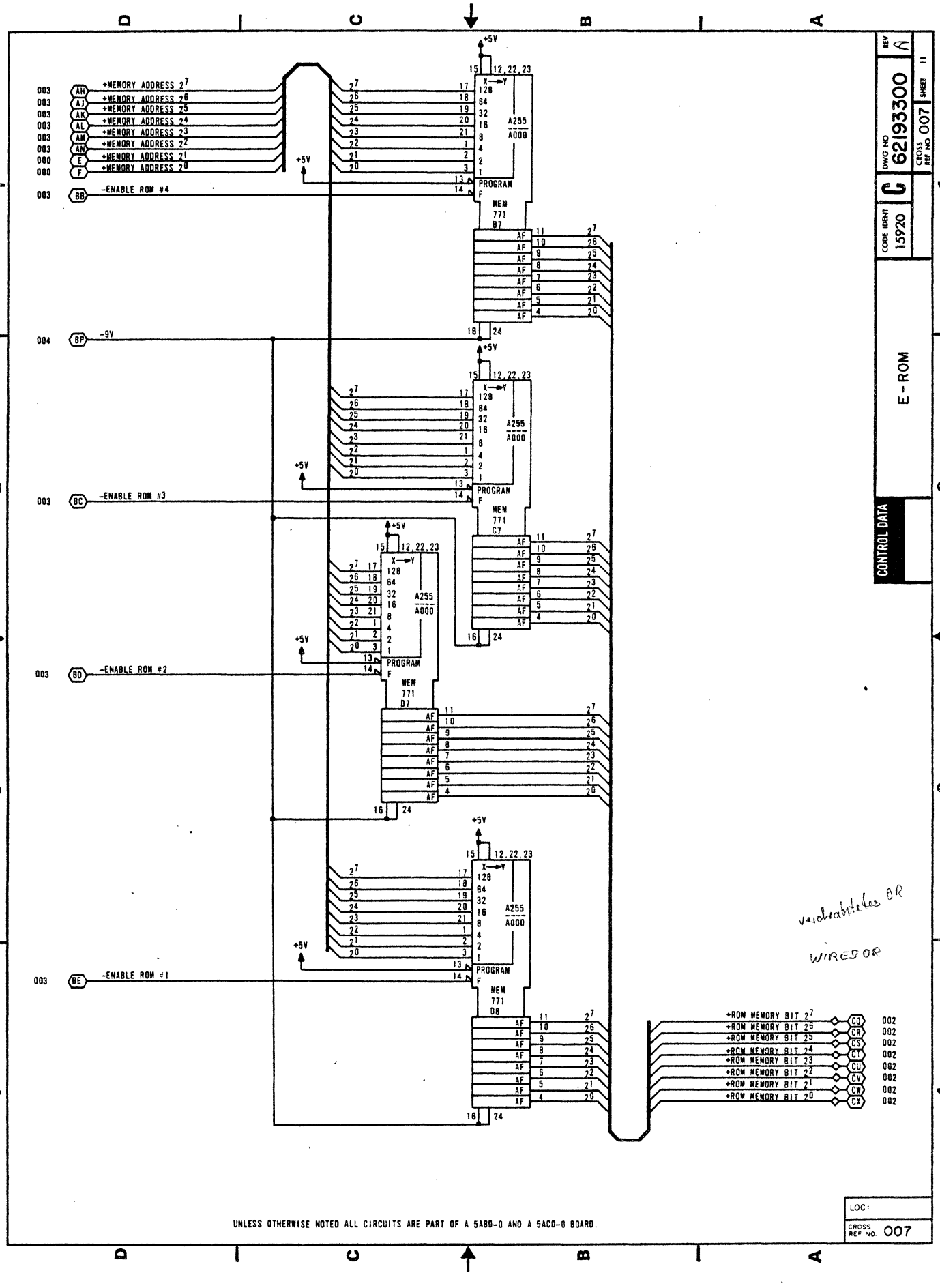

+MEMORY ADDRESS 27
+MEMORY ADDRESS 26
+MEMORY ADDRESS 25
+MEMORY ADDRESS 24
+MEMORY ADDRESS 23
+MEMORY ADDRESS 22
+MEMORY ADDRESS 21
+MEMORY ADDRESS 20
-ENABLE ROM #8
-ENABLE ROM #7
-ENABLE ROM #6
-ENABLE ROM #5
-9V
+5V
A255
A000
PROGRAM
MEM
771
04
06
C6
+ROM MEMORY BIT 27
+ROM MEMORY BIT 26
+ROM MEMORY BIT 25
+ROM MEMORY BIT 24
+ROM MEMORY BIT 23
+ROM MEMORY BIT 22
+ROM MEMORY BIT 21
+ROM MEMORY BIT 20
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 5A80-0 AND A 5AC0-0 BOARD.
DWG NO 62193300
REV A
SHEET 10
CODE IDENT 15920
C
CROSS REF NO. 006
E - ROM
CONTROL DATA
LOC:
CROSS REF NO. 006

DIAGRAM 007
E-ROM WORD ADDRESS 0000 TO ADDRESS 1023

This diagram shows the first set of four E-ROM chips which may be present on the card. The chips are the same type as described by the backup page for diagram 004. They share the same Memory Address input lines (diagram 000 and 003) and the same Data bus drivers (diagram 002). However, each E-ROM chip has its unique -Enable ROM #n input signal (diagram 003).


CONTROL DATA
E-ROM
DWG NO 62193300
REV A
CODE IDENT 15920
C
SHEET 11
CROSS REF NO 007
+MEMORY ADDRESS 2^7
+MEMORY ADDRESS 2^6
+MEMORY ADDRESS 2^5
+MEMORY ADDRESS 2^4
+MEMORY ADDRESS 2^3
+MEMORY ADDRESS 2^2
+MEMORY ADDRESS 2^1
+MEMORY ADDRESS 2^0
-ENABLE ROM #4
-ENABLE ROM #3
-ENABLE ROM #2
-ENABLE ROM #1
-9V
+5V
PROGRAM MEM 771 B7
PROGRAM MEM 771 C7
PROGRAM MEM 771 D7
PROGRAM MEM 771 D8
A255 A000
+ROM MEMORY BIT 2^7
+ROM MEMORY BIT 2^6
+ROM MEMORY BIT 2^5
+ROM MEMORY BIT 2^4
+ROM MEMORY BIT 2^3
+ROM MEMORY BIT 2^2
+ROM MEMORY BIT 2^1
+ROM MEMORY BIT 2^0
variables OR
WIRED OR
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 5A80-0 AND A 5AC0-0 BOARD.
LOC:
CROSS REF NO. 007

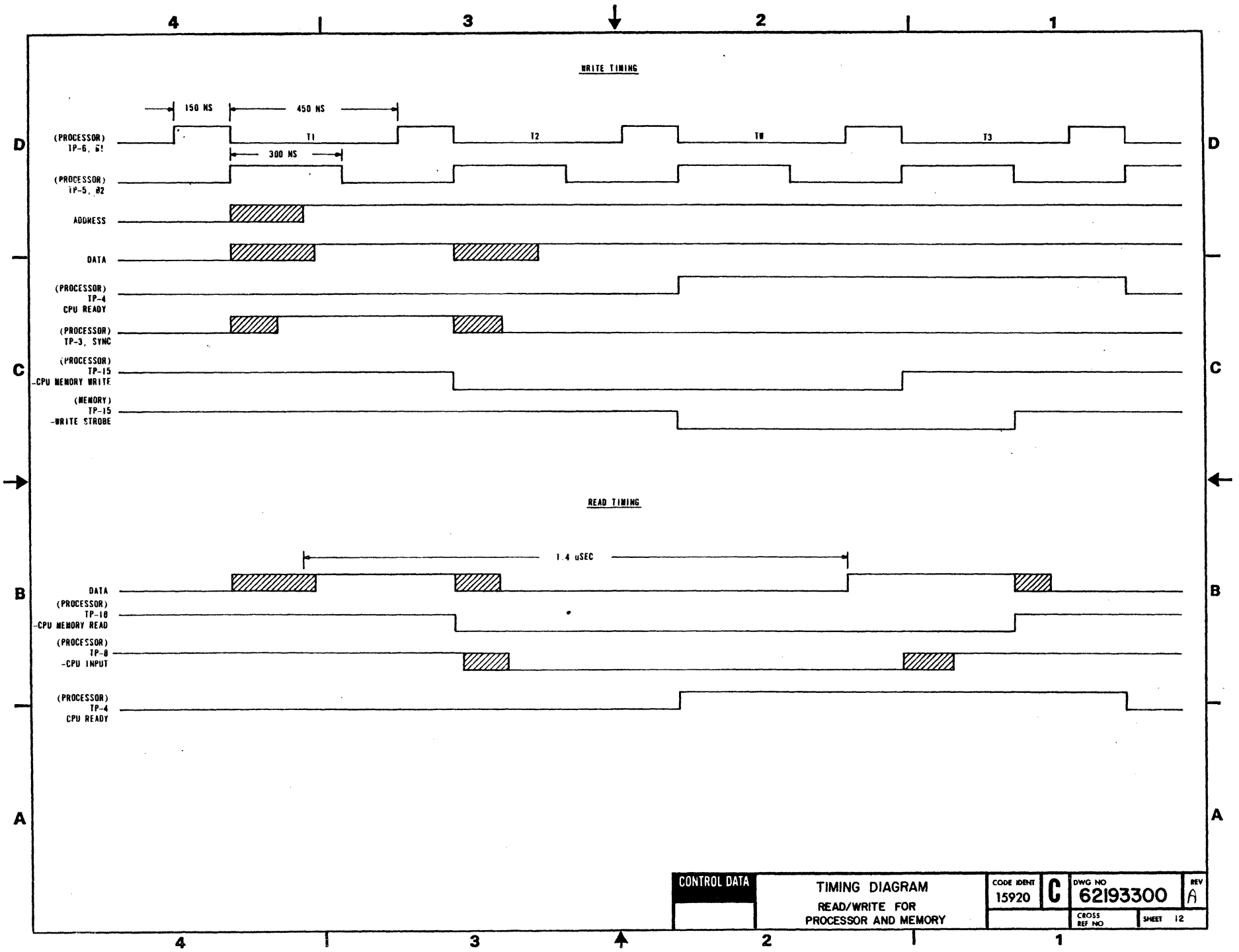
TIMING DIAGRAM
READ/WRITE FOR PROCESSOR AND MEMORY

The top half of this diagram contains waveforms which illustrate timing characteristics of a Write operation. The bottom half illustrates those for a Read operation. In both cases, the processor card circuits control the operation and Ø1 and Ø2 signals are the two timing pulses which govern the operating speed of the microprocessor contained in the processor card. See the description of logic diagram 102 for Ø1 and Ø2 details.

The Address of the RAM location being written into, or of the RAM or ROM location being read from, may be placed on the shared Address bus by one of many functional cards on the bus (e.g., processor, refresh, an I/O card, etc.). Descriptions for logic diagrams 000, 001, and 003 define the Address values used.

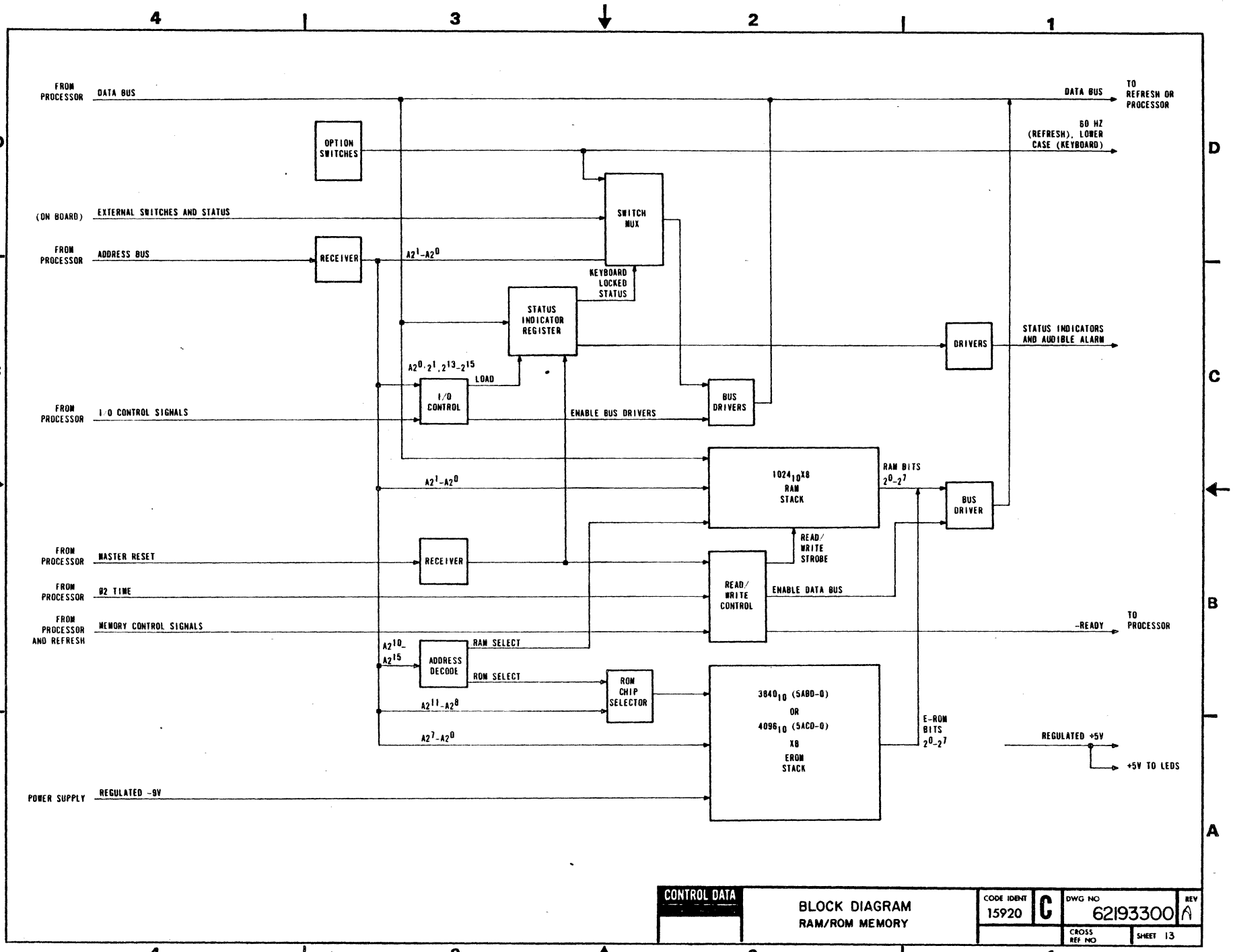
WRITE TIMING — Data for writing into RAM may be placed on the shared Data bus by one of several cards on the bus (e.g., processor, an I/O card, etc.). Descriptions for logic diagrams 002 and 003 define Write-into-RAM data. Sync signal is issued by the processor at the start of each machine cycle (see description of logic diagram 100). - CPU Memory Write signal is issued by the processor, via the shared bus, to write the 8-bit Data bus contents into RAM at a location specified by the 16-bit Address bus contents. If not disabled, CPU Ready signal (diagram 100) becomes active after the Memory Control circuits (diagram 001) place an active - Ready signal on the shared bus. - Write Strobe signal (diagram 001) is active to write into RAM.

READ TIMING — An addressed RAM or ROM location yields its 8-bit data word for placement on the shared Data bus when either: 1) -CPU Memory Read (from processor) or 2) - Memory Read (from some shared bus card) becomes active. If the Read is for processor use, - CPU Input signal (diagram 100) is active low long enough to accomplish the Data input. CPU Ready signal (diagram 100) becomes active after the Memory Control Circuits (diagram 001) place an active - Ready signal on the shared bus.


WRITE TIMING
150 NS
450 NS
300 NS
T1
T2
TW
T3
(PROCESSOR) TP-6, 5!
(PROCESSOR) TP-5, Ø2
ADDRESS
DATA
(PROCESSOR) TP-4 CPU READY
(PROCESSOR) TP-3, SYNC
(PROCESSOR) TP-15 -CPU MEMORY WRITE
(MEMORY) TP-15 -WRITE STROBE
READ TIMING
1.4 uSEC
DATA
(PROCESSOR) TP-18 -CPU MEMORY READ
(PROCESSOR) TP-8 -CPU INPUT
(PROCESSOR) TP-4 CPU READY
CONTROL DATA
TIMING DIAGRAM
READ/WRITE FOR PROCESSOR AND MEMORY
CODE IDENT 15920
C
DWG NO 62193300
REV A
CROSS REF NO
SHEET 12

BLOCK DIAGRAM
RAM/ROM MEMORY

This is a block diagram of the RAM/E-ROM card detailed logic circuits shown on the preceding pages of this logic diagram set. It identifies the major functional circuits of the RAM/E-ROM card. The diagram also serves as a functional flow summary. All of the functional circuits and signals identified on this diagram appear in a functional diagram figure in Section 4 where RAM/E-ROM theory of operation is described. Since thorough descriptions and references to the detailed logic circuits in Section 5 accompany the figure in Section 4, further description here would be duplication and is therefore omitted.



CONTROL DATA	BLOCK DIAGRAM RAM/ROM MEMORY	CODE IDENT 15920	C	DWG NO 62193300	REV A
				CROSS REF NO	SHEET 13

DISPLAY CONTROL PROCESSOR CARD LOGIC DIAGRAMS

Following pages contain the logic circuit diagrams for the display control processor card used in the basic logic module.

DIAGRAM 100
8080 MICROPROCESSOR AND
ADDRESS AND DATA BUS DRIVERS

This diagram shows the LSI Microprocessor, I/O Ready control, the Microprocessor Input Data Buffer/Drivers, and the Microprocessor Output Address Bus and Data Bus Drivers.

MICROPROCESSOR INPUT DATA BUFFERS/DRIVERS (939C9 and 939C10) — When enabled (microprocessor output pin 17 active) by an active low - CPU Input signal on driver input pins 1, these TTL circuits (National type DM8097 tri-state buffers, or equivalent) provide one Input Data byte to the microprocessor.

MICROPROCESSOR OUTPUT ADDRESS BUS AND DATA BUS BUFFER/DRIVERS (939D9 through 939D12) — These TTL circuits (National type DM8097 tri-state buffers) pass their particular microprocessor output signal when their enable input (pin 1 or 15) is active low. The 16 +Address bus lines provide shared bus addressing up to 64K 8-bit words or device addressing for up to 256 channels. +Gate Upper Address signal (P2-49 shared bus input) must be active high to transmit the high order four address bits. None of the driver enable inputs may be active low if another circuit card is using the shared bus. The upper four address bits have the special driver enable to allow the option of an external module being able to control memory locations (instead of the processor) under special circumstances. In such operation, the external module must prevent the enable to these upper four bit drivers and substitute, on the shared bus lines for these bits, other special address bits. Either +Hold Acknowledge signal being inactive low or - CPU Input signal being active low (OR gate 201D4D) allows transmitting the low-order 12 Address bus bits. The eight Data bus buffers/drivers transmit Data bits from the microprocessor to the shared Data bus when their enable input (pin 1 or 15) is active low. This occurs when neither - Hold Acknowledge signal nor -CPU Input signal is active low (NOR gate 140B5B). +Data bus 2^7 - 2^0 output connector pins (P2-14, P2-13, etc.) also carry Input data during input operations to the processor card. In this case, these data bits feed the microprocessor Input Data Buffer/Drivers.

I/O READY CONTROL (140D13C, 141D8B, etc.) — This circuit detects when an addressed shared bus circuit is ready. This may be when requested data is ready on the Data bus or when a circuit has accepted data from the processor. NOR 140D13B issues an active high +CPU Ready/+Data Ready signal if either of the following two Ready conditions are true:

- - Ready signal (P2-32 from a circuit on shared bus) active low and - Disable Ready signal (P2-48 from shared bus) inactive high.
- - Disable Ready signal inactive high, - CPU Memory Read signal (diagram 103) inactive high, and - CPU Memory Write signal (diagram 103) inactive high.

LSI MICROPROCESSOR (558C13) — This circuit (Intel MOS 8080 type, or equivalent) serves as a single-chip, 8-bit-parallel, central processor unit (CPU). It is the heart of the processor circuit card. All other circuits which connect to the microprocessor exists to properly serve its needs. The following paragraphs describe the chip's I/O signals. For internal circuit details, see the Control Data circuit type definition document (15135300) which defines the 558 type chip. If necessary, for further reference, see the vendor's specification (Intel Corporation, 3065 Bowers Avenue, Santa Clara, Califomia 95051 specification for Silicon Gate MOS 8080). For theory of operation of this chip, as used in this processor circuit card, see Microprocessor Functions in Section 4. Also, see Programming in Section 2 for the instruction repertoire and other programming information which determines the specific value/content of each I/O signal line at any particular time during operation.

+ Processor Reset signal (diagram 102) performs an initialize function in the microprocessor. While this signal is active high, the chip's internal program counter is cleared and the instruction register is set to zero. After active + Processor Reset, program execution starts with location zero of memory (memory being in a circuit card on the shared bus). Also, Interrupt Enable (INTE) and Hold Acknowledge (HLDA) conditions are cleared (reset). Reset does not clear flags, accumulator, or other registers; however, contents of HL and DE registers may be exchanged.

+Ø1 and +Ø2 signals (diagram 102) establish the basis for a microprocessor machine cycle. These signals are non-standard voltage levels, i.e., low is -1.0v to +0.6v and high is +10.4v to +13.6v. Each two interations of Ø1, accompanied by one interation of Ø2 (as shown in description for diagram 102), forms what is arbitrarily termed one State Time. Typically, a machine cycle consists of three to five State Times. Timing diagrams at the back of these processor logic diagrams, and in Sections 2 and 4, illustrate timing further.

+Address 2^{15} - 2^{0} signals (558C13 outputs) are Address bus information. These 16, three-state signals (high, low, or floating) allow addressing external memory locations (via an external, associated, Address bus) up to 64K 8-bit words or they specify an I/O device number (I/O channel) for up to 256 devices. Bit 2^{0} is the least significant. Bus drivers send these signals to the Address bus.

+Data Bus 2^{7} - 2^{0} signals (558C13 inputs/outputs) are Data bus information. These eight, three-state signals (high, low, or floating) allow bidirectional communication (via the shared bus) between memory and I/O devices for instructions and data transfers. Bit 2^{0} is the least significant. Bus drivers send output data signals to the Data bus. The Microprocessor Input Data Buffers/Drivers receive and supply input data signals to the microprocessor. The microprocessor also uses these eight Data lines to convey status information to the Memory Control (diagram 103) and Communication Line Control register (diagrams 105 and 106). This occurs at the beginning of each machine cycle at Sync time.

+D BIN signal (558C13 output pin 17) specifies that the Data bus information is required in the input mode. This signal active high enables the Microprocessor Input Data Buffers/Drivers and notifies shared bus circuits (via P2-47) of the active input mode.

+Sync signal (558C13 output pin 19) specifies the beginning of each microprocessor machine cycle. This signal is made active high during the first State Time (see +Ø1 and Ø2 signals description preceding). Circuits on diagrams 103, 105, and 106 use the +Sync signal to latch status and set up I/O control. Also, -Sync (via P2-46) notifies shared bus circuits (e.g., memory, I/O, etc.) of the Sync condition of the microprocessor.

+Interrupt Enable (+INTE) signal (558C13 output pin 16, not used) being active high specifies that the microprocessor will accept external Interrupts. This condition automatically resets (inactive low), to disable accepting Interrupts, by either: 1) the active +Processor Reset signal or 2) during the first State Time of the instruction fetch cycle when an Interrupt is accepted. Instructions $E1_{16}$ and $D1_{16}$ (see Instruction Repertoire in Section 2) may be used to set or reset (enable or disable) this signal within the microprocessor control circuits. Shared bus circuits could use this signal (via a shared bus signal line not connected in the circuit application shown by this diagram) to determine if Interrupt processing is available.

+Interrupt (+INT) signal (diagram 106) being active high notifies the microprocessor that an Interrupt Request is being received from a shared bus circuit associated with the processor. The microprocessor will recognize an active +Interrupt signal either: 1) after completing any current instruction or 2) while it is Halted (see Status Definitions in Section 2 for Halt information). If the microprocessor is in Hold state or if +Interrupt Enable (+INTE) is inactive (reset), the interrupt request is ignored (not processed). The microprocessor issues an active INTA (Interrupt Acknowledge via $D2^{0}$) at active Sync time if it accepts the Interrupt request (see Status Definitions in Section 2 for INTA information). If accepted, the next instruction fetch cycle does not advance the microprocessor program counter and a one byte instruction (8 bits), usually Restart ($11\ AAA\ 111_{2}$) can be inserted (see Programming in Section 2).

+Hold signal (via P2-44) being active high notifies the microprocessor that a shared bus circuit requests the processor to enter Hold state. The microproecssor recognizes an active +Hold signal if either of the following conditions are active: 1) Halt state active, or 2) State Time Two (ST2) or State Time Wait (TW) if +Ready input signal to microprocessor is active high. In Hold state, the microprocessor floats the +Address 2^{15} - 2^{0} lines and the +Data 2^{7} - 2^{0} lines. It also acknowledges the state by making +Hold Acknowledge (+HLDA) output signal active high. The microprocessor finishes executing any current machine cycle. When +Hold signal drops to inactive low, operation resumes from the first State Time (ST1) of the next machine cycle. See timing in Section 2 for further information.

+Hold Acknowledge (+HLDA) signal (558C13 output pin 21) being active high specifies that the micrprocessor recognizes a +Hold input and is allowing the Address bus and Data bus to float. +Hold Acknowledge goes active high at either: 1) State Time Three (ST3) for Read Memory or Input or 2) clock period following ST3 for Write Memory or Output. See timing in Section 2 for further information. Shared bus circuits receive +HLDA notification via P2-45 after flip-flop 175D15B sets at the end of -Ø4 to latch the active +HLDA condition.

+Wait signal (558C13 output pin 24, not used) being active high specifies that the microprocessor is in the Wait state (waiting for data from an external module). +Wait goes active high if an active high +CPU Ready signal is not received by Ø2 clock at State Time Two (ST2). See timing in Section 2 for further information. Time Out circuits and shared bus circuits would receive active Wait notification if it were used.

+CPU Ready signal is made active high by a shared bus circuit associated with the processor to indicate to the microprocessor that stable memory or Input data is available or that a Write Memory or Output operation is complete. During a Read Memory operation, +CPU Ready must go active high by Ø2 clock at State Time Two (ST2) or the microprocessor enters Wait state.

-Write signal (558C13 output pin 18, not used) is held active low by the microprocessor for writing to shared bus memory (Write Memory) or for writing to some associated device I/O channel (Write Output). Data Bus information ($+D2^7 - 2^0$) is not changed by the microprocessor while -Write signal is active low. With -Write signal inactive high, the microprocessor will perform Read Memory or Input operations. Shared bus circuits would receive -Write/+Read state notification if it were used.

-5v, +5v, +12v, and ground are operating-voltage levels required on microprocessor pins as shown.

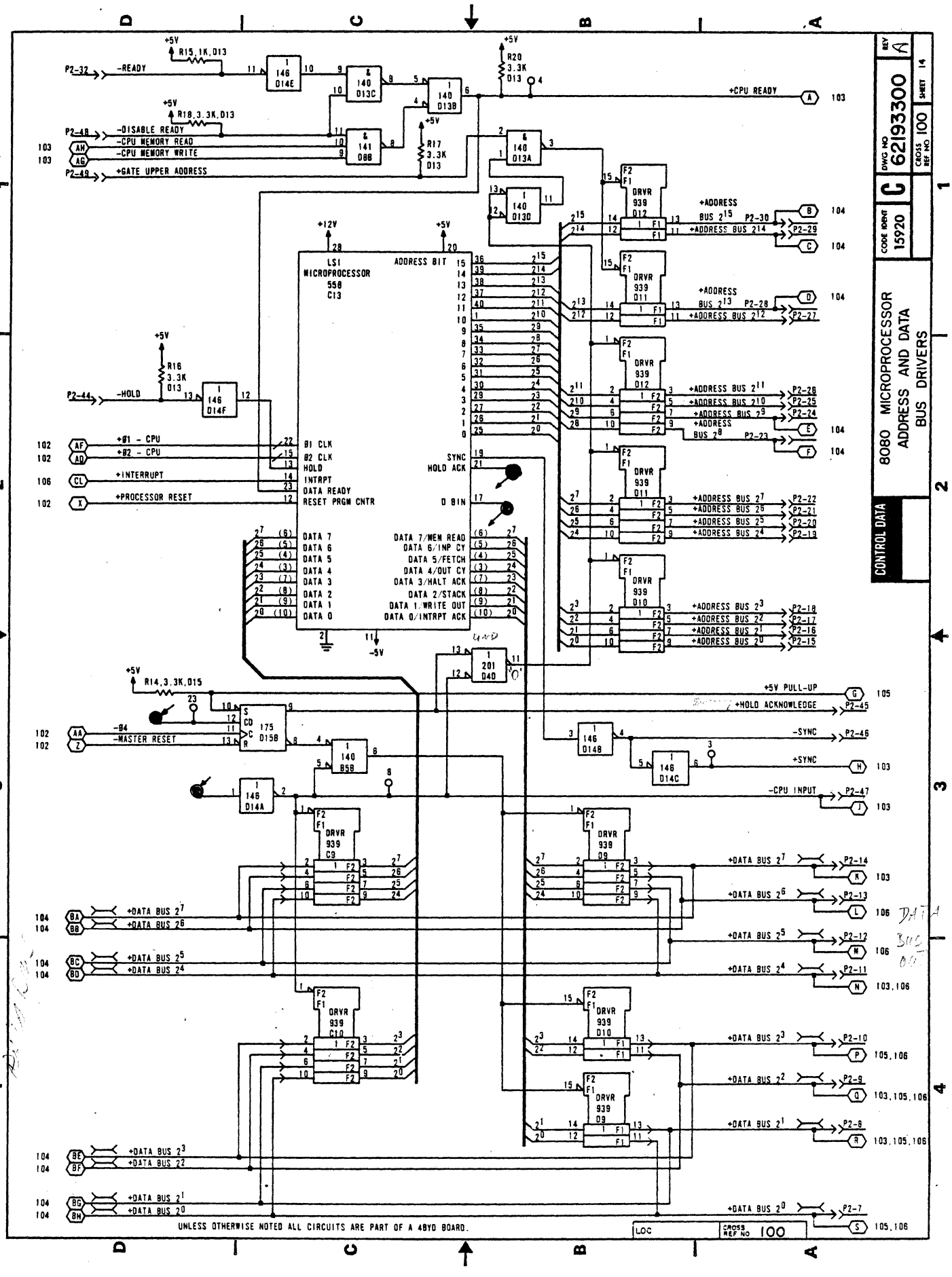

8080 MICROPROCESSOR ADDRESS AND DATA BUS DRIVERS
CONTROL DATA
DWG NO 62193300
REV A
SHEET 14
CROSS REF NO 100
CODE IDENT 15920
LSI MICROPROCESSOR 558 C13
ADDRESS BIT
DRVR 939
-READY
-DISABLE READY
-CPU MEMORY READ
-CPU MEMORY WRITE
+GATE UPPER ADDRESS
-HOLD
+Ø1 - CPU
+Ø2 - CPU
+INTERRUPT
+PROCESSOR RESET
-Ø4
-MASTER RESET
+CPU READY
+5V PULL-UP
+HOLD ACKNOWLEDGE
-SYNC
+SYNC
-CPU INPUT
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48YD BOARD.
LOC
CROSS REF NO 100

DIAGRAM 101
BAUD COUNTER

This circuit comprises a frequency-selectable, communication line, baud rate counter (clock).

FREQUENCY SELECT SWITCHES, SWITCHES MUX, AND PRELOAD MEMORY (S1-1 through S1-8, 189A14, and 768A12) — Four of these eight switches select one of four low frequency rates for the baud counter and four more select one of four high frequency rates. The clock rate selected will be that specified by the low frequency switches (S1-1, S1-3, S1-5, or S1-7) if: 1) the High/300/Low Frequency Switch signal, from an operator panel via P1-21, is logic high on the select input of quad, 2-input multiplexer 189A14 and 2) the same named signal, from an operator panel via P1-32, is logic low. Multiplexer 189A14 will select the clock rate specified by the high frequency group of four switches (S1-2, S1-4, S1-6, and S1-8) if: 1) the High/300/Low Frequency Switch signal on P1-21 is logic low and 2) the same named signal on P1-32 is logic high. Multiplexer 189A14 selects from neither low or high groups of switches when the inputs on P1-21 and P1-32 are both high. In this case, multiplexer 189A14 issues all low (zero) outputs which place an address of 00000 on ROM 768A12. This results in a counter preload value of 1100 0000 which enables 300 baud rate counting (see description following).

The table located in the upper right corner of this diagram defines the switch settings required for each of several, common-use, baud rates for RS-232-C type communication lines.

Note that NAND gate 143A13A recognizes when all four output lines from multiplexer 189A14 are high because all four selected switches are off (open). This occurs only if 110 baud is specified and results in an active -110 Baud signal to select two Stop bits after each character code in UART communications (diagram 106). If -110 Baud signal is inactive high (baud rate selected is faster than 110 baud), only one Stop bit will be used.

Multiplexer 189A14 outputs are a selected address which pick one of 32 8-bit words prestored in ROM 768A12. Actually, only one of ten prestored words is used to obtain a preload count value which allows the counter to cycle so as to produce one of the 10, common-use, switch-selected, baud rates.

3-STAGE COUNTER (158A6, 158A9, 158A10, and 240B4A) — Three 16-count, up-binary counters, cascaded together and feeding a J-K flip-flop, form the actual counting portion of the Baud Counter. Depending on one of the 10 common Frequency Select Switches settings, the 3-stage counter will output a +Communication Clock signal with cycle frequency as follows:

Frequency Select Switches Set For Baud Rate (see table on diagram)	Approximate (±0.2%) +Communication Clock Signal Frequency	Approximate (±0.2%) +Communication Clock Signal Cycle Time
110	1,760 Hz	568 microsec
150	2,400 Hz	417 microsec
200	3,200 Hz	313 microsec
300*	4,800 Hz	208 microsec
600	9,600 Hz	104 microsec
1200	19,200 Hz	52 microsec
1800	28,800 Hz	35 microsec
2400	38,400 Hz	26 microsec
4800	76,800 Hz	13 microsec
9600	153,600 Hz	6.5 microsec

*Or P1-21 and P1-32 both high from external switch.

Note that +Communication Clock signal frequency is 16 times that of the desired baud rate. This is what the UART (diagram 106) requires to receive/transmit at the selected baud rate. Obviously, as the baud rate selected increases in frequency, so must the preload value on the counter stages from memory 768A12. Since the counter increments (counts) once for each highgoing +6.745 MHz Out clock pulse, at the 110 Baud Rate (1,760 Hz clock signal output) the preload value must let the counter increment 3,832 times (3,832 highgoing +6.745 MHz Out clock signals). At the other extreme, at the 9600 Baud Rate (153,600 Hz clock signal output) the counter increments only 44 times for each cycle of +Communication Clock signal. This occurs as 22 counts in the 3 stages for the high half-wave of each cycle and 22 counts again for the low half-wave. Thus, every second time that third stage (158A10) carry output (pin 15) goes high (indicating full count reached), flip-flop 240B4A completes one Baud Counter clock cycle (of duration as specified by the Frequency Select switches which preload the counter via memory 768A12). Memory 768A12 prestored values used to preload the counter stages are as follows:

Baud Rate Selected	Address Input From MUX 189A14 (Binary)	Preload Value Issued From Memory 768A12 (Binary)
110	01111	0101 0010
150	01110	1000 0000
200	01101	1010 0000
300	01100 or 00000*	1100 0000
600	01011	1110 0000
1200	01010	1111 0000
1800	01001	1111 0011
2400	01000	1111 1000
4800	00111	1111 1100
9600	00110	1111 1110

* 00000 address value exists when both High/300/Low Frequency Switch inputs, from an associated 3-position switch, are logic high to select 300 baud.

+6.745 MHz Out signal, arriving on P2-51, is the primary main timing signal for the Baud Counter and for Processor Main Timing. It must be tied to 6.745 MHz Oscillator output pin P2-52 (diagram 102) for normal operation. For test purposes, this signal could be a different frequency in which case all operations would shift in timing accordingly. Note that +6.745 MHz Out inverts to -6.745 MHz In to become the clock pulse for the Processor Main Timing circuits (diagram 102).

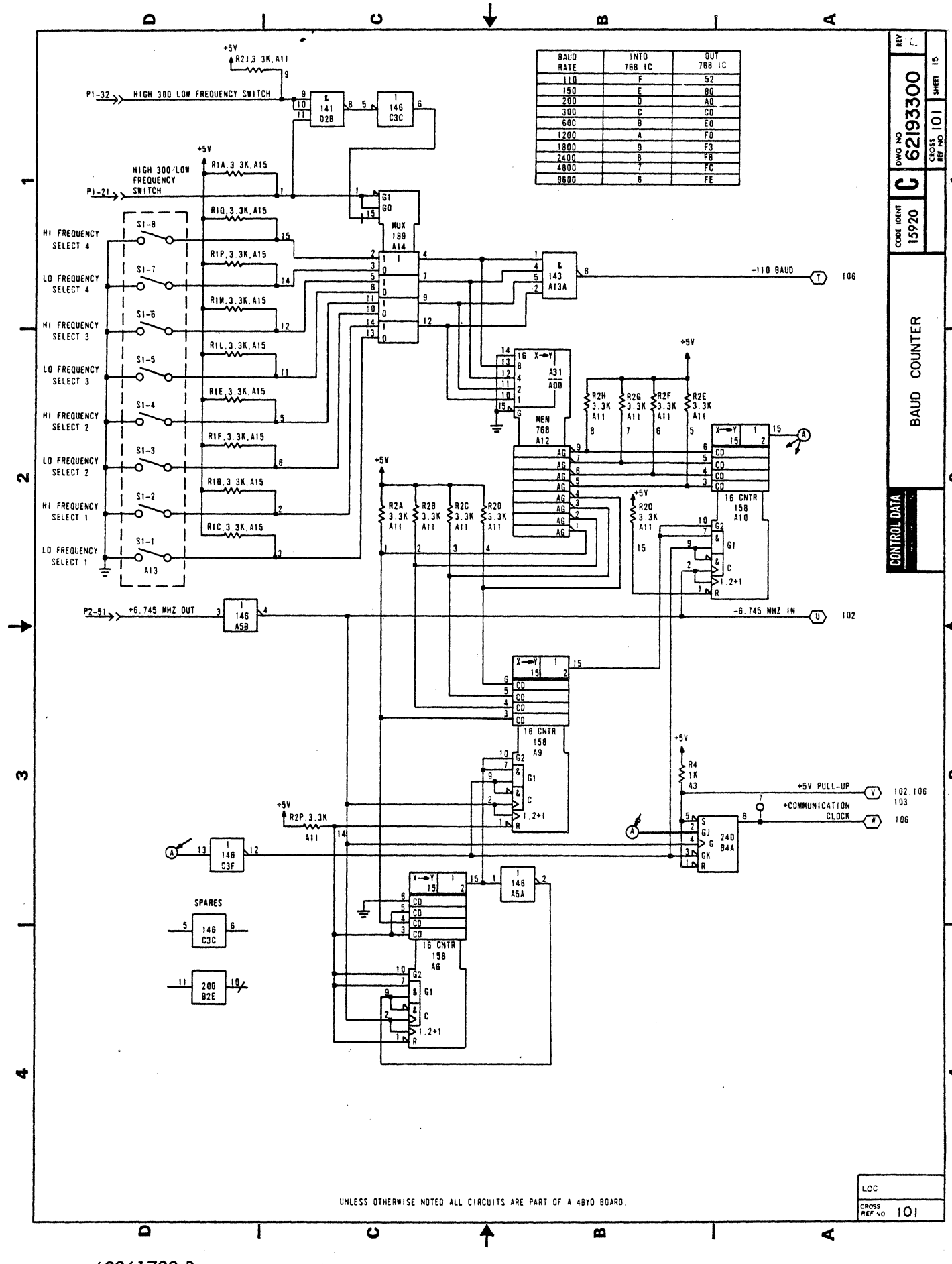

BAUD RATE | INTO 768 IC | OUT 768 IC
110 | F | 52
150 | E | 80
200 | D | A0
300 | C | C0
600 | B | E0
1200 | A | F0
1800 | 9 | F3
2400 | 8 | F8
4800 | 7 | FC
9600 | 6 | FE
HIGH 300 LOW FREQUENCY SWITCH
HIGH 300/LOW FREQUENCY SWITCH
HI FREQUENCY SELECT 4
LO FREQUENCY SELECT 4
HI FREQUENCY SELECT 3
LO FREQUENCY SELECT 3
HI FREQUENCY SELECT 2
LO FREQUENCY SELECT 2
HI FREQUENCY SELECT 1
LO FREQUENCY SELECT 1
+6.745 MHZ OUT
-6.745 MHZ IN
-110 BAUD
+5V PULL-UP
+COMMUNICATION CLOCK
SPARES
MUX 189 A14
MEM 768 A12
16 CNTR 158 A10
16 CNTR 158 A9
16 CNTR 158 A6
DWG NO 62193300
REV C
SHEET 15
CROSS REF NO 101
CODE IDENT 15920
BAUD COUNTER
CONTROL DATA
LOC
CROSS REF NO 101
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48YD BOARD.

DIAGRAM 102
MASTER RESET AND TIMING

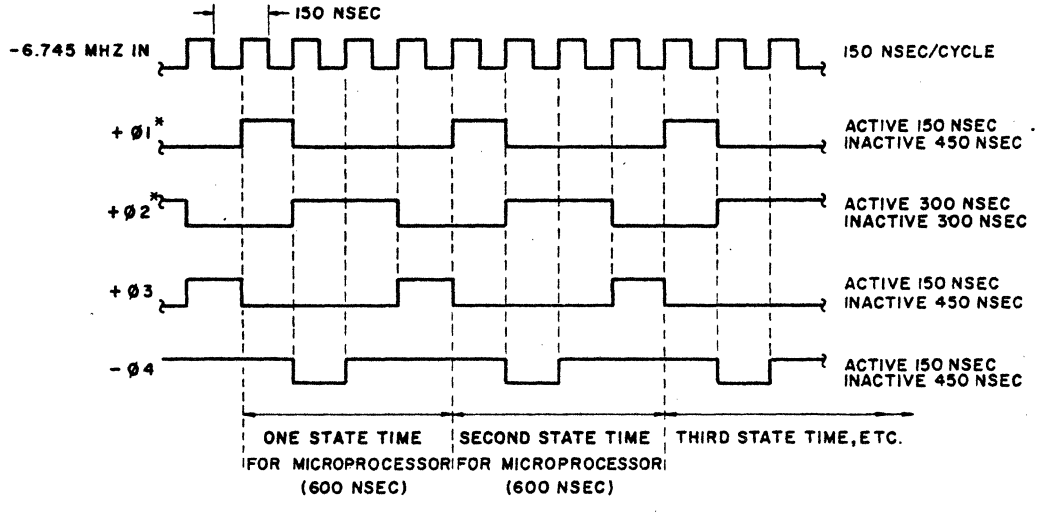
The circuits shown on this diagram perform the Master Reset function and generate the main timing signals required for processor circuits operation.

MASTER RESET CIRCUITS (193A2A, 193A2B, and associated gates) — These circuits initialize processor circuit operations for either: 1) +5v power application or 2) an active Master Reset switch. This occurs as follows. Either +5v power coming up or activated +Master Reset Switch signal lines (P1-29 and P1-30 from the switch) will act via NOR 148A4C on retriggerable, monostable, multivibrator 193A2A. This vibrator then issues an active -Master Reset signal of approximately 310 microseconds duration. This signal being active resets many processor circuits (HLDA flip-flop, Memory Control, 64 Character Buffer, Communication Control Register, Keyboard Character Control, and Universal Asynchronous Receiver/Transmitter shown on diagrams 100, 103, 105, and 106). It also resets the timing chain flip-flops 175A3A and 175A3B (see description below). Via P2-31, the circuits of shared bus cards may be Master Reset at the same time as the processor circuits are. 193A2A pin 13 output triggers multivibrator 193A2B when the Master Reset function is active. This vibrator issues an active high +Processor Reset signal which clears the microprocessor (diagram 100) program counter and sets the microprocessor instruction register to zero. After such a reset, program execution in the microprocessor starts with location zero of the program stored in memory.

6.745 MHz GENERATOR (C15) — This circuit produces the + 6.745-MHz, square-wave, main timing signal which drives all other timing signals in the processor. The + 6.745-MHz Generator output (P2-52) must connect (via mating-connector, backplane wiring) to + 6.745-MHz input (P2-51, diagram 101) to drive the processor circuits at this normal operating rate. For circuit testing, this connection may be removed and a slower clock pulse applied to + 6.745-MHz input (P2-51). The minimum clock frequency allowable is X MHz. A slower clock pulse applied here slows all other processor circuit timing down proportionally.

- 6.745 MHz IN SIGNAL (diagram 101) — This is the approximately 150-nanosecond, square-wave, main timing signal which drives all other processor circuits timing during normal operation. It is the clock for Ø1 through Ø4 main timing signals generated by circuits shown on this diagram. It also is the clock for the Communications Line Baud Counter (diagram 101).

TIMING CHAIN (175A3A, 175A3B, and associated Ø1 through Ø4 output gates) — With main timing signal - 6.745 MHz In (6.745 MHz Generator output via diagram 101) running, these two Timing Chain flip-flops clock at 150-nanosecond intervals to produce Ø1, Ø2, Ø3, and Ø4 timing signals. The constant-cycling chain generates signals as follows:



* INCLUDES NONSTANDARD VOLTAGE LEVELS.
LOW IS -1.0V — +0.6 V AND HIGH IS +10.4V — 13.6 V.

01893

The microprocessor (diagram 100) uses +Ø1 and +Ø2 timing signals for execution timing. Each +Ø1 cycle, with +Ø2 spaced as shown preceding, is one State Time for the microprocessor. A State Time is always a fixed, 600-nanosecond period of execution. Up to five State Times (excluding Wait or Hold time) may be used to complete a particular microprocessor instruction. See diagram 100 description and Microprocessor Functions in Section 4 for execution details.

Besides the microprocessor use of +Ø1 and +Ø2, circuits throughout the processor card and others on the shared bus synchronize their operation from the various Timing Chain signals.

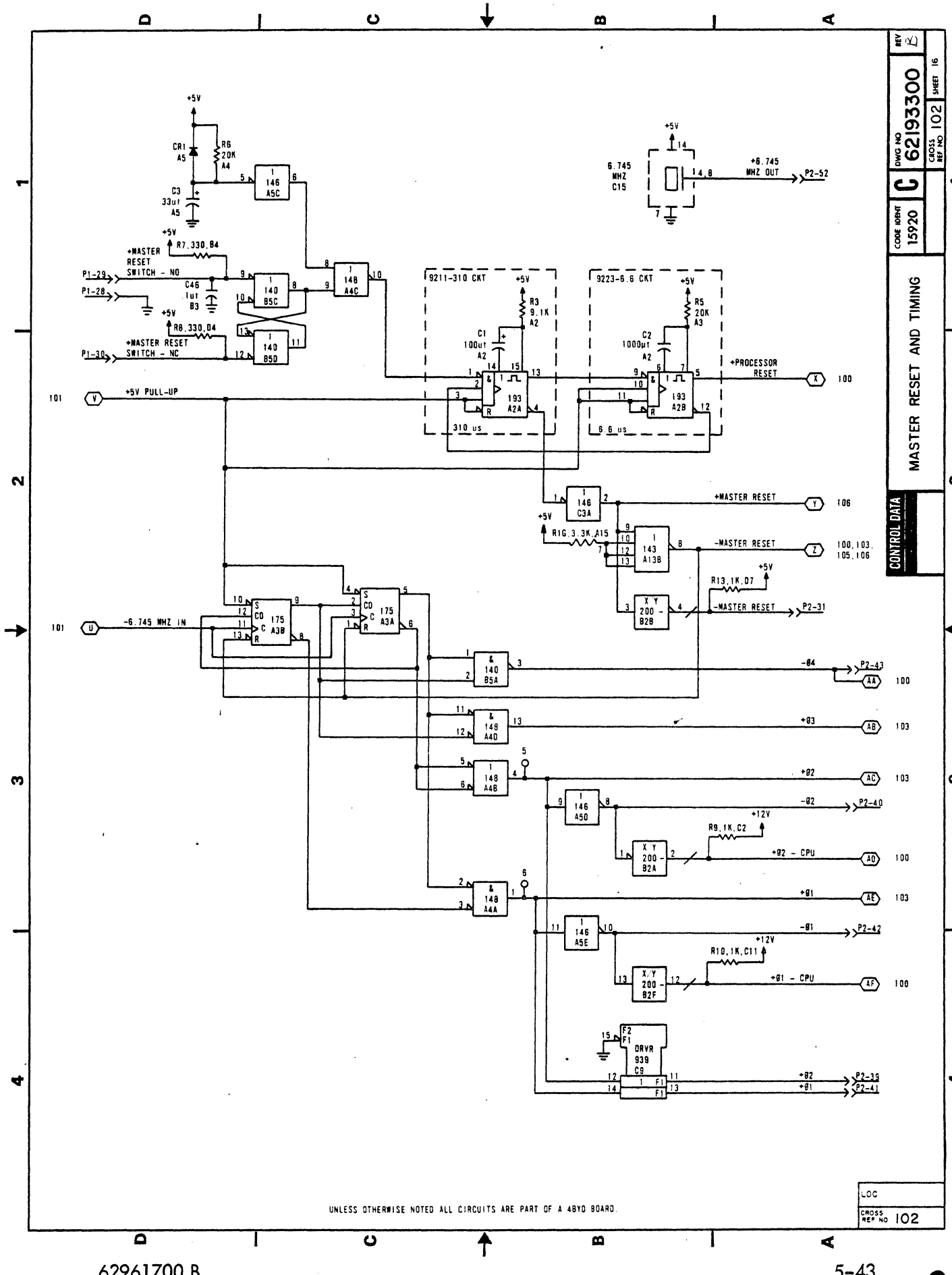

MASTER RESET AND TIMING
CONTROL DATA
DWG NO 62193300
REV E
SHEET 16
CROSS REF NO 102
CODE IDENT 15920
+5V
CR1 A5
R6 20K A4
C3 33uf A5
+MASTER RESET SWITCH - NO
+MASTER RESET SWITCH - NC
P1-29
P1-28
P1-30
R7,330,B4
R8,330,D4
C46 1uf B3
6.745 MHZ C15
+6.745 MHZ OUT
P2-52
9211-310 CKT
9223-6.6 CKT
R3 9.1K A2
R5 20K A3
C1 100uf A2
C2 1000µf A2
+PROCESSOR RESET
310 us
6.6 us
+5V PULL-UP
+MASTER RESET
R1G,3.3K,A15
-MASTER RESET
R13,1K,D7
-6.745 MHZ IN
-Ø4
+Ø3
+Ø2
-Ø2
+12V
R9,1K,C2
+Ø2 - CPU
+Ø1
-Ø1
R10,1K,C11
+Ø1 - CPU
DRVR 939 C9
+Ø2
+Ø1
P2-43
P2-40
P2-42
P2-39
P2-41
P2-31
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48YD BOARD.
LOC
CROSS REF NO 102

DIAGRAM 103
MEMORY CONTROL SIGNALS, -5 VOLT REGULATOR, AND 64 CHARACTER BUFFER

These circuits issue memory control signals, generate a regulated -5 volts for shared bus use, and provide a first-in/first-out buffer for 64 8-bit, receive-data characters.

MEMORY CONTROL CIRCUIT (240B3A, 240B3B, 240B4B, and associated gates) — Depending on certain Data bus contents under various conditions, Memory Read, Memory Write, Input Strobe, or Output Strobe control signals issue from this Memory Control circuit. An active -Master Reset signal (diagram 102) will inactivate (clear) all of these control signals. Following paragraphs define these Memory Control circuits/signals.

-CPU Memory Write signal (240B3A) is active low to write the Data bus word into a RAM on the shared bus at a location specified by the Address bus contents. For CPU Memory Write timing, see Write Timing portion of Timing Diagram shown on sheet 12 of this logic set. This signal will become active at highgoing +Ø2 (diagram 102) when +Sync signal (from microprocessor, diagram 100) is active high if all three of the following conditions are true:

- +CPU Ready signal (diagram 100) inactive low on flip-flop 240B3A input.
- +Data Bus 2^1 signal (diagram 100) at logical low to specify a Write Memory or Output device channel function being executed by the microprocessor.
- +Data Bus 2^4 signal (diagram 100) at logical low to specify that only a Write Memory function is being executed by the microprocessor (if this signal was logical high, it would specify that an Output device channel function, instead of a Memory Write function, was being executed).

At highgoing +Ø2, when +Sync is inactive low and after +CPU Ready has become active high — then, flip-flop 240B3A changes state and -CPU Memory Write signal ends (goes inactive high).

-CPU Memory Read signal (240B4B) is active low to allow the processor to read a word from either RAM or ROM on the shared bus. Such read occurs from the address specified by the Address bus contents. For CPU Memory Read timing, see Read Timing portion of Timing Diagram shown on sheet 12 of this logic set. This signal will become active at highgoing +Ø2 (diagram 102) when +Sync signal (from microprocessor, diagram 100) is active high if either of the two following sets of conditions are true:

- Set A

  +Data Bus 2^1 signal (diagram 100) at logical high to specify a Read Memory or Input device channel function being executed by the microcprocessor.

  +Data Bus 2^2 signal (diagram 100) at logical high to specify that only a Pushdown Stack Read Memory function is being executed by the microprocessor.

- Set B

  +Data Bus 2^7 signal (diagram 100) at logical high to specify that only a normal Read Memory function is being executed by the microprocessor.

At highgoing Ø3, after +CPU Ready has become active high and with -CPU Input signal (diagram 100) inactive high — then, flip-flop 240B4B force-clears and -CPU Memory Read signal ends (goes inactive high).

+Input Strobe signal (148D1D) is active high to allow the processor to perform an Input function which is present on the Address bus and Data bus. This strobe allows the I/O Function Decoder (diagram 104) to recognize the type of Input function present. For Input timing, see Timing Diagram shown on sheet 21 of this logic set. This strobe will be active high if CPU Memory Read flip-flop (240B4B) is not set (output pin 10 low) and -CPU Input signal (diagram 100) is active low.

+Output Strobe/-Output Strobe signals (175A1A) are active to allow the processor to perform an Output function which is present on the Address bus and Data bus. This strobe allows the I/O Function Decode (diagram 104) to recognize the type of Output function present. For Output timing, see Timing Diagram shown on sheet 21 of this logic set. This strobe will become active at highgoing +Ø1 (diagram 102) after Output Operation flip-flop 240B3B output pin 9 has been set high at the preceding highgoing +Ø2 (diagram 102). Flip-flop 240B3B will clock output pin 9 high at +Ø2 when +Sync signal (from microprocessor, diagram 100) is active high if both of the following conditions are true:

- + CPU Ready signal (diagram 100) inactive low on flip-flop 240B3B input.
- + Data Bus 2^4 signal (diagram 100) at logical high to specify that only an Output Write function to a device is being executed by the microprocessor.

At highgoing +Ø2, after + CPU Ready has become active high, flip-flop 240B3B output pin 9 goes low. At the following highgoing +Ø1, Output Strobe flip-flop 175A1A clears and ends the active strobe signals.

-5 VOLT REGULATOR (9226-5P) — This regulator supplies -5 volt power to shared bus pins P2-5 and P2-6 for use by circuits which may be present on the shared bus. The power supplied is -5 volts ±5% with a maximum 75 milliamps.

64-CHARACTER, RECEIVE, DATA BUFFER (3341B10, 3341B11, and associated gates) — This is a 64-character, 8-bits-per-character, first-in/first-out (FIFO) buffer used to asynchronously receive data communications words. It consists of two Fairchild type 334 LSI FIFO chips (or equivalent), each chip having a capacity of 64 4-bit words. To allow the asynchronous receipt of words, this buffer temporarily stores received data words (received and deserialized by the UART shown on diagram 106). See Timing Diagram shown on sheet 22 of this logic set for FIFO timing. The FIFO operates similar to loading a series of balls into a 64-ball-capacity tube with each ball representing one 8-bit Received Data/Parity word.

A ball consisting of +Receive Data 2^6 - 2^0 bits and +Parity Error bit, enters the first FIFO word location only if both +Input Ready (pin 2) and Shift In (pin 3) are active high. +Input Ready output from the FIFO informs the UART (diagram 106) that the first word location in the FIFO is empty and thus available to accept a new word. With +Input Ready thus active, +Receive Data 2^6 - 2^0 and +Parity Error will enter the FIFO first word location if either set of the following conditions are true on the FIFO Input Clock (pin 3) gates:

- -Carrier On, -Data Set Ready, and -Data Terminal Ready signals (diagram 105) all active low (communications lines ready).

AND

- +Block Shift In (FIFO) signal (diagram 106) inactive low (no block shift).

OR

- +Test Mode signal being active high (P1-31 from Test Mode switch via shared bus connector).

AND

- +Frame Error signal (diagram 106) inactive low (no frame error for character received).

AND

- +Communication Line Character Ready signal (diagram 106) active high (serial-to-parallel conversion complete for character received and parallel code of character is ready on the eight + Receive Data 2^6 - 2^0 and + Parity Error lines).

Entering the new 8-bit word in the first FIFO location forces + Input Ready output signal (pin 2) inactive low. The new word stays in the first location until the + Input Clock (pin 3) also drops low. At this time, if the next (second) word location in the FIFO is empty, the new word in the first location propagates to the second location. Upon this transfer of the data from the first location, + Input Ready output signal becomes active high to signify that the FIFO is ready for a new word. If the FIFO is full, (preventing the word from propagating from the first to the second location) then + Input Ready remains inactive low. Once a word is in the second location in the FIFO, subsequent shifts to next empty locations are automatic. Thus, 8-bit data words automatically fall through to the farthest empty word location available. In such manner, the FIFO fills up from the last (64th) word location to the first word location. Each time a word is shifted out (see following paragraph), all words in the FIFO shift down one location leaving space for one new word at the beginning.

When a word loaded in the FIFO automatically propagates to the last location (64th), + Output Ready (pin 14) becomes active high and generates active high + Buffer Character Ready signal. This is a Status input function (see Programming in Section 2), indicating that a word loaded in the buffer has propagated to output position. With + Output Ready active, the FIFO clocks out the 8-bit word from the last location when + Output Clock is high (pin 15, inversion of - Communication Line Data signal, from diagram 104, which specifies the Communication Line Input function). This drops + Output Ready to inactive low and output data remains on the output Data lines until + Output Clock drops low. At this time, if a word is present in the adjacent upstream location (63rd location), it transfers into the last location causing + Output Ready to go active high again. An 8-bit output word from the FIFO becomes Received Data and Parity Error input to the Data Bus Input Function Multiplexer (diagram 104).

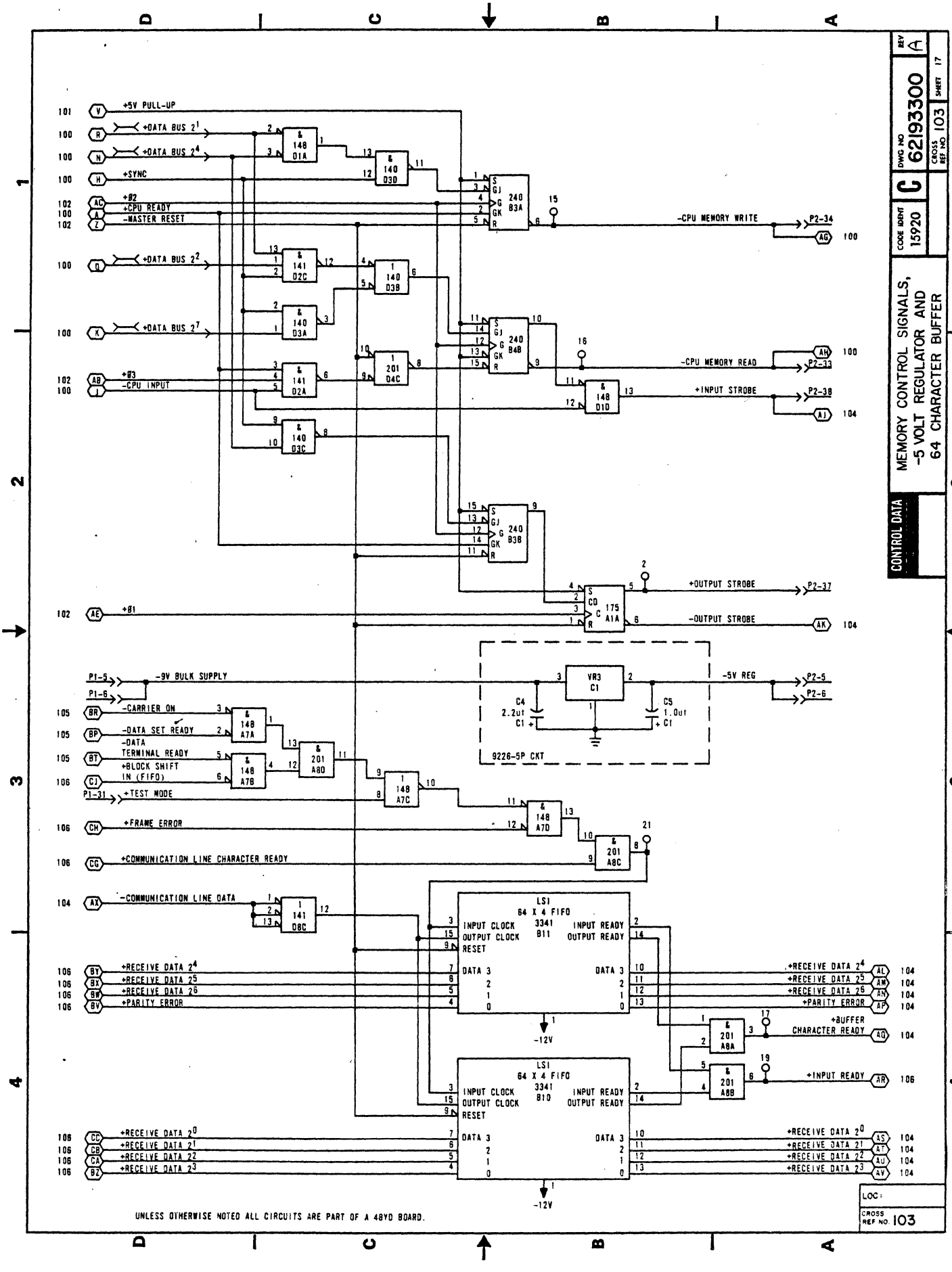

CONTROL DATA
MEMORY CONTROL SIGNALS, -5 VOLT REGULATOR AND 64 CHARACTER BUFFER
CODE IDENT 15920
DWG NO 62193300
REV A
SHEET 17
CROSS REF NO 103
+5V PULL-UP
+DATA BUS 2^1
+DATA BUS 2^4
+SYNC
+Ø2
+CPU READY
-MASTER RESET
+DATA BUS 2^2
+DATA BUS 2^7
+Ø3
-CPU INPUT
-CPU MEMORY WRITE
-CPU MEMORY READ
+INPUT STROBE
+OUTPUT STROBE
-OUTPUT STROBE
+Ø1
-9V BULK SUPPLY
-5V REG
VR3 C1
C4 2.2uf
C5 1.0uf
9226-5P CKT
-CARRIER ON
-DATA SET READY
-DATA TERMINAL READY
+BLOCK SHIFT IN (FIFO)
+TEST MODE
+FRAME ERROR
+COMMUNICATION LINE CHARACTER READY
-COMMUNICATION LINE DATA
LSI 64 X 4 FIFO 3341 B11
LSI 64 X 4 FIFO 3341 B10
INPUT CLOCK
OUTPUT CLOCK
RESET
INPUT READY
OUTPUT READY
DATA 3
DATA 2
DATA 1
DATA 0
-12V
+RECEIVE DATA 2^4
+RECEIVE DATA 2^5
+RECEIVE DATA 2^6
+PARITY ERROR
+BUFFER CHARACTER READY
+INPUT READY
+RECEIVE DATA 2^0
+RECEIVE DATA 2^1
+RECEIVE DATA 2^2
+RECEIVE DATA 2^3
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48YD BOARD.
LOC:
CROSS REF NO 103

DIAGRAM 104
I/O FUNCTION DECODER AND MULTIPLEXER INPUTS TO DATA BUS

This diagram shows the I/O Function Decoder (demultiplexer) and the multiplexer which selects one of four types of data words for input to the shared Data bus.

I/O FUNCTION DECODER (525D7) — This dual, 2-line to 4-line decoder recognizes I/O control functions present on + Address Bus 2^{15}, 2^{14}, 2^{13}, 2^{9}, and 2^{8} lines (diagram 100). + Input Strobe and - Output Strobe signals (diagram 103) specify whether the function is for input to the microprocessor (diagram 100) or if it is output for circuits outside the processor. See Processor I/O Functions in Section 2 for programming information. Functions are recognized (decoded) as follows:

+ Input Strobe Active High	- Output Strobe Active Low	+ Address Bus Bits 2^{15} Through 2^{8}	I/O Function Decoded
Yes	No	111 XXX 00	Input Communication Line Data (clocks a received and assembled word in from FIFO Buffer shown on diagram 103)
Yes	No	111 XXX 10	Input Keyboard Data (clears + Keyboard Character Ready status in circuit shown on diagram 105 after active - Keyboard Ready)
No	Yes	111 XXX 00	Output Data (strobes a character code intended for transmission into the UART shown on diagram 106)
No	Yes	111 XXX 01	Output Communication Line Control (strobes Communication Line Control data, from the microprocessor and via the Data bus, into the Communication Control register shown on diagrams 105 and 106).
No	Yes	111 XXX 10	Output Printer Data (via shared bus pin P2-56, notifies an optional printer circuit on the bus that printer data is on the shared bus).

DATA BUS INPUT FUNCTION MULTIPLEXER (508B6 - 508B9) — This dual, 4-bit, data selector/multiplexer selects information for the Input Function Data bus drivers as specified by one of four possible input functions. + Address Bus 2^{9} and 2^{8} bits (diagram 100) specify the input function which selects information as follows:

Address Bus Bits		Input Information Selected For Data Bus
2^{9}	2^{8}	
Low (0)	Low (0)	Communication Line Receive Data (from FIFO Buffer shown on diagram 103).
Low (0)	High (1)	Status of communication line, printer, and keyboard (+ Transmit Register Empty, + Frame Error Status, + Buffer Character Ready, + Hold Register Empty, - Printer Buffer 3/4 Full, + Printer Ready, + Keyboard Character Ready all from various processor control circuits, plus + Printer Character Request from a printer via shared bus pin P2-53).
High (1)	Low (0)	Keyboard Data (+ Keyboard Data 2^{7} - 2^{0} bits, from associated keyboard, via P1-42 through P1-49 respectively).
High (1)	High (1)	Communication Line Control Status (-Data Set Ready, -Carrier On, -Clear To Send, -Ring Indicator, Highlight Present, -Request To Send, -Secondary Carrier On, and Paging Present conditions as determined by circuits shown on diagram 105).

INPUT FUNCTION DATA BUS DRIVERS (939C7 and 939C8) — These TTL circuits (National, type DM 8097, tri-state buffers, or equivalent) transmit the signal present on their input (Input function information from MUX 508B6 through 508B9 outputs) only while their enable input (pin 1) is active low. This occurs when + Input Strobe signal (diagram 103) is active high and while + Address Bus 2^{15} - 2^{13} signal lines (diagram 100) = 111_2. The drivers place their information on the shared Data bus (diagram 100).

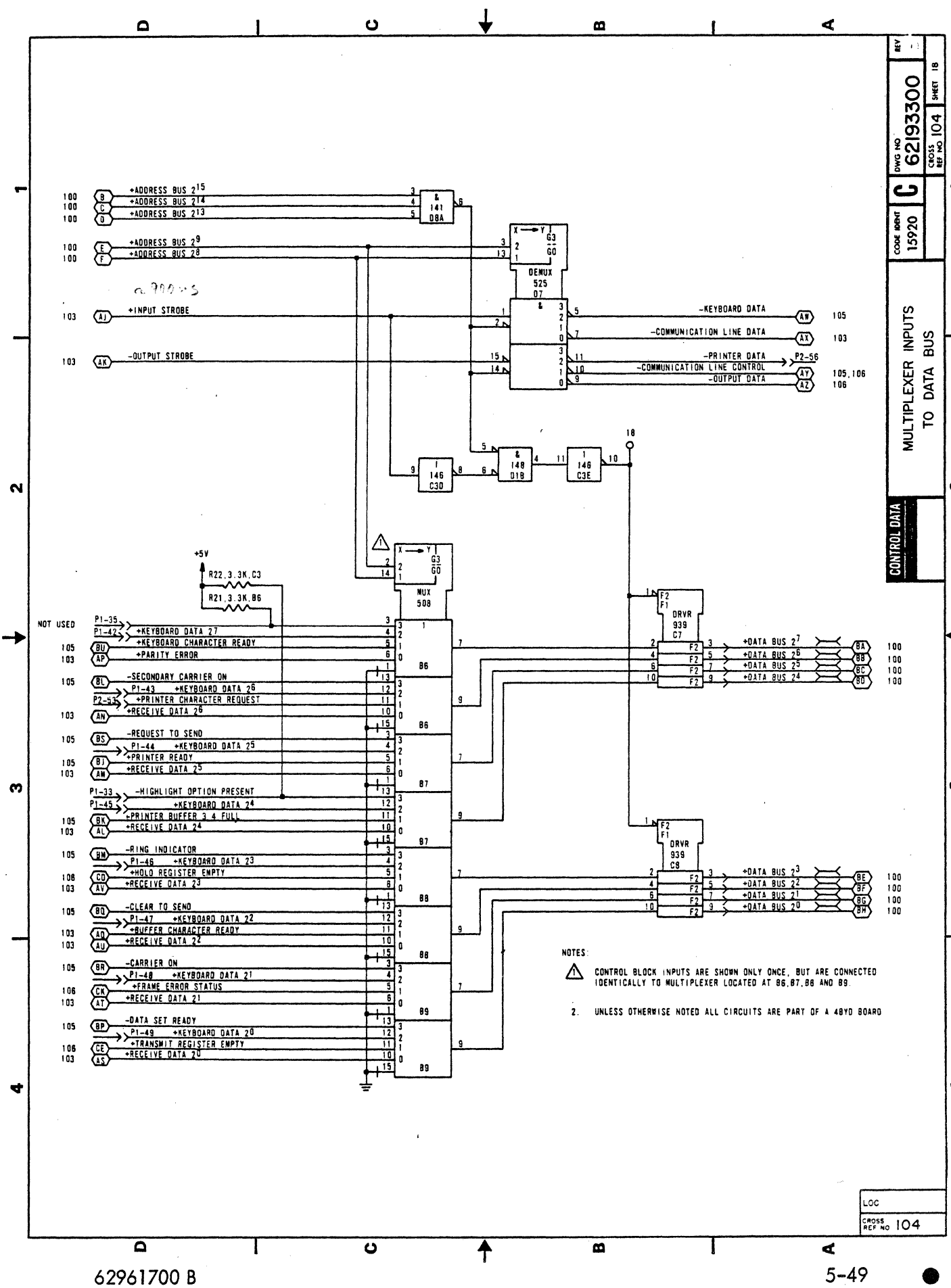

MULTIPLEXER INPUTS TO DATA BUS
CONTROL DATA
DWG NO 62193300
CODE IDENT 15920
SHEET 18
REV
+ADDRESS BUS 2^15
+ADDRESS BUS 2^14
+ADDRESS BUS 2^13
+ADDRESS BUS 2^9
+ADDRESS BUS 2^8
+INPUT STROBE
-OUTPUT STROBE
DEMUX 525 D7
-KEYBOARD DATA
-COMMUNICATION LINE DATA
-PRINTER DATA
-COMMUNICATION LINE CONTROL
-OUTPUT DATA
+5V
R22, 3.3K, C3
R21, 3.3K, B6
MUX 508
NOT USED
+KEYBOARD DATA 2^7
+KEYBOARD CHARACTER READY
+PARITY ERROR
-SECONDARY CARRIER ON
+KEYBOARD DATA 2^6
+PRINTER CHARACTER REQUEST
+RECEIVE DATA 2^6
-REQUEST TO SEND
+KEYBOARD DATA 2^5
+PRINTER READY
+RECEIVE DATA 2^5
-HIGHLIGHT OPTION PRESENT
+KEYBOARD DATA 2^4
+PRINTER BUFFER 3 4 FULL
+RECEIVE DATA 2^4
-RING INDICATOR
+KEYBOARD DATA 2^3
+HOLD REGISTER EMPTY
+RECEIVE DATA 2^3
-CLEAR TO SEND
+KEYBOARD DATA 2^2
+BUFFER CHARACTER READY
+RECEIVE DATA 2^2
-CARRIER ON
+KEYBOARD DATA 2^1
+FRAME ERROR STATUS
+RECEIVE DATA 2^1
-DATA SET READY
+KEYBOARD DATA 2^0
+TRANSMIT REGISTER EMPTY
+RECEIVE DATA 2^0
DRVR 939 C7
DRVR 939 C8
+DATA BUS 2^7
+DATA BUS 2^6
+DATA BUS 2^5
+DATA BUS 2^4
+DATA BUS 2^3
+DATA BUS 2^2
+DATA BUS 2^1
+DATA BUS 2^0
NOTES:
1. CONTROL BLOCK INPUTS ARE SHOWN ONLY ONCE, BUT ARE CONNECTED IDENTICALLY TO MULTIPLEXER LOCATED AT 86,87,88 AND 89.
2. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48YD BOARD
LOC
CROSS REF NO 104

DIAGRAM 105
RS232 SIGNALS

Mainly, the circuits shown on this diagram receive and issue RS-232-C type interface signals. Following paragraphs identify and define these signals. See Processor I/O Functions in Section 2 for programming information.

RS-232-C INPUTS (902C5 and 902D5) — Two, RS-232-C to DTL/TTL, quad, line receivers constantly monitor eight RS-232-C input interface signal lines for status and serial data. The lines monitored and their use are as follows:

Input Signal	Use
+ Printer Buffer 3/4 Full	Status input to MUX on diagram 104
+ Printer Ready	Status input to MUX on diagram 104
+ Secondary Received Line Signal Detector (Secondary Carrier On)	Communication Line Control Status input to MUX on diagram 104
+ Ring Indicator	Communication Line Control Status input to MUX on diagram 104
- Received Data (Receive Serial Data)	Serial, input data stream to UART on diagram 106. Also to LED driver to provide an operator's panel indication of actively receiving data. High-to-low initiates data receive.
+ Data Set Ready	Communication Line Control Status input to MUX on diagram 104. Also input to FIFO Input Clock (diagram 103). In addition, to LED driver enable input (pin 15) to allow an operator's panel indication for Clear To Send and/or Carrier On.
+ Clear To Send	Communication Line Control Status input to MUX on diagram 104. Also to LED driver to provide an operator's panel indication of lines being clear for sending (transmitting)
+ Received Line Signal Detector (Carrier On)	Communication Line Control Status input to MUX on diagram 104. Also to LED driver to provide an operator's panel indication of lines having the required carrier signal.

LED DRIVERS (939C7 and 939C8) — These TTL circuits (National, type DM8097 tri-state buffers, or equivalent) transmit the signal present on their input only while their enable input (pin 15) is active low. When active high, a driver output illuminates a connected LED on an operator's panel. 939C7 has a constant-enable low tied to pin 15 so it will always pass an active + Transmit Serial Data signal and/or an active + Receive Data signal. 939C8 will issue an active + Carrier On signal and/or an active + Clear To Send signal only when a Data Set Ready active condition holds input pin 15 low.

RS-232-C OUTPUTS (900D6) — One DTL/TTL to RS-232-C, quad, line driver constantly issues four RS-232-C output interface signal lines. The signals issued are as follows:

Processor Internal Signal	RS-232-C Output Issued
+ Data Bus 2^0 (from microprocessor and stored in Communication Line Control register)	+ Data Terminal Ready
+ Data Bus 2^1 (from microprocessor and stored in Communication Line Control register)	+ Request To Send
+ Data Bus 2^3 (from microprocessor and stored in Communication Line Control register)	+ Secondary Request To Send
+ Data Bus 2^2 (from microprocessor and stored in Communication Line Control register) or + Transmit Serial Data (from UART on diagram 106)	+ Transmitted Data

COMMUNICATION LINE CONTROL REGISTER (520C6 this diagram and 520C4 on diagram 106) — The two quad, D-type, edge-triggered flip-flops which form this register, load with the contents of + Data Bus 2^5 - 2^0 lines from the microprocessor (diagram 100) when - Communication Line Control signal (diagram 104) pulses low to high. This occurs for the active Communication Line Control function at microprocessor sync time (at this time, the microprocessor issues I/O control on + Data Bus 2^5 - 2^0 lines). The signals stored and issued by the Communication Line Control register and their uses are as follows:

Signal Stored/Issued	Use
+ Data Bus 2^0	+ Data Terminal Ready output to RS-232-C interface because an Interrupt Acknowledge function is specified by bit 2^0 being high. Also, an enable for FIFO Input Clock (diagram 103). In addition, to LED driver to provide an operator's panel indication of the terminal being ready.
+ Data Bus 2^1	+ Request To Send output to RS-232-C interface because a Write Output function is specified by bit 2^1 being high. Also, a Communication Line Control Status input to MUX on diagram 104. In addition, to LED driver to produce an operator's panel indication of the terminal requesting to send.
+ Data Bus 2^2	+ Transmitted Data output to RS-232-C interface because a Stack function is specified by bit 2^2 being high.
+ Data Bus 2^3	+ Secondary Request To Send output to RS-232-C interface because a Halt Acknowledge function is specified by bit 2^3 being high.
+ Data Bus 2^4 (diagram 106)	+ Block Shift In for an enable for FIFO Input Clock (diagram 103) because an Output Device function is specified by bit 2^4 being high.
+ Data Bus 2^5 (diagram 106)	+ Clear Frame Error Status because a Fetch function is specified by bit 2^5 being high.

KEYBOARD CHARACTER READY CIRCUIT (175D15A) — When an associated keyboard has an input character, the highgoing - Keyboard Ready strobe signal (from the keyboard via P1-50) generates the active high + Keyboard Character Ready signal which is a Status input to the MUX shown on diagram 104. If - Keyboard Data signal (an Input function decoded by circuits on diagram 104) is active low, active + Keyboard Character Ready signal from flip-flop 175D15A is cleared since active - Keyboard Data signal means that the character specified as being available for input (by + Keyboard Character Ready signal) is being received as input + Keyboard Data 2^7 - 2^0 bits via the MUX shown on diagram 104. It requires another strobe of - Keyboard Ready signal from the keyboard to set the flip-flop, to indicate another character available from the keyboard.

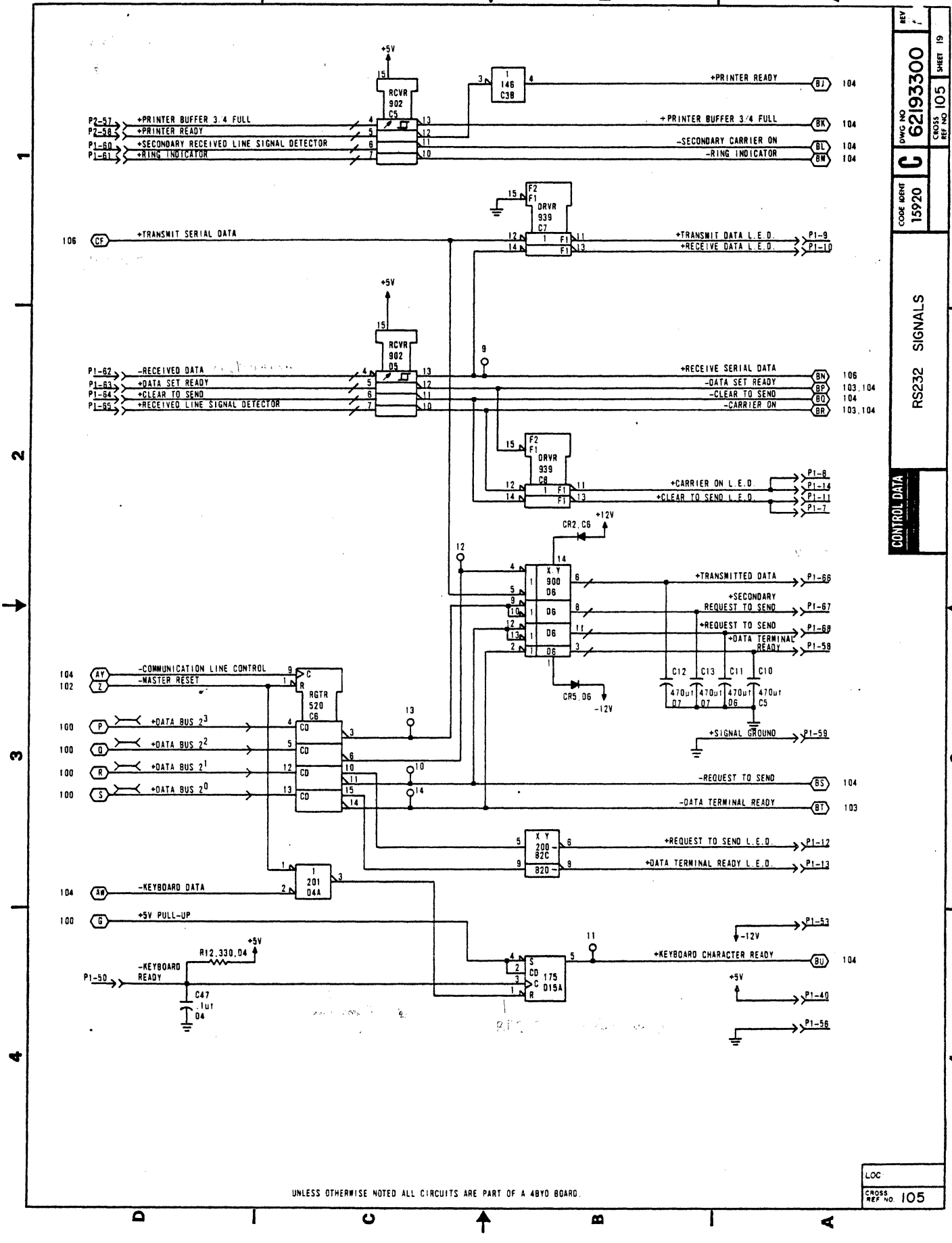

RS232 SIGNALS
CONTROL DATA
DWG NO 62193300
CODE IDENT 15920
SHEET 19
CROSS REF NO. 105
+PRINTER READY
+PRINTER BUFFER 3/4 FULL
-SECONDARY CARRIER ON
-RING INDICATOR
+TRANSMIT SERIAL DATA
+TRANSMIT DATA L.E.D.
+RECEIVE DATA L.E.D.
-RECEIVED DATA
+RECEIVE SERIAL DATA
-DATA SET READY
-CLEAR TO SEND
-CARRIER ON
+CARRIER ON L.E.D.
+CLEAR TO SEND L.E.D.
+TRANSMITTED DATA
+SECONDARY REQUEST TO SEND
+REQUEST TO SEND
+DATA TERMINAL READY
+SIGNAL GROUND
-COMMUNICATION LINE CONTROL
-MASTER RESET
+DATA BUS 2^3
+DATA BUS 2^2
+DATA BUS 2^1
+DATA BUS 2^0
-REQUEST TO SEND
-DATA TERMINAL READY
+REQUEST TO SEND L.E.D.
+DATA TERMINAL READY L.E.D.
-KEYBOARD DATA
+5V PULL-UP
-KEYBOARD READY
+KEYBOARD CHARACTER READY
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48Y0 BOARD.
LOC
CROSS REF NO. 105

DIAGRAM 106
UART, COMMUNICATION CONTROL REGISTER, AND EXTERNAL INTERRUPT

The top half of this diagram shows the Universal Asynchronous Receiver/Transmitter (UART). The remainder shows half of the Communication Control Register (the other half appears on diagram 105) and the -External Interrupt signal which may be received via P2-50 of the shared bus from some interrupt-requesting circuit.

UART (941B13) — This TTL-compatible LSI circuit will simultaneously receive and transmit asynchronous data. In general, it deserializes data received from the RS-232-C Modem Receivers (+Receive Serial Data signal from diagram 105) and serializes data for transmission via the RS-232-C Modem Drivers (+Transmit Serial Data signal to diagram 105). The UART assemblies received serial data into a 7-bit, parallel data word with an eighth parity bit, and issues the 8-bit result to the FIFO Buffer (diagram 103) for temporary storage until the Input Data Multiplexer (diagram 104) can use the word. The UART disassemblies transmit data from its 7-bit form (+Data Bus 2^6 through +Data Bus 2^0 from diagram 100) into serial RS-232-C form and issues these serial bits to the RS-232-C driver (diagram 105). Following paragraphs define each UART I/O signal line shown on this diagram.

+5V, -12V, AND GROUND (pins 1, 2, and 3) are required power and signal ground.

-Receive Data Gate Enable input (pin 4) is tied low to constantly allow Receive Data $2^6 - 2^0$ outputs.

+Receive Data $2^6 - 2^0$ outputs (pins 6 - 12) carry the assembled parallel word (character) received via the +Receive Serial Data line (pin 20). A parallel received word passes to the FIFO Buffer (diagram 103) for temporary storage.

+Parity Error output (pin 13) is at high level if a received character's parity bit does not agree with the switch-selected parity.

+Frame Error output (pin 14) is at high level if a received character's serial code stream does not end with a valid stop bit.

-Receiver Status Gate Enable input (pin 16) is tied low to constantly allow status outputs: Parity Error, Frame Error, Buffer Full, and Transmitter Hold Register (Buffer) Empty.

+Communication Clock input signal (diagram 101), to Receiver Clock pin 17 and Transmitter Clock pin 40, is a square-wave clock signal whose frequency is 16 times the desired receive and transmit baud rate. The Baud Counter (diagram 101) supplies the correct rate as selected by switches, and the diagram 101 description defines the frequency selected for each allowable baud rate.

+Input Ready input signal (diagram 103), to Buffer Reset Data pin 18, being at low level resets Buffer Full output pin 19 to low level.

+Communication Line Character Ready output (Buffer Full pin 19) is at high level when an entire character has been received and assembled as a parallel data bit code.

+Receive Serial Data input signal (diagram 105), to pin 20, is the serial-bit input data stream. A high-to-low transition on this line initiates data receive.

+Master Reset input signal (diagram 102), to pin 21, pulsed to a high sets outputs: Transmit Serial Data, Shift Register Empty, and Hold Register Empty to a high level. Active high +Master Reset also resets outputs: Buffer Full, Parity Error, and Frame Error to a low level.

+Hold Register Empty output (pin 22) is at high level when the transmit hold register (buffer) is ready for a new character to serialize out.

-Output Data input signal (diagram 104), to Transmitter Data Load pin 23, is low level to strobe +Data Bus $2^6 - 2^0$ character data into the transmit hold register (buffer).

+Transmit Register Empty output (Shift Register Empty pin 24) is at high level after a full character is transmitted serially. It remains high until the start of transmission of the next character or for one-half of a Transmitter Clock period in the case of continuous transmission.

+Transmit Serial Data output (pin 25) issues the serial bits for character transmission. It is at high level when no data is transmitting.

+Data Bus 2^6 - 2^0 input signals (diagram 100), to Transmitter Data 7 - 1 pins 32-26, is the parallel-bit output (transmit) character word. -Output Data signal (diagram 104) strobes these seven bits into the transmit hold register (buffer).

+Transmitter Data 8 input (pin 33) is dependent on the Mark Parity switch (S1-9). Furthermore, the Even/No/Odd parity select input (P1-7) must be high. The P1-7 input arrives from a switch located on an associated operator panel. With the Mark Parity switch open, the input is high indicating mark parity. With the switch closed, the input is low indicating space parity.

+Control Register Load input (pin 34) is tied high to constantly allow entering control bits in an internal holding register. The control bits allowed are: Word Length 1, Word Length 2, Stop Bit Select, Odd/Even Parity Bit, and Parity Bit Inhibit.

+Inhibit Parity input (pin 35) is dependent on the +Inhibit Parity input signal (P1-14). The P1-14 input arrives from a switch located on an associated operator panel. When this input is high, it prevents parity bit transmission or receipt (Stop bit immediately follows the last Serial Data bit and +Parity Error output is held low). With the externally-located switch closed, the input is low allowing parity operation according to input pin 39 condition.

-110 Baud input signal (diagram 101), to +Stop Bit Select pin 36, selects the number of Stop bits at the end of a serially-transmitted character. Active low -110 Baud signal places a high on this input and selects two Stop bits. -110 Baud signal being inactive high places a low on this input and selects one Stop bit.

+Word Length Bits 2 and 1 inputs (pins 37 and 38 respectively) select the number of data bits per character as follows:

Pin 37 Bit 2	Pin 38 Bit 1	Data Bits Per Character
Tied High	Low (via Enable Parity switch closed)	7
Tied High	High (via Enable Parity switch open)	8

+Even/No/Odd input (pin 39) selects odd or even parity mode for both receiving and transmitting. This input is dependent on an externally-located switch. The input being high specifies even parity and a low input odd parity. However, if the +Inhibit Parity signal is high on input pin 35, parity is ignored (not transmitted and not received). In such case, the +Mark/-Space switch (UART input pin 33) determines the signal level of the bit transmitted in the parity bit position.

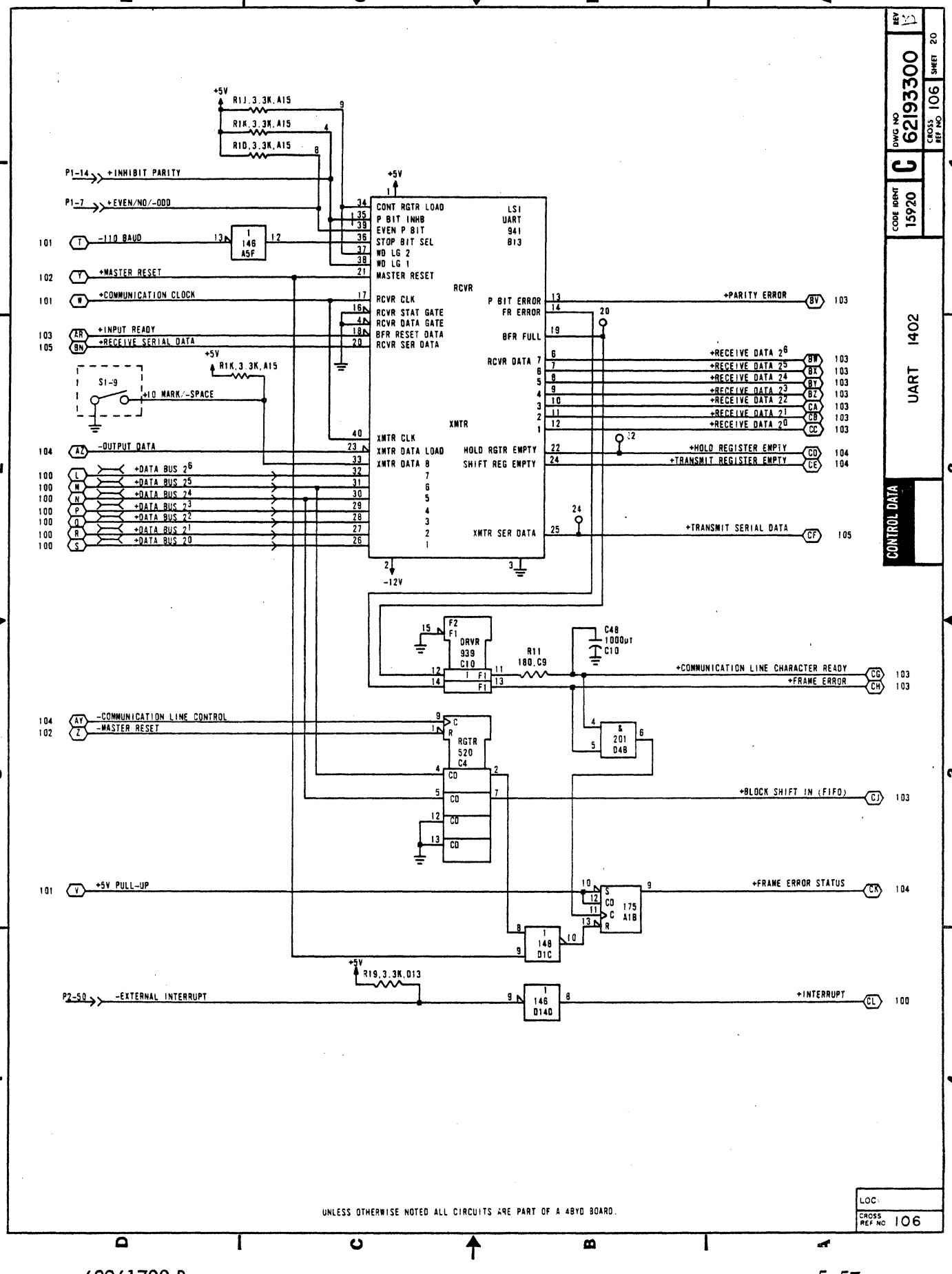
NOTE

P1-7 should arrive from an external, 3-position switch. Such switch positions should be EVEN/NO/ODD. In both EVEN and NO positions, this input must be high. However, in the NO position, the 3-position switch must make the +Inhibit Parity input (P1-14) high also to allow transmitting either a mark or space in the parity bit position.

COMMUNICATIONS CONTROL REGISTER (520C4) — This quad, D-type, edge-triggered flip-flop forms half of the Communications Control register (the other half appears on diagram 105). See diagram 105 description for definition of functions for both halves of the register.

FRAME ERROR STATUS CONTROL (175A1B) — This circuit issues an active +Frame Error Status signal for input to the Data Bus Input Multiplexer (diagram 104) if +Frame Error output is active high from the UART after an entire received character is assembled in the UART internal buffer register (+Communication Line Character Ready signal active high). Either: 1) +Data Bus 2^5 from diagram 100 and stored in the Communication Control register or 2) +Master Reset from diagram 102 will force - clear the +Frame Error Status signal to inactive low.

-EXTERNAL INTERRUPT signal (P2-50) is active low if a circuit on the shared bus wishes to interrupt processor operations and gain control of the bus.


CONTROL DATA
UART 1402
CODE IDENT 15920
DWG NO 62193300
REV C
SHEET 20
CROSS REF NO 106
LSI UART 941 B13
CONT RGTR LOAD
P BIT INHB
EVEN P BIT
STOP BIT SEL
WD LG 2
WD LG 1
MASTER RESET
RCVR
RCVR CLK
RCVR STAT GATE
RCVR DATA GATE
BFR RESET DATA
RCVR SER DATA
P BIT ERROR
FR ERROR
BFR FULL
RCVR DATA 7
XMTR
XMTR CLK
XMTR DATA LOAD
XMTR DATA 8
HOLD RGTR EMPTY
SHIFT REG EMPTY
XMTR SER DATA
+5V
-12V
R11,3.3K,A15
R1K,3.3K,A15
R1D,3.3K,A15
R19,3.3K,D13
P1-14 +INHIBIT PARITY
P1-7 +EVEN/NO/-ODD
-110 BAUD
+MASTER RESET
+COMMUNICATION CLOCK
+INPUT READY
+RECEIVE SERIAL DATA
S1-9
+10 MARK/-SPACE
-OUTPUT DATA
+DATA BUS 2^6
+DATA BUS 2^5
+DATA BUS 2^4
+DATA BUS 2^3
+DATA BUS 2^2
+DATA BUS 2^1
+DATA BUS 2^0
+PARITY ERROR
+RECEIVE DATA 2^6
+RECEIVE DATA 2^5
+RECEIVE DATA 2^4
+RECEIVE DATA 2^3
+RECEIVE DATA 2^2
+RECEIVE DATA 2^1
+RECEIVE DATA 2^0
+HOLD REGISTER EMPTY
+TRANSMIT REGISTER EMPTY
+TRANSMIT SERIAL DATA
C48 1000pf C10
R11 180,C9
DRVR 939 C10
+COMMUNICATION LINE CHARACTER READY
+FRAME ERROR
-COMMUNICATION LINE CONTROL
-MASTER RESET
RGTR 520 C4
+BLOCK SHIFT IN (FIFO)
+5V PULL-UP
+FRAME ERROR STATUS
P2-50 -EXTERNAL INTERRUPT
+INTERRUPT
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 4BYD BOARD.
LOC:
CROSS REF NO 106

TIMING DIAGRAM
I/O TIMING
PROCESSOR

This diagram contains waveforms which define the major timing characteristics of processor I/O operations.

+Ø1 and +Ø2 signals, of duration and spacing as shown here, govern the microprocessor (diagram 100) execution timing. Each Ø1 cycle is one Microprocessor State Time (see State Time definitions in Sections 2 and 4). Circuits shown on diagram 102 generate +Ø1 and +Ø2.

+Address Bus and +Data Bus outputs from the microprocessor (diagram 100) are loaded by the microprocessor and the information is stable in relation to Ø1 and Ø2 as shown on this timing diagram.

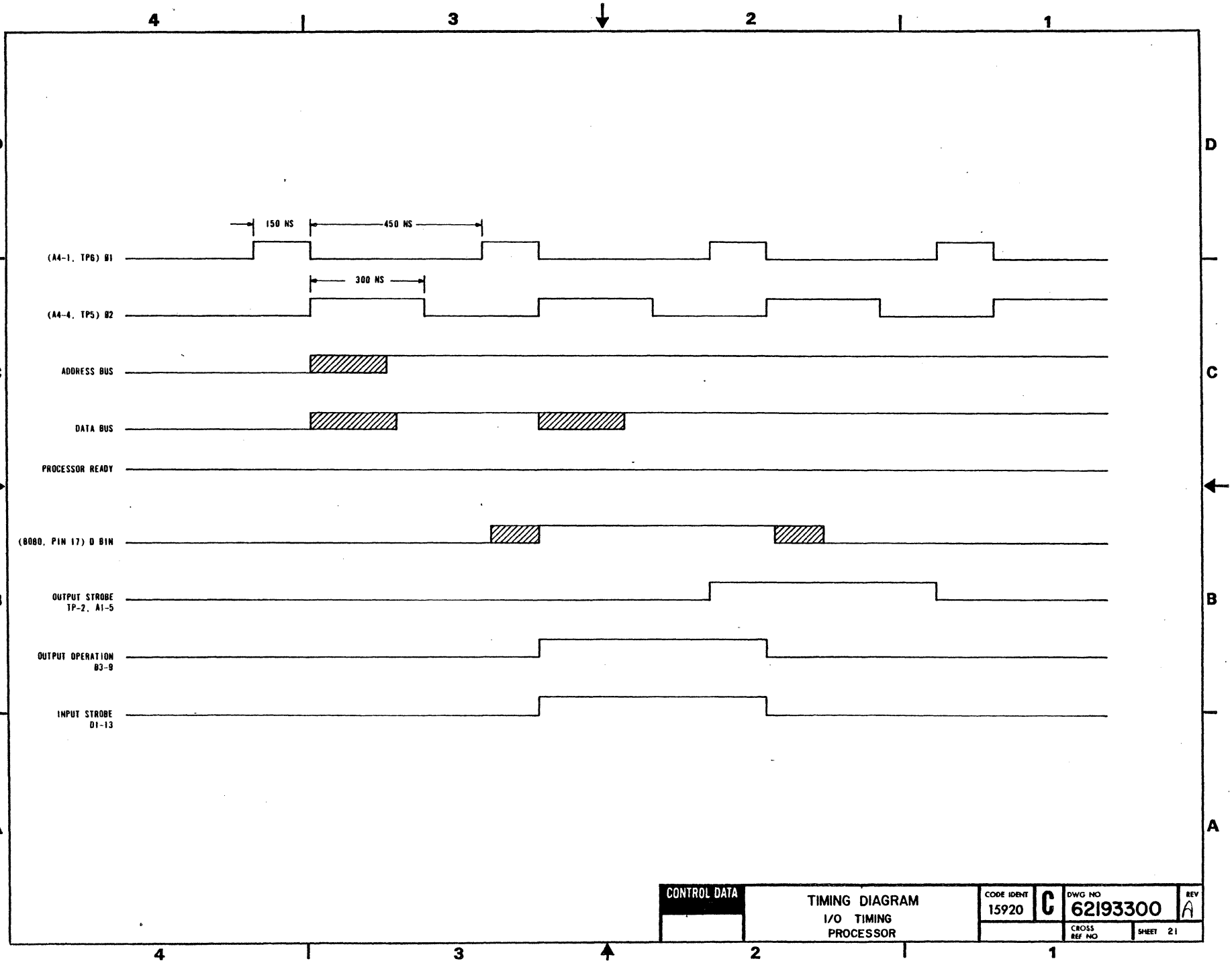
+Processor Ready signal (diagram 100) is assumed constantly active for a processor I/O operation.

+D BIN signal issues from the microprocessor (diagram 100), for the time shown here, if an input operation is being executed by the microprocessor.

+Input Strobe signal is issued by I/O Strobe Control circuits (shown on diagram 103) at the first highgoing +Ø2 +D BIN becomes active.

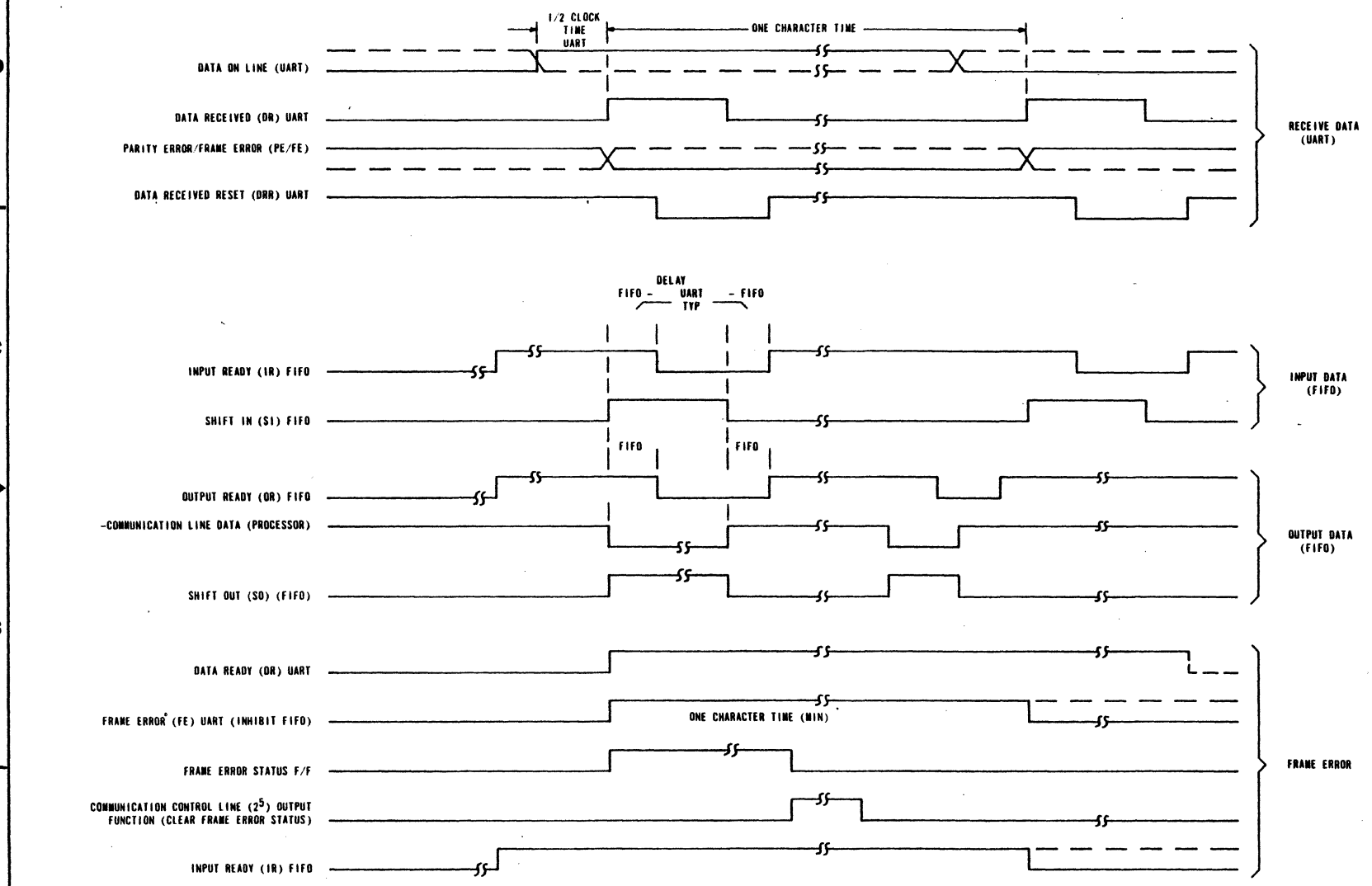
+Output Operation signal will become active high at highgoing +Ø2 and at active +Sync time (+Sync not shown, see diagram 103) if Microprocessor Data 2^4 output is high specifying an output.

+Output Strobe signal becomes active high at the first highgoing +Ø1 after +Output Operation becomes active (see diagram 103).


4
3
2
1
D
C
B
A
150 NS
450 NS
300 NS
(A4-1, TP6) Ø1
(A4-4, TP5) Ø2
ADDRESS BUS
DATA BUS
PROCESSOR READY
(8080, PIN 17) D BIN
OUTPUT STROBE
TP-2, A1-5
OUTPUT OPERATION
B3-9
INPUT STROBE
D1-13
CONTROL DATA
TIMING DIAGRAM
I/O TIMING
PROCESSOR
CODE IDENT
15920
C
DWG NO
62193300
REV
A
CROSS
REF NO
SHEET 21

TIMING DIAGRAM
UART/FIFO RECEIVE DATA
PROCESSOR

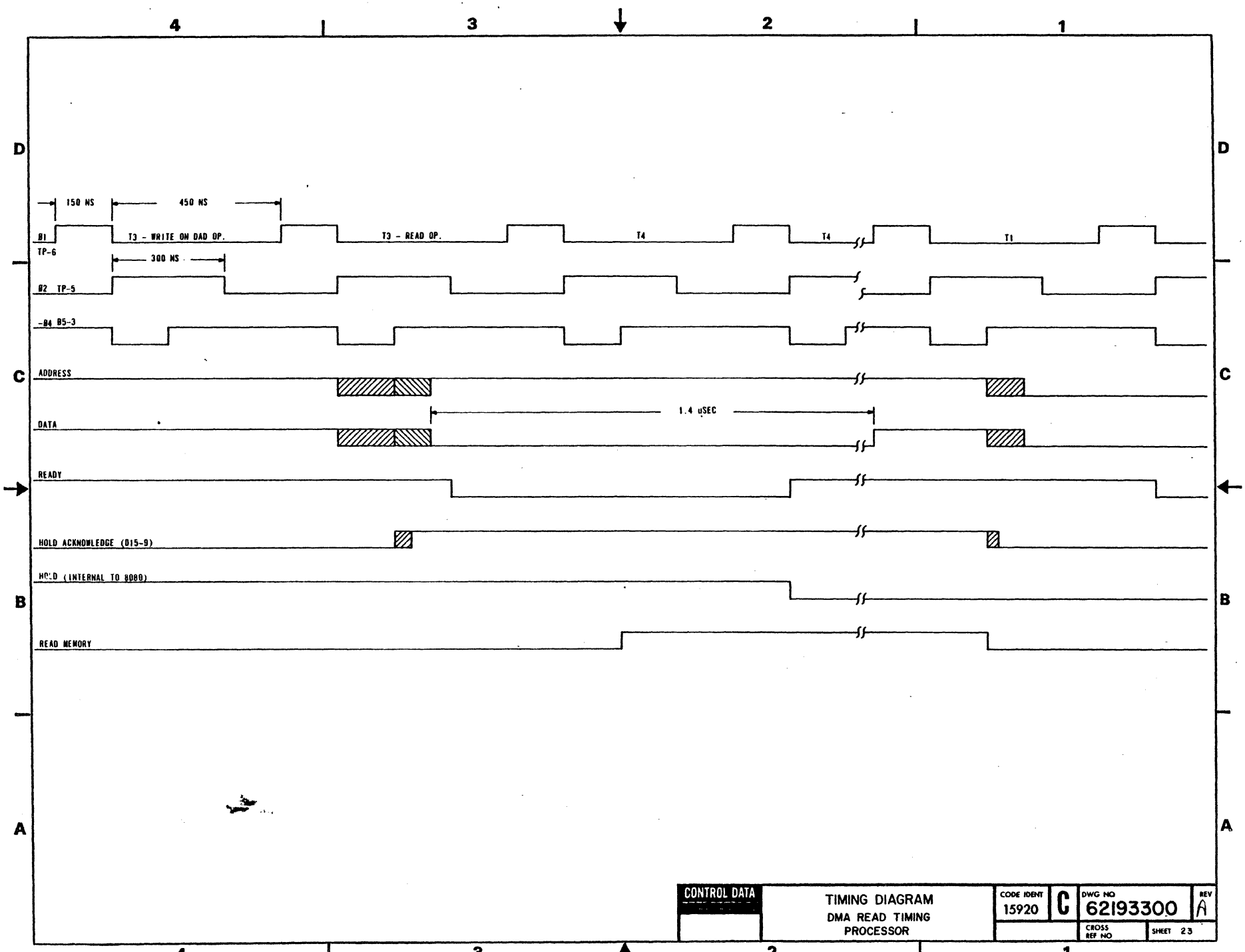
The waveforms shown on this diagram show the major timing characteristics of the following UART/FIFO Receive Data operations in the processor circuits: 1) Receive Data (UART), 2) Input Data (FIFO), 3) Output Data (FIFO), and 4) Frame Error.



CONTROL DATA	TIMING DIAGRAM UART/FIFO RECEIVE DATA PROCESSOR	CODE IDENT 15920	C	DWG NO 62193300	REV A
				CROSS REF NO	SHEET 22

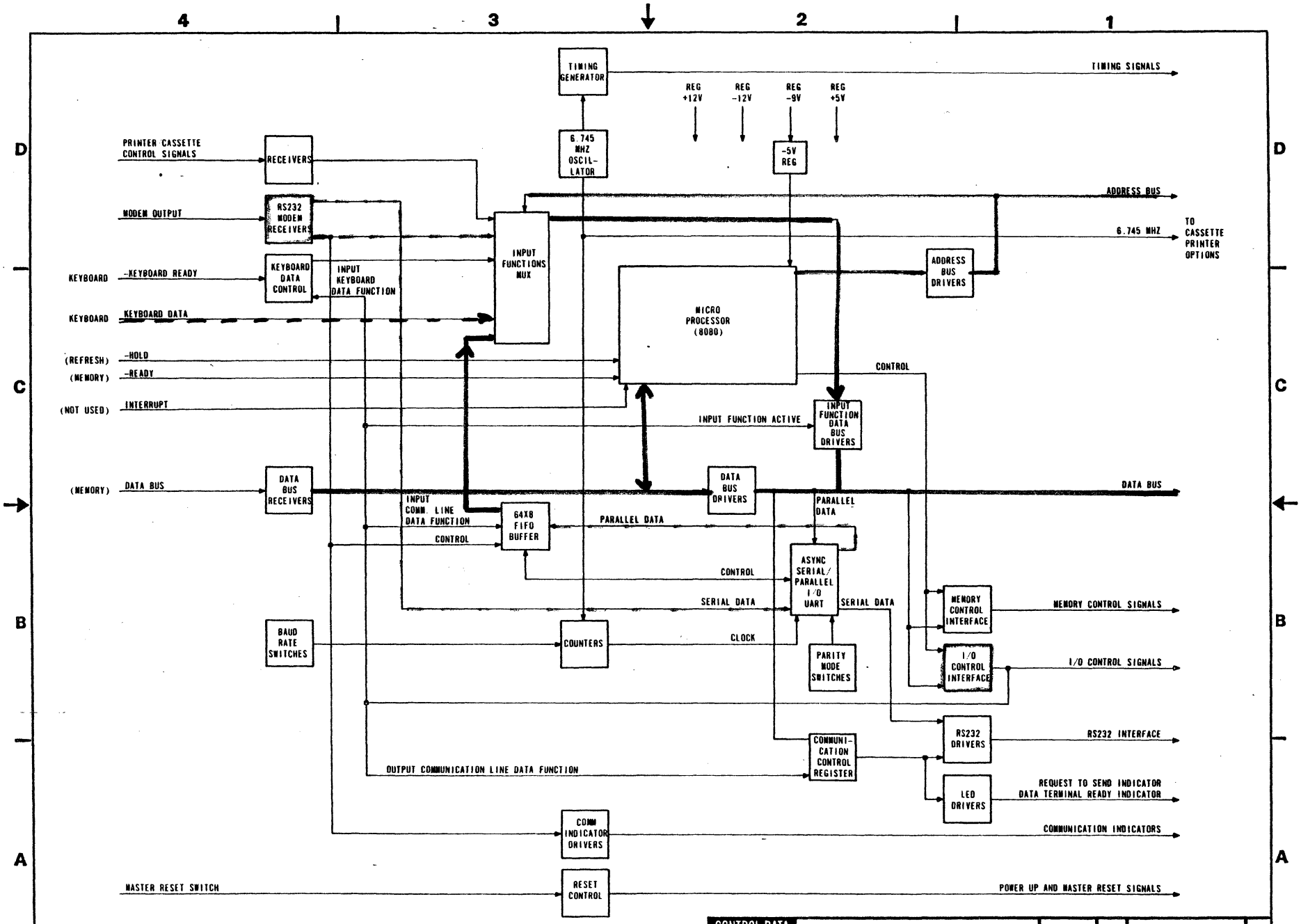
TIMING DIAGRAM
DMA READ TIMING
PROCESSOR

These waveforms illustrate the major timing characteristics of the DMA Read operation in the processor circuits.


150 NS
450 NS
Ø1
T3 - WRITE ON DAD OP.
T3 - READ OP.
T4
T4
T1
TP-6
300 NS
Ø2 TP-5
-Ø4 B5-3
ADDRESS
1.4 uSEC
DATA
READY
HOLD ACKNOWLEDGE (D15-9)
HOLD (INTERNAL TO 8080)
READ MEMORY
CONTROL DATA
TIMING DIAGRAM
DMA READ TIMING
PROCESSOR
CODE IDENT
15920
C
DWG NO
62193300
REV
A
CROSS REF NO
SHEET 23

BLOCK DIAGRAM
PROCESSOR

This is a block diagram of the processor card detailed logic circuits shown on the preceding pages of this logic diagram set. It identifies the major functional circuits of the processor card. The diagram also serves as a functional flow summary. All of the functional circuits and signals identified on this diagram appear in a functional diagram figure in Section 4 where processor theory of operation is described. Since thorough descriptions and references to the detailed logic circuits in Section 5 accompany the figure in Section 4, further description here would be duplication and is therefore omitted.



CONTROL DATA	BLOCK DIAGRAM PROCESSOR	CODE IDENT 15920	C	DWG NO 62193300	REV A
				CROSS REF NO	SHEET 24

REFRESH CONTROL CARD LOGIC DIAGRAMS

Following pages contain the logic circuit diagrams for the refresh control card used in the basic logic module.

DIAGRAM 200
LINE LOCK CIRCUIT AND DOT COUNTER

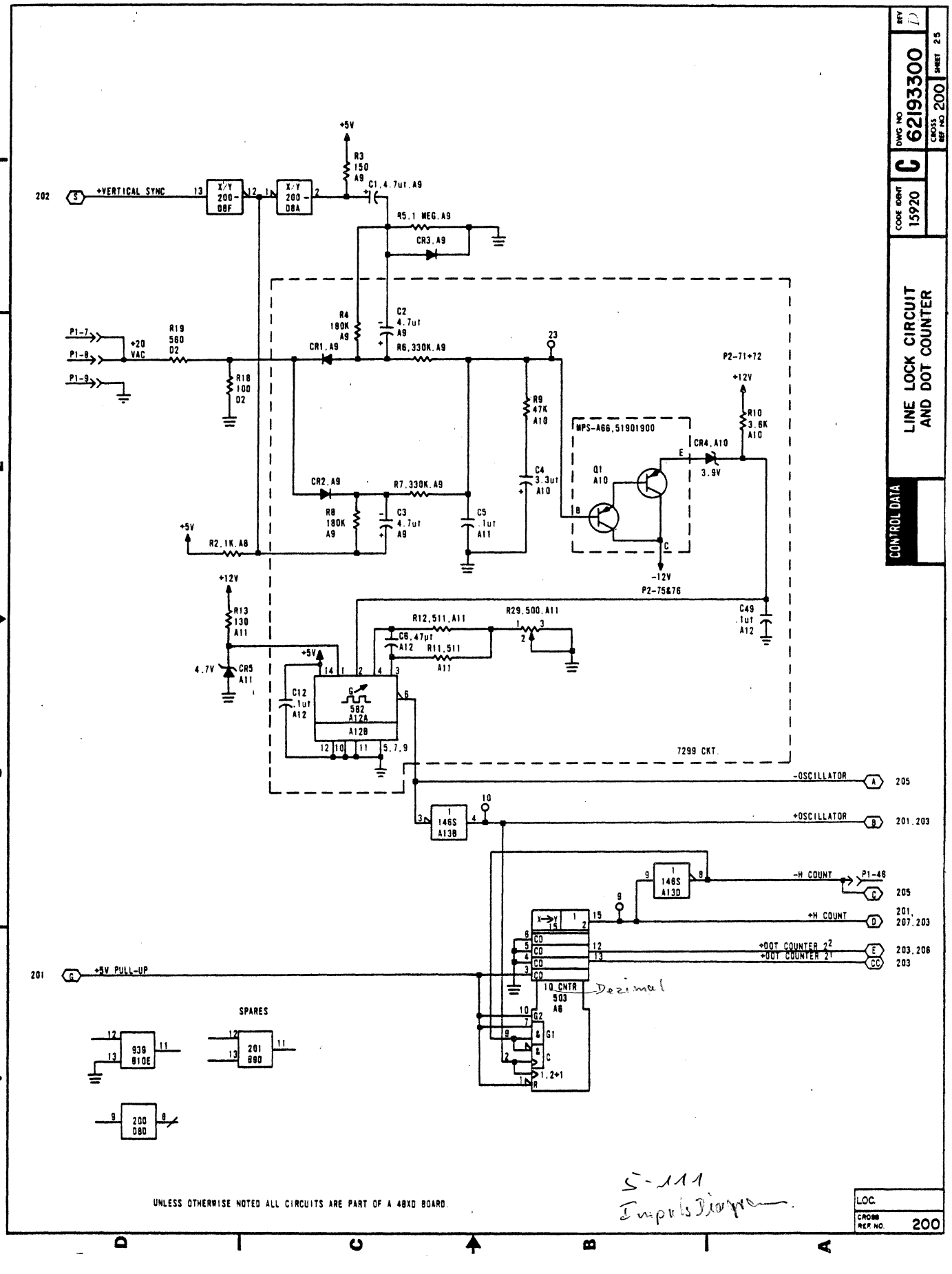
The circuits shown on this diagram comprise an input-power-line-frequency, lock-on circuit and a character-cell, horizontal-dot counter.

LINE LOCK CIRCUIT (7299 and associated components) — This compensating oscillator circuit issues an -Oscillator signal which governs the speed of refresh circuit operations. It monitors the frequency of the input power to the refresh circuits (P1-7 and P1-8) and issues a high-speed -Oscillator output signal (582A12A, pin 6) synchronized within the input power frequency. +Vertical Sync signal (diagram 202), which occurs once before each screen refresh operation, is the feedback input to the Line Lock circuit. If +Vertical Sync frequency decreases (screen refresh time increases), the Line Lock circuit increases the frequency of its -Oscillator output to speed up the refresh operation. If +Vertical Sync frequency increases (screen refresh time decreases), the Line Lock circuit decreases the frequency of its -Oscillator output to slow down the refresh operation. -Oscillator output signal clocks the Dot Counter and is an enable for the Horizontal Counter (diagram 201) and Video Generator circuits (diagrams 203 and 205). Potentiometer R29 at A11 adjusts the circuit to stabilize on frequency.

DOT COUNTER (503A6) — This counter specifies the horizontal scan line position within the nine display dot positions available across a character cell. The 4-bit, up-decade counter increments once for each cycle of the +Oscillator output from the Line Lock circuit. This counter increments once every 68.51 nanoseconds (see Timing Diagram, Dot Counter Timing, Refresh, at back of this logic set). Each count in the Dot Counter represents one of the nine dots used in a scan line across a character cell. Counter carry output preloads the counter to a count of 1, therefore the counter continuously cycles from 1 to 9 so it matches the nine dot times in a scan across a character cell. Dot Counter cycle time (period of +H Count output) = 9 x 68.51 nanoseconds = 616.59 nanoseconds. This is the horizontal scan line time across a character. +H Count output clocks the Horizontal Counter (diagram 201) and is an enable for the Video Generator circuits (diagrams 203 and 205), and Memory Address Register Control (diagram 207). In addition, +H Count issues to the shared bus (via P1-46) to synchronize optional edit card operations. +Dot Counter 2^1 and 2^2 outputs governs Refresh Read Clock timing (diagram 203). Output 2^2 also acts as a clear enable for the memoryAddress Register (diagram 206).

NOTE

When adjusting potentiometer R29 (Phase Lock adjustment), tie test point 23 to signal ground level. This blocks the Line Lock input to the Phase Lock circuit and allows quick, accurate, Phase Lock synchronization.



S-111
Impulse Diagram

DIAGRAM 201
HORIZONTAL COUNTER

These circuits keep track of the horizontal beam position during each scan line operation. Beam position is counted in units of character cell time (a character cell time is the duration required for the beam to move, on one scan line, across one 9-dot-wide character cell). Each scan line operation, counted/controlled by these Horizontal Counter circuits, consists of four sequential segments as follows:

- Display time (otherwise termed horizontal unblank time when the beam moves across one scan line of the 80 character cells where display may occur on the crt screen).
- Front porch time (3-character scan line time allowed after the 80th displayable character position).
- Horizontal sync time (2-character scan line time, following front porch time, allowed for beam retrace to left side of crt screen).
- Back porch time (17-character scan line time, following horizontal sync time, allowed for beam settling and for loading displayable character codes from refresh memory).

Following paragraphs describe circuit operation for the four segments of a scan line. Refer to Timing Diagram, Horizontal Timing, Refresh at the back of this logic set for waveforms which illustrate these four segments.

When +Oscillator and +H Count signals are toggling (see diagram 200), the Horizontal Counter constantly cycles through its four sequential-count segments to track the horizontal beam position which is constantly scanning the crt screen. To start each of the four segments, the counter automatically preloads to a unique value which determines the number of H Counts in that segment's count time. Each segment's preload value is fixed by Horizontal Counter preload control flip-flops 175A1A and 175A1B and associated translation gates (top half of this diagram). Flip-flops 175A1A and 175A1B change condition for each of the sequential count segments. Their condition preloads segment starting-count values in the two counter stages (503A7 and 158A8) as follows:

Preload Control Flip-Flops		H Counter Segment Active	Preload Value Clocked Into H Counter (By Highgoing +Oscillator Signal)
175A1A	175A1B		
*Clear (Out pin 5 = L)	*Clear (Out pin 9 = L)	Unblank (80 counts)	$1111\ 0111_2$ (loads at end of 80 H Counts to set counter for front porch segment counting)
Set (Out pin 5 = H)	Clear (Out pin 9 = L)	Front Porch (3 counts)	$1111\ 1000_2$ (loads at end of 3 H Counts to set counter for sync segment counting)
Set (Out pin 5 = H)	Set (Out pin 9 = H)	Sync (2 counts)	$1110\ 0001_2$ (loads at end of 2 H Counts to set counter for back porch segment counting)
Clear (Out pin 5 = L)	Set (Out pin 9 = H)	Back Porch (17 counts)	$1000\ 0000_2$ (loads at end of 17 H Counts to set counter for unblank segment counting)
*Clear etc.	*Clear etc.	Unblank etc.	$1111\ 0111_2$ etc.

* 175A1A and 175A1B condition after an active low reset input (+GR Tester Only input signal via P1-12).

NOTE: Total H Counter cycle = 102 H Counts = 62.9 µsec.

+Oscillator signal (diagram 200) cycles once every 68.51 nsec. This is the beam time at one dot within one scan line within one character cell.

+H Count signal (diagram 200) cycles once every 616.59 nsec. This is the time required for the beam to scan across one scan line of one character cell (one character cell scan line width = nine dot times).

+Horizontal Unblank signal (NAND 148B6B) being active high enables the 80-character time unblank segment.

-Horizontal Front Porch signal (NAND 140A2D) being active low enables the 3-character time front porch segment.

-Horizontal Sync signal (NAND 140A2C) being active low enables the 2-character-time sync segment.

+Horizontal Back Porch signal (NAND 201A5C) being active high enables the 17-character time back porch segment.

+Refresh Enable signal (FF 140B5D/140B5C) is exactly 80 character counts long (49.3 μsec.). It goes active high at the 17th back porch count (when 16-counter 158A8 reaches 1111_2 count) when +Horizontal Back Porch signal is still active. +Refresh Enable remains active until cleared by carry output from 16-counter 158A8 at the end of the 80-character time unblank count. +Refresh Enable activates Line Buffer Control circuits (diagram 203).

-Disable Refresh signal (NOR 148D5B) goes active low when either: 1) -Vertical Unblank (diagram 202) is inactive high or 2) at the 80th unblank H Count (when 16-counter 158A8 reaches 1111_2 count) when +Horizontal Unblank signal is still active. -Disable Refresh remains active until cleared by the 17th count during back porch segment to allow refresh during the following 80-character unblank segment. -Disable Refresh acts on DMA Channel Control circuits (diagram 207).

+H Column 10 signal (10-counter 503A7 carry output) goes active high for each 10 +H Counts kept track of. This is the enable which allows 16-counter 158A8 to count once for each group of 10 +H Counts (one for each 10 character cell scan line times). +H Column 10 signal also enables Memory Address Register Control circuits (diagram 207).

+Horizontal Count 2^3 signal (10-counter 503A7) goes active high whenever the 10-counter reaches or loads with an H Count of $1XXX_2$. This signal is an enable for DMA Channel Control circuits (diagram 207).

+GR Tester Only signal (P1-12 input) is available for clearing circuits to a known state when special testing is in process (using a General Radio test unit, or equivalent).

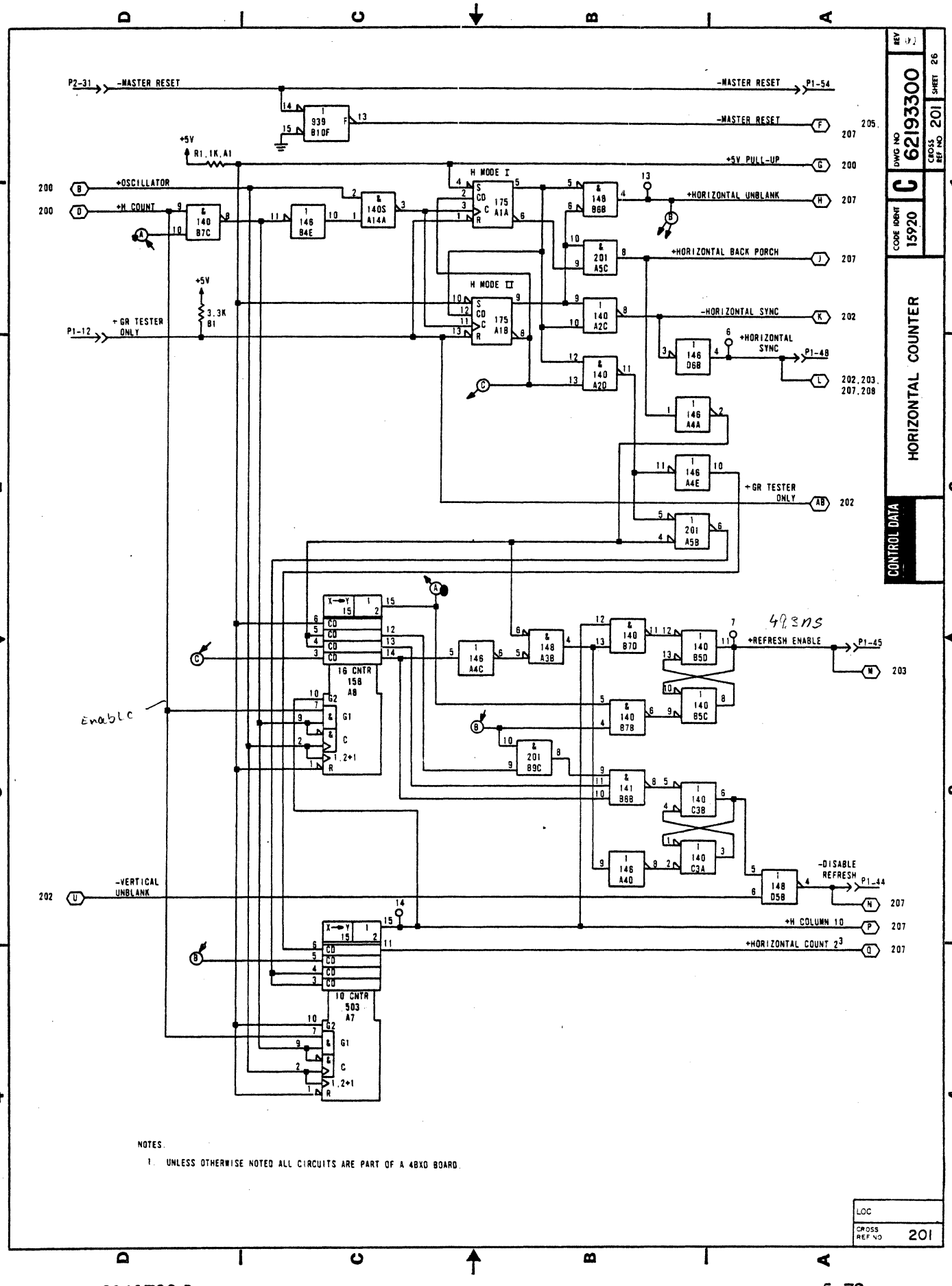

P2-31 -MASTER RESET
-MASTER RESET P1-54
-MASTER RESET F 207
+5V R1, 1K, A1
+5V PULL-UP G 200
200 B +OSCILLATOR
200 D +H COUNT
H MODE I
+HORIZONTAL UNBLANK H 207
+HORIZONTAL BACK PORCH J 207
H MODE II
+5V 3.3K B1
P1-12 +GR TESTER ONLY
-HORIZONTAL SYNC K 202
+HORIZONTAL SYNC P1-48
L 202, 203, 207, 208
+GR TESTER ONLY AB 202
+REFRESH ENABLE P1-45
M 203
49.3ns
16 CNTR 158 A8
Enable
10 CNTR 503 A7
202 U -VERTICAL UNBLANK
-DISABLE REFRESH P1-44
N 207
+H COLUMN 10 P 207
+HORIZONTAL COUNT 2^3 Q 207
NOTES.
1. UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 4BX0 BOARD.
REV
DWG NO 62193300
SHEET 26
CROSS REF NO 201
CODE IDENT 15920 C
HORIZONTAL COUNTER
CONTROL DATA
LOC
CROSS REF NO 201

DIAGRAM 202
VERTICAL COUNTER

These circuits keep track of the vertical beam position during each crt full-screen refresh operation. Beam position is counted in units of scan line time (a scan line time is the duration required for the beam to complete one horizontal scan across the screen). Each vertical portion of the refresh operation, counted/controlled by these Vertical Counter circuits, consists of four sequential segments as follows:

- Display time (otherwise termed vertical unblank time when the beam moves down the 240 scan lines where the maximum of 24 lines of characters may appear on the crt screen).
- Front porch time (with 60-Hz input power, which specifies 60 refresh operations each second, this is a 2-scan-line time allowed after the 240th display-producing scan line. For 50-Hz refresh, this time equals 28 scan line times).
- Vertical sync time (6-scan-line time, following front porch time, allowed for beam flyback to top left corner of crt screen).
- Back porch time (with 60-Hz input power, which specifies 60 refresh operations each second, this is a 17-scan-line time, following sync time, allowed for beam settling. For 50-Hz refresh, this time equals 44 scan line times).

Following paragraphs describe circuit operation for the four vertical segments of a refresh operation. Refer to Timing Diagram, Vertical Timing -60 Hz and 50 Hz Refresh at the back of this logic set for waveforms which illustrate these four segments.

When +Horizontal Sync/-Horizontal Sync signals are toggling (see diagram 201), the Vertical Counter constantly cycles through its four sequential-count segments to track the vertical beam position as it moves down the crt screen during a refresh. To start each of the four segments, the counter automatically preloads to a unique value which determines the number of scan lines to be counted in that segment's count time. Each segment's preload value is fixed by: 1) the Vertical Counter preload control flip-flops 240D4A and 240D4B, 2) by multiplexers 508D3 and 508C2, and 3) by associated translation gates (top half of this diagram). Flip-flops 240D4A and 240D4B change condition for each of the sequential count segments. Their condition controls multiplexers 508D3 and 508C2 which, in turn, preload segment starting-count values in the two counter stages (158C1 and 158D1) as follows:

Preload Control Flip-Flop		V Counter Segment Active **	Preload Value Clocked Into V Counter (By Highgoing +Horizontal Sync)
240D4A	240D4B		
*Clear (Out pin 6 = L)	*Clear (Out pin 10 = L)	Unblank (240 counts)	$0001\ 0000_2$ loads as first count of this 240-count segment for either 60 or 50-Hz refresh.
Set (Out pin 6 = H)	Clear (Out pin 10 = L)	Front Porch (2 counts if 60 Hz refresh or 28 counts if 50 Hz)	$1111\ 1110_2$ loads as first count of this 2-count segment for 60-Hz refresh.
Clear (Out pin 6 = L)	Set (Out pin 10 = H)	Sync (6 counts)	$1111\ 1010_2$ loads as first count of this 6-count segment for either 60 or 50-Hz refresh.
Set (Out pin 6 = H)	Set (Out pin 10 = H)	Back Porch (17 counts if 60 Hz refresh or 44 counts if 50 Hz)	$1110\ 1111_2$ loads as first count of this 17-count segment for 60-Hz refresh. 1101 0100 loads as first count of this 44-count segment for 50-Hz refresh.
*Clear etc.	*Clear etc.	Unblank etc.	$0001\ 0000_2$ etc.

* 240D4A and 240D4B condition after an active low reset input (+GR Tester Only input signal via diagram 201).

** NOTE: Total V Counter cycle = 265 Horizontal Sync counts if 60-Hz refresh = 16.66 msec. For 50-Hz refresh, total cycle = 318 counts = 20.00 msec.

-Horizontal Sync signal (diagram 201) is active low during Sync segment of each horizontal scan line operation. At the end of the Sync segment, -Horizontal Sync goes inactive high. If the Vertical Counter has completed counting scan line times for one of the four sequential segments (16-counter 158C1 carry output pin 15 = high), -Horizontal Sync signal ending toggles the Vertical Counter preload control flip-flops (240D4A and 240D4B) to the next sequential counter segment.

+Horizontal Sync signal (diagram 201) goes active high at the Sync segment of each horizontal scan line operation. This highgoing signal is the clock for the Vertical Counter stages (158C1 and 158D1). Thus, the counter keeps track of the number of horizontal scan line times completed during any given segment. Such count includes the preload to each segment's starting point as the first count (see preceding tabular description of preloading).

+60 Hz signal (P2-53) must be high if input power is 60 Hz. 60-Hz input power specifies 60 full-screen, crt refresh operations per second. If 50-Hz power (50 refresh operations per second) is present, this input must be low. The high or low condition of the +60 Hz signal preloads the Vertical Counter, via multiplexers 508D3 and 508C2, with the proper starting values for front porch and back porch segments (see preceding tabular description of preloading).

+Vertical Sync/-Vertical Sync signals are active only when Vertical Counter preload control flip-flops specify the counter's Sync segment being active. This is true while flip-flop 240D4A is clear and flip-flop 240D4B is set.

+Vertical Unblank/-Vertical Unblank signals are active only when Vertical Counter preload control flip-flops specify the counter's Unblank segment being active. This is true while both flip-flops (240D4A and 240D4B) are clear.

+Monitor Vertical Sync signal is active high when +Vertical Sync and -Vertical Sync signals are (240D4A clear and 240D4B set).

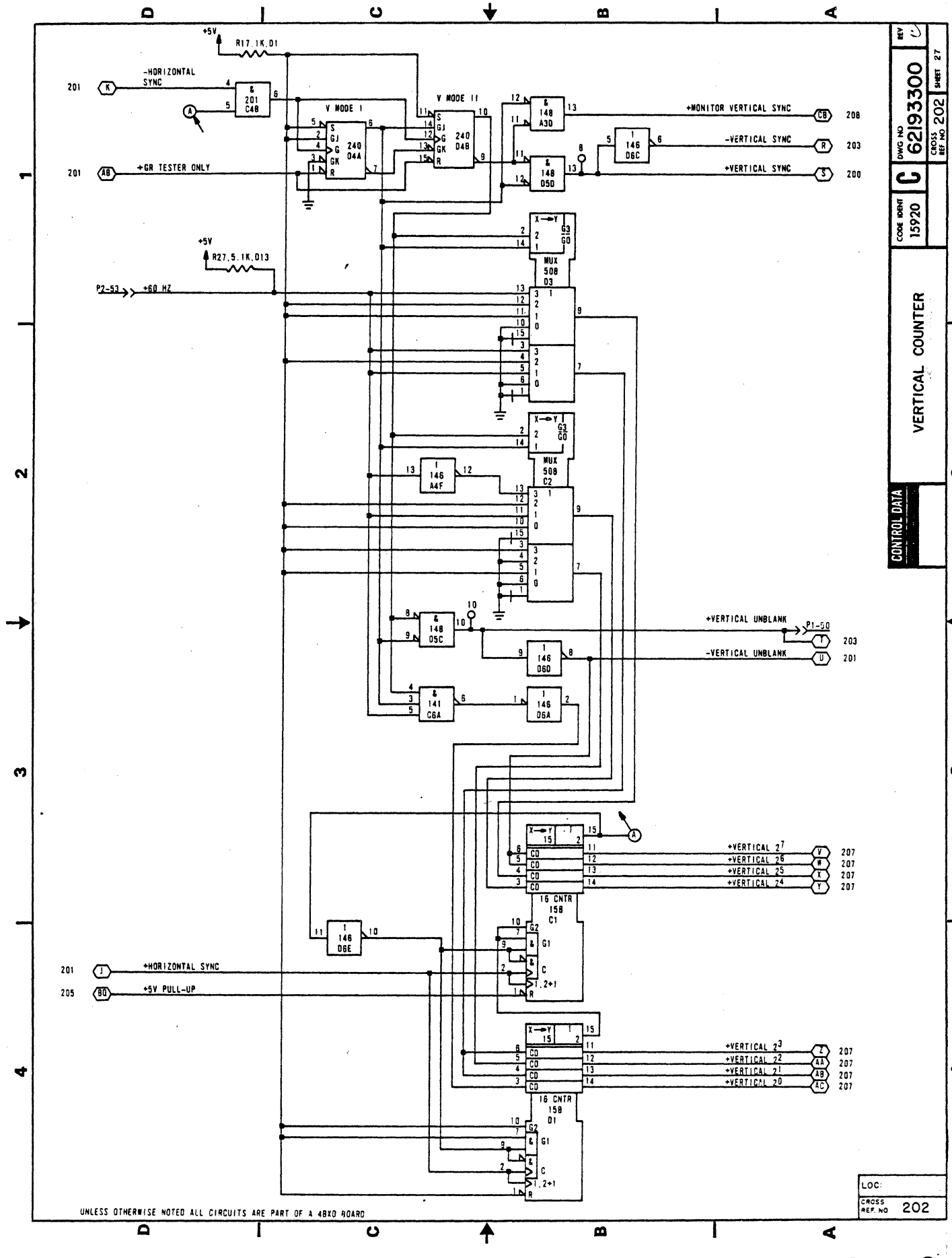

VERTICAL COUNTER
CONTROL DATA
DWG NO 62193300
REV C
SHEET 27
CROSS REF NO 202
CODE IDENT 15920
+5V
R17.1K.D1
-HORIZONTAL SYNC
201 K
&
201
C48
V MODE I
240
D4A
V MODE II
240
D4B
+GR TESTER ONLY
201 AB
&
148
A3D
+MONITOR VERTICAL SYNC
CB 208
1
146
D8C
-VERTICAL SYNC
R 203
+VERTICAL SYNC
S 200
+5V
R27.5.1K.D13
P2-53
+60 HZ
X→Y
G3
G0
MUX
508
D3
MUX
509
C2
1
146
A4F
&
148
D5C
+VERTICAL UNBLANK
P1-50
T 203
1
146
D6D
-VERTICAL UNBLANK
U 201
&
141
C6A
1
146
D6A
+VERTICAL 2^7
+VERTICAL 2^6
+VERTICAL 2^5
+VERTICAL 2^4
V 207
W 207
X 207
Y 207
CD
16 CNTR
158
C1
1
146
D6E
G2
G1
C
1,2+1
R
201 J
+HORIZONTAL SYNC
205 BD
+5V PULL-UP
+VERTICAL 2^3
+VERTICAL 2^2
+VERTICAL 2^1
+VERTICAL 2^0
Z 207
AA 207
AB 207
AC 207
16 CNTR
158
D1
LOC:
CROSS REF NO 202
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 4BXD BOARD

DIAGRAM 203
VIDEO GENERATOR AND LINE BUFFER CONTROLS

The circuits shown on this diagram comprise the video signal generator and line buffer control circuits.

LINE BUFFER CONTROL CIRCUITS (240C9A and associated gates) — These circuits issue various control signals which govern acquiring and using external memory data (from a memory on the shared bus) to refresh the crt display screen. Following paragraphs describe these control circuits.

+Refresh Read Clock/-Refresh Read Clock signals (AND 201A5D) are active each time Line Buffer data is required for the next displayable character-cell portion of a scan line (each displayable character-cell scan line is nine dot times wide). These signals activate when: 1) +Refresh Enable signal (diagram 201) is active indicating beam position within the horizontal character-display area of 80 character cells and 2) Dot Counter (diagram 200) holds any count from 010_2 through 111_2 for the scan line of the present character cell being scanned. Active +Refresh Read Clock signal is an enable condition for +Shift Memory #1 signal (see description in text following). Via P2-59, it also is an enable for shifting (recirculating) memory data stored in the optional extended memory which may be present on the shared bus. Active -Refresh Read Clock signal allows the Multiplexer (diagram 204) to latch the next required recirculating character code from either: 1) Line Buffer #1 or 2) the optional extended memory module line buffer (Line Buffer #2). Which of the two sources is selected depends on +Recirculate Line Buffer #1 and -Recirculate Line Buffer #1 controls signals (see description in text following).

+Recirculate Line Buffer #1/-Recirculate Line Buffer #1 signals (flip-flop 240C9A) govern which line buffer should be read from or written into (#1, shown on diagram 204, supplies refresh character codes for the basic 12 lines of characters or #2, in optional extended memory, supplies character codes for the additional 12 (character lines). Flip-flop 240C9A issues these two signals as follows. During beam flyback (after the 10th scan line of the 24th line where characters may appear) +Vertical Unblank signal (diagram 202), is inactive low. This forces flip-flop 240C9A clear (output pin 7 = high and pin 6 = low). This makes -Recirculate Line Buffer #1 signal inactive high which prevents Line Buffer #1 (diagram 204) from loading with new Data bus codes (pin 2 input to Line Buffer #1 is held high, see diagram 204 description). During this same time, +Recirculate Line Buffer #1 signal (240C9A output pin 6) is inactive low which allows the Multiplexer (diagram 204) to select (read) the 8-bit codes recirculating on the outputs of Line Buffer #1 as the correct refresh data (see diagram 204 description of the Multiplexer). Flip-flop 240C9A maintains this condition until the end of the 10th scan line of the first row of 80 characters displayed on the crt screen. At that time, flip-flop 240C9A is clocked (toggled) to opposite state (by +Line 10 signal from scan line counter 503C15 going inactive). Now, -Recirculate Line Buffer #1 signal is active low and +Recirculate Line Buffer #1 signal is active high. This condition allows loading (writing) Line Buffer #1 (diagram 204) with new Data bus codes and allows the Multiplexer (diagram 204) to select (read) the 8-bit codes recirculating on the outputs of Line Buffer #2 (from extended memory module) as the correct refresh data. Flip-flop 240C9A maintains this condition until the end of the 10th scan line of the second row of 80 characters displayable on the crt display screen. At that time, flip-flop 240C9A toggles back to the same condition as for the top row of characters to allow reading refresh data from the recirculating outputs of Line Buffer #1. Note that -Recirculate Line Buffer #1 and +Recirculate Line Buffer #1 signals pass out to the shared bus on P2-61 and P2-62 respectively. This provides control to Line Buffer #2 which resides in the optional extended memory module which must be present on the shared bus in order to refresh a crt display screen with 24 rows of characters. The following chart show how +Recirculate Line Buffer #1 and -Recirculate Line Buffer #1 signals control which line buffer is being read from for the present character row refresh and which one is being written into for the upcoming character row refresh.

Character Row On CRT Being Refreshed	Flip-Flop 240C9A Condition	+Recirculate Line Buffer #1 Signal	-Recirculate Line Buffer #1 Signal	Recirculating Line Buffer Being Read From For Present Character Row Refresh	Recirculating Line Buffer Being Written Into For Next Character Row Refresh
1 (top)	Clear	Low (Inactive)	High (Inactive)	#1	#2*
2*	Set	High (Active)	Low (Active)	#2*	#1
3	Clear	Low (Inactive)	High (Inactive)	#1	#2*
4*	Set	High Active	Low (Active)	#2*	#1
o	o	o	o	o	o
o	o	o	o	o	o
o	o	o	o	o	o
24 (bottom)*	Set	High (Active)	Low (Active)	#2*	#1

* If extended memory is absent, writing/reading operations with Line Buffer #2 do not occur. However, flip-flop 240C9A still cycles through the extended memory character row conditions to allow writing into Line Buffer #1 for the following basic (12 rows of characters without extended rows displayed between) display row of characters. Thus, with extended memory absent, only write/read operations with Line Buffer #1 occur and only refresh data read from Line Buffer #1 appears on the crt screen.

+Refresh Write Clock signal (NOR 146B4D) is active high when the following three conditions are true.

- +Read Memory F/F signal (diagram 207) active high.
- +Ready signal (diagram 207) active high.
- -Ø2 signal (shared bus input P2-40) at inactive high half-cycle.

These conditions being true specify the time that the Shift Memory Clock signal occurs for writing next character row refresh codes into either: 1) Line Buffer #1 (diagram 204) or 2) Line Buffer #2 (in extended memory via shared bus output P2-60).

+Shift Memory #1 signal (NOR 140B13D) is either the clock which: 1) recirculates Line Buffer #1 outputs (diagram 204) to supply a refresh read character code for the present character row refresh operation in process, or 2) writes a new character code into Line Buffer #1 in preparation for the next character row refresh operation. +Shift Memory #1 pulses active for a refresh read from Line Buffer #1 if the following two conditions are true on NAND 140B13A.

- +Refresh Read Clock signal active high (occurs once during each character cell scan at +Dot Counter 2^2).
- -Recirculate Line Buffer #1 signal inactive high (true during the entire 10 scan lines time for each 80-character row being refreshed from Line Buffer #1 character codes).

+Shift Memory #1 pulses active for a refresh write into Line Buffer #1 if the following two conditions are true on NAND 140B13C.

- +Refresh Write Clock signal active high (occurs once within each 10 character cells scanned along each scan line).
- +Recirculate Line Buffer #1 signal active high (true during the entire 10 scan lines time when any one of the 12 extended memory, 80-character rows may be refreshed from Line Buffer #2 character codes. At this time, Line Buffer #1 is being written into with character codes for the next character row refresh operation).

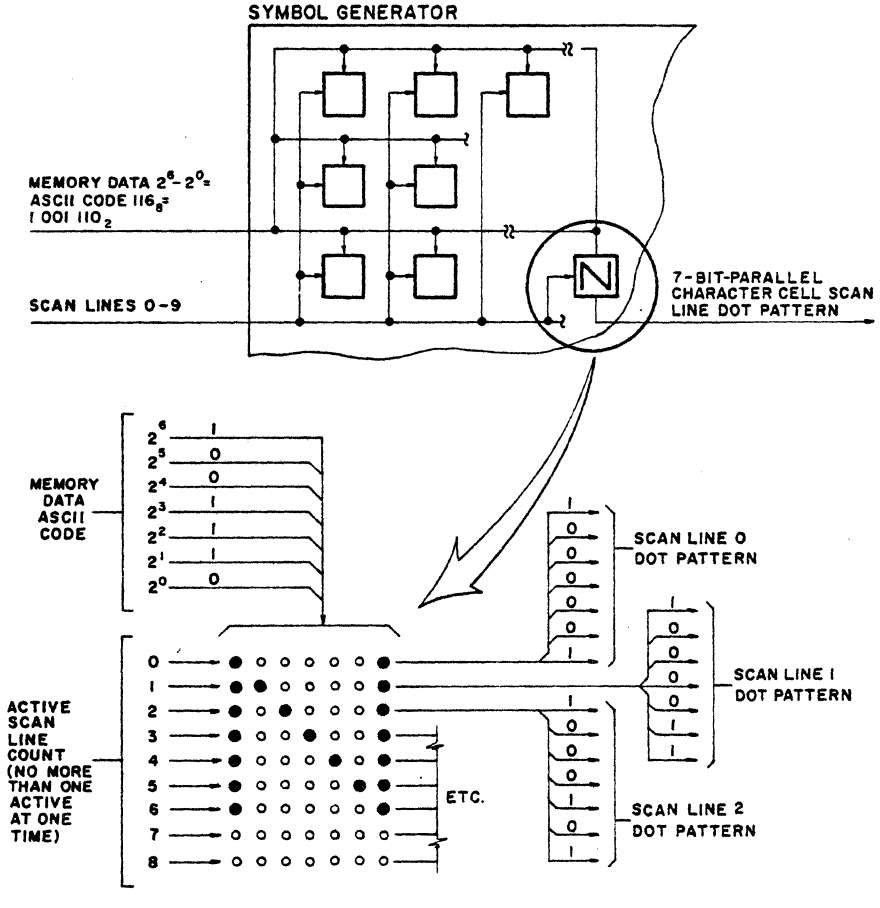
-1920 input signal (P2-54 from shared bus) will be held active low if the extended memory module is present on the shared bus. This specifies that refresh read and refresh write operations for the optional 12 lines possible on the crt display screen will occur (Line Buffer #2 in extended memory will be written in and will be read from for the additional 12 display lines allowing 960 basic display characters plus 960 extended display characters for a total of 1920 display characters). This condition determines memory addressing in the Memory Address register (diagram 206).

-Odd Line Disable signal (NAND 140B7A) is active low to prevent DMA addressing (diagram 207) for writing extended display character row characters in Line Buffer #2 if the extended memory is not present on the shared bus (-1920 signal is inactive high).

-960 Disable signal (NAND 140C7B) is active low to disable video output to the crt (diagram 205) for extended display character row refresh if the extended memory is not present on the shared bus (-1920 signal is inactive high).

VIDEO GENERATOR (503C15, MCM 6571L B14, and 547A15) — These circuits comprise the Video Generator which issues the proper serial video signal for the crt beam to properly illuminate/not illuminate each successive horizontal dot of each scan line in each character row displayable on the crt screen. Following paragraphs describe how the Video Generator circuits operate.

Symbol Generator MCM 6571L B14 is a permanently programmed, read-only memory matrix which provides video on/off condition for each of the 7-dot-wide scan lines required to display each of the 32 ASCII control codes and each of the 96 ASCII alpha/numeric/symbol character codes (see Section 7 for the crt screen dot matrix of each displayable ASCII code). The Symbol Generator is a static device where any addressing combination of the displayable character code on the +Memory Data $2^6 - 2^0$ inputs, along with one active count from the 10-line scan line counter, provides a parallel, 7-bit, scan line dot pattern output without depending on any clocking signal(s). The following illustrates Symbol Generator operation for the displayable character N.



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The 7-bit-parallel, character cell scan line dot pattern output from the Symbol Generator enters the parallel-load, 8-bit shift register 547A15 for conversion into the serial Video signal required by the crt for beam on/off conditions.

Parallel-load, 8-bit shift register 547A15 converts Symbol Generator output into the serial Video signal for crt display refresh. When shift/load input (pin 1) is low, this register loads from its eight C1D inputs. This occurs each time the Dot Counter (diagram 200) reaches full character cell +H Count on a scan across the cell if either of the following conditions is true.

- The +Memory Data code (from diagram 204) has either one or both bits 2^5 and 2^6 set specifying a displayable character code (range 040_8 to 177_8).
- A control key code is present (+Control Key signal from P1-41 is active high). This allows displaying a control code (range 00 to 37_8) which is on the +Memory Data lines (from diagram 204).

Scan line counter 503C15 keeps track of which horizontal scan line (within a character row of 10 scan lines) the crt display refresh beam is at. While the beam passes through the scan lines of the 24 character-display rows on the crt screen (+Vertical Unblank signal from diagram 202 being active high), this counter operates as a continuous ring counter which increments from zero through nine decimal. Since the count clock is +Horizontal Sync signal (diagram 201), the counter increments during the Sync time at the end of each horizontal beam scan across a 10-scan row of characters. Active low -Vertical Sync signal (diagram 203) clears the scan line counter to zero. Each time the counter reaches a count of 10 and issues an active high carry output signal (+Line 10), such carry output acts via NOR 146B4C to load the counter back to zero (load input pin 9 active low and data inputs hardwired low). This ring count continues for each active +Horizontal Sync signal until the 10th (last) scan line of the 24th (last) character row. At this point, +Vertical Unblank signal (diagram 202) becomes inactive low and disables the counter. An active -Vertical Sync (active low at the end of a full screen refresh) resets the counter so it is ready to start counting scan lines again for refreshing the top row of characters on the screen.

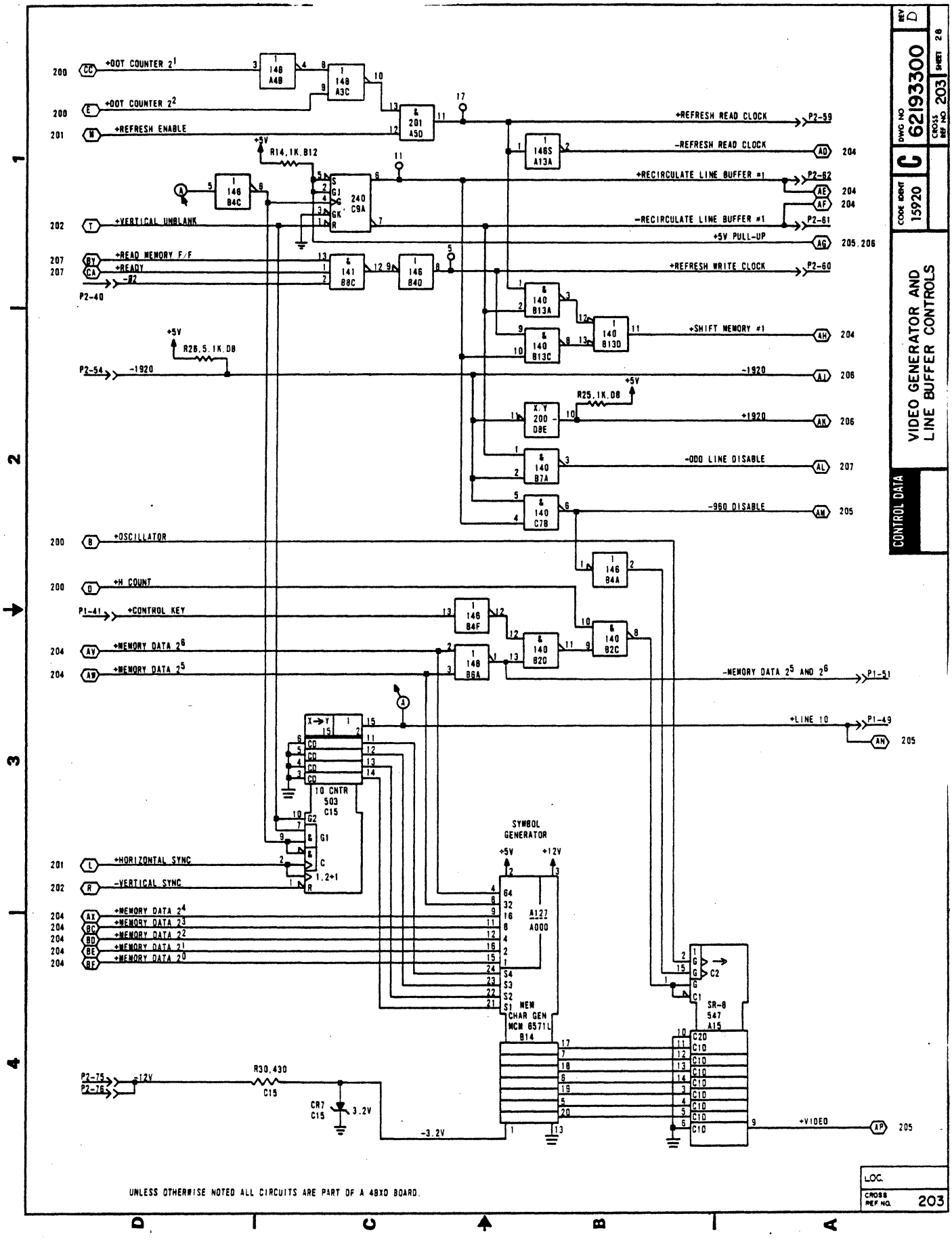
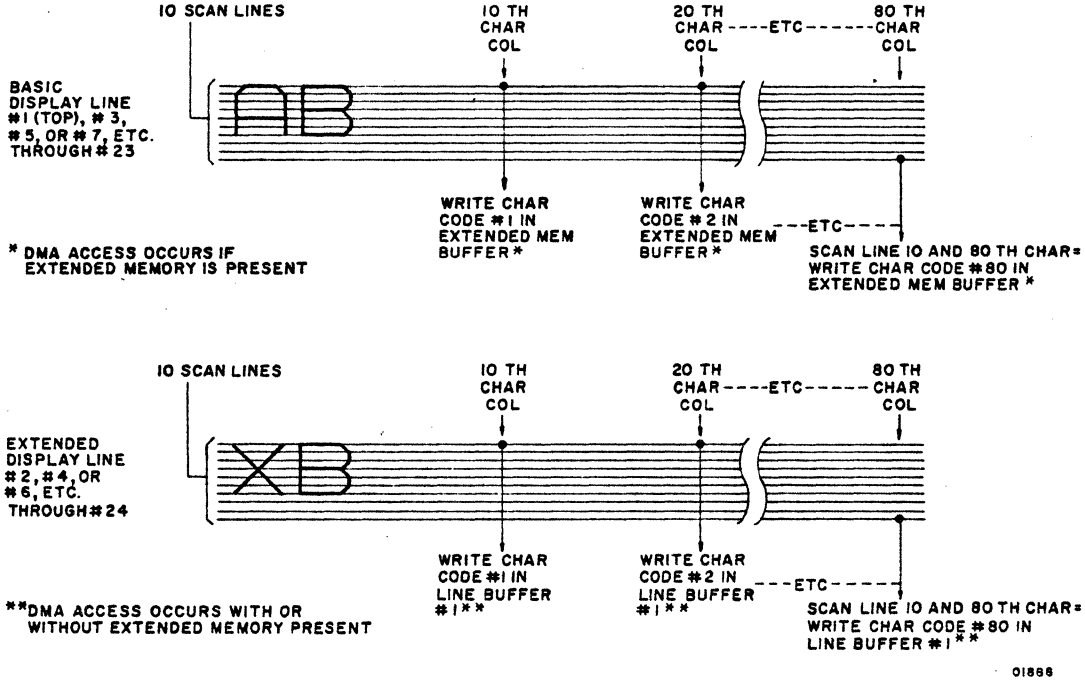

VIDEO GENERATOR AND LINE BUFFER CONTROLS
CONTROL DATA
DWG NO 62193300
REV D
SHEET 2 8
CODE IDENT 15920
C
CROSS REF NO 203
+OOT COUNTER 2^1
+OOT COUNTER 2^2
+REFRESH ENABLE
+REFRESH READ CLOCK
-REFRESH READ CLOCK
+RECIRCULATE LINE BUFFER #1
-RECIRCULATE LINE BUFFER #1
+VERTICAL UNBLANK
+5V PULL-UP
+READ MEMORY F/F
+READY
-R2
+REFRESH WRITE CLOCK
+SHIFT MEMORY #1
-1920
+1920
-ODD LINE DISABLE
-960 DISABLE
+OSCILLATOR
+H COUNT
+CONTROL KEY
+MEMORY DATA 2^6
+MEMORY DATA 2^5
-MEMORY DATA 2^5 AND 2^6
+LINE 10
+HORIZONTAL SYNC
-VERTICAL SYNC
+MEMORY DATA 2^4
+MEMORY DATA 2^3
+MEMORY DATA 2^2
+MEMORY DATA 2^1
+MEMORY DATA 2^0
SYMBOL GENERATOR
NEW CHAR GEN MCM 6571L B14
SR-8 547 A15
10 CNTR 503 C15
R14,1K,B12
R26,5.1K,D8
R25,1K,D8
R30,430 C15
CR7 C15 3.2V
-3.2V
+12V
+VIDEO
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48XD BOARD.
LOC.
CROSS REF NO. 203

DIAGRAM 204
LINE BUFFER #1 AND MULTIPLEXER

These logic circuits comprise the refresh character line buffer (Line Buffer #1) for the basic 12 character lines displayable on the crt. Also shown on this logic diagram is the multiplexer which selects refresh character codes from either: 1) Line Buffer #1 or 2) extended memory Line Buffer #2 (for optional 12 character lines added to the crt display).

LINE BUFFER #1 (183D13 and 183C13) — Two, quad, 80-bit shift registers form Line Buffer #1. Together, they hold all 80 8-bit codes which specify the contents of one row of 80 character positions on the crt screen (the 8-bit codes consist of a 7-bit ASCII code plus a cursor designation bit). Character rows supplied by Line Buffer #1 are: the top row on the screen (1st), the 3rd, the 5th, etc. through the 23rd (if present, extended memory Line Buffer #2 supplies the 2nd, 4th, 6th, through the 24th character rows). Line Buffer #1 operates in two modes. One is the input data mode where the 8-bit code on +Data Bus $2^7 - 2^0$ lines enters the buffer. This occurs on the highgoing state of -Shift Memory #1 signal (diagram 203) if -Recirculate Line Buffer #1 signal (diagram 203) is held low. The second buffer mode is the recirculate output data mode. This mode is active when -Recirculate Line Buffer #1 signal is held high. During this condition, each -Shift Memory #1 clock signal cycle causes all 80 8-bit codes stored in the buffer to shift right circular one position. The 8-bit code previously on the buffer output lines reenters the buffer and the other 79 8-bit codes shift right one position. Each successive right shift operation supplies a new character refresh code on the buffer outputs. This operation occurs 80 times during each scan line of character row refresh. This way the displayable character codes for an 80-character row follow the beam during each scan line.

Line Buffer #1 recirculates to supply displayable character codes for proper dot pattern during refresh scanning for the basic 12 displayable rows of characters as described in the preceding paragraph. While Line Buffer Control (diagram 203) is cycling through one of the optional 12 displayable rows of 80 characters (this occurs whether extended memory is present or not for actually displaying the 12 additional rows of characters), Line Buffer #1 is loaded with the 80 character codes for refreshing the succeeding basic 12-row display. This occurs as follows. During each scan line count for an extended display row, Line Buffer Control loads a character code (from +Data Bus $2^7 - 2^0$) into Line Buffer #1 once each 10 character cell times along that scan line time. Thus, eight times during each extended display character row count, a character code for the following basic display row loads in Line Buffer #1. After all 10 scan line counts for the extended row, all 80 character codes for the following basic row are loaded and ready to refresh that row. If extended memory is present on the shared bus, its Line Buffer #2 loads in the same manner during the 10 scan line times when a basic character row is being refreshed. The following illustrates this alternate writing/reading process for both the basic and extended character line buffers.



MEMORY DATA MULTIPLEXER (74298C14 and 74298C14) — Two, quad, 2-input registers form the Memory Data Multiplexer. Together, they select the 8-bit code which specifies the display contents at the present character cell position along a row of 80 characters on the crt. When refresh is occurring for one of the basic 12 lines (rows) of characters, Line Buffer Control (Diagram 203) holds +Recirculate Line Buffer #1 signal low on Multiplexer input pin 10 and strobes -Refresh Read Clock (-Clock Latch) signal low on pin 11. This selects the recirculated code present on Line Buffer #1 outputs as the refresh code for the Video Generator (diagram 203) and Cursor Video Circuits (diagram 205). If refresh is occurring for one of the extended 12 lines (rows) of characters, +Recirculate Line Buffer #1 signal is high on Multiplexer input pin 10 when -Refresh Read Clock (-Clock Latch) signal strobes low on pin 11. This selects the recirculated code from Line Buffer #2 (in extended memory) as the refresh code. Selected Memory Data 2^4 and 2^3 bits exit to the shared bus via P1-18 and P2-19 respectively for use by the optional data protect module which may be on the shared bus.

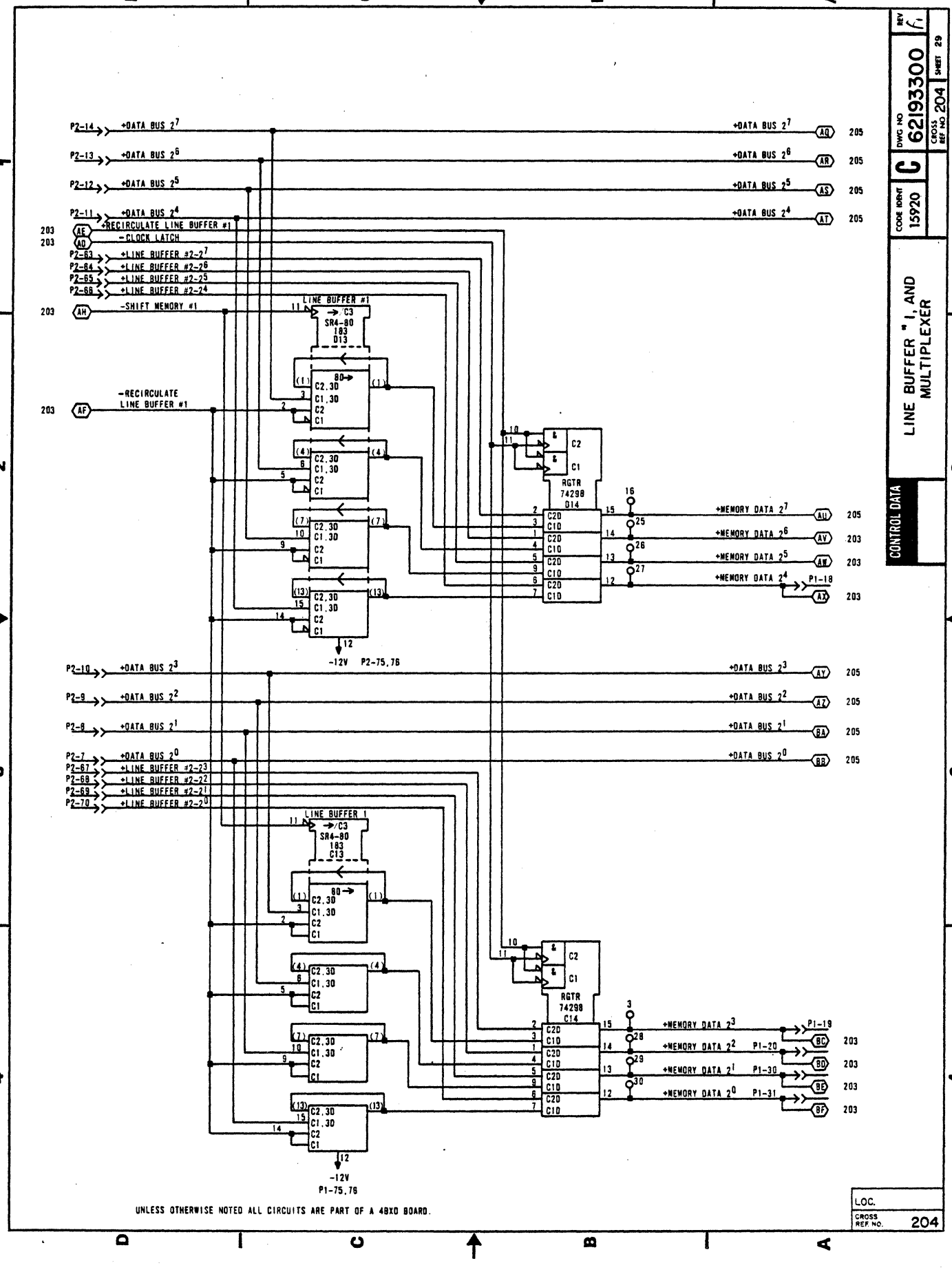

LINE BUFFER "1" AND MULTIPLEXER
CONTROL DATA
DWG NO 62193300
REV
SHEET 29
CODE IDENT 15920
CROSS REF NO 204
LINE BUFFER #1
LINE BUFFER 1
RGTR 74298 D14
RGTR 74298 C14
-12V P2-75,76
-12V P1-75,76
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48X0 BOARD.
LOC.
CROSS REF. NO. 204

DIAGRAM 205
START ADDRESS REGISTER AND BLINK COUNTER AND CURSOR VIDEO CIRCUITS

These circuits comprise the Start Address Register, the Blink Counter, the Cursor Video Control Circuit, and the Monitor Video Signal Enable Circuit.

START ADDRESS REGISTER (520C12, 520D12, and associated control gates) — Two, quad, D-type, edge-triggered flip-flops form the Start Address register. For the start of each full-screen refresh, this register supplies bits 2^{11} through 2^4 of the first address in DMA memory (DMA memory being a RAM module on the shared bus) where the first character code of the top row of display characters resides. These eight address bits become the middle bits of the 16-bit memory address issued to the shared bus by the Memory Address register (Counter) located on diagram 206. The start address is variable and is controlled by the firmware in the processor module. The processor module loads the Start Address register via shared bus data, address, and control lines. This occurs as follows:

- Processor addresses the refresh module by holding + Memory Address Bus $2^{15} - 2^{13}$ lines (diagram 206) to a value of 101_2.
- Processor places XXXX $XXXX_2$ on + Data Bus $2^7 - 2^0$ lines (diagram 204). This value is always the middle eight bits of the 16-bit address of the first character (display column one) for one of the 24 possible rows of characters. It must be the first character of a row to allow a display line-scroll capability. The missing, most and least significant address digits, are subsequently generated by circuits on diagram 206.
- Processor issues an active high + Output Strobe signal (P2-37) which clocks + Data Bus $2^7 - 2^0$ into the Start Address register where they become the Start Address $2^{11} - 2^4$ bits.

See diagram 206 description for how the remaining eight binary bits (most and least significant bits) are formed.

BLINK COUNTER (158C5) — Up-binary counter 158C5 increments by one at each active highgoing +Vertical Sync signal (diagram 202). This occurs once at the end of each full-screen crt refresh (once each 16.66 msec for 60-Hz refresh or once each 20.00 msec for 50-Hz refresh). This is a continuous-running 16-counter (whenever + Vertical Sync is cycling) so its carry output (pin 15) occurs once every 16 +Vertical Sync times (16 X 16.66 msec or 16 X 20 msec, which is approximately four times per second for either one). The carry output (termed + Blink Counter Terminal Count) passes to the shared bus via P1-47 to provide timing for the optional edit module which may be present on the bus. Output pin 11 from the Blink Counter will be low for the first eight counts and high for the last eight counts, which also is an overall cycle of approximately four times per second. The pin 11 output prevents cursor display during the first eight counts (first half counter cycle) by holding a low on pin 11 of Cursor Video Enable flip-flop 240C9B.

CURSOR VIDEO CONTROL CIRCUIT (240C9B) and 141B8A) — This circuit does two things. One, it recognizes the presence of a valid, displayable cursor (full width underline in the 10th scan line of one character cell on the entire crt display) and two, it blinks the refresh of the cursor video at a rate of approximately four times per second. A low level on pin 11 output from the Blink Counter (pin 11 is low approximately four times per second during one half-cycle of the Blink Counter) holds Cursor Video Enable flip-flop 240C9B in the disable cursor condition (output pin 9 low). This provides the blinking by alternately preventing/enabling video output for a valid, displayable cursor. When Blink Counter pin 11 is high (during last half-cycle of count and occurring approximately four times per second), Cursor Video Enable flip-flop 240C9B output pin 9 will go active high at the highgoing end of - H Count signal (diagram 200) if the following three conditions are concurrently true at NAND 141B8A..

- + Memory Data 2^7 signal (diagram 204) active high (specifies that the cursor bit of the present character cell code is set).
- + Line 10 signal (diagram 203) active high (specifies that the horizontal beam is scanning in the cursor display scan line which is scan line 10).
- -960 Disable signal (diagram 203) inactive high (specifies either of two conditions: 1) one of the basic 12 lines (rows) of characters is being refreshed so + Memory Data 2^7 being active high is a valid cursor designation at the present character cell along scan line 10, or 2) extended memory module is present on the shared bus so a valid cursor designation may appear in one of the 12 extended character row locations since no high-floating bits 2^7 are present as in the case when extended memory is absent, making bit 2^7 of extended character row locations high-floating).

If -960 Disable signal is active low, it specifies that an extended memory character row is being counted through in the refresh module circuits but that extended memory module is not present. In this case, all + Memory Data 2^7 bits will be floating high and must be blocked by the active low -960 Disable signal to prevent displaying a constant cursor in scan line 10.

MONITOR VIDEO SIGNAL ENABLE CIRCUIT (140A14C, 140B13B, and associated gates) — When + Vertical And Horizontal Unblank signal (diagram 207) is active high, + Monitor Video output signal (140SA14D) reflects either one of the following two types of scan line information. One is a serial dot pattern for a character cell scan line (this video dot pattern arrives from the Video Serializer (diagram 203) and is clipped into properly and uniformly spaced dot-bursts of beam video by the constantly cycling - Oscillator signal (diagram 200). The other type of +Monitor Video output is the cursor, which is a constant, beam-on, video signal across the 10th scan line of a character cell. Cursor video turns on at the end of the horizontal dot count for the scan across the preceding character cell and remains on until the end of the horizontal dot count for the scan across the present (cursor location) cell. Therefore, the cursor displays as a solid underline across the full 9-dot width of the character cell. + Monitor Video output signal passes through the Video Driver circuit (diagram 208) on its way to the crt.

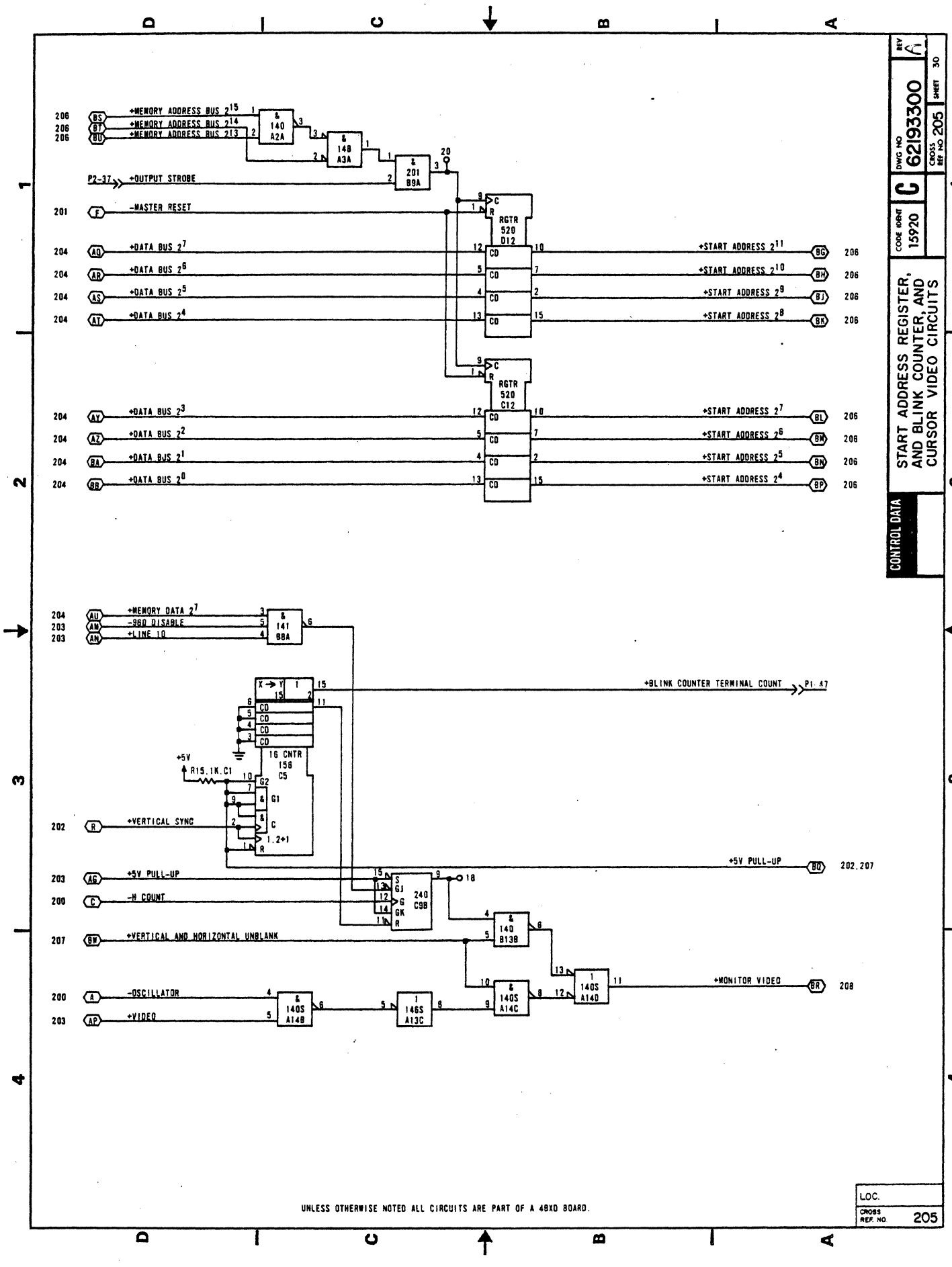

CONTROL DATA
START ADDRESS REGISTER, AND BLINK COUNTER, AND CURSOR VIDEO CIRCUITS
CODE IDENT 15920
DWG NO 62193300
REV C
SHEET 30
CROSS REF NO 205
+MEMORY ADDRESS BUS 2^15
+MEMORY ADDRESS BUS 2^14
+MEMORY ADDRESS BUS 2^13
& 140 A2A
& 148 A3A
& 201 B9A
P2-37
+OUTPUT STROBE
-MASTER RESET
RGTR 520 D12
RGTR 520 C12
+DATA BUS 2^7
+DATA BUS 2^6
+DATA BUS 2^5
+DATA BUS 2^4
+DATA BUS 2^3
+DATA BUS 2^2
+DATA BUS 2^1
+DATA BUS 2^0
+START ADDRESS 2^11
+START ADDRESS 2^10
+START ADDRESS 2^9
+START ADDRESS 2^8
+START ADDRESS 2^7
+START ADDRESS 2^6
+START ADDRESS 2^5
+START ADDRESS 2^4
+MEMORY DATA 2^7
-960 DISABLE
+LINE 10
& 141 B8A
+BLINK COUNTER TERMINAL COUNT
P1-47
16 CNTR 158 C5
+5V
R15.1K.C1
+VERTICAL SYNC
+5V PULL-UP
-H COUNT
240 C9B
+VERTICAL AND HORIZONTAL UNBLANK
-OSCILLATOR
+VIDEO
& 140S A14B
1 146S A13C
& 140 B13B
& 140S A14C
1 140S A14D
+MONITOR VIDEO
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48XD BOARD.
LOC.
CROSS REF. NO 205

DIAGRAM 206
MEMORY ADDRESS REGISTER AND ADDRESS BUS DRIVERS

This diagram shows the Memory Address Register (Counter) and the Address Bus Drivers.

MEMORY ADDRESS REGISTER (158C11, 158B11, 158D11, and associated gates) — Three up-binary counters, cascaded together and modified by presence/absence of extended memory (1920-character screen refresh), form the Memory Address register (Counter). During display screen refresh, this register always generates/issues a 16-bit address which specifies the location in DMA memory (DMA memory being a RAM module on the shared bus) where the code representing the next display character resides. Preceding each full-screen refresh, the register (158C11 and 158D11 only) loads with the predetermined, middle eight bits of the starting address (+ Start Address $2^{11} - 2^{4}$) from the Start Address register (diagram 205). This occurs at highgoing - Memory Address Register Clock signal (diagram 207) when - Load Memory Address Register signal (diagram 207) is active low just preceding the refresh count for the 24th character row of the preceding full-screen refresh. This allows Line Buffer #1 (diagram 204) to be loaded, via DMA, concurrently while character row 24 refresh counting occurs. The predetermined, middle eight bits of the starting address which loads are variable as loaded from the processor in the Start Address register. At the same time that an active low - Load Memory Address Register signal loads the middle eight bits, the value 0000_2 loads into the least significant four bits (158B11 only). After such loading, the register contains the start address bits XXXX XXXX 0000_2 (XXO_{16}). The Address Bus Drivers (see their description following) issue this value to the shared bus as the lower 12 bits of the DMA address to fetch the code for the first character. This first character code will load in Line Buffer #1 (diagram 204).

After the start address is loaded, each successive low-to-high transition of - Memory Address Register Clock signal (diagram 207) increments the Memory Address register value by one address location. This successively fetches individual character codes for the next character row refresh while the present character row is being counted/refreshed (if extended memory module is not present on the shared bus, fetches for and refresh of those rows of characters does not occur; only the counting which accounts for their unused position occurs).

With expanded memory present, when the Memory Address register increments to a count of 0111 1000 0000_2 (1920_{10}), NAND gates 141C6B, 148B6D, and 140B5A recognize this condition and apply a low to NOR gate 140A2B. The resulting output from NOR 140A2B combines with +Dot Counter 2^2 signal (diagram 200) in NAND 201A5A to force-clear the lower 12 bits of the Memory Address register to zero. This happens when the fetch for the 1920_{10}th character code has just finished and the next chararacter code fetch for refresh must come from the first refresh memory location which is 0010 0000 0000 0000_2 (2000_{16} on the shared bus address scheme).

With expanded memory absent, when Memory Address register increments to a count of 0011 1100 0000 (960_{10}), NAND gates 141C6B, 148B6C, and 140B5B recognize this condition and apply a low to NOR gate 140A2B. The resulting output from NOR 140A2B combines with the +Dot Counter 2^2 signal (diagram 200) in NAND 201A5A to force-clear the lower 12 bits of the Memory Address register to zero. This happens when the fetch for the 960_{10}th character code has just finished and the next character code fetch for refresh must come from the first refresh memory location which is 0010 0000 0000 0000_2 (2000_{16} on the shared bus address scheme).

ADDRESS BUS DRIVERS (939 type circuits at B10A - B10D, C10A - C10F, and D10A - D10D) — When - Enable Address Bus signal (diagram 207) is active low, these TTL circuits (three-state buffers) place the 16-bit Memory address on the shared, DMA, Memory Address Bus $2^{15} - 2^{0}$ lines. The most significant four binary bits are hard-wired to always to 0010_2. The remaining 12 lower-order bits are always those output by the Memory Address register (Counter) and, as such, they are variable from 0000 0000 0000_2 to 0111 1000 0000_2 if extended memory is present (1920 characters in 24 display lines), or they vary from 0000 0000 0000_2 to 0011 1100 0000_2 if extended memory is absent (960 characters in 12 display lines). Thus the 16-bit memory address issued may vary from 0010 0000 0000 0000_2 to 0010 0111 1000 0000_2 (2000_{16} - 2780_{16}) with expanded memory or from 0010 0000 0000 0000_2 to 0010 0011 1100 0000_2 (2000_{16} - $23C0_{16}$) for basic, 12-line display.

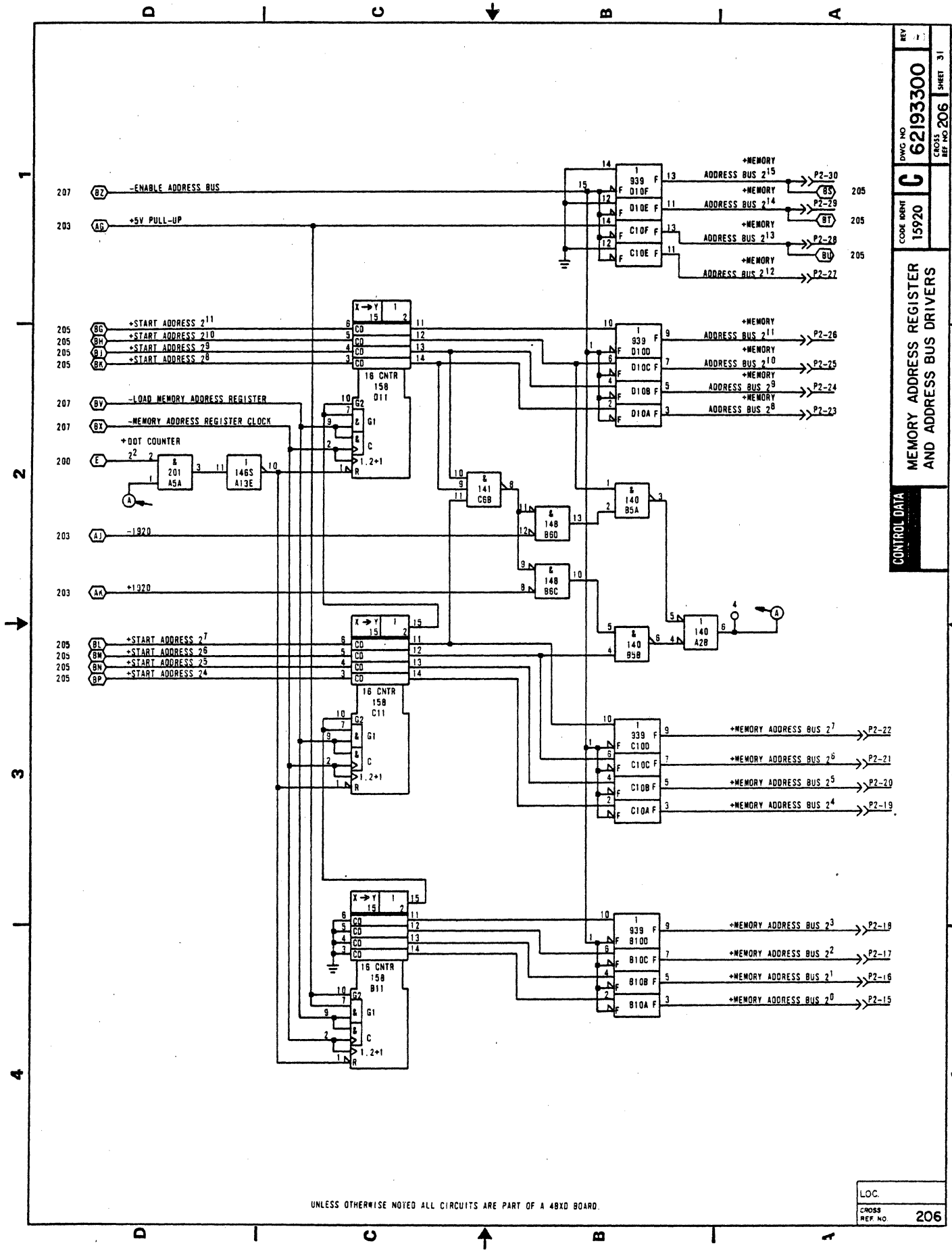

CONTROL DATA
MEMORY ADDRESS REGISTER AND ADDRESS BUS DRIVERS
CODE IDENT 15920
DWG NO 62193300
REV C
SHEET 31
CROSS REF NO 206
-ENABLE ADDRESS BUS
+5V PULL-UP
+START ADDRESS 2^11
+START ADDRESS 2^10
+START ADDRESS 2^9
+START ADDRESS 2^8
-LOAD MEMORY ADDRESS REGISTER
-MEMORY ADDRESS REGISTER CLOCK
+DOT COUNTER
-1920
+1920
+START ADDRESS 2^7
+START ADDRESS 2^6
+START ADDRESS 2^5
+START ADDRESS 2^4
16 CNTR 158 D11
16 CNTR 158 C11
16 CNTR 158 B11
+MEMORY ADDRESS BUS 2^15
+MEMORY ADDRESS BUS 2^14
+MEMORY ADDRESS BUS 2^13
+MEMORY ADDRESS BUS 2^12
+MEMORY ADDRESS BUS 2^11
+MEMORY ADDRESS BUS 2^10
+MEMORY ADDRESS BUS 2^9
+MEMORY ADDRESS BUS 2^8
+MEMORY ADDRESS BUS 2^7
+MEMORY ADDRESS BUS 2^6
+MEMORY ADDRESS BUS 2^5
+MEMORY ADDRESS BUS 2^4
+MEMORY ADDRESS BUS 2^3
+MEMORY ADDRESS BUS 2^2
+MEMORY ADDRESS BUS 2^1
+MEMORY ADDRESS BUS 2^0
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48X0 BOARD.
LOC.
CROSS REF. NO. 206

DIAGRAM 207
MEMORY ADDRESS REGISTER CONTROL AND DMA CHANNEL CONTROL CIRCUITS

This diagram shows the Memory Address Register Control and DMA Channel Control circuits. Used to enable both of these circuits is the 231st Unblank Scan Line Detector.

231ST UNBLANK SCAN LINE DETECTOR (206D2) — This 8-input NAND gate recognizes the 231st scan line during a full-screen refresh operation. This specifies the beginning of the first scan line in the 24th row of 24 possible lines of characters. This occurs when +Vertical Unblank signal (diagram 202) is active high and when +Vertical $2^7 - 2^0$ signals (from Vertical Counter on diagram 202) = 1111 $0101_2 = 245_{10}$. Since the Vertical Counter is a 256_{10} counter which preloads to start the next segment on reaching full count of 255_{10} (see diagram 202 description), the count of 245_{10} reached is the 231st displayable scan line since the start of the Vertical Unblank segment. Count of 246_{10} = scan line 232, etc., through count of 254 = scan line 240 (last displayable scan line). The vertical scan line = 231_{10} becomes active by the active-going Horizontal Sync segment which follows the display portion of the 230th scan line. Thus the count corresponding to the 231st scan line is reached before the Horizontal Back Porch segment which precedes the Horizontal Unblank display segment of the 231st scan line. See diagrams 201 and 202 descriptions for definitions of Horizontal and Vertical segments. Output from the 231st Unblank Scan Line Detector first enables Memory Address Register Control and then DMA Channel Control circuits as described following.

The end of the 230th scan line immediately precedes refreshing the last row of characters on the screen (row 24, which is always scan-counted but displays only if extended memory option is present). This is time for the refresh control circuits to concurrently begin loading the basic refresh line buffer (Line Buffer #1, diagram 204) for the top row of characters which will be required by the next full-screen refresh.

MEMORY ADDRESS REGISTER CONTROL (Gates 141C6C, 201B9B, 140B2B, 141B3C, and 140B2A) — At the proper time/conditions, these circuits issue -Load Memory Address Register, -Memory Address Register Clock, and +Vertical And Horizontal Unblank signals to the Memory Address register (diagram 206) and the Monitor Video Signal Enable Circuits (diagram 205).

-Load Memory Address Register signal (NAND 141C6C) is active low to enable loading the start address for the next full-screen refresh. This occurs when the following three conditions are active.

- 231st scan line during Vertical Unblank refresh segment. The corresponding count becomes active at active-going Horizontal Sync segment following scan line 230_{10} and preceding the 17-character/column - count Horizontal Back Porch segment which starts the 231st scan line. After its initiation, this scan line remains through the normal Horizontal Back Porch, Unblank, and Front Porch segments).
- +Horizontal Sync signal (diagram 201) active high (Start of scan line 231_{10} which is the top scan line of character row 24).
- +H Column 10 signal (diagram 201) active high.

- Memory Address Register Clock signal (NOR 140B2A) pulses active low to load the starting address into the Memory Address register when the following two conditions are true on NAND 140B2B.

- + Load Memory Address Register signal active high
- + H Count signal (diagram 200).

- Memory Address Register Clock signal (NOR 140B2A) pulses active low to increment the Memory Address register (Counter) when the following three conditons aretrue on NAND 141B3C.

- + Vertical And Horizontal Unblank signal active high (see description in a following paragraph).
- +H Column 10 signal (diagram 201) active high.
- - Odd Line Disable signal (diagrar 203) inactive high (this signal is active low only to prevent DMA addressing for writing extended display character row codes in Line Buffer #2 if the extended memory option is not present).

+ Vertical And Horizontal Unblank signal (AND 201B9B) is active high to allow + Monitor Video signal (diagram 205) to pass to the Video -To-Monitor driver (diagram 208) to refresh the crt screen. This unblank signal is the result of both + Vertical Unblank signal (diagram 202) and + Horizontal Unblank signal (diagram 201) being active.

DMA CHANNEL CONTROL (240C8A, 240C8B, 140C7C/140C7D, and associated gates) — At the proper time/conditions, these circuits issue the following DMA channel control signals: -Hold and -Memory Read. These circuits receive the following DMA channel control signals: Ø4, +HLDA, and Ready.

- Hold signal (200B8B) is made active low when the refresh circuits request using the shared bus for DMA operation. This signal passes to the processor module via P2-44. The precessor will complete its machine cycle, enter Hold state, and issue/maintain an active Hold Acknowledge (+HLDA see description in a following paragraph) back to the refresh module. The processor releases the shared bus to exclusive refresh module use when in Hold state (as long as - Hold signal remains active). - Hold signal becomes active and remains so as long as the following conditions are true to hold a low on Hold flip-flop 240C8A input pin 1.

- - Odd Line Disable signal (diagram 203) inactive high
- -Disable Refresh signal (diagram 201) inactive high
- + Horizontal Count signal (diagram 201) active high
- +Line 24 active (first scan line of line 24 which is 231st in the Vertical Unblank segment).
- +Horizontal Back Porch signal (diagram 201) active high

-Memory Read signal (200D8C) is made active low when the refresh circuits request using the shared bus for a DMA read operation. This signal passes to the refresh memory module (RAM module) via P2-35. The RAM module will return to the refresh module (+Data Bus $2^7 - 2^0$) the character code stored at the addressed (+Memory Address Bus $2^{15} - 2^0$ on diagram 206) RAM location. -Memory Read signal becomes active by Read Memory flip-flop 240C8B setting on the low-to-high transaction of -Ø4 signal (from processor module timing via P2-43 on the shared bus) if the following conditions are true. Hold flip-flop is already set (Hold flip-flop sets to request the shared bus for a DMA operation). -Master Reset signal (diagram 201) is not active low. +HLDA signal (from processor module via P2-45) is not inactive low (+HLDA is held active high by the processor when a refresh module DMA is authorized by the processor). +Read Memory F/F signal from pin 10 of the flip-flop enables +Refresh Write Clock signal (diagram 203) for basic Line Buffer #1 and Line Buffer #2 (#2 resides in optional extended memory module). Pin 9 output from Read Memory flip-flop being low force clears Hold flip-flop as soon as the force set conditions on Hold flip-flop input pin 1 disappear. As soon as Hold flip-flop clears, -Hold signal to the processor goes inactive and the processor removes the active high +HLDA input (P2-45). With +HLDA inactive low, Read Memory flip-flop is held clear (output pin 9 held high) which allows Hold flip-flop to be force-set by the next of active Hold-requesting conditions (see -Hold signal description paragraph preceding).

- Enable Address Bus signal (140C7C) is active low when the refresh circuits have acquired DMA use of the shared bus from the processor module. This signal being active low gates the address of DMA requested data from the refresh module's Memory Address register (diagram 206) to the shared bus. The signal is active when Hold flip-flop is set and + HLDA is active high from the processor. - Ready signal (P2-32 from addressed memory module via shared bus) is active low when the addressed memory module has the requested information ready and on the + Data Bus $2^7 - 2^0$ lines (diagram 204). Active -Ready signal is an enable for +Refresh Write Clock signal (diagram 203) which clocks DMA acquired character refresh codes into either basic Line Buffer #1 or extended memory Line Buffer #2.

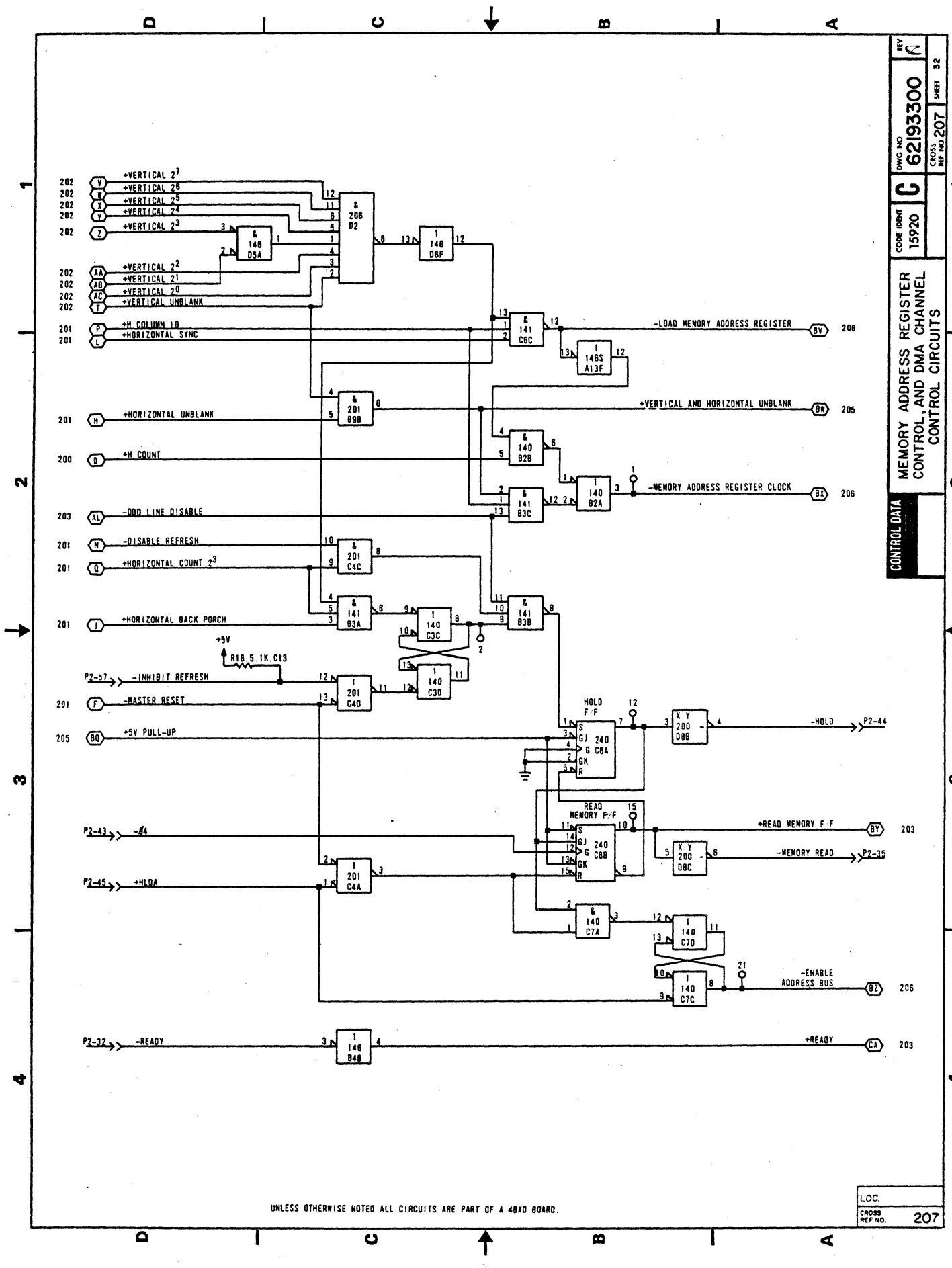
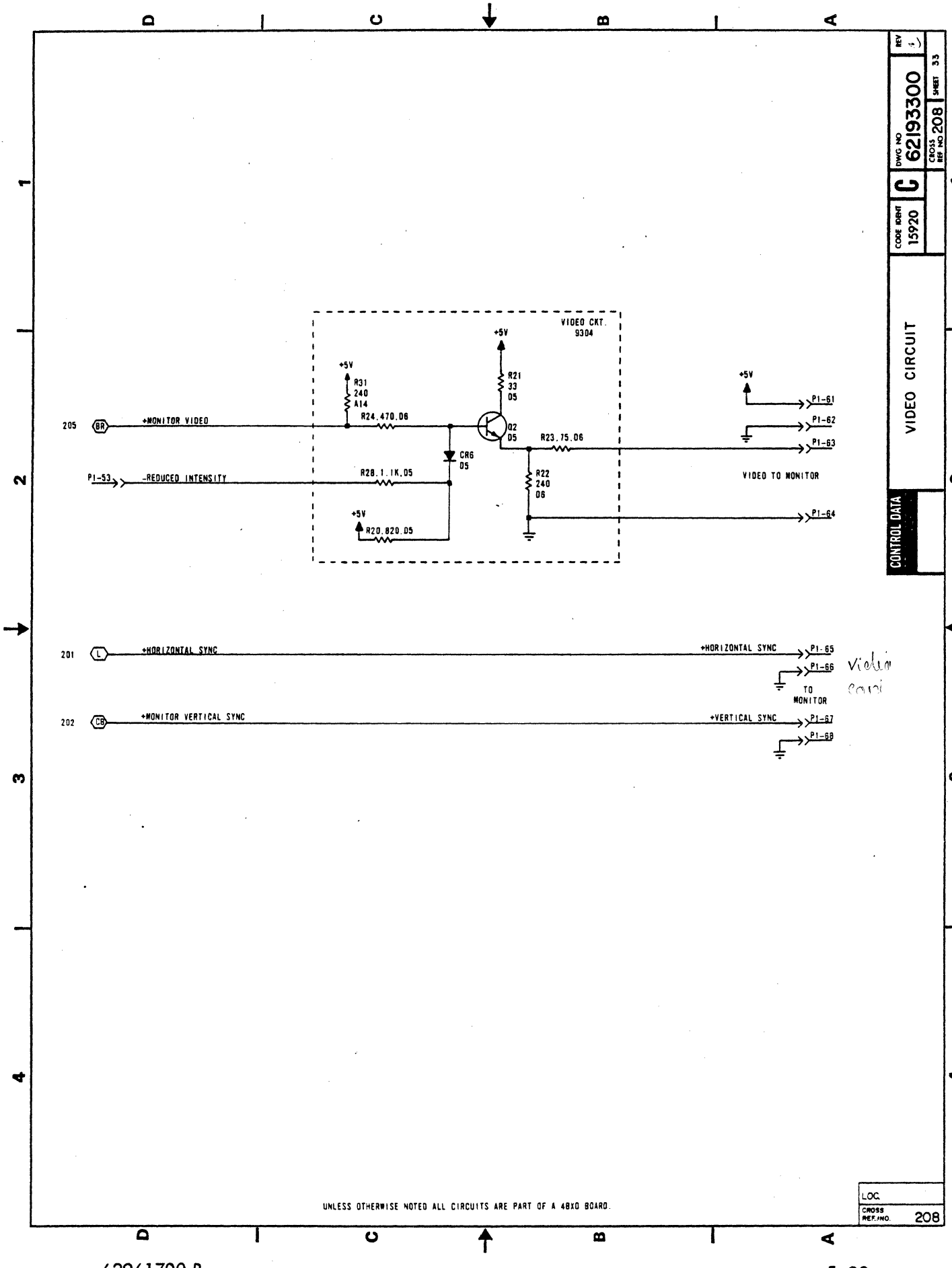

DWG NO 62193300
REV A
SHEET 32
CROSS REF NO 207
CODE IDENT 15920
C
MEMORY ADDRESS REGISTER CONTROL, AND DMA CHANNEL CONTROL CIRCUITS
CONTROL DATA
+VERTICAL 2^7
+VERTICAL 2^6
+VERTICAL 2^5
+VERTICAL 2^4
+VERTICAL 2^3
+VERTICAL 2^2
+VERTICAL 2^1
+VERTICAL 2^0
+VERTICAL UNBLANK
+H COLUMN 10
+HORIZONTAL SYNC
+HORIZONTAL UNBLANK
+H COUNT
-ODD LINE DISABLE
-DISABLE REFRESH
+HORIZONTAL COUNT 2^3
+HORIZONTAL BACK PORCH
+5V
R16.5.1K.C13
-INHIBIT REFRESH
-MASTER RESET
+5V PULL-UP
-HLDA
+HLDA
-READY
-LOAD MEMORY ADDRESS REGISTER
+VERTICAL AND HORIZONTAL UNBLANK
-MEMORY ADDRESS REGISTER CLOCK
HOLD F/F
-HOLD
READ MEMORY F/F
+READ MEMORY F.F
-MEMORY READ
-ENABLE ADDRESS BUS
+READY
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48X0 BOARD.
LOC.
CROSS REF. NO. 207

DIAGRAM 208
VIDEO CIRCUIT

This diagram shows the three output signals from the refresh control module which drive the video display monitor. The top circuit shown on this diagram receives the on/off, serial, video signal from the Monitor Video Enable Circuit (diagram 205). If present on the shared bus, the optional highlight module may reduce intensity of the + Monitor Video signal (this done via - Reduced Intensity signal from highlight via P1-53). The resulting video stream passes to the video display monitor via P1-63 and P1-64 signal lines. + Horizontal Sync and + Vertical Sync signals, shown on the lower portion at this diagram (generated by circuits shown on diagrams 201 and 202 respectively), pass directly to the video display monitor via P1-65/P1-66 and P1-67/P1-68 signal lines.


VIDEO CKT.
9304
+5V
R31
240
A14
R24.470.06
205
BR
+MONITOR VIDEO
R21
33
05
Q2
05
R23.75.06
CR6
05
P1-53
-REDUCED INTENSITY
R28.1.1K.05
R22
240
06
R20.820.05
P1-61
P1-62
P1-63
VIDEO TO MONITOR
P1-64
201
L
+HORIZONTAL SYNC
P1-65
P1-66
TO
MONITOR
202
CB
+MONITOR VERTICAL SYNC
+VERTICAL SYNC
P1-67
P1-68
REV
DWG NO
62193300
CROSS REF NO 208
SHEET 33
CODE IDENT
15920
VIDEO CIRCUIT
CONTROL DATA
UNLESS OTHERWISE NOTED ALL CIRCUITS ARE PART OF A 48X0 BOARD.
LOC.
CROSS REF. NO.
208

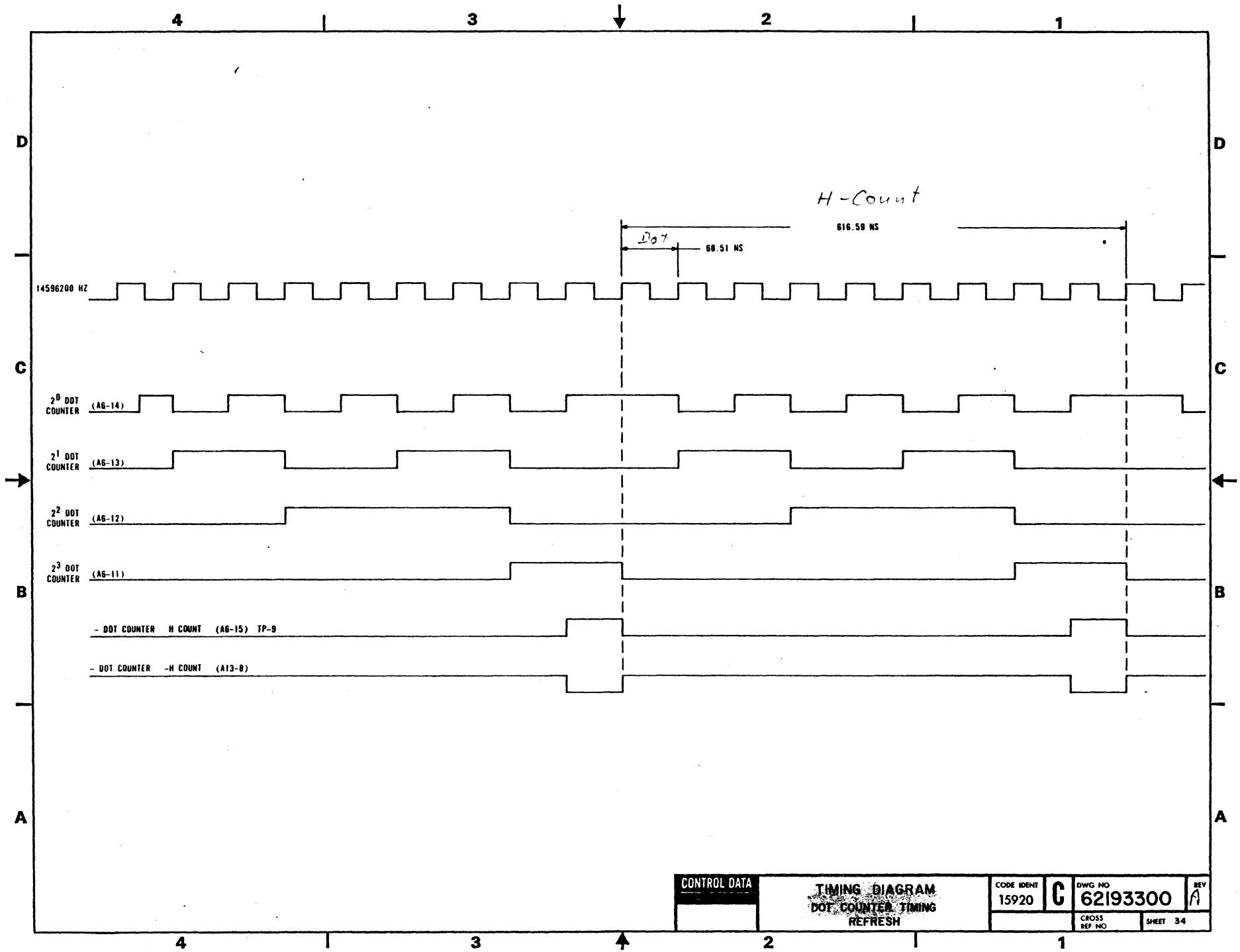
TIMING DIAGRAM
DOT COUNTER TIMING REFRESH

The waveforms shown on this sheet illustrate timing characteristics of the Dot Counter (diagram 200). The Dot Counter keeps track of the horizontal beam position while it passes across the nine horizontal dot locations of a scan line within a character cell dot matrix. Refer to the backpage description of diagram 200 for circuit details.

14596200 Hz — The top waveform is the Oscillator signal output from the Line Lock circuit (diagram 200). This constantly-running signal govems the rate of the beam scan by clocking the Dot Counter (and other circuits described elsewhere). Each cycle of this signal is 68.51 nanoseconds long. Each highgoing pulse of this signal increments the Dot Counter.

2^0, 2^1, 2^2, AND 2^3 DOT COUNTER OUTPUTS — These are the count outputs from the constantly-running 4-bit up-decade, Dot Counter. A constant ring-count occurs with these bits changing count-state once every 68.51 nanoseconds (the rate of the 14596200 Hz clock signal). 2^2 only is used. 2^2 enables a Refresh Read Clock signal (diagram 203) to be active once during the midpoint of each 9-dot-count cycle of the Dot Counter.

CARRY PULSE — DOT COUNTER + H COUNT/- H COUNT — These two waveforms show the + H Count ripple-carry from the Dot Counter. They show the cycle time of the counter. Once the counter is running, a full count preloads the counter with a count of one. After this, each count equals the time for the scan line to pass across one dot within the character cell. Thus each dot scan time is 68.51 nanoseconds. The Dot Counter increments once for each successive dot time until all nine dots of a character cell scan line are counted. At this time, the carry output goes active to indicate completion of the scan across that character. This occurs once every 616.59 nanoseconds (68.51 nanoseconds by 9 dots = 616.59 nanoseconds). The active carry output increments the character position Horizontal Counter (diagram 201) once for every 9 dots scanned.


4
3
2
1
D
C
B
A
H-Count
616.59 NS
Dot
68.51 NS
14596200 HZ
2^0 DOT COUNTER (A6-14)
2^1 DOT COUNTER (A6-13)
2^2 DOT COUNTER (A6-12)
2^3 DOT COUNTER (A6-11)
- DOT COUNTER H COUNT (A6-15) TP-9
- DOT COUNTER -H COUNT (A13-8)
CONTROL DATA
TIMING DIAGRAM
DOT COUNTER TIMING
REFRESH
CODE IDENT 15920
C
DWG NO 62193300
REV A
CROSS REF NO
SHEET 34

TIMING DIAGRAM
HORIZONTAL TIMING REFRESH

This diagram shows the timing scheme for the horizontal scan line refresh operation. This timing applies to each horizontal beam scan line used by the crt. The Horizontal Counter (diagram 201) is the main control circuit for the horizontal scanning operation. Refer to the backpage description of diagram 201 for circuit details.

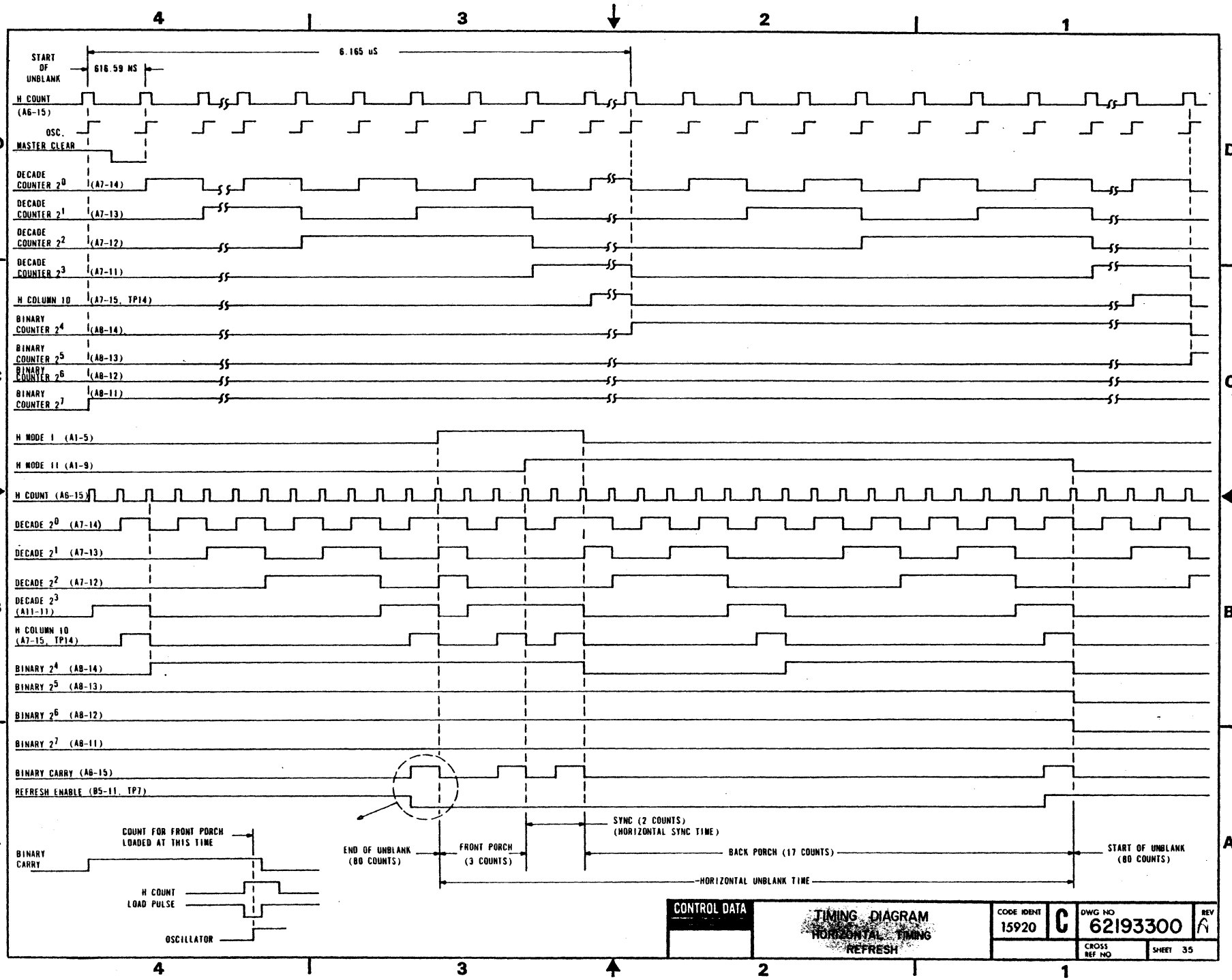
This timing diagram shows the basic count pattern: 1) from the decade counter which keeps track of each successive group of 10 character positions along a scan line, and 2) from the binary counter which keeps track of the number of groups of 10 character positions along a scan line. These counters (part of the Horizontal Counter shown on diagram 201) operate together to track the horizontal character position of any one beam scan across the scrt screen. Note that active + H Count (from the Dot Counter shown in diagram 200) is the enable condition for Horizontal Timing increments. + H Count is active each time the horizontal beam scans across the ninth dot position of a character cell (see preceding Timing Diagram and its backup page description).

The waveforms of this timing diagram illustrate the timing for one complete horizontal scan line operation. During the 80 H Counts, while the beam scans across the 80 character positions on the screen, the following occurs:

- The decade and binary counters keep track of the beam position.
- Refresh Enable is active to allow unblanking dot positions for displaying character patterns.

After the 80th character position is scanned, a 3-character "front porch" time is counted in the Horizontal Counter. After this, a 2-character Horizontal Sync time is counted. During active Horizontal Sync time, the beam retraces back to the left side of the crt screen for the next scan. After Sync time, a 17-character "back porch" time is counted in the Horizontal Counter. During this time, the beam stabilizes and moves into position for starting scanning across another line of 80 character positions.

As seen by the preceding, one complete horizontal scan line cycle = 80 + 3 + 2 + 17 character count times = 102 character count times = 102 by 616.59 nsec (each character count time = 616.59 nsec) = 62.9 μsec.


START OF UNBLANK
616.59 NS
6.165 uS
H COUNT (A6-15)
OSC.
MASTER CLEAR
DECADE COUNTER 2^0 (A7-14)
DECADE COUNTER 2^1 (A7-13)
DECADE COUNTER 2^2 (A7-12)
DECADE COUNTER 2^3 (A7-11)
H COLUMN 10 (A7-15, TP14)
BINARY COUNTER 2^4 (A8-14)
BINARY COUNTER 2^5 (A8-13)
BINARY COUNTER 2^6 (A8-12)
BINARY COUNTER 2^7 (A8-11)
H MODE I (A1-5)
H MODE II (A1-9)
H COUNT (A6-15)
DECADE 2^0 (A7-14)
DECADE 2^1 (A7-13)
DECADE 2^2 (A7-12)
DECADE 2^3 (A11-11)
H COLUMN 10 (A7-15, TP14)
BINARY 2^4 (A8-14)
BINARY 2^5 (A8-13)
BINARY 2^6 (A8-12)
BINARY 2^7 (A8-11)
BINARY CARRY (A6-15)
REFRESH ENABLE (B5-11, TP7)
COUNT FOR FRONT PORCH LOADED AT THIS TIME
BINARY CARRY
H COUNT LOAD PULSE
OSCILLATOR
END OF UNBLANK (80 COUNTS)
FRONT PORCH (3 COUNTS)
SYNC (2 COUNTS) (HORIZONTAL SYNC TIME)
BACK PORCH (17 COUNTS)
START OF UNBLANK (80 COUNTS)
HORIZONTAL UNBLANK TIME
CONTROL DATA
TIMING DIAGRAM
HORIZONTAL TIMING
REFRESH
CODE IDENT 15920
C
DWG NO 62193300
REV A
CROSS REF NO
SHEET 35

TIMING DIAGRAMS
VERTICAL TIMING — 60 HZ REFRESH AND — 50 HZ REFRESH

This diagram, and the one following, shows the timing scheme for the vertical scan refresh operation. This timing applies to each full-screen refresh operation. The Vertical Counter (diagram 202) is the main control circuit for the vertical scanning operation. Refer to the backpage description of diagram 202 for circuit details.

These timing diagrams show the count pattern of the two binary counters which keep track of the number of vertical scan lines during a crt full-screen refresh operation. These counters (part of the Vertical Counter shown on diagram 202) operate together to track the vertical, scan line position of the beam during any one full-screen refresh down the crt screen. Note that active + Horizontal Sync (from the Horizontal Counter shown on diagram 201) is the enable condition for Vertical Timing increments. + Horizontal Sync is active each time the beam completes a horizontal scan line and retraces to the left side of the crt to begin the next horizontal scan line (see preceding Timing Diagram and its backup page description).

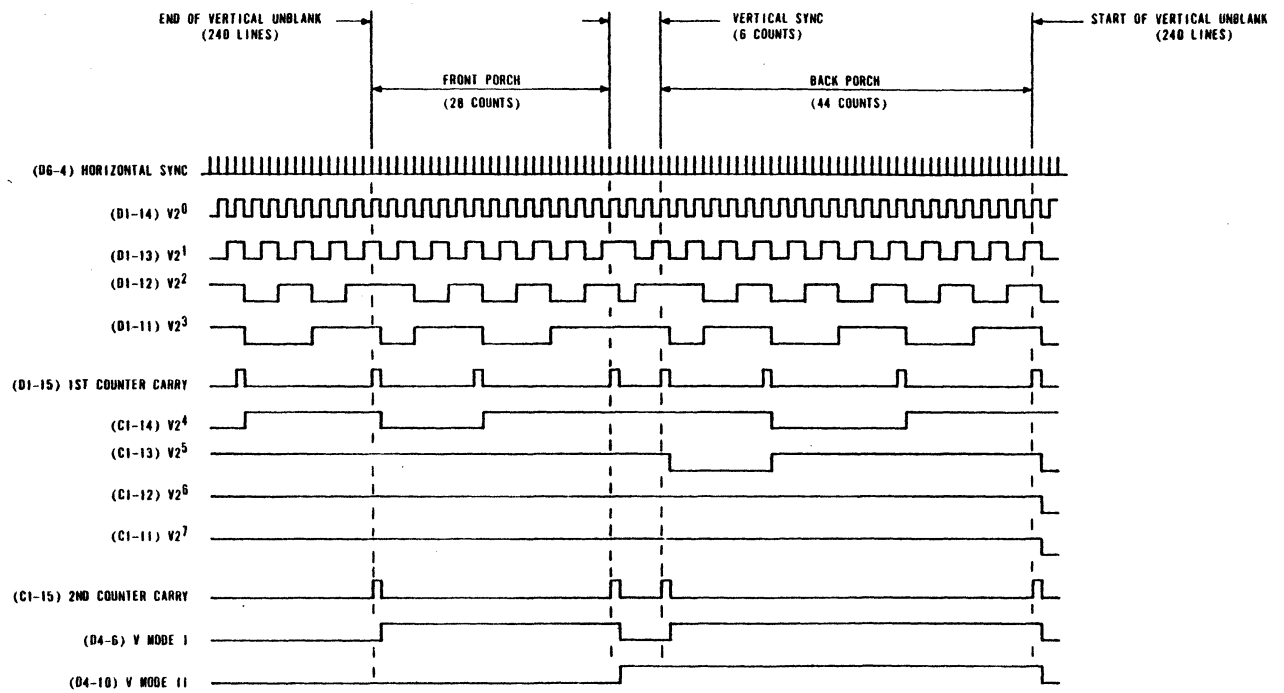
The waveforms of these timing diagrams illustrate the timing for one complete, vertical, crt refresh operation. During the 240 Horizontal Sync counts, while the beam drops down across the 24 possible character line positions on the screen (240 horizontal scan line positions), the following occurs:

- The two binary counters keep track of the vertical beam position (in multiples of scan line position).
- Vertical Unblank is active to allow unblanking dot positions for displaying character patterns.

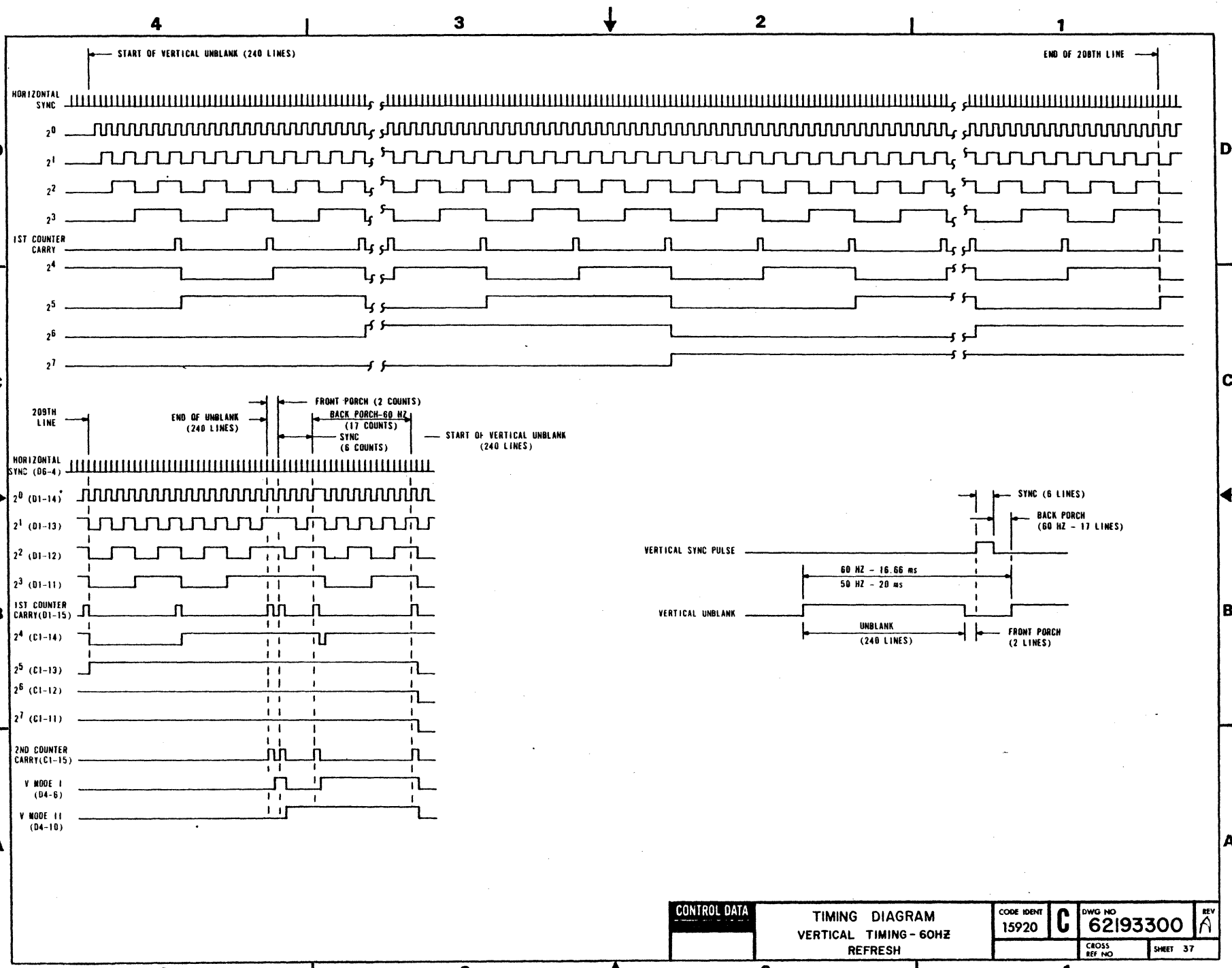
For 60-Hz input power which specifies 60 full-screen refresh operations per second, the following occurs. After the 240th scan line is completed, a 2-scan-line "front porch" time is counted in the Vertical Counter. After this, a 6-scan-line Vertical Sync time is counted. During active Vertical Sync time, the beam flys back to the top, left corner of the crt screen for the next refresh operation. After Sync time, a 17-scan-line "back porch" time is counted in the Vertical Counter. During this time, the beam stabilizes and moves into position for starting scanning across another full screen of 24 lines of characters (240 horizontal scan lines).

As seen by the preceding, one complete vertical refresh cycle for 60 Hz = 240 + 2 + 6 + 17 scan line count times = 265 scan line count times = 265 by 62.9 μsec (each scan line time = 62.9 μsec) = 16.66 msec.

For 50-Hz input power, which specifies 50 full-screen refresh operations per second, each complete vertical refresh cycle = 240 + 28 + 6 + 44 scan line count times = 318 scan line count times = 318 by 62.9 μsec (each scan line time = 62.9 μsec) = 20.00 msec.



CONTROL DATA	TIMING DIAGRAM VERTICAL TIMING - 50HZ REFRESH	CODE IDENT 15920	C	DWG NO 62193300	REV A
				CROSS REF NO	SHEET 36

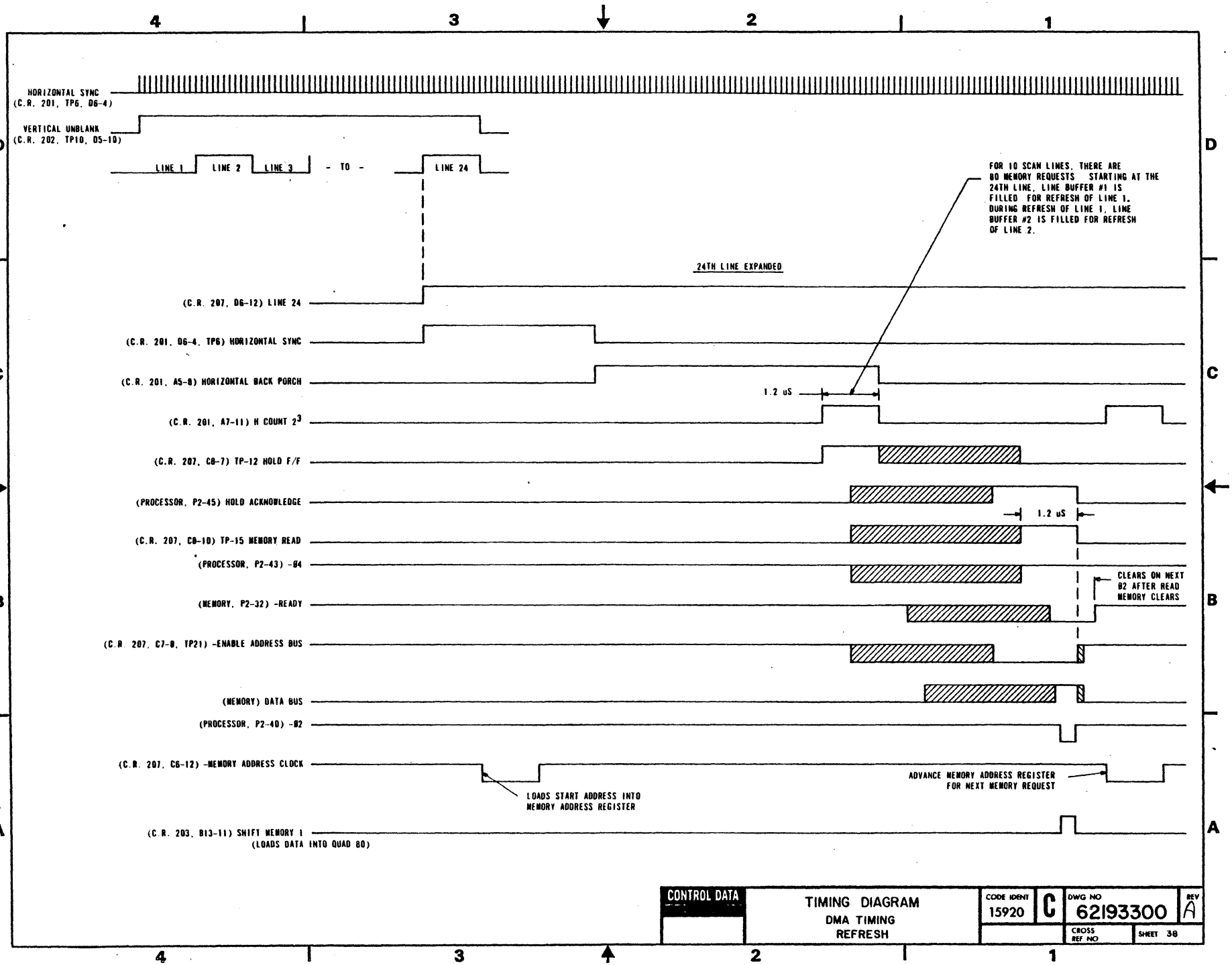


CONTROL DATA	TIMING DIAGRAM VERTICAL TIMING - 60HZ REFRESH	CODE IDENT 15920	C	DWG NO 62193300	REV A
				CROSS REF NO	SHEET 37

TIMING DIAGRAM
DMA TIMING REFRESH

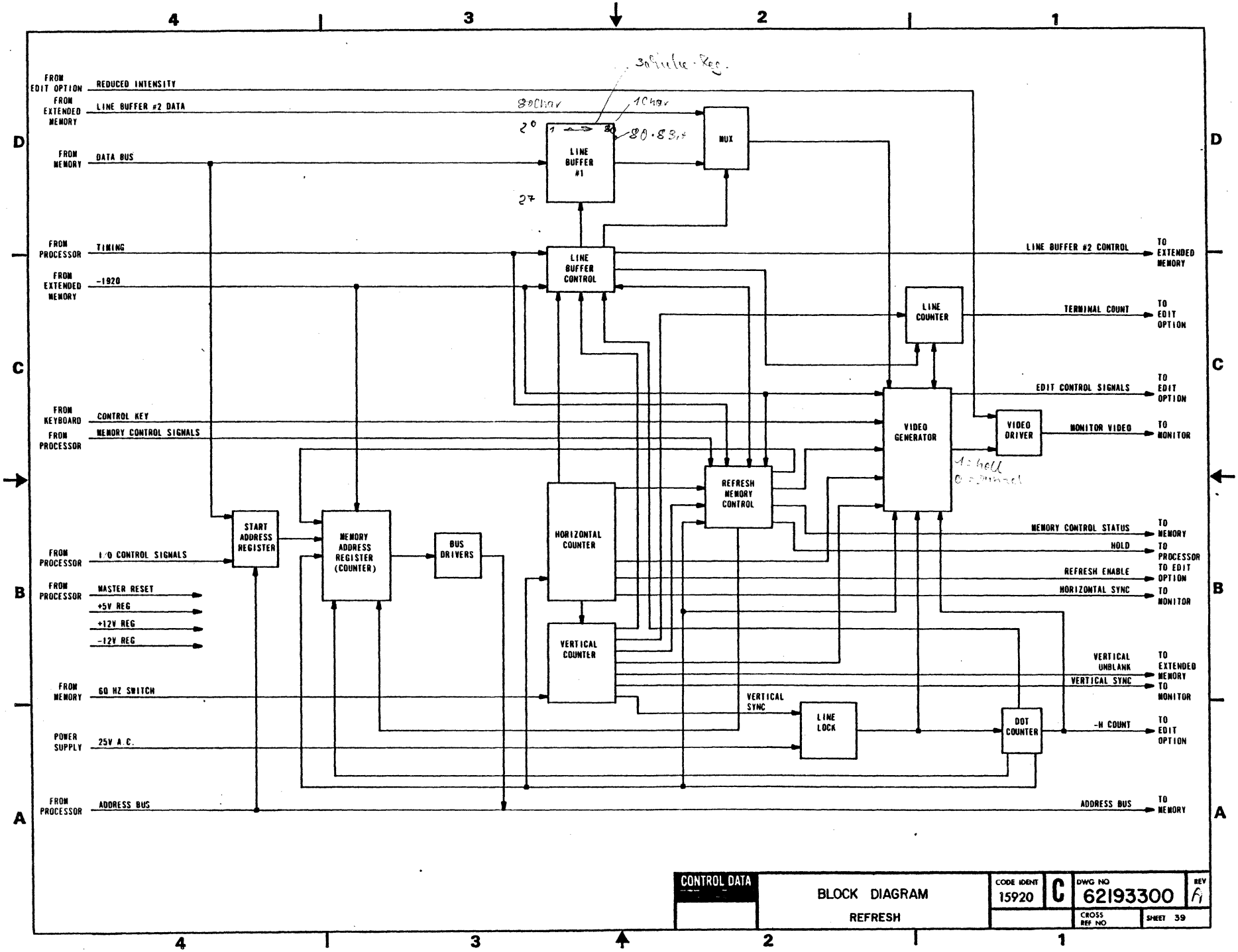
The waveforms shown on this diagram illustrate timing for DMA requests issued by the refresh control card to acquire crt refresh character codes. Whenever the refresh control circuits require a character refresh code from a refresh memory location (refresh memory is in the RAM located on the shared bus), they must request control of the shared bus from the processor circuits. They do this by placing an active + Hold signal on the bus. The processor gives bus control to the refresh circuits by returning an active Hold Acknowledge signal. Following this, the refresh places the address of the desired code on the Address bus and issues an active Memory Read signal to the shared bus. The addressed memory location responds with the code stored there by placing that code on the Data bus and making the shared bus Read signal active. After this, the refresh circuits shift the code into either the basic, quad 80 Line Buffer #1 (for basic 12 lines of displayable characters) or the optional, extended memory, quad 80, Line Buffer #2 (for extended display lines of characters which comprise the optional 12 additional lines of characters).

For a detailed description of any one of these waveforms, see the backpage description of the logic diagram referenced by the name of the waveform. For example, the 24th line expanded waveform named Horizontal Sync is described on the backpage for Control Refresh diagram 201. Also note that any card test point (e.g., TP-6) which displays the signal is specified. All signals without card test points must be checked from the generating circuit element (e.g., D6-12) on Control Refresh card for Line 24 signal.


HORIZONTAL SYNC
(C.R. 201, TP6, D6-4)
VERTICAL UNBLANK
(C.R. 202, TP10, D5-10)
LINE 1
LINE 2
LINE 3
- TO -
LINE 24
FOR 10 SCAN LINES, THERE ARE 80 MEMORY REQUESTS STARTING AT THE 24TH LINE, LINE BUFFER #1 IS FILLED FOR REFRESH OF LINE 1. DURING REFRESH OF LINE 1, LINE BUFFER #2 IS FILLED FOR REFRESH OF LINE 2.
24TH LINE EXPANDED
(C.R. 207, D6-12) LINE 24
(C.R. 201, D6-4, TP6) HORIZONTAL SYNC
(C.R. 201, A5-8) HORIZONTAL BACK PORCH
1.2 uS
(C.R. 201, A7-11) H COUNT 2^3
(C.R. 207, C8-7) TP-12 HOLD F/F
(PROCESSOR, P2-45) HOLD ACKNOWLEDGE
1.2 uS
(C.R. 207, C8-10) TP-15 MEMORY READ
(PROCESSOR, P2-43) -Ø4
CLEARS ON NEXT Ø2 AFTER READ MEMORY CLEARS
(MEMORY, P2-32) -READY
(C.R. 207, C7-8, TP21) -ENABLE ADDRESS BUS
(MEMORY) DATA BUS
(PROCESSOR, P2-40) -Ø2
(C.R. 207, C6-12) -MEMORY ADDRESS CLOCK
LOADS START ADDRESS INTO MEMORY ADDRESS REGISTER
ADVANCE MEMORY ADDRESS REGISTER FOR NEXT MEMORY REQUEST
(C.R. 203, B13-11) SHIFT MEMORY 1
(LOADS DATA INTO QUAD 80)
CONTROL DATA
TIMING DIAGRAM
DMA TIMING
REFRESH
CODE IDENT 15920
C
DWG NO 62193300
REV A
CROSS REF NO
SHEET 38

BLOCK DIAGRAM
REFRESH

This is a block diagram of the refresh control card detailed logic circuits shown on the preceding pages of this logic diagram set. It identifies the major functional circuits of the refresh control card. The diagram also serves as a functional flow summary. All of the functional circuits and signals identified on this diagram appear in a functional diagram figure in Section 4 where refresh theory of operation is described. Since thorough descriptions and references to the detailed logic circuits in Section 5 accompany the figure in Section 4, further description here would be duplication and is therefore omitted.



CONTROL DATA	BLOCK DIAGRAM REFRESH	CODE IDENT 15920	C	DWG NO 62193300	REV A
				CROSS REF NO	SHEET 39