CONTROL DATA INSTITUT

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VORLÄUFIGE AUSGABE (ENGL.)

T E R M I N A L 92450

SCHULUNGSHANDBUCH

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T E R M I N A L 92450

SCHULUNGSHANDBUCH

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TERMINAL-Kurzbeschreibung

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3.2.3 Display Quality – Display quality parameters such as resolution, distortion, stability, raster size change, contrast, and brightness shall be those defined in CDC Specification, Raster Scan CRT Display.

3.2.4 Display Brightness – Brightness is adjustable by the operator over a range that is suitable for various office ambient lighting conditions. Standard phosphor is type P4, white.

3.3 Cursor – The cursor indicates the current entry or output symbol position. It is represented on the display screen as a blinking underline of the symbol position. The blink rate is approximately four times per second.

3.4 External Controls, Indicators, and Connectors – Operator controls are located on the front panel to the right of and below the CRT face, and on the connector panel and ac entry panel at the rear of the unit. All indicators are located on the front panel below the CRT and to the right of the CRT. The front panel, ac entry panel, and connector panel are shown in Figures 4, 5, and 6 respectively.

3.4.1 POWER ON/OFF Switch – Power is applied to the terminal by pressing the righthand side of the rocker switch located on the operator control panel. Power is removed by pressing the lefthand side of the POWER ON/OFF switch.

Following application of ac power, the terminal is automatically cleared and set to the initial state as defined by the feature and mode switches.

3.4.2 ON LINE/LOCAL Switch – This switch allows the operator to place the keyboard offline and check the operation of the terminal without communicating with the modem. When this switch is activated, the transmit portion of the terminal is disabled and data originating at the keyboard is automatically transferred to memory and displayed.

Operation of the terminal in local mode allows for offline preparation, editing, and listing of bulk data when the tape cassette and printer peripherals are associated with the terminal.

3.4.3 FULL DUPLEX/HALF DUPLEX Switch – This two-position switch determines how data originating from the keyboard is routed within the terminal when operating in character mode.

HALF DUPLEX: Data is sent to modem and the terminal's memory for display and/or editing as applicable.

FULL DUPLEX: Data is sent to modem only. Data must be received to be displayed. Not available in line or block mode.

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Char-Mode jeder Char einzeln zum Modem
Line-Mode jeder Zeichen ins MEM - RAM → Display
        mit zeilenende CR → 1 Zeile zum Modem

Block - Mode
mit Sendkey ges. Block zum Modem

Klein + groß Buchstaben

9600 Baut

Anzeige
1. V24 - LED
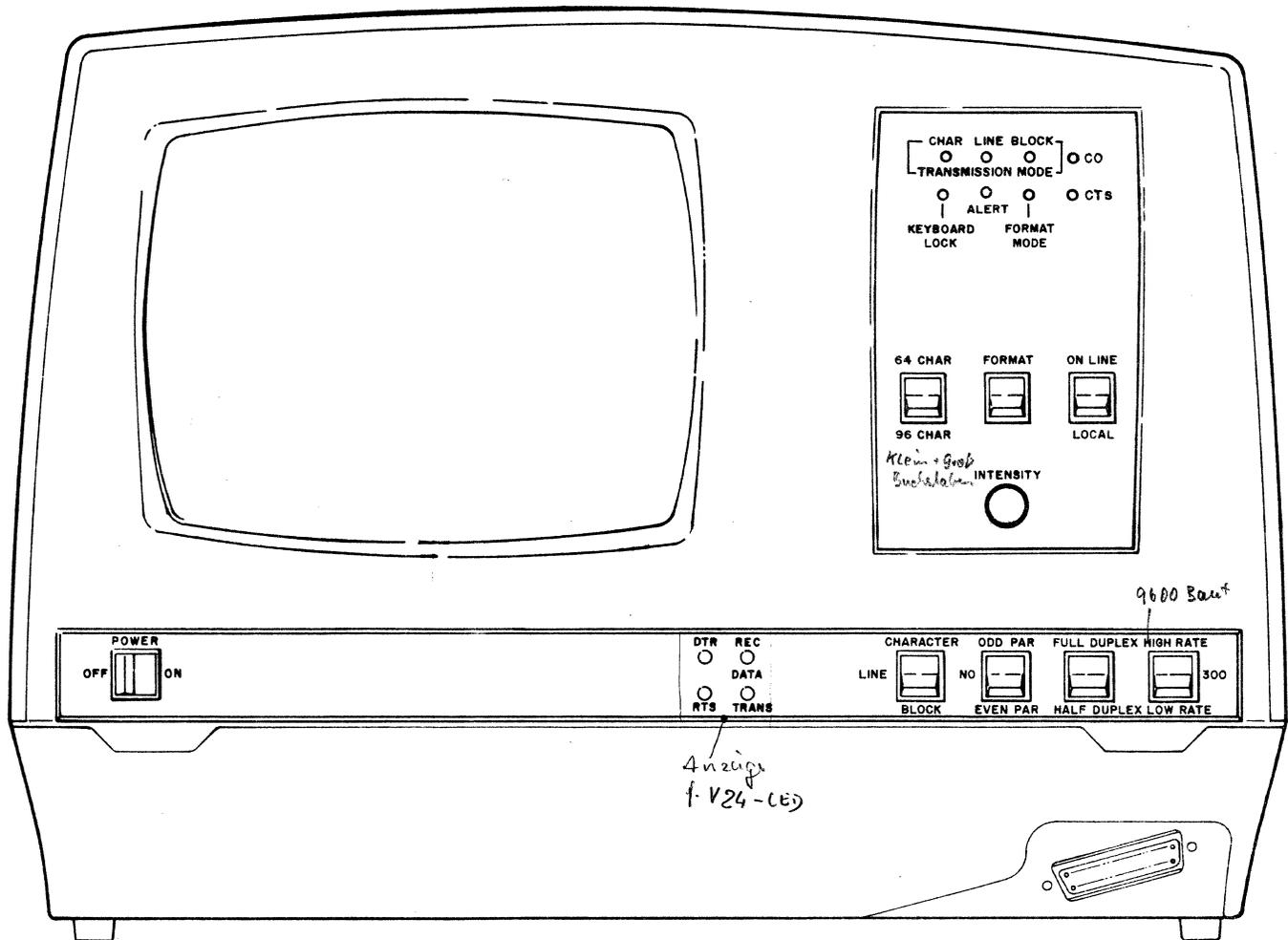
01696

Figure 4 - Front Panel Controls

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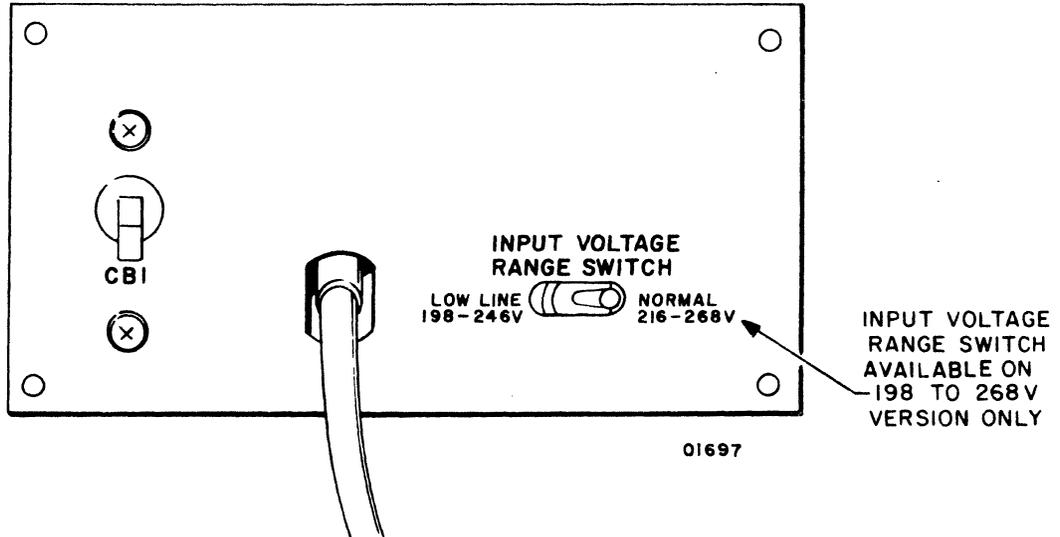
Figure 5 - AC Entry Panel

Figure 6 - Connector Panel

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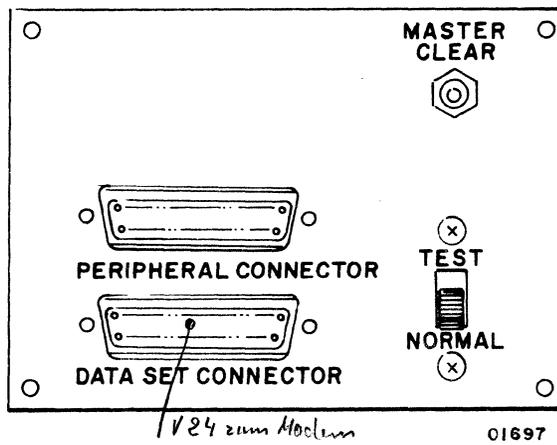PAGE 22

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3.4.4 64/96 CHARacter Switch - This two-position switch selects either
64- or 96-character output from the keyboard. With the switch in
64 position, the terminal disables the generation of octal codes 140
through 176. Those symbols not generated in the 64 position are
lowercase A through Z and those represented on the keyboard in a
contrasting color. Activation of an alpha character key, with the
keyboard in lowercase, will cause the generation of the uppercase
character labeled on that key.

3.4.5 INTENSITY Control - Located on the front panel to the right of the
CRT, this control allows the operator to adjust the video intensity
to ambient lighting conditions.

3.4.6 HIGH RATE/300/LOW RATE Switch - A three-position rocker switch
located on the front panel. This switch allows the operator to select
one of three baud rates, two of which are preset at installation.
Either the HIGH RATE or LOW RATE position allows the terminal to
operate at 110 baud, 150 baud, 200 baud, 300 baud, 600 baud, 1200 baud,
1800 baud, 2400 baud, 4800 baud, or 9600 baud. The center position
selects 300 baud at all times. The terminal may be preset to the same
baud rate in both HIGH RATE and LOW RATE positions. The terminal will
be set to 110 baud in the LOW RATE position and 9600 baud in the
HIGH RATE position upon shipment. Reference Internal Switches for
further details on baud-rate selection.

3.4.7 CHARACTER/LINE/BLOCK Switch - A three-position rocker switch that
allows the operator to select the mode of transmission. The ter-
minal may be operated in character, line, or block mode. The
operational characteristics in each mode are as follows.

3.4.7.1 Character Mode - Data originating at the keyboard is transferred
to the interface as keys are actuated. Outgoing data is serialized
in a manner consistent with teletypewriter conventions and transferred
to the modem in a character-by-character fashion. A three-character
internal buffer is provided to accommodate sporadic typing speeds in
excess of the line/character rate.

3.4.7.2 Line Mode - Data originating at the keyboard is routed directly
to the display memory for storage and later transmission. Data is
transferred from the display memory to the interface upon operator
entry into memory of the carriage return code. Data is transferred
to the remote device from the beginning of the current line to the
first carriage return code position. Upon encountering the carriage
return code in memory, the CR code is transmitted by the interface,
transmission is terminated, and the cursor is reset to the beginning
of the current line.

Data received during the transmit operation will be ignored with the
exception of a break condition. Receipt of a break will cause the
terminal to abort the transmission at the current cursor position.

The keyboard is disabled during line transmission and the KEYBOARD
LOCK indicator lit.

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3.4.7.3 Block Mode - Data entry, via the keyboard, is stored in memory for later transmission. A transmit operation is initiated by pressing the SEND key. Data transmission takes place from the first previous STX code {to the left of the current cursor position or above the current line} to the first termination code following that STX code. The termination code may be selected as an ETX and/or EOT code via an internal switch. If an STX code is not present between the cursor position and the first character position of the first line {beginning of page} the transmission will take place from the beginning of page. STX codes that may be present following the current cursor position are transmitted as data characters if encountered prior to a termination code or end of page. If a termination code is not present between the message starting point and the end of page {last character position of the last line}, the transmission will terminate at the end of page and the cursor will be placed in the last character position of the last line following transmission. The page will not scroll.

The keyboard is disabled during the transmission and the KEYBOARD LOCK indicator lit.

The termination code may be transmitted in the data stream or disabled from transmission, as determined by the position of an internal switch.

Pressing of a backspace, clear or line feed key will perform the described function. Pressing the backspace, clear or line feed key in conjunction with the CONTROL key will enter the representative code in memory at the cursor position. The cursor will advance one position to the right.

3.4.8 EVEN PAR/NO/ODD PAR Switch - A three-position switch which selects either Even, Odd, or No parity. The terminal will test incoming data or generate parity for transmitted data as per the setting of this switch. When in the NO position, the internal Mark/Space switch will determine the signal level of the parity bit transmitted. Bit 2^7 in the transmitted word will be set as selected by this switch. Incoming data is checked as selected. Incorrect parity will cause the terminal to display a parity error symbol {all dot positions in a 5- by 7-dot matrix unblanked} in the error position. If retransmitted as stored, the character transmitted in place of a received character error will be a DEL {177_8} code. Received data parity is not checked when space or mark parity is selected.

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3.4.9 FORMAT Switch - A two-position rocker switch that allows the oper-
ator to disable the keyboard. If the switch is positioned to FORMAT,
the keyboard is disabled with the exception of the peripheral mode
controls. The KEYBOARD LOCK indicator will be lit. The terminal is
returned to full operation when the switch is in the alternate position.

Use of the switch with the edit option installed allows for selection
of either format or block mode. Refer to the paragraph entitled
Edit Option for a description of format mode.

3.4.10 ALERT Indicator - The ALERT indicator is mounted on the front panel.

The ALERT indicator lights upon receipt of a break condition at the
modem interface.

The ALERT indicator is also used to indicate terminal operating con-
dition in test mode. Refer to Test/Normal switch in the Requirements
section of this specification. The ALERT indicator may also be lit
as required by the multidrop option.

Any received data that contains a space condition as the 10th bit is
interpreted as a break condition, and results in the keyboard being
disabled and the ALERT and KEYBOARD LOCK indicators lighting.

The terminal may utilize the loss of Secondary Received Line Signal
Detector as a break indication. An internal switch is provided to
allow use of this feature. Reference Internal Switches later in
this specification.

The keyboard may be unlocked and the respective indicators extinguished
by actuating the BREAK key. A break condition is not transmitted
when the BREAK key is used in this manner.

3.4.11 Basic Communications Status Indicators - Two status indicators are
provided to indicate the presence or absence of signals required for
reliable telecommunications. These signals relate to the modem inter-
face only.

3.4.11.1 CO Indicator {Carrier On} - Indicates, when lit, the presence of
the Receive Carrier and Data Set Ready signals required to allow data
entry from a distant station. Absence of either signal will cause the
indicator to be extinguished and the Receive Data signal to be ignored.

3.4.11.2 CTS Indicator {Clear to Send} - Indicates, when lit, that the
modem has activated the transmit carrier and is ready to accept data
from the terminal for subsequent modulation and transmission. If
Clear to Send is not present, the terminal will not transmit data to
the modem.

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3.4.12 Additional Communications Status Indicators - Provision for four status indicators is included to indicate the presence or absence of signals required for reliable telecommunications. These signals relate to the modem interface only and are provided as a standard feature.

3.4.12.1 RTS Indicator {Request to Send} - Indicates, when lit, that the terminal is conditioned to transmit.

3.4.12.2 DTR Indicator {Data Terminal Ready} - Indicates, when lit, that the terminal is conditioned to accept data from the modem. If extinguished, any data presented to the terminal from the modem will be disregarded.

3.4.12.3 REC DATA Indicator {Receive Data} - Indicates the presence of data as transferred from the modem.

3.4.12.4 TRANS DATA Indicator {Transmit Data} - Indicates, when lit, that data is being transferred to the modem.

3.4.13 TRANSMISSION MODE Indicators - Labeled CHAR, LINE, and BLOCK, these indicators indicate the position of the CHARACTER/LINE/BLOCK switch.

3.4.14 KEYBOARD LOCK Indicator - Indicates, when lit, that the keyboard, with the exception of the peripheral control keys, is disabled. The following conditions will cause the keyboard to be disabled:

- When in block mode, receipt of an STX will disable the keyboard until such time as a termination code is received {ETX or EOT}.

- The keyboard is disabled during the transfer of data from the display memory to an external device.

- Receipt of a break condition or framing error {10th bit received as a space condition}.

- Additional conditions may be established for KEYBOARD LOCK with the addition of the multidrop option to either terminal.

3.4.15 FORMAT MODE Indicator - The FORMAT MODE indicator applies to the edit option only and is lit when the terminal is placed in format mode {FORMAT switch in FORMAT position}. Refer to the paragraph entitled Edit Option for a description of this indicator.

3.4.16 MASTER CLEAR Switch - Located on the rear panel, this switch is a momentary contact pushbutton. When actuated, the MASTER CLEAR switch will return the terminal to the initial condition and clear the display memory.

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3.4.17 TEST/NORMAL Switch - Located on the rear panel, the TEST/NORMAL switch is a two-position slide switch. To enter test mode, the slide switch must be placed in the TEST position and the MASTER CLEAR switch momentarily actuated. To reenter normal mode, the TEST/NORMAL switch must be placed in the NORMAL position and the MASTER CLEAR switch momentarily actuated.

While in test mode, terminal operation is local only.

Test mode is designed to provide a means for the operator to test the operation of the terminal without elaborate test facilities. It is intended to establish a high degree of confidence in the operational status of the terminal and is not intended to perform fault isolation below the terminal level.

Test mode is divided into eight sections as detailed in the following paragraphs.

3.4.17.1 Test 0, Checksum - Entry into Test 0 is accomplished upon actuation of the MASTER CLEAR switch {rear panel} or upon initial application of power when in test mode.

It is the intent of this test to ascertain the display terminal internal program coding is as intended. The test is performed by comparing the sum of 256-byte segments of the program with a stored sum in the test routine.

3.4.17.2 Test 1, RAM Check - Entry into Test 1 takes place upon exiting Test 0.

It is the intent of this test to ascertain the proper operation of the display terminal's random-access read/write memory. The test consists of loading the RAM memory {full page} with each of the 256 possible characters, in sequence, and checking {reading} each location to ensure the intended character was stored.

3.4.17.3 Test 2, Pattern and I/O - Entry into Test 2 takes place upon exiting Test 1.

It is the intent of this test to ascertain proper operation of the read/write memory when a shifting pattern is stored, and to ascertain proper operation of the transmit and receive data logic.

3.4.17.4 Test 3, Keyboard Data Entry - Entry into Test 3 takes place upon exiting Test 2.

It is the intent of this test to ascertain proper keyboard operation. Operation of this test requires that the operator actuate each key on the keyboard. As any key is actuated, the display terminal will input the data character received from the keyboard into every location of the display memory.

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PIN NUMBER	CCITT	EIA	SIGNAL NAME	ORIGIN
1	101	AA	Protective Ground	Modem/Terminal
2	103	BA	Transmitted Data	Terminal
3	104	BB	Received Data	Modem
4	105	CA	Request to Send {RTS}	Terminal
5	106	CB	Clear to Send {CTS}	Modem
6	107	CC	Data Set Ready {DSR}	Modem
7	102	AB	Signal Ground	Modem/Terminal
8	109	CF	Received Line Signal Detector {CO}	Modem
9			Unused	
10			Unused	
11			Unused	
12	122	SCF	Secondary Received Line Signal Detector {SCO}	Modem
13	121	SCB	Secondary Clear to Send {SCTS}	Not Used
14	118	SBA	Secondary Transmitted Data	Not Used
15	114	DB	Transmission Signal Element Timing	Not Used
16	119	SBB	Secondary Received Data	Not Used
17	115	DD	Receiver Signal Element Timing	Not Used
18			Unused	
19	120	SCA	Secondary Request to Send {SRTS}	Terminal
20	108.2	CD	Data Terminal Ready {DTR}	Terminal
21	110	CG	Signal Quality Detector	Not Used
22	125	CE	Ring Indicator	Not Used
23	111/112	CH/CI	Data Signal Rate Selector	Not Used
24	113	DA	Transmit Signal Element Timing	Not Used
25			Unused	

Table 4 - Interface Circuit Assignments

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3.4.17.5   Test 4 - Reserved.

3.4.17.6   Test 5 - Reserved.

3.4.17.7   Test 6, Printer Test - Entry into Test 6 takes place upon exiting Test 3 with a printer present and ready, the printer option installed, and the PRINT ON LINE key actuated. If any of these conditions are not satisfied, the test will be bypassed.

It is the intent of this test to ascertain the proper operation of the printer control option and the printer.

3.4.17.8   Test 7, Terminal Configuration - Entry into Test 7 takes place upon exiting Test 6.

This test is provided to assure proper setting of certain internal and external switches and to check for the presence of installed options.

3.4.18   CB1 {Circuit Breaker} - Primary and secondary power overload protection is accomplished in this terminal through the use of a circuit breaker located on the rear panel. The circuit breaker is rated at 3.5 amps for those terminals manufactured for use on 102-V ac to 127-V ac. A circuit breaker rated at 2.0 amps is provided for those terminals manufactured for use on 195-V ac to 268-V ac.

3.4.19   INPUT VOLTAGE RANGE SWITCH - This switch is provided on those terminals manufactured for use on 195 to 268-V ac, primary power only. If line voltage, as measured at the terminal input, may vary between 195 and 246-V ac, the INPUT VOLTAGE RANGE SWITCH must be in the LOW LINE position. If line voltage may vary between 216 and 268-V ac, the INPUT VOLTAGE RANGE SWITCH must be in the NORMAL position.

3.4.20   Keyboard Connector - Located at the front of the terminal, this connector provides all voltages and control signals necessary for keyboard operation. The connector is also the data input point from the keyboard assembly.

3.4.21   DATA SET CONNECTOR - Located on the rear panel, this connector is the interface point to the external communications equipment.

3.4.21.1   Physical and Electrical Requirements - The interface signals conform to EIA Standard RS-232-C and CCITT Recommendation V.24 as applied to asynchronous telecommunications.

The interface circuit assignments and origins are listed in Table 4.

The connector used is equivalent to ITT, Cannon DBC-25S.

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3.4.21.2 Functional Requirements

3.4.21.2.1 Protective Ground - This conductor is electrically connected to the terminal frame and to the power source protective ground through the terminal ac power system.

3.4.21.2.2 Transmitted Data - The Transmitted Data circuit is used to transfer data from the terminal to the modem. Data is transmitted as a 10- or 11-bit serial word. In the order of transmission, the data word contains a start bit (spacing), data bits 2^0 through 2^6, a parity bit and one or two stop bits (marking). At 110 baud, the transmitted word contains 11 bits. At all other baud rates the transmitted word contains 10 bits. Rate of transmission is determined by internal selector switches and an external HIGH RATE/300/LOW RATE switch.

Within the field created by the start and stop bits, a marking condition is provided for a binary one indication and a spacing condition is provided as binary zero indication.

3.4.21.2.3 Received Data - The Received Data circuit is used to transfer data from the modem to the terminal. The received data word must contain, in the order of reception, a start bit (spacing), data bits 2^0 through 2^6, a parity bit, and a stop bit (marking). Data must be presented to the terminal at a rate identical to the data rate selected for transmitted data.

Within the field created by the start and stop bits, a marking condition is interpreted as a binary one and a spacing condition is interpreted as a binary zero.

3.4.21.2.4 Request to Send (RTS) - The Request to Send signal line is switched to the on condition by the terminal to initiate a transmit operation. Request to Send is disabled unless Data Set Ready and Data Terminal Ready are on. An internal switch is provided to maintain Request to Send in the on condition whenever Data Terminal Ready and Data Set Ready are on. Or, in the alternate position, allow Request to Send to be switched off during periods of no outgoing traffic. Request to Send remains on for a minimum of 1 millisecond following the transmission of the last data bit.

3.4.21.2.5 Clear to Send (CTS) - The Clear to Send signal line is expected to be switched to the on condition by the modem in response to the Request to Send signal being switched to the on condition by the terminal. The terminal immediately begins transmitting data upon receipt of the Clear to Send signal.

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3.4.21.2.6 <u>Data Set Ready</u> {DSR} - This signal line, when on, indicates the modem is in the data mode. Data will not be transmitted, nor will the Received Data line be monitored, if Data Set Ready is off.

3.4.21.2.7 Signal Ground - Signal ground establishes the common ground reference potential for the control and data circuits.

3.4.21.2.8 Received Line Signal Detector {<u>Carrier On</u>} - The Received Line Signal Detector is provided to the terminal from the modem to indicate the presence or absence of a received carrier. If the Signal Detector signal line is off, the Received Data line is ignored.

3.4.21.2.9 Secondary Received Line Signal Detector {SC} - The Secondary Received Line Signal Detector provides for circuit assurance during character, block, or line transmissions. If an off condition occurs during the process of a transmission, the terminal interprets this as a lost or aborted connection and terminates transmission. The keyboard is disabled and the ALERT indicator lights. The operator may release the keyboard and extinguish the indicator by actuating the BREAK key.

This feature is enabled via an internal switch.

3.4.21.2.10 Secondary Request to Send {SRTS} - The terminal maintains this circuit in an on condition at all times with the following exceptions:

- During block or line transmissions, the Secondary Request to Send signal is switched to the Off condition for the period that the Request to Send is in the on condition.

- The Secondary Request to Send is switched to the off condition for 240 milliseconds following the actuation of the BREAK key unless the key is actuated while the keyboard is disabled.

- Data Terminal Ready is conditioned to off.

- Data Set Ready is conditioned to off.

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3.4.21.2.11 <u>Data Terminal Ready (DTR)</u> - The Data Terminal Ready circuit is maintained in the on condition when power is applied to the terminal with the following exceptions:

● The Data Terminal Ready circuit is switched to the off condition when the terminal is placed in local mode unless an associated peripheral equipment is online.

● If the EOT disconnect feature is enabled, receipt of an EOT code (004_8) causes the Data Terminal Ready circuit to be switched to the off condition for a minimum of 50 milliseconds. Once Data Set Ready is off, Data Terminal Ready is returned to an on condition within 100 milliseconds. If Data Set Ready is never conditioned to off, Data Terminal Ready will not return to an on condition until data transmission is initiated.

3.4.22 PERIPHERAL CONNECTOR - Located on the rear panel, this connector provides a means of interfacing to the tape cassette and an RS-232-C compatible receive-only printer.

The connector used is equivalent in operation, to ITT, Cannon DBC-25S.

Explanation of the circuits and the functional characteristics of the interface may be found in the printer control specification.

3.5 Internal Switches - All internal switches are mounted on printed circuit cards located in the logic card rack assembly. A printed decal is provided inside the terminal indicating the location and function of each of these switches.

3.5.1 <u>REQUEST TO SEND SWITCHED/CONSTANT Switch</u> - When activated, this switch causes the Request to Send signal to be on whenever Data Set Ready and Data Terminal Ready are on.

In the CONSTANT position, Request to Send operates as follows:

● Character Mode, half duplex - Request to Send is on with the first keystroke and is switched off a minimum of 1 millisecond following transmission of a CR code (015_8), or by actuating the BREAK key on the keyboard.

● Special Operation - In this mode, the operator may specify up to four specific delimiter codes from columns 0 through 7 of ANSI X 3.4 - 1973 to terminate the RTS signal. These codes are specified by the operator by placing the terminal in character mode. The operator then must press the SEND key followed by four other key operations. It should be noted that to enter any code from columns 0 and 1 of Table 6, the control key, in conjunction with a specific alphanumeric key, must be used. To enter any code from columns 2 through 7 of Table 5, the alphanumeric key or the shift key in conjunction with a specific alphanumeric key must be used. If less than four special delimiters are desired, the four key operations still must be preformed to complete the sequence.

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After the special operation has been performed to enter the delimiter characters, the RTS signal is initiated on the first keystroke and removed at least one millisecond after the transmission of one of the special delimiter codes.

This operation has no effect on the data received from the Higher Level Processor. Each control code received will be processed as shown in Table 8 of this specification.

● Termination - If terminal power is removed {on/off switch} or the terminal is master cleared {via the MC switch on the rear panel, the CR code becomes the only delimiter as indicated in Character mode, half duplex above. After a power off or master clear, the operator must perform the actions described in Special Operation above.

● Character mode, full duplex - Request to Send is on with the first keystroke and is switched off following activation of local mode, master clear, line, or block mode.

● Line or block mode - Request to Send is switched on upon pressing the CR key in line mode, or the SEND key in block mode.

Request to Send remains on during transmission of the message. Request to Send is switched off a minimum of 1 millisecond following transmission of the last bit in the message. A block or line transmission may be terminated, and therefore Request to Send switched off by any of the following actions:

● Actuation of the BREAK key

● Master clear

● Power removal

● Actuation of LOCAL mode switch

3.5.2 MARK/SPACE PARITY Switch - This switch in combination with the front panel switch, ODD PAR/NO/EVEN PAR, selects mark or space parity for transmitted data when the front panel switch is in the NO position. Bit 2^7 of the transmitted data word will be set to the signal level selected by the MARK/SPACE switch. Received data parity is not checked when the MARK/SPACE switch is selected.

3.5.3 CONSTANT DATA TERMINAL READY Switch - When in the enable position, this switch causes the terminal to maintain the Data Terminal Ready signal on whenever primary ac power is applied to the terminal, except as dictated by the EOT disconnect feature. When in the disabled position, the Data Terminal Ready signal will be conditioned off when all ON LINE/LOCAL switches {terminal and options} are conditioned to LOCAL.

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3.5.4 EOT DISCONNECT ENABLE/DISABLE Switch - If this switch is activated, receipt of an EOT {004_8} code causes the Data Terminal Ready circuit to be switched to the off condition for a minimum period of 50 milliseconds. Once Data Set Ready is switched off, Data Terminal Ready is switched on within 100 milliseconds. If Data Set Ready is never conditioned to off, Data Terminal Ready will not return to an on condition until data transmission is initiated.

If this switch is deactivated, the receipt of an EOT code has no effect on the Data Terminal Ready circuit.

3.5.5 BAUD RATE Selector Switches - The BAUD RATE SELECTOR switches are a block of eight rocker switches. As indicated by the internal decal, the four switches designated LOW control the terminal line speed when the external HIGH RATE/300/LOW RATE switch is in the LOW RATE position. The remaining four rocker switches, designated HIGH, control the terminal line speed when the external HIGH RATE/300/LOW RATE switch is in the HIGH RATE position.

Any one of ten baud rates may be selected in either the HIGH or LOW switch positions. The designations HIGH and LOW are for convenience only. An identical or higher baud rate can be selected for the LOW position as relating to the HIGH position.

Baud rates that may be selected are 110 baud, 150 baud, 200 baud, 300 baud, 600 baud, 1200 baud, 1800 baud, 2400 baud, 4800 baud, and 9600 baud.

Operating speed is selected from a crystal-controlled oscillator, accurate within ±0.2 percent per bit.

3.5.6 ENABLE ETX TERMINATION Switch - This switch applies to the operation of the terminal in block mode only. If activated, this switch causes the termination of block transfer to occur upon encountering an ETX {003_8} code in the transmit data stream. In the alternate position, transmission of an ETX has no effect on the block transfer.

3.5.7 ENABLE EOT TERMINATION Switch - This switch applies to the operation of the terminal in block mode only. If activated, this switch causes the termination of block transfer to occur upon encountering an EOT {004_8} code in the transmit data stream. In the alternate position, transmission of an EOT has no effect on the block transfer.

3.5.8 ENABLE TRANSFER TERMINATION CODE Switch - This switch applies to the operation of the terminal in block mode only. If enabled, this switch will allow transmission of the termination code selected as defined in this specification.

In the alternate position, transmission of the termination code is disabled and the block transfer operation is terminated following the transfer of the character preceding the termination code.

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3.5.9 BATCH MODE Switch - If the BATCH MODE switch is positioned to enable, the terminal will be maintained in character mode, online, and full duplex regardless of the positioning of the front panel switches. The scroll feature is disabled regardless of the position of the SCROLL ENABLE/DISABLE switch.

3.5.10 ENABLE COMMUNICATIONS CIRCUIT ASSURANCE FEATURE Switch - This two-position switch allows for the use of the secondary channel carrier as a means to interrupt data transmission either to or from the terminal.

If this switch is placed in the ENABLE position, the Secondary Received Line Signal Detector will be monitored during any transmit operation. If an off condition occurs on this circuit, the transmit operation will be terminated, the Request to Send circuit conditioned to off, Secondary Request to Send conditioned to on, the ALERT and KEYBOARD LOCK indicators illuminated, and the keyboard disabled. The keyboard may be enabled, and the indicators extinguished, by actuating the BREAK key. A break signal is not transmitted.

Secondary Request to Send is maintained in the on condition during periods of no transmit activity. This circuit is switched to an off condition for a minimum of 240 milliseconds upon actuation of the BREAK key.

If the switch is in the DISABLE position, the terminal will not respond to a loss of carrier on the secondary channel.

3.5.11 SELECT BACKGROUND CHARACTER Switch - This switch allows for the selection of either a 040_8 or 000_8 code as the background fill character inserted in memory during a clear operation. If the 040_8 code is selected, the terminal will transmit all codes as stored, including the 040_8 code, except as modified by protected fields and delimiter codes such as CR, STX, ETX, and EOT.

If the terminal is conditioned to insert 000_8 codes during a clear operation, all codes except the 000_8 code are transmitted as stored, except as modified by protected fields and delimiter codes such as CR, STX, ETX, and EOT. If in format mode and a protected field is encountered during a transmit operation {edit option installed} an HT {011_8} code is automatically inserted into the data stream in place of the protected field. If the terminal is conditioned to block mode, the X-Y coordinates of each SO {016_8} and ETB {027_8} will automatically be transmitted if encountered during a transmit operation if the X-Y positioning feature is enabled. When an SO code is encountered, an ESC {033_8} followed by 061_8 {numeric 1} and two data words representing the X-Y coordinates of the SO and ETB codes, are inserted prior to the transmission of the respective code.

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3.5.12 SCROLL ENABLE/DISABLE Switch - If the SCROLL ENABLE/DISABLE switch
is in the ENABLE position, data entry or cursor movement that causes
the cursor to be placed in the next line while the cursor is in the
bottom or last line of the display area, causes the page to scroll.
A scroll operation causes all lines of displayed data to be repositioned
to the line position immediately above the current position of display.
The top, or first, display line is lost; a cleared line appears in the
last line position. The cursor remains on that line unless repositioned
through the use of the cursor up { } key or backspace { } key.

The cursor home position is defined as the first character position of
the last line.

If the SCROLL ENABLE/DISABLE switch is in the DISABLE position, data
entry or cursor movement that causes the cursor to be placed in the
next line, while the cursor is in the last line, causes the cursor
to be repositioned to the first line of the display area.

The home position is defined as the first character position of the
first line.

Operation of this switch applies to block mode only. The terminal
maintains scroll mode when operating in character or line modes regard-
less of the position of this switch.

With the edit option installed, operation of the terminal in format
mode overrides this switch and causes the scroll feature to be
disabled. The scroll feature will not be enabled in response to
externally sourced data that would otherwise cause the terminal to
exit format mode.

3.6 Coding Requirements - The display terminal has the capability to generate
and recognize 128 discrete codes. The basic device allows for the stor-
age and display of the 95 alphanumeric characters recommended under
ASCII X3.4-1968 as shown in Table 5.

Where applicable, control character definitions also comply with
ASCII X3.4, but variations are made available to augment external
control of display terminal functions. Control coding is shown
in Table 6.

3.6.1 Alphanumeric Characters - As shown in Table 5, octal codes 040_8 through
176_8, when received at the interface or generated by the keyboard,
results in the indicated character being displayed. Provision is made,
via an external switch, for disabling the generation of octal codes
140_8 through 176_8. If, however, a code within this subset is received
by the terminal from an external device, the character assigned to that
code will be displayed as shown in Table 5.

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b7→ b6→ b5→					0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4	b_3	b_2	b_1	COLUMN→ / ROW↓	2	3	4	5	6	7
0	0	0	0	0	SP	0	@	P	`	p
0	0	0	1	1	!	1	A	Q	a	q
0	0	1	0	2	"	2	B	R	b	r
0	0	1	1	3	#	3	C	S	c	s
0	1	0	0	4	$	4	D	T	d	t
0	1	0	1	5	%	5	E	U	e	u
0	1	1	0	6	&	6	F	V	f	v
0	1	1	1	7	´	7	G	W	g	w
1	0	0	0	8	(	8	H	X	h	x
1	0	0	1	9	)	9	I	Y	i	y
1	0	1	0	10	*	:	J	Z	j	z
1	0	1	1	11	+	;	K	[	k	{
1	1	0	0	12	,	<	L	\	l	¦
1	1	0	1	13	–	=	M	]	m	}
1	1	1	0	14	.	>	N	^	n	~
1	1	1	1	15	/	?	O	___	o	

Table 5 – Alphanumeric Character Codes

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Bits				COLUMN / ROW	0 0 0 — 0	0 0 1 — 1	1 1 1 — 7
b4	b3	b2	b1				
0	0	0	0	0	NUL	DLE	
0	0	0	1	1	SOH	DC1	
0	0	1	0	2	STX	DC2	
0	0	1	1	3	ETX	DC3	
0	1	0	0	4	EOT	DC4	
0	1	0	1	5	ENQ	NAK	
0	1	1	0	6	ACK	SYN	
0	1	1	1	7	BEL	ETB	
1	0	0	0	8	BS	CAN	
1	0	0	1	9	HT	EM	
1	0	1	0	10	LF	SUB	
1	0	1	1	11	VT	ESC	
1	1	0	0	12	FF	FS	
1	1	0	1	13	CR	GS	
1	1	1	0	14	SO	RS	
1	1	1	1	15	SI	US	DEL

Table 6 - Control Character Codes

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3.6.2 Control Characters - All control characters may be generated by the keyboard for immediate transmission or stored in the display memory for later transmission. When stored, the control codes will appear as blanks unless the CONTROL key is pressed; see Table 3 for the symbol assignments. When received at the interface, these codes are treated as idle characters or will perform specific functions as indicated in Table 7. An idle code is not stored when received at the interface.

3.7 Alphanumeric Keyboard - The terminal keyboard provides for operator entry of specific symbol and control codes which are displayed or transmitted as directed by the FULL DUPLEX/HALF DUPLEX, or CHARACTER/LINE/BLOCK switches. Terminal and peripheral function keys are provided in addition to the alphanumeric and control code entry keys. Operation of the function keys is modified by the presence or absence of peripherals and by the operating mode of the terminal.

The keyboard and key locations are shown in Figures 7 and 8.

Codes and functions generated by the keyboard are shown in Table 8. Code and function assignments shown in this table refer to the code entered, or functions performed, in block mode. Variations in function operation or code entry are outlined in the following text.

Key location numbers shown in Table 8 refer to the key number assignments shown in Figure 8. The key number assignments are arbitrary.

3.7.1 Alphanumeric and Control Code Entry - Actuation of any of the alphanumeric symbol or control code keys causes the code for that key to be transferred to the terminal control logic. The keyboard has "N" key rollover capability; codes are transmitted as each key is actuated regardless of the state of the remaining keys.

The keyboard is a three-level device - i.e., 1st level, key only (lowercase); 2nd level, key and SHIFT (uppercase); 3rd level, key and CONTROL or key, SHIFT, and CONTROL actuated (control characters).

An external switch (64 CHAR/96 CHAR) is provided to disable the generation of codes 140_8 through 176_8. If this switch is in the 64-CHARacter position, uppercase characters are generated in level 1 in place of the lowercase characters.

3.7.1.1 SHIFT Keys - When two symbols share a key the upper symbol or control function is active only while one of the two SHIFT keys or the SHIFT LOCK key is actuated. Symbols shaded in yellow, and lowercase alpha characters, are disabled when the 96/64 CHAR(acter) switch is in the 64 position.

Actuating the SHIFT key in conjunction with a key labeled with a single legend, or with a function text above the legend, causes the transmission of the uppercase code for the symbol indicated on the key.

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ASCII DESIGNA-TION	OCTAL CODE	TERMINAL OPERATION WHEN RECEIVED IN		
		CHAR/LINE MODES	BLOCK MODE	FORMAT MODE
NUL	000	Idle	Idle	Idle
SOH	001	Idle	Idle	Idle
STX	002	Idle	Store in memory	Store in memory (Exit Format Mode)
ETX	003	Idle	Store in memory	Store in memory
EOT	004	Idle or Disconnect	Idle or Disconnect	Idle or Disconnect
ENQ	005	Idle or Answerback	Idle or Answerback	Idle or Answerback
ACK	006	Idle	Idle	Idle
BEL	007	Audible alarm actuated for 200 to 250 milli-seconds	Audible alarm actuated for 200 to 250 milli-seconds	Audible alarm actuated for 200 to 250 milli-seconds
BS	010	Backspace	Backspace	Backspace
HT	011	Idle	Basic Terminal - Idle; Edit Option Installed - Tab to end tab character	Tab to end tab character
LF	012	Line Feed	Line Feed	New Line
VT	013	Idle	Idle	Idle
FF	014	Idle	Idle	Idle
CR	015	Carriage Return	Store, and Carriage Return	Store, and Carriage Return
SO	016	Basic Terminal - Idle; Highlight Installed - Begin reduced intensity	Basic Terminal - Idle; Highlight Installed - Begin reduced intensity	Idle
SI	017	Basic Terminal - Idle; Highlight Installed - Store, End Tab, Reduced Intensity, or Blink	Basic Terminal - Idle; Highlight Installed - Store, End Tab, Reduced Intensity, or Blink	Store, End Tab Protect
DLE	020	Idle	Idle	Idle

Table 7 - Control Character Functions

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ASCII DESIGNA-TION	OCTAL CODE	TERMINAL OPERATION WHEN RECEIVED IN		
		CHAR/LINE MODES	BLOCK MODE	FORMAT MODE
DC1	021	Idle	Idle	Idle
DC2	022	Idle	Idle	Idle
DC3	023	Idle	Idle	Idle
DC4	024	Idle	Idle	Idle
NAK	025	Skip {→}	Skip {→}	Skip {→}
SYN	026	Idle	Idle	Idle
ETB	027	Basic Terminal - Idle; Highlight Installed - Store, Initiate Blink Field	Basic Terminal - Idle; Highlight Installed - Store, Initiate Blink Field	Idle
CAN	030	Clear Screen	Clear Screen	Clear Screen
EM	031	Reset	Reset	Reset
SUB	032	Cursor Up {↑}	Cursor Up {↑}	Cursor Up {↑}
ESC	033	Idle	Basic Terminal - Idle; Edit Option Installed - Idle or Enable X-Y Position	Basic Terminal - Idle; Edit Option Installed - Idle or Enable X-Y Position
FS	034	Idle	Idle	Idle
GS	035	Idle	Idle	Idle
RS	036	Idle	Idle	Idle
US	037	Idle	Idle	Idle
DEL	177	Idle	Idle	Idle

Table 7 - Control Character Functions {Contd}

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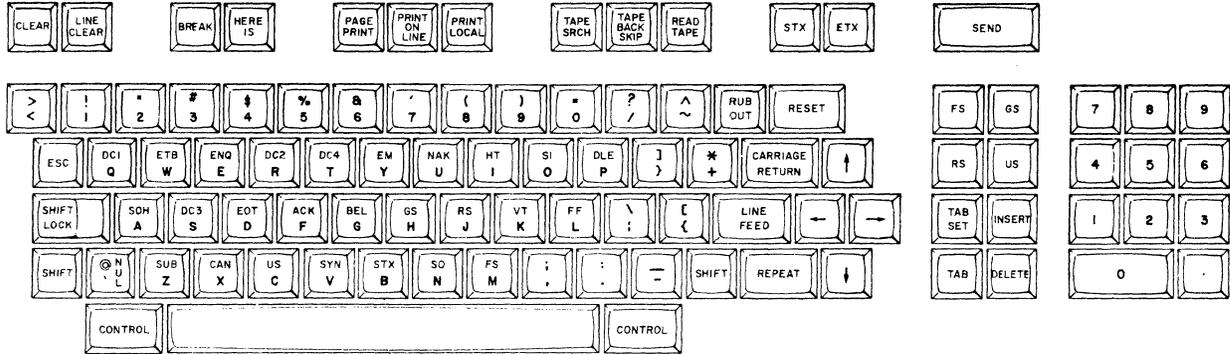
Figure 7 - Display Terminal Keyboard
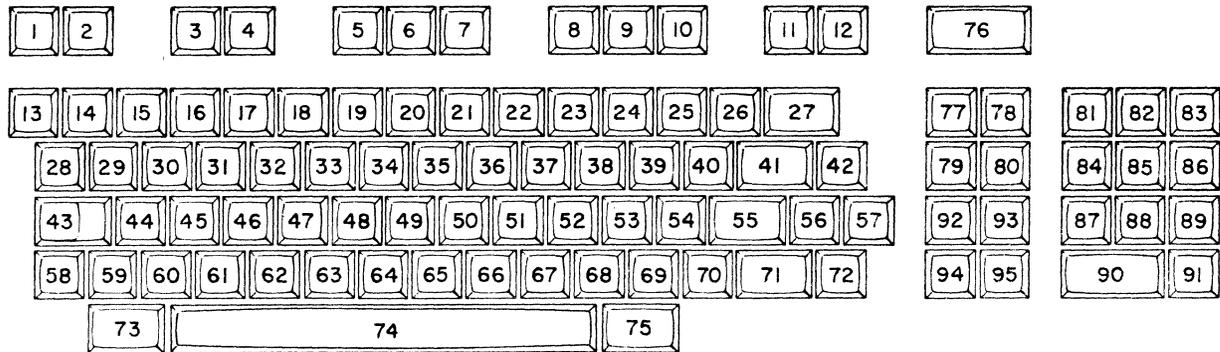
Figure 8 - Key Locations

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KEY NUMBER*	LEVEL 1** SYMBOL/FUNCTION OCTAL CODE		LEVEL 2** SYMBOL/FUNCTION OCTAL CODE		LEVEL 3** SYMBOL/FUNCTION OCTAL CODE	
1	Clear		Clear		CAN	030
2	Line Clear		Line Clear		Line Clear	
3	Break		Break		Break	
4	Here Is		Here Is		Here Is	
5	Page Print		Page Print		Page Print	
6	Print On Line		Print On Line		Print On Line	
7	Print Local		Print Local		Print Local	
8	Tape Search		Tape Search		Tape Search	
9	Tape Backskip		Tape Backskip		Tape Backskip	
10	Read Tape		Read Tape		Read Tape	
11	STX	002	STX	002	STX	002
12	ETX	003	ETX	003	ETX	003
13	<	074	>	076	<	074
14	1	061	!	041	1	061
15	2	062	"	042	2	062
16	3	063	#	043	3	063
17	4	064	$	044	4	064
18	5	065	%	045	5	065
19	6	066	&	046	6	066
20	7	067	'	047	7	067
21	8	070	(	050	8	070
22	9	071	)	051	9	071
23	0	060	=	075	0	060
24	/	057	?	077	/	057
25	~	176	∧	136	~	176

*Refer to Figure 8 for key location
**Level 1 - Key only actuated
   Level 2 - Key and SHIFT actuated
   Level 3 - Code output for both:
       1. Key and CONTROL actuated
       2. Key, SHIFT, and CONTROL

Table 8 - Keyboard Coding

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KEY NUMBER*	LEVEL 1** SYMBOL/FUNCTION	OCTAL CODE	LEVEL 2** SYMBOL/FUNCTION	OCTAL CODE	LEVEL 3** SYMBOL/FUNCTION	OCTAL CODE
26	Rubout	177	Rubout	177	Rubout	177
27	Reset		Reset		Reset	
28	ESC	033	ESC	033	ESC	033
29	q	161	Q	121	DC1	021
30	w	167	W	127	ETB	027
31	e	145	E	105	ENQ	005
32	r	162	R	122	DC2	022
33	t	164	T	124	DC4	024
34	y	171	Y	131	EM	031
35	u	165	U	125	NAK	025
36	i	151	I	111	HT	011
37	o	157	O	117	SI	017
38	p	160	P	120	DLE	020
39	}	175	]	135	}	175
40	+	053	*	052	+	053
41	Carriage Return		Carriage Return		CR	015
42	Cursor Up		Cursor Up		Cursor Up	
43	Shift Lock		Shift Lock		Shift Lock	
44	a	141	A	101	SOH	001
45	s	163	S	123	DC3	023
46	d	144	D	104	EOT	004
47	f	146	F	106	ACK	006
48	g	147	G	107	BEL	007
49	h	150	H	110	GS	035
50	j	152	J	112	RS	036

* Refer to Figure 8 for key location
** Level 1 - Key only actuated
Level 2 - Key and SHIFT actuated
Level 3 - Code output for both:
1. Key and CONTROL actuated
2. Key, SHIFT, and CONTROL

Table 8 - Keyboard Coding (Contd)

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KEY NUMBER⋈	LEVEL 1⋈⋈ SYMBOL/FUNCTION OCTAL CODE		LEVEL 2⋈⋈ SYMBOL/FUNCTION OCTAL CODE		LEVEL 3⋈⋈ SYMBOL/FUNCTION OCTAL CODE	
51	k	153	K	113	VT	013
52	l	154	L	114	FF	014
53	¦	174	\	134	¦	174
54	{	173	[	133	{	173
55	Line Feed		Line Feed		LF	012
56	Backspace		Backspace		BS	010
57	Skip		Skip		Skip	
58	Shift		Shift		Shift	
59	`	140	@	100	NUL	000
60	z	172	Z	132	SUB	032
61	x	170	X	130	CAN	030
62	c	143	C	103	US	037
63	v	166	V	126	SYN	026
64	b	142	B	102	STX	002
65	n	156	N	116	SO	016
66	m	155	M	115	FS	034
67	⌐	054	;	073	⌐	054
68	.	056	:	072	.	056
69	-	055	_	137	-	055
70	Shift		Shift		Shift	
71	Repeat		Repeat		Repeat	
72	Cursor Down		Cursor Down		Cursor Down	
73	Control		Control		Control	
74	Space	040	Space	040	Space	040
75	Control		Control		Control	

⋈ Refer to Figure 8 for key location
⋈⋈ Level 1 - Key only actuated
   Level 2 - Key and SHIFT actuated
   Level 3 - Code output for both:
         1. Key and CONTROL actuated
         2. Key, SHIFT, and CONTROL

Table 8 - Keyboard Coding (Contd)

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KEY NUMBER*	LEVEL 1** SYMBOL/FUNCTION OCTAL CODE		LEVEL 2** SYMBOL/FUNCTION OCTAL CODE		LEVEL 3** SYMBOL/FUNCTION OCTAL CODE	
76	Send		Send		Send	
77	FS	034	FS	034	FS	034
78	GS	035	GS	035	GS	035
79	RS	036	RS	036	RS	036
80	US	037	US	037	US	037
81	7	067	7	067	7	067
82	8	070	8	070	8	070
83	9	071	9	071	9	071
84	4	064	4	064	4	064
85	5	065	5	065	5	065
86	6	066	6	066	6	066
87	1	061	1	061	1	061
88	2	062	2	062	2	062
89	3	063	3	063	3	063
90	0	060	0	060	0	060
91	.	056	.	056	.	056
92	Tab Set	017	SO	016	Tab Set	017
93	Insert Character		Insert Line		Insert Character	
94	Tab		Back Tab		HT	011
95	Delete Character		Delete Line		Delete Character	

*Refer to Figure 8 for key location
**Level 1 – Key only actuated
Level 2 – Key and SHIFT actuated
Level 3 – Code output for both:
    1. Key and CONTROL actuated
    2. Key, SHIFT, and CONTROL

Table 8 - Keyboard Coding (Contd)

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3.7.1.2 CONTROL Keys - Actuation of either CONTROL key in conjunction with any data key or combination of data key and SHIFT key, causes the generation of the codes outlined in Table 8, level 3.

In block or line modes, all function codes generated while actuating the CONTROL key are stored for transfer.

3.7.1.3 ESC {Escape} Key - Actuation of this key causes storage of an 033_8 code in line or block modes, or transmission of an 033_8 code in character mode.

3.7.1.4 RUB OUT Key - Actuation of the RUB OUT key causes storage of a 177_8 code in line or block modes, or transmission of a 177_8 code in character mode.

3.7.1.5 FS, GS, RS and US Keys - Actuation of these keys causes the storage in line or block modes, or transmission in character mode, of the following codes:

$$FS - 034_8$$

$$GS - 035_8$$

$$RS - 036_8$$

$$US - 037_8$$

3.7.1.6 STX Key - Actuation of the STX key causes the storage in line or block modes, or transmission in character mode, of an 002_8 code. Block mode operation allows the use of this code as a message delimiter if stored in memory.

3.7.1.7 ETX Key - Actuation of the ETX key causes the storage in line or block modes, or transmission in character mode, of an 003_8 code. Block mode operation allows the use of this code as a message delimiter if stored in memory.

3.7.2 Special Function Keys

3.7.2.1 BREAK Key - Actuation of this key causes the Transmitted Data signal to be held to a space {logical 0} condition from a minimum of 240 milliseconds to a maximum of 300 milliseconds.

Receipt of a code or condition interpreted as a break signal causes the keyboard to be disabled. Keyboard release is accomplished by actuating the BREAK key. Under these conditions, a break signal is not transmitted.

3.7.2.2 HERE IS Key - The HERE IS key is used in conjunction with the answerback option. Without this option, the key causes no terminal activity. Refer to the Display Terminal Options section of this specification.

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3.7.2.3 SEND Key - Actuation of the SEND key causes the transmission of data stored in memory from the beginning of page; or from the first STX code encountered between the current cursor position and the beginning of page, to the first termination code encountered during transmission; or to the end of page. This key is operative in block or format {edit option installed} modes only.

3.7.2.4 REPEAT Key - A REPEAT key is provided on the terminal keyboard to allow for continued entry of a specific character, or cursor movement at a rate of 15 $\pm$3 characters per second, unless operating the terminal online in character mode. In this case, the repeat rate is limited to the character rate of the communications facility.

Operation of the keyboard requires that the REPEAT key be actuated prior to actuating the key to be repeated.

All keys, with the exception of the alternate-action peripheral control keys, are subject to the repeat operation.

3.7.2.5 PAGE PRINT Key - Actuation of the PAGE PRINT key does not cause terminal activity unless the printer control option is installed. Refer to the Display Terminal Options section of this specification.

3.7.2.6 PRINT ON LINE Key - Actuation of the PRINT ON LINE key does not cause terminal activity unless the printer control option is installed. Refer to the Display Terminal Options section of this specification.

3.7.2.7 PRINT LOCAL Key - Actuation of the PRINT LOCAL key does not cause terminal activity unless the printer control option is installed. Refer to the Display Terminal Options section of this specification.

3.7.2.8 TAPE SRCH Key - Actuation of the TAPE SRCH key does not cause terminal activity unless the cassette control option is installed. Refer to the Display Terminal Options section of this specification.

3.7.2.9 TAPE BACK SKIP Key - Actuation of the TAPE BACK SKIP key does not cause terminal activity unless the cassette control option is installed. Refer to the Display Terminal Options section of this specification.

3.7.2.10 READ TAPE Key - Actuation of the READ TAPE key does not cause terminal activity unless the cassette control option is installed. Refer to the Display Terminal Options section of this specification.

3.7.3 Editing and Cursor Control Keys - Detailed explanations of the controls, and definition variations between character, line, block, and format modes are as follows:

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3.7.3.1 CARRIAGE RETURN Key

1. Character Mode - The carriage return function positions the cursor
    to the beginning of the current line. It is caused by actuating
    the CARRIAGE RETURN key or by receipt of a CR code from an external
    device. Generation of the carriage return function at the key-
    board results in the immediate transmission of a CR code.

2. Line Mode - Actuation of the CARRIAGE RETURN key causes the
    CR code to be entered into memory and the terminal to transmit
    all data contained on the current line to the left of, and
    including, the CR code. The cursor will be positioned in the
    first character location of that line following transmission.
    Receipt of a CR code causes the cursor to be positioned to the
    first character location of the current line. Entry of the
    carriage return into memory, without initiating a transmit oper-
    ation, may be performed by actuating the CONTROL key in conjunction
    with the CARRIAGE RETURN key.

3. Block Mode - Actuation of the CARRIAGE RETURN key causes the cursor
    to be repositioned to the first character position of the next line
    The CR code is inserted into the display memory at the cursor
    position prior to performing the carriage return function.

    Entry of the CR code into memory without causing the carriage
    return function may be performed by actuating the CARRIAGE RETURN
    key in conjunction with the CONTROL key.

    When a CR code is encountered during transmission, the cursor is
    repositioned to the first position of the next line and trans-
    mission continues from that point. The CR code is transmitted
    when encounterd during the transmit operation and an LF code
    {012$_8$} is automatically inserted into the data stream immediately
    following the transmission of each CR code. Data located on the
    line to the right of a CR code is not transmitted. If a CR code
    is encountered in the last display line during transmission, the
    transmit operation is terminated. The cursor will be located in
    the first character position of the first line following terminatio

    Receipt of a CR {015$_8$} code causes the entry of that code into
    the display memory and causes the cursor to be reset to the
    beginning of the current line.

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3.7.3.2   LINE FEED Key

1.   Character Mode - Performing a line feed causes the cursor to be placed in the same relative horizontal position in the line immediately below the current line. Data previously stored in memory is not affected. This is caused by actuation of the LINE FEED key or by receipt of an 012_8 code from an external device. Generation of the line feed function at the keyboard results in the immediate transmission of an 012_8 code.

2.   Line and Block Modes - Performing a line feed causes the cursor to be repositioned to the first character position of the next line. Stored data is not altered. This is caused by actuation of the LINE FEED key. Receipt of an LF (012_8) code causes the cursor to be repositioned to the same relative position in the next line.

The LF code may be entered into memory by actuating the CONTROL key in conjunction with the LINE FEED key. If entered in this manner, the line feed function is not performed.

3.7.3.3   Backspace { ← } Key

1.   Character Mode - Backspacing causes the cursor to be placed in the character position immediately preceding the current cursor position. This is caused by actuation of the Backspace key or receipt of an 010_8 code. Data previously stored in memory is not affected. Generation of the backspace function at the keyboard causes the immediate transmission of an 010_8 code.

2.   Line and Block Modes - Backspacing causes the cursor to be placed in the character position previous to the current cursor position including movement to the end of the previous line. This is caused by actuation of the Backspace key or receipt of an 010_8 code. Data previously stored in memory is not affected. The BS code may be entered into memory by actuating the CONTROL key in conjunction with the Backspace key. When entered in this manner, the backspace function is not performed.

3.7.3.4   CLEAR Key

1.   Character Mode -

Full Duplex -   Will transmit a CAN (030_8) code but not perform the clear function.

Half Duplex -   Will transmit a CAN (030_8) code and perform the clear function as indicated in block and line mode.

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3.7.3.4 CLEAR Key {contd}

2. Line and Block Modes - The clear function enters either a space $\{040_8\}$ or a null $\{000_8\}$ code as determined by the position of an internal switch, in each position of the display memory and repositions the cursor to the home position. This is caused by actuation of the CLEAR key or by receipt of a CAN $\{030_8\}$ code from an external device.

The CAN $\{030_8\}$ code may be entered into the display memory for later transmission by actuating the X key or CLEAR key in conjunction with the CONTROL key. When entered in this manner, a clear function is not performed.

3.7.3.5 LINE CLEAR Key

1. Character Mode - Disabled.

2. Line and Block Modes - The clear function causes the entry of a space $\{040_8\}$ or a null $\{000_8\}$ code, as determined by the position of an internal switch, in the area from, and including, the current cursor position to the end of the current line. The cursor is not moved. This is caused by actuation of the LINE CLEAR key.

3.7.3.6 RESET Key -

1. Character Mode -

Full Duplex - Will transmit an EM $\{031_8\}$ code, but will not perform the reset function.

Half Duplex - Will transmit an EM $\{031_8\}$ code and will perform the reset function as in the line and block mode.

2. Line and Block Modes - A reset function performed with the RESET key causes the cursor to be placed in the home position. Data stored in memory is not affected.

The reset function is caused by actuation of the RESET key or by receipt of an EM $\{031_8\}$ code from an external device. The EM code may be entered into the display terminal memory for later transmission by actuating the Y key in conjunction with the CONTROL key. When entered in this manner, a reset function is not performed.

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3.7.3.7 Skip {→} Key

1. Character Mode - Will transmit a NAK {025$_8$} in both full and half duplex but will perform the skip function in half duplex only.

2. Line and Block Modes - A skip function causes the cursor to be repositioned to the next character position. Stored data is not affected. This is caused by actuation of the Skip key or receipt of a NAK {025$_8$} code from an external device.

3.7.3.8 Cursor Down {↓} Key

1. Character Mode - Will transmit an LF {012$_8$} code in both full and half duplex but will perform a cursor down function in half duplex only.

2. Line and Block Modes - A cursor down function causes the cursor to be repositioned to the next line in the same relative horizontal position. Data stored in memory is not affected. The cursor down function is caused by actuation of the Cursor Down key or receipt of an LF {012$_8$} code from an external device.

3.7.3.9 Cursor Up {↑} Key

1. Character Mode - Will transmit a SUB {032$_8$} in both full and half duplex but will perform the cursor up function in half duplex only.

2. Line and Block Modes - A cursor up function causes the cursor to be repositioned to the same relative horizontal position of the previous line. This is caused by actuation of the Cursor Up key or the receipt of a SUB {032$_8$} from an external device.

   Stored data is not altered.

3.7.3.10 TAB SET Key - The TAB SET key is intended for use with the edit option. A complete description of the tab function and this key is provided in the paragraph entitled Edit Option.

If the edit option is not present in the terminal, actuation of this key will cause the entry, in line or block modes or transmission in character mode, of the SI {017$_8$} code. The SI code is treated as an idle code in character mode and is not entered into the display memory, but is transmitted upon key actuation.

Actuation of the TAB SET key in conjunction with the SHIFT key will cause transmission in character mode, or entry into memory in line or block modes, of the SO {016$_8$} code.

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3.7.4 Expanded Format and Edit Controls - Edit and format controls are provided to accommodate terminal operation with the edit option installed. These controls are labeled INSERT, DELETE and TAB. An operational description of these controls is contained in the paragraph entitled Edit Option. These controls are inoperative unless the edit option is installed.

3.8 Display Terminal Options - This section describes operational options only. Cosmetic changes to the display terminal such as color changes, logos, cable lengths, and character set variations are not included.

3.8.1 Auto Answerback Option - The answerback option adds the capability of automatic identification of the terminal upon receipt of specific coding or actuation of the HERE IS key. The HERE IS key is included in the display terminals. With the addition of this option, the display terminal will transmit a series of up to 21 characters to the modem interface upon receipt of an ENQ (005_8) code from the modem interface or following actuation of the HERE IS key.

A mode switch is provided on the option card that allows the data transferred from the answerback option to be entered into the display memory or to be transferred to the modem interface without local copy. With the mode switch in the MAINT position {local copy enabled}, codes issued by the option that correspond to display functions will be entered into the display memory. The function is not performed; idle codes are stored.

Data received during the transmit cycle is ignored with the exception of a break condition. If a break is received, the answerback sequence is aborted following transmission of the word in process.

3.8.1.1 Answerback Option Encoding - Encoding of the 21 characters is performed by the installation technician through diode insertion/deletion. The delivered option is configured to transfer the following code sequence. Diode positions are provided with high-retention sockets to allow reprogramming as required.

Code	Mnemonic	Code	Mnemonic
015_8	CR	102_8	B
012_8	LF	101_8	A
177_8	DEL	103_8	C
101_8	A	113_8	K
116_8	N	040_8	SPACE
123_8	S	124_8	T
127_8	W	105_8	E
105_8	E	123_8	S
122_8	R	124_8	T
		015_8	CR
		012_8	LF
		177_8	DEL

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This section contains basic logic module operating theory. Information includes general architecture definition, logic functions, and interface definition. See Section 2 for operation controls and for all theory associated with programming logic module operations.

GENERAL ARCHITECTURE

The basic logic module provides the control and operational logic circuits required in a processor-based, display/keyboard, serial interface, communications terminal.

The basic module consists of the minimum amount of functional circuits which allow the terminal using the module to perform: 1) keyboard input, 2) crt display, and 3) RS-232-C/CCITT V.24 type I/O communications. This minimum configuration consists of the following assemblies/circuits.

- Logic chassis assembly

- Memory card assembly

- Display control processor card assembly

- Refresh control card assembly

- + 5v regulator card assembly

Figures 4-1 and 4-2 illustrate/define the module architecture. Both figures show the expandability (accomplished by adding optional function assemblies/circuit cards) of the basic module. The number of option cards depends on the particular application/ usage of the terminal containing the module.

The remainder of this section contains operating theory for the basic module assemblies/ cards only. Each available option is described in a separate publication pertaining to that option only (see Foreword).
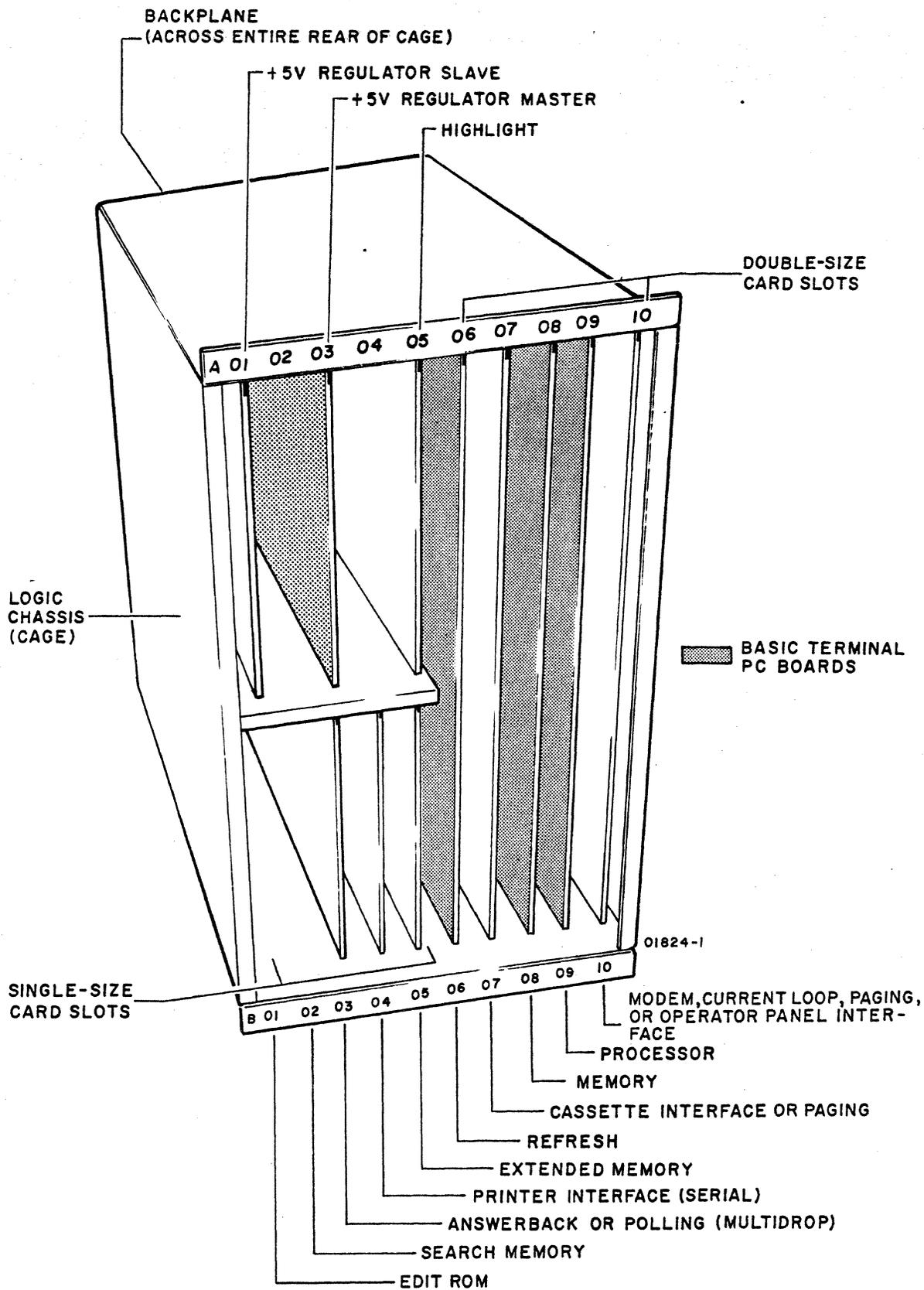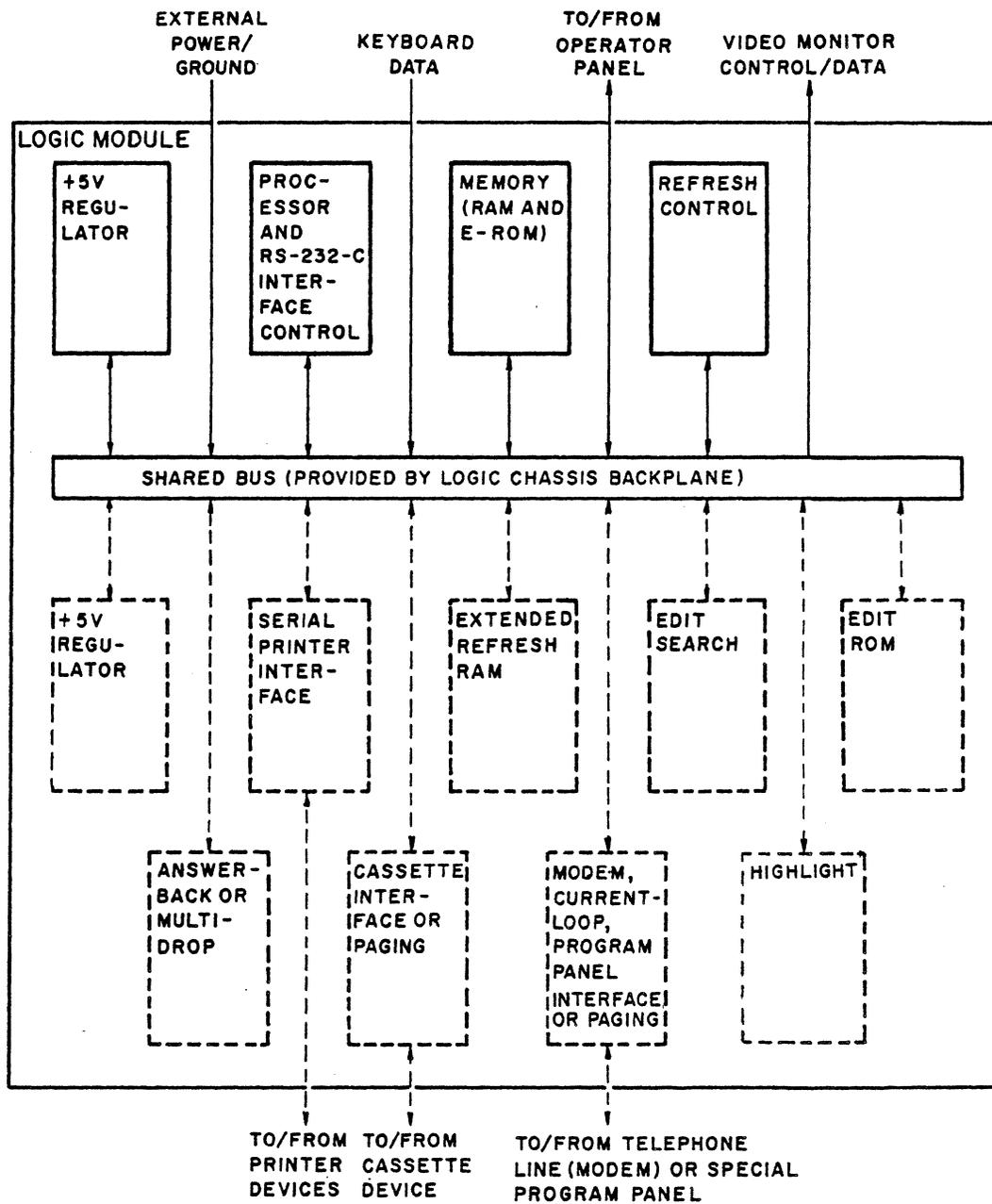
Figure 4-1. Logic Module Physical Architecture

The diagram labels include:

- BACKPLANE (ACROSS ENTIRE REAR OF CAGE)
- +5V REGULATOR SLAVE
- +5V REGULATOR MASTER
- HIGHLIGHT
- DOUBLE-SIZE CARD SLOTS
- LOGIC CHASSIS (CAGE)
- BASIC TERMINAL PC BOARDS
- SINGLE-SIZE CARD SLOTS
- MODEM, CURRENT LOOP, PAGING, OR OPERATOR PANEL INTERFACE
- PROCESSOR
- MEMORY
- CASSETTE INTERFACE OR PAGING
- REFRESH
- EXTENDED MEMORY
- PRINTER INTERFACE (SERIAL)
- ANSWERBACK OR POLLING (MULTIDROP)
- SEARCH MEMORY
- EDIT ROM

Top row slots: A 01 02 03 04 05 06 07 08 09 10

Bottom row slots: B 01 02 03 04 05 06 07 08 09 10

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EXTERNAL
POWER/
GROUND

KEYBOARD
DATA

TO/FROM
OPERATOR
PANEL

VIDEO MONITOR
CONTROL/DATA

LOGIC MODULE

| +5V REGU-LATOR | PROC-ESSOR AND RS-232-C INTER-FACE CONTROL | MEMORY (RAM AND E-ROM) | REFRESH CONTROL |

SHARED BUS (PROVIDED BY LOGIC CHASSIS BACKPLANE)

| +5V REGU-LATOR | SERIAL PRINTER INTER-FACE | EXTENDED REFRESH RAM | EDIT SEARCH | EDIT ROM |

| ANSWER-BACK OR MULTI-DROP | CASSETTE INTER-FACE OR PAGING | MODEM, CURRENT-LOOP, PROGRAM PANEL INTERFACE OR PAGING | HIGHLIGHT |

TO/FROM
PRINTER
DEVICES

TO/FROM
CASSETTE
DEVICE

TO/FROM TELEPHONE
LINE (MODEM) OR SPECIAL
PROGRAM PANEL

NOTE: SOLID LINES SHOW BASIC LOGIC MODULE
FUNCTIONAL SUBASSEMBLIES. BROKEN LINES
SHOW OPTIONAL FUNCTION CARDS.

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Figure 4-2. Logic Module Functional Architecture

BASIC LOGIC MODULE FUNCTIONS

Following paragraphs define the functions provided by the basic logic module. Briefly, these functions are:

- Shared data/control/power bus architecture provided by the logic chassis assembly which houses and interconnects the basic and optional function circuit card assemblies.

- Random-access memory (RAM) for crt refresh character storage and pre-programmed read-only memory (ROM) containing processor sequencing/execution information (control firmware). Both of these memory functions are provided by one double-size circuit card assembly.

- Control processor (controlling element of the shared-bus scheme) provided by one double-size circuit card assembly.

- CRT refresh control provided by one double-size circuit card assembly.

- Regulated + 5v logic circuit power provided by one single-size circuit assembly.

LOGIC CHASSIS FUNCTIONS

The logic chassis houses the slide-in circuit cards. It provides mating connectors for each card intended for placement in the chassis. It includes a backplane which supplies shared-bus and individual circuit paths (via circuit board and/or backplane wire-wrap connections) for all required interconnections between the allowable circuit cards within the chassis. In addition, the connectors which receive circuit cards provide wire-wrap type connector pins for all required I/O signal lines (e.g., to crt, from keyboard, to/from operator's panel, to/from RS-232-C type communication lines, etc.). Figure 4-3 shows placement of the basic and optional card assemblies in the chassis.

4.1 MEMORY CARD FUNCTIONS

Basically, the circuits contained on this card provide: 1) an erasable read-only memory (E-ROM) which is programmed (burned) with a set of nonvolatile 8-bit data words which provide operation execution directions (control firmware) to the processor card circuits, and 2) a random-access memory (RAM) which serves as storage for codes which represent characters displayable on a video monitor. A memory card may contain various sizes of E-ROM storage. A programmed set of 4096_{10}, 8-bit data words of E-ROM storage is required to store execution control information when the edit option is present in the module.

BACKPLANE
(ACROSS ENTIRE REAR OF CAGE)

+5V REGULATOR SLAVE*

+5V REGULATOR MASTER

HIGHLIGHT*

DOUBLE-SIZE
CARD SLOTS

A 01 02 03 04 05 06 07 08 09 10

LOGIC
CHASSIS
(CAGE)

BASIC TERMINAL
PC BOARDS

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SINGLE-SIZE
CARD SLOTS

B 01 02 03 04 05 06 07 08 09 10

MODEM, CURRENT LOOP, PAGING, OR OPERATOR PANEL INTER-FACE*

PROCESSOR

MEMORY

CASSETTE INTERFACE OR PAGING*

REFRESH

EXTENDED MEMORY*

PRINTER INTERFACE (SERIAL)*

ANSWERBACK OR POLLING (MULTIDROP)*

SEARCH MEMORY*

EDIT ROM*

* OPTIONAL CARDS. ONE +5V REGULATOR ALWAYS
REQUIRED AT A03, BUT AN ADDITIONAL ONE MAY
BE PRESENT AT A01 TO SUPPLY ADDITIONAL
POWER REQUIRED FOR OPTION CARDS.

Figure 4-3. Card Placement in Chassis

The RAM allows the processor to store up to 1028_{10}, 8-bit data words. Each word may represent one 7-bit ASCII character code plus a cursor present/absent bit. These 1028 code-storage locations allow storing all the codes which may be displayed in 12 lines of 80 characters per line on the video monitor (12 lines x 80 characters = 960 code-storage locations). So that the terminal using these circuits may display up to 24 lines of 80 characters per line, the shared bus and refresh card circuits are designed to accept an optional extended RAM card to handle the additional character code storage locations required.

Figure 4-4 is a functional diagram of the memory card circuits. The following paragraphs briefly describe the functions shown in this figure. For circuit details, see the referenced logic diagrams (and their backup page descriptions) in Section 5. For further reference, timing details (waveforms) appear on timing diagrams at the back of Section 5.

Address Receiver

These circuits constantly monitor the 16 Address bus lines from the processor.

Option Switches

These switches allow manually setting/selecting/directing special control firmware operating modes/functions for the terminal which uses the memory card. The condition of these switches guides operations in the processor and refresh circuits.

Switch Multiplexer

This multiplexer allows the processor to read the condition of the various option switches and/or operating conditions monitored by the multiplexer. Address bus 2^1 and 2^0 (from the processor) act as an input function code to select one of four groups of input function words possible from this multiplexer.

Switch Multiplexer Bus Drivers

During one of the four possible input switch functions to the processor, these drivers place the Switch Multiplexer output on the 8-bit shared Data bus for the processor.

FROM PROCESSOR DATA BUS

DATA BUS TO REFRESH OR PROCESSOR

OPTION SWITCHES (000, 001)

60 HZ (REFRESH), LOWER CASE (KEYBOARD)

(ON BOARD) EXTERNAL SWITCHES AND STATUS

SWITCH MUX (000,001)

FROM PROCESSOR ADDRESS BUS

RECEIVER (000, 001, 003)

$A2^1 - A2^0$

KEYBOARD LOCKED STATUS

STATUS INDICATOR REGISTER (000)

DRIVERS (000)

STATUS INDICATORS AND AUDIBLE ALARM

$A2^0, 2^1, 2^{13} - 2^{15}$ LOAD

FROM PROCESSOR I/O CONTROL SIGNALS

I/O CONTROL (000)

ENABLE BUS DRIVERS

BUS DRIVERS (000)

$A2^1 - A2^0$

$1024_{10} X8$ RAM STACK (003)

RAM BITS $2^0 - 2^7$

BUS DRIVER (002)

READ WRITE STROBE

FROM PROCESSOR MASTER RESET

RECEIVER (001)

FROM PROCESSOR Ø2 TIME

READ WRITE CONTROL (001)

ENABLE DATA BUS

FROM PROCESSOR AND REFRESH MEMORY CONTROL SIGNALS

-READY TO PROCESSOR

$A2^{10}$
$A2^{15}$

ADDRESS DECODE (001)

RAM SELECT

ROM SELECT

$A2^{11} - A2^8$

ROM CHIP SELECTOR (003)

NOTE: DESIGNATIONS IN PARENTHESES, E.G., (000) REFERENCE THE LOGIC DIAGRAMS WHICH SHOW THE DETAILED CIRCUITS.

$A2^7 - A2^0$

4096_{10} (5ACD-0) X8 EROM STACK (004 - 007)

E-ROM BITS $2^0 - 2^7$

REGULATED +5V

+5V TO LEDS

POWER SUPPLY REGULATED -9V

Figure 4-4. RAM/E-ROM Functional Diagram

I/O Control

These circuits recognize either an input or output function from the processor (determined by Address bus $2^{15} - 2^{13}$ and Input Strobe or Output Strobe active). For an input function, the contents of Address bus 2^1 or 2^0 enable the Switch Multiplexer and I/O Control enables the Switch Multiplexer Bus Drivers to send the selected information to the processor. For an output function, I/O Control loads the Status Indicator register with the contents of the data bus.

Status Indicator Register and Drivers

During an output function from the processor, this register loads with the contents of the Data bus. The output from this register indicates processor/terminal operating modes.

Address Decode

These circuits examine Address bus $2^{15} - 2^{10}$ to determine whether either a RAM addressed or E-ROM addressed function is active from the processor.

RAM Stack

The random-access memory stack provides read/write storage for up to 1024 8-bit words. Address bus $2^9 - 2^0$ locates a word in the RAM. When Address Decode determines that a RAM function is active, RAM is selected, and Read/Write Control enables either the read or write operation in the RAM Stack. For a write, Data bus $2^7 - 2^0$ loads in the word location specified by Address bus $2^9 - 2^0$. For a read the RAM issues RAM Memory Bits $2^7 - 2^0$ from the location addressed by Address bus $2^9 - 2^0$. The 8-bit word read is made available to the Bus Drivers for placement on the Data bus.

Read/Write Control

These circuits act under direction of control signals received from the processor to control read/write RAM operations and issue a Ready response to the processor.

E-ROM Chip Selector

When Address Decode determines that an E-ROM function is active, E-ROM Chip Selector uses Address bus $2^{11} - 2^8$ to enable (select) one of the 16 E-ROM chips possible in the E-ROM stack.

E-ROM Stack

The erasable read-only memory stack provides fixed storage (burned-in) for up to 4096 8-bit words of control firmware. When Address Decode determines that an E-ROM function is active, E-ROM Chip Selector and Address bus $2^7 - 2^0$ addresses one word location and the 8 bits stored at that location appear on the eight E-ROM output lines $2^7 - 2^0$. This word is made available to the Bus Drivers for placement on the Data bus.

Bus Drivers

For either a RAM or E-ROM read operation, Read/Write control enables the Bus Drivers so the 8-bit information word read from memory is placed on the Data bus.

Master Reset

If the processor issues an active Master Reset signal, Status Indicator register and Read/Write Control circuits are reset to initial (clear) condition.

4.2 PROCESSOR CARD FUNCTIONS

This assembly acts as the controlling element for all operations within the logic module and for all external operations (e.g., keyboard data input, video monitor output, communication line message sending/receiving, optional serial printout, and optional tape cassette operations). The processor circuits control/sequence the flow of data and control signals over the shared bus supplied by the logic chassis backpanel. This includes the optional functions which may be added to the basic module. Basically, the assembly is an 8-bit/byte processor which utilizes externally-stored programs (control firmware) to execute operations. Such information resides in the E-ROM of the memory card assembly which is a required part of the basic module. Such execution instructions are applications oriented and as such are generally installed in the E-ROM (burned in) on a unique, customer-requirement basis. Once the processor circuits are initiated to perform an operation that they are capable of, they are the controlling entity for such sequences, communications, calculations, etc., as are

necessary to complete the particular operation. As such, they: 1) secure any needed information from the associated program-store memory (E-ROM) and execute such information, 2) utilize any associated (on the shared-bus), operating memory (RAM) as required (for temporary storage), and 3) request/accept/transmit I/O communications associated with the operation. The processor card includes RS-232-C/CCITT V.24 type communication interface and control circuits which provide asynchronous, serial communication with a modem. The main features of these interface control circuits are a universal asynchronous receiver/transmitter (which will receive and transmit simultaneously) and a first-in/first-out (FIFO) buffer for 64 8-bit received characters (8th bit for parity).

Figure 4-5 is a functional diagram of the processor card circuits. The following paragraphs briefly describe each of the functions shown in this figure. For circuit details, see the referenced logic diagrams (and their backup page descriptions) in Section 5. For further reference, timing details (waveforms) appear on timing diagrams at the back of Section 5. In addition, programming timing requirements are defined under Programming in Section 2.

6.745 MHz Oscillator, Rate Select Switches, and Timing Generator

These circuits generate the master timing required for all processor internal and external operations. Timing is initiated by a 6.745 MHz oscillator which drives various multistage counters. The resulting outputs govern not only internal processor operations, but also supply timing to the shared bus so associated circuit cards may synchronize their operation with the processor. These timing circuits include manually-selectable switches which allow setting the communications line baud rate to any one of eight standard, RS-232-C type, serial, asynchronous speeds (110, 150, 200, 300, 600, 1200, 2400, 4800, or 9600 baud).

Microprocessor

The microprocessor functional area of the processor card consists of a single chip, 8-bit parallel, central processor unit (Intel 8080 type, or equivalent) which recognizes and executes approximately 100 instructions (see Instruction Repertoire in Section 2). The microprocessor sends/receives 8-bit data bytes on a common Data bus (see Data Bus Format in Section 2). It issues 16-bit, external memory, data byte address to an Address bus (see Address Bus Format in Section 2). If enabled by special instruction, it will recognize and execute an external Interrupt according to a fixed scheme (see Interrupt Scheme in Section 2). Other microprocessor capabilities include: 1) shared bus control, 2) channel strobe capability, and 3) status output. See Section 2 for microprocessor programming information. Following paragraphs describe: 1) the functional arrangement and information flow within the microprocessor chip and 2) microprocessor interface. Understanding such information aids in determining proper operation of the microprocessor chip and surrounding circuits in the processor subassembly.
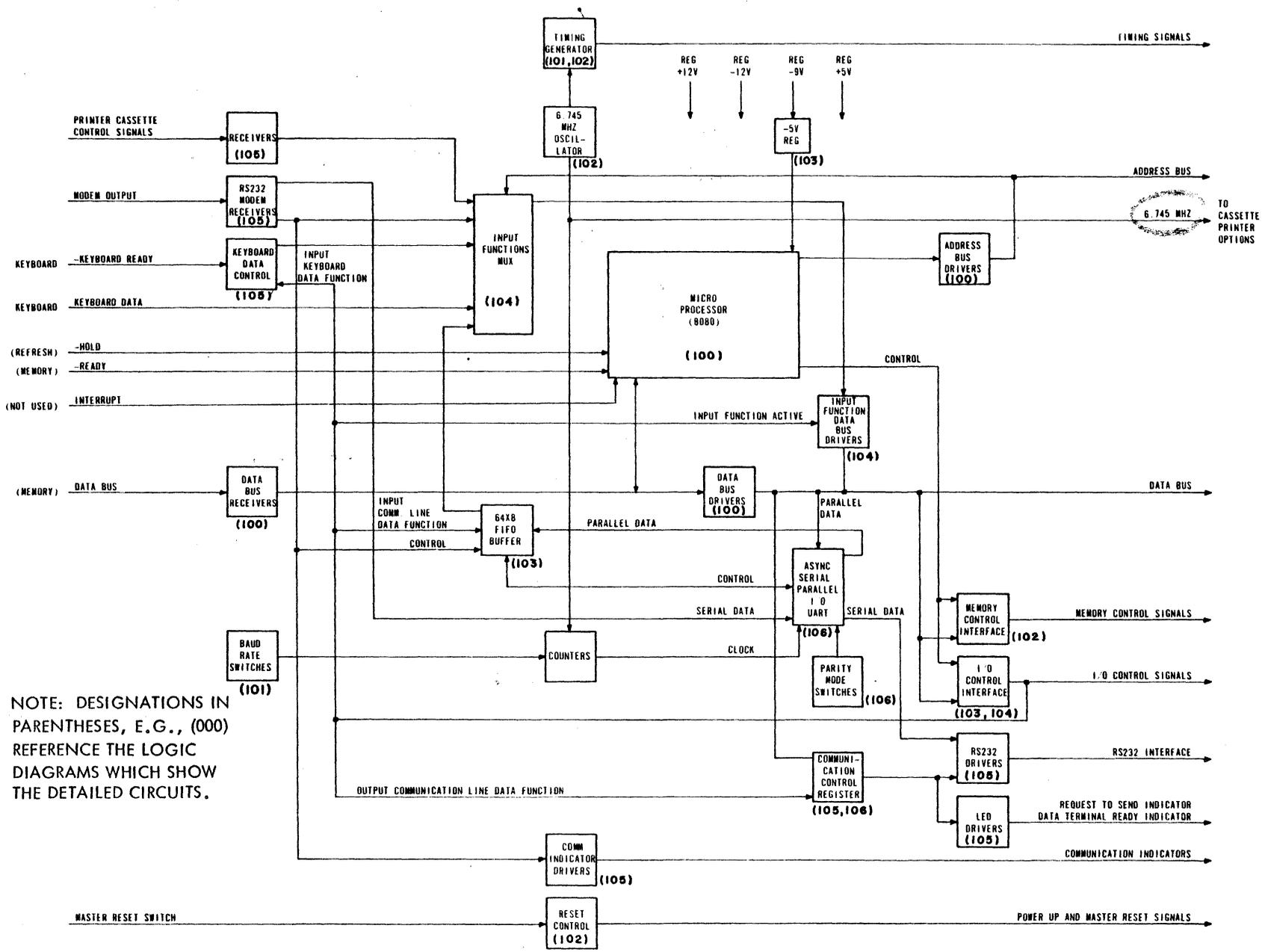
NOTE: DESIGNATIONS IN
PARENTHESES, E.G., (000)
REFERENCE THE LOGIC
DIAGRAMS WHICH SHOW
THE DETAILED CIRCUITS.

Figure 4-5. Processor Functional Diagram

Microprocessor Functions

Figure 4-6 identifies and defines the functional areas of the microprocessor. Following paragraphs briefly describe each of these functional areas. Since the microprocessor is a replaceable item and is not repairable, the descriptions include only functional theory which will aid in determining whether the chip as a whole is performing correctly. It should be understood that the microprocessor has more capability than is required in this application. Therefore, some microprocessor I/O function controls are not used.
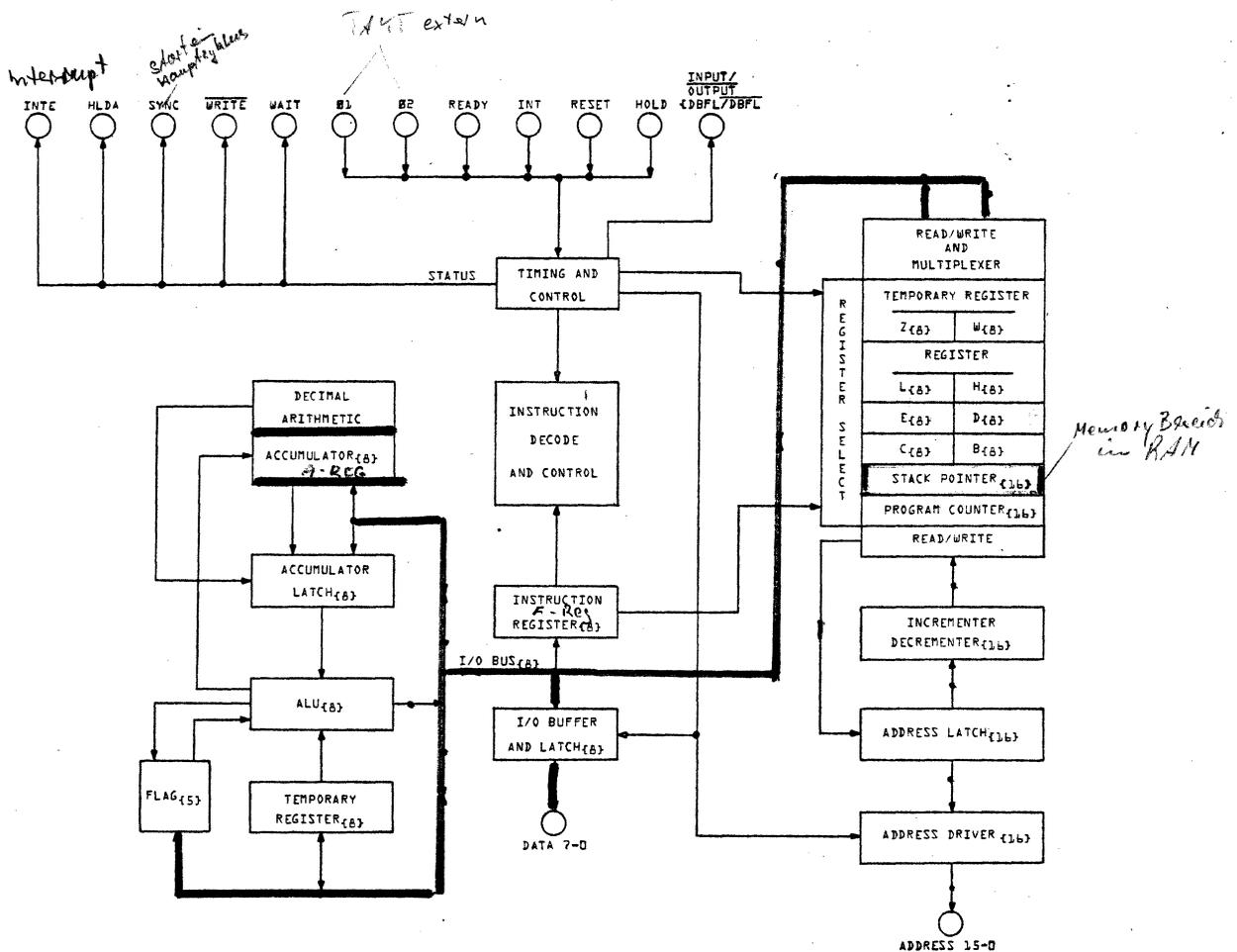
Figure 4-6. Microprocessor Chip Functional Diagram

INTEL 8080

Working Registers: The microprocessor contains seven accessible, working registers. These 8-bit registers are the Accumulator and the B, C, D, E, H, and L registers. Data operations occur between these registers and they also provide a means of addressing external memory (memory on the shared bus).

Stack Pointer Register: This is a programmer-accessible 16-bit register. Its contents specify the address in RAM (memory card or extended memory option card) where the first 8-bit byte of "stack" information resides. Stack information consists of either data or addresses which are set aside in memory by programming and which are retrievable after some intermediate operation(s). Information from the Program Counter register, any of the seven working registers, or from the Flag register may be stored/retrieved in/from a Stack location.

Flag Register: This circuit holds five conditions bits which reflect results of micro- processor operations. Such conditions affect execution of subsequent instructions. Instruction Repertoire in Section 2 defines flag conditions/use.

Timing and Control: These circuits synchronize microprocessor operation to timing and control signals received (e.g., Ø1, Ø2, Ready, INT, Reset, and Hold). They also issue five status conditions signals (e.g., INTE, HLDA, Sync, Write, and Wait) at the beginning of each machine cycle. In addition, they issue a signal specifying whether the microprocessor is in input or output mode (e.g., Input/Output, other- wise termed DBFL for Data Bus Flow or D BIN for Data Bus Input). See Microprocessor Interface, later in this section, for definitions of these signals received/issued.

Arithmetic Logic Unit: The Arithmetic Logic Unit (ALU) governs binary arithmetic and logical operations required for instruction execution. Operations available are add, subtract, logical product, exclusive OR, or inclusive OR.

Decimal Arithmetic: These circuits govern decimal operations possible in the micro- processor. Certain instructions allow decimal operations on data. Any 4-bit, binary data group may be treated as a decimal number as long as it represents a decimal digit from 0 through 9. Thus an 8-bit byte may represent two decimal digits.

I/O Buffer and Latch: All 8-bit bytes to/from the external world (shared bus) are sequenced through these circuits. See Microprocessor Interface, later in this section, for definition of these I/O lines.

Address Driver: These drivers issue all 16-bit addresses of external (on the shared bus) memory locations (up to 64K) for read or write operations. They also issue I/O channel addresses (ultimate capability would be up to 256 each for input and for output) for operations which send/receive information to I/O channels (e.g., various peripherals such as the optional printer or tape cassette). See Microprocessor Interface, later in this section, for definition of these output lines.

Miscellaneous Temporary Registers, Latches, Instruction Handling Circuits etc.:
These remaining circuits (shown in figure 4-6) are vital for sequencing and executing instruction operations within the microprocessor.

Microprocessor Interface

Figure 4-7 identifies all I/O signals for the microprocessor. Figure 4-8 summarizes I/O timing for an instruction cycle within the microprocessor. Figure 4-9 shows microprocessor state transitions which occur in response to certain inputs and which causes certain outputs. Following paragraphs describe the function of each microprocessor I/O signal. For futher detail, refer to the microprocessor chip specification referenced in the Foreword of this manual.

			MICROPROCESSOR CHIP (INTEL 8080 OR EQUIVALENT)			
A_{10}	1			40		A_{11}
GND	2			39		A_{14}
D_4	3			38		A_{13}
D_5	4			37		A_{12}
D_6	5			36		A_{15}
D_7	6			35		A_9
D_3	7			34		A_8
D_2	8			33		A_7
D_1	9			32		A_6
D_0	10			31		A_5
−5V	11			30		A_4
RESET	12			29		A_3
HOLD	13			28		+12V
INT	14			27		A_2
ϕ_2	15			26		A_1
INTE	16			25		A_0
DBFL	17			24		WAIT
$\overline{WR}$	18			23		READY
SYNC	19			22		ϕ_1
+5V	20			21		HLDA
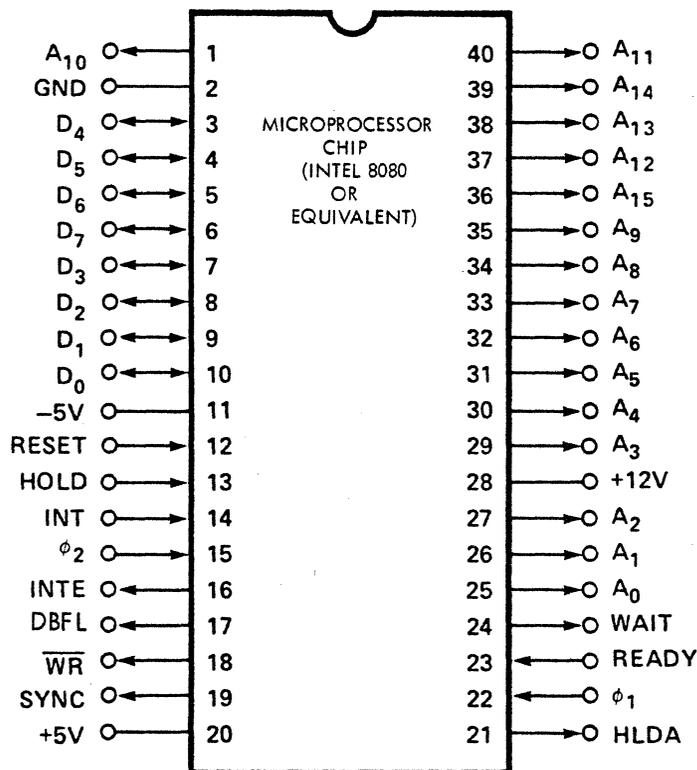
Figure 4-7. Microprocessor I/O Signals
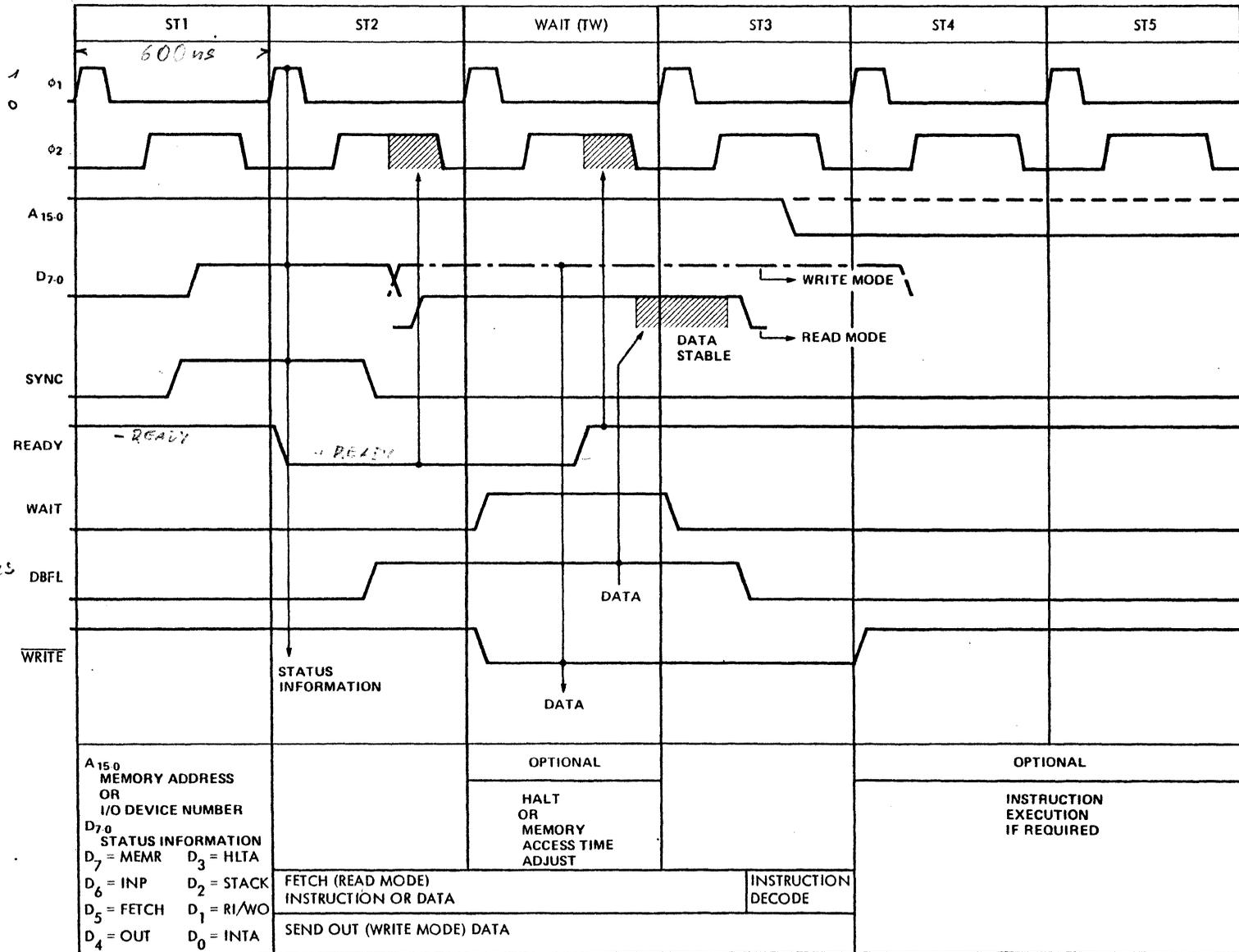
Figure 4-8. Microprocessor I/O Timing for Instruction Cycle
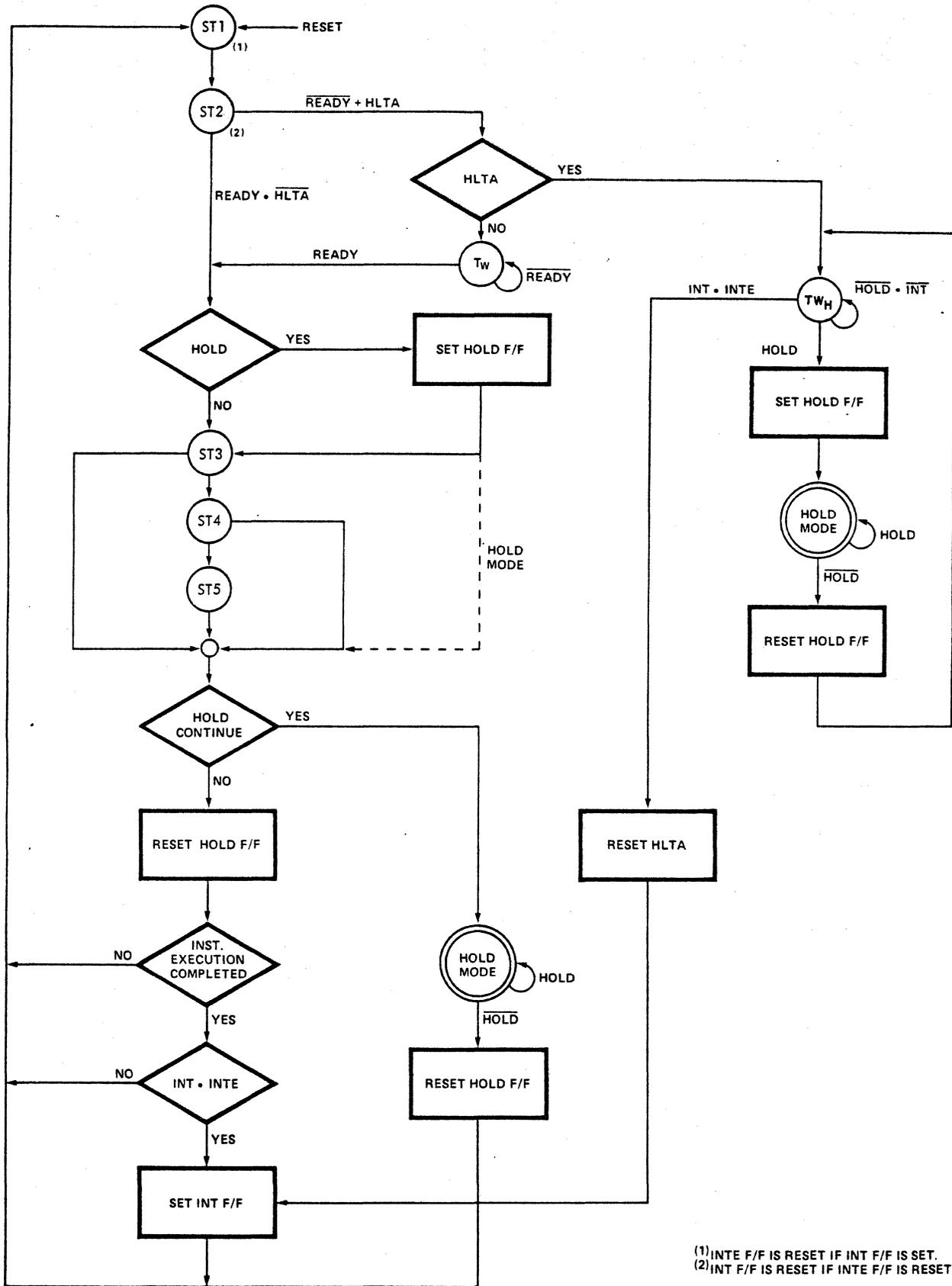
Figure 4-9. Microprocessor State Transitions

(1) INTE F/F IS RESET IF INT F/F IS SET.
(2) INT F/F IS RESET IF INTE F/F IS RESET

<u>Signal Ground</u>: This is the required logic circuit, common, signal ground reference point.

<u>-5v, +5v, and +12v</u>: These are input power voltages required for operation.

<u>Ø1 and Ø2</u>: These two timing input pulses govern the operating speed of the microprocessor.

<u>Address $_{15}$ through Address $_0$</u>: These output lines issue the address of either an external memory byte or an I/O channel. A high specifies a logical 1 and a low a logical 0.

<u>Data $_7$ through Data $_0$</u>: These bidirectional lines receive/issue 8-bit instructions or data transfers for communications between the microprocessor and either memory or I/O channels. A high specifies a logical 1 and a low a logical 0. At the beginning of each machine cycle, during active sync time, the microprocessor issues status information on these eight lines. Figure 4-10 shows the status bit definitions on the Data lines.

DATA BUS BIT	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
STATUS INDICATED BY ACTIVE HIGH BIT	MEM * REQ	INP *	FETCH	OUT	HLTA	STACK	RI/WO	INTA *

* MAY BE USED FOR CONTROL OF MICRO-PROCESSOR'S INPUT MULTIPLEXER

└H (1) = INTERRUPT ACK

H (1) = READ OR INPUT
L (0) = WRITE OR OUTPUT

H (1) = ADDRESSING PUSHDOWN STACK

H (1) = HALT ACK

H (1) = ADDRESSING AND SENDING TO AN OUTPUT DEVICE

└H (1) = FETCH FOR FIRST BYTE OCCURRING

H (1) = ADDRESS OF AN INPUT DEVICE ON ADDRESS BUS

└H (1) = DATA BUS TO CARRY DATA READ FROM MEMORY

Figure 4-10. Microprocessor Status Byte

Reset: An active high on this input allows an external source to clear the content of the Program Counter register to zero and set the Instruction register content to zero. Also cleared to zero (reset) are the Interrupt Enable (INTE) and Hold Acknowledge (HLDA) flip-flops which issue INTE and HLDA signals.

Hold: An active high on this input requests the microprocessor to enter Hold state.

Hold Acknowledge: An active high Hold Acknowledge output occurs in response to the Hold input and indicates that the Data and Address I/O lines are in the floating condition (these lines are three-state: high, low, or floating).

Interrupt: An active high Interrupt input (INT) requests the microprocessor to interrupt normal instruction sequence execution (after completing the current instruction) and take an alternate special path due to conditions specified by the unique interrupt.

Interrupt Enable (Not Used): An active high Interrupt Enable output (INTE) indicates that the microprocessor will recognize and process interrupts. An EI instruction enables interrupts by setting the Interrupt Enable flip-flop. A DI instruction resets the flip-flop and disables interrupt processing (in this case, INTE output is inactive low).

Sync: The microprocessor issues this pulse to indicate the beginning of each machine cycle. Status information is issued on the Data line outputs at this time. External circuits may use the Sync signal to coordinate their operation with the microprocessor. .

Data Bus Flow: The microprocessor issues a high Data Bus Flow (DBFL) signal (otherwise termed $\overline{D}$ BIN, Data Bus Input) to indicate it is in the input mode. Low level indicates output mode.

$\overline{Write}$ (Not Used): A low level $\overline{Write}$ output indicates that either a Write-To-Memory or Write-To-Output-Channel operation is in process. A high level indicates either a Read-From-Memory or a Read-From-Input-Channel operation. Data on D_7-D_0 must not change while $\overline{Write}$ is active low.

Ready: This input being active high indicates that requested memory or I/O channel input is available and valid. If Ready does not become active by $\emptyset 2$ of State Time 2, the microprocessor enters Wait state.

Wait (Not Used): The microprocessor issues an active high Wait signal to indicate that it is waiting for a Ready signal from an external area from which it requested information.

Input Function Multiplexer

The multiplexer selects information for the Data bus as requested by one of four possible input functions being active. The four types of input data chosen from are: 1) communication line receive data, 2) communication line/printer/keyboard status information, 3) keyboard data, and 4) communication line control status. See Programming in Section 2 for input function definitions.

Input Function Data Bus Drivers

These circuits consists of three-state buffer/drivers which place input function data (selected by the Input Function Multiplexer) on the shared Data bus lines. The three states possible are high, low, or floating.

Keyboard Data Control

This circuit recognizes when a keyboard-generated, input data character is ready.

Printer/Cassette Control Signal Receivers

These circuits receive status signals from either the optional printer interface or the optional cassette interface. Signals received are RS-232-C compatible (see the EIA RS-232-C standard). These status signals become inputs to the Input Function Multiplexer.

RS-232-C Modem Receivers

These RS232- to -TTL type line receivers accept standard RS-232-C or CCITT V.24 type communication signals (see the EIA RS-232-C standard). Such signals received become: 1) received serial data input to the Asynchronous Serial/Parallel I/O circuit, 2) status input to the Input Function Multiplexer, and 3) control input to the FIFO Buffer.

Asynchronous Serial/Parallel I/O

This circuit deserializes data from the RS-232-C Modem Receivers and converts it into 7-bit data (character) codes which become input to the FIFO Buffer. The circuit also serializes Data bus, 7-bit codes and issues them as a serial data stream compatible with RS-232-C (or CCITT V.24) type communication interface. This asynchronous receiver/transmitter circuit also monitors the received data for character parity errors and framing errors (Stop bit not a marking logical 1).

Parity Mode Switches

These switches enable even or odd parity checking on the received data stream by the Asynchronous Serial/Parallel I/O circuit.

First In First Out (FIFO) Buffer

During receive data communications, this buffer allows storing 64 8-bit words of data (7 data plus one parity) which have been deserialized by the Asynchronous Serial/Parallel I/O circuit. The FIFO stores 8-bit words in a word-serial, flow-through fashion. Each time a new data word (character) is assembled, it loads into the FIFO and pushes all 64 words currently in the FIFO ahead one word location. The word in the end location is supplanted by the one preceding it, etc. The Communcation Line Data input function (see description in Programming, Section 2) clocks the 8-bit words out of the FIFO, one word at a time, serially, with the first word that was stored being the first word clocked out etc., making the last word stored being the last clocked out. FIFO 8-bit words are used as parallel input to the Input Functions Multiplexer.

I/O Control Interface

These circuits constantly monitor microprocessor address, data, and control outputs to determine when an input or output function is active. When an I/O function is recognized, the I/O Control Interface circuits issue enables which allow executing the the function. These circuits include control flip-flops which issue Input Strobe and Output Strobe signals. They also include an I/O function demultiplexer which recognizes the following functions: 1) Keyboard Data input, 2) Communication Line Data input, 3) Printer Data output, 4) Communication Line Control output, and 5) Data output.

Memory Control Interface

By constantly monitoring microprocessor data and control outputs, these circuits determine whether a CPU Memory Read or CPU Memory Write function is active. If either one is active, these circuits indicate so to the shared bus to enable the function in the appropriate circuit cards on the bus.

Data Bus Receivers and Data Bus Drivers

The three-state Data bus receivers place 8-bit input Data words, from the shared, I/O, Data bus lines, on the microprocessor Data lines when the microprocessor requests instruction data. The three-state Data bus drivers place 8-bit, output, Data words, from the microprocessor, on the shared, I/O, Data bus lines when the microprocessor wishes to issue data resulting from its calculations/executions. The three states possible from either the receivers or the drivers are high, low, and floating.

Address Bus Drivers

These circuits consist of three-state buffer/drivers which transmit Address signals, from the microprocessor, to the shared, I/O, Address bus lines when the micro-processor wishes to address information to/from some circuit card on the shared bus. The three states possible on the output lines are high, low, or floating.

Communication Line Control Register

For an active Communication Line Control output function (see Programming in Section 2), this register loads with the contents of the shared, I/O, Data bus lines. At this time, each Data bus line has a specific communication line control signifi-cance and will initiate signals/actions accordingly.

LED Drivers

These circuits issue power to light operator panel indicators when Request To Send and/or Data Terminal Ready communication line control conditions are active and loaded in the Communication Control register.

RS-232-C Drivers

These TTL-to-RS-232-C type line drivers transmit serial data and control signals to the RS-232-C (or CCITT V.24) communication interface.

Communication Indicator Drivers

These circuits issue power to light operator panel indicators showing the constant condition of the following communication line signals: 1) transmit data line, 2 2) receive data line, 3) carrier on line, and 4) clear to send line.

Reset Control

These circuits issue reset (clear) signals for either Master Reset switch activation (on the operator panel) or during power application to the processor circuits. Active reset condition clears various processor circuits to the initial (or starting) condition. Reset also passes to the shared bus so other card circuits may be initialized by it.

-5v Regulator

An integrated circuit voltage regulator chip located on the processor card uses -9v, bulk, external power to supply regulated -5v to the shared bus for use by whichever cards on the bus may require it.

4.3 REFRESH CARD FUNCTIONS

The refresh card provides circuits which drive the video, horizontal sync, and vertical sync of a crt video monitor. The circuits generate and issue drive signals which allow displaying either 12 lines or 24 lines (optional) of 80 characters per line on a 12-inch diagonal crt. The refresh circuits rely on the processor within the basic logic module for operation/sequence control/directions. The refresh circuits receive displayable data (character) codes and video control character codes from a refresh RAM in the logic module. Circuit design allows receiving display codes for the basic 12-line crt display from the basic memory circuit card and receiving the codes for an additional 12 lines from the extended memory refresh RAM option card which may reside in the logic module. Circuit design also includes capability to interface and operate with an edit option card in the module. The highlight option allows and controls displaying reduced intensity or blinking fields of characters on the crt. All control and data signal flow between the refresh card circuits and other circuit cards (processor, memory, extended memory refresh RAM, and highlight) is via the shared bus provided by the logic module chassis which houses the cards.

Figure 4-11 is a functional diagram of the refresh card circuits. The following paragraphs briefly describe: 1) video display refresh characteristics and 2) the functions shown in figure 4-11. For circuit details, see the referenced logic diagrams (and their backup page descriptions) in Section 5. For further reference, timing details (waveforms) appear on timing diagrams at the back of Section 5.
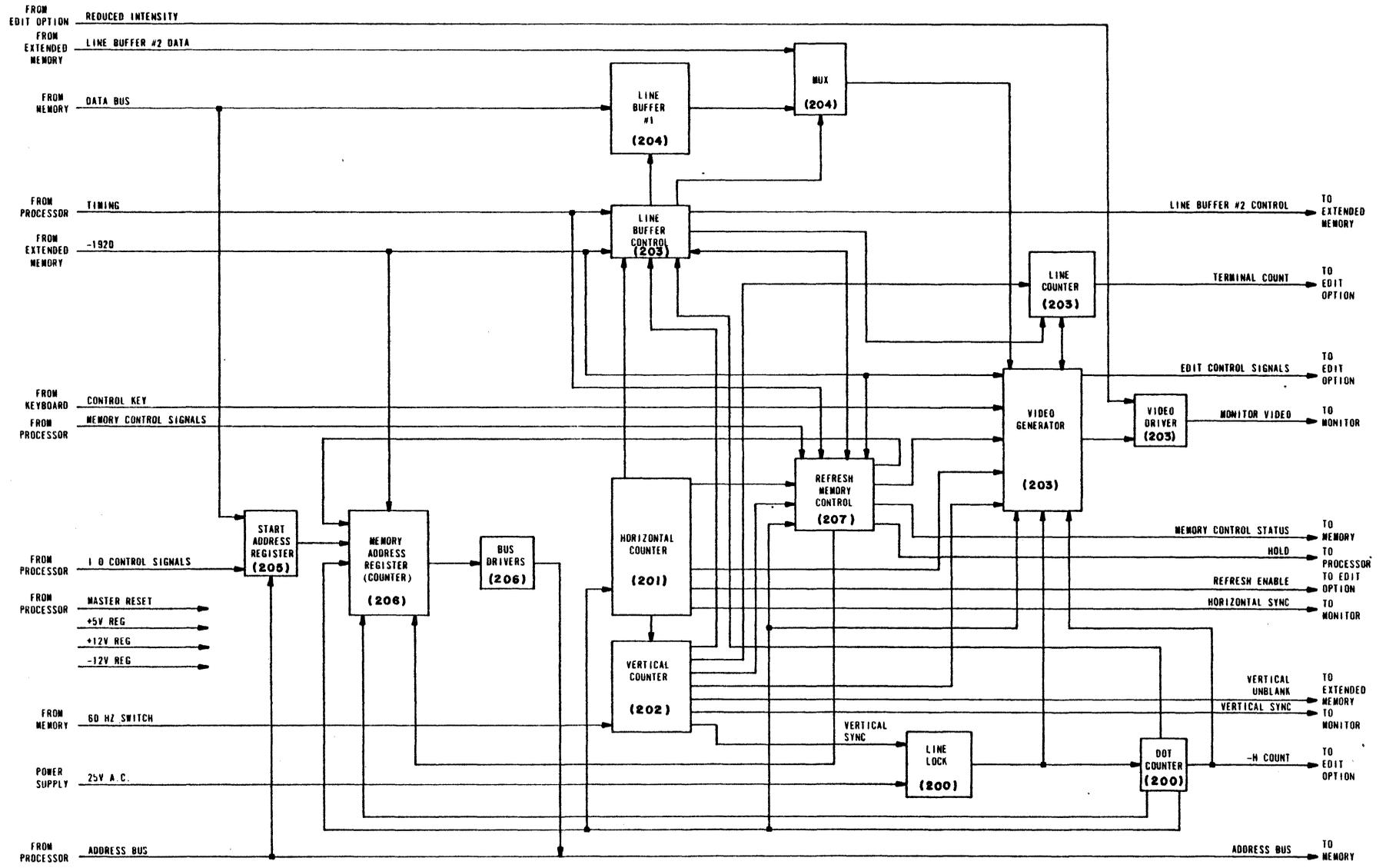
NOTE: DESIGNATIONS IN PARENTHESES,
E.G., (000) REFERENCE THE LOGIC DIAGRAMS
WHICH SHOW THE DETAILED CIRCUITS.

Figure 4-11. Refresh Functional Diagram

Required Video Display (CRT) Refresh Characteristics

To aid understanding refresh circuits operation, the following paragraphs define the display characteristics of the crt hardware which depends on the refresh circuits for video, horizontal sync, and vertical sync.

Display Line

The refresh circuits drive the crt to display 12 lines (24 lines optional with extended memory) of characters. Each line has 80 character positions. All lines and character positions may be used in a message to make a full-screen display (page) with a maximum of 960 characters (or 1920 characters with extended memory). Figure 4-12 shows the pattern of display lines as they appear on the crt. All 24 line positions are present on both the 12-line and 24-line versions. However, the 12-line version blanks (displays no characters) in the 12 extra line positions during refresh scanning (see Scan Line).
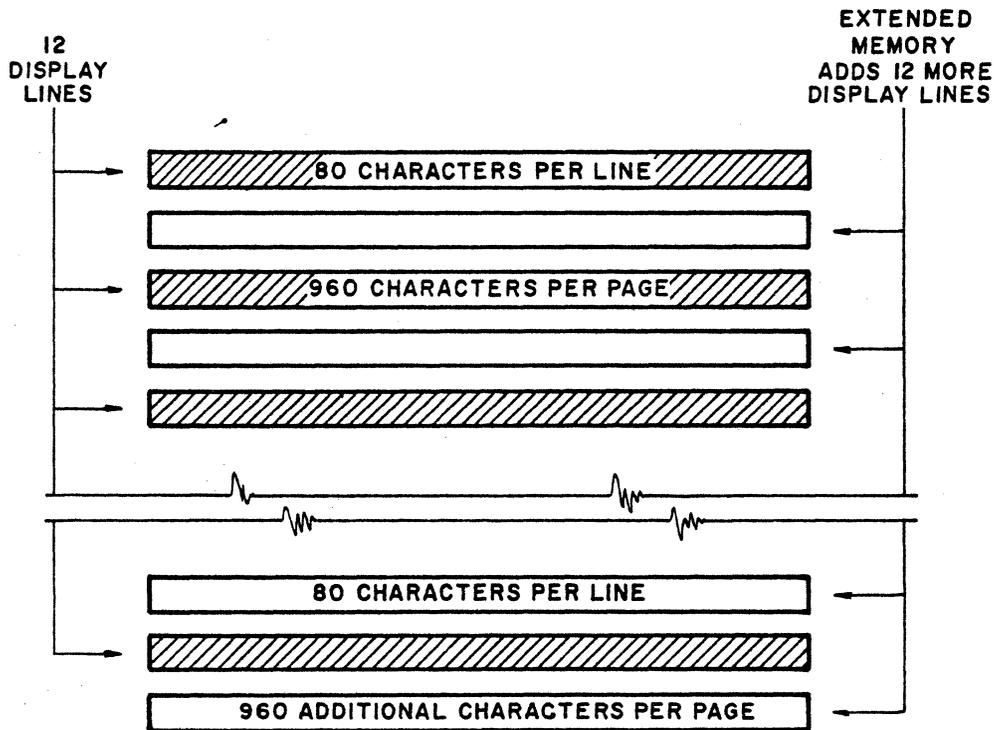
Figure 4-12. Display Lines

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Scan Line

Each display line of characters requires 10 horizontal scan lines. Figure 4-13 shows the relationship between characters and the scan lines which produce them. As the electron beam of the crt makes one scan of the display screen, the refresh circuit video output unblanks the beam to illuminate dots in only one row of each character matrix for each of the 80 character positions. As seen in figure 4-13, it requires up to nine scans to produce the dot patterns for the characters shown. All character dot patterns appear within a 7-dot wide by 9-dot high matrix. There is 2-dot spacing between adjacent 7-dot wide character boundaries. Most characters have their matrix within the top seven scan lines. Characters which have descending elements (lowercase g, p, etc.) and displayable control functions (H_T, C_R, etc.) use the eighth and ninth scan lines. The last scan line (tenth) is for line spacing and cursor display.
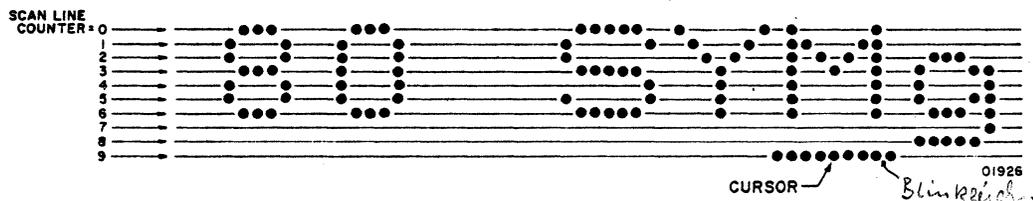
Figure 4-13. Character Line Formation by Scan Lines

Cursor

The refresh circuits generate the video to display the data entry point marker termed the cursor. The cursor underlines the character position on the screen where the next input or output action occurs. The cursor is a horizontal line approximately nine dots wide. The cursor displays in the bottom (tenth) scan line in a character line (see figure 4-13).

Character

The display uses a series of closely spaced dots to portray a character. The refresh circuits supply video signals such that the scanning crt electron beam unblanks (turns on sufficiently to illuminate the phosphor coating on the face of the crt) within a 7-dot wide by 9-dot high matrix as required to produce the dots to portray a character. On either side of each character's 7-dot wide matrix is one blank column of 9 dots to provide 2-dot spacing between adjacent characters. Figure 4-13 shows the dot patterns for several characters and figure 4-14 shows the entire dot matrix cell within which any character displays. The basic characters displayed are the 95 alphanumeric symbols (040_8 - 176_8) per ANSI ASCII Standard X3.4 1968. In addition, the 32 control codes (000_8 - 037_8) plus the DEL code (177_8) are displayable. This gives a total of 128 displayable characters. See Section 7 for the dot patterns of all displayable characters.
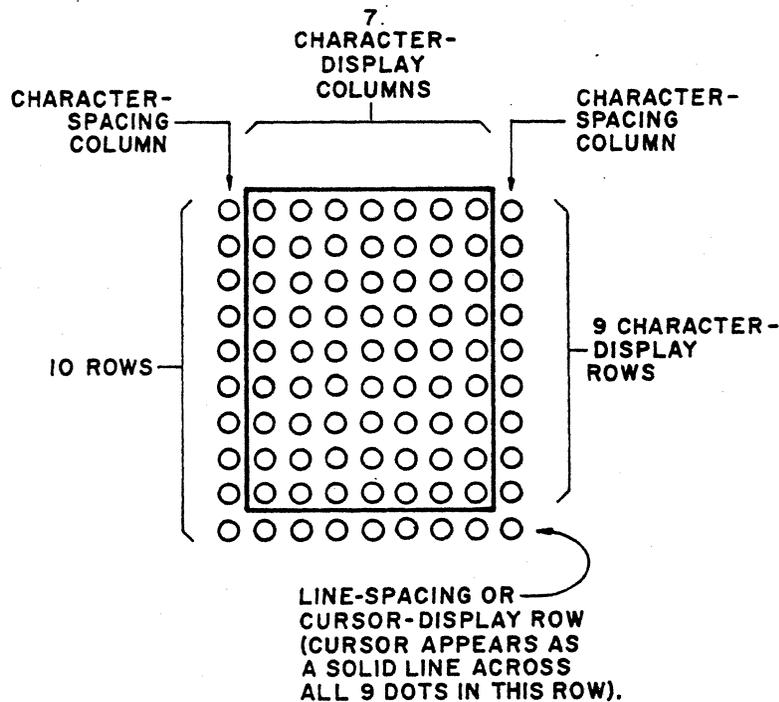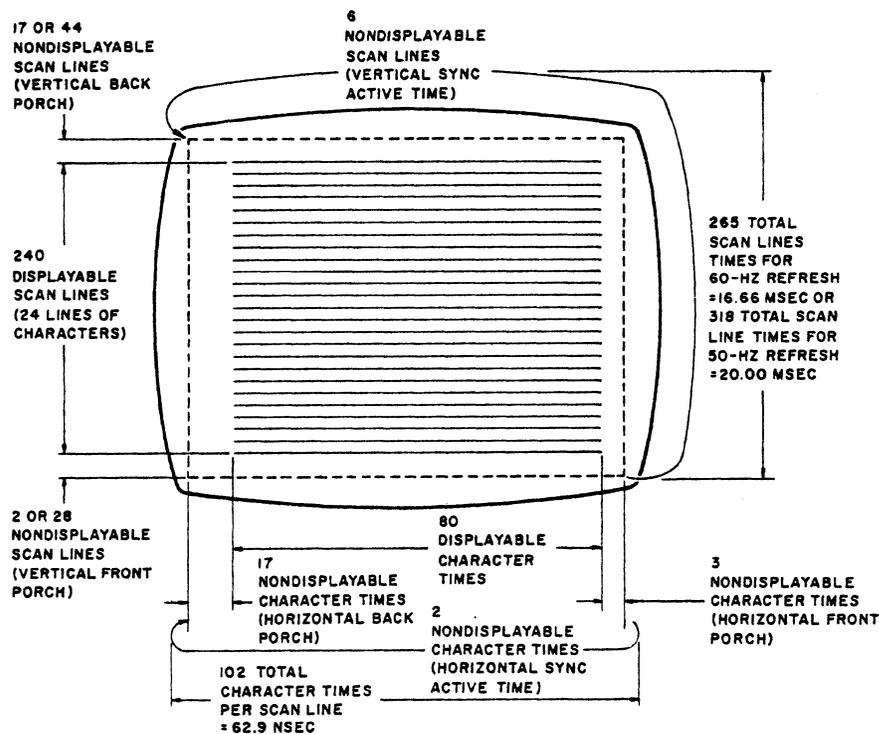

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Figure 4-14. The Character Cell Dot Matrix

Video Display Refresh Timing

Figure 4-15 illustrates screen refresh timing. Table 4-1 defines timing characteristics of the screen refresh operation for both 60-Hz and 50-Hz refresh.

Figure 4-15. Screen Refresh Timing

TABLE 4-1. REFRESH TIMING

60-HZ REFRESH	50-HZ REFRESH	REFRESH COMPONENT
68.51 nsec	68.51 nsec	1 dot scan time.
616.59 nsec	616.59 nsec	1 character scan time (1 space dot, plus 7 display dots, plus 1 space dot for a total of 9 dots).
62.9 µsec	62.9 µsec	1 scan line time (80 display characters, plus 3 front porch characters, plus 2 sync characters, plus 17 back porch characters for a total of 102 total character times).
49.3 µsec	49.3 µsec	80-character displaying time (one line of characters).
13.6 µsec	13.6 µsec	Horizontal retrace time (22 character times composed of front porch, sync, and back porch).
16.66 msec	20.00 msec	Vertical, full-screen refresh time (for 60 Hz = 240 character-displaying scan line times, plus 2 front porch scan line times, plus 6 sync scan line times, plus 17 back porch scan line times for a total of 265 scan line times; for 50 Hz = 240 character-displaying scan line times, plus 28 front porch scan line times, plus 6 sync scan lines times, plus 44 back porch scan line times for a total of 318 scan line times.
1.57 msec	4.91 msec	Vertical retrace time (for 60 Hz = 25 scan line times including front porch, sync, and back porch; for 50 Hz = 78 scan line times including extended front porch, sync, and extended back porch).

Line Lock Circuit

This circuit monitors the frequency of the input power supplied to the refresh circuit card. It then issues an oscillator output which matches the rate of crt full-screen refresh cycles to the frequency of the input power. Thus, if input power has a 60-Hz frequency, 60 full-screen refresh operations occur each second. Such synchronization prevents jitter and distortion in the visual display on the crt. Line Lock circuit output governs the speed of the Dot Counter, Horizontal Counter, and Video Generator.

Start Address Register

ASCII codes representing displayable characters are stored in the RAM portion of the memory card circuits (address range 2000_{16} through $23FF_{16}$ for basic, 12-line display or 2000_{16} through $277F_{16}$ with extended memory option for 24-line display). Firmware executed in the processor card circuits selects the starting address of the first character (leftmost) of the first (top) line of 80 characters for display on the crt. Such firmware causes the processor to place this starting address on the shared Data bus lines for loading into the Start Address register for the start of each full-screen refresh operation. This start address is always that of the leftmost of 80 consecutive displayable characters which may form a line of characters on the crt. A start address cannot be that of a character located elsewhere along a character line. This scheme allows the firmware to implement scrolling (shifting up or down) all lines of characters displayed on the crt. Start Address register contents load in the Memory Address register (Counter) at the beginning of the screen refresh operation.

Memory Address Register (Counter) and Address Bus Drivers

These circuits issue to the shared Address bus the address in refresh memory where a character for display is located. Such address may be to the basic 12-line refresh RAM provided by the memory card circuits or it may be to the optional extended memory refresh RAM which may be present on the shared bus. The Memory Address register loads from the Start Address register before the start of each new refresh operation. Once loaded, the Memory Address register begins incrementing by one for each consecutive character until all 80 characters for the top display line are loaded into either Line Buffer #1 (for one of the 12 basic display lines of characters) or into Line Buffer #2 in the extended memory card circuits (for one of the 12 extended memory lines of characters). Line Buffer #1 always loads with odd number display lines (first, third, etc.) of characters while #2 always loads with even number lines (second, fourth, etc.). When the last (tenth) scan line of any line of characters is completed, the line buffer associated with that line is full. The following line of 80 character positions will load into the other line buffer concurrently, while the first line buffer supplies 10 scan lines for displaying a row of 80 characters. This process continues until all display lines of characters (12 or 24) are refreshed on the crt.

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Dot Counter

This circuit counts the number of dots used in one scan line component of one character (see Character paragraph in preceding text). After counting the nine dots which comprise each such component, this counter issues a control signal which increments the character position Horizontal Counter and loads the video serializer portion of the Video Generator with a new set of dots for one scan across one characters. At 60-Hz refresh rate (for 60-Hz input power), this occurs once every 619.59 nanoseconds as a scan line progresses across a line of characters.

Horizontal Counter

This counter maintains horizontal character position count for each scan line. It maintains control for beam scan during each: 1) 80-character display line, 2) end of line (after 80th character), 3) retrace operation, and 4) start of line (preceding first character). It issues the Horizontal Sync pulse required by the crt.

Vertical Counter

This counter maintains vertical scan line count down the entire crt display. It maintains control for beam scan during each: 1) 12/24 character lines, 2) end of lines (bottom of screen), 3) flyback to start of screen operation, and 4) start of display (preceding top character line). It issues the Vertical Sync pulse required by the crt.

Refresh Memory Control

These circuits govern memory address loading, memory address increment, video blank/unblank for extended memory absence/presence, and issue memory status signals.

Video Generator and Video Driver

The Video Generator uses 7-dot ASCII displayable character codes (received from basic or extended refresh RAM via the Line Buffer Multiplexer) to generate the blank/unblank dot pattern for the seven dots of each scan line for each character. The Video Driver issues this serial, video stream to the crt.

Line Counter

This counter keeps track of the current scan line within a character line. As such, it allows selecting the correct scan line coordinate of a character's dot components which are permanently stored in the symbol generator portion of the Video Generator. The 7-bit ASCII code from the Line Buffer Multiplexer is the other coordinate required to generate a particular 7-dot, blank/unblank, dot stream for refreshing one scan line of one character.

Line Buffer #1

This recirculating buffer supplies the refresh ASCII codes for all 80 character positions in each/any one of the basic, 12-line-display character rows. This buffer loads such ASCII codes during the refresh time for the extended display character row position immediately preceding a basic character row. This occurs whether the extended memory card is present or not. Line Buffer #1 shifts these codes along in unison with the beam scan to provide the blank/unblank dot stream for each character along each scan line which is refreshing a basic character row.

Line Buffer Control and Line Buffer Multiplexer

These circuits load and select ASCII code components from the basic 12-line Line Buffer #1 or the extended memory RAM Line Buffer #2.

+ 5V REGULATOR CARD FUNCTIONS

A separate hardware maintenance manual contains the theory of operation for the + 5 regulator (see Foreword).