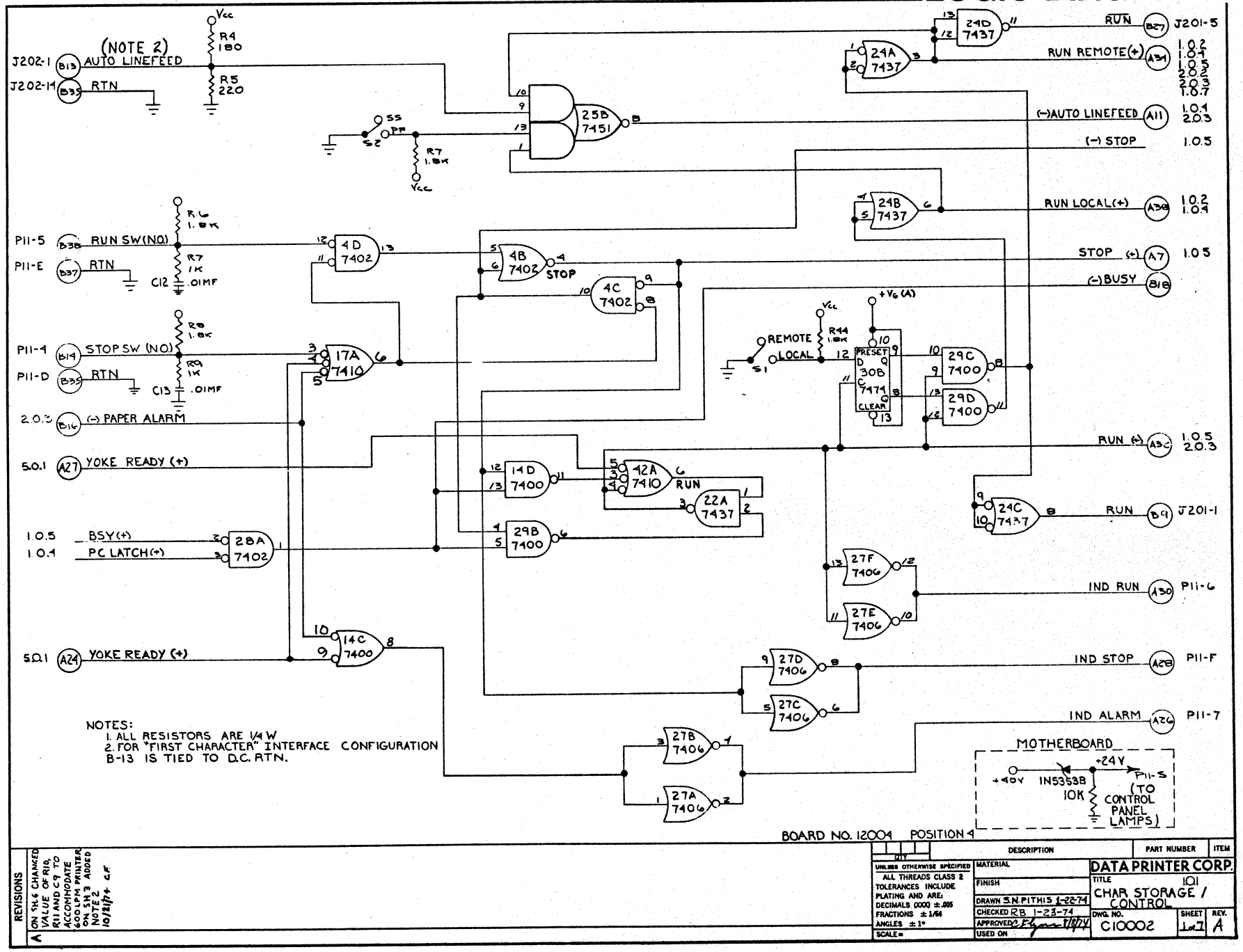


Figure 1.0.1 Character Storage/Control

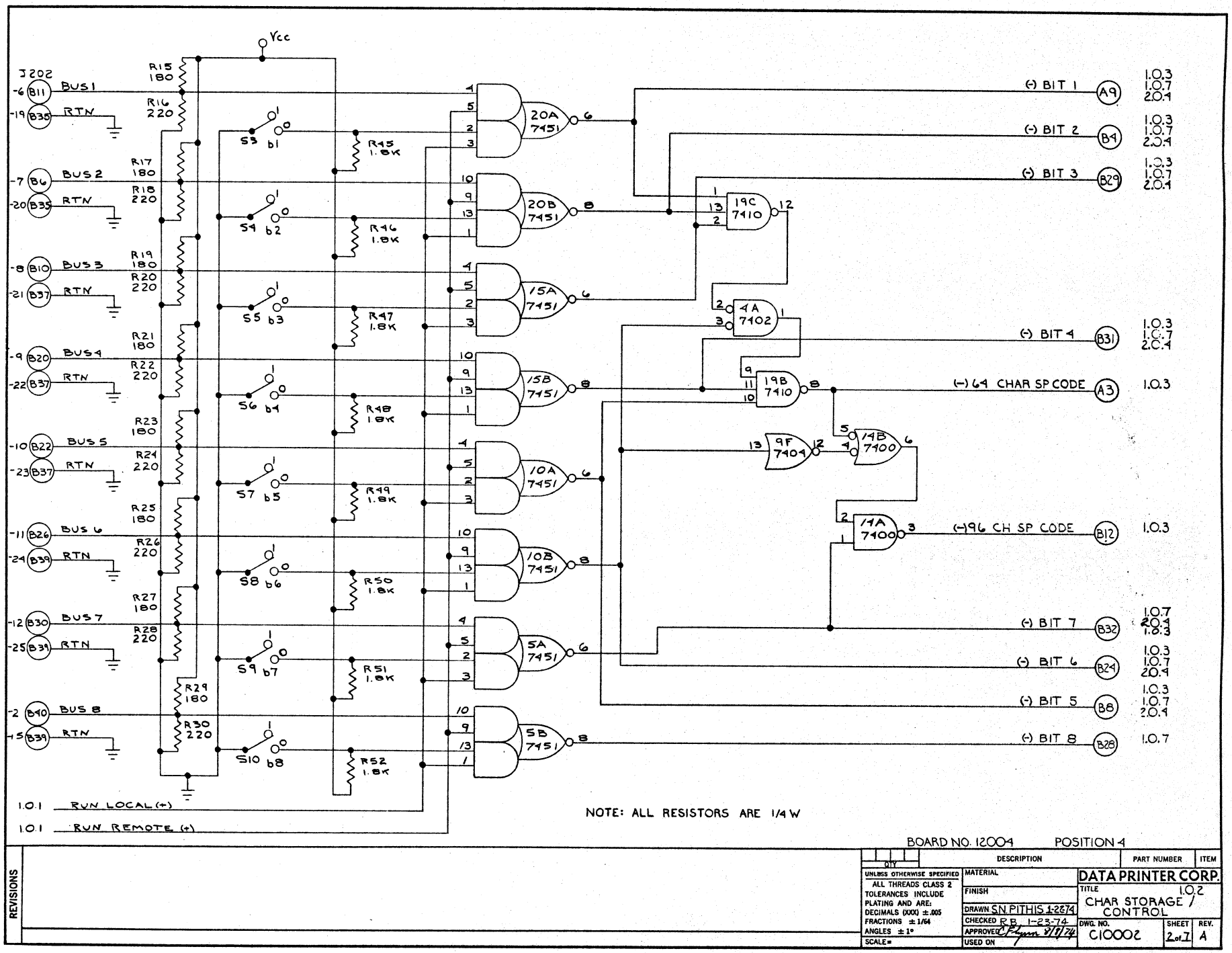
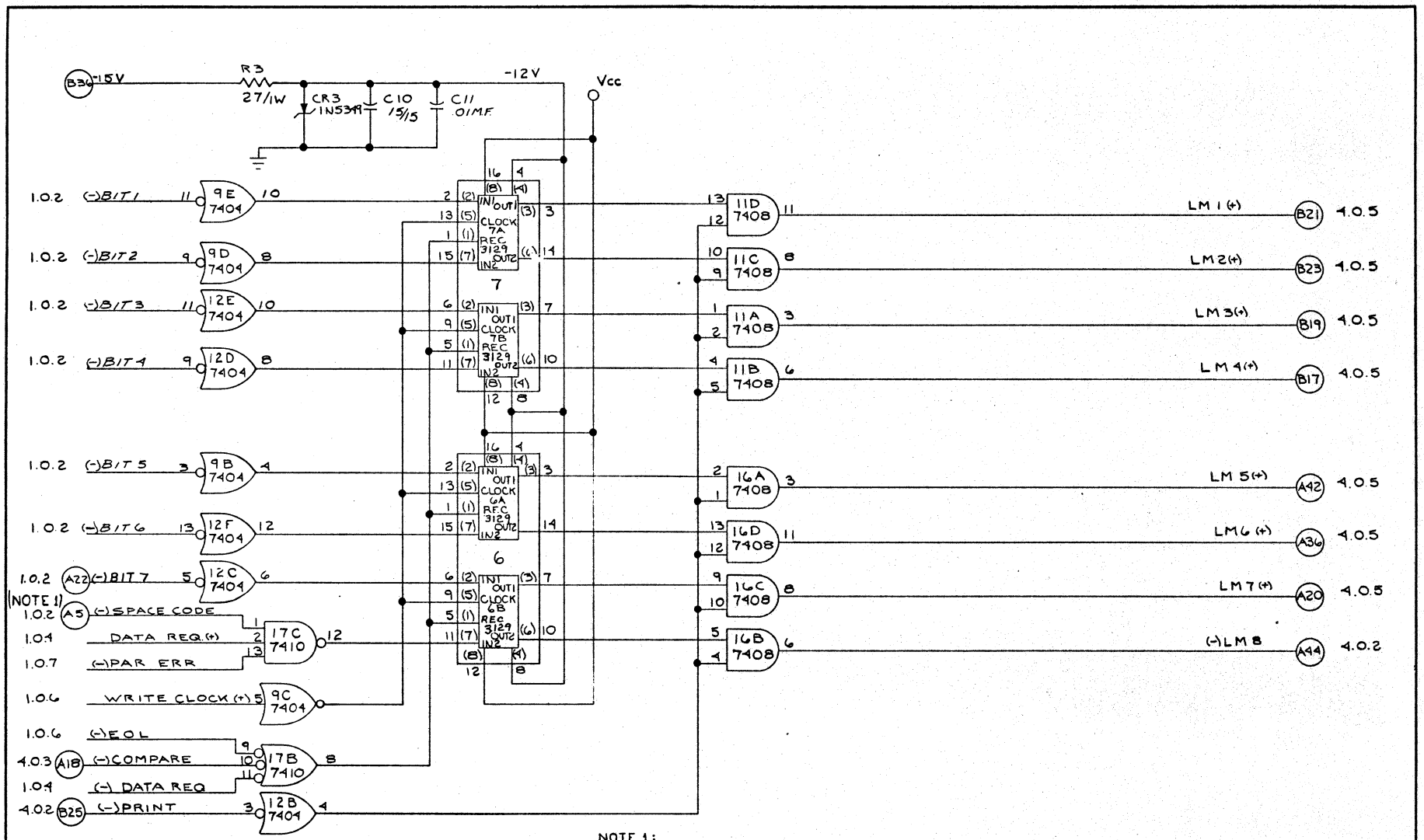


 Figure 1.0.2 Character Storage/Control



NOTE 1:
FOR 64 CHARACTER ASCII SET (-) SPACE CODE SIGNAL ORIGINATES AT 4A-3 (SHIFT 2 (-) 64 CHAR SP CODE)
FOR 96 CHARACTER ASCII SET (-) SPACE CODE SIGNAL ORIGINATES AT 4B-12 (SHIFT 2 (-) 96 CHAR SP CODE)

NOTE 2:
FOR 136 COLUMN PRINTER IC's 6A, 6B, 7A AND 7B MUST BE TMS3131 OR EQUIVALENT

BOARD NO. 12004 POSITION 4

REVISIONS

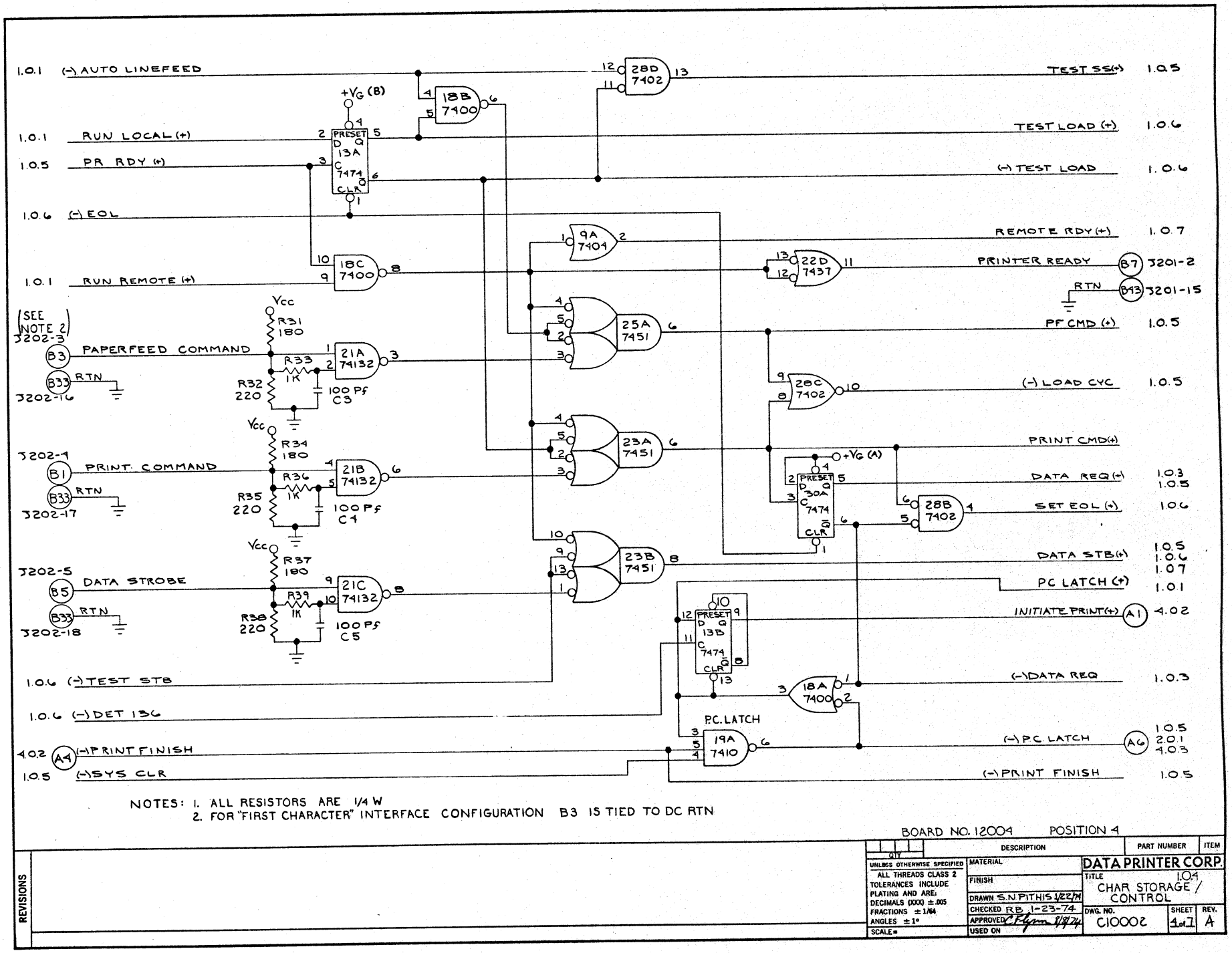
QTY	DESCRIPTION	PART NUMBER	ITEM

UNLESS OTHERWISE SPECIFIED
ALL THREADS CLASS 2
TOLERANCES INCLUDE PLATING AND ARE:
DECIMALS (XXX) ±.005
FRACTIONS ±1/64
ANGLES ±1°
SCALE=

MATERIAL
FINISH
DRAWN Steve N Pitnic
CHECKED RB 1-23-74
APPROVED [illegible] 2/8/74
USED ON

DATA PRINTER CORP.
TITLE 1.0.3 CHAR STORAGE / CONTROL
DWG. NO. C10002
SHEET 3 of 7
REV. A

Figure 1.0.3 Character Storage/Control



NOTES: 1. ALL RESISTORS ARE 1/4 W
2. FOR "FIRST CHARACTER" INTERFACE CONFIGURATION B3 IS TIED TO DC RTN

BOARD NO. 12004 POSITION 4

REVISIONS	QTY	DESCRIPTION	PART NUMBER	ITEM

UNLESS OTHERWISE SPECIFIED: ALL THREADS CLASS 2; TOLERANCES INCLUDE PLATING AND ARE: DECIMALS (XXX) ±.005; FRACTIONS ±1/64; ANGLES ±1°; SCALE=

MATERIAL
FINISH
DRAWN S.N PITHIS 1/22/74
CHECKED RB 1-23-74
APPROVED C.F. Lynn 8/8/74
USED ON

DATA PRINTER CORP.
TITLE 1.0.4 CHAR STORAGE / CONTROL
DWG. NO. C10002
SHEET 1 of 7
REV. A

Figure 1.0.4 Character Storage/Control

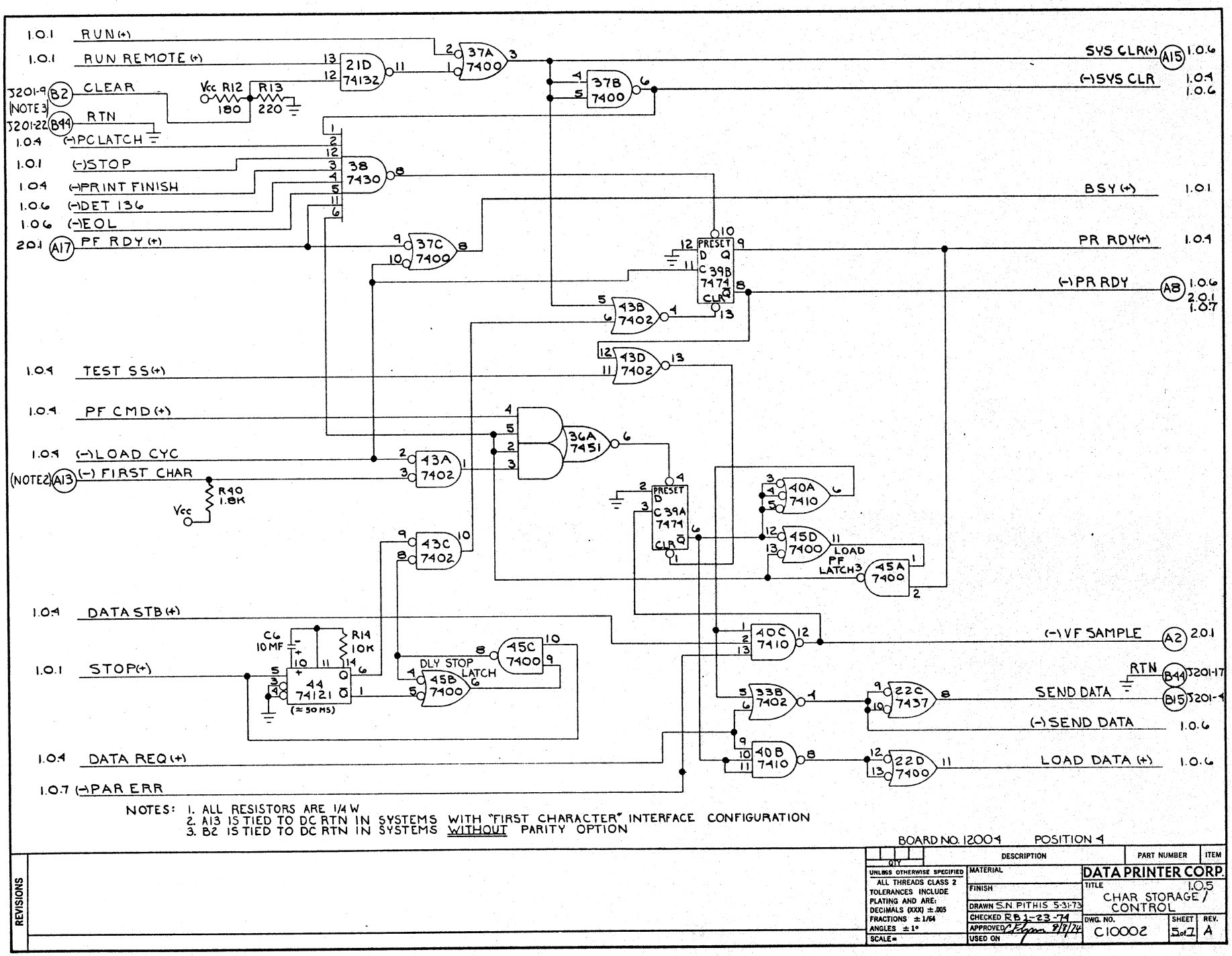
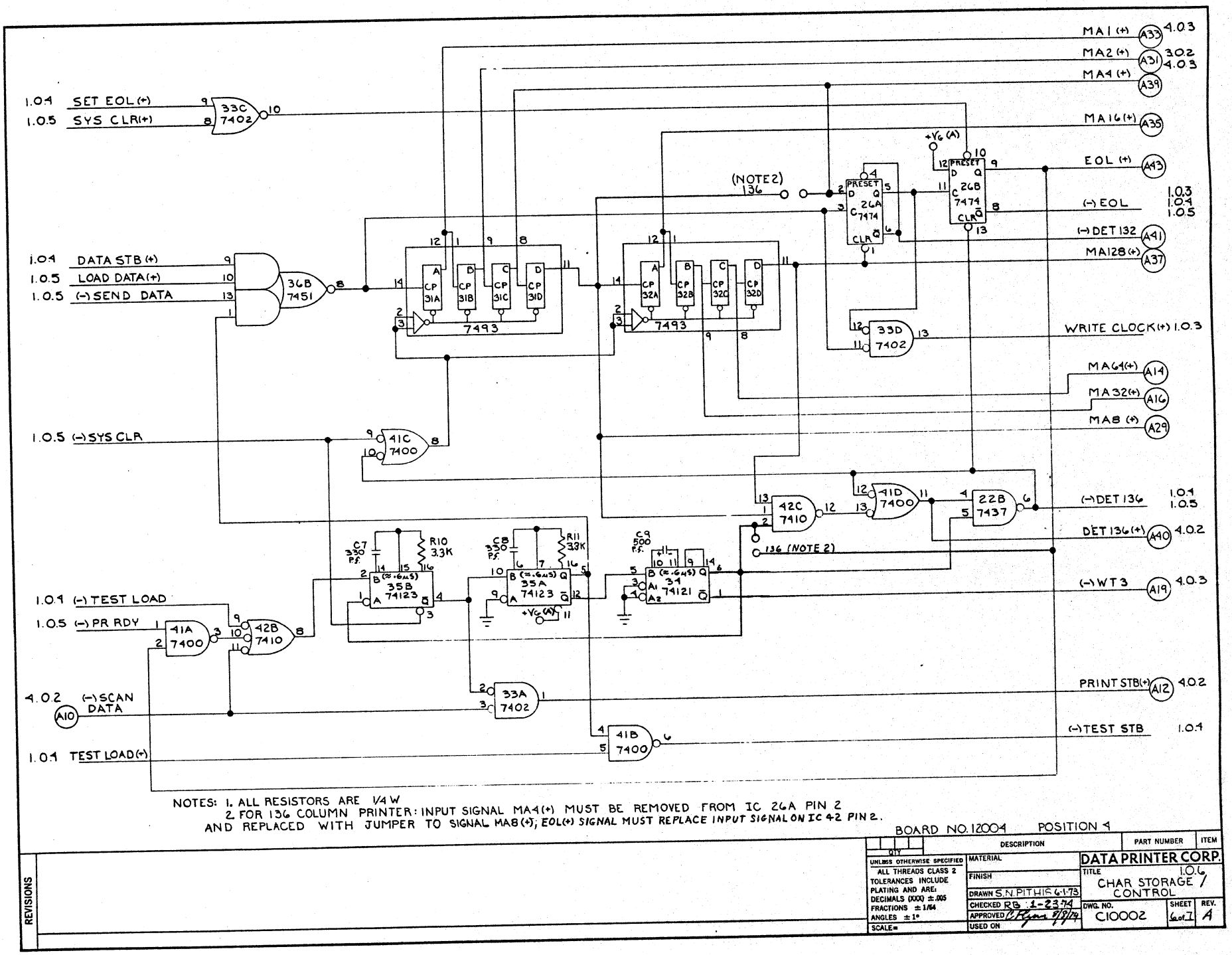


Figure 1.0.5 Character Storage/Control



NOTES: 1. ALL RESISTORS ARE 1/4 W
2. FOR 136 COLUMN PRINTER: INPUT SIGNAL MA4(+) MUST BE REMOVED FROM IC 26A PIN 2 AND REPLACED WITH JUMPER TO SIGNAL MA8(+); EOL(+) SIGNAL MUST REPLACE INPUT SIGNAL ON IC 42 PIN 2.

BOARD NO. 12004 POSITION 4

QTY	DESCRIPTION	PART NUMBER	ITEM

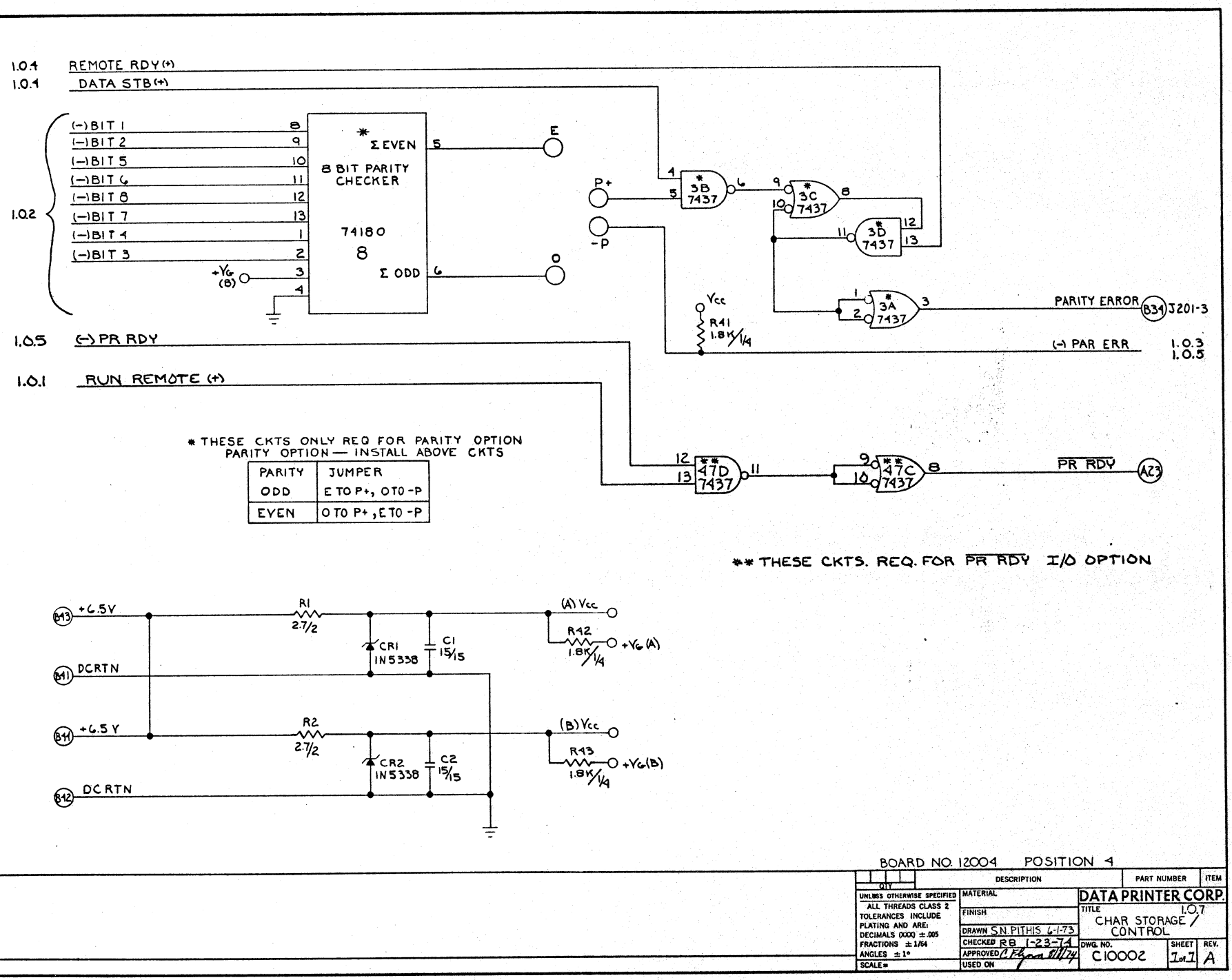
UNLESS OTHERWISE SPECIFIED
ALL THREADS CLASS 2
TOLERANCES INCLUDE PLATING AND ARE:
DECIMALS (XXX) ±.005
FRACTIONS ±1/64
ANGLES ±1°
SCALE=

MATERIAL
FINISH
DRAWN S.N. PITHIS 6-1-73
CHECKED RB 1-23-74
APPROVED C. Ryan 9/9/74
USED ON

DATA PRINTER CORP.
TITLE 1.0.6 CHAR STORAGE / CONTROL
DWG. NO. C10002
SHEET 6 of 7
REV. A

REVISIONS

78 **Figure 1.0.6 Character Storage/Control**



BOARD NO. 12004 POSITION 4

REVISIONS

QTY	DESCRIPTION	PART NUMBER	ITEM

UNLESS OTHERWISE SPECIFIED
ALL THREADS CLASS 2
TOLERANCES INCLUDE PLATING AND ARE:
DECIMALS (XXX) ±.005
FRACTIONS ±1/64
ANGLES ±1°
SCALE=

MATERIAL
FINISH
DRAWN S.N. PITHIS 6-1-73
CHECKED RB 1-23-74
APPROVED
USED ON

DATA PRINTER CORP.
TITLE 1.0.7 CHAR STORAGE / CONTROL
DWG. NO. C10002
SHEET 1 of 1
REV. A

Figure 1.0.7 Character Storage/Control

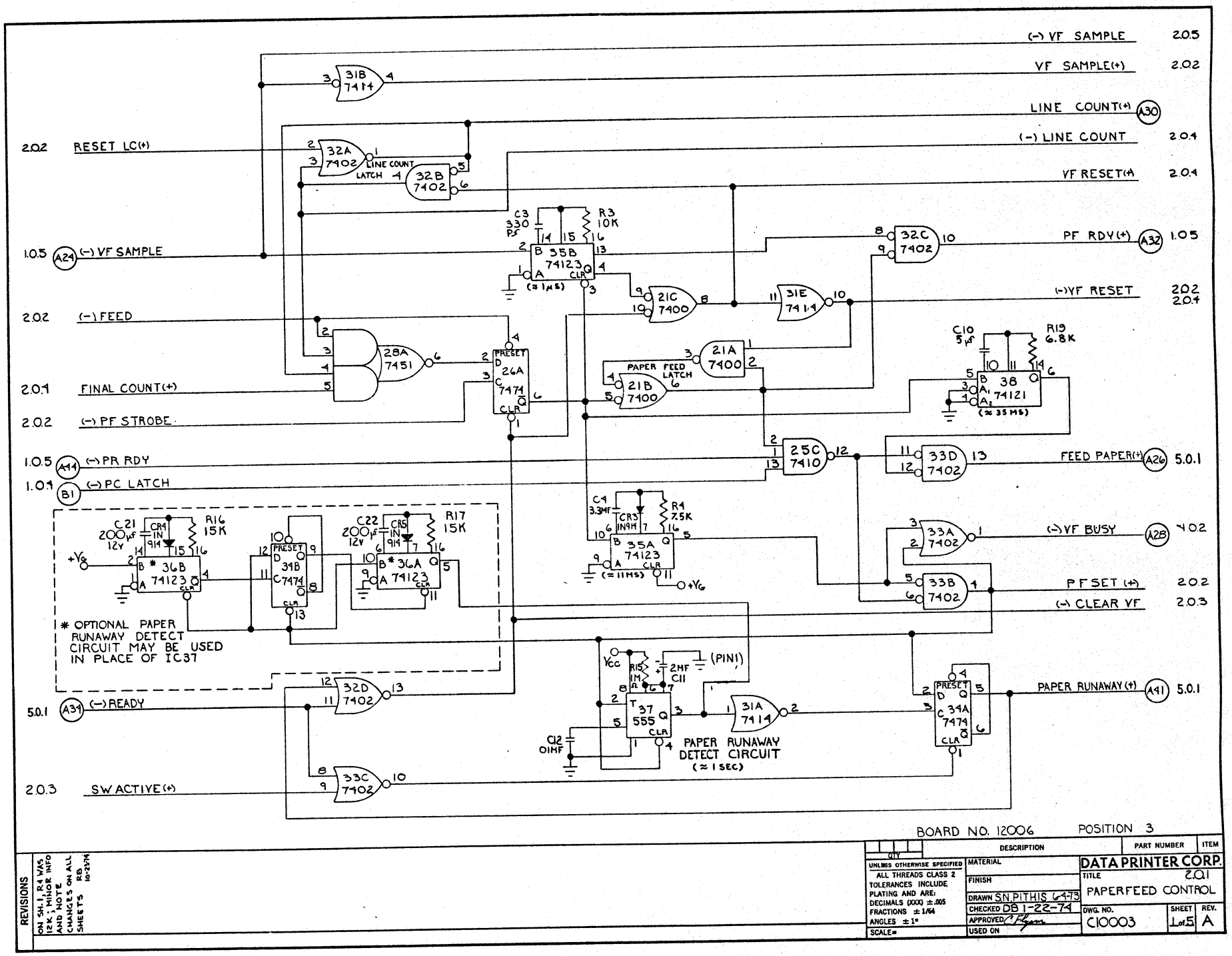


Figure 2.0.1 Paperfeed Control

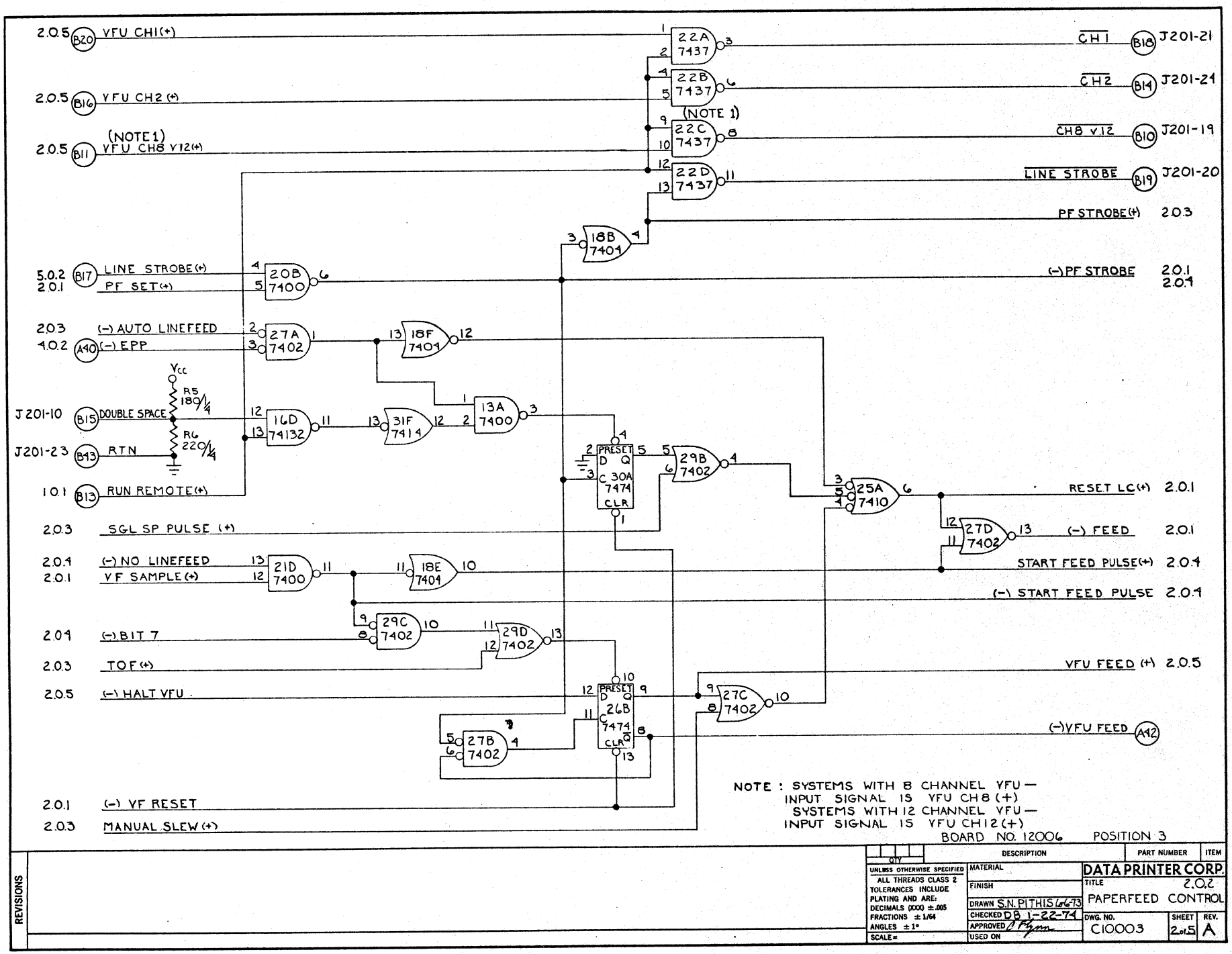


Figure 2.0.2 Paperfeed Control

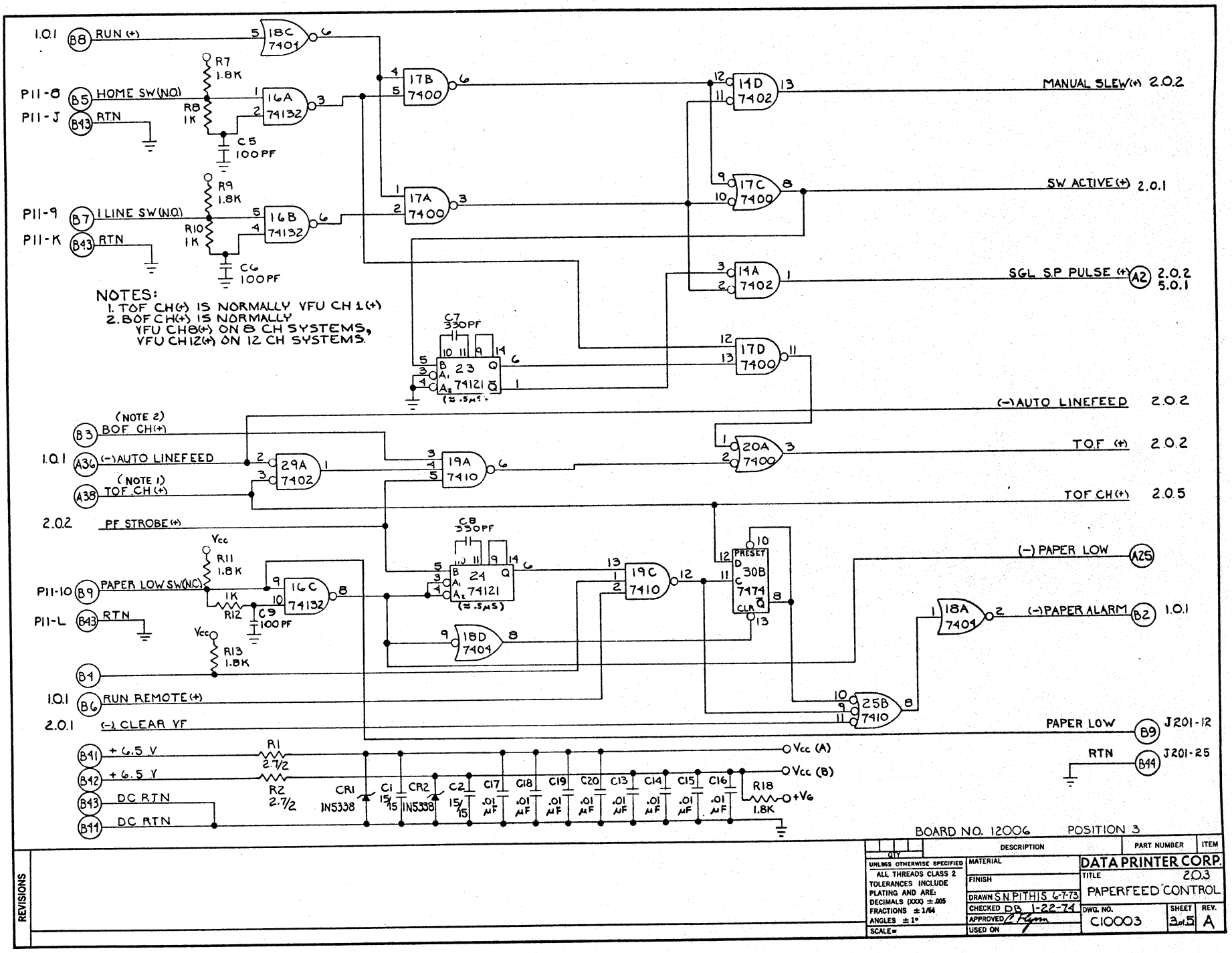


Figure 2.0.3 Paperfeed Control

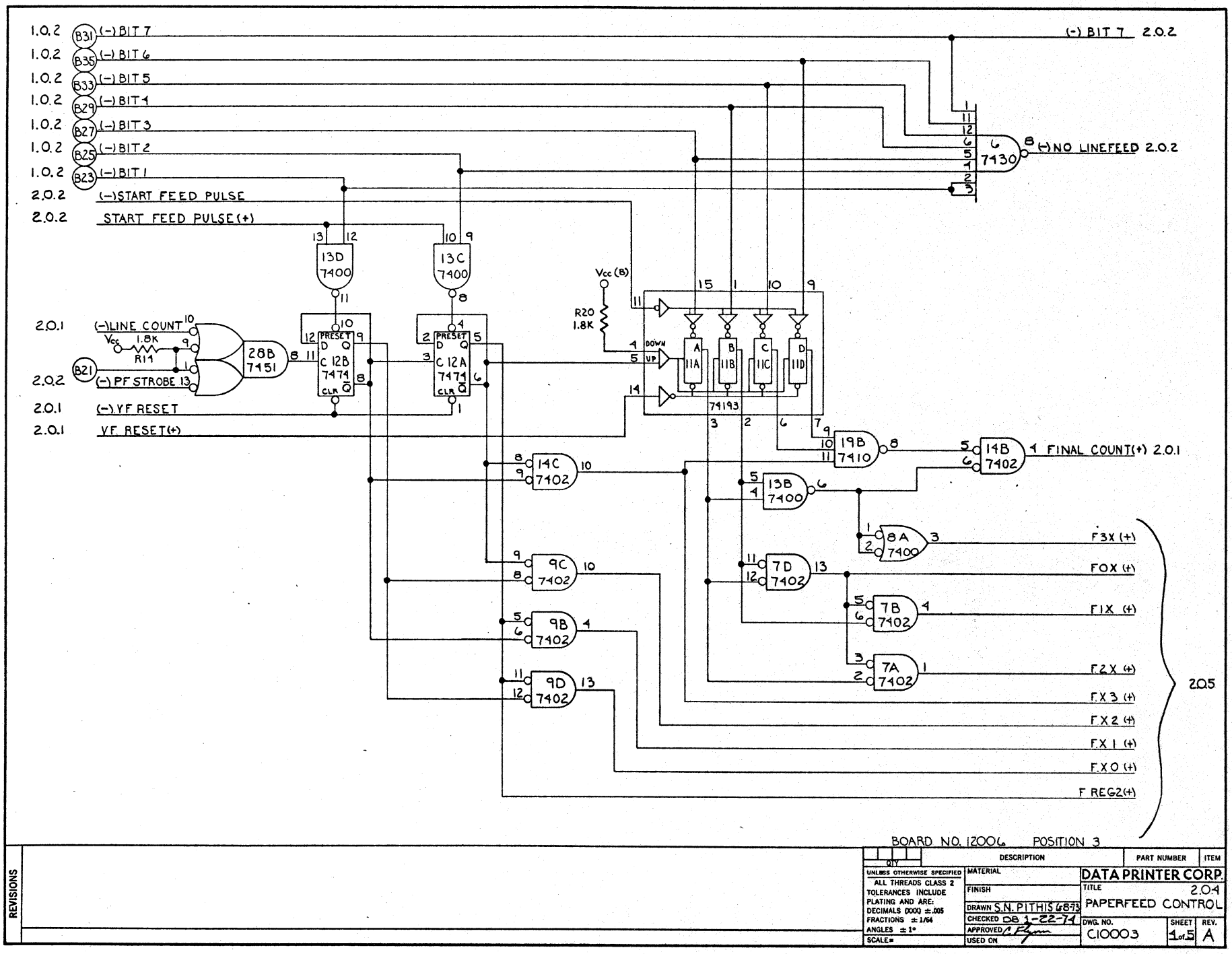


Figure 2.0.4 Paperfeed Control

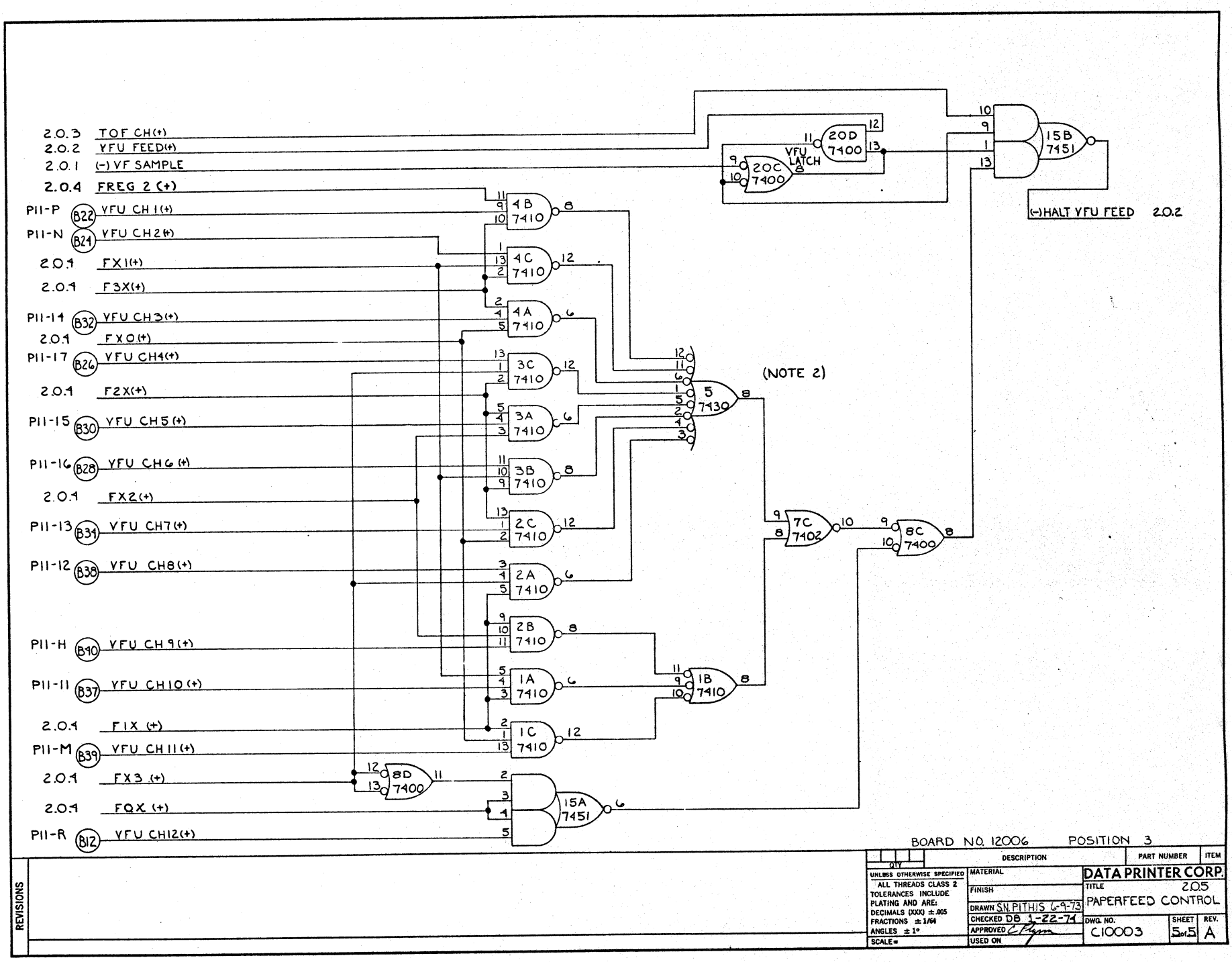


 Figure 2.0.5 Paperfeed Control

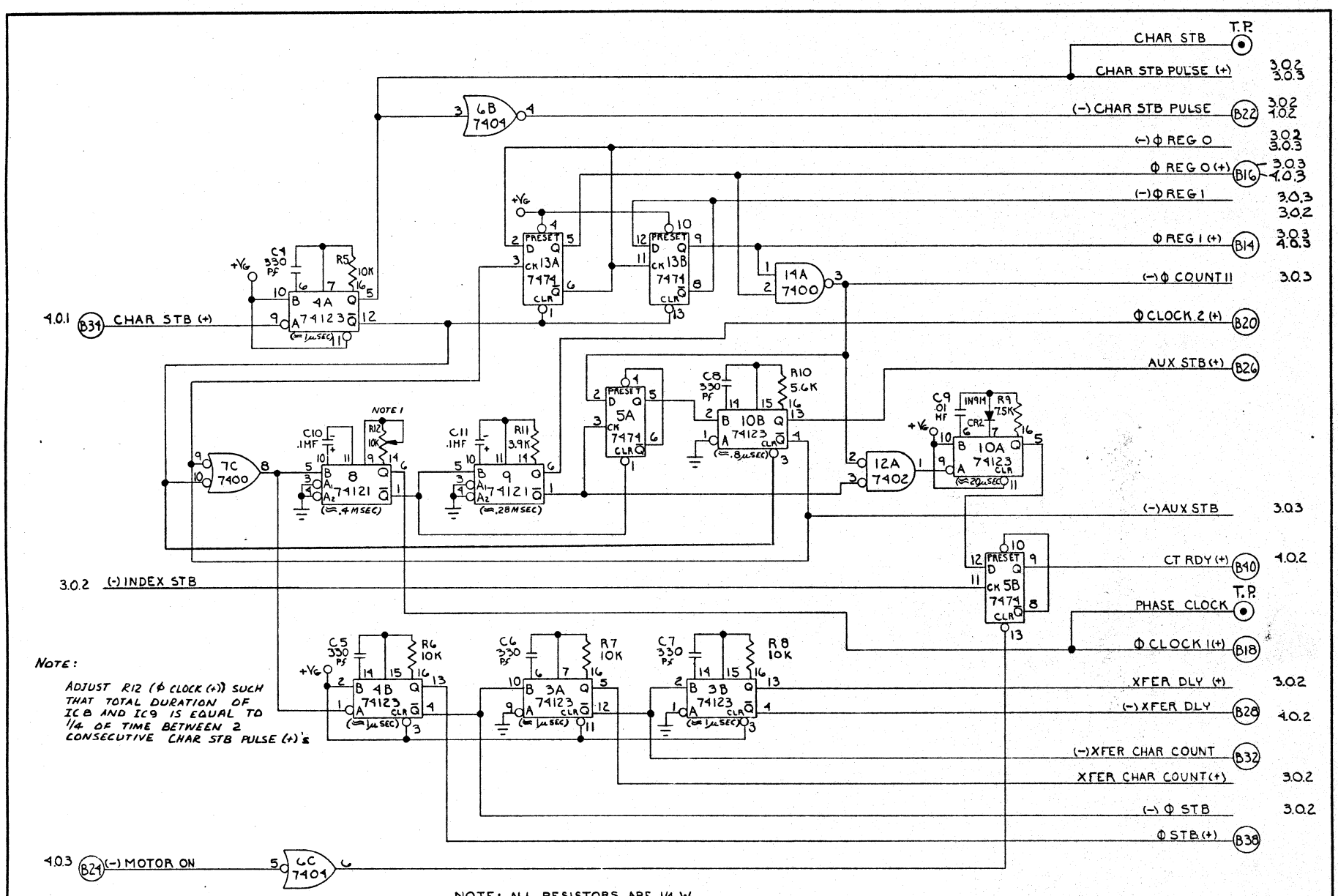
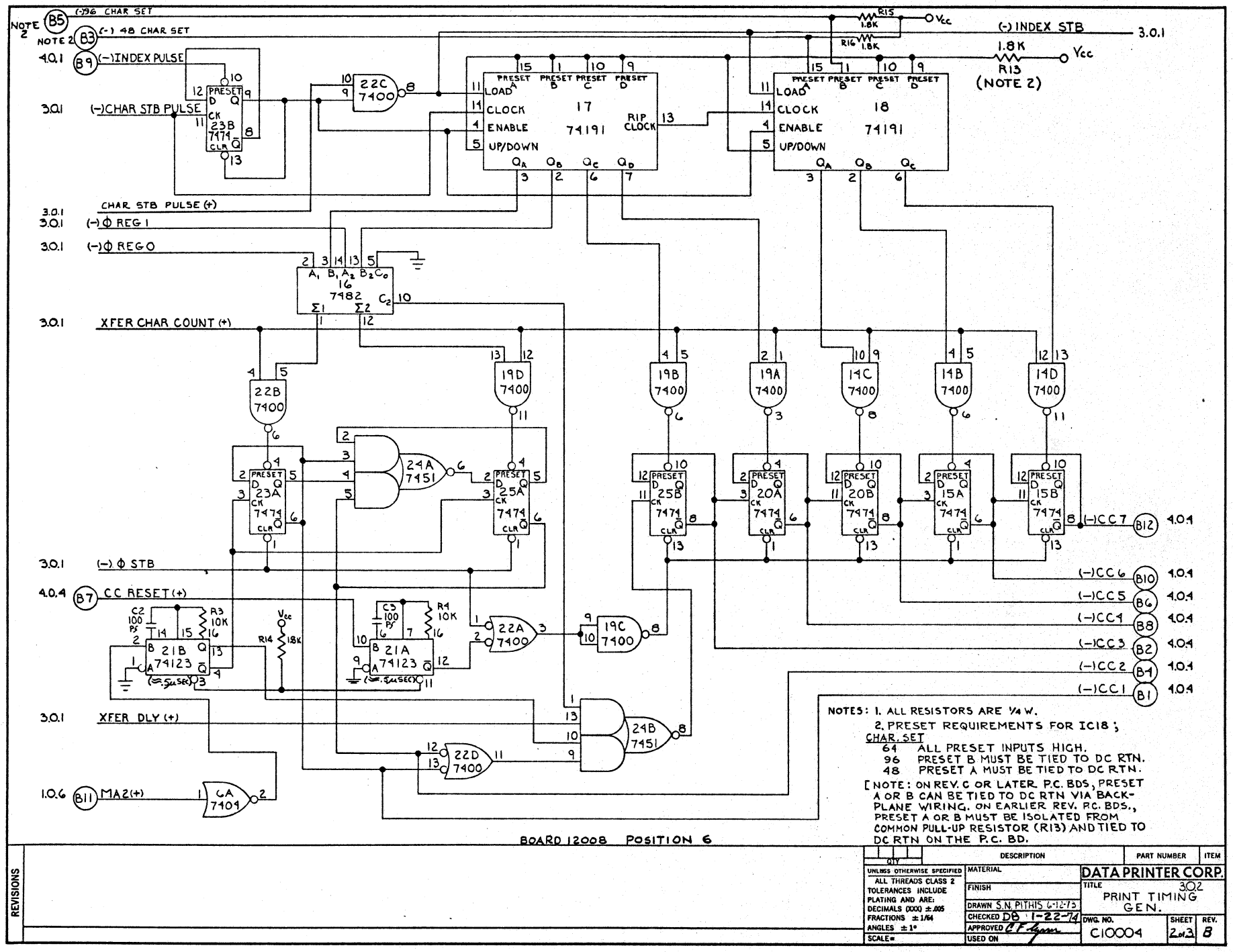


Figure 3.0.1 Print Timing Generator



86 **Figure 3.0.2 Print Timing Generator**

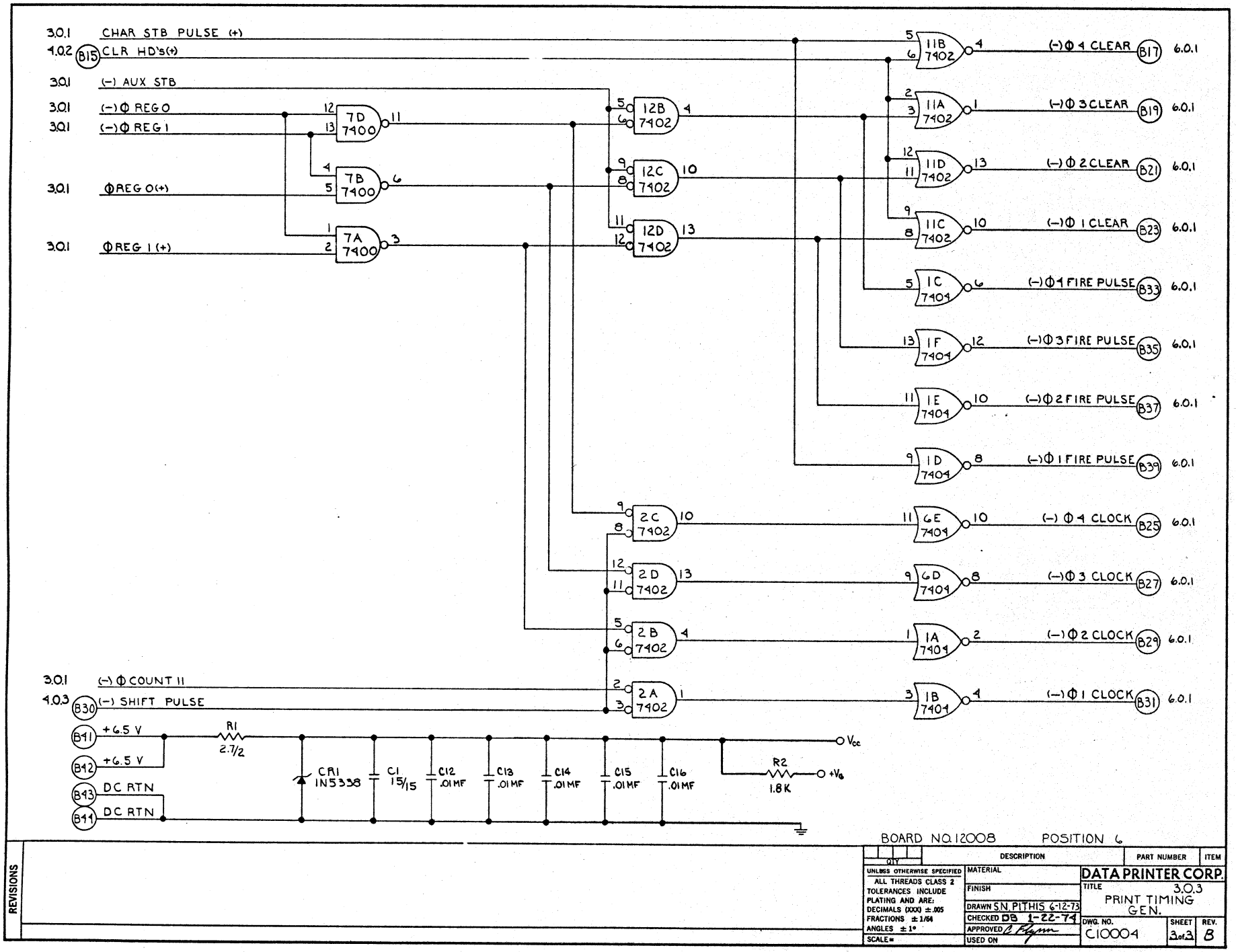


Figure 3.0.3 Print Timing Generator

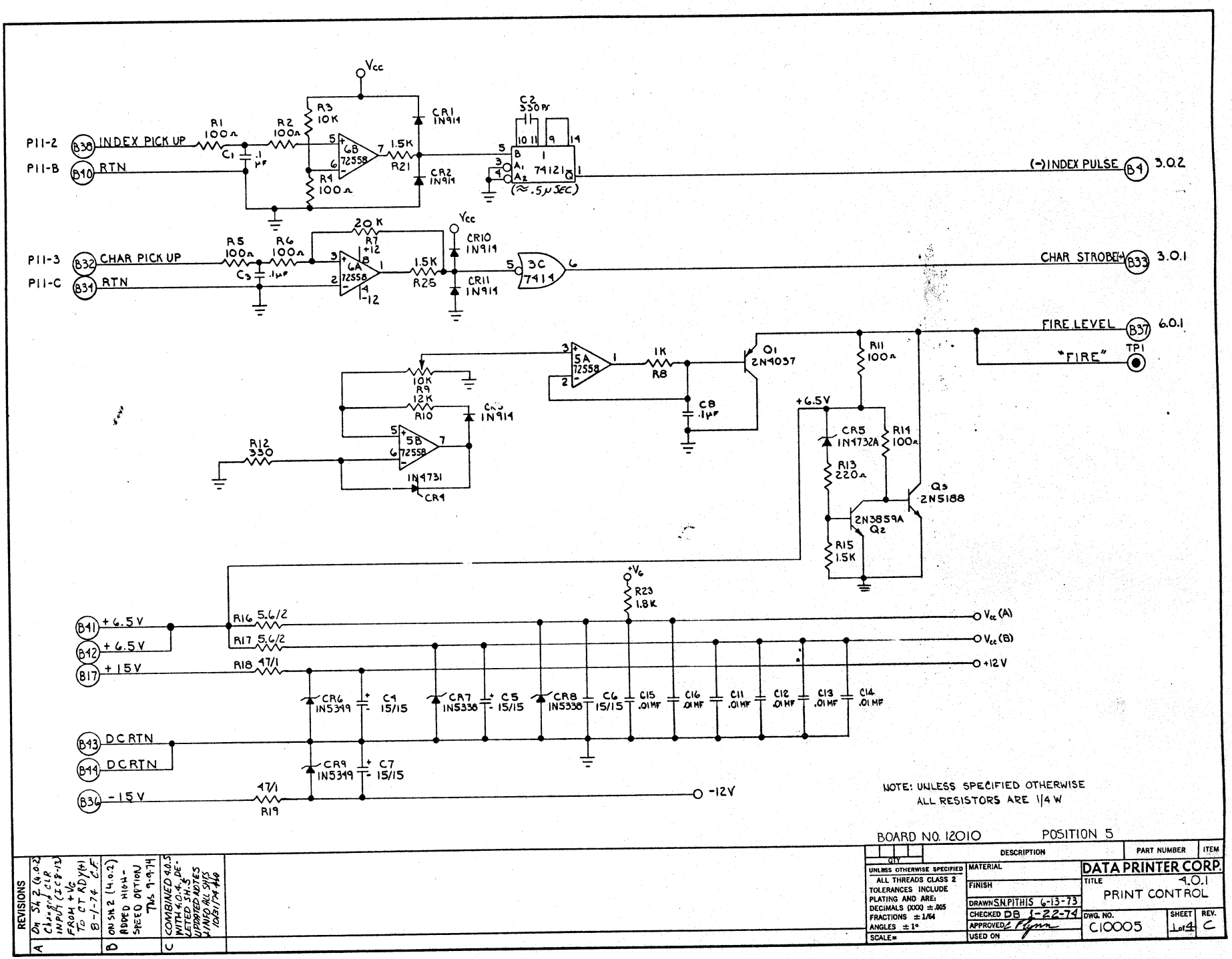


Figure 4.0.1 Print Control

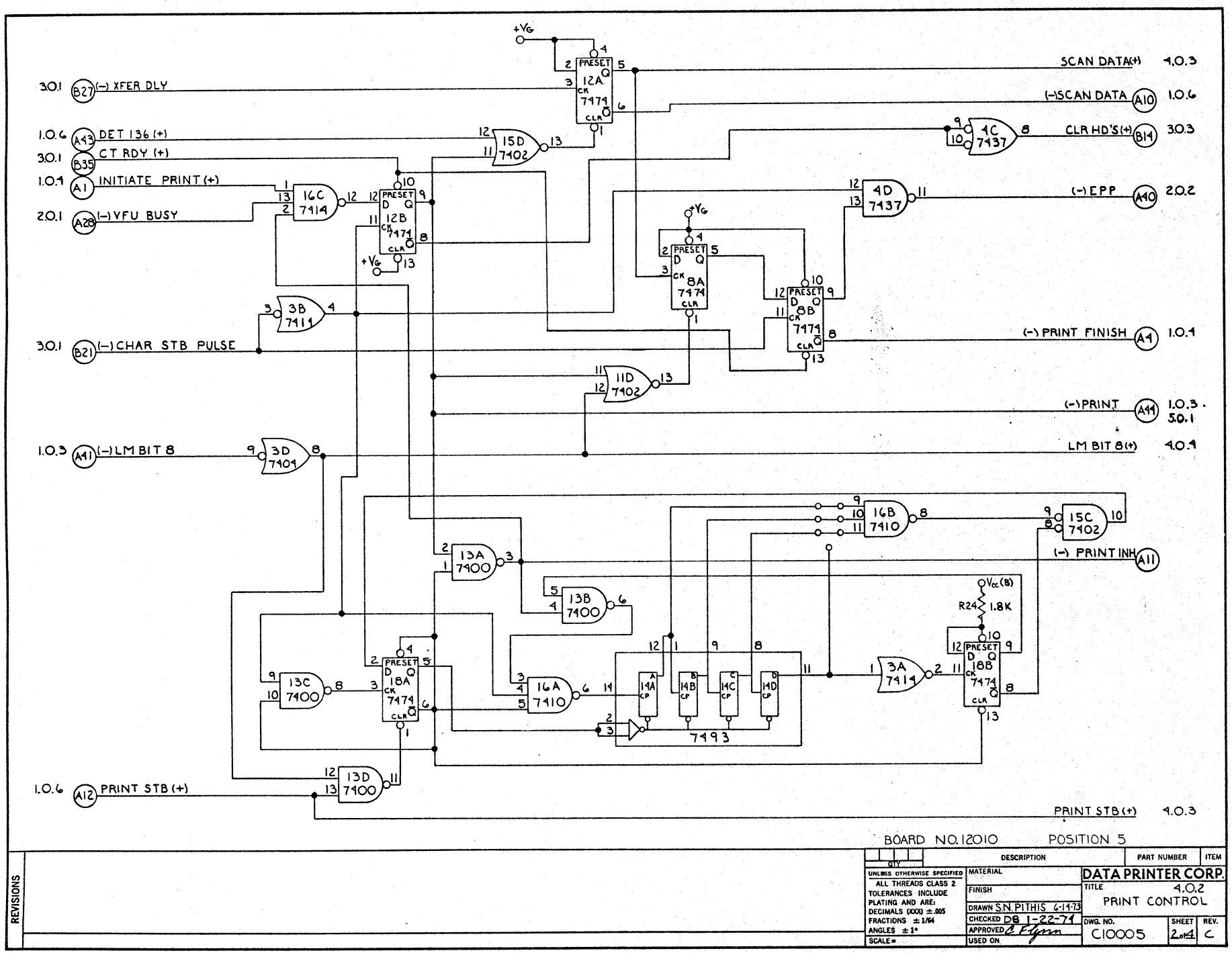


Figure 4.0.2 Print Control

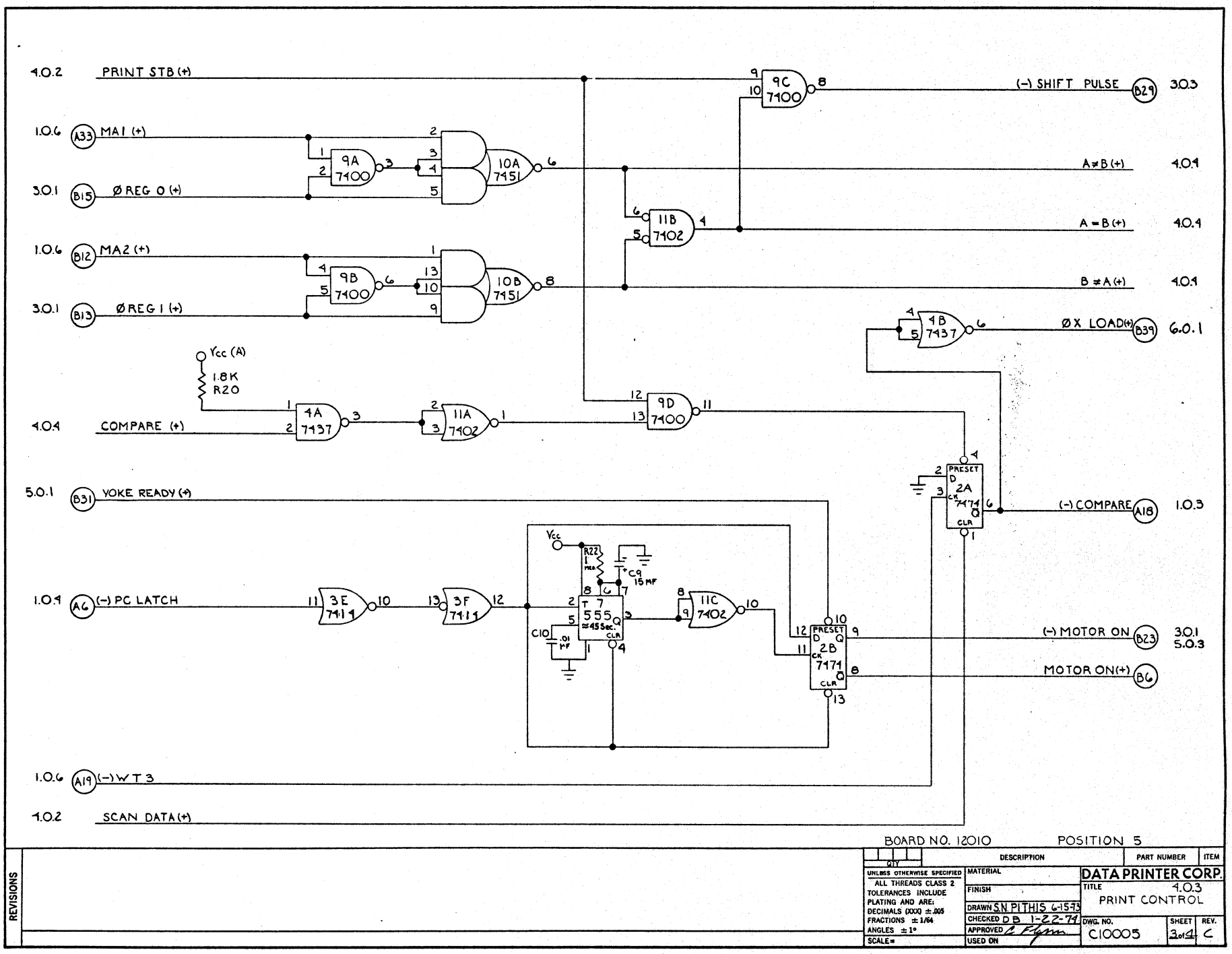


 Figure 4.0.3 Print Control

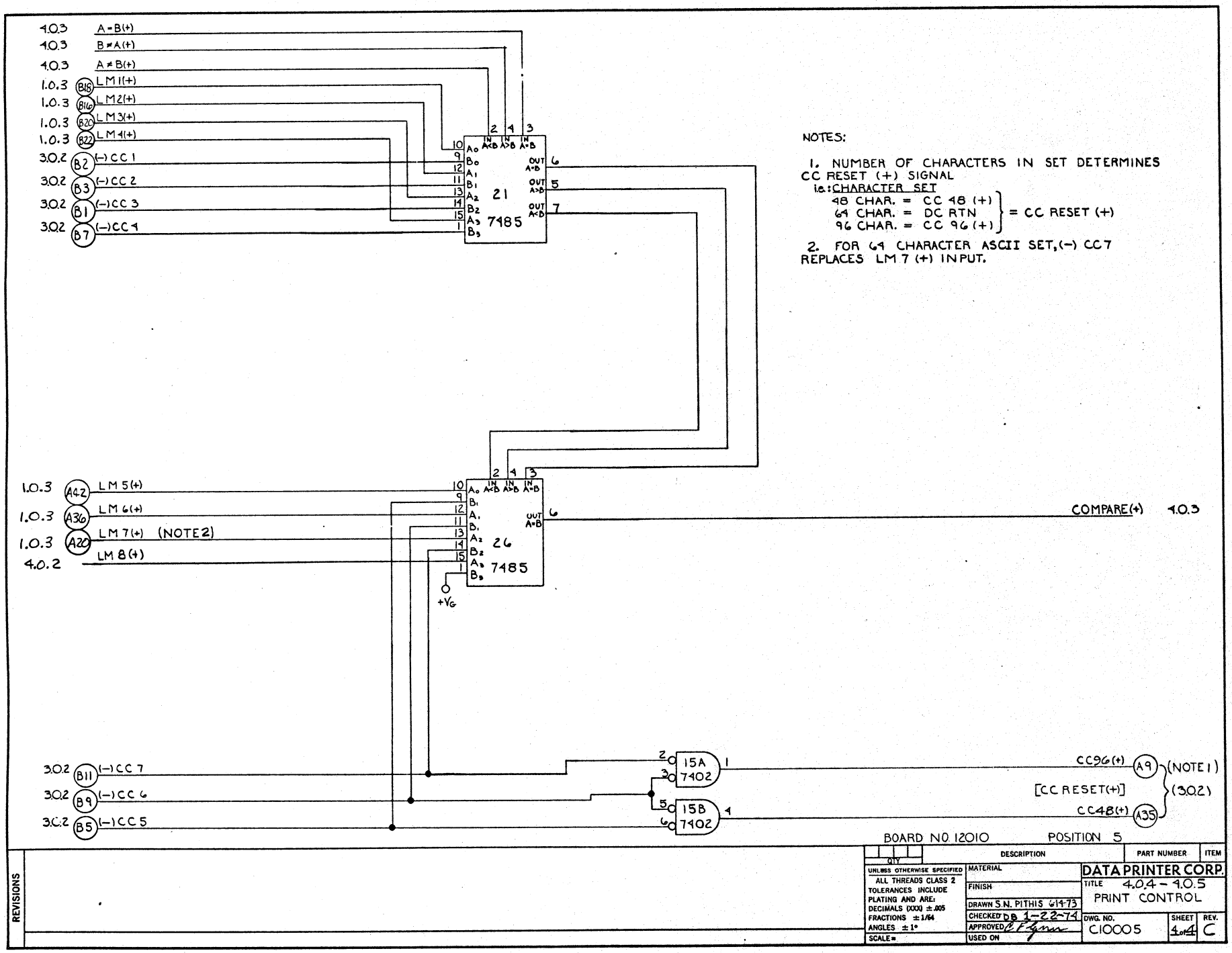


Figure 4.0.4 Print Control

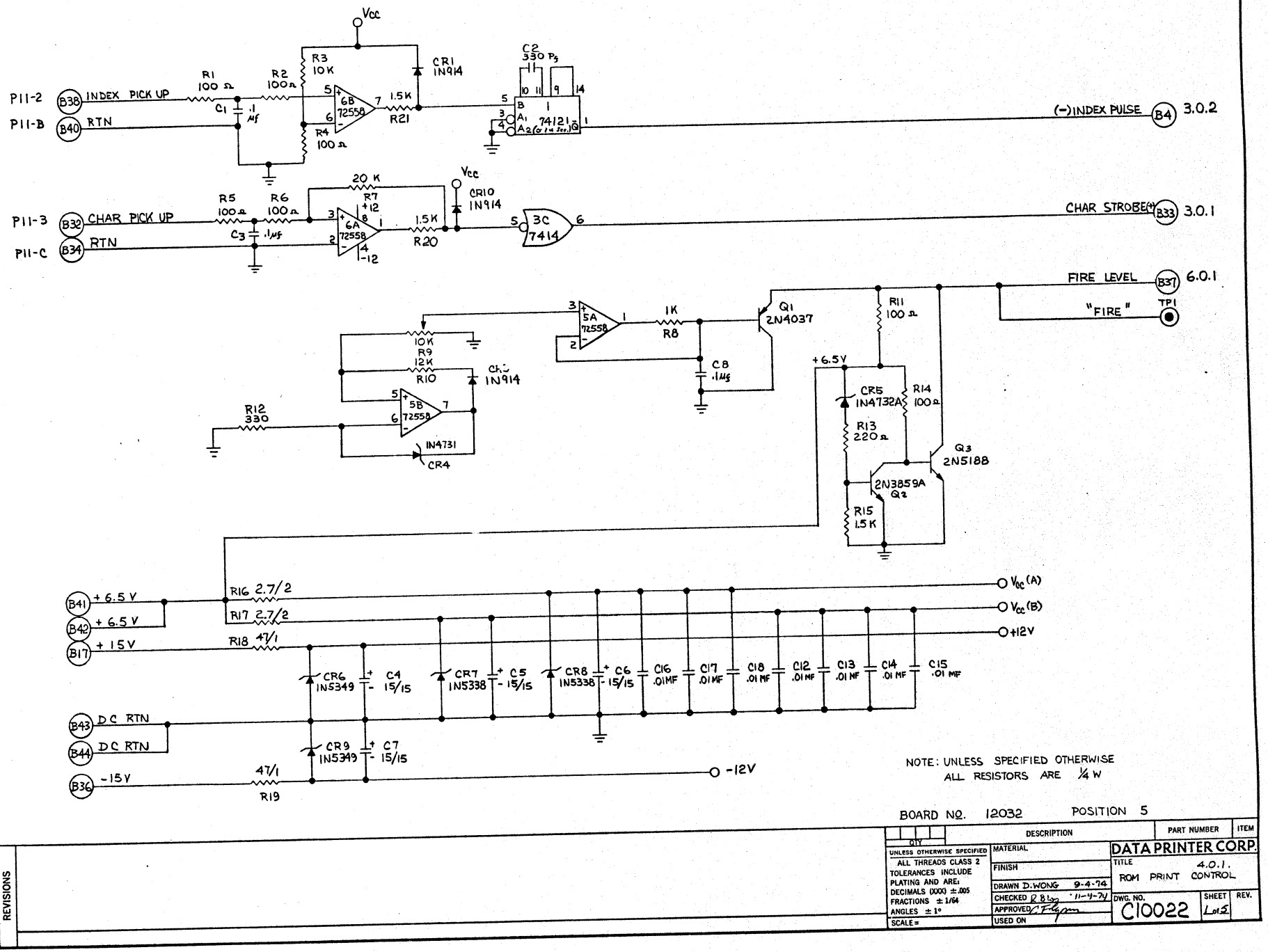


Figure 4.0.1 ROM Print Control

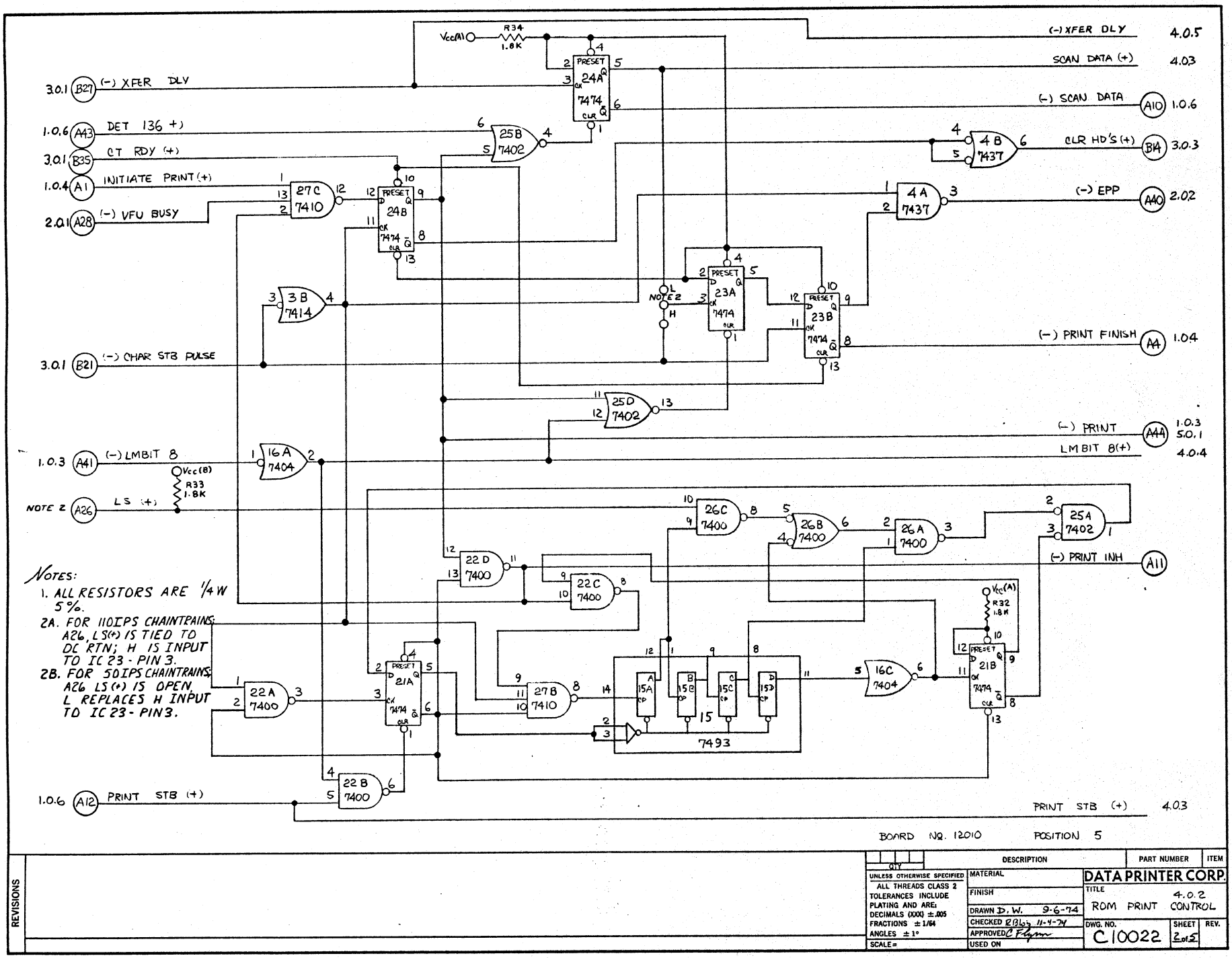
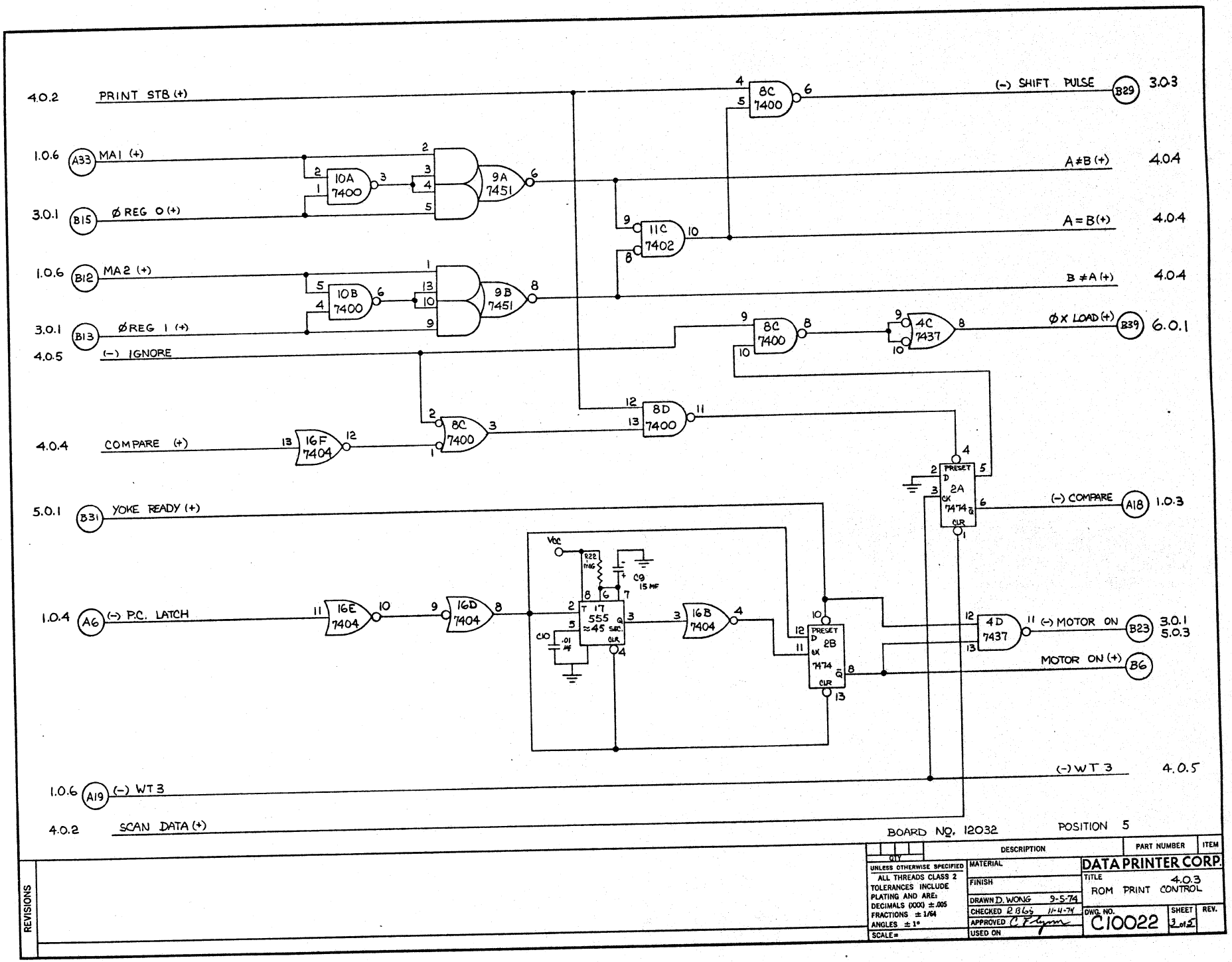


Figure 4.0.2 ROM Print Control



94 **Figure 4.0.3 ROM Print Control**

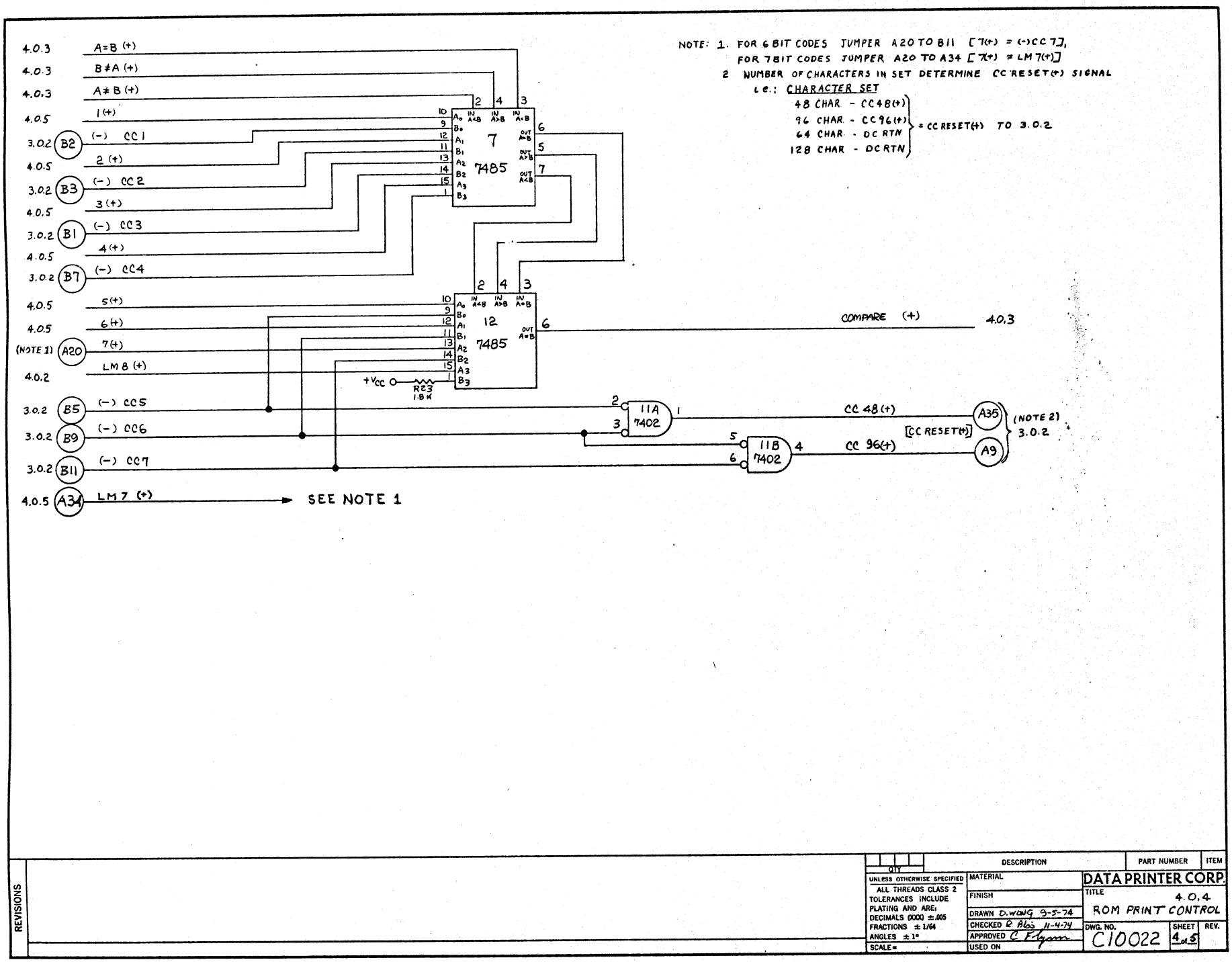
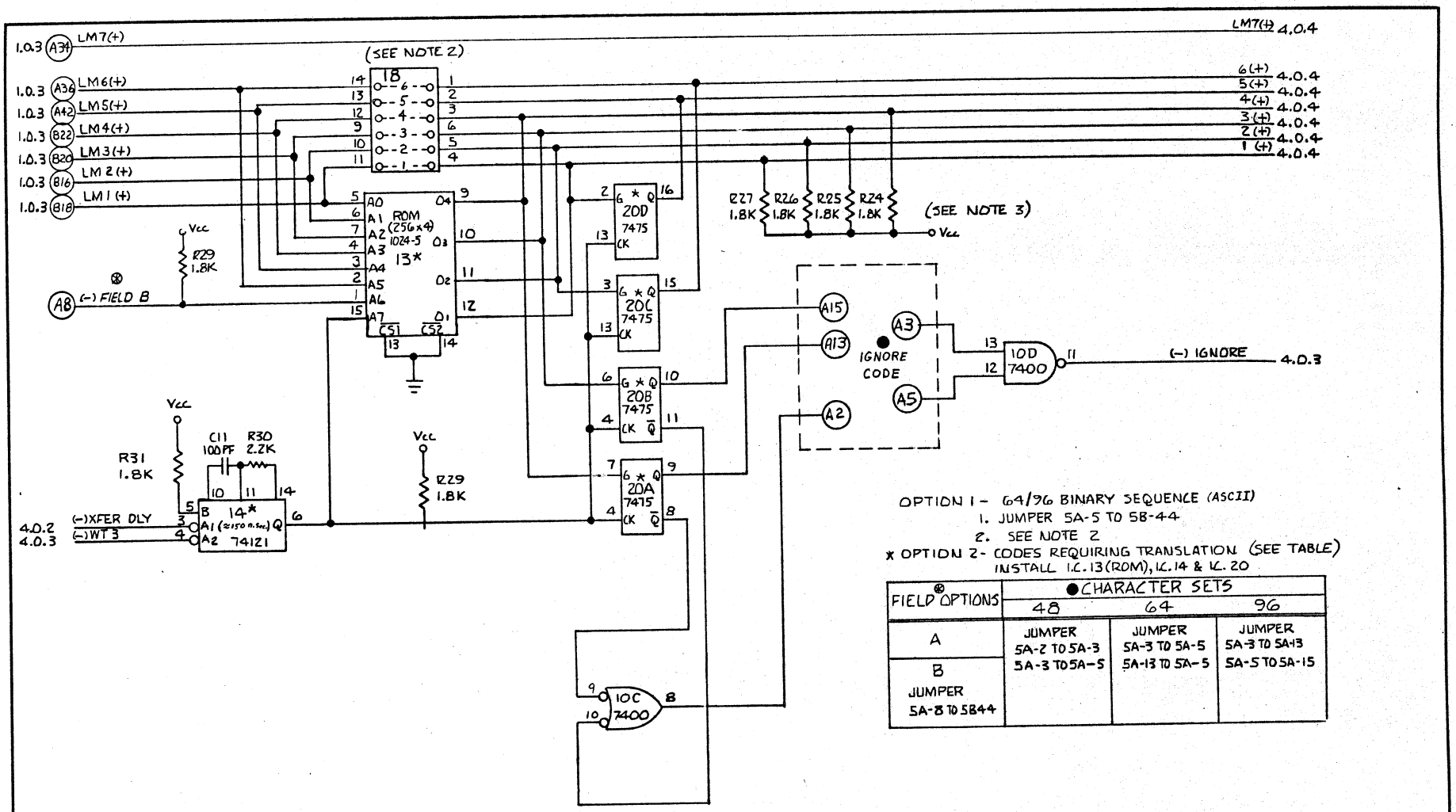


Figure 4.0.4 ROM Print Control



FIELD ⊗ OPTIONS	● CHARACTER SETS		
	48	64	96
A	JUMPER 5A-2 TO 5A-3, 5A-3 TO 5A-5	JUMPER 5A-3 TO 5A-5, 5A-13 TO 5A-5	JUMPER 5A-3 TO 5A-13, 5A-5 TO 5A-15
B JUMPER 5A-8 TO 5B44			

Figure 4.0.5 ROM Print Control

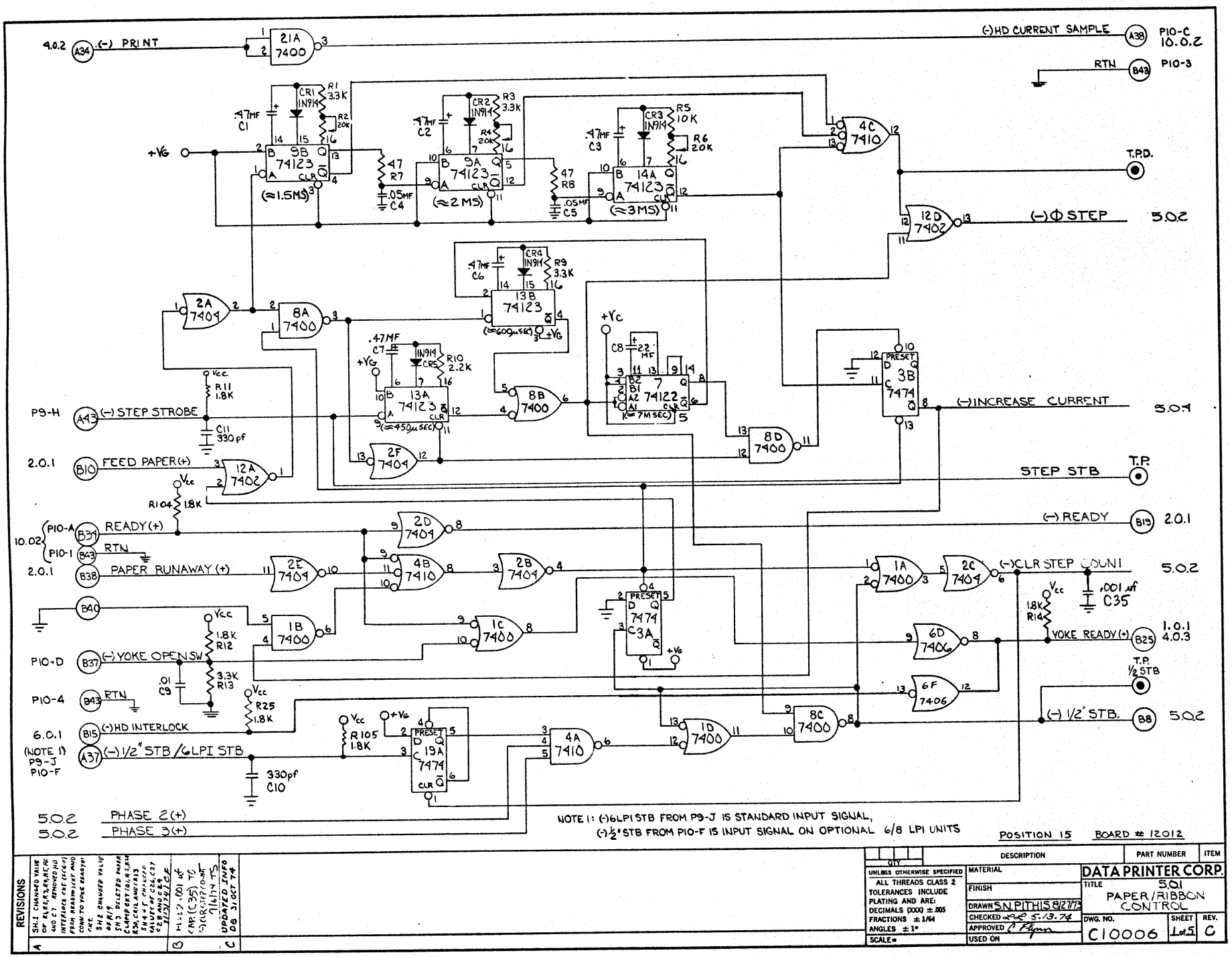
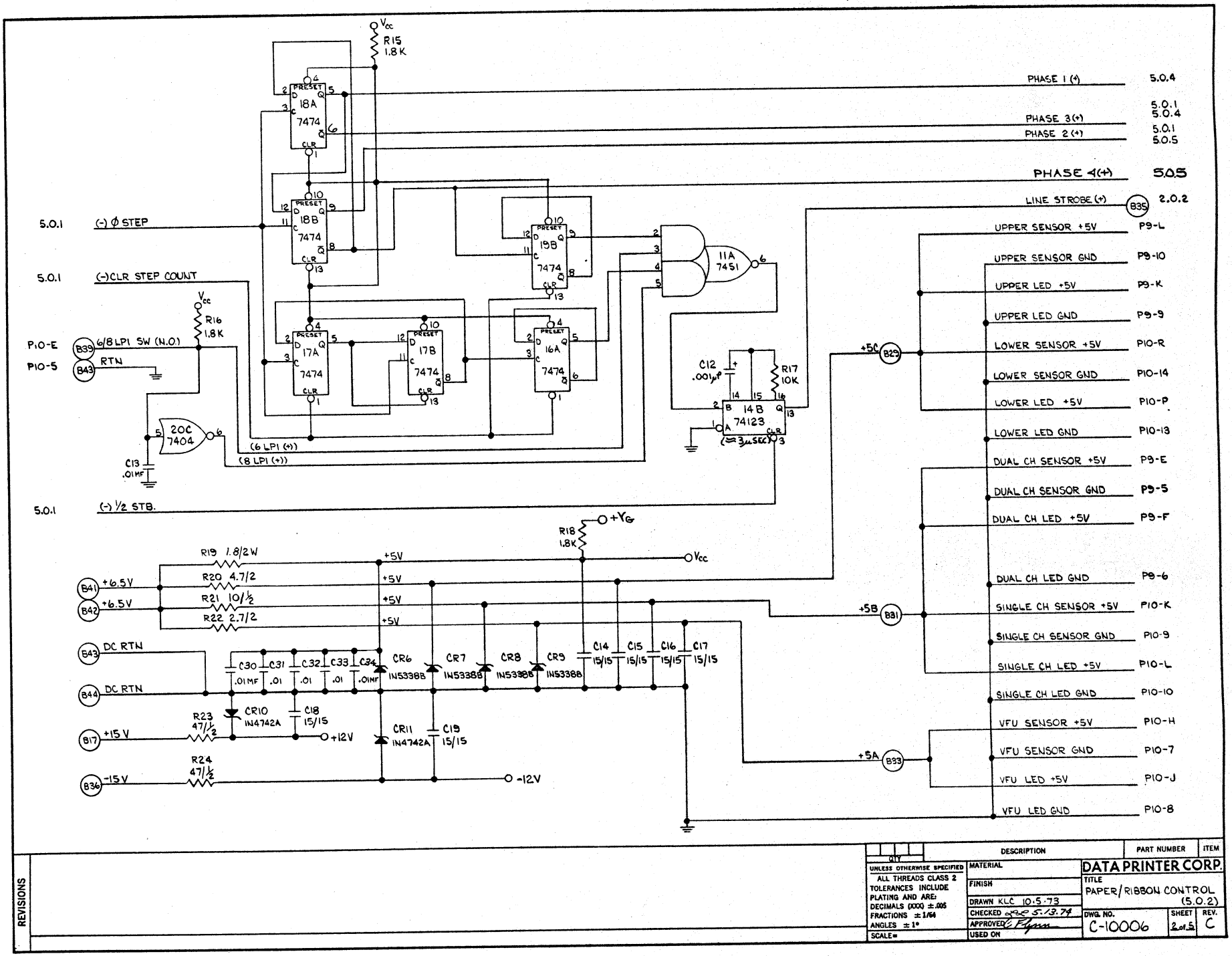


Figure 5.0.1 Paper/Ribbon Control



98 **Figure 5.0.2 Paper/Ribbon Control**

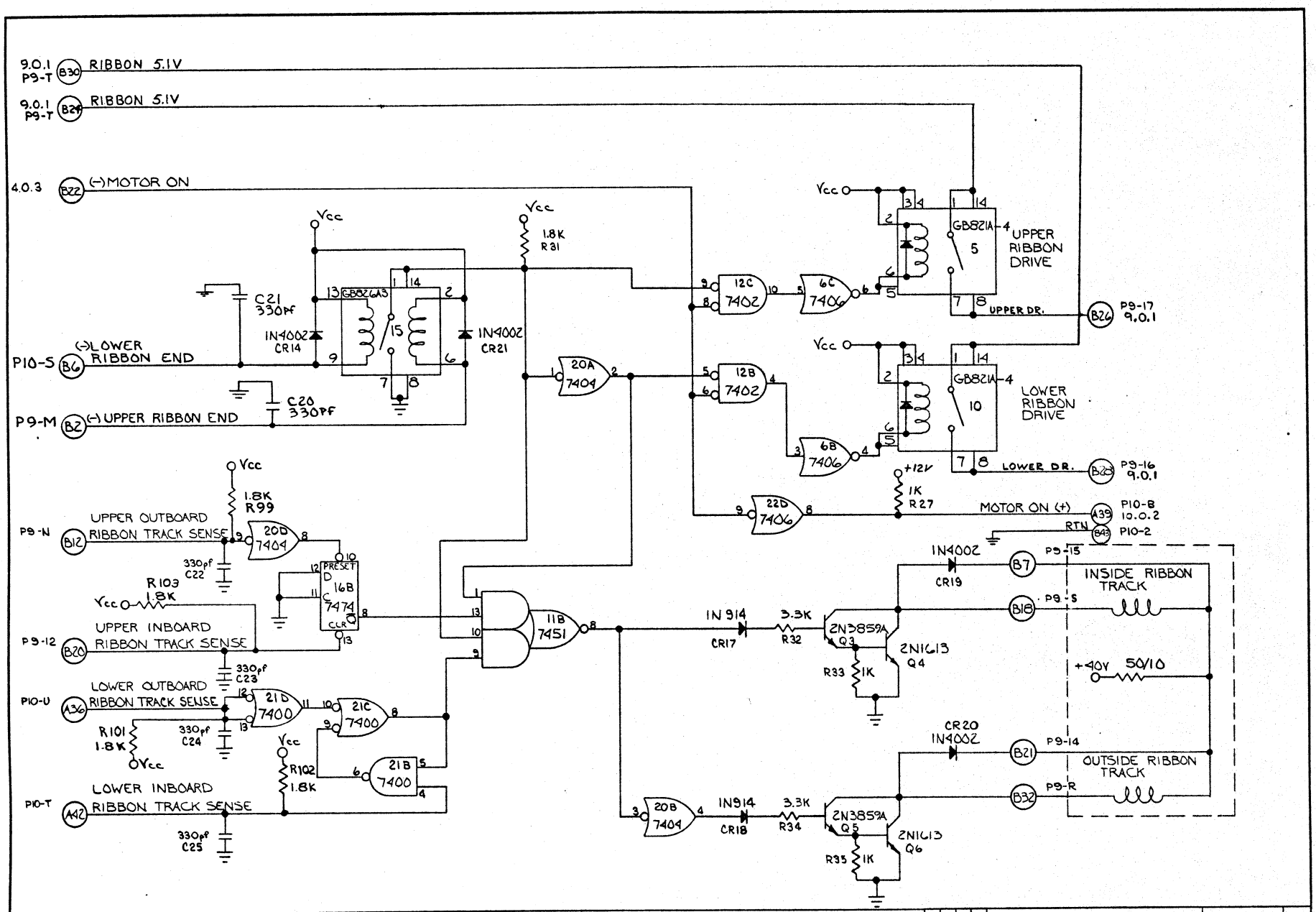
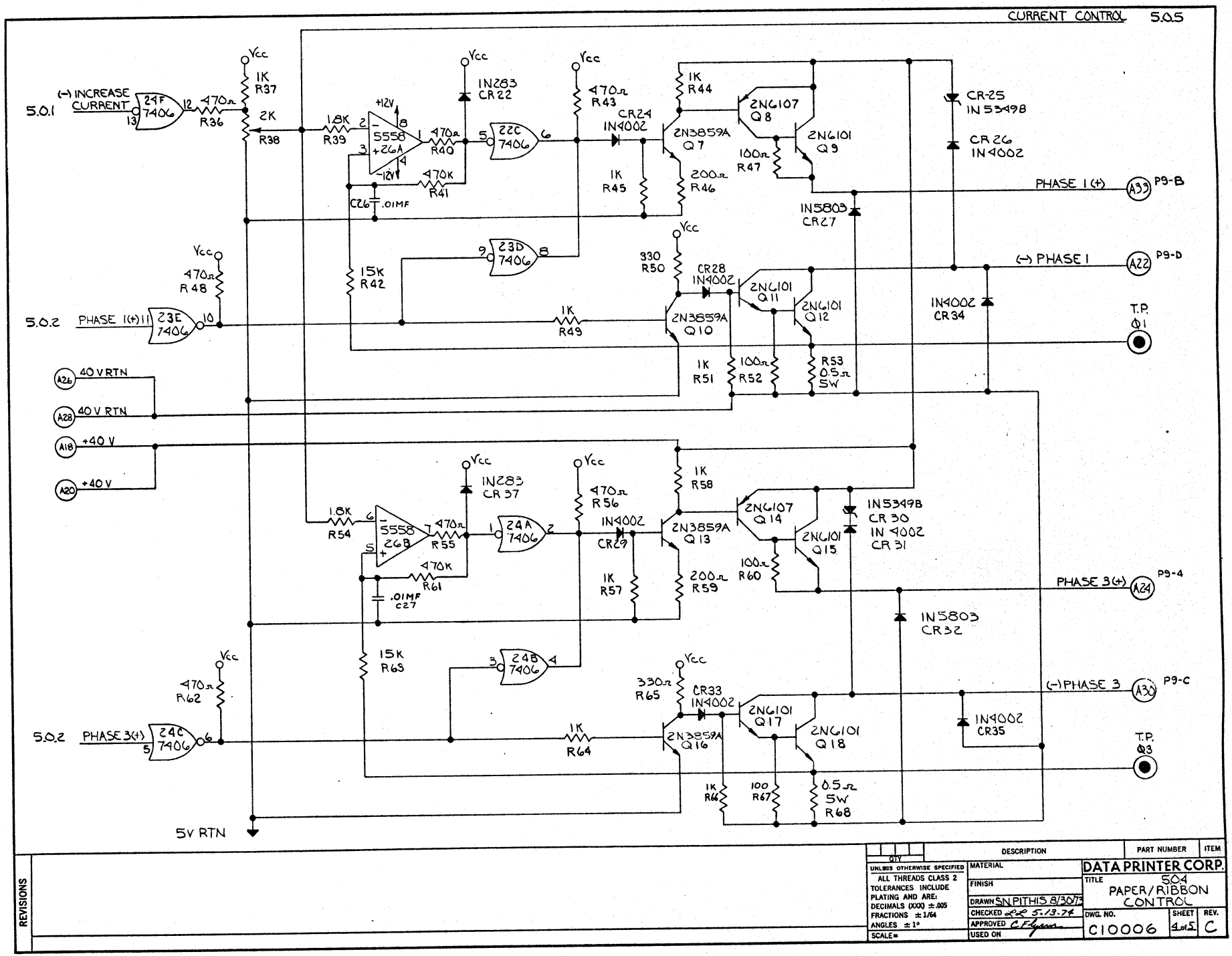


Figure 5.0.3 Paper/Ribbon Control



100 **Figure 5.0.4 Paper/Ribbon Control**

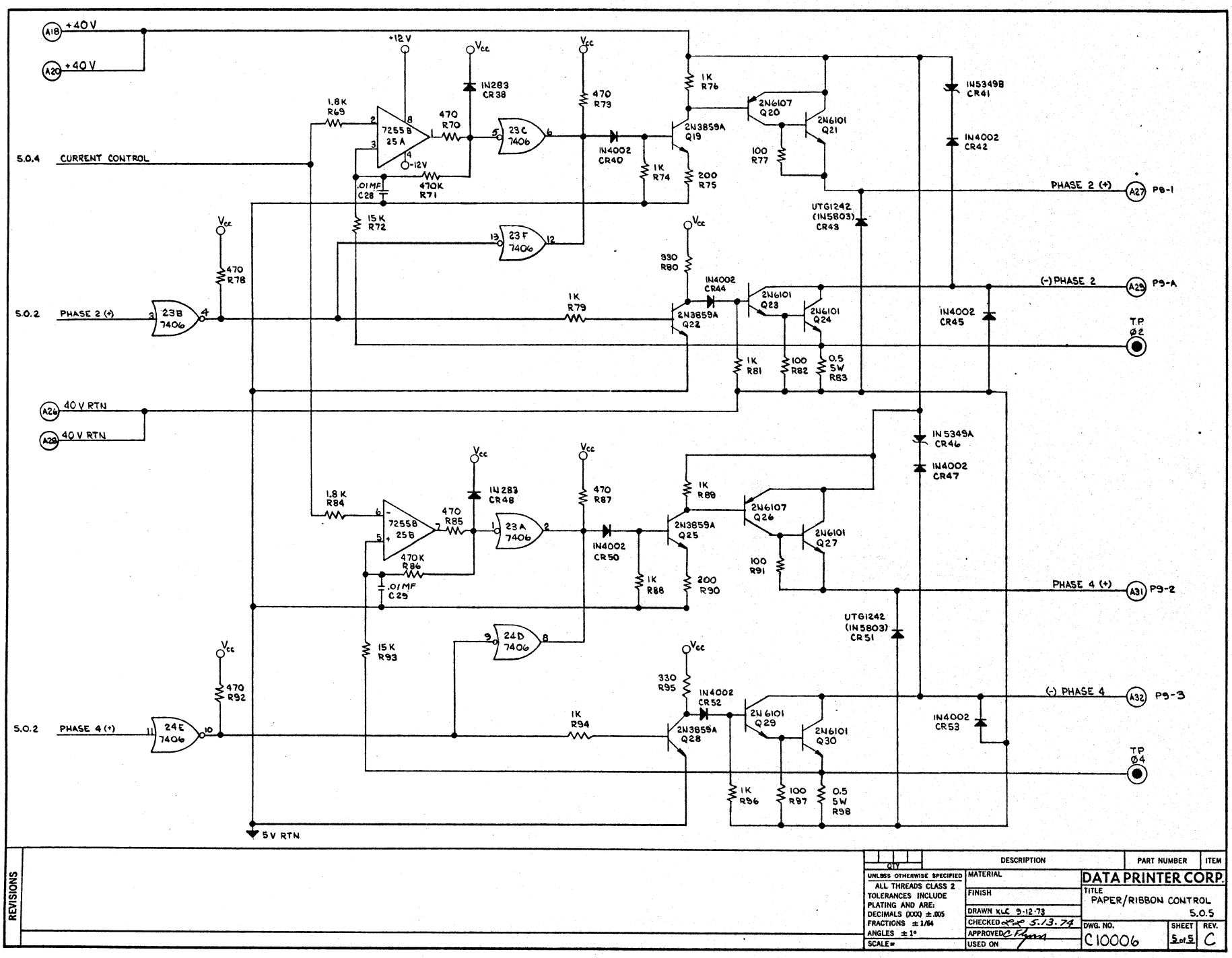


Figure 5.0.5 Paper/Ribbon Control

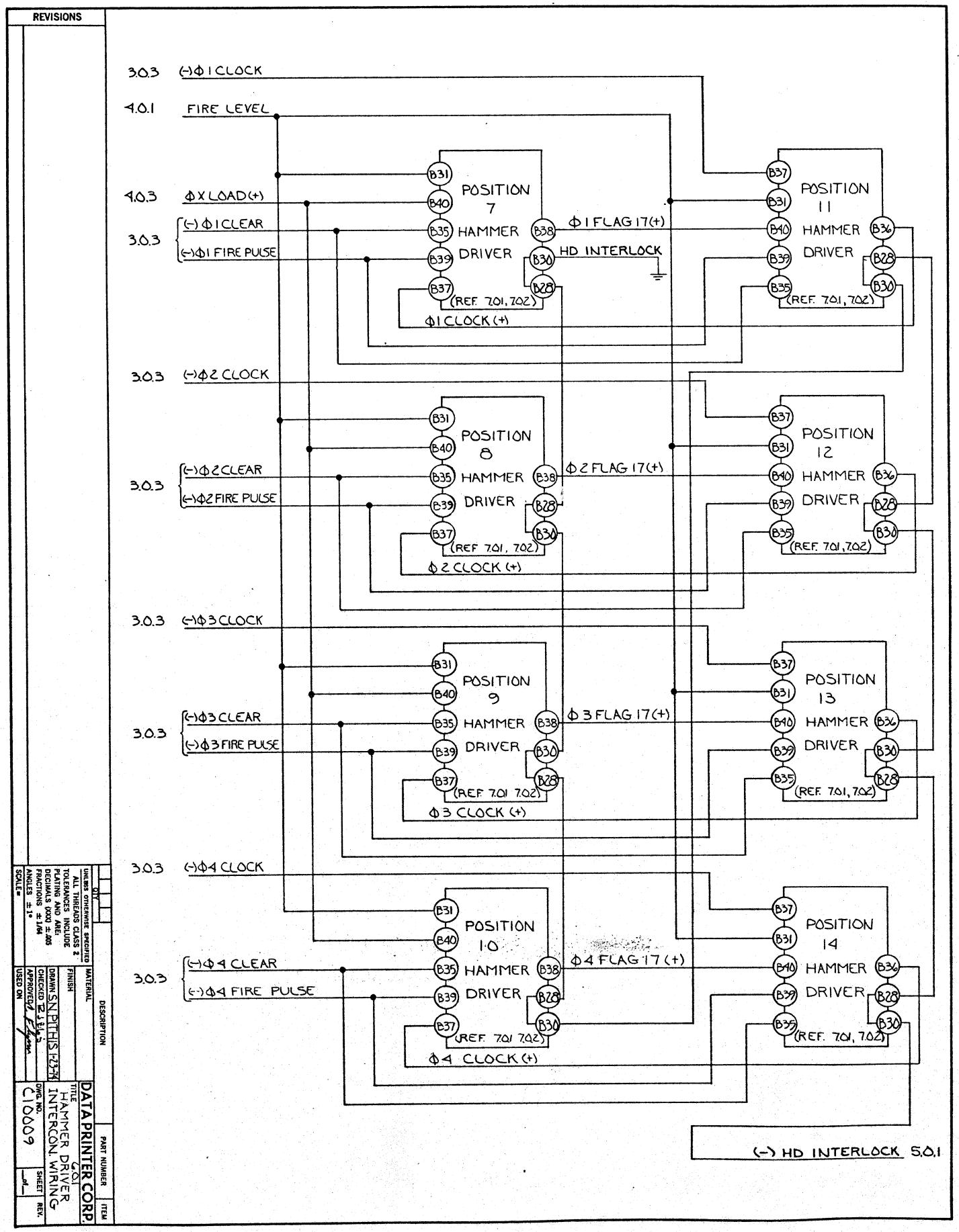


Figure 6.0.1 Hammer Driver Interconnector Wiring

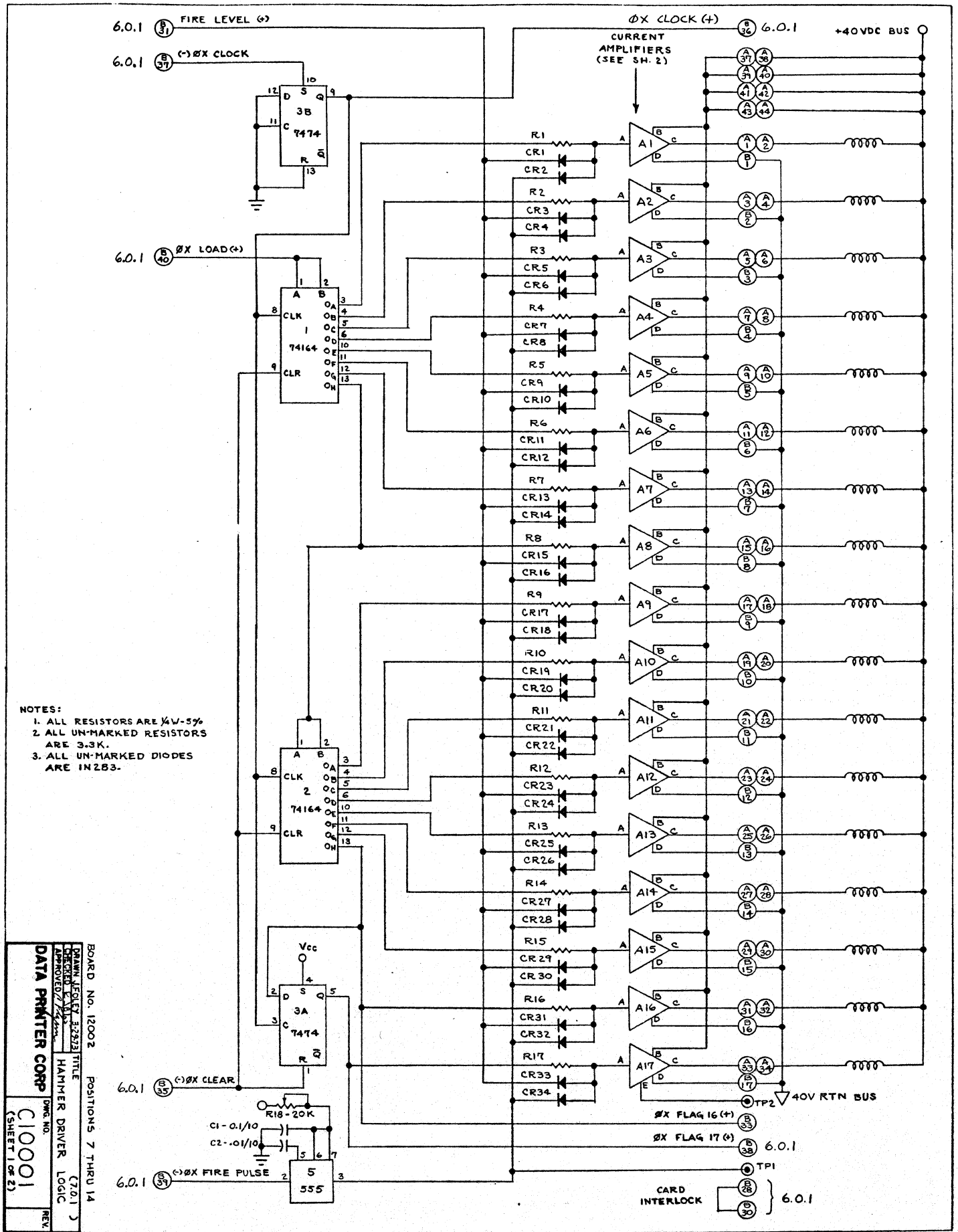
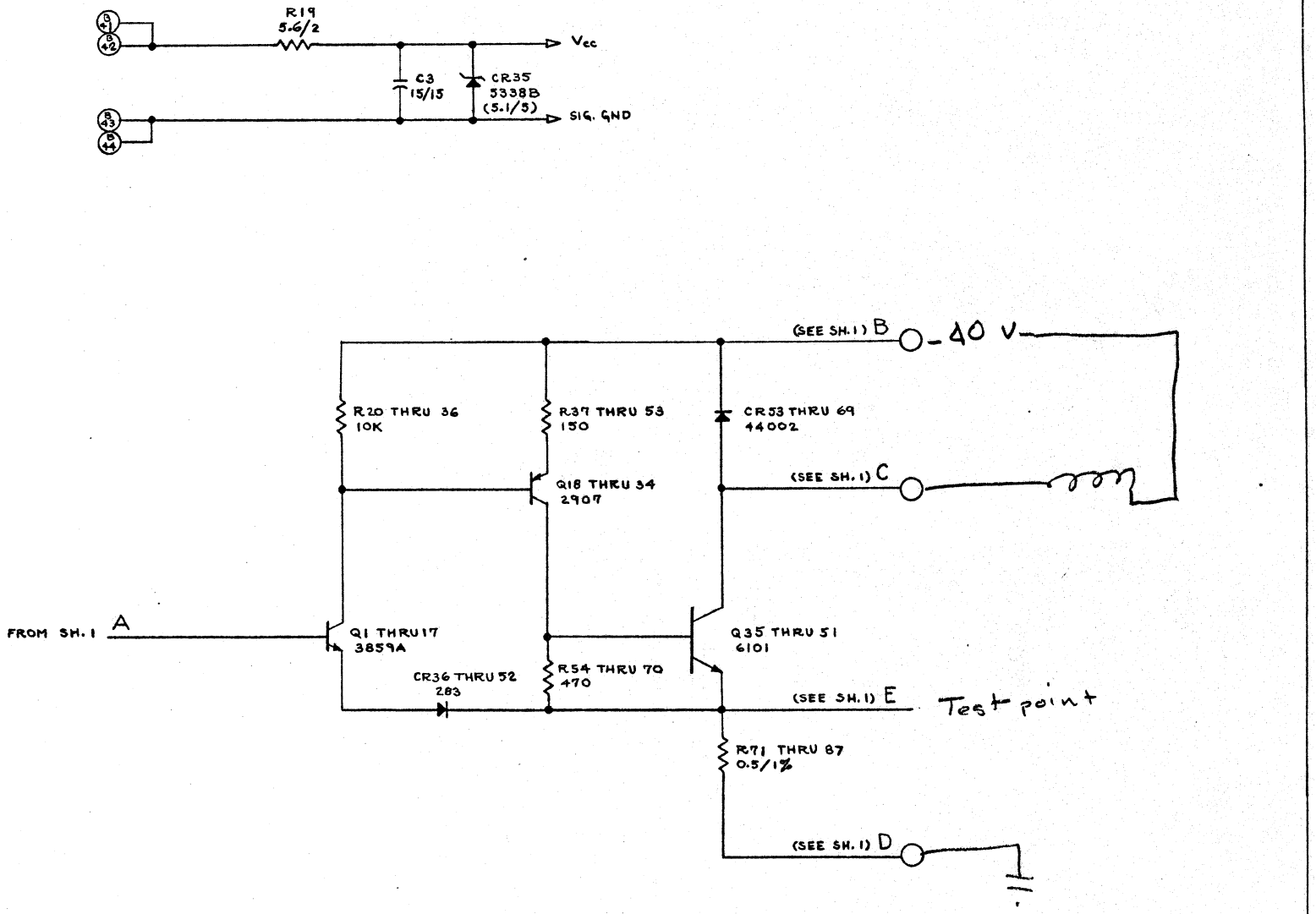
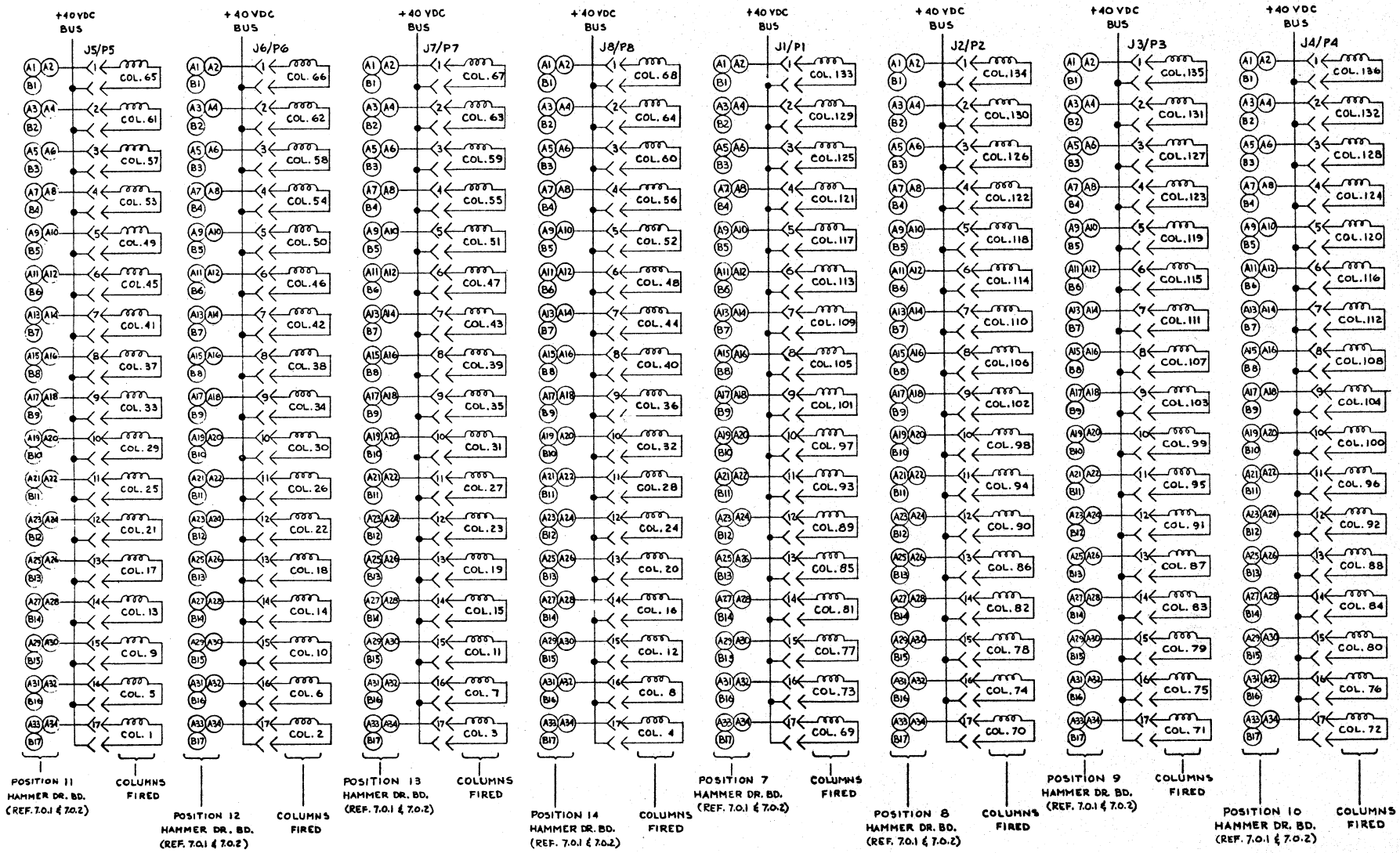


Figure 7.0.1 Hammer Driver Logic



104 **Figure 7.0.2 Hammer Driver Logic**



SYMBOLS

(A1) (A2) (B1) = HAMMER DRIVER CARD CONNECTOR/MOTHER BOARD CARD RECEPTACLE CONTACT NO'S.

—1← = MOTHER BOARD EDGE CONNECTOR CONTACTS (TOPSIDE)/HAMMER ACTUATOR PLUG.

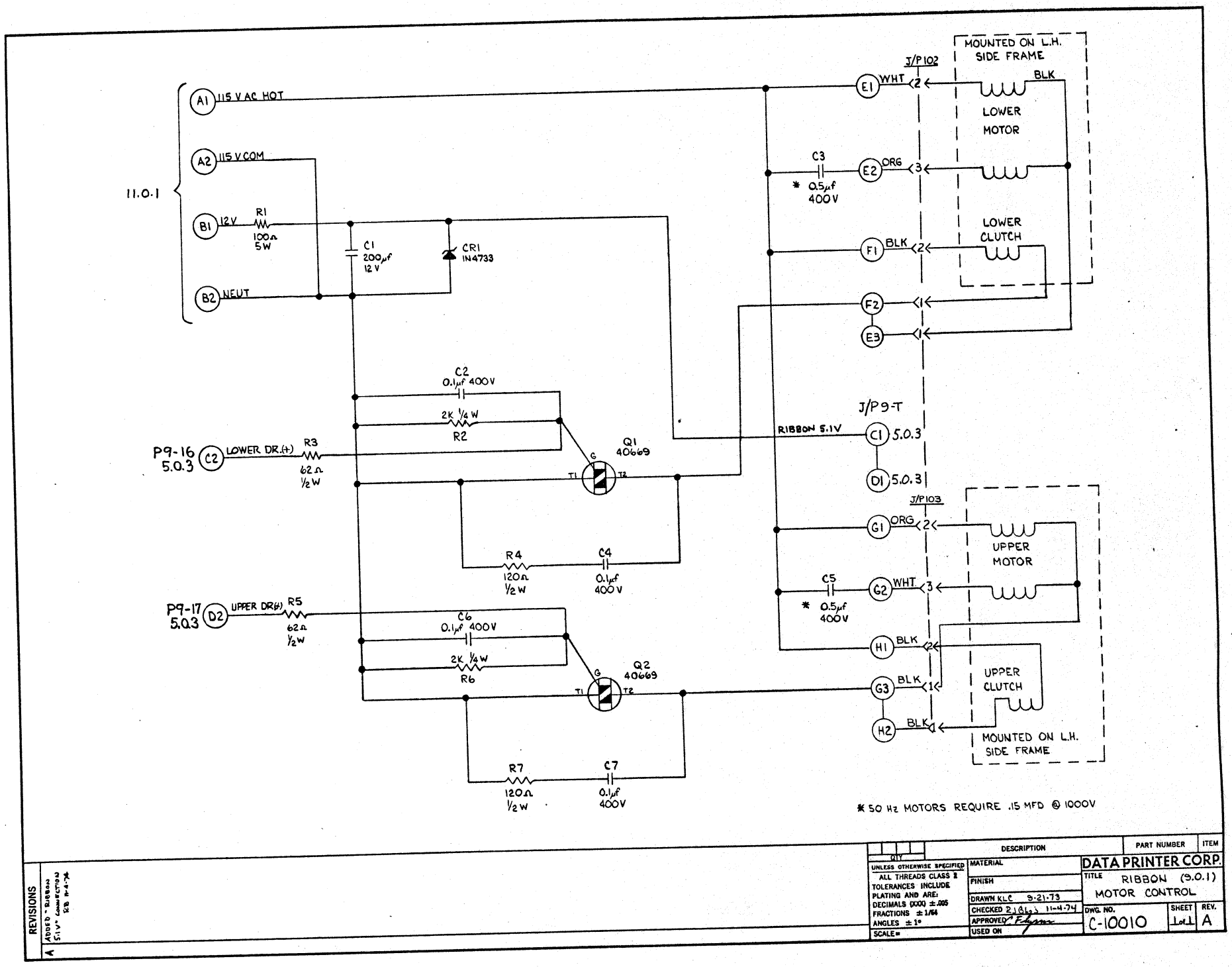
—< = SAME AS ABOVE, EXCEPT THESE ARE BOTTOM-SIDE CONTACTS WHICH ARE ALL TIED TO +40 VDC BUS.

COL. 1 = HAMMER BANK ACTUATOR COIL WITH APPLICABLE PRINT POSITION NO.

REVISIONS

DRAWN RJB 8-24-73	TITLE	HAMMER ACTUATOR WIRING (8.0.1)
CHECKED [illegible]		
APPROVED [illegible]		
DATA PRINTER CORP	DWG. NO.	C10008
	REV.	

Figure 8.0.1 Hammer Actuator Wiring



106 **Figure 9.0.1 Ribbon Motor Control**

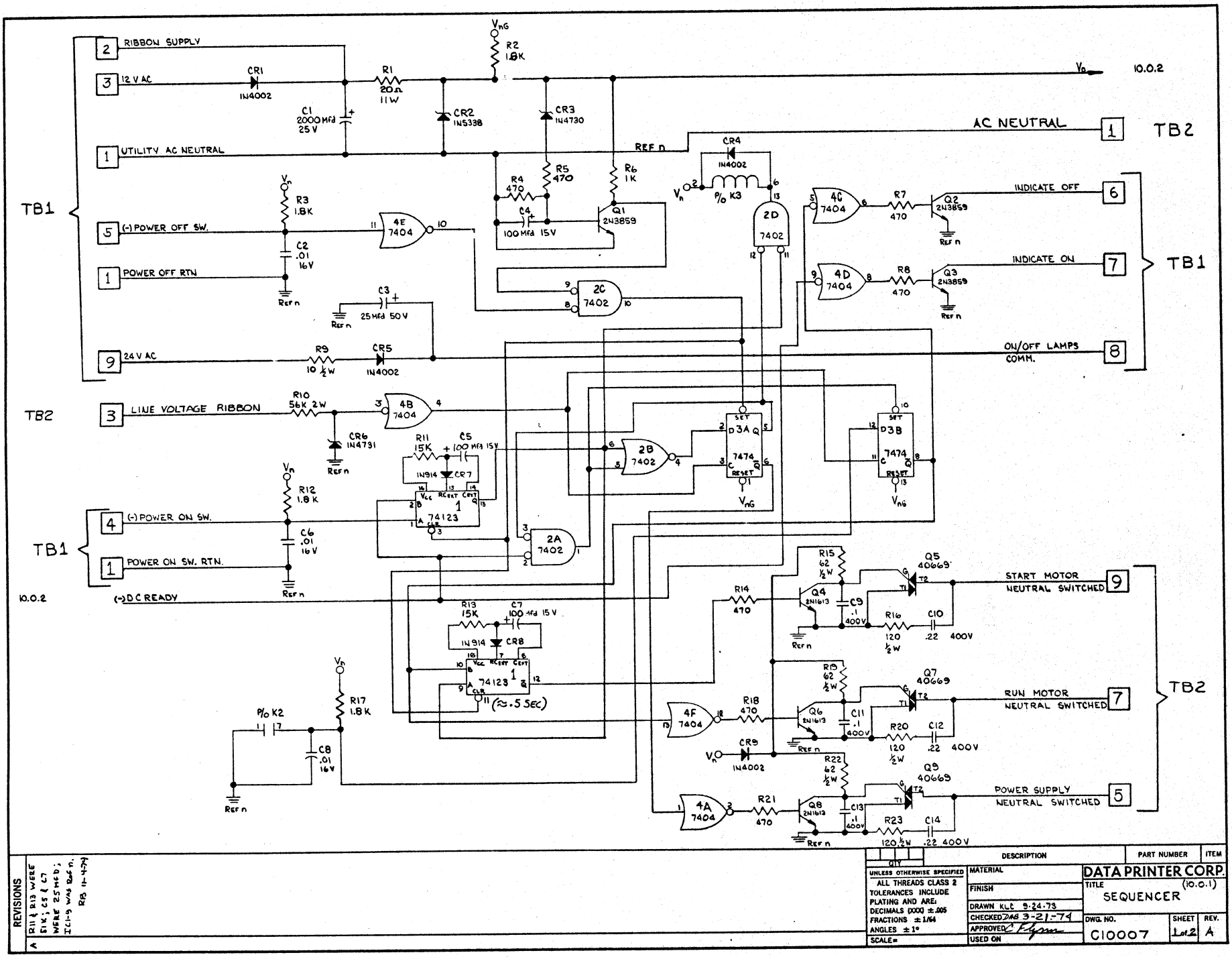
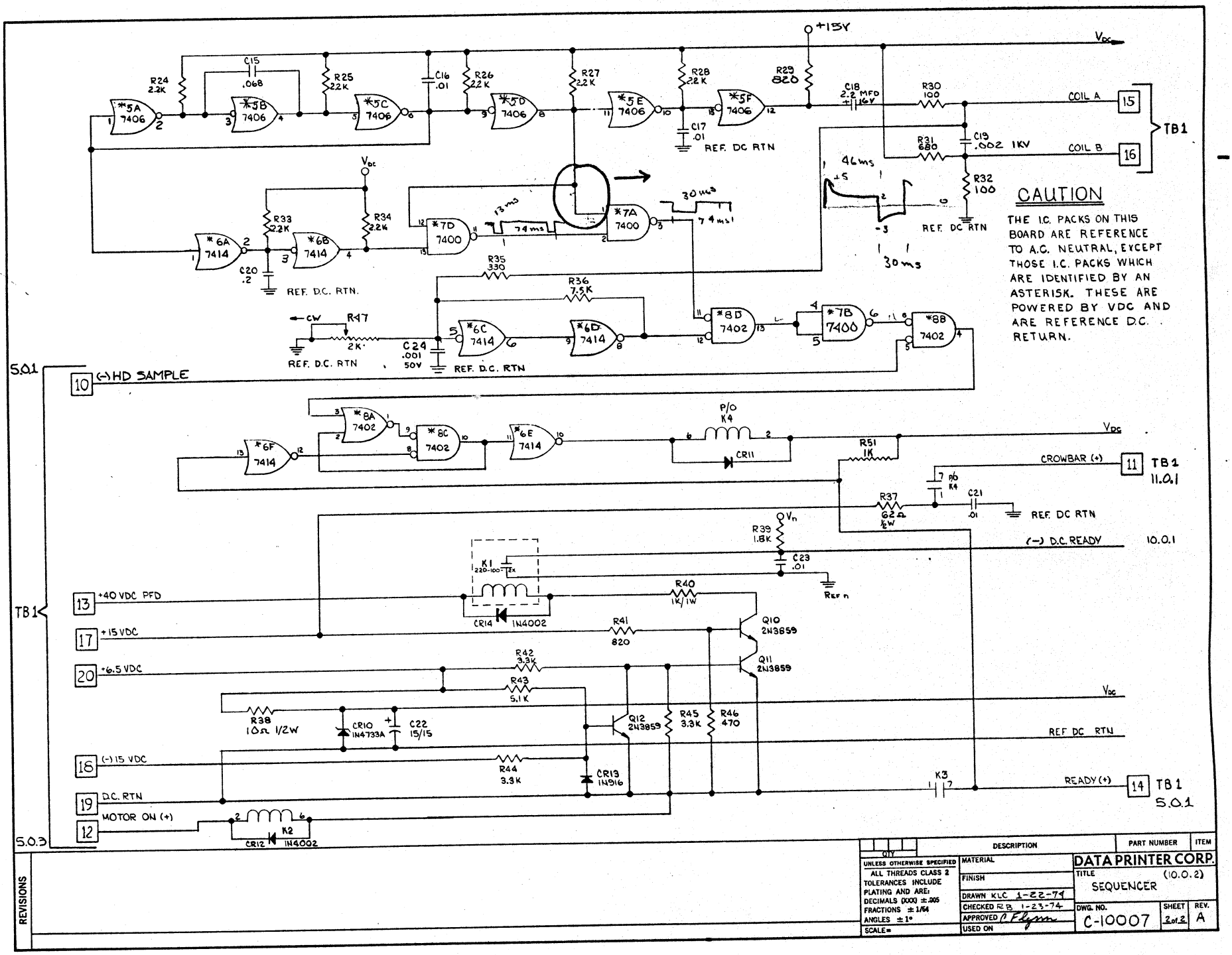


Figure 10.0.1 Sequencer



108 **Figure 10.0.2 Sequencer**

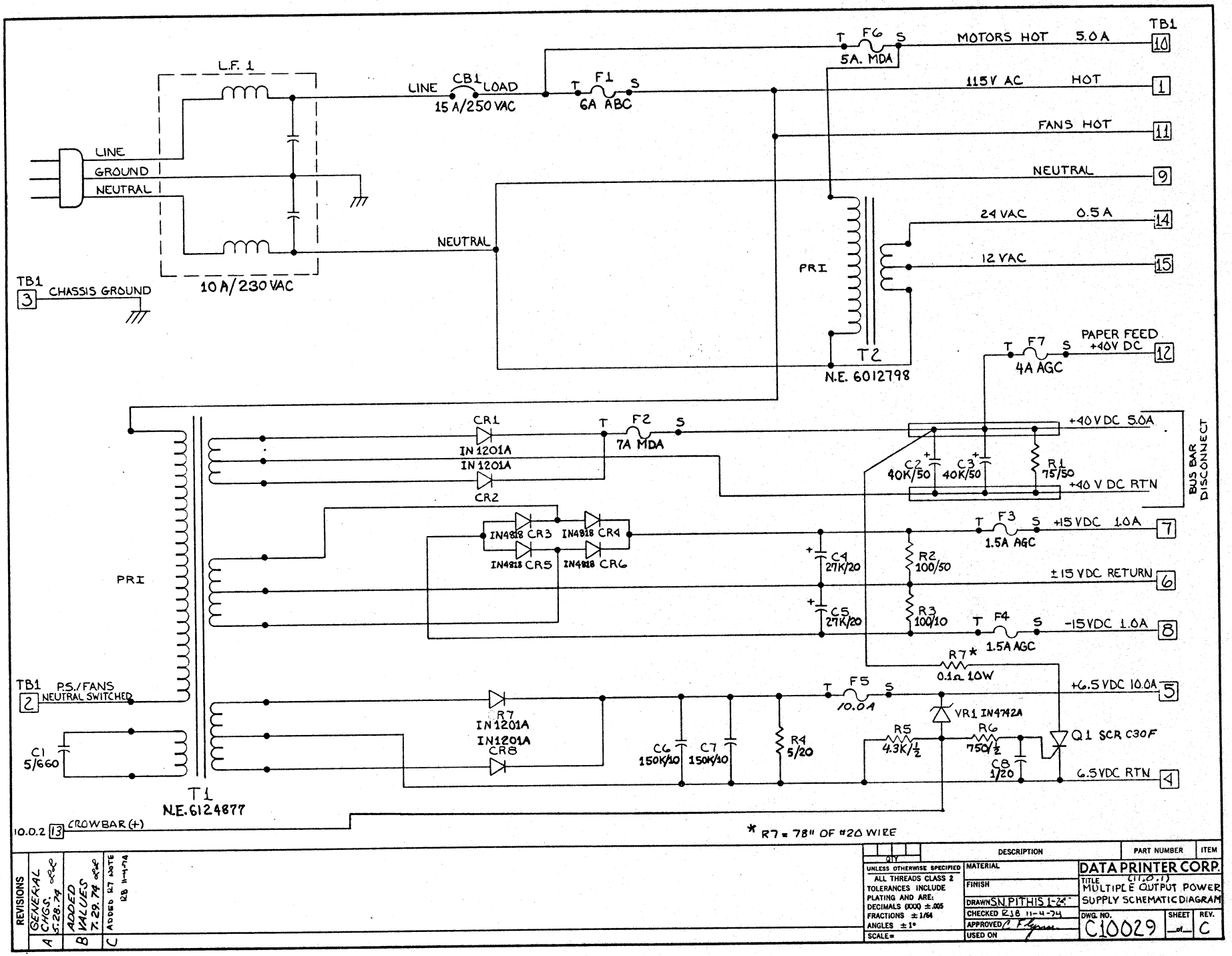
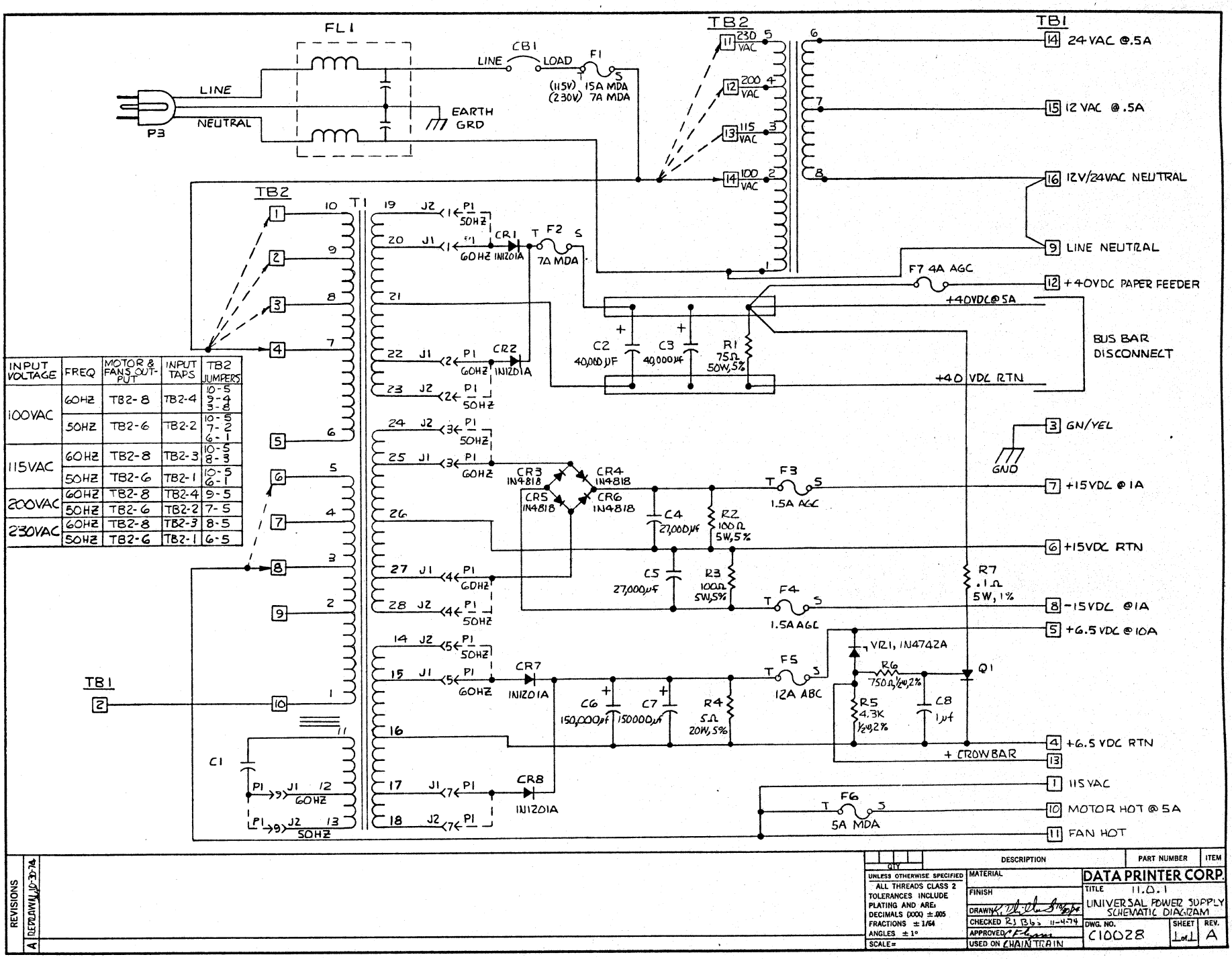


Figure 11.0.1 Multiple Output Power Supply Schematic Diagram



110 **Figure 11.0.1 Universal Power Supply Schematic Diagram**

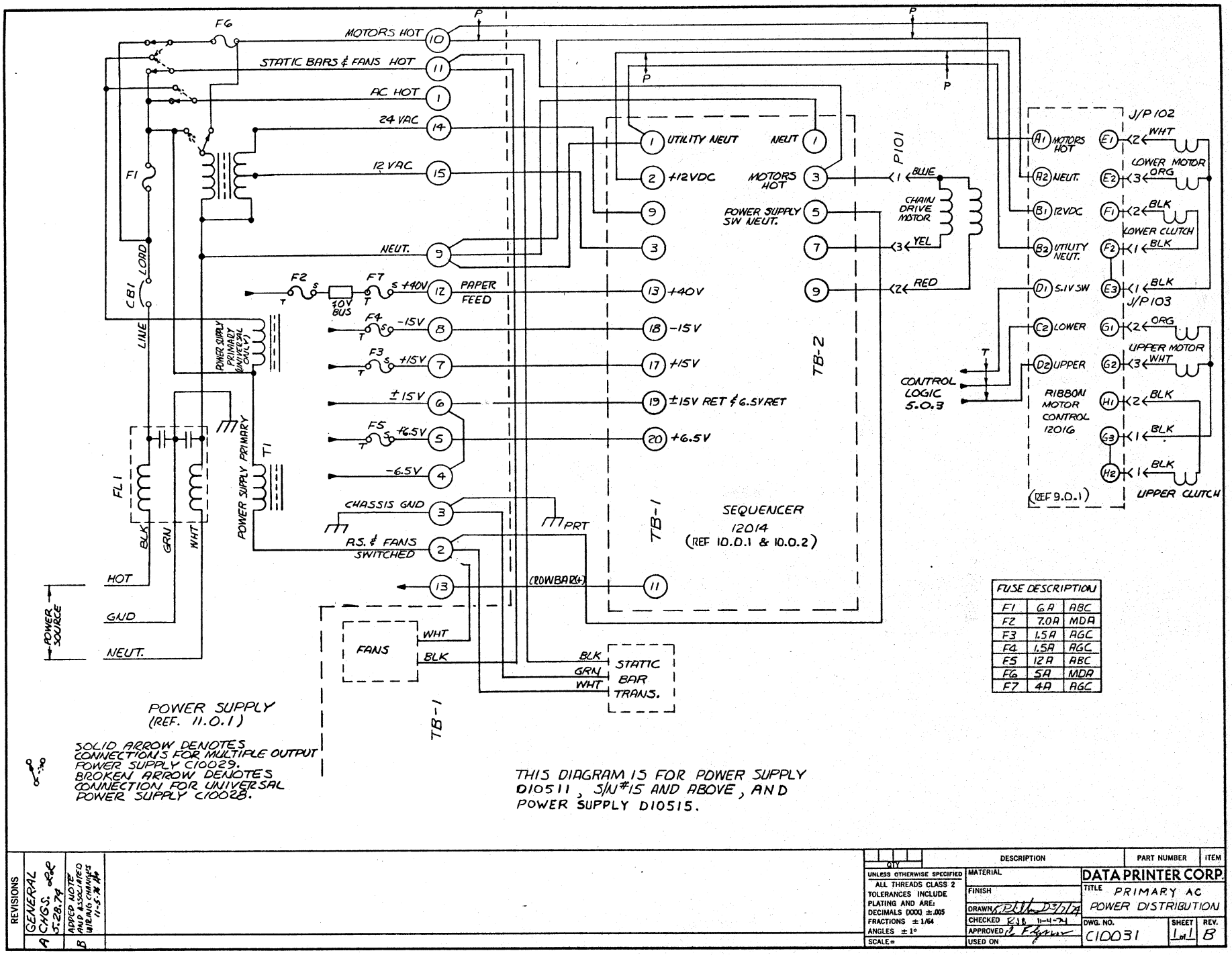
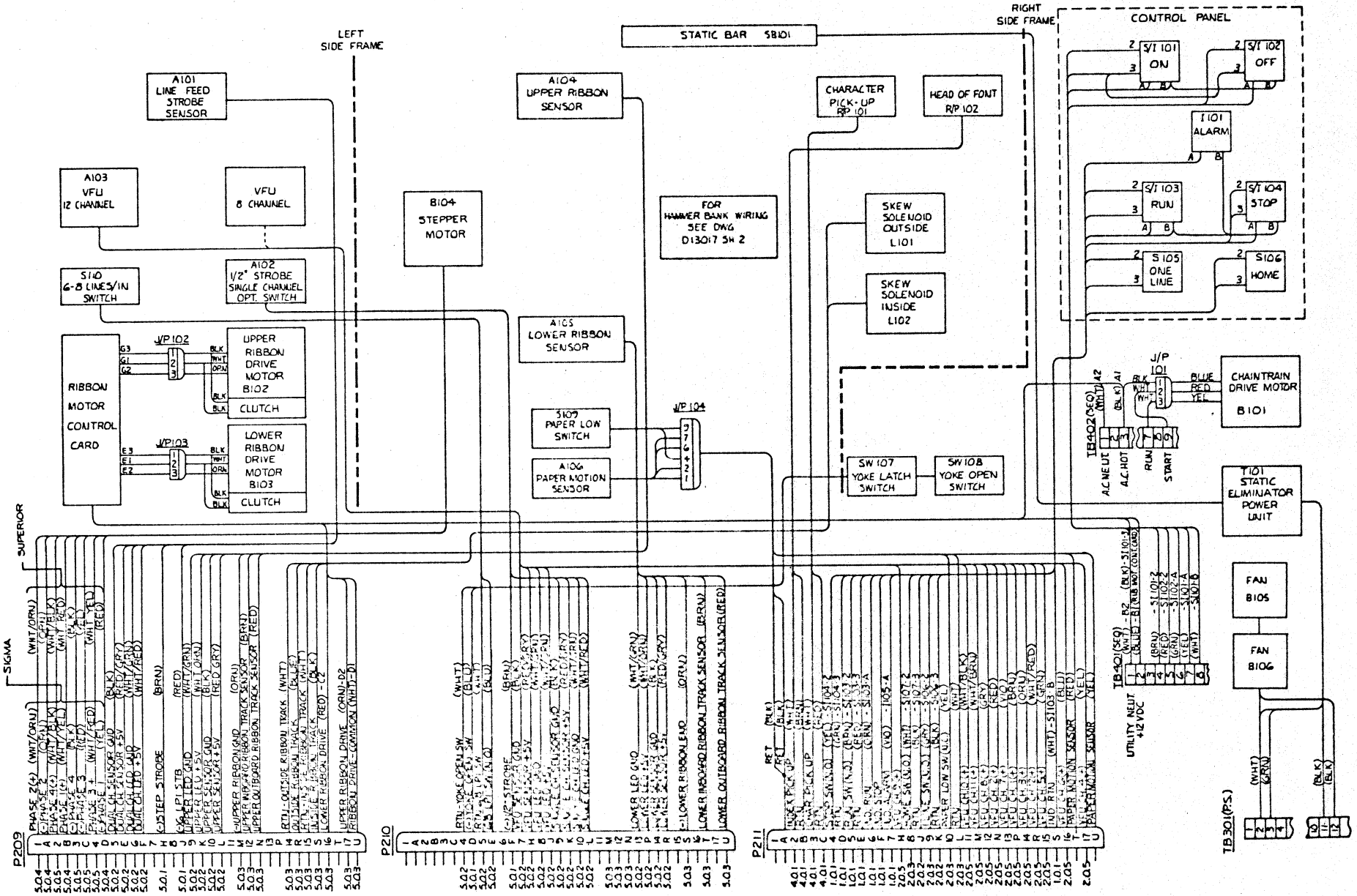


Figure 12.0.1 Primary AC Power Distribution Diagram



112 **Figure 13.0.1 Chaintrain Interconnecting Wiring Diagram**

APPENDIX D

ELECTRICAL CIRCUITS

DETAILED FUNCTIONAL DESCRIPTIONS

DATA INPUT CONTROL

Electrical Diagram No. 1.X.X.
P.C. Board No. 2603

Functional Description

For the purpose of this discussion, it will be assumed that the printer is in an operational condition, i.e., power has been applied, paper is loaded in the printer, and no alarm conditions exist.

1. Run Control (Local and Remote)

The momentary closure of the RUN switch resets the STOP latch which, together with (–) PRINTER BUSY being high, causes the RUN latch to set. RUN (+) going high clocks the state of the LOCAL/REMOTE switch into a storage register, the output of which is gated with RUN (+) to generate the (–) RUN REMOTE signal which, in turn, generates the RUN REMOTE (+) signal. RUN REMOTE (+) enables the receiver circuits for on-line (Remote) operation. The $\overline{Q}$ output of the Local/Remote storage register is gated with RUN (+) to generate the RUN LOCAL signals used to control the test (Local) mode of operation.

2. Local Paperfeed Control

In the Local mode of operation, paper feeding is controlled by the position of the SS/PF (Single Space/Program Feed) switch. When operating in the SS mode, the (–) AUTO LINEFEED signal is held at a constant low level which, as an input to the Paperfeed Control Logic, causes the printer to line space at the completion of each print operation.

When operating in the PF mode, the (–) AUTO LINEFEED signal remains high allowing the setting of a D Register (which shall hereafter be referred to as the PF CMD Reg). The setting of the PF CMD Reg causes the (–) PAPERFEED CMD signal to go low. Recognition of the command by the Memory Control Logic causes (–) PRINTER BUSY to go low, causing the PF CMD Reg to be cleared.

3. Local Print Operations

Initially, (–) PRINTER BUSY being high places the TEST PRINT CMD latch in a set condition. RUN LOCAL (+) going high enables the set output of this latch to generate the (–) PRINT CMD signal. The Memory Control Logic responds to the command by dropping the (–) PRINTER BUSY signal and raising the SEND DATA (+) signal. (–) PRINTER BUSY going low allows the TEST PRINT CMD latch to be reset by the first DATA STROBE to occur after the fall of SEND DATA (+). SEND DATA (+) will fall after the Line Memory has been filled (80 or 132 characters). At the completion of the print and paperfeed operations, (–) PRINTER BUSY going high will again set the TEST PRINT CMD latch, causing the continual recycling of operations until the STOP switch is depressed.

4. Combined Local Print and Test VF Operations

When cycling in the Program Feed (PF) mode, it should be noted that at the completion of each paperfeed operation, (–) PRINTER BUSY will go high followed by the rise of PRINTER RDY (+).

This results in the setting of both the TEST PRINT CMD latch and the PF CMD Reg. As previously stated, the Memory Control Logic responds to a command by dropping (-) PRINTER BUSY and raising SEND DATA (+). This clears the PF CMD Reg. with the net result that the PF CMD Reg. remains set for only about 100 nanoseconds. This is sufficient to condition the Memory Control Logic to accept the next character loaded as the Paperfeed Instruction character. The (-) PRINT CMD signal which remains low at this time, prevents PRINTER RDY (+) from falling. TEST STROBE pulses, which are derived from the Memory Control as a result of the Test Command signals, are then used to generate (-) DATA STROBE pulses.

The first DATA STROBE causes the character, selected by the Data Bit switches (b1 through b7), to be transferred to the Paperfeed Control Logic. Subsequent DATA STROBE's cause the loading of Test characters into the Line Memory. When the Line Memory is filled, SEND DATA (+) falls, allowing the next (-) DATA STROBE pulse to terminate the Test Print command.

5. Stop Control

The momentary closure of the STOP switch causes the STOP latch to set, which in turn causes the RUN latch to reset as soon as (-) PRINTER BUSY goes high. RUN (+) going low inhibits any further Remote or Local operations.

PAPERFEED CONTROL LOGIC

Electrical Diagram No. 2.X.X.
P.C. Board No. 2613

Functional Description

In the RUN mode, paperfeed is initiated either automatically at the end of a print cycle by means of the AUTO LINEFEED signal, or upon command indicated by a low-going pulse on the (–)VF SAMPLE input to the Paperfeed Control. In the STOP mode, the HOME and ONE LINE switches are enabled to provide a means of manually controlling the paper movement.

1. Run Mode, Auto Linefeed

(–) AUTO LINEFEED being low at the leading edge of the PRINT FINISH (+) pulse, causes the $\overline{Q}$ output of the Auto Feed Register, 9B on 2.1.2, to switch high. This results in the generation of a high RESET LC (+) signal and a low (–) FEED signal through gates 11B and 18B. The (–) FEED level presets the Paper Feed Register, 9A on 2.1.1. The Q output of register 9A is gated at 11C with the output of the paperfeed cycle governor and the (–) PRINT FINISH level, to produce a PAPERFEED SET (+) high level at the termination of the PRINT FINISH signal. The governor prevents successive feed operations from occurring too rapidly.

The RESET LC (+) signal clears the Line Count Latch, 15B/15C and the 15B output (now high) is gated with (–) FEED at gate 13B. When (–) FEED goes high on the leading edge of the next Line Strobe, the D input to the Paperfeed Register, 9A, goes low to allow the trailing edge of the Line Strobe to switch the Q output of the register low and terminate the PAPERFEED SET (+) command.

The above describes an automatic single space operation. If, however, automatic double-spacing is required, the external device will hold the DOUBLE SPACE (+) command, pin 27 on 2.1.2, high. This signal is routed through a latching network, 21A and 18D, to maintain the (–) FEED level until after the expiration of the first Line Strobe. This causes the Paperfeed Register, 9A on 2.1.1 to ignore the first Line Strobe (because its D input is still high) and to be reset on the second Line Strobe which results in a 2 line feed.

2. Run Mode, Feed on Command

a. Initiating the Feed Operation
The effect of the (–) VF SAMPLE, pin 15 on 2.1.1, is best explained by referencing the following description to Figure D-1.

1) (–) VF SAMPLE is inverted at 10A to form the positive-going VF SAMPLE (+) pulse. This is routed along two paths (2) and (3).

2) The latch 23B/23A is set to condition a trigger circuit 20B which (2a) causes (–) PF RDY, through gate 15D to go high, and (2b) enables one input to the VF Reset gate, 19B which will generate a VF RESET (+) if the Paperfeed Register, 9A, is not set.

3) VF SAMPLE (+) checks the condition of the (–) NO LINEFEED level at gate 14A on 2.1.2. The (–) NO LINEFEED level being low, indicates that gate 4A on 2.1.3 is sensing all "1's" at its inputs, i.e., all the (–) BIT levels are high (code 000 000) signifying a No Linefeed request.

4) If (–) NO LINEFEED is low, the (–) FEED signal through gate 18B will not be generated, and the Paperfeed Register, 9A on 2.1.1, will not be set. This results in the generation of the VF RESET (+) signal through gate 19B and inverter 16D, terminating the paper feed cycle.

5) If the NO LINEFEED code does not exist at VF SAMPLE time, VF SAMPLE (+) is gated through 14A on 2.1.2 and inverted at 10B to form START FEED PULSE (+).

6) This generates the (–) FEED signal through gate 18B to set the Paperfeed Register, 9A on 2.1.1, which inhibits the VF RESET (+) and delivers a high PAPERFEED SET (+) output to the Memory Control.

7) START FEED PULSE (+) samples (-) BIT 1 through (-) BIT 7 on 2.1.3 to store the complement of the Paperfeed Instruction code in the Format Registers (24A/B, 12A/B, and 7A/B).

8) The START FEED PULSE also checks the state of BIT 7 at gate 18A on 2.1.2 to determine the type of feed operation to be performed:
Bit 7 @ 0 = Line Count (1 to 63 lines);
Bit 7 @ 1 = VFU Feed (skip to the specified channel on the VF Tape or to Home position in systems without a Vertical Format Control Unit)

If (-) BIT 7 is low (Bit 7 @ 1), the START FEED PULSE (8a) sets the VFU Feed Register, 22B on 2.1.2, through gates 18A and 1C. The (-) VFU FEED signal forms RESET LC (+) through gate 11B, to reset the Line Count Latch, 15D/15C on 2.1.1, and also to maintain the (-) FEED level through gate 18B on 2.1.2.

If (-) BIT 7 is high (Bit 7 @ 0), (8b) the Line Count Latch, which was set by the VF Reset signal at the end of a previous feed operation, remains set.

b. Tracking and Halting Paper Movement

Paper movement results in the generation of a Line Strobe Pulse for each line advanced. If the feed operation is a counting type, the Line Count Latch is set and provides a high level at gate 14D on 2.1.3, to allow the leading edges of the LINE STROBE (+) pulses to advance the Format Registers, which are wired as a six-stage binary counter. When the register is advanced to a count of all "1's", all inputs to gate 3A go high to produce a high FINAL COUNT (+) level through inverter 16A. This level is gated with the high LINE-COUNT (+) level at gate 13B on 2.1.1 to lower the D input to the Paper Feed Register 9A. The trailing edge of the Line Strobe which generated Final Count now switches the Q output of the Paper Feed Register low, which through gate 11C and inverter 16C, terminates the PAPERFEED SET (+) signal.

The $\overline{Q}$ output of the Paper Feed Register going high removes the inhibit on gate 19B to generate the VF RESET signals, which clear the Paperfeed Control registers and starts the paper feed governing timer.

If the feed operation is a result of a command to skip to a VFU Channel or skip to Top of Form, LINE COUNT (+) is low and inhibits the Line Strobes at gate 14D on 2.1.3 from advancing the Format Registers, i.e. the format code is held in the registers until the operation is complete. The outputs of the Format Registers [F1 (+) through F 4 (+)] are routed to the VF Control Logic where they are decoded and gated with the appropriate VF Channel output. When the selected channel is sensed, the VF Control transmits a low (-) HALF VFU FEED level to the Paperfeed Control to address the D input to the VFU Feed Register, 22B on 2.1.2. At the leading edge of the next VFU PULSE (+), derived from the Line Strobe in the VF Control, the $\overline{Q}$ output of the register is switched high, causing the (-) FEED level to go high through gates 11B and 18B. This level, gated with the high output of the Line Count Latch at 13B on 2.1.2, lowers the D input to the Paperfeed Register, and the trailing edge of the (-) LINE STROBE resets the register to terminate the Paperfeed Set command. In systems not equipped with Vertical Format Units, a HALF PAGE STROBE (+) signal is generated each time the paperfeed drive shaft makes one complete revolution (5.5 inches of paper, or one-half of a standard 11-inch form). This signal addresses a single-stage binary counter, 22A on 2.1.2, and a HOME STROBE (+) is generated on alternate counts through trigger 17B and gate 23C. The HOME STROBE (+) pulse, through gate 23D clears the VFU Feed Register, 22B, to terminate the (-) FEED level and finally to halt the feeding operation at the "Top of Form" position.

3. Manual Feed

a. ONE LINE Switch

If RUN (+) is low (system in a STOP condition), depressing the ONE LINE switch on the operator's control panel, or receipt of the (-) 1 LINE PULSE from the VF Control will

generate a (-) SGL SP PULSE, through trigger and gating circuits on 2.1.4. This pulse clears the Auto Feed Register, 9B on 2.1.2, to generate a low (-) FEED level. The operation from this point on is identical to that described in paragraph 1 above (Run Mode, Auto Linefeed).

b. HOME Switch
If RUN (+) is low (system in a STOP condition) depressing the HOME switch, or receipt of the (-) HOME PULSE from the VF Control, will generate a TOF Pulse (+), through trigger and gating circuits on 2.1.4. This pulse presets the VFU Feed Register, 22B on 2.1.2, through gate 1C. Operation from this point on is identical to that described in paragraph 2 above (Run Mode, Feed on Command)

c. Manual Paper Slew
If RUN (+) is low (system in a STOP condition), depressing the ONE LINE and HOME switches simultaneously, causes the (-) MANUAL SLEW level to go low through gate 5A on 2.1.4. This level, through gates 11B and 18B on 2.1.2, lowers the (-) FEED signal to hold the Paper Feed Register, 9A on 2.1.1, set for as long as the buttons are held. Release of either button raises the (-) FEED signal, allowing the next (-) LINE STROBE to reset the register

d. Paper Low Detection
When the last form of paper advances beyond the Paper Low sensing mechanism, the Paper Low Switch opens, causing the input at pin 56 on 2.1.4 to go high. If the system is operating in other than the Run Local mode, the Paper Low level is sensed by trigger 6A, and through gate 11B, produces a (-) PAPER LOW PULSE at the time of the next Line or Home Strobe (depending on optional wiring). This pulse is routed to the Data Input Control for control of the Run and Stop latches.

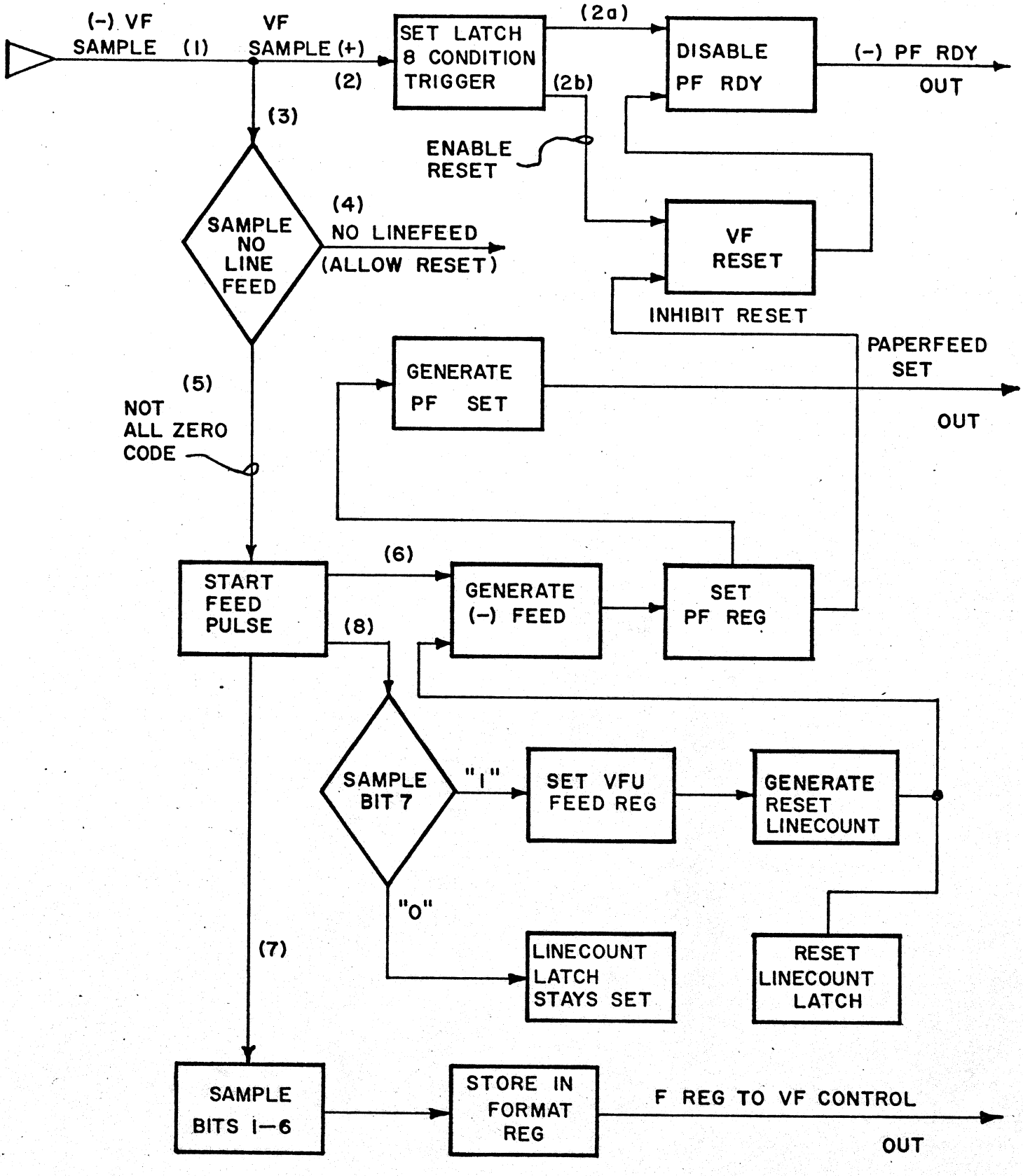


Figure D-1. Paperfeed Control VF Sample Time, Block Diagram

PRINT CONTROL LOGIC

Electrical Diagram No. 3.X.X.
P.C. Board No. 2619

Functional Description

1. Index Pulse Shaping (Refer to Figure D-2)

The trigger circuit, 11B, on dwg. 3.1.1 is wired to detect the falling edge of the INDEX (+) signal from the Level Converter, and to form a 3.0 to 6.0 microsecond pulse at that time for use by the Compare logic. At T1, because INDEX (+) is high, 3A-1 is high but 3A-2 is low, resulting in a high output at 3A-3. At T2, when INDEX (+) goes low, 3A-2 goes high satisfying the gating requirements and causing (-) INDEX PULSE to go low. At the same time, the capacitor on the trigger circuit begins to charge towards the triggering level. In 3 to 6 microseconds, the capacitor has reached that level, causing the output of 11B to switch high. This results in 3A-1 going low to terminate the (-) INDEX PULSE.

2. Character Strobe Pulse Shaping (Refer to Figure D-3)

The trigger circuit, 6B, on dwg. 3.1.1 is wired to detect the falling edge of the CHAR STROBE (+) signal from the Level Converter, and to form a 3.0 to 6.0 microsecond pulse at that time for use by the Print Control in initiating timing sequences and by the Compare Control in generating the print drum character codes. The operation of the circuitry is similar to the Index Pulse shaper, except that an alternate gating arrangement is used to achieve a positive-going pulse output. At T1, because CHAR STROBF (+) is high, 12A-3 is high and 12A-2 is low, resulting in a low output at 12A-1.

At T2, when CHAR STROBE (+) goes low, 12A-3 goes low, satisfying the gating requirements to cause 12A-1 to rise. At the same time, the capacitor on the trigger circuit begins to charge towards the triggering level. In 3 to 6 microseconds, the capacitor has reached that level, causing the output of 6B to switch high, removing the low level from 12A2, to terminate the CHARACTER STROBE PULSE (+).

3. Entering into and Exiting from a Print Cycle

The PRINT (+) output of the Print Register, 20A on dwg. 3.1.2, is held low during a power-on sequence by SYS RDY (+) at its Clear input. SYS RDY (+) does not go high until all power is present and Character Strobe pulses are being generated. In order to enter a Print Cycle, the D input of the Print Register must be high at the rising edge of (-) CHAR STROBE PULSE addressing the register's Clock input. The D input to the register is dependent upon the input levels to gate 12C, which must both be low to allow entering into the Print Cycle, i.e.,

a) 12C-8 must be low. 12C-8 is a result of gating at 14B – and if low, indicates that a Paperfeeding operation is not in process [(-) VF BUSY], that the Print Cycle Governor (via 10C) has timed out after a previous Print Cycle. PRINT ENABLE (+) must be low (see next section) and (-) END PRINT from the Memory Control is high. (-) END PRINT is used in terminating a Print Cycle and, at the time prior to a Print Cycle, is high.

b) (-) INITIATE PRINT from the Memory Control must be low.

Therefore, when the (-) INITIATE PRINT signal goes low, which indicates that the Line Memory has been loaded and is ready to be scanned for printing, the D input to the Print Register will go high if the other inhibiting cycles mentioned above are complete. This will allow the next (-) CHAR STROBE PULSE to set the register's Q output [Print (+)] high, thus entering the system into a Print Cycle. When PRINT (+) goes high, it starts the print cycle governing timer, made up of register 20B and the 6-bit binary counter (5A, 5B, and 9A thru 9D). This governor is provided to prevent the next request for a Print Cycle from being honored before the hammers have had a chance to settle or, a Print Cycle happens to be a short one, the governor insures a minimum time delay (48 character strobes, approximately 75MS) between the start of one Print Cycle and the start of the next.

During the time that PRINT (+) is high, Memory scanning subcycles (discussed in the next section) are initiated and continue until the Memory Control indicates that the Line Memory has been emptied

by maintaining a low (-) END PRINT level, which holds the D input to the Print Register low, allowing the next (-) CHAR STROBE PULSE to reset the Q output low, thus exiting the system from a Print Cycle. When PRINT (+) goes low, it releases the inhibit on the print governor counter (via 14A), which prevents the system from entering an ensuing Print Cycle until the hammers recently fired have had a chance to mechanically settle. Note that, when PRINT (+) is high, a count of 34 in the print governor counter will inhibit further counting via 14A until PRINT (+) goes low. The counter will then resume counting until a count of 48 is reached, at which time the print governor register will be reset and the counter cleared.

(-) PRINT is routed to the Clock input of the Print Finish Register, on diagram 3.1.1, to set the (-) PRINT FINISH level low. This level remains low until the next (-) CHAR STROBE pulse occurs and is sent to the Paperfeed Control for implementing an automatic line feed, and to the Memory Control as an indication that the (-) END PRINT command has been acted upon.

Figure D-4, which shows the relationships of the various pulses initiated by each Character Strobe during a Print Cycle, should be studied and understood. As an aid to understanding the operation of the trigger circuits (two forms of which were discussed in detail in paragraphs 1 and 2 above) which are used to form the timing train, it is urged that the reader trace the pulses through the circuits shown on dwg. 3.1.1, starting with the (-) CHAR STROBE PULSE and continuing through triggers 6A and 1A, and monostable multivibrators 13 and 18. In the following descriptions, these pulses will be referred to as having been generated by the Character Strobe Pulse; their duration and time relationship may be derived by reference to the timing diagram.

4. The Scan Data Sub-Cycles

During a Print Cycle, each (-) CLEAR D PULSE generated by the Char Strobe Pulse prepares the Print Enable register, 15B, (on 3.1.2) by clocking its Q output to a high level, and clears the HD MEM FLAG storage register 15A. Thus, (-) CLEAR D Pulse following the Char Strobe Pulse which placed the system in a Print Cycle, sets the Q output of the Print Enable register high, since its D input sees the high PRINT (+) level. The low-going (-) PRINT ENABLE level is routed through gate 14B on 3.1.2, which results in a low level to the D input of the print register 20A. This level, if it remains low, will cause the print register to be reset on the next (-) CHAR STROBE pulse, thus aborting the Print Cycle. At the same time, PRINT ENABLE (+) is applied to trigger circuit 11A on 3.1.3 which, after a delay of approximately 3 microseconds, allows the SCAN DATA (+) level to rise. SCAN DATA (+) is routed to the Memory Control to initiate a Line Memory addressing cycle (scanning the Memory). Prior to the rise of SCAN DATA (+), the inverted output of trigger 11A is gated with the high PRINT ENABLE (+) level at gate 3C to form (-) PRESET D, which is transmitted to the 136th stage of the Hammer Driver shift register to load a "Flag" bit, which during the scanning cycle will be shifted through the register and will eventually appear at the output of the first stage.

The result of SCAN DATA (+) going high is that the Memory Control begins to deliver (-) PRINT STROBES in synchronism with Line Memory address pulses. The (-) PRINT STROBES are doubly inverted by gates 10B and 3D on 3.1.3 to form (-) LOADS which are transmitted to the Hammer Drivers to shift data into and through the shift register. The (-) LOAD pulses are also routed to the Clock input of the HD MEM FLAG storage register 15A on 3.1.2, to monitor the condition of the HD MEM FLAG (+) level.

This scanning and loading cycle continues until HD MEM PRE-FLAG (+) goes high to indicate that the Flag bit loaded into the 136th stage of the Hammer Driver shift register has advanced to the final stage, (first Hammer Driver position), i.e. the Line Memory has been addressed 135 times. On the next load (136th shift pulse), the Flag bit is shifted out of the Hammer Driver shift registers into 15A which, via gate 2B, clears the print enable register. PRINT ENABLE (+) going low, immediately causes SCAN DATA, on 3.1.3, to drop which, in turn, informs the Memory Control to cease addressing the Line Memory. For each succeeding Character Strobe Pulse, the sequence described above is repeated until the Memory Control issues an End Print command to terminate the Print Cycle.

The scanning sub-cycle is initiated by the Character Strobe and is terminated by the Flag bit having been shifted the entire length of the Hammer Driver shift register. Under normal conditions, this termination occurs well in advance of the next Character Strobe. If, however, for some reason a malfunction occurs and the Flag bit does not appear at the end of the shift register, the PRINT ENABLE

(+) level remains high, and at the next Character Strobe Pulse time, the Print Register will be reset to abort the Print Cycle. (–) PRINT going high, sets the Print Finish register, 8A on 3.1.1, and, via gate 2A on 3.1.1, generates a (–) CLEAR to reset the Hammer Driver shift register stages.

PRINT (+) is also routed to 3.1.1 and, when low, inhibits trigger circuit 6A, causing 6A's output to remain low. This results in the TRANSFER (+) signal going high which, in turn, transfers the cleared state of the Hammer Driver shift registers into the Hammer Driver latches.

It should be noted that, whenever the PRINT (+) register is in the reset state, (–) CLEAR remains at a low level and TRANSFER (+) remains high (except during Character Strobe Pulse time). This ensures that the Hammer Driver shift registers and storage latches are held reset at all times other than during a Print Cycle.

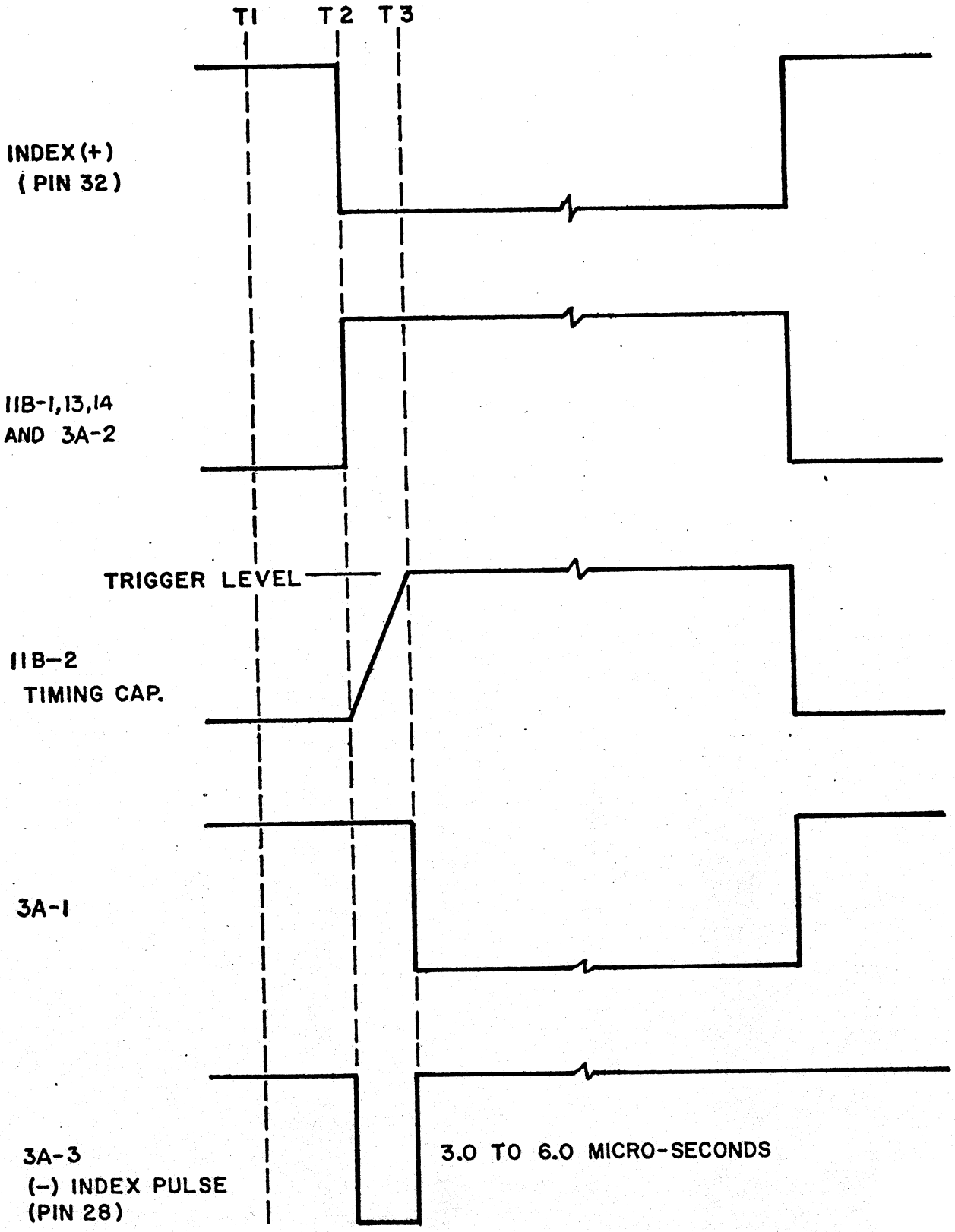


Figure D-2. Print Control Index Pulse Shaping, Timing Diagram

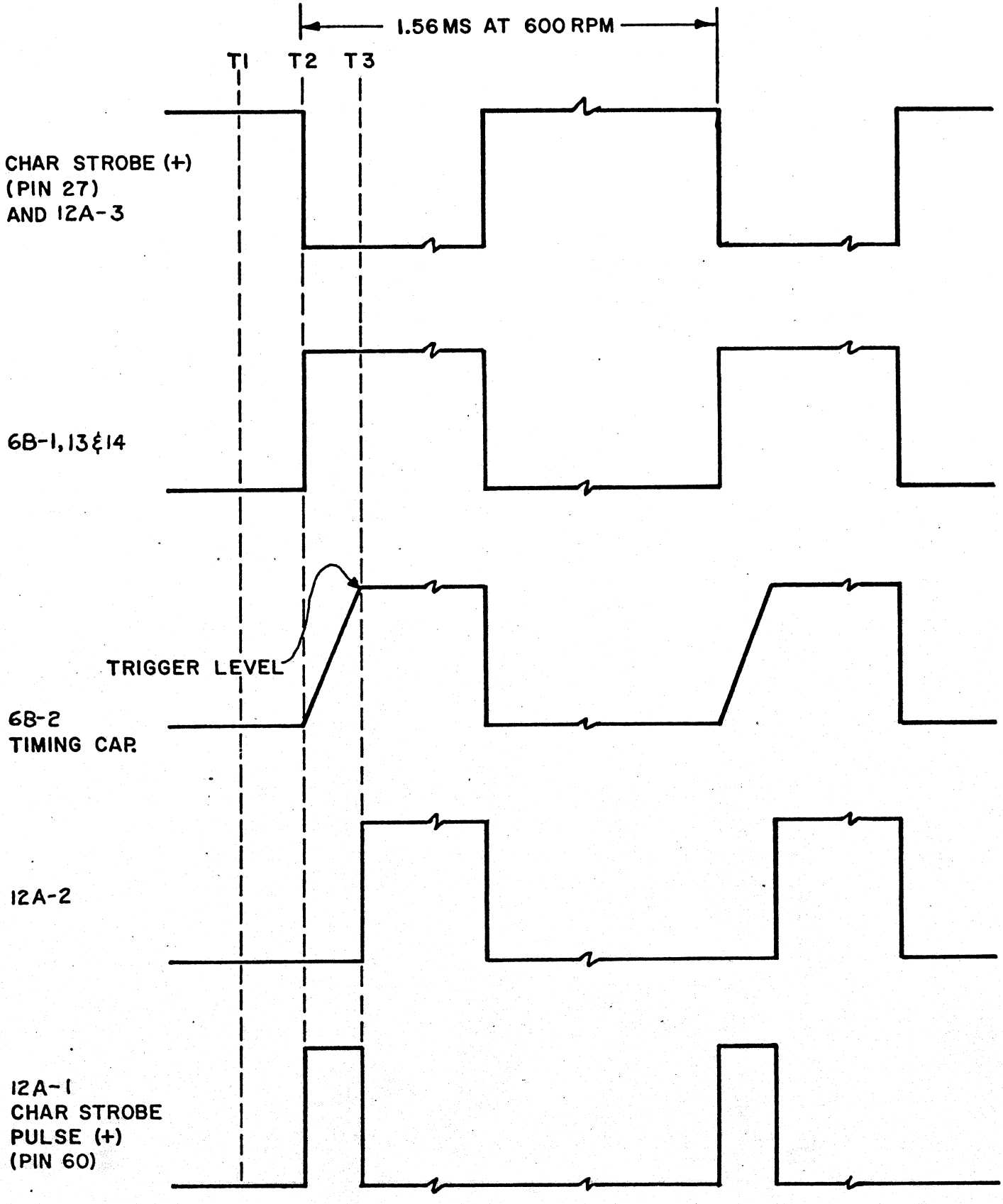


Figure D-3. Print Control Character Strobe Pulse Shaping, Timing Diagram

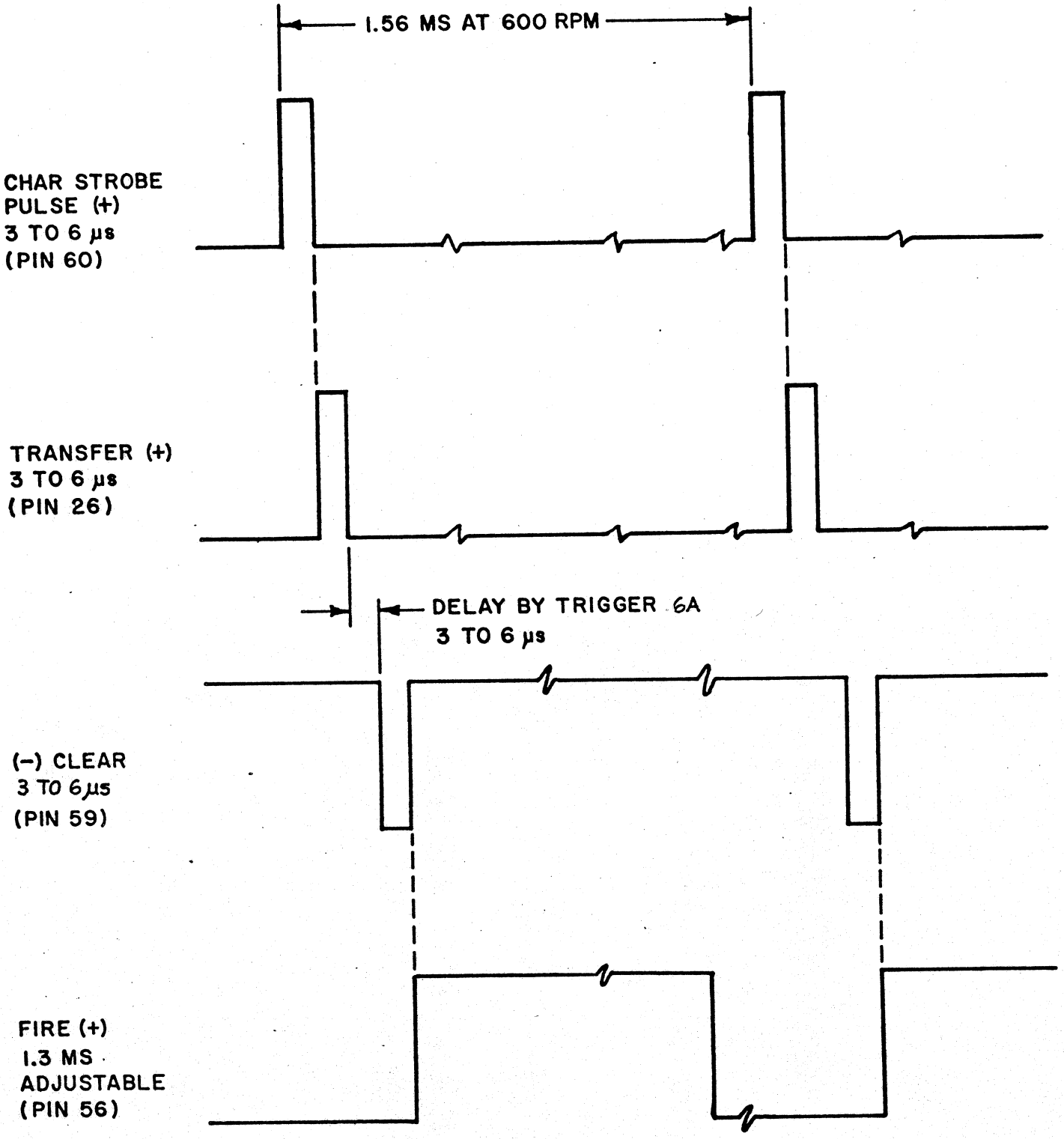


Figure D-4. Print Control Char Strobe Pulse Train (During A Print Cycle), Timing Diagram

COMPARE-OUTPUT CONTROL LOGIC

Electrical Diagram No. 4.X.X.
P.C. Board No. 2604

Functional Description

1. Print Drum Character Code Generator

The codes which represent the characters on the print drum are formed in the Compare-Output Control by counting the Character Strobe Pulses which are generated by the print drum character pickup and shaped in the Print Control. Since these pulses occur continually as long as power is supplied to the system, an additional marker known as the Index Pulse is supplied to give the code generating counter a starting point. The Index Pulse occurs mid-way between the Character Pulse identifying the last character on the drum and the Character Pulse identifying the first character on the drum. It is thus a marker which indicates that the next Character Strobe to occur will be for the first character.

The (-) INDEX PULSE (3.0 to 6.0 microseconds) is routed to the "Clear" inputs of all six D Registers which are wired in a binary counter configuration. This resets the counter so that the "Q" outputs of the individual stages assume the levels "100 000" (reading from right to left, i.e. – high order to low order). The leading edge of the next CHAR STROBE PULSE (+) (3.0 to 6.0 microseconds) causes the counter to advance one count and present the code "100 001", which represents the first character on the drum. For each succeeding CHAR STROBE PULSE (+), the counter is advanced once in binary fashion until the next (-) INDEX PULSE occurs to clear the counter down to the starting levels.

2. Data Comparison

The (-) LM BITS delivered to the Compare-Output Control are outputs from the Line Memory which are significant during the print operation. Their combined levels form a code which represents the character stored in a particular column in Memory. Note that these levels might change for each Memory column addressed while a scanning sequence is taking place. It is the function of the Compare section of the logic to identify those codes which are identical, bit for bit, with the print drum character code established in the binary counter at the beginning of the scan. The (–)LM BIT levels are inverted to supply the complementary levels required for comparison.

Each "And-or-Invert Gate" (7451) operates on one bit from the Line Memory and the corresponding bit from the Character Code Generator to supply a high output only when the two bits are at the same level (either "1" or "0"). The outputs of the six gates are wired to an "8 Input Positive Nand Gate" (7430), to produce a low (-) COMPARE output when all of its inputs are coincidentally high, i.e., when all bits compare. The 8-input gate is further conditioned by a COMP GATE (+) derived from the Print Control to identify the time slots in which comparisons are significant.

An additional "8-Input Positive Nand Gate" (7430) with optional input wiring identifies "Space" (non-print) codes from the Line Memory. The gate supplies (-) SPACE CODE which acts as an inhibit on a "Nand Gate" (7400) to prevent the generation of ENABLE HD MEM (+) when the Memory contains a Space code. The ENABLE HD MEM (+) level, which is the result of a comparison is routed to the 136th stage of the Hammer Driver shift register to be loaded in preparation for printing.

3. Interface Output Lines

The signals RUN REMOTE (the result of Gating RUN (+) with (-) RUN LOCAL), SEND DATA (+), PRINTER RDY (+) and (-) PARITY ERROR are system status levels which are transmitted to the external device for use in controlling data transmission to the Printer.

The status conditions are gated by the Compare-Output Control with the Run Remote condition, then transmitted through Line Drivers (7440) capable of sending TTL levels through a maximum of 50 feet of twisted pair cable into a terminating network and receiver in the external device.

4. Lamp Drivers

The operator's control panel contains three status indicating lamps – RUN, STOP, and ALARM. These lamps are turned on by transistor circuits which draw approximately 35 milli-amperes through the bulb from +24 volts. The transistor circuits have input networks designed to accept the TTL levels of the status signals from the system.

Electrical Diagram No. 5.X.X.
P.C. Board No. 2607

Functional Description

1. Manual Form Feed – Stop Mode

In systems equipped with a Vertical Format Unit, commands directing manual feeding operations originate in the VF Control through gating on 5.1.3, and are routed to the Paperfeed Control to initiate paper movement. The manual 1 Line and the manual Slew cycles are controlled in the Paperfeed Control and are discussed in that section of the descriptions. The manual Home operation, under control of a format tape, requires direction from the VF Control and is described here. The initially high state of (-) VFU FEED from the Paperfeed Control, conditions a steering latch, 5A/5B on 5.1.2, such that the 5B output is high. Depression of the HOME switch generates a low (-) HOME PULSE through gating on 5.1.3 which is routed to the Paperfeed Control and causes (-) VFU FEED to fall. This does not change the state of the steering latch on 5.1.2, but provides a level at gate 1B to allow each (-) LINE STROBE pulse occurring while paper is moving to generate a VFU PULSE (+). At the time a hole is sensed in Channel 1 (Top of Form) of the Format tape, VFU CH 1 (+) goes high and generates a low (-) HALT VFU FEED through gate 6B. This level in conjunction with the leading edge of the next VFU PULSE (+), resets the VFU Feed Register in the Paperfeed Control and (-) VFU FEED rises. The trailing edge of the Line Strobe is then used by the Paperfeed Control to halt the feeding operation.

2. Channel Selection and Form Skipping – Run Mode

Channel selection and form skipping, when the system is in a Run condition, is essentially the same as the Manual Homing operation described above. While the system is in Run, however, the low-going (-) VFU FEED is accompanied by a (-) VF SAMPLE from the Memory Control. This pulse will condition the steering latch, 5A/5B on 5.1.2, to check the output of gate 11D through inverter 13C. A low output at 11D (high at 13C) indicates that the channel on the format tape identified by the code stored in the Format Register in the Paperfeed Control has been sensed by the Vertical Format Unit, and through gate 6B, causes (-) HALT VFU FEED to go low and terminate the feeding operation. The various bit configurations possible in the Format Register are decoded in gates shown on 5.1.1 and 5.1.2 to examine the outputs of the Vertical Format Unit. The gating arrangements are presented in tabular form in Table D-1.

3. Paper Low/Paper Out

A Paper Low condition will cause the Paperfeed Control to generate a (-) PAPER LOW PULSE each time the paper is advanced (this pulse is inhibited when operating in the Local mode). The pulse causes the VF Control to generate a (-) PAPER ALARM pulse through gates 2A and 1A on 5.1.2. The alarm pulse is routed to the Data Input Control as a command to go to a Stop condition. At this time, operation may be resumed on a single line basis by depression of the RUN button. When the paper moves into a Top of Form position (the last sheet of paper has moved past the printing position), VFU CH 1 (+) goes high, and the accompanying (-) PAPER LOW PULSE sets the Paper Out Latch, 2B/2C on 5.1.2, through gate 2D. The output of the latch now causes the (-) PAPER ALARM signal to assume a constant low level through gates 2A and 1A to hold the system in a Stop condition. This level will be maintained until a fresh supply of paper is provided; i.e. when PAPER LOW (+) goes low to reset the Paper Low Latch.

4. Paper Runaway

Each time paper is advanced, FEED PAPER (+) goes high and through gate 14C. Inverter 13A on 5.1.2 starts a 2 second time-out cycle in triggers 16B and 16A. If the FEED PAPER (+) level remains high for the period of the timer the Paper Runaway Latch, 5D/9B is set and through gate 5C generates a low (-) PAPER ALARM at gate 1A to force the system into a Stop condition, and a low (-) CLEAR VF

level at gate 1D to terminate the feeding operation. The Paper Runaway Latch is cleared only if the HOME or ONE LINE switch on the operator's control panel is depressed.

5. Automatic Skip from Bottom of Form to Top of Form

When operating in the Auto Linefeed mode, this feature is provided so that paper automatically skips over the tear line for listing purposes. When a hole is sensed in the Bottom of Form channel (8 or 12) of the format tape, the high VFU BOF CH 8/12 (+) level through gate 14D on 5.1.3 is sampled at gate 15C by the (-) LINE STROBE pulse, to form a (-) HOME PULSE at gate 15D. The operation at this point is identical to the Manual Homing operation and causes paper to feed to Top of Form (Channel 1). See paragraph 1.

TABLE D-1

CHANNEL SELECTION GATING

Format[1] Register Bits 4321	Gating for Channel Detection[2]
1111	F11XX(+) 14B,13F . F2(+) F Reg . VFU Ch 1 VFU = (-)Det Ch 1 8C
1110	F11XX(+) 14B,13F . F2(+) F Reg . VFU Ch 1 VFU = (-)Det Ch 1 8C
1101	F11XX(+) 14B,13F . FXX01(+) 7C . VFU Ch 2 VFU = (-)Det Ch 2 8B
1100	F11XX(+) 14B,13F . FXX00(+) 7B . VFU Ch 3 VFU = (-)Det Ch 3 8A
1011	F10XX(+) 11A . FXX11(+) 14A,13E . VFU Ch 4 VFU = (-)Det Ch 4 4A
1010	F10XX(+) 11A . FXX10(+) 7A . VFU Ch 5 VFU = (-)Det Ch 5 12A
1001	F10XX(+) 11A . FXX01(+) 7C . VFU Ch 6 VFU = (-)Det Ch 6 12B
1000	F10XX(+) 11A . FXX00(+) 7B . VFU Ch 7 VFU = (-)Det Ch 7 4C
0111	F01XX(+) 11B . FXX11(+) 14A,13E . VFU Ch 8 VFU = (-)Det Ch 8 4B
0110[3]	F01XX(+) 11B . FXX10(+) 7A . VFU Ch 9 VFU = (-)Det Ch 9 10B
0101[3]	F01XX(+) 11B . FXX01(+) 7C . VFU Ch 10 VFU = (-)Det Ch 10 10A
0100[3]	F01XX(+) 11B . FXX00(+) 7B . VFU Ch 11 VFU = (-)Det Ch 11 10C
0011[3]	F00XX(+) 11C . (-)FXX11 14A . VFU Ch 12 VFU = (-)Det Ch 12[4] 6A

Notes: 1. a) – The Format Register holds the complement of the Instruction Character Code.
b) – Only the four low order bits of the Instruction Code are significant for feeding under VFU Control
2. a) – The dot implies "AND" and signifies that a detection is made when all inputs are high.
b) – The sources of the gating signals are indicated under the signals.
3. – In systems equipped with 8 Channel Vertical Format Units, the inputs to the Ch 9, 10, 11, and 12 gates are replaced with constant high levels. Therefore, if a non-existent channel is selected, a single space will result.
4. – Any Instruction Code other than those listed in column 1 is not legitimate and will result in a single space.

VF CONTROL LOGIC (SPECIAL)

Electrical Diagram No. 5.X.X.
P.C. Board No. 2612

Functional Description

The function of this P. C. Board is identical to the function of P. C. Board No. 2607, with the following exception:

1. Transmission of Channel Status

The special VF Control is equipped with three line driving circuits, 18A, 16B, and 16A on 5.1.1, to transmit to the external device the status of three Vertical Format Unit channels ($\overline{Ch1}$, $\overline{Ch2}$, and $\overline{Ch8}$ or $\overline{12}$) for use by the operating program in tracking paper position. The outputs of the respective channels from the VFU are gated with the Run Remote condition, and the selection of either Ch 8 or Ch 12 (depending on the Vertical Format Unit supplied with the system) is accomplished by wire jumpering on the printed circuit board.

MEMORY CONTROL LOGIC

Electrical Diagram No. 6.X.X.
P.C. Board No. 2622

Functional Description

1. Clearing the Line Memory

In order to ensure that the Line Memory is free to accept a full line of data when communication with the external device or the internal test function begins, the Memory Control performs a "clearing" operation each time the system is switched from the Stop to the Run condition. Since the Line Memory functions as a shift register, it is necessary to address its entire length during a "padding" sub-cycle, while inhibiting data entry. In preparation for this "padding" operation, certain static conditions are established while the system is still in the Stop condition. The RUN (+) level (pin 46) from the Data Input Control is low and through gate 22D and inverter 19C on 6.1.3, forms a low (–) SYS CLEAR level and a high SYS CLEAR (+) level. Through gate 18C and inverter 19E it also holds the Memory Tracking Counter, 25 and 20, in a reset (zero count) condition. The high SYS CLEAR (+) level thus established, holds the Printer Rdy Register, 16A of 6.1.1, in a reset state through gate 11A, while the low (–) SYS CLEAR level holds the Print Data Latch, 17D/21A, reset, and the Inh Print Latch, 24C/9C on 6.1.2, set, and also inhibits the operation of the Master Clocking Oscillator, 14A/14B. Since the system is in a Stop condition, the (–) PRINT COMD level (Pin 23) from the Data Input Control is high and through gate 3C on 6.1.1, holds the Data Request Register, 4A, reset. Under these conditions, since all of the inputs to gate 21C are high, the (–) SET EOL level is low, and holds the EOL Register, 10B on 6.1.3, preset, through gate 17B and inverter 22B.

When the system is switched to the RUN condition, the RUN (+) level from the Data Input Control goes high and inverts the levels of the Sys Clear signals to release the "holds" previously established. Note that this is merely a release, and does not change the conditions of the registers and latches that were held. At this time, both inputs to gate 13B on 6.1.2 are low, the output of 13D is low, and the output of 13C is high, thus allowing the high-going (–) SYS CLEAR to remove the inhibit from the Master Clocking Oscillator, 14A/14B. The oscillator now produces a continual train of pulses, which are routed to the input of gate 7A. Since (–) PF CHAR and (–) DATA REQUEST are both high, gate 22A through inverter 12B produces a high, enabling input to gate 7A to generate (–) WRITE CLOCK pulses and WRITE CLOCK (+) pulses through inverter 19A. The (–) WRITE CLOCK pulses are routed to the Memory Tracking Counter, 25 and 20 on 6.1.3, and the WRITE CLOCK (+) pulses are routed to the line Memory to act as shifting commands. The WRITE CLOCK (+) pulses are also used to sample the status of the Memory Tracking Counter. While the Line Memory is being addressed in this manner, the LOAD BIT 8 (+) level from gate 3A on 6.1.1 is held low by the fact that (–) DATA REQUEST is still high. This inhibits data entry into the 8th (Tally) channel of the Line Memory. In later cycles, lack of data in the Tally channel signifies "no data."

The "padding" cycle continues until, at the leading edge of the 150th (–) WRITE CLOCK, the Memory Tracking Counter on 6.1.3 presents high inputs to gates 15C and 5D, and the trailing edge of that WRITE CLOCK (+) pulse switches the Q output of the Det 150 Register, 10A low. The rising edge of the $\overline{Q}$ output of the Register is delayed 3 to 6 microseconds at trigger 23B and inverter at 19F to preset the Register, thus forming a 3 to 6 microsecond (–) DET 150 pulse. At the leading edge of this pulse, the Inh Print Latch, 24C/9C on 6.1.2 is reset and removes the enabling input to gate 21C on 6.1.1, to cause the (–) SET EOL level to go high. This removes the preset on the EOL Register, 10B on 6.1.3, and the (–) DET 150 pulse clears that register and EOL (+) goes low. The low EOL (+) level, through gate 3B, trigger 8A, and gate 11A on 6.1.1, presets the Printer Rdy Register, 16A, to switch the PRINTER RDY (+) level high. This terminates the Line Memory clearing cycle, and informs the external device or the internal test function that the system is prepared to act upon a Paperfeed or Print Command.

2. Paperfeed Command – Remote Operation/Standard Interface

At the termination of the Line Memory clearing cycle, or at the end of a previous printing or paperfeeding cycle, the high PRINTER RDY (+) level is routed to the Compare Output Control to be trans-

mitted to the external device. Let us assume that, at this time, the external device is prepared to issue a forms control code to the printer, and raises the Paperfeed Command line. The (-) PAPERFEED COMD level (pin 44) from the Data Input Control now goes low and is gated at 6A on 6.1.1 with the low (-) PRINTER RDY level to preset the PF Char Register, 16B, through gate 17A. The low (-) PF CHAR level is routed to gate 22A on 6.1.2 to cause SEND DATA (+) to go high. This level is routed to the Compare Output Control for transmission to the external device as an indication that the printer has accepted the Paperfeed Command and is prepared to receive the instruction code. The external device will now transmit a Data Strobe to the printer which will be used to sample the instruction code on the Data Busses into the Paperfeed Control. The (-) DATA STROBE pulse (pin 48) from the Data Input Control is gated at 18A on 6.1.2 with the level indicating that a command has been recognized [in this case, (-) PF CHAR indicating the recognition of the Paperfeed Command] to form a positive going DATA STROBE (+) pulse. This pulse is gated at 17C on 6.1.1 with the high Q output of the PF Char Register, 16B, to form, through gate 11C and inverter 12C, a low-going (-) VF SAMPLE, which is routed to the Paperfeed Control and the VF Control for use in storing the instruction character. The (-) PF RDY level (pin 28) from the Paperfeed Control now begins to go high in answer to the VF Sample. However, the output of gate 17C (VF Sample time) acts as an inhibit at gate 7B. At the end of the VF Sample time, both lower inputs to 7B are high causing the output to go low, and through gates 5C and 6D, this clears the PF Char Register, 16B, which in turn (through the Compare Output Control) lowers the Send Data line to the external device. (Note that Send Data is terminated on the *trailing* edge of the transmitted Data Strobe).

When the SEND DATA level drops, the external device will drop the Paperfeed Command, and (-) PAPERFEED COMD (pin 44) from the Data Input Control will rise. Through gates 6A and 11B on 6.1.1, this will switch the Printer Rdy Register, 16A, to lower the PRINTER READY line transmitted to the external device through the Compare Output Control, and break communications until the requested paperfeed operation is complete.

When the VF Sample generated by the Memory Control was sent to the Paperfeed Control it answered by raising the PAPERFEED SET (+) level (pin 20) at the input to gate 24B on 6.1.2. At the time the external device drops the Paperfeed Command, (-) PRINTER RDY rises and gate 24B through inverter 19D generates a high FEED PAPER (+) level, which through the Level Converter causes paper to start moving. At the same time (-) VF BUSY from trigger 23A goes low and indicates to the Print Control that the system is occupied in feeding paper. At the end of the feeding cycle, PAPERFEED SET (+) and FEED PAPER (+) drop. However, the (-) VF BUSY level is held low by the trigger for approximately 8 milliseconds to allow for paper settling before the inhibit on an ensuing Print operation is removed. At the end of the feeding operation (not including settling time), the (-) PF RDY level (pin 28) from the Paperfeed Control goes low, and through gate 7B on 6.1.1, inverter 12F, gate 3D, trigger 8B, and inverter 12E, presets the Printer Rdy Register, 16A, to indicate to the external device, through the Compare Output Control, that the operation is complete, and the system is prepared to accept another command.

3. Print Command – Remote Operation/Standard Interface

When the external device is prepared to transmit data to be printed, its answer to the Printer Ready level from the Compare Output Control will be to raise the Print Command line. At this time the (-) PRINT COMD (pin 23) from the Data Input Control drops and through gate 3C on 6.1.1, removes the holding clear on the Data Request Register, 4A. At the same time the low (-) PRINT COMD level is gated with the low (-) PRINTER RDY level at gate 6B, and through inverter 12D, sets the Print Data Latch, 17D/21A. The rising output of 17D switches the Q output of the Data Request Register, 4A, high, and the low $\overline{Q}$ output forms a high LOAD BIT 8 (+) level through gate 3A to condition the Tally channel of the Line Memory for the ensuing load cycle. The high DATA REQUEST (+) level is routed through gate 18D on 6.1.2 to set the Inh Print Latch, 24C/9C. The low (-) DATA REQUEST is routed through gate 22A on 6.1.2 to form a high SEND DATA (+) level to be transmitted to the external device by the Compare Output Control as an indication that the Print Command has been accepted and the system is ready to accept data for printing. At the same time the low (-) DATA REQUEST level is routed through gate 24A to present a high WRITE (+) level to the Line Memory to indicate that ensuing data should be loaded.

The external device now answers the Send Data line by transmitting Data Strobes which act as samples for levels it has established on the input Data Busses. The low-going (–) DATA STROBE pulses (pin 48) from the Data Input Control are gated at 18A on 6.1.2 with the fact that a command has been accepted [in this case the (–) DATA REQUEST level at gate 22A] and forms positive-going DATA STROBE (+) pulses. These pulses, through gate 7A and inverter 19A, generate (–) WRITE CLOCK and WRITE CLOCK (+) pulses to be used in addressing and tracking the Line Memory.

When the external device has transmitted the Data Strobe identifying the last character to be loaded into Memory, it drops the Print Command. At this time the (–) PRINT COMD level from the Data Input Control rises, and through gates 6B and 11B on 6.1.1, resets the Printer Ready Register, 16A, and through gate 3C, clears the Data Request Register, 4A. This results in both the Printer Ready and Send Data lines transmitted to the external device from the Compare Output Control, dropping. At this time communications are broken until the printer has processed (printed) the data just loaded, and is prepared to accept another command.

If, during the data loading cycle described above, the external device transmits more than 132 characters, on the 132nd Write Clock (derived from the Data Strobe) gate 5A on 6.1.3 detects the count in the Tracking Counter, and through gate 15B, raises the D input to the EOL Register, which is then set on the trailing edge of the Write Pulse. The high EOL (+) level is routed through gate 3C on 6.1.1 to clear the Data Request Register, 4A. This drops the Send Data line to the external device to indicate that the Line Memory has been filled and any further data transmitted will be ignored. The Printer Ready line to the external device is maintained high, however, until the Print Command is dropped.

4. Print Command – Remote Operation/First Character Interface

When the system is provided with a First Character Interface, it is not necessary for the external device to transmit Paperfeed Commands, since the Memory Control will interpret the first data character transmitted with each Print Command as a Paperfeed Instruction code and will store that code for use in controlling form feed after the next print cycle. All characters following the first are stored in the Line Memory and printed after the Print Command drops.

When the (–) PRINT COMD level (pin 23) from the Data Input Control goes low, the output of gate 6B on 6.1.1 rises and switches the PF Char Register, 16B, to produce a (–) VF SAMPLE from the first Data Strobe through gates 17C and 11C and inverter 12C. The Print Data Latch, 17D/21A, is also set by Print Command, and the low (–) PRINT DATA level at gate 24B on 6.1.2 prevents the high PAPERFEED SET (+) level received from the Paperfeed Control in answer to the VF Sample, from generating the FEED PAPER (+) signal. The PAPERFEED SET (+) signal takes effect only after the Print Data Latch is reset at Print Finish time, and the result is a Feed after Print operation.

The trailing edge of the VF Sample resets the PF Char register, 16B, in the same manner as described in paragraph 3 above, and all characters following are loaded into the Line Memory, also as described above.

5. Local (Test) Commands

When operating in the Local mode, the Data Input Control utilizes the high PRINTER RDY (+) level (pin 27) in combination with the (–) PRINTER BUSY level to simulate both the Paperfeed and Print Commands. These two commands are generated simultaneously, resulting in operation similar to Remote Operation with First Character Interface, described in paragraph 4 above.

In order to simulate the Data Strobes, the Master Clocking Oscillator, 14A/14B, is caused to generate Test Strobes during the load cycle. The low (–) RUN LOCAL level is gated with (–) LOAD DATA on 13A on 6.1.2. (–) LOAD DATA originates at gate 11B on 6.1.1, and goes low upon receipt of a Command from the Data Input Control. At this time, the output of gate 13A on 6.1.2, goes high and through gates 13D and 13C starts the oscillator running. The output of the oscillator through inverter 19B, is gated at 18B with the low (–) LOAD DATA level, and forms positive-going TEST STROBE (+) pulses. These are routed to the Data Input Control where they are gated with the Local condition then re-routed to the Memory Control as Data Strobes. When 132 Test Strobes have been sent, the Memory Tracking Counter causes the Send Data level to drop (as described in paragraph 3 above) and the Test Print Command is terminated by the Data Input Control.

6. Padding the Line Memory

Since the Line Memory is made up of 150 bit long MOS shift registers, it is necessary to move the loaded data, which may consist of 1 to 132 characters, to the end of the registers to position it properly for the un-loading cycle. As the data is being positioned, blanks (no bits) are "padded" into the registers so that "short line" print-out is possible.

At the end of the load cycle, when the dropping of the Print Command clears the Data Request Register, 4A on 6.1.1, the (–) DATA REQUEST level goes high and through gate 21C generates a low (–) SET EOL level. This sets the EOL Register, 10B on 6.1.3. PRINTER RDY (+) going low removes the inhibit on gate 13B on 6.1.2, and through 13D and 13C starts the Master Clocking Oscillator, 14A/14B, whose output is gated through 7A to produce Write Clocks which continue to address the Line Memory. This continues until the Memory Tracking Counter, 25 and 20 on 6.1.3, reaches a count of 150, at which time register 10A is set and produces a 3 to 6 microsecond low-going (–) DET 150 pulse. The pulse resets the Inh Print Latch, 24C/9C on 6.1.2, to stop the Master Clocking Oscillator. The INH PRINT (+) level going low at the input to gate 21C on 6.1.1, raises the (–) SET EOL level which, through gate 21B generates a low (–) INITIATE PRINT level, which indicates to the Print Control that both the loading and "padding" operations are complete and the system may now enter a Print Cycle.

7. Memory Control During the Print Cycle

When the Print Control has acted upon the Initiate Print Command, it answers by raising the SCAN DATA (+) level, which through gate 18D on 6.1.2, sets the Inh Print Latch, 24C/9C. The output of the latch, through gates 13B, 13D, and 13C starts the Master Clocking Oscillator, 14A/14B, running. The oscillator output, through inverter 19B, is gated with the high SCAN DATA (+) level at 22C to deliver to the Print Control low-going (–) PRINT STROBE pulses, which are used to synchronize the Print Control operation with the Line Memory read-out. At the same time the oscillator generates, through gate 7A, (–) WRITE CLOCK pulses for use in Memory tracking, and through inverter 19A, WRITE CLOCK (+) pulses which address the Line Memory. As each data character is read from the Memory, the Memory Control checks the status of the Tally channel, LM BIT 8(+) (pin 13). When this level is high, it indicates that a character is present on the Memory's output busses and, through gate 9D and inverter 12A on 6.1.2, forms a high COMP GATE (+) level to direct the Compare Output Control to compare the Line Memory character with the character in printing position on the print drum. If a comparison exists, the Compare Output Control lowers the (–) COMPARE level (pin 15) and through gate 24A on 6.1.2, the Memory Control raises the WRITE (+) level, to direct the Line Memory to empty that position, i.e., not to re-circulate data. If no comparison occurs, the (–) COMPARE level is high and the WRITE (+) level is low, directing the Line Memory to re-load the data.

Memory addressing continues until the Tracking Counter, 25 and 20 on 6.1.3, steps to a count of 132 to set the EOL Register 10B. The low (–) EOL level is routed through gate 24A on 6.1.2 to prevent data re-circulation in Memory. Note that at this time, the Master Clocking Oscillator is still running and the Line Memory continues to be addressed until the Tracking Counter steps to 150, and (–) DET 150 (10A on 6.1.3) goes low to reset the Inh Print Latch, 24C/9C on 6.1.2. This stops the oscillator and terminates the cycle. Addressing the Line Memory for its full length (150 characters) is necessary to position data properly after each scan.

The above cycle is repeated each time the Print Control raises SCAN DATA (+). For each Character Strobe from the print drum, and during each scan, data is compared, until eventually, the Line Memory is empty and a scan will take place in which LM BIT 8 (+) remains low for the entire cycle. At this time the End Print Register, 4B on 6.1.2, which was set at the start of the scan by SCAN DATA (+), will not have been reset by LM BIT 8 (+) at the termination of the scan. The low (–) END PRINT level is sampled at this time by the Print Control, and interpreted as a command to end the Print Cycle and generate the (–) PRINT FINISH pulse. This pulse resets the Print Data Latch, 17D/21A on 6.1.1, which through gate 3D, produces a high input to trigger 8B. 1 to 3 microseconds after the termination of the (–) PRINT FINISH pulse, the output of trigger 8B goes high, and through inverter 12E, presets the Printer Ready Register, 16A, as an indication that the system has completed the operation and is prepared to accept another command.

8. Aborting a Load Cycle

Under normal conditions, if the operator should push the STOP button while data is being loaded into the Memory, the Data Input Control, to prevent loss of information, will delay switching the system out of the Run condition until the printer is not busy, i.e., it has finished the operation in process. However, if the STOP button is pushed while data is being loaded, and for some reason, the external device ceases transmission, it is necessary to force a not Run condition after a reasonable delay. When STOP (+) (pin 22) goes high it starts a time-out of approximately 75 milliseconds in trigger 8A. After that time, the output of the trigger goes high, and through gate 11A, clears the Printer Ready Register, 16A, causing a print-out of the loaded characters, after which the system is switched out of the Run condition.

MOS 8 X 132 MEMORY

Electrical Diagram No. 6.X.X.
P. C. Board No. 2623

Functional Description

The Line Memory is an 8 X 132 bit, sequential access semi-conductor system, which uses MOS static shift registers as its basic storage elements. This 8 X 132 Memory (P.C. board 2623), with the addition of a single jumper to the back-board wiring, is interchangeable with D.P.C. 8 X 150 MOS Memory (P. C. board 2610). The required jumper carries signal LOAD DATA (+), which originates on the Memory Control and is outputed on pin 11 of the Memory Control. LOAD DATA (+) inputs the 8 X 132 Memory on pin 28 (6.2.2). (Note: Pin 28 is unused on the 8 X 150 Memory, P.C. board 2610.)

1. Compatibility

The 8 X 132 Memory, to be compatible and interchangeable with the 8 X 150 Memory, must be capable of accommodating 150 shift pulses for proper positioning of data. This is accomplished by decoding and gating an 8-bit binary counter (on 6.2.2), such that shift pulses (–) W CLOCK are inhibited between the counts of 133 and 150 during all write or read cycles.

DATA LOW (+), when low, holds the counter in the cleared state. When a Load Data cycle is initiated, DATA LOAD (+) will go high and remain high until both the Load Data and Print Cycles have been completed. With LOAD DATA high, the leading edge of each WRITE CLOCK (+) will cause the 8-bit binary counter to advance one count. Gate 6D on 6.2.2 will become active at a count of 132. The active state of 6D provides a low-level D input to register 5A, thereby allowing the trailing edge of the WRITE CLOCK (+) pulse (which advanced the counter to 132) to reset register 5A. The Q output of 5A going low will lock 5A in its cleared state and inhibit, via gate 6C, the further generation of (–) W CLOCK pulses. Each successive WRITE CLOCK will then advance the binary counter until a count of 150 is reached.

At the count of 150, via gates 9B and 6B, the D input of register 5B will go low, allowing the 150th WRITE CLOCK (+) pulse to clear 5B which, in turn, clears the 8-bit to zero, presets register 5A, and enables trigger circuit 9A to cycle. When 9A completes its cycle, its output gated with LOAD DATA (+), via gate 6A, provides a preset to 5B. At this time, the 8 x 132 Memory is conditioned to start its next cycle or sub-cycle.

2. Write (Load) Data Cycle (Refer to Figure D-5)

During the load cycle, the high WRITE (+) level from the Memory Control is inverted on 6.2.2 to provide a (–) WRITE signal to 6.2.1. (–) WRITE is then inverted to form a high level which enables all of the input data bit [(–) Bit 1 through (–) Bit 6, (–) Bit 8 (See note on 6.2.1), and LOAD BIT 8 (+)] lines on 6.2.1. Note that during the load cycle, LOAD BIT 8 (+) is held high by the Memory Control

in order to insert a "Tally" bit in each Memory position loaded. To load data, the Memory Control generates positive-going, WRITE CLOCK (+) pulses, which, via gate 6C on 6.2.2, provide (–) WRITE CLOCK pulses to shift and store data in the MOS shift registers on 6.2.2.

At the end of the load cycle, the Memory Control lowers the LOAD BIT 8 (+) line, but maintains the high WRITE (+) level, and continues to send Write Clock pulses, to "pad" the Memory with no "Tally" bits, until 150 Write Clock pulses have occurred. This terminates the Load cycle, and the Memory is prepared to be addressed in an un-loading (Read/Re-Circulate) cycle.

3. Read/Re-Circulate (Unload) Cycle (Refer to Figure D-6)

During this cycle, the Compare Output Control through the Memory Control, determines whether data read out from the Memory is to be replaced. As the system enters the Print Cycle, the Print Control raises the PRINT (+) level, which is bufferred through gates 7C and 7A on 6.2.1 and acts as an allowing level on the Memory's output busses. At the rise of PRINT (+), therefore, data in the last stages of the registers is presented to the system on the (–) LM BIT lines to be compared with the character code of the symbol in printing position. If the two codes do not compare, the Memory Control holds the WRITE (+) level low, which results in the data being recirculated in the MOS shift registers. Therefore, at the trailing edge of the Write Clock pulse, that data is statically re-stored in the input stages, and all other data is shifted one position, so that the data originally in the second-to-last position in Memory, now appears at the output busses.

If data on the output busses compares with the print character, the Memory Control raises the WRITE (+) level to inhibit the re-entry of the compared code.

For each scan of Memory, this cycling continues until 132 columns have been addressed. Then the Memory Control holds the WRITE (+) line high to prevent any further data re-entry while it "pads" to a count of 150 to position data correctly for the start of the next scan.

The scanning cycles repeat until such time as no further "Tally" bits (LM BIT 8) are in the Memory, and the Memory Control signals the Print Control to end the Print Cycle.

Figure D-6 represents the start of a Read/Re-Circulate cycle in which the second code (next-to-last position) in Memory compares with the code from the print drum.

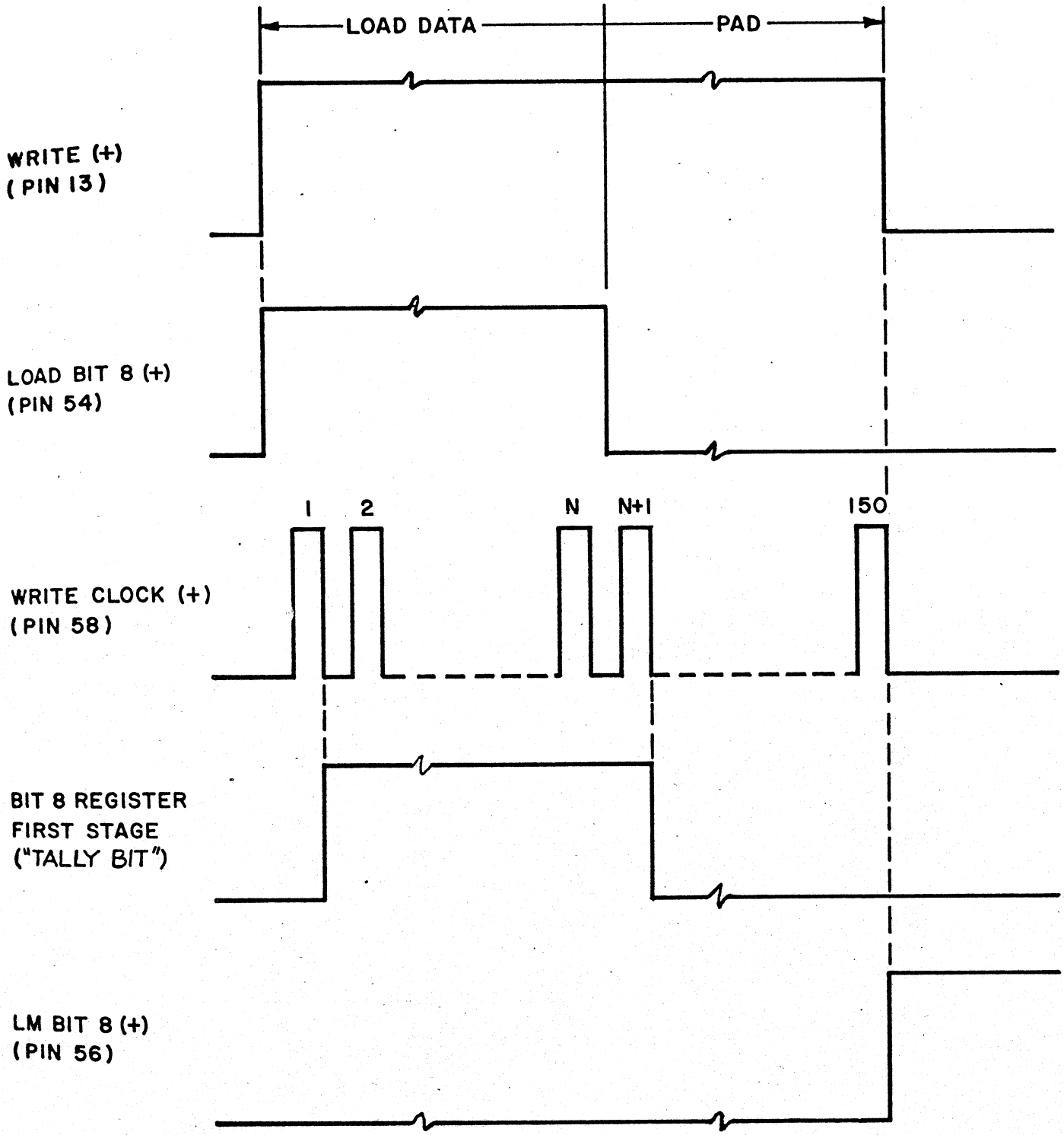


Figure D-5. Line Memory Load Data Cycle, Timing Diagram

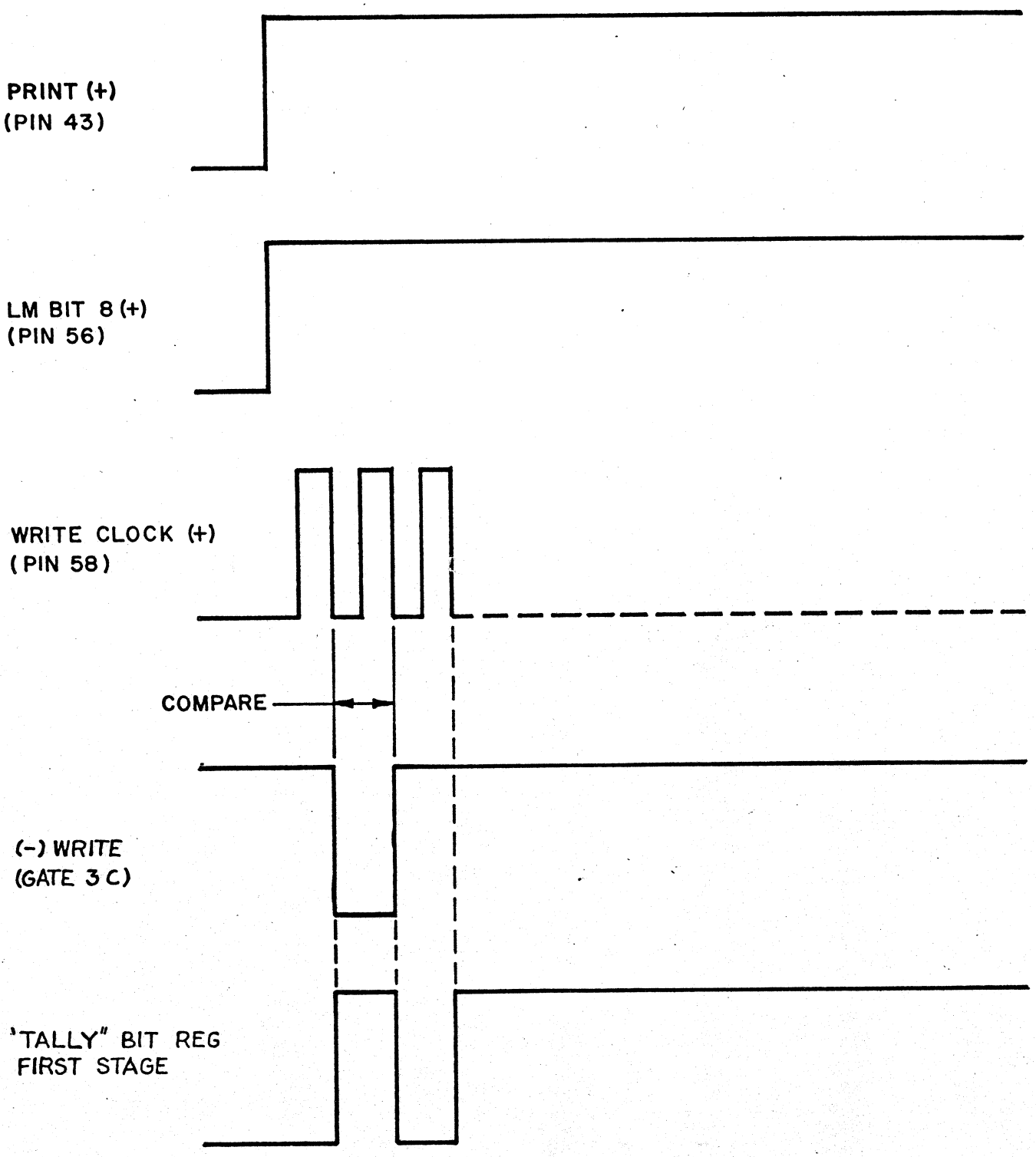


Figure D-6. Line Memory Read/Recirculate Cycle (2nd Character Compares), Timing Diagram

Electrical Diagram No. 7.X.X.
P. C. Board No. 2628

Functional Description

1. Paper Feed Control

The FEED PAPER (+) level is brought into the Paper/Ribbon Control card through pin 41 (7.1.2) and is inverted at gate 3B to form the (–) MOVE PAPER signal. On 7.1.1, this signal is buffered through parallel inverters (1D, 1E, and 1F) to provide the necessary current for driving the paper feed circuitry.

Previous to the receipt of a FEED PAPER (+) command from the system's control logic, the lower Darlington pair (Q7 and Q8) is off; i.e., pin 25 is at +40V. This level causes the upper Darlington pair (Q5 and Q6) to be on, drawing current from +40V through the brake coil and into the 75-ohm resistor (pin 32). This current is known as "Brake Hold Current" and equals 40/75 or 533 milli-amps. It should be noted that at this time, the 350-microfarad capacitor connected to pin 30 is charged to +40V.

When (–) MOVE PAPER goes low (a command from the control logic to move paper), the outputs of the three buffering inverters (1D, 1E, and 1F) go high to turn the lower Darlington pair on and the upper Darlington pair off. As the upper pair turns off, "Brake Hold Current" is removed and, as the lower pair turns on, it will initially draw high current ("Clutch Pulse Current" = 5.5A peak) through the clutch coil from the charged 350-microfarad capacitor. After the capacitor is discharged, the circuit will continue to draw "Clutch Hold Current" through the 50-ohm resistor (800 milli-amps), for as long as the (–) MOVE PAPER signal remains low. It should be noted that, at this time, the 350-microfarad capacitor is discharged.

When the (–) MOVE PAPER level goes high at the end of the paper feed cycle, the lower Darlington pair is turned off and the upper pair is turned on. Initially, the upper pair will draw high current ("Brake Pulse Current" = 5.5A peak) through the brake coil into the discharged 350-microfarad capacitor. After the capacitor is charged, the circuit will continue to draw "Brake Hold Current" through the brake coil into the 75-ohm resistor (533 milli-amps) for as long as the (–) MOVE PAPER signal remains high. (Refer to Figure D-7.)

2. Ribbon Feed Control

Ribbon feed is activated only during the print cycle; i.e., when the PRINT (+) level (7.1.2 – pin 12) is high. This level is inverted at 1C to pre-set the two-stage counter (2A and 2B), so that the output of gate 3C is low. This low level is gated with the ribbon direction levels at gates 3A and 3D to turn on either Q1 or Q2 and energize one of the ribbon feed solenoids.

When PRINT (+) goes low at the end of the print cycle, the pre-set level is removed from the two-stage counter (2A and 2B) and, after three INDEX (+) pulses from the print drum are received, both inputs to gate 3C are low and its output goes high, thereby deenergizing the ribbon feed solenoid. Counting of three INDEX (+) pulses; i.e., three print drum revolutions, is necessary, since the ribbon feed mechanism utilizes a pawl and ratchet driven from the print drum. Three drum revolutions are required to cause a single ratcheting action.

3. Ribbon Reversing Control

Two magnetic reed switches at the ribbon feed mechanism are utilized to detect the end of ribbon in either direction. As the ribbon is feeding from the top to the bottom mandrel (lower ribbon feed solenoid engaged), its depletion is detected by the Upper Ribbon End Switch; i.e., closure of this switch is a command to reverse the direction of feed and start moving ribbon from the bottom to the top mandrel. The Lower Ribbon End Switch detects ribbon depletion on the bottom mandrel.

Closure of the Lower Ribbon End Switch (7.1.2 – pins 44 and 46) causes the contact of relay K1 to close and latch, and closure of the Upper Ribbon End Switch (pins 43 and 45) causes the contact to open. The latching relay is used to "remember" the last ribbon direction command when power is shut down.

To understand the operation of the ribbon reversing logic, consider the following example. Ribbon is feeding from the top to the bottom mandrel; i.e., the contact of relay K1 is closed which, through inverter 1A, produces a high level at the input to gate 5D. The other input to this gate is also high at this time, hence its output is low causing the Lower Ribbon Feed Solenoid to be energized. As the ribbon is depleted from the upper mandrel, the Upper Ribbon End Switch closes momentarily and opens the contact of relay K1, transferring the high level from the input of gate 5D to the input of gate 5C. This immediately de-energizes the Lower Ribbon Feed Solenoid; however, the upper ribbon feed solenoid is not energized at this time since the Q output of register 6B into gate 5C is low. After two INDEX (+) pulses through inverter 1B are counted by registers 6A and 6B, the Q output of 6B into gate 5C goes high. (This represents at least one full drum revolution.) At this time, the output of gate 5C goes low and energizes the Upper Ribbon Feed Solenoid. The delay between the de-energizing of one solenoid and the energizing of the other ensures that the two ribbon feed pawls are not engaged at the same time.

4. Ribbon Tracking Control

The ribbon mechanism contains two sets of switches which monitor the position of the left-hand edge of the ribbon. Each set contains two switches, one of which closes when the ribbon has skewed to its left-most limit, and the other closes when the ribbon has skewed to its right-most limit. Only one set of switches is active at a time; i.e., the upper set is active only when ribbon is feeding onto the upper mandrel, and the lower set is active only when ribbon is feeding onto the lower mandrel.

The closures of these ribbon tracking switches are interpreted as commands to skew the ribbon to its other limit. The actual skewing is accomplished by the action of two solenoids located at the right-hand side of the ribbon mandrels, and are linked in such a manner that when the upper solenoid is energized, the right-hand side of the upper mandrel is angled inward and the right-hand side of the lower mandrel is angled outward. The opposite is true when the lower solenoid is energized. This ang ling of the mandrels causes the ribbon to skew either to the right or to the left, and is dependent upon which way the ribbon is feeding.

To understand the operation of the control logic, consider the following example. The ribbon is feeding onto the top mandrel, and is being skewed to the left. This means that the lower ribbon tracking solenoid is energized and the right-hand side of the lower mandrel is angled inward. As the ribbon reaches its left-most limit, the Upper Outboard Ribbon Tracking Switch (7.1.2 – pins 15 and 47) closes to reverse the setting of latch 7B/7C; i.e., the output of 7B goes high. This output gates with the high output of relay K1 at gate 5B. The output of 5B goes low and, through gate 7A, turns on transistor Q3 to energize the Upper Ribbon Tracking Solenoid. This causes the ribbon to skew to the right until its right-most limit is reached.

Note that the angling of the ribbon mandrels is opposite to that described above when ribbon is feeding onto the bottom mandrel.

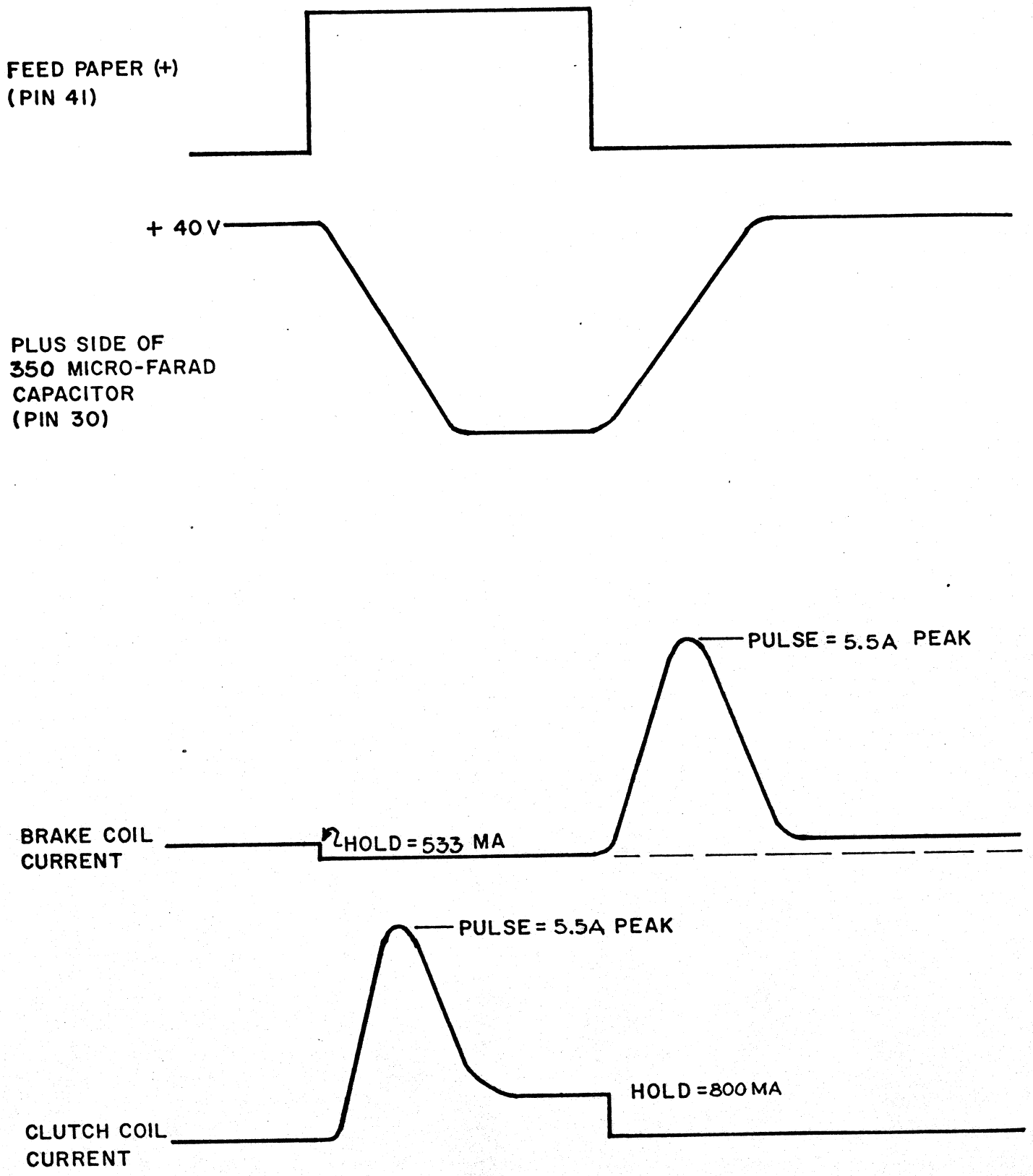


Figure D-7. Paper/Ribbon Control Paper Feed, Timing Diagram

LEVEL CONVERTER

Electrical Diagram No. 8.X.X.
P. C. Board No. 2615

Functional Description

1. Reluctance Pickup Amplifiers

The four amplifiers shown in the schematic are identical in configuration and operation; therefore, in discussing timing considerations, only the Character Strobe amplifier is considered.

The amplifiers are configured as zero-cross detectors with built-in hystersis for noise rejection. The outputs are isolated from the lines to the control logic through TTL inverters.

The output of the reluctance pickup is fed to the positive (+) input of a voltage comparator (u710) through a current limiting and by-pass filter network. As the signal at the (+) input rises above the level of the negative (–) input (ground), the output of the comparator switches to a positive TTL level. The output is fed back to the (+) input to aid in switching, and also to supply current through the limiting resistors to the winding of the reluctance pickup. This feed-back raises the base level of the input signal by approximately 100 millivolts, thus requiring at least a 100-millivolt negative swing from neutral on the pickup line to cause reverse switching of the amplifier. During the next portion of the cycle, the pickup output swings negative more than 100 millivolts, and the (+) input to the comparator falls below the (–) input. At this time, the comparator output switches to 0 vdc and, through the feed-back resistor, removes the 100-millivolt bias on the reluctance pickup. Timing considerations (see Figure D-8) show that, due to the shape of the teeth on the pulse generator, the rising edge of the output of the comparator is the significant edge used by the control logic for timing purposes.

2. Alarm

The two timing circuits (SG83) shown on the schematic are used to detect the absence of character strobe pulses from the output of the amplifier. The HD Card Interlock and yoke latch switch are also monitored by these elements.

The output of each timing circuit switches to "1" only if its input remains positive for the length of time determined by the resistor-capacitor network (approximately 4 milliseconds). Thus, if the character strobe remains positive or zero for more than 4 milliseconds, or if the card interlock or the yoke latch switch opens, one of the timers switches positive and presents a (–) ALARM signal to the control logic through an associated NOR gate.

3. Bus Drivers

The (–) CLEAR HD MEM, (–) LOAD HD MEM, and TRANSFER HD MEM (+) drivers convert TTL signal levels from the control logic, through a double-inverting amplifier with relatively high current-sinking to ground capabilities. These drivers address the multiple input busses on all of the Hammer Drivers.

4. FIRE HD (+) Driver

The drive utilizes a differential amplifier to control the positive level of the Fire pulse delivered to the Hammer Drivers. FIRE (+) from the control logic is double-inverted to present a zenered positive level at the resistor tree. The arm of the potentiometer in the tree is wired to the left side of the differential amplifier to establish a controlled and adjustable level during FIRE (+) time. This starts to turn the output transistor off [FIRE HD (+) rises] until the right side of the differential amplifier supplies the differential emitter current. At this time, the output level is controlled. If an alarm condition occurs, the (–) ALARM signal inhibits the driver at its input.

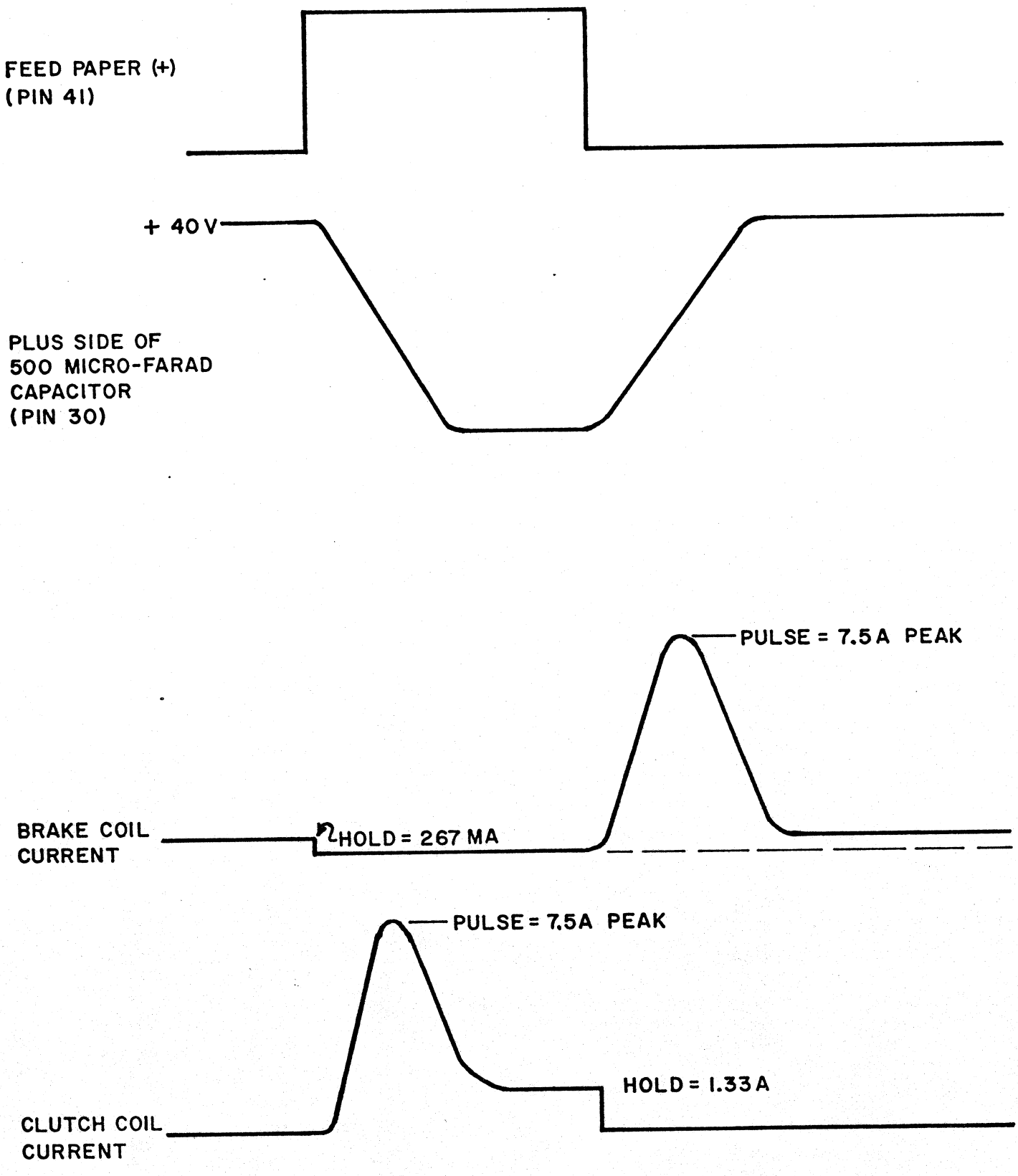


Figure D-8. Level Converter Character Strobe, Timing Diagram

Electrical Diagram No. 9.X.X.
P. C. Board No. 2601

Functional Description

For the purposes of this discussion, it will be assumed:

a) the printer is a 132 column model; i.e., there are 17 Hammer Drivers containing a 136-bit shift register,

b) the system is in a "Print Cycle",

c) the scan of the line memory involved is one in which all data compares with the code for the character coming into print position; i.e., the letter "B", for example, is to be printed in all columns; the following scan is one in which no comparisons occur, and

d) the Hammer Driver under discussion is the last one in the series; i.e., the one which will cause print-out to occur in columns 1 through 8.

The numbers across the tops of the timing diagrams refer to times in microseconds after the print drum code has been established, e.g. time B0614 occurs 614 microseconds after the "B" code from the print drum has been set up. The times shown for the various pulses are nominal and may vary from system to system within the limits described in Appendix A.

1. Load and Transfer Cycles

Immediately after the "B" code from the print drum has been established in the control logic, any data in the Hammer Driver shift register is transferred from each stage to the storage latches by means of the TRANSFER HD MEM (+) pulse. All stages of the shift register are then cleared to the "0" state by (–) CLEAR HD MEM.

In preparation for the ensuing shift register loading sequence, (–) PRESET D forces the 136th stage of the shift register on the first Hammer Driver in the series (not the Hammer Driver under discussion) to the "1" state. This is known as a flag bit and will be used to signal the control logic when it has been shifted to the end of the register.

The (–) LOAD HD MEM pulses which now occur are synchronous with pulses which address the system's line memory, and when comparison occurs, the (–) LOAD HD MEM pulse accompanying the comparison causes the 136th register stage to be set, while any other data in the register is shifted down one stage. In the case under discussion, it will be noted that the flag bit inserted at the beginning of the cycle appears at the input to the 8th stage on the trailing edge of the 128th load pulse (B128), and is shifted into the 8th stage on the trailing edge of B129.

At B136 time, the flag bit now appears at the output of the first stage of the shift register as HD Mem Flag (+) and signals the control logic to provide one more shift pulse to "dump" the flag bit and align the data in the register with the proper print columns.

When the next code from the print drum has been established in the control logic (C0000), the data held in the shift register stages is transferred to the corresponding storage latches on the Hammer Driver. The shift register is then cleared down as in the previous cycle, and the loading sequence is repeated. Referring to Figure D-9, it will be noted that the loading sequence between C0000 and D0000, causes only the flag bit to be shifted through the register since no comparisons occurred during that cycle.

2. Fire Cycle

The FIRE HD (+) pulses "sample" the outputs of the storage latches by means of the resistor-diode networks and, if a latch is at "0", the node of the network is held at OV and the transistors in the current amplifier section remain off. If, however, the latch is at "1" (as during time C0000 to D0000), the Fire pulse causes the node of the network to rise to a controlled level. This level turns the first stage transistor on which, through an intermediate stage, turns the power driver on, which draws current through the associated actuator coil and through the 0.5-ohm precision resistor. The voltage at the

precision resistor is sensed by the emitter of the first stage transistor, which causes the current through the resistor (and thus through the actuator coil) to be limited and controlled at a level defined by the voltage at the base of the first stage transistors. When the Fire pulse returns to O V. (C1452), the transistors are turned off, and the inductive voltage swing-back from the actuator coil is clamped by the Zener diode.

It has been mentioned that the FIRE HD (+) pulses are of controlled level and width. Since various circuit voltage drops will have an effect on the final current output, the dimensions of the Fire pulse are adjusted while scoping a test point on one of the Hammer Drivers, while the associated circuit is operating. (See Figure D-10.)

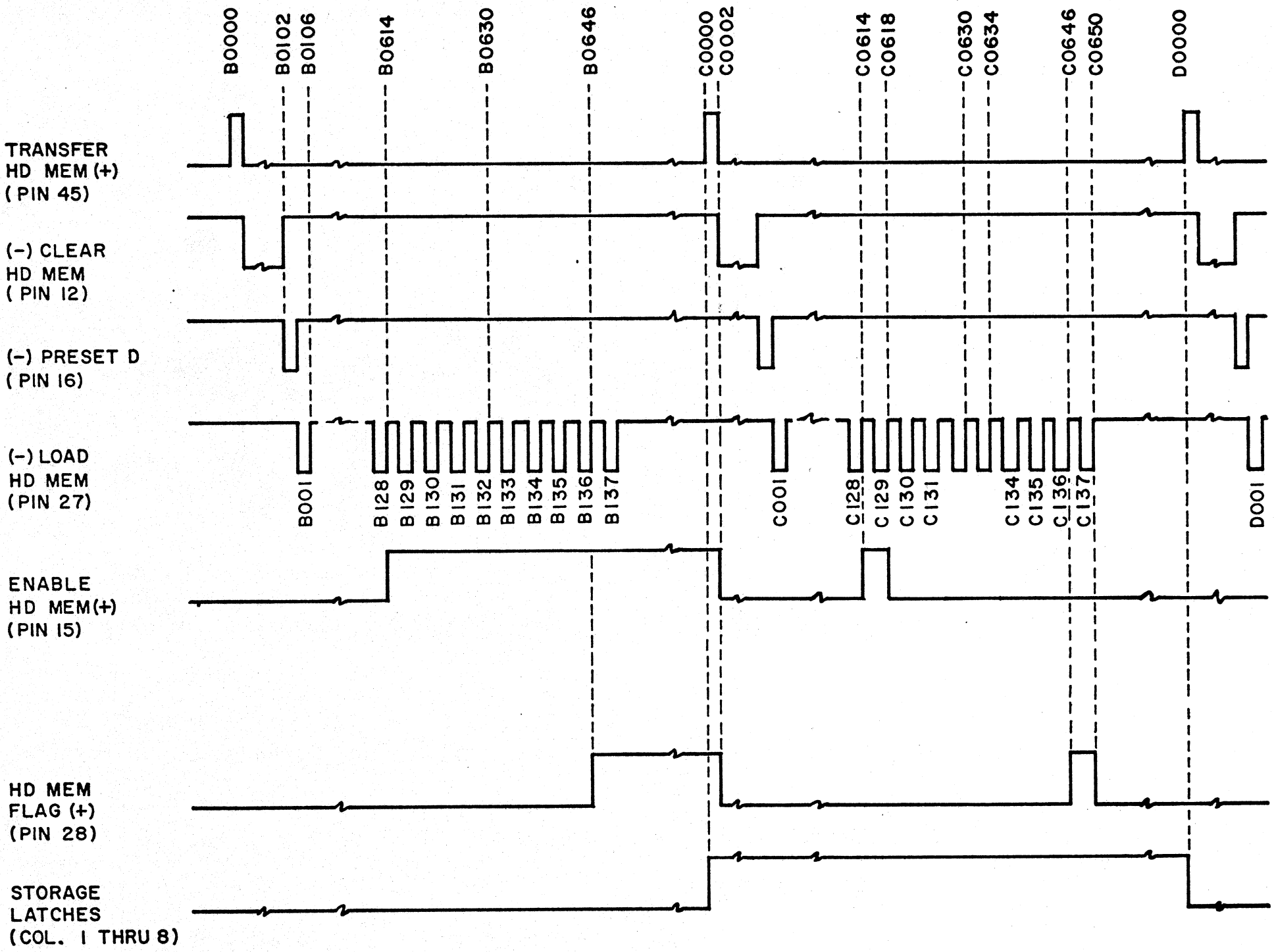


Figure D-9. Hammer Driver, Load and Transfer Cycles, Timing Diagram

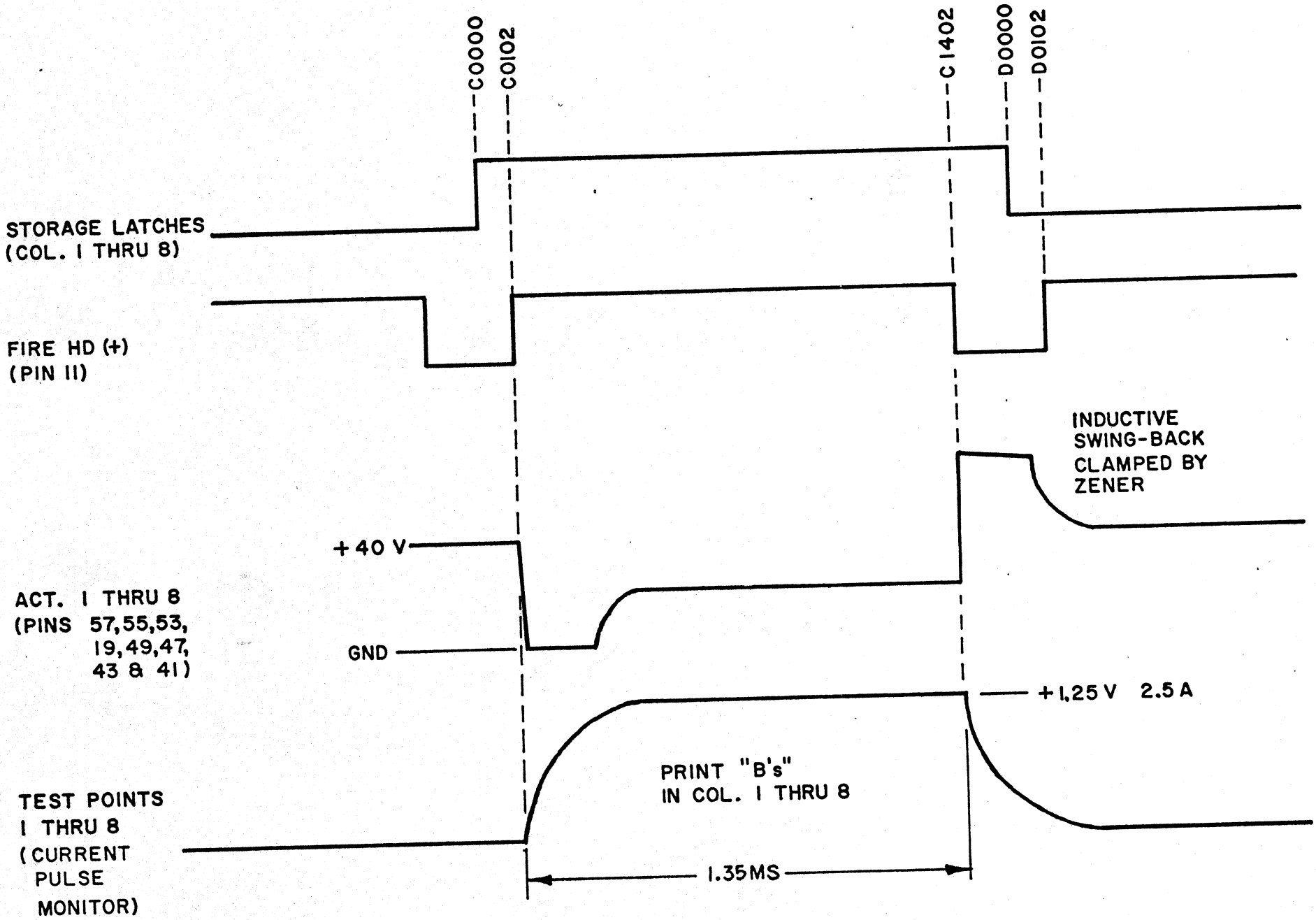


Figure D-10. Hammer Driver Fire Cycle, Timing Diagram

No Case

D 12026-C	D	D 12002-?	A	CHAIN TRAIN PLB
D 12004-C	H	D 12004-A	H	
D 12006-C	H	D 12006-A	H	Comp.
D 12028-F	H	D 12008-B	B	
D 12036-?	E	D 12010-C	D	(ROM PRINT CTL 12032-?) A
D 12012-D	J	D 12012-C	J	
D 12014-C	F	D 12014-A	F	

EVC OR LATER Need A+D ←

Are Compatible

W/S Air 1-26-77

12:00 called
Marie will call back date

6 hrs 8:55 called Marie status of Data
still no answer expressed importance she
will try to have answer by afternoon

12:00 Marie called gave info

10002 Rev. A sh. 6 clgd. value of R10, R11 and C9 to accommodate 600 LPM printer on sh. 3 added note 2

REV. B added Refs to 13.0.1 diag. on sh. 1

ON HAND

REV. C removed broken line between 16 packs 40A and 33B and replaced with solid line on sh. 5

REV. D ECN 223, 210

REV. E ECN 243

REV. F ECN 247

REV. G ECN 394, 403

REV. H ECN 504

10003 REV. A sh. 1, R4 was 12K; Minor info. and note clgs. on all shts.

REV. B added note to sht. 1; Note 3 to sht. 3 VFU output line to sh. 5

REV. C Removed optional paper runaway detect circuit on sh. 1.

REV. D ECN 212

REV. E ECN 242

REV. F ECN 262

REV. G ECN 301

REV. H ECN 414

10005 REV.A on sh.2 (4.0.2.) chgd. CLR input (IC8-13) from +VG to CT RDY (+)
REV.B sh.2 (4.0.2.) added high speed option
REV.C combined (4.0.5.) with (4.0.4.) deleted sh.5 updated notes and info on all pages
REV.D ECN 371

10006 REV.A sh.1 chgd. value of R1, R2, R3, R4, R5, R6 and C7. Removed HD interlock CKT (IC6-F) from ready (+) CKT and conn. to yoke ready (+) CKT. sh.2 chgd. value of R19. sh.3 deleted paper clamps CKT (Q1, Q2, R28, R30, CR12 and CR13. sh.4 and 5 chgd. value of C26, C27, C28 and C29.
REV.B added .001 mf Cap (C35) to (-) CLR step count
REV.C updated info
REV.D added B15, B25 and B37 lines to sh.1. added note to sh.1. on sh.2 added (4.0.6) and (13.0.1) Refs, CR7 was IN5338; on sh.3 added B2 and B6 lines
REV.E ECN 225
REV.F ECN 237

10006 REV. G 407, 408, 428
REV. H 911
REV. J 912

10007 REV. A R11 and R13 were 51K; C5 and C7 were 25 MFD. (IC 1-9) was ref n.
REV. B added saturable reactor
REV. C Chgd. TB No.
REV. D ECN 219, 214
REV. E ECN 239
REV. F ECN 906

10020 REV. A —
REV. B General Chgs.
REV. C Chgd. wave form at test point 1.
REV. D ECN 496

10021 REV. A Chgd. C4, C8, R9 and R10
REV. B corrected values and designations of components
REV. C Chgd R11. Removed +Vg from 2B-3 and tied 2B-3 8A-12 Chgd. R12
REV. D added timing info and note 1
REV. E Chgd. preset and clear inputs on IC's 16 and 20 On sh 4. Added IC 37 on sh. 3

C10021 REV. F added C24 and C25
REV. G ECN 221 and 224
REV. H ECN 238

10022 REV. A ECN 399

10033 REV. A ECN 213, 216 and 228
REV. B ECN 241
REV. C ECN 359
REV. D ECN 419
REV. E ECN 796

TITLE

INITIAL MODIFICATION KIT
DATA PRINTER CORP LINE PRINTER
MODEL V-132-C

COMPUTER HARDWARE INC.

NOTES:
1. USED WITH PART NUMBER AC-1201.
2. INSTALL THIS DRAWING IN DATA PRINTER CORP. MANUALS FOR MODEL V-132-C LINE PRINTER, VOLUMES I & II AS SHOWN AT THE BOTTOM OF EACH SHEET.
3. MODIFICATIONS TO DATA PRINTER CORP. CIRCUITRY ARE SHOWN BY DASHED LINES.

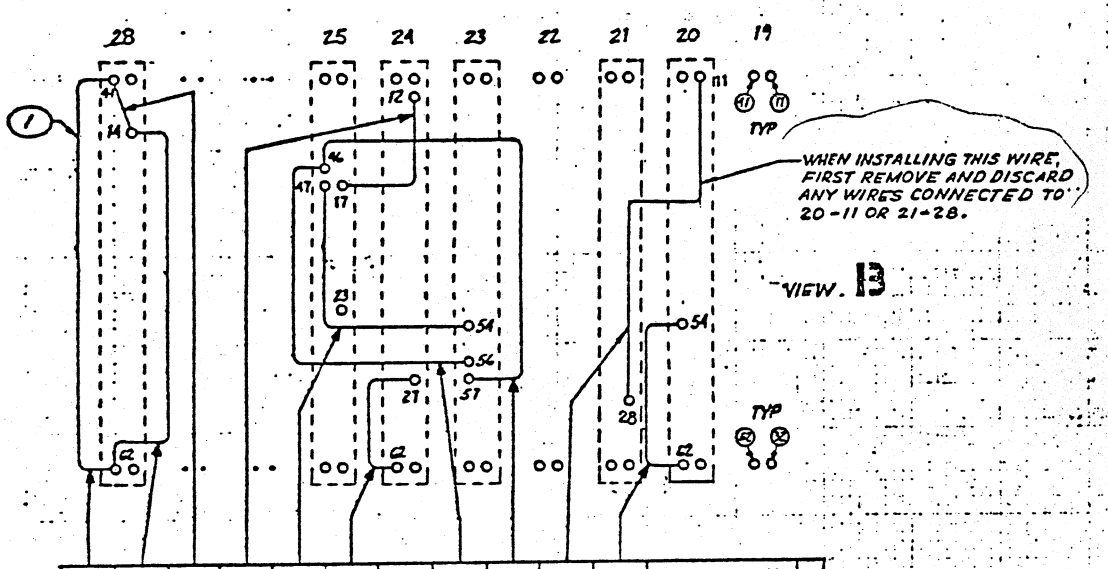
TABLE OF MODIFICATIONS (X = REQUIRED)

AC-1201-1 (NATIVE USE)	AC-1201-3 (1403 USE)	AC-1201-5 (1443 USE)	VOLUME II PAGE	FIGURE	MODIFICATION
X		X	71	1.1.2	PIN 28-14 (PAPERFEED), GROUNDED
X	X	X	71	1.1.2	PIN 28-41 (AUTOLINEFEED), GROUNDED
X	X	X	74	2.1.2	PIN 24-27 (DOUBLE SPACE), GROUNDED
	X	X	74	2.1.2	PIN 24-12 (LINE STROBE) WIRED TO PIN 25-17 (DRIVER INPUT, FIG. 4.1.2)
X	X	X	80	4.1.1	CR08, CR09, R19 (BLANK LINE SUPPRESS) ADDED TO PC BOARD 2604 (COMPARE OUTPUT)
X	X	X	81	4.1.2	CR10 (POWER-OFF PULL DOWN) ADDED TO PC BOARD 2604 (COMPARE OUTPUT); INPUT PINS 25-17 (LINE STROBE), 25-46 (VFU CH 1/9), 25-47 (VFU CH12) ADDED
X	X	X	81	4.1.2	PIN J201-6 WIRED TO PIN 25-23; PIN J201-19 GROUNDED
X		X	83	5.1.1	PIN 23-56 (VFU CH1) WIRED TO PIN 25-46 (DRIVER INPUT, FIG. 4.1.1)
X	X	X	84	5.1.2	PIN 23-54 (VFU CH12) WIRED TO PIN 25-47 (DRIVER INPUT, FIG. 4.1.1)
	X	X	84	5.1.2	PIN 23-57 (VFU CH9) WIRED TO PIN 25-46 (DRIVER INPUT, FIG. 4.1.1)
	X		86 OR 120	6.1.1	I/O MODE JUMPER IN STANDARD MODE POSITION ON PC BOARD 2608 OR 2622 (MEMORY CONTROL)
X		X	86 OR 120	6.1.1	I/O MODE JUMPER IN FIRST CHARACTER MODE POSITION ON PC BOARD 2608 OR 2622 (MEMORY CONTROL)
	X	X	88	6.1.3	PIN 20-54 (CLEAR) GROUNDED

ATTACH DWG TO VOL. II, INSIDE FRONT COVER.

TYPE-SIZE	DWG. NO.	REV. LET.
SA	1202	C

WIRING SIDE OF CARD BAY MOTHERBOARD



VIEW B

○	○			○	○		○		○	✓	-1 ASSEMBLY (STANDARD)
○			○	○	○			○	○	○	-3 ASSEMBLY (1403)
●	●		✓	○	✓		●	✓	●	●	-5 ASSEMBLY (1443)
✓	✓	✓	✓	✓	✓		✓	✓		✓	
AUTO LINE FEED	PAPER FEED CMD		LINE STB.	VFU CH12	DOUBLE SPACE		VFU CH1	VFU CH9	LOAD DATA	CLEAR	LINE BEING CONNECTED
1	2	3	4	5	6	7	8	9	10	11	JUMPER NO.

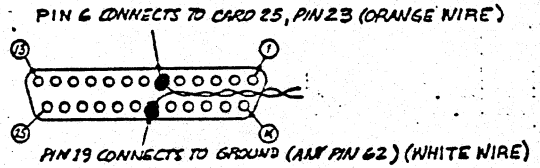
JUMPER TABLE

NOTES:

1. THIS DRAWING USED IN CONJUNCTION WITH SCHEMATIC DRAWING SA-1202 AND DATA PRINTER CORP. MANUAL, "MODEL V-132-C LINE PRINTER VOL II, PARTS BREAKDOWN & ELECTRICAL DIAGRAMS" .(9-6) MEANS (FIGURE NUMBER - INDEX NUMBER).
2. IN EXISTING WIRING ONLY, A WIRE IS CONSIDERED TO BE GROUNDED IF IT CONNECTS TO A PIN THAT IS, IN TURN, WIRED TO A PIN 62 (GROUND). TO REWORK SUCH INDIRECT WIRING, RECORD POSITIONS OF ALL WIRES, REMOVE WIRES AND REWIRE PER VIEW B. CONNECT ANY OTHER WIRING INVOLVED DIRECTLY TO A PIN 62.

(3) USE EXISTING JUMPER UNLESS IN POOR CONDITION. REPLACE WITH ITEM 1.

(4) STRIP ITEM 1 .12 INCH AND SOLDER TO FULL LENGTH OF IC LEAD.



WIRING SIDE OF J201

VIEW A

ELECTRICAL MODIFICATION PROCEDURE

1. COMPARE WIRING OF J201 (LOCATED AT BASE OF WIRING SIDE OF ELECTRONICS BAY, 9-2) WITH DETAIL A. (SEE NOTE 2 FOR OLDER EQUIPMENT.) IF NOT IN CONFORMANCE RELOCATE J201 WIRES TO CARD 25 PINS.
2. CONFIGURE ELECTRONICS BAY PER JUMPER TABLE IN VIEW B. CIRCLE "○" MEANS THAT NEW JUMPER MUST BE ADDED IF NOT PRESENT. ABSENCE OF CIRCLE "○" MEANS JUMPER MUST BE REMOVED IF PRESENT. USE OHMMETER ON X 10 SCALE TO DETERMINE STATUS OF JUMPERS. IF THE PIN 62 (GROUND PIN) INDICATED IS FILLED, USE THE NEAREST PIN 62 HAVING ROOM. USE WIRE COLOR TO CONTRAST WITH ORIGINAL WIRING. LEAVE ENOUGH SLACK IN WIRING TO ALLOW WIRING TO EXTEND BEYOND ENDS OF WIRE-WRAP PINS DURING INSPECTION. DO NOT DRESS NEW WIRING AGAINST EXISTING WIRING. (SEE NOTE 2 FOR OLDER EQUIPMENT.)
3. MODIFY CARDS IN ELECTRONICS BAY LOCATIONS 20 AND 25 PER VIEWS C,D,E,F, AND G. NOTIFY ENGINEERING IF CARD TYPE DOES NOT CORRESPOND TO ANY DRAWING.
4. RECORD WORK (MARK IN APPLICABLE CIRCLES) ON SCHEMATIC DRAWING (ITEM 4) INSTALL IN PRINTER MANUALS (SEE DRAWING FOR LOCATIONS). POSITION SHEETS AGAINST SPINE OF MANUAL, TRIM OFF ANY EXCESS LENGTH PROTRUDING OUT OF THE MANUAL AND STAPLE IN TWO PLACES AT TOP OF SHEET. WHEN STAPLING TO COVER, ENDS OF STAPLES MUST BE ON INSIDE.

AR	AR	AR	211548	GROMMET STRIP NYTRIM .12	CSG-13	WECKESSER CO.	5
1	1	1	212102	DWG SCHEMATIC SA-1202	—	CHI	4
3	3	3	211219	DIODE	FH-1100	FAIRCHILD	3
1	1	1	210050	RES 4.7K 1/4W 5%	11470142	GPL	2
AR	AR	AR	211493	WIRE 30 AWG KYNAR INSUL.	DD-1002-59	CHI	1
-5	-3	-1	PART OR FILE NUMBER	NOMENCLATURE	MFG PART NO OR MATERIAL	MFG NAME OR SPECIFICATION	ITEM NO
QTY REQD			LIST OF MATERIALS				

FILE NUMBER	
-1	211882
-3	211883
-5	211884

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LETTER	DRN	CHK	DATE
E	JDF	7.7	7-17-73

CHANGE RECORD NO 1201

UNLESS OTHERWISE SPECIFIED: DIMENSION TOLERANCE, ANGULAR DIMENSION, DECIMAL 2 PLACE, DECIMAL 3 PLACE, FRACTIONAL, BREAK SHARP EDGES MAX INSIDE CORNERS MAX, ALL MACHINE SURFACES √, CHAMFER ALL THREADS (FULL THREAD (INTO BEST)), DO NOT SCALE THIS PRINT

TITLE: INITIAL MODIFICATION KIT — DA-1256 PRINTER

COMPUTER HARDWARE INC

DRAWN	CHECKED
L WHITEHEAD 10/24/73	10/29/73
DESIGN: L WHITEHEAD	TYPE SIZE: AC
SCALE: NONE	DWG NO: 1201 SHEET 1 OF 5
	REV LET: E

AC 1201

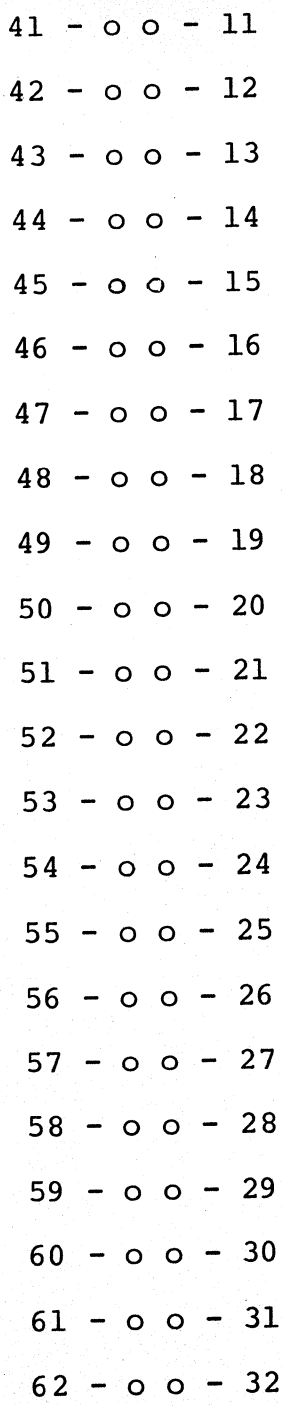


Fig. 5-1 44 PIN P C BOARD EDGE CONNECTOR

[View from Wiring Side (Rear) of Mother Board]

TITLE

1443 COMPATIBLE PRINTER
MODIFICATION KIT
FOR DPC MODEL V-132-C

COMPUTER HARDWARE INC.

SIGNALS FROM CPU	IBM P7 SIGNAL	RETURN	CHI J1/P1 SIGNAL	RETURN	V132C BAY CARD/PIN*	CHAIN
PROCESS BIT 1	D7	D8	B	D	27-45	B - 9
PROCESS BIT 2	D6	D8	A	C	27-11	B - 2
PROCESS BIT 4	B5	D8	F	J	27-41	B - 1
PROCESS BIT 8	D5	D8	E	H	27-42	B - 3
PROCESS BIT A	B4	D8	L	N	27-43	B - 5
PROCESS BIT B	D4	D8	K	M	27-44	B - 7
CARRIAGE CONTROL	B7	D8	R	T	26-46	A - 11
SPACE SUPPRESS	B10	D8	P	S	27-46	B - 11
PROCESS D CYCLE	D12	D8	V	X	26-16	A - 12
TIME 105-000	G4	J8	U	W	26-43	A - 5
TIME 090-000	G12	J8	Z	LB	26-42	A - 3
TIME 060-090	J4	J8	Y	LA	26-15	A - 10
INHIBIT PRINT CLOCK RESET	J12	J8	LD	LF	26-41	A - 1
SIGNALS TO CPU						
PRINT CLOCK CTL TRIGGER	B12	D8	LC	LE	26-30	A - 40
RESET SCM	J11	J8	LJ	LM	26-57	A - 33
CARRIAGE CHAN 1	J9	J8	LN	LR	26-52	A - 23
CARRIAGE CHAN 9	J7	J8	LP	LS	26-20	A - 20
CARRIAGE CHAN 12	G7	J8	LH	LK	26-45	A - 9
PROCESS RELEASE	G9	J8	LU	LW	26-60	A - 39
CARRIAGE BUSY	J6	J8	LT	LV	26-17	A - 14
PRINT READY	J10	J8	LY	AA	26-27	A - 34
CABLE SHIELD	NO CONNECTION		FF,HH		FRAME GND	

*SIGNALS ONLY SHOWN; ALL RETURNS JOINED AT P1 AND CONNECTED TO MOTHERBOARD GROUND.

TYPE-SIZE	DWG. NO.	REV. LET.
SA	1235 SHEET 1 OF 2	NC1

FIGURE 6A

TITLE

1443 COMPATIBLE PRINTER
MODIFICATION KIT
FOR DPC MODEL V-132-C

COMPUTER HARDWARE INC.

INTERCARD SIGNALS *	FROM CARD/PIN	TO CARD/PIN
PRINTER READY	25-30	26-51
RUN	25-29	26-53
XEQ CARRIAGE IMM	26-59	27-52
SEND CAR CTL	26-56	27-51
LOAD CAR DLYD	26-50	27-30
SET SINGLE SPACE	26-47	27-55
PRINT COMMAND	26-48	28-13
SEND DATA	25-32	26-54
BUS 1	27-21	28-20
BUS 2	27-26	28-19
BUS 3	27-23	28-56
BUS 4	27-29	28-55
BUS 5	27-17	28-23
BUS 6	27-16	28-22
BUS 7	27-28	28-28
DATA STROBE	26-49	28-42
DATA BIT A	27-53	26-55
VFU CH 1	23-56	26-11
VFU CH 9	23-57	26-12
VFU CH 12	23-54	26-13
CH 1	26-44	27-47
LINE STROBE	23-24	26-14
GROUND JUMPER	26-62	26-58
-12 VDC (26 AWG)	18-28	26-32

*FOR CONTINUATION OF RUN WITHIN PRINTER LOGIC, SEE MANUAL:
"DATA PRINTER CORP. MODEL V-132-C LINE PRINTER, VOL. II".

TYPE-SIZE	DWG. NO.	REV. LET.
SA	1235 SHEET 2 OF 2	NC 1

FIGURE 6B

TITLE

INITIAL MODIFICATION KIT
DATA PRINTER CORP LINE PRINTER
MODEL V-132-C

COMPUTER HARDWARE INC.

NOTES:
1. USED WITH PART NUMBER AC-1201.
2. INSTALL THIS DRAWING IN DATA PRINTER CORP. MANUALS FOR MODEL V-132-C LINE PRINTER, VOLUMES I & II AS SHOWN AT THE BOTTOM OF EACH SHEET.
3. MODIFICATIONS TO DATA PRINTER CORP. CIRCUITRY ARE SHOWN BY DASHED LINES.

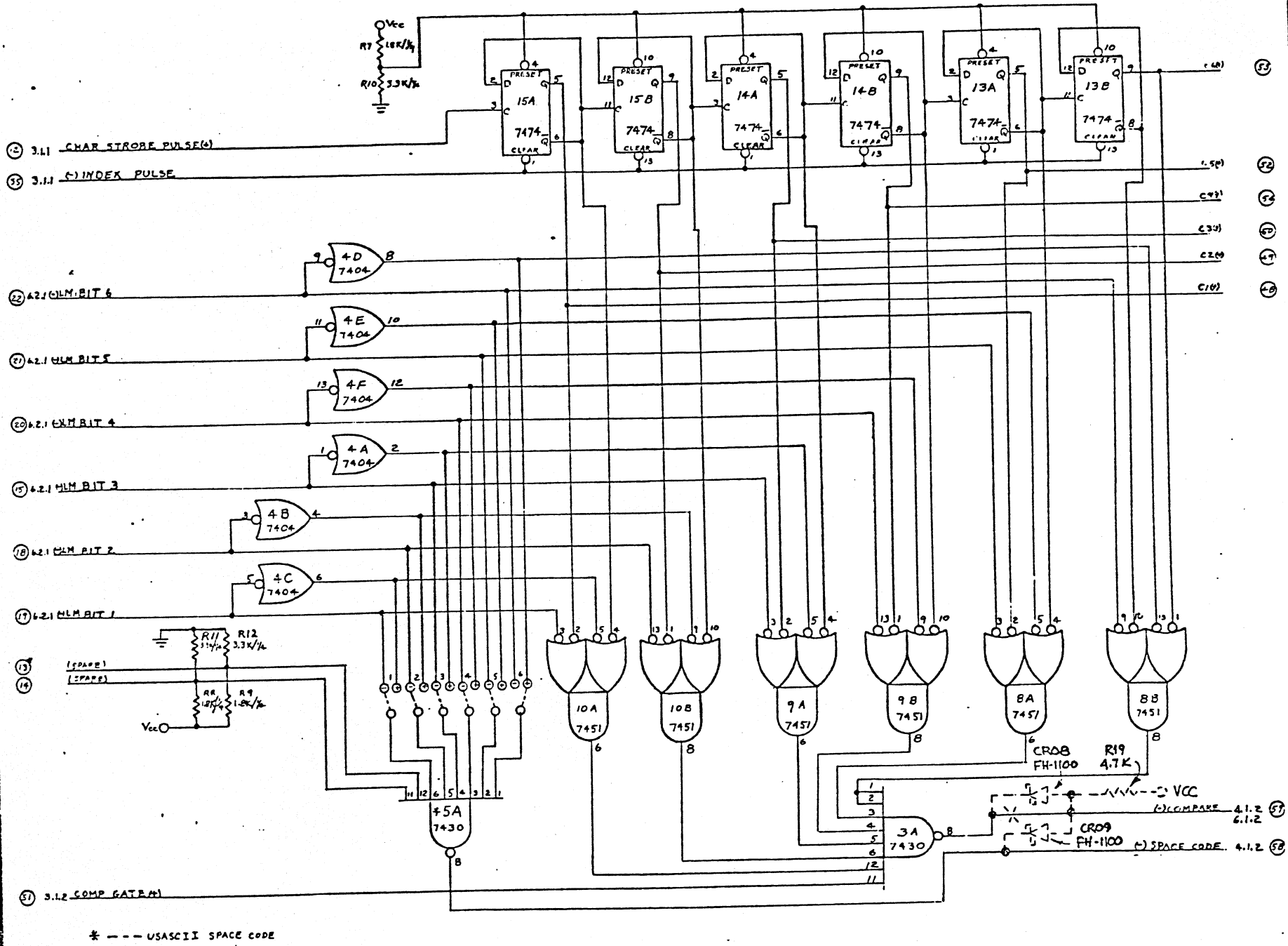
TABLE OF MODIFICATIONS (X = REQUIRED)

AC-1201-1 (NATIVE USE)	AC-1201-3 (1403 USE)	AC-1201-5 (1443 USE)	VOLUME II PAGE	FIGURE	MODIFICATION
X		X	71	1.1.2	PIN 28-14 (PAPERFEED), GROUNDED
X	X	X	71	1.1.2	PIN 28-41 (AUTOLINEFEED), GROUNDED
X	X	X	74	2.1.2	PIN 24-27 (DOUBLE SPACE), GROUNDED
	X		74	2.1.2	PIN 24-12 (LINE STROBE) WIRED TO PIN 25-17 (DRIVER INPUT, FIG. 4.1.2)
X	X	X	80	4.1.1	CR08, CR09, R19 (BLANK LINE SUPPRESS) ADDED TO PC BOARD 2604 (COMPARE OUTPUT)
X	X	X	81	4.1.2	CR10 (POWER-OFF PULL DOWN) ADDED TO PC BOARD 2604 (COMPARE OUTPUT); INPUT PINS 25-17 (LINE STROBE), 25-46 (VFU CH 1/9), 25-47 (VFU CH12) ADDED
X	X	X	81	4.1.2	PIN J201-6 WIRED TO PIN 25-23; PIN J201-19 GROUNDED
X		X	83	5.1.1	PIN 23-56 (VFU CH1) WIRED TO PIN 25-46 (DRIVER INPUT, FIG. 4.1.1)
	X		84	5.1.2	PIN 23-54 (VFU CH12) WIRED TO PIN 25-47 (DRIVER INPUT, FIG. 4.1.1)
	X		84	5.1.2	PIN 23-57 (VFU CH9) WIRED TO PIN 25-46 (DRIVER INPUT, FIG. 4.1.1)
	X		86 OR 120	6.1.1	I/O MODE JUMPER IN STANDARD MODE POSITION ON PC BOARD 2608 OR 2622 (MEMORY CONTROL)
X		X	86 OR 120	6.1.1	I/O MODE JUMPER IN FIRST CHARACTER MODE POSITION ON PC BOARD 2608 OR 2622 (MEMORY CONTROL)
	X	X	88	6.1.3	PIN 20-54 (CLEAR) GROUNDED

ATTACH DWG TO VOL. II, INSIDE FRONT COVER.

TYPE-SIZE	DWG. NO.	REV. LET.
SA	1202 SHEET 1 OF 4	C

ATTACH DWG TO DPC MANUAL VOL. II, FIGURE 4.1.1.



MODIFIED DATA PRINTER CORP SCHEMATIC C-2108

DATA PRINTER CORP LINE PRINTER
MODEL V-132-C

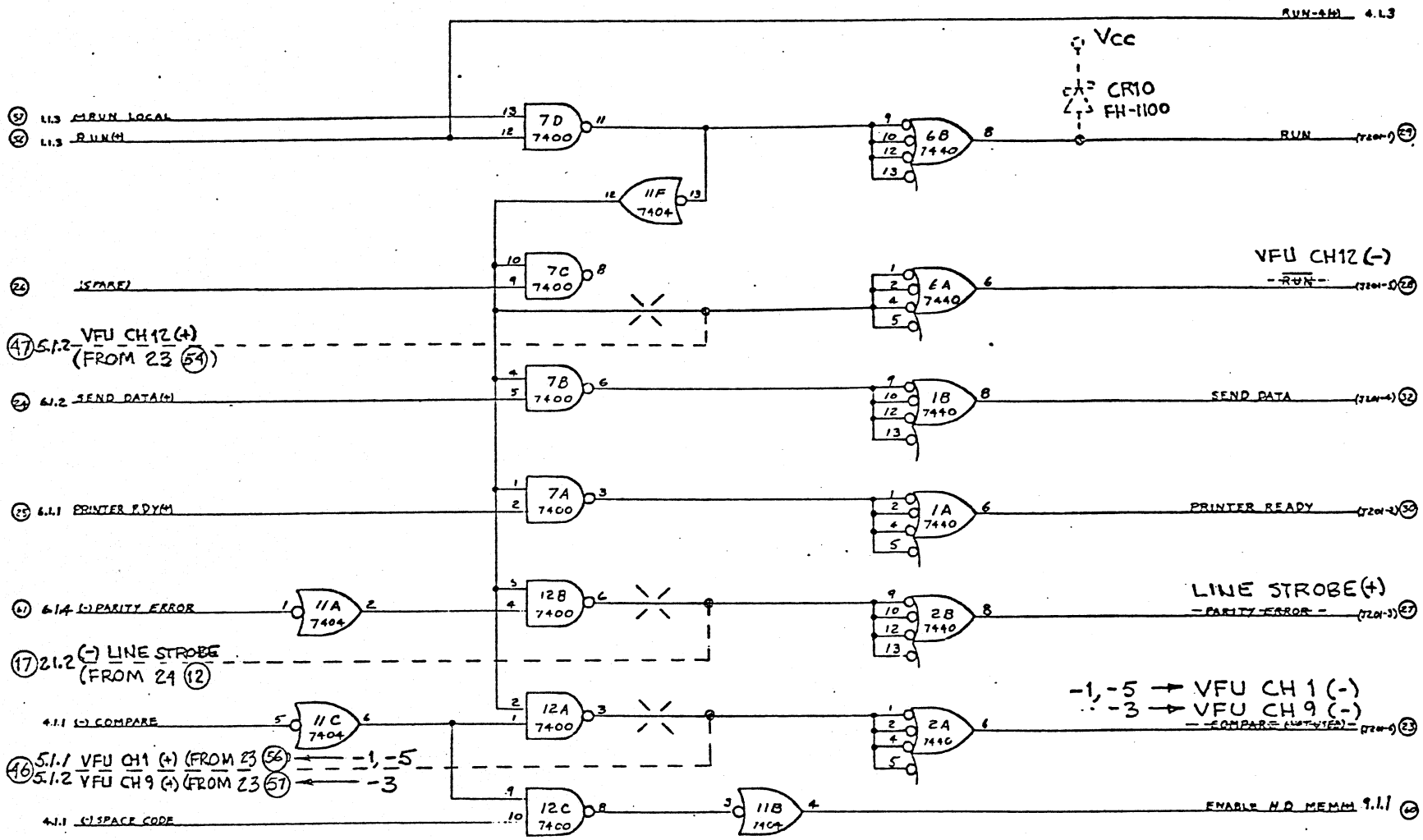
COMPUTER TRANSCEIVERS INC.

TYPE-SIZE	DWG. NO.	REV. LET.
SA	1202 SHEET 2 OF 4	C

ATTACH DWG TO DPC MANUAL VOL. II, FIGURE 4.1.2.

DATA PRINTER CORP LINE PRINTER
MODEL V-132-C

COMPUTER HARDWARE INC.



MODIFIED DATA PRINTER CORP SCHEMATIC C-2108

TYPE-SIZE	DWG. NO.	REV. LET.
SA	1202	C
	SHEET 3 OF 4	

MODIFIED DATA PRINTER CORP FIG. 5.2.7

P201		P202	
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Run	1	Not Used
14	Return	14	
2	Printer Ready	3	Paperfeed Command
15	Return	16	Return
4	Send Data	4	Print Command
17	Return	17	Return
10	Not Used	5	Data Strobe
23		18	Return
12	Paper Low	6	Bus 1
25	Return	19	Return
5	VFU Ch 12	7	Bus 2
18	Return	20	Return
3	Line Strobe	8	Bus 3
16	Return	21	Return
9	Clear	9	Bus 4
22	Return	22	Return
2	Not Used	10	Bus 5
15		23	Return
20	Line Strobe	11	Bus 6
7	Return	24	Return
21	Not Used	12	Bus 7
8		25	Return
24	Not Used		
11			
19	Return		
6	VFU Ch 1 or VFU Ch 9		