CHROMATICS

CGC 7900
Color Graphics Computer

Preliminary OEM Manual
February, 1981

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CGC 7900 COLOR GRAPHICS COMPUTER SYSTEM

PRELIMINARY OEM MANUAL
February, 1981

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TABLE OF CONTENTS

OEM MANUAL - INTRODUCTION	1
CGC 7900 HARDWARE OVERVIEW	2
CPU CARD	3
EPROM/RASTER PROCESSOR CARD	4
BUFFER MEMORY CARDS	5
IMAGE MEMORY CARDS	5
CGC 7900 SYSTEM MEMORY MAP	7
CGC 7900 MEMORY MAP	9
EPROM	10
IMAGE MEMORY	11
PLANE MODE	12
Z MODE	13
COLOR STATUS MODE	15
COLOR LOOKUP TABLE	17
COLOR LOOKUP TABLE ADDRESSES	18
OVERLAY MEMORY ADDRESSING	19
OVERLAY CHARACTER CELL ADDRESSES	21
HARDWARE LATCHES AND CMOS/STATIC RAM	23
BITMAP ROLL COUNTER	24
X PAN	25
Y PAN	26
X AND Y ZOOM	27
BLINK SELECT	28
PLANE SELECT	29
PLANE VIDEO SWITCH	30
COLOR STATUS FOREGROUND/BACKGROUND	31
OVERLAY ROLL COUNTER	32
IMAGE SELECT	33
OVERLAY CURSOR BLINK	33
OVERLAY CHARACTER BLINK	33
I/O MAP	35
SERIAL PORTS	36
SERIAL PORT PINOUTS	37
INTERFACING RS-232 AND RS-449	38
BAUD RATE GENERATOR	39
JOYSTICK	40
BEZEL SWITCHES	42
INTERRUPT MASK	43
BUS INTERRUPTS (BINT)	44
BUS CHIP SELECTS	45
BCS1 ADDRESSES	46
LIGHT PEN	46
SYNC ADDRESSES	47
BUFFER MEMORY PARITY	48

DISK PORT 49
DISK PORT PINOUT 51

REAL TIME CLOCK 53

PROGRAMMABLE SOUND GENERATOR 56
PROGRAMMING THE PSG 57
PSG REGISTERS 58
PSG MUSICAL NOTES 60

KEYBOARD 61
KEYBOARD CABLE PINOUT 63
KEYBOARD DATA BUS 64
KEYBOARD LED SELECT CODES 65
INTERFACING PERIPHERALS TO THE KEYBOARD PORT 66
KEYBOARD TIMING 67

CGC 7900 SYSTEM BUS 69
P1 CONNECTOR IDENTIFICATION 70
P1 SIGNAL DESCRIPTIONS 72
P2 CONNECTOR IDENTIFICATION 75
P2 SIGNAL DESCRIPTIONS 77

SYNC SIGNALS 81
HORIZONTAL TIMING 83
VERTICAL TIMING 84

CONFIGURING BUFFER MEMORY CARDS 85
BUFFER MEMORY CARD ADDRESS SELECTION 86
CONFIGURING IMAGE MEMORY PLANES 87
IMAGE MEMORY CONFIGURATION JUMPERS 91

OEM MANUAL - INTRODUCTION

This manual is intended to provide information to the OEM customers of Chromatics, Incorporated, concerning the internal details of the CGC 7900 Color Graphics Computer System. The information contained in this manual should be considered proprietary in nature. It is provided solely to aid our OEM customers in interfacing to the end-user.

This manual should be used in conjunction with the CGC 7900 Operator's Manual. The Operator's Manual gives more detailed information about the 7900 system software.

While the information in this document is believed to be accurate, no guarantees are made. Chromatics reserves the right to make product changes at any time.

CGC 7900 HARDWARE OVERVIEW

The CGC 7900 is a self-contained computer system. It is capable of extremely high-resolution color graphics displays. The 7900 Central Processing Unit (CPU) uses the MC68000 microprocessor. The system may be equipped with a hard disk and two floppy disks, a light pen, joystick, and several Megabytes of memory for images and programs.

The chassis contains a motherboard with 12 or 24 card connectors. The lower portion of the chassis houses the digital electronics, and the upper portion contains the analog circuitry. Power supplies and the hard disk drive are mounted in the bottom of the chassis. Six fans mounted below the card cage ventilate the chassis. The system is mounted on casters for easy transportation.

The analog chassis contains a high-resolution, 19-inch color Cathode Ray Tube (CRT). The CRT is treated with a long persistance phosphor, to minimize the problem of interlace flicker. All high voltages are present only in the analog chassis.

CPU CARD

The CGC 7900 Central Processing Unit (CPU) card contains the MC68000 microprocessor, which can directly address 16 Megabytes of memory. This card generates most of the control signals used by the processor to control memory.

The CPU card contains 4K bytes of static memory. This may optionally be replaced by CMOS memory, powered by a battery backup supply on this card. The CMOS option includes a Real-Time Clock, also located on the CPU card.

All input/output interface hardware in the standard 7900 system is found on the CPU card. This includes the keyboard, joystick, disk, bezel keys, and two serial ports. I/O is connected to the CPU card by edge connectors on the back of the card. Each of the I/O interfaces is discussed in a separate section of this manual.

A Programmable Sound Generator is installed on the CPU card. It may be operated by the CGC system programs or by user programs. It connects to a speaker, below the keyboard, on the chassis front. A Quiet Lock key on the keyboard disables the speaker.

EPROM/RASTER PROCESSOR CARD

EPROM sockets on this card are addressed from 800000 to 80FFFF. The EPROMs must be 2532 type (32K bits), 350 nanoseconds or faster. See the "Memory Map" section of this manual for programming requirements.

The Raster Processor is a bipolar circuit, microprogrammed to perform an address translation function in the 7900 system. This device assists the MC68000 in moving pixels on the image memory screen.

This card also contains bus terminators which decrease noise on the motherboard. Because of the extremely high processor speeds (up to 8 MHz), these terminators are very important in the 7900 system.

BUFFER MEMORY CARDS

The 7900 contains one or more Buffer Memory cards. Each card holds 128K bytes of dynamic RAM for system memory requirements and user programs. The first card is addressed at zero, and other cards are usually addressed on 128K boundaries above zero.

Each card stores a parity bit for each byte of data stored. Parity is stored with each write, and checked with each read. If a parity error is detected the card will assert a low level on the parity error line of the bus. If the parity flip-flop is enabled, this will interrupt the 68000 processor. Systems which use the parity checking feature must write data to ALL buffer memory when the system is powered-up, or risk a parity error if a location is read that was not previously written.

IMAGE MEMORY CARDS

Up to 16 Image Memory cards, or planes, may be installed in the 7900. The number of planes determines how many simultaneous colors may be displayed in the high-resolution Bitmap memory. Typical systems will contain 1, 4, 8 or 16 Image planes.

Each plane may be accessed through several addressing modes. These are discussed under "Image Memory" in the Memory Map section of this manual. Because of the varied addressing modes, a plane might respond to addresses anywhere between A00000 and E1FFFF.

CGC 7900 SYSTEM MEMORY MAP

	000000	200000	400000	600000	800000	A00000	C00000	E00000
000000	Buffer Memory Card 0				EPROM	Z	Image Plane 0	Color Status Map
020000	Buffer Memory Card 1						Image Plane 1	Misc
040000	. .					Mode	Image Plane 2	
060000							. .	
080000						Screen	. .	
0A0000							. .	
0C0000						Memory	. .	
0E0000							Image Plane 7	
100000							Image Plane 8	
120000							. .	
140000			One Block = 128K				. .	
160000							. .	
180000							. .	
1A0000							. .	
1C0000							. .	
1E0000							Image Plane 15	I/O

CGC 7900 MEMORY MAP

The processor in the CGC 7900 is capable of directly addressing over 16 Megabytes of memory, using a 24-bit address bus. The addressing range is 000000 to FFFFFF (hex). Chromatics reserves the upper half of this space, beginning at 800000 (hex).

The lower half of the 7900 address space will normally contain one or more Buffer Memory cards. Each card contains 128K bytes of dynamic RAM. The first card must be located at address 000000-1FFFFF (the first 128K of memory) to provide the processor with room for interrupt vectors. The remainder of this card, plus any other Buffer Memory cards which may be installed, is allocated among various system functions, and user programs.

The "Thaw" command allocates memory among input/output buffers, stacks, the Create Buffer, function key buffers, etc. If battery-powered CMOS RAM (optional) is installed in your system, the parameters set up by "Thaw" will be remembered and used to allocate memory next time the system is powered up. If CMOS RAM is not present, memory will be allocated according to default parameters in PROM.

EPROM

System EPROM begins at address 800000. The Raster Processor card contains EPROM for the standard system. Space is provided for 32K words (64K bytes), addressed from 800000 to 80FFFF. The card will accomodate Motorola 2532-C35 EPROMs (or equivalent) which have access times of 350 nanoseconds or faster.

2532 EPROMs are capable of storing 32K bits of data, arranged as 4K of 8-bit bytes. Since the 68000 fetches all instructions as 16-bit words, two 2532s must be accessed simultaneously for each instruction fetch. This requires that data in the 2532s be separated into "odd" bytes and "even" bytes. Each 4K of words in EPROM thus requires two 2532s, one containing all the "odd" numbered bytes in the program, and one containing all the "even" numbered bytes. A total of 16 2532s may be inserted in the sockets provided on the Raster Processor card.

A special mapping is provided for convenience during processor startup. When external Reset is applied, the 68000 fetches its stack pointer and program counter as two 32-bit words, from addresses 000000 and 000004, respectively. The EPROM circuitry maps addresses 800000 and 800004 into this space. Thus, the first two long words in EPROM should contain the initial values of stack pointer and program counter.

store stack pointer

store program counter

IMAGE MEMORY

Image memory on the CGC 7900 consists of from one to sixteen Refresh Memory cards. Each Refresh Memory card, or plane, contains 128K bytes of dynamic RAM. The bits on these planes are manipulated by software to produce high-resolution Bitmap images. Then, the information in the planes is brought out through the image control logic and the Color Lookup Table, to produce an image on the screen.

All areas of the memory map designated as image memory are protected against Bus Errors. Regardless of the number of planes installed in the image memory of a 7900 system, it is impossible to receive a Bus Error from image memory accesses.

The CGC 7900 provides several ways to address image memory. Each of these methods is discussed in turn.

PLANE MODE

In Plane mode, each plane of image memory is accessed as an independent 128K chunk of memory. Writing a byte, word, or long word into the image memory in Plane mode will write only into that plane. Plane mode addressing is equivalent to the way memory is addressed in most computer systems, and is the same way that Buffer Memory is addressed in the 7900.

Plane mode addressing begins at address C00000 and ends at DFFFFF (hex). Each plane occupies 128K bytes. The planes are numbered from 0 to 15, although many systems will not have all planes installed. In particular, most systems will be configured in one of the following ways:

Total Planes In System	Plane Numbers Assigned
1	0
4	0,1,2,7
8	0 thru 7
16	0 thru 15

Plane 7 is normally assigned for use as the "blink" plane, so it is important that a plane 7 exist in all but the most basic systems.

Z MODE

Z mode is one of the two special modes provided for accessing image memory planes.

Consider the image memory to be arranged as a set of 16 planes, one in front of another. Each plane contains 1024 x 1024 bits, or 128K bytes. Each pixel on the screen is represented by a single bit from each of the 16 planes. Z mode allows the processor to write a 16-bit word to memory, and have each bit fall into the corresponding location of its plane.

For example, consider an instruction to write the first pixel in image memory (the upper left corner of the screen):

```
MOVE.W    #PixelData, ZScreenStart
```

Bit 0 of "PixelData" will be moved into the first bit of image plane 0. Bit 1 will be moved into the first bit of image plane 1, and so on. The Z mode hardware allows writing to individual bits, without the problem of modifying adjacent bits in each plane.

Z mode addressing occupies a full 2 Megabytes of the address space. It begins at address A00000 and ends at BFFFFF. Note that since only 768 lines of the image memory are visible at a time, the pixel addressed at BFFFFF is not normally visible. The last visible pixel of image memory is addressed at B7FFFF (assuming pan and zoom are not in effect).

In Z mode, no assumptions are made concerning the number of planes in a system. If a plane does not exist, any bits which should be written into that plane are simply thrown away. When reading back data in Z mode, any bits which should come from non-existant planes will be returned as logical highs, or ones. 1

Z mode access to individual planes is restricted by Plane Select. Plane Select is a 16-bit latch, located at address E40012. If a bit of this latch is a one, the corresponding plane is enabled. If a bit is zero, the plane is disabled. Disabled planes may not be written into using Z mode, and reading from them in Z mode will return a zero in the bit positions of the disabled planes. In this way, non-existant

planes may be masked using Plane Select so that bits returned from them will be zeros.

COLOR STATUS MODE

Color Status mode provides a very fast way to write color information into the image memory planes. Color Status occupies 128K bytes, the same area one image plane occupies in Plane mode. Color Status mode is mapped from E00000 to E1FFFF. This is a "write-only" area of memory. Attempts to read from this area will be greeted with bytes of all FFs.

Before using Color Status mode, it is necessary to load the Color Status Foreground and Background latches. Each of these contains a 16-bit number. Color Status Foreground is located at E40016, and Color Status Background is at E40018. Each of these should be loaded with the 16-bit quantity you would write into image memory if you were using Z mode addressing. For example, if the foreground of the pattern you are writing requires color number 5, you would load the Color Status Foreground latch with 5. Similarly, Color Status Background might be loaded with color number 0. (These numbers refer to entries in the Color Lookup Table.)

After loading the latches, you may write to the Color Status area of memory. Each bit you write will affect a single pixel of the image, one bit in each of the 16 image planes. If you write a bit which is a 1, the pixel will be written in foreground color, as defined by the Color Status Foreground latch. If a bit is 0, the pixel will be written in background color, defined by Color Status Background.

For example: to make the first 32 pixels of the screen white, we might execute the following code.

```
ForeG   EQU     $E40016     Foreground latch
BackG   EQU     $E40018     Background latch
ColStat EQU     $E00000     Color Status mode starts here

        MOVE.W  #7,ForeG    set up FG Color Status
                            (assume color 7 = white)

WRITE   MOVE.L  #$FFFFFFFF,ColStat   write 32 bits of ones
```

The single instruction at label WRITE modifies the color of 32 pixels. The same operation would require 32 writes in Z mode, or 16 writes in Plane mode (to write all 16 planes).

The following example will write an alternating series of 32 red and green pixels into the first 32 pixels of the screen.

```
MOVE.W  #4,ForeG        make foreground color = 4
MOVE.W  #2,BackG        make background color = 2
                        (assume 4 = red, 2 = green)

MOVE.L  #$AAAAAAAA,ColStat   write alternating bits
```

1010101010

Color Status mode allows writing bytes, words, or long words, to modify 8, 16, or 32 pixels, respectively.

The image memory planes are grouped into two sets of 8 planes each. Each of these two sets may contain an image, and Plane Select is normally used to decide which of the two is written into when a 16-bit Z mode write is performed. When writing with Color Status, it may be useful to write both images with the same color (otherwise one image would be written with zeros). To prevent this problem from occurring, always load the Color Status latches with the same number in the upper and lower bytes. Following this rule, our first example above must be corrected to contain the statement

```
MOVE.W  #$0707,ForeG     set up FG Color Status
                         (assume color 7 = white)
```

(Copying the lower byte into the upper byte of the latch information.)

COLOR LOOKUP TABLE

The Color Lookup Table consists of 256 locations, each of which holds a 24-bit number. Eight of these bits determine the red component of a color, eight for green, and eight for blue. A pixel in the Bitmap (image memory) is given a color by summing the bits in whichever set of 8 planes is being viewed (weighted binary sum), and the resulting value points to an entry in the Color Lookup Table. The color components in that entry of the Color Lookup Table provide the color of that pixel.

The table is arranged as 256 long words (1K bytes), starting at address E30000. Each long word is organized as follows:

Bits	31-24	23-16	15-8	7-0
	FF	8-bit red	8-bit green	8-bit blue

The high byte (bits 31-24) of each entry are undefined, so they read out as FF hex. The next 8 bits set the red intensity, followed by green and blue.

The Color Lookup Table may be read or written at any time. Values written into the table are not used on the screen until the next vertical retrace, so it is not useful to write a single entry more than once per screen scan (1/60 second with 60 Hz power). Writing to the Color Lookup Table at any time will not cause the display to "glitch."

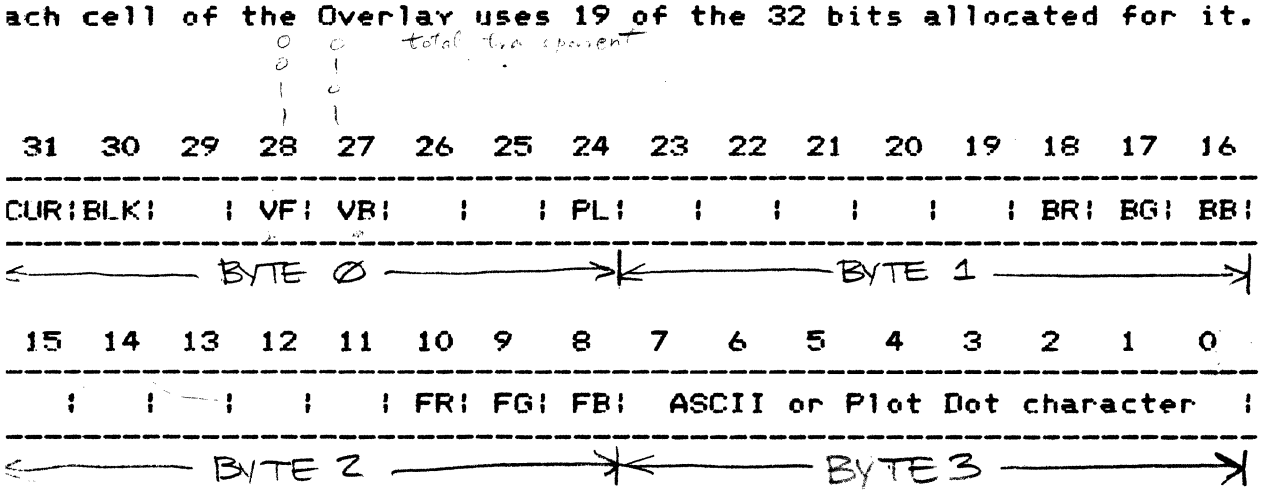
COLOR LOOKUP TABLE ADDRESSES

0 E30000	52 E300D0	104 E301A0	156 E30270	208 E30340
1 E30004	53 E300D4	105 E301A4	157 E30274	209 E30344
2 E30008	54 E300D8	106 E301A8	158 E30278	210 E30348
3 E3000C	55 E300DC	107 E301AC	159 E3027C	211 E3034C
4 E30010	56 E300E0	108 E301B0	160 E30280	212 E30350
5 E30014	57 E300E4	109 E301B4	161 E30284	213 E30354
6 E30018	58 E300E8	110 E301B8	162 E30288	214 E30358
7 E3001C	59 E300EC	111 E301BC	163 E3028C	215 E3035C
8 E30020	60 E300F0	112 E301C0	164 E30290	216 E30360
9 E30024	61 E300F4	113 E301C4	165 E30294	217 E30364
10 E30028	62 E300F8	114 E301C8	166 E30298	218 E30368
11 E3002C	63 E300FC	115 E301CC	167 E3029C	219 E3036C
12 E30030	64 E30100	116 E301D0	168 E302A0	220 E30370
13 E30034	65 E30104	117 E301D4	169 E302A4	221 E30374
14 E30038	66 E30108	118 E301D8	170 E302A8	222 E30378
15 E3003C	67 E3010C	119 E301DC	171 E302AC	223 E3037C
16 E30040	68 E30110	120 E301E0	172 E302B0	224 E30380
17 E30044	69 E30114	121 E301E4	173 E302B4	225 E30384
18 E30048	70 E30118	122 E301E8	174 E302B8	226 E30388
19 E3004C	71 E3011C	123 E301EC	175 E302BC	227 E3038C
20 E30050	72 E30120	124 E301F0	176 E302C0	228 E30390
21 E30054	73 E30124	125 E301F4	177 E302C4	229 E30394
22 E30058	74 E30128	126 E301F8	178 E302C8	230 E30398
23 E3005C	75 E3012C	127 E301FC	179 E302CC	231 E3039C
24 E30060	76 E30130	128 E30200	180 E302D0	232 E303A0
25 E30064	77 E30134	129 E30204	181 E302D4	233 E303A4
26 E30068	78 E30138	130 E30208	182 E302D8	234 E303A8
27 E3006C	79 E3013C	131 E3020C	183 E302DC	235 E303AC
28 E30070	80 E30140	132 E30210	184 E302E0	236 E303B0
29 E30074	81 E30144	133 E30214	185 E302E4	237 E303B4
30 E30078	82 E30148	134 E30218	186 E302E8	238 E303B8
31 E3007C	83 E3014C	135 E3021C	187 E302EC	239 E303BC
32 E30080	84 E30150	136 E30220	188 E302F0	240 E303C0
33 E30084	85 E30154	137 E30224	189 E302F4	241 E303C4
34 E30088	86 E30158	138 E30228	190 E302F8	242 E303C8
35 E3008C	87 E3015C	139 E3022C	191 E302FC	243 E303CC
36 E30090	88 E30160	140 E30230	192 E30300	244 E303D0
37 E30094	89 E30164	141 E30234	193 E30304	245 E303D4
38 E30098	90 E30168	142 E30238	194 E30308	246 E303D8
39 E3009C	91 E3016C	143 E3023C	195 E3030C	247 E303DC
40 E300A0	92 E30170	144 E30240	196 E30310	248 E303E0
41 E300A4	93 E30174	145 E30244	197 E30314	249 E303E4
42 E300A8	94 E30178	146 E30248	198 E30318	250 E303E8
43 E300AC	95 E3017C	147 E3024C	199 E3031C	251 E303EC
44 E300B0	96 E30180	148 E30250	200 E30320	252 E303F0
45 E300B4	97 E30184	149 E30254	201 E30324	253 E303F4
46 E300B8	98 E30188	150 E30258	202 E30328	254 E303F8
47 E300BC	99 E3018C	151 E3025C	203 E3032C	255 E303FC
48 E300C0	100 E30190	152 E30260	204 E30330	
49 E300C4	101 E30194	153 E30264	205 E30334	
50 E300C8	102 E30198	154 E30268	206 E30338	
51 E300CC	103 E3019C	155 E3026C	207 E3033C	
52 E300D0	104 E301A0	156 E30270	208 E30340	

OVERLAY MEMORY ADDRESSING

he Overlay consists of 4080 character cells, arranged 85 per ine and 48 lines. Each cell is addressed as a long word (32 its). The Overlay is mapped from addresses E38000 to E3BFBC.

ach cell of the Overlay uses 19 of the 32 bits allocated for it.

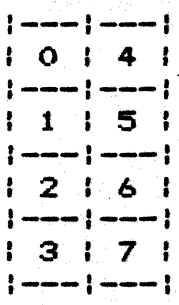


CUR	places a cursor in the cell if SET
BLK	blinks the foreground character in the cell if SET
VF	makes the foreground visible if SET (else transparent)
VB	makes the background visible if SET (else transparent)
PL	uses bits 0-7 as PLOT DOT descriptor if SET (else ASCII)
BR	turns on Red in background if SET
BG	turns on Green in background if SET
BB	turns on Blue in background if SET
FR	turns on Red in foreground if SET
FG	turns on Green in foreground if SET
FB	turns on Blue in background if SET

Bits 0-7 are interpreted in a number of ways:

If PL is CLEAR, implying ASCII characters, bits 0-6 are used to select an ASCII character. If bit 7 is CLEAR, the character will be taken from the standard ASCII character ROM. If bit 7 is SET, the character will be taken from the alternate character set ROM.

If PL is SET, implying Plot Dots, each of the bits 0-7 is used to turn a Plot Dot on or off. The dots in each character cell are arranged as follows:



The Plot Dots above are numbered to correspond with the bits which control them. If a bit is SET, the Plot Dot associated with that bit will be in foreground color, as determined by FR, FG and FB. If a bit is CLEAR, the associated Plot Dot will be in background color, determined by BR, BG and BB.

OVERLAY CHARACTER CELL ADDRESSES

Line No.	First Cell	Last Cell
1	E38000	E38150
2	E38154	E382A4
3	E382A8	E383F8
4	E383FC	E3854C
5	E38550	E386A0
6	E386A4	E387F4
7	E387F8	E38948
8	E3894C	E38A9C
9	E38AA0	E38BF0
10	E38BF4	E38D44
11	E38D48	E38E98
12	E38E9C	E38FEC
13	E38FF0	E39140
14	E39144	E39294
15	E39298	E393E8
16	E393EC	E3953C
17	E39540	E39690
18	E39694	E397E4
19	E397E8	E39938
20	E3993C	E39A8C
21	E39A90	E39BE0
22	E39BE4	E39D34
23	E39D38	E39E88
24	E39E8C	E39FDC
25	E39FE0	E3A130
26	E3A134	E3A284
27	E3A288	E3A3D8
28	E3A3DC	E3A52C
29	E3A530	E3A680
30	E3A684	E3A7D4
31	E3A7D8	E3A928
32	E3A92C	E3AA7C
33	E3AA80	E3ABD0
34	E3ABD4	E3AD24
35	E3AD28	E3AE78
36	E3AE7C	E3AFCC
37	E3AFD0	E3B120
38	E3B124	E3B274
39	E3B278	E3B3C8
40	E3B3CC	E3B51C
41	E3B520	E3B670
42	E3B674	E3B7C4
43	E3B7C8	E3B918
44	E3B91C	E3BA6C
45	E3BA70	E3BBC0
46	E3BBC4	E3BD14
47	E3BD18	E3BE68
48	E3BE6C	E3BFBC

HARDWARE LATCHES AND CMOS/STATIC RAM

he area of memory from E40000 to E40FFF serves several urposes. First, the CPU card contains 4K bytes of memory at hese addresses. This will either be static RAM (2114) or CMOS AM (6514). CMOS is only installed if your system contains the ptional battery backup supply, which allows the CMOS to store nformation while system power is off.

econd, several system features use hardware latches mapped onto he same addresses as RAM. Writing to any of these addresses ill write into both RAM and the latch. Reading from the ddress will not affect the latch, but RAM will respond with the roper information.

f CMOS RAM is installed, the procedure for configuring these atches at power-up is simple: Read the RAM and write the data ack into the same address. This will cause the latches to esume the state they had when the CMOS RAM was last written.

Address	Function
E40000	Bitmap Roll Counter
E40002.....	X Pan
E40004	Y Pan
E40006.....	X and Y Zoom
E40008	Unused (reserved)
E4000A.....	Used
E4000C	By
E4000E.....	Raster Processor
E40010	Blink Select
E40012.....	Plane Select
E40014	Plane Video Switch
E40016.....	Color Status Foreground
E40018	Color Status Background
E4001A.....	Overlay Roll Counter

This area of memory is also the default area for user-defined function keys. Function key definitions are stored in the upper 2K of this memory, so the definitions can be maintained by the battery-backed CMOS RAM (if installed). If the user requires more than 2K for his function key definitions, the function key buffer may be moved with the "Thaw" command.

BITMAP ROLL COUNTER

The Bitmap Roll Counter is a 10-bit latch at address E40000 The value stored in this latch is left-shifted by 10 bits, an added (modulo 2^20) to ANY address in the Z mode of Bitma memory, during any read, write, or screen refresh access to th Bitmap. This latch has the effect of determining which physica set of RAM bits will be accessed by addresses A00000 thru A003F (the top raster line of the Bitmap).

> Since the value in this latch is added during all Z mode accesses to the Bitmap, its function is transparent to the CPU. That is, the CPU can always read and write to A00000 as the first pixel on the Bitmap.

This latch is useful for hardware scrolling the Bitmap. If th current Bitmap character height is N pixels, adding N to th Bitmap Roll Counter will have the effect of moving all pixels o the screen up N raster lines (one character line). Then th software need only erase the bottom line of the Bitmap, and th scrolling is complete. Scrolling down is accomplished b decrementing the Bitmap Roll Counter.

The Bitmap Roll Counter is independent of the Y Pan register although both latches have the ability to cause the Bitmap imag to scroll up and down. Altering the Y Pan register causes given point on the screen to have a different address in memory altering the Bitmap Roll Counter will never change the addres which corresponds to a given screen location (although it wil cause a different RAM chip to be associated with that location) See "Y Pan."

X PAN

he X Pan register is a 10-bit latch at address E40002. The alue in this latch is added (modulo 1024) to the screen refresh ddress counter as each line of the Bitmap is beins displayed on he screen. The X Pan register has the effect of determinins here the left edse of the imase (the vertical column of pixels elow the pixel at A00000) will appear on the screen.

> NOTE: The lowest 2 bits of the X Pan register are NOT sisnificant. X Pan will only allow the imase to be moved in increments of 4 pixels. You must increment or decrement the X Pan register by at least 4, in order to alter the screen display.

t is desirable to sync Pan to vertical retrace, so that lterins the Pan registers (X Pan and Y Pan) will not cause tearins" of the imase.

Y PAN

The Y Pan register is a 10-bit latch at address E40004. The value in this latch is left-shifted by 10 bits, and added (modulo 2^20) to the screen refresh address counter as each line of the Bitmap is being displayed on the screen. The Y Pan register has the effect of determining where the top edge of the image (the horizontal row of pixels addressed from A00000 to A003FF) will appear on the screen.

All 10 bits of the Y Pan register are significant. Since the lowest two bits of the X Pan register are NOT significant, diagonal pan may be accomplished by incrementing both X Pan and Y Pan in steps of 4.

The Y Pan register has an especially important use. Recall that the screen only displays 768 lines, but there are actually 1024 lines of pixels in the Bitmap memory. Incrementing the Y Pan register allows the remaining 256 lines to become visible.

X AND Y ZOOM

he X and Y Zoom registers are addressable together by 16-bit ord operations, or individually by 8-bit byte operations. X oom is a 4-bit register at E40006, and Y Zoom is a 4-bit egister at E40007.

he CGC 7900 performs zoom by pixel magnification. With no oom, the X and Y Zoom registers are both zero, and each pixel n memory is refreshed to the screen only once. This provides he default conditions of 1024 pixels per horizontal line, and 68 lines visible. If each pixel in memory was brought out to he screen twice, there would be room for only 512 of them on ach screen line; this corresponds to an X Zoom factor of two, nd occurs when the X Zoom register contains the value 1.

f each line of pixels is brought out to the screen twice, each dot" placed on the screen would be twice as tall as before. here would then be room for only 384 lines of information, with ach line twice its previous height. This corresponds to a Y oom factor of two, and occurs when the Y Zoom register contains he value 1.

> In general, the 4-bit contents of a Zoom register is one less than the current magnification factor. The highest magnification possible is 16 times, which occurs when one of the Zoom registers contains the value 15.

hen zoom is in effect, not all of the pixels in memory may be iewed on the screen at a time. The X Pan and Y Pan registers etermine what area of the memory is viewed. They contain the ixel number on the line, and the line number, of the first ixel placed on the screen.

t is desirable to sync zoom to vertical retrace, so that ltering the Zoom registers will not cause "tearing" of the mage.

BLINK SELECT

Blink Select is a 16-bit latch at address E40010. Each bit of the latch corresponds to one of the 16 possible planes in Bitmap memory, numbered 0 thru 15.

If a bit in the latch is SET, the information from the corresponding plane is masked to zero and unmasked at a 1.9 hertz rate. This causes a pixel containing that bit to change color numbers (point to a different color in the Lookup Table). The pixel then changes colors at 1.9 hertz.

If a bit in the latch is CLEAR, the information from the corresponding plane is not altered by the Blink Select latch.

NOTE: Blink Select should only be read or written using word (16-bit) operations.

PLANE SELECT

lane Select is a 16-bit latch at address E40012. Each bit of he latch correponds to one of the 16 possible planes in Bitmap emory, numbered 0 thru 15.

lane Select controls Z mode access to the Bitmap planes. If a it in the latch is SET, the Z mode hardware is allowed to read nd write information in that plane.

f a bit in the latch is CLEAR, the Z mode hardware will not rite into the corresponding plane. Reading a pixel in Z mode ill cause the corresponding plane to show up as a zero bit.

NOTE: Plane Select should only be read or written using word (16-bit) operations.

PLANE VIDEO SWITCH

Plane Video Switch is a 16-bit latch at address E40014. Each bit of the latch corresponds to one of the 16 possible planes in Bitmap memory, numbered 0 thru 15.

Plane Video Switch determines which planes are allowed to feed the Color Lookup Table. If a bit in the latch is SET, the plane is enabled to feed the Lookup Table normally.

If a bit in the latch is CLEAR, the information in the plane is masked to zero before feeding to the Color Lookup Table. This restricts the total number of available colors in the system, just as if a plane had been removed from the system.

NOTE: Only 8 planes at a time feed the Color Lookup Table. An image may be composed of up to 8 planes, either plane numbers 0 thru 7, or numbers 8 thru 15. The Image Select Switch (see "Overlay Roll Counter") determines which set of 8 planes is being viewed.

NOTE: Plane Video Switch should only be read or written using word (16-bit) operations.

COLOR STATUS FOREGROUND/BACKGROUND

Color Status Foreground is a 16-bit latch at address E40016. Color Status Background is a 16-bit latch at address E40018. Each of these contains 16-bit pixel data, used when writing to the Bitmap memory in Color Status mode (addresses E00000 thru 1FFFF).

See "Image Memory Addressing - Z Mode" for details on the use of these registers.

OVERLAY ROLL COUNTER

The Overlay Roll Counter is a latch at address E4001A. The low 12 bits are used for Overlay scrolling, and the upper 3 bits have special uses as discussed below.

The Overlay is an area of memory containing 4096 long words (32 bits each). Of these, 4080 are visible on the screen at one time, arranged 85 horizontally by 48 vertically. The low 12 bits of the Overlay Roll Counter decide which of these 4096 locations is considered as the first character cell of the Overlay, by adding the 12-bit value, modulo 4096, to any address which tries to access memory in the Overlay address space.

> By altering the low 12 bits of the Overlay Roll Counter, you determine which physical RAM location is addressed as the beginning of the Overlay. As far as the CPU is concerned, however, the first cell of the Overlay is always addressed at E38000.

The Overlay Roll Counter is primarily useful for scrolling. By adding 85 to the lower 12 bits of the latch, the apparent effect is that every line of characters on the Overlay screen has moved up one line. Then, the software need only erase the last line of the Overlay (which is in a known location in memory) and scrolling is complete. Scrolling down is accomplished by subtracting 85 from the low 12 bits of the Overlay Roll Counter.

It is not necessary to scroll a line at a time. If the low 12 bits of the Overlay Roll Counter are incremented by one, every character on the screen will move left one position. The characters at the beginning of each line will move to the end of the previous line. The first character on the screen will move into the 16-cell area that is not visible.

IMAGE SELECT

Bit 13 of the Overlay Roll Counter (E4001A) is the Image Select switch. If CLEAR, Bitmap planes 0 thru 7 are selected as the image to be displayed in Bitmap. If SET, planes 8 thru 15 are selected.

OVERLAY CURSOR BLINK

Bit 14 of the Overlay Roll Counter (E4001A) determines whether the Overlay cursor will blink. If SET, any Overlay character cell with the cursor bit on will contain a blinking cursor. If CLEAR, Overlay cursor(s) will not blink.

Overlay cursors are produced by hardware, so their color is always white.

OVERLAY CHARACTER BLINK

Bit 15 of the Overlay Roll Counter (E4001A) determines whether the Overlay characters are allowed to blink. If SET, any Overlay character cell with the blink bit on will blink (foreground color will blink to background). If CLEAR, no characters in the Overlay will blink.

If this bit is clear, the blink bits in each Overlay cell may be used for other purposes, such as a flag for protected fields on the screen.

I/O MAP

eripheral input/output is mapped into the last 32K of memory, eginning at address FF8000.

FF800X	RS-232 Serial Port
FF804X	RS-449 Serial Port
FF808X	Keyboard
FF80CX	Joystick
FF810X	Disk
FF814X	Bezel Switches
FF818X	Baud Rate Generator
FF81CX	Real Time Clock
FF820X	Interrupt Mask
FF824X	Bus Chip Select 1
FF828X	Bus Chip Select 2
FF82CX	Bus Chip Select 3
FF830X	Bus Chip Select 4
FF834X	Bus Chip Select 5
FF838X	Bus Chip Select 6
FF83CX	Sound Generator

SERIAL PORTS

The RS-232 and RS-449 serial interfaces are located on the CPU card. Peripherals connect to these ports through standard D-type connectors on the back of the CPU card.

The RS-232 and RS-449 ports are mapped identically. Each is configured with an Intel 8251A USART.

RS-232 Serial Port

Data register:	FF8001
Control/Status register:	FF8003

RS-449 Serial Port

Data register:	FF8041
Control/Status register:	FF8043

NOTE: The serial ports should be accessed only through byte (8-bit) operations.

The user is referred to Intel literature for details on programming the 8251A.

SERIAL PORT PINOUTS

RS-232 (25-pin connector)

Pin #	Signal	Description
2	TxD	Transmitted Data (output)
3	RxD	Received Data (input)
4	RTS	Request To Send (output)
5	CTS	Clear To Send (input)
6	DSR	Data Set Ready (input)
7	Gnd	Signal Ground
20	DTR	Data Terminal Ready (output)

Other pins are not connected in the 7900.

RS-449 (37-pin connector)

Pin #	Signal	Description
4	SD-A	Send Data (output: equiv. to TxD)
22	SD-B	
6	RD-A	Receive Data (input: equiv. to RxD)
24	RD-B	
7	RS-A	Request to Send (output: equiv. to RTS)
25	RS-B	
9	CS-A	Clear to Send (input: equiv. to CTS)
27	CS-B	
11	DM-A	Data Mode (input: equiv. to DSR)
29	DM-B	
13	RR-A	Receiver Ready (output: equiv. to DTR)
31	RR-B	
18	TM	Test Mode (input: equiv. to DSR)
20	RC	Receiver Common (used for TM only)

Other pins are not connected in the 7900.

INTERFACING RS-232 AND RS-449

Both RS-232 and RS-449 are specifications for interconnecting data equipment. Originally designed for connecting a terminal to a modem, these two "standards" are now applied to interconnect a wide variety of data systems.

RS-449 is a more recent specification. It is designed to be upward compatible from RS-232, so that RS-232 systems can interface to RS-449 with a simple wiring change. RS-449 allows much longer cable lengths between systems, as it employs balanced line drivers and receivers for greater noise immunity. RS-449 also allows higher data rates, although the CGC 7900 limits data rates to 19,200 baud (this insures compatibility between the RS-232 and RS-449 systems.)

RS-449 outputs may be fed to RS-232 inputs. The "high" side of the RS-449 output driver should be connected to the RS-232 input receiver. The "low" side of the RS-449 output driver should be grounded. The "high" side is termed "-A" in the pinout chart.

RS-232 outputs may be fed to RS-449 inputs. The RS-232 output driver should be connected to the "high" side of the RS-449 input receiver. The "low" side of the RS-449 input receiver should be connected to RS-232 signal ground, pin 7.

In these configurations, RS-232 limits for cable length and data rate must be followed. Cable length should not exceed 50 feet.

BAUD RATE GENERATOR

he 7900 uses a Motorola K1135A Dual Baud Rate Generator, apable of producing two independent clocks. One of these locks feeds the USART for the RS-232 serial port, the other eeds the RS-449 USART. The output frequency of the Baud Rate enerator is 16 times the selected baud rate. The USARTs should e programmed to accept a 16x clock.

his is a "write-only" area of memory; the contents of the BRG ay not be read.

oth baud rates are set simultaneously by an 8-bit byte written o the Baud Rate Generator, at address FF8181. The upper 4 bits letermine the RS-449 baud rate, and the lower 4 determine the S-232 baud rate, according to the following table.

Baud Rate	4-bit Value
50	0
75	1
110	2
134.5	3
150	4
300	5
600	6
1200	7
1800	8
2000	9
2400	A
3600	B
4800	C
7200	D
9600	E
19200	F

Example: to set the RS-449 port to 9600 baud, and the RS-232 port to 110 baud, do a

```
MOVE.B    #$E2,$FF8181
```

NOTE: The Baud Rate Generator should be accessed only through byte (8-bit) operations.

JOYSTICK

Joystick data addresses:

X: FF80C2

Y: FF80C4

Z: FF80C8

The joystick incorporates a 10-bit analog-to-digital converter. The A-to-D can only convert one axis of joystick data at a time, and it requires approximately 25 microseconds to perform a conversion.

The procedure for reading a joystick axis is as follows: Read a word from the address listed for the desired axis. This selects the axis, and causes the A-to-D to begin conversion. Then, wait for conversion to occur. You can tell when conversion is complete by reading back bit 11 of the SAME address. Or, simply wait for a time interval greater than 25 microseconds. When conversion is complete, read back the data. For example:

```
        MOVE.L   #$FF80C2,A0     point A0 to X-axis

LOOP    MOVE.W   (A0),D0         select the axis and read data
        BTST     #11,D0          conversion done?
        BNE.S    LOOP            no, so wait

        ANDI.L   #$3FF,D0        mask to 10 bits
```

When this routine exits, D0 contains valid data from the joystick X-axis.

he address you read from has the effect of selecting which axis f analog data is sent to the A-to-D converter. However, eading from any of the addresses above will return output data rom the A-to-D. Taking advantage of this fact, it is possible o read data from a previous conversion while beginning the next onversion. For example:

```
MOVE.L   #$FF80C2,A0     point to X-axis

BSR      WAIT            wait for conversion (as above)

MOVE.L   #$FF80C4,A0     point to Y-axis

MOVE.W   (A0),D0         read converted X-value, and
                         also begin conversion of Y
..etc...
```

NOTE: Accessing any addresses other than those listed above may cause more than one axis to be simultaneously selected. The analog signals would be combined in unpredictable ways.

The joystick has the capacity to produce an interrupt whenever it is moved in any of the three axes. If the joystick interrupt bit is unmasked (in the Interrupt Mask register), moving the joystick "off top dead center" will cause an interrupt. The joystick continues to produce interrupts for as long as it is held off center in any of the three axes. Interrupts occur at one of two rates. Slow (approx. 10 hertz) is the normal rate. By pressing the REPEAT key on the keyboard, the interrupt rate may be increased to approximately 50 hertz.

BEZEL SWITCHES

Bezel Switch data:

Read (byte) from FF8141

The states of all 8 Bezel Switches are read simultaneously by reading a byte from the Bezel Switch address. Bits 0 thru 7 represent the condition of the 8 switches.

Bezel Switch data is ACTIVE LOW. If a switch is depressed, the corresponding bit will be ZERO.

Pressing any Bezel Switch will cause an interrupt if the proper bit is cleared in the Interrupt Mask register.

INTERRUPT MASK

ıe Interrupt Mask is a 16-bit latch which determines what ıterrupts are passed through to the 68000 processor. The Mask s loaded by a 16-bit Word written to address FF8200. This is a ırite-only" latch. Programs which modify the Interrupt Mask hould keep a copy of its contents in RAM.

he following table describes which interrupt is affected by ach bit in the Mask. If a bit is SET, interrupts are INHIBITED rom the corresponding device.

Vector Addr.	Mask Bit	Device
12C	0	Real Time Clock
110	1	RS-449 Tx Ready
130	2	BINT 2 (P1-100)
10C	3	RS-232 Tx Ready
108	4	Disk
134	5	BINT 3 (P1-102)
114	6	Bezel Keys
128	7	Keyboard
124	8	RS-449 Rx Ready
118	9	Light Pen (P1-96)
138	10	BINT 4 (P1-104)
104	11	Joystick
100	12	Vertical Retrace (P2-94)
13C	13	BINT 5 (P1-106)
11C	14	BINT 1 (P1-98)
120	15	RS-232 Rx Ready

Here is the same information (organized by vector addresses):

100	12	Vertical Retrace (P2-94)
104	11	Joystick
108	4	Disk
10C	3	RS-232 Tx Ready
110	1	RS-449 Tx Ready
114	6	Bezel Keys
118	9	Light Pen (P1-96)
11C	14	BINT 1 (P1-98)
120	15	RS-232 Rx Ready
124	8	RS-449 Rx Ready
128	7	Keyboard
12C	0	Real Time Clock
130	2	BINT 2 (P1-100)
134	5	BINT 3 (P1-102)
138	10	BINT 4 (P1-104)
13C	13	BINT 5 (P1-106)

BUS INTERRUPTS (BINT)

Five interrupt lines are provided on the bus for peripherals to use.

BINT1 and BINT2 are in use by the 7900 system or are reserved for future use. BINT3, BINT4 and BINT5 are available for user peripherals. Each of these is pulled-up on the CPU card. User circuits should provide an open-collector gate to pull down the line to ground when an interrupt is desired. The line must remain low until the interrupt is serviced by the CPU.

Signal Name	Vector Address	Bus Pin #	Use
BINT1	11C	P1-98	System
BINT2	130	P1-100	System
BINT3	134	P1-102	User
BINT4	138	P1-104	User
BINT5	13C	P1-106	User

When the interrupt is serviced, the processor will fetch the address of the interrupt service routine from the memory locations listed above. BINTs must be enabled and disabled through the Interrupt Mask Register. See the preceding page for mask bit assignments.

BUS CHIP SELECTS

ix lines are provided on the system bus for selecting system nd user peripherals. Each of these lines will go LOW when the ppropriate block of memory is accessed.

CS1, BCS2 and BCS3 are in use by the 7900 system or are eserved for future use. BCS4, BCS5 and BCS6 are available for ser peripherals. It is suggested that the user completely ecode the low 6 bits of the address, in order to make efficient se of the available address space.

A block of 64 memory addresses is reserved for each Bus Chip Select line. The table below lists the starting address for each block.

Signal Name	Block Address	Bus Pin #	Use
BCS1	FF8240	P1-73	System
BCS2	FF8280	P1-76	System
BCS3	FF82C0	P1-75	System
BCS4	FF8300	P1-78	User
BCS5	FF8240	P1-77	User
BCS6	FF8280	P1-80	User

Logic on the CPU card provides DTACK whenever BCS addresses are accessed, so the user's devices do not need to assert this signal.

All BCS lines assert VPA. This allows slow peripherals, such as MC6800 series devices, to use BCS lines for selection.

BCS1 ADDRESSES

Several system peripherals are selected using the signal BCS1. These are the light pen, buffer memory parity functions, and sync information (vertical and horizontal retrace timing).

LIGHT PEN

Enable Light Pen: Write (word) to FF8240

Write a 1 to enable blue flood, or 0 to disable it.

Writing to FF8240 will enable the light pen, or re-enable it from a previous "hit." If bit 0 of the data written is CLEAR, the blue flood is disabled. If bit 0 is SET, touching the light pen will cause the Overlay to flood blue in areas which have the "Foreground Visible" bit set. After a hit, blue flood is disabled until explicitly re-enabled.

If blue flood is disabled, only bright blue or white areas of the screen will be able to cause a light pen hit.

After an interrupt, read back the location of the hit:

X address: FF8242 (0 <= X <= 1022)

Y address: FF8244 (0 <= Y <= 766)

Each address holds a 10-bit number, corresponding to the absolute screen coordinates where the hit was detected. Bit 0 of the number will always be zero, so the effective resolution of the light pen is 511 by 383.

NOTE: Bits 15 through 10 of the hit location will float high, and be read back as ones!

NOTE: Light Pen addresses should be accessed only through word (16-bit) operations.

SYNC ADDRESSES

Sync:

Read (word) from FF824C

All sync information is available by reading a word (16 bits) from address FF824C. The bits reveal the following information:

Bit 0: Low during vertical retrace

Bit 1: Interlace Flag

Bit 2: Low during horizontal retrace

All other bits float high.

Bit 0 is low while the CRT beam is being blanked during vertical retrace. The falling edge of this bit coincides with the falling edge of signal VERT (P2-94 on the bus), and the Vertical Retrace interrupt, if enabled.

Bit 1 is high during the first field of the interlaced display. Field one is the field containing the first visible line of the CRT. This bit is low during field two, the field containing the second line.

Bit 2 is low while the CRT beam is being blanked during horizontal retrace.

BUFFER MEMORY PARITY

Check for parity error:

Read (word) from FF8246

To check if a parity error has been detected in a buffer memory card, read a word (16 bits) from address FF8246. If bit 0 is low, it means one or more buffer memory cards have signalled an error.

Parity flip-flop:

Write (word) to FF8248

The parity flip-flop is set or reset by writing a word (16 bits) to address FF8248. Writing a one to this address sets the parity flip-flop which generates an immediate bus error. This is used for testing the bus error handling software. The software must read the other parity address to see if the bus error was a result of parity, or other causes.

To recover from a parity error, the software must reset the parity flip-flop by writing a zero to FF8248.

NOTE: Each buffer memory card has a jumper which must be installed before parity checking will function.

NOTE: If parity checking is enabled, the software should write into ALL buffer memory when the system is powered up. Otherwise, if a program reads from a location that was not previously written into, a parity error will result.

DISK PORT

ata:

Read/Write (word) at FF8100

tatus:

Read/Write (word) at FF8120

he disk port communicates over 8 bidirectional data lines and 8 ontrol lines. Hardware on the CPU card handles 16-bit data ransfers over the 8-bit port.

he CGC 7900 disk interface was desigsned to accomodate an ntelligent disk controller, the Data Technology Corporation 403D. This controller uses a protocol which requires the ontroller to take the initiative in most exchanges of data. he CPU selects the controller, after which the controller asks or its instructions.

hen the CPU wants to write data to the disk, it first selects he disk by writing to FF8120. This sets Select low, and also ets Data Bit 0 low. This disk controller recognises this and sserts Busy low. Asserting Busy immediately resets Select to he high state. The controller will request instructions oncerning the type of operation about to take place, and the PU responds by writing data.

he CPU writes its 16-bit data words to FF8100. This causes cknowledge to go low. The disk controller sets Request high nd the high-order (most significant) byte is transferred to the isk. When this first byte is accepted by the disk, it sets equest low again and the low-order byte is transferred.

When the disk controller has data for the CPU, or needs information from the CPU, it sets Message low which initiates a CPU interrupt. The CPU may then read the status of the disk controller to determine what is required. Bits in the status register are defined as follows:

15 thru 6	5	4	3	2	1	0
unused	RDY*	BSY*	REQ*	MSG*	C*/D	I*/O

Bit 5 is Ready, which is low when the hardware has assembled a 16-bit word for the CPU to read. Other bits are as defined in the pinout chart (see following page).

DISK PORT PINOUT

he disk connects to the CPU card at connector "A", the bottom onnector on the card. The followins table describes the isnals on this connector. Control lines are ACTIVE LOW if ndicated with an asterisk (*).

Pin No.	Description	Direction
1	Data Bit 0	Bidirectional
2	Data Bit 1	Bidirectional
3	Data Bit 2	Bidirectional
4	Data Bit 3	Bidirectional
5	Data Bit 4	Bidirectional
6	Data Bit 5	Bidirectional
7	Data Bit 6	Bidirectional
8	Data Bit 7	Bidirectional
9	Acknowledge*	CPU to Disk
10	Reset*	CPU to Disk
11	Select*	CPU to Disk
12	Busy*	Disk to CPU
13	Request*	Disk to CPU
14	Message*	Disk to CPU
15	I* / O	Disk to CPU
16	C* / D	Disk to CPU
17	Ground	
.	"	
.	"	
.	"	
26	"	

Reset* is an open-collector line. All other output lines are driven by TTL bus drivers. All control inputs are terminated on the CPU card by 220/330 ohm resistor networks.

I*/O is used by the disk to tell the CPU whether the next exchange is to be an input or output.

C*/D is used by the disk to tell the CPU whether control or data information is to be exchanged.

REAL TIME CLOCK

National Semiconductor MM58167 Real Time Clock may optionally e installed in your 7900 system. This device contains esisters for months, days, etc., down to milliseconds. A set f latches may also be programmed to produce an interrupt at elected intervals.

ll access to the Real Time Clock should be through byte (8-bit) erations. The values transferred to and from the clock will e in the form of two BCD values, concatenated in an eight-bit yte. The following table describes what the upper and lower 4 its of each register will contain.

Address	.....Register Contents.....			
	(bits 7-4)	(bits 3-0)		
FF81C1	thousandths			(0-9)
FF81C3	tenths	hundredths	Seconds counters	(00-99)
FF81C5	tens	units		(00-59)
FF81C7	tens	units	Minutes counter	(00-59)
FF81C9	tens	units	Hours counter	(00-23)
FF81CB		units	Day of Week counter	(1-7)
FF81CD	tens	units	Day of Month counter	(1-31)
FF81CF	tens	units	Months counter	(1-12)
FF81D1	thousandths			
FF81D3	tenths	hundredths	Seconds latches	
FF81D5	tens	units		
FF81D7	tens	units	Minutes latch	
FF81D9	tens	units	Hours latch	
FF81DB		units	Day of Week latch	
FF81DD	tens	units	Day of Month latch	
FF81DF	tens	units	Months latch	

The following addresses in the Real Time Clock are used for command or status information (not BCD).

FF81E1	interrupt status register
FF81E3	interrupt control register
FF81E5	counter reset
FF81E7	latch reset
FF81E9	status bit
FF81EB	"GO" command
FF81ED	standby interrupt
FF81FF	test mode

Writing to the "GO" address resets all counters from seconds to thousandths of seconds.

The status bit should be read after reading any time register. The low bit of this data will be a one if the time register changed during the read, meaning the time register should be read again for valid data.

The bits in the interrupt control and status registers are defined as follows:

Bit No.	Function
0	Comparator (latch equals real-time)
1	Every Tenth of a Second
2	Every Second
3	Every Minute
4	Every Hours
5	Every Day
6	Every Week
7	Every Month

o enable an interrupt at the specified rate, write a "1" into ne corresponding bit of the interrupt control register. (You ust also enable the Real-Time Clock interrupt in the Interrupt ask Register of the CPU.) To clear the interrupt, and discover hat bit caused it, read the interrupt status register.

he user is referred to National Semiconductor literature for urther details on programming the MM58167.

PROGRAMMABLE SOUND GENERATOR

The 7900 uses a General Instruments AY-3-8910 Programmable Sound Generator (PSG). The PSG is located on the CPU card, along with its associated amplifier circuitry. A volume control is also located on the CPU card.

Address	Function
FF83C1	Latch Address
FF83C3	Read From PSG
FF83C5	Write To PSG

The PSG uses a multiplexed addressing system, which is not directly compatible with the MC68000 processor. It is necessary to perform two operations to write a value to the PSG: First tell it which register you want to write into, then provide the data which goes in the register.

If desired, further values can then be entered into the same register without performing the "Latch Address" function again.

Example of code to write "Value" to "Register" in the PSG:

```
MOVE.B    #Register,$FF83C1    tell it which register
MOVE.B    #Value,$FF83C5       put the value in it
```

All of the PSG registers may be read, as well as written. It is necessary to perform the same sequence as for writing: latch the register address (using a write), then read the register (using a read).

NOTE: The PSG should be accessed through byte (8-bit) operations only.

PROGRAMMING THE PSG

he CGC 7900 feeds the PSG with a clock frequency of 1/8 the ain system clock frequency. In the standard 7900 system, this rovides the PSG with a 1.780 Megahertz clock.

he frequency of a tone from any of the 3 analog outputs (A, B r C) is defined to be

$$Ft = Fclk / (16*TP)$$

here Ft is the frequency of the desired tone, Fclk is the PSG lock frequency, and TP is the number which must be entered into he PSG Tone Period register to produce the desired frequency. olving for TP,

$$TP = 111250 / Ft$$

P is allowed to be up to a 12-bit number. The lower eight bits re entered into the Fine Tune register, and the upper four bits re entered into the Coarse Tune register.

The calculations for noise period are identical:

$$NP = 111250 / Fn$$

Where Fn is the desired noise frequency, and NP is the number which must be entered into the PSG Noise Period register. NP may be up to a 5-bit number.

Envelope period (the duration of a tone) is defined to be

$$Te = 256*EP / Fclk$$

Where Te is the desired envelope duration (in seconds), Fclk is the PSG clock frequency defined above, and EP is the 16-bit number which must be entered into the PSG Envelope Period registers. Solving for EP,

$$EP = Te * 6953$$

PSG REGISTERS

The PSG contains 16 internal registers, each of which may be accessed by the Latch Address/Write to Register procedure mentioned earlier. The registers are defined as follows:

Register #	Purpose
0	Fine Tune A (8 bits)
1	Coarse Tune A (4 bits)
2	Fine Tune B (8 bits)
3	Coarse Tune B (4 bits)
4	Fine Tune C (8 bits)
5	Coarse Tune C (4 bits)
6	Noise Period (5 bits)
7	Output Enable (active low)
8	A Amplitude (5 bits)
9	B Amplitude (5 bits)
10	C Amplitude (5 bits)
11	Envelope Period Fine (8 bits)
12	Envelope Period Coarse (8 bits)
13	Envelope Shape/Cycle Control (4 bits)
14	not used
15	not used

one and/or noise are enabled by register 7:

7	6	5	4	3	2	1	0
X	X	An	Bn	Cn	At	Bt	Ct

A logic zero on any of the "n" bits enables noise from that channel. A logic zero on any of the "t" bits enables tone from that channel. Unused channels are turned off by writing logic ones in the desired bits.

Registers 8, 9 and 10 control the output amplitudes:

7	6	5	4	3	2	1	0
X	X	X	A	manual level ctrl			

A logic one in bit 4 specifies the channel's amplitude to be controlled by the envelope generator (Auto mode). If bit 4 is a zero, the amplitude is fixed by the value in bits 0-3.

The envelope generator is controlled by register 13:

7	6	5	4	3	2	1	0
X	X	X	X	cont	attk	alt	hold

Bits 0-3 describe the envelope with "continue," "attack," "alternate," and "hold." See General Instruments literature for the envelope waveforms.

The following table provides values which may be entered into the Tune registers (A, B or C) to produce the musical notes shown. Please note that the given values are approximations which best fit the required frequencies for each note. It is necessary to divide up each value and load the low 8 bits into the Fine Tune register, and the upper eight bits into the Coarse Tune register.

PSG MUSICAL NOTES

Note	Freq.	Dec.	Hex	Note	Freq.	Dec.	Hex
C 1	32.7	3402	0D4A	C 5	523.2	213	00D5
C# 1	34.6	3211	0C8B	C# 5	554.4	201	00C9
D 1	36.7	3031	0BD7	D 5	587.3	189	00BD
D# 1	38.9	2861	0B2D	D# 5	622.3	179	00B3
E 1	41.2	2700	0A8C	E 5	659.3	169	00A9
F 1	43.7	2548	09F4	F 5	698.5	159	009F
F# 1	46.2	2405	0965	F# 5	740	150	0096
G 1	49	2270	08DE	G 5	784	142	008E
G# 1	51.9	2143	085F	G# 5	830.6	134	0086
A 1	55	2023	07E7	A 5	880	126	007E
A# 1	58.3	1909	0775	A# 5	932.3	119	0077
B 1	61.7	1802	070A	B 5	987.8	113	0071
C 2	65.4	1701	06A5	C 6	1046.5	106	006A
C# 2	69.3	1605	0645	C# 6	1108.7	100	0064
D 2	73.4	1515	05EB	D 6	1174.7	95	005F
D# 2	77.8	1430	0596	D# 6	1244.5	89	0059
E 2	82.4	1350	0546	E 6	1318.5	84	0054
F 2	87.3	1274	04FA	F 6	1396.9	80	0050
F# 2	92.5	1203	04B3	F# 6	1480	75	004B
G 2	98	1135	046F	G 6	1568	71	0047
G# 2	103.8	1072	0430	G# 6	1661.2	67	0043
A 2	110	1011	03F3	A 6	1760	63	003F
A# 2	116.5	955	03BB	A# 6	1864.6	60	003C
B 2	123.5	901	0385	B 6	1975.5	56	0038
C 3	130.8	850	0352	C 7	2093	53	0035
C# 3	138.6	803	0323	C# 7	2217.5	50	0032
D 3	146.8	758	02F6	D 7	2349.3	47	002F
D# 3	155.6	715	02CB	D# 7	2489	45	002D
E 3	164.8	675	02A3	E 7	2637	42	002A
F 3	174.6	637	027D	F 7	2793.8	40	0028
F# 3	185	601	0259	F# 7	2959.9	38	0026
G 3	196	568	0238	G 7	3135.9	35	0023
G# 3	207.7	536	0218	G# 7	3322.4	33	0021
A 3	220	506	01FA	A 7	3520	32	0020
A# 3	233.1	477	01DD	A# 7	3729.3	30	001E
B 3	246.9	451	01C3	B 7	3951	28	001C
C 4	261.6	425	01A9	C 8	4186	27	001B
C# 4	277.2	401	0191	C# 8	4434.9	25	0019
D 4	293.7	379	017B	D 8	4698.6	24	0018
D# 4	311.1	358	0166	D# 8	4978	22	0016
E 4	329.6	338	0152	E 8	5274	21	0015
F 4	349.2	319	013F	F 8	5587.6	20	0014
F# 4	370	301	012D	F# 8	5919.9	19	0013
G 4	392	284	011C	G 8	6271.9	18	0012
G# 4	415.3	268	010C	G# 8	6644.9	17	0011
A 4	440	253	00FD	A 8	7040	16	0010
A# 4	466.2	239	00EF	A# 8	7458.6	15	000F
B 4	493.9	225	00E1	B 8	7902.1	14	000E

KEYBOARD

he CGC 7900 contains an intellisent keyboard, with its own 8035 icroprocessor. The CPU communicates to the keyboard processor ver a 12-bit data bus, 8 bits of which are bidirectional. The nterface is asynchronous: each processor will interrupt the ther when it has something to say.

hen a key is pressed, the keyboard processor determines an 8-bit code to transmit. Most of these are 7-bit ASCII codes, xcept the labeled keys on the top of the keyboard produce pecial 8-bit codes which the CPU software must interpret. The 11, M2, CTRL and SHIFT modifiers are used by the keyboard rocessor to modify the transmitted code. These four keys are lso brought out to the 12-bit data bus, so that the CPU can ead them directly if necessary.

he keyboard processor next presents the data to the CPU, and trobes the Key Strobe line on the keyboard bus. Keyboard nterface logic on the CPU card sets the Host Acknowledge line ow to indicate that data has not yet been accepted by the CPU. hen the CPU services the Key Strobe interrupt, the Host cknowledge line is set high once again. The CPU services a Key trobe interrupt by reading a word (16 bits) from address FF8080.

hen the CPU wishes to modify the keyboard lights, it must write o the keyboard address. After writing to the keyboard lights nce, the CPU must wait for data to be accepted before writing gain. This requires waiting approximately 100 microseconds etween writes to the keyboard lights.

> NOTE: After the keyboard processor has accepted data for the lights, it will strobe the Key Strobe line on the CPU card. This pulse is "intercepted" by the keyboard interface logic on the CPU card and does not actually generate a CPU interrupt.

Several keys on the keyboard produce special functions:

RESET provides an active-low output directly to the CPU card, to reset the entire system. This is independent of the keyboard processor.

QUIET LOCK is an alternate action key, giving a high or low output to the CPU card. The 7900 uses this to enable and disable the speaker. This is independent of the keyboard processor.

ALPHA LOCK is an alternate action key which modifies the alphabetic ASCII characters produced by the typewriter area of the keyboard. When UP, alpha characters are normally upper case, and SHIFT modifies them to lower case. When DOWN, alpha keys are normally lower case and SHIFT modifies them to upper case. This is under control of the keyboard processor.

All keys on the keyboard are two-key rollover, except the cursor movement (arrow) keys. These four are N-key rollover, and produce unique codes when two are pressed simultaneously. When properly interpreted by the CPU, these unique codes allow diagonal cursor movement.

All keys on the keyboard have two repeat speeds (except for the special keys mentioned above). Auto repeat is invoked if a key is depressed for more than 0.75 second. Auto repeat occurs at 10 hertz. Manual repeat is invoked by pressing the desired key and simultaneously holding the REPEAT key. Manual repeat occurs at 50 hertz. The REPEAT key is also used to generate interrupts as part of the joystick interface.

KEYBOARD CABLE PINOUT

he keyboard connects to the CPU over a 26-pin ribbon cable. he lines are defined as follows:

Pin No.	Function
1	RESET to CPU (active low)
2	Data Bit 0
3	Data Bit 1
4	Data Bit 2
5	Data Bit 3
6	Data Bit 4
7	Data Bit 5
8	Data Bit 6
9	Data Bit 7
10	Data Bit 10
11	Data Bit 11
12	Data Bit 9
13	Data Bit 8
14	Quiet Lock (key up = logic high)
15	LED Strobe (active low)
16	Key Strobe (active low)
17	Host Acknowledge (high if CPU ready)
18	Repeat (low when REPEAT depressed)
19	Ground
21	Ground
23	Ground
25	Ground
20	+5 Volts
22	+5 Volts
24	+5 Volts
26	+5 Volts

KEYBOARD DATA BUS

The keyboard data bus bits are defined as follows:

Bit	Read (keyboard to CPU)	Write (CPU to keyboard)
0	Key Data Bit 0	LED Select Bit 0
1	Key Data Bit 1	LED Select Bit 1
2	Key Data Bit 2	LED Select Bit 2
3	Key Data Bit 3	LED Select Bit 3
4	Key Data Bit 4	LED Select Bit 4
5	Key Data Bit 5	
6	Key Data Bit 6	
7	Key Data Bit 7	LED Switch: 1-on, 0-off
8	SHIFT Key (active high)	
9	CTRL Key (active high)	
10	M1 Key (active high)	
11	M2 Key (active high)	

KEYBOARD LED SELECT CODES

To control an LED on the keyboard, it is necessary to place the proper LED select code on bits 0 thru 4 of the data bus, and set bit 7 high to turn the LED on, or low to turn it off. The following table provides select codes for each keyboard LED.

Key Name	Select Code (Hex)
F1	01
F2	02
F3	03
F4	04
F5	05
F6	06
F7	07
F8	08
F9	09
F10	0A
F11	0B
F12	0C
Calc Mode	0E
Rubber Band	0F
Plot	10
Roll	11
Create	12
Blink	13
Fill	14
Overlay	15
Cursor On/Off	16
2-color LED (Red)	17
2-color LED (Green)	18

Two special select codes are provided for direct control of all LEDs: Select code 00 turns all LEDs off (including the 2-color LED). Select code 1F (hex) turns on all LEDs (except the 2-color LED), regardless of the state of bit 7.

NOTE: You must wait approximately 100 microseconds between successive writes to the keyboard lights.

INTERFACING PERIPHERALS TO THE KEYBOARD PORT

Some users may wish to interface their own devices to the keyboard port on the 7900 CPU card. Any device connected to this port should conform to the cable wiring specifications given earlier. In addition, the following items should be noted:

If the keyboard device is powered by the supply provided on the keyboard port, it must draw less than 1.5 amperes at +5 volts.

All logic levels on the keyboard bus are TTL.

When the keyboard device wishes to present data to the CPU, it must provide an active-low Key Strobe of 10 to 30 microseconds. Data must be presented on the bus during Key Strobe, and be valid at least one microsecond before and after Key Strobe. The keyboard device must recognize that while Host Acknowledge is low, the CPU is unable to receive new data.

When the CPU wants to write data to the keyboard device, it will set LED Strobe low. The keyboard device must recognize this signal as putting the keyboard bus into a "write" mode. When LED Strobe is low, the keyboard device must accept data from the CPU; then, IT MUST STROBE THE KEY STROBE LINE TO INDICATE ACCEPTANCE OF DATA. This strobe must also be 10 to 30 microseconds in duration.

> NOTE: To maintain compatibility with other 7900 features, the keyboard device should provide a means for setting Quiet Lock high or low (to enable or disable the speaker), and for setting Repeat high or low (to enable interrupts from the Joystick).

KEYBOARD TIMING

CGC 7900 SYSTEM BUS

he 7900 system bus uses two connectors, P1 and P2. P1 is the ain connector for address, data and control lines, interfacing he CPU to memory and peripherals. P1 is the upper connector in he digital chassis.

2 is the lower connector in the digital chassis. P2 is used or video data and control, including signals used to control he analog high voltage supplies. For this reason, it is ecommended that P2 be considered a reserved area, for hromatics' use only. DAMAGE TO THE SYSTEM COULD RESULT IF USER EVICES ARE CONNECTED TO P2!

GC 7900 circuit cards have the same physical dimensions as equired by the Motorola VERSAbus specification. However, the us arrangement differs significantly (see the following pages). n general, VERSAbus cards MAY NOT be plugged directly into the GC 7900 card case.

P1 CONNECTOR IDENTIFICATION

Odd Pin No. Component Side	Signal Name	Even Pin No. Circuit Side	Signal Name
1	+5V	2	+5V
3	GND	4	GND
5	D00	6	D01
7	D02	8	D03
9	D04	10	D05
11	D06	12	D07
13	D08	14	D09
15	D10	16	D11
17	D12	18	D13
19	D14	20	D15
21	CMOS +5V	22	CMOS TRIGGER
23	GND	24	GND
25	LDS*	26	UDS*
27	GND	28	GND
29	DTACK*	30	AS*
31	GND	32	GND
33		34	READ/WRITE*
35		36	A01
37	A02	38	A03
39	A04	40	A05
41	A06	42	A07
43	A08	44	A09
45	A10	46	A11
47	A12	48	A13
49	A14	50	A15
51	A16	52	A17
53	A18	54	A19
55	A20	56	A21
57	A22	58	A23
59		60	
61	GND	62	GND
63		64	
65		66	
67	GND	68	GND
69		70	SYSCLK

71	GND	72	GND
73	BCS1*	74	SYSRESET*
75	BCS3*	76	BCS2*
77	BCS5*	78	BCS4*
79		80	BCS6*
81	BUSERR*	82	
83	FC0*	84	FC1*
85	FC2*	86	
87	IRQ1*	88	IRQ2*
89	IRQ3*	90	IRQ4*
91	IRQ5*	92	IRQ6*
93	IRQ7*	94	INTON*
95	IACKIN*	96	LPEN*
97	BG0*	98	BINT1*
99	BG1*	100	BINT2*
101	BG2*	102	BINT3*
103	BG3*	104	BINT4*
105	BG4*	106	BINT5*
107	BRQ0*	108	BRQ1*
109	BRQ2*	110	BRQ3*
111	BRQ4*	112	
113	BGACK*	114	BVPA*
115	BVMA*	116	
117		118	ADDR0-7*
119	GND	120	GND
121	-12V	122	-12V
123	GND	124	GND
125	+12V	126	+12V
127	+12V	128	+12V
129	+5V	130	+5V
131	+5V	132	+5V
133	-5V	134	-5V
135	GND (FOR CMOS +5)	136	GND
137	GND	138	GND
139	GND	140	GND

P1 SIGNAL DESCRIPTIONS

D00-D15 (Pins 5-20): The tristate, bidirectional data bus.

CMOS +5V (Pin 21): Supply for CMOS RAM on the CPU card, maintained during power outages by a battery.

CMOS TRIGGER (Pin 22): Goes low to disable CMOS memory access during power down and start-up, preventing spurious memory writes.

LDS* (Pin 25): Lower Data Strobe. An active low, tristate signal which indicates a data transfer on D00-D07.

UDS* (Pin 26): Upper Data Strobe. An active low, tristate signal which indicates a data transfer on D08-D15.

DTACK* (Pin 29): Data Transfer ACKnowledge. An active low, open collector signal generated by a peripheral or memory device. It indicates acceptance of data during a write, or that data has been placed on the bus in response to a read. If a non-existant memory location is accessed and DTACK* does not occur, a bus error is generated.

AS* (Pin 30): Address Strobe. An active low, tristate signal which indicates that a valid address is present on the address lines.

READ/WRITE* (Pin 34): A tristate signal used to define the type of cycle in progress. This line is high for a read cycle, low for a write cycle.

A01-A23 (Pins 36-58): Tristate address bus. Note that the lowest bit of the address is simulated by UDS* and LDS*, for 8-bit accesses.

SYSCLK (Pin 70): System Clock. This is the highest frequency clock used on the bus, 14.24 MHz in the standard 7900 system.

BCS1*-BCS6* (Pins 73, 75, 76, 77, 78, 80): Bus Chip Selects. Active low outputs from the CPU used to select certain areas of memory. See "System Memory Map."

SYSRESET* (Pin 79): System Reset. An active low, open collector signal used to reset the system. It may be generated by the

rocessor or by external devices. This line is held low during ower-up.

USERR* (pin 81): Bus Error. An active low, open collector line hich is pulled low in the event of a catastrophic system ailure. The 7900 uses this for memory parity error.

C0*-FC2* (pins 83-85): Function Code. Active low, tristate ines which indicate the state of the bus master, such as hether an interrupt acknowledge cycle is in progress.

RQ1*-IRQ7* (pins 87-93): Interrupt Request. Open collector, ctive low lines which may be pulled low by peripherals to equest an interrupt. IRQ7* is highest priority and is used uring power-up.

NTON* (pin 94): Interrupt On CPU. Active low signal which ndicates one of the 16 interrupts on the CPU card is pending. hould be tested by secondary bus masters, to allow them to elease the bus if an interrupt is waiting for service.

ACKIN* (pin 95): Interrupt Acknowledge In. Active low signal hich indicates the CPU is fetching an interrupt vector.

LPEN* (pin 96): Light Pen Interrupt. Active low, open collector signal asserted by the Light Pen logic when a hit is detected.

BG0*-BG4* (pins 97, 99, 101, 103, 105): Bus Grant. Active low signals which inform a device that it may become the bus master. Issued by the CPU in response to Bus Request. All tristate signals will go to a high impedance at the end of the bus cycle in which a Bus Grant is asserted.

BINT1*-BINT5* (pins 98, 100, 102, 104, 106): Bus Interrupt. Active low, open collector signals which allow peripherals to interrupt the CPU card. See "Interrupt Mask" for details.

BRQ0*-BRQ4* (pins 107-111): Bus Request. Active low, open collector signals used by secondary bus masters to gain access to the bus. BR04* is highest priority.

BGACK* (pin 113): Bus Grant Acknowledge. Active low signal asserted by the secondary bus master when it has assumed control of the bus.

BVPA* (Pin 114): Bus Valid Peripheral Address. Active low signal which informs the CPU that an MC6800 peripheral device is responding to the current bus cycle.

BVMA* (Pin 115): Bus Valid Memory Address. Active low, tristate line which is asserted in response to BVPA*. Used to synchronise MC6800 peripherals.

ADDR0-7* (Pin 118): Addresses 0-7 in use. Active low signal, asserted when memory locations 000000 thru 000007 are being accessed. Used during power-up to disable RAM and enable EPROM.

GND (for CMOS +5) (Pin 135): This is the supply return for the CMOS battery power. It should not be used for normal grounding purposes.

P2 CONNECTOR IDENTIFICATION

Odd Pin No. Component Side	Signal Name	Even Pin No. Circuit Side	Signal Name
1	ground	2	ground
3	ground	4	ground
5	ground	6	ground
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13		14	
15	IBIT0	16	IBIT1
17	IBIT2	18	IBIT3
19	PW0	20	R*
21	CSF*	22	CSB*
23	PWE	24	PSEL*
25	VM0	26	VM1
27	VM2	28	VM3
29	VLC	30	VDE0*
31	VDE1*	32	IBSEL
33	VB00	34	VB01
35	VB02	36	VB03
37	VB04	38	VB05
39	VB06	40	VB07
41	VB08	42	VB09
43	VB10	44	VB11
45	VB12	46	VB13
47	VB14	48	VB15
49	VB16	50	VB17
51	VB18	52	VB19
53	VB20	54	VB21
55	VB22	56	VB23
57	VB24	58	VB25
59	VB26	60	VB27
61	VB28	62	VB29
63	VB30	64	VB31
65	VB32	66	VB33
67	VB34	68	VB35
69	VB36	70	VB37

71	VB38	72	VB39
73		74	
75	BLINK	76	OLC
77	IVLC	78	PSW*
79	LBNK*	80	RA1
81	RA2	82	RA3
83	RA4	84	RA5
85	RA6	86	WU*
87	WL*	88	BIT*
89	CSE	90	EP*
91		92	LXZ*
93	MRAS*	94	VERT*
95	RFSH*	96	OMEM*
97	MCAS*	98	CROLL*
99	RAS*	100	CAS*
101	ground	102	ground
103	CH	104	HG
105	VMUX	106	
107	RC0	108	RC1
109	RC2	110	RC3
111	RC4	112	RC5
113	RC6	114	
115		116	
117		118	14M
119	-5V	120	-5V

P2 SIGNAL DESCRIPTIONS

BIT0-IBIT3 (pins 15-18): These lines hold a 4-bit number used o select one of 16 planes (in Plane Mode) or one of 16 bits (in Mode), according to the state of IBSEL.

'WO (pin 19): Plane Write Override. Keeps Plane Select latches 'rom affecting memory accesses in Plane Mode. This line is high 'hen Plane Mode addresses are used.

R* (pin 20): Read (active low).

CSF*, CSB* (pins 21 and 22): Color Status Foreground and Background strobes. These lines strobe information into the Color Status latches.

PWE (pin 23): Plane Write Enable. This line enables Plane Mode access to memory when low, and Z Mode or Color Status Mode when high. When asserted, this line overrides the IBIT lines.

PSEL* (pin 24): Plane Select strobe. This line strobes information into the Plane Select latch (1 bit per plane).

VM0-VM3 (pins 25-28): Video Mux select. Selects which 4 bits are currently being brought out on VB00-VB39 for display.

VLC (pin 29): Video Latch Control. This line strobes data from video RAM into latches, prior to bit selection by VM0-VM3.

VDE0*-VDE1* (pins 30-31): Video Data Enable. One of these two lines will be low, determining whether image planes 0-7 or 8-15 are currently being displayed.

IBSEL (pin 32): Selects Bit (Z mode) or Plane mode access to image memory.

VB00-VB39 (pins 33-72): Video Bus. Data from video RAM is brought out on these lines, 4 bits at a time, from each of 10 possible planes. (Note: only 8 planes, 0 thru 7, are currently supported by the CGC 7900.) Each of these lines is named in the form VBbp, where b is the bit number (0-3) and p is the plane number (0-9), of the data on the line.

BLINK (pin 75): A 1.9 Hz blink signal used to blink information

from image memory.

OLC (Pin 76): Output Latch Control. This line strobes data out of image memory when the CPU wishes to read from image memory.

IVLC (Pin 77): Internal Video Latch Control. This line strobes data from image RAM into "holding" latches, prior to the latches strobed by VLC.

PSW* (Pin 78): Plane Video Switch. This line strobes data into the Plane Switch latches, to determine which planes are fed to the Color Lookup Table for display.

LBNK* (Pin 79): Load Blink Select. This line strobes data into the Blink Select latches, to determine whether the data from each plane will blink (be masked to zero) at the rate set by BLINK.

RA1-RA6 (Pins 80-85): RAM Address. In Z Mode, these lines select a pixel to be read or written. In Plane Mode, they choose one 16-bit word from the 64-bit internal data bus of the RAM card.

WU*, WL* (Pins 86-87): Write Upper/Write Lower. Active low signals formed by gating UDS* and LDS* with the Write line.

BIT* (Pin 88): Bit mode. Active low signal indicating a Bit mode (Z mode) access is in progress.

CSE (Pin 89): Color Status Enable. This signal allows the Color Status addressing mode to become active.

EP* (Pin 90): Reserved for future use (hardware erase-page function).

LXZ* (Pin 92): Load X Zoom. This active low signal strobes a 4-bit number into the X Zoom register on the Color Lookup card.

MRAS*, MCAS* (Pins 93 and 97): Memory Row Address Strobe and Column Address Strobe. These RAM control lines are used during CPU accesses.

VERT* (Pin 94): Vertical Retrace. This line is low during the vertical retrace blanking interval.

:FSH* (pin 95): Refresh. This signal is used during memory ·efresh cycles.

)MEM* (pin 96): This signal pre-decodes some of the CMOS address ;pace for video hardware latches.

:ROLL* (pin 98): Character Roll strobe. This strobe loads the)verlay Roll Counter latch.

RAS*, CAS* (pins 99 and 100): Row Address Strobe and Column Address Strobe. All other memory control lines are derived from these two signals, which are always present regardless of the type of memory cycle in progress.

:H (pin 103): Character Horizontal. This signal enables the fetch of data for video display. It is advanced from HG to compensate for delays in fetching pixel data thru the Color Lookup Table.

HG (pin 104): Horizontal Gate. This is the horizontal sync signal.

VMUX (pin 105): Video Mux. This clock runs the counters whose outputs appear on VM0-VM3.

RC0-RC6 (pins 107-113): Row/Column addresses. These lines contain the addresses of whatever image memory is being accesses, in the matrixed form required by dynamic RAM.

14M (pin 118): The 14.24 MHz master clock. SYSCLK on P1 is synchronized to this signal, however its phase is different due to propagation delays.

SYNC SIGNALS

he CGC 7900 uses interlaced scan. Odd-numbered raster lines re scanned during one field, and even-numbered lines are canned during the next field. The fields are synchronized to he 60-cycle power line, so each field lasts 1/60 second, and it akes 1/30 second to display an entire frame. Interlacing is chieved by delaying the start of vertical sweep on odd fields.

he display scans 768 lines, with 1024 pixels per line. Each ixel is scanned for 35.11 nanoseconds. Three 8-bit igital-to-analog converters receive red, green and blue data rom the Digital Chassis and convert this data into three video ignals. RGB video output is available.

ll of the following signals are available at the Analog hassis, behind the CRT tube of the 7900. All sync signals are ifferential TTL, and may be received with Advanced Micro evices AM26LS33 or equivalent. Note that the polarity of the eceived signal may be altered to suit your equipment by wapping the input lines to the receiver. Sync signals are ound at J6, a 10-pin right-angle connector near the front orner of the Deflection Module. It is suggested that a Y-cable rrangement be used to feed these signals into the 7900 and the ser's equipment.

> NOTE: To prevent possible damage to the CGC 7900, insure that J6 is properly connected BEFORE applying power to the system. External devices connected to J6 must NOT impair the normal sync signals at this connector!

(1) Clock: J6 pins 4 and 9 (red/black pair). A 1.78 MHz square wave, from which all other syncs are derived. When video is active, 16 pixels are scanned during each cycle of this clock.

(2) Horizontal Reset: J6 pins 2 and 7 (yellow/black pair). The sync signal which triggers each horizontal line. Video begins 912.9 nanoseconds after Horizontal Reset goes high.

(3) Vertical Release: J6 pins 1 and 6 (green/black pair). The sync signal which triggers vertical sweep, and inhibits sweep at the proper times to provide interlace. On even fields, this signal rises simultaneously with a Horizontal Reset rising edge. On odd fields, it is delayed by 20.79 microseconds for interlace. The falling edge of this signal is triggered by power line frequency (60 hertz).

(4) Analog Video: These three signals are available on the Video Amplifier card, on the back wall of the Analog Chassis. P1 provides green, P2 is blue, and P3 is red. These signals should be received by a 50-ohm coaxial cable in each of the connectors. For best results, a 50-ohm load should be provided at the user's end of the cable. The voltage levels at each of these connectors are: zero for black, minus one volt (nominal) for maximum intensity. This level may not be adjusted without disturbing the 7900 video alignment.

HORIZONTAL TIMING

VERTICAL TIMING

CONFIGURING BUFFER MEMORY CARDS

he two rotary switches on the edge of the Buffer Memory card etermine the card's address. To set up a card, perform the ollowing steps:

. Determine what the memory address of the card should be. he card must have address 000000, and if other cards are nstalled, they will normally have consecutive addresses ollowing the first card. Consult the table below to see what witch settings correspond to the card's desired memory address.

NOTE: The 7900 memory map requires that Buffer Memory cards be addressed below 800000.

NOTE: All possible memory addresses require that the first switch be set to a number between 0 and 7. THE SYSTEM WILL FAIL if The left-hand switch on the card is set to 8 or higher!

2. Arrange the card so that the component side is up, and the old edge connector is pointing away from you. The two rotary switches should now be visible on the right side of the card's ear edge.

3. Using a small screwdriver, set the two switches so that the rrow on the left switch is pointing to the first digit of the equired setting, and the arrow on the right switch is pointing to the second digit. For example, if you are installing a card t address 020000, the table says that the correct setting is 01. Set the left switch to 0 and the right switch to 1.

(Some switches may not be marked at the odd numbered positions. If yours is not, assume that position 1 lies halfway between 0 and 2, and so on.)

BUFFER MEMORY CARD ADDRESS SELECTION

Switch Position	Memory Address	Switch Position	Memory Address	Switch Position	Memory Address
00	000000	2C	580000	58	B00000
01	020000	2D	5A0000	59	B20000
02	040000	2E	5C0000	5A	B40000
03	060000	2F	5E0000	5B	B60000
04	080000	30	600000	5C	B80000
05	0A0000	31	620000	5D	BA0000
06	0C0000	32	640000	5E	BC0000
07	0E0000	33	660000	5F	BE0000
08	100000	34	680000	60	C00000
09	120000	35	6A0000	61	C20000
0A	140000	36	6C0000	62	C40000
0B	160000	37	6E0000	63	C60000
0C	180000	38	700000	64	C80000
0D	1A0000	39	720000	65	CA0000
0E	1C0000	3A	740000	66	CC0000
0F	1E0000	3B	760000	67	CE0000
10	200000	3C	780000	68	D00000
11	220000	3D	7A0000	69	D20000
12	240000	3E	7C0000	6A	D40000
13	260000	3F	7E0000	6B	D60000
14	280000	40	800000	6C	D80000
15	2A0000	41	820000	6D	DA0000
16	2C0000	42	840000	6E	DC0000
17	2E0000	43	860000	6F	DE0000
18	300000	44	880000	70	E00000
19	320000	45	8A0000	71	E20000
1A	340000	46	8C0000	72	E40000
1B	360000	47	8E0000	73	E60000
1C	380000	48	900000	74	E80000
1D	3A0000	49	920000	75	EA0000
1E	3C0000	4A	940000	76	EC0000
1F	3E0000	4B	960000	77	EE0000
20	400000	4C	980000	78	F00000
21	420000	4D	9A0000	79	F20000
22	440000	4E	9C0000	7A	F40000
23	460000	4F	9E0000	7B	F60000
24	480000	50	A00000	7C	F80000
25	4A0000	51	A20000	7D	FA0000
26	4C0000	52	A40000	7E	FC0000
27	4E0000	53	A60000	7F	FE0000
28	500000	54	A80000		
29	520000	55	AA0000		
2A	540000	56	AC0000		
2B	560000	57	AE0000		

CONFIGURING IMAGE MEMORY PLANES

Each Image Memory Plane is assigned a unique number, from 0 to 5. Two planes in a system may NOT have the same number assigned.

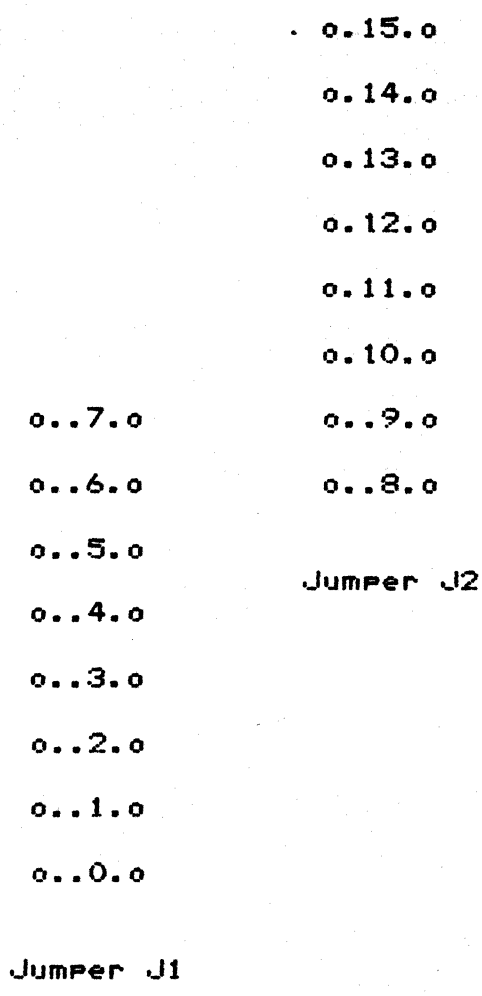
. Arrange the Image Memory card so that the component side of the card is facing you, and the gold edge connector is to the right. Locate the rotary switch, in the lower left corner of the board. The switch has a slot, which is facing down (towards you). On this side of the switch is also an arrow, which will point to one of 16 positions around the switch.

Refer to the following table, and use a small screwdriver to turn the slot until the arrow points to the proper position for your card.

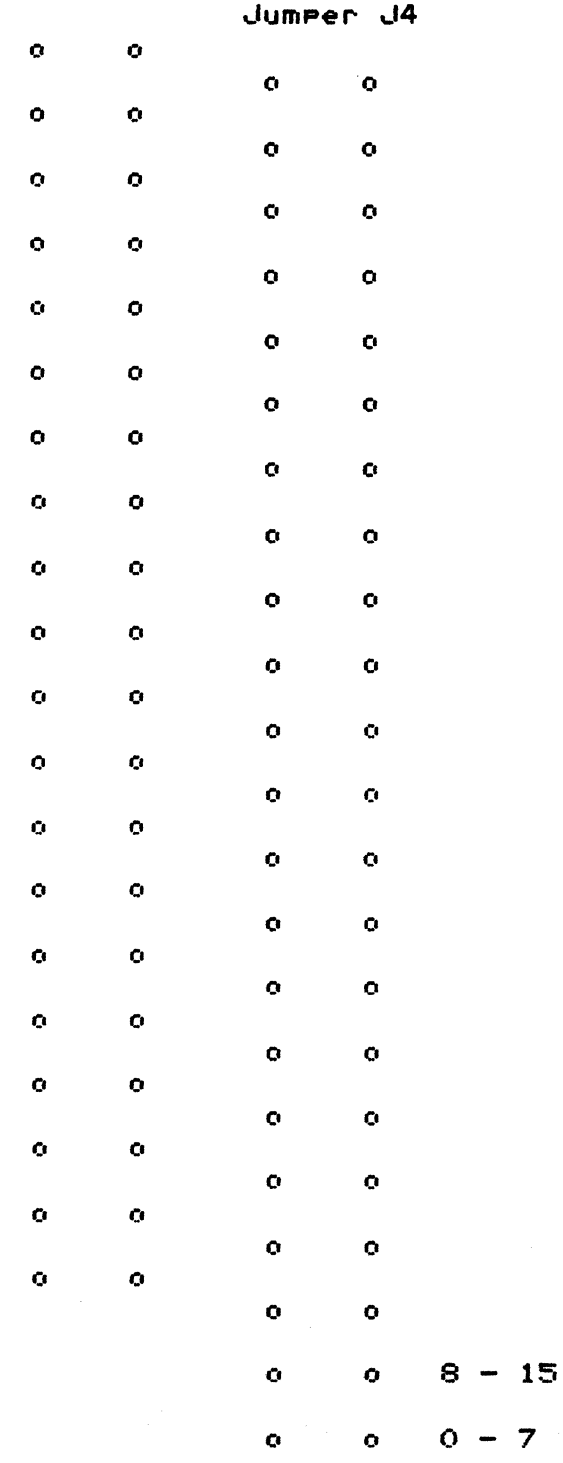
Image Plane Number	Switch Position
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	A
11	B
12	C
13	D
14	E
15	F

The odd numbered positions on the switch may not be labeled. If not, assume that position 1 lies halfway between 0 and 2, and so on.

2. Again, arrange the card so that the gold edge connector is to the right. Locate the two vertical rows of pins near the center of the right edge. Refer to the following chart, and place one (1) jumper on one of the pairs of pins, to select the desired plane number. Remove any other jumpers on these two rows of pins.



3. Locate the two vertical rows of pins near the lower right corner of the card. Refer to the folowing chart, and place one (1) jumper on the pair of pins marked "0-7", or on the pair marked "8-15", depending on which of these ranges includes the desired plane number.



4. Now, if the desired plane number is greater than 7, subtract eight from it. Thus, plane 8 becomes 0, 9 becomes 1, and so on. (If your plane number is less than 8, do not alter it.) Refer to the following table, and place four (4) jumpers on pairs of pins marked with the plane number you have just calculated.

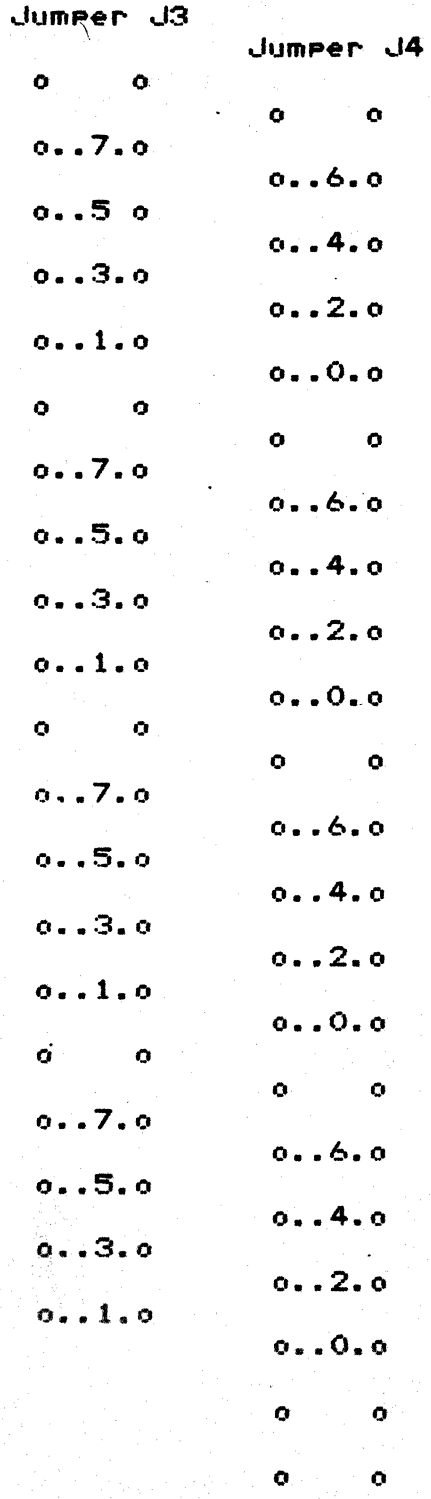


IMAGE MEMORY CONFIGURATION JUMPERS