Technical Manual No.
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Revision F

ADDENDUM H - EMBEDDED FORMATTER (DUAL-MODE)

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ADDENDUM H

DUAL-MODE EMBEDDED FORMATTER

This addendum presents a physical and electrical description of the dual-mode embedded formatter installed on the Cipher Magnetic Tape Transport to which this manual is assigned. The addendum, together with the special-configuration also included in the manual, presents all additional operational and maintenance information necessitated by the addition of the formatter to the transport. (For design information, refer to the product specification.) Please read this addendum, the supplement, and the manual thoroughly before operating or placing the transport into the system.

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SECTION I

DESCRIPTION

PHYSICAL DESCRIPTION

1-1. All components and circuitry of the formatter embedded within the chassis of the Cipher magnetic tape transport are incorporated on a single printed-wiring board. Also mounted on this board are six connectors, XJ101, XJ102, XJ103, XP101A, XP102A and XP103A, which provide all interface connections between the formatter and the transport(s), and another connector, IP101, which provides all connections from the board to the interface harness from the system. Connector IP101 is readily accessible from the rear of the transport.

1-2. The embedded formatter has no separate power supply or controls. These facilities are provided through the interface connections with the transport and/or the system.

FUNCTIONAL DESCRIPTION

1-3. The embedded formatter contains all logic and functions associated with the reading and writing of IBM/ANSI-compatible PE and NRZI magnetic tapes. Its circuitry includes all logic required for the generation of data records, CRC, LRC, file-mark patterns, and ID bursts involved in magnetic tape recording, and for the data recovery operations of data decoding, buffering, and error and file-mark detection. It performs all timing necessary for the writing of compatible interblock gaps and proper head positioning within the block.

MECHANICAL AND ELECTRICAL SPECIFICATIONS

1-4. Mechanical and electrical specifications are compatible with those of the transport on which the formatter is mounted.

INTERFACE SPECIFICATIONS

1-5. Interface specifications for the formatter are the same as those for the transport, as described in the basic manual. The formatter interface configuration is as shown in Figure 1-1 of this addendum.

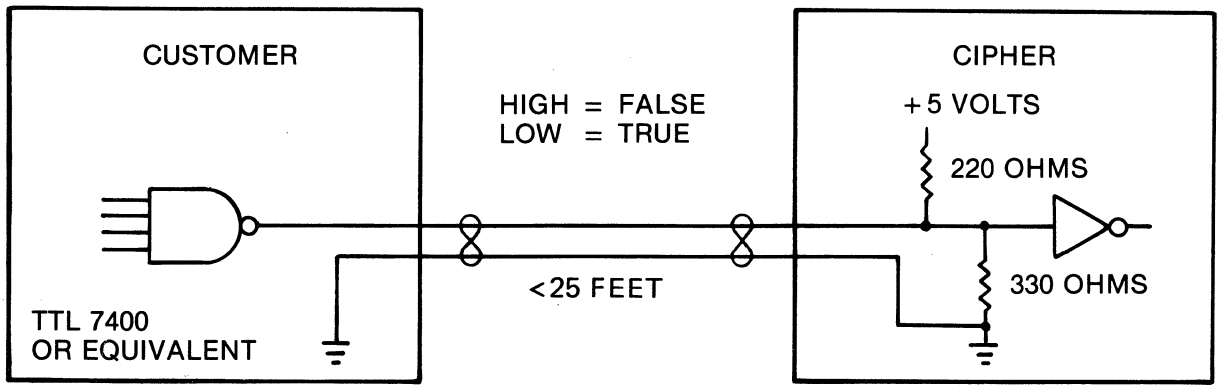


Figure 1-1. Interface Configuration

SECTION II

INSTALLATION, SWITCH SETTINGS, AND JUMPERS

INSTALLATION

2-1. As noted in Section I, the formatter is installed on the transport during manufacture. The manner of installation and all parts and components involved therein are shown in the drawing and parts list presented in the SPECIAL-CONFIGURATION SUPPLEMENT preceding this addendum.

SWITCHES

2-2. The dual-mode formatter PWB incorporates one four-position DIP switch (S1), two six-position DIP switches (S2 and S3), one five-position rotary switch (S4), and four jumpers, all of which are used to implement various configuration parameters. The functions of each of these switches and jumpers are presented here as a check list and guide to the technician in making any desired changes in the various modes of operation.

2-3. Density Selection. Switch S1, positions 1 and 2, are used with seven-track transports to select high-low density combinations.* S1-1 OFF, S1-2 ON selects densities of 800 and 200 bpi; S1-1 ON, S1-2 ON, 800 and 566 bpi; S1-1 OFF, 556 and 200 bpi.

2-4. Parity Generation. Switch S1-3, in OFF position, selects internal parity generation. ON position selects external parity generation.

2-5. Formatter Address. Switch S1-4, in OFF position, selects formatter address 0; S1-4 ON selects formatter address 1.

2-6. Speed Selection. Switches S2 and S3, in conjunction with the proper headers, are used to set the formatter for operation at either of any two standard tape speeds from 12.5 to 125 ips. Switch S2, with header U7E, sets the high speed, and switch S3, with header U7C, sets the low speed. (See Table 2-1 for switch settings and Table 2-2 for header component values for different speeds.) When transport-to-formatter input ISPEED is true, operation will be at the high-speed setting.

*The host transport must not be a seven-track machine.

2-7. Host Transport Address. For transports not having a logical unit address select switch, rotary switch S4 is used to set the address of the host transport. With S4 in OFF position, the host transport is selected. Transport address 0, 1, 2, or 3 is obtained by turning S4 to position 0, 1, 2, or 3, respectively. In a transport with a logical unit address switch, switch S4 should be set in the address 0 position.

JUMPER OPTIONS

2-8. Jumper W1 is used to route the formatter-to-transport output IWARS to J101 in the host transport. This jumper is used only on transports (such as Model 100X) in which IWARS is not routed within the transport to the control section.

2-9. Jumper W2 routes +5-volt power from the transport via J101-S to the formatter. This jumper must be removed if power is to be supplied from the system interface through IP101, or through E1, E2. In this case, the +5-volt power supply on the transport must be readjusted to compensate for the decrease in load.

2-10. Jumper W3, in the PE mode, causes IRTH2 to be forced true during the data portion of the record.

2-11. Jumper W4 provides for the use of transports with no Read Data strobes.

SPEED (ips)	SWITCH S2 AND S3 POSITIONS						FREQ. AT TP38 (MHz)
	1	2	3	4	5	6	
125	ON	ON	OFF	OFF	OFF	OFF	10.8
112.5	OFF	ON	OFF	OFF	OFF	OFF	9.72
75	OFF	OFF	ON	OFF	OFF	OFF	6.48
50	ON	OFF	OFF	ON	OFF	OFF	4.32
45	OFF	OFF	OFF	ON	OFF	OFF	3.89
37.5	OFF	ON	OFF	ON	OFF	OFF	3.24
25	OFF	OFF	OFF	OFF	ON	OFF	2.16
25 (alt.)	ON	ON	OFF	OFF	ON	OFF	2.16
22.5	OFF	ON	OFF	OFF	ON	OFF	1.94
18.75	OFF	ON	ON	OFF	ON	OFF	1.62
12.5	OFF	ON	OFF	OFF	OFF	ON	1.08
12.5 (alt.)	ON	ON	ON	OFF	OFF	ON	1.08

Table 2-1. Speed Selection Switch Settings

SPEED (ips)	HEADER COMPONENTS			
	C1	C2	C3	R1
12.5	1 µf	470pf	1 µf	1K
18.75	1 f	330pf	1 µf	1K
25	.47 µf	270pf	.22 µf	1.3K
37.5	.47 µf	180pf	.47 µf	820Ω
45	.47 µf	120pf	.47 µf	820Ω
75	.47 µf	68pf	N/A	1K
125	.47 µf	33pf	.47 µf	430Ω

Table 2-2. Component Values in Speed Headers U7E and U7C

SECTION III

INTERFACE CONNECTIONS

CONNECTORS

3-1. As noted in paragraph 1-2 of this addendum, all interface connections to the formatter are made through seven connectors: XJ101, XJ102, XJ103, XP101A, XP102A and XP103A from formatter to transport and IP101 from formatter to controller harness. Connectors XJ101, XJ102, and XJ103 are connected by cables to J101, J102, and J103, respectively, on the host transport, and connectors XP101A, XP102A, and XP103A are used for daisy chaining. Up to three additional external drives may be attached to the formatter, using Cipher daisy-chain cables.

PIN ASSIGNMENTS

3-2. The signals, mnemonics, and connector pin assignments pertaining to the interface of the formatter and controller are presented in Table 3-1. (Note that all interface mnemonics are prefixed with the letter "I".) Formatter/transport interface signals and pin assignments are as presented in Table 3-2. Plus 5-volt connectors and pin assignments are shown in Table 3-3.

CONNECTOR	LIVE PIN	GROUND PIN	SIGNAL*
IP101 Controller to Formatter	B1	B2	Formatter Address (IFAD)
	A1	A2	Transport Address (ITAD0)
	B3	B2	Transport Address (ITAD1)
	A3	A2	Initiate Command (IGO)
	B4	B5	Reverse (IREV)
	A4	A5	Write (IWRT)
	B6	B5	Write File Mark (IWFM)
	A6	A5	Edit (IEDIT)
	B7	B8	Erase (IERASE)
	A7	A8	Threshold Level 1 (ITHR1) (NRZI only)
	B9	B8	Read Threshold Level 2 (ITHR2)
	A9	A8	Density Select (IDEN) (NRZI only)
	B10	B11	Parity Select (IPAR) (NRZI only)
	A10	B15	Load and Online (ILOL)
	B12	B11	Rewind (IREW)
	A12	A11	Off-Line (IOFL)
	B13	B14	Last Word (ILWD)
	A13	A14	Formatter Enable (IFEN)
	A15	A14	Write Data Parity (IWP)
	B16	B17	Write Data 0 (IW0)
	A16	A17	Write Data 1 (IW1)
	B18	B17	Write Data 2 (IW2)

*See Section III for definitions of interface functions.

Table 3-1. Interface Connections, Formatter/Controller

CONNECTOR	LIVE PIN	GROUND PIN	SIGNAL*
IP101 Controller to Formatter	A18	A17	Write Data 3 (IW3)
	B19	B20	Write Data 4 (IW4)
	A19	A20	Write Data 5 (IW5)
	B21	B20	Write Data 6 (IW6)
	A21	A20	Write Data 7 (IW7)
IP101 Formatter to Controller	B22	B23	Formatter Busy (IFBY)
	A22	A23	Data Busy (IDBY)
	B24	B23	Identification (IIDENT/ICCG)
	A24	A23	Hard Error (IHER)
	B25	B26	Corrected Error (ICER)
	A25	A26	File Mark (IFMK)
	B27	B26	Ready (IRDY)
	A27	A26	On Line (IONL)
	B28	B29	Rewinding (IRWD)
	A28	A29	File Protect (IFPT)
	B30	B29	Load Point (ILDP)
	A30	A29	End of Tape (IEOT)
	A31	A32	NRZI (INRZ)
	B33	B32	7 Track (I7TR) (NRZI only)
	A33	A32	Single (ISGL)
	B34	B35	Speed (ISPEED)
	A34	A35	Write Strobe (IWSTR)

*See Section III for definitions of interface functions.

Table 3-1. Interface Connections, Formatter/Controller (Continued)

CONNECTOR	LIVE PIN	GROUND PIN	SIGNAL*
IP101 Formatter to Controller	B36	B35	Read Strobe (IRSTR)
	A36	A35	Read Data Parity (IRP)
	B37	B38	Read Data 0 (IR0)
	A37	A38	Read Data 1 (IR1)
	B39	B38	Read Data 2 (IR2)
	A39	A38	Read Data 3 (IR3)
	B40	B41	Read Data 4 (IR4)
	A40	A41	Read Data 5 (IR5)
	B42	B41	Read Data 6 (IR6)
	A42	A41	Read Data 7 (IR7)

*See Section III for definitions of interface functions.

Table 3-1. Interface Connections, Formatter/Controller (Continued)

CONNECTOR	LIVE PIN	GROUND PIN	SIGNAL
XJ101 - XP101A	27	See Table 3-3	Ready (IRDY)
	35	--	On Line (IONL)
	33	--	Rewinding (IRWD)
	31	--	File Protect (IFPT)
	25	--	Load Point (ILDP)
	29	--	End of Tape (IEOT)
	37	--	Data Density Indicator (IDOI)
XJ103 - XP103A	20	19	NRZI (INRZ)
	22	21	Seven Track (I7TR)
	24	23	Single (ISGL)
	26	25	Speed (ISPEED)
	4	3	Read Data Strobe (IRDS)
	2	1	Read Data Parity (IRDP)
	6	5	Read Data 0 (IRD0)
	8	7	Read Data 1 (IRD1)
	16	15	Read Data 2 (IRD2)
	18	17	Read Data 3 (IRD3)
	28	27	Read Data 4 (IRD4)
	30	29	Read Data 5 (IRD5)
	34	33	Read Data 6 (IRD6)
	36	35	Read Data 7 (IRD7)
XJ101 - XP101A	1	2	Load and On Line (ILOL)
	17	18	Select 0 (ISLT0)

Table 3-2. Transport/Formatter Interface Connections

CONNECTOR	LIVE PIN	GROUND PIN	SIGNAL
XJ101 - XP101A	19	20	Select 1 (ISLT1)
	21	22	Select 2 (ISLT2)
	23	24	Select 3 (ISLT3)
	5	6	Synchronous Forward Command (ISFC)
	9	10	Synchronous Reverse Command (ISRC)
	13	14	Rewind Command (IRWC)
	11	12	Off-Line Command (IOFFC)
	15	16	Set Write Status (ISWS)
(XJ101 only)	39	See Table 3-3	(IWARS) (JUMPER OPTION)
	3	4	Overwrite (IOVW)
	7	8	Data Density Select (IDDS)
J102 - XP102A	11	12	Read Threshold 2 (IRTH2)
	9	10	Read Threshold 1 (IRTH1)
	5	6	Write Amplifier Reset (IWARS)
	1	2	Write Data Strobe (IWDS)
	19	20	Write Data Parity (IWDP)
	21	22	Write Data 0 (IWD0)
	23	24	Write Data 1 (IWD1)
	25	26	Write Data 2 (IWD2)
	27	28	Write Data 3 (IWD3)
	29	30	Write Data 4 (IWD4)
	31	32	Write Data 5 (IWD5)

Table 3-2. Transport/Formatter Interface Connections (Continued)

CONNECTOR	LIVE PIN	GROUND PIN	SIGNAL
J102 - XP102A	33	34	Write Data 6 (IWD6)
	35	36	Write Data 7 (IWD7)

Table 3-2. Transport/Formatter Interface Connections (Continued)

+5 VOLTS		GROUND	
Connector	Pin	Connector	Pin
XJ101	26	XP101A	26
	28		28
	30		30
	32		32
	34		34
	36		36
	38		38
	40		
XP101A	39		
	40		
XP102A	39	XP102A	37
	40		38

Table 3-3. Plus 5-volt Power Connections

FORMATTER INTERFACING

3-3. The formatter is designed so that any two Cipher formatters may be daisy-chained on the formatter/controller interface.

3-4. All interface lines are low-true at the interface, with the true level being less than 0.8V and the false level being greater than 2.4V. All pulses widths must be at least 1 microsecond.

INTERFACE INPUTS (CONTROLLER TO FORMATTER)

3-5. Formatter Address (IFAD). This is a level which selects one of two possible formatters. A true level on the IFAD line selects formatter address 1; a false level selects formatter address 0. The formatter address is determined by switch S1-4: in OFF position, formatter address is 0; in ON position, formatter address is 1.

3-6. Transport Address (ITAD0, ITAD1). The levels on these two lines determine which of the four possible transports is connected to the formatter. These lines are decoded by the formatter/transport interface. See Table 3-4.

3-7. Initiate Command (IGO). This is a pulse which initiates the command specified by the command lines. The information on the command lines is copied into the corresponding formatter flip-flops on the trailing edge of the IGO pulse. If the formatter and the selected transport are ready, the command is accepted by the formatter, and the IFBY signal is set true.

ITAD0	ITAD1	ADDR
0	0	SLT0
0	1	SLT1
1	0	SLT2
1	1	SLT3

Table 3-4. Transport Addressing

3-8. Command Lines. The levels on these lines specify commands to the formatter. The levels on the command lines are transferred to the formatter on the trailing edge of the IGO pulse. The levels must be held steady from 0.5 microsecond before to 0.5 microsecond after the trailing edge of IGO. Table 4-1 defines the command coding for various tape operations.

a. Reverse (IREV). This is a level which, when true, specifies reverse tape motion and when false, specifies forward tape motion.

b. Write (IWRT). This is a level which, when true, specifies the write mode of operation and when false, specifies the read mode of operation.

c. Write File Mark (IWFM). This is a level which, when true and IWRT is also true, causes a file mark to be written on the tape. When this level is true and IWRT is false, a file search is initiated. The operation terminates when a file mark is detected or if load point is encountered in reverse. Read data will also be available during the operation.

d. EDIT (IEDIT). This is a level which, when true during a read reverse operation, modifies the read reverse stop delay to optimize head positioning for a subsequent edit operation. When this level is true and IWRT is true, the IOVW line is activated, and the selected transport operates in the edit mode.

e. ERASE (IERASE). This is a level which, when true in conjunction with a true level in the IWRT line, causes the formatter to execute a dummy write command. The formatter will be conditioned to execute a normal write command but no data will be recorded. A length of tape, as defined by ILWD, will be erased. Alternately, if IERASE, IWRT, and IWFM command lines are true, the formatter is conditioned to execute a dummy write file mark command. A fixed length of tape approximately 3.75 inches will be erased.

f. Read Threshold Level 2 (ITHR2). The levels on this line are utilized in transports with extra low read threshold capabilities. When true, the extra low threshold is specified, and when false, the normal threshold is specified. The true level should be used only when it is required to recover data of very low amplitude.

g. Read Threshold Level 1 (ITHR1). The levels on this line are utilized only in transports with single-gap heads to specify the operating level of the read threshold circuits. A true level specifies selection of the high read threshold level, and a false level specifies the normal read threshold. The true level is normally used only when it is required to perform a read-after-write data check.

h. Density Select (IDEN) (Optional - Seven-Track). When the external density select option is incorporated in seven-channel transports, the levels on this line control the packing density of data transfers to and from tape. This level, when true, selects the lower of two possible packing densities. When false, the higher packing density is selected.

i. Parity Select (IPAR). The levels on this line are effective only for seven-channel transports. They control the parity mode for write and read data transfers. When true, this level selects the even (BCD) parity mode. When false, it selects the odd (binary) parity mode.

3-9. Rewind (IREW). This is a pulse which causes the selected transport to rewind to the load point. This pulse is routed directly to the transport and does not cause the formatter to go busy.

3-10. Off-line Command (IOFL-IRWU). This is a pulse which causes the selected transport to revert to the off-line mode. Depending on the tape transport configuration, this line will also cause the selected transport to rewind and unload. This pulse is routed directly to the transport and does not cause the formatter to go busy.

NOTE

Current Cipher transports are not equipped with the IRWU option.

3-11. Last Word (ILWD). This is a level which, when true during a WRITE or ERASE (variable-length) command, indicates that the next character to be strobed into the formatter is the last character of the record. It is set true by the controller at the time the last data character of the record is placed on the interface lines.

3-12. Formatter Enable (IFEN). This is a level which, when false, causes the formatter to reset to the quiescent state. This signal is not gated by FAD; hence, if two formatters are connected to the interface, both will reset simultaneously upon receipt of a false-going IFEN level. This line may be used to disable the formatter if controller power is lost, or to clear the formatter logic in the case of illegal commands or unusual conditions.

3-13. Write Data Lines, Write Parity (IW0-IW7, IWP). The eight Write Data lines are utilized to transmit write data from the controller to the formatter. IW0 corresponds to the most significant bit and IW7 to the least significant bit of each character.

3-14. For nine-channel operation, the eight data bits appearing on W0-7 are written onto the corresponding channels on tape. For seven-channel operation, W0 and W1 are not utilized and the remaining six data bits are written onto tape. In either case, W7 corresponds to the least significant bit of the character. Line WP is optional and is used only if it is required to write the parity bit specified by the customer. When this option is not employed, the formatter generates parity internally on the basis of data contained on W0-7, together with the current parity mode.

3-15. The first character of a record should be available on these lines a minimum of one-half cell time before the first IWSTR and remain until the trailing edge of the first IWSTR is issued by the formatter. The next character of information must then be placed on these lines within one-half a character period. Subsequent characters of a record are processed in this manner, until ILWD is set true by the controller when the last character is transmitted.

3-16. Load and On-Line (ILOL). This is a pulse which causes a remote load sequence. A second pulse, spaced a minimum 1 second from the initial pulse, causes the transport to be placed on line. This pulse is routed directly to the transport interface and may be used only on transports equipped with this option.

NOTE

Current Cipher transports are not equipped with this option.

INTERFACE OUTPUTS (FORMATTER TO CONTROLLER)

3-17. Formatter Busy (IFBY). This level is normally utilized by the controller to inhibit further commands to the formatter. The level goes true on the trailing edge of the IGO when a command is issued by the controller and will remain true until tape motion ceases after the execution of the command.

3-18. Data Busy (IDBY). This is a level which goes true when the tape on the selected transport has reached operating speed and traversed the IBG, and the formatter is about to write a preamble on the tape or look for a read signal from the tape. IDBY remains true until the data transfer is completed and the appropriate postrecord delay is completed. IDBY goes false as the capstan starts to decelerate the tape.

3-19. Identification/Check Character Gate (IIDENT/ICCG). The functions of this line differ depending upon mode of operation. These functions are described for PE and NRZI mode in paragraphs 3-20 and 3-21, respectively.

3-20. PE Mode. This is a level which goes true to identify phase-encoded (PE) tapes. When reading forward off of the BOT, the formatter inspects the parity channel for the presence or absence of the identification burst, which distinguishes PE tapes. If an identification burst is detected, this line is set true for a short period as the BOT tab passes over the read head.

3-21. NRZI Mode. This level is set true by the formatter when the read information being transmitted to the controller is a cyclic redundancy check character (CRCC) or a longitudinal redundancy check character (LRCC). It is false when data characters are being transmitted. Data and check information can be distinguished by gating read strobe (RSTR) with CCG or its inverse.

3-22. Hard Error (IHER). This is a pulse or level which, when true, indicates that an uncorrectable read error has been detected by the formatter. When the ERASE command is given to the formatter, the IHER line is disabled. In NRZI mode, this line will be set true for one or more of the following:

a. Vertical parity error on data character.

b. Longitudinal parity error.

c. CRCC parity error.

d. Improper record format.

e. CRC error.

3-23. In the case of a vertical parity error, the HER line will be pulsed at the time that the read strobe (RSTR pulse) is issued for the character in error. In all other cases, HER will be pulsed after the complete record has been read. All error information will be transferred to the controller before Data Busy (DBY) goes false. In PE mode, IHER is true for one or more of the following:

a. False preamble detection.

b. False postamble detection.

c. Multichannel dropout.

d. Parity error without associated channel dropouts.

3-24. In all cases except parity error, the formatter will cease transmission of further read data and search for the IBG. When a parity error is detected, the erroneous character will be transmitted and labeled by a pulse on the IHER line at RSTR time.

3-25. Corrected Error (ICER) (PE Only). This is a pulse which indicates that a single-track dropout has been detected and that the formatter is performing error correction. When the ERASE command is given to the formatter, the ICER line is disabled.

NOTE

When a read-after-write operation is being performed, the record should be rewritten if either a HER or CER error is detected.

3-26. File Mark (IFMK). This is a pulse which indicates that the formatter read logic has detected a file mark. This may be during any READ FORWARD or READ REVERSE command, or during a WRITE FILE MARK command for a read-after-write transport.

3-27. Transport Status. These lines indicate the status of the selected transport and are defined exactly the same as in the interface inputs description. Status lines are as follows: IRDY, IONL, IRWD, IFPT, ILDP, IEOT, INRZ, ISGL, ISPEED, and I7TR.

3-28. Write Strobe (IWSTR). This is a pulse for each data character to be written on the tape. The write data lines (IWP, IW0-IW7) are sampled by IWSTR and are copied character by character into the formatter write logic. The first character must be available before the first IWSTR is generated, and subsequent characters must be set up on the lines within one-half a character period after the trailing edge of each IWSTR pulse. This line will be active during ERASE (variable-length) commands, but data copied into the formatter will have no meaning.

3-29. Read Strobe (IRSTR). This is a pulse which indicates that a read character is present on the controller interface. The read strobes will have the same period as the write data over long-term data transfers. However, due to skew and velocity changes, the instantaneous rate may vary. The controller logic must sample the Read Data lines (IRP, IR0-IR7) at RSTR time. Read strobes (IRSTR) are disabled if the ERASE command is specified. The transmission of check characters (CRC and LRC) is flagged by the check character gate line (ICCG).

3-30. Read Data Lines (IRP, IR0-IR7). The nine read data lines transmit read data from the formatter to the controller. Each character read from the tape is availabe by sampling these lines in parallel by RSTR. Data remains on IRP, IR0-IR7 for a full character period. The corresponding IRSTR pulse is one-third of a character period wide and is timed to occur during the center of each character period.

INTERFACE OUTPUTS (FORMATTER TO TRANSPORT)

3-31. Transport Select Lines (ISLT0-ISLT3). The levels of these four lines are utilized to select one transport from the possible four. The levels are generated in the formatter by decoding address lines ITAD0 and ITAD1. Only one line can be true at a time. When a transport is selected all interface lines to and from the transport are activated, and the transport is connected to the formatter.

3-32. Synchronous Forward Command (ISFC). This is a level which, when true and the selected transport is ready and on line, causes the tape to move in the forward direction at the specifed speed. When the level goes false, tape motion ceases.

3-33. Synchronous Reverse Command (ISRC). This is a level which, when true and the selected transport is ready and on-line, causes the tape to move in the reverse direction at the specified speed. When the level goes false, tape motion ceases.

3-34. Rewind Command (IRWC). This is a pulse which, if the selected transport is ready and on-line, causes the transport to rewind to BOT.

3-35. Off-Line Command (IOFC). This is a pulse which places the selected transport under local control. An off-line command can be given while a rewind is in progress, provided IOFC is separated by at least 1 microsecond from IRWC.

3-36. Set Write Status (ISWS). The level on this line is the output of a flip-flop within the formatter which identifies the read/write status specified in the last command. The level on this line controls the selected transport's read/write electronics. When this level is set true, it causes the selected transport to enter the write mode of operation. When this level is false, the transport will enter the read mode of operation.

3-37. Regardless of the state of the ISWS line, the transport will be forced into the read mode of operation under any one of the following conditions:

a. An RWC or OFC is received.

b. Transport is switched to the off-line mode.

3-38. Overwrite (IOVW). This is a level which, when true, causes special action in the write electronics of the selected transport to facilitate the editing of tapes. The level is the output of a flip-flop in the formatter logic which stores the condition edit as specified in the last command.

3-39. Read Threshold 2 (IRTH2). The level on this line is the output of a flip-flop within the formatter which stores the condition of IRTH2 specified in the last command. The output on this line is used only by transports which have extra low read threshold capabilities. When this level is true, the read electronics of the selected transport are conditioned to operate in the extra low read threshold mode. When false, the transport reverts to the normal read threshold.

3-40. Read Threshold 1 (IRTH1). The level on this line is the output of a flip-flop within the formatter which stored the condition of ITHR1 specified in the last command. When this level is true and the transport has a single-gap head, the read electronics of the transport are conditioned to operate in the high read threshold mode. When false, the transport reverts to the normal read threshold.

3-41. Write Amplifier Reset (IWARS). This pulse occurs at the end of a write operation. In NRZI mode it causes the LRC character to be written onto tape. In nine-channel NRZI systems, WARS occurs four character periods after the CRC character is written. In seven-channel NRZI systems, WARS occurs four character periods after the last data character is written. In phase-encode mode the WARS pulse occurs immediately following the last character of the postamble during all write operations.

3-42. The leading edge of the IWARS pulse resets the write register in the selected transport at the end of skew delays. This reset action causes all channels to be erased in a uniform direction in the inter-record gap (IRG). Additionally, the WARS pulse is utilized to control the early turn-off of write current during edit operations.

3-43. Write Data Strobe (IWDS). In NRZI mode, this is a pulse for each data character to be written onto tape. In PE operation the frequency of the WDS pulse is twice that of the data transfer rate. The trailing edge of each WDS pulse is utilized to copy data appearing on WDP, WD0-WD7 into the write register in the selected transport logic. The formatter logic holds WDP, WD0-7 steady for the duration of each WDS.

3-44. In nine-channel NRZI systems, the CRC character is written by an additional WDS pulse. This WDS pulse occurs four character periods after the last data character has been written. The appropriate CRC data on WDP, WD0-7 accompanies this pulse.

3-45. Write Data (IWDP, IWD0-IWD7). These nine lines are utilized to transfer the phase-encoded data from the formatter to the selected transport. The information is copied on the edge of each IWDS pulse into the selected transport write logic and written directly onto the tape.

3-46. Data Density Select (IDDS - Optional). The level on this line is the output of a flip-flop in the formatter which stores the condition of DEN as specified in the last command. The levels on this line control the packing density of data transfers to and from tape. IDDS is routed to the Density Indicator line (IDDI). When used with a NRZI, seven-channel transport, a true level on this line selects the lower of two possible packing densities, a false level, the high of the two. When used with a dual-mode transport, the true level selects NRZI and the false level selects PE.

3-47. Load and On Line (ILOL). This signal is described in paragraph 3-16 as a controller-to-formatter input.

INTERFACE INPUTS (TRANSPORT TO FORMATTER).

3-48. Ready (IRDY). This is a level which is true only when the transport is ready to receive external commands. The following conditions must exist:

a. Initial load or rewind sequence is complete.

b. Transport is on line.

c. Transport is not rewinding.

3-49. On Line (IONL). This is a level which, when true, indicates that the selected transport is under remote control. This level is false when the transport is off line and cannot be operated remotely.

3-50. Rewinding (IRWD). This is a level which is true when the selected transport is engaged in a rewind operation.

3-51. File Protect (IFPT). This is a level which is true when the transport power is on and a reel of tape without a write enable ring is mounted on the transport.

3-52. Load Point (ILDP). This is a level which is true when the BOT tab is located under the photo-tab sensor. The ILDP level goes false when the tab leaves the photo-tab sensor.

3-53. End of Tape (IEOT). This is a level which, when true, indicates that the EOT reflective tab is positioned under the photo-tab sensor. This level is not staticized, and transitions to and from the true state are not necessarily clean.

3-54. Data Density Indicator (IDDI). The levels on this line are relevant only to seven-channel systems. They select either the high or low-density mode of operation for both transport and formatter. When true, the high-density mode is selected; when false, the low-density mode is selected. DDI is normally controlled by the density select switch (HI DEN) located on the selected transport. Alternatively, if the selected transport contains the external density select option, density selection may be controlled from the customer's equipment via the DEN and DDS interface lines.

3-55. NRZI (INRZ). This is a level which, when true, indicates that the transport is of the NRZI type. When false, this level indicates that the transport is of the PE type. When the level on this line is true, the PE circuitry is disabled. When the level is false, the NRZI circuitry is disabled.

3-56. Seven-Track (I7TR). This level, when true, indicates that a seven-channel transport has been selected. When false, it indicates that a nine-channel transport has been selected. This line also forces the formatter to the NRZI mode of operation.

3-57. Single (ISGL). This level, when true, indicates that the selected transport has a single-gap read/write head. When false, the level indicates that the selected transport has a dual-gap read-after-write head. The levels on this line condition the formatter to generate appropriate delays for the generation of the IRG and for head positioning.

3-58. Speed (ISPEED). This line is used when it is desired to attach transports of two different tape speeds to the formatter. When false, it indicates the selected transport is a high-speed unit; when true, it indicates the selected transport is a low speed one.

3-59. Read Data Strobe (IRDS) (NRZI Only). This pulse is generated for each character of information read from tape on the selected transport. The formatter logic samples read data appearing on RDP, RD0-7 on the trailing edge of each RDS pulse.

3-60. Read Data Lines (IRDP, IRD0-IRD7). The nine read data lines are employed to transmit read data from the selected transport to the formatter. In NRZI mode, each character of information is identified by a pulse on the RDS line and is copied into the formatter logic on the trailing edge of RDS.

3-61. In PE mode, these lines are the outputs of nine peak detectors, individually gated with the output of a threshold detector associated with each channel. The read signals are replicas of the PE waveforms used to drive the write amplifiers.

SECTION IV

OPERATION

BASIC OPERATION

4-1. The formatter is capable of executing the commands listed in Table 4-1. When a command is received from the customer's controller, the formatter "goes busy" and performs all control and timing functions necessary to execute the command. Any errors occuring during execution of the command are reported to the controller. On completion of the command execution, the formatter signals the controller, and the controller is then free to issue a further command. Two other command lines, which cause the transport to rewind or to be switched off line, are provided. These commands are routed directly to the selected transport and do not cause the formatter to go busy.

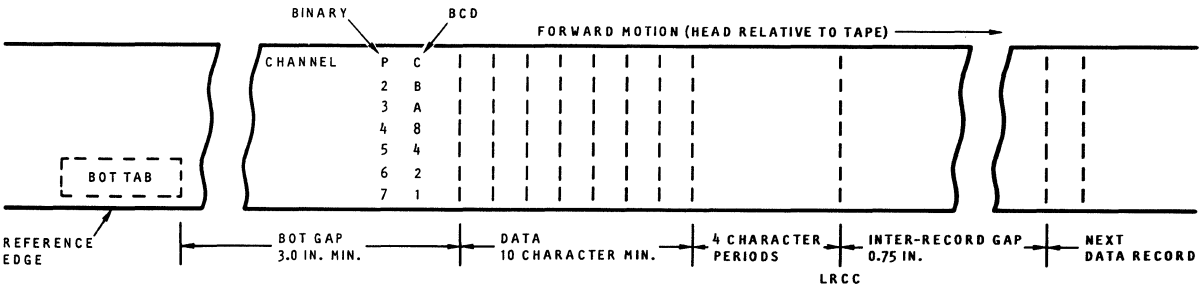
4-2. An automatic read-after-write data check is performed during each WRITE command for transports with dual-gap heads. Read-after-write data is transmitted to the controller in the same manner as during READ commands. NRZI seven- and nine-channel tape formats are illustrated in Figures 4-1 and 4-2, respectively, and Figure 4-3 illustrates the nine-track PE tape format.

NRZI MODE

4-3. Operations performed by the formatter in the NRZI mode are described in the subparagraphs hereof.

4-4. Gap Generation. The formatter provides all timing necessary for generation of the following gaps for nine- and seven-channel tape formats:

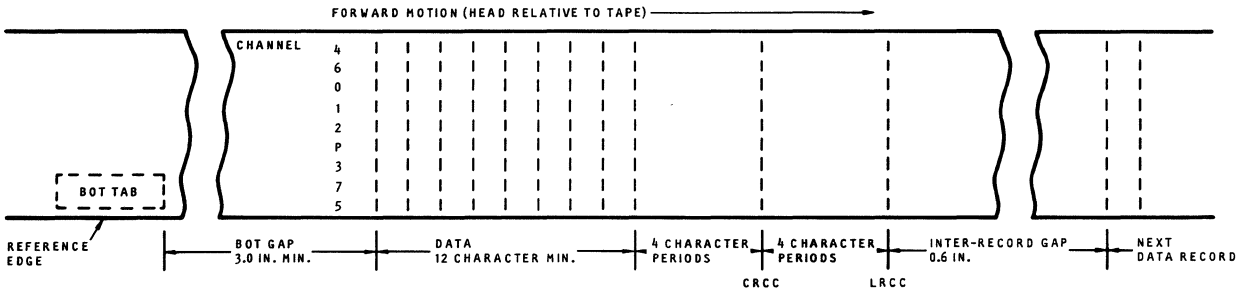
a. Interblock gap: a gap between each record with a nominal length on a nine-channel tape of 0.6 inch (minimum, 0.5 inch); on a seven-channel tape, 0.75 inch (minimum, 0.68 inch). Maximum interblock gap length depends on the number of consecutive erasures and is not limited by the formatter.



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) CONTAINS ODD DATA PARITY FOR BINARY TAPES, OR EVEN PARITY FOR BCD TAPES.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE LRCC) IS EVEN. IT IS POSSIBLE IN THE 7-TRACK FORMAT FOR THIS CHARACTER TO BE ALL ZEROS, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
5. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 4, 5, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS AND BY A NORMAL IRG (0.75 IN.) FROM THE FOLLOWING RECORD.
6. DATA PACKING DENSITY MAY BE 200, 256, OR 800 BITS PER INCH.

Figure 4-1. Seven-Track NRZI Format



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 5 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRCC AND LRCC) IS EVEN. IN THE 9-TRACK FORMAT THE LRCC WILL NEVER BE AN ALL-ZEROS CHARACTER.
5. IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL ZEROS, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL ZEROS. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.6 IN.) FROM THE FOLLOWING RECORD.
7. DATA PACKING DENSITY IS FIXED AT 800 BITS PER INCH.

Figure 4-2. Nine-Track NRZI Format

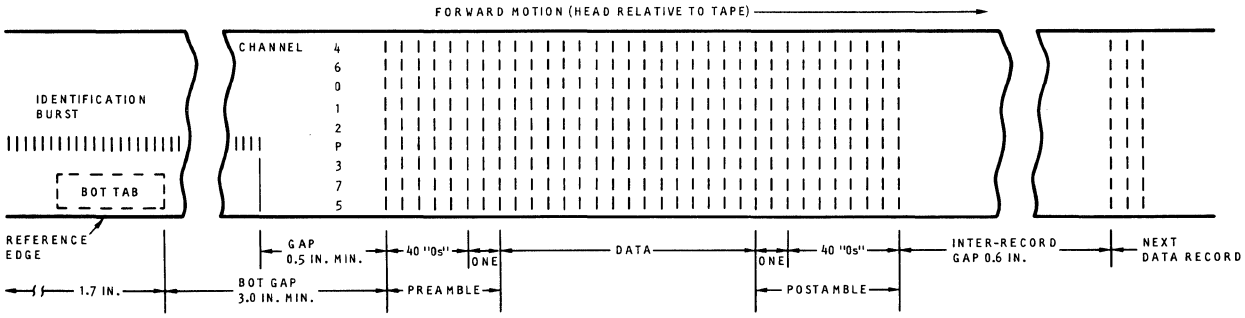


Figure 4-3. Nine-Track PE Tape Format

b. Initial gap: a gap preceding the writing of the first data character of the first record from BOT, extending approximately 3.5 inches past the trailing edge of the BOT tab.

c. File mark gap: a gap of approximately 3.5 inches of tape preceding the file mark. The file mark is followed by a normal IBG.

REV	WRT	WFM	EDIT	ERASE	COMMAND
0	0	0	0	0	Read Forward
1	0	0	0	0	Read Reverse
1	0	0	1	1	Read Reverse Edit
0	1	0	0	0	Write
0	1	0	1	0	Write Edit
0	1	1	0	0	Write File Mark
0	1	0	0	1	Erase Variable Length
0	1	1	0	1	Erase Fixed Length
0	0	0	0	1	Space Forward
1	0	0	0	1	Space Reverse
0	0	1	0	0	File Search Forward
1	0	1	0	0	File Search Reverse
0	0	1	0	1	File Search Forward (ignore data)
1	0	1	0	1	File Search Reverse (ignore data)

1 = true 0 = false

Table 4-1. Command Coding

4-5. Writing. During a write operation, the formatter controls the transfer of write data from the controller to the selected transport. The data transfer rate is a function of the tape speed and the data packing density. The CRC and LRC check characters are generated internally by the formatter and are inserted automatically at the end of the record.

4-6. Reading. During reading, data is transferred character by character from the transport to the formatter. The formatter separates data and check characters, performs various error checks, and retransmits the information to the controller via nine data lines and a strobe line, RSTR. Both the data and check characters are identified by a special interface line (CCG), which is true when the check characters are being transmitted.

NOTE

Under certain circumstances, the CRC or LRC character may not exist on tape (all 0's character). In this case, no character (or associated RSTR pulse) will be transmitted to the controller.

4-7. File Mark. When executing a Write File Mark (WFM) command, the formatter automatically generates the appropriate file mark patterns to record onto tape. During any read operation (read forward, read reverse, or read-after-write), the formatter tests for the presence of the file mark pattern. When this is detected, the FMK interface line to the controller is pulsed. In addition, the file mark characters read from tape are transmitted to the controller. When reading in a forward direction, the first character is transmitted as a data character (CCG false), and the second is transmitted as a check character (CCG true). When reading is in reverse, the two characters are reversed.

4-8. In the case of seven-channel operations in the binary (odd parity) mode, the file mark data character (0001111) has "incorrect" parity, and a data parity error (HER) is signalled to the controller. The controller should therefore be designed to ignore error conditions when a file mark is detected.

4-9. Parity. For nine-channel operation, all data transfers take place in the odd parity mode. For seven-channel operation, data parity may either be odd (binary mode) or even (BCD mode) and is selected by the controller via interface line IPAR.

4-10. When writing, the formatter generates the appropriate parity bit from the data present on the eight data lines. A switch option which allows the parity bit to be supplied externally by the controller is provided. In a read operation, the data received from the transport is checked for parity.

4-11. Density Selection. In nine-channel operation, all data transfers take place at a data packing density of 800 bpi. In seven-channel operation, the formatter can perform data transfers at either of two of the three possible packing densities of 800, 556, and 200 cpi. A seven-track machine must not be used as the host transport. The desired density combination (800/556, 800/200) must be identical for both formatter and transport.

4-12. The current density (high or low) can be controlled by a density select switch (HI DEN) on the front panel of the selected transport. When the switch is illuminated, the formatter is conditioned to operate in the high-density mode.

4-13. As an alternative to this, an optional feature in the transport logic permits selection of the current operating density by the controller via the interface line, IDEN.

4-14. BCD Zero Conversion. In the seven-channel BCD (even parity) mode, an all-0's character is invalid. In this mode, the formatter detects the presence of an all-0's character from the controller and automatically substitutes a BCD ten (001010) character.

4-15. Error Checking. During any read operation (read forward, read reverse, or read-after-write) the formatter performs the following checks:

a. Vertical parity check on each data character.

b. Vertical parity check on CRC character.

c. Longitudinal parity check.

d. Improper record format.

e. CRC check.

4-16. Options. The following options are available:

a. Formatter address: 0 or 1.

b. Internal or external write parity generation.

c. Seven-channel density combinations.

PHASE-ENCODE MODE

4-17. Operations performed by the formatter in the PE mode are described in the subparagraphs hereof.

4-18. Identification Burst (Figure 4-3). When performing any write operation from BOT, the formatter automatically writes an IBM-compatible identification mark on the tape. This mark consists of a series of flux reversals at 1600 cpi in channel P, with all other channels erased. Three inches of tape are then erased before the first block of data is written.

4-19. When reading from BOT, the formatter samples the output of the parity track. If the identification mark is found, the IDENT line is pulsed.

4-20. Preamble. When writing, the formatter generates a preamble which precedes the data field of the record. The preamble consists of 40 zero bits, followed by a one bit, recorded in each of the nine tracks.

4-21. Postamble. A postamble is written following the data field of the record. The postamble also consists of 40 zero characters preceded by a one character in each of the nine tracks. When reading, the formatter separates the preamble and postamble from the data.

4-22. Data. When writing, the formatter accepts data character by character and converts it into a phase-encoded signal in which the following conditions exist:

a. A 0 bit is characterized as a flux transition in the middle of the bit cell away from the erase direction of magnetization.

b. A 1 bit is characterized by a transition in the middle of the bit cell toward the erase direction of magnetization.

4-23. File Mark. When in the write mode of operation the formater generates the IBM/ANSI-compatible file mark, preceded by a long (3.5 inches) gap of erased tape. With the formatter in the read mode, the compatible file mark is detected and verified by the file mark status line (IFMK).

4-24. Gaps. The formatter provides the timing required to generate the following gaps:

a. Interblock gap (IRG): a gap with a nominal length of 0.6 inch written between each record.

b. Initial gap: when writing from BOT, an identification burst, followed by a 3-inch gap, written before the first record.

c. File mark gap: a gap of approximately 3.75 inches preceding a file mark.

4-25. All gaps are written by saturating the tape in the erase direction of magnetization.

4-26. Parity. During a write operation, the formatter generates odd parity derived from the data present on the eight data channels. When reading, the formatter checks that the parity of the nine tracks is odd. An error is signaled when the parity check fails.

4-27. Dropout and Error Correction. The formatter provides single and multiple-track dropout detection. When a single-track dropout occurs, the formatter corrects the data by the use of the data in the other seven tracks and the parity bits. A status line to the controller indicates when error correction is taking place. After a dropout has been detected, the output of the affected track will be ignored, and no attempt will be made to resynchronize the discriminators of that track.

SECTION V

DETAILED ELECTRICAL AND LOGIC DESCRIPTION

INTRODUCTION

5-1. This section consists of a detailed description of the formatter logic operation. Relevant schematic and assembly drawings are presented at the end of Section VII. Reference should also be made to Section IV for a discussion of the block diagram level. Before proceeding, it will be useful to list some of the conventions that have been adopted concerning waveform names, logic levels, and logic symbols.

INTERNAL FORMATTER SIGNALS

5-2. The formatter logic levels are 0 volts and +4 volts (approximately). The basic waveform names within the formatter have been chosen to correspond to the high-true condition (e.g., the waveform WRT is at +4 volts when writing and at 0 volts when not writing). (See Table 5-1 for detailed descriptions of all waveforms and mnemonics.) The inverse waveform (low-true equivalent) usually retains the same basic name but has an asterisk preceding the mnemonic (e.g., WRT, *WRT). Logic signals which perform gating functions are identifed at the gate in the form which will satisfy the gate logic.

INTERFACE SIGNALS

5-3. All signals on the controller/formatter and formatter/transport interfaces are low-true, with signal levels of +3 volts for false and 0 volts for true. The false level of +3 volts is determined by a 220/330-ohm resistor chain which terminates each line at the receiver end. Interface waveform names are always prefixed by the letter "I", e.g., IWRT.

LOGIC ELEMENTS AND SYMBOLS

5-4. The formatter logic is designed primarily around the low-power Schottky TTL series of integrated circuit (IC) elements. The ICs on the PWB are in a grid array, with each location identified by row (letter) and column (number). The symbol for each logic element includes the appropriate U number and identifies each input and output pin. The device type is listed as well. Two different types of gating elements are employed: the high-true NAND and the high-true NOR. Both types consist of a gating function followed by an inversion.

WAVEFORM MNEMONICS	FUNCTION
BDDLY (Block Detect Delay) (Sheet 25, Drawing No. 360001-300)	Pulse which initiates BLKDET after ENV has remained true for four character periods or terminates BLKDET after ENV is lost for four character periods.
BGNPRMBL (Begin Preamble) (Sheet 27)	Indicates data being read is first of preamble. Also enables file mark detector.
BLKDET (Block Detect) (Sheet 25)	Indicates data envelope has been detected.
BOBPLS (Beginning of Block Pulse) (Sheet 25)	Pulse occuring on rising edge of BLKDET. Initiates block format control logic.
CHARGATE (Character Gate) (Sheets 19 and 24)	Distinguishes data transitions from phase transitions. When true, indicates next transition should be data bit. After data transition, CHARGATE will be set false for three quarters of the bit cell time.
CCDLY (Check Character Delay) (Sheet 6)	This signal causes a four-character delay before writing of a check character.
CCE (Check Character Error) (Sheet 15)	Signifies that an additional character was detected following the check characters.
CCG (Check Character Gate) (Sheet 15)	This line goes true whenever a check character is being transmitted to the controller.
CDP (Character Detect Pulse) (Sheet 14)	A pulse generated each time a NRZ character has been detected.
CHDDROP (P, 0-7) (Channel Drop) (Parity, 0-7) (Sheets 16-24)	Indicates channel has been dropped (i.e., data transition did not occur within specified time). Once set true, will remain true for entire record.
CHNBIT (0-3) (Channel Bit) (0-3) (Sheet 26)	These four bits are used to time-multiplex nine data channels
CHNDROP (Channel Drop) (Sheet 26)	Time-multiplexed channel drop signal derived from CHDDROP (P, 0-7).
CHPLS (Character Pulse) (Sheet 27)	Pulse occurring at character frequency. Used to increment block delay counter.

Table 5-1. Formatter Signals, Functions, and Mnemonics

WAVEFORM MNEMONICS	FUNCTION
CIR (Clear Input Register) (Sheet 14)	This signal clears the input register after a character has been loaded into the output register.
COR (Clear Output Registers) (Sheet 15)	This signal clears the output registers at the end of a NRZI read operation.
CRCE (CRC Enable) (Sheet 6)	When true, conditions the write logic to write the CRC character.
CRCPE (CRC Parity Error) (Sheet 15)	Signifies that a parity error has occurred in the CRC character.
CRCER (CRC Error) (Sheet 15)	Indicates that the computed CRC character did not agree with the CRC character read.
CRCDLY (CRC Delay) (Sheet 6)	A four-character delay before writing of the CRC character.
CRCP, 0-7 (CRC Parity, 0-7) (Sheet 7)	CRC character bits.
DATABSY (Data Busy) (Sheet 4)	Signal indicating data transfer in progress. Set true after prerecord gap. Set false at beginning of postrecord gap.
DATAIN (R1, R2, R3) (Data In) (Registers 1, 2, 3) (Sheet 30)	Serial data entering postamble delay register 1, 2, or 3.
DATAINSB (Data in Skew Buffer (Sheet 29)	Serial data to be entered into skew buffer. Valid only during DATARDY.
DATAOUTSB (Data Out Skew Buffer) (Sheet 29)	Serial data out of skew buffer. Valid only during RDOUTSB.
DATARDY (Data Ready) (Sheet 29)	Indicates that a data bit is ready to be entered into the skew buffer.
DATAXFER (Data Transfer) (Sheet 4)	Indicates data transfer in progress. Set true after prerecord gap. Set false upon completion of RAMPDWN.
DCEQ0 (Drop Channel Equal To Zero) (Sheet 26)	Indicates no channels dropped.
DCEQ1 (Drop Channel Equal to 1) (Sheet 26)	Indicates one channel dropped.

Table 5-1. Formatter Signals, Functions, and Mnemonics (Continued)

WAVEFORM MNEMONICS	FUNCTION
DCGTI (Drop Channel Greater Than I) (Sheet 26)	Indicates more than one channel dropped.
DDATA (P, 0-7) (Detected Data) (Parity, 0-7) (Sheets 16-24)	Indicates data transition has occurred and allows corresponding DDATA line to be entered into skew buffer.
DLYRST (Delay Reset) (Sheet 5)	Pulse issued upon completion of gap count.
EDIT (Edit) (Sheet 31)	Edit command received.
ENDIDTST (End Identification Test) (Sheet 5)	Disables identification burst test.
ENDRD (End Read) (Sheet 27)	Signal indicating read process has been completed and end of block has been detected.
ENV (Envelope) (Sheet 26)	Indicates data envelope has been detected. At least two tracks must be active for this to occur.
EOBPLS (End of Block Pulse) (Sheet 25)	A pulse occurring on trailing edge of BLKDET.
EOBWDW (End of Block Window) (Sheet 27)	This signal prevents EOBPLS from setting format error.
ERASE (Erase) (Sheet 3)	ERASE command received. Valid only during WRITE command.
FMK (File Mark) (Sheet 28)	Indicates valid ANSI/IBM-compatible file mark has been detected.
FMTER (Format Error) (Sheet 27)	Indicates incorrect block format. Will occur for any one of following conditions: character (not all-0's) was detected during the first half of postamble; End of Block pulse occurred at wrong time; preamble too long; more than one track dropped.
GAPTST (Gap Test) (Sheet 27)	Allows ENDRD to be set after 24 character periods.
GER (Gate Error Report) (Sheet 15)	This signal allows a hard error (IHER) to be transmitted to the controller.

Table 5-1. Formatter Signals, Functions and Mnemonics (con't.)

WAVEFORM MNEMONICS	FUNCTION
GFC (Gate Format Check) (Sheet 15)	This signal is set true at the end of the check character and will allow any subsequent character to generate a check character error (CCE).
GO (Go) (Sheet 3)	Buffered signal of IGO.
GOAGN (Go Again) (Sheet 4)	This line is used during a search file command to reissue a GO command after each record until a file mark has been detected.
GO1 (Go 1) (Sheet 4)	Sets FBY true.
GO2 (Go 2) (Sheet 4)	Synchronizes command with CHCK.
HCTP (Half-Character-Time Pulse) (Sheet 15)	A pulse ocurring midway between two characters, forcing the received data from the input registers to the output registers.
ICP (Isolated Character Pulse) (Sheet 14)	Signifies that two character lines have elapsed without character detection.
IDBRST (Identification Burst) (Sheet 5)	Instructs formatter to write ID burst.
IDBDET (Identification Burst Detected) (Sheet 28)	Indicates ID burst has been detected. Occurs when BLKDET is false and parity channel is active.
LONG GAP (Long Gap) (Sheet 4)	Modifies gap counter to generate initial gap and allows an ID burst to be written during write operation.
LRCP, 0-7 (Sheet 15)	LRC character bits generated from read data. This is used to detect LRC errors.
LRCDLY (LRC Delay) (Sheet 6)	A four-character delay before writing of the LRC characters.
LRCE (LRC Error) (Sheet 15)	Indicates a parity error was detected in the LRC.
LWDCLK (Last Word Clock) (Sheet 2)	Clock used to synchronize ILWD.

Table 5-1. Formatter Signals, Functions, and Mnemonics

WAVEFORM MNEMONICS	FUNCTION
LWDS (Last Word Synchronized) (Sheet 6)	LWD synchronized by WRCLK.
MK1DETE (Mark One Detect Enable) (Sheet 25)	Enables PE decoders to detect single all-1's character at end of preamble.
MK2DET (Mark Two Detect) (Sheet 28)	Indicates all-1's character at beginning of postamble has been detected. Signal sets RDDATA false.
NFMK (NRZI File Mark) (Sheet 15)	When true, a valid NRZI file mark has been detected.
NRCLK (NRZI Read Clock) (Sheet 2)	Clock used by NRZI read recovery logic.
NRZ (NRZ Status) (Sheet 8)	Buffered INRZ status.
ORXFER (Output Register Transfer) (Sheet 30)	Enables output registers.
PAMBIEN (Preamble 1 Enable) (Sheet 6)	Causes formatter to write all-1's character at end of preamble and beginning of postamble.
PAMB1S (Write Preamble/ Postamble Ones) (Sheet 6)	Causes formatter to write all-1's character.
PAMB0S (Write Preamble/ Postamble Zeros) (Sheet 6)	Causes formatter to write all-0's characters.
PAR (Even Parity) (Sheet 3)	When true, specifies even parity. Used for internal parity generation and for parity error detection.
PARITY (Parity) (Sheet 28)	True condition indicates odd parity detected. Under single-channel dropout conditions, with no parity error, this line is used to generate data for dropped channel.
PARITY ERR (Parity Error) (Sheet 28)	Indicates nonvalid parity condition.
PRMBLTST (Preamble Test) (Sheet 27)	True when over preamble portion of data block.
PSTMBLTST (Postamble Test) (Sheet 27)	True when over postamble portion of data block.

Table 5-1. Formatter Signals, Functions, and Mnemonics (con't.)

WAVEFORMS MNEMONICS	FUNCTION
PSTRECGAP (Postrecord Gap) (Sheet 4)	Used by gap counter to generate postrecord gap at completion of read or write operation.
RAMPDWN (Ramp Down) (Sheet 4)	Goes true at completion of postrecord gap; used by gap counter to generate Ramp Down Delay.
RAMPUP (Ramp Up) (Sheet 4)	Used to gate FWD command onto transport interface lines and allows tape movement. During a write operation, releases "write data format" logic.
RCG (Received Character Gate) (Sheet 15)	When true, at least one data bit has been detected.
RCHCK (Read Character Clock) (Sheet 31)	Clock used at character frequency. Used only in read delay counter.
RDCLK (Read Clock) (Sheet 31)	Clock occurring at 24 times character frequency. This is a master clock used for synchronization of all read logic.
RDDATA (Read Data) (Sheet 27)	Indicates data portion of record being processed.
RDENBL (Read Enable) (Sheet 25)	Signal initiated by write logic to enable read logic.
RDLY (Read Delay) (Sheet 27)	Pulse occurring every 24 character periods during preamble test, postambe test, or gap test.
RDOUTSB (Read Out Skew Buffer) (Sheet 26)	This signal, which is synchronized with SFRM, forces readout of one character from skew buffer.
RDSTRBE (Read Strobe Enable) (Sheet 28)	Signal which allows read data to be presented to controller interface lines. Delayed four character periods from beginning of RDDATA to allow first data character to proceed from skew buffer to data output register.
RDY (Ready) (Sheet 8)	Buffered signal of IRDY.
REND (Read End) (Sheet 15)	Signifies the end of a NRZI read operation.

Table 5-1. Formatter Signals, Functions, and Mnemonics (con't.)

WAVEFORM MNEMONICS	FUNCTION
RESET (Reset) (Sheet 4)	Identical to RESET I but may also be generated by LDP status during a REVERSE command.
RESETI (Reset I) (Sheet 3)	General Reset signal which disables formatter. Generated during initial power-up when IFEN is false, or if IFAD is incorrect.
REV (Reverse) (Sheet 3)	Latched status of IREV.
RP, 0-7 (Read Parity, 0-7) (Sheet 15)	NRZI data bits read from tape.
RSTRB (Read Strobe) (Sheet 14)	Used to generate IRSTR in NRZI. Issued each time a character is to be transferred to the controller.
SBFLL (Skew Buffer Full) (Sheet 29)	Indicates that last location in skew buffer has just been filled. Also sets RDOUTSB at next frame time.
SCH (P, 0-7) (Select Channel) (Parity, 0-7) (Sheet 26)	These lines used to sample data on channels 0 through 7.
SFRM (Select Frame) (Sheet 26)	Function to allow one additional clock period to process information regarding data character (i.e., parity, all-0's character, etc).
SPDCLK (Speed Clock) (Sheet 2)	Clock used by gap counter.
SPEDATA (2, 7) (Synchronized PE Data 2, 7) (Sheets 19 and 24)	These two signals reflect complement of RD2 and 7. Used only for synchronization of tracking oscillator.
SRDOUT (Start Readout) (Sheet 26)	Set true at first frame time after first skew buffer full indication. Initiates RDDATA.
STARTGAP (Start Gap) (Sheet 4)	Used by gap counter to generate prerecord gap.
STRT RD (Start Read) (Sheet 4)	Signal used to generate RDENBL at completion of Start Gap.
TESTIDBRST (Test ID Burst) (Sheet 5)	Gated with IDBRSTDET to generate IIDENT.

Table 5-1. Formatter Signals, Functions, and Mnemonics (con't.)

WAVEFORM MNEMONICS	FUNCTION
VPER (Vertical Parity Error) (Sheet 15)	Signifies that a vertical parity error has been detected.
WDEC0 (Write Data Encode 0) (Sheet 6)	Control signal used by the write data encoder.
WDEC1 (Write Data Encode 1) (Sheet 6)	Control signal used by the write data encoder.
WDP, 0-7 (Write Data Parity, 0-7) (Sheet 7)	Data to be written on tape.
WDSE (Write Data Strobe Enable) (Sheet 6)	Enables IWDS during all WRITE commands except ERASE.
WEND (Write End) (Sheet 6)	Pulse generated on completion of WRITE command. Used only to terminate erase operation.
WFM (Write File Mark) (Sheet 3)	Latched status of IWFM.
WMK1 (Write Mark One) (Sheet 6)	Instructs the formatter to write the all-1's character delimiting the preamble from the data.
WKM2 (Write Mark Two) (Sheet 6)	Instructs the formatter to write the all-1's character delimiting the data from the postamble.
WPSTMZRS (Write Postamble Zeros) (Sheet 6)	Causes 40 all-0 characters to be written during the postamble.
WPRMZRS (Write Preamble Zeros) (Sheet 6)	Causes 40 all-0 characters to be written during the preamble.
WRCLK (Write Clock) (Sheet 2)	Clock used to transfer data to transport.
WRITE (Write) (Sheet 6)	True during preamble, data field, and postamble. Used to enable write data encoder logic.
WRITE 1 (Sheet 6)	Prevents generation of 3200-fci burst during write file mark operation on tracks to be dc erased.
WRT (Write) (Sheet 3)	Latched status of IWRT.

Table 5-1. Formatter Signals, Functions, and Mnemonics (con't.)

WAVEFORM MNEMONICS	FUNCTION
WRTDATA (Sheet 6)	Causes formatter to write data portion of block.
WRTSTRB (Write Strobe) (Sheet 2)	Strobe occurring at character frequency used to generate IWSTR.
W4, W6 (Sheet 7)	Dummy bits to be written when writing a seven-track, all-0's character using even parity
XSITPLS (2, 7) (Transition Pulse) (2, 7) (Sheets 19 and 24)	Pulse occurring for each flux transition prior to MKI detection, after which it will occurr only for data transitions.
ZEROS (Zeros) (Sheet 28)	Will go true whenever 0 is detected in all nine tracks during skew buffer readout.
200 FCI (Sheet 8)	When true, density is 200 bpi.
200/PE (Sheet 8)	Indicates density is either 200 bpi or 1600 bpi. Used as a clock scalar.
200/800 FCI (Sheet 8)	Indicates density is either 200 bpi or 800 bpi. Used as a clock scalar.
556 FCI (Sheet 8)	When true, density is 556 bpi.
800 FCI (Sheet 8)	When true, density is 800 bpi.

Table 5-1. Formater Signals, Functions and Mnemonics (con't.)

NOTE

See also the paragraphs on NAND/NOR gates and J-K flip-flops in the basic manual, Section IV.

5-5. The high-true NAND (e.g., LS7400, LS7420) can be used as a NAND gate for high-true inputs or as a NOR gate for low-true inputs. Similarly, the high-true NOR (e.g., LS7402) can be used as a NOR gate for high-true inputs or as a NAND gate for low-true inputs. The logic symbols shown on the schematic correspond with the logic function that each gate provides in the circuit. Figure 5-1 illustrates the logic symbols for the LS7400 and LS7401 integrated circuits. Further descriptions in this addendum will refer to gates simply as NOR or NAND, without regard to signal polarity. The presence or absence of circles (state indicators) at the gate inputs indicate the element type. Also, when it is necessary to refer to a particular element or to a signal with no waveform name, it will be identified by the appropritate output pin number (e.g., UE5). Other conventions are illustrated in Figure 5-2. A dot at the output is added to indicate an open collector output.

EMBEDDED DUAL-MODE FORMATTER PWB CIRCUIT OPERATION AND DESCRIPTION

5-6. The PWB consists of a logic board containing 260 integrated circuits (ICs). It provides the logic used to read and write both NRZI and PE-encoded data on tape. It also provides the various control and timing functions required by the formatter. Refer to the schematic diagram of the formatter, Drawing No. 360001-300, and Assembly Drawing No. 160001-000, which shows locations of connectors and test points. The formatter performs the following major logic functions:

a. Formatter and Transport address selection.

b. Status and configuration reporting of selected transport to controller.

c. Generation of initial gaps, interrecord gaps, and file mark gaps.

d. Writing of seven-channel NRZI data.

e. Writing of nine-channel NRZI and PE data.

f. Reading of seven-channel NRZI data.

g. Reading of nine-channel NRZI and PE data.

h. Interpretation and storage of various formatter commands.

i. Data buffering.

j. Error detection.

k. Error correction (PE only).

l. File mark generation and detection.

m. NRZI check character generator and detection.

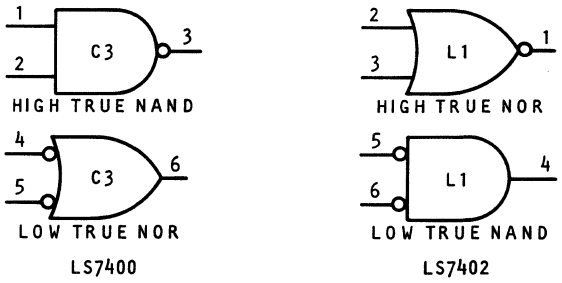


Figure 5-1. Logic Symbols LS7400 and LS7402

Figure 5-2. Logic Symbols, 74LS38 and LS7405

5-7. The formatter printed wiring board (PWB) draws approximately 2.2 amperes from the +5-volt supply.

5-8. Clock Logic. All timing on the dual-mode PWB is controlled by the clocks described in paragraphs 5-13 through 5-16, which are produced by the clock pulse generator as described in paragraphs 5-9 through 5-12.

5-9. Clock Pulse Generator. The clock pulse generator (Sheet 2, Drawing No. 360001-300) produces clocks which are used for gap generation, data encoding, NRZI read decoding, and as a standby frequency reference for phase-encode read. It operates at either of two speeds, which facilitates the daisy-chaining of drives of two different speeds on the tape transport interface.

5-10. The speeds are determined by settings of switches S2 and S3 (Sheet 1 of the schematic and Table 2-1). Since, by convention, the lower speed drive asserts the SPEED line, switch S3 is set to the parameter for high speed and S2 for low.

5-11. Switches S2 and S3 select a crystal clock and a scaling parameter to produce two waveforms which are frequency-proportional to speed: NRCLK, which drives the NRZI read logic, and SPDCLK which drives the gap-generation logic. The frequency of SPDCLK, a square wave, is one-twelfth that of NRCLK, which is a pulse of approximately 50 nanoseconds.

5-12. Waveforms WRCLK, WRTG, WRTSTRB, and WDS control write data encoding. These waveforms, as shown in Figure 5-3, are phase related. The Enable pulses to U3L (74LS379) occur at six times the character rate, as determined by the density scalar consisting of ICs U3N and U3M (74IS161).

5-13. Frequency Lock Clock (Sheet 3). The SPEED line is used to enable one of two voltage-controlled oscillators to generate RDCLK, whose frequency is 24 times the nominal character frequency and is used in the phase-encode read recovery logic. This signal is applied to U12D-2 and U7F-12, which, together with NAND gate U10D, produce a divide-by 24 counter. The output of this counter is applied to pin 3 of phase detectors U6C and U6E, each of which produces positive or negative pulses on pins 5 and 10, depending upon the difference in the two frequencies on pins 1 and 3. These two voltage pulses either add to or subtract from the charges stored in capacitors C1 and C3, thereby increasing or decreasing the voltage at pin 8 of phase detectors U6C and U6E. This voltage is applied to the frequency control input of the selected voltage-control oscillator to increase or decrease its frequency. Thus RDCLK attempts to track at 24 times the reference frequency at pin 1 of the phase detectors.

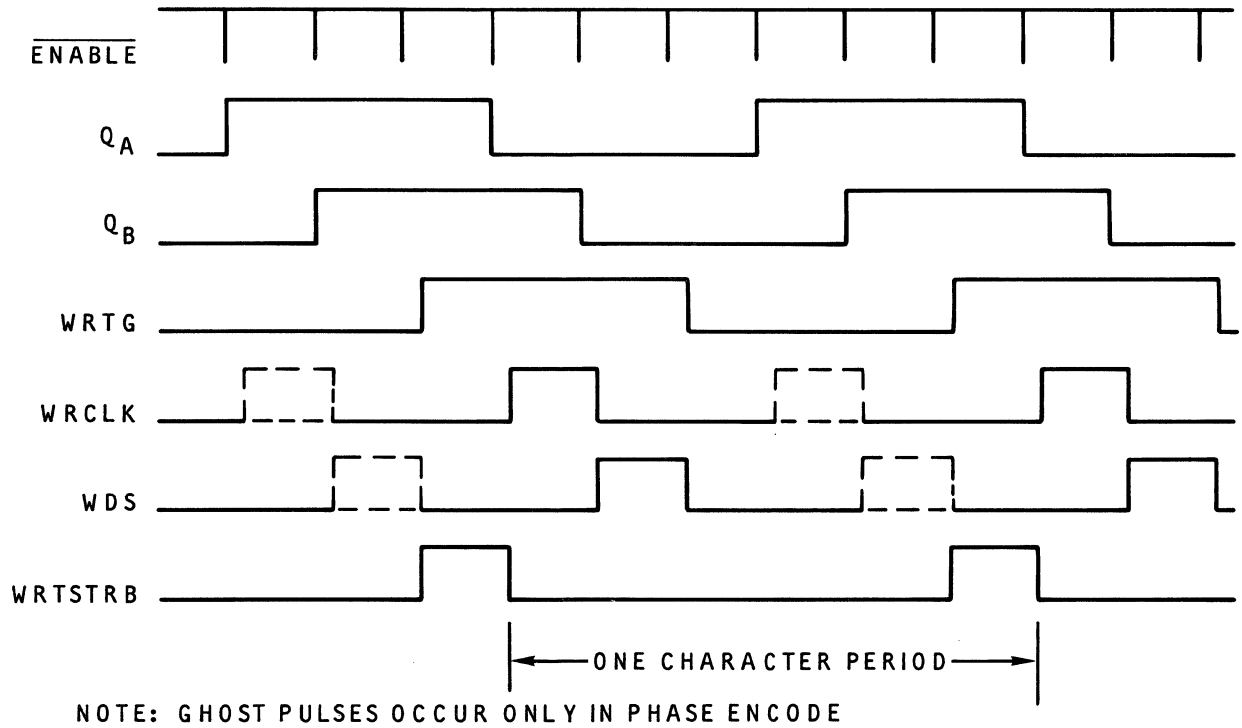


Figure 5-3. Write Encoding Clock Pulses

5-14. For purposes of stability, certain discrete components of the VCO itself are changed, depending upon the speed of the transport to which the formatter is attached. These three or four components are on an eight-pin header socket assembly. Hence, only the header needs to be changed to change the speed of the formatter; no soldering or unsoldering is required.

5-15. The reference frequency at pin 1 of the phase detectors is derived from one of three sources. When no data is being transmitted from the transports, as indicated by a false status of ENV on U6A-3, the reference frequency source is WRTG. When the transport is transmitting read data, ENV on U6A-4 will be true, and the reference

frequency will be derived from U6A-5 as follows: if channel 2 is active, *CHDROP2 is high, and the frequency reference is XSITPLS2 on U6A-10; if channel 2 has been dropped, the frequency reference will be XSITPLS7, on U6A-12. The signals on U6A-11 and -13 are used to discriminate between the phase and data transitions, since the transition pulse occurs at twice the character frequency before mark one is detected rather than at the character frequency.

5-16. Read Character Clock (RCHCK). The clock, the output of U10D-11, is required as a character frequency by both the block format control logic and the block detector logic. Timing relationships of RCDLK and RCHCK are shown in Figure 5-4.

5-17. Command Registers (Sheet 3, Drawing No. 360001-300). These registers sample the controller command inputs when an initiation pulse (IGO) is given and maintain these lines in a static state throughout the command for use by the formatter and the transport.

5-18. The formatter is selected by a comparison of the formatter address line, IFAD, with the setting of switch S1-4. If selected, the formatter asserts one of four drive select lines, ISLT0, ISLT1, ISLT2, or ISLT3, as determined by decoding of the two drive select lines, ITAD0 and ITAD1. Also, if IFEN is asserted, the reset condition will be removed from the formatter.

5-19. Commands are strobed into the registers by the GO1 pulse, which occurs when an initiate command is accepted by the formatter. Reverse is gated with RAMPUP to force the drive to move tape either forward (ISFC) or reverse (ISRC). IRTH1, ISWS, IOVW, and IDDS are the stored equivalents of controller commands ITHR1, IWRT, IEDIT, and IDEN, respectively. Note the polarity reversal between IDEN and IDDS. IDEN is asserted for low density, whereas IDDS is asserted for high density.

5-20. IRTH2 is generally an equivalent of ITHR2, except that it can be asserted by jumper option to force low threshold over the data portion of a phase-encode record. IRWC and IOFFC are processed directly to the transport interface, forcing the selected transport (ISLTi) to rewind or go off line, respectively. Note that some transports interpret the IOFFC command to unload tape in addition to going off line. IPAR is used to select the permissible even parity recording in seven-track mode.

5-21. Gap Control (Sheet 4, Drawing No. 360001-300). This logic conditionally accepts the controller initiate command (IGO) and produces the time delays required to allow the transport to attain speed prior to writing/reading the first data character. It also produces the post-record delay required to ensure ANSI-compatible interrecord gaps as well as for producing the busy status indications to the controller. These time delays are listed in Table 5-2 as functions of tape drive speed. Another purpose of the logic is the generation of additonal initiate commands to effect a search file function.

5-22. The waveform diagram for a write operation from load point in phase encode is shown in Figure 5-5. Note that NRZI (7- and 9-track) has identical waveforms, except that IDBRST and TSTIDBRST are not generated. Read operation is essentially identical to this, with STARTGAP and LONGGAP being approximately one-fourth as long as indicated in Table 5-2.

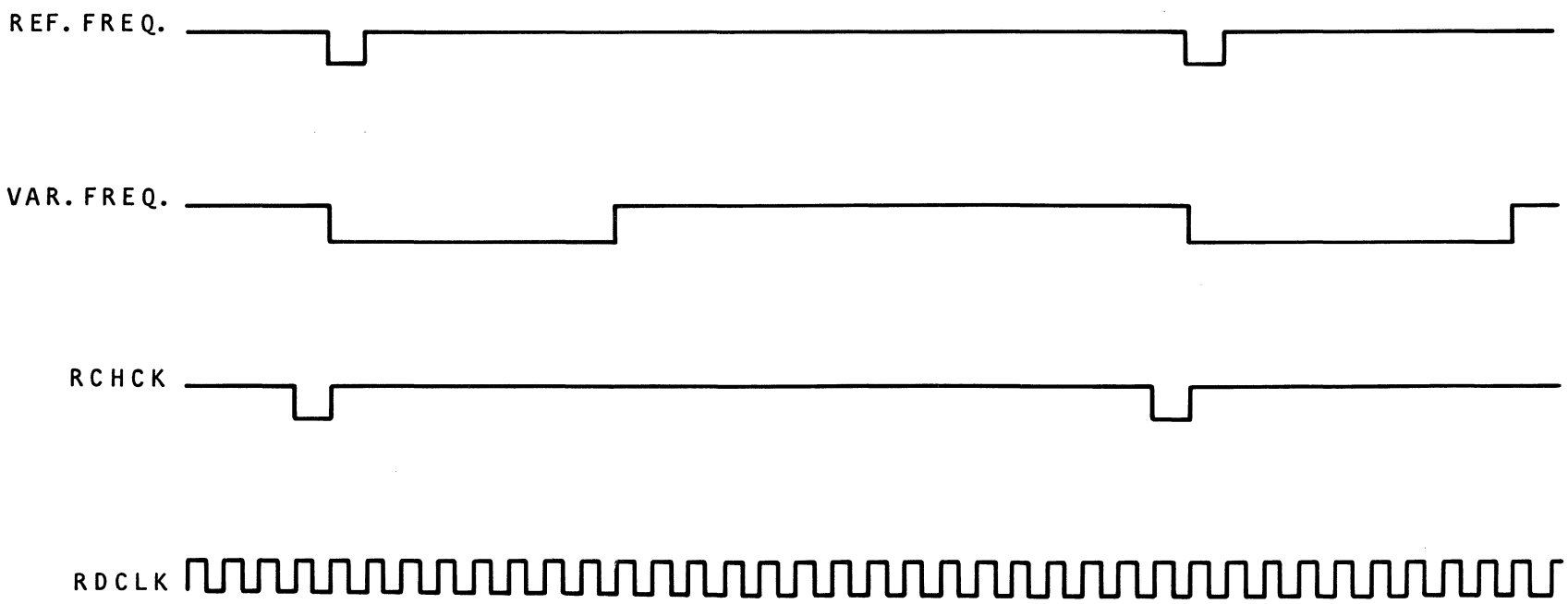


Figure 5-4. Read Clock Waveforms

		12.5 IPS	18.75 IPS	22.5 IPS	25 IPS	37.5 IPS	45 IPS	50 IPS	75 IPS	112.5 IPS	125 IPS
PRE-RECORD	READ FROM LDP	114	76.0	63.3	57.0	38.0	31.7	28.5	19.0	12.67	11.4
	READ	26	17.3	14.4	13.0	8.7	7.2	6.5	4.3	2.9	2.6
	WRITE FROM LDP	455	30.3	253	228	152	126.4	113.8	75.8	50.6	45.5
	WRITE 9TR DUAL GAP	34	22.7	18.9	17.0	11.3	9.4	8.5	5.7	3.8	3.4
	WRITE 9TR SGL GAP	46	30.7	25.6	23.0	15.3	12.8	11.5	7.7	5.1	4.6
	WRITE 7TR DUAL GAP	45	30.0	25.0	22.5	15.0	12.5	11.3	7.5	5.0	4.5
	WRTIE 7TR SGL GAP	57	38	31.7	28.5	19.0	15.8	14.3	9.5	6.3	5.7
	WRITE FILE MARK	273	18.2	152	136.5	91.0	75.8	68.3	45.5	30.3	27.3
POST-RECORD	WRITE	6	4.0	3.3	3.0	2.0	1.7	1.5	1.0	0.67	0.6
	READ FORWARD	0.7	0.47	0.39	0.35	0.23	0.19	0.18	0.12	0.08	0.07
	READ REV. 9TR EDIT	11.4	7.6	6.33	5.70	3.80	3.17	2.85	1.90	1.27	1.14
	READ REV. 9TR	6.0	4.0	3.33	3.0	2.0	1.67	1.50	1.00	0.67	0.60
	READ REV. 7TR EDIT	22.8	15.2	12.7	11.4	7.60	6.33	5.70	3.80	2.53	2.28
	READ REV. 7TR	11.4	7.6	6.33	5.70	3.80	3.17	2.85	1.90	1.27	1.14
PE ID BURST	RAMPDOWN	34.1	22.7	18.9	17.1	11.4	9.47	8.53	5.68	3.79	3.41
	START WRITE	34.1	22.7	18.9	17.1	11.4	9.47	8.53	5.68	3.79	3.41
	END WRITE	364	24.3	202	182	121	101	91.0	60.7	40.4	36.4
	START SEARCH SGL	108.1	72.1	60.1	54.1	36.03	30.03	27.03	18.02	12.01	10.81
	END SEARCH SGL	113.8	75.9	63.2	56.9	37.93	31.61	28.45	18.97	12.64	11.38
	START SEARCH DUAL	109.5	73.0	60.8	54.8	36.5	30.42	27.38	18.25	12.17	10.95
	END SEARCH DUAL	115.2	76.8	64.0	57.6	38.4	32.0	28.8	19.2	12.80	11.52

Table 5-2. Gap Control Delays (Milliseconds)

Revised

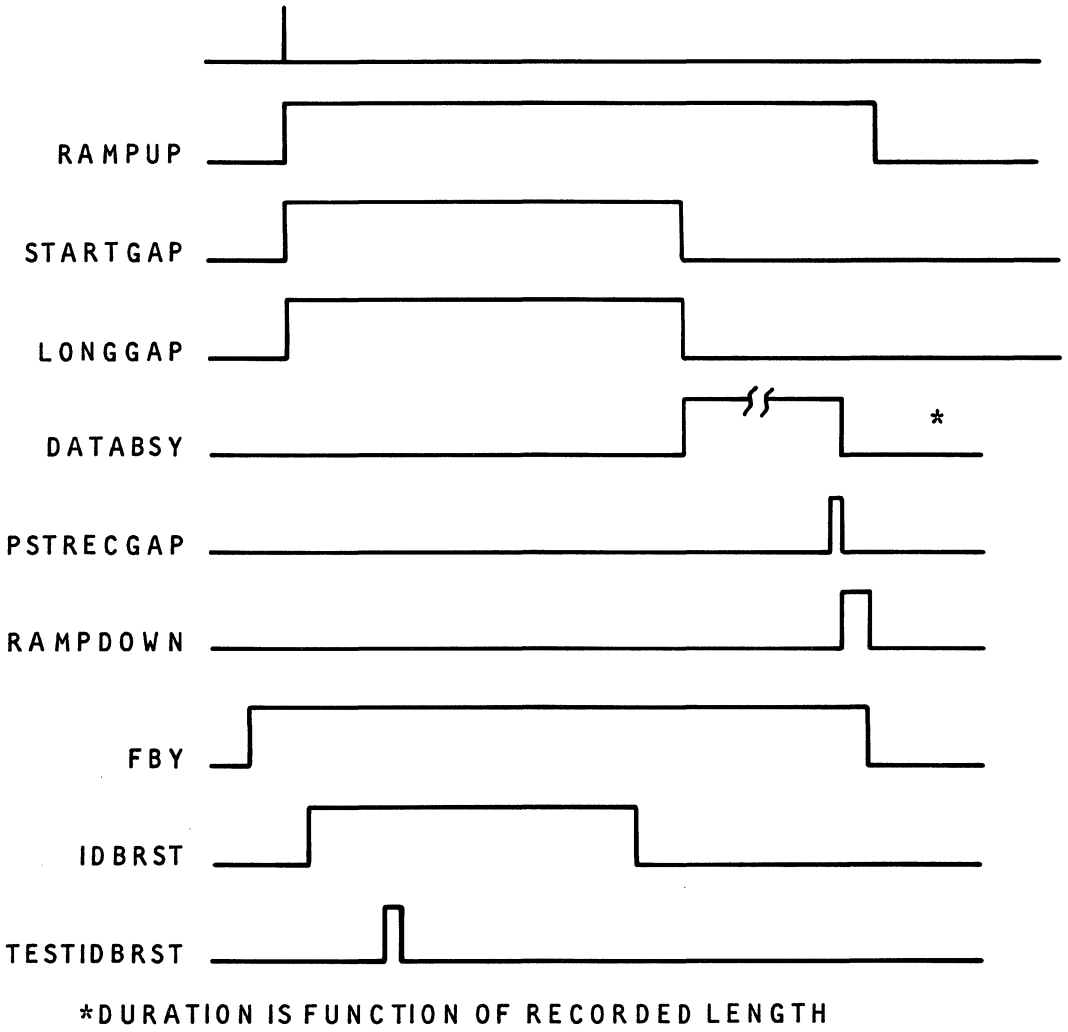


Figure 5-5. Gap Timing, Write From Load Point in PE

5-23. Figure 5-6 illustrates a typical write operation with the tape at other than load point. Note that the start gap duration depends upon head type (single- or dual-gap, seven- or nine-track). The single/dual-gap variation reflects the 0.15-inch variation in interrecord gap which could occur due to the presence or absence of read-after-write heads. The seven/nine-track variation reflects the difference in conventional interrecord gap size (0.6 inch for nine-track, 0.75 inch for seven). Note also that DATABSY is longer in duration for dual-gap versus single-gap heads, again reflecting the time required to traverse the 0.15-inch read-to-write gap.

5-24. Read-forward timing (not for load point) is illustrated in Figure 5-7. This timing is simpler, since it is independent of transport configuration. DATABSY is set before the read head is over the record on tape, thereby enabling the read electronics to "search" for the record. Since the interrecord gap can be much longer than nominal

(25 feet) the duration of DATABSY is not necessarily only the duration of the record to be read. Note that if no data is present on tape, DATABSY could be true until the end of the tape. It is the responsibility of the system to prevent such an occurrence or to terminate it via IFEN should it result from a timeout.

5-25. Read reverse is illustrated in Figure 5-8. Note that the transport continues to move tape, after the record has ended, to position it over the head for a rewrite, which is typically the next operation. The edit function operates to return the tape to the same position with respect to the write head as when the record was originally written. Therefore, it is reasonable to expect that rewriting of a record with the same number of characters will replace the original with a new record in the same position on the tape. In view of the irregularities in tape transport mechanisms and capstan servo misadjustments, however, the number of overwrites should be limited. Otherwise, resulting record drift would lead to nonstandard interrecord gaps.

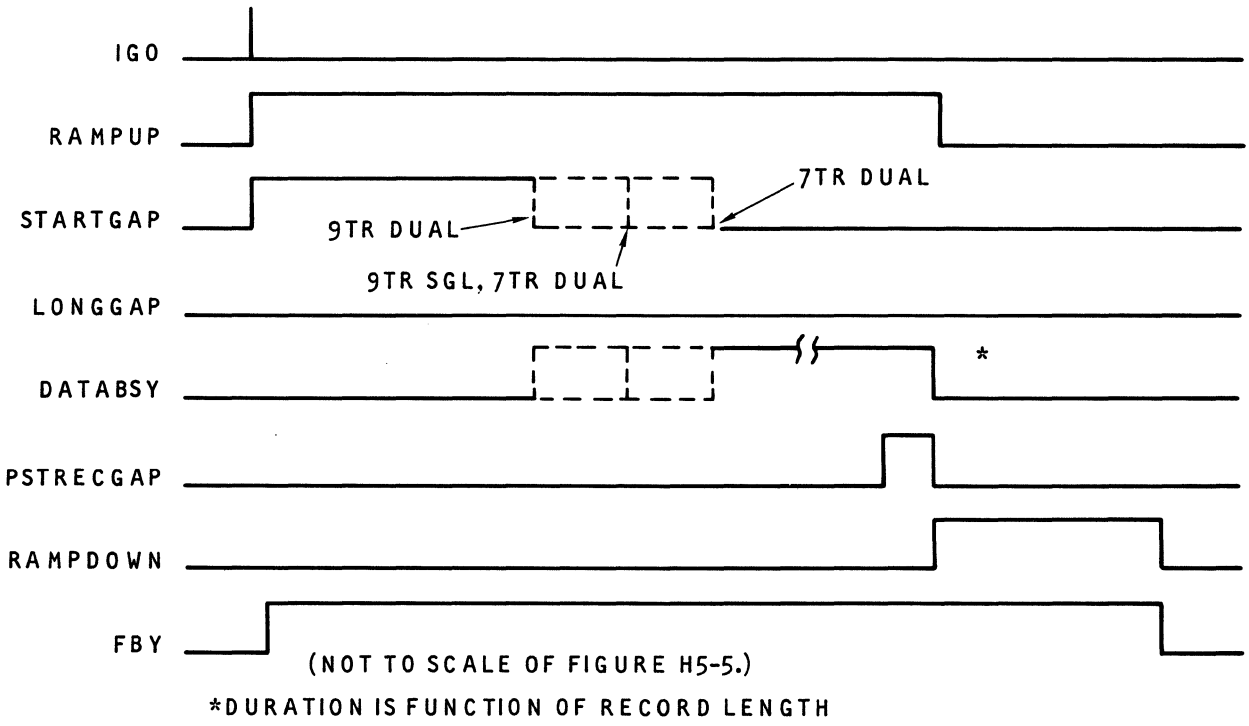


Figure 5-6. Gap Timing, Normal Write

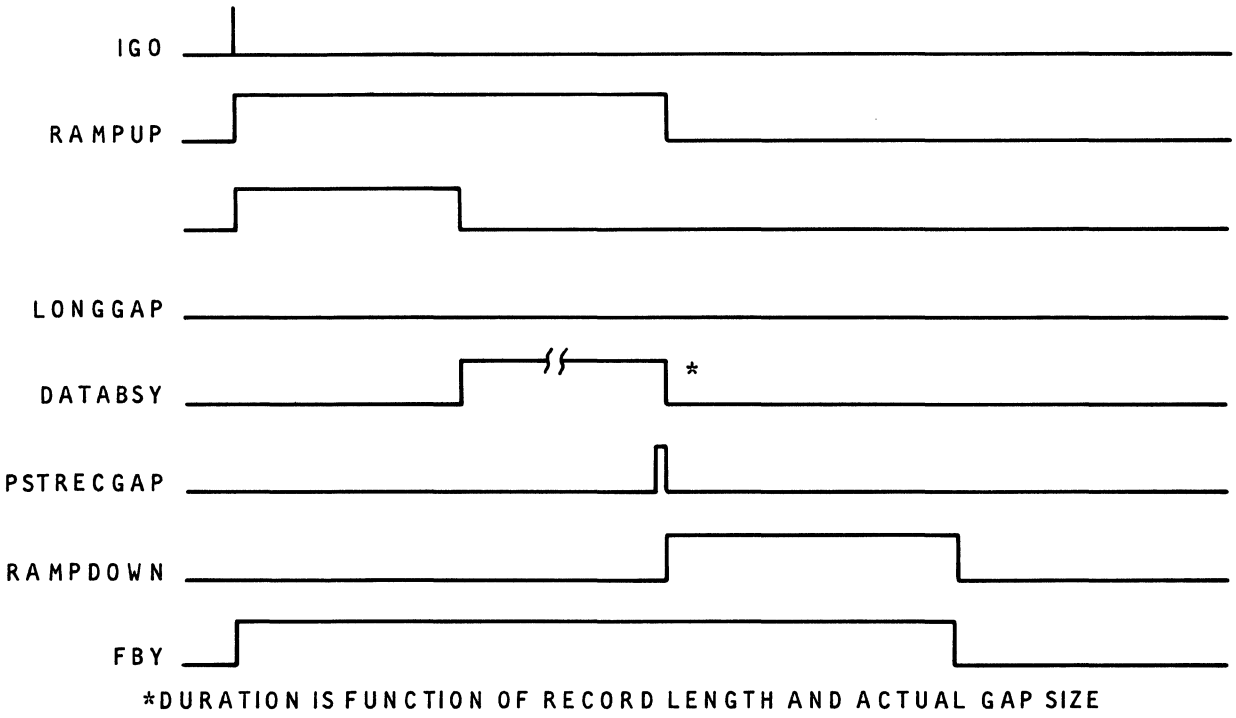


Figure 5-7. Gap Timing, Read Forward

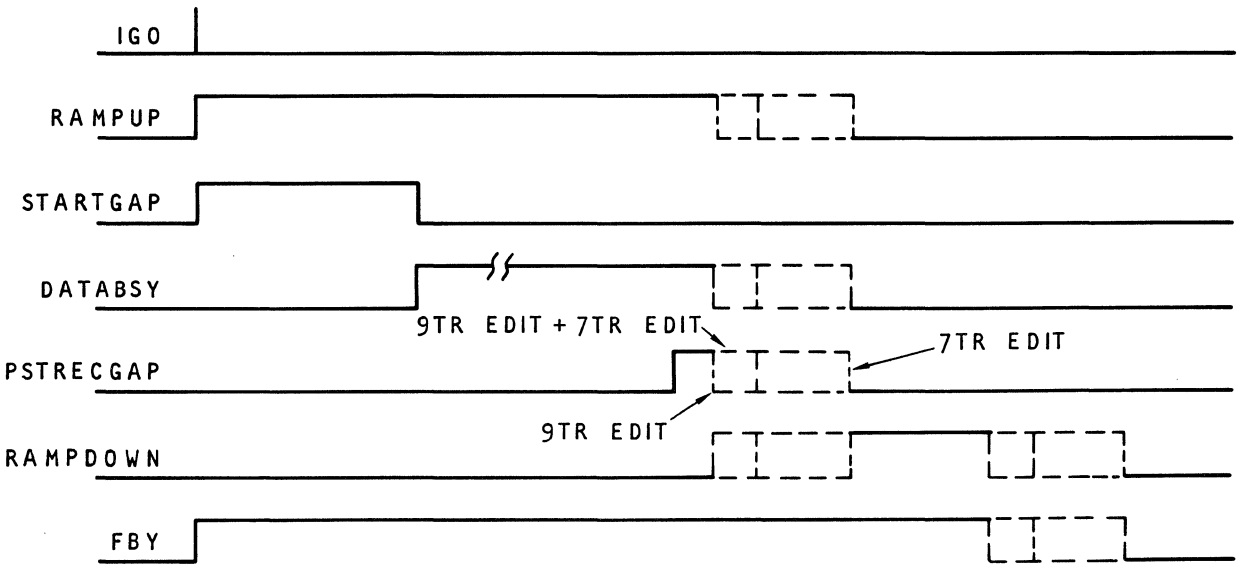


Figure 5-8. Gap Timing, Read Reverse

5-26. File-search operation is illustrated in Figure 5-9. In this example, a file search (forward or reverse) is set up and initiated. The tape transport traverses three non-file-mark records before encountering a file-mark record. The formatter then terminates the operation conventionally.

5-27. Figure 5-10 illustrates a reverse operation into load point and at load point. Note that the formatter is reset on detecting LDP. Should an initiate command be given in a reverse operation while tape is at LDP, the formatter momentarily goes busy (FBY asserted) and then is reset once again.

NOTE

In a forward file-search operation, should the end-of-tape marker be encountered the operation will be suspended after reading of the current record on the next record encountered. Should no records occur, the formatter will read off the end of the tape. It is the responsibility of the system to prevent this.

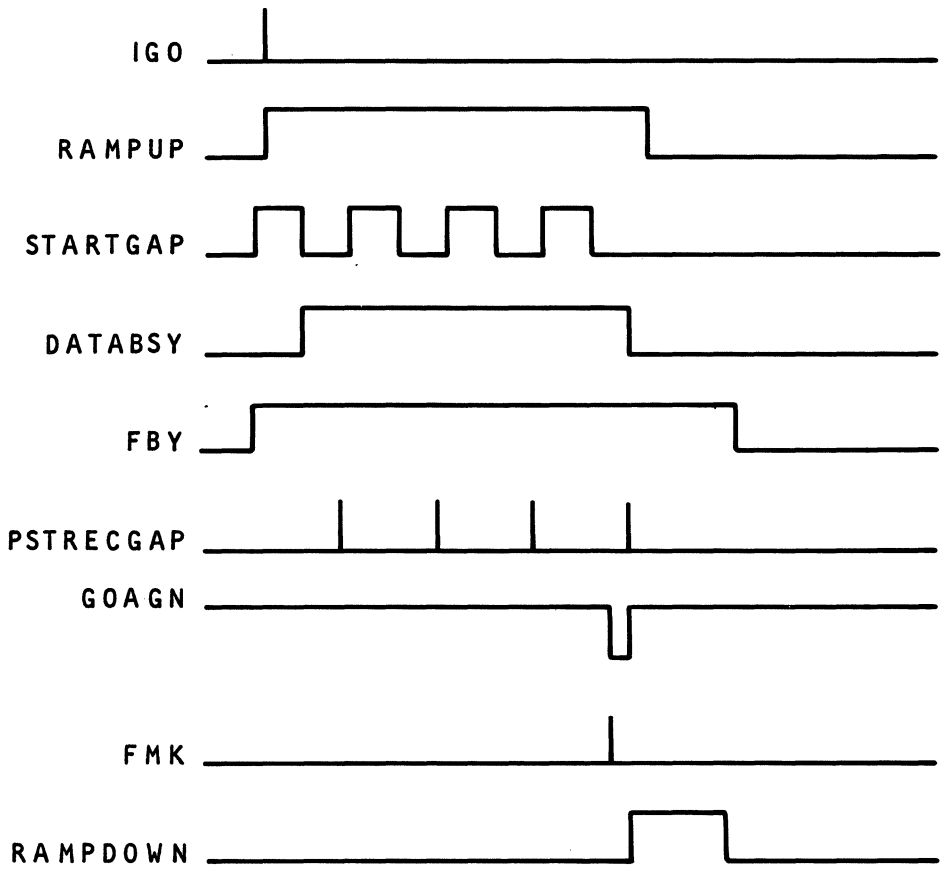


Figure 5-9. Gap Timing, File Search

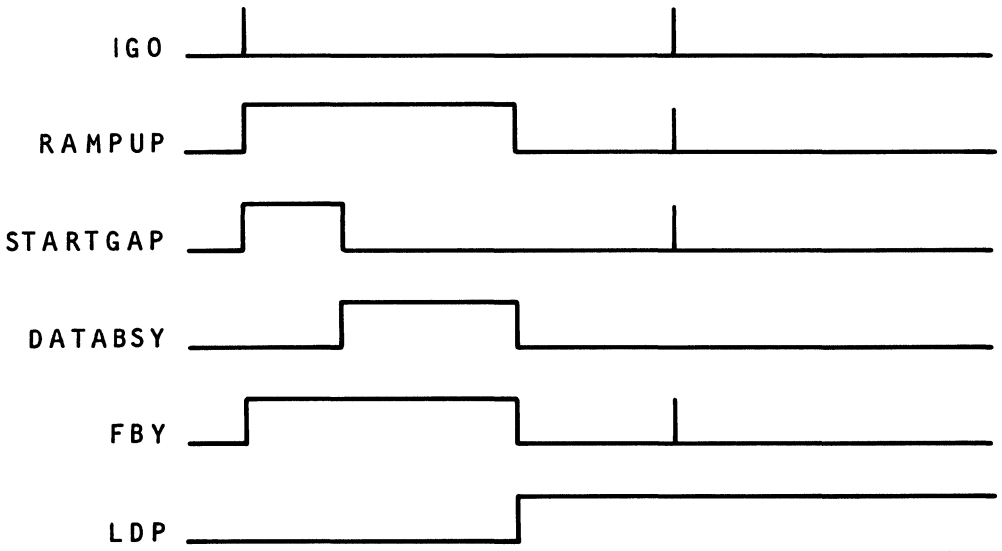


Figure 5-10. Gap Timing, Reverse Operation At LDP

5-28. Finally, Figure 5-11 illustrates the timing, in microseconds, between the initiate command, IGO, and RAMPUP. Note that FBY is asynchronously set by the falling edge of the IGO.

5-29. Gap Counter (Sheet 5, Drawing No. 360001-300). This logic works in conjunction with the gap control logic (Sheet 3) to provide the time delays illustrated in Figures 5-5 through 5-10 and enumerated in Table 5-2. IDBRST and ISTIDBRST are generated in this logic, and their operation is shown in Figure 5-5.

5-30. The counter is enabled by one of three exclusively asserted functions: STARTGAP, PSTRECGAP, and RAMPDOWN. The timings selected by these functions are qualified by such functions as 7TR, EDIT, REV, WRT, LONGGAP, SGL, and WFM. Figure 5-12 presents an example of the operation of the counter. Here an enable function (STRTGAP, PSTRECGAP, RAMPDOWN) is asserted, and TDO3 is multiplexed to the DLYRST flip-flop. The three enable functions (Sheet 4) are timed out by the DLYRST function. Hence, the duration of the enable line is W+1 clock periods, where:

$$W = \sum_{i} Z^{i-1}$$

and i is the decoded TDi, or the time is:

$$T = (W+1)\,(138.9 \times 10^{-6} / V) \text{ sec.}$$

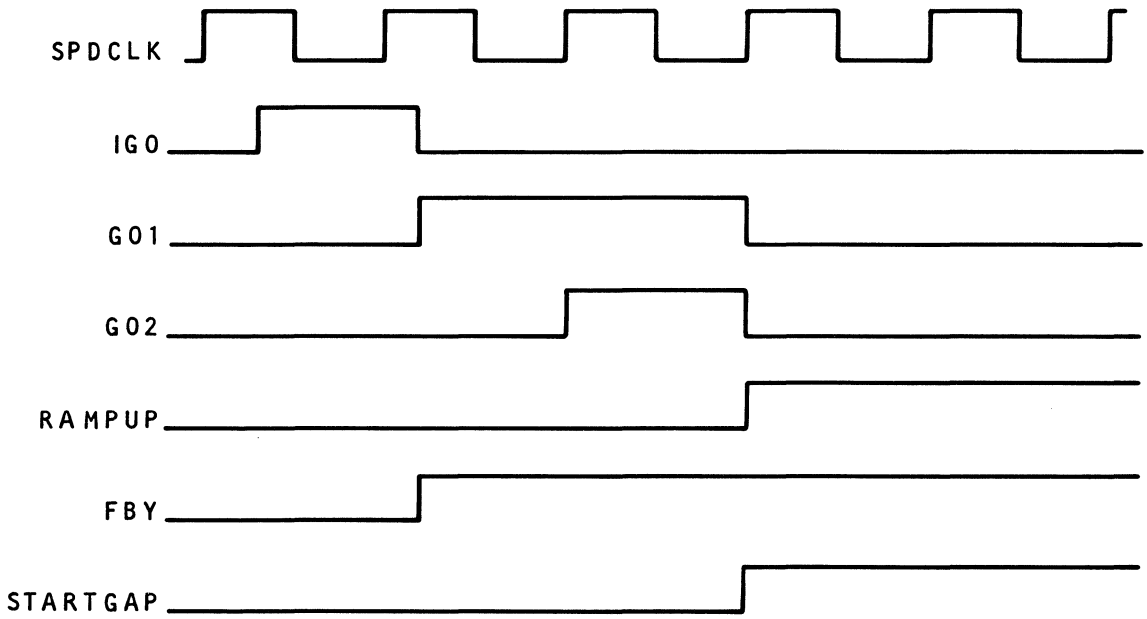


Figure 5-11. Gap Timing, Initiate Synchronization

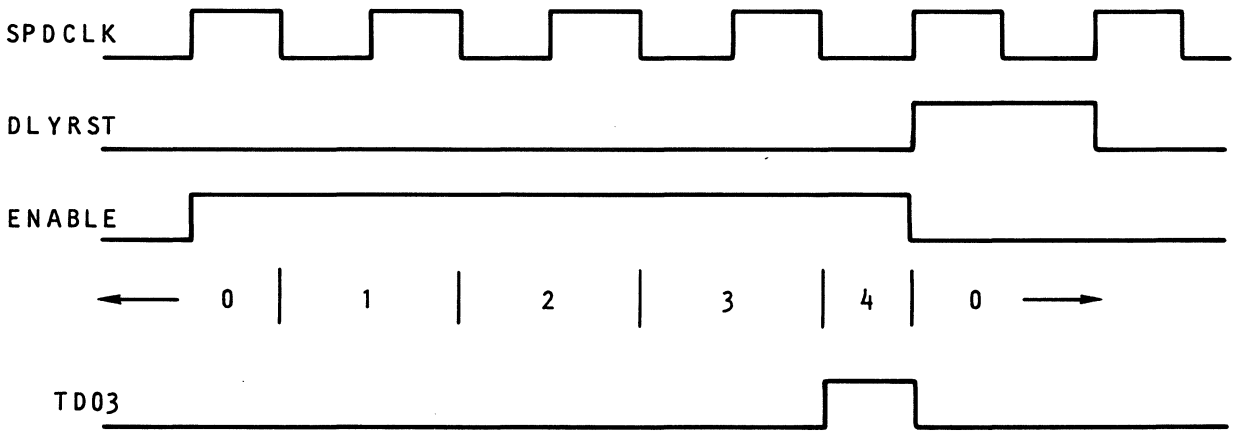


Figure 5-12. Gap Counter Timing Illustration

where V is in ips. Assume the read-forward postrecord gap at 12.5 ips:

$$T = (2^6+1)(138.9 \times 10^{-6}/12.5) = 0.72 \ \mu sec.$$

which agrees with Table 5-2. Note also that the waveform generated by TDO2, should the counter be free running, is one-fourth the frequency of SPDCLK.

5-31. Write Control (Sheet 6, Drawing No. 360001-300). This logic controls the formatting of the write data. Its principal functions are as follows:

a. Inserting preamble and postamble in PE.

b. Generating data strobes until stopped by LWD.

c. Producing time delays separating CRC and LRC from data portion of record in NRZI.

d. Writing file mark 0's (80 flux changes) in PE.

e. Controlling data encoding multiplexers.

f. Generating WEND.

5-32. Figure 5-13 illustrates the waveforms to be expected during the recording of a PE record.

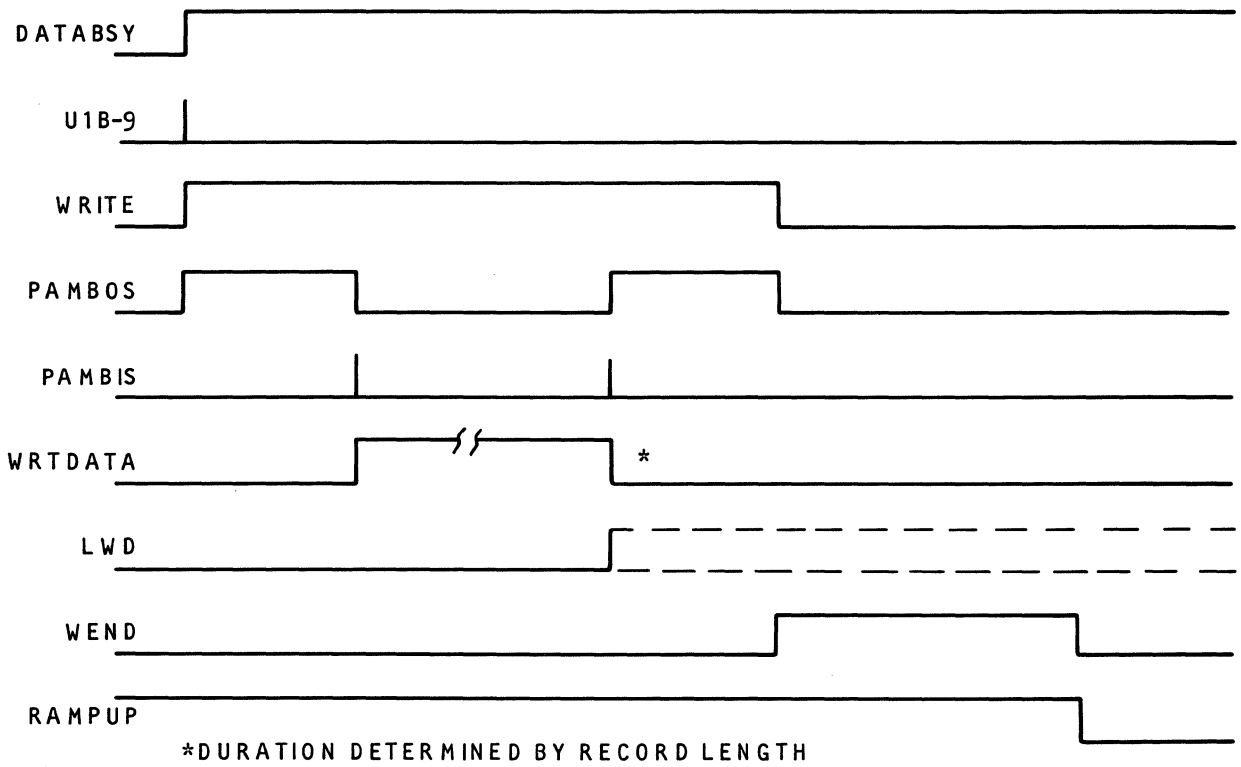


Figure 5-13. Write Formatting, Phase Encode

5-33. The rising edge of DATABSY sets flip-flop U1B (upper left of this logic, Sheet 6). The output of this flip-flop is transferred to either the second or fourth flip-flop, depending on the level of NRZ. In PE, the second flip-flop is set. In any event, the signal WRITE is asserted, clearing th first flip-flop. The second flip-flop produces the signal PAMBOS, which releases the WRDLY counter, asserts WDEC1, WRITE1, and WDSE. These signals allow the write data encoder (Sheet 7) to output 3200-fci encoded data to the transport.

5-34. When the counter reaches 40, the second flip-flop, U5C-10, is reset. If the command is WFM, this completes the write operation; otherwise, flip-flop three, U7F-6, is set for one clock cycle. This condition asserts PAMB1S, which generates PAMB1EN, which, in turn, writes the preamble, terminating the character on tape. The fourth flip-flop, U4A-6, is set next. Note that if operation is in NRZI mode, the preamble process is bypassed, and writing of data takes place immediately. WRTDATA conditions WEDC0 and WDEC1 to duplicate WRTG. This allows the proper encoding of input data (paragraphs 5-37 through 5-43). When the final character is to be recorded, the controller asserts LWD, which is synchronized with WRTG by flip-flop U5C (left center, schematic sheet 6).

5-35. In phase-encode recording mode, this signal resets WRTDATA and sets the fifth flip-flop, U40-10. This flip-flop sets up the command for encoding the postamble delimiting character, exactly as was done for the preamble. One clock period later it is reset and flip-flop U40-6 is set, again releasing the delay counter to encode the 40 all-0's characters comprising the remainder of the postamble. This accomplished, the last flip-flop is reset, which allows WRITE to go false, thereby generating WEND and terminating the operation. (Actually, read-after-write transports will continue until the read verification is complete.)

5-36. In NRZI operation, WRTDATA is cleared by LWDS (on one character time, if the operation is a WFM), and flip-flop U4A-10 is reset, producing the signal CCDLY and preventing further recording for three character times (the spacing between the first check character and last data character). In nine-track NRZI, flip-flop U4B-7 then goes set, conditioning the CRC character for encoding. After one character time it is reset, and flip-flop U4B-9 goes set for three more character times and then goes reset. Again, with the reset of the last flip-flop the signal WRITE goes false. This signal then generates the transport WARS signal, producing the LRC character while simultaneously informing the gap control logic that the written record is complete.

5-37. Write Data Encoder (Sheet 7, Drawing No. 360001-300). The purposes of the write data encoder logic are as follows:

a. Generation of PE all-0's for use in preamble, postamble and file mark.

b. Generation of PE 1's character for preamble and postamble.

c. Generation of parity on incoming data.

d. Generation of nine-track, NRZI, cyclic redundancy check (CRC) character.

e. Detection of a seven-track, NRZI, all-0's character and replacement of it with a BCD 10 character.

f. Encoding of both NRZI and PE data.

5-38. Write data encoding is accomplished by the four-input, inverting multiplexers, U10L, U9M, U9N, U10M, and U10L and the D registers (shown on the schematic, sheet 7, at right of the multiplexers). The encoding process is controlled by the select inputs to these multiplexers and the ratio of WRCLK to WRTG. In NRZI, this ratio is unity (i.e., one WRCLK pulse for each WRTG), while in PE it is two to one.

5-39. In NRZI encoding, WDEC0, WDEC1, and PAMBIEN are always low at the rising edge of WRCLK, while WRITE and WRITE1 are always high. As a result, controller write data (which is inverted) is selected by the multiplexers, inverted, and stored in the registers by the rising edge of WRCLK. The data is transmitted to the transport, accompanied by write data strobes (WDS). The result is that the characters are transmitted to the transport with essentially no processing by the formatter. After all nine-track data is transmitted, the formatter asserts the WDEC0 line to the multiplexers, selecting the CRC character for transmission. This character is produced by the network shown at the left on sheet 7 of the schematic as a result of the actual write data. This character is used for error detection during reading. Seven-track records may be written with odd or even parity. In nine-track records, parity is always odd. When even parity is selected and the character to be written is all 0's, there is no means by which the transport, in reading back, can distinguish a character. As a result, the write lines are monitored by the network consisting of U10P and U6L, and the occurrence of such a character will force W4 and W6 to be asserted, effectively writing a BCD 10 code.

5-40. NRZI file marks are generated by asserting WDEC1 and negating WDEC0. This conditions the multiplexers to the file mark patterns as shown below:

	0	1	2	3	4	5	6	7	P
SEVEN-TRACK	0	0	0	0	1	1	1	1	0
NINE-TRACK	0	0	0	1	0	0	1	1	0

5-41. As stated previously, in PE mode the frequency of WRCLK is twice that of WRTG, since there are two flux transitions possible for each data bit (as opposed to one in NRZI). When WRTG is low (Figure 5-14), the rising edge of WRCLK samples the data lines into the register, as in NRZI. Shortly thereafter, a WDS pulse which copies this data into the transport register is issued. When WRTG is high, WDEC0 and WDGC1 are asserted, causing the outputs of the registers to be inverted and applied to their D inputs. The rising edge of WRCLK (which is missing in NRZI) at this time forces all registers to toggle, producing the PE data transitions. This transition is subsequently copied into the transport. Note that the data transitions for 1 bits are falling edges, toward the direction of erased tape, while the 0 bit is a rising edge. Note also that there is always a data transition but not necessarily a phase transition.

5-42. The PE preamble/postamble and file mark patterns are all identical. They consist of 80 flux transitions equivalent to 40 all-0's characters. This is produced by selection of the file mark inputs to the multiplexers while WRTG is low. Note that these inputs are all high (the level of a 0 bit). The all-1's character delimiting the end/beginning of the preamble/postamble is encoded by assertion of PAMBIEN while WRTG is low, thereby disabling the multiplexers and forcing their outputs high (the level of a 1 bit). The file mark is completed by disabling of the registers associated with dc-erased tracks 1, 3, and 4 by WRITE1.

5-43. PE tapes are identified by a 1600-fci burst written on channel P in the vicinity of the BOT marker. The formatter accomplishes this by dividing the WRCLK by a factor of 4 and applying the resulting signal on WDP. The WDPs are generated normally.

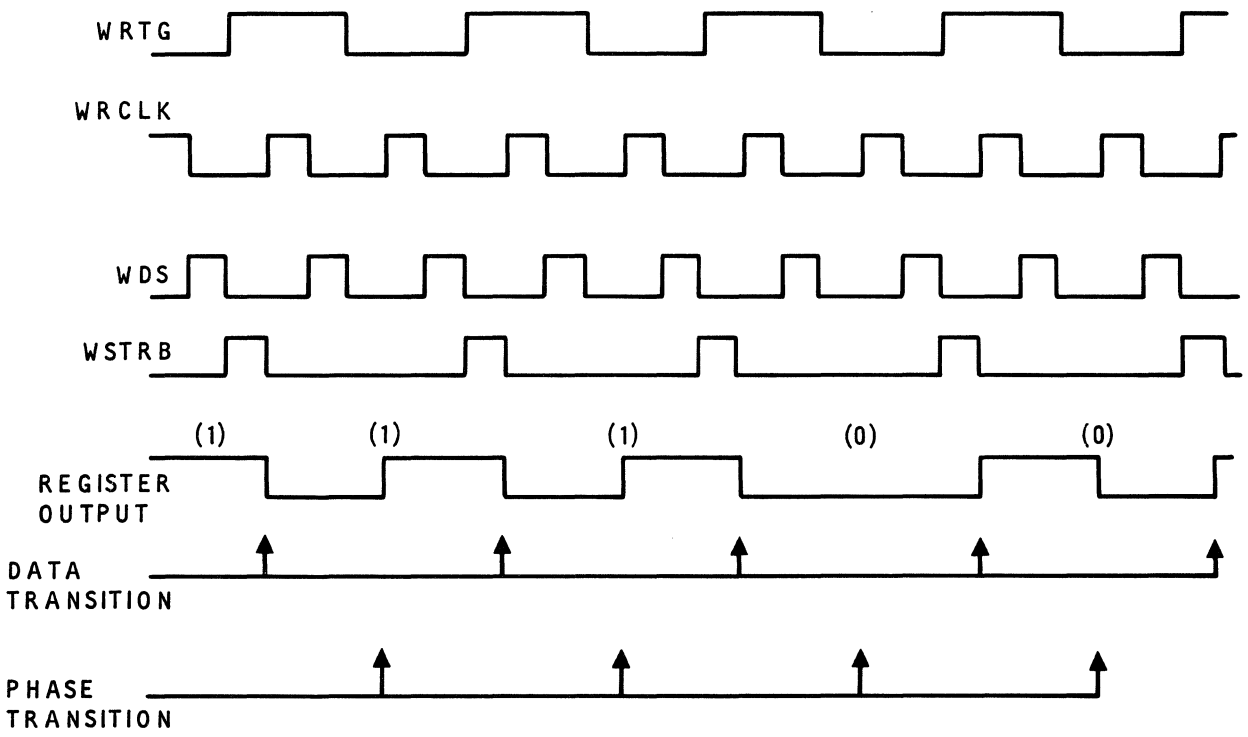


Figure 5-14. PE Writer Data Timing

5-44. NRZI Read Control (Sheet 14, Drawing No. 360001-300). The purposes of the read control logic are as follows:

a. Detection of first received characters.

b. Development of half-character timing required to transfer characters between input and output data registers.

c. Development of isolated character timing required to distinguish check characters.

d. Detection of end of record.

5-45. For purposes of discussing timing it is important to remember that a nine-track record might not have a CRC character but must have an LRC character, and that seven-track records might have no LRC character. These situations impose a problem primarily in discriminating check characters in a reverse read operation. The second problem is resolved by the observation that such a record must have at least two characters spaced a single character period apart.

5-46. Nine-track, Read-Forward Operation. This discussion provides the general framework for explaining the other modes. At the start of the read operation, the FCD flip-flop is cleared. The circuit awaits the first RCG pulse, which sets the CD flip-flop (U10E) at center left. This produces a one-clock (NRCLK)-period character-detect pulse (CDP) and sets the first-character-detected (FDC) flip-flop. The CDP resets the interval counter consisting of devices U12K, U10H, and U12J. The '393 counter counts 16 NRCLK pulses, enabling the D input to the '74 latch. This flip-flop goes set for one clock period, after which it clocks the '175 Johnson counter (U12J) with the result that Q_0 is set and Q_1 and Q_2 are reset. The counter counts another 16 NRCLK pulses and again steps the '175 counter, setting Q_0 and Q_1 and clearing Q_2.

5-47. Again the counter counts another 16 NRCLK pulses, and, when the '74 latch is set, produces a pulse HCTP as well as stepping the '175 counter. This HCTP pulse simultaneously clears the CD flip-flop and sets the character in output register (CIOR) flip-flop. The falling edge of CD causes the character in the input register (paragraph 5-56) to be transferred to the output register (synchronously), and generates the CIR pulse which clears the input register. The counter now continues to operate, searching for a check character. However, it is usually interrupted by receipt of a RCG pulse, indicating the second data character is received. This produces a character detect pulse which starts events leading to another HCTP one-half character time later. Simultaneously, it sets the gate read strobe flip-flop (GRDSTRB), since a character resides in the output register (CIOR true). After 16 NRCLK pulses, RSTRB is asserted. Sixteen NRCLK pulses later RSTRB goes false so that a read strobe is generated to the controller, allowing it to transfer the character in the output register. Subsequently, a HCTP pulse occurs, moving the new character into the output register.

5-48. These events continue until the last data character is in the output register. As indicated previously, the interval counter continues to run after having produced the HCTP pulse which transferred the last character into the output register. The state of the counter is now Q_0, Q_1, Q_2 set. Another 16 pulses produces Q_1, Q_2 set, Q_o cleared, another16 pulses and Q_2 is set, Q_o and Q_1 cleared. Another 16 pulses clears the flip-flop, which gates the isolated character pulse. This is about one character time since the last character was received. The cycle repeats for an additional character time, thereby producing and ICP pulse.

5-49. This pulse sets the GRDSTRB flip-flop, thereby generating a read strobe for the last data character. It also sets the first stage of the isolated character shift register. Events continue as before until either a CDP pulse occurs because the CRC character is received or an ICP pulse occurs, indicating two more character periods have elapsed with no character received. In either case, the second stage of the isolated character shift register is set. However, a CDP pulse would have the effect of loading the CRC character into the output register and synchronizing the counter in phase with the new character. The counter continues until the next ICP pulse, at which time the third stage of the isolated character shift register is set. This condition asserts CCG and generates a read strobe if CIOR was set, indicating a non-zero CRC in the output register. Two character times later, depending on the race between ICP and CDP, the isolated character register is stepped to the fourth stage. The LRC character which is received generates a CDP and is read into the output register, if this has not already occurred. Following this, the counter continues to run and steps shift register U12F.

5-50. The first ICP generates the gate format check (GFC), which examines for any subsequent illegal characters arriving from the transport. Two pulses later, the gate error report (GER) signal is asserted, allowing the hard error signal and file mark, if any, to be asserted. One more ICP, and REND is asserted, informing the gap control logic that the read operation is complete.

5-51. Seven-Track, Read-Forward Operation. Seven-track, read-forward operation is identical to nine-track, until the last data character is processed. Note that the first two stages of the isolated character shift register are forced set by seven-track status. The ICP pulse generated between the last data character and the LRC character sets the third stage. This ICP pulse also outputs the last data character, which is now in the output register. Subsequently, the fourth stage of the isolated character register is set either by receipt of the LRC or by an ICP pulse. This condtion asserts CCG. If the LRC character is present, it is entered into the output register and sets the CIOR flip-flop. The next ICP pulse (two character periods after the LRC character) generates the read strobe to output the LRC if the CIOR flip-flop is set (no character, no read strobe). This ICP pulse also sets GFC. The operation is then identical to nine-track operation.

5-52. Nine-Track, Read-Reverse Operation. In nine-track, read-reverse operation, the first character received, the LRC, sets FCD and is entered into the output register. An ICP pulse, which generates a read strobe and sets the first stage of the isolated character shift register, is subsequently generated. Note that CCG is asserted at this time. The next expected event is the CRC character, which, if it occurs, sets the second stage of the isolated character register and is input into the output register; otherwise, the ICP sets the second stage. The next ICP sets the third stage and generates a read strobe if CIOR is set (indicating a CRC is in the output register). The next event is the receipt of the last data character of the record (working from last to first), which sets the fourth stage of the isolated character shift register and clears CCG. Data characters are then output by CDP pulses, exactly as in read-forward operation, until the first character is encountered. It is entered into the output register and remains there until an ICP pulse occurs, drives this character out, and sets GFC. The remainder of the operation is exactly like that of read-forward.

5-53. Seven-Track, Read-Reverse Operation. Seven-track, read-reverse starts by forcing the first two stages of the isolated character register set as soon as the first character, which may be the LRC or last data character, is detected.

5-54. When this character occurs, it is entered into the output register and starts the clock. If it is the LRC character, a ICP pulse, which sets the third stage of the isolated character shift register, is generated two character times later. The ICP pulse also generates a read strobe under a CCG flag (fourth stage of isolated-character register not set). Next, a CDP occurs for the last data character, setting the fourth stage of the ICR. The operation is then as it was in nine-track operation.

5-55. If the LRC character is absent, the first received character is the last data character and must be followed by at least one more data character. This data character forces the third and fourth stages on the isolated character register to be set and outputs the last data character currently in the output register. The operation is then as in nine-track operation.

5-56. NRZI Read Data Registers (Sheet 13, Drawing No. 360001-300). The purpose of this logic is to provide a set of registers to receive a read character (NRZI) from the tape drive while buffering an output character. This double buffering is required primarily to distinguish check characters from data characters in read-reverse operations. In addition, the logic provides the facility to distinguish data characters received from a transport which is not using a RDS. It also recognizes valid NRZI file marks.

5-57. The falling edge of a read data signal or the read data strobe (if used) copies the transport data into the first register, where it resides for about one-half character time. While in this register, it is sensed by the OR network to generate RCG, indicating that a character is received. This received character forces the NRZI read control (paragraph 5-44) to produce an output cycle transferring the character in the second register (if any) to the computer, after which *CD transfers the received character to the record register, and *CIR shortly thereafter clears the input register. While the character resides in the output register, it sets up the input to the file-mark-holding flip-flop, U18B. If any character other than a file mark character is detected, the flip-flop is set, subsequently preventing the setting of the NFMK flip-flop, U15J, at gate error report time (GER). The output of the second register is presented to the controller read data drivers.

5-58. NRZI Read Error Logic (Sheet 15, Drawing No. 360001-300). The purpose of this logic is to examine the recovered read data for read errors and format errors on write, including the folowing:

a. Vertical parity error (odd on nine-track, possibly even on seven-track).

b. CRC parity error, where the CRC parity is odd if the record contains an even number of data characters.

c. CRC error.

d. Check character error, meaning the record format is in error.

e. LRC error.

5-59. Vertical parity is computed for all data characters and pulses the HER line for the particular character in error. CRC parity error is computed for both forward and reverse operation. If RSTRB is generated without a CCG flag, a data character is being processed and the flip-flop holding the error flag is toggled for each such character. The flip-flop is therefore set if the record contains an odd number of data characters; otherwise, it is reset. When a check character occurs, its parity determines whether or not it will toggle the flip-flop. The LRC character always has odd parity (in nine-track operation), hence it will toggle the flip-flop, and the parity of the CRC will determine the final state. If the flip-flop is set at GER, the CRC parity is incorrect.

5-60. CRC parity is computed in the forward direction only. All data characters and the CRC character are operated on by the CRC logic (identical to that on the write data encoder). At the end of the operation, all bits in the register are set, with the exception of RCR2 and RCR4. As a result, the D input of the sampling flip-flop is low if CRC is correct. The RSTRB generated by the LRC character samples this register. At GER time, an error is reported to the controller. A check character error signal checks for the existence of characters where none should exist (GFC) and reports the existence of any such character to the controller.

5-61. In all NRZI read operations, either seven- or nine-track, the tape must be polarized in the same direction at the end of the operation as at the beginning. This means that an even number of data transitions must have occurred in each track, which is the objective of the LRC character. The logic merely counts (modulo 2) the number of data transitions on each track, and if any flip-flop remains set at GER time, indicating an odd number of data transitions, an error is reported.

PE READ RECOVERY LOGIC

5-62. Block Detector (Sheet 25, Drawing No. 352040-300). This circuitry is driven entirely by two signals: Envelope (ENV) and Read Enable (RDENBL). When a read enable condition is true, indicating that the read section of the formatter logic should be searching for data, this logic is conditioned. If at least two channels are active, envelope (ENV) is detected. When this condition occurs, counter U11C counts four character periods before enabling Block Detect (BLKDET). ENV must be true for at least four character periods before BLKDET will go true. Once BLKSET is set true, loss of envelope for at least four character periods is required before BLKDET will go false. BLKDET conditions the phase detectors and the format control logic, preventing noise on the tape transport interface from being detected inadvertently as a data record.

5-63. Operation of this logic is best described using the block detector transition diagram, Figure 5-15. Assuming counter U10B is in state 001, which means U10B-10 is low, U10B-2 is low, and U10B-12 is high, detection of the envelope generates a next state of 010; otherwise it stays in state 001. Once in state 010, if ENV remains true, the counter will advance to state 011; otherwise, it will return to state 001. If the state counter is in either state 010 or 011, the time delay counter, U11C, will be released via its reset input, pin 1. When this counter times out, the state counter goes to state 100, which is the block detect state. Once the state counter is in this state, the same path must be followed in order to lose block detect. Note that when block detect is lost the counter is in state 000. Once in state 000, it will remain there until RDENBL goes false. Hence, only one block detection can occur for each STARTRD signal from the write logic.

5-64. Block Format Control Logic (Sheet 27, Drawing No. 352040-300, Figures 5-16 and 5-17). This logic decodes a phase data block into five intervals: the first half of the preamble, the second half of the preamble, the data portion of the record, the first half of the postamble, and the last half of the postamble. During these decoded intervals, certain tests are performed to detect whether the recorded block has a correct format. If not, FMTER (TP30) is generated. The sequence is started by the signal BOBPLS, on U8A-2. This pulse, which is one read clock period long, sets flip-flop U8A-6, which is BGNPRMBL (TP26). This flip-flop goes set approximately four characters into the preamble. The signal is used to enable the file mark detector and also generates the signal PRMBLTST on U9B-13.

5-65. PRMBLTST releases the dual counter (U8D). The counter counts a total of 24 character periods, then produces the signal RDLY for one clock period. This signal conditions U8C-10, provided a file mark has not been detected. It then resets flip-flop U8A-6, while simultaneously resetting U9A-7. Since U9A-7 is high, it is true for the last half of the preamble. This signal again produces the function PRMBLTST, which releases the counter. Should the counter reach its maximum count and produce the signal RDLY before TP32 goes false, a format error will be generated. This would indicate a long preamble, since mark one would have been detected late.

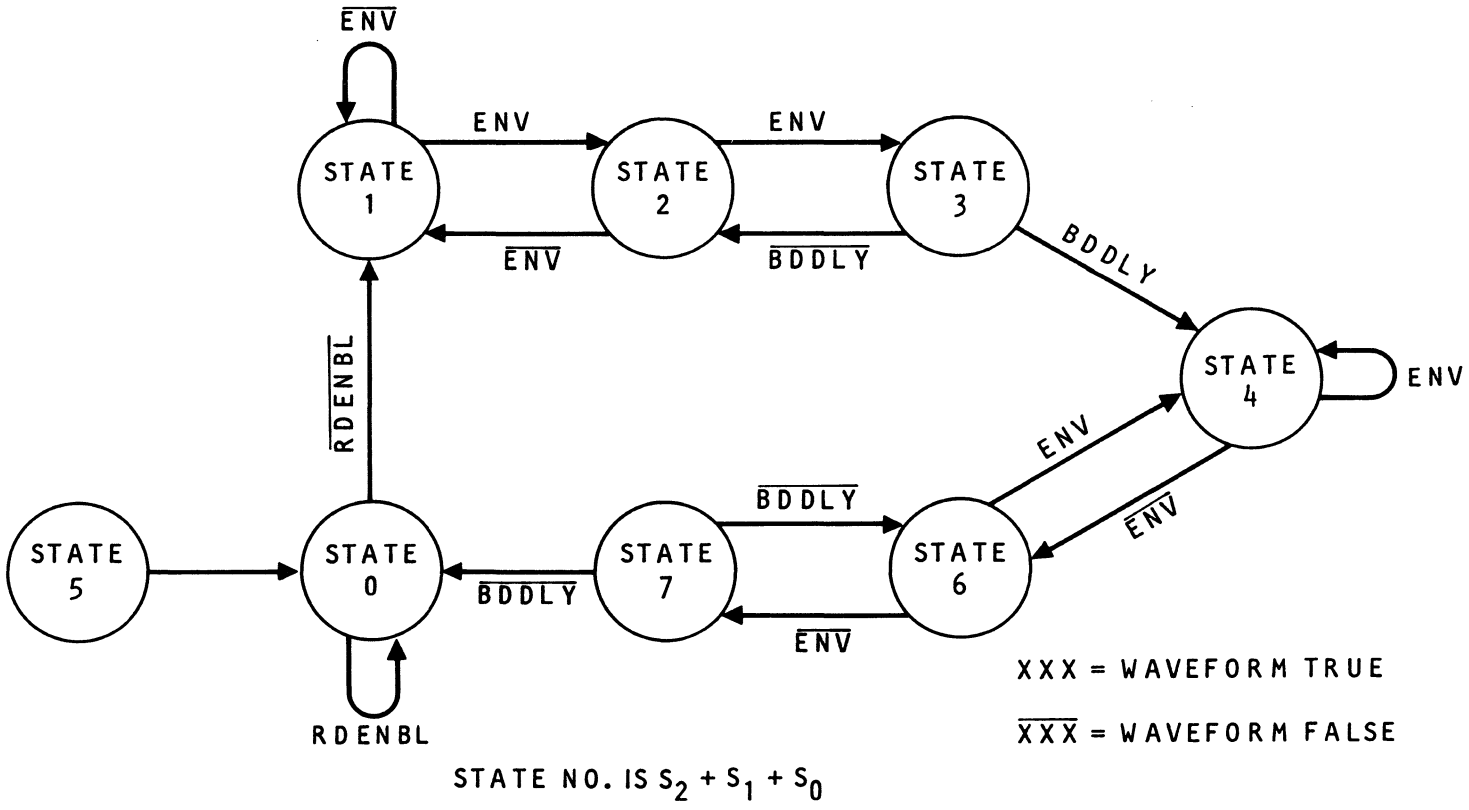


Figure 5-15. Block Detector Transition Diagram

Revised

5-66. Flip-flop U9A is set as pin 7 goes false when the signal SRDOUT (Start Readout) occurs on U9C-1. This signal indicates that the first character has been assembled in the skew buffer and is ready to be processed through postamble detection logic. At this time, RDDATA, on TP3, goes true. This signal will remain true for the entire data portion of the record. If more than one drop channel occurs while RDDATA and DGTI are true (U9D-11 and -9 respectively), a format error will be generated, since more than one drop channel will have occurred over the data portion of the record. When the beginning of the postamble is detected, MK2DET will be true on U10D-4. This will reset flip-flop U10A whose negated output will then go high (TP35). This indicates the beginning of the postamble. At this time, the skew buffer should contain an all-0's character. If not, U9D-12 (*ZEROS) will go true, producing a format error. Note also that the beginning of the postamble produces the signal PSTMBLTST (U9B-1), which once again releases the counter (U8D). When the counter reaches the count 24 condition, the signal RDLY is generated. This simultaneously sets U10A-9, causing the beginning of the postamble function on TP35 to go low, and U10A-7 (EOBWDW). During this time, the signal EOBPLS appears on U9D-3. Should this signal occur at any other point in the data record, a format error will be generated. Note that this test is disabled by a file mark condition, since a file mark ordinarily consists of nothing more than a preamble on the selected tracks.

5-67. EOBPLS also sets flip-flop U8B-6. This condition clears the sequence counter consisting of the five flip-flops (top of sheet). Therefore, an EOPBLS always terminates the read operation. Hence, the end of a one-word read operation is a function of the data envelope and not of any particular characters of the data itself. The gap test condition also releases the 24 character counter, which eventually sets flip-flop U8B-10 to an end read (ENDRD) condition. ENDRD is a signal sent to the write section of the formatter logic indicating that the read section has completed activites on this block. This signal will eventually force a ramp down on the tape drive.

5-68. Character Control (Sheet 28, Drawing No. 352040-300). The exclusive OR gate used in conjunction with flip-flop U9F is the modulo 2 counter for detecting parity. At channel 0 time, the contents of DATAOUTSB are copied into U9F. If DATAOUTSB is a 1 at that time, U9F-6 is set. Otherwise, it is reset. For channel times 1 through 7 and parity, U9F will be toggled if DATAOUTSB is true at that particular time.

5-69. The contents of U9F are sampled by register U8H at frame time whenever a character is being read out of the skew buffer. If parity is correct (odd), U9F-6 will be high at that time; hence U8H-12 will then be high. To accommodate the time delay between the skew buffer and the output register, parity is delayed by two character times before being presented to NAND gate U9B. It is then conditioned by *RDSTRBE, and, if parity is incorrect, a parity error pulse (PARITYERR) will be generated at TP 29 and transmitted to the controller interface. The character parity, U8H-12, is also presented to the error correction logic (sheet 30).

5-70. The all-0's character discriminator consists of inverter U9E-13 and -12, AND gate U9C-4, -5 and -6 and flip-flop U9F, immediately to the right. If a character containing all 0's is presented out of the skew buffer, U9F-10 will be high continously. At channel 0 time the output of the AND gate will be true, thereby setting the flip-flop. This flip-flop will stay set for the entire character if there are no 1 bits present in the character which would cause the *K input to be asserted.

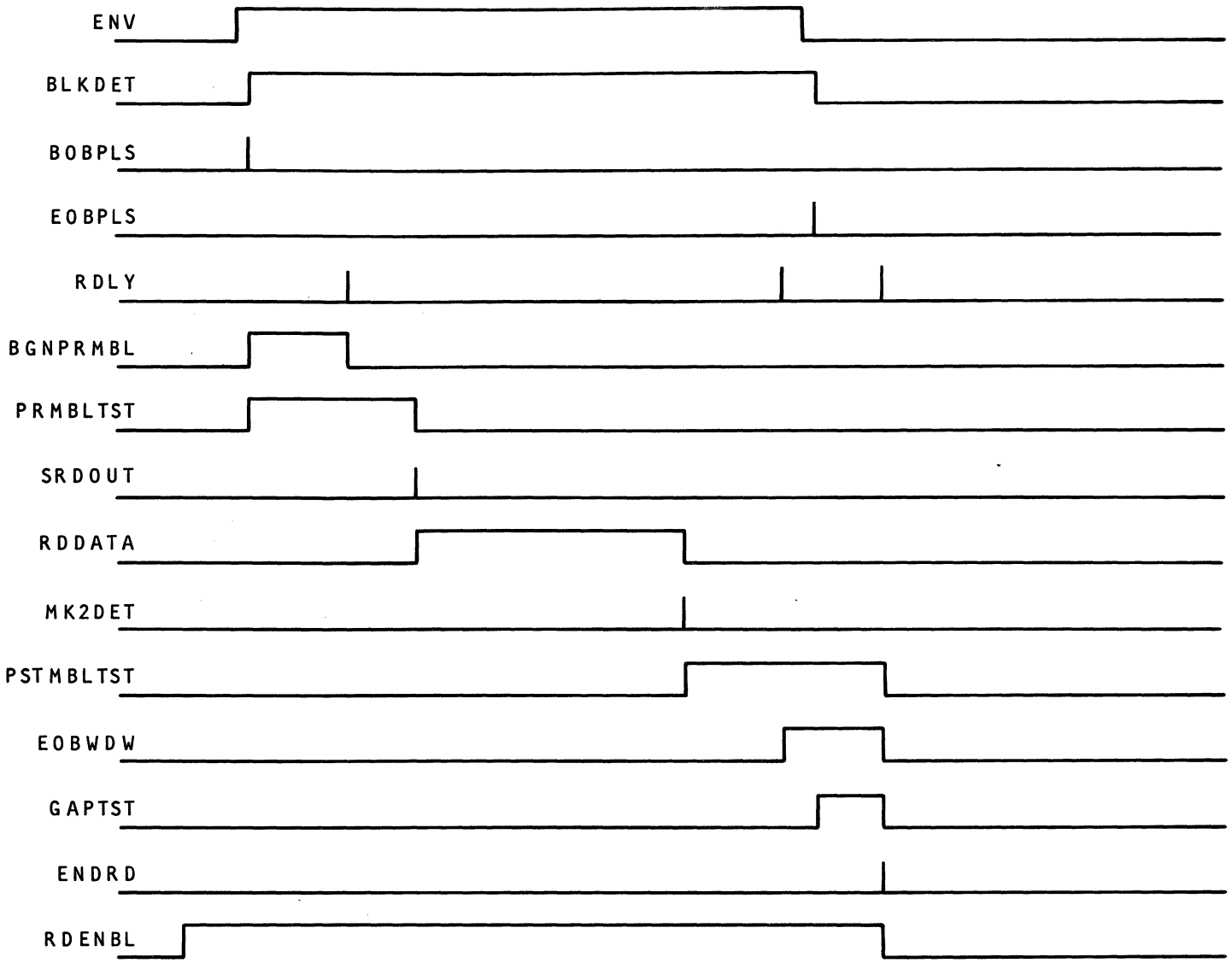


Figure 5-16. Read Record Timing

Revised

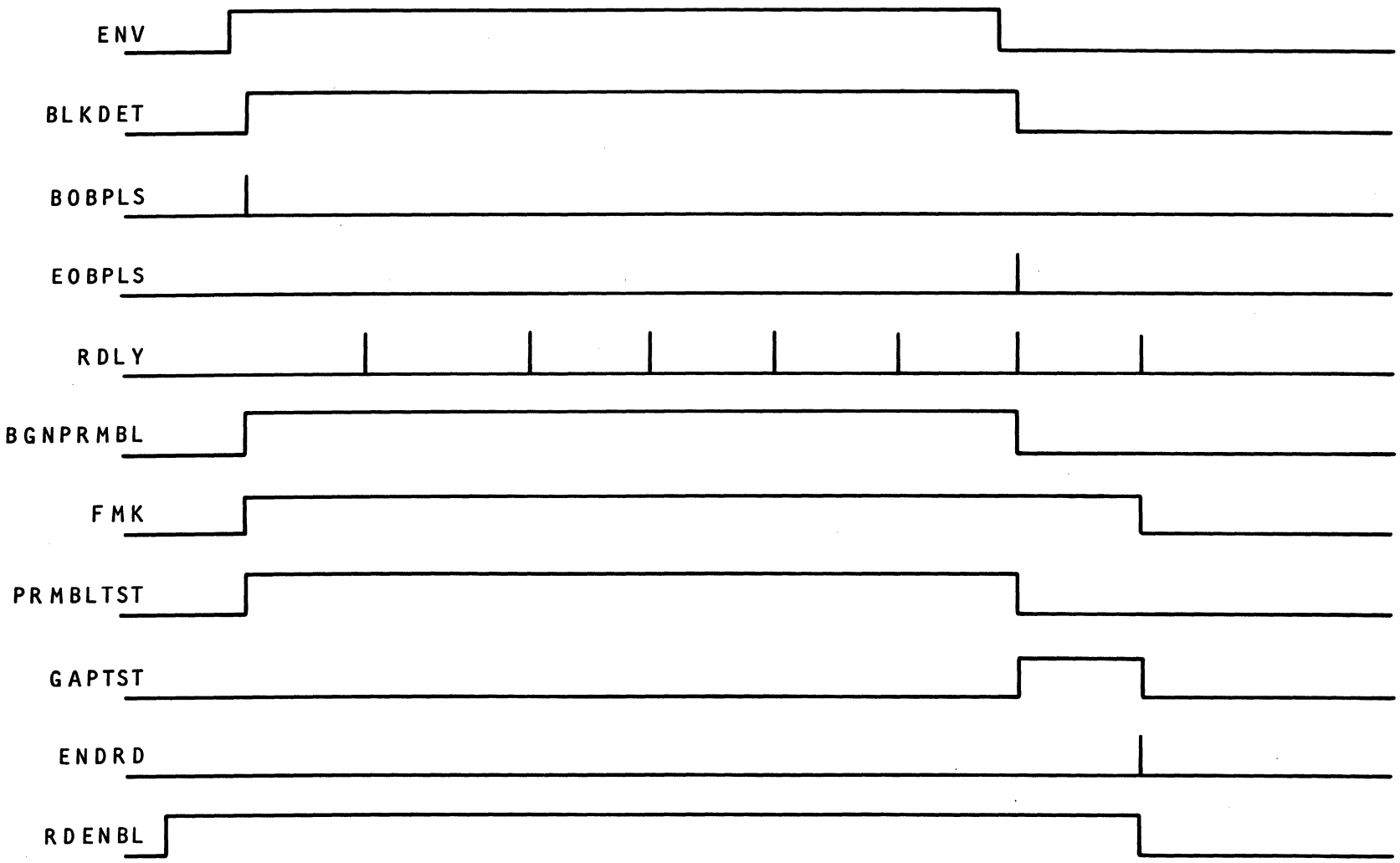


Figure 5-17. Read FMK Timing

5-71. At frame time, when the character is being read out of the skew buffer, the condition of this flip-flop is sampled by register U8H. If the character contained all 0 bits, pin 5 will be forced true. Such characters occur only during the postamble. An all-1's character detector consists of NAND gate U9C8, 9, and 10, and the flip-flop immediately to its right, U9H. If the character consists of all 1 bits, DATAINR2, which is presented to the NAND gate, will be true continuously. At channel 0 time, the output will be true; hence, flip-flop U9H will be set. The flip-flop will stay set as long as there are only 1 bits in DATAINR2. Any 0 bit will condition the K input on the flip-flop, causing it to be reset. The flip-flop is sampled at frame time when a character is being read out of the skew buffer. If the flip-flop is set, indicating that the character consists of all 1's, U8H-2 will be set true.

5-72. The all-1's and all-0's character detectors are combined in NAND gate U8F. This NAND gate will be conditioned true if it senses an all-1's data character in register 2, and an all-0's data character being read out of the skew buffer. Such a condition indicates the start of the postamble or the end of the data record. This condition is identified as MK2DET. Should a single-channel dropout condition occur, the logic will still operate correctly, since the all-1's data detector is driven by corrected data while the all-0's data detector is driven by the output of the skew buffer, which will be forced low during the corrected channel. The all-0's character detector is also used to detect erroneous postamble conditions (sheet 3).

5-73. The ANSI-IBM file mark detector consists of three inverters (sheet 28), an 8-input NAND gate, and flip-flop 9H. The detector is examining for channels 2, 6, and 7 active, while channels 1, 3, and 4 are simultaneously inactive during the beginning of the preamble. Such a condition causes U9H-9 to be reset. The reset state is FMK (TP 27). FMK is cleared if RDENBL goes false, indicating that the read section is reset.

5-74. The counter, U7B, is a time delay which allows characters to proceed through the postamble detection logic to the output register before enabling read strobes. As the first bit of the first character is being read out of the skew buffer, U7B-14 will be set true. A condition in which U7B-14 is true and pins 13, 12, and 11 are false indicates that only one character is in register 1 of the postamble detection logic. As the second character is read out of the skew buffer, the first is read into register 2 of the postamble detection logic and the new character into register 1. At this time, U7B-13 goes true. The subsequent character forces the initial character into register 3 of the postamble detection logic, and U7B-12 goes true. Finally, the next character arriving causes the initial character to be transmitted to the output register; U7B-11 goes true at this time. This condition will allow a read strobe to be generated to the controller interface.

5-75. U5D is the ID burst detector. All phase-encoded tapes must begin with a 1600-fci burst on the parity channel and dc erasure on all other channels. Since block detection requires that at least two channels be active, it cannot be true at this time; hence, U50-1 is conditioned true. Simultaneously the parity channel is active; hence, U5D-2 is true, and an ID burst condition is detected. IDBRSTDET will subsequently be gated with positional logic, indicating that the drive is ramping up over the initial gap. It will therefore generate IIDENT to the controller interface.

5-76. Channel Selection (Sheet 26, Drawing No. 352040-300 and Figure 5-18). The major output signals in this circuitry include the select channel conditions, which divide the read character clock to produce 10 intervals, one for each of the nine data channel and one for the frame channel. The drop-channel multiplexing logic samples the nine data channels for channel-drop conditions to produce a time multiplex channel-drop signal, drop counting logic, envelope detection logic, detection logic for a skew-buffer-full condition, and latches for generating a readout skew buffer.

5-77. Channel selection logic consists of a decimal counter composed of binary counter U19C and NAND gate U20B. For simplicity, the reset condition of the counter is decoded as select channel 0, SCH0, the count one condition as select channel 1, SCH1, etc., through the count seven condition, which is called select channel 7, SCH7. The count eight condition of the counter is decoded as select channel parity, SCHP, and a count nine condition as select frame, SFRM.

5-78. The select frame condition enables the parallel load on counter U19C through pin 9. This causes the counter to be reset to the 0 state, which implies that the next channel to be selected is channel 0. The counter is decoded by demultiplexer W8C and NAND gates U20B-8 and -11. The outputs of the decoding network are the complementary conditions: select channel 0 through 7, select channel parity, and select frame. Channel 0 parity and frame are also inverted before being transmitted to other portions of logic.

5-79. The four bits of the counter are also used for time multiplexing purposes. For example, consider the channel drop multiplexer, which consists of NAND gate U20B-6, multiplexer U20C, and NAND gate U20B-3. During channel times 0 through 7, channel bit 3 is low, thereby enabling multiplexer U20C. The other three channel bits are applied to the selection inputs of this multiplexer. Therefore, channel drop 0 condition is selected during channel 0 time; channel drop 1 condition is selected during channel 1 time, and so forth. The multiplexed output is available on *U20B-3.

5-80. *CHNDROP is also inverted and is available at TP 51. During select channel parity time, NAND gate U30B-1 is enabled, and the channel drop parity condition is output from the multiplexer. During frame time, neither NAND gate U20B nor multiplexer U20C is selected. Therefore, CHNDROP, on TP 51 is true at every frame time. This condition is required by the skew buffer control logic but should not be construed as being a valid channel drop condition.

5-81. The next operation to be performed is that of counting the number of channels actually dropped and comparing them to a count of one. The counting is done by the 16-state counter, U18A. Note that the counter is parallel enabled at each channel 0 time. Therefore, the counter samples the condition of channel drop at channel 0 time. If channel 0 were to be dropped, the counter would be preloaded with a count 1 condition; otherwise, the counter would be cleared. Following this, the counter is incremented each time it sees a channel drop condition.

5-82. The counter is then continously compared to a count 1 condition through the magnitude comparator, U19A. At frame time, the output of the magnitude comparator is latched by register U20A. At frame time, if the count in the counter is less than 1, U19A-7 will be high, and the latch will record a drop channel equal to 0 condition, meaning that all channels are active. If the count is a 1 frame time, U19A-6 will be true, and the latch will record a drop-channel-equal-to-1 condition. For a count greater than 1, U19A-5 will be true and the latch will record a drop-channel-greater-than-1 condition.

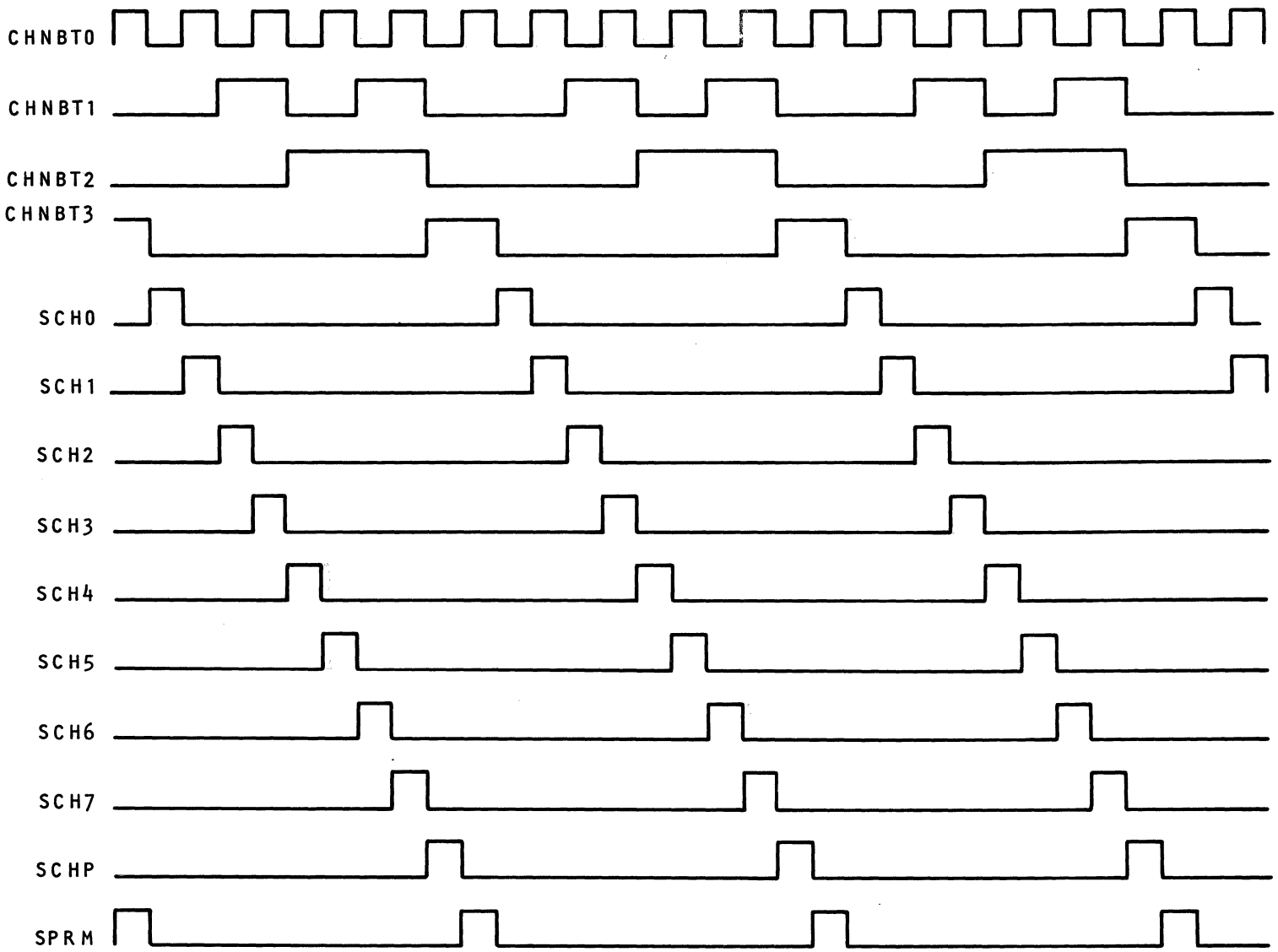


Figure 5-18. Channel Select Timing

Revised

5-83. The count-8 condition is also sampled by the register to produce the signal ENV. If the counter fails to reach state 8, it means that at least two channels are active. Therefore, the signal ENV will be asserted. This signal is used by the block detection logic and also by the read clock selection logic to enable the read clock source to be the input data rather than the crystal write clock. The three drop channel conditions, drop channel equal to 0 (DCEQ0), drop channel equal to 1 (DCE01), and drop channel greater than 1 (DCG11) are used by the error correction and format error logic for correcting parity errors or for detecting uncorrectable read errors.

5-84. The combination of OR gate U17C and J-K flip-flop U18B forms an any-1's detector. SBFLL, generated by the skew buffer control logic, indicates that a read-in is in process and that the skew buffer has filled its last location on this particular track. Should the signal be true for any of the nine channels, flip-flop U18B-6 will be set true. The state of this flip-flop is sampled at frame time by register U20A. Should the register be set, indicating that at least one skew buffer location has been filled, RDOUTSB (TP 54) will be set true for one frame period. This signal will force the readout of one character from the skew buffer. In addition, the signal SRDOUT will clear the preamble test and set the read data state of the block format control.

5-85. PE Detectors (Sheets 16-24, Drawing No. 352040-300 and Figure 5-19). The PE data detectors are duplicated nine times, once for each data channel. Their function is to synchronize with the incoming data stream, recover the data transition, and ignore the phase transition. The logic is clocked synchronously by the signal RDCLK, which occurs at 24 times the nominal character frequency (24 times for each data transition). Referring to sheet 19 the PE data detector logic outputs some signals not generated by seven of the other data channels. However, the internal logic is identical in all nine tracks.

5-86. Phase-encoded read data from the transports is applied to U16P-5. This data is synchronized by register U17V and phase-delayed by one clock period. The output of exclusive-OR gate U18W is a pulse for each transition of the input data. Before the block has been detected, MKIDETE will be false, causing flip-flop U18L-10 to be reset and U20N-1 to be asserted high. The transition pulse is then routed to U18D-2. U18D-1 is initially high, since *BLKDET does not occur for at least four character periods after the start of the preamble. NAND gate U18D will assert the parallel load input on U17E and the K input of J-K flip-flop U17M, thereby resetting both the counter and the J-K flip-flop on the next clock cycle. When the counter resets, *CHDROP2 will go high for every input data transition until Mark One has been detected. Mark One is detected by the absence of a phase transition before the all-1's character which separates the 40 preamble 0's from the data portion of the record. The absence of this phase transition allows CHARGATE2 to go set for the first time, thereby allowing the transition on U18W-6 to be applied to the J input of the DDRDY flip-flop.

5-87. Once Mark One has been detected, U20N-1 will be high only when CHARGATE2 is true (that is, when a gated transition is expected). Therefore, when the preamble portion of the record is completed, transition pulses on U20N-3 occur only for data transitions. The transition pulse is applied to the DDRDY2 flip-flop and causes it to go set, indicating that a data transition has been received from the tape transport for this channel. Simultaneously, the DDATA2 flip-flop samples the polarity of the data at the time this data transition occurs. Hence, DDATA2 corresponds to the actual data bit and will be sampled at channel 2 time. Subsequently, both flip-flops will reset. Note that the logic will operate correctly even if the data transition occurs at channel 2 time. Also, note that it is impossible for a DDRDY2 indication to occur unless a Mark One has been detected.

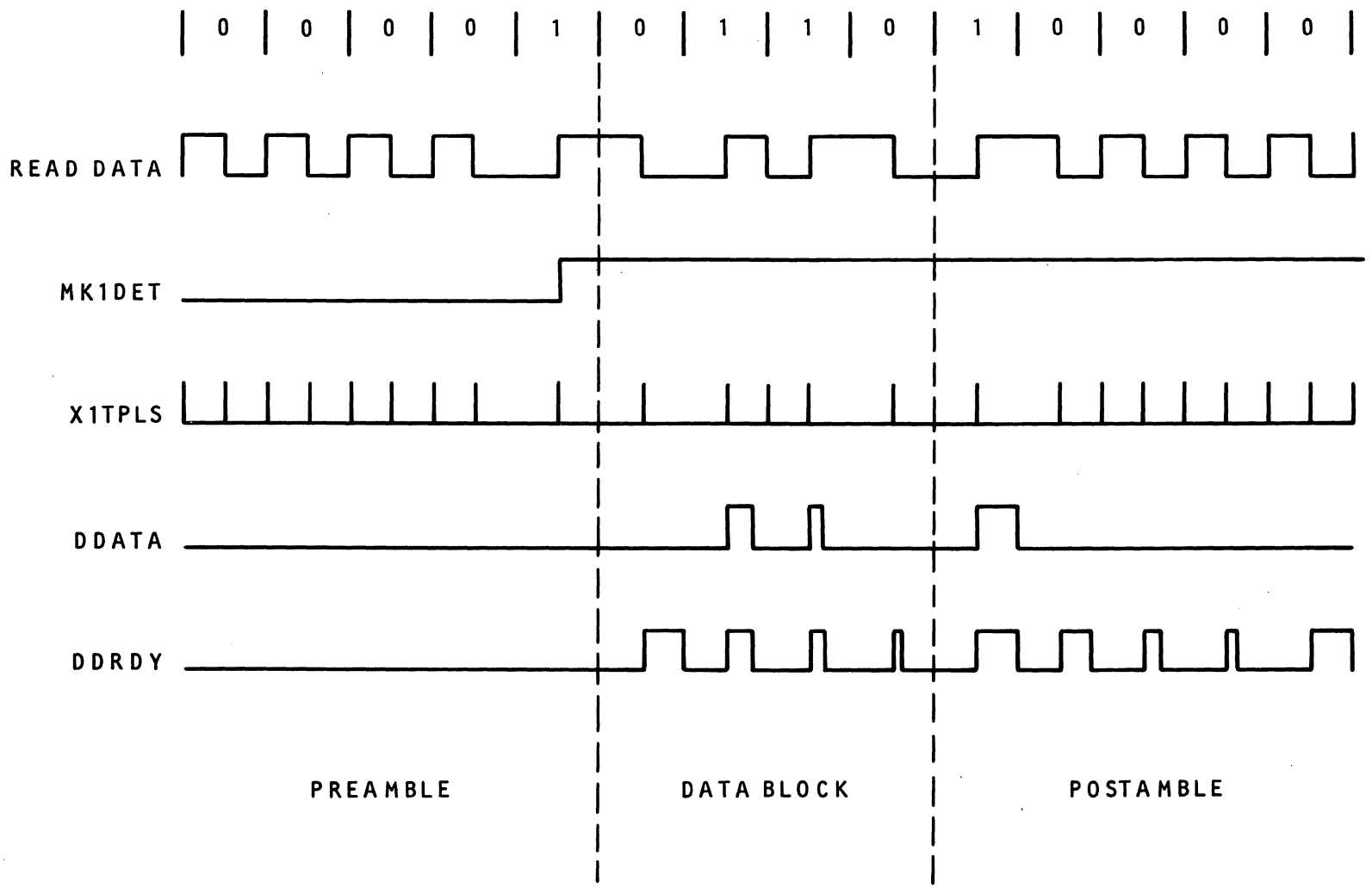


Figure 5-19. PE Detector

Revised

5-88. It is possible that a channel will drop out during a data record, due to deficiencies of the media whereby the input envelope fails below threshold. Since data transitions must always occur at least once per character time in phase encoding, it can be assumed from the absence of the data transition that a channel drop condition has occurred. Absence of this data transition will allow counter U17E, together with its extensions, U17M and one location of U17V, to reach a count 31. This is detected by NAND gate U20V, which causes CHDROP2 to be asserted. When CHDROP2 is asserted, U20D-12 will go low and, since a block detect is present, pin 11 will also go low. This prevents transition pulses from being gated through NAND gate U18D. Hence, the counter stalls at a count 31 condition, and CHDROP2 remains asserted. This condition will evoke error correction on this track. After block detection, a channel which is dropped remains dropped for the remainder of the data record.

5-89. Skew Buffer (Sheet 29, Drawing No. 352040-300). The skew buffer is a first-in first-out type of storage for 10 data channels, of which only nine are actively used. The tenth data channel is required to simplify detection and counting operations, such as parity and drop channel. The two major outputs from the skew buffer are DATAOUTSB and SBFLL. The skew buffer is capable of writing and reading information simultaneously within the same frame period. It samples information for input on the nine data channels. This is accomplished through the multiplexer consisting of U16H, U16F-6 and U16F-8. U16F-8 (TP44, DATARDY) will be true for one clock period. Whenever the corresponding data channel has a bit of information to be entered into the skew buffer, the bit is on TP 45, DATAINSB. DATAINSB is constructed from the output of the phase detectors, which are time multiplexed coincidentally with the data-ready signals. The data signals have no meaning at all if their corresponding ready signals are not asserted. The polarity of the data is reconstructed through exclusive OR gate U19P. When tape direction is forward, *REV is high and the exclusive OR inverts the signal before inputting the data to the skew buffer. In a forward direction, a low on 16F-11 is a data bit 1.

5-90. The skew buffer consists of four shift registers, each 10 bits in length. The first shift register is composed of U15B, an eight-state shift register, together with one circuit of register U16C (input pin 6 and output pin 7) and one circuit or register U16D (input pin 6 and output pin 7). The next register is composed of eight-bit shift register U17A and one location each of U16C and U16D. The third shift register is composed of eight-bit shift register U16A and one location each of U16C and U16D. The last register is composed of eight-bit register U15A, together with one location each of U16C and U16D.

5-91. When no information is to be entered, these four shift registers recirculate through the A inputs of multiplexer U15C. However, when a bit of information is to be entered, indicated by a high on *TP 44 for one clock period, the multiplexer selects inputs B instead of A. This causes all information in the particular location of each 10-bit shift register to be transferred to the register to its left. The data bit is then entered into the first shift register U17A. The information which was in the last register, U16D-10, is discarded.

5-92. When information for any particular channel has been entered into all four shift registers, the skew buffer is said to be full. This condition is detected by the fact that an address of the next location in the skew buffer to be filled is maintained by operation of two ten-bits shift registers in parallel with the four data-shift registers.

5-93. Initially, all four shift registers will be cleared until RDENBLE goes true. When the first bit of data is to be entered, register U16D-12 and 5 are low, indicating that the bit is to be entered into location 0. U16D-12 is the least-significant bit. Pins 6 and 2 of U16E, a full adder, are both low. Assuming there is no readout of the skew buffer in process, AND gate U15E is low. However, since the skew buffer is being read into, U16E-7, the carry input to the full adder, is true. Hence, the output of the full adder will be a binary 1. That is, pin 4 will be high, and pin 1 will be low. Following these lines around to the eight-bit shift registers, shift register U16B will have a high input and shift register U17B a low input. Therefore, the next time this channel becomes available for entering information the address presented will be address 1, whereas it was formerly address 0.

5-94. This process continues for all nine channels until such time as one or more channels have four bits of information entered into their corresponding skew buffers. At this time, the address on register U16D-12 and -5 will be 3, both high. Therefore, the corresponding inputs to adder U16E-8 and -2 will both be high. Again, assuming an input (TP 44) is true, the outputs of the adder will both be low, and the output of NOR gate U15F-1 will be true. This, together with the fact that TP 44 is true, produces a skew-buffer-full indication on U15E-11. This condition is latched and, at the beginning of the next frame period, will produce a readout of the skew buffer.

5-95. Information is read out of the skew buffer by multiplexer U15-D. The information contained in the skew buffer is presented through the four inputs of this multiplexer, pins 6, 3, 4, and 5. The address of the next location to be entered into is presented to the multiplexer on pins 14 and 2. For its respective channel, the address bits point to the next location where data is to be entered. The address of information to be read out is therefore one less this address. For example, consider that the next location to be written into is address 3, pins 14 and 2 are both high on U15D. The multiplexer selects U15D-3 as the data to be output. Looking at the shift register, this is actually address 2. This bit of information is output from the skew buffer on DATAOUTSB (TP 47). This readout process continues for the entire frame period, until one data bit of information has been extracted from each of the nine channels. While this is taking place, readout buffer U15E-10 is high. Since there is no channel drop condition, U15E-9 is high. This has the effect of subtracting one from the next address to be entered into for each of the nine data channels. Therefore, one location from each skew buffer has been emptied.

5-96. Adder U16E will produce the correct address if both the readout and read-in skew buffers are high simultaneously. In this case, the next address to be entered is the same as the previous address. Since the read clock operates at a frequency 24 times the nominal character frequency and each channel is sampled at each 10 read clocks, the effective sampling rate for each channel is 2.4 times the nominal character frequency. This sampling rate allows for considerable peak shift in the input data. Should a channel be dropped, it is not desirable to have a skew-buffer-full indication for that channel. It is desirable to have a logic 0 on DATAOUTSB so that this channel can be corrected if it is a single-channel dropout. This is accomplished by CHNDROP U15D-1 and -15 together with *CHNDROP on U15E-9. Note that channel drop, as discussed previously, is always true at frame time. Using this mechanism, therefore, DATAOUTSB and SBFLL are both false at frame time.

5-97. Error Logic (Sheet 30, Drawing No. 352040-300). This circuitry contains four registers, of which three are organized as 10-bit shift registers and the last as a parallel-in, parallel-out register. The 10-bit shift registers are very similar to those used in the skew buffer. Their purpose is to provide a three-character delay in order to permit calculation of actual parity and correction of data for single-frame drop-out

conditions. In addition, they provide a sufficient delay for detection of the all-1's character followed by two all-0's characters, which indicates the end of the data portion of a data record and the beginning of the postamble period.

5-98. Assuming the data in the four registers is static, that is, that data is not currently being read out of the skew buffer, the RDOUTSB buffer on U11L-1 is low. Therefore, the output of R1, U12G-12, is routed back as data input to R1, U13L-2. The output of R2 is routed to the input of R2, and the output of R3 is routed to the input of R3. The data in the four registers remains static. Should a readout skew buffer occur, U11L-1 will be high. The effect is to route DATAOUTSB to the input of register 1, U13L-2. The output of register 1 will be routed to the input of register 2, U13N-2, and the output of register 2 will be routed to the input of register 3, U13M-2.

5-99. Finally, the contents of register 3 will be transferred to the register composed of U12M and U12N. This is the output register for data going across to the controller. Should a drop channel condition exist, the data out of the skew buffer going into register 1 on a readout skew buffer will be forced low for the channel. As the data is being transferred into data register 1, the parity detection circuits are calculating the parity of the resulting data character, which may be even or odd. Following this, as the erroneous data character is read into register 2 from register 1, the complement of the parity obtained in the previous operation is substituted for the data bit in the erroneous channel. This is accomplished by gates OR U13C-8 and NOR U15F-4.

5-100. Read Strobe Pulse Generator. NOR gate U15F-10 and J-K flip-flop U13A comprise a pulse generator for read strobes. As noted previously, RDSTRBE is a function which goes true when the first valid data character is tranferred to the output register. At this time, RDOUTSB is valid also. Once SCH1 is true, flip-flop U13A-10 is set. This flip-flop will be reset at SCH7 time, the result being a read strobe pulse of 1 microsecond, minimum, generated at a data rate of 125 ips. If no format error exists, the read strobe will be gated out to the controller interface.

5-101. Other Error Logic and Related Functions. Immediately below the read strobe driver on the schematic are the nine drivers for the data lines themselves, followed by the driver for the file mark detector and the driver for IDBRST. A logic function which combines the test ID burst is performed on the front end of the IDBRST. This operation affirms that the transport is ramping up on the initial gap and that the ID burst condition has been met.

5-102. The next driver is the corrected error driver, which indicates that a parity error was detected along with one dropped channel. The next two drivers are wire ORed on the output and indicate a hard error function. The first hard error is a parity error detected with no dropped channel (hence, there is no point in correcting the parity error). The second hard error is a parity error.

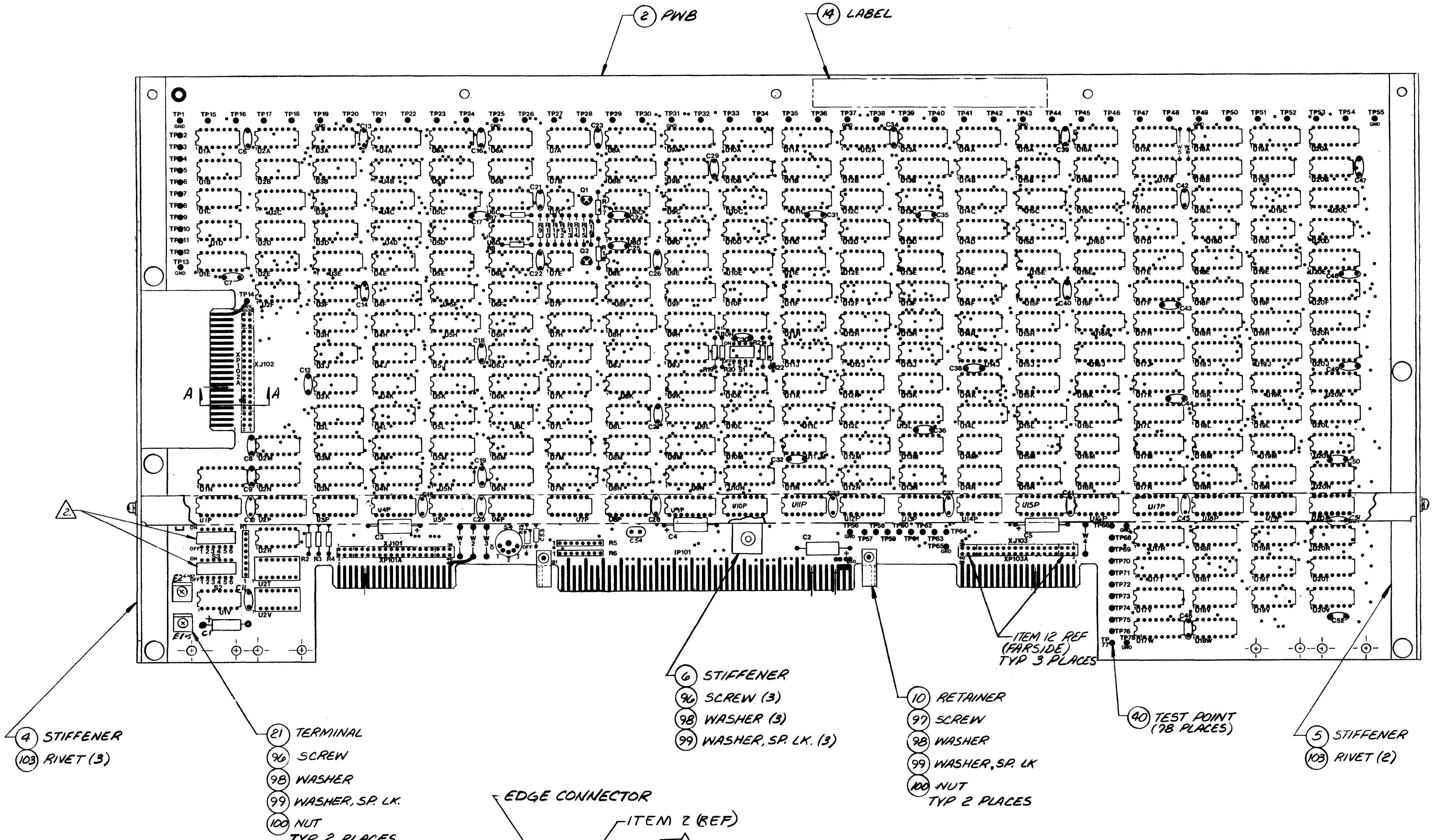
SECTION VI

ENGINEERING DOCUMENTATION

The parts list, schematic diagrams, and assembly drawing for the dual mode embedded formatter are included in the remainder of this section. Engineering documentaion applicable to the configuration of the transport to which this manual is assigned, where different from that in the basic manual, is presented in the special-configuration supplement immediately following this addendum.

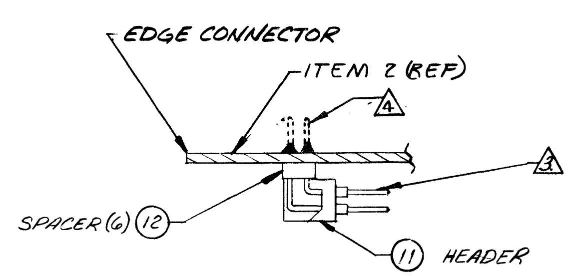
160001-000 REV AL

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
A	ENG. REL	J.M.	2/23/79	SGS	2/26/79
B	INC ECO 5366	WN	4/4/79	[illegible]	[illegible]
C	INC ECO 5367	WN	4/4/79	[illegible]	[illegible]
D	REWORK PER ECO 5539	LVS	5/1/79	[illegible]	5/1/79
E	INCORP ECO 6253	CW	9/24/79	[illegible]	9-24-79
F	INCORP ECO 6417	CW	11/12/79	[illegible]	11-21-79
G	INCORP ECO 6443	CW	11/12/79	[illegible]	11-21-79
H	INCORP ECO 6591	CW	11/12/79	[illegible]	11-21-79
J	INCORP ECO 6658	RL	11/12/79	[illegible]	11-21-79
K	INCORP ECO 6744	CW	11/21/79	[illegible]	11-21-79
L	INCORP ECO 6901 (REWORK ONLY)	J.G.	1-18-80	[illegible]	1-21-80
M	INCORP ECO 6945 (DOC CHG ONLY)	RL	2-12-80	[illegible]	2-13-80
N	INCORP ECO 7026	RL	2-12-80	[illegible]	2-13-80
P	INCORP ECO 7039	RL	2-12-80	[illegible]	2-13-80
R	INCORP ECO 7104	RL	2-12-80	[illegible]	2-13-80
S	INCORP ECO 7159	Jim R.	4-18-80	AA	4/21/80
T	INCORP ECO 7201	Jim R.	4-18-80	AA	4/21/80
U	INCORP ECO 8226	SGS	10-16-80	[illegible]	10-21-80
V	INCORP ECO 8457	LJ	11-11-80	[illegible]	11-17-80
W	INCORP ECO 8747	LJ	12-9-80	[illegible]	12-16-80
Y	INCORP ECO 8908	LJ	12-22-80	[illegible]	12-23-80
Z	INCORP ECO 9311	LJ	2-12-81	[illegible]	2-17-81
AA	INCORP ECO 10170	EC	7-22-81	[illegible]	8-10-81
AB	INCORP ECO 10410	EC	7-22-81	[illegible]	8-10-81
AC	INCORP ECO 11287	FN	9-26-81	[illegible]	[illegible]
AD	INCORP ECO 12342	UA	1/29/82	[illegible]	[illegible]
AE	INCORP ECO 13486	EC	6/29/82	[illegible]	[illegible]
AF	INCORP ECO 13897	EC	8/31/82	[illegible]	[illegible]
AG	INCORP ECO 13995	EC	9/28/82	[illegible]	10-1-82
AH	INCORP ECO 14989	EC	2/1/83	[illegible]	2/18/83
AJ	INCORP ECO 15320	EPC	3/18/83	[illegible]	3/[illegible]/83
AK	INCORP ECO 16605	EPC	9/20/83	[illegible]	10/5/83
AL	INCORP ECO 16718	EPC	9/[illegible]/83	[illegible]	10/3/83



NOTES:

1. FOR SCHEMATIC SEE 360001-300.
2. DO NOT FLOW SOLDER DIP SWITCHES S1, S2 & S3. ORIENT SWITCH NUMBERS WITH SILKSCREEN NUMBERS ON PWB.
3. CLIP PINS ON HEADERS (ITEM 11) FOR KEYING AS FOLLOWS: PIN 28 FOR XJ101, PIN 8 FOR XJ102, & PIN 38 FOR XJ103.
4. CUT PINS ON COMPONENT SIDE FOR MAX PROTRUSION OF .10
5. ON SOLDER SIDE, FLUSH CUT IC PINS 1 THRU 7 OR 1 THRU 8 OF U3P, U4P, U5P, U14P & U15P



SECTION A-A
HEADER INSTALLATION
TYP 3 PLACES
SCALE: 2/1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS .XX = ± .XXX = ± ANGLES ±	APPROVALS	DATE	Cipher Data Products SAN DIEGO CALIF
	DWN [illegible]	2/23/79	TITLE PWB ASSY-FMTR, DUAL MODE, EMB. BASIC
	CHK [illegible]	2/23/79	
	MECH ENG [illegible]	2-26-79	SIZE D · CODE IDENT NO. 32274 · DRAWING NO. 160001-000 · REV AL
	ELEC ENG [illegible]	2/26/79	
	MFG ENG [illegible]	2/26/79	
	QC [illegible]	2/26/79	
DO NOT SCALE DRAWING	DOC CHK [illegible]	2/26/79	SCALE 1/1 · SHEET 1 OF 1

TP1 GND TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 GND TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP40 TP41 TP42 TP43 TP44 TP45 TP46 TP47 TP48 TP49 TP50 TP51 TP52 TP53 TP54 TP55 GND

A A

XJ102 XP102A

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54

Q1 Q2

R1 R2 R3 R4 R5 R6 R19 R20 R21 R22

S1 S2 S3

W1 W2 W3 W4 W5

E1 E2

B1

IP101

XJ101 XP101A

XJ103 XP103A

TP55 TP56 TP57 TP58 TP59 TP60 TP61 TP62 TP63 TP64 TP65 TP66 TP67 TP68 TP69 TP70 TP71 TP72 TP73 TP74 TP75 TP76 TP77 TP78 GND

U1P U2P U3P U4P U5P U6P U7P U8P U9P U10P U11P U12P U13P U14P U15P U16P U17P U18P U19P U20P

U1R U2R U3R U4R U5R U6R U7R U8R U9R U10R U11R U12R U13R U14R U15R U16R U17R U18R U19R U20R

U1T U2T U3T U4T U5T U6T U7T U8T U9T U10T U11T U12T U13T U14T U15T U16T U17T U18T U19T U20T

U1V U2V U3V U4V U5V U6V U7V U8V U9V U10V U11V U12V U13V U14V U15V U16V U17V U18V U19V U20V

SPARE GATE LIST

I.C.	TYPE	NOTES	QTY
U1A	'51	2 WIDE	1
U5E	32		1
U5J	14		3
U7H	86		1
U9K	174	SEE SH. 7	1
U11M	7438		1
U12A	174	SEE SH. 7	3
U12M	378	SEE SH.30	3
U13C	32		1
U15J	74		1
U18P	174	SEE SH. 24	1
U20A	378	SEE SH. 26	1

LAST REF DESIG. USED
C54
E2
Q2
R23
S4
TP-78
W6

SPEED HEADER VALUES

SPEED	C1	C2	C3	R1
12.5	1uf	470Pf	1uf	1K
18.75	1uf	330Pf	1uf	1K
25	.47uf	270Pf	.22uf	1.3K
37.5	.47uf	180Pf	.47uf	820Ω
45	.47uf	120Pf	.47uf	820Ω
75	.47uf	68Pf	N/A	1K
125	.47uf	33Pf	.47uf	430Ω

TRANSPORT ADDRESS SW S4

POSITION	TRANSPORT ADDRESS
0	0
1	1
2	2
3	3
OFF	OFF

JUMPER OPTIONS

JUMPER	FUNCTION
W1	ROUTES IWARS TO J101
W2	SUPPLIES +5 VOLTS TO J101-5
W3	FORCES IRTH2 TRUE WHEN OVER DATA PORTION OF RECORD(PE ONLY)
W4	ALLOWS USE OF DRIVES WITHOUT READ DATA STROBES

DENSITY SELECTION SW SETTINGS

DENSITY	S1-1	S1-2
800/200	OFF	ON
800/556	ON	ON
556/200	OFF	OFF

FMTR ADDRESS SELECTION

ADDRESS	S1-4
0	OFF
1	ON

SPEED SELECTION SWITCH SETTINGS

SPEED	SWITCHES S2 & S3 — 1	2	3	4	5	6	TP-38 FREQ.(MHZ)
125	ON	ON	OFF	OFF	OFF	OFF	10.8
112.5	OFF	ON	OFF	OFF	OFF	OFF	9.72
75	OFF	OFF	ON	OFF	OFF	OFF	6.48
50	ON	OFF	OFF	ON	OFF	OFF	4.32
45	OFF	OFF	OFF	ON	OFF	OFF	3.89
37.5	OFF	ON	OFF	ON	OFF	OFF	3.24
25	OFF	OFF	OFF	OFF	ON	OFF	2.16
25(ALT)	ON	ON	OFF	OFF	ON	OFF	2.16
22.5	OFF	ON	OFF	OFF	ON	OFF	1.94
18.75	OFF	ON	ON	OFF	ON	OFF	1.62
12.5	OFF	ON	OFF	OFF	OFF	ON	1.08
12.5(ALT)	ON	ON	ON	OFF	OFF	ON	1.08

TEST POINT CROSSREFERENCE

MNEMONIC	T.P.	SH.	MNEMONIC	T.P.	SH.
BGNPRMBL	26	27	RDOUTSB	54	26
BLKDET	34	25	RDP	71	16
CCE	40	15	RDS	69	13
CCG	60	14	RDØ	72	17
CCT1	58	14	RD1	74	18
CCT2	62	14	RD2	75	19
CCT3	63	14	RD3	77	20
CCT4	64	14	RD4	76	21
CHDROP	51	26	RD5	68	22
CRCDLY	23	6	RD6	70	23
CRCE	21	6	RD7	66	24
CRCER	42	15	RSTRB	50	14
CRCPE	36	15	SFRM	52	26
DATAINSB	45	29	SGL	11	8
DATAOUTSB	47	29	SPDCLK	17	2
DATARDY	44	29	SPEED	28	8
DATAXFER	12	4	START GAP	10	4
DDI	57	8	TESTIDBRST	16	5
ENV	53	26	WMK1	7	6
EOBWDW	33	27	WMK2	5	6
FCD	39	14	WPRMZRS	24	6
FHPRMBL	32	27	WPSTMZRS	18	6
FHPSTMBL	35	27	WRTDATA	22	6
FMK	27	28	VPER	41	15
FMTR	30	27	7TR	61	8
GOAGN	2	4	+5 VOLTS	14	10
IDBRST	4	5	GND	1	10
LONG GAP	6	4	GND	13	10
LRCDLY	20	6	GND	19	10
LRCE	46	15	GND	25	10
NRCLK	38	2	GND	31	10
NRZ	59	8	GND	37	10
PARITY ERR	29	28	GND	43	10
PSTRECGAP	9	4	GND	49	10
RAMPDOWN	8	4	GND	55	10
RAMPUP	15	4	GND	56	10
RDCLK	73	31	GND	65	10
RDDATA	3	27	GND	67	10
RDENBL	48	25	GND	78	10

PARITY GENERATION

	SW S1-3
INTERNAL	OFF
EXTERNAL	ON

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
A	ENG RELEASE	JM	2-13-79	SGS	2-26-79
B	INC ECO 5370	VN	4-2-79		4/2/79
C	INC ECO 5541	VN	4-30-79		5/3/79
D	INC ECO 6419	LVS	11/30 80		11/10
E	INC ECO 6445	LVS	11/30 80		11/10
F	INC ECO 6747	LVS	11/30 80		11/10
G	INC ECO 6946	D.G.	1-18-80		1-21 80
H	INC ECO 8445	LJ	10-22 80		10-22 80
J	INC. ECO 8568	LJ	11-12 80		11-14 80
K	INC. ECO 11288	FN	9-26 81		9-30 81
L	INC. ECO 11927	EC	12-13 82		1-19 82
M	INCORP ECO 12334	UA	2/22/82		2-24-82

360001-300

REV M

REV STATUS: REV M M L C A M F B A M A G M M D A A A A A A A A
OF SHEETS: SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS		DATE
DWN		2/13/79
CHK		3/26/79
MFG ENG		2/26/79
QC		4/26/79
ENGR		5/24/79
PROD REL		2-26-79

DO NOT SCALE DRAWING

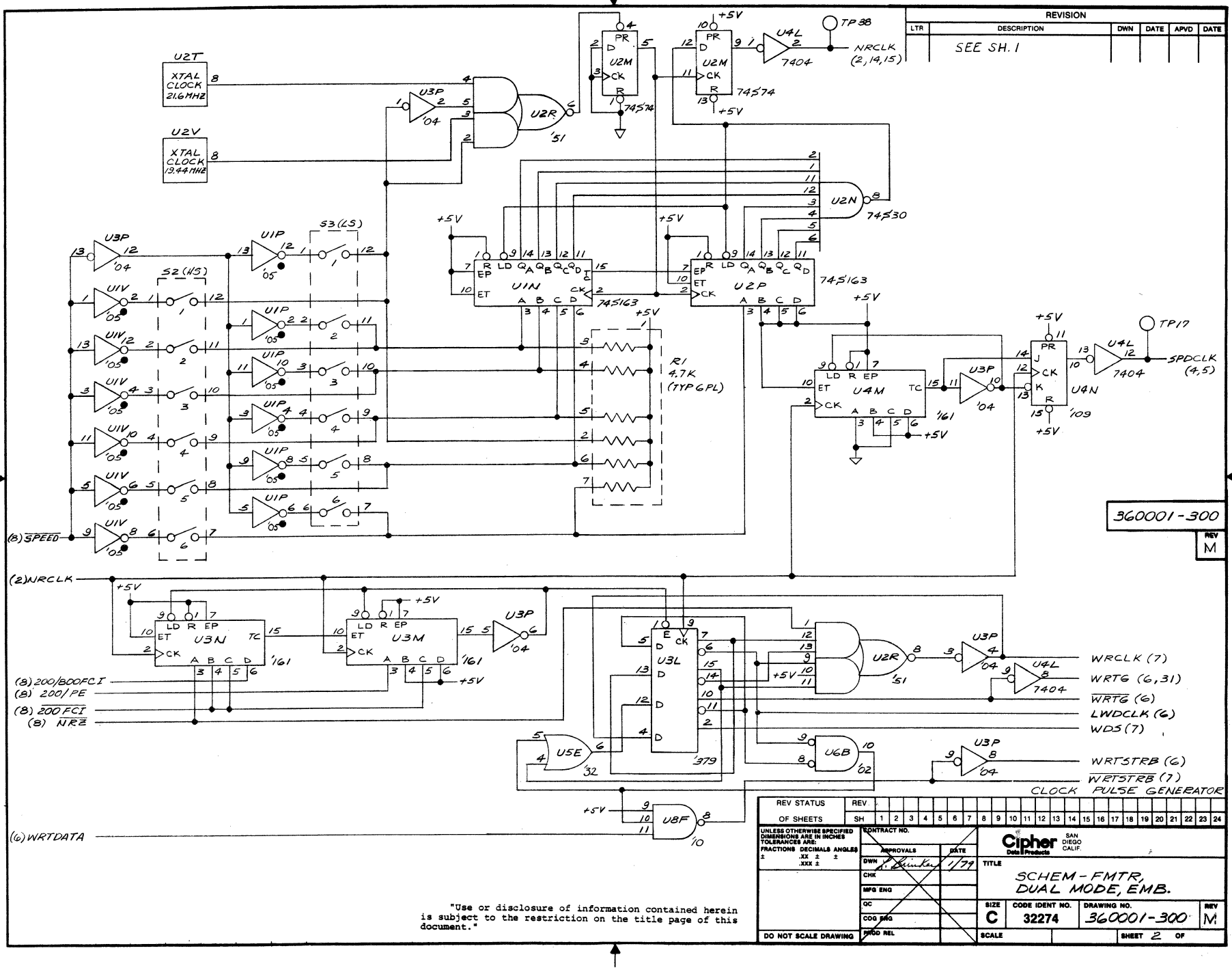
Cipher Data Products SAN DIEGO CALIF.

TITLE: SCHEM-FMTR, DUAL MODE, EMB

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	M

SCALE | SHEET 1 OF 32

REV STATUS CNTD OF SHEETS: REV A L A A C M H A | SH 25 26 27 28 29 30 31 32 33 34 35


REVISION
LTR DESCRIPTION DWN DATE APVD DATE
SEE SH. 1
U2T XTAL CLOCK 21.6MHZ
U2V XTAL CLOCK 19.44MHZ
U3P '04
U2R '51
U2M 74S74
U4L 7404
TP38
NRCLK (2,14,15)
U2N 74S30
U1P '05
S3(LS)
S2(HS)
U1V '05
U1N U2P 74S163
R1 4.7K (TYP 6PL)
U4M '161
U4N '109
TP17
SPDCLK (4,5)
(8) SPEED
(2) NRCLK
U3N U3M '161
(8) 200/800FCI
(8) 200/PE
(8) 200FCI
(8) NRZ
U3L '379
U5E '32
U6B '02
U8F '10
WRCLK (7)
WRTG (6,31)
WRTG (6)
LWDCLK (6)
WDS (7)
WRTSTRB (6)
WRTSTRB (7)
(6) WRTDATA
CLOCK PULSE GENERATOR
360001-300
REV M
REV STATUS
OF SHEETS
SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±
CONTRACT NO.
APPROVALS DATE
DWN J. Quinby 1/79
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
Cipher Data Products SAN DIEGO CALIF.
TITLE
SCHEM-FMTR, DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV M
SCALE
SHEET 2 OF
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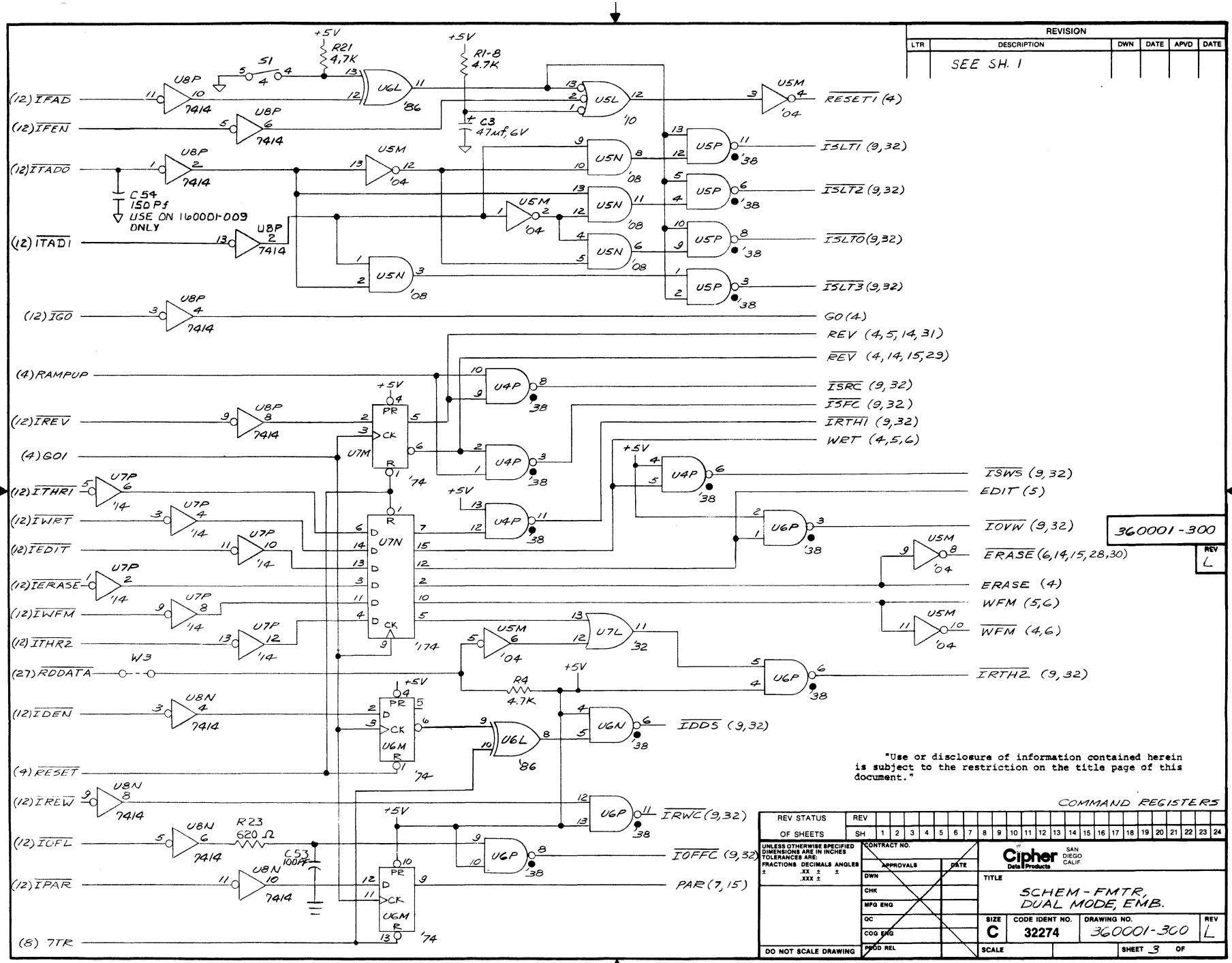
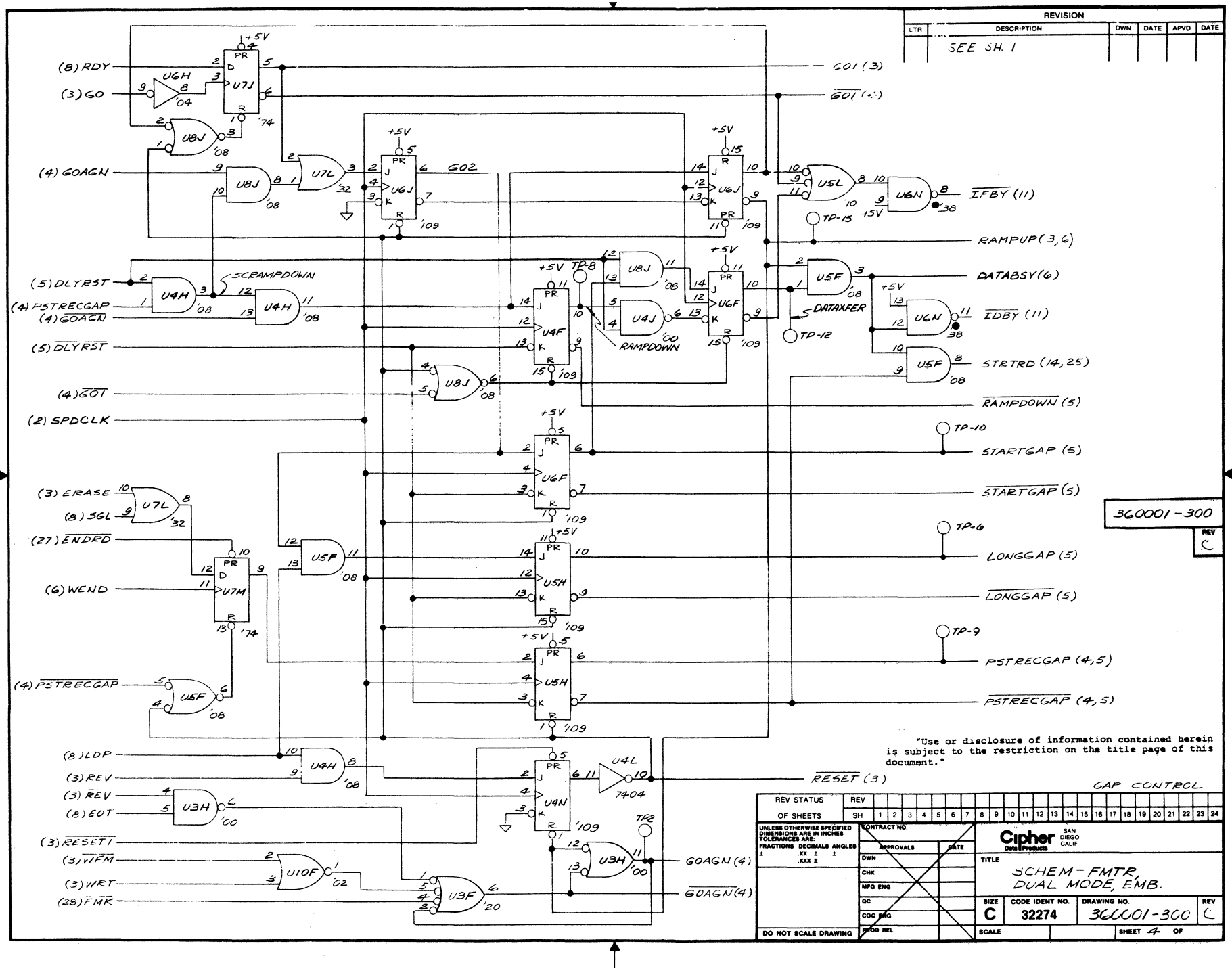

REVISION
LTR DESCRIPTION DWN DATE APVD DATE
SEE SH. 1
(12) IFAD
(12) IFEN
(12) ITADO
(12) ITADI
(12) IGO
(4) RAMPUP
(12) IREV
(4) GO1
(12) ITHR1
(12) IWRT
(12) IEDIT
(12) IERASE
(12) IWFM
(12) ITHR2
(27) RODATA
(12) IDEN
(4) RESET
(12) IREW
(12) ICFL
(12) IPAR
(8) TTR
R21 4.7K
R1-8 4.7K
C3 47uf, 6V
C54 150 Pf USE ON 160001-009 ONLY
C53 100PF
R23 620 Ω
R4 4.7K
RESET1 (4)
ISLT1 (9,32)
ISLT2 (9,32)
ISLT0 (9,32)
ISLT3 (9,32)
GO (4)
REV (4,5,14,31)
REV (4,14,15,29)
ISRC (9,32)
ISFC (9,32)
IRTH1 (9,32)
WRT (4,5,6)
ISWS (9,32)
EDIT (5)
IOVW (9,32)
ERASE (6,14,15,28,30)
ERASE (4)
WFM (5,6)
WFM (4,6)
IRTH2 (9,32)
IDDS (9,32)
IRWC (9,32)
IOFFC (9,32)
PAR (7,15)
"Use or disclosure of information contained herein is subject to the restriction on the title page of this document."
COMMAND REGISTERS
360001-300
REV L
REV STATUS
OF SHEETS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES
APPROVALS DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
CONTRACT NO.
Cipher Data Products SAN DIEGO CALIF.
TITLE
SCHEM-FMTR, DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV L
SCALE
SHEET 3 OF


REVISION
LTR DESCRIPTION DWN DATE APVD DATE
SEE SH. 1
(8) RDY
(3) GO
U6H '04
U7J '74
U8J '08
(4) GOAGN
U7L '32
GO2
U6J '109
GO1 (3)
GO1 (3)
U5L '10
U6N '38
IFBY (11)
TP-15
RAMPUP (3,6)
(5) DLYRST
U4H '08
SCRAMPDOWN
(4) PSTRECGAP
(4) GOAGN
U4H '08
U4F '109
TP-8
U8J '08
U4J '00
RAMPDOWN
U6F '109
U5F '08
DATABSY (6)
DATAXFER
TP-12
U6N '38
IDBY (11)
U5F '08
STRTRD (14, 25)
(5) DLYRST
(4) GOT
U8J '08
RAMPDOWN (5)
(2) SPDCLK
TP-10
STARTGAP (5)
(3) ERASE
(8) SGL
U7L '32
U6F '109
STARTGAP (5)
(27) ENDRD
U7M '74
U5F '08
U5H '109
TP-6
LONGGAP (5)
(6) WEND
LONGGAP (5)
TP-9
(4) PSTRECGAP
U5F '08
U5H '109
PSTRECGAP (4,5)
PSTRECGAP (4,5)
(8) LDP
(3) REV
(3) REV
(8) EOT
U4H '08
U3H '00
U4N '109
U4L 7404
RESET (3)
(3) RESET
(3) WFM
(3) WRT
(28) FMR
U10F '02
U3F '20
TP2
U3H '00
GOAGN (4)
GOAGN (4)
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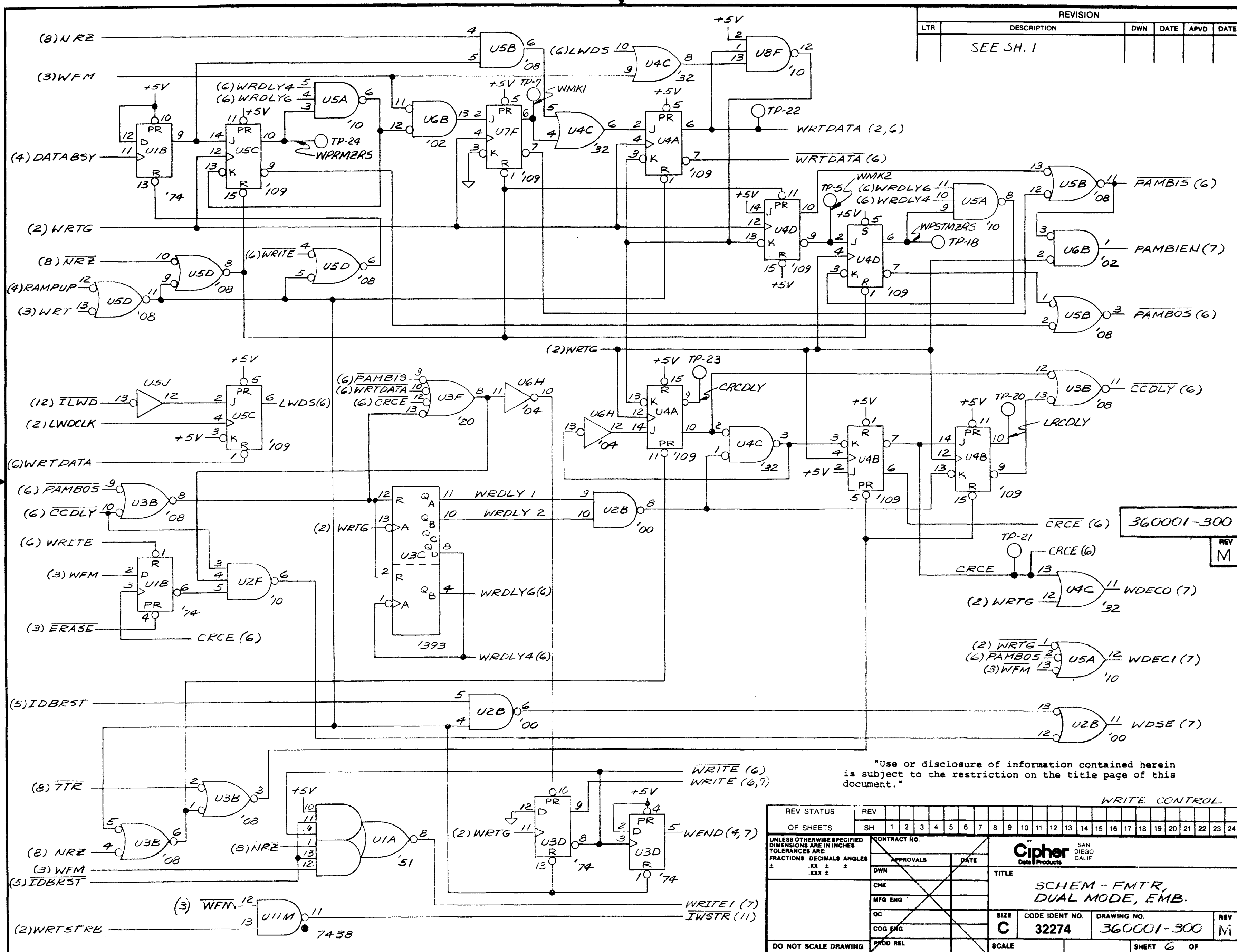
GAP CONTROL
REV STATUS REV
OF SHEETS SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±
CONTRACT NO.
APPROVALS DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
Cipher Data Products SAN DIEGO CALIF
TITLE
SCHEM-FMTR, DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV C
SCALE
SHEET 4 OF
360001-300
REV C


REVISION
LTR
DESCRIPTION
DWN
DATE
APVD
DATE
SEE SH. 1
(8) NRZ
(3) WFM
(4) DATABSY
(2) WRTG
(8) NRZ
(4) RAMPUP
(3) WRT
(6) WRDLY4
(6) WRDLY6
(6) WRITE
(6) LWDS
TP-7
WMK1
TP-22
TP-24
WPRMZRS
WRTDATA (2,6)
WRTDATA (6)
WMK2
TP-5
WPSTMZRS
TP-18
PAMBIS (6)
PAMBIEN (7)
PAMBOS (6)
(2) WRTG
TP-23
CRCDLY
TP-20
LRCDLY
CCDLY (6)
(12) ILWD
(2) LWDCLK
(6) WRTDATA
LWDS (6)
(6) PAMBIS
(6) WRTDATA
(6) CRCE
(6) PAMBOS
(6) CCDLY
(6) WRITE
(3) WFM
(3) ERASE
CRCE (6)
WRDLY 1
WRDLY 2
(2) WRTG
WRDLY6 (6)
WRDLY4 (6)
'393
CRCE (6)
360001-300
REV
M
TP-21
CRCE (6)
CRCE
(2) WRTG
WDECO (7)
(2) WRTG
(6) PAMBOS
(3) WFM
WDEC1 (7)
(5) IDBRST
WDSE (7)
(8) 7TR
(8) NRZ
(3) WFM
(5) IDBRST
(8) NRZ
(2) WRTG
WRITE (6)
WRITE (6,7)
WEND (4,7)
WRITE1 (7)
IWSTR (11)
(3) WFM
(2) WRTSTRB
7438
WRITE CONTROL

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REV STATUS	REV																								
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS — DATE — DWN — CHK — MFG ENG — QC — COG ENG — PROD REL

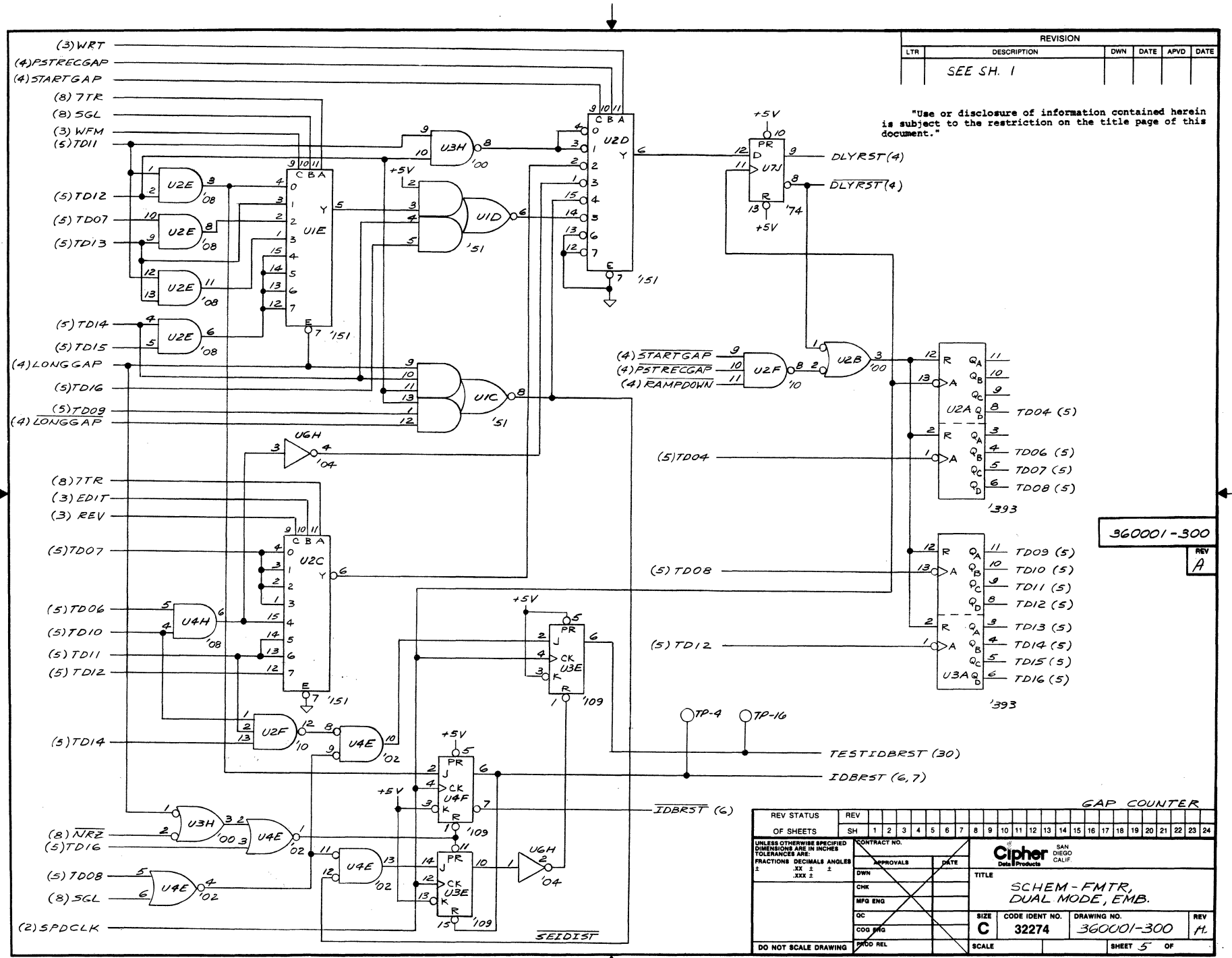
Cipher Data Products — SAN DIEGO CALIF

TITLE: SCHEM - FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	M

SCALE — SHEET 6 OF

DO NOT SCALE DRAWING



REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				

360001-300
REV A

GAP COUNTER

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

DO NOT SCALE DRAWING

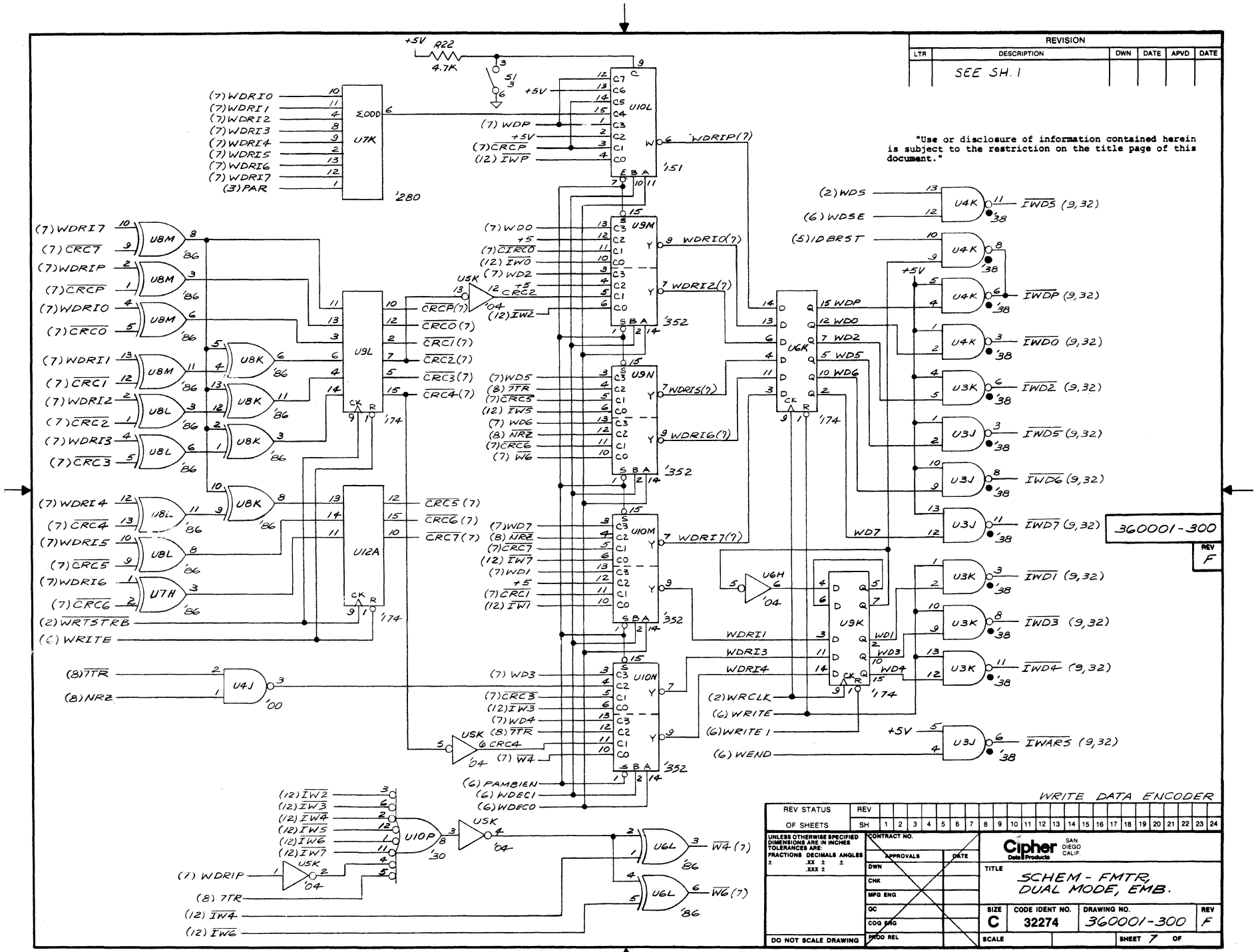
Cipher Data Products, SAN DIEGO CALIF.

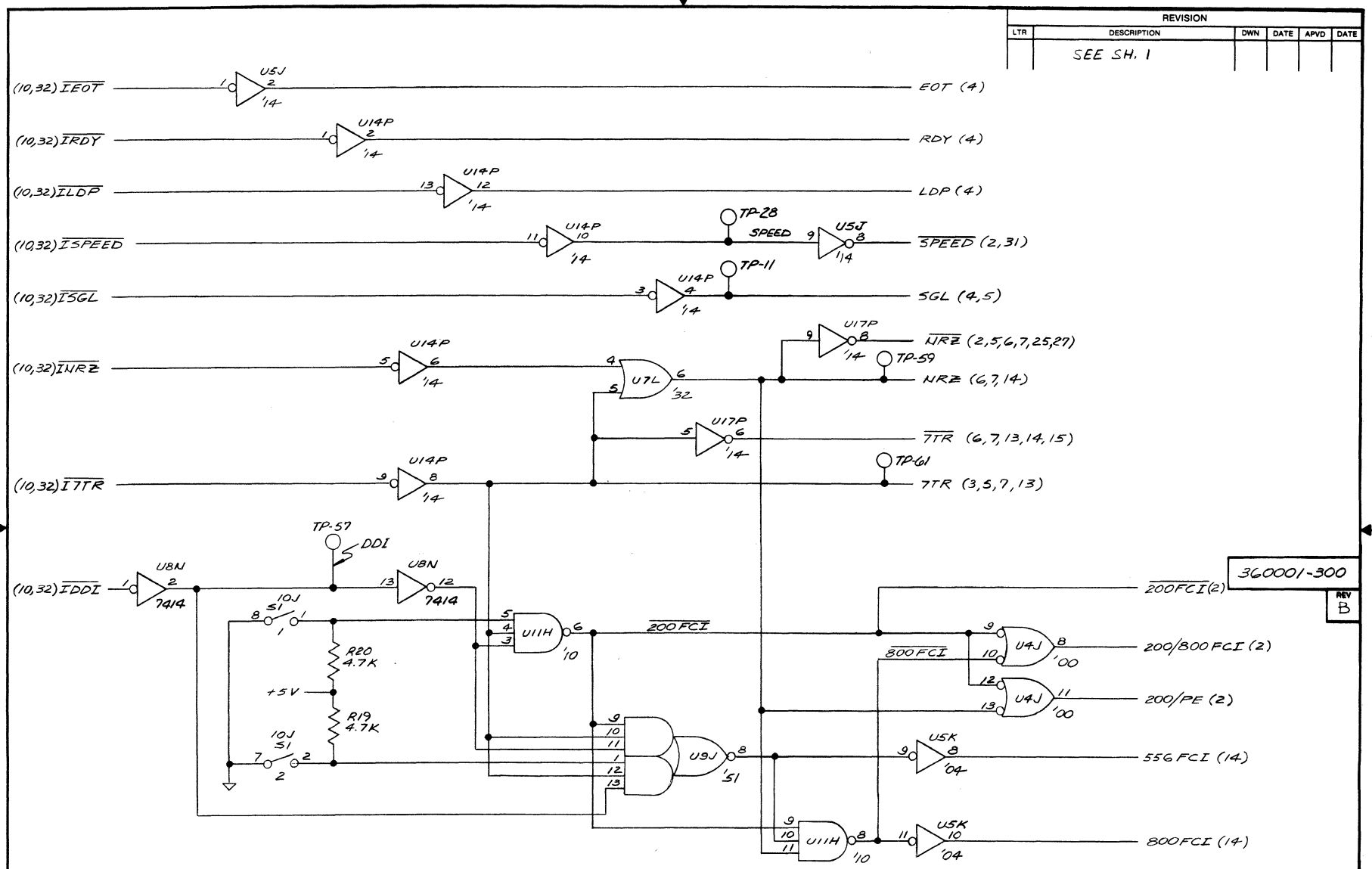
TITLE: SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

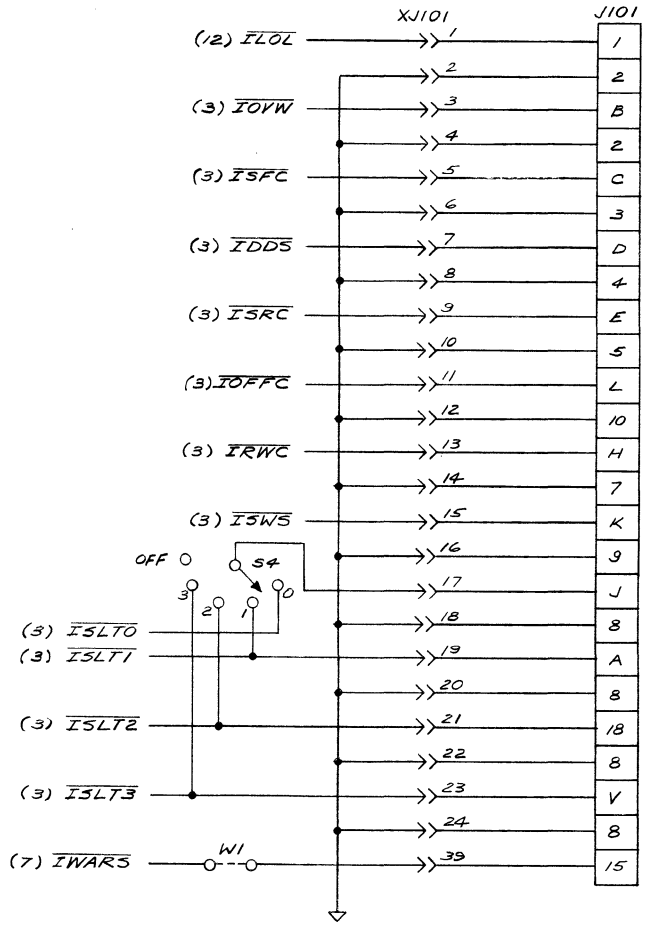
SCALE

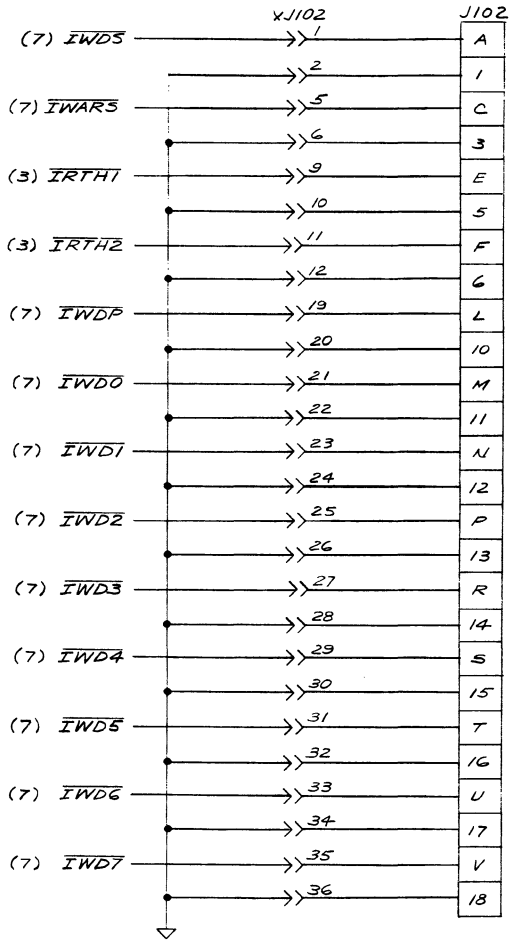
SHEET 5 OF


REVISION
LTR | DESCRIPTION | DWN | DATE | APVD | DATE
SEE SH. 1
"Use or disclosure of information contained herein is subject to the restriction on the title page of this document."
+5V R22 4.7K
U7K '280
U10L '151
U9M '352
U9N '352
U10M '352
U10N '352
U10P '30
U9L '174
U12A '174
U6K '174
U9K '174
U8M '86
U8K '86
U8L '86
U7H '86
U4J '00
U5K '04
U6H '04
U4K '38
U3K '38
U3J '38
U6L '86
(7) WDRI0
(7) WDRI1
(7) WDRI2
(7) WDRI3
(7) WDRI4
(7) WDRI5
(7) WDRI6
(7) WDRI7
(3) PAR
(7) WDP
(7) CRCP
(12) IWP
WDRIP(7)
(7) WDO
(7) CIRCO
(12) IWO
(7) WD2
(12) IW2
(7) WD5
(8) 7TR
(7) CRC5
(12) IW5
(7) WD6
(8) NRZ
(7) CRC6
(7) W6
(7) WD7
(8) NRZ
(7) CRC7
(12) IW7
(7) WD1
(7) CRC1
(12) IW1
(7) WD3
(7) CRC3
(12) IW3
(7) WD4
(7) CRC4
(7) W4
(6) PAMBIEN
(6) WDEC1
(6) WDEC0
WDRI0(7)
WDRI2(7)
WDRI5(7)
WDRI6(7)
WDRI7(7)
WDRI1
WDRI3
WDRI4
(2) WDS
(6) WDSE
(5) IDBRST
(2) WRTSTRB
(6) WRITE
(2) WRCLK
(6) WRITE 1
(6) WEND
CRCP(7)
CRCO(7)
CRC1(7)
CRC2(7)
CRC3(7)
CRC4(7)
CRC5(7)
CRC6(7)
CRC7(7)
IWDS (9,32)
IWDP (9,32)
IWDO (9,32)
IWD2 (9,32)
IWD5 (9,32)
IWD6 (9,32)
IWD7 (9,32)
IWD1 (9,32)
IWD3 (9,32)
IWD4 (9,32)
IWAR5 (9,32)
W4(7)
W6(7)
WRITE DATA ENCODER
360001-300
REV F
REV STATUS REV
OF SHEETS SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±
CONTRACT NO.
APPROVALS DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
Cipher Data Products SAN DIEGO CALIF.
TITLE SCHEM - FMTR, DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV F
SCALE
SHEET 7 OF



REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				





360001-300

REV A

FORMATTER TO TAPE DRIVE CONNECTOR

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

DO NOT SCALE DRAWING

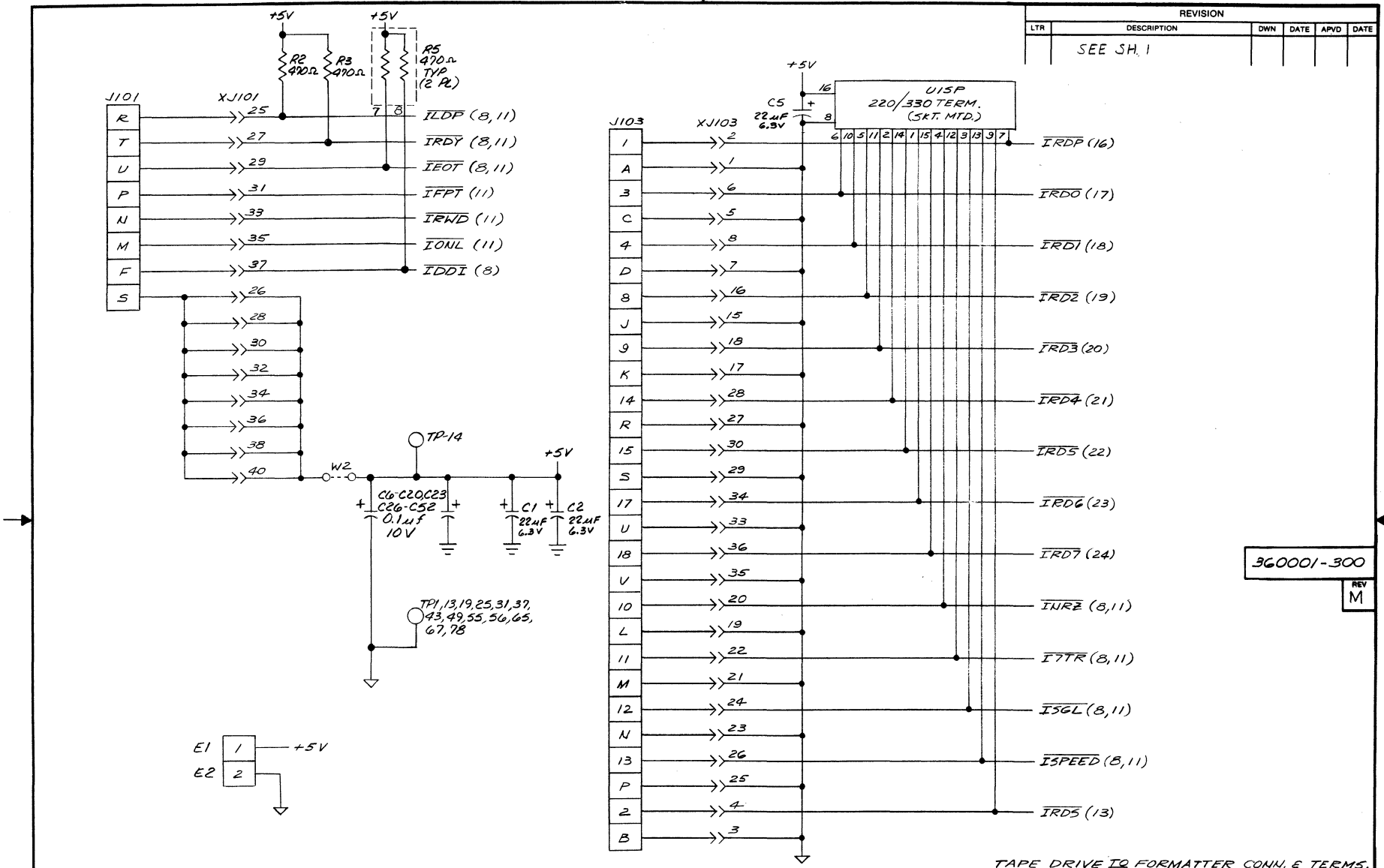
Cipher Data Products SAN DIEGO CALIF.

TITLE: SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE

SHEET 9 OF



REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				

360001-300
REV M

TAPE DRIVE IQ FORMATTER CONN. & TERMS.

REV STATUS	REV																						
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

DO NOT SCALE DRAWING

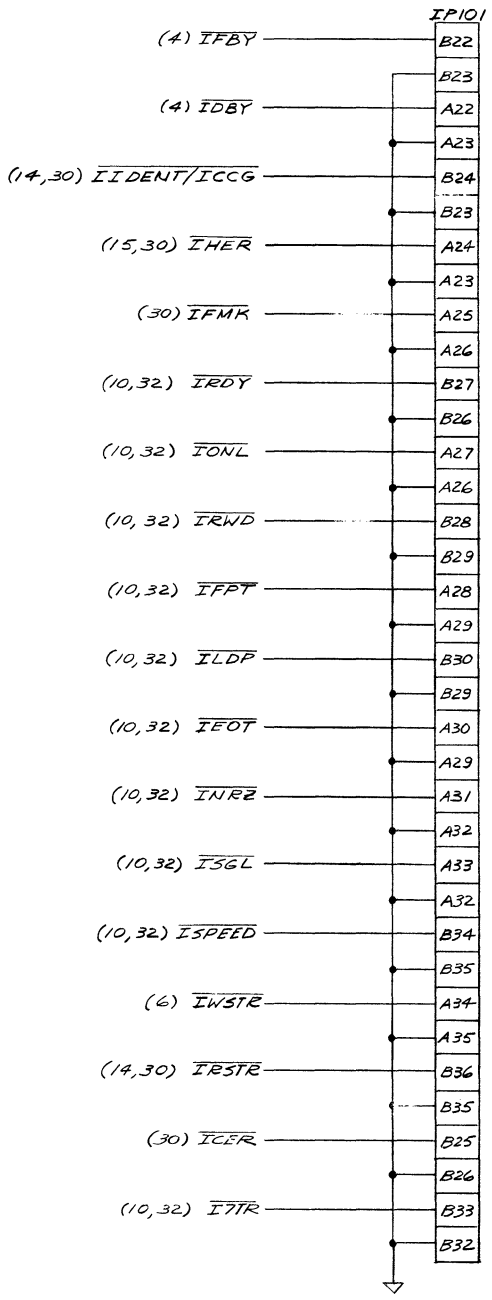
Cipher Data Products SAN DIEGO CALIF.

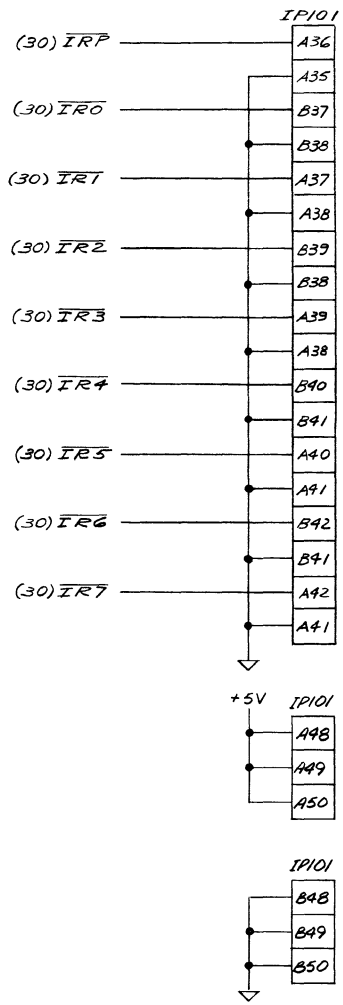
TITLE: SCHEM - FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	M

SCALE | SHEET 10 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				





FORMATTER TO CONTROLLER CONNECTOR

360001-300 REV A

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

DO NOT SCALE DRAWING

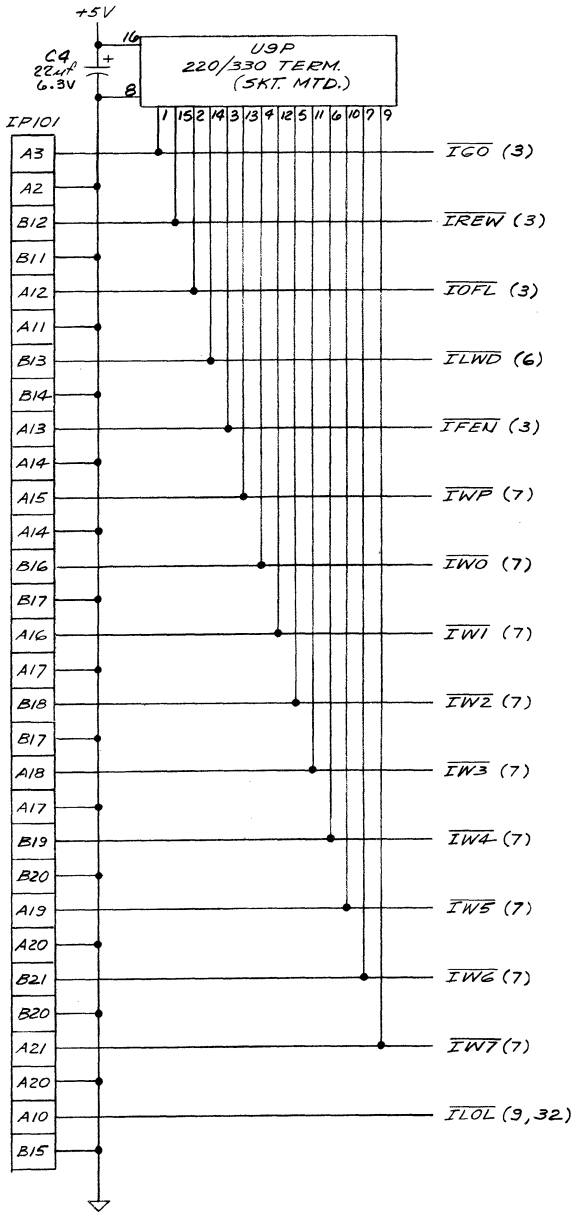
Cipher Data Products SAN DIEGO CALIF.

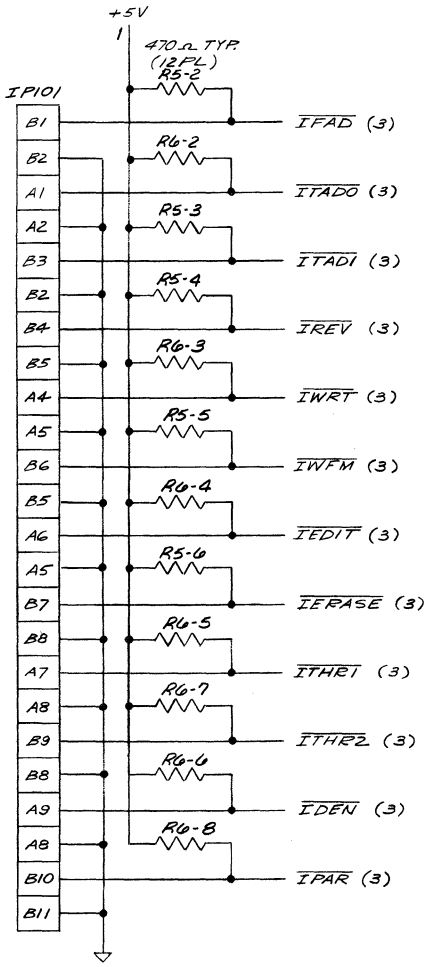
TITLE: SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE | SHEET 11 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				





360001-300
REV G

CONTROLLER TO FORMATTER CONNECTOR & TERMS.

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

CONTRACT NO.

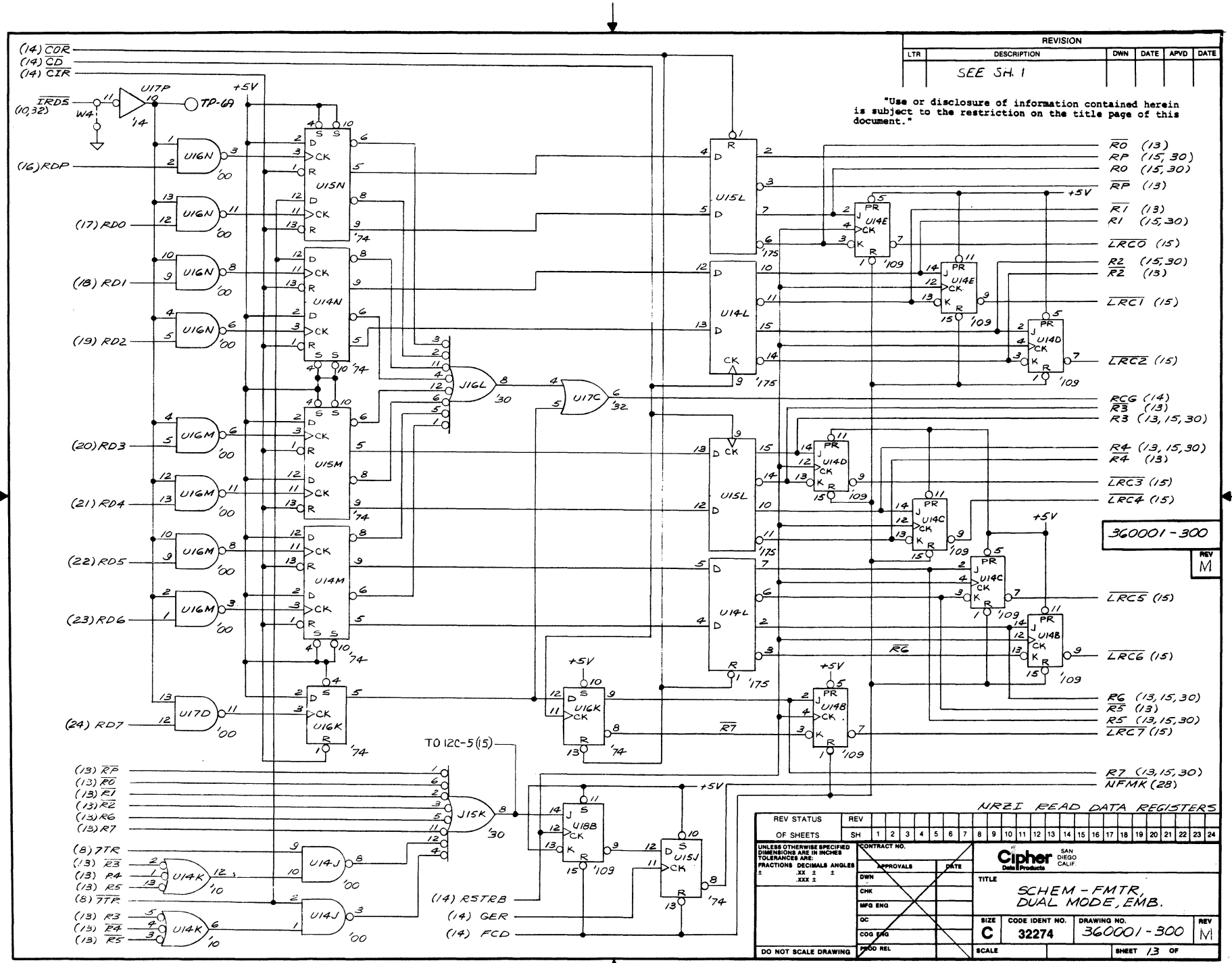
APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
MOD REL	

Cipher Data Products SAN DIEGO CALIF

TITLE: SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	G

SCALE | SHEET 12 OF



REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				

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360001-300 REV M

NRZI READ DATA REGISTERS

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

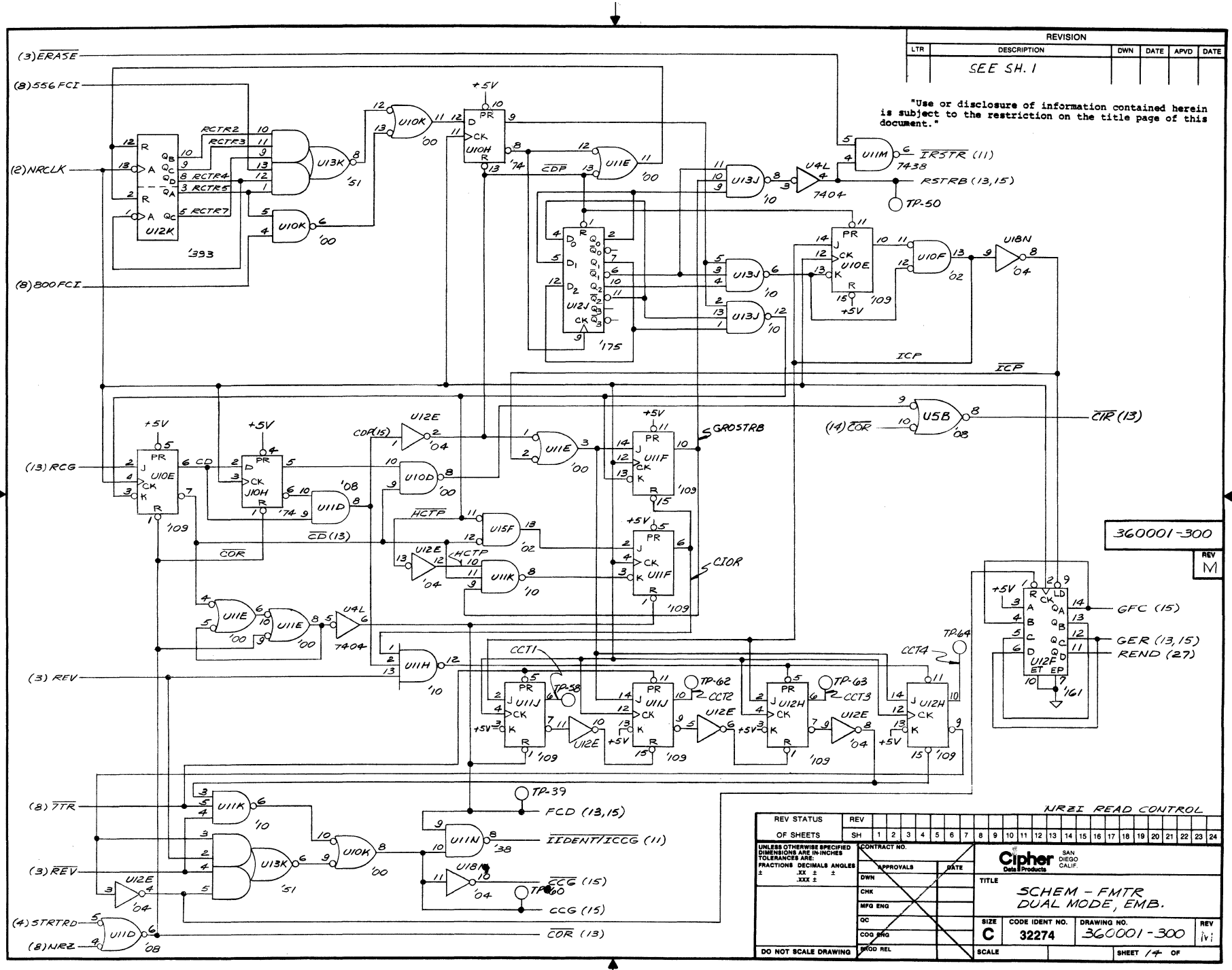
Cipher Data Products SAN DIEGO CALIF.

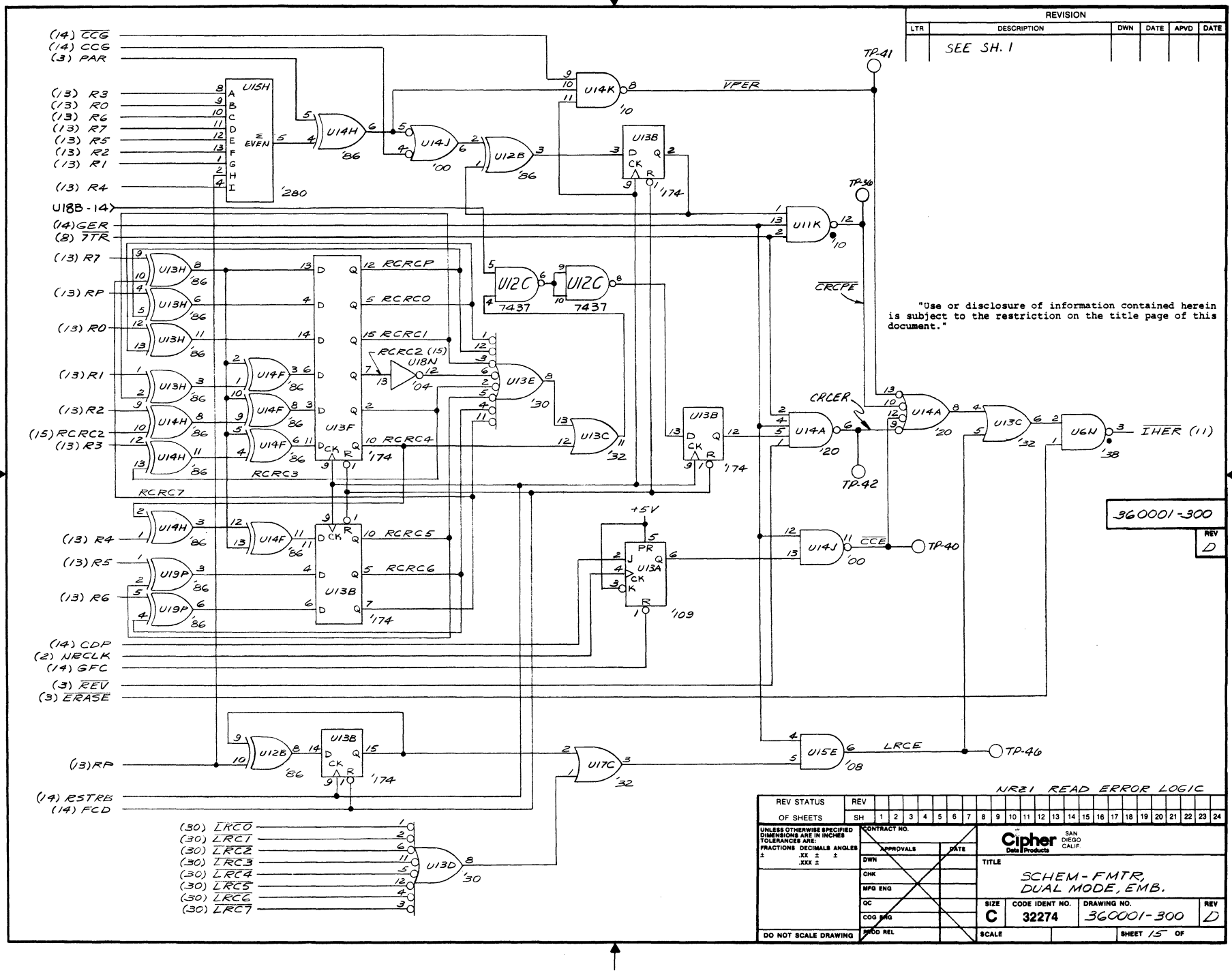
TITLE: SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	M

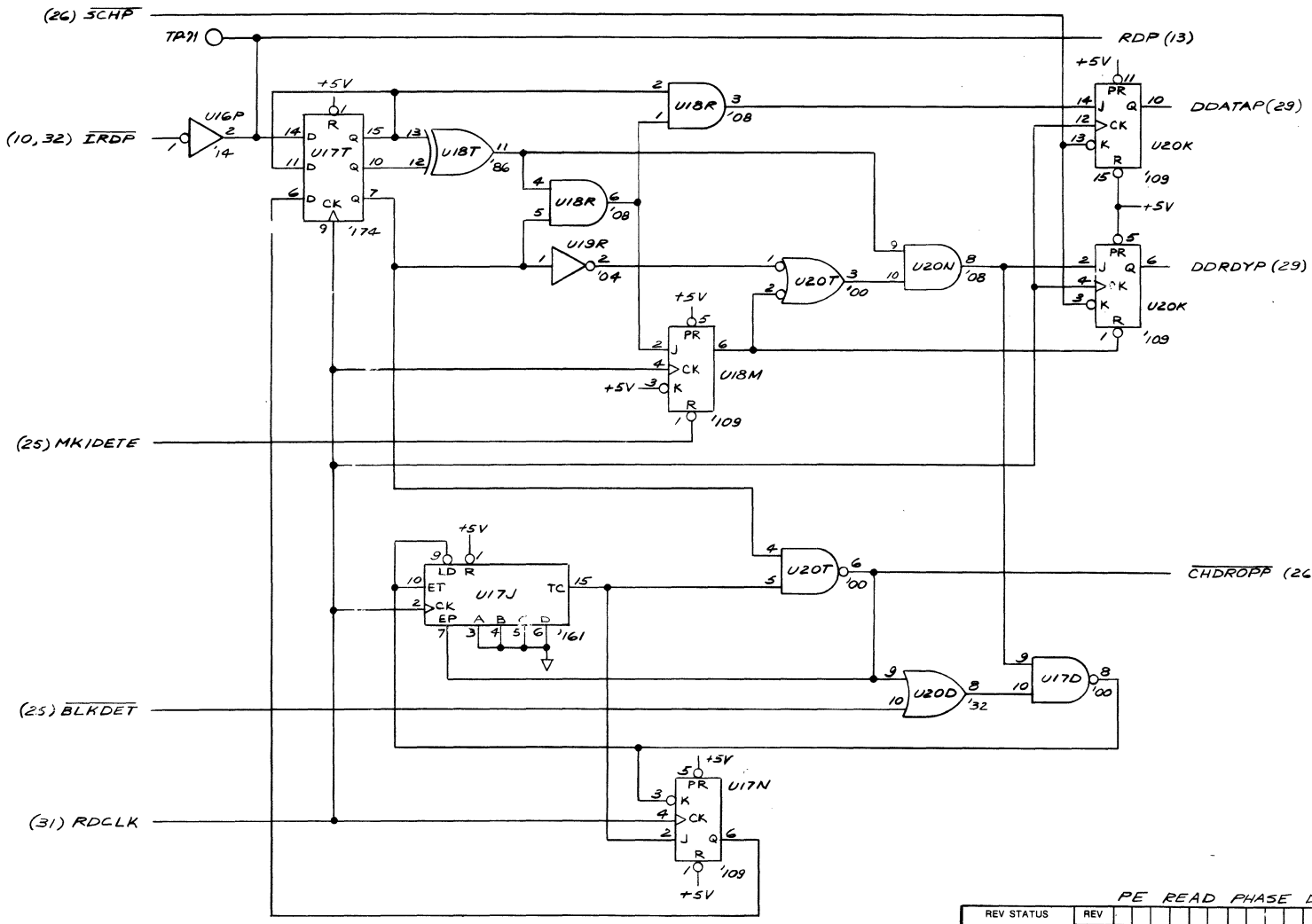
SCALE

SHEET 13 OF


REVISION
LTR | DESCRIPTION | DWN | DATE | APVD | DATE
SEE SH. 1
"Use or disclosure of information contained herein is subject to the restriction on the title page of this document."
(3) ERASE
(8) 556 FCI
(2) NRCLK
(8) 800 FCI
U12K '393
RCTR2
RCTR3
RCTR4
RCTR5
RCTR7
U13K '51
U10K '00
U10H '74
CDP
U11E '00
U13J '10
U4L 7404
U11M 7438
IRSTR (11)
RSTRB (13,15)
TP-50
U12J '175
U10E '109
U10F '02
U18N '04
ICP
(13) RCG
U10E
U10H '74
U11D '08
CD (13)
COR
CD(15)
U12E '04
U10D '00
HCTP
U15F '02
U11K '10
U11F '109
GROSTRB
CIOR
(14) COR
U5B '08
CIR (13)
360001-300
REV M
U12F '161
GFC (15)
GER (13,15)
REND (27)
TP-64
CCT4
CCT1
TP-58
U11J '109
TP-62
CCT2
TP-63
CCT3
U12H '109
(3) REV
U11H '10
(8) TR
(3) REV
U11K '10
U13K '51
U10K '00
TP-39
FCD (13,15)
U11N '38
IIDENT/ICCG (11)
U18M '04
ICCG (15)
TP-60
CCG (15)
(4) STRTRD
(8) NRZ
U11D '08
COR (13)
NRZI READ CONTROL
REV STATUS
OF SHEETS
SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
Cipher Data Products SAN DIEGO CALIF.
TITLE
SCHEM - FMTR
DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV M
SCALE
SHEET 14 OF


REVISION
LTR DESCRIPTION DWN DATE APVD DATE
SEE SH. 1
(14) CCG
(14) CCG
(3) PAR
(13) R3
(13) R0
(13) R6
(13) R7
(13) R5
(13) R2
(13) R1
(13) R4
U18B-14
(14) GER
(8) TTR
(13) R7
(13) RP
(13) R0
(13) R1
(13) R2
(15) RCRC2
(13) R3
(13) R4
(13) R5
(13) R6
(14) CDP
(2) NRCLK
(14) GFC
(3) REV
(3) ERASE
(13) RP
(14) RSTRB
(14) FCD
(30) LRC0
(30) LRC1
(30) LRC2
(30) LRC3
(30) LRC4
(30) LRC5
(30) LRC6
(30) LRC7
U15H
'280
U14H
'86
U14J
'00
U12B
'86
U14K
'10
U13B
'174
U11K
'10
U13H
'86
U14F
'86
U14H
'86
U19P
'86
U13F
U13B
'174
U12C
7437
U18N
'04
U13E
'30
U13C
'32
U14A
'20
U6N
'38
U14J
'00
U13A
'109
U15E
'08
U17C
'32
U13D
'30
RCRC0
RCRC1
RCRC2 (15)
RCRC3
RCRC4
RCRC5
RCRC6
RCRC7
TP-41
VPER
TP-36
CRCPE
CRCER
TP-42
IHER (11)
TP-40
CCE
+5V
LRCE
TP-46
"Use or disclosure of information contained herein is subject to the restriction on the title page of this document."
360001-300
REV D
NRZI READ ERROR LOGIC
REV STATUS
OF SHEETS
SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±
CONTRACT NO.
APPROVALS DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
Cipher Data Products SAN DIEGO CALIF.
TITLE
SCHEM-FMTR, DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV D
SCALE
SHEET 15 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

PE READ PHASE DISCRIMINATOR CHANNELP

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
MOD REL	

DO NOT SCALE DRAWING

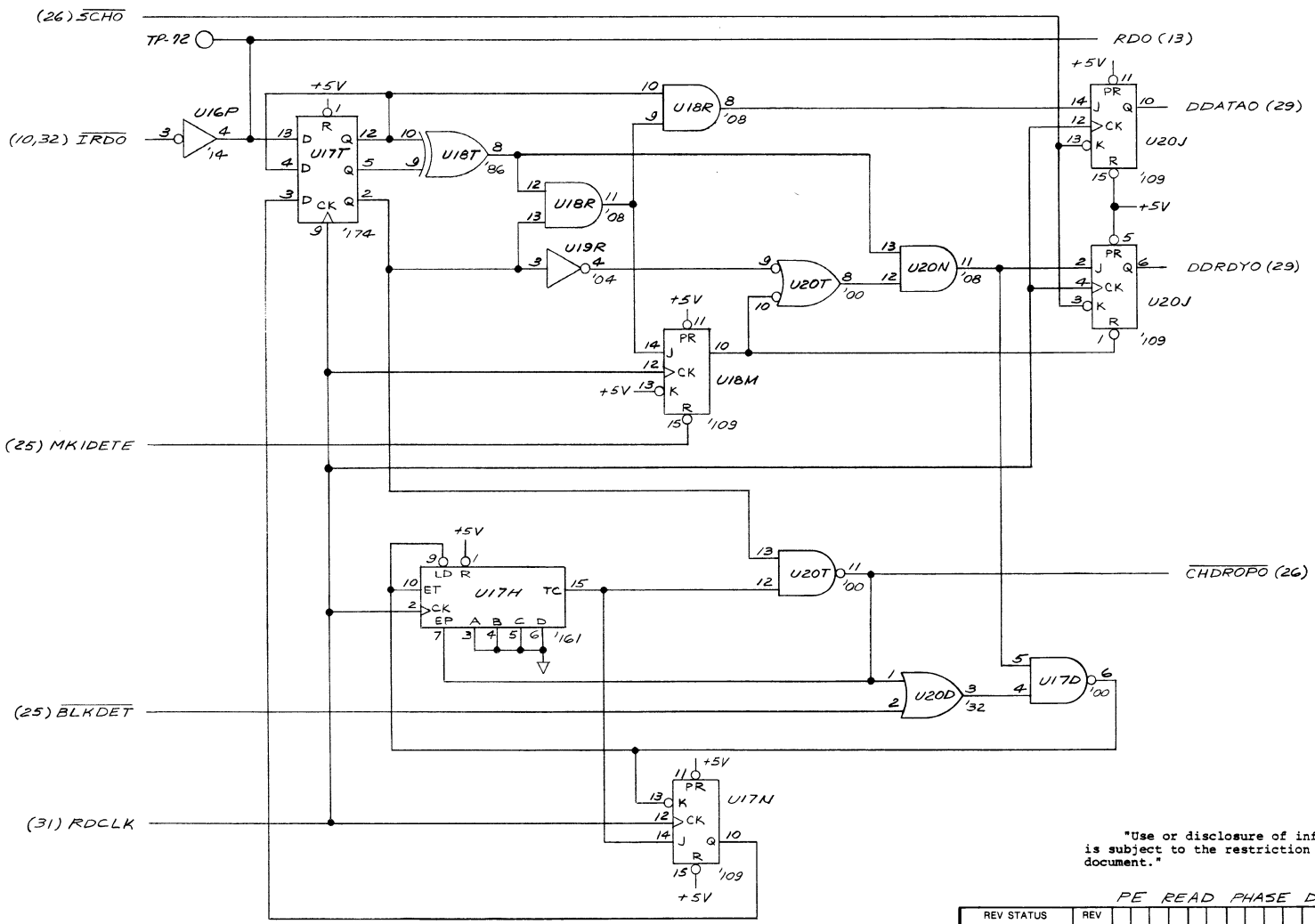
Cipher Data Products SAN DIEGO CALIF.

TITLE: SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE | SHEET 16 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

PE READ PHASE DISCRIMINATOR, CHANNEL 0

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

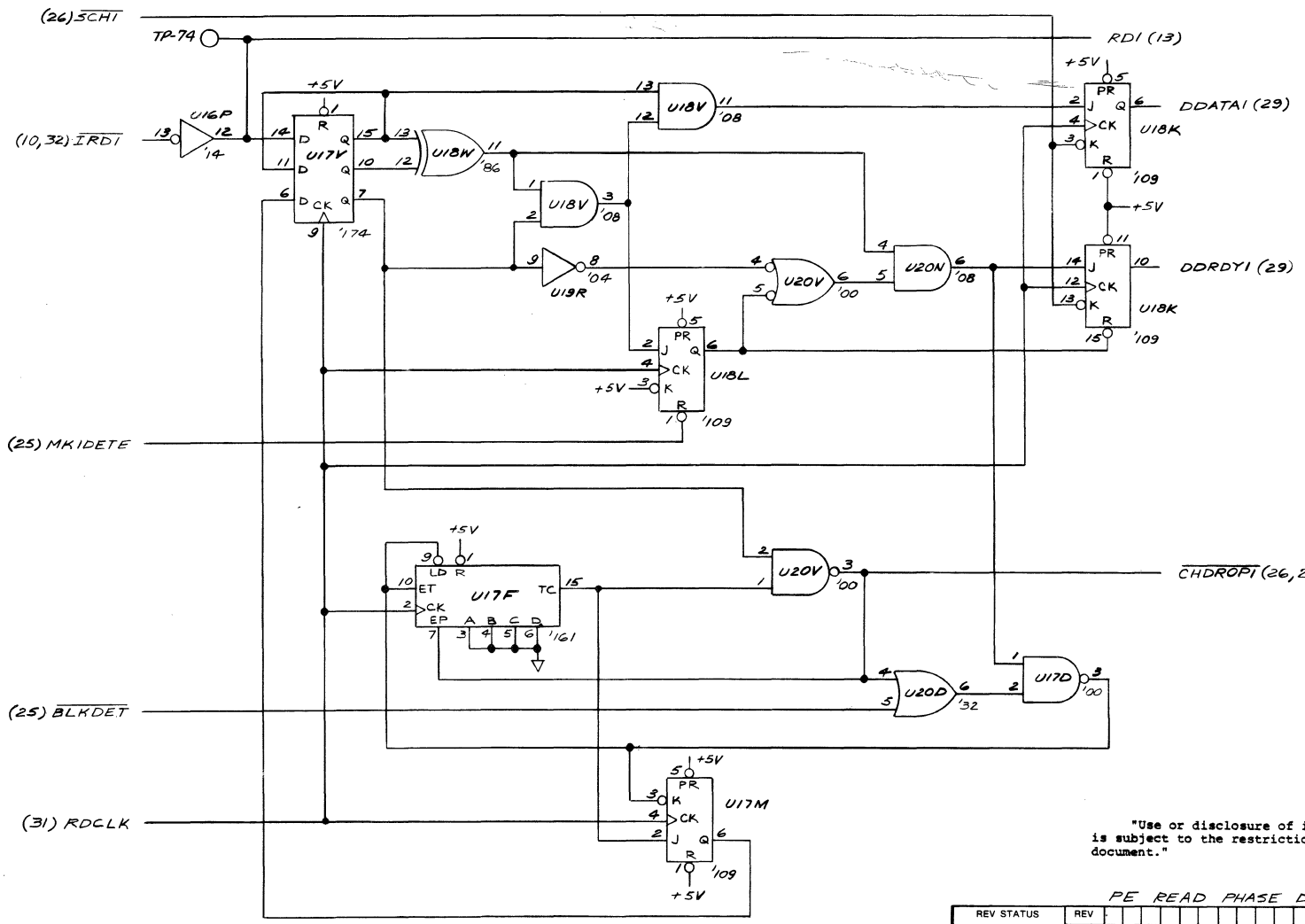
Cipher Data Products SAN DIEGO CALIF

TITLE: SCHEM - FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE | SHEET 17 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

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PE READ PHASE DISCRIMINATOR, CHANNEL I

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

Cipher Data Products SAN DIEGO CALIF

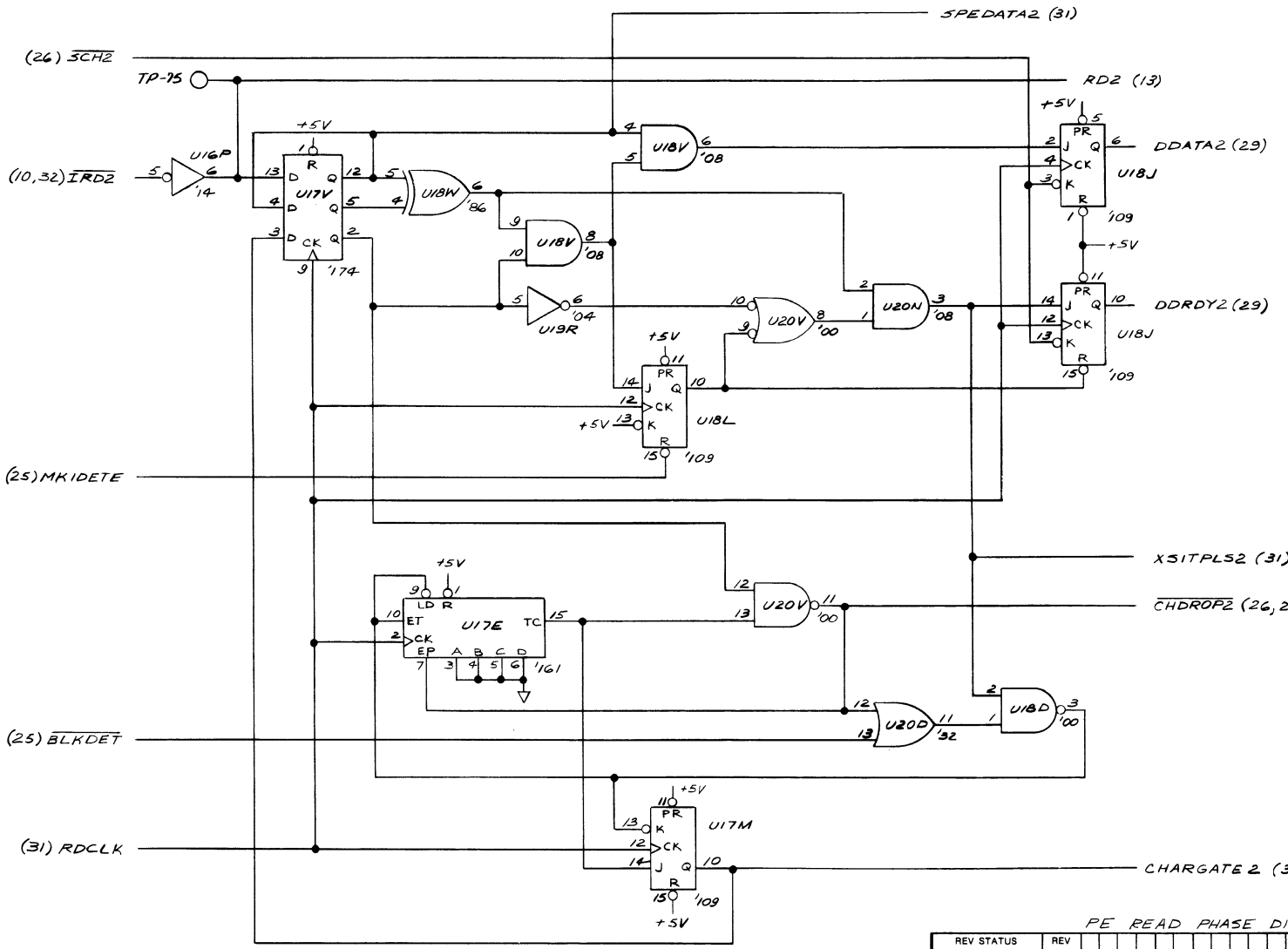
TITLE
SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE

SHEET 18 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

PE READ PHASE DISCRIMINATOR CHANNEL 2

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

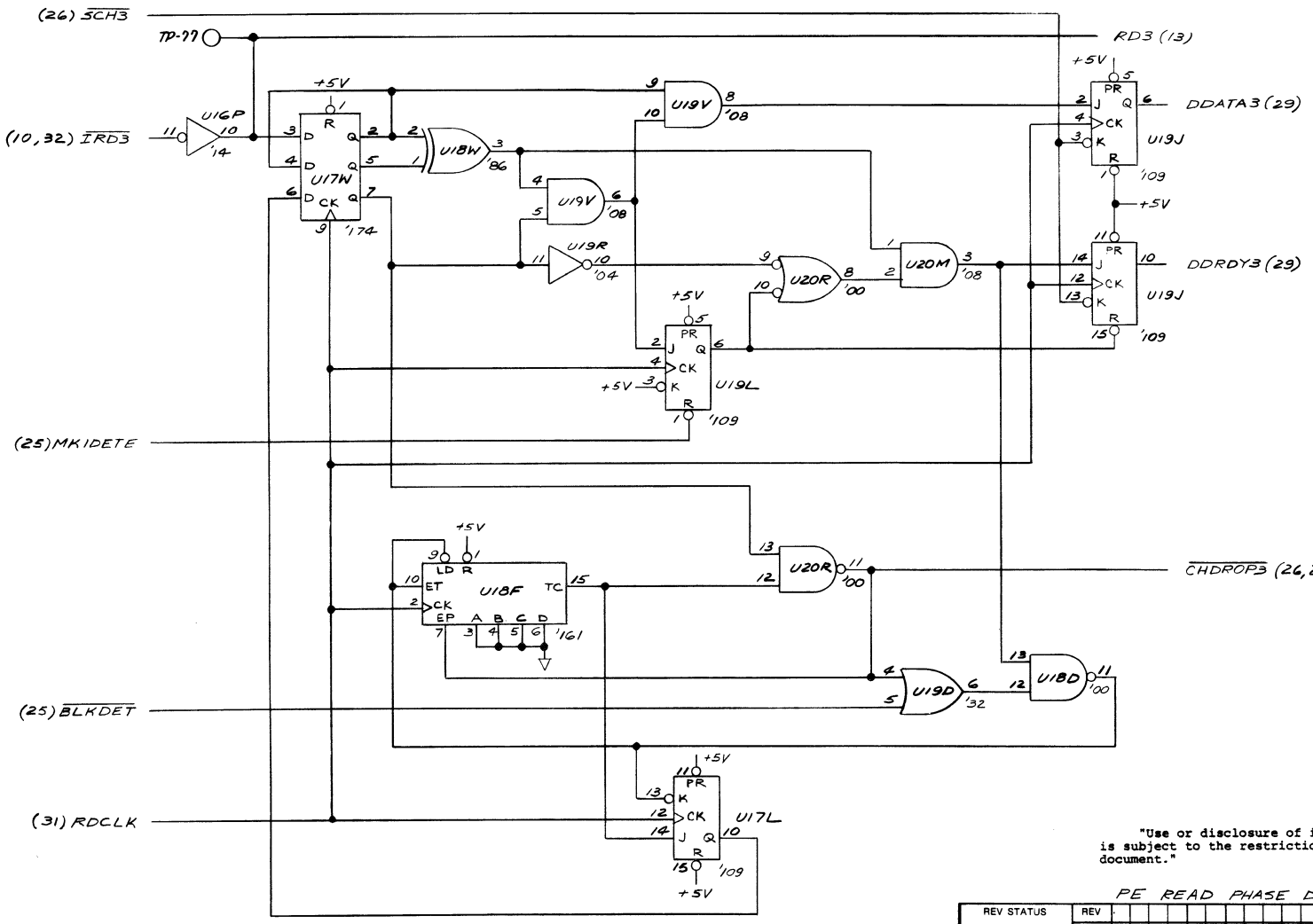
Cipher Data Products SAN DIEGO CALIF

TITLE: SCHEM - FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE | SHEET 19 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

CHDROP3 (26,28)

PE READ PHASE DISCRIMINATOR CHANNEL 3

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

Cipher Data Products SAN DIEGO CALIF.

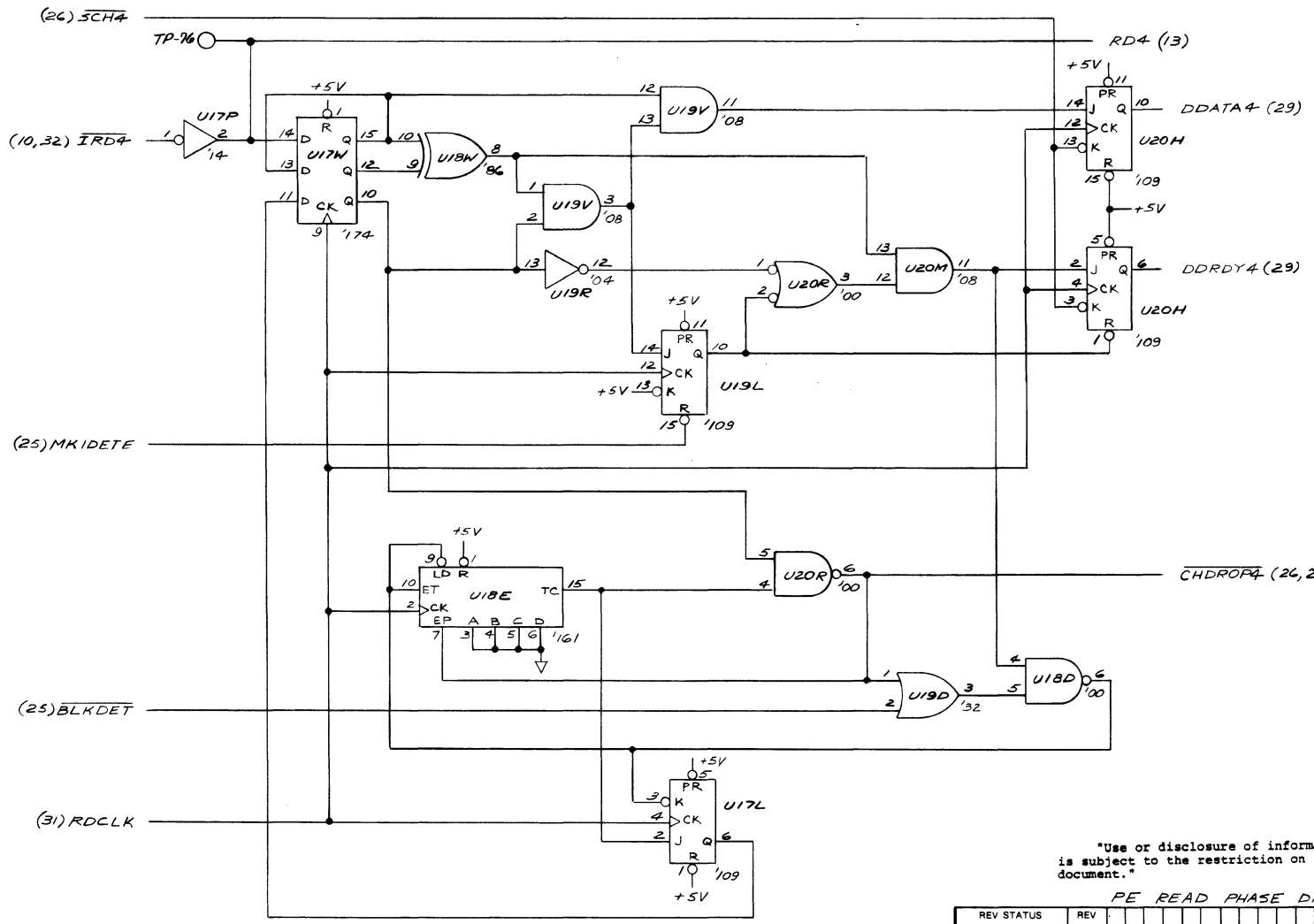
TITLE: SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE

SHEET 20 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH.1				



360001-300

REV A

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PE READ PHASE DISCRIMINATOR CHANNEL4

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

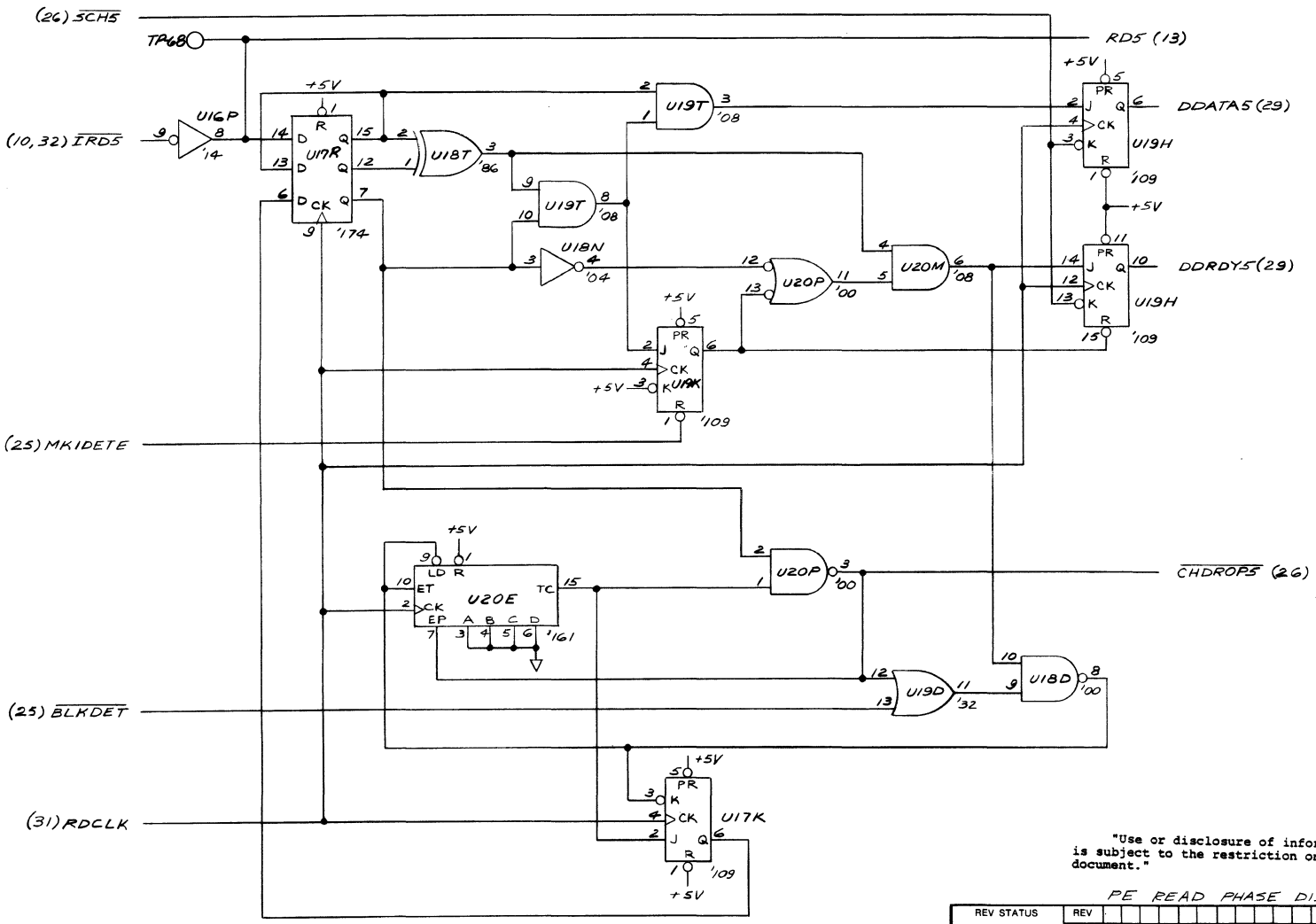
Cipher Data Products SAN DIEGO CALIF.

TITLE: SCHEM - FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE | SHEET 21 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

PE READ PHASE DISCRIMINATOR CHANNEL 5

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

DO NOT SCALE DRAWING

Cipher Data Products — SAN DIEGO CALIF.

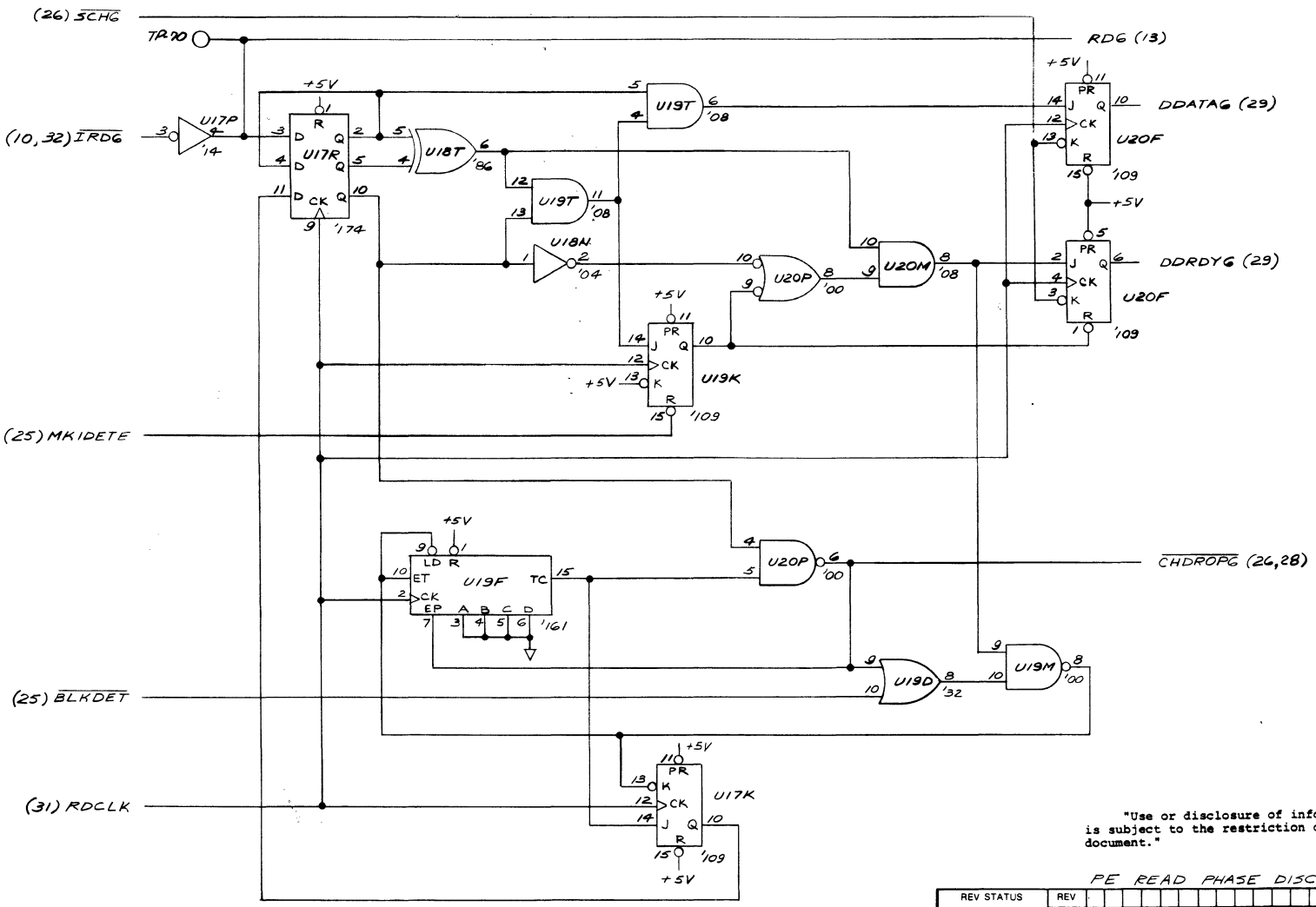
TITLE: SCHEM - FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE

SHEET 22 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

PE READ PHASE DISCRIMINATOR CHANNEL G

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

Cipher Data Products SAN DIEGO CALIF

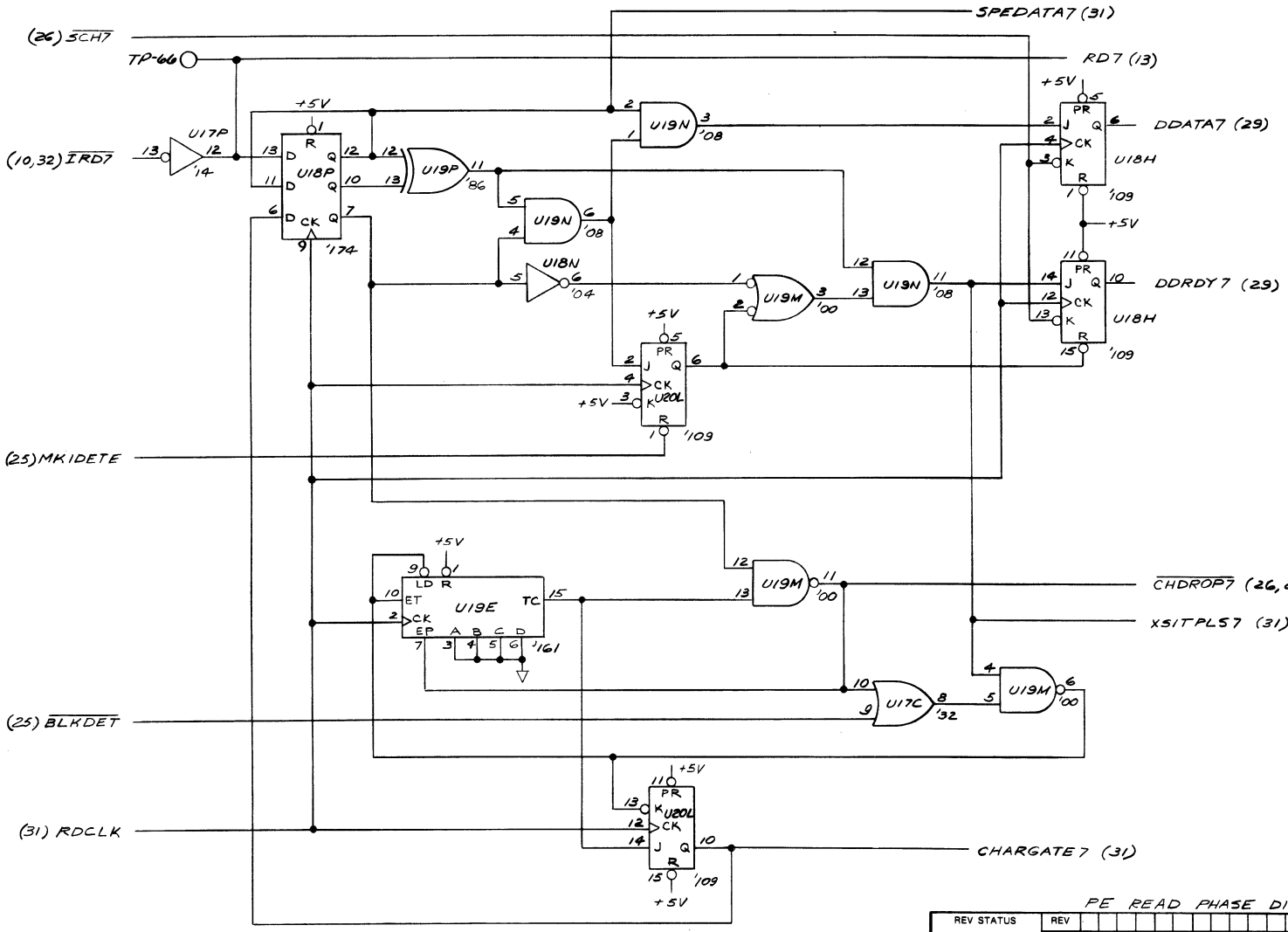
TITLE
SCHEM-FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE

SHEET 23 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

PE READ PHASE DISCRIMINATOR CHANNEL7

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

DO NOT SCALE DRAWING

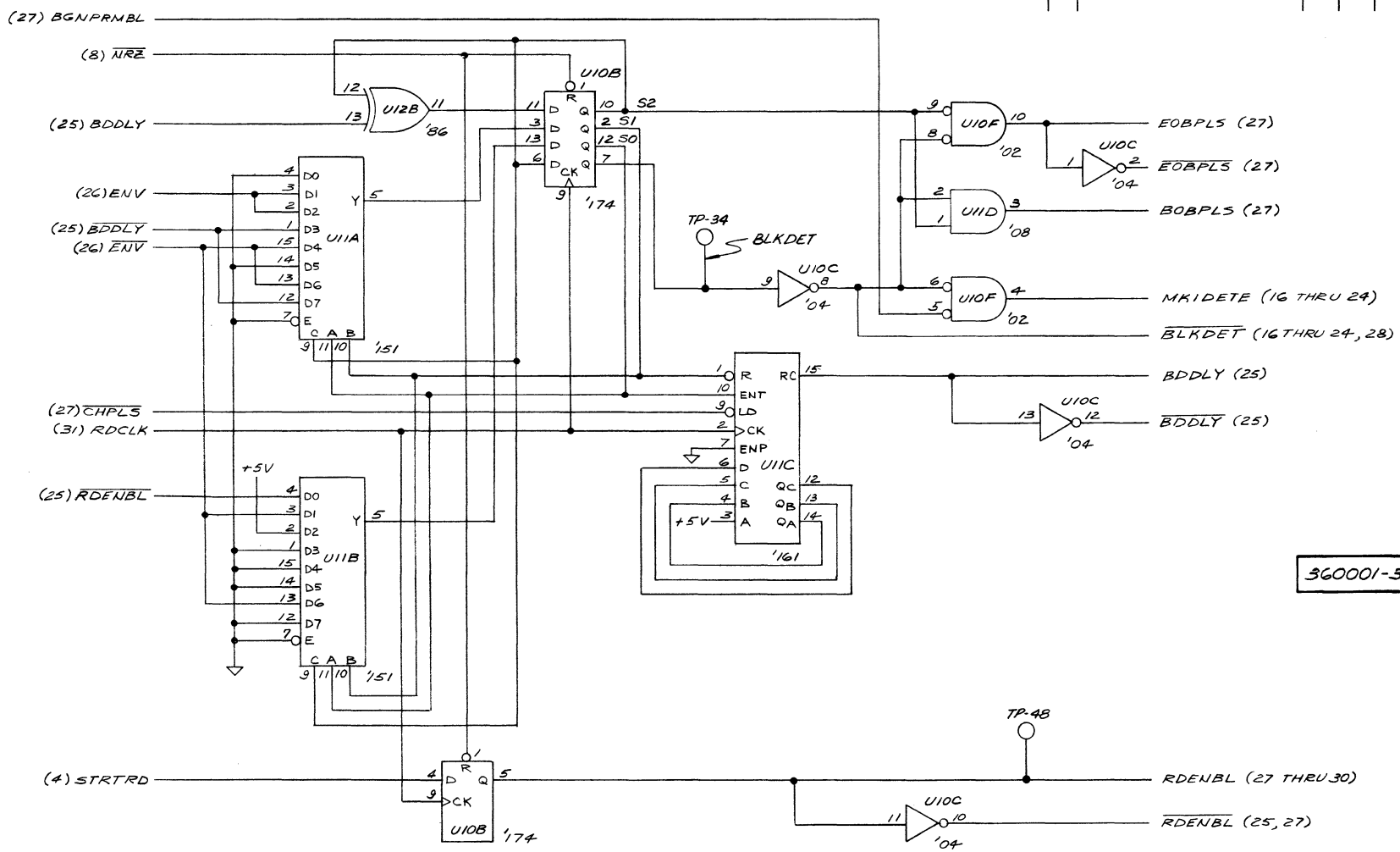
Cipher Data Products SAN DIEGO CALIF.

TITLE: SCHEM-FMTR, DUAL MODE, EMB.,

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

SCALE | SHEET 24 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				



360001-300

REV A

BLOCK DETECTOR

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

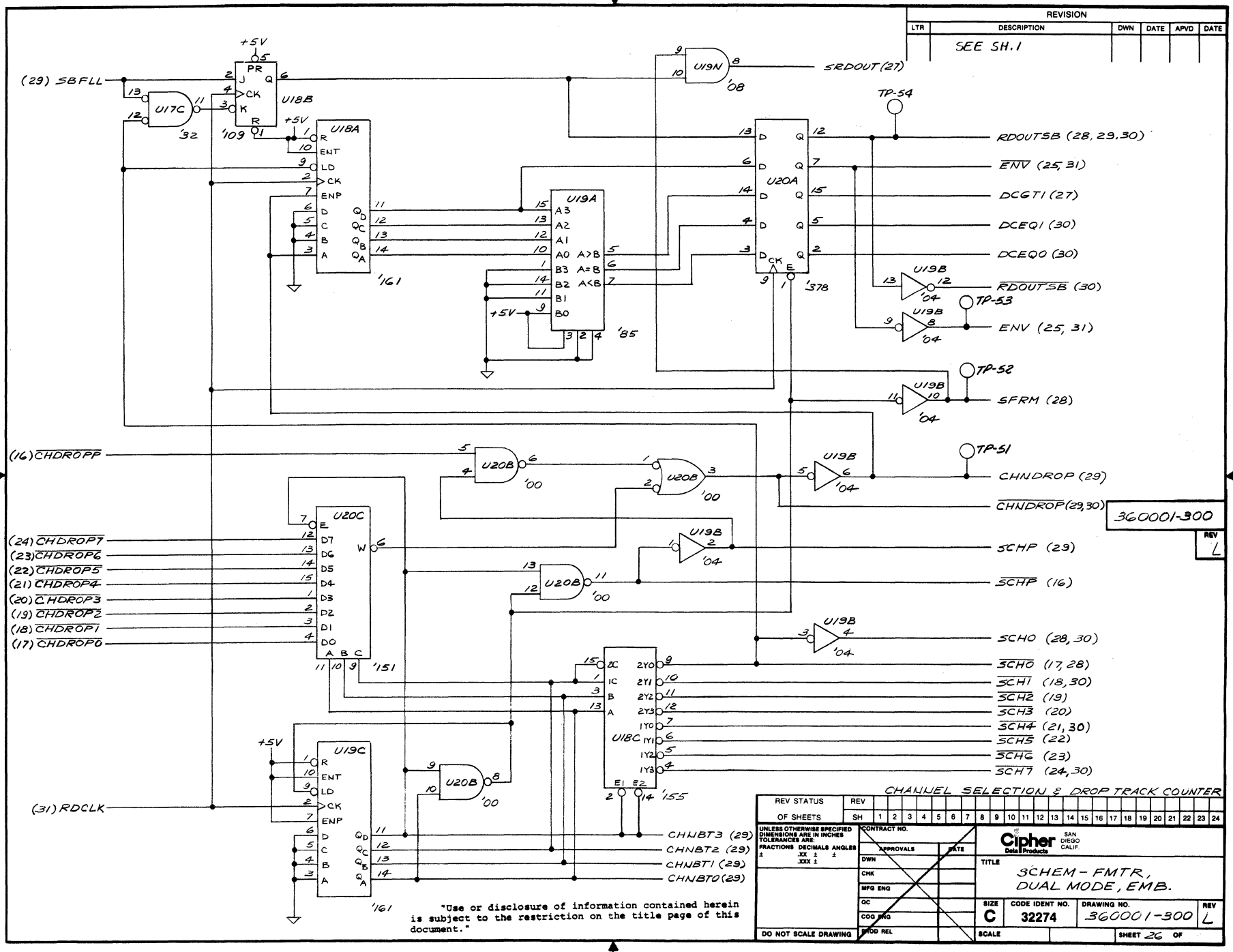
CONTRACT NO.	APPROVALS	DATE
	DWN	
	CHK	
	MFG ENG	
	QC	
	COG ENG	
	PROD REL	

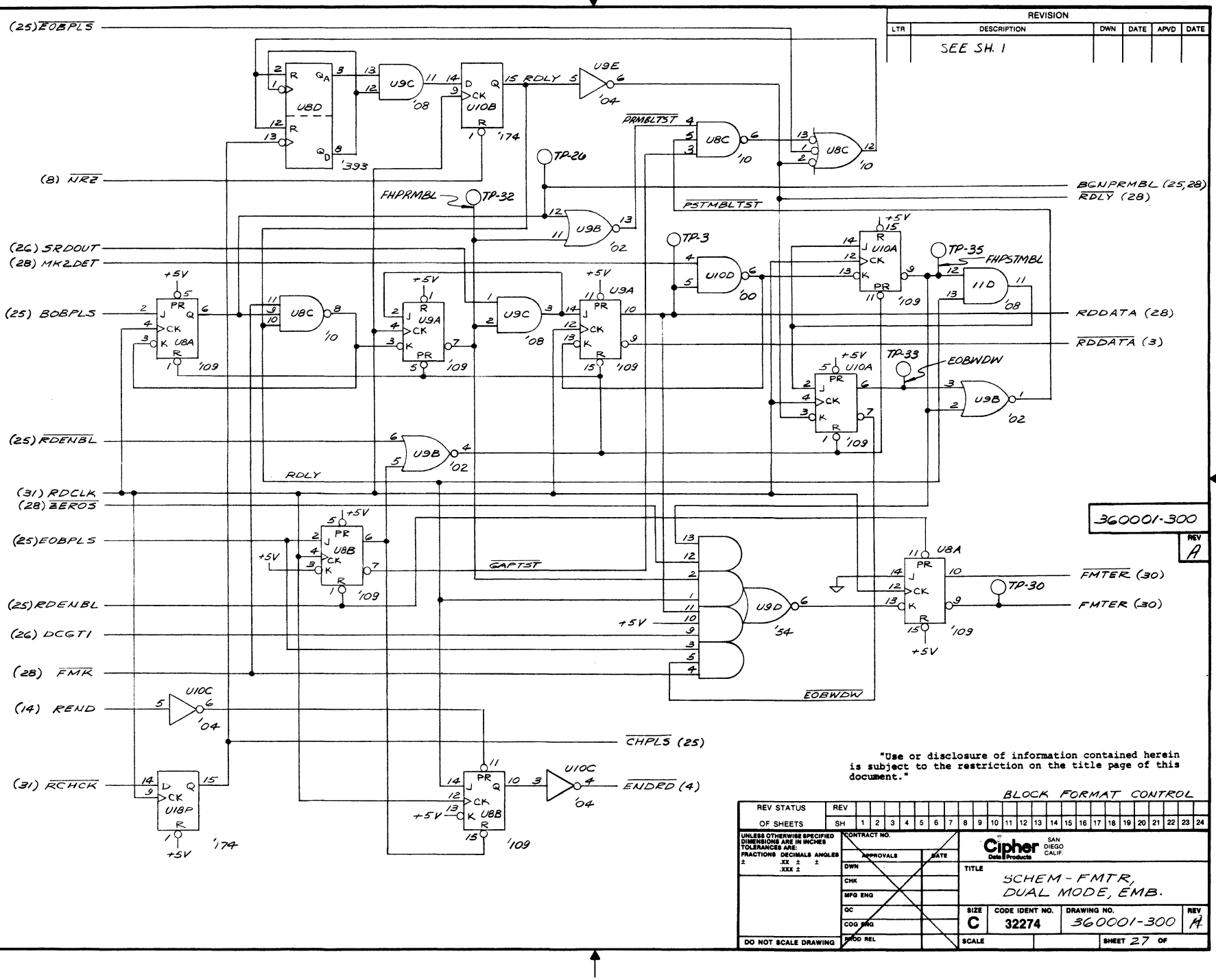
Cipher Data Products SAN DIEGO CALIF.

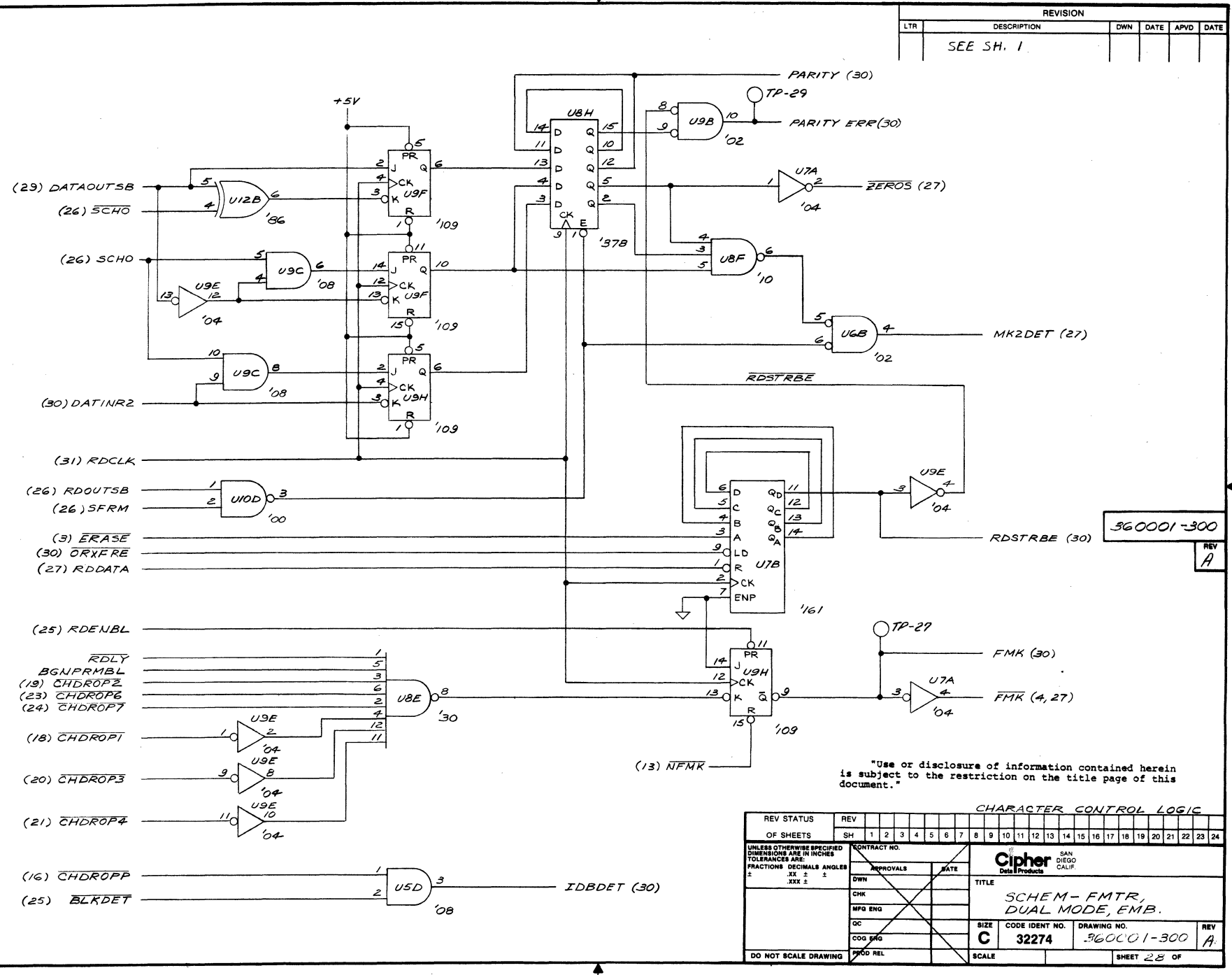
TITLE: SCHEM - FMTR, DUAL MODE, EMB.

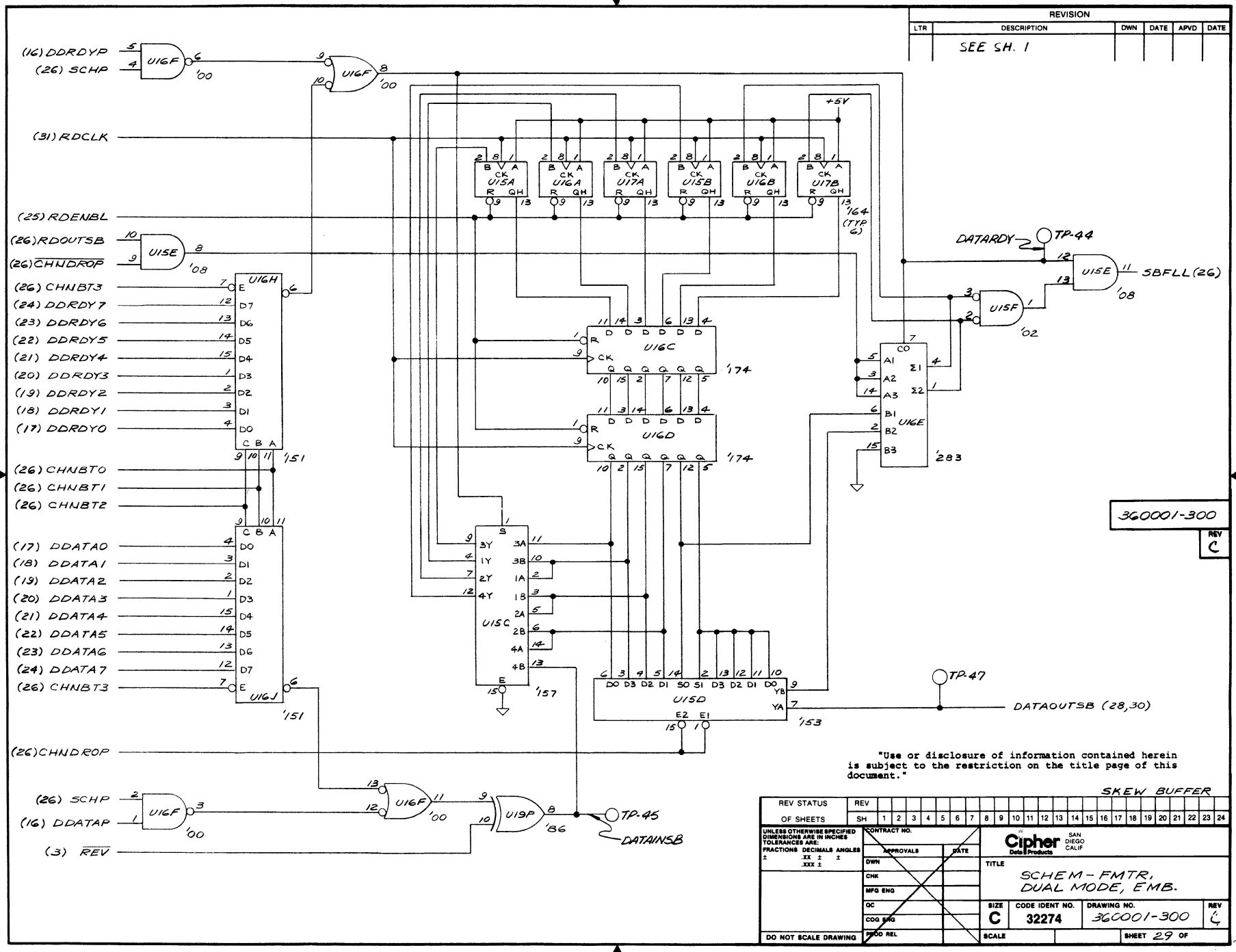
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	A

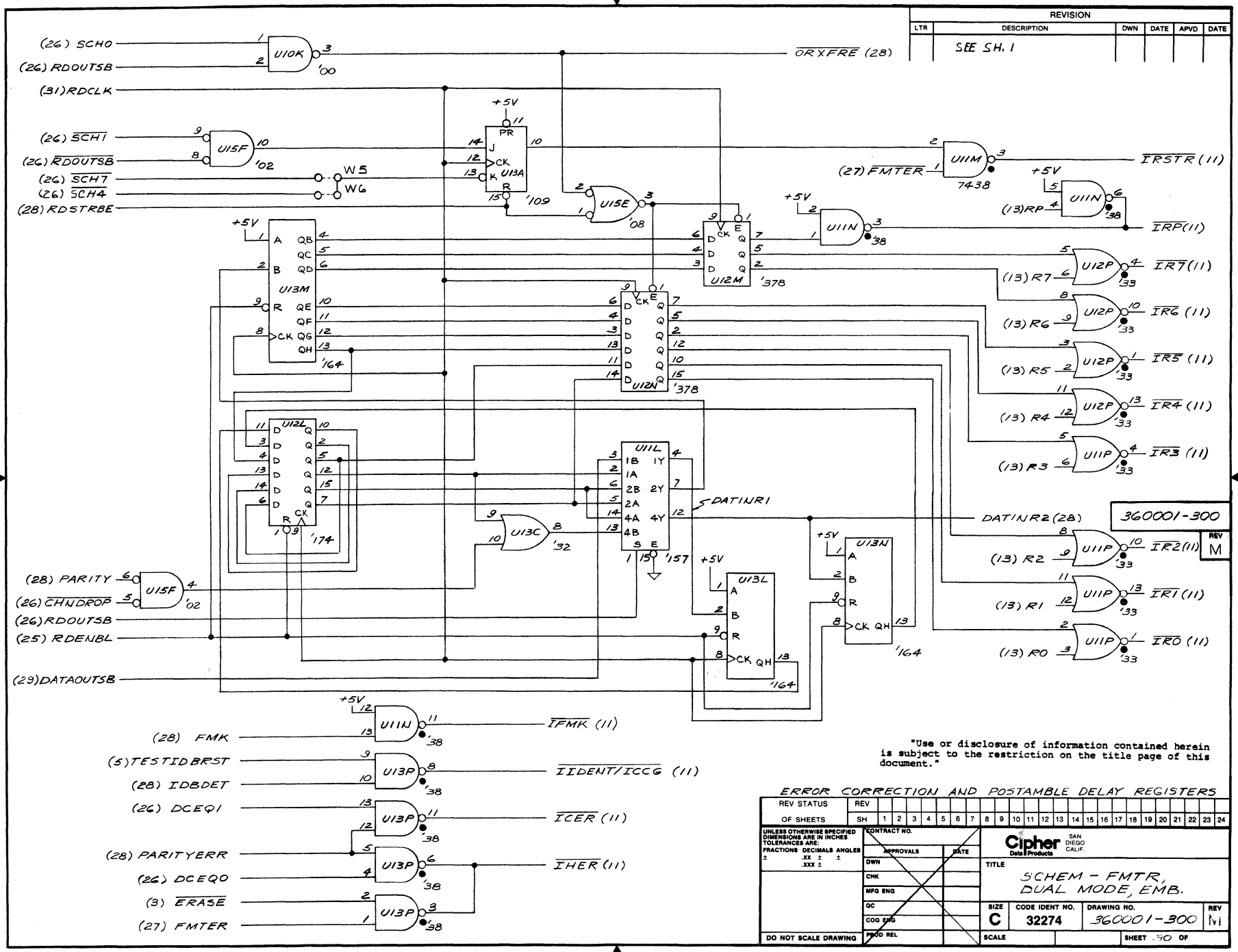
SCALE | SHEET 25 OF


REVISION
LTR DESCRIPTION DWN DATE APVD DATE
SEE SH.1
(29) SBFLL
+5V
U18B
U17C
'32
'109
U18A
'161
U19N
'08
SRDOUT(27)
U19A
'85
U20A
'378
TP-54
RDOUTSB (28, 29.30)
ENV (25, 31)
DCGT1 (27)
DCEQ1 (30)
DCEQ0 (30)
U19B
'04
RDOUTSB (30)
TP-53
ENV (25, 31)
TP-52
SFRM (28)
(16) CHDROPP
U20B
'00
TP-51
CHNDROP (29)
CHNDROP(29,30)
360001-300
REV L
U20C
'151
(24) CHDROP7
(23) CHDROP6
(22) CHDROP5
(21) CHDROP4
(20) CHDROP3
(19) CHDROP2
(18) CHDROP1
(17) CHDROP0
SCHP (29)
SCHP (16)
SCH0 (28, 30)
U18C
'155
SCH0 (17, 28)
SCH1 (18, 30)
SCH2 (19)
SCH3 (20)
SCH4 (21, 30)
SCH5 (22)
SCH6 (23)
SCH7 (24, 30)
U19C
(31) RDCLK
CHNBT3 (29)
CHNBT2 (29)
CHNBT1 (29)
CHNBT0(29)
"Use or disclosure of information contained herein is subject to the restriction on the title page of this document."
CHANNEL SELECTION & DROP TRACK COUNTER
REV STATUS
OF SHEETS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±
CONTRACT NO.
APPROVALS DATE
DWN
CHK
MFG ENG
QC
COG ENG
MOD REL
DO NOT SCALE DRAWING
Cipher Data Products SAN DIEGO CALIF.
TITLE
SCHEM-FMTR, DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV L
SCALE
SHEET 26 OF


(25) EOBPLS
U8D
'393
U9C
'08
U10B
'174
RDLY
U9E
'04
PRMBLTST
U8C
'10
TP-26
(8) NRZ
FHPRMBL
TP-32
BGNPRMBL (25,28)
RDLY (28)
PSTMBLTST
U9B
'02
(26) SRDOUT
(28) MK2DET
TP-3
U10D
'00
U10A
'109
TP-35
FHPSTMBL
11D
'08
RDDATA (28)
RDDATA (3)
(25) BOBPLS
U8A
U8C
U9A
U9C
TP-33
EOBWDW
(25) RDENBL
RDLY
(31) RDCLK
(28) ZEROS
(25) EOBPLS
U8B
GAPTST
(25) RDENBL
(26) DCGTI
U9D
'54
U8A
FMTER (30)
TP-30
(28) FMR
(14) REND
U10C
'04
CHPLS (25)
(31) RCHCK
U11P
'174
U11B
'109
ENDRD (4)
+5V
REVISION
LTR
DESCRIPTION
DWN
DATE
APVD
DATE
SEE SH. 1
360001-300
REV A
"Use or disclosure of information contained herein is subject to the restriction on the title page of this document."
BLOCK FORMAT CONTROL
REV STATUS
REV
OF SHEETS
SH
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±
CONTRACT NO.
APPROVALS
DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
Cipher Data Products SAN DIEGO CALIF.
TITLE
SCHEM-FMTR, DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV A
SCALE
SHEET 27 OF


REVISION
LTR
DESCRIPTION
DWN
DATE
APVD
DATE
SEE SH. 1
+5V
(29) DATAOUTSB
(26) SCHO
(26) SCHO
(30) DATINR2
(31) RDCLK
(26) RDOUTSB
(26) SFRM
(3) ERASE
(30) ORXFRE
(27) RDDATA
(25) RDENBL
RDLY
BGNPRMBL
(19) CHDROP2
(23) CHDROP6
(24) CHDROP7
(18) CHDROP1
(20) CHDROP3
(21) CHDROP4
(16) CHDROPP
(25) BLKDET
U12B
'86
U9F
'109
U9C
'08
U9E
'04
U9H
'109
U10D
'00
U8E
'30
U9E
'04
U9E
'04
U9E
'04
U5D
'08
IDBDET (30)
U8H
'378
PARITY (30)
TP-29
U9B
'02
PARITY ERR(30)
U7A
'04
ZEROS (27)
U8F
'10
U6B
'02
MK2DET (27)
RDSTRBE
U7B
'161
U9E
'04
RDSTRBE (30)
U9H
'109
(13) NFMK
TP-27
FMK (30)
U7A
'04
FMK (4, 27)
"Use or disclosure of information contained herein is subject to the restriction on the title page of this document."
CHARACTER CONTROL LOGIC
REV STATUS
OF SHEETS
REV
SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±
CONTRACT NO.
APPROVALS
DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
Cipher Data Products
SAN DIEGO CALIF.
TITLE
SCHEM- FMTR, DUAL MODE, EMB.
SIZE
C
CODE IDENT NO.
32274
DRAWING NO.
360001-300
REV
A
SCALE
SHEET 28 OF
360001-300
REV
A


REVISION
LTR DESCRIPTION DWN DATE APVD DATE
SEE SH. 1
(16) DDRDYP
(26) SCHP
U16F '00
(31) RDCLK
+5V
U15A U16A U17A U15B U16B U17B '164 (TYP 6)
(25) RDENBL
(26) RDOUTSB
(26) CHNDROP
U15E '08
U16H '151
(26) CHNBT3
(24) DDRDY7
(23) DDRDY6
(22) DDRDY5
(21) DDRDY4
(20) DDRDY3
(19) DDRDY2
(18) DDRDY1
(17) DDRDY0
U16C '174
U16D '174
U16E '283
U15F '02
DATARDY
TP-44
U15E '08
SBFLL(26)
(26) CHNBT0
(26) CHNBT1
(26) CHNBT2
(17) DDATA0
(18) DDATA1
(19) DDATA2
(20) DDATA3
(21) DDATA4
(22) DDATA5
(23) DDATA6
(24) DDATA7
(26) CHNBT3
U16J '151
U15C '157
U15D '153
TP-47
DATAOUTSB (28,30)
(26) CHNDROP
(26) SCHP
(16) DDATAP
(3) REV
U16F '00
U19P '86
TP-45
DATAINSB
360001-300
REV C
"Use or disclosure of information contained herein is subject to the restriction on the title page of this document."
SKEW BUFFER
REV STATUS
OF SHEETS
SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±
CONTRACT NO.
APPROVALS DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
Cipher Data Products SAN DIEGO CALIF
TITLE
SCHEM-FMTR, DUAL MODE, EMB.
SIZE C
CODE IDENT NO. 32274
DRAWING NO. 360001-300
REV C
SCALE
SHEET 29 OF



REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				

360001-300 REV M

ERROR CORRECTION AND POSTAMBLE DELAY REGISTERS

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DWN	
CHK	
MFG ENG	
QC	
COG ENG	
PROD REL	

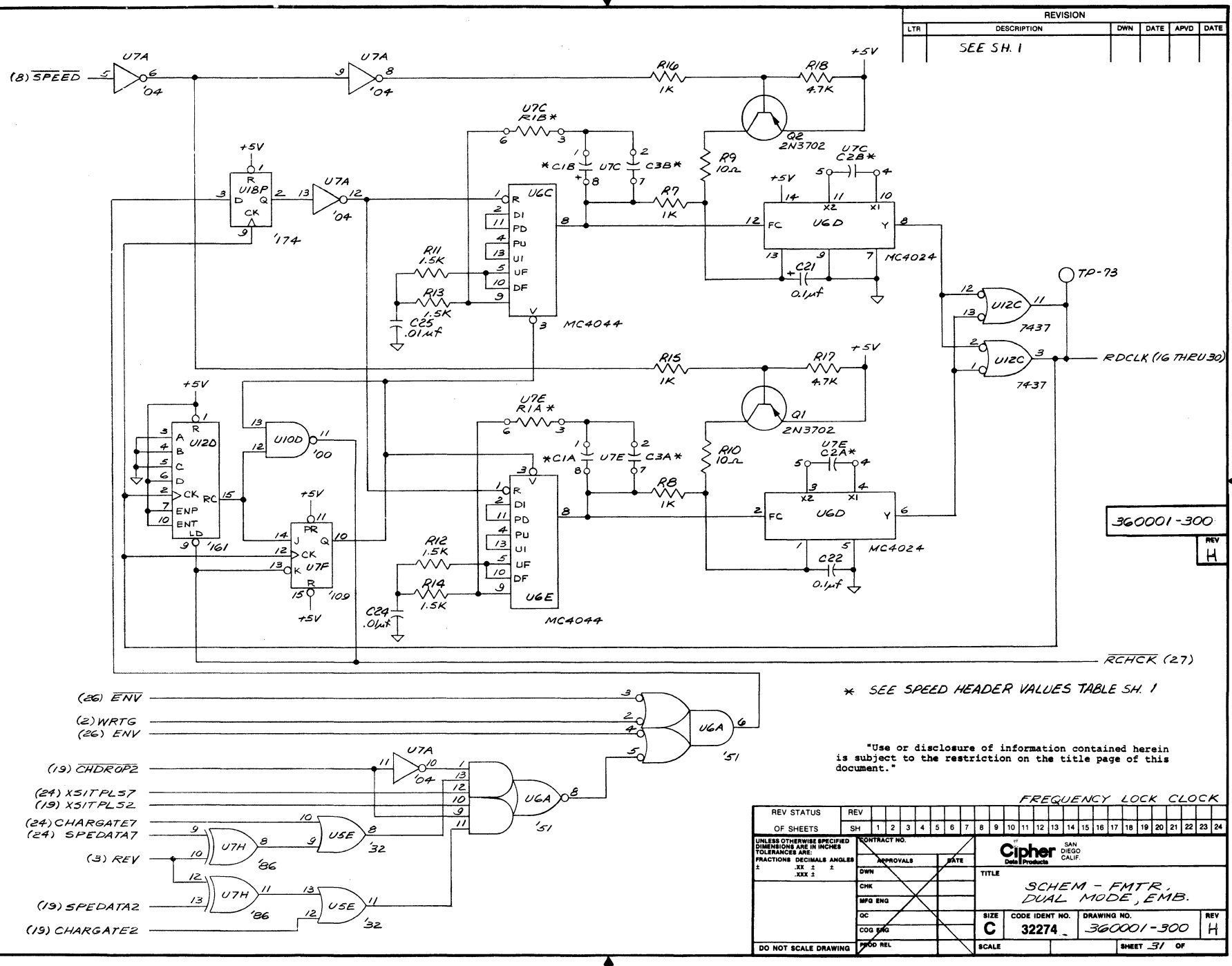
DO NOT SCALE DRAWING

Cipher Data Products SAN DIEGO CALIF.

TITLE: SCHEM - FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	360001-300	M

SCALE | SHEET 30 OF


REVISION
LTR DESCRIPTION DWN DATE APVD DATE
SEE SH. 1
(8) SPEED
U7A '04
R16 1K
R18 4.7K
+5V
Q2 2N3702
U7C R1B*
U7C C1B*
U7C C3B*
R9 10Ω
U7C C2B*
U18P '174
R7 1K
U6C
U6D
MC4024
C21 0.1μf
MC4044
R11 1.5K
R13 1.5K
C25 .01μf
U12C 7437
TP-73
RDCLK (1G THRU 30)
R15 1K
R17 4.7K
Q1 2N3702
U7E R1A*
U7E C1A*
U7E C3A*
R10 10Ω
U7E C2A*
R8 1K
U6E
U12D '161
U10D '00
U7F '109
R12 1.5K
R14 1.5K
C24 .01μf
C22 0.1μf
RCHCK (27)
360001-300
REV H
* SEE SPEED HEADER VALUES TABLE SH. 1
(26) ENV
(2) WRTG
(26) ENV
UGA '51
(19) CHDROP2
(24) XSITPLS7
(19) XSITPLS2
(24) CHARGATE7
(24) SPEDATA7
(3) REV
(19) SPEDATA2
(19) CHARGATE2
U7H '86
U5E '32
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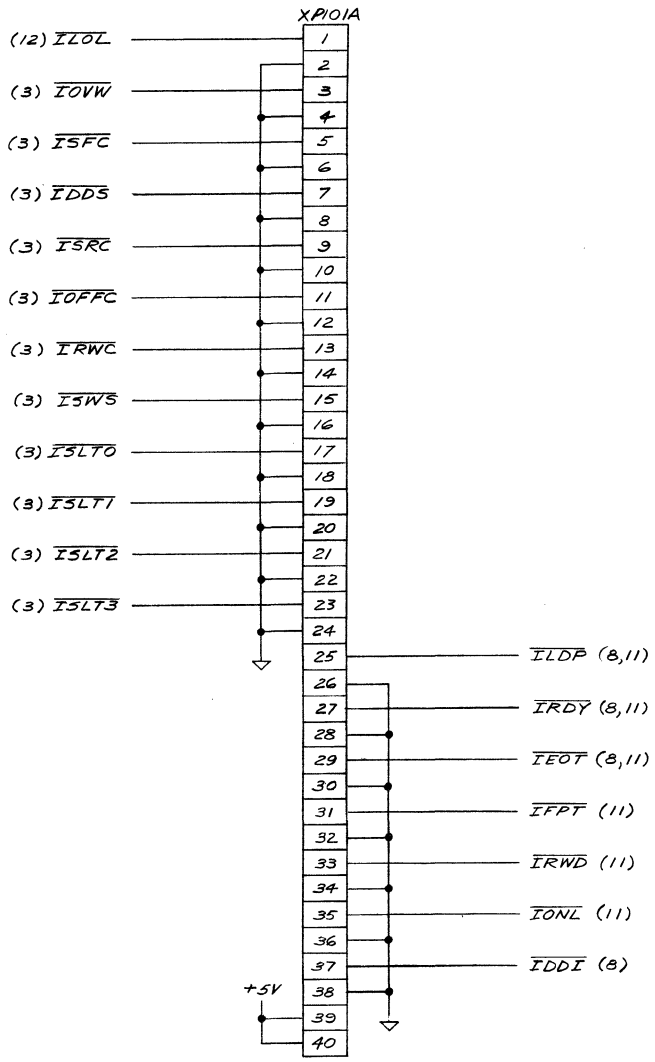
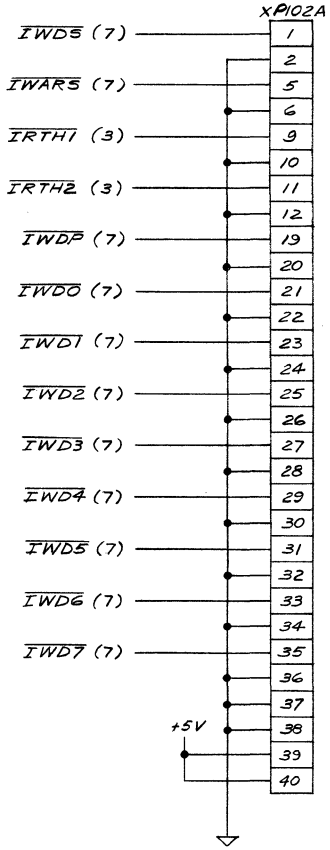
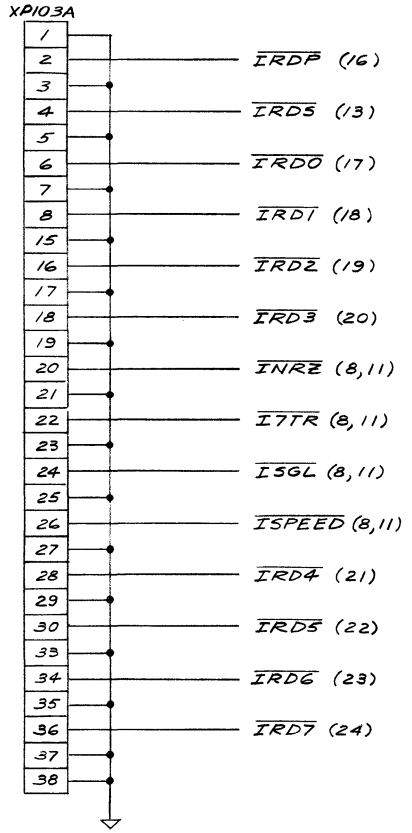
FREQUENCY LOCK CLOCK
REV STATUS REV
OF SHEETS SH 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±
CONTRACT NO.
APPROVALS DATE
DWN
CHK
MFG ENG
QC
COG ENG
PROD REL
DO NOT SCALE DRAWING
Cipher Data Products SAN DIEGO CALIF.
TITLE SCHEM - FMTR, DUAL MODE, EMB.
SIZE C CODE IDENT NO. 32274 DRAWING NO. 360001-300 REV H
SCALE SHEET 31 OF

REVISION					
LTR	DESCRIPTION	DWN	DATE	APVD	DATE
	SEE SH. 1				







360001-300
REV A

TAPE DRIVE DAISY CHAIN CONNECTORS

REV STATUS	REV																							
OF SHEETS	SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

DO NOT SCALE DRAWING

CONTRACT NO.	APPROVALS	DATE
	DWN	
	CHK	
	MFG ENG	
	QC	
	COG ENG	
	PROD REL	

Cipher Data Products SAN DIEGO CALIF.

TITLE: SCHEM - FMTR, DUAL MODE, EMB.

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	32274	36CC01-300	A

SCALE

SHEET 32 OF

QTY GIVEN IS NUMBER OF PARTS OR LENGTH OF MATERIAL IN FEET

ITEM	CIPHER PART #	QTY	DESCRIPTION 1 / DESCRIPTION 2	MFG-NAME / MFG-PART#	REF-DES	ST-DATE	END-DATE
1	360001-300	REF	SCHEM-FMTR,DUAL MODE,EMB	CIPHER DATA PROD			
2	760001-101	1	PWB-FMTR,DUAL MODE,EMB	DIBBLE ELECTRONICS TYPE ML			
3							
4	760002-501	1	STIFFENER-END,NOTCHED	CIPHER DATA PROD			
5	760003-601	1	STIFFENER END	CIPHER DATA PROD			
6	760003-611	1	STIFFENER-BRIDGE	CIPHER DATA PROD			
7	- 9 ARE BLANK.						
10	731501-300	2	RETAINER-P/C CONNECTOR	CIPHER DATA PROD			
11	211001-150	3	HEADER-PCB	AMP INC. 2-87565-0	XJ101,102,103		
12	210040-046	6	SPACER-CONNECTOR	AMP PROD. PLAN Y 102285-1			
13							
14	731006-800	1	LABEL-ASSY	CIPHER DATA PROD			
15							
16	201191-063	4	CAPACITOR-ALUM WITH EPOXY END SEAL,22UFD,6.3V	PANASONIC CO. ECEBOJV220SR	C1,2,4,5		
17	201105-101	45	CAP-CER DISK,.1UF,10V	CENTRALAB UK10-104	C6-23,26-52		
18	201105-010	2	CAP-CER,DISK,.01UF,500V	CERA-MITE 5HKS-S10	C24,25		
19	201161-470	1	CAP-TANT 47UF 6V 10%	NATIONAL COMPONENT IND. CS13BB476K	C3		
20	201112-100	1	CAP-CER,100PF,50V,10%	CENTRE ENGINEERING G2610-050-NPO-101K	C53		
21	210114	2	TERMINAL-QUICK DISCONNECT TAB, RIGHT ANGLE	KEYSTONE 1256	E1,2		
22							

QTY GIVEN IS NUMBER OF PARTS OR LENGTH OF MATERIAL IN FEET

ITEM	CIPHER PART #	QTY	DESCRIPTION 1 / DESCRIPTION 2	MFG-NAME / MFG-PART#	REF-DES	ST-DATE	END-DATE
23	204012-999	2	TRANSISTOR,PNP SILICON	TEXAS INSTRUMENTS 2N3702	R1,2		
24							
25	205254-500	1	RES,NETWORK,SIP,4.7K OHM	BOURNS INC. 4308-R-101-472	R1		
26	205252-100	2	RES NETWORK,470 OHMS,SIP	BOURNS INC. 4308R-101-471	R5,6		
27	200071-100	2	RES-FC 10 OHM 1/4W 5%	NOT ON FILE RCR07G100JM	R9,10		
28	200072-470	2	RES-FC 470 OHM 1/4W 5%	NOT ON FILE RCR07G471JM	R2,3		
29	200073-100	4	RES-FC 1.00K 1/4W 5%	NOT ON FILE RCR07G102JM	R7,8,15,16		
30	200073-150	4	RES-FC 1.50K 1/4W 5%	NOT ON FILE RCR07G152JM	R11,12,13,14		
31	200073-470	7	RES-FC 4.70K 1/4W 5%	NOT ON FILE RCR07G472JM	R4,17-22		
32	200072-620	1	RES-FC 620 OHM 1/4W 5%	NOT ON FILE RCR07G621JM	R23		
33							
34							
35	211015-001	1	SWITCH-DIP,4POS,SEALED	AMP INC. 3-435668-4	S1		
36	211015-005	2	SWITCH-DIP,6 POS SEALED	AMP INC. 2-435668-6	S2,3		
37	210806-001	1	SWITCH-ROTARY SELECTOR	SPECTROL 87-11-15	S4		
38							
39							
40	205026-999	78	TEST POINT .058 DIA PIN	AMP INC. 60802-2	TP1-78		
41							
42							
43	211011-008	2	SOCKET,8 PIN LOW PROFILE	AUGAT 208-AG39D	XU7C,XU7E		
44	211011-016	2	SOCKET,16 PIN LOW PROFILE	AUGAT 216-AG39D	XU9P,XU15P		

QTY GIVEN IS NUMBER OF PARTS OR LENGTH OF MATERIAL IN FEET

ITEM	CIPHER PART #	QTY	DESCRIPTION 1 / DESCRIPTION 2	MFG-NAME / MFG-PART#	REF-DES	ST-DATE	END-DATE
45	205255-500	2	RESISTOR NETWORK-220/330	BECKMAN INSTRUMENTS,INC. 898-5-R220/330	U9P,15P		
46	970221-001	18	IC-QUAD 2 INPUT POS,NAND GATE	TEXAS INSTRUMENTS SN74LS00N	U2B,3H,4J,10D,10K11E, 14J,16F,16M,16N,17D, 18D,19M,20B,20P,20R, 20T,20V	08-01-83	L*109
47	203081-001	5	IC-QUAD 2INPUT POS-NOR-GA	TEXAS INSTRUMENTS SN74LS02N	U4E,6B,9B,10F,15F		
48	970011-001	11	IC-HEX INVERTER	TEXAS INSTRUMENTS SN74LS04N	U3P,5K,5M,6H,7A,9E,,, 10C,,12E,18N,19B,19R		
49	203026-600	2	IC-TTL HEX,INVERTER POS NAND (OPEN COLLECTOR)	TEXAS INSTRUMENTS SN74LS05N	U1V,1P	04-01-83	L*107
50	970010-001	18	IC-QUAD 2 INPUT POS AND GATE	TEXAS INSTRUMENTS SN74LS08N	U2E,3B,4H,5B,5D,5F, 5N,8J,9C,11D,15E,18R, 18V,19N,19T,19V,20M, 20N	04-01-83	L*108
51	203029-002	9	IC-TPL 3-INP POS-NND GT	TEXAS INSTRUMENTS SN74LS10N	U2F,5A,5L,8C,8F,11H,, 11K,13J,14K		
52	203085-001	6	IC-SCHM,TRIG INPUT,HEX IV	TEXAS INSTRUMENTS SN74LS14N	U5J,7P,14P,16P,17P		
53	203031-100	2	IC-DUAL 4-INPUT NAND GATE	TEXAS INSTRUMENTS SN74LS20N	U3F,14A		
54	203034-100	6	IC,8-INPUT NAND GATE	TEXAS INSTRUMENTS SN74LS30N	U8E,10P,13D,13E,15K,, 16L		
55	203035-032	7	IC,QUAD 2 INPUT POSORGATE	TEXAS INSTRUMENTS SN74LS32N	U4C,5E,7L,13C,17C,,,, 19D,20D		
56	203061-033	2	IC-QUAD 2IN NOR BFR OC	TEXAS INSTRUMENTS SN74LS33N	U12P,11P		
57	203036-038	9	IC-QUAD,2INP,POS NAND BUF	TEXAS INSTRUMENTS SN74LS38N	U3J,3K,4K,4P,5P,6N,,, 6P,11N,13P		
58	203038-100	7	IC-DUAL 2W-2I,AND-OR-INVT	TEXAS INSTRUMENTS SN74LS51N	U1A,1C,1D,2R,6A,9J,,, 13K		
59	203038-054	1	IC-4 WIDE,AND OR INVT GTE	TEXAS INSTRUMENTS SN74LS54N	U9D		
60	203039-001	12	IC-DUAL-D FLIP-FLOP	TEXAS INSTRUMENTS SN74LS74N	U1B,3D,6M,7J,7M,10H,, 14M,14N,15J,15M,15N,, 16K		

QTY GIVEN IS NUMBER OF PARTS OR LENGTH OF MATERIAL IN FEET

ITEM	CIPHER PART #	QTY	DESCRIPTION 1 / DESCRIPTION 2	MFG-NAME / MFG-PART#	REF-DES	ST-DATE	END-DATE
61	203040-085	1	IC-4 BIT MAGTD COMPTR	TEXAS INSTRUMENTS SN74LS85N	U19A		
62	203042-001	12	IC-QUAD EXCLUSIVE OR GATE	TEXAS INSTRUMENTS SN74LS86N	U6L,7H,8K,8L,8M,12B,, 13H,14F,14H,18T,18W,, 19P		
63	203094-501	45	IC-DUAL J-K POS-EDGE-TRIG	TEXAS INSTRUMENTS SN74LS109AN	U3E,4A,4B,4D,4F,4N, 5C,5H,6F,6J,7F,8A,8B, 9A,9F,9H,10A,10E,11F, 11J,12H,13A,14B,14C, 14D,14E,17K,17L,17M, 17N,18B,18H,18J,18K, 18L,18M,19H,19J,19K, 19L,20F,20H,20J,20K, 20L		
64							
65	203046-151	9	IC-1 OF 8 DATA SEL/MUXR	TEXAS INSTRUMENTS SN74LS151N	U1E,2C,2D,10L,11A,,,, 11B,16H,16J,,20C		
66	203046-153	1	IC,4-1 LINE SEL/MLTP	TEXAS INSTRUMENTS SN74LS153N	U15D		
67	203046-155	1	IC-DECODER/MULTIPLEXER	TEXAS INSTRUMENTS SN74LS155N	U18C		
68	203047-157	2	IC-QUAD,2 TO 1 LINE,DATA	TEXAS INSTRUMENTS SN74LS157N	U11L,15C		
69	203048-100	18	IC-SYN,4-BIT COUNTER	NATIONAL SEMICONDUCTORS DM74LS161N	U3M,3N,4M,7B,11C,12D, 12F,17E,17F,17H,17J,, 18A,18E,18F,19C,19E,, 19F,20E		
70	203049-164	9	IC-8-BIT PARALLEL OUTPUT, SERIAL SHIFT REC	TEXAS INSTRUMENTS SN74LS164N	U13L,13M,13N,15A,15B, 16A,16B,17A,17B		
71	203051-174	16	IC,HEX D-TYPE FLIP FLOP	TEXAS INSTRUMENTS SN74LS174N	U6K,7N,9K,9L,10B,12A, 12L,13B,13F,16C,16D,, 17R,17T,17V,17W,18P		
72	203051-100	3	IC-QUAD D-TYPE FLIP-FLOP	TEXAS INSTRUMENTS SN74LS175N	U12J,14L,15L		
73	203061-280	2	IC-PARITY TREE,9 INPUT	TEXAS INSTRUMENTS SN74LS280N	U7K,15H		

QTY GIVEN IS NUMBER OF PARTS OR LENGTH OF MATERIAL IN FEET

ITEM	CIPHER PART #	QTY	DESCRIPTION 1 / DESCRIPTION 2	MFG-NAME / MFG-PART#	REF-DES	ST-DATE	END-DATE
74	203052-283	1	IC-4-BIT BIN FULL ADDER	TEXAS INSTRUMENTS SN74LS283N	U16E		
75	203061-352	4	IC-MUX,DUAL 4 IN,INV. OUTPUTS	TEXAS INSTRUMENTS SN74LS352N	U9M,9N,10M,10N		
76	203052-378	4	IC-HEX,D-TYPE FLIP-FLOPS	TEXAS INSTRUMENTS SN74LS378N	U8H,12M,12N,20A		
77	203052-379	1	IC-QUAD D-TYPE FLIP-FLOPS	TEXAS INSTRUMENTS SN74LS379N	U3L		
78	203052-300	5	IC-DUAL 4 BIT COUNTER	TEXAS INSTRUMENTS SN74LS393N	U2A,3A,3C,8D,12K		
79	203062-030	1	IC-NAND,8 INPUT	TEXAS INSTRUMENTS SN74S30N	U2N		
80	203062-074	1	IC-FF,DUAL,TYPE D	TEXAS INSTRUMENTS SN74S74N	U2M		
81	799607-001	2	INTERCHANGABLE 4 BIT COUNTER	CIPHER DATA PROD	U1N,2P		
82	203026-999	1	IC-HEX INVERTER	TEXAS INSTRUMENTS SN7404N	U4L		
83	203067	1	IC-QUAD 2-INP POS-NND BFR	TEXAS INSTRUMENTS SN7437N	U12C		
84	203036	1	IC-QUAD 2-INP POS-NND BFR	TEXAS INSTRUMENTS SN7438N	U11M		
85	203071-999	1	IC-DUAL V CONT MLTV	MOTOROLA SEMI. MC4024P	U6D		
86	203012-999	2	IC-PHASE FREQ DET	MOTOROLA SEMI. MC4044P	U6C,6E		
87	203029-500	2	IC-HEX ST INVERTER	TEXAS INSTRUMENTS SN7414N	U8N,8P		
88							
89							
90	210222-216	1	CLOCK-CRYSTAL,HYBRID 21.6 MHZ	MOTOROLA SEMI. K1114A,21.6 MHZ	U2T		
91	210222-194	1	CLOCK-CRYSTAL,HYBRID, 19.44 MHZ	MOTOROLA SEMI. K1114A,19.44 MHZ	U2V		
92	- 95 ARE BLANK.						

QTY GIVEN IS NUMBER OF PARTS OR LENGTH OF MATERIAL IN FEET

ITEM	CIPHER PART #	QTY	DESCRIPTION 1 DESCRIPTION 2	MFG-NAME MFG-PART#	REF-DES	ST-DATE	END-DATE
96	213271-405	5	SCREW-PAN HD PHIL, 4-40 X 5/16,CAD,BLK,ZINC	ANY ACCEPTABLE SOURCE			
97	213271-409	2	SCREW-PAN HD PHIL, 4-40 X 9/16,CAD,BLK,ZINC	ANY ACCEPTABLE SOURCE			
98	207402-021	7	WASHER,FLAT #4	ANY ACCEPTABLE SOURCE			
99	207403-011	7	WASHER,SPLIT LOCK #4	ANY ACCEPTABLE SOURCE WASHER #4 CAD.			
100	207405-051	4	NUT,HEX #4 4-40	NUT #4 CAD.			
101							
102							
103	210708-458	5	RIVET-BLIND	HARTWELL CORP. HNR4-5-8			
104	208500-298	.3	WIRE BUS TND COPPER 22AWG	ALPHA WIRE CORP. 298	W1,2,5		
105	209100-552	.3	TUBING TFL 22 GA	ALPHA WIRE CORP. TFT-200/22-NAT	W1,2,5		
106	**********						
107	203026-600	2	IC-TTL HEX,INVERTER POS NAND (OPEN COLLECTOR)	TEXAS INSTRUMENTS SN74LS05N	U1V,1P	L*49	03-31-83
108	203027-001	18	IC-QUAD 2-INP POS-AND GT	TEXAS INSTRUMENTS SN74LS08N	U2E,3B,4H,5B,5D,5F, 5N,8J,9C,11D,15E,18R, 18V,19N,19T,19V,20M, 20N	L*50	03-31-83
109	203023-001	18	IC-QUAD 2-INP POS-NND GT	TEXAS INSTRUMENTS SN74LS00N	U2B,3H,4J,10D,10K, 11E,14J,16F,16M,16N, 17D,18D,19M,20B,20R, 20T,20V	L*46	07-31-83