| APPLICATION | | REVISIONS | | | |
|---|---|---|---|---|---|
| NEXT ASSY | USED ON | REV. | DESCRIPTION | DATE | APPROVED |
| | CM6000 | A | NEW RELEASE | 2-11-85 | |

REV. | SH | DWG. NO.

PRELIMINARY

| | | | |
|---|---|---|---|
| UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ± | REMOVE BURRS AND SHARP EDGES. ALL DIAMETERS ON COMMON CENTERS TO BE CONCENTRIC WITHIN .005. | COMPUTER MEMORIES, INC. | |
| MATERIAL | APPROVALS / DRAWN | DATE | CM6000 THEORY OF OPERATION |
| FINISH | CHECKED Wm Mowry | 2-13-85 | SIZE A / FSCM NO. / DWG. NO. 600007 / REV. A |
| DO NOT SCALE DRAWING | ISSUED | | SCALE / SHEET 1 of 25 |

THEORY OF OPERATION #600007

The scope of this document is to familiarize the reader with the CM 6000 main board electronics.

A simplified block diagram of the main board is shown in Figure 1. The A.M.T. may be thought of as both a "talker" and a "listener". For example, when the A.M.T. issues a seek command, it is in effect "talking" to the drive, after which it "listens" for the drive to issue a seek complete.

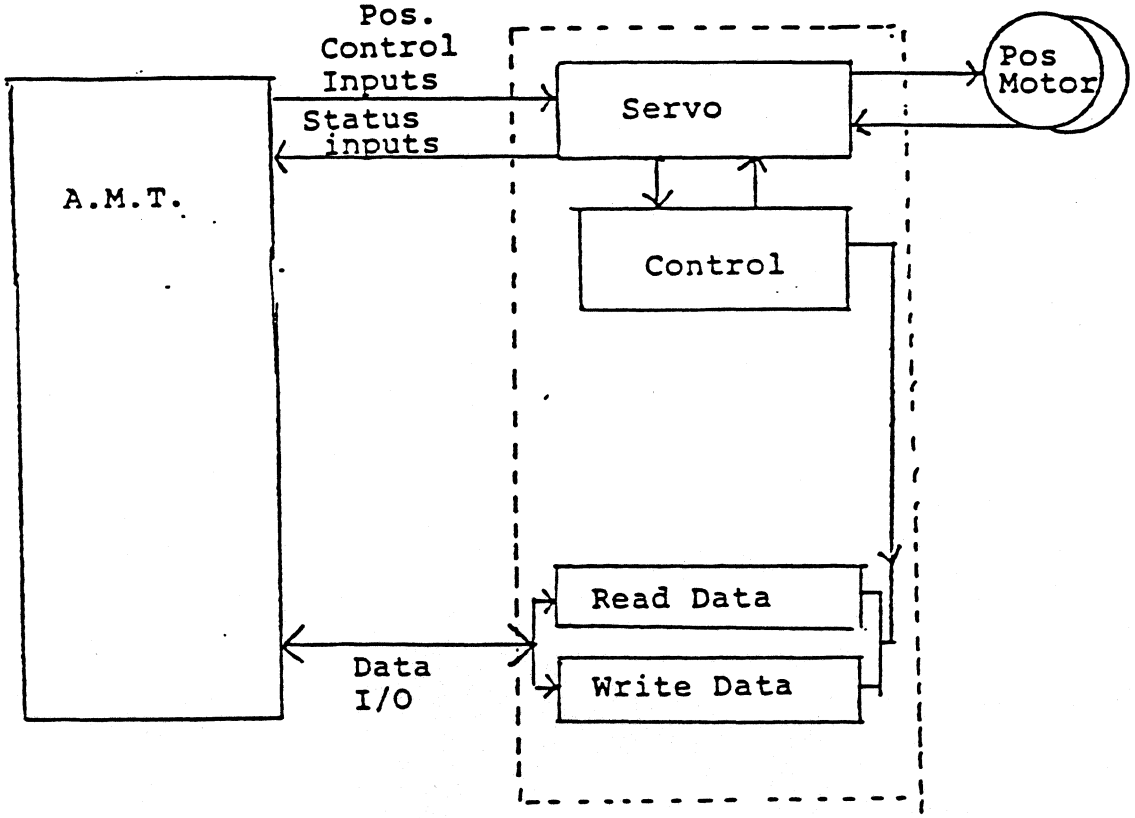



FIG. 1

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV. A |

Communication between the A.M.T. and main board may be broken down into two basic types. They are, Data I/O, and Control. The positioning contol inputs to the main board are shown in Fig. 2. Grounding any one of the drive select inputs, serves to "wake up" or "address" the drive. This may be accomplished by entering "Function 1" on the A.M.T.

Pulling the "Direction In" line low, causes an inward seek for every "step" pulse received. Converesely, letting the direction line "float" will instruct the drive to seek outward. Keep in mind that all of the input lines on the J1 connector, have pull up resistors connected to them. An open or intermittent cable on the A.M.T. may cause one of these lines to become inactive, often resulting in a "time out" condition on the A.M.T. when a seek operation is attempted.

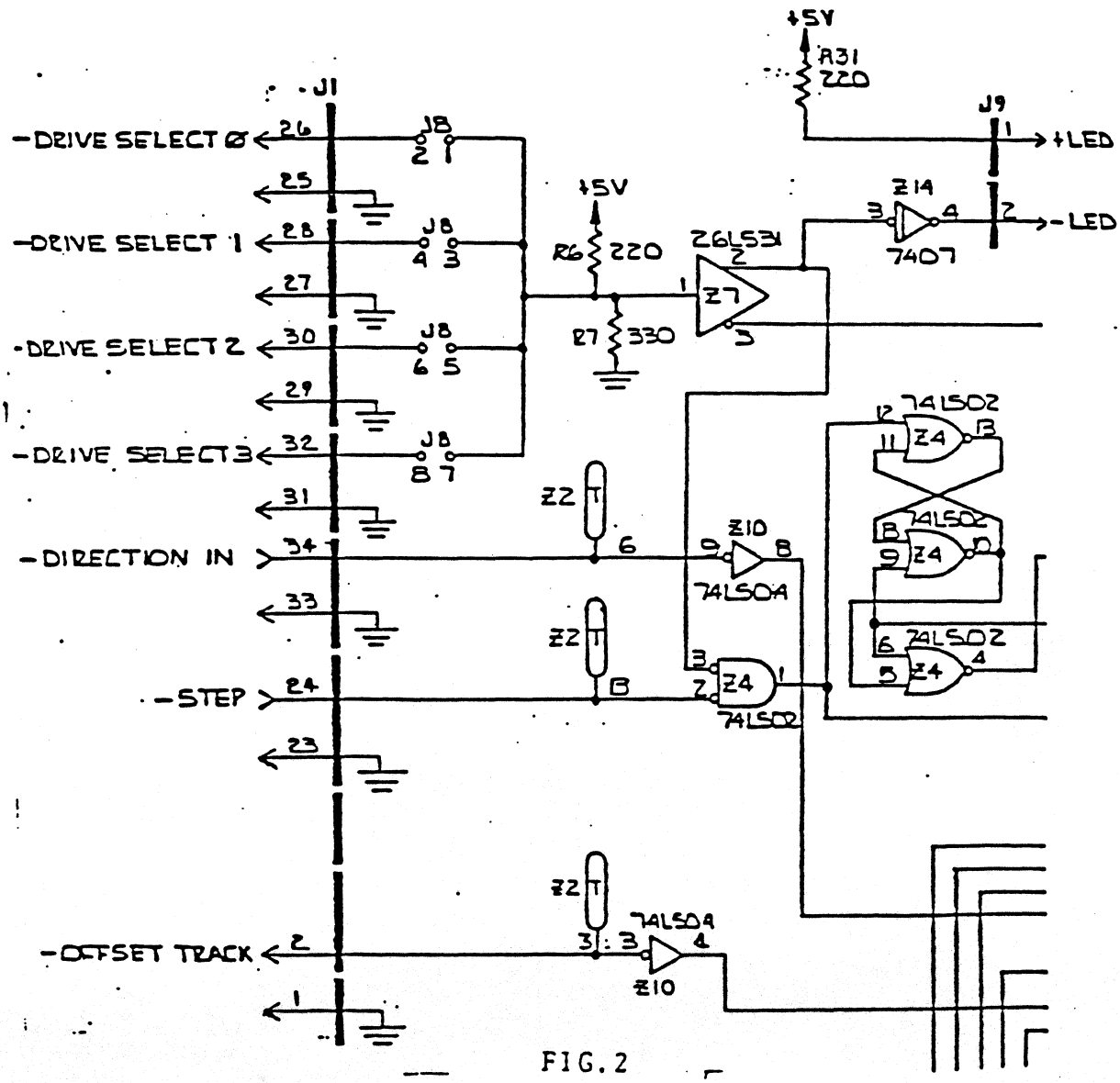


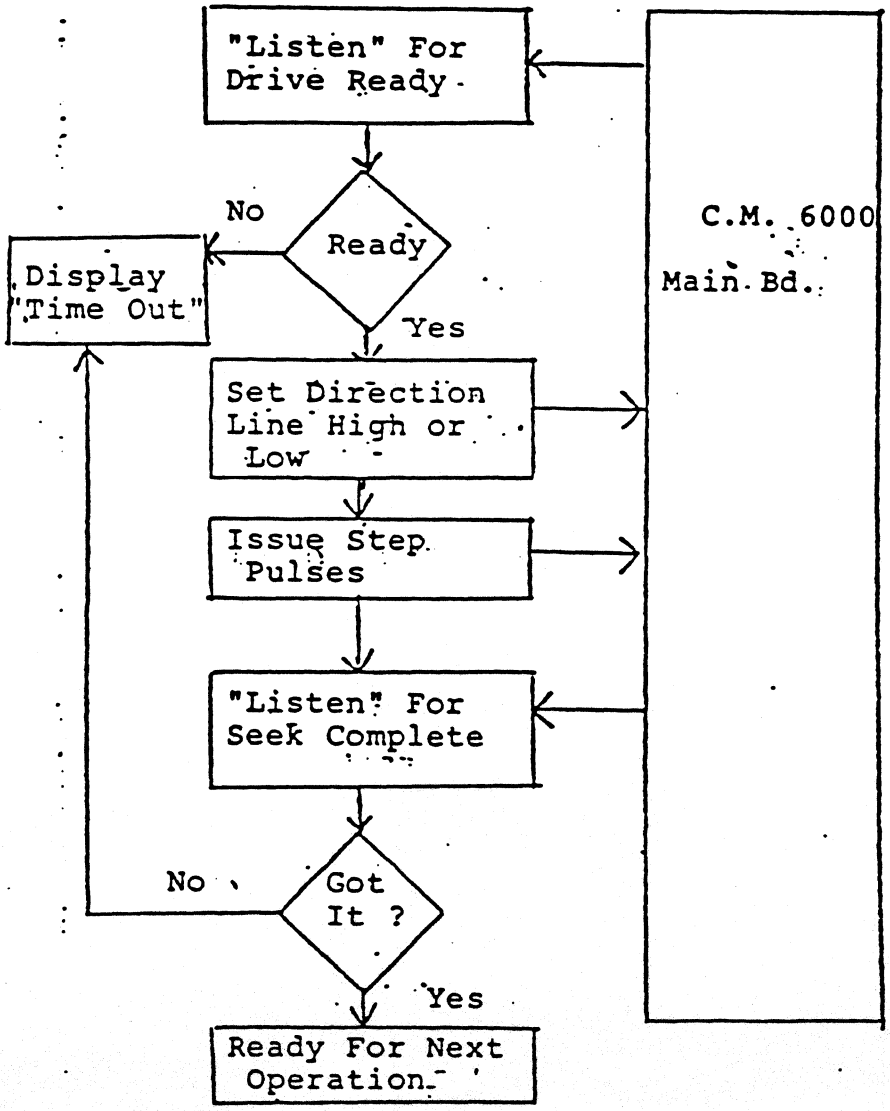

FIG. 2

| COMPUTER MEMORIES | | | |
|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 500007 |

As mentioned earlier, the A.M.T. acts as both a "talker" and a "listner". Let's pause for a moment and clarify what is meant by the term "listner" from the drives point of view. When the drive is not performing a seek or Read/Write operation, it is, in a sense, acting as a "listener".

For example, after power up and initilization, the drive acts as a "listener" and waits for the A.M.T. to select it. After sensing a low on any one of the drive select inputs, the drive, in turn, pulls the selected line low, informing the A.M.T. that it has been selected and is "on line". Refer to Figure 3.

This interaction, or "handshaking" between the drive and controller, prevents the A.M.T. from trying to issue a command to the drive, when it is not yet ready to do so. For example, during a seek operation a typical sequence of events are illustrated in the following flow chart.




| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV. |

Figure 3 shows the output status lines to the A.M.T. The A.M.T. uses these signals to verify the current condition, or state that the drive is in.

For example, when Function 4, (Rezero) is entered on the A.M.T., the A.M.T. sets the direction line high, and issues a series of step pulses to the main board. After issuing the step pulses, the A.M.T. "listens" for the Track 000 line to go low. Indicating that the head is in fact at Track Zero. If the A.M.T. does not detect a low on the Track 000 output line, after a fixed length of time, it will display "time out" indicating a fault has occured during Rezero.

The write fault output, shown in Figure 3, is used to alert the A.M.T. of a problem in the write circuitry. Although a number of conditions may cause this line to be set, most often the problem can be isolated to the write circuitry itself. More about that later.

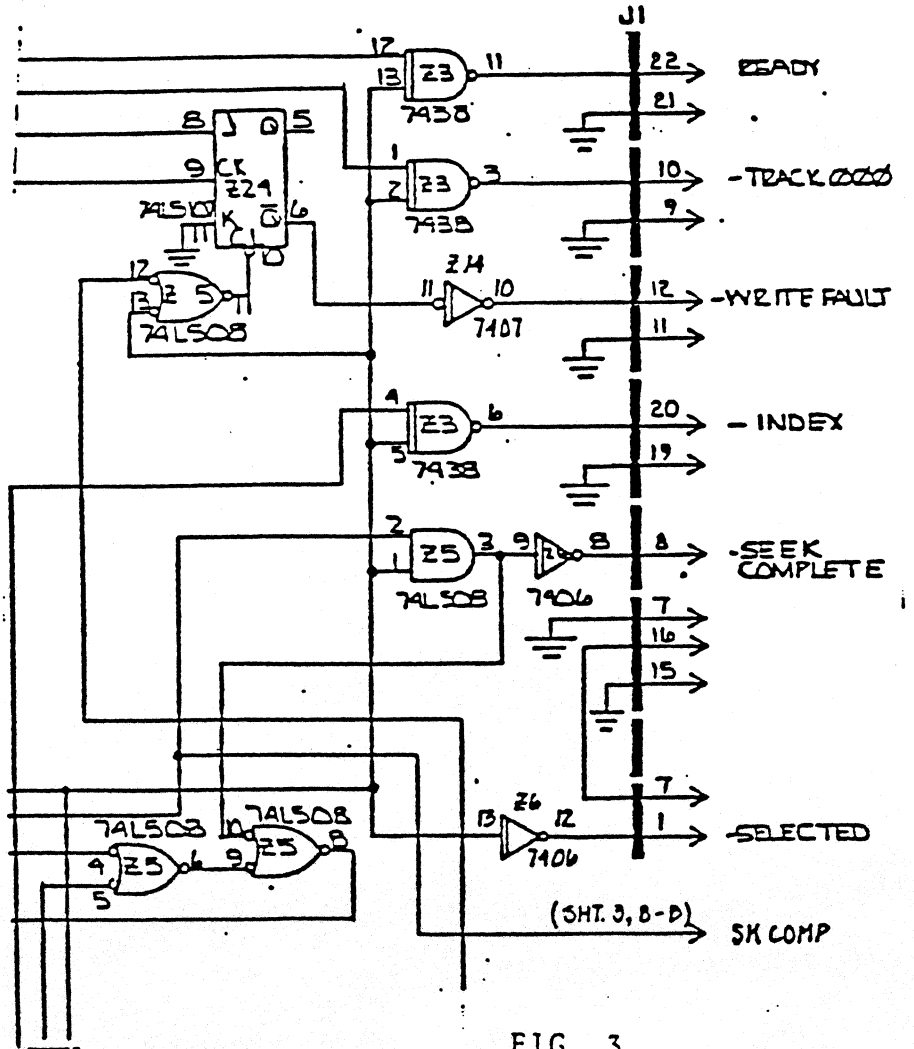



FIG. 3

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | R |

The main point to remember at this time however, is that a definite communication between the drive and the A.M.T. exists. By observing these output status lines, trouble shooting time may be greatly reduced.

As mentioned earlier, the CM6000 main board, may be broken down into four basic sections. They are as follows:

1- Control
2- Servo
3- Read \
4- Write / DATA I/O

We will begin by discussing the control section first. The control section consists of Z21 (6803 microprocessor), Z20 (EPROM) and Z19 (6522 P.I.A.).

Upon power up, the microprocessor is initially reset for approximatley40 ms. This is done to set up the internal registers in the processor and inhibit program execution until the power supply has had time to stabilize. The Reset signal is derived from hybrid 2 pin 4. The time duration of this signal is detemined by the value of C44.

After reset, the processor will begin its initilization routine. The following flowchart should help the reader to visualize the relationship between program execution inside the processor, and the "real word" outside the microprocessor.

REV.

SH

DWG. NO.

Set Spindle Motor Enable

Disable Brake

Start Spindle Motor

Set Motor Speed Control

" Listen" for Spindle Tach

Got It?

NO

Stop.

YES

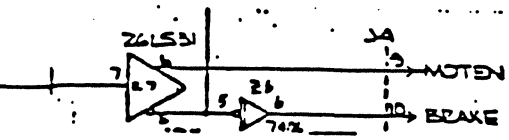
Speed O.K.?

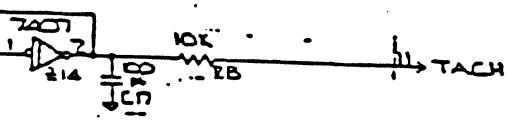
NO

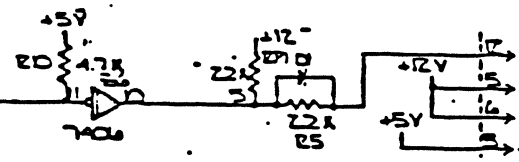
Update Motor Speed Control

YES

Go to Next Operation




| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | P |

Many routines that the processor performs, are similar in nature, to the spindle motor sequence. A command is issued (start spindle motor) and the processor "listens" for the spindle motor response by monitoring the tach output from the motor. Not only will the processor verify that the motor is spinning, but by measuring the time interval between pulses, can correct the motor speed by changing the duty cycle on the "Motor" control output line.

Many of the I/O discretes or "Talk, Listen" lines, are not connected directly to the microprocessor, but instead are connected to Z19. Refer to Fig. 4.

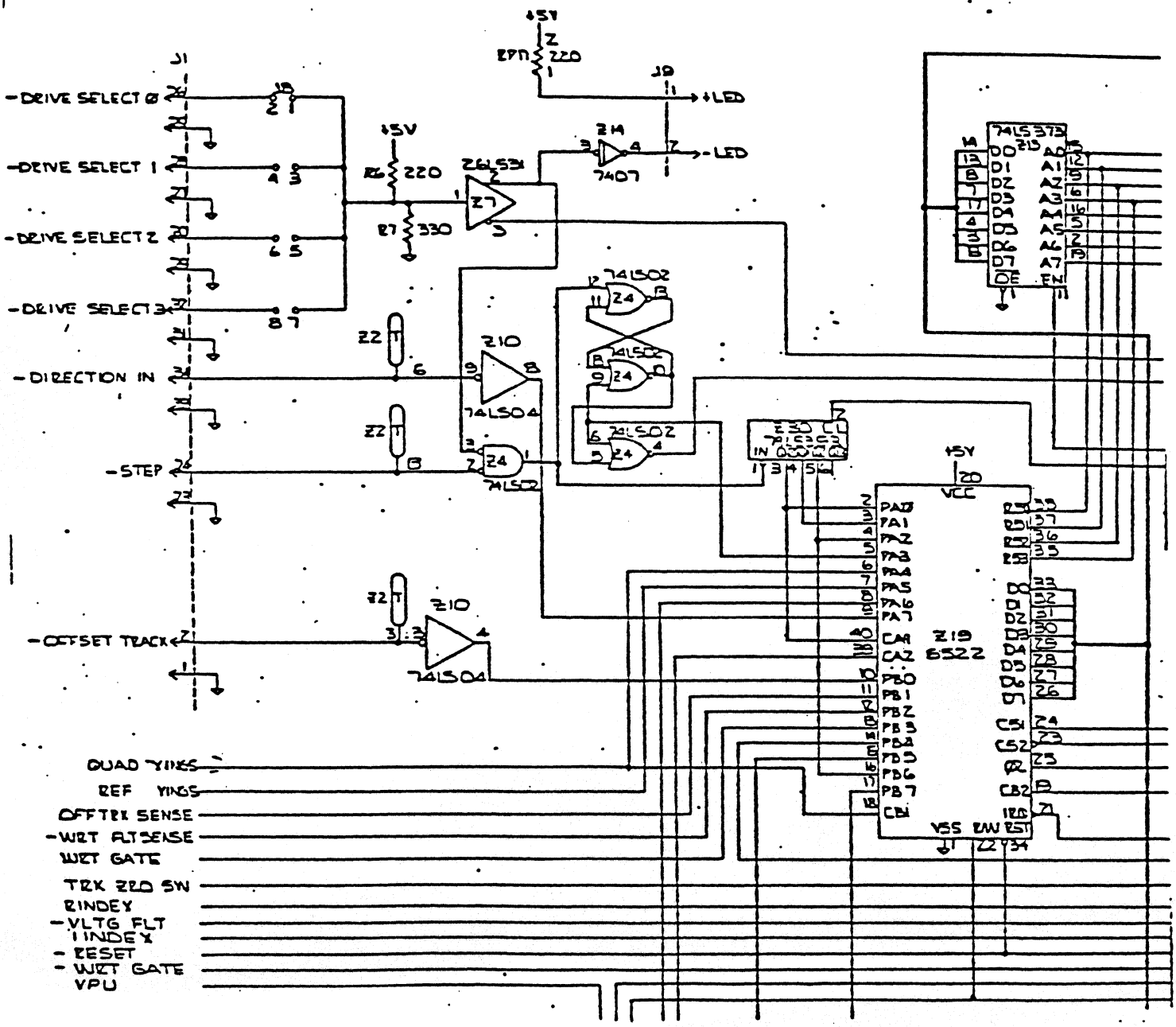



FIG 4

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV |

This I.C. is known as a P.I.A. (Periphial Inteface Adapter), and is widely used in many microprocessor based designs. This chip enables the processor to communicate with a greater number of I/O lines, then would normally be available without it.

The 6522 consists mainly of eight data lines (D0 to D7) and two bidirectional ports (PA0 to PA7 and PB0 to PB7). Each bit on the two ports may be configured as either an input or an output, hence the name "bidirectional".

For example, PA4 (pin 6 on 6522) is acting as an input for Quad Xings, while PA6 (Pin 8) is acting as an output line for Hi WC.

In this way, Z19 may be thought of as a "messenger" for the microprocessor.

At this time we will now discuss the servo circuit. If the reader is not familure with the servo burst correction concept, it is recommended that the Drive Debug Procedure, Dwg. no. 600005 be reviewed first. The debug procedure will provide general information about the servo such as, why it is needed, the relationship between the encoder and the track, etc.

Figure 5 illustrates a very basic servo system. In this example, we will assume that each time S1 is closed, the positioner motor will rotate 1 degree and that the feedback signal consists of digital pulses, with each low to high transition representing 1 degree of rotation in the positioner motor. Refer to the following flowchart. (See next page for flow chart)

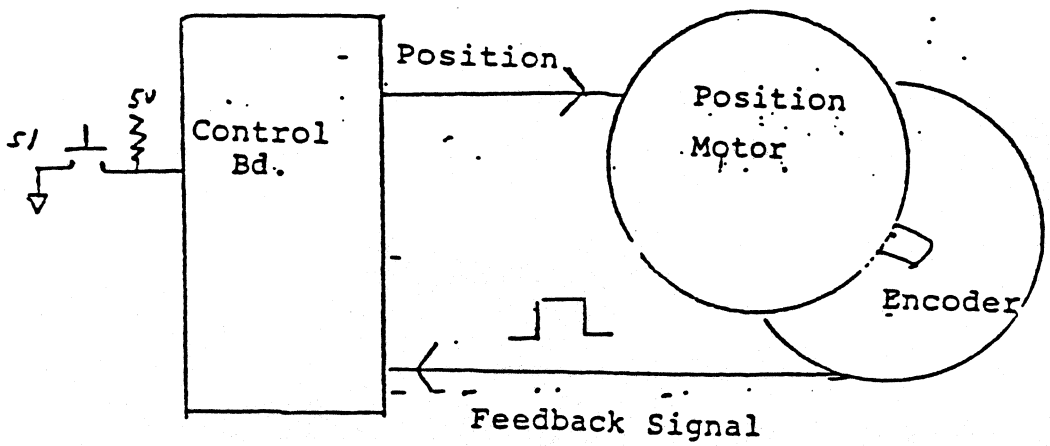
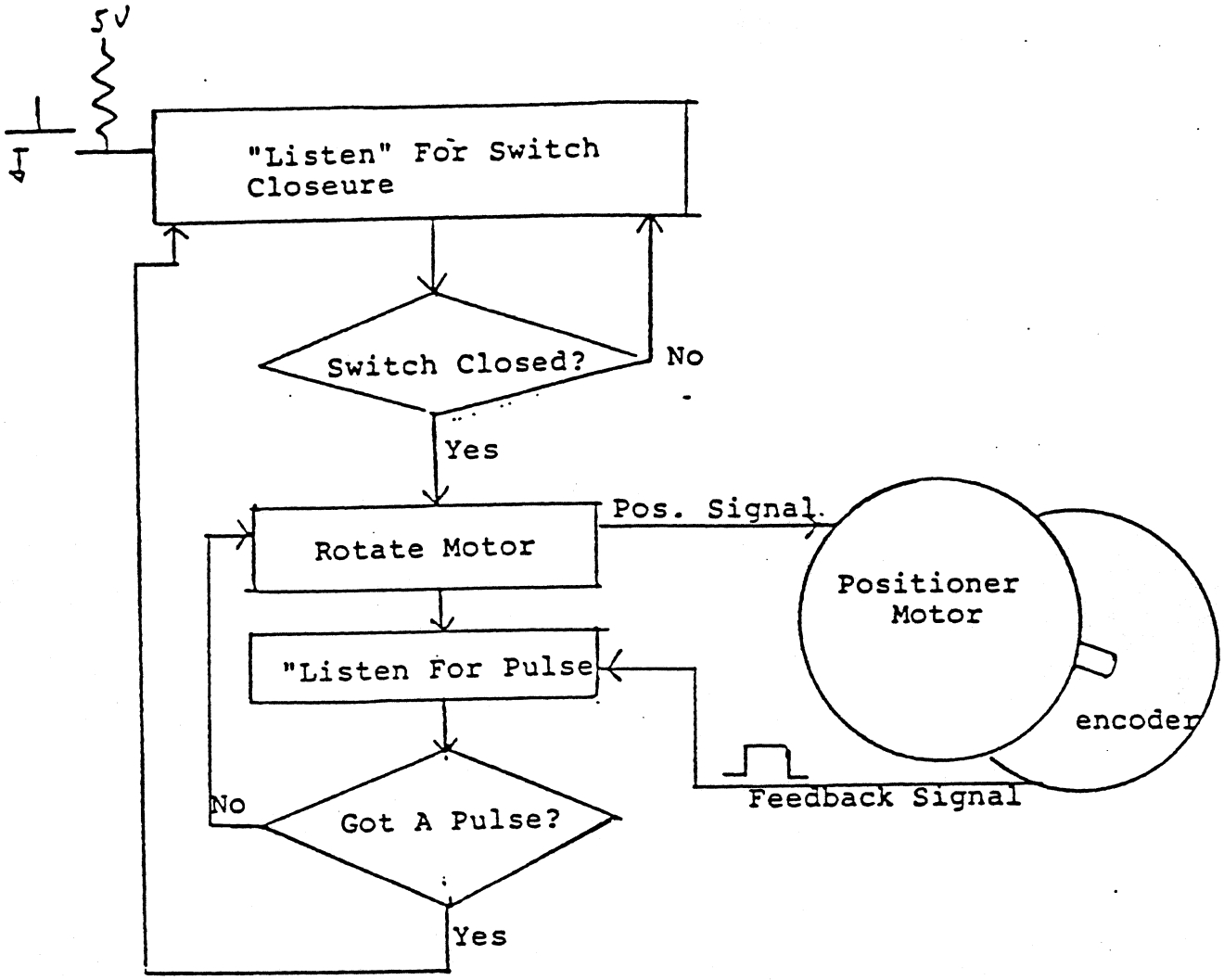



FIG. 5

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | RE |




| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV. A |

The "Talk", "Listen" approach may be used to describe the operation of our basic servo in Figure 5.

The control board "Talks" to the positioner motor through the position signal line and "Listens" to the feedback signal from the encoder indicating how far it has rotated. In this case, 1 degree of motor rotation for every pulse "Listened to" on the feedback line.

Now that we have established the basic concept of a closed loop servo, let's expand on that idea and discuss the CM6000 servo circuit. Refer to Figure 6. (Fig.6 on next page). Although more complex then our servo in Figure 5, the servo in Figure 6 operates on the same basic principle.

For example, in our simple servo in Figure 5, when we wanted to rotate the positioner motor, we closed S1. The motor would rotate one degree each time we closed this switch. In Figure 6 we have replaced the switch with step input. Each time this line is pulled low, the positioner motor rotates an increment that is equivelent to one track. In terms of degrees of rotation this is approximatley .06 degrees per track.

In Figure 5, the motor was controlled by the positioner signal line. In Figure 6 the "Vel ref" signal may be thought of as our positioner signal. Since the microprocessor generates this signal, it must first be transformed to a signal that the motor can "understand". This is accomplished by the use of a D/A (digital to analog) converter, (Z12). As the name implies, this chip will accept binary or digital information from the processor and convert it into a D.C. level that the positioner motor can use. This signal is fed into the power amp, which in turn drives the positioner motor.

On the servo in Figure 5, the Control Board looked at the pulses on the feedback line, to tell it when the motor had rotated one degree.

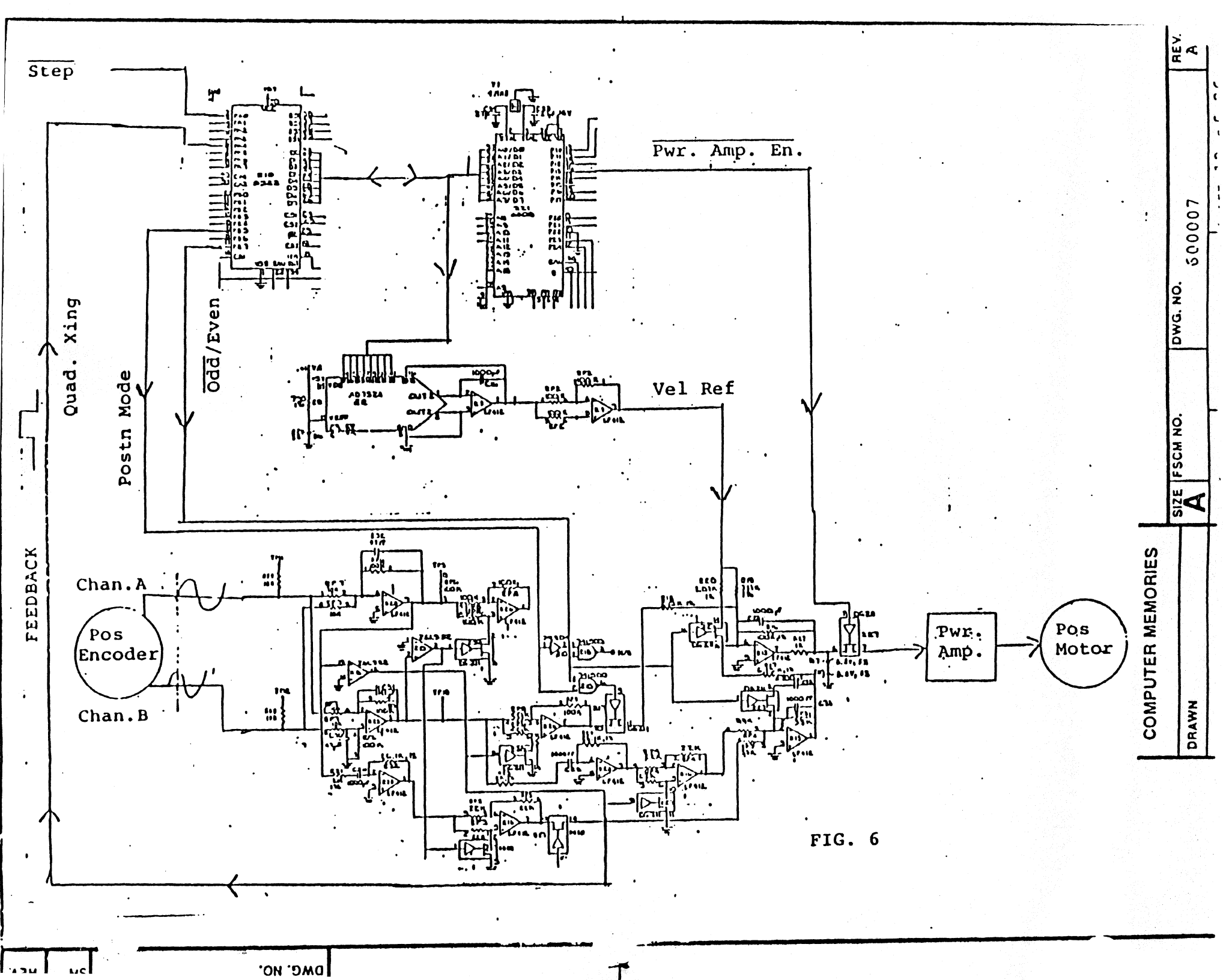

Step
Pwr. Amp. En.
Odd/Even
Quad. Xing
Postn Mode
Vel Ref
Chan.A
Pos Encoder
Chan.B
FEEDBACK
Pwr. Amp.
Pos Motor
COMPUTER MEMORIES
SIZE A
FSCM NO.
DWG. NO. 500007
REV. A
DRAWN
DWG. NO.

FIG. 6

The servo in Figure 6 is similar in this respect, the main difference being in the encoder. Let's pause for a moment and discuss the encoder used on the CM6000. In general, the encoder consists of a glass disc that is connected to the positioner motor shaft, as the shaft rotates so does the encoder disk. Refer to Figure 7.

As the encoder disc rotates, the amount of light reaching the photo transistor varies with it. This signal variation is further conditioned by circuitry inside the encoder and the resultant signals may be observed at the channel A and channel B output of the positioner motor.

Depending on the direction of rotation, channel A will lead or lag channel B by 90 degrees.

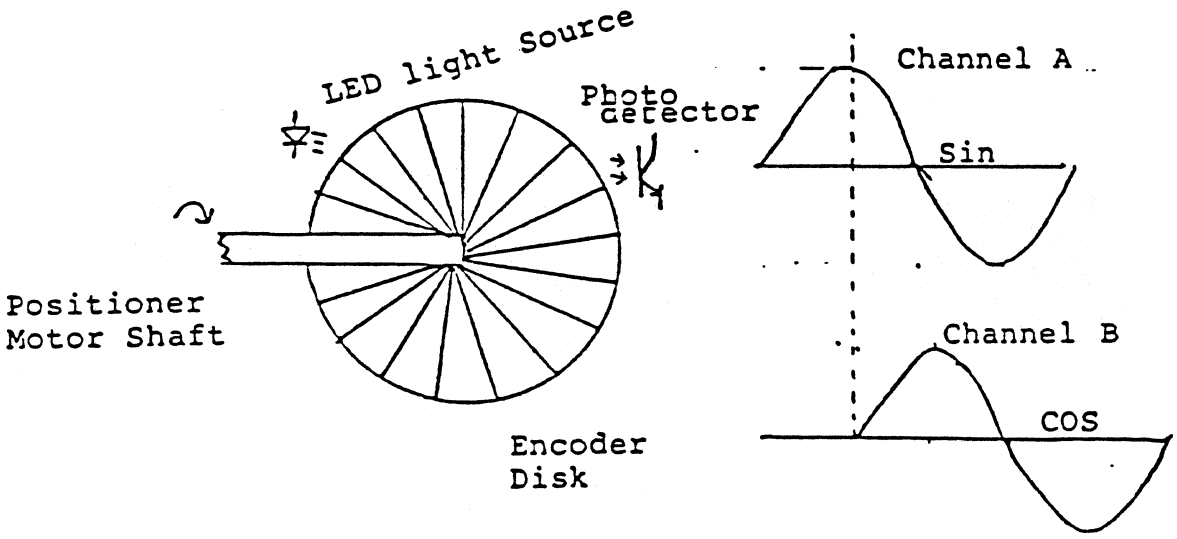



FIG 7

Since the microprocessor cannot make use of an analog signal, channel A and B must first converted into a digital form. This is accomplised by feeding channel A and B into a summing amplifier (Z 25 pin 6) and a differential amplifier (Z25 pin 2). The resultant "Sum" and "Differance" signals are then fed into a pair of zero crossing detectors and converted into TTL levels. Refer to Fig. 7.1

Notice that the zero crossing point of the encoder output at T.P. 10 corresponds to the track center on the disc. Also note that the zero crossing point of T.P. 10 occurs at the center of each Quad Xing bit. Since the microprocessor "Listens" to the Quad Xings, it can determine the track boudries by "Listening" for Quad Xing to change state.

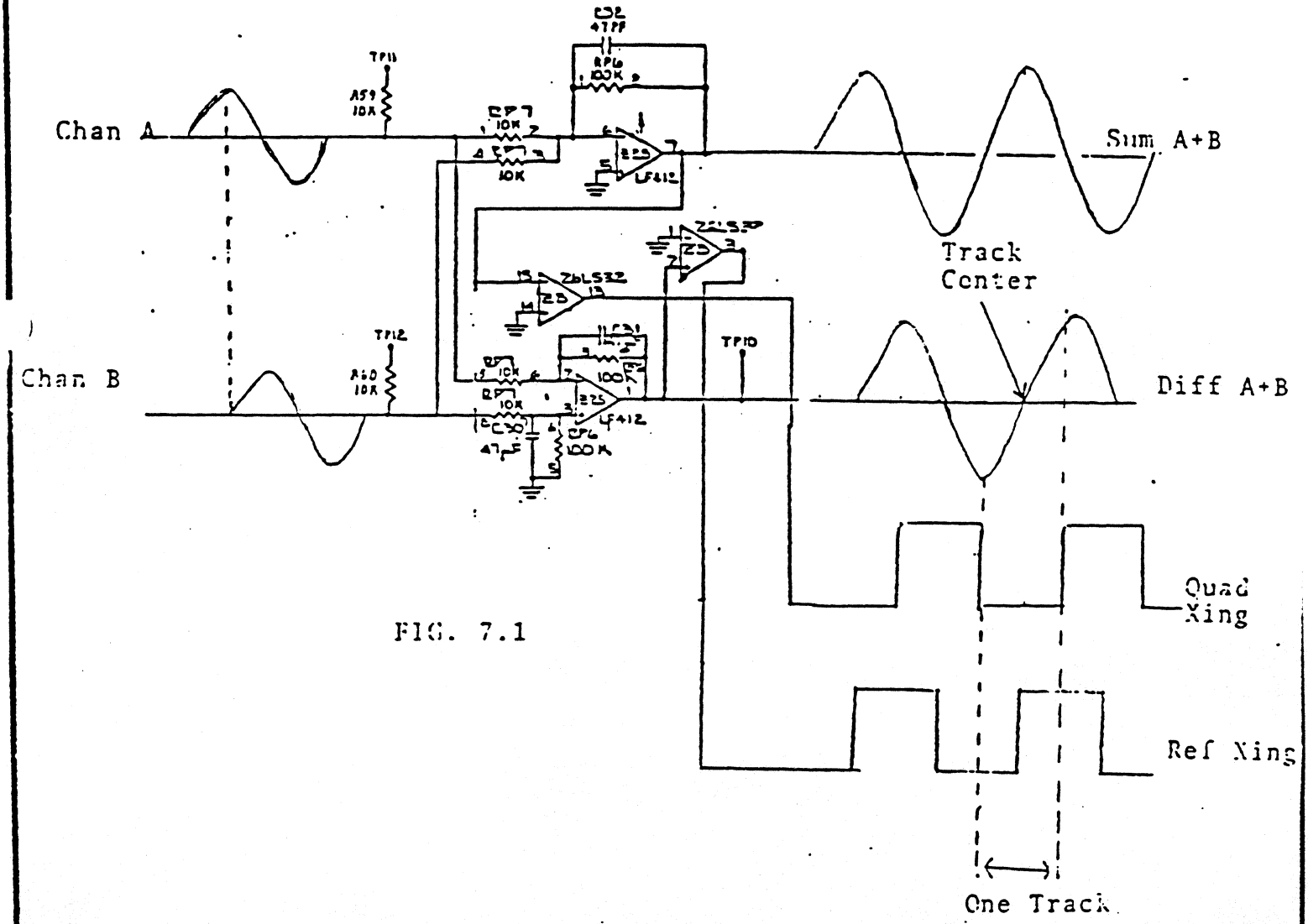
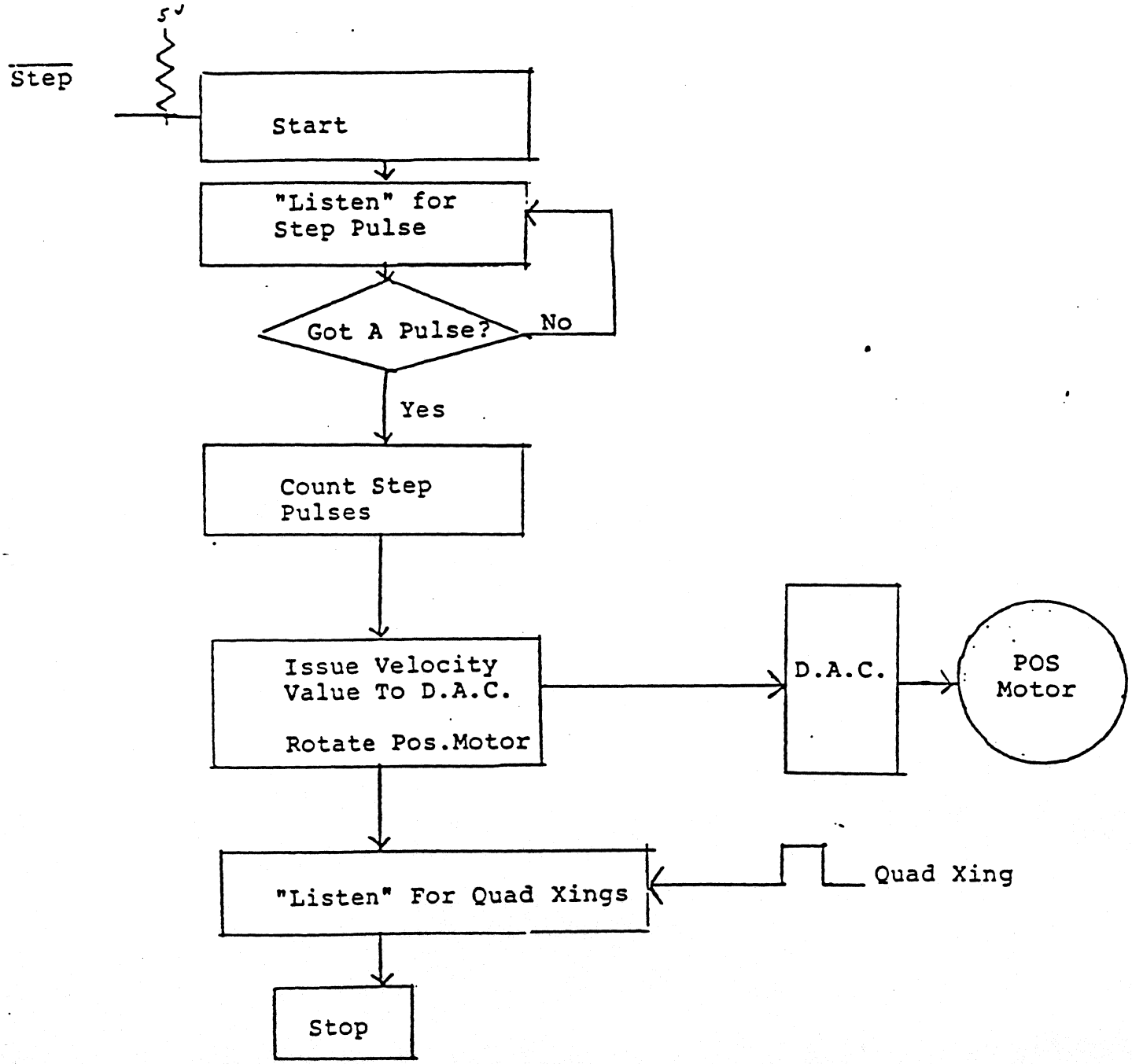



FIG. 7.1

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV |

Let's pause now and review what we have covered so far, refer to the following flowchart (Fig. 7.2):




| | | | | |
|---|---|---|---|---|
| COMPUTER MEMORIES | | | | |
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 300007 | R' |

Now that a basic overview of the CM6000 servo has been established, we may now analyze the circuit in greater detail.

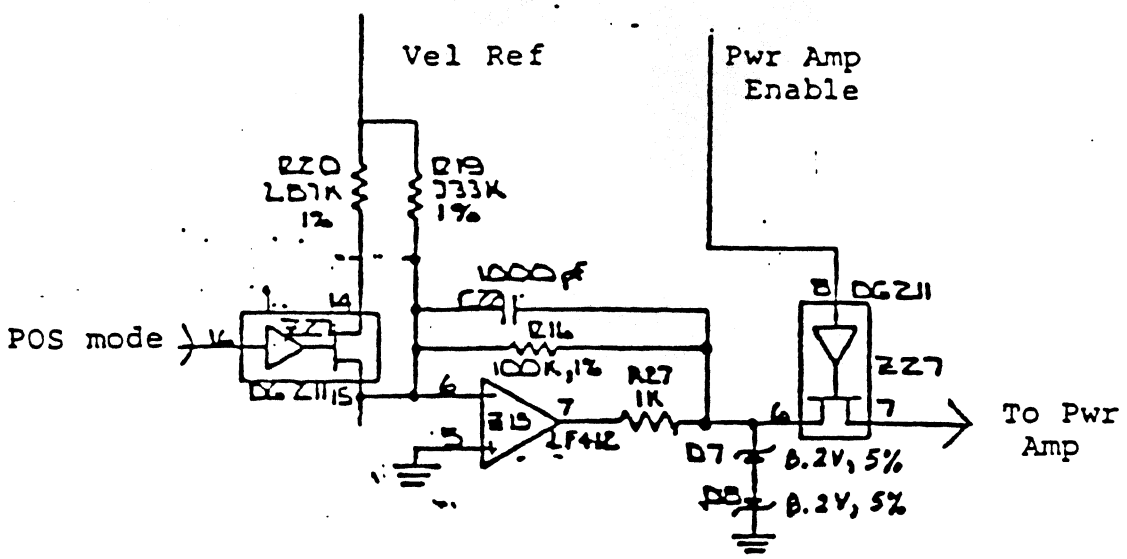
You may have wondered at this point, how the microprocessor is able to rotate the positioner motor very fast, (approximatley 200 tracks in 40 ms) and still manage to stop the head on the right track.

As you know, the microprocessor counts the quad Xings and uses them to determine how many tracks the positioner motor has rotated. If the processor "knew" how many tracks it had to rotate the positioner motor, it could then reduce the velocity signal low enough so the positioner motor would not "overtshoot" in to the next track. The major drawback of using this scheme would be a slow access time. Access time is defined as the amount of time required for the head to seek from one track to some other "destination" track. To overcome this problem, the CM6000 makes use of two different modes of operation during a seek routine. They are, position mode, and velocity mode.

In the velocity mode, servo gain is very high and in the position mode, the servo gain is much lower. To understand how we can make use of the two different servo gains to achieve fast access time with minimum overshoot, try to think of the position mode as a sort-of "brake" for the positioner motor. Similar to the brake on an automobile.

We stated earlier that if the microprocessor knew how many tracks it had to seek to, it could adjust the velocity level and "land" on track. As it turns out, the microprocessor does know how many tracks it must seek to before it reaches the final or"destination tion" track.

Because the A.M.T. issues step pulses very fast, (25us intervals), the microprocessor can collect all of the step pulses before the final track is reached. Knowing this, we may now discuss how switching from the velocity mode to the position mode reduces the servo gain, thus enabeling the microprocessor to "put on the brakes" right before the head has reached its final "destination" track.




Z15 in Figure 8 is known as a "summing amplifier". Its ouput is the algebraic sum of the inputs, multiplied by the gain, (Av). Since we are only discussing the velocity reference signal input at this time, we will ignore all other signal inputs to this amplifier. Note that the POS mode line is connected to the input of Z27 analog switch. In the position mode, this input is high and Z27 acts as an open switch.

Recalling basic OP amp theory, the D.C. gain for this amplifier in the position mode is roughly equal to

$$\frac{R16\ 100K}{R19\ 133K} = Av\ .75$$

In the velocity mode, the POS mode line is low. When this occurs, Z27 is switched on and the input resistance to the amplifier is now the parallel combination of R19 and R20. The gain of the amplifier in this mode may be represented by

$$R16\ 100K \Big/ \frac{R20 \times R19}{R19+R20} = Av\ 36$$

As you can see, the gain (Av) of Z15 is much higher in the velocity mode.

When the microprocessor executes a seek routine, It goes into the position or low gain mode, one track before the destination track. This results in a fast access time with a minimum overshoot.

In the previous discussion, we focused our attention on the Vel Ref inpout to the summing amplifier (Z15). There are two other inputs to this amplifier besides Vel Ref. They are the velocity feed back input and the position null input. Lets look at the velocity feedback input to the summing amplifier first.

We mentioned earlier, that when seek command is accepted by the microprocessor, it issues a Vel Ref input to the summing amplifier and rotates the positioner motor until the head reaches its destination track.

The velocity feedback acts to "govern" or control the speed of the positioner motor during a seek operation. This signal is injected into the summing amplifier via R17 and is a type of negative feedback.

The velocity feedback signal is derived from two differentiator circuits Z28 outlined in Figure 9.

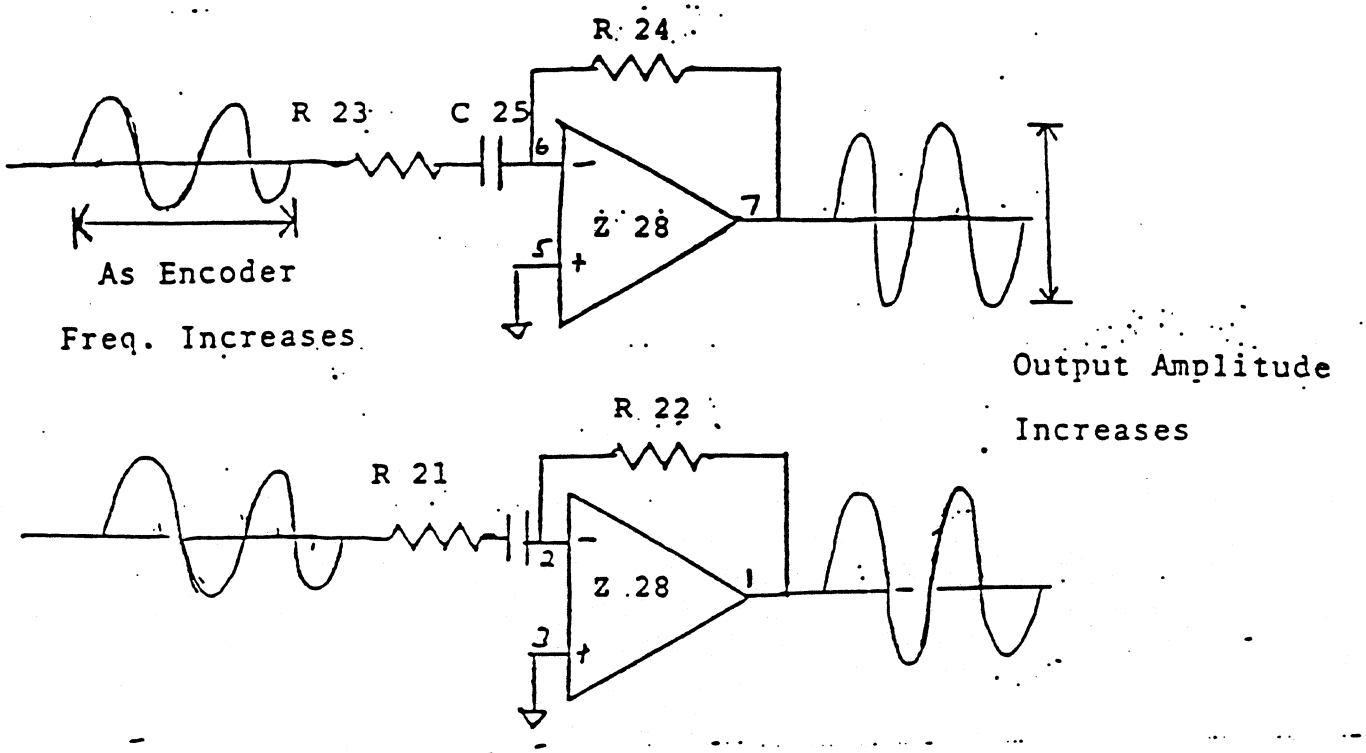



FIG 9

The differentiator circuit is such that the output will increase as the frequency of the input increases. In the case of the CM6000, the differentiator inputs are connected to the sum and difference amplifiers mentioned earlier. As the positioner motor rotates faster, the frequency of the encoder sinewave will increase and the output of the differentiator will also increase. Since the output of the differentiator tends to oppose the positioner motor rotation, it is considered to be a type of negative feedback.

The last input to the Z15 summing amplifier is the offset null signal. This signal is injected into the summing amplifier via R18 and is active during the position mode. This circuit is used to keep the head on track when no servo burst correction is used, such as when the drive is run with a preburn prom. Refer to Figure 9.1.

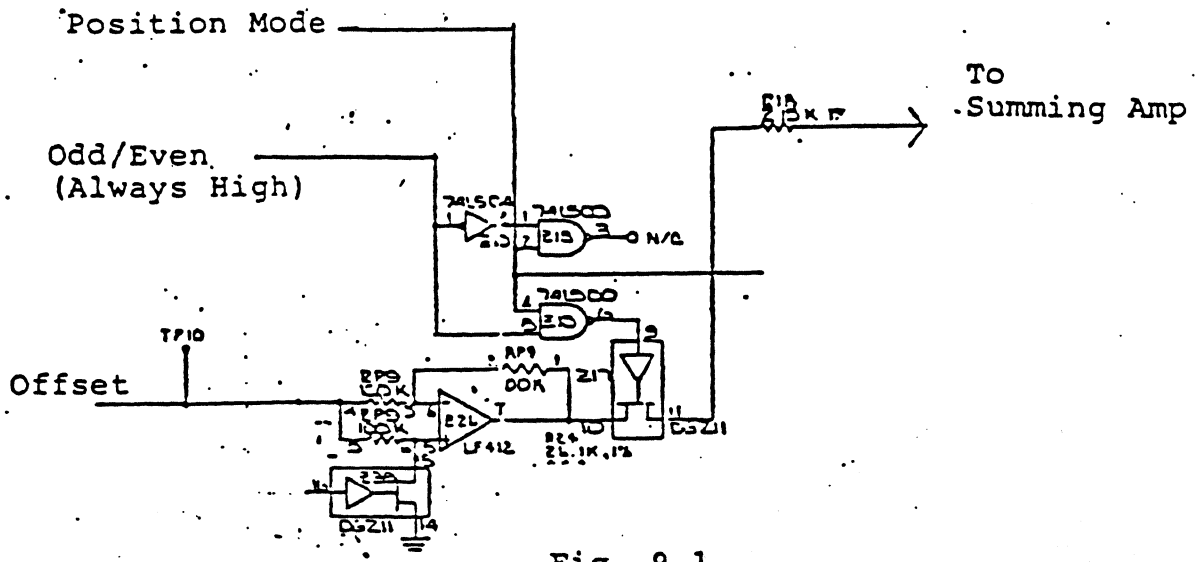



Fig. 9.1

For example, suppose the drive has been initilized and the drive head is positioned on track. If the head should start to drift from track center, the offset voltage at T.P.10 will increase or decrease. This voltage is fed into the summing amplifier via R18 and is such that it will cause the positioner motor to rotate back until T.P. 10 approaches zero. This is why T. P. 10 is always at or near zero when the preburn prom is used.

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 300007 | REV A |
| ISSUED | | | | |

We just mentioned that T.P. 10 will always be at or near zero, when the heads are stationary on track and the preburn prom is used. At this time, you may be wondering why the final or servo burst correction prom is needed at all. The reason is for thermal compensation. As explained in the Drive Debug Procedure, the mechanical components of the drive will expand as the drive warms up. And since the dirve heads are connected to these mechanical components, they too will move. If T.P. 10 was the only reference used to indicate the center of the track, as the drive warmed up, the heads would move off of the track center, yet the microprocessor would think that the heads are on track because T.P. 10 is at a zero voltage level! To overcome this problem, we need a method by which the head itself tells that microprocessor if it is on the center of the track, regardless of what value T.P. 10 is. This is where the servo burst correction comes into play.

The servo burst is written on the disc surface based on the zero crossing of T.P. 10. This is why it is very important that the drive has been warmed up, or temperature stabilized, before the servo burst is written on the disc. If we allow the mechanical components to expand to their normal operating dimensions when the servo burst is written, then T.P. 10 should be close to zero when we correct on the burst after the drive is warmed up.

We will now examine the servo burst decode circuit outlined in Figure 10. This circuit is commonly known as a sample and hold. The head output is amplified and fed to the base of Q3. Each time the analog switch (Z39) is turned on, the servo burst charges C39 and C38. The stored charge is compared by Z38 and the resultant offtrack sense signal is fed to the microprocessor. Refer to Figure 10.

The microprocessor "Listens" to the offtrack sense signal, and will rotate the positioner motor until the amplitude of Burst A equals the amplitude of Burst B. When Burst A = Burst B, the head is at track center. The servo burst correction occurs only when the final prom is used.

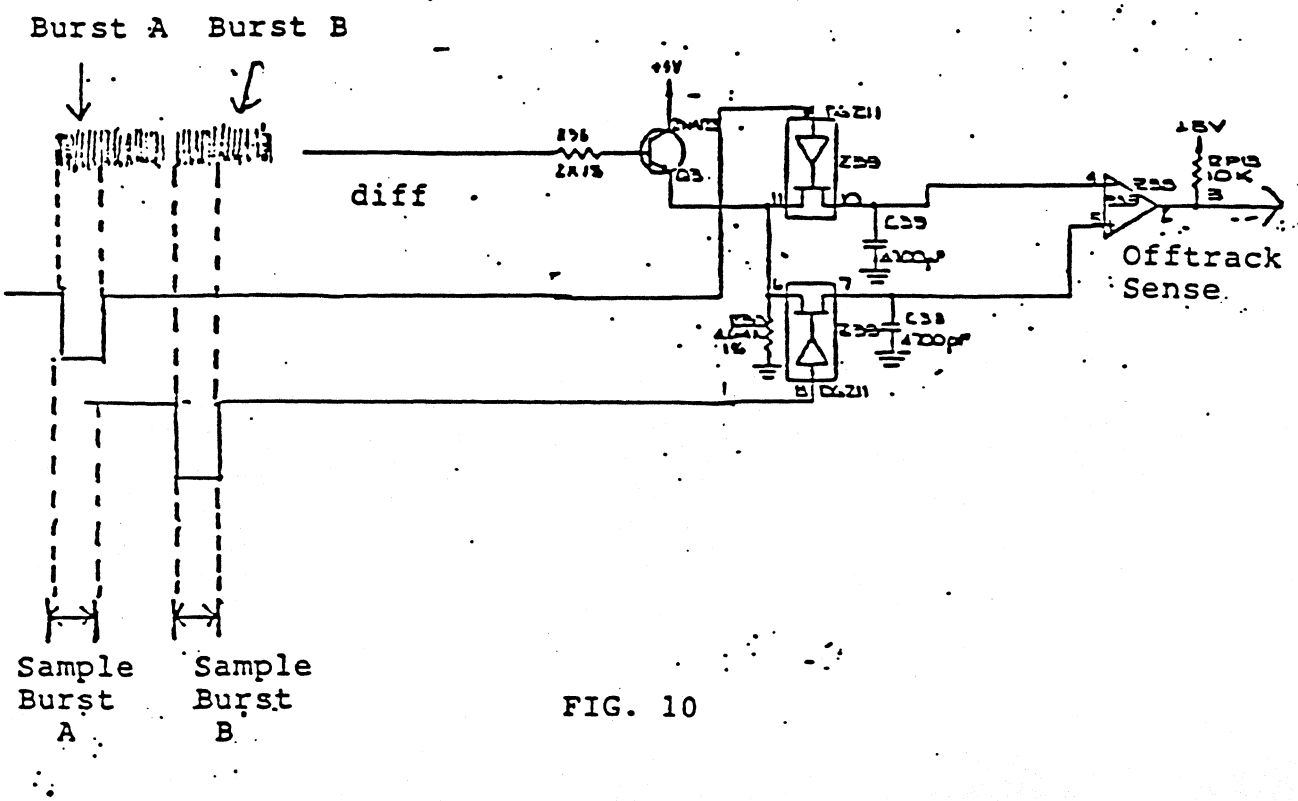



FIG. 10

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV. A |

To discuss the Read Data circuit refer to Figure 11 .

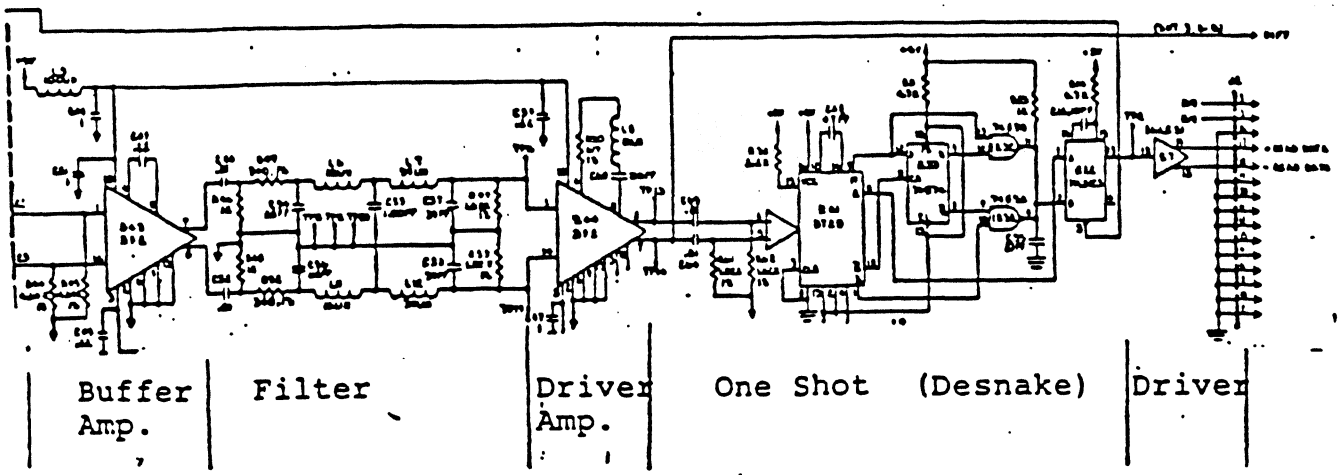



FIG. 11

The operation of this circuit is very straight forward. The disc head output is fed into F.E.T. array H1 (not shown) and is amplified by Z43, filtered and amplified further by Z44. The amplified signal is then fed into a one shot Z41 and further conditioned by Z33 and Z32. This section is sometimes referred to as a "De Snake circuit". For more information about why the De Snake circuit is used. Refer to Drive Debug Procedure (Dwg.600005 Page 3).

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV A |

The next section we will examine is the write data circuity. Before the A.M.T. can write any data to the drive, it must:
(1) Select the desired head.
(2) Pull the Write Gate line low.
(3) Ensure the Write Protect line is set high.

Although there is no specific sequence that must be followed, the A.M.T. must meet the above conditions prior to a Write Data operation. Refer to Fig. 12

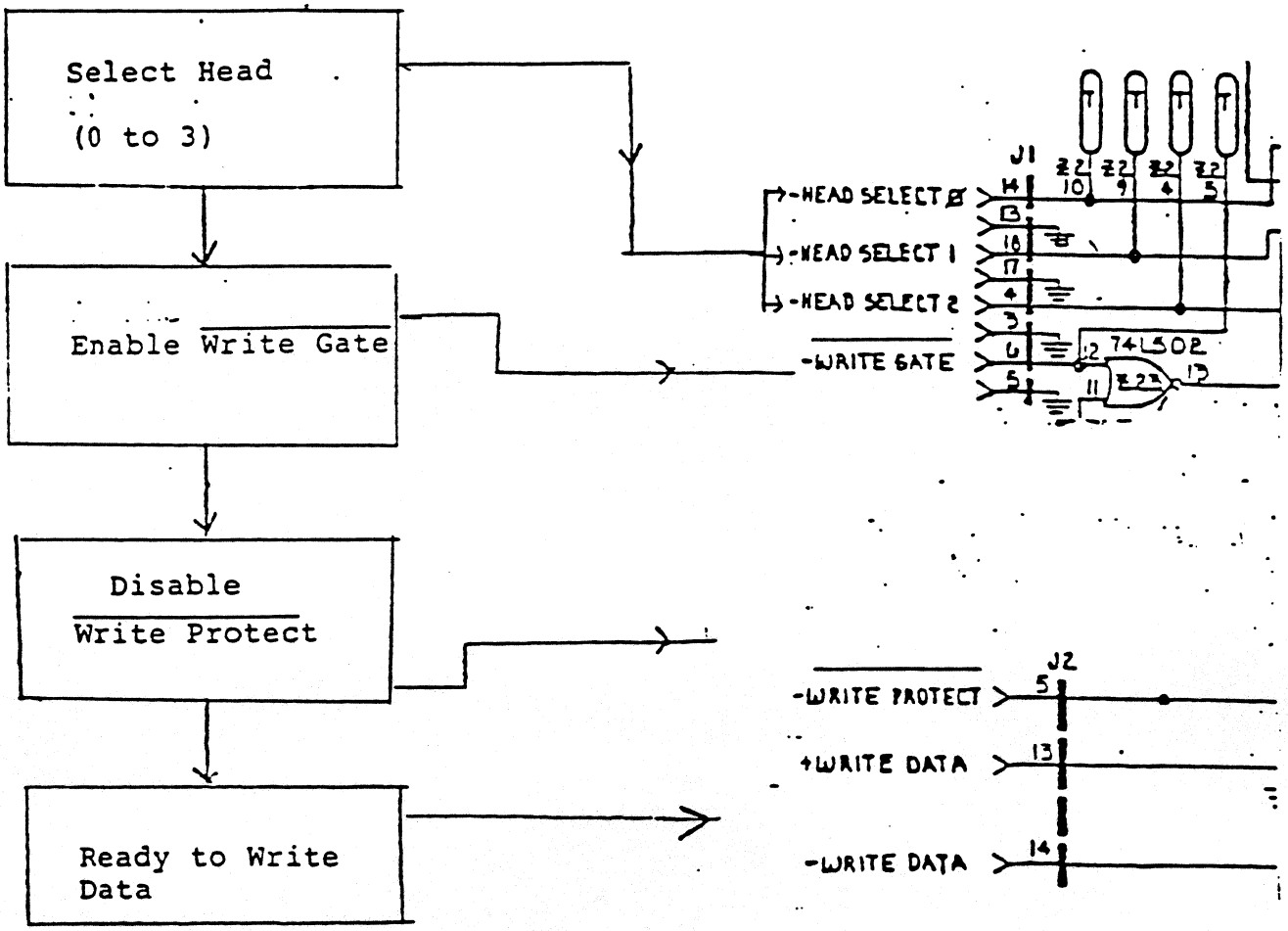



FIG. 12

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV. A |

The A.M.T. does not have exclusive control over the write enable circuitry. The CM6000 main board may also disable the write circuit completely, or partially.

Lets clarify what is meant by partially disabling the write circuit. As you know, the servo burst is written on the first two sectors of surface zero and surface one. We need a way to protect the servo burst from being "Overwritten" with data.

The Usermask signal provides a means by which servo information is not overwritten. This signal is active for the first 128 uS following the spindle index. Refer to Fig. 13

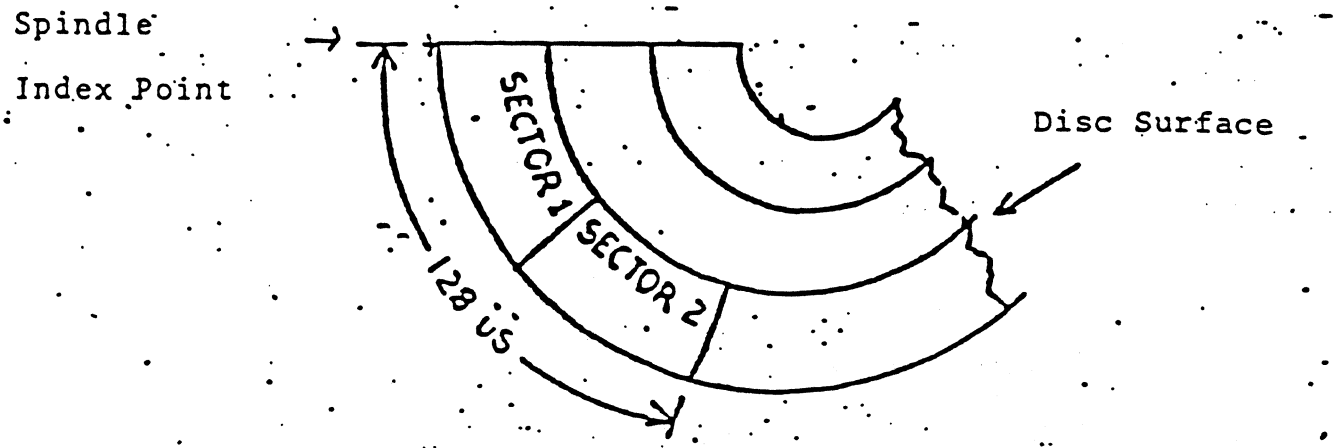



FIG. 13

In order to understand how the Usermask signal from being overwritten, refer to Fig. 14. Notice that Wrt Dsbl, Usrmsk, and Write Protect are all wire ORed to H3 pin 4. When H3 pin 4 is pulled low, the write data amplifier (H3) is disabled and no data may be written.

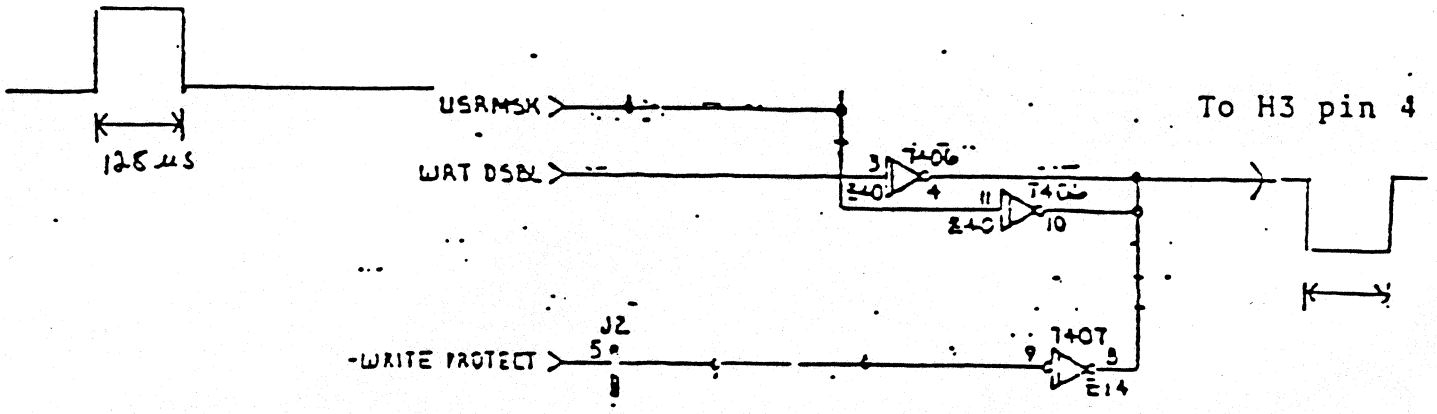



FIG. 14

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 300007 | REV |

Besides protecting the servo burst from being overwritten, the usermask signal is also used to select head 0 or head 1 for reading the servo burst. We mentioned earlier that the servo burst is written only on surface 0 and surface 1. Therefore, no matter what head is currently selected during a read or write operation, we must have a way to automatically select head 0 or 1 during the usermask time period, in order to read the servo burst.

During the usermask time period, the Quad Xing line controls whether head 0 or head 1 is selected for reading the servo burst.
On all odd numbered tracks, the servo burst is written on surface 1, and on all even tracks the burst is written on surface 0.
This is done to prevent "Overcrowding" of adjacent servo bursts.

In Fig. 15 notice that when Usrmsk is active, head select 0,1, and 2 are disabled and Quad Xing controls the output state of Z37 pin 3. When Quad Xing is high (even track) Z37 pin 3 will be low, and head 0 will be selected by Z36 Read decoder chip.
Conversely, when Quad Xing is low (odd track) Z37 pin 3 will be high Z36 will select head 1 for reading the servo burst. Remember that the servo burst is "Read" by the sample and hold circuit mentioned earlier.

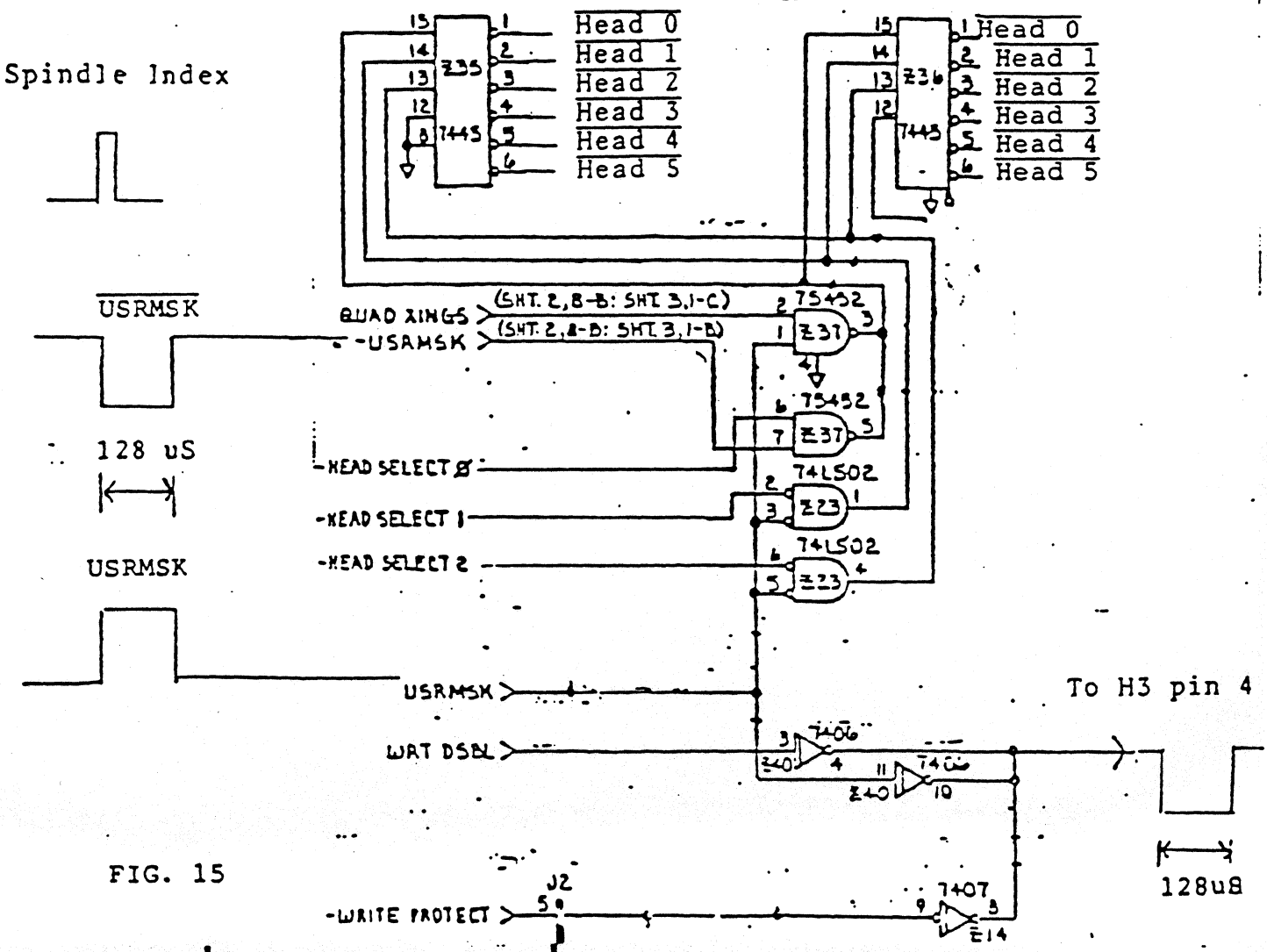



FIG. 15

| COMPUTER MEMORIES | | | | |
|---|---|---|---|---|
| DRAWN | SIZE A | FSCM NO. | DWG. NO. 600007 | REV |

We stated earlier that the main board itself may partially or completely disable the Write Data circuit. When the microprocessor senses a write fault condition via Write Fault Sense, it will disable the write circuit completely via Wrt Dsbl line. When this occurs, the only way to clear the write fault is to recycle the power supply connected to the main Bd.

A number of conditions may cause the write fault to be set. Probably the most common failure is an open read/write head. However a defective hybrid such as H1(F.E.T. array) or H3 (write data Amp.) or H2 (write fault sense detector) may also cause a write fault condition.

Attempting to write data with the Write Gate line high will result in a write fault condition. Although the A.M.T. controls this line, an open or intermittent cable on the A.M.T. may allow the Write Gate line to "Float". Since this input line has a pull up resitor connected to it, the write gate input will be at a high level if allowed to float.

It should also be mentioned that attempting to write data on a head that does not exist will also set the write fault output line. For example, if an attempt is made to write data on head five of a Snow White drive, a write fault condition will be present simply because the Snow White drive only has four heads!

As you can see, many different conditions may cause a "Write Fault" failure, and care should be exercised when attempting to isolate this type of problem.