commodore semiconductor group

# NMOS
# CMOS
# LCD

1981 Component Data Catalog

commodore semiconductor group
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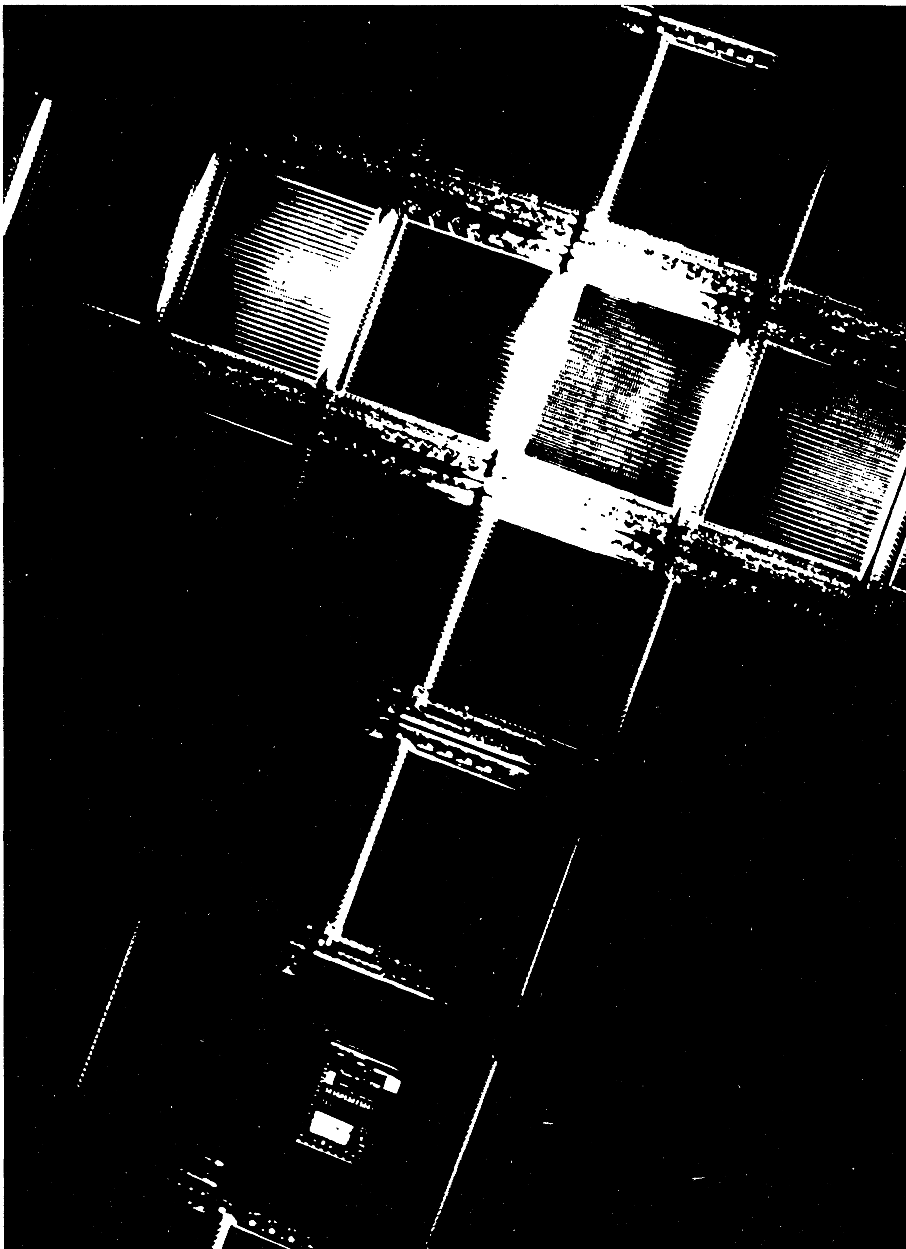


# NUMERICAL AND FUNCTIONAL INDEX

## NUMERICAL INDEX



## FUNCTIONAL INDEX

### Microprocessors



### Peripheral Devices

**Random Access Memories**



**Read-Only Memories**

# PRODUCT CROSS REFERENCE GUIDE

## STATIC RAM

| PART NUMBER | REPLACE WITH |
|---|---|
| **AMD** | **MOS Technology** |
| AM9114BPC | MPS2114-45 |
| AM9114BDC | MCS2114-45 |
| AM91L14BPC | MPS2114L-45 |
| AM91L14BDC | MCS2114L-45 |
| AM9114CPC | MPS2114-30 |
| AM9114CDC | MCS2114-30 |
| AM91L14CPC | MPS2114L-30 |
| AM91L14CDC | MCS2114L-30 |
| AM9114EPC | MPS2114-20 |
| AM9114EDC | MCS2114-20 |
| **AMI** | **MOS Technology** |
| S2114-3 | MPS2114-30 |
| S2114L-3 | MPS2114L-30 |
| S2114-2 | MPS2114-20 |
| S2114L-2 | MPS2114L-20 |
| **EMM** | **MOS Technology** |
| 2114UCB | MPS2114-45 |
| 2114UCA | MCS2114-45 |
| L2114UCB | MPS2114L-45 |
| L2114UCA | MCS2114L-45 |
| 2114-3CB | MPS2114-30 |
| 2114-3CA | MCS2114-30 |
| L2114-3CB | MPS2114L-30 |
| L2114-3CA | MCS2114L-30 |
| 2114-2CB | MPS2114-20 |
| 2114-2CA | MCS2114-20 |
| L2114-2CB | MPS2114L-20 |
| L2114-2CA | MCS2114L-20 |
| **Fujitsu** | **MOS Technology** |
| MB8114N | MPS2114-30 |
| MB8114NL | MPS2114L-30 |
| MB8114E | MPS2114-20 |
| MB8114EL | MPS2114L-20 |
| **Hitachi** | **MOS Technology** |
| HM472114-4 | MCS2114L-45 |
| **Intel** | **MOS Technology** |
| P2114 | MPS2114-45 |
| C2114 | MCS2114-45 |
| P2114L | MPS2114L-45 |
| C2114L | MCS2114L-45 |
| P2114-3 | MPS2114-30 |
| C2114-3 | MCS2114-30 |
| P2114L-3 | MPS2114L-30 |
| C2114L-3 | MCS2114L-30 |
| P2114-2 | MPS2114-20 |
| C2114-2 | MCS2114-20 |
| P2114L-2 | MPS2114L-20 |
| C2114L-2 | MCS2114L-20 |

| PART NUMBER | REPLACE WITH |
|---|---|
| **Intersil** | **MOS Technology** |
| P2114 | MPS2114-45 |
| P2114L | MPS2114L-45 |
| P21143 | MPS2114-30 |
| P2114L3 | MPS2114L-30 |
| P21142 | MPS2114-20 |
| P2114L2 | MPS2114L-20 |
| **Motorola** | **MOS Technology** |
| MCM2114P-45 | MPS2114-45 |
| MCM2114C-45 | MCS2114-45 |
| MCM21L14P-45 | MPS2114L-45 |
| MCM21L14C-45 | MCS2114-45 |
| MCM2114P-30 | MPS2114-30 |
| MCM2114C-30 | MCS2114-30 |
| MCM21L14P-30 | MPS2114L-30 |
| MCM21L14C-30 | MCS2114L-30 |
| MCM2114P-20 | MPS2114-20 |
| MCM2114C-20 | MCS2114-20 |
| MCM21L14P-20 | MPS2114L-20 |
| MCM21L14C-20 | MCS2114L-20 |
| **T.I.** | **MOS Technology** |
| TMS4045-45NL | MPS2114-45 |
| TMS4045-45JL | MCS2114-45 |
| TMS40L45-45NL | MPS2114L-45 |
| TMS40L45-45JL | MCS2114L-45 |
| TMS4045-30NL | MPS2114-30 |
| TMS4045-30JL | MCS2114-30 |
| TMS40L45-30NL | MPS2114L-30 |
| TMS40L45-30JL | MCS2114L-30 |
| TMS4045-20NL | MPS2114-20 |
| TMS4045-20JL | MCS2114-20 |

## ROM

| PART NUMBER | REPLACE WITH |
|---|---|
| **AMD** | **MOS Technology** |
| AM9217BPC | MPS2316 |
| AM9217BDC | MCS2316 |
| AM9232BPC | MPS2332 |
| AM9232BDC | MCS2332 |
| **AMI** | **MOS Technology** |
| S68316A | MPS2316 |
| S68332 | MPS2332 |
| **EA** | **MOS Technology** |
| EA2316B | MPS2316 |
| EA2332 | MPS2332 |
| **G.I.** | **MOS Technology** |
| RO-3-9316B | MPS2316 |
| RO-3-9332B | MPS2332 |
| **Intel** | **MOS Technology** |
| P2316B | MPS2316 |
| C2316B | MCS2316 |

| PART NUMBER | REPLACE WITH |
|---|---|
| **Intel** | **MOS Technology** |
| P2332 | MPS2332 |
| C2332 | MCS2332 |
| **Motorola** | **MOS Technology** |
| MCM68316B | MPS2316 |
| MCM68332 | MPS2332 |
| **National** | **MOS Technology** |
| MM2316B | MPS2316 |
| MM52132 | MPS2332 |
| MM52164 | MPS2364 |
| **NEC** | **MOS Technology** |
| UPD2316B | MPS2316 |
| UPD2332 | MPS2332 |
| UPD2364 | MPS2364 |
| **Signetics** | **MOS Technology** |
| 2632N | MPS2332 |
| 2664N | MPS2364 |
| **T.I.** | **MOS Technology** |
| TMS4732NL | MPS2332 |
| TMS4732JL | MCS2332 |
| TMS4764NL | MPS2364 |
| TMS4764JL | MCS2364 |
| **Mostek** | **MOS Technology** |
| MK31000N-3 | MCS2316 |
| MK31000P-3 | MPS2316 |
| MK36000P-5 | MPS2364 |
| MK36000N-5 | MCS2364 |

## MICROPROCESSORS

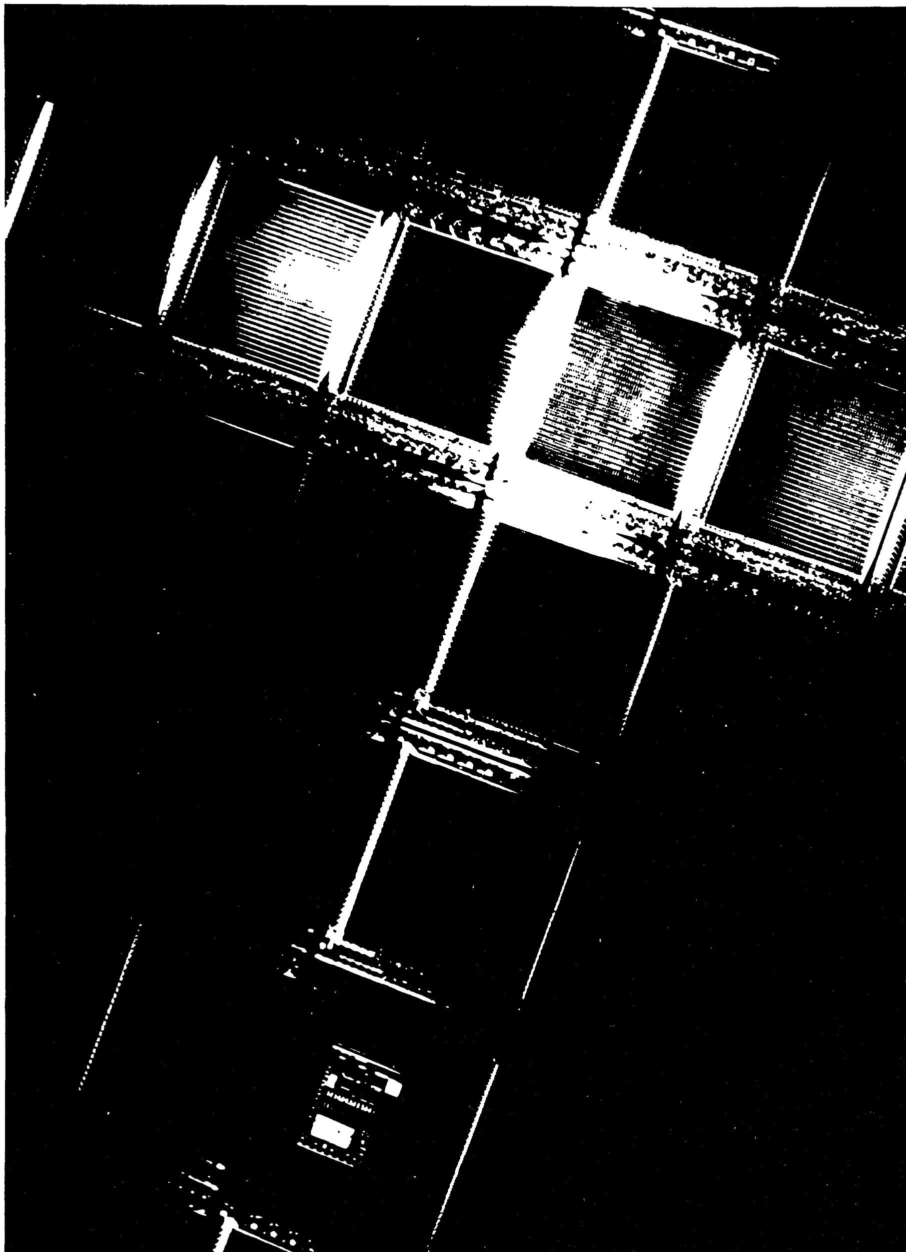
| PART NUMBER | REPLACE WITH |
|---|---|
| **Synertek** | **MOS Technology** |
| SYP = Plastic | MPS = Plastic |
| SYC = Ceramic | MCS = Ceramic |
| SYP/C6502 | MPS/CS6502 |
| SYP/C6503 | MPS/CS6503 |
| SYP/C6504 | MPS/CS6504 |
| SYC/C6505 | MPS/CS6505 |
| SYP/C6506 | MPS/CS6506 |
| SYP/C6507 | MPS/CS6507 |
| SYP/C6512 | MPS/CS6512 |
| SYP/C6513 | MPS/CS6513 |
| SYP/C6514 | MPS/CS6514 |
| SYP/C6515 | MPS/CS6515 |
| A = 2MHz | A = 2MHz |
| B = 3MHz | B = 3MHz |
| SYP/C6502A | MPS/CS6502A |
| SYP/C6502B | MPS/CS6502B |
| SYP/C6503A | MPS/CS6503A |
| SYP/C6503B | MPS/CS6503B |
| SYP/C6504A | MPS/CS6504A |

| MICROPROCESSORS (CONT.) | |
|---|---|
| **PART NUMBER** | **REPLACE WITH** |
| **Synertek** | **MOS Technology** |
| SYP/C6504B | MPS/CS6504B |
| SYP/C6505A | MPS/CS6505A |
| SYP/C6505B | MPS/CS6505B |
| SYP/C6506A | MPS/CS6506A |
| SYP/C6506B | MPS/CS6506B |
| SYP/C6507A | MPS/CS6507A |
| SYP/C6507B | MPS/CS6507B |
| SYP/C6512A | MPS/CS6512A |
| SYP/C6512B | MPS/CS6512B |
| SYP/C6513A | MPS/CS6513A |
| SYP/C6513B | MPS/CS6513B |
| SYP/C6514A | MPS/CS6514A |
| SYP/C6514B | MPS/CS6514B |
| SYP/C6515A | MPS/CS6515A |
| SYP/C6515B | MPS/CS6515B |
| SYP6520 | MPS6520 |
| SYP6520A | MPS6520A |
| SYC6520 | MCS6520 |
| SYC6520A | MCS6520A |
| SYP6522 | MPS6522 |
| SYP6522A | MPS6522A |
| SYC6522 | MCS6522 |
| SYC6522A | MCS6522A |
| SYP6530 | MPS6530 |
| SYC6530 | MCS6530 |
| SYP6532 | MPS6532 |
| SYP6532A | MPS6532A |
| SYC6532 | MCS6532 |
| SYC6532A | MCS6532A |

| PART NUMBER | REPLACE WITH |
|---|---|
| **Rockwell** | **MOS Technology** |
| R6502P | MPS6502 |
| R6502AP | MPS6502A |
| R6502C | MCS6502 |
| R6502AC | MCS6502A |
| R6503P | MPS6503 |
| R6503AP | MPS6503A |
| R6503AC | MCS6503A |
| R6504P | MPS6504 |
| R6504AP | MPS6504A |
| R6504C | MCS6504 |
| R6504AC | MCS6504A |
| R6505P | MPS6505 |
| R6505AP | MPS6505A |
| R6505C | MCS6505 |
| R6505AC | MCS6505A |
| R6506P | MPS6506 |
| R6506AP | MPS6506A |
| R6506C | MCS6506 |
| R6506AC | MCS6506A |
| R6507P | MPS6507 |
| R6507AP | MPS6507A |
| R6507C | MCS6507 |
| R6507AC | MCS6507A |
| R6512P | MPS6512 |
| R6512AP | MPS6512A |
| R6512C | MCS6512 |
| R6512AC | MCS6512A |
| R6513P | MPS6513 |
| R6513AP | MPS6513A |
| R6513C | MCS6513 |
| R6513AC | MCS6513A |

| PART NUMBER | REPLACE WITH |
|---|---|
| **Rockwell** | **MOS Technology** |
| R6514P | MPS6514 |
| R6514AP | MPS6514A |
| R6514C | MCS6514 |
| R6514AC | MCS6514A |
| R6515P | MPS6515 |
| R6515AP | MPS6515A |
| R6515C | MCS6515 |
| R6515AC | MCS6515A |
| R6520P | MPS6520 |
| R6520AP | MPS6520A |
| R6520C | MCS6520 |
| R6520AC | MCS6520A |
| R6522P | MPS6522 |
| R6522AP | MPS6522A |
| R6522C | MCS6522 |
| R6522AC | MCS6522A |
| R6530P | MPS6530 |
| R6530C | MCS6530 |
| R6532P | MPS6532 |
| R6532AP | MPS6532A |
| R6532C | MCS6532 |
| R6532AC | MCS6532A |
| R6500/IP | MPS6500/I |
| R6500/IAP | MPS6500/IA |
| R6500/IC | MCS6500/I |
| R6500/IAC | MCS6500/IA |

# Section 2
# NMOS



# commodore semiconductor group

## NMOS

# 6500 Microprocessors

- Single +5V Supply
- N-Channel, Silicon-Gate, Depletion-Load Technology
- 8-Bit Parallel Processing
- 56 Instructions
- Decimal and Binary Arithmetic
- 13 Addressing Modes
- Programmable Stack Pointer and Variable-Length Stack
- Usable With Any Type or Speed Memory
- 1 or 2 MHz Operation
- Pipelined Architecture

### DESCRIPTION

The 6500 Series microprocessors represent the first totally software-compatible microprocessor family. This family of products includes a range of software-compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the 6500 group are software-compatible within the group and are bus compatible with the M6800 product offering.

The family includes five microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high-performance, low-cost applications where single-phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multi-processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz and 2 MHz ("A" suffix on product numbers) maximum operating frequencies.

### MEMBERS OF THE FAMILY

| Part Numbers | | Clocks | Pins | $\overline{IRQ}$ | $\overline{NMI}$ | RDY | Addressing |
|---|---|---|---|---|---|---|---|
| Plastic | Ceramic | | | | | | |
| MPS6502 | MCS6502 | On-Chip | 40 | √ | √ | √ | 16 (64 K) |
| MPS6503 | MCS6503 | " | 28 | √ | √ | | 12 (4 K) |
| MPS6504 | MCS6504 | " | 28 | √ | | | 13 (8 K) |
| MPS6505 | MCS6505 | " | 28 | √ | | √ | 12 (4 K) |
| MPS6506 | MCS6506 | " | 28 | √ | | | 12 (4 K) |
| MPS6507 | MCS6507 | " | 28 | | | √ | 13 (8 K) |
| MPS6512 | MCS6512 | External | 40 | √ | √ | √ | 16 (64 K) |
| MPS6513 | MCS6513 | " | 28 | √ | √ | | 12 (4 K) |
| MPS6514 | MCS6514 | " | 28 | √ | | | 13 (8 K) |
| MPS6515 | MCS6515 | " | 28 | √ | | √ | 12 (4 K) |

### PIN FUNCTIONS

#### Clocks ($\Phi 1$ and $\Phi 2$)

The 651X requires a two-phase, non-overlapping clock that runs at the $V_{CC}$ voltage level.

The 650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Details of this feature are discussed in the 6502 portion of this data sheet.

#### Address Bus (A0-A15)

(See sections on each processor for respective address lines on those devices.)

These outputs are TTL-compatible, capable of driving one standard TTL load and 130pF.

#### Data Bus (D0-D7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers capable of driving one standard TTL load and 130pF.

#### Data Bus Enable (DBE)

This TTL-compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation, DBE would be driven by the phase two ($\Phi 2$) clock, thus allowing data input from microprocessor only during $\Phi 2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

**Ready (RDY)**

This input signal allows the user to single-cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (Φ1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (Φ2) in which the Ready signal is low. This feature allows microprocessor interfacing with low-speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

**Interrupt Request ($\overline{\text{IRQ}}$)**

This TTL-compatible signal requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

**Non-Maskable Interrupt ($\overline{\text{NMI}}$)**

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{\text{NMI}}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{\text{IRQ}}$ will be performed, regardless of the state of the interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{\text{NMI}}$ also requires an external 3KΩ register to $V_{CC}$ for proper wire-OR operations.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupts lines that are sampled during Φ2 and will begin the appropriate interrupt routine on the Φ1 following the completion of the current instruction.

**Set Overflow Flag (S.O.)**

A NEGATIVE-going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of Φ1.

**SYNC**

This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during Φ1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Φ1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

**Reset**

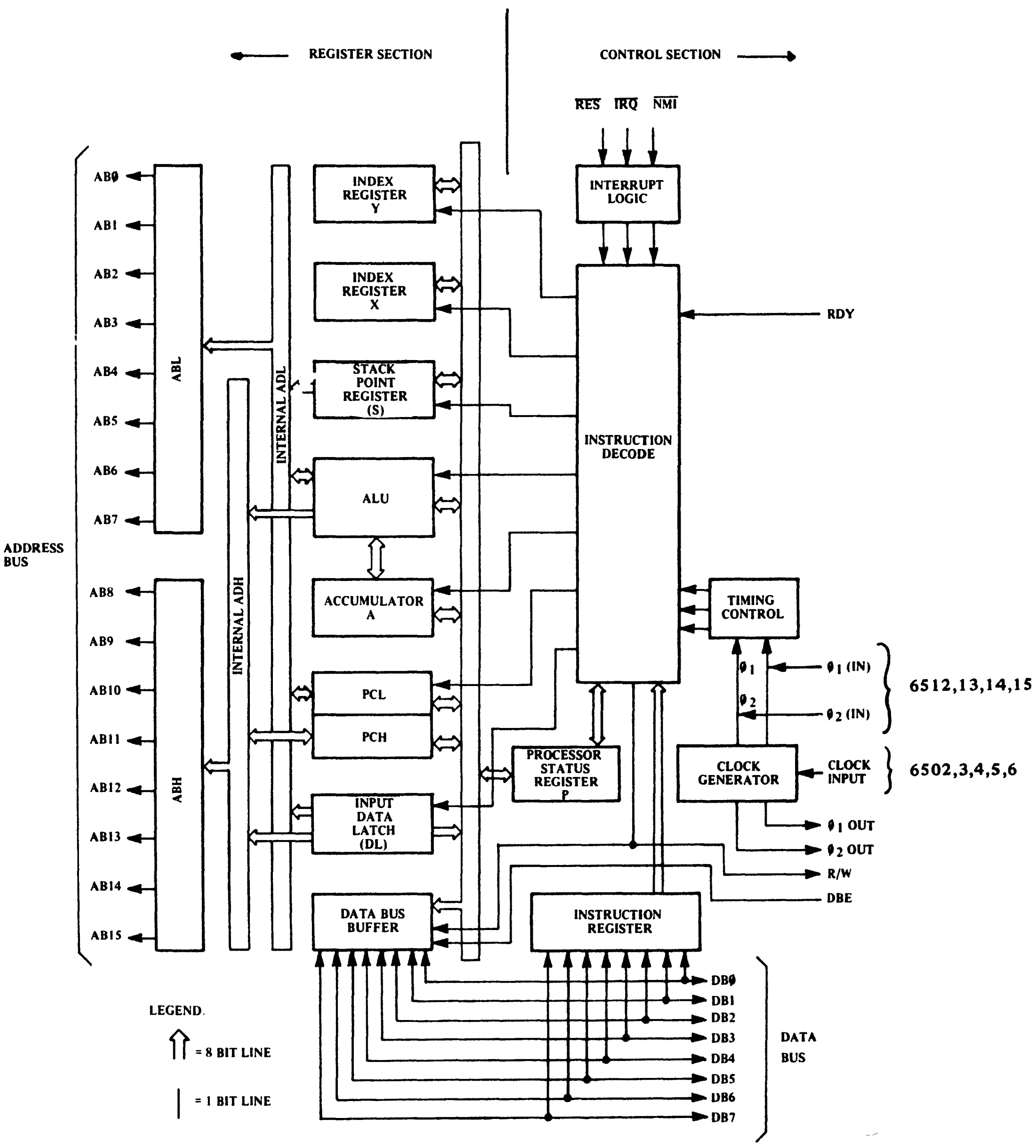
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from memory vector locations FFFC and FFFD. This is the start location for program control.

After $V_{CC}$ reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

## INTERNAL ARCHITECTURE




**NOTES**

1. Clock Generator is not included on 6512,13,14,15
2. Addressing Capability and control options vary with each of the 6500 Products.

**INSTRUCTION SET—OP CODES, Execution Time, Memory Requirements**

| Instructions | | Immediate | | | Absolute | | | Zero Page | | | Accum. | | | Implied | | | (IND, X) | | | (IND), Y | | | Z, Page, X | | | ABS, X | | | ABS, Y | | | Relative | | | Indirect | | | Z, Page, Y | | | Condition Codes | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mnemonic | Operation | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | N | Z | C | I | D | V |
| A D C | A+M+C→A (4)(1) | 69 | 2 | 2 | 6D | 4 | 3 | 65 | 3 | 2 | | | | | | | 61 | 6 | 2 | 71 | 5 | 2 | 75 | 4 | 2 | 7D | 4 | 3 | 79 | 4 | 3 | | | | | | | | | | ✓ | ✓ | ✓ | - | - | ✓ |
| A N D | A∧M→A (1) | 29 | 2 | 2 | 2D | 4 | 3 | 25 | 3 | 2 | | | | | | | 21 | 6 | 2 | 31 | 5 | 2 | 35 | 4 | 2 | 3D | 4 | 3 | 39 | 4 | 3 | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| A S L | C←7 0←0 | | | | 0E | 6 | 3 | 06 | 5 | 2 | 0A | 2 | 1 | | | | | | | | | | 16 | 6 | 2 | 1E | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| B C C | BRANCH ON C=0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 90 | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B C S | BRANCH ON C=1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B0 | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B E Q | BRANCH ON Z=1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | F0 | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B I T | A∧M | | | | 2C | 4 | 3 | 24 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | $M_7$ | ✓ | - | - | - | $M_6$ |
| B M I | BRANCH ON N=1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 30 | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B N E | BRANCH ON Z=0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D0 | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B P L | BRANCH ON N=0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 10 | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B R K | (See Fig. 1) | | | | | | | | | | | | | 00 | 7 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| B V C | BRANCH ON V=0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 50 | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B V S | BRANCH ON V=1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 70 | 2 | 2 | | | | | | | - | - | - | - | - | - |
| C L C | 0→C | | | | | | | | | | | | | 18 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | 0 | - | - | - |
| C L D | 0→D | | | | | | | | | | | | | D8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | 0 | - |
| C L I | 0→1 | | | | | | | | | | | | | 58 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | 0 | - | - |
| C L V | 0→V | | | | | | | | | | | | | B8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | 0 |
| C M P | A-M (1) | C9 | 2 | 2 | CD | 4 | 3 | C5 | 3 | 2 | | | | | | | C1 | 6 | 2 | D1 | 5 | 2 | D5 | 4 | 2 | DD | 4 | 3 | D9 | 4 | 3 | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| C P X | X-M | E0 | 2 | 2 | EC | 4 | 3 | E4 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| C P Y | Y-M | C0 | 2 | 2 | CC | 4 | 3 | C4 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| D E C | M-1→M | | | | CE | 6 | 3 | C6 | 5 | 2 | | | | | | | | | | | | | D6 | 6 | 2 | DE | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| D E X | X-1→X | | | | | | | | | | | | | CA | | | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| D E Y | Y-1→Y | | | | | | | | | | | | | 88 | | | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| E O R | A⊻M→A (1) | 49 | 2 | 2 | 4D | 4 | 3 | 45 | 3 | 2 | | | | | | | 41 | 6 | 2 | 51 | 5 | 2 | 55 | 4 | 2 | 5D | 4 | 3 | 59 | 4 | 3 | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| I N C | M+1→M | | | | EE | 6 | 3 | E6 | 5 | 2 | | | | | | | | | | | | | F6 | 6 | 2 | FE | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| I N X | X+1→X | | | | | | | | | | | | | E8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| I N Y | Y+1→Y | | | | | | | | | | | | | C8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| J M P | JUMP TO NEW LOC | | | | 4C | 3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | 6C | 5 | 3 | | | | - | - | - | - | - | - |
| J S R | (See Fig 2) JUMP SUB | | | | 20 | 6 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| L D A | M→A (1) | A9 | 2 | 2 | AD | 4 | 3 | A5 | 3 | 2 | | | | | | | A1 | 6 | 2 | B1 | 5 | 2 | B5 | 4 | 2 | BD | 4 | 3 | B9 | 4 | 3 | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| L D X | M→X (1) | A2 | 2 | 2 | AE | 4 | 3 | A6 | 3 | 2 | | | | | | | | | | | | | | | | | | | BE | 4 | 3 | | | | | | | B6 | 4 | 2 | ✓ | ✓ | - | - | - | - |
| L D Y | M→Y (1) | A0 | 2 | 2 | AC | 4 | 3 | A4 | 3 | 2 | | | | | | | | | | | | | B4 | 4 | 2 | BC | 4 | 3 | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| L S R | 0→7 0→C | | | | 4E | 6 | 3 | 46 | 5 | 2 | 4A | 2 | 1 | | | | | | | | | | 56 | 6 | 2 | 5E | 7 | 3 | | | | | | | | | | | | | 0 | ✓ | ✓ | - | - | - |
| N O P | NO OPERATION | | | | | | | | | | | | | EA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| O R A | A∨M→A | 09 | 2 | 2 | 0D | 4 | 3 | 05 | 3 | 2 | | | | | | | 01 | 6 | 2 | 11 | 5 | 2 | 15 | 4 | 2 | 1D | 4 | 3 | 19 | 4 | 3 | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| P H A | A→$M_s$ S-1→S | | | | | | | | | | | | | 48 | 3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| P H P | P→$M_s$ S-1→S | | | | | | | | | | | | | 08 | 3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| P L A | S+1→S $M_s$→A | | | | | | | | | | | | | 68 | 4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| P L P | S+1→S $M_s$→P | | | | | | | | | | | | | 28 | 4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | (RESTORED) | | | | | |
| R O L | ←7 0←C← | | | | 2E | 6 | 3 | 26 | 5 | 2 | 2A | 2 | 1 | | | | | | | | | | 36 | 6 | 2 | 3E | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| R O R | →C 7 0→ | | | | 6E | 6 | 3 | 66 | 5 | 2 | 6A | 2 | 1 | | | | | | | | | | 76 | 6 | 2 | 7E | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| R T I | (See Fig. 1) RTRN INT | | | | | | | | | | | | | 40 | 6 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | (RESTORED) | | | | | |
| R T S | (See Fig. 2) RTRN SUB | | | | | | | | | | | | | 60 | 6 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| S B C | A-M-C→A (1) | E9 | 2 | 2 | ED | 4 | 3 | E5 | 3 | 2 | | | | | | | E1 | 6 | 2 | F1 | 5 | 2 | F5 | 4 | 2 | FD | 4 | 3 | F9 | 4 | 3 | | | | | | | | | | ✓ | ✓ | (3) | - | - | ✓ |
| S E C | 1→C | | | | | | | | | | | | | 38 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | 1 | - | - | - |
| S E D | 1→D | | | | | | | | | | | | | F8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | 1 | - |
| S E I | 1→I | | | | | | | | | | | | | 78 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | 1 | - | - |
| S T A | A→M | | | | 8D | 4 | 3 | 85 | 3 | 2 | | | | | | | 81 | 6 | 2 | 91 | 6 | 2 | 95 | 4 | 2 | 9D | 5 | 3 | 99 | 5 | 3 | | | | | | | | | | - | - | - | - | - | - |
| S T X | X→M | | | | 8E | 4 | 3 | 86 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | 96 | 4 | 2 | - | - | - | - | - | - |
| S T Y | Y→M | | | | 8C | 4 | 3 | 84 | 3 | 2 | | | | | | | | | | | | | 94 | 4 | 2 | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| T A X | A→X | | | | | | | | | | | | | AA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| T A Y | A→Y | | | | | | | | | | | | | A8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| T S X | S→X | | | | | | | | | | | | | 8A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| T X A | X→A | | | | | | | | | | | | | 8A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| T X S | X→S | | | | | | | | | | | | | 9A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| T Y A | Y→A | | | | | | | | | | | | | 98 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |

**NOTES**

1. Add 1 to "N" if Page Boundary is Crossed
2. Add 1 to "N" if Branch Occurs to Same Page
   Add 2 to "N" if Branch Occurs to Different Page
3. Carry Not = Borrow
4. If in Decimal Mode Z Flag is Invalid
   Accumulator Must be Checked for Zero Result

X Index X

Y Index Y

A Accumulator

M Memory Per Effective Address

$M_S$ Memory Per Stack Pointer

+ Add

− Subtract

∧ AND

∨ OR

⊻ Exclusive OR

✓ Modified

- Not Modified

$M_7$ Memory Bit 7

$M_6$ Memory Bit 6

N No Cycles

# No Bytes

## INSTRUCTION SET—ALPHABETICAL SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Pointer
TYA Transfer Index Y to Accumulator

## ADDRESSING MODES

**Accumulator Addressing.** This form of addressing is represented with a one-byte instruction, implying an operation on the accumulator.

**Immediate Addressing.** In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

**Absolute Addressing.** In absolute addressing, the second byte of the instruction specifies the eight low-order bits of the effective address while the third byte specifies the eight high-order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

**Zero Page Addressing.** The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high-address byte. Careful use of the zero page can result in significant increase in code efficiency.

**Indexed Zero Page Addressing.** (X, Y indexing) — This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

**Indexed Absolute Addressing.** (X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

**Implied Addressing.** In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

**Relative Addressing.** Relative addressing is used only with branch instructions and establishes a destination for the conditional branch. The second byte of the instruction becomes the operand which is an offset added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

**Indexed Indirect Addressing.** In indexed indirect addressing (referred to as Indirect, X), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low-order eight bits of the effective address. The next memory location in page zero contains the high-order eight bits of the effective address. Both memory locations specifying the high and low-order bytes of the effective address must be in page zero.

**Indirect Indexed Addressing.** In indirect indexed addressing (referred to as Indirect, Y), the second byte of the instruction points to a memory location in page zero. The contents on this memory location is added to the contents of the Y index register, the result being the low-order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high-order eight bits of the effective address.

**Absolute Indirect.** The second byte of the instruction contains the low-order eight bits of a memory location. The high-order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low-order byte of the effective address. The next memory location contains the high-order byte of the effective address which is loaded into the 16-bit program counter.

**ABSOLUTE MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | Vdc |
| Input Voltage | $V_{IN}$ | −0.3 to +7.0 | Vdc |
| Operating Temperature | $T_A$ | 0 to +70 | °C |
| Storage Temperature | $T_{STG}$ | −55 to +150 | °C |

**CAUTION**

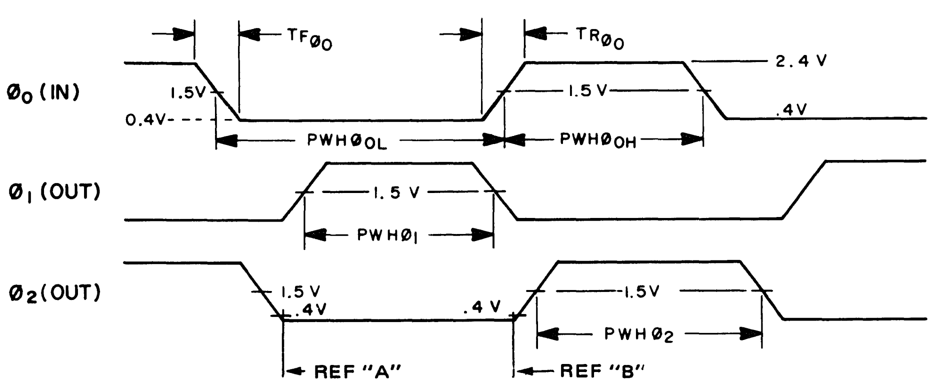
*This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.*

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0V ± 5%, $V_{SS}$ = 0, $T_A$ = 25°C)
$\emptyset_1$, $\emptyset_2$ applies to 6512, 13, 14, 15, $\emptyset_{o\,(in)}$ applies to MCS6502, 03, 04, 05 and 06

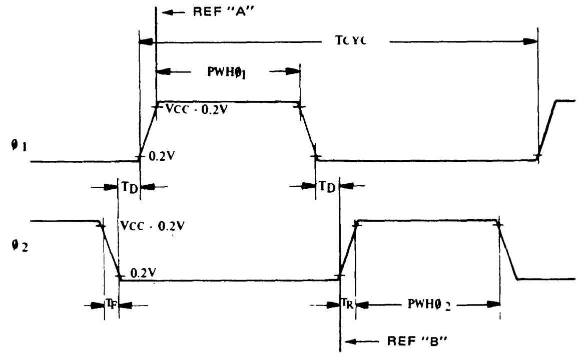
| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | $V_{SS}$ + 2.4<br>$V_{CC}$ − 0.2 | | $V_{CC}$<br>$V_{CC}$ + 0.25 | Vdc | Logic, $\emptyset_{o\,(in)}$<br>$\emptyset_1$, $\emptyset_2$ |
| $V_{IL}$ | Input Low Voltage | $V_{SS}$ − 0.3<br>$V_{SS}$ − 0.3 | | $V_{SS}$ + 0.4<br>$V_{SS}$ + 0.2 | Vdc | Logic, $\emptyset_{o\,(in)}$<br>$\emptyset_1$, $\emptyset_2$ |
| $V_{IHT}$ | Input High Threshold Voltage | $V_{SS}$ + 2.0 | | | Vdc | $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O. |
| $V_{ILT}$ | Input Low Threshold Voltage | | | $V_{SS}$ + 0.8 | Vdc | $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O. |
| $I_{IN}$ | Input Leakage Current | | | <br>2.5<br>100<br>10.0 | <br>μA<br>μA<br>μA | ($V_{IN}$ = 0 to 5.25V, $V_{CC}$ = 0)<br>Logic (Excl. RDY, S.O.)<br>$\emptyset_1$, $\emptyset_2$<br>$\emptyset_{o\,(in)}$ |
| $I_{TSI}$ | Three-State (Off State) Input Current | | | 10 | μA | ($V_{IN}$ = 0.4 to 2.4V, $V_{CC}$ = 5.25V)<br>Data Lines |
| $V_{OH}$ | Output High Voltage | $V_{SS}$ + 2.4 | | | Vdc | ($I_{LOAD}$ = −100μAdc, $V_{CC}$ = 4.75V)<br>SYNC, Data, A0–A15, R/W |
| $V_{OL}$ | Output Low Voltage | | | $V_{SS}$ + 0.4 | Vdc | ($I_{LOAD}$ = 1.6mAdc, $V_{CC}$ = 4.75V)<br>SYNC, Data, A0–A15, R/W |
| $P_D$ | Power Dissipation | | .25 | .70 | W | |
| C<br>$C_{IN}$<br><br>$C_{OUT}$<br>$C\emptyset_{o\,(in)}$<br>$C\emptyset_1$<br>$C\emptyset_2$ | Capacitance | | <br><br><br><br><br>30<br>50 | <br>10<br>15<br>12<br>50<br>50<br>80 | pF | ($V_{IN}$ = 0, $T_A$ = 25°C, f = 1MHz)<br>Logic<br>Data<br>A0–A15, R/W, SYNC<br>$\emptyset_{0\,(in)}$<br>$\emptyset_1$<br>$\emptyset_2$ |

**NOTE**
$\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistors.

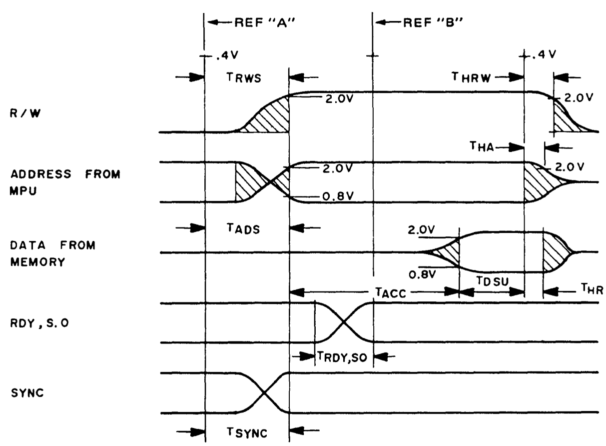
**CLOCK TIMING—6502, 03, 04, 05, 06**



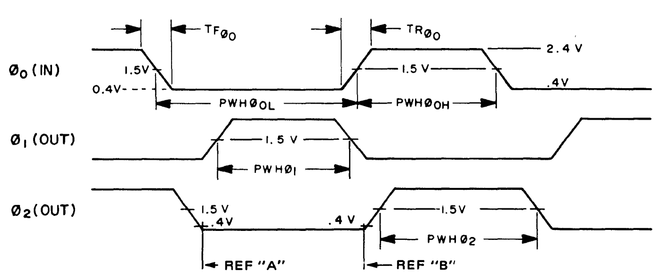
## CLOCK TIMING— 6512, 13, 14, 15




## TIMING FOR READING DATA FROM MEMORY OR PERIPHERALS




## TIMING FOR WRITING DATA TO MEMORY OR PERIPHERALS




**NOTE**
"REF." means Reference Points on clocks.

## 1 MHz TIMING

### CLOCK TIMING— 6512, 13, 14, 15

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CYC}$ | Cycle Time | 1000 | | | nsec |
| PWH $\phi 1$<br>PWH $\phi 2$ | Clock Pulse Width $\phi 1$<br>(Measured at $V_{CC}$ − 0.2 V) $\phi 2$ | 430<br>470 | | | nsec |
| $T_F$ | Fall Time (Measured from 0.2 V to $V_{CC}$ − 0.2 V) | | | 25 | nsec |
| $T_D$ | Delay Time Between Clocks (Measured at 0.2 V) | 0 | | | nsec |

### CLOCK TIMING—6502, 03, 04, 05, 06

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CYC}$ | Cycle Time | 1000 | | | ns |
| $PWH\phi_O$ | $\phi_{O\,(IN)}$ Pulse Width (measured at 1.5 V) | 460 | | 520 | ns |
| $TR\phi_O$, $TF\phi_O$ | $\phi_{O\,(IN)}$ Rise, Fall Time | | | 10 | ns |
| $T_D$ | Delay Time Between Clocks (measured at 1.5 V) | 5 | | | ns |
| $PWH\phi_1$ | $\phi_{1\,(OUT)}$ Pulse Width (measured at 1.5 V) | $PWH\phi_{oL}-20$ | | $PWH\phi_{oL}$ | ns |
| $PWH\phi_2$ | $\phi_{1\,(OUT)}$ Pulse Width (measured at 1.5 V) | $PWH\phi_{oH}-40$ | | $PWH\phi_{oH}-10$ | ns |
| $T_R$, $T_F$ | $\phi_{1\,(OUT)}$, $\phi_{2\,(OUT)}$ Rise, Fall Time<br>(measured .8 V to 2.0 V)<br>(Load = 30pF + 1 TTL) | | | 25 | ns |

### READ/WRITE TIMING

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{RWS}$ | Read/Write Setup Time From MCS6500 | | 100 | 300 | ns |
| $T_{ADS}$ | Address Setup Time From MCS6500 | | 100 | 300 | ns |
| $T_{ACC}$ | Memory Read Access Time | | | 575 | ns |
| $T_{DSU}$ | Data Stability Time Period | 100 | | | ns |
| $T_{HR}$ | Data Hold Time – Read | 10 | | | ns |
| $T_{HW}$ | Data Hold Time – Write | 30 | 60 | | ns |
| $T_{MDS}$ | Data Setup Time From MCS6500 | | 150 | 200 | ns |
| $T_{RDY}$ | RDY, S.O. Setup Time | 100 | | | ns |
| $T_{SYNC}$ | SYNC Setup Time From MCS6500 | | | 350 | ns |
| $T_{HA}$ | Address Hold Time | 30 | 60 | | ns |
| $T_{HRW}$ | R/W Hold Time | 30 | 60 | | ns |

## 2 MHz TIMING

### CLOCK TIMING— 6512, 13, 14, 15, 16

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CYC}$ | Cycle Time | 500 | | | nsec |
| PWH $\phi$1<br>PWH $\phi$2 | Clock Pulse Width $\phi$1<br>(Measured at $V_{CC}$ − 0.2 V) $\phi$2 | 215<br>235 | | | nsec |
| $T_F$ | Fall Time (Measured from 0.2 V to $V_{CC}$ − 0.2 V) | | | 12 | nsec |
| $T_D$ | Delay Time Between Clocks (Measured at 0.2 V) | 0 | | | nsec |

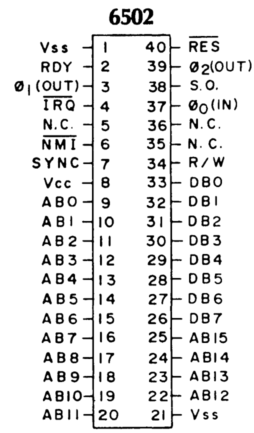
### CLOCK TIMING— 6502, 03, 04, 05, 06

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CYC}$ | Cycle Time | 500 | | | ns |
| $PWH\phi_o$ | $\phi_{o\,(IN)}$ Pulse Width (measured at 1.5 V) | 240 | | 260 | ns |
| $TR\phi_o$, $TF\phi_o$ | $\phi_{o\,(IN)}$ Rise, Fall Time | | | 10 | ns |
| $T_D$ | Delay Time Between Clocks (measured at 1.5 V) | 5 | | | ns |
| $PWH\phi_1$ | $\phi_{1\,(OUT)}$ Pulse Width (measured at 1.5 V) | $PWH\phi_{oL}-20$ | | $PWH\phi_{oL}$ | ns |
| $PWH\phi_2$ | $\phi_{2\,(OUT)}$ Pulse Width (measured at 1.5 V) | $PWH\phi_{oH}-40$ | | $PWH\phi_{oH}-10$ | ns |
| $T_R$, $T_F$ | $\phi_{1\,(OUT)}$, $\phi_{2\,(OUT)}$ Rise, Fall Time<br>(measured .8 V to 2.0 V)<br>(Load = 30pF + 1 TTL) | | | 25 | ns |

### READ/WRITE TIMING

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{RWS}$ | Read/Write Setup Time From 6500A | | 100 | 150 | ns |
| $T_{ADS}$ | Address Setup Time From 6500A | | 100 | 150 | ns |
| $T_{ACC}$ | Memory Read Access Time | | | 300 | ns |
| $T_{DSU}$ | Data Stability Time Period | 50 | | | ns |
| $T_{HR}$ | Data Hold Time – Read | 10 | | | ns |
| $T_{HW}$ | Data Hold Time – Write | 30 | 60 | | ns |
| $T_{MDS}$ | Data Setup Time From 6500A | | 75 | 100 | ns |
| $T_{RDY}$ | RDY, S.O. Setup Time | 50 | | | ns |
| $T_{SYNC}$ | SYNC Setup Time From 6500A | | | 175 | ns |
| $T_{HA}$ | Address Hold Time | 30 | 60 | | ns |
| $T_{HRW}$ | R/W Hold Time | 30 | 60 | | ns |

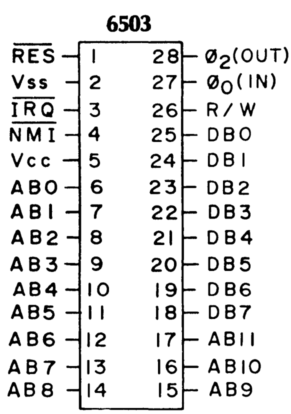
**(40 Pin Package)**




**FEATURES**

- 65K Addressable Bytes of Memory
- IRQ Interrupt
- NMI Interrupt
- On-the-chip Clock
  - ✓ TTL Level Single Phase Input
  - ✓ RC Time Base Input
  - ✓ Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used for single cycle execution)
- Two Phase Output Clock for Timing of Support Chips

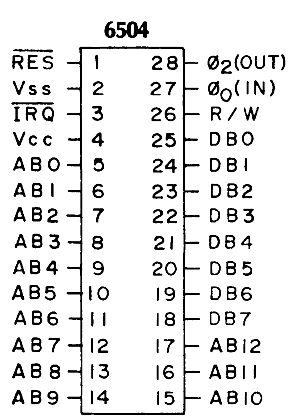
**(28 Pin Package)**




**FEATURES**

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bi-Directional Data Bus

**(28 Pin Package)**

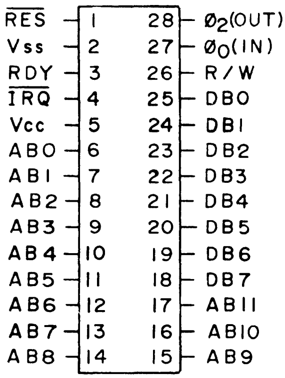



**FEATURES**

- 8K Addressable Bytes of Memory (AB00–AB12)
- On-the-chip Clock
- IRQ Interrupt
- 8 Bit Bi-Directional Data Bus

**(28 Pin Package)**

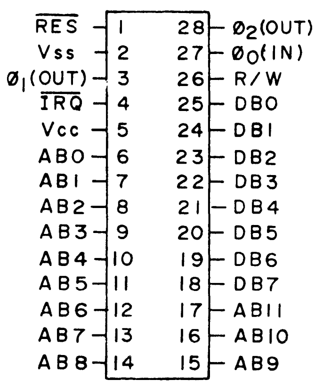
**6505**




**FEATURES**
- 4K Addressable Bytes of Memory (AB00–AB11)
- On-the-chip Clock
- $\overline{\text{IRQ}}$ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus

**(28 Pin Package)**

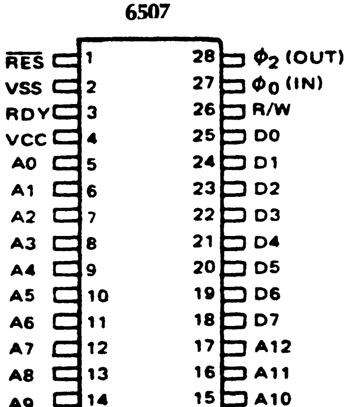
**6506**




**FEATURES**
- 4K Addressable Bytes of Memory (AB00–AB11)
- On-the-chip Clock
- $\overline{\text{IRQ}}$ Interrupt
- Two phases off
- 8 Bit Bi-Directional Data Bus

**(28 Pin Package)**

**6507**




**FEATURES**
- 8K Addressable Bytes of Memory (A0–A12)
- On-the-chip Clock
- RDY Signal
- 8 Bit Bi-Directional Data Bus

## (40 Pin Package)

**6512**

| | | | |
|---|---|---|---|
| Vss | 1 | 40 | $\overline{RES}$ |
| RDY | 2 | 39 | $\emptyset_2$(OUT) |
| $\emptyset_1$ | 3 | 38 | S.O. |
| $\overline{IRQ}$ | 4 | 37 | $\emptyset_2$ |
| Vss | 5 | 36 | DBE |
| $\overline{NMI}$ | 6 | 35 | N.C |
| SYNC | 7 | 34 | R/W |
| Vcc | 8 | 33 | DB0 |
| AB0 | 9 | 32 | DB1 |
| AB1 | 10 | 31 | DB2 |
| AB2 | 11 | 30 | DB3 |
| AB3 | 12 | 29 | DB4 |
| AB4 | 13 | 28 | DB5 |
| AB5 | 14 | 27 | DB6 |
| AB6 | 15 | 26 | DB7 |
| AB7 | 16 | 25 | AB15 |
| AB8 | 17 | 24 | AB14 |
| AB9 | 18 | 23 | AB13 |
| AB10 | 19 | 22 | AB12 |
| AB11 | 20 | 21 | Vss |

**FEATURES**

- 65K Addressable Bytes of Memory
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus
- SYNC Signal
- Two phase input
- Data Bus Enable

## (28 Pin Package)

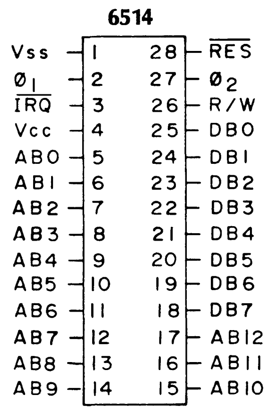
**6513**

| | | | |
|---|---|---|---|
| Vss | 1 | 28 | $\overline{RES}$ |
| $\emptyset_1$ | 2 | 27 | $\emptyset_2$ |
| $\overline{IRQ}$ | 3 | 26 | R/W |
| $\overline{NMI}$ | 4 | 25 | DB0 |
| Vcc | 5 | 24 | DB1 |
| AB0 | 6 | 23 | DB2 |
| AB1 | 7 | 22 | DB3 |
| AB2 | 8 | 21 | DB4 |
| AB3 | 9 | 20 | DB5 |
| AB4 | 10 | 19 | DB6 |
| AB5 | 11 | 18 | DB7 |
| AB6 | 12 | 17 | AB11 |
| AB7 | 13 | 16 | AB10 |
| AB8 | 14 | 15 | AB9 |

**FEATURES**

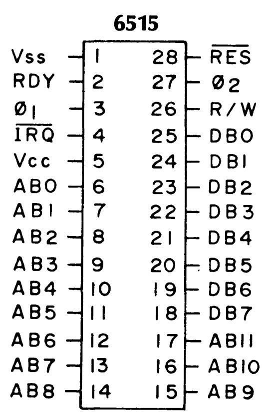
- 4K Addressable Bytes of Memory (AB00–AB11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bi-Directional Data Bus

**(28 Pin Package)**




**FEATURES**
- 8K Addressable Bytes of Memory (AB00–AB12)
- Two phase clock input
- IRQ Interrupt
- 8 Bit Bi-Directional Data Bus

**(28 Pin Package)**




**FEATURES**
- 4K Addressable Bytes of Memory (AB00–AB11)
- Two phase clock input
- IRQ Interrupt
- 8 Bit Bi-Directional Data Bus

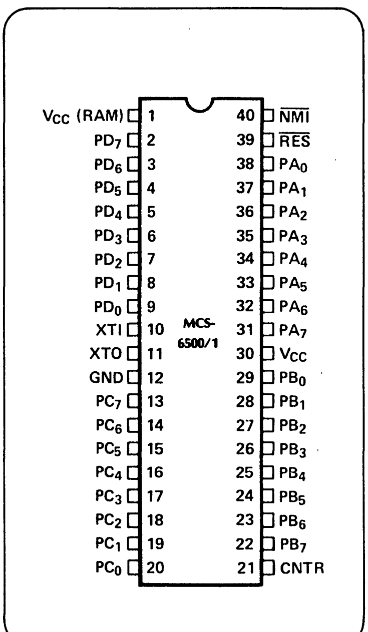
# 6500/1
# One-Chip 8-Bit Microcomputer

- **Single +5 Volt Power Supply.**
- **2048 Bytes of ROM.**
- **64 Bytes of RAM.**
- **32 Bi-Directional I/O Lines.**
- **16-Bit Programmable Interval Timer/Event Counter.**
- **Software-Compatible with MCS6502.**
- **Pipeline Architecture for High-Performance.**
- **Thirteen Address Modes With True Indexing Capability.**
- **Variable Length Stack.**
- **Two Index Registers.**

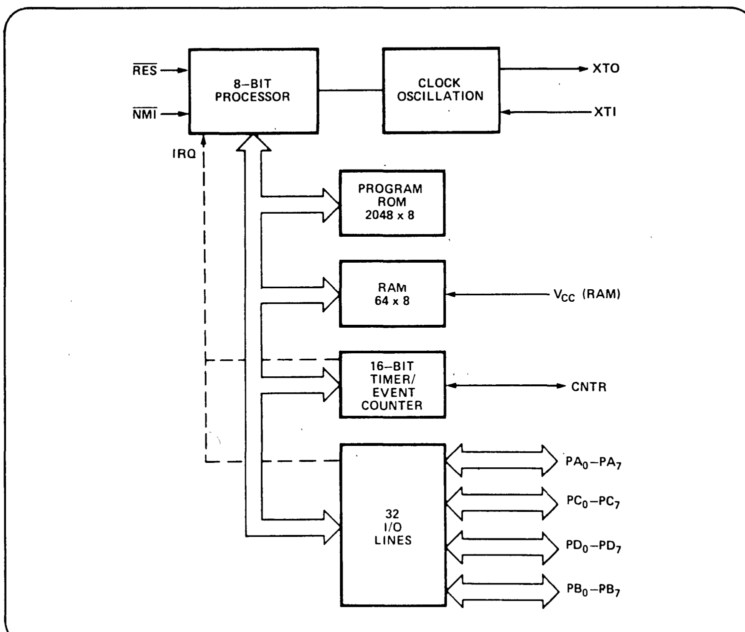
## Description

The 6500/1 is a completely self-contained single-chip microcomputer system. Included in the 6500/1 are 2048 bytes of mask-programmable ROM, 64 bytes of RAM, 32 I/O lines, a 16-bit timer/counter, and an on-chip clock oscillator. The internal processor architecture is identical to the 6502 to provide software compatibility and to assure high-performance operation.

## PIN CONFIGURATION




## BLOCK DIAGRAM




**Note**
MCS = Ceramic package
MPS = Plastic package

## INTERNAL ARCHITECTURE

### Index Registers

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Indexing simplifies many types of programs, especially those which make extensive use of tables.

### Stack Pointer

The Stack Pointer is an 8-bit register used to control the addressing of the variable-length Stack. It is automatically decremented and incremented by the CPU when the Stack is accessed.

The Stack is used automatically by the CPU for interrupt processing and subroutine calling and may also be used by the programmer for other temporary storage functions.

### Arithmetic and Logic Unit (ALU)

All arithmetic and logical operations are done in the ALU. The ALU has no internal memory and is used only to perform transient numerical operations.

### Accumulator

The Accumulator is a special-purpose 8-bit register which is used to hold the results of most arithmetic and logical operations.

### Program Counter

The 16-bit Program Counter provides the addresses which step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher byte of the Program Counter (PCH) is placed on the high-order 8 bits. The Counter is incremented each time an instruction or data is fetched from program memory.

### Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the internal data bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

### Timing Control

The Timing Control Unit keeps track of the instruction cycle being executed. This unit is set to $T_0$ each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers depends on decoding the contents of both the instruction register and timing control unit.

### Interrupt Logic

The interrupt logic controls the processor interface to the interrupt inputs to ensure proper timing, enabling and sequencing of the interrupt signals which the processor recognizes and services.

### Clock Oscillator

The Clock Oscillator provides all the timing signals used by the CPU. A 2MHz crystal must be used with the 1MHz MCS6500/1 and a 4MHz crystal for the 2MHz MCS6500/1A.

### 2K x 8 ROM

The 2048-byte Read Only Memory (ROM) usually contains the program instructions and other fixed data. These program instructions and constants are permanently stored in the ROM by metal mask programming during fabrication of the 6500/1.

### 64 x 8 RAM

The 64-byte Random Access Memory (RAM) contains the user program stack and is used as scratchpad memory. This RAM is completely static, requiring no clock or dynamic refresh. A standby power pin allows RAM memory to be maintained at a reduced operating power. In the event that power is lost and execution stops, this standby power retains RAM data until execution resumes.

### Status/Control Register

The 8-bit Status/Control Register controls and reports the status of eight signals — five control signals and three status signals.

**Counter/Latch**

The Counter/Latch consists of a 16-bit counter and a 16-bit latch register. The counter contains either a count of $\phi 2$ clock periods or a selected external event, depending on the counter mode selected in the Status/Control Register. The counter initialization value is stored in the latch.

**Input/Output (I/O) Ports**

The 6500/1 provides four 8-bit I/O ports—PA, PB, PC, and PD. The 32 I/O lines of these ports are bidirectional; all signals may be used for either input or output.

**INSTRUCTION SET**

The 6500/1 instruction set is identical to that of the 6502 described in the preceding data sheet.

**COMMENT**

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**ABSOLUTE MAXIMUM RATINGS**

| Rating | Symbol | Allowable Range | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | V |
| Input/Output Voltage | $V_{IN}$ | −0.3 to +7.0 | V |
| Operating Temp. | $T_{OP}$ | 0 to 70 | °C |
| Storage Temp. | $T_{STG}$ | −55 to +150 | °C |

**Note**

All inputs contain protection circuitry to prevent damage due to static discharge. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0V ±5%, $T_A$ = 0-70°C, unless otherwise noted)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage | −0.3 | | 0.8 | V |
| $V_{IHXT}$ | Input High Voltage (XTL1) | 2.4 | | $V_{CC}$ | V |
| $V_{ILXT}$ | Input Low Voltage (XTL1) | −0.3 | | 0.4 | V |
| $I_{IN}$ | Input Leakage ($\overline{RES}$, $\overline{NMI}$) | | | 2.5 | μA |
| $I_{TSI}$ | Three-State Input Leakage ($PA_0$-$PA_7$, $PB_0$-$PB_7$, $PC_0$-$PC_7$, $PD_0$-$PD_7$, CNTR), $V_{IN}$ = 0.4 to 2.4V | | | 10.0 | μA |
| $V_{OH}$ | Output High Voltage, $I_{LOAD}$ = 100μA | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage, $I_{LOAD}$ = 1.6mA | | | 0.4 | V |
| $P_D$ | Power Dissipation | | 500 | | mW |
| $I_{RR}$ | Standby Current (RAM only) | | 10 | | mA |
| $C_{IN}$ | Input Capacitance ($\overline{RES}$, $\overline{NMI}$) | | | 10.0 | pF |
| $C_{TSI}$ | Three-State Input Capacitance ($PA_0$-$PA_7$, $PB_0$-$PB_7$, $PC_0$-$PC_7$, $PD_0$-$PD_7$, CNTR) | | | 10.0 | pF |
| $C_{INX}$ | Input Capacitance (XTL1) | | | 50.0 | pF |
| $C_{OUT}$ | Output Capacitance: $V_{IN}$ = 0V, $T_A$ = 25°C, f = 1.0 MHz | | | 10.0 | pF |

commodore semiconductor group

NMOS

PRELIMINARY

# 6508
# Microprocessor With RAM and I/O

- 8-Bit Bi-directional I/O Port
- 256 Bytes fully Static RAM (internal)
- Single +5 volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- 8 BIT Bi-directional Data Bus
- Addressable memory range of up to 65K bytes
- Direct memory access capability
- Bus compatible with M6800
- Pipeline architecture
- 1 MHz and 2 MHz operation
- Use with any type or speed memory

## DESCRIPTION

The 6508 is a low-cost microcomputer system capable of solving a broad range of small-systems and peripheral-control problems at minimum cost to the user.

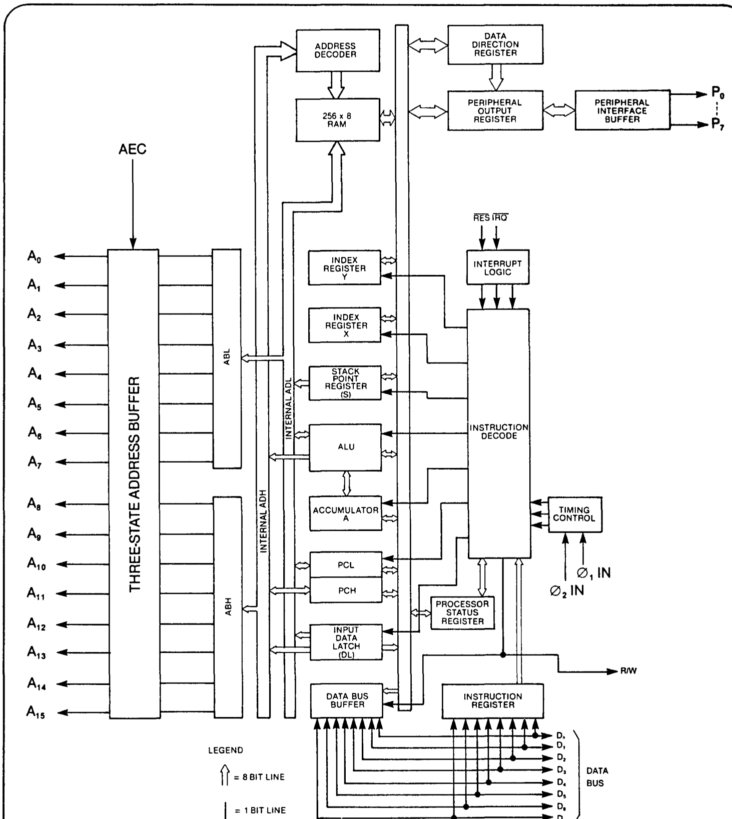
One full page (256 bytes) of RAM is located (on chip) concurrently at Page 0 and Page 1, allowing Zero Page Addressing and stack operations with no additional RAM.

## PIN CONFIGURATION

6508

| | | | |
|---|---|---|---|
| RES | 1 | 40 | $\varnothing_2$ IN |
| $\varnothing_1$ IN | 2 | 39 | R/W |
| $\overline{IRQ}$ | 3 | 38 | $DB_0$ |
| AEC | 4 | 37 | $DB_1$ |
| $V_{DD}$ | 5 | 36 | $DB_2$ |
| $A_0$ | 6 | 35 | $DB_3$ |
| $A_1$ | 7 | 34 | $DB_4$ |
| $A_2$ | 8 | 33 | $DB_5$ |
| $A_3$ | 9 | 32 | $DB_6$ |
| $A_4$ | 10 | 31 | $DB_7$ |
| $A_5$ | 11 | 30 | $P_0$ |
| $A_6$ | 12 | 29 | $P_1$ |
| $A_7$ | 13 | 28 | $P_2$ |
| $A_8$ | 14 | 27 | $P_3$ |
| $A_9$ | 15 | 26 | $P_4$ |
| $A_{10}$ | 16 | 25 | $P_5$ |
| $A_{11}$ | 17 | 24 | $P_6$ |
| $A_{12}$ | 18 | 23 | $P_7$ |
| $A_{13}$ | 19 | 22 | $A_{15}$ |
| $V_{SS}$ | 20 | 21 | $A_{14}$ |

## BLOCK DIAGRAM



## DESCRIPTION (cont.)

An 8-bit Bi-Directional I/O Port is located on-chip with the Output Register at Address 0 0 0 1 and the Data-Direction Register at Address 0 0 0 0. The I/O Port is bit-by-bit programmable.

The Three-State sixteen-bit Address Bus allows Direct Memory Accessing (DMA) and multi-processor systems sharing a common memory.

The internal processor architecture is identical to the 6502 to provide software compatibility.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | −0.3 to +7.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

### COMMENT

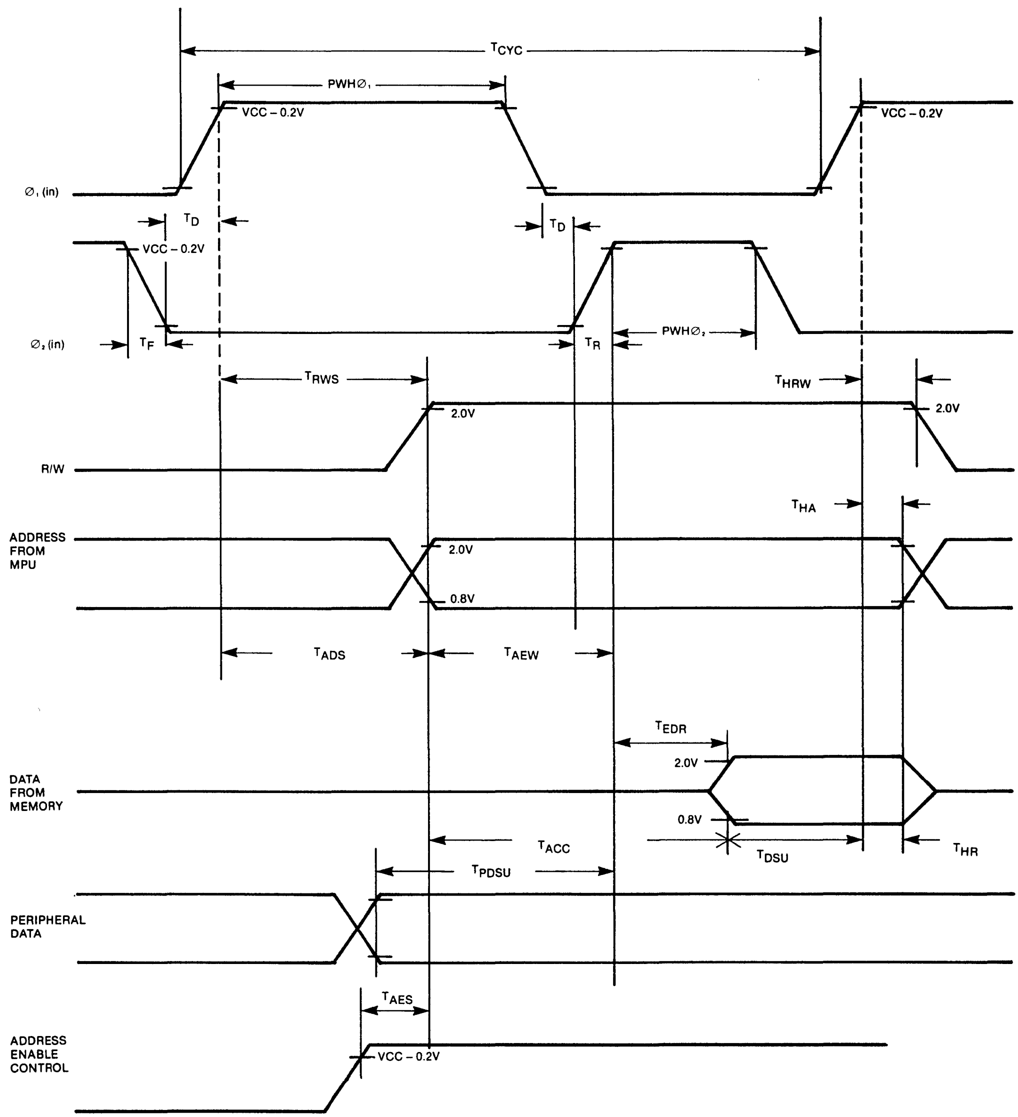
*This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.*

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = 0, $T_A$ = 0° to +70°C)

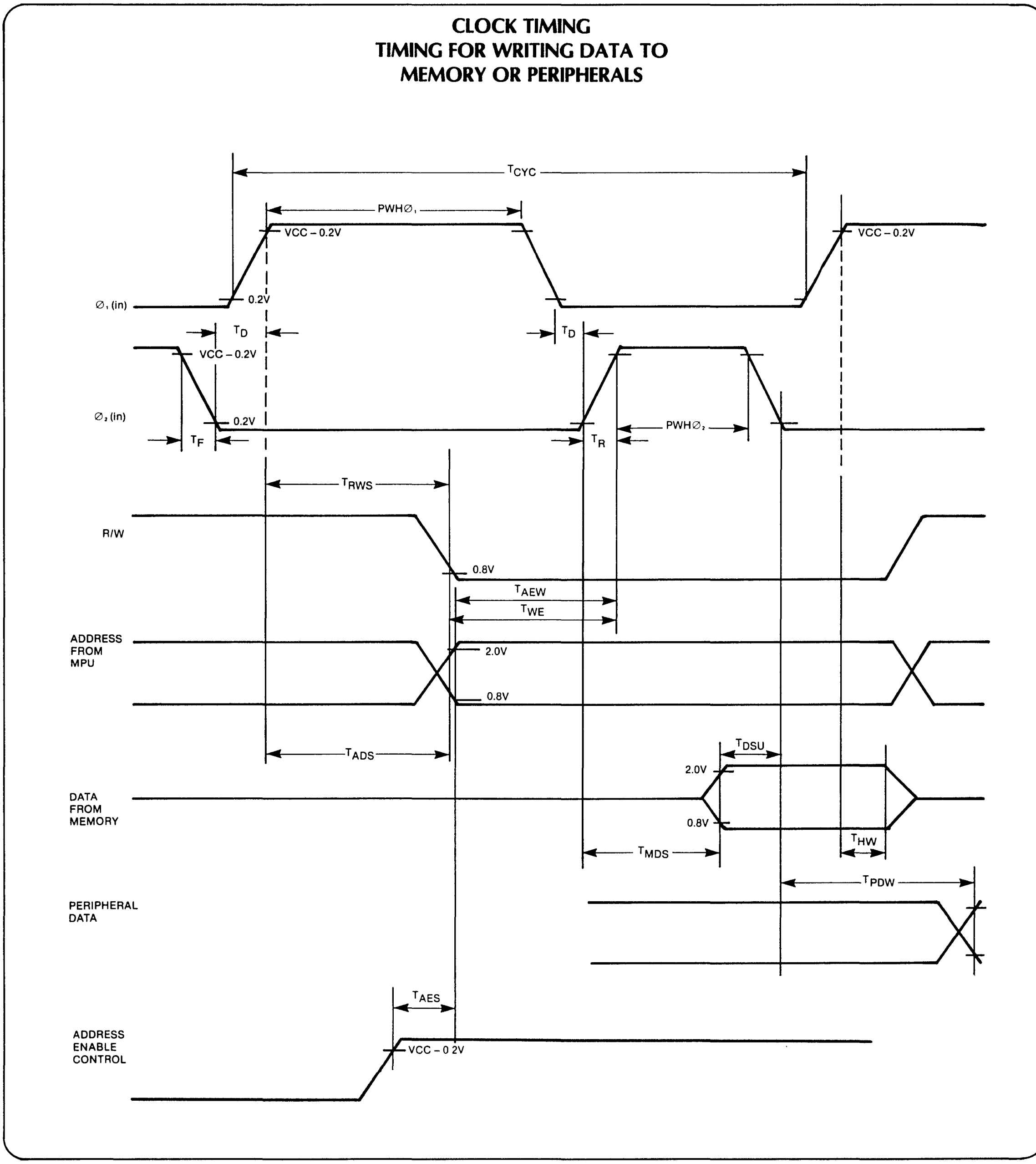
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage $\phi_1$, $\phi_{2(in)}$ | $V_{CC}$ − 0.2 | | $V_{CC}$ + 1.0 V | Vdc |
| | Input High Voltage $\overline{RES}$, $P_0$–$P_7$ $\overline{IRQ}$, Data | $V_{SS}$ + 2.0 | | | Vdc |
| $V_{IL}$ | Input Low Voltage $\phi_1$, $\phi_{2(in)}$ | $V_{SS}$ − 0.3 | | $V_{SS}$ + 0.2 | Vdc |
| | $\overline{RES}$, $P_0$–$P_7$ $\overline{IRQ}$, Data | | | $V_{SS}$ + 0.8 | Vdc |
| $I_{IN}$ | Input Leakage Current ($V_{IN}$ = 0 to 5.25 V, $V_{CC}$ = 5.25 V) Logic | | | 2.5 | μA |
| | $\phi_1$, $\phi_{2(in)}$ | | | 100 | μA |
| $I_{TSI}$ | Three State (Off State) Input Current ($V_{IN}$ = 0.4 to 2.4 V, $V_{CC}$ = 5.25 V) Data Lines | | | 10 | μA |
| $V_{OH}$ | Output High Voltage ($I_{OH}$ = −100 μAdc, $V_{CC}$ = 4.75 V) Data, A0–A15, R/W, $P_0$–$P_7$ | $V_{SS}$ + 2.4 | | | Vdc |
| $V_{OL}$ | Out Low Voltage ($I_{OL}$ = 1.6 mAdc, $V_{CC}$ = 4.75 V) Data, A0–A15, R/W, $P_0$–$P_7$ | | | $V_{SS}$ + 0.4 | Vdc |
| $P_D$ | Power Dissipation | | | | W |
| C | Capacitance ($V_{IN}$ = 0, $T_A$ = 25°C, f = 1 MHz) | | | | pF |
| $C_{IN}$ | Logic, $P_0$–$P_7$ | | | 10 | |
| | Data | | | 15 | |
| $C_{OUT}$ | A0–A15, R/W | | | 12 | |
| $C_{\phi_1}$ | $\phi_1$ | | 30 | 50 | |
| $C_{\phi_2}$ | $\phi_2$ | | 50 | 80 | |

## TIMING DIAGRAMS

### CLOCK TIMING
### TIMING FOR READING DATA FROM MEMORY OR PERIPHERALS



## TIMING DIAGRAMS (cont.)



**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5 V ± 5%, $V_{SS}$ = 0 V, $T_A$ = 0°-70°C)

| Symbol | Parameter | 1 MHz Timing | | | 2 MHz Timing | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Clock Timing $T_{CYC}$ | Cycle Time | 1000 | | | 500 | | | ns |
| $PWH_{\phi_1}$<br>$PWH_{\phi_2}$ | Clock Pulse Width $\phi_1$<br>(Measured at $V_{CC}$ − 0.2 V) $\phi_2$ | 430<br>470 | | | 215<br>235 | | | ns<br>ns |
| $T_F$, $T_R$ | Fall Time, Rise Time (Measured from 0.2 V to $V_{CC}$ − 0.2 V) | | | 25 | | | 15 | ns |
| $T_D$ | Delay Time between Clocks (Measured at 0.2 V) | 0 | | | 0 | | | ns |

**READ/WRITE TIMING (LOAD = 1 TTL)**

| Symbol | Parameter | Min | Typ | Max | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $T_{RWS}$ | Read/Write Setup Time from 6508 | | 100 | 300 | | 100 | 150 | ns |
| $T_{ADS}$ | Address Setup Time from 6508 | | 100 | 300 | | 100 | 150 | ns |
| $T_{ACC}$ | Memory Read Access Time | | | 575 | | | 300 | ns |
| $T_{DSU}$ | Data Stability Time Period | 100 | | | 50 | | | ns |
| $T_{HR}$ | Data Hold Time – Read | | | | | | | ns |
| $T_{HW}$ | Data Hold Time – Write | 10 | 30 | | 10 | 30 | | ns |
| $T_{MDS}$ | Data Setup Time from 6508 | | 150 | 200 | | 75 | 100 | ns |
| $T_{HA}$ | Address Hold Time | 10 | 30 | | 10 | 30 | | ns |
| $T_{HRW}$ | R/W Hold Time | 10 | 30 | | 10 | 30 | | ns |
| $T_{AEW}$ | Delay Time, Address valid to $\phi_2$ positive transition | 180 | | | | | | ns |
| $T_{EDR}$ | Delay Time, $\phi_2$ positive transition to Data valid on bus | | | 395 | | | | ns |
| $T_{DSU}$ | Delay Time, Data valid to $\phi_2$ negative transition | 300 | | | | | | ns |
| $T_{WE}$ | Delay Time, R/W negative transition to $\phi_2$ positive transition | 130 | | | | | | ns |
| $T_{PDW}$ | Delay Time, $\phi_2$ negative transition to Peripheral Data valid | | | 1 | | | | µs |
| $T_{PDSU}$ | Peripheral Data Setup Time | 300 | | | | | | ns |
| $T_{AES}$ | Address Enable Setup Time | | | 60 | | | | ns |

## SIGNAL DESCRIPTION

### Clocks ($\phi_1$, $\phi_2$)
The 6508 requires a two phase non-overlapping clock that runs at the $V_{CC}$ voltage level.

### Address Bus ($A_0$-$A_{15}$)
These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

### Data Bus ($D_0$-$D_7$)
Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

### Reset
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After $V_{CC}$ reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

### Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses.

### Address Enable Control (AEC)
The Address Bus is valid only when the Address Enable Control line is high. When low, the Address Bus is in a high-impedance state. This feature allows easy DMA and multiprocessor systems.

### I/O Port ($P_0$-$P_7$)
Eight pins are used for the peripheral port, which can transfer data to or from peripheral devices. The Output Register is located in RAM at Address 0 0 0 1, and the Data Direction Register is at Address 0 0 0 0. The outputs are capable at driving one standard TTL load and 130 pF.

### Read/Write (R/W)
This signal is generated by the microprocessor to control the direction of data transfers on the Data Bus. This line is high except when the microprocessor is writing to memory or a peripheral device.

NOTE
The 6508 economizes on chip area by locating Page Zero and Page One concurrently in the same 256 bytes of RAM. This allows Page Zero addressing, with stack operations in Page One, with only 256 bytes of memory on-chip, resulting in lower chip area and hence, cost. During the initialization sequence, the stack pointer should be started at location 01FF. When talking to internal RAM, the Data Bus is in a high-impedance state.

## ADDRESSING MODES

### Accumulator Addressing
This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

### Immediate Addressing
In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

### Absolute Addressing
In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

### Zero Page Addressing
The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

### Indexed Zero Page Addressing
(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

## ADDRESSING MODES (cont.)

### Indexed Absolute Addressing

(X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

### Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

### Relative Addressing

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

### Indexed Indirect Addressing

In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

### Indirect Indexed Addressing

In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

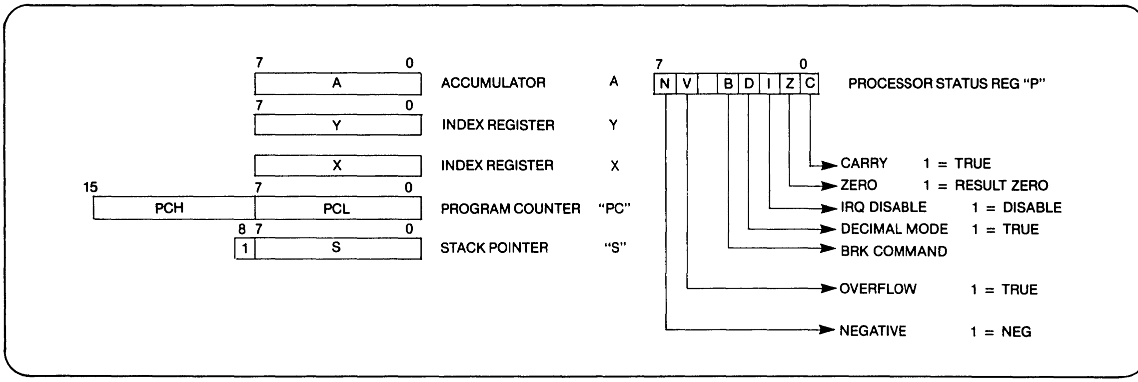
### Absolute Indirect

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

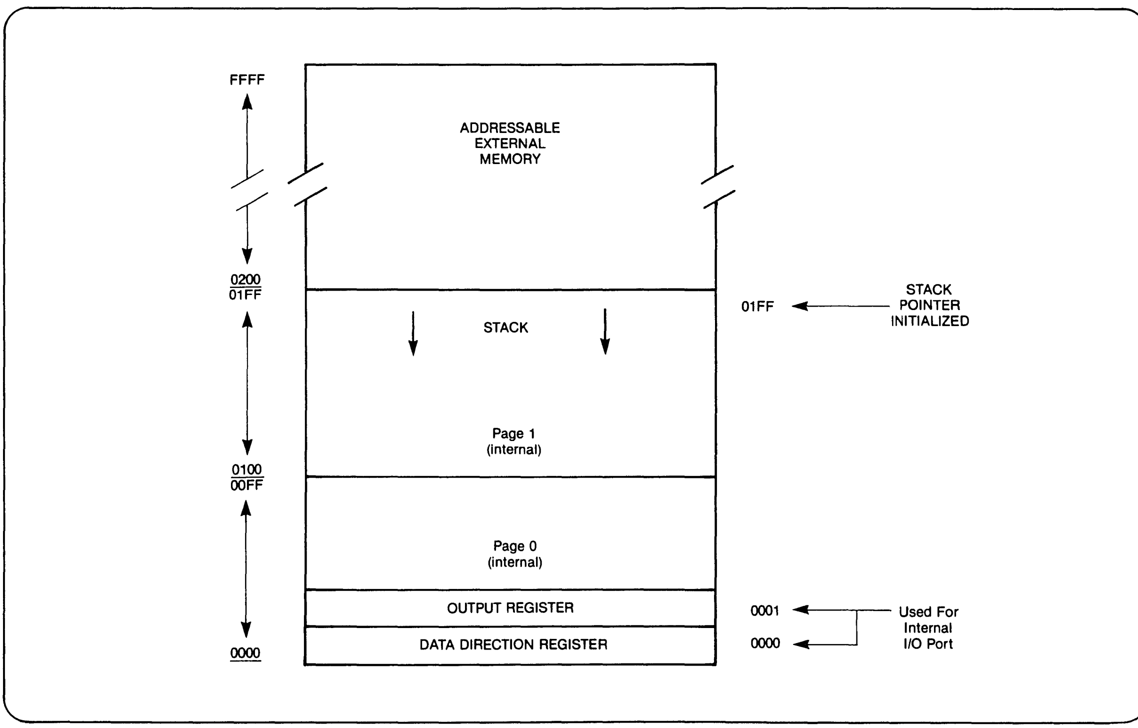
#### INSTRUCTION SET—ALPHABETIC SEQUENCE

| | |
|---|---|
| ADC | Add Memory to Accumulator with Carry |
| AND | "AND" Memory with Accumulator |
| ASL | Shift left One Bit (Memory or Accumulator) |
| BCC | Branch on Carry Clear |
| BCS | Branch on Carry Set |
| BEQ | Branch on Result Zero |
| BIT | Test Bits in Memory with Accumulator |
| BMI | Branch on Result Minus |
| BNE | Branch on Result not Zero |
| BPL | Branch on Result Plus |
| BRK | Force Break |
| BVC | Branch on Overflow Clear |
| BVS | Branch on Overflow Set |
| CLC | Clear Carry Flag |
| CLD | Clear Decimal Mode |
| CLI | Clear Interrupt Disable Bit |
| CLV | Clear Overflow Flag |
| CMP | Compare Memory and Accumulator |
| CPX | Compare Memory and Index X |
| CPY | Compare Memory and Index Y |
| DEC | Decrement Memory by One |
| DEX | Decrement Index X by One |
| DEY | Decrement Index Y by One |
| EOR | "Exclusive-or" Memory with Accumulator |
| INC | Increment Memory by One |
| INX | Increment Index X by One |
| INY | Increment Index Y by One |
| JMP | Jump to New Location |
| JSR | Jump to New Location Saving Return Address |
| LDA | Load Accumulator with Memory |
| LDX | Load Index X with Memory |
| LDY | Load Index Y with Memory |
| LSR | Shift One Bit Right (Memory or Accumulator) |
| NOP | No Operation |
| ORA | "OR" Memory with Accumulator |
| PHA | Push Accumulator on Stack |
| PHP | Push Processor Status on Stack |
| PLA | Pull Accumulator from Stack |
| PLP | Pull Processor Status from Stack |
| ROL | Rotate One Bit Left (Memory or Accumulator) |
| ROR | Rotate One Bit Right (Memory or Accumulator) |
| RTI | Return from Interrupt |
| RTS | Return from Subroutine |
| SBC | Subtract Memory from Accumulator with Borrow |
| SEC | Set Carry Flag |
| SED | Set Decimal Mode |
| SEI | Set Interrupt Disable Status |
| STA | Store Accumulator in Memory |
| STX | Store Index X in Memory |
| STY | Store Index Y in Memory |
| TAX | Transfer Accumulator to Index X |
| TAY | Transfer Accumulator to Index Y |
| TSX | Transfer Stack Pointer to Index X |
| TXA | Transfer Index X to Accumulator |
| TXS | Transfer Index X to Stack Register |
| TYA | Transfer Index Y to Accumulator |

## PROGRAMMING MODEL




## 6508 MEMORY MAP




## APPLICATIONS NOTES

Locating the Output Register at the internal I/O Port in Page Zero enhances the powerful Zero Page Addressing instructions of the 6508.

By assigning the I/O pins as inputs (using the Data Direction Register) the user has the ability to change the contents of address 0001 (the Output Register) using peripheral devices. The ability to change these contents using peripheral inputs, together with Zero Page Indirect Addressing instructions, allows novel and versatile programming techniques not possible earlier.

## INSTRUCTION SET—OP CODES, Execution Time, Memory Requirements

| INSTRUCTIONS | | IMMEDIATE | | | ABSOLUTE | | | Z PAGE | | | ACCUM | | | IMPLIED | | | (IND,X) | | | (IND),Y | | | Z PAGE,X | | | ABS,X | | | ABS,Y | | | RELATIVE | | | INDIRECT | | | Z PAGE,Y | | | CONDITION CODES | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MNEMONIC | OPERATION | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | OP | N | # | N | Z | C | I | D | V |
| A D C | A+M+C→A (1) | 69 | 2 | 2 | 6D | 4 | 3 | 65 | 3 | 2 | | | | | | | 61 | 6 | 2 | 71 | 5 | 2 | 75 | 4 | 2 | 7D | 4 | 3 | 79 | 4 | 3 | | | | | | | | | | ✓ | ✓ | ✓ | - | - | ✓ |
| A N D | A∧M→A (1) | 29 | 2 | 2 | 2D | 4 | 3 | 25 | 3 | 2 | | | | | | | 21 | 6 | 2 | 31 | 5 | 2 | 35 | 4 | 2 | 3D | 4 | 3 | 39 | 4 | 3 | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| A S L | C←[7 Ø]←0 | | | | ØE | 6 | 3 | Ø6 | 5 | 2 | ØA | 2 | 1 | | | | | | | | | | 16 | 6 | 2 | 1E | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| B C C | BRANCH ON C=Ø (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 9Ø | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B C S | BRANCH ON C=1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | BØ | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B E Q | BRANCH ON Z=1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | FØ | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B I T | A∧M | | | | 2C | 4 | 3 | 24 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | $M_7$ | ✓ | - | - | - | $M_6$ |
| B M I | BRANCH ON N=1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 3Ø | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B N E | BRANCH ON Z=Ø (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | DØ | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B P L | BRANCH ON N=Ø (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1Ø | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B R K | (See Fig 1) | | | | | | | | | | | | | ØØ | 7 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | 1 | - | - |
| B V C | BRANCH ON V=Ø (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 5Ø | 2 | 2 | | | | | | | - | - | - | - | - | - |
| B V S | BRANCH ON V=1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 7Ø | 2 | 2 | | | | | | | - | - | - | - | - | - |
| C L C | Ø→C | | | | | | | | | | | | | 18 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | Ø | - | - | - |
| C L D | Ø→D | | | | | | | | | | | | | D8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | Ø | - |
| C L I | Ø→I | | | | | | | | | | | | | 58 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | Ø | - | - |
| C L V | Ø→V | | | | | | | | | | | | | B8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | Ø |
| C M P | A−M (1) | C9 | 2 | 2 | CD | 4 | 3 | C5 | 3 | 2 | | | | | | | C1 | 6 | 2 | D1 | 5 | 2 | D5 | 4 | 2 | DD | 4 | 3 | D9 | 4 | 3 | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| C P X | X−M | EØ | 2 | 2 | EC | 4 | 3 | E4 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| C P Y | Y−M | CØ | 2 | 2 | CC | 4 | 3 | C4 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| D E C | M−1→M | | | | CE | 6 | 3 | C6 | 5 | 2 | | | | | | | | | | | | | D6 | 6 | 2 | DE | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| D E X | X−1→X | | | | | | | | | | | | | CA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| D E Y | Y−1→Y | | | | | | | | | | | | | 88 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| E O R | A⊻M→A (1) | 49 | 2 | 2 | 4D | 4 | 3 | 45 | 3 | 2 | | | | | | | 41 | 6 | 2 | 51 | 5 | 2 | 55 | 4 | 2 | 5D | 4 | 3 | 59 | 4 | 3 | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| I N C | M+1→M | | | | EE | 6 | 3 | E6 | 5 | 2 | | | | | | | | | | | | | F6 | 6 | 2 | FE | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| I N X | X+1→X | | | | | | | | | | | | | E8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| I N Y | Y+1→Y | | | | | | | | | | | | | C8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| J M P | JUMP TO NEW LOC | | | | 4C | 3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | 6C | 5 | 3 | | | | - | - | - | - | - | - |
| J S R | (See Fig. 2) JUMP SUB | | | | 2Ø | 6 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| L D A | M→A (1) | A9 | 2 | 2 | AD | 4 | 3 | A5 | 3 | 2 | | | | | | | A1 | 6 | 2 | B1 | 5 | 2 | B5 | 4 | 2 | BD | 4 | 3 | B9 | 4 | 3 | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| L D X | M→X (1) | A2 | 2 | 2 | AE | 4 | 3 | A6 | 3 | 2 | | | | | | | | | | | | | | | | | | | BE | 4 | 3 | | | | | | | B6 | 4 | 2 | ✓ | ✓ | - | - | - | - |
| L D Y | M→Y (1) | AØ | 2 | 2 | AC | 4 | 3 | A4 | 3 | 2 | | | | | | | | | | | | | B4 | 4 | 2 | BC | 4 | 3 | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| L S R | Ø→[7 Ø]→C | | | | 4E | 6 | 3 | 46 | 5 | 2 | 4A | 2 | 1 | | | | | | | | | | 56 | 6 | 2 | 5E | 7 | 3 | | | | | | | | | | | | | Ø | ✓ | ✓ | - | - | - |
| N O P | NO OPERATION | | | | | | | | | | | | | EA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| O R A | A∨M→A | Ø9 | 2 | 2 | ØD | 4 | 3 | Ø5 | 3 | 2 | | | | | | | Ø1 | 6 | 2 | 11 | 5 | 2 | 15 | 4 | 2 | 1D | 4 | 3 | 19 | 4 | 3 | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| P H A | A→$M_S$ S−1→S | | | | | | | | | | | | | 48 | 3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| P H P | P→$M_S$ S−1→S | | | | | | | | | | | | | Ø8 | 3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| P L A | S+1→S $M_S$→A | | | | | | | | | | | | | 68 | 4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| P L P | S+1→S $M_S$→P | | | | | | | | | | | | | 28 | 4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | (RESTORED) | | | | | |
| R O L | ←[7 Ø]←[C]← | | | | 2E | 6 | 3 | 26 | 5 | 2 | 2A | 2 | 1 | | | | | | | | | | 36 | 6 | 2 | 3E | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| R O R | →[C]→[7 Ø]→ | | | | 6E | 6 | 3 | 66 | 5 | 2 | 6A | 2 | 1 | | | | | | | | | | 76 | 6 | 2 | 7E | 7 | 3 | | | | | | | | | | | | | ✓ | ✓ | ✓ | - | - | - |
| R T I | (See Fig 1) RTRN INT | | | | | | | | | | | | | 4Ø | 6 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | (RESTORED) | | | | | |
| R T S | (See Fig 2) RTRN SUB | | | | | | | | | | | | | 6Ø | 6 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| S B C | A−M−C→A (1) | E9 | 2 | 2 | ED | 4 | 3 | E5 | 3 | 2 | | | | | | | E1 | 6 | 2 | F1 | 5 | 2 | F5 | 4 | 2 | FD | 4 | 3 | F9 | 4 | 3 | | | | | | | | | | ✓ | ✓ | (3) | - | - | ✓ |
| S E C | 1→C | | | | | | | | | | | | | 38 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | 1 | - | - | - |
| S E D | 1→D | | | | | | | | | | | | | F8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | 1 | - |
| S E I | 1→I | | | | | | | | | | | | | 78 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | 1 | - | - |
| S T A | A→M | | | | 8D | 4 | 3 | 85 | 3 | 2 | | | | | | | 81 | 6 | 2 | 91 | 6 | 2 | 95 | 4 | 2 | 9D | 5 | 3 | 99 | 5 | 3 | | | | | | | | | | - | - | - | - | - | - |
| S T X | X→M | | | | 8E | 4 | 3 | 86 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | 96 | 4 | 2 | - | - | - | - | - | - |
| S T Y | Y→M | | | | 8C | 4 | 3 | 84 | 3 | 2 | | | | | | | | | | | | | 94 | 4 | 2 | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| T A X | A→X | | | | | | | | | | | | | AA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| T A Y | A→Y | | | | | | | | | | | | | A8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| T S X | S→X | | | | | | | | | | | | | BA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| T X A | X→A | | | | | | | | | | | | | 8A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |
| T X S | X→S | | | | | | | | | | | | | 9A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | - | - | - | - | - | - |
| T Y A | Y→A | | | | | | | | | | | | | 98 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | ✓ | ✓ | - | - | - | - |

(1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED

(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE.
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE.

(3) CARRY NOT=BORROW

(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX, X
Y INDEX, Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
$M_S$ MEMORY PER STACK POINTER

\+ ADD
− SUBTRACT
∧ AND
V OR

⊻ EXCLUSIVE OR
✓ MODIFIED
\- NOT MODIFIED
$M_7$ MEMORY BIT 7
$M_6$ MEMORY BIT 6

N NO CYCLES
\# NO BYTES

**NOTE**

MOS Technology cannot assume liability for the use of undefined OP Codes

# 6520
# Peripheral Adapter

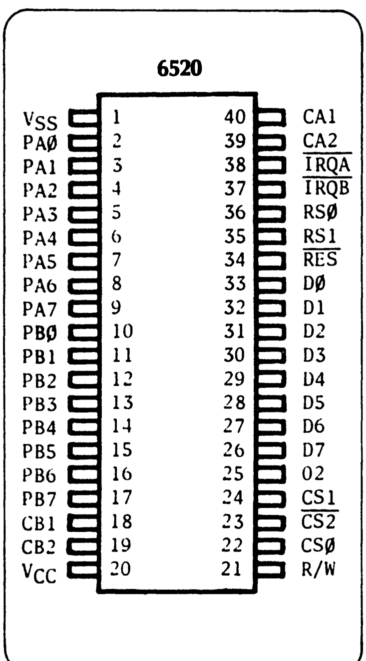
- **Fully TTL Compatible**
- **CMOS Compatible Peripheral Control lines**
- **8-Bit Bidirectional Data Control Transfer**
- **N-channel, Depletion-Load Technology**
- **Single +5V Supply**
- **Fully Automatic Handshake**
- **Independent Interrupt Control**

## DESCRIPTION

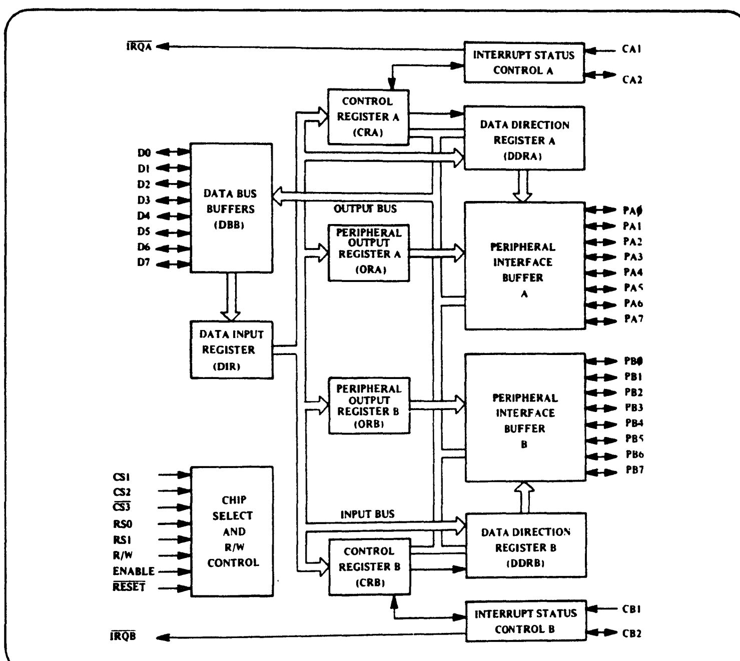
The 6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems encountered in the implementation of microcomputer systems. It allows an effective trade-off between software and hardware by providing significant capability and flexibility. When coupled with the power and speed of the 6500 family of microprocessors, the 6520 allows implementation of very complex systems at minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit, bidirectional ports. Each of these lines is programmable to be either input or output. In addition, four peripheral control/interrupt lines are provided. These lines may be used to interrupt the processor or for automatic handshaking of data between the processor and a peripheral device.

## PIN CONFIGURATION




## BLOCK DIAGRAM




**Note**
MSC = Ceramic package
MPS = Plastic package

## INTERNAL ORGANIZATION

The 6520 is organized into two independent sections referred to as the "A side" and the "B side". Each section contains a Control Register (CRA and CRB), Data Direction Register (DDRA and DDRB), and Output Register (ORA and ORB), interrupt status control logic and the buffer necessary to drive the Peripheral Interface buses.

In addition to the above mirrored logic, the 6520 contains a Data Input Register. When the microprocessor writes data into the 6520, the data is latched into this register before being transferred into one of six internal registers of the 6520. The purpose of this register is to ensure smooth transitions on the output lines and to guarantee that the voltage will remain stable except when it is going to opposite polarity.

### Control Registers (CRA and CRB)

Figure 1 illustrates the bit designation and functions in the Control Registers. There registers allow the microprocessor to control the operation of the interrupt lines (CA1, CA2, CB1, CB2), and the peripheral control lines (CA2 and CB2). A single bit in each register controls the addressing of the Data Direction Registers and the Output Registers. In addition, bits 6 and 7 are used to indicate the status of the interrupt input lines (CA1, CA2, CB1, CB2). Normally, these interrupt status bits are interrogated by the microprocessor during the interrupt-service routines to determine the source of the interrupt to be handled. The remaining bits in these registers are discussed below under "Interface to the Peripheral Device".

Figure 1
**Control Register Bit Designations**

| | 7 | 6 | 5 4 3 | 2 | 1 0 |
|---|---|---|---|---|---|
| **CRA** | IRQA1 | IRQa2 | CA2 Control | DDRA Access | CA1 Control |

| | 7 | 6 | 5 4 3 | 2 | 1 0 |
|---|---|---|---|---|---|
| **CRB** | IRQB1 | IRQB2 | CB2 Control | DDRB Access | CB1 Control |

### Data Direction Registers (DDRA and DDRB)

The Data Direction Registers are programmed by the processor to configure each line in the 8-bit Peripheral I/O port to act as either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Placing a 0 in the DDR causes the corresponding Peripheral I/O line to act as an input, while a 1 causes it to act as an output.

### Peripheral Output Registers (ORA and ORB)

The Peripheral Output Registers store the output data which appears at the Peripheral I/O port. Writing a 0 into a bit in ORA causes the corresponding line on the Peripheral A port to go low if that line is programmed to act as an output, while a 1 causes the corresponding output to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

### Interrupt Status Control Logic

The four interrupt/peripheral control lines CA1, CA2, CB1 and CB2 are controlled by the two Interrupt Status Controls (A and B). This logic interprets the contents of the corresponding Control Register, detects active transitions on the interrupt inputs and performs other operations necessary to ensure proper operation of the four lines. The operation of the lines themselves is described in detail below under "Interface to the Peripheral Device".

### Peripheral Interface and Data Bus Buffers

These buffers provide the current and voltage drive necessary to ensure proper system operation and to meet device specifications of the 6520.

## OPERATION

This section describes the interaction between the 6520 and the processor first, then discusses the interface between the device and the peripheral device with which it is associated.

### Interface With the Processor

The basic interface between the 6520 and the 650X microprocessor is handled by an 8-bit bi-directional data bus, three chip-select lines, two register-select lines, two interrupt request lines, a read/write line, an enable line and a reset line.

**Data Bus (D0-D7).** The 8-bit bi-directional data bus allows the transfer of data between the microprocessor and the 6520. The data bus output drivers are three-state devices which remain in the high-impedance state except when the processor reads data from the peripheral adapter.

**Enable (E).** This input is the only microprocessor interface timing input on the device. All data transfers into and out of the 6520 are controlled by this signal. This input is normally connected to the $\phi 2$ clock signal of the processor.

**Read/Write (R/W).** This microprocessor-generated signal controls the direction of data transfers on the data bus. A low on this line enables the input buffers for a microprocessor Write cycle; data is transferred from the processor to the 6520 under timing control of the Enable input if the device has been chip-selected. A high on the line allows the 6520 to transfer data to the data bus.

**Chip Select Lines (CS1, CS2, $\overline{CS3}$).** These three inputs allow the processor to select the proper peripheral interface device. CS1 and CS2 must be high and $\overline{CS3}$ low for selection of the device. Data transfers are then performed under control of the Enable and R/W signals. Normally, these lines will be connected to the processor's address lines directly or through address decoding logic.

A single bit in each Control Register (CRA and CRB) controls access to the DDR or the Peripheral Interface. If Bit 2 in the CR is a 1, a Peripheral Output Register (ORA or ORB) is selected. If Bit 2 is a 0, the appropriate DDR is selected. Internal registers are selected by the Register Select Lines and the DDR Access Control bit as shown in Table 1.

**Table 1. CR and RS Interaction Logic**

| RS1 | RS0 | CRA2* | CRB2* | Register Selected |
|---|---|---|---|---|
| 0 | – | 1 | X | Peripheral Interface A |
| 0 | 0 | 0 | X | Data Direction Register A |
| 0 | 1 | X | X | Control Register A |
| 1 | 0 | X | 1 | Peripheral Interface B |
| 1 | 0 | X | 0 | Data Direction Register B |
| 1 | 1 | X | X | Control Register B |

NOTE
*Refers to Data Direction Register Access Control Bit

**Register Select Lines (RS0 and RS1).** These lines are used to select the various registers inside the 6520 (see Table 1). Normally, these lines are connected to address output lines on the processor and operate in conjunction with the chip-select inputs (CS1, CS2 and $\overline{CS3}$) to allow the microprocessor to address a single 8-bit register in the microprocessor address space.

The processor can *write* directly into CRA, CRB, DDRA, DDRB, ORA and ORB. It can also directly read the contents of CRA, CRB, DDRA and DDRB. Reading ORA and ORB is discussed separately in the next two paragraphs.

ORA consists of 8 lines which may be programmed to act as inputs or outputs. When acting as outputs, each line reflects the contents of the corresponding bit in the output register. When programmed as inputs, these lines go high or low depending on the input data. ORA has no effect on lines programmed as inputs, which means the 8 lines of the port may contain input, output or a mixture of both depending on the programming. As a result, the processor's sorfware must recognize and interpret only those bits which are inportant to the particular peripheral operation being performed. Since the processor always reads ORA pins instead of the actual register, it is possible for data read into the processor to differ from the contents of the register for a particular output line if the I/O pin is not allowed to go to a full high (+2.4VDC) when the corresponding ORA bit contains a 1.

ORB operates similarly to ORA except that data is read directly from the register for lines programmed to act as outputs. It is therefore possible to load down the Peripheral B output lines without causing incorrect data to be transferred back into the processor during a Read operation.

**Reset ($\overline{RES}$).** This active-low line resets the contents of all MCS6520 registers to a logic 0. It can be used as a power-on reset or as a master reset during system operation.

**Interrupt Request Lines ($\overline{IRQA}$ and $\overline{IRQB}$).** These active-low lines act to interrupt the processor directly or via external interrupr prioritization circuitry. All of these lines may be tied together in a wired-OR configuration. There is one interrupt request line for each peripheral port. Each has two interrupt flag bits (Bits 6 and 7 in the corresponding CR) which act as the link between peripheral interrupt signals and the processor's interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs CA1, CA2, CB1 and CB2.

**Interface to the Peripheral Device**

The 6520 provides two 8-bit bi-directional ports and four interrupt/control lines for interfacing to peripheral devices. These ports and the associated interrupt/control lines are referred to as the "A side" and "B side". Since each side has unique characteristics, they will be discussed separately.

**Peripheral A I/O Port (PA0–PA7).** The buffers which drive these lines contain "passive" pull-up devices which are resistive in nature, allowing the input voltage to go to $V_{dd}$ for a logic 1. In input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode.

**Peripheral B I/O Port (PB0–PB7).** The primary difference between these lines and their corresponding lines on the "A side" lies in the characteristics of the buffers driving them. The "B side" buffers are push-pull devices which are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage is not guaranteed to go higher than +2.4V; therefore, they are TTL-compatible but not CMOS compatible. When Peripheral B I/O lines are programmed to act as inputs, the output buffer enters a high-impedance state.

**Peripheral A Interrupt/Control Lines (CA1 and CA2).** CA1 is an interrupt input only. An active transition of the signal on this input will set Bit 7 of CRA to a logic 1. This active transition can be programmed by the processor setting a 0 in Bit 1 of the CRA if the interrupt flag (Bit 7) is to be set on a negative transition or to a 1 if the interrupt flag is to be set on a positive transition. Setting this flag will interrupt the processor through $\overline{IRQA}$ if Bit 0 of CRA is a 1.

CA2 can act as a totally independent interrupt input or as a peripheral control output. As an input (Bit 5 of CRA = 0), it acts to set the interrupt flag (Bit 6 of CRA) to a 1 on the active transition selected by Bit 4 of CRA. In this mode, CA2 operates identically with CA1. In Output Mode (Bit 5 of CRA = 1), CA2 generates a simple pulse each time the processor reads the data on the port. This pulse can then be used to control counters, shift registers and other logic elements which make sequential data available on the peripheral input lines. A second output mode can be used in conjunction with CA1 to handshake between the processor and the peripheral. On the "A side", this technique allows positive control of data transfers from the peripheral device to the processor. The CA1 input signals the processor that data is available by means of an interrupt to the processor. The processor reads the data and sets CA2 low, signalling the peripheral device that it can now make data available again. If Bit 4 of CRA is set to a 1, CA2 becomes a simple peripheral control output which can be set high or low by setting Bit 3 of CRA to a 1 or a 0, respectively.

**Peripheral B Interrupt/Control Lines (CB1 and CB2).** These lines operate identically to CA1 and CA2 (see above) with the following exceptions:

In one output mode, CB2's pulse output occurs when the processor writes data into the Peripheral B Output Register rather than pulsing on a read as with CA2.

In handshaking mode, CB2 operates on data transfers from the processor into the peripheral device rather than vice versa.

The operation of CA1, CA2, CB1 and CB2 with one another is summarized in Tables 2-5.

**Table 2. CA1/CB1 Control**

| CRA (CRB) Bit 1 | CRA (CRB) Bit 0 | Active Transition of Input Signal* | $\overline{IRQA}$ ($\overline{IRQB}$) Interrupt Outputs |
|---|---|---|---|
| 0 | 0 | Negative | Disable – remains high |
| 0 | 1 | Negative | Enable – goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1) |
| 1 | 0 | Positive | Disable – remains high |
| 1 | 1 | Positive | Enable – as explained above |

*NOTE
Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

**ABSOLUTE MAXIMUM RATINGS**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | −0.3 to +7.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

**CAUTION**

*This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.*

**DC CHARACTERISTICS** ($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = 0, $T_A$ = 0 to 70°C unless otherwise noted)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage (Normal Operating Levels) | +2.0 | | $V_{CC}$ | Vdc | |
| $V_{IL}$ | Input Low Voltage (Normal Operating Levels) | −0.3 | | +.8 | Vdc | |
| $I_{IN}$ | Input Leakage Current | | +1.0 | +2.5 | μAdc | $V_{IN}$ = 0 to 5.0 Vdc R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, CS1, $\overline{\text{CS2}}$, CA1, CB1, Φ 2 |
| $I_{TSI}$ | Three-State (Off State Input Current) | | +2.0 | +10 | μAdc | ($V_{IN}$ = 0.4 to 2.4 Vdc, $V_{CC}$ = max) D0-D7, PB0-PB7, CB2 |
| $I_{IH}$ | Input High Current | −100 | −250 | | μAdc | ($V_{IH}$ = 2.4 Vdc) PA0-PA7, CA2 |
| $I_{IL}$ | Input Low Current | | −1.0 | −1.6 | mAdc | ($V_{IL}$ = 0.4 Vdc) PA0-PA7, CA2 |
| $V_{OH}$ | Output High Voltage | 2.4 | | | Vdc | ($V_{CC}$ = min, $1_{Load}$ = −100 μAdc |
| $V_{OL}$ | Output Low Voltage | | | +0.4 | Vdc | ($V_{CC}$ = min, $1_{Load}$ = 1.6 mAdc) |
| $I_{OH}$ | Output High Current (Sourcing) | −100 | −1000 | | μAdc | ($V_{OH}$ = 2.4 Vdc) |
| $I_{OL}$ | Output Low Current (Sinking) | 1.6 | | | mAdc | ($V_{OL}$ = 0.4 Vdc) |
| $I_{OFF}$ | Output Leakage Current (Off State) | | 1.0 | 10 | μAdc | IRQA, IROB |
| $P_D$ | Power Dissipation | | 200 | 500 | mW | |
| $C_{IN}$ | Input Capacitance | | | 10<br>7.0<br>20 | pF | ($V_{IN}$ = 0, $T_A$ = 25°C, f = 1.0 MHz)<br>D0-D7, PA0-PA7, PB0-PB7, CA2, CB2,<br>R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, CS1, CS2,<br>CA1, CB1, Φ 2 |
| $C_{OUT}$ | Output Capacitance | | | 10 | pF | ($V_{IN}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) |

**NOTE**
Negative sign indicates outward current flow, positive indicates inward flow.

**Table 3. CA2/CB2 Input Modes**

| CRA (CRB) Bit 5 | Bit 4 | Bit 3 | Active Transition of Input Signal* | IRQA (IRQB) Interrupt Output |
|---|---|---|---|---|
| 0 | 0 | 0 | Negative | Disable – remains high |
| 0 | 0 | 1 | Negative | Enable – goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2) |
| 0 | 1 | 0 | Positive | Disable – remains high |
| 0 | 1 | 1 | Positive | Enable – as explained above |

*NOTE
Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

**Table 4. CA2 Output Modes**

| CRA Bit 5 | Bit 4 | Bit 3 | Mode | Description |
|---|---|---|---|---|
| 1 | 0 | 0 | "Handshake" on Read | CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor. |
| 1 | 0 | 1 | Pulse Output | CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken. |
| 1 | 1 | 0 | Manual Output | CA2 set low |
| 1 | 1 | 1 | Manual Output | CA2 set high |

**Table. 5 CB2 Output Modes**

| CRB Bit 5 | Bit 4 | Bit 3 | Mode | Description |
|---|---|---|---|---|
| 1 | 0 | 0 | "Handshake" on Write | CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device. |
| 1 | 0 | 1 | Pulse Output | CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available. |
| 1 | 1 | 0 | Manual Output | CB2 set low |
| 1 | 1 | 1 | Manual Output | CB2 set high |

**AC CHARACTERISTICS** $T_A$ = 0°C to +70°C, $V_{CC}$ = 5 V ± 5% (unless otherwise specified)

| Symbol | Characteristics | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | READ CYCLE (Loading 30 pF and one TTL load) | | | | |
| $T_{AEW}$ | Delay Time, Address Valid to Enable Positive Transition | 180 | | | ns |
| $T_{EDR}$ | Delay Time, Enable Positive Transition to Data Valid on Bus | | | 395 | ns |
| $T_{PDSU}$ | Peripheral Data Setup Time | 300 | | | ns |
| $T_{HR}$ | Data Bus Hold Time | 10 | | | ns |
| $T_{CA2}$ | Delay Time, Enable Negative Transition to CA2 Negative Transition | | | 1.0 | µs |
| $T_{RS1}$ | Delay Time, Enable Negative Transition to CA2 Positive Transition | | | 1.0 | µs |
| $t_r$, $t_f$ | Rise and Fall Time for CA1 and CA2 Input Signals | | | 1.0 | µs |
| $T_{RS2}$ | Delay Time from CA1 Active Transition to CA2 Postive Transition | | | 2.0 | µs |
| $t_{rE}$, $t_{fE}$ | Rise and Fall Time for Enable Input | | | 25 | µs |
| | WRITE CYCLE | | | | |
| $T_E$ | Enable Pulse Width | 0.470 | | 20 | µs |
| $T_{AEW}$ | Delay Time, Address Valid to Enable Positive Transition | 180 | | | ns |
| $T_{DSU}$ | Delay Time, Data Valid to Enable Negative Transition | 300 | | | ns |
| $T_{WE}$ | Delay Time, Read/Write Negative Transition to Enable Positive Transition | 130 | | | ns |
| $T_{HW}$ | Data Bus Hold Time | 10 | | | ns |
| $T_{PDW}$ | Delay Time, Enable Negative Transition to Peripheral Data Valid | | | 1.0 | µs |
| $T_{CMOS}$ | Delay Time, Enable Negative Transition to Peripheral Data Valid, CMOS ($V_{CC}$ −30%) PA0-PA7, CA2 | | | 2.0 | µs |
| $T_{CB2}$ | Delay Time, Enable Positive Transition to CB2 Negative Transition | | | 1.0 | µs |
| $T_{DC}$ | Delay Time, Peripheral Data Valid to CB2 Negative Transition | 0 | | 1.5 | µs |
| $T_{RS1}$ | Delay Time, Enable Positive Transition to CB2 Positive Transition | | | 1.0 | µs |
| $t_r$, $t_f$ | Rise and Fall Time for CB1 and CB2 Input Signals | | | 1.0 | µs |
| $T_{RS2}$ | Delay Time, CB1 Active Transition to CB2 Positive Transition | | | 2.0 | µs |

## TIMING DIAGRAM

### READ TIMING CHARACTERISTICS

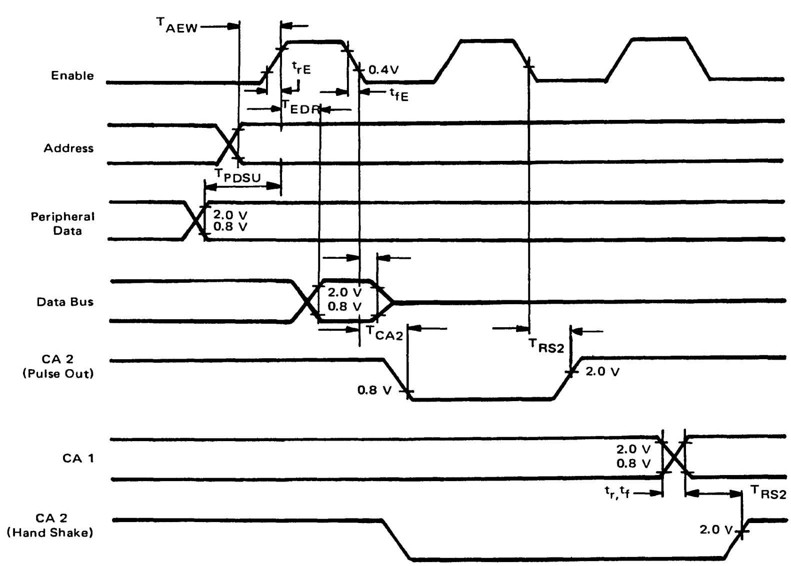



Figure 1

## WRITE TIMING CHARACTERISTICS

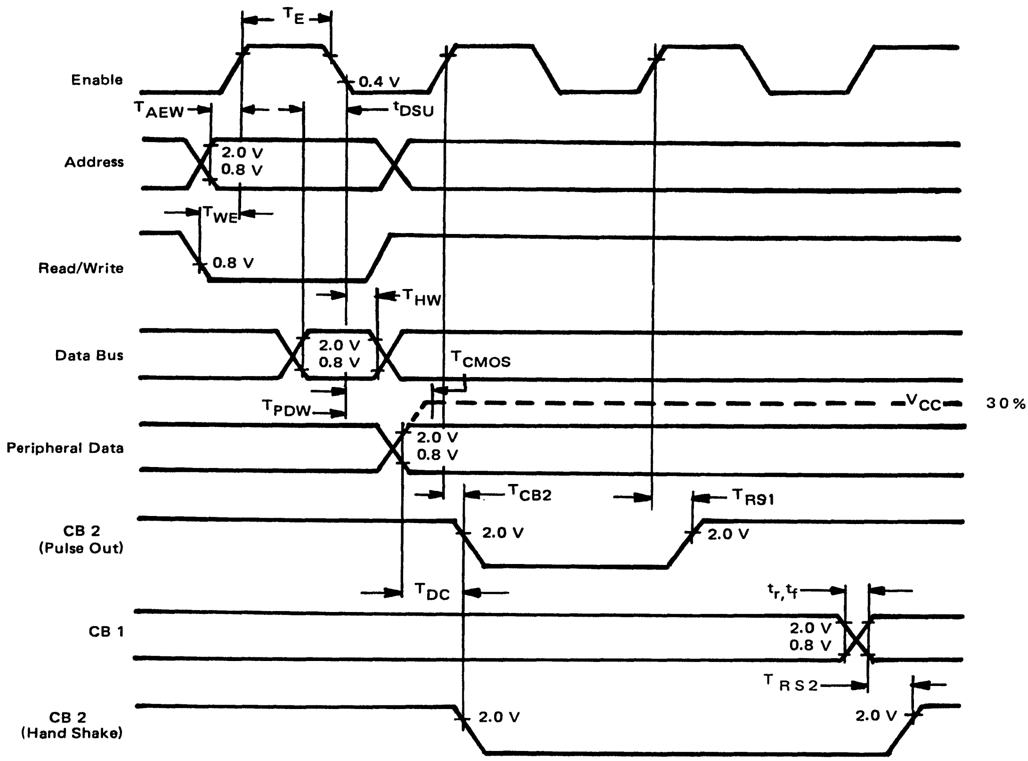



Figure 2

**commodore semiconductor group**

**NMOS**

# 6522
# Versatile Interface Adapter (VIA)

- Completely Static
- Fully TTL Compatible
- CMOS Compatible Peripheral Control Lines
- 8-Bit Bidirectional Data/Control Transfer
- 2 Powerful Interval Timers
- Shift Register for Serial/Parallel and Parallel/Serial Transfers
- Input Data Latching on Peripheral Ports
- Fully Automatic Handshake
- Independent Interrupt Control
- Single +5V Supply

## DESCRIPTION

The 6522 Versatile Interface Adapter (VIA) provides all of the capability of the 6520 Peripheral Adapter. In addition, it offers a pair of powerful interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability over that of the 6520 allows control of bidirectional data transfers between VIAs in a multiple processor system.

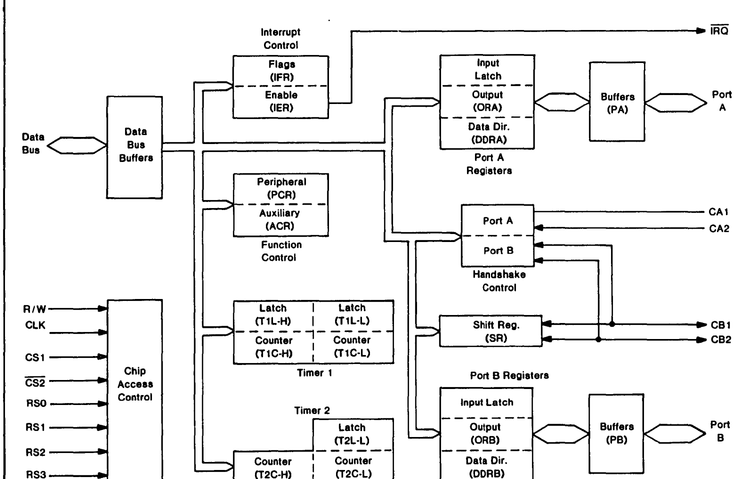
Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each line in these ports can be programmed to act as either an input or an output. Serveral peripheral I/O lines can also be controlled directly from the 6522's internal interval timer, permitting the generation of programmable-frequency square waves and for counting pulses generated externally. Internal registers are organized into an interrupt flag register, an interrupt enable register and a pair of function control registers. This permits easy control of the many features of the device.

## PIN CONFIGURATION

**6522**

| | | | |
|---|---|---|---|
| $V_{SS}$ | 1 | 40 | CA1 |
| PA0 | 2 | 39 | CA2 |
| PA1 | 3 | 38 | RS0 |
| PA2 | 4 | 37 | RS1 |
| PA3 | 5 | 36 | RS2 |
| PA4 | 6 | 35 | RS3 |
| PA5 | 7 | 34 | $\overline{RES}$ |
| PA6 | 8 | 33 | D0 |
| PA7 | 9 | 32 | D1 |
| PB0 | 10 | 31 | D2 |
| PB1 | 11 | 30 | D3 |
| PB2 | 12 | 29 | D4 |
| PB3 | 13 | 28 | D5 |
| PB4 | 14 | 27 | D6 |
| PB5 | 15 | 26 | D7 |
| PB6 | 16 | 25 | Φ2 |
| PB7 | 17 | 24 | CS1 |
| CB1 | 18 | 23 | $\overline{CS2}$ |
| CB2 | 19 | 22 | R/$\overline{W}$ |
| $V_{CC}$ | 20 | 21 | $\overline{IRQ}$ |

## BLOCK DIAGRAM




**Note**
MCS = Ceramic package
MPS = Plastic package

## INTERFACE TO THE PROCESSOR

This section contains a description of the buses and control lines which are used to interface the 6522 to the system processor.

**Phase Two Clock (Φ2).** Data transfers between the 6522 and the system processor take place only while the Phase Two Clock is high. In addition, Φ2 acts as the time base for the various timers and shift registers on the chip.

**Chip Select Lines (CS1, $\overline{CS2}$).** The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected 6522 register will be accessed when CS1 is high and $\overline{CS2}$ is low.

**Register Select Lines (RS0, RS1, RS2, RS3).** The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal 6522 register which is to be accessed. The sixteen possible combinations access the registers shown in Table 1.

**Table 1. Register Select Line Definitions**

| RS3 | RS2 | RS1 | RS0 | Register | Remarks |
|---|---|---|---|---|---|
| L | L | L | L | ORB | |
| L | L | L | H | ORA | Controls Handshake |
| L | L | H | L | DDRB | |
| L | L | H | H | DDRA | |
| L | H | L | L | T1L-L<br>T1C-L | Write Latch<br>Read Counter |
| L | H | L | H | T1C-H | Trigger T1L-L/ T1C-L Transf. |
| L | H | H | L | T1L-L | |
| L | H | H | H | T1L-H | |
| H | L | L | L | T2L-L<br>T2C-L | Write Latch<br>Read Counter |
| H | L | L | H | T2C-H | Triggers T2L-L/ T2C-L Transfer |
| H | L | H | L | SR | |
| H | L | H | H | ACR | |
| H | H | L | L | PCR | |
| H | H | L | H | IFR | |
| H | H | H | L | IER | |
| H | H | H | H | ORA | No Effect on Handshake |

**Read/Write Line (R/W).** The direction of data transfers between the 6522 and the system processor is controlled by the R/W line. If R/W is low, data will be transferred out of the processor into the selected 6522 register (write operation). If R/W is high and the chip is selected, data will be transferred out of the 6522 to the data bus (read operation).

**Data Bus (DBO - DB7).** The 8 bi-directional data bus lines are used to transfer data between the 6522 and the system processor. The internal drivers will remain in the high-impedance state except when the chip is selected (CS1 = 1, $\overline{CS2}$ = 0), Read/Write is high and the Phase Two Clock is high. At this time, the contents of the selected register are placed on the data bus. When the chip is selected, with Read/Write low and Φ2 = 1, the data on the data bus will be transferred into the selected 6522 register.

**Reset ($\overline{RES}$).** The Reset input clears all internal registers (except T1, T2, and SR) to logic 0. This places all peripheral interface lines in the input state, disables the timers, shift register, and interrupts from the chip.

**Interrupt Request ($\overline{IRQ}$).** The Interrupt Request output goes low whenever an internal interrupt flag is set and the correspondeing interrupt enable bit is a logic 1. This output is "open drain" to allow the interrupt request signal to be wire-ORed with other equivalent signals in the system.

**INTERFACE TO THE PERIPHERAL.** This section contains a brief description of the buses and control lines used to drive peripheral devices under control of the MCS6522 registers.

**Peripheral A Port (PAO - PA7).** The Peripheral A port consists of 8 lines which can be individually programmed to act as input or output under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data can be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.

**Peripheral A Control Lines (CA1, CA2).** The two peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A Port input lines. The various modes of operation are controlled by the system processor through the internal control registers. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

**Peripheral B Port (PB0 - PB7).** The Peripheral B port consists of 8 bi-directional lines controlled by an output register and a Data Direction Register in much the same manner as the PA port. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.

**Peripheral B Control Lines (CB1, CB2).** The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.

## OPERATION

This section contains a discussion of the various blocks of logic shown in the block diagram. In addition, the internal operation of the 6522 is described in detail.

### Chip Access Control.

The Chip Access Control contains the necessary logic to detect the chip select condition and to decode the Register Select inputs to allow access to the desired register. In addition, the R/W and $\Phi 2$ signals are utilized to control the direction and timing of data transfers. When writing into the 6522, data is first latched into a data input register during $\Phi 2$. Data is then transferred into the desired internal register during $\overline{\Phi 2}$ - $\overline{\text{Chip Select}}$. This allows the peripheral I/O line to change without "glitching." When the processor reads the 6522, data is transferred from the desired internal register directly onto the Data Bus during $\Phi 2$.

### Port A Registers, Port B Registers

Three registers are used in accessing each of the 8-bit peripheral ports. Each port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and an Input Register (IRA,IRB). When the pin is programmed to act as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A 1 in the Output Register causes the pin to go high, and a 0 causes the pin to go low.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the data on the PA pins. With input latching enabled, IRA will reflect the contents of the Port A prior to setting the CA1 Interrupt Flag (IFR1) by an active transition on CA1.

The IRB register operates in a similar manner. However, for output pins, the corresponding IRB bit will reflect the contents of the Output Register bit instead of the actual pin. This allows proper data to be read into the processor if the output pin is not allowed to go to full voltage. With input latching enabled on Port B, setting CB1 interrupt flag will cause IRB to latch this combination of input data and ORB data until the interrupt flag is cleared.

### Handshake Control

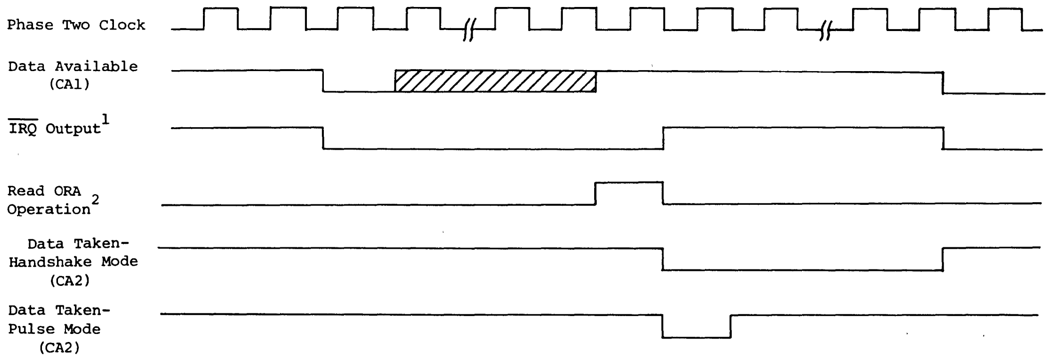
The 6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

**Read Handshake.** Positive control of data transfers from peripheral devices into the system processor can be accomplished using "Read" handshaking. In this case, the peripheral device must generate "Data Ready" to signal the processor that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the 6522, automatic "Read" handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The Data Ready signal will set an internal flag which may either interrupt the processor or be polled by software. The Data Taken signal can be either a pulse or a DC level which is set low by the system processor and cleared by the Data Ready signal. These options are shown in Figure 1 which illustrates the normal Read handshaking sequence.

**Write Handshake.** The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for "Write" handshaking, the processor must generate the "Data Ready"signal (through the 6522) and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the 6522. CA2 or CB2 acts as a Data Ready output in either the DC level or pulse mode and CA1 or CB1 accepts the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 2.

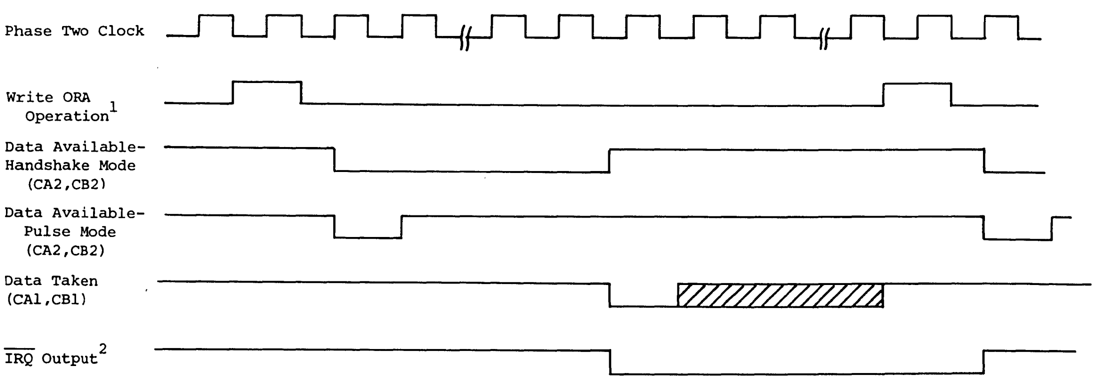
READ HANDSHAKE TIMING SEQUENCE




**NOTES**
1. Signals "data available" to the system processor.
2. R/W = 1, $\overline{CS2}$ = 0, CS1 = 1, RS3 = 0, RS2 = 0, RS1 = 0, RS0 = 1.

**Figure 1.**

WRITE HANDSHAKE TIMING SEQUENCE




**NOTES**
1. R/W = 0, $\overline{CS2}$ = 1, RS3 = 0, RS2 = 0, RS1 = 0, RS0 = 1.
2. Signals "data taken" to the system processor.

**Figure 2.**

## Timer 1 (T1)

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data to be loaded into the counter. After loading, the counter decrements at system clock rate. Upon reaching zero, an interrupt flag will be set, and $\overline{IRQ}$ will go low. The timer will then disable any further interrupts, or automatically transfer the contents of the latches into the counter and continue to decrement. In addition, the timer can be instructed to invert the output signal on a peripheral pin each time it "times-out". Each of these modes is discussed separately below.

**Writing T1.** Operations which take place when writing to each of the four T1 addresses are shown in Table 2.

**Table 2. Writing to T1 Registers**

| RS3 | RS2 | RS1 | RS0 | Operation (R/W = L) |
|---|---|---|---|---|
| L | H | L | L | Write into low order latch. |
| L | H | L | H | Write into high order latch.<br>Write into high order counter.<br>Transfer low order latch into low order counter.<br>Reset T1 interrupt flag. |
| L | H | H | L | Write low order latch. |
| L | H | H | H | Write high order latch.<br>Reset T1 interrupt flag. |

Note that the processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter.

The second set of addresses allows the processor to write into the latch register without affecting the count-down in progress. This is discussed in detail below.

**Reading T1 Registers.** For reading the Timer 1 registers, the four addresses relate directly to the four registers as shown in Table 3.

**Table 3. Reading T1 Registers**

| RS3 | RS2 | RS1 | RS0 | Operation (R/W = H) |
|---|---|---|---|---|
| L | H | L | L | Read T1 low order counter. Reset T1 interrupt flag. |
| L | H | L | H | Read T1 high order counter. |
| L | H | H | L | Read T1 low order latch. |
| L | H | H | H | Read T1 high order latch. |

**Timer 1 Operating Modes.** Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are shown in Table 4.

**Table 4. T1 Operating Modes**

| ACR7 Output Enable | ACR6 "Free-Run" Enable | Mode |
|---|---|---|
| 0 | 0 | Generate a single time-out interrupt each time T1 is loaded. PB7 disabled. |
| 0 | 1 | Generate continuous interrupts. PB7 disabled. |
| 1 | 0 | Generate a single interrupt and an output pulse on PB7 for each T1 load operation. |
| 1 | 1 | Generate continoous interrupts and a square wave output on PB7. |

**One-Shot Mode.** The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7=1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

**NOTE**

**PB7 will act as an output if DDRB7 = 1 or if ACR7 = 1. However, if both DDRB7 and ACR7 are logic 1, PB7 will be controlled from Timer 1 and ORB7 will have no effect on the pin**

In the one-shot mode, writing into the high order latch has no effect on the operation of T1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation. When the processor writes into the high-order counter, the T1 interrupt flag will be cleared, the contents of the low-order latch will be transferred into the low-order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the phase two following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared.

**Free-Running Mode.** The most important advantages associated with the latches in T1 are the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode (ACR6 =1), the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of contining to decrement from zero after a time-out the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described below. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out

All interval timers in the 6500 family devices are "retriggerable." Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period.

**Timer 2 (T2)**

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high-order counter. The counter registers act as a 16-bit counter which decrements at Φ2 rate.

Timer 2 addressing is summarized in Table 5.

**Table 5. T2 Addressing**

| RS3 | RS2 | RS1 | RS0 | R/W = 0 | R/W = 1 |
|---|---|---|---|---|---|
| H | L | L | L | Write T2L-L | Read T2-L<br>Clear Interrupt flag |
| H | L | L | H | Write T2C-H<br>Transfer T2L-L to T2C-L<br>Clear Interrupt flag | Read T2C-H |

**T2 Interval Timer Mode.** As an interval timer, T2 operates in the "one shot" mode similar to T1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H

**T2 Pulse-Counting Mode.** In the pulse-counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessaryu to rewrite T2C-H to allow the interrupt flag to set on subquent down-counting operations. The pulse must be low on the leading edge Φ2.

**Shift Register (SR)**

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling shifting in external devices. The control bits which allow control of the various shift register operating modes are located in the Auxiliary Control Register. These bits can be set and cleared by the system processor to select one of the operating modes.

**SR Input Modes.** Bit 4 of the Auxiliary Control Register selects the input or output modes. There are three input modes and four output modes, differing primarily in the source of the pulses which control the shifting operation. With ACR4 = 0 the input modes are selected by ACR3 and ACR2 as shown in Table 6.

**Table 6. SR Input Mode Selection**

| ACR4 | ACR3 | ACR2 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Shift Register Disabled |
| 0 | 0 | 1 | Shift in under control of Timer 2 |
| 0 | 1 | 0 | Shift in at System Clock Rate |
| 0 | 1 | 1 | Shift in under control of external input pulses |

**SR Output Modes.** The four Shift Register Output Modes are selected by setting the Input/Output Control Bit (ACR4) to a logic 1 and then selecting the specific output mode with ACR3 and ACR2. In each of these modes the Shift Register shifts data out of Bit 7 to the CB2 pin. At the same time the contents of Bit 7 are shifted back into Bit 0. As in the input modes, CB1 is used either as an output to provide shifting pulses out or as an input to allow shifting from an external pulse. The four modes are shown in Table 7.

**Table 7. SR Output Mode Selection**

| ACR4 | ACR3 | ACR2 | Mode |
|---|---|---|---|
| 1 | 0 | 0 | Shift out – Free-running mode.<br>Shift rate controlled by T2. |
| 1 | 0 | 1 | Shift out – Shift rate controlled by T2.<br>Shift pulses generated on CB1. |
| 1 | 1 | 0 | Shift out at system clock rate. |
| 1 | 1 | 1 | Shift out under control of an external pulse. |

**Interrupt Control**

Controlling interrupts within the 6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signalling to the processor that an active interrupt exists. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This bit can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-ORed" with other devices in the system to interrupt the processor.

In the 6522, all the interrupt flags are contained in one register (see Table 8). In addition, Bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows convenient polling of several devices within a system to locate the source of an interrupt.

**Table 8. Interrupt Flags**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Interrupt Flag Register | IRQ | T1 | T2 | CB1 | CB2 | SR | CA1 | CA2 |
| Interrupt Enable Register | Set/ clear control | T1 | T2 | CB1 | CB2 | SR | CA1 | CA2 |

**Interrupt Flag Register (IFR).** The IFR is a read/bit-clear register. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: IRQ = IFR6 X IER6 + IFR5 X IER5 + IFR4 X IER4 + IFR3 X IER3 + IFR2 X IER2 + IFR1 X IER1 + IFR0 X IER0, where X = logical AND, + = logical OR.

Bits six through zero are latches which are set and cleared as shown in Table 9.

IFR Bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts.

**Interrupt Enable Register (IER).** For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If Bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in Bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

**Table 9. Bits 6–0 of IFR**

| Bit # | Set by | Cleared by |
|---|---|---|
| 0 | Active transition of the signal on the CA2 pin. | Reading or writing the A Port Output Register (ORA) using address 0001. |
| 1 | Active transition of the signal on the CA1 pin. | Reading or writing the A Port Output Reigster (ORA) using address 0001. |
| 2 | Completion of eight shifts | Reading or writing the Shift Register. |
| 3 | Active transition of the signal on the CB2 pin. | Reading or writing the B Port Output Register. |
| 4 | Active transition of the signal on the CB1 pin. | Reading or writing the B Port Output Register |
| 5 | Time-out of Timer 2. | Reading T2 low order counter. Writing T2 high order counter. |
| 6 | Time-out of Timer 1. | Reading T1 low order counter. Writing T1 high order latch. |

Setting selected bits in the IER is accomplished by writing to the same address with Bit 7 in the data word set to a logic 1. In this case, each 1 in Bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows convenient control of interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/W line high. Bit 7 will be read as a logic 0.

**Function Control**

Control of the various functions and operating modes within the 6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the interval timers (T1, T2), and the Shift Register (SR).

**Peripheral Control Register (PCR).** The Peripheral Control Register is organized as shown in Figure 3.

**Figure 3. PCR Organization**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | CB2 Control | | | CB1 Control | CA2 Control | | | CA1 Control |

Each of these functions is discussed in detail below.

**1. CA1 Control**

Bit 0 of the PCR selects the active transition of the input signal applied to the CA1 interrupt input pin. If this bit is a logic 0, the CA1 interrupt flag will be set by a negative transition (high to low) of the signal on the CA1 pin. If PCR0 is a logic 1, the flag will be set by a positive transition.

**2. CA2 Control**

The CA2 pin can be programmed to act as an interrupt input or as a peripheral control output. As an input, CA2 operates in two modes, differing primarily in the methods available for resetting the interrupt flag. Each of these two input modes can operate with either a positive or a negative active transition as described above for CA1.

In the output mode, the CA2 pin combines the operations performed on the CA2 and CB2 pins of the 6520. This added flexibility allows the processor to perform a normal "write" handshaking in a system which uses CB1 and CB2 for the serial operations described above. The CA2 operating modes are selected as shown in Table 10.

In the independent input mode, writing or reading the ORA register has no effect on the CA2 interrupt flag. This flag must be cleared by writing a logic 1 into the appropriate IFR bit. This mode allows the processor to handle interrupts which are independent of any operations taking place on the peripheral I/O ports.

**3. CB1 Control**

Control of the active transition of the CB1 input signal operates in exactly the same manner as that described above for CA1. If the Shift Register function has been enabled, CB1 will act as an input or output for the shift register clock signals. In this mode the CB1 interrupt flag will still respond to the selected transition of the signal on the CB1 pin.

**Table 10. CA2 Operating Mode Selection**

| PCR3 | PCR2 | PCR1 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | **Input mode.** Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register. |
| 0 | 0 | 1 | **Independent interrupt input mode.** Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag. |
| 0 | 1 | 0 | **Input mode.** Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear the IFR0 with a read or write of the Peripheral A Output Register. |
| 0 | 1 | 1 | **Independent interrupt input mode.** Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag. |
| 1 | 0 | 0 | **Handshake output mode.** Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1. |
| 1 | 0 | 1 | **Pulse Output mode.** CA2 goes low for one cycle following a read or write of the Peripheral A Output Register. |
| 1 | 1 | 0 | **Manual output mode.** The CA2 output is held low in this mode. |
| 1 | 1 | 1 | **Manual output mode.** The CA2 output is held high in this mode. |

**4. CB2 Control**
With the serial port disabled, operation of the CB2 pin is a function of the three high-order bits of the PCR. The CB2 modes are very similar to those described previously for CA2, and are selected as shown in Table 11.

**Table 11. CB2 Operating Mode Selection**

| PCR7 | PCR6 | PCR5 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | **Interrupt input mode.** Set CB2 interrupt flag (IFR3) on a negative transition of the CB2 input signal. Clear IFR3 on a read or write of the Peripheral B Output Register. |
| 0 | 0 | 1 | **Independent interrupt input mode.** Set IFR3 on a negative transition of the CB2 input signal. Reading or writing ORB does not clear the CA2 interrupt flag. |
| 0 | 1 | 0 | **Input mode.** Set CB2 interrupt flag on a positive transition of the CB2 input signal. Clear the CB2 interrupt flag on a read or write of ORB. |
| 0 | 1 | 1 | **Independent input mode.** Set IFR3 on a positive transition of the CB2 input signal. Reading or writing ORB does not clear the CB2 interrupt flag. |
| 1 | 0 | 0 | **Handshake output mode.** Set CB2 low on a write ORB operation. Reset CB2 high with an active transition of the CB1 input signal. |
| 1 | 0 | 1 | **Pulse output mode.** Set CB2 low for one cycle following a write ORB operation. |
| 1 | 1 | 0 | **Manual output mode.** The CB2 output is held low in this mode. |
| 1 | 1 | 1 | **Manual output mode.** The CB2 output is held high in this mode. |

**Auxiliary Control Register (ACR).** Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference. ARC organization is shown in Figure 4.

**Figure 4. ACR Organization**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | T1 Control | | T2 Control | Shift Register Control | | | PB Latch Enable | PA Latch Enable |

Each of these functions is described in detail below.

**1. PA Latch Enable**
The 6522 provides input latching on both the PS and PB ports. In this mode, the data present on the peripheral A input pins will be latched within the chip when the CA1 interrupt flag is set. Reading the PA port will result in these latches being transferred into the processor. As long as the CA1 interrupt flag is set, the data on the peripheral pins can change without affecting the data in the latches. This input latching can be used with any of the CA2 input or output modes.

It is important to note that on the PA port, the processor always reads the data on the peripheral pins (as reflected in the latches). For output pins, the processor still reads the latches. This may or may not reflect the data currently in the ORA. Proper system operation requires careful planning on the part of the system designer if input latching is combined with output pins on the peripheral ports.

Input latching is enabled by setting Bit 0 in the Auxiliary Control Register to a logic 1. As long as this bit is a 0, the latches will directly reflect the data on the pins.

**2. PB Latch Enable**
Input latching on the PB port is controlled in the same manner as that described for the PS port. However, with the Peripheral B port, the input latch will store either the voltage on the pin or the contents of the Output Register (ORB), depending on whether the pin is programmed to act as an input or an output. As with the PA port, the processor always reads the input latches.

**3. Shift Register (SR) Control**
The Shift Register operating mode is selected as shown in Table 12.

**Table 12. SR Operating Mode Selection**

| ACR4 | ACR3 | ACR2 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Shift Register Disabled. |
| 0 | 0 | 1 | Shift in Under Control of Timer 2. |
| 0 | 1 | 0 | Shift in Under Control of System Clock. |
| 0 | 1 | 1 | Shift in Under Control of External Clock Pulses. |
| 1 | 0 | 0 | Free-running Output at Rate Determined by Timer 2. |
| 1 | 0 | 1 | Shift Out Under Control of Timer 2. |
| 1 | 1 | 0 | Shift Out Under Control of the System Clock. |
| 1 | 1 | 1 | Shift Out Under Control of External Clock Pulses. |

**4. T2 Control**
If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

**5. T1 Control**
Timer 1 operates in the one-shot or free-running mode with the PB7 output control enabled or disabled. These modes are selected as shown in Table 13.

**Table 13. T1 Mode Selection**

| ACR7 | ACR6 | Mode |
|---|---|---|
| 0 | 0 | One-shot Mode- Output to PB7 Disabled. |
| 0 | 1 | Free-running Mode- Output to PB7 Disabled. |
| 1 | 0 | One-shot Mode- Output to PB7 Enabled. |
| 1 | 1 | Free-running Mode. Output to PB7 Enabled. |

**ABSOLUTE MAXIMUM RATINGS**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | −0.3 to +7.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

**CAUTION**
*This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.*

**DC CHARACTERISTICS** $V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = 0, $T_A$ = 0 to +70 °C (unless otherwise noted)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage (normal operation) | +2.4 | | $V_{CC}$ | Vdc | |
| $V_{IL}$ | Input Low Voltage (normal operation) | −0.3 | | +0.4 | Vdc | |
| $I_{IN}$ | Input Leakage Current | | ±1.0 | ±2.5 | μAdc | $V_{in}$ = 0 to 5 Vdc<br>R/W, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, Φ 2 |
| $I_{TSI}$ | Off-State Input Current | | ±2.0 | ±10 | μAdc | $V_{in}$ = .4 to 2.4 V<br>$V_{CC}$ = Max, D0 to D7 |
| $I_{IH}$ | Input High Current | −100 | −250 | | μAdc | $V_{IH}$ = 2.4 V<br>PA0 - PA7, CA2, PB0 - PB7, CB1, CB2 |
| $I_{IL}$ | Input Low Current | | −1.0 | −1.6 | mAdc | $V_{IL}$ = 0.4 Vdc<br>PA0 - PA7, CA2, PB0 - PB7, CB1, CB2 |
| $V_{CH}$ | Output High Voltage | 2.4 | | | Vdc | $V_{CC}$ = min, $I_{load}$ = −100 μAdc<br>PA0 - PA7, CA2, PB0 - PB7, CB1, CB2 |
| $V_{OL}$ | Output Low Voltage | | | +0.4 | Vdc | $V_{CC}$ = min, $I_{load}$ = 1.6 mAdc |
| $I_{OH}$ | Output High Current (sourcing) | −100<br>−3.0 | −1000<br>−5.0 | | μAdc<br>mAdc | $V_{OH}$ = 2.4 V<br>$V_{OH}$ = 1.5 V, PB0 - PB7, CB1, CB2 |
| $I_{OL}$ | Output Low Current (sinking) | 1.6 | | | mAdc | $V_{OL}$ = 0.4 Vdc. |
| $I_{off}$ | Output Leakage Current (off state) | | 1.0 | 10 | μAdc | $\overline{IRQ}$ |
| $C_{in}$ | Input Capacitance | | | 7.0<br>10<br>20 | pF<br>pF<br>pF | $T_A$ = 25 °C, f = 1 Mhz<br>R/W, $\overline{RES}$, RE0, RS1, RS2, RS3, CS1, CS2<br>D0 - D7, PA0 - PA7, CA2, PB0 - PB7, CB1, CB2<br>Φ 2 input |
| $C_{out}$ | Ouput Capacitance | | | 10 | pF | $T_A$ = 25 °C, f = 1 Mhz |
| $P_d$ | Power Dissipation | | | 1000 | MW | |

## READ TIMING CHARACTERISTICS

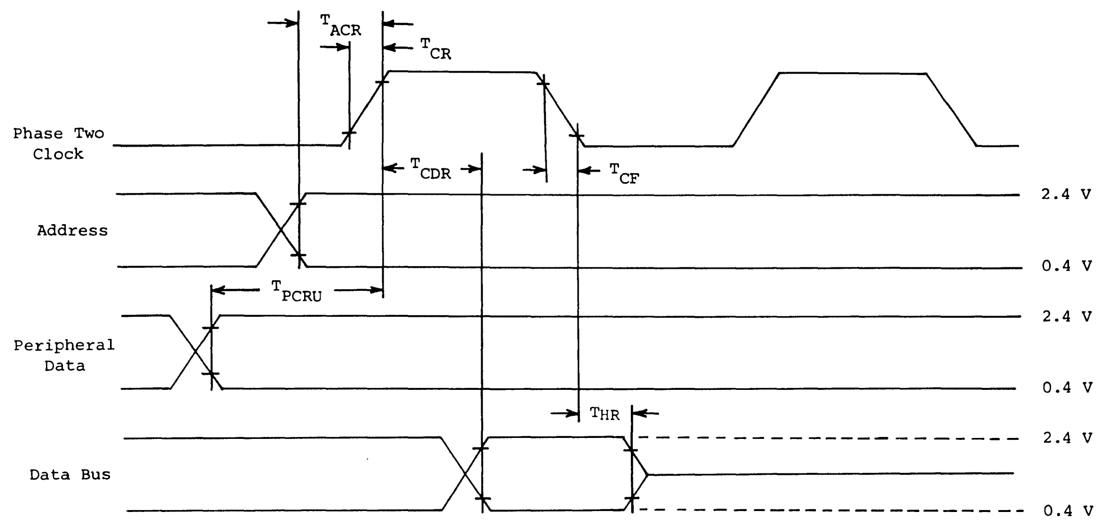



**Figure 21.**

## WRITE TIMING CHARACTERISTICS

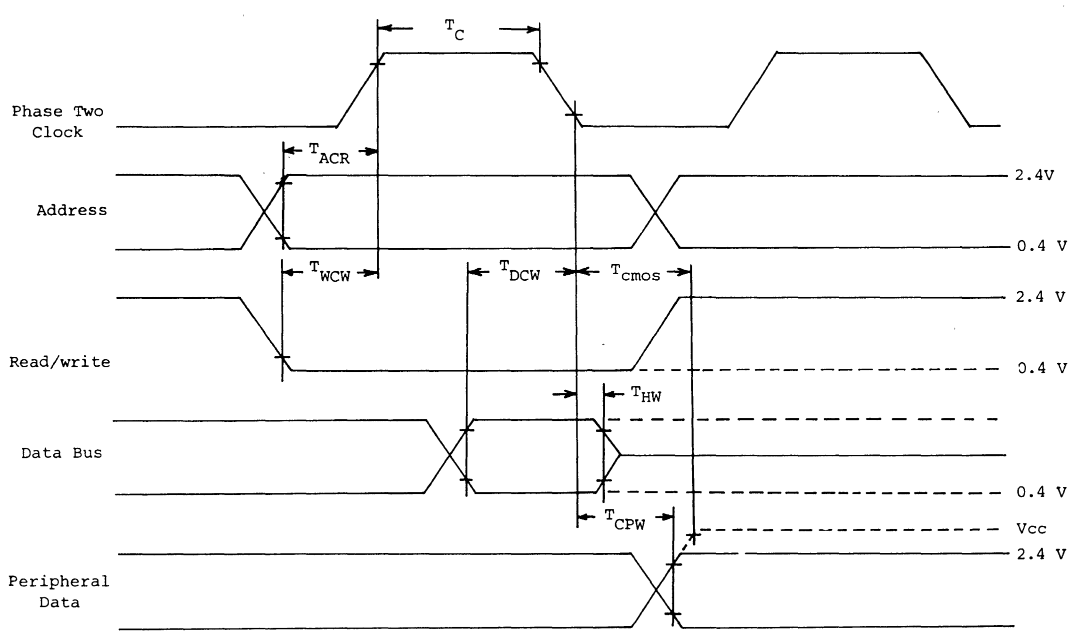



**Figure 22.**

## I/O TIMING CHARACTERISTICS

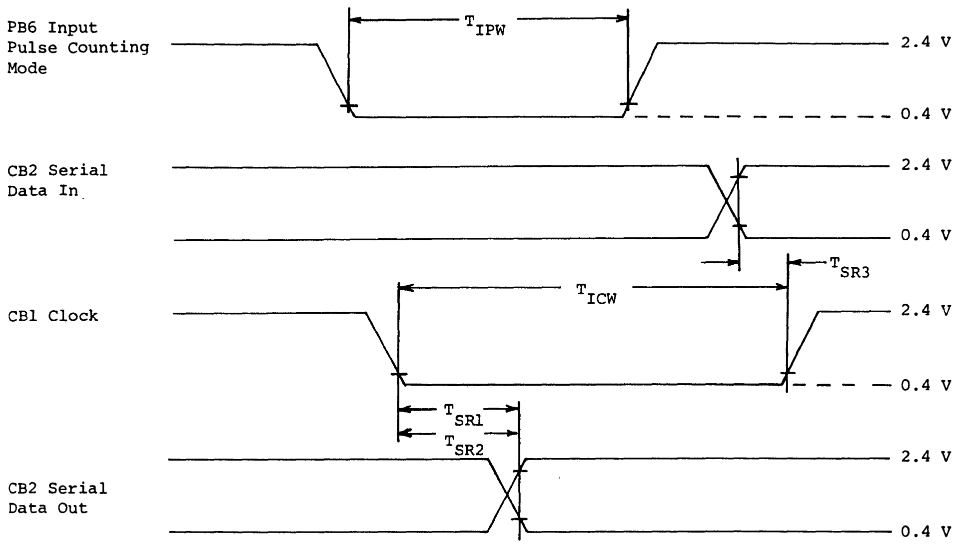



**Figure 23.**

**AC CHARACTERISTICS** TA = 0°C to +17°C, $V_{CC}$ = 5V ± 5% (unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{ACR}$ | READ CYCLE (Figure 22, loading 130 pF and one TTL load)<br>Delay Time, Address Valid to Clock Positive Transition | 180 | | | nS |
| $T_{CDR}$ | Delay Time, Clock Positive Transition to Data Valid on Bus | | | 395 | nS |
| $T_{PCR}$ | Peripheral Data Setup Time | 300 | | | nS |
| $T_{HR}$ | Data Bus Hold Time | 10 | | | nS |
| $T_{RC}$<br>$T_{RF}$ | Rise and Fall Time For Clock Input | | | 25 | nS |
| $T_C$ | WRITE CYCLE (Figure 22)<br>Enable Pulse Width | 0.47 | | 25 | |
| $T_{ACW}$ | Delay Time, Address Valid to Clock Positive Transition | 180 | | | nS |
| $T_{DCW}$ | Delay Time, Data Valid to Clock Negative Transition | 300 | | | nS |
| $T_{WCW}$ | Delay Time, Read/Write Negative Transition to Clock Positive Transition | 180 | | | nS |
| $T_{HW}$ | Data Bus Hold Time | 10 | | | nS |
| $T_{CPW}$ | Delay Time, Enable Negative Transition to Peripheral Data Valid | | | 1.0 | µS |
| $T_{CMOS}$ | Delay Time, Clock Negative Transition to Peripheral Data Valid CMOS ($V_{CC}$ – 30%) | | | 2.0 | µS |

**Peripheral Interface Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{RF}$ | Rise and Fall Time For CA1, CB1, CA2 and CB2 Input Signals. | | | 1.0 | μS |
| $T_{CA2}$ | Delay Time, Clock Negative Transition to CA2 Negative Transition (Read Handshake or Pulse Mode). | | | 1.0 | μS |
| $T_{RS1}$ | Delay Time, Clock Negative Transition to CA2 Positive Transition (Pulse Mode). | | | 1.0 | μS |
| $T_{RS2}$ | Delay Time, CA1 Active Transition to CA2 Positive Transition (Handshake Mode). | | | 2.0 | μS |
| $T_{WHS}$ | Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (Write Handshake). | | | 1.0 | μS |
| $T_{DC}$ | Delay Time, Peripheral Data Valid to CB2 Negative Transition. | 0 | | 1.5 | μS |
| $T_{RS3}$ | Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (Pulse Mode). | | | 1.0 | μS |
| $T_{RS4}$ | Delay Time, CB1 Active Transition to CA2 or CB2 Positive Transition (Handshake Mode). | | | 2.0 | μS |
| $T_{IL}$ | Delay Time, Peripheral Data Valid to CA1 or CB1 Active Transition (Input Latching). | 300 | | | nS |
| $T_{SR1}$ | Delay Time, CB1 Negative Transition to CB2 Data Valid (Internal SR Clock, Shift Out). | | | 300 | nS |
| $T_{SR2}$ | Delay Time, Negative Transition of CB1 Input Clock to CB2 Data Valid (External Clock, Shift Out). | | | 300 | nS |
| $T_{SR3}$ | Delay Time, CB2 Data Valid to Positive Transition of CB1 Clock (Shift In, Internal or External Clock). | | | 300 | nS |
| $T_{IPW}$ | Pulse Width — PB6 Input Pulse | 2 | | | μS |
| $T_{ICW}$ | Pulse Width — CB1 Input Clock | 2 | | | μS |
| $I_{IPS}$ | Pulse Spacing — PB6 Input Pulse | 2 | | | μS |
| $I_{ICS}$ | Pulse Spacing — CB1 Input Pulse | 2 | | | μS |

# 6523 Tri-Port Interface

- 24 Individually Programmable I/O Lines
- Completely Static Operation
- Two TTL Drive Capability
- 6 Directly Addressable Registers
- 1 MHz, 2 MHz

## DESCRIPTION

The 6523 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. The 6523 can provide 24 individually programmable I/O lines.

## 6523 ADDRESSING

| 6523 Registers (Direct Addressing) | | |
|---|---|---|
| *000 | R0 | PRA — Port Register A |
| 001 | R1 | PRB — Port Register B |
| 010 | R2 | PRC — Port Register C |
| 011 | R3 | DDRA — Data Direction Register A |
| 100 | R4 | DDRB — Data Direction Register B |
| 101 | R5 | DDRC — Data Direction Register C |
| 110 | | Illegal State |
| 111 | | Illegal State |

**Note**
*RS2, RS1, RS0 respectively

## ORDER NUMBER

MXS 6525 ___

Frequency Range
No Suffix = 1 MHz
A = 2 MHz
B = 3 MHz

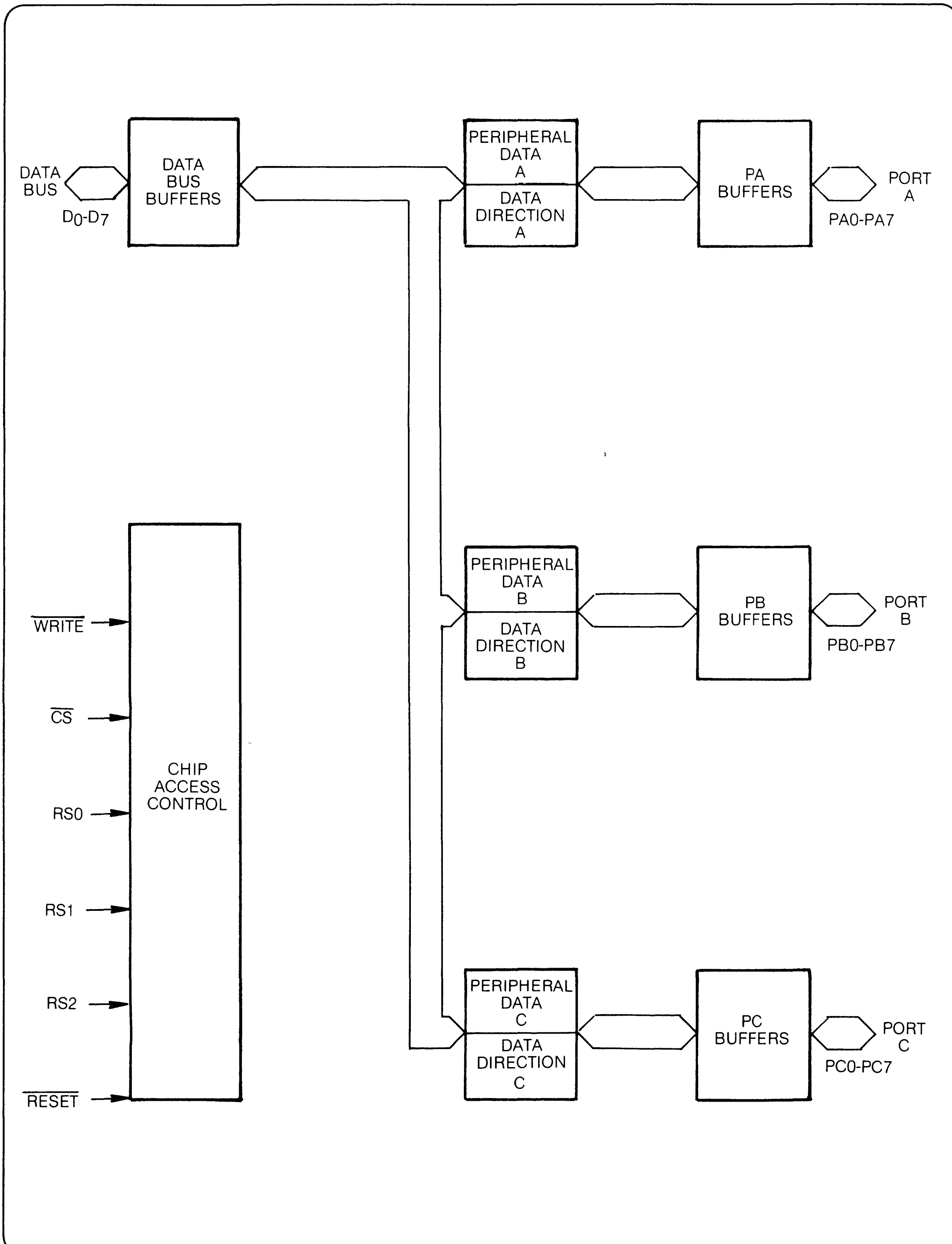
Package Designator
C = Ceramic
P = Plastic

## PIN CONFIGURATION

**6523**

| | | | |
|---|---|---|---|
| $V_{SS}$ | 1 | 40 | DB7 |
| PA0 | 2 | 39 | DB6 |
| PA1 | 3 | 38 | DB5 |
| PA2 | 4 | 37 | DB4 |
| PA3 | 5 | 36 | DB3 |
| PA4 | 6 | 35 | DB2 |
| PA5 | 7 | 34 | DB1 |
| PA6 | 8 | 33 | DB0 |
| PA7 | 9 | 32 | PC7 |
| PB0 | 10 | 31 | PC6 |
| PB1 | 11 | 30 | PC5 |
| PB2 | 12 | 29 | PC4 |
| PB3 | 13 | 28 | PC3 |
| PB4 | 14 | 27 | PC2 |
| PB5 | 15 | 26 | PC1 |
| PB6 | 16 | 25 | PC0 |
| PB7 | 17 | 24 | RS0 |
| $\overline{CS}$ | 18 | 23 | RS1 |
| $\overline{WRITE}$ | 19 | 22 | RS2 |
| $V_{DD}$ | 20 | 21 | $\overline{RST}$ |

## INTERNAL ARCHITECTURE



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | −0.3 to +7.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

## CAUTION

*This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.*

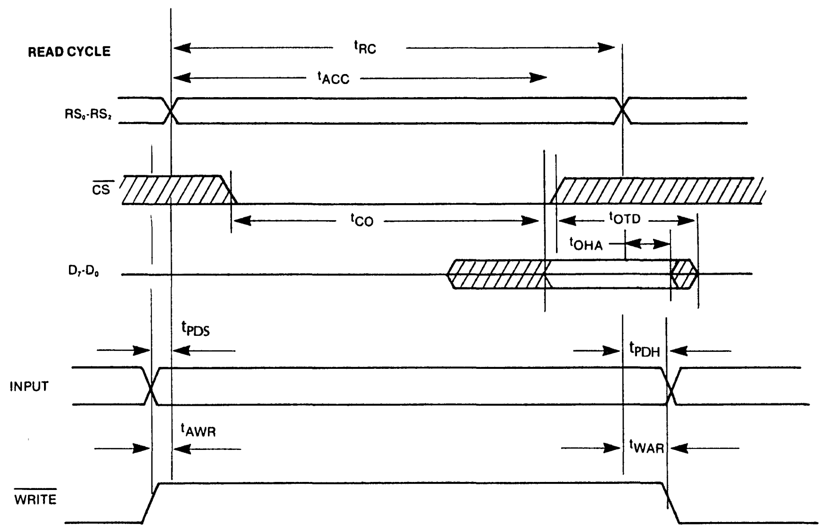
## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = 0 V, $T_A$ = 0° to 70°C)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage (Normal Operating Levels) | +2.0 | | $V_{CC}$ | Vdc |
| $V_{IL}$ | Input Low Voltage (Normal Operating Levels) | −0.3 | | +.8 | Vdc |
| $I_{IN}$ | Input Leakage Current<br>$V_{IN}$ = 0 to 5.0 Vdc<br>$\overline{\text{WRITE}}$ $\overline{\text{RST}}$, $\overline{\text{CS}}$, $RS_0$-$RS_2$ | 0 | ±1.0 | ±2.5 | μAdc |
| $I_{TSI}$ | Three-State (Off State Input Current)<br>($V_{in}$ = 0.4 to 2.4 Vdc, $V_{CC}$ = max)<br>DO-D7 | 0 | ±2.0 | ±10 | μAdc |
| $V_{OH}$ | Output High Voltage<br>($V_{CC}$ = min, Load = 200 μAdc) | 2.4 | 3.5 | $V_{CC}$ | Vdc |
| $V_{OL}$ | Output Low Voltage<br>($V_{CC}$ = min, Load = 3.2 mAdc) | $V_{SS}$ | .2 | +0.4 | Vdc |
| $I_{OH}$ | Output High Current (Sourcing)<br>($V_{OH}$ = 2.4 Vdc) | −200 | −1000 | | μAdc |
| $I_{OL}$ | Output Low Current (Sinking)<br>($V_{OL}$ = 0.4 Vdc) | 3.2 | | | mAdc |
| $I_{CC}$ | Supply Current | | 55 | 100 | mA |
| $C_{in}$ | Input Capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz)<br>D0-D7, PA0-PA7, PB0-PB7, PC0-PC7,<br>$\overline{\text{WRITE}}$ $\overline{\text{RST}}$, $RS_0$-$RS_2$, $\overline{\text{CS}}$ | | 7 | 10 | pF |
| $C_{out}$ | Output Capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | | 7 | 10 | pF |

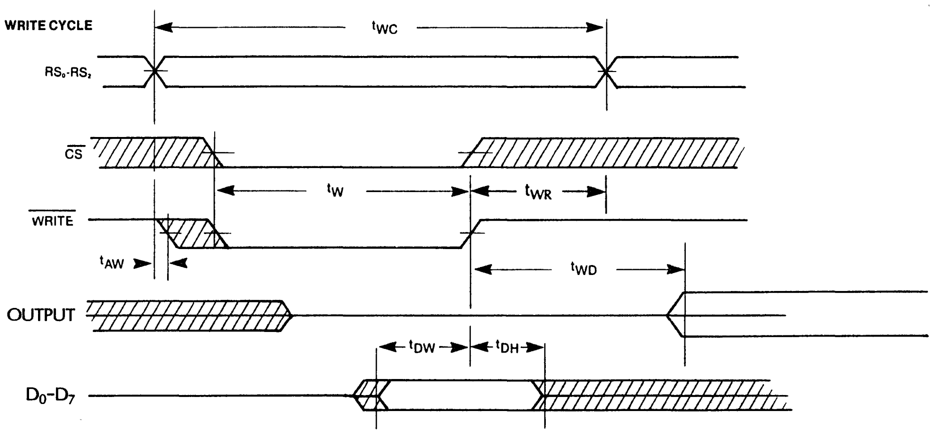
**Note**
Negative sign indicates outward current flow, positive indicates inward flow.

## TIMING DIAGRAMS

### READ CYCLE




### WRITE CYCLE



**WRITE CYCLE**

| Symbol | Parameter | 1 MHz Min | 1 MHz Max | 2 MHz Min | 2 MHz Max | Units |
|---|---|---|---|---|---|---|
| $t_{WS}$ | Write Cycle Time | 700 | | 350 | | μS |
| $t_{AW}$ | Address to write set-up time | 0 | | 0 | | μS |
| $t_W$ | Write Pulse Width | 450 | | 225 | | μS |
| $t_{WR}$ | Write Release Time | 250 | | 150 | | μS |
| $t_{DW}$ | Data to Write Overlap | 150 | | 75 | | μS |
| $t_{DH}$ | Data Hold | 50 | | 40 | | μS |
| $t_{WD}$ | Write to Peripheral Output | 1000 | | 500 | | μS |

**READ CYCLE**

| Symbol | Parameter | 1 MHz Min | 1 MHz Max | 2 MHz Min | 2 MHz Max | Units |
|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 700 | | 350 | | μS |
| $t_{ACC}$ | Access time | 450 | | 225 | | μS |
| $t_{CO}$ | Chip Select to Output Valid | 450 | | 225 | | μS |
| $t_{OTD}$ | Chip Deselected to Output Off | 0 | 100 | 0 | 100 | μS |
| $t_{OHA}$ | Output Hold From Address Change | 50 | | 50 | | μS |
| $t_{PDS}$ | Peripheral Data Setup Time | 120 | | 60 | | μS |
| $t_{PDH}$ | Peripheral Data Hold Time | 0 | | 0 | | μS |
| $t_{AWR}$ | Write to Address Setup | 0 | | 0 | | μS |
| $t_{WAR}$ | Write to Address Hold | 0 | | 0 | | μS |

**commodore semiconductor group**

**NMOS**

PRELIMINARY

# 6525 Tri-Port Interface

- **24 Individually Programmable I/O Lines or 16 I/O Lines, 2 Handshake Lines and 5 Interrupt Inputs**
- **Priority or Non-Priority Interrupts**
- **Automatic Handshaking**
- **Completely Static Operation**
- **Two TTL Drive Capability**
- **8 Directly Addressable Registers**
- **1 MHz, 2 MHz and 3 MHz Operation**

## DESCRIPTION

The 6525 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It combines two dedicated 8-bit I/O ports with a third 8-bit port programmable for either normal I/O operation or priority interrupt/handshaking control. Depending on the mode selected, the 6525 can provide 24 individually programmable I/O lines or 16 I/O lines, 2 handshake lines and 5 priority interrupt inputs.

## 6525 ADDRESSING

| 6525 Registers (Direct Addressing) | | |
|---|---|---|
| *000 | R0 | PRA – Port Register A |
| 001 | R1 | PRB – Port Register B |
| 010 | R2 | PRC – Port Register C |
| 011 | R3 | DDRA – Data Direction Register A |
| 100 | R4 | DDRB – Data Direction Register B |
| 101 | R5 | DDRC – Data Direction Register C/ Interrupt Mask Register |
| 110 | R6 | CR – Control Register |
| 111 | R7 | AIR – Active Interrupt Register |

**Note**
*RS2, RS1, RS0 respectively

## ORDER NUMBER

**MXS 6525 ___**

Frequency Range
No Suffix = 1 MHz
A = 2 MHz
B = 3 MHz

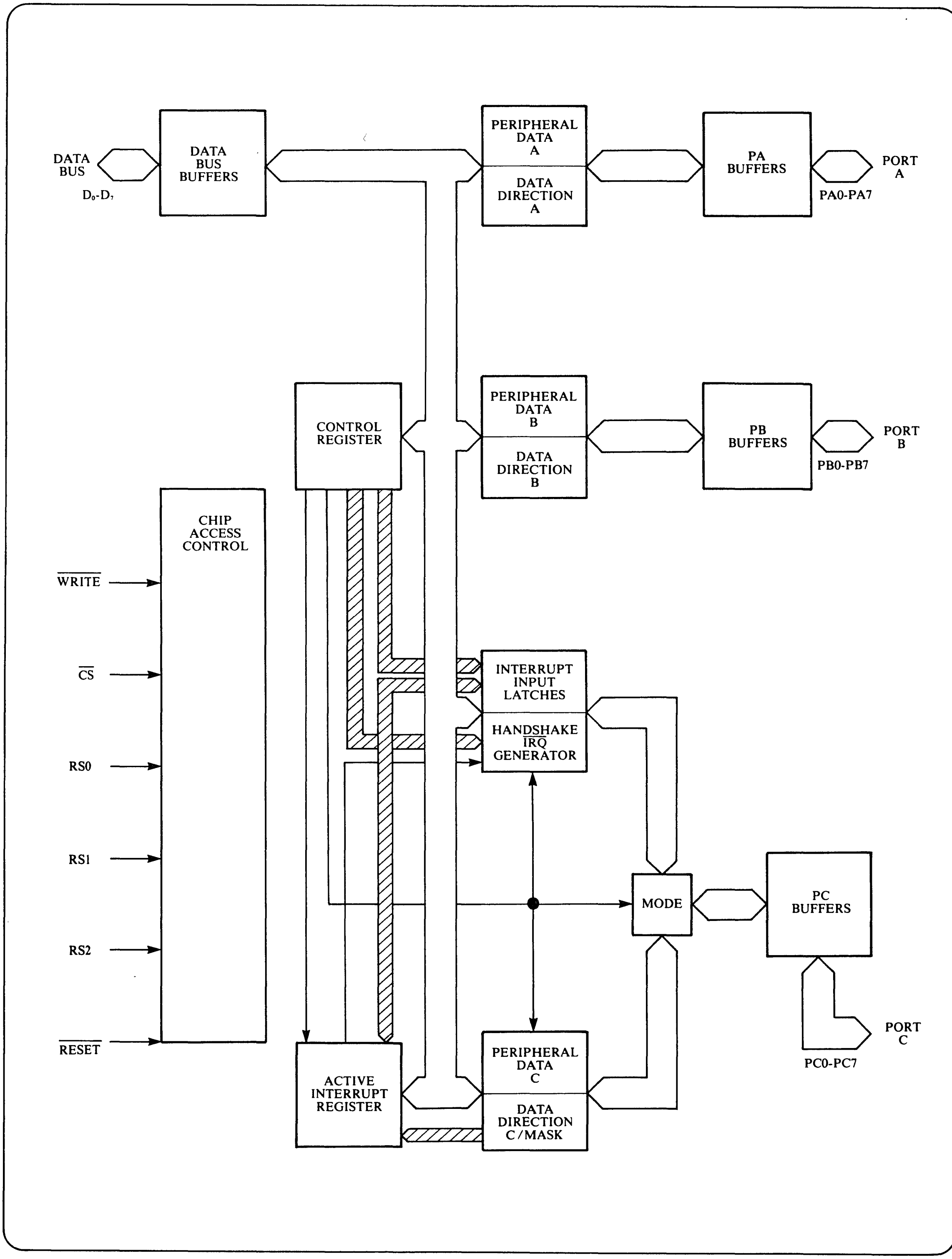
Package Designator
C = Ceramic
P = Plastic

## PIN CONFIGURATION

**6525**

| | | | |
|---|---|---|---|
| $V_{SS}$ | 1 | 40 | DB7 |
| PA0 | 2 | 39 | DB6 |
| PA1 | 3 | 38 | DB5 |
| PA2 | 4 | 37 | DB4 |
| PA3 | 5 | 36 | DB3 |
| PA4 | 6 | 35 | DB2 |
| PA5 | 7 | 34 | DB1 |
| PA6 | 8 | 33 | DB0 |
| PA7 | 9 | 32 | PC7 |
| PB0 | 10 | 31 | PC6 |
| PB1 | 11 | 30 | PC5 |
| PB2 | 12 | 29 | PC4 |
| PB3 | 13 | 28 | PC3 |
| PB4 | 14 | 27 | PC2 |
| PB5 | 15 | 26 | PC1 |
| PB6 | 16 | 25 | PC0 |
| PB7 | 17 | 24 | RS0 |
| $\overline{CS}$ | 18 | 23 | RS1 |
| $\overline{WRITE}$ | 19 | 22 | RS2 |
| $V_{DD}$ | 20 | 21 | $\overline{RST}$ |

## 6525 INTERNAL ARCHITECTURE



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | −0.3 to +7.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

### CAUTION

*This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.*

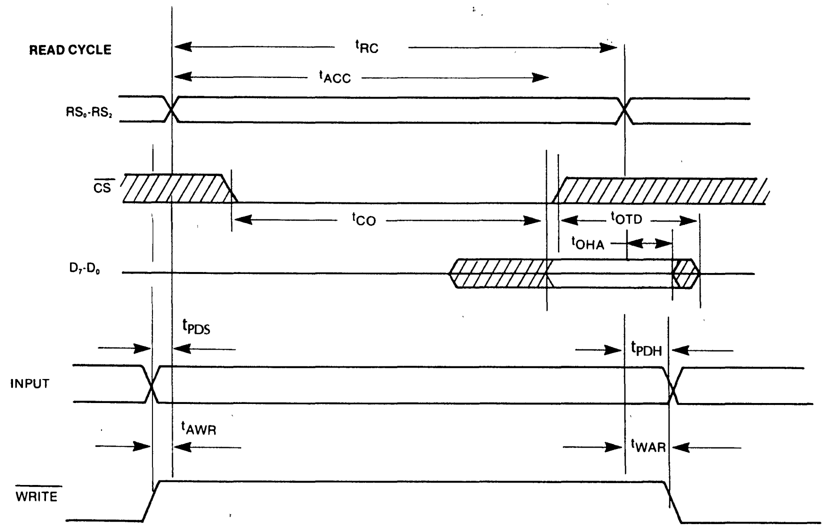
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = 0 V, $T_A$ = 0° to 70°C)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage (Normal Operating Levels) | +2.0 | 1.5 | $V_{CC}$ | Vdc |
| $V_{IL}$ | Input Low Voltage (Normal Operating Levels) | −0.3 | 1.2 | +.8 | Vdc |
| $I_{IN}$ | Input Leakage Current<br>$V_{IN}$ = 0 to 5.0 Vdc<br>$\overline{\text{WRITE}}$ $\overline{\text{RST}}$, $\overline{\text{CS}}$, $RS_0$-$RS_2$ | 0 | ±1.0 | ±2.5 | μAdc |
| $I_{TSI}$ | Three-State (Off State Input Current)<br>($V_{in}$ = 0.4 to 2.4 Vdc, $V_{CC}$ = max)<br>D0-D7, PA0-PA7, PB0-PB7, PC0-PC7 | 0 | ±2.0 | ±10 | μAdc |
| $V_{OH}$ | Output High Voltage<br>($V_{CC}$ = min, Load = 200 μAdc) | 2.4 | 3.5 | $V_{CC}$ | Vdc |
| $V_{OL}$ | Output Low Voltage<br>($V_{CC}$ = min, Load = 3.2 mAdc) | $V_{SS}$ | 0.2 | +0.4 | Vdc |
| $I_{OH}$ | Output High Current (Sourcing)<br>($V_{OH}$ = 2.4 Vdc) | −200 | −1000 | | μAdc |
| $I_{OL}$ | Output Low Current (Sinking)<br>($V_{OL}$ = 0.4 Vdc) | 3.2 | | | mAdc |
| $I_{CC}$ | Supply Current | | 55 | 100 | mA |
| $C_{in}$ | Input Capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz)<br>D0-D7, PA0-PA7, PB0-PB7, PC0-PC7,<br>$\overline{\text{WRITE}}$ $\overline{\text{RST}}$, $RS_0$-$RS_2$, $\overline{\text{CS}}$ | | 7 | 10 | pF |
| $C_{out}$ | Output Capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | | 7 | 10 | pF |
| $I_{IL}$ | Input Low Current<br>($V_{IL}$ = 0.4 Vdc) | | −2.0 | −3.2 | mA |
| $I_{IH}$ | Input High Current<br>($V_{IH}$ = 2.4 Vdc) | −200 | −500 | | μA |

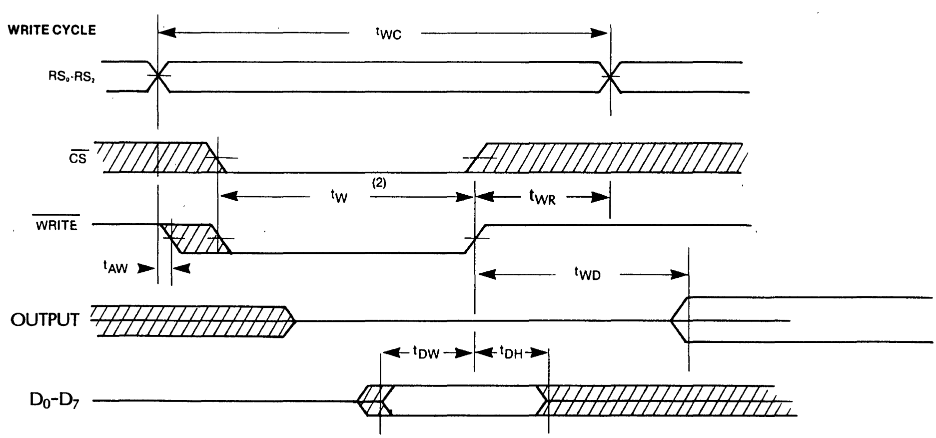
**Note**
Negative sign indicates outward current flow, positive indicates inward flow.

## TIMING DIAGRAMS

### READ CYCLE




### WRITE CYCLE



**WRITE CYCLE**

| Symbol | Parameter | 1 MHz | | 2 MHz | | 3 MHz | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_W$ | Write Cycle Time | 700 | | 350 | | 220 | | nS |
| $t_{AW}$ | Address to write set-up time | 0 | | 0 | | 0 | | nS |
| $t_{WP}$ | Write Pulse Width | 450 | | 225 | | 160 | | nS |
| $t_{WR}$ | Write Release Time | 0 | | 0 | | 0 | | nS |
| $t_{DW}$ | Data to Write Overlap | 150 | | 75 | | 75 | | nS |
| $t_{DH}$ | Data Hold | 50 | | 40 | | 40 | | nS |
| $t_{WD}$ | Write to Peripheral Output | 1000 | | 500 | | 330 | | nS |

**READ CYCLE**

| Symbol | Parameter | 1 MHz | | 2 MHz | | 3 MHz | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 700 | | 350 | | 220 | | nS |
| $t_{ACC}$ | Access time | 450 | | 225 | | 160 | | nS |
| $t_{CO}$ | Chip Select to Output Valid | 450 | | 225 | | 160 | | nS |
| $t_{OTD}$ | Chip Deselected to Output Off | 0 | 100 | 0 | 100 | 0 | 100 | nS |
| $t_{OHA}$ | Output Hold From Address Change | 50 | | 50 | | 50 | | nS |
| $t_{PDS}$ | Peripheral Data Before Read | 120 | | 60 | | 40 | | nS |
| $t_{PDH}$ | Peripheral Data After Read | 0 | | 0 | | 0 | | nS |
| $t_{AWR}$ | Write to Address Setup | 0 | | 0 | | 0 | | nS |
| $t_{WAR}$ | Write to Address Hold | 0 | | 0 | | 0 | | nS |

**6525 Control Registers**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| CR | $CB_1$ | $CB_0$ | $CA_1$ | $CA_0$ | $IE_4$ | $IE_3$ | IP | MC |
| AIR | | | | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
| DDRC When MC = 1 | | | | $M_4$ | $M_3$ | $M_2$ | $M_1$ | $M_0$ |
| PRC When MC = 1 | CB | CA | $\overline{IRQ}$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

## CA, CB Functional Description

### CA OUTPUT MODES

| $CA_1$ | $CA_0$ | Mode | Description |
|---|---|---|---|
| 0 | 0 | "Handshake" on Read | CA is set high on an active transition of the $I_3$ interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor. |
| 0 | 1 | Pulse Output | CA goes low for 1 $\mu$S after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken. |
| 1 | 0 | Manual Output | CA set low. |
| 1 | 1 | Manual Output | CA set high. |

### CB OUTPUT MODES

| $CB_1$ | $CB_0$ | Mode | Description |
|---|---|---|---|
| 0 | 0 | "Handshake" on Write | CB is set low on microprocessor "Write B Data" operation and is set high by an active transition of the $I_4$ interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device. |
| 0 | 1 | Pulse Output | CB goes low for 1 $\mu$S after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available. |
| 1 | 0 | Manual Output | CB set low. |
| 1 | 1 | Manual Output | CB set high. |

### INTERRUPT MASK REGISTER DESCRIPTION

When the Interrupt Mode is selected (MC = 1), the Data Direction Register for Port C (DDRC) is used to enable or disable a corresponding interrupt input. For example: If $M_0 = 0$ then $I_0$ is disabled and any $I_0$ interrupt latched in the interrupt latch register will not be transferred to the AIR and will not cause IRQ to go low. The interrupt latch can be cleared by writing a zero to the appropriate bit in PRC.

### PORT REGISTER C DESCRIPTION

Port Register C (PRC) can operate in two modes. The mode is controlled by bit MC in register CR. When MC = 0, PRC is a standard I/O port, operating identically to PRA & PRB. If MC = 1, then port register C is used for handshaking and priority interrupt input and output.

**PRC When MC = 0:**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $PC_7$ | $PC_6$ | $PC_5$ | $PC_4$ | $PC_3$ | $PC_2$ | $PC_1$ | $PC_0$ |

**PRC When MC = 1:**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CB | CA | $\overline{IRQ}$ | $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

### INTERRUPT EDGE CONTROL

Bits $IE_4$ and $IE_3$ in the control register (CR) are used to determine the active edge which will be recognized by the interrupt latch.

If $IE_4$ ($IE_3$) = 0 then $I_4$ ($I_3$) latch will be set on a negative transition of $I_4$ ($I_3$) input.

If $IE_4$ ($IE_3$) = 1 then $I_4$ ($I_3$) latch will be set on a positive transition of the $I_4$ ($I_3$) input.

All other interrupt latches ($I_2$, $I_1$, $I_0$) are set on a negative transition of the corresponding interrupt input.

| | | | | |
|---|---|---|---|---|
| $I_4$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

**Interrupt Latch Register**
Clears on Read of AIR Using Following Equation

$ILR \leftarrow ILR \oplus AIR$

| | | | | |
|---|---|---|---|---|
| $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |

**Active Interrupt Register**
Clears following Read of AIR

**Interrupt Priority Select**
IP = 0 No Priority
IP = 1 Interrupts Prioritized

| |
|---|
| IP |

## FUNCTIONAL DESCRIPTION

### 1. IP = 0 No Priority

All interrupt information latched into interrupt latch register (ILR) is immediately transferred into active interrupt register (AIR) and $\overline{IRQ}$ is pulled low. Upon read of interrupt register the $\overline{IRQ}$ is reset high and the appropriate bit(s) of the interrupt latch register is cleared by exclusive OR-ing. The ILR with AIR ($ILR \oplus AIR$). After the appropriate interrupt request has been serviced a Write to the AIR will clear it and initiate a new interrupt sequence if any interrupts were received during previous interrupt servicing. In this non-prioritized mode it is possible for two or more interrupts to occur simultaneously and be transferred to the AIR. If this occurs it is a software effort to recognize this and respond accordingly.

### 2. IP = 1 *Interrupts Prioritized*

In this mode the Interrupt Inputs are prioritized in the following order $I_4 > I_3 > I_2 > I_1 > I_0$

In this mode only one bit of the AIR can be set at any one time. If an interrupt occurs it is latched into the interrupt latch register, the $\overline{IRQ}$ line is pulled low and the appropriate bit of the AIR is set. To understand fully the operation of the priority interrupts it is easiest to consider the following examples.

A. The first case is the simplest. A single interrupt occurs and the processor can service it completely before another interrupt request is received.

1. Interrupt $1_1$ is received.
2. Bit $I_1$ is set high in Interrupt Latch Register.
3. $\overline{IRQ}$ is pulled low.
4. $A_1$ is set high.
5. Processor recognizes $\overline{IRQ}$ and reads AIR to determine which interrupt occurred.
6. Bit $I_1$ is reset and $\overline{IRQ}$ is reset to high.
7. Processor Services Interrupt and signals completion of Service routine by writing to AIR.
8. $A_1$ is reset low and interrupt sequence is complete.

B. The second case occurs when an interrupt has been received and a higher priority interrupt occurs. (See Note)

1. Interrupt $I_1$ is received.
2. Bit $I_1$ is set high on the Interrupt Latch Register.
3. $\overline{IRQ}$ is pulled low and $A_1$ is set high.
4. Processor recognizes $\overline{IRQ}$ and reads AIR to determine which interrupt occurred.
5. Bit $I_1$ is reset and $\overline{IRQ}$ is reset high.
6. Processor begins servicing $I_1$ interrupt and the $I_2$ interrupt is received.
7. $A_2$ is set, $A_1$ is reset low and $\overline{IRQ}$ is pulled low.
8. Processor has not yet completed servicing $I_1$ interrupt so this routine will be automatically stacked in 6500 stack queue when new $\overline{IRQ}$ for $I_2$ of interrupt is received.
9. Processor reads AIR to determine $I_2$ interrupt occurrence and bit $I_2$ of interrupt latch is reset.
10. Processor services $I_2$ interrupt, clears $A_2$ by writing AIR and returns from interrupt. Returning from interrupt causes 650X processor to resume servicing $I_1$ interrupt.
11. Upon clearing $A_2$ bit in AIR, the $A_1$ bit will not be restored to a one. Internal circuitry will prevent a lower priority interrupt from interrupting the resumed $I_1$.

C. The third case occurs when an interrupt has been received and a lower priority interrupt occurs.

1. Interrupt $I_1$ is received and latched.
2. $\overline{IRQ}$ is pulled low and $A_1$ is set high.
3. Processor recognizes $\overline{IRQ}$ and reads AIR to determine that $I_1$ interrupt occurred.
4. Processor logic servicing $I_1$ interrupt during which $I_0$ interrupt occurs and is latched.
5. Upon completion of $I_1$ interrupt routine the processor writes AIR to clear $A_1$ to signal 6525 that interrupt service is complete.

6. Latch $I_0$ interrupt is transferred to AIR and $\overline{IRQ}$ is pulled low to begin new interrupt sequence.

**NOTE**

It was indicated that the 6525 will maintain Priority Interrupt information from previously serviced interrupts.

This is achieved by the use of an Interrupt Stack. This stack is pushed whenever a read of AIR occurs and is pulled whenever a write to AIR occurs. It is therefore important not to perform any extraneous reads or writes to AIR since this will cause extra and unwanted stack operations to occur.

The only time a read of AIR should occur is to respond to an interrupt request.

The only time a write of AIR should occur is to signal the 6525 that the interrupt service is complete.

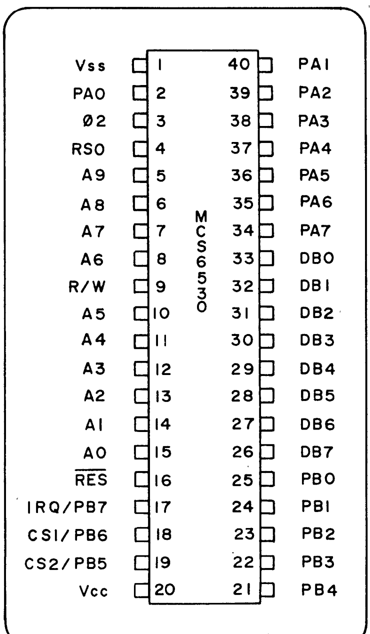
# 6530
# Memory, I/O, Timer Array

- **8-Bit Bidirectional Data Bus**
- **1024 x 8 ROM**
- **64 x 8 Static RAM**
- **2 8-Bit Bidirectional Data Ports**
- **2 Programmable Peripheral Data Direction Registers**
- **Programmable Interval Timer**
- **TTL & CMOS Compatible Peripheral Lines**
- **Programmable Timer Interrupt**
- **High-Impedance Three-State Data Pins**
- **Allows Up To 7K Contiguous Bytes of ROM Without External Decoding**

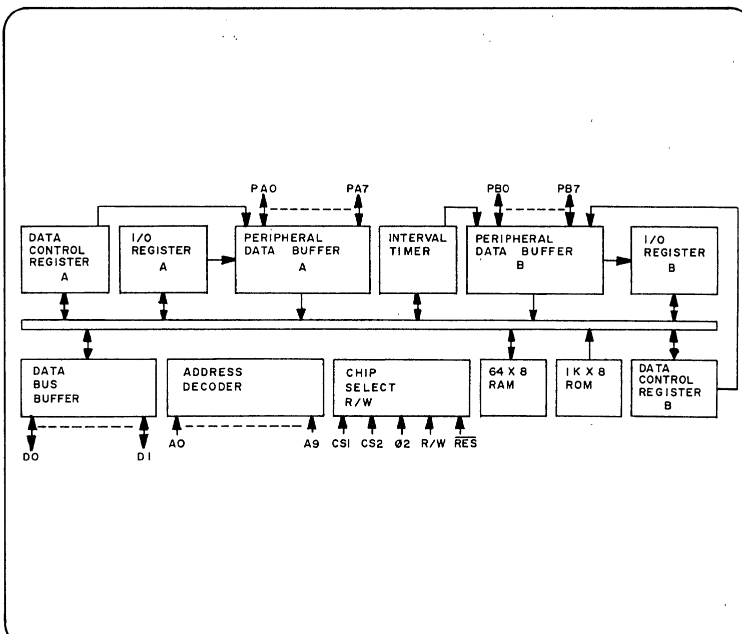
## DESCRIPTION

The 6530 is designed to operate in conjunction with a member of the 6500 microprocessor family. It is comprised of a mask-programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software-controlled, 8-bit, bidirectional data ports and a software-programmable interval timer with interrupt. The two ports allow direct interfacing between the microprocessor and the peripheral device(s) while the timer is capable of timing in various intervals from 1 to 262,144 clock periods.

## PIN CONFIGURATION




## BLOCK DIAGRAM




**Note**
MCS = Ceramic package
MPS = Plastic package

## INTERFACE SIGNAL DESCRIPTION

### Reset ($\overline{RES}$)

During system initialization a Logic Ø on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This will cause all I/O buses to act as inputs, protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF state during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

### Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or high level clock ($V_{IL} < 0.2$, $V_{IH} = V_{CC}\ ^{+.3}_{-.2}$).

### Read/Write (R/W)

The R/W signal is supplied by the microprocessor and is used to control the transfer of data between the microprocessor and the 6530. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the 6530. A low on the R/W pin allows a write by the processor (with proper addressing) to the 6530.

### Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the data direction register. The pin will be normally high with a low indicating an interrupt from the 6530. An external pull-up device is not required; however, if collector-ORed with other devices, the internal pullup may be omitted with a mask option.

### Data Bus (D0-D7)

The 6530 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when a Read operation occurs.

### Peripheral Data Ports

The 6530 has 16 pins available for peripheral I/O operations. Each pin is individually programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which are discussed later. The pins are set up as an input by writing a 0 into the corresponding bit of the data direction register. A 1 into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the 1 state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor reads the peripheral pin. When the peripheral device gets information from the 6530, it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a 1 and less than 0.8 volts for a 0 as the peripheral pins are all TTL compatible.

### Address Lines (A0-A9)

There are 10 address pins. In addition to these 10, there is the ROM SELECT pin. The above pins, A0-A9 and ROM SELECT, are always used as addressing pins. There are two additional pins which are mask-programmable and can be used either individually or together as CHIP SELECTS. They are pins PB5 and PB6. When used as peripheral data pins they cannot be used as chip selects.

## INTERNAL ORGANIZATION

The 6530 is divided into four basic sections, RAM, ROM, I/O and timer. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

### ROM 1K Byte (8K Bits)

The 8K ROM is in a 1024 x 8 configuration. Lines A0-A9 and RS0 are needed to address the entire ROM. With the addition of CS1 and CS2, seven 6530's may be addressed, giving up to 7168 x 8 bits of available contiguous ROM.

### RAM - 64 Bytes (512 Bits)

A 64 x 8 static RAM is contained in the 6530. It is addressed by A0-A5 (Byte Select), RS0, A6, A7, A8, A9 and, depending on the number of chips in the system, CS1 and CS2.

### Internal Peripheral Registers

There are four internal registers, two data direction registers and two peripheral I/O data registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A 1 written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Anything then written into the I/O Register will appear on that corresponding peripheral pin. A 0 written into the DDR inhibits the output buffer from transmitting data to or from the I/O Register. For example, a 1 loaded into DDRA Bit 3 sets up peripheral pin PA3 as an output. If a 0 had been loaded, PA3 would be configured as an input and remain in the high state. The two data I/O registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor.

During a read operation the microprocessor is not reading the I/O Registers but is actually reading the peripheral data pins. For the peripheral data pins which are programmed

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done to avoid future interrupts until after another Write timer operation.

**ADDRESSING**

Addressing of the 6530 offers many variations. The user may configure a system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition, there is the possibility of three additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are chip-selects (CS1 and CS2). The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as a chip-select. The third additional address line is RS0. The 6502 and 6530 in a two chip system would use RS0 to distinguish between ROM and non-ROM sections of the 6530. With the addressing pins available, a total of 7K contigous ROM may be addressed with no external decode.

**I/O Register - Timer Addressing**

Figure 2 illustrates the address decoding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected, A1 and A0 decode the divide-by matrix. This decoding is defined in Figure 2. In addition, A3 is used to enable the interrupt flag to PB7.

**Figure 2. Addressing Decode for I/O Register and Timer**

| | ROM SELECT | RAM SELECT | I/O TIMER SELECT | R/W | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|
| Read ROM | 1 | 0 | 0 | 1 | X | X | X | X |
| Write RAM | 0 | 1 | 0 | 0 | X | X | X | X |
| Read RAM | 0 | 1 | 0 | 1 | X | X | X | X |
| Write DDRA | 0 | 0 | 1 | 0 | X | 0 | 0 | 1 |
| Read DDRA | 0 | 0 | 1 | 1 | X | 0 | 0 | 1 |
| Write DDRB | 0 | 0 | 1 | 0 | X | 0 | 1 | 1 |
| Read DDRB | 0 | 0 | 1 | 1 | X | 0 | 1 | 1 |
| Write Per. Reg. A | 0 | 0 | 1 | 0 | X | 0 | 0 | 0 |
| Read Per. Reg. A | 0 | 0 | 1 | 1 | X | 0 | 0 | 0 |
| Write Per. Reg. B | 0 | 0 | 1 | 0 | X | 0 | 1 | 0 |
| Read Per. Reg. B | 0 | 0 | 1 | 1 | X | 0 | 1 | 0 |
| Write Timer | | | | | | | | |
| ÷ 1T | 0 | 0 | 1 | 0 | * | 1 | 0 | 0 |
| ÷ 8T | 0 | 0 | 1 | 0 | * | 1 | 0 | 1 |
| ÷ 64T | 0 | 0 | 1 | 0 | * | 1 | 1 | 0 |
| ÷ 1024T | 0 | 0 | 1 | 0 | * | 1 | 1 | 1 |
| Read Timer | 0 | 0 | 1 | 1 | * | 1 | X | 0 |
| Read Interrupt Flag | 0 | 0 | 1 | 1 | X | 1 | X | 1 |

**NOTES**

* $A_3$ = 1 Enables IRQ to PB7
$A_3$ = 0 Disables IRQ to PB7

as outputs, the microprocessor will read the corresponding data bits of the I/O Register. The only way the I/O Register data can be changed is by a microprocessor Write operation. The I/O Register is not affected by a Read of the data on the peripheral pins.

**Interval Timer**

The Timer section of the 6530 contains three basic parts: preliminary divide-down register, programmable 8-bit register and interrupt logic. There are illustrated in Figure 1.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be 1, 8, 64 or 1024 system clock periods. When a full count is reached, an interrupt flag is set to a logic 1. After the interrupt flag is set, the internal clock begins counting down to a maximum of −255 clock periods. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to this maximum.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Timer register.

At the same time data is being written to the Interval Timer, the counting intervals of 1, 8, 64 and 1024 clock periods are decoded from address lines A0 and A1. During a Read or Write operation, address line A3 controls the interrupt capability of PB7, i.e., $A_3 = 1$ enables $\overline{IRQ}$ on PB7, $A_3 = 0$ disables $\overline{IRQ}$ on PB7. When PB7 is to be used as an interrupt flag with the interval timer, it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs, PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read.

On the next count time after the timer has counted down to zero, an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by 1 rate of the system clock. After interrupt, if the timer is read and shows a value of 1 1 1 0 0 1 0 0, the time since interrupt is 28 clock periods, since values are in two's complement form.

After the interrupt, whenever the timer is written or read, the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flag is read on DB7 all other DB outputs (DB0 thru DB6) go to 0.

**BASIC ELEMENTS OF INTERVAL TIMER**

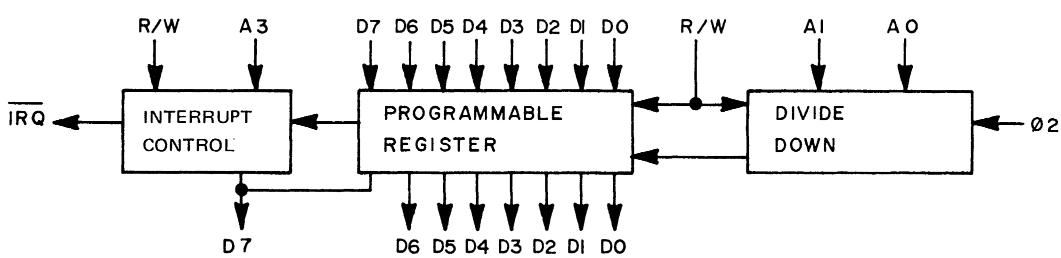



Figure 1

### ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −.3 to +7.0 | V |
| Input/Output Voltage | $V_{IN}$ | −.3 to +7.0 | V |
| Operating Temperature Range | $T_{OP}$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{STG}$ | −55 to +150 | °C |

### CAUTION

*All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.*

### ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0V ± 5%, $V_{SS}$ = 0V, $T_A$ = 0 - 70°C)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | $V_{SS}$+2.4 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input Low Voltage | $V_{SS}$−.3 | | $V_{SS}$+.4 | V | |
| $I_{IN}$ | Input Leakage Current | 0 | 1.0 | 2.5 | μA | $V_{IN}$ = $V_{SS}$−5V<br>A0-A9, RS, R/W, $\overline{RES}$, 02, PB6*, PB5* |
| $I_{TSI}$ | Input Leakage Current for High Impedance State (Three State) | | ±1.0 | ±10.0 | μA | $V_{IN}$ = .4V to 2.4V; D0-D7 |
| $I_{IH}$ | Input High Current | −100. | −300. | | μA | $V_{IN}$ = 2.4V<br>PA0-PA7, PB0-PB7 |
| $I_{IL}$ | Input Low Current | | −1.0 | −1.6 | MA | $V_{IN}$ = .4V<br>PA0-PA7, PB0-PB7 |
| $V_{OH}$ | Output High Voltage | $V_{SS}$+2.4 | $V_{SS}$+3.5 | $V_{CC}$ | V | $V_{CC}$ = MIN, $I_{LOAD}$ ≤ −100 μA<br>(PA0-PA7, PB0-PB7, D0-D7) |
| $V_{OL}$ | Output Low Voltage | $V_{SS}$ | $V_{SS}$+.2 | $V_{SS}$+.4 | V | $V_{CC}$ = MIN, $I_{LOAD}$ ≤ 1.6 MA |
| $I_{OH}$ | Output High Current (Sourcing) | −100<br>−3.0 | −1000<br>−5.0 | | μA<br>MA | $V_{OH}$ ≥ 2.4V (PA0-PA7, PB0-PB7, D0-D7)<br>≥ 1.5V Available for other than TTL (Darlingtons) (PA0, PB0) |
| $I_{OL}$ | Output Low Current (Sinking) | 1.6 | | | MA | $V_{OL}$ ≤ .4V (PA0-PA7)<br>(PB0-PB7) |
| $C_{Clk}$ | Clock Input Capacitance | | 20 | 30 | pF | |
| $C_{IN}$ | Input Capacitance | | 7 | 10 | pF | |
| $C_{OUT}$ | Output Capacitance | | 7 | 10 | pF | |
| $P_D$ | Power Dissipation | | 500 | 1000 | MW | |

**NOTE**
*When programmed as address pins
All values are D.C. readings

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CYC}$ | READ CYCLE<br>Clock Period | 1 | | 10 | µS |
| TR, TF | Rise and Fall Times | | 10 | 25 | NS |
| TC | Clock Pulse Width | 470 | | | NS |
| TWCW | R/W Valid Before Positive Transition of Clock | 180 | | | NS |
| TACW | Address Valid Before Positive Transition of Clock | 180 | | | NS |
| TDCW | Data Bus Valid Before Negative Transition of Clock | 300 | | | NS |
| THW | Data Bus Hold Time | 10 | | | NS |
| TCPW | Peripheral Data Valid After Negative Transition of Clock | | | 1 | µS |
| TCMOS | Peripheral Data Valid After Negative Transition of Clock Driving CMOS (Level=$V_{CC}$ −30%) | | | 2 | µS |
| TWCR | WRITE CYCLE<br>R/W Valid Before Positive Transition of Clock | 180 | | | NS |
| TACR | Address Valid Before Positive Transition of Clock | 180 | | | NS |
| TPCR | Peripheral Data Valid Before Positive Transition of Clock | 300 | | | NS |
| TCDR | Data Bus Valid After Positive Transition of Clock | | | 395 | NS |
| THR | Data Bus Hold Time | 10 | | | NS |
| TIC | $\overline{\text{IRQ}}$ (Interval Timer Interrupt) Valid Before Positive Transition of Clock | 200 | | | NS |

**NOTES**
Loading = 30 pF + 1 TTL load

## TIMING DIAGRAMS

### WRITE TIMING CHARACTERISTICS

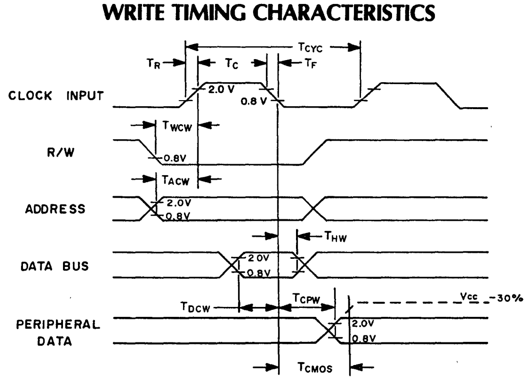



Figure 2

### READ TIMING CHARACTERISTICS

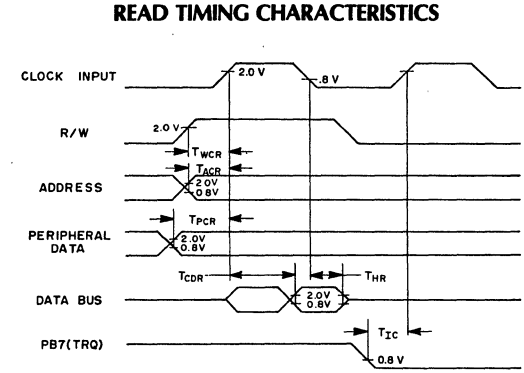



Figure 3

# 6532
# Memory, I/O, Timer Array

- **8-Bit Bidirectional Data Bus**
- **128 x 8 Statis RAM**
- **2 8Bit Bidirectional Data Ports**
- **2 Programmable Peripheral Data Direction Registers**
- **Programmable Interval Timer**
- **TTL & CMOS Compatible Peripheral Lines**
- **High-Impedance, Three-State Data Pins**

## DESCRIPTION

The 6532 is functionally nearly identical to the 6530 (described in this section of the Data Catalog). Like the 6530, the 6532 is designed to operate in conjunction with a member of the 6500 microprocessor family. Instead of having 1024 bytes of ROM and 64 bytes of static RAM, the 6532 has 128 bytes of static RAM and no ROM.

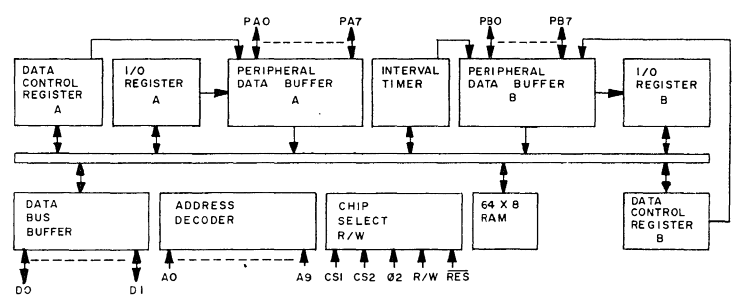
In virtually all other respects, the 6532 operates identically to the 6530 and the reader is referred to the detailed data sheet on the 6530 contained in this section of the Data Catalog for further information.

## PIN CONFIGURATION

**MCS6532**

| | | | |
|---|---|---|---|
| VSS | 1 | 40 | A6 |
| A5 | 2 | 39 | Ø2 |
| A4 | 3 | 38 | CS1 |
| A3 | 4 | 37 | $\overline{CS2}$ |
| A2 | 5 | 36 | $\overline{RS}$ |
| A1 | 6 | 35 | R/W |
| A0 | 7 | 34 | $\overline{RES}$ |
| PA0 | 8 | 33 | DB0 |
| PA1 | 9 | 32 | DB1 |
| PA2 | 10 | 31 | DB2 |
| PA3 | 11 | 30 | DB3 |
| PA4 | 12 | 29 | DB4 |
| PA5 | 13 | 28 | DB5 |
| PA6 | 14 | 27 | DB6 |
| PA7 | 15 | 26 | DB7 |
| PB7 | 16 | 25 | $\overline{IRQ}$ |
| PB6 | 17 | 24 | PB0 |
| PB5 | 18 | 23 | PB1 |
| PB4 | 19 | 22 | PB2 |
| VDD | 20 | 21 | PB3 |

## BLOCK DIAGRAM




**Note**
MSC = Ceramic package
MPS = Plastic package

## INTERFACE SIGNAL DESCRIPTION

### Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

### Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or high level clock ($V_{IL} < 0.2$, $V_{IH} = V_{CC} {}^{+.3}_{-.2}$).

### Read/Write (R/W)

The R/W signal is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the 6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the 6532. A low on the R/W pin allows a write (with proper addressing) to the 6532.

### Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the 6532. An external pull-up device is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

### Data Bus (D0-D7)

The 6532 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs.

### Peripheral Data Ports

The 6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PA7 also has other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the 6532 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volts for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.

### Address Lines (A0-A6)

There are 7 address pins. In addition to these 7, there is the $\overline{\text{RAM SELECT}}$ pin. The above pins, A0-A6 and $\overline{\text{RAM SELECT}}$, are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$.

## INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The 6532 is divided into four basic sections, RAM, I/O, TIMER, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of 2 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

### RAM - 128 Bytes (1024 Bits)

The 128 X 8 Read/Write memory acts as a conventional static RAM. Data can be written into the RAM from the microprocessor by selecting the chip (CS1 = 1, $\overline{CS2}$ = 0) and by setting $\overline{RS}$ to a logic 0 (0.4V). Address lines A0 through A6 are then used to select the desired byte of storage.

### Internal Peripheral Registers

The Peripheral A I/O port consists of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Data Direction Register (DDRA) causes the corresponding line of the PA port to act as an input. A logic one causes the corresponding PA line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Output Register (ORA).

Data is read directly from the PA pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Output Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Output Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the peripheral pin to act as an output.

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition will set the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag will cause $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled. The PA7 line should be set up as an input for this mode.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

Setting of the PA7 interrupt flag will occur on an active transition even if the pin is being used as a normal input or as a peripheral control output. The flag will also be set by an active transition if interrupting from PA7 is disabled. The reset signal ($\overline{RES}$) will disable the PA7 interrupt and will set the active transition to negative (high to low). During the system initialization routine, it is possible to set the interrupt flag by a negative transition. It may also be set by changing the polarity of the active interrupt. It is therefore recommended that the interrupt flag be cleared *before* enabling interrupting from PA7.

Clearing of the PA7 Interrupt Flag occurs when the microprocessor reads the Interrupt Flag Register.

The operation of the Peripheral B Input/Output port is exactly the same as the normal I/O operation of the Peripheral A port. The eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Output Register (ORB).

The primary difference between the PA and the PB ports is in the operation of the output buffers which drive these pins. The buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read PB" operation, sufficient logic is provided in the chip to allow the microprocessor to read the Output Register instead of reading the peripheral pin as on the PA port.

**Interval Timer**

The Timer section of the 6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

The interval timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of −255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Timer register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64 and 1024T are decoded from address lines A0 and A1. During a Read or Write operation, address line A3 controls the interrupt capability, i.e., $A_3 = 1$ enables IRQ, $A_3 = 0$ disables IRQ. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted thru 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number. Therefore, we must subtract 1.

| | | |
|---|---|---|
| Value read | = | 1 1 1 0 0 1 0 0 |
| Complement | = | 0 0 0 1 1 0 1 1 |
| ADD 1 | = | 0 0 0 1 1 1 0 0 = 28 Equals two's complement of register |
| SUB 1 | = | 0 0 0 1 1 0 1 1 = 27 |

Thus, to arrive at the *total* elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (= 52). With a divide by 8, total time to interrupt is (52 X 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrup was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (DB7 for the timer, DB6 for edge detect) data bus lines D0-D5 to go to 0.

**BASIC ELEMENTS OF INTERVAL TIMER**

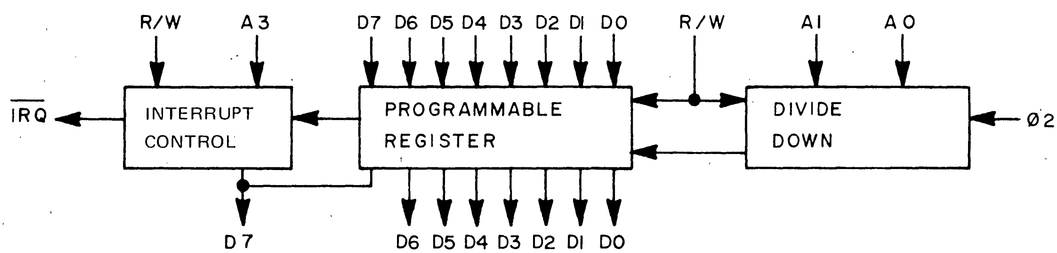



**Figure 1**

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −.3 to +7.0 | V |
| Input/Output Voltage | $V_{IN}$ | −.3 to +7.0 | V |
| Operating Temperature Range | $T_{OP}$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{STG}$ | −55 to +150 | °C |

## CAUTION

*All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.*

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0V ± 5%, $V_{SS}$ = 0V, $T_A$ = 25°C)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | $V_{SS}$+2.4 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input Low Voltage | $V_{SS}$−.3 | | $V_{SS}$+.4 | V | |
| $I_{IN}$ | Input Leakage Current | | 1.0 | 2.5 | μA | $V_{IN}$ = $V_{SS}$ +5V<br>A0-A6, $\overline{RS}$, R/W, $\overline{RES}$, 02, CS1, $\overline{CS2}$ |
| $I_{TSI}$ | Input Leakage Current for High Impedance State (Three State) | | ±1.0 | ±10.0 | μA | $V_{IN}$ = .4V to 2.4V; D0-D7 |
| $I_{IH}$ | Input High Current | −100. | −300. | | μA | $V_{IN}$ = 2.4V<br>PA0-PA7, PB0-PB7 |
| $I_{IL}$ | Input Low Current | | −1.0 | −1.6 | MA | $V_{IN}$ = .4V<br>PA0-PA7, PB0-PB7 |
| $V_{OH}$ | Output High Voltage | $V_{SS}$+2.4<br>$V_{SS}$+1.5 | | | V | $V_{CC}$ = MIN, $I_{LOAD}$ ≤ −100 μA (PA0-PA7, PB0-PB7, D0-D7)<br>$I_{LOAD}$ ≤ −3 MA (PA0, PB0) |
| $V_{OL}$ | Output Low Voltage | | | $V_{SS}$+.4 | V | $V_{CC}$ = MIN, $I_{LOAD}$ ≤ 1.6 MA |
| $I_{OH}$ | Output High Current (Sourcing) | −100<br>−3.0 | −1000<br>−5.0 | | μA<br>MA | $V_{OH}$ ≥ 2.4V (PA0-PA7, PB0-PB7, D0-D7)<br>≥ 1.5V Available for other than TTL (Darlingtons) (PB0, PB7) |
| $I_{OL}$ | Output Low Current (Sinking) | 1.6 | | | MA | $V_{OL}$ ≤ .4V (PA0-PA7) (PB0-PB7) |
| $C_{Clk}$ | Clock Input Capacitance | | | 30 | pF | |
| $C_{IN}$ | Input Capacitance | | | 10 | pF | |
| $C_{OUT}$ | Output Capacitance | | | 10 | pF | |
| $P_D$ | Power Dissipation | | 500 | 1000 | MW | |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CYC}$ | WRITE CYCLE<br>Clock Period | 1 | | | $\mu S$ |
| TR, TF | Rise and Fall Times | | | 25 | NS |
| TC | Clock Pulse Width | 470 | | | NS |
| TWCW | R/W Valid Before Positive Transition of Clock | 180 | | | NS |
| TACW | Address Valid Before Positive Transition of Clock | 180 | | | NS |
| TDCW | Data Bus Valid Before Negative Transition of Clock | 300 | | | NS |
| THW | Data Bus Hold Time | 10 | | | NS |
| TCPW | Peripheral Data Valid After Negative Transition of Clock | | | 1 | $\mu S$ |
| TCMOS | Peripheral Data Valid After Negative Transition of Clock Driving CMOS (Level=$V_{CC}$ −30%) | | | 2 | $\mu S$ |
| TWCR | READ CYCLE<br>R/W Valid Before Positive Transition of Clock | 180 | | | NS |
| TACR | Address Valid Before Positive Transition of Clock | 180 | | | NS |
| TPCR | Peripheral Data Valid Before Positive Transition of Clock | 300 | | | NS |
| TCDR | Data Bus Valid After Positive Transition of Clock | | | 395 | NS |
| THR | Data Bus Hold Time | 10 | | | NS |
| TIC | $\overline{IRQ}$ Valid Before Positive Transition of Clock | 200 | | | NS |

**NOTES**
Loading = 30 pF + 1 TTL load for PA0-PA7,
PB0-PB7 = 130 pF + 1 TTL load for D0-D7

## TIMING DIAGRAMS

**WRITE TIMING CHARACTERISTICS**

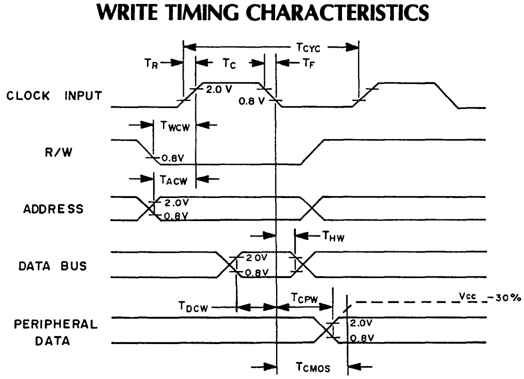



**Figure 2**

**READ TIMING CHARACTERISTICS**

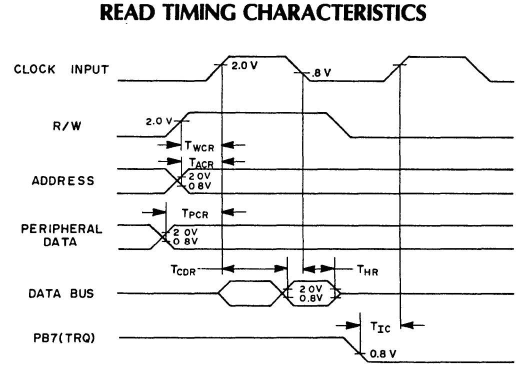



**Figure 3**

commodore semiconductor group

**NMOS**

# 6560/6561 Video Interface Chip (VIC)

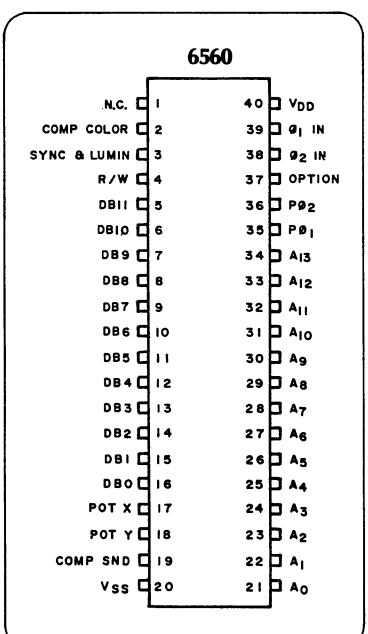
- Fully Expandable System With 16K Byte Address Space
- Mask-Programmable Sync Generation (NTSC-6560 or PAL-6561)
- On-Chip Color Generation
- Up to 600 Independently Programmable And Movable Background Locations
- Screen Grid Size Up to 192 x 200
- Two Selectable Graphic Character Sizes
- On-Chip Sound System
- On-Chip DMA And Address Generation
- 16 Addressable Control Registers
- Light Gun/Pen For Target Games

## DESCRIPTION

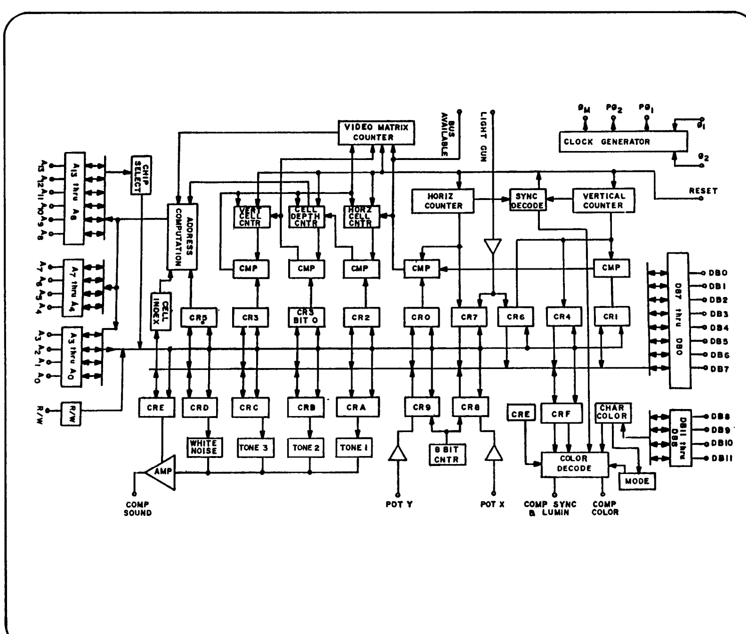
The 6560/6561 Video Interface Chip (VIC) is designed to implement color video graphics applications such as low-cost CRT terminals, biomedical monitors, control system displays and arcade/home video games. It provides all circuitry necessary for generating color programmable charcter graphics with high-screen resolution. VIC also incorporates sound effects and A/D converters for use in a video game environment.

Its on-chip sound system includes three independent, programmable tone generators, a white-noise generator and an amplitude modulator. It is designed so that no CPU wait states are required during screen refresh and offers the option of interlaced or non-interlaced operation via a switch which is programmable. The 6560/6561 provides two modes of color operation.

## PIN CONFIGURATION




## BLOCK DIAGRAM




**Note**

MCS = Ceramic package

MPS = Plastic package

## 6560 SIGNAL DESCRIPTION

**Address Bus ($A_0$-$A_{13}$)**
The 14-bit address bus ($A_0$-$A_{13}$) is bidirectional. During $P0_2 = 1$, the address pins are in the input mode. In this mode the microprocessor can access any of the sixteen VIC Control Registers. The high order pins of the Address Bus ($A_8$ thru $A_{13}$) act as Chip Select pins in this input mode. A true chip select condition occurs when $A_{13} = A_{11} = A_{10} = A_9 = A_8 = 0$ and $A_{12} = 1$, which equates to a VIC chip select address of 1000 in HEX. The lower order 4 bits of the address bus ($A_0$ thru $A_3$) are used as the control register select portion of the input address.

During $P0_1 = 1$, the VIC address pins will be in the output mode if data (either Character Pointer or Character Cell) is to be fetched. In this mode, VIC will output the address of the memory location to be fetched. The address from VIC will be valid 50ns after the rising edge of $P0_1$ and remain valid until the rising edge of $P0_2$.

**Read/Write (R/W)**
This signal is an input only and controls the flow of data between VIC and the microprocessor. When the R/W signal is low and the VIC chip select conditions have been satisfied, the microprocessor can write data into the selected VIC Control Register. If the R/W signal is high and the chip select conditions have been met, the microprocessor can read data from the selected VIC Control Register.

It is important to note that all VIC/microprocessor data transfers can only occur when $P0_2 = 1$. During $P0_1$, the VIC will be fetching data from memory for display and the R/W signal must be held high to insure that VIC will not write into any memory location.

**Data Bus ($DB_0$-$DB_{11}$)**
The 12-bit data bus, $DB_0$ - $DB_{11}$, is divided into two sections. The low-order eight bits, $DB_0$ thru $DB_7$, are used both to interface to the microprocessor and to fetch data needed for display, while the high-order four bits are used exclusively for retrieving color and mode information. The operation of the low-order eight bits ($DB_0$ thru $DB_7$) can also be separated into two categories: microprocessor interface and video data interface. During $P0_2 = 1$, $DB_7$ thru $DB_0$ are used exclusively for data transmission between the microprocessor and VIC. During $P0_1 = 1$, $DB_7$ thru $DB_0$ are used for fetching display data.

### CLOCKS

**Master Oscillator Clock Inputs—($\Phi 1$ and $\Phi 2$).** The 6560 requires a 14.31818 MHz (NTSC), Two-Phase Clock. The clock signals must be +5V and non-overlapping. The 6561 requires a 4.436187 MHz clock for PAL standard.

**System Clocks—($P0_1$ and $P0_2$).** These clocks are the master timing generator for the VIC System. They are +5V, non-overlapping 1.02 MHz clocks capable of driving the capacitance of the 6512 microprocessor.

**Memory Clock—(Optional, $\Phi M$).** This is a single-phase, 2.04 MHz clock used when memories in the VIC System require a strobe after the address bus is valid. It is one of the options available on Pin 37.

**Analog to Digital Converters (POTX and POTY).**
These input pins are used to convert potentiometer position into a microprocessor-readable 8-bit hex number. This is accomplished by a simple RC time constant integration technique. The potentiometer is used to charge an external capacitor tied to the pot pin.

**Composite Sound (COMP SND).**
This pin provides the output of the sound synthesizer portion of the 6560 shown in the VIC Block Diagram. It is a high-impedance output (approximately 1KΩ) and must be buffered and amplified externally to drive a speaker.

**Composite Sync and Luminance (SYNC & LUMIN).**
This pin is an open-drain output which provides all necessary video synchronization and luminance information required by a standard television.

**Composite Color (COMP COLOR).**
This signal provides the necessary color information required by a standard television to receive a full-color picture. The composite color pin is a high-impedance output buffer which provides the reference burst signal plus the color-encoded phase and amplitude information at the proper 3.579545 MHz frequency.

**Reset**
This optional Pin 37 input signal is used to synchronize the horizontal and vertical sync counter to an external signal.

**Bus Available**
This optional Pin 37 output signal indicates the state of the VIC with respect to the video memory fetch. The pin will go low 2 μsec before VIC performs any memory access and will remain low until the entire screen has been refreshed.

**Light Gun/Pen**
The optional Pin 37 input signal causes the current dot position being scanned onto the screen to be latched onto control registers 6 and 7, upon a negative-going edge. This pin would be used in conjunction with a photo detector for use in a "target shoot" type game or for light pen applications.

**AVAILABLE AUXILIARY/BACKGROUND COLORS**
0 BLACK
1 WHITE
2 RED
3 CYAN
4 MAGENTA
5 GREEN
6 BLUE
7 YELLOW

8 ORANGE
9 LIGHT ORANGE
A PINK
B LIGHT CYAN
C LIGHT MAGENTA
D LIGHT GREEN
E LIGHT BLUE
F LIGHT YELLOW

**AVAILABLE BORDER/ CHARACTER COLORS**
0 BLACK
1 WHITE
2 RED
3 CYAN
4 MAGENTA
5 GREEN
6 BLUE
7 YELLOW

## THEORY OF OPERATION

To produce programmable color characters, VIC accesses external memory which can be divided into three areas: character pointers, display characters and color pointers. The character pointer area is a block of bytes in RAM (typically 506 bytes called the Video Matrix) in which each byte points to a particular character to be displayed. The character area consists of a set of 8 or 16 byte blocks (usually called cells) which contain the actual dot patterns to be displayed. These character cells can be located in either RAM or ROM, depending on how the objects are to be displayed or moved on the screen. The color pointer area is a block of nibbles in RAM (typically 506 four-bit nibbles called the Color Matrix). The four-bit color pointers are used to define the color of any character to be displayed and to select one of the two color modes.

It is the task of an external microprocessor to organize the Video Matrix, Color Matrix and Character Cells into the proper format to display the data desired on-screen.

To understand the operation of VIC more completely, refer to Figure 1. This is a typical Video Matrix, in which 22 characters horizontally by 23 characters vertically are to be displayed, yielding a total of 506 character display locations, with a screen resolution of 176 horizontal by 184 vertical dots. Each one of these character display locations has a corresponding character pointer, or index, which specifies (points at) a character to be displayed in a particular location.

In the example shown, rectangle (B,15) has a character index of 2B. This means character number 2B is to be displayed in that rectangle. VIC will fetch the character index value 2B and perform an address computation to locate the character to be displayed. The computation is quite simple. If 8 x 8 character cells are selected, the index is left shifted 3 times (multiply by 8) and the starting address of the character cells, found in VIC Control Register CR5, is added to the left-shifted value. In this case, the character cell starting address is 3400H which is added to the left-shifted value of the character index to yield the actual character location in memory of 3558H.

The number of times that any particular character can be displayed is unlimited. By using the same character index (2B for example) elsewhere on the grid, the character data will be displayed again. Alternately, through the use of a simple software driver, VIC can be used as a bit-mapped display system provided enough RAM (approximately 4K bytes of cell RAM) is available.

**TYPICAL VIDEO MATRIX (23 x 22)**

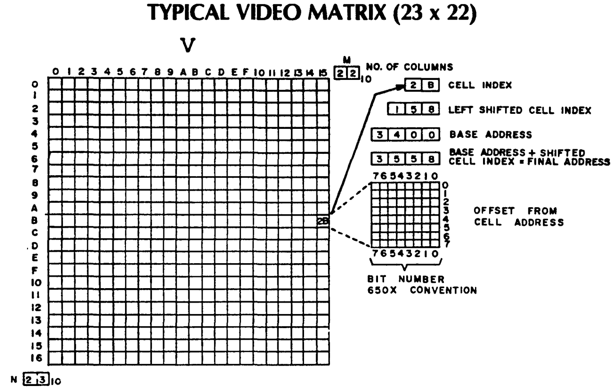



**Figure 1**

## VIC CONTROL REGISTERS

1000 ORIGIN

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | (bit number) |
|---|---|---|---|---|---|---|---|---|---|---|
| $CR_0$ | 1000 | I | $S_X^6$ | $S_X^5$ | $S_X^4$ | $S_X^3$ | $S_X^2$ | $S_X^1$ | $S_X^0$ | Screen Origin X-Coordinate |
| $CR_1$ | 1001 | $S_Y^7$ | $S_Y^6$ | $S_Y^5$ | $S_Y^4$ | $S_Y^3$ | $S_Y^2$ | $S_Y^1$ | $S_Y^0$ | Screen Origin Y-Coordinate |
| $CR_2$ | 1002 | $B_V^9$ | $M_6$ | $M_5$ | $M_4$ | $M_3$ | $M_2$ | $M_1$ | $M_0$ | No. of Video Matrix Columns |
| $CR_3$ | 1003 | $R_0$ | $N_5$ | $N_4$ | $N_3$ | $N_2$ | $N_1$ | $N_0$ | D | No. of Video Matrix Rows |
| $CR_4$ | 1004 | $R_8$ | $R_7$ | $R_6$ | $R_5$ | $R_4$ | $R_3$ | $R_2$ | $R_1$ | Raster Value |
| $CR_5$ | 1005 | $B_V^{13}$ | $B_V^{12}$ | $B_V^{11}$ | $B_V^{10}$ | $B_C^{13}$ | $B_C^{12}$ | $B_C^{11}$ | $B_C^{10}$ | Base Address Control |
| $CR_6$ | 1006 | $L_H^7$ | $L_H^6$ | $L_H^5$ | $L_H^4$ | $L_H^3$ | $L_H^2$ | $L_H^1$ | $L_H^0$ | Light Pen Horizontal |
| $CR_7$ | 1007 | $L_V^7$ | $L_V^6$ | $L_V^5$ | $L_V^4$ | $L_V^3$ | $L_V^2$ | $L_V^1$ | $L_V^0$ | Light Pen Vertical |
| $CR_8$ | 1008 | $P_X^7$ | $P_X^6$ | $P_X^5$ | $P_X^4$ | $P_X^3$ | $P_X^2$ | $P_X^1$ | $P_X^0$ | Pot X |
| $CR_9$ | 1009 | $P_Y^7$ | $P_Y^6$ | $P_Y^5$ | $P_Y^4$ | $P_Y^3$ | $P_Y^2$ | $P_Y^1$ | $P_Y^0$ | Pot Y |
| $CR_A$ | 100A | $S_1$ | $F_1^6$ | $F_1^5$ | $F_1^4$ | $F_1^3$ | $F_1^2$ | $F_1^1$ | $F_1^0$ | $F_{IN}(1)$ |
| $CR_B$ | 100B | $S_2$ | $F_2^6$ | $F_2^5$ | $F_2^4$ | $F_2^3$ | $F_2^2$ | $F_2^1$ | $F_2^0$ | $F_{IN}(2)$ |
| $CR_C$ | 100C | $S_3$ | $F_3^6$ | $F_3^5$ | $F_3^4$ | $F_3^3$ | $F_3^2$ | $F_3^1$ | $F_3^0$ | $F_{IN}(3)$ |
| $CR_D$ | 100D | $S_4$ | $F_4^6$ | $F_4^5$ | $F_4^4$ | $F_4^3$ | $F_4^2$ | $F_4^1$ | $F_4^0$ | $F_{IN}(4)$ |
| $CR_E$ | 100E | $C_A^3$ | $C_A^2$ | $C_A^1$ | $C_A^0$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | Amplitude |
| $CR_F$ | 100F | $C_B^3$ | $C_B^2$ | $C_B^1$ | $C_B^0$ | R | $C_E^2$ | $C_E^1$ | $C_E^0$ | Color Control |

**Note**
N. U. = NOT USED.

**Figure 2**

### REGISTER DESCRIPTION

There are 16 eight-bit control registers within the 6560 which enable the microprocessor to control all operating modes of VIC. The control registers and their functions are tabulated and explained below, while a diagram of the register locations and contents are shown in Figure 2.

### CR0

Bits 0-6 determine how far from the left-hand side of the T.V. screen the first column of characters will appear. It is used to horizontally center various sizes of video matrices on-screen. Bit 7 selects interlaced scan mode (I = 1).

### CR1

Determines how far from the top of the T.V. screen the first row of characters will appear. It is used to vertically center various sizes of video matrices on-screen.

### CR2

Bits 0-6 set the number of columns in the Video Matrix. Bit 7 is part of the Video Matrix address found in CR5.

### CR3

Bits 1-6 set the number of rows in the Video Matrix. Bit 0 is used to select either 8 x 8 character matrices (D = 0) or 16 x 8 character matrices (D = 1). Bit 7 is part of the raster value found in CR4.

### CR4

Contains the number of the line currently being scanned by the T.V. raster beam.

**CR5**
Bits 0-3 determine the starting address of the character cell space. (Note that these bits form bits A13 through A10 of the actual address.) Bit 4-7 (along with Bit 7 of CR2) determine the starting address of the Video Matrix (these bits form bits A13 through A9 of the actual address).

**CR6**
Contains the latched horizontal position of the light gun/pen.

**CR7**
Contains the latched vertical position of the light gun/pen.

**CR8**
Contains the digitized value of POTX.

**CR9**
Contains the digitized value of POTY.

**CRA**
Bits 0-6 set the frequency of the first audio oscillator. Bit 7 turns the oscillator on (= 1) or off (= 0).

**CRB**
Same as CRA for second audio oscillator.

**CRC**
Same as CRA for third audio oscillator.

**CRD**
Same as CRA but sets frequency of noise source.

**CRE**
Bits 0-3 set the volume of the composite audio signal (Note that at least one sound generator must be turned on for any sound to be produced). Bits 4-7 contain the Auxiliary color code used in conjunction with the "Multicolor" mode of operation.

**CRF**
Bits 4-7 select one of 16 colors for the background common to all characters. (Essentially, they set the color of the background area within the Video Matrix.) Bits 0-2 select 1 of 8 colors for the exterior border area of the screen (all area outside the Video Matrix). Bit 3 determines whether the Video Matrix will be displayed as different colored characters on a common background color (R = 1) or inverted (R = 0), that is, all characters will be the same color (the background color in $CR_F$) while each character's background will now be a different color, determined by the code in the Color RAM. Note that the R bit has no effect when Multicolor mode is selected and the CRF also functions differently in this mode. Refer to the section called "Operating Modes" for complete information.

**COLOR OPERATING MODES**
VIC incorporates two modes of color operation – HI-RES (high resolution) mode and Multicolor mode. Basically, the operating mode affects how the Character Cell information will be translated into dots on the T.V. screen. The operating mode is determined by the MSB of the color pointer associated with each character location in the Video Matrix. If the MSB of a character's color pointer is zero, that character will be displayed in HI-RES mode. Alternately, if the MSB is one, the character will be displayed in the Multicolor mode.

With HI-RES mode selected, there is a one-to-one correspondence between Character Cell bits and the dots displayed on-screen. That is, all one bits of a character will be displayed in one color, and all zero bits in another color. The foreground color of the character is specified by the remaining 3 bits of the character's color pointer, while the character's background color is specified by Control Register F.

With Multicolor mode selected, each two bits of a character cell correspond to one dot on-screen and the color of that dot is determined by the two-bit code. Unlike HI-RES mode, in which only two colors can be displayed in a single character, Multicolor mode allows four colors per character; however, since two bits of cell data now correspond to a single dot on-screen, the horizontal resolution is half that of the HI-RES mode. That is, each 8x8 Character Cell in memory maps onto an 8x4 character on-screen (8 lines of 4 dots each). Note that the amount of memory required for these 8x4 Multicolor characters is the same as that for 8x8 HI-RES characters; the data is simply mapped differently on-screen.

In Multicolor mode, the two bits which make up a dot select one of four colors for that dot. The four codes created by these two bits tell VIC where to find the color information for the dot. The color of the dot can be either the Background color (in CRF), the Exterior Border color in (CRF), the Auxiliary color (in CRE) or the Foreground color (bits 0 thru 2 of the character's color pointer).

The Multicolor mode color select codes are:

00 — Background color ($CR_F$)
01 — Exterior Border color ($CR_F$)
10 — Foreground color (Color RAM)
11 — Auxiliary color ($CR_E$)

Note that the two-bit code is not itself a color code; rather it is a pointer to four different color codes, allowing greater color flexibility, as each code pointed to has either 3 or 4-bit resolution.

**Example:**

Given:

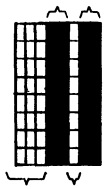
$CR_F$ = 1F  Character Background color is WHITE (1), Exterior Border color is YELLOW (7), Invert is not selected (R = 1).

$CR_E$ = 6X  Auxiliary color is BLUE (6).

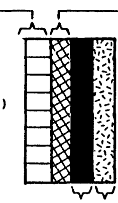
and a character definition of:

| | bit 76543210 | HEX |
|---|---|---|
| byte | 0 00011011 | 1B |
| | 1 00011011 | 1B |
| | 2 00011011 | 1B |
| | 3 00011011 | 1B |
| | 4 00011011 | 1B |
| | 5 00011011 | 1B |
| | 6 00011011 | 1B |
| | 7 00011011 | 1B |

If the color pointer nybble for that character is 0 (0000), then the Foreground color is BLACK (0) and HI-RES modes is selected (MSB = 0). The character will then appear on-screen as:




If the color pointed nybble for that character is 8 (1000), then the Foreground color is BLACK (0) and the Multicolor mode is selected (MSB = 1). The character will then appear on-screen as:




(Note that this is given solely as an example and due to color transition limitations of most TV sets, closely spaced dots of different colors will not appear sharply defined on-screen.)

Since the mode of display for a character is selected by the character's color pointer and each character location on-screen has a unique color pointer, it is possible to freely intermix HI-RES and Multicolor characters. This provides great display flexibility, allowing HI-RES characters for alphanumerics, etc. and Multicolor characters for a wider array of colors available simultaneously.

**EXAMPLE OF VIC CONTROL REGISTER USE:**
For simplicity, assume all characters are in the HI-RES mode and the VIC Registers are loaded with the following values:

| Reg | Contents (HEX) | Binary | Results |
|---|---|---|---|
| CR0 | 03 | 0/000 0011 | Moves Video Matrix over 3(x4) dot widths from the left side of the screen. Interlace is not selected (I = 0). |
| CR1 | 19 | 0001 1001 | Moves Video Matrix down HEX 19 (x2) dot heights from top of screen. |
| CR2 | 96 | 1/001 0110 | Sets HEX 16 (=22 base 10) columns in Video Matrix. (Bit 7 is used with $CR_5$.) |
| CR3 | 2E | X/010 111/0 | Sets 010111 (=23 base 10) rows in Video Matrix. 8 x 8 character matrices are selected (D = 0). |
| CR5 | Should be set to access the proper memory locations of the specific system. Suppose it is desired to locate the Video Matrix starting at address HEX 0200, and the character matrices starting at address HEX 3400. In order to accomplish this, $CR_5$ is set: | | |
| CR5 | 0D | 0000 1101 | and bit 7 of $CR_2$ is set to 1. |
| | This would create a 14-bit address of the form:<br>$CR_5$ BITS  $CR_2$ BIT<br>76 547<br>00 001X XXXX XXXX<br>0 2 0 0<br>for the Video Matrix.<br>It would also create a 14-bit address of the form:<br>$CR_5$ BITS<br>32 10<br>11 01XX XXXX XXXX<br>3 4 0 0<br>for the character matrices. | | |
| CRA | 00 | 0/000 0000 | Oscillator 1 is OFF. |
| CRB | 9A | 1/001 1010 | Oscillator 2 is ON, with a relative frequency of 1A. |
| CRC | 00 | 0/000 0000 | Oscillator 3 is OFF. |
| CRD | A5 | 1/010 0101 | Noise generator is ON with a relative frequency of 25. |
| CRE | XF | XXXX 1111 | Sound effects are set for loudest volume. |
| CRF | 0E | 0000/1/110 | The background color common to all characters is black (0), the border color is dark blue (6) and each character is displayed in its own color on the black background (R = 1). |

These register values will produce a screen with a properly centered Video Matrix of 23x22 characters, each character appearing in color on a black background, with a dark blue border surrounding the Video Matrix area. Additionally, the sound effects generator will be producing a pitched oscillation, along with white noise.

All of these registers can be modified to produce different effects.

For example:

If the number in CR0 is increased, the Video Matrix region will shift farther to the right. If the number in CRB is reduced (leaving bit 7 a one) the frequency of oscillator 2 will go down.

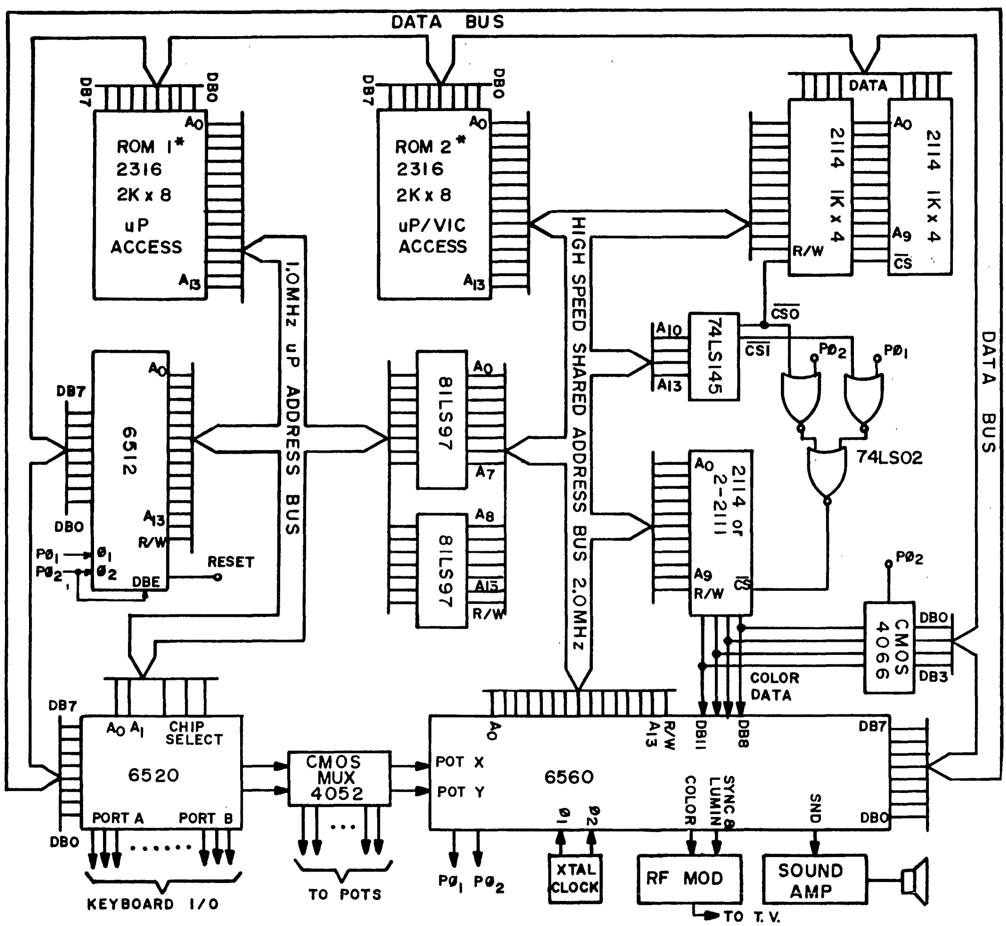
If CRF is changed to 06 (turning R OFF), the border will remain dark blue, but now the Video Matrix will appear as black characters on different colored backgrounds.

For VIC to produce a picture on-screen, the number of rows and columns and appropriate centering values must be loaded into the proper registers.

**MINIMUM SYSTEM DESCRIPTION**

A minimum VIC System would consist of a microprocessor, VIC, ROM, RAM and I/O. The basic system includes one $\mu$P (6512), one Video Interface Chip (VIC/6560), one PIA (6520), two 1K x 4 static RAMS, two 256 x 4 static RAMS, and one or more program/graphics ROMS (2K x 8 or 4K x 8). See Figure 3.

**VIC MINIMUM SYSTEM**




*NOTE
ROM 1 or ROM 2 is optional, since either can be cartridge loaded. ROM 1 is accessed by the processor only. ROM 2 can be accessed by the processor or VIC.

**Figure 3**

The tasks involved in a complete game are divided between the $\mu$P and VIC. The $\mu$P controls the game logic and VIC controls the video display as well as the sound generation.

**6512 Microprocessor**
The 6512 is a member of the 6500 microprocessor family, which has gained wide acceptance in the video game industry. The 6512 architecture and addressing capability are well suited to graphic data manipulation. Alternately, a 6502 processor can be used by feeding VIC P02 OUT into the 6502 00 IN; however, tri-state buffers must then be added to the data bus as well as the address bus.

**6560 Video Interface Chip**
The 6560 is a video display device which reads data that has been formatted by the $\mu$P and supplies the appropriate color graphic signals to the RF modulator. To accomplish this, the 6560 does a transparent DMA of the $\mu$P's memory space, accessing ROM and/or RAM.

**6520 Peripheral Interface Adapter**
This chip is used for keyboard scanning and joystick multiplexing.

**Resident RAM = 2 (2114) and (2111)**
These RAM chips are used as working storage by the $\mu$P and for holding the screen organization and color matrices. They may be modified by the $\mu$P at any time. Note that to achieve a full bit-map display, a minimum of 4K bytes of character RAM are necessary.

**Program/Graphics ROM(s)**
These chips normally contain the game logic and/or coded graphic data. There is no need for a resident ROM in a minimum system. A cartridge ROM can contain all the relevant information.

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Ambient Temperature under Bias | −10° to 80°C |
| Storage Temperature | −65°C to 150°C |
| Voltage on any Pin* | −0.5V to +7V |
| Power Dissipation | 1.0W |

NOTE
*With respect to Ground

**COMMENT**
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

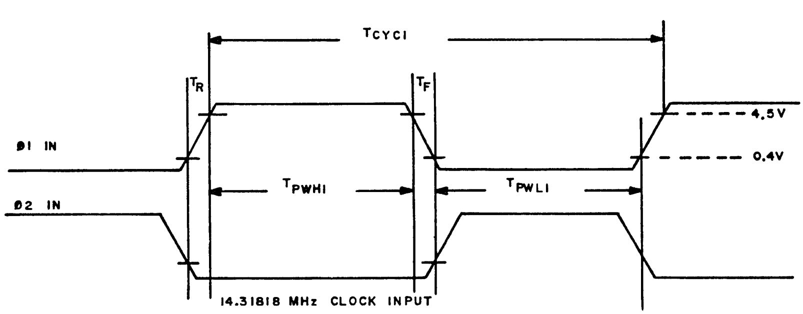
**DC CHARACTERISTICS** $T_A$ = 0°C to +50°C, $V_{DD}$ = 5V ± 5% (unless otherwise specified)

| Parameter | Min | Max | Typ | Units |
|---|---|---|---|---|
| **Read/Write, Reset (Option)** | | | | |
| Address and Data-Input State | | | | |
| $V_{IL}$ | −0.2 | 0.4 | | Volts |
| $V_{IH}$ | 2.4 | 5.6 | | Volts |
| Input Capacitance | | 8.0 | 5.0 | pF |
| Input Leakage (all outputs in high impedance state) | | 10.0 | 1.0 | $\mu$A |
| **Address and Data-Output State** | | | | |
| $V_{OL}$ | | 0.4 | | Volts |
| $V_{OH}$ | 2.4 | | | Volts |
| $I_{OL}$ — Sink current $V_{OL}$ = 0.4 | 2.4 | | | mA |
| $I_{OH}$ — Source current $V_{OH}$ = 2.4 | 200 | | | $\mu$A |
| Impedance in Three State Condition | 1 x $10^6$ | | | Ohms |
| **Clock Input ($\phi_1$ and $\phi_2$ Input)** | | | | |
| Frequency | | | 14.31818 | MHz |
| Capacitance | | 10.0 | | pF |
| $V_{IL}$ | −0.2 | 0.3 | | Volts |
| $V_{IH}$ | 4.5 | | 5.0 | Volts |
| **Clock Outputs ($P\phi_1$, $P\phi_2$)** | | | | |
| $V_{OL}$ | | 0.3V | | Volts |
| $I_{OL}$ @ 0.3 Volts $V_{OL}$ | 1.6 | | | mA |
| $V_{OH}$ | $V_{DD}$−.2 | | | Volts |
| $I_{OH}$ @ 4.7 Volts $V_{OH}$ | 200 | | | $\mu$A |
| Loading | | 120.0 | | pF |
| Frequency | | | 1.02 | MHz |

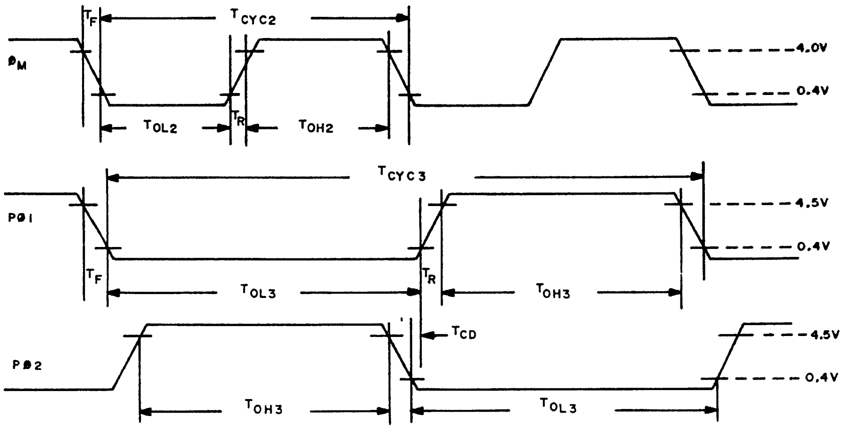
**DC CHARACTERISTICS** $T_A = 0°C$ to $+50°C$, $V_{DD} = 5V \pm 5\%$ (unless otherwise specified)

| Parameter | Min | Max | Typ | Units |
|---|---|---|---|---|
| **Composite Sound** | | | | |
| Output Impedance | | 2000 | 1000 | Ω |
| Max. Current (Sink or Source) | | 500 | | μA |
| Output Offset Voltage | 2.2 | 2.8 | 2.5 | Volts |
| $V_{OH}$ (Max. Amplitude) | 3.2 | | 3.5 | Volts |
| $V_{OL}$ (Max. Amplitude) | | 1.8 | 1.5 | Volts |
| $V_{OH}$ (Min. Amplitude) | 2.55 | | 2.6 | Volts |
| $V_{OL}$ (Min. Amplitude) | | 2.45 | 2.4 | Volts |
| **Pot Inputs** | | | | |
| $V_{TRIGGER}$ (Rising Edge) | 2.2 | 2.8 | 2.5 | Volts |
| **Pot Reset** | | | | |
| $V_{OL}$ | | 0.2 | | Volts |
| $I_{OL}$ @ $V_{OL} = 0.2$ | 500 | | | μA |
| **Light Pen Input (Option)** | | | | |
| $V_{TRIGGER}$ (Falling Edge) | 2.8 | 2.2 | 2.5 | Volts |
| **$\phi_M$ (Option)** | | | | |
| $V_{OL}$ | | 0.4 | | Volts |
| $I_{OL}$ @ 0.3 Volts $V_{OL}$ | 1.6 | | | mA |
| $V_{OH}$ | $V_{DD}$ −.7 | | | Volts |
| $I_{OH}$ @ 4.7 Volts $V_{OH}$ | 100 | | | μA |
| Loading | | 60 | | pF |
| Frequency | | | 2.04 | MHz |
| **Bus Available (Option)** | | | | |
| $V_{OL}$ | | 0.3 | | Volts |
| $I_{OL}$ | 1.6 | | | mA |
| $V_{OH}$ | 2.4 | | | Volts |
| $I_{OH}$ | 100 | | | μA |
| $V_{DD}$ | 4.75 | 5.25 | 5.00 | Volts |
| $I_{DD}$ | | 150 | 120 | mA |

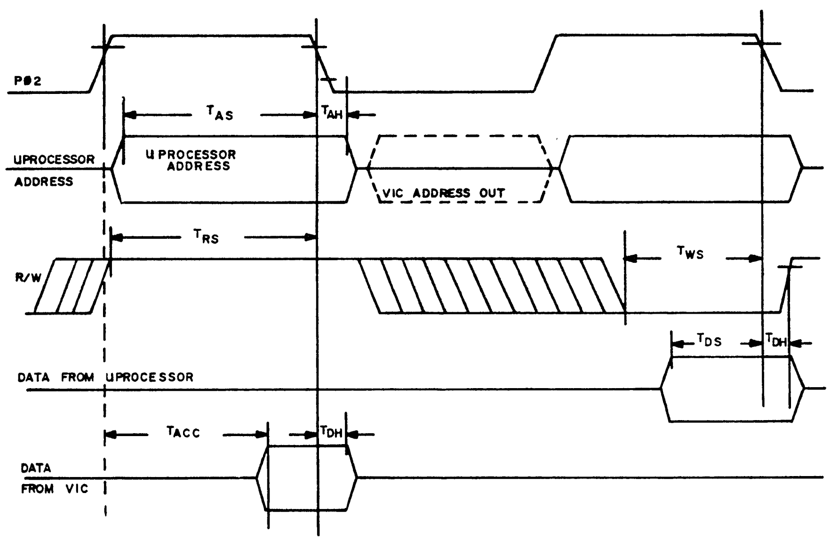
**VIC INPUT CLOCKS**



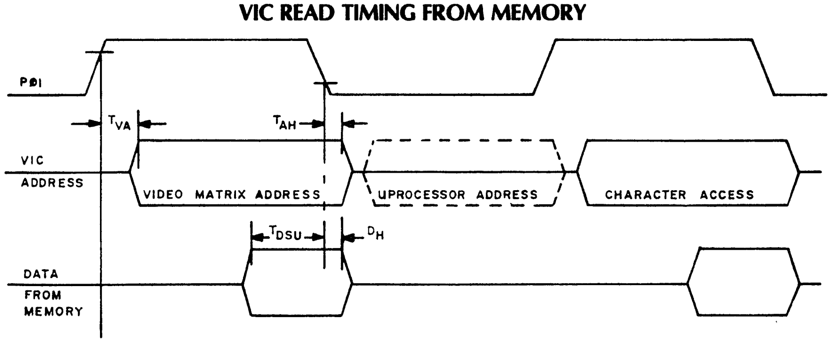
## VIC OUTPUT CLOCKS




## MICROPROCESSOR READ/WRITE TIMING TO VIC




## VIC READ TIMING FROM MEMORY



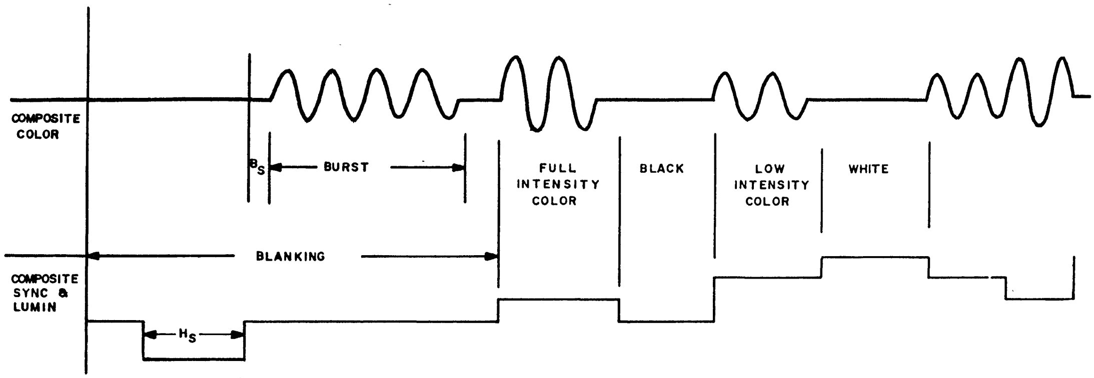
## VIC SYSTEM TIMING

| Symbol | Characteristic | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | **VIC Input Clock Timing** | | | | |
| $T_{CYC1}$ | Input Clock Cycle Time | 69.82 | | 69.84 | ns |
| $T_{PWH1}$ | Clock High | 20 | | | ns |
| $T_{PWL1}$ | Clock Low | 20 | | | ns |
| $T_R$, $T_F$ | Rise and Fall Time | | | 10 | ns |
| | **VIC Output Clock Timing** | | | | |
| $T_{CYC2}$ | Two MHz Clock Cycle Time | 480 | | 500 | ns |
| $T_{OL2}$ | $\phi_M$ Clock Output Low | 200 | | 260 | ns |
| $T_{OH2}$ | $\phi_M$Clock Output High | 180 | | 250 | ns |
| $T_{CYC3}$ | 1MHz $\mu$Processor Clocks Cycle Time | 960 | | 990 | ns |
| $T_{OL3}$ | $P\phi_1$, $P\phi_2$ Clocks Low | 380 | | 500 | ns |
| $T_{OH3}$ | $P\phi_1$, $P\phi_2$ Clocks High | 380 | | 500 | ns |
| $T_{CD}$ | Delay Time Between Clocks At .4v | 5 | | 20 | ns |
| $T_R$ | Rise Time, Max. $C_L$ | | | 80 | ns |
| $T_F$ | Fall Time, Max. $C_L$ | | | 40 | ns |
| | **Microprocessor Read/Write Timing to VIC** | | | | |
| $T_{AS}$ | Address Set Up Time | 375 | | | ns |
| $T_{AH}$ | Address Hold Time | 5 | | | ns |
| $T_{RS}$ | Read Set Up Time | 375 | | | ns |
| $T_{WS}$ | Write Set Up Time | 275 | | | ns |
| $T_{DS}$ | Data Set Up Time | 200 | | | ns |
| $T_{ACC}$ | Data Access Time | 350 | | | ns |
| $T_{DH}$ | Data Hold Time | 30 | | | ns |
| | **VIC Read Timing From Memory** | | | | |
| $T_{VA}$ | Time To Valid Address From $P\phi_1$ | | | | ns |
| $T_{AH}$ | Address Hold Time | 10 | | | ns |
| $T_{DSU}$ | Data Set Up Time | 60 | | | ns |
| $D_H$ | Data Hold Time | 20 | | | ns |
| | **Composite Sync, Color And Luminance Timing** | | | | |
| BLANKING | Blanking Period (No Video) | 10.0 | 11.0 | 12.0 | $\mu s$ |
| $B_S$ | Breeze Way | .3 | .5 | .7 | $\mu s$ |
| BURST | Color Burst Reference Signal | 4.0 | 5.0 | 6.0 | $\mu s$ |
| | **Composite SYNC Output Timing** | | | | |
| $H_S$ | Horizontal Sync Pulse | 4.0 | 5.0 | 6.0 | $\mu s$ |
| $H_L$ | Horizontal Line Period | 63.0 | 63.5 | 64.0 | $\mu s$ |
| $H_{L/2}$ | One Half Horizontal Line Period | 30.0 | 31.5 | 32.5 | $\mu s$ |
| E | Equalization Pulse | 2.0 | 2.5 | 3.0 | $\mu s$ |
| $E_L$ | Equalization Time Period | 188.0 | 190.5 | 192.0 | $\mu s$ |
| $V_S$ | Vertical Sync Period | 188.0 | 190.5 | 192.0 | $\mu s$ |
| $V_S$ to $V_S$ | Vertical Sync to Vertical Sync Time Period | | 16.66 | | ms |

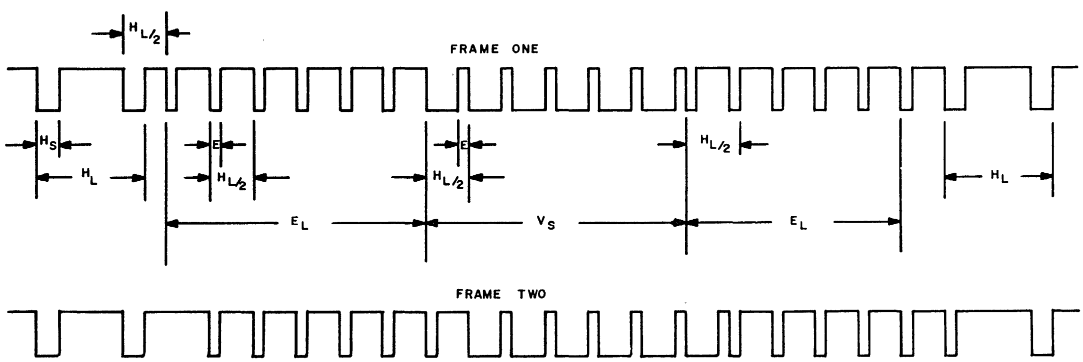
**Notes**

1. The color burst signal is the 3.579545 MHz color phase reference from which all other color information is measured.
   For Example: Full intensity blue is a 3.579545 MHz signal which has a relative delay of 135ns from burst if the burst signal was available throughout the entire $H_L$ period.
2. The number of $H_L$ periods between $V_S$ periods is 262.5 in the interlace mode.
3. The number of $H_L$ periods between $V_S$ periods in the non-interlace mode is 262 per frame.
4. NTSC only.

## Composite SYNC, Color and Luminance




## Composite SYNC Output



# commodore semiconductor group

## NMOS

# 6562/6563
# Video Interface Chip (VIC)

- **Fully Programmable System With 16K Byte Address Space**
- **Mask-programmable Sync Generation (NTSC-6562 or PAL-6563)**
- **On-Chip Color Generation**
- **Up to 1000 Independently Programmable and Movable Background Locations**
- **Screen Grid Size Up to 320 x 200**
- **Two Selectable Graphic Character Sizes**
- **On-Chip Sound System**
- **On-Chip DMA and Address Generation**
- **16 Addressable Control Registers**
- **Light Gun/Pen for Target Games**

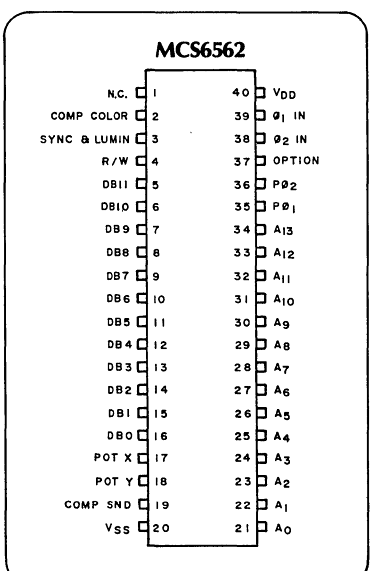
## DESCRIPTION

The MCS6562/6563 is functionally nearly identical to the MCS6560/6561 described in this section of the Data Catalog. Like the 6560/6561, the 6562/6563 is designed to be used in implementing color video graphics applications such as low-cost CRT terminals, biomedical monitors, control system displays and arcade/home video games. It provides all circuitry necessary for generating color programmable character graphics with high-screen resolution. VIC also incorporates sound effects and A/D converters for use in a video game environment.

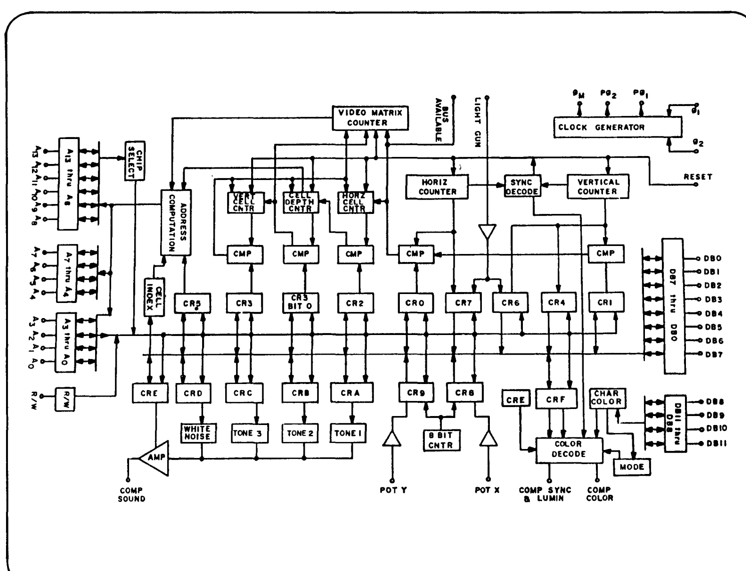
Principal differences between the 6562/6563 and the 6560/6561 lie in the size of screen display attainable. The 6562/6563 is capable of up to 1000 independently programmable and movable background locations on a standard TV and the screen grid may be up to 320 horizontal dots by 200 vertical dots. In addition, the 6562/6563 sound synthesizer produces three waveforms and features three amplitude modulators, along with programmable frequency and programmable noise generator.

In virtually all other respects, the 6562/6563 is identical to the 6560/6561 and the interested reader is referred to that data sheet in the Data Catalog for further discussion.

## PIN CONFIGURATION




## BLOCK DIAGRAM




**Note**
MCS = Ceramic package
MPS = Plastic package

## THEORY OF OPERATION

In order to produce programmable color characters, VIC access external memory which can be divided into three areas: character pointers, display characters and color pointers. The character pointer area is a block of bytes in RAM (typically 920 bytes called the Video Matrix) in which each byte points to a particular character to be displayed. The character area consists of a set of 8 or 32 byte blocks (usually called cells) which contain the actual dot patterns to be displayed. These character cells can be located in either RAM or ROM depending on how the objects are to be displayed or moved on the screen. The color pointer area is a block of nybbles in RAM (typically 920-4 bit nybbles called the Color Matrix). The 4 bit color pointers are used to define the color of any character which is to be displayed and to select one of the two color modes.

It is the task of an external microprocessor to organize the Video Matrix, Color Matrix and Character Cells into the proper format to display the data desired on-screen.

To understand the operation of VIC more completely, consider the diagram shown in Figure 1. This is a typical Video Matrix, in which 40 characters horizontally by 23 characters vertically are to be displayed, yielding a total of 920 character display locations, with a screen resolution of 320 horizontal by 184 vertical dots. Each one of these character display locations has a corresponding character pointer, or index, which specifies (points at) a character to be displayed in that particular location. In the example shown, rectangle (B,27) has a character index of 2B. This means character number 2B is to be displayed in that rectangle. VIC will fetch the character index value 2B and perform an address computation to locate the desired character to be displayed. The computation is quite simple. If 8 x 8 character cells are selected, the index is left shifted 3 times (multiply by 8) and the starting address of the character cells, found in VIC Control Register $CR_5$, is added to the left shifted value. In this case, the character cell starting address is 3000 (in HEX) which is added to the left shifted value of the character index to yield the actual character location in memory of 3158 (in HEX). Note here that the actual character displayed is an eight dot by eight dot matrix which can be stored in either ROM or RAM. Also, the number of times that any particular character can be displayed is unlimited. By using the same character index (2B for example) elsewhere on the grid, the character data will be displayed again. Alternately, through the use of a simple software driver, VIC can be used as a bit-mapped display system provided enough RAM is available (approximately 8K bytes of cell RAM).

**TYPICAL VIDEO MATRIX**
**(23 x 40)**

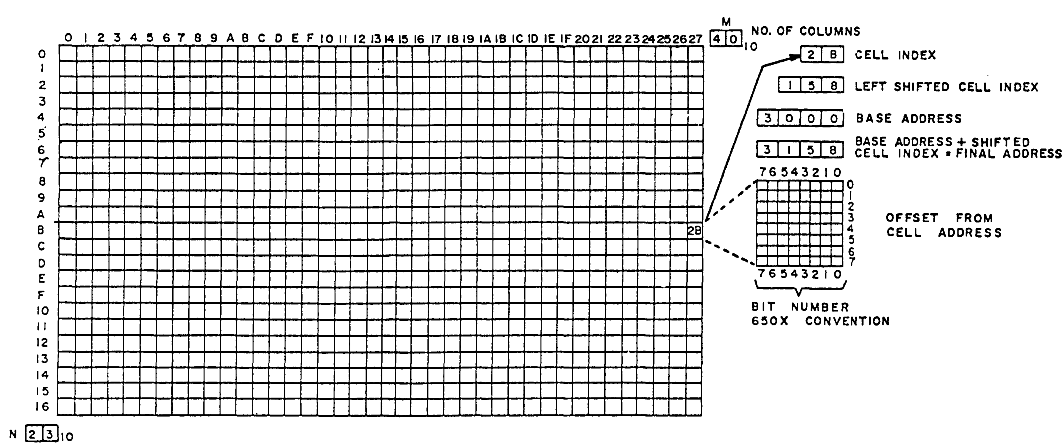



**FIGURE 1**

## VIC CONTROL REGISTERS

1000 ORIGIN

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | (bit number) |
|---|---|---|---|---|---|---|---|---|---|---|
| $CR_0$ | 1000 | I | $S_X^6$ | $S_X^5$ | $S_X^4$ | $S_X^3$ | $S_X^2$ | $S_X^1$ | $S_X^0$ | SCREEN ORIGIN X-COORDINATE |
| $CR_1$ | 1001 | $S_Y^7$ | $S_Y^6$ | $S_Y^5$ | $S_Y^4$ | $S_Y^3$ | $S_Y^2$ | $S_Y^1$ | $S_Y^0$ | SCREEN ORIGIN Y-COORDINATE |
| $CR_2$ | 1002 | R | $M_6$ | $M_5$ | $M_4$ | $M_3$ | $M_2$ | $M_1$ | $M_0$ | NO. OF VIDEO MATRIX COLUMNS |
| $CR_3$ | 1003 | $R_0$ | $N_5$ | $N_4$ | $N_3$ | $N_2$ | $N_1$ | $N_0$ | D | NO. OF VIDEO MATRIX ROWS |
| $CR_4$ | 1004 | $R_8$ | $R_7$ | $R_6$ | $R_5$ | $R_4$ | $R_3$ | $R_2$ | $R_1$ | RASTER VALUE |
| $CR_5$ | 1005 | $B_V^{13}$ | $B_V^{12}$ | $B_V^{11}$ | $B_V^{10}$ | $B_C^{13}$ | *$B_C^{12}$ | *$B_C^{11}$ | N | BASE ADDRESS CONTROL |
| $CR_6$ | 1006 | $L_H^7$ | $L_H^6$ | $L_H^5$ | $L_H^4$ | $L_H^3$ | $L_H^2$ | $L_H^1$ | $L_H^0$ | LIGHT PEN HORIZONTAL |
| $CR_7$ | 1007 | $L_V^7$ | $L_V^6$ | $L_V^5$ | $L_V^4$ | $L_V^3$ | $L_V^2$ | $L_V^1$ | $L_V^0$ | LIGHT PEN VERTICAL |
| $CR_8$ | 1008 | $P_X^7$ | $P_X^6$ | $P_X^5$ | $P_X^4$ | $P_X^3$ | $P_X^2$ | $P_X^1$ | $P_X^0$ | POT X |
| $CR_9$ | 1009 | $P_Y^7$ | $P_Y^6$ | $P_Y^5$ | $P_Y^4$ | $P_Y^3$ | $P_Y^2$ | $P_Y^1$ | $P_Y^0$ | POT Y |
| $CR_A$ | 100A | $A_2^3$ | $A_2^2$ | $A_2^1$ | $A_2^0$ | $A_1^3$ | $A_1^2$ | $A_1^1$ | $A_1^0$ | AMPLITUDE 1,2 |
| $CR_B$ | 100B | $F_1^7$ | $F_1^6$ | $F_1^5$ | $F_1^4$ | $F_1^3$ | $F_1^2$ | $F_1^1$ | $F_1^0$ | $F_{IN}^{(1)}$ (SAWTOOTH) |
| $CR_C$ | 100C | $F_2^7$ | $F_2^6$ | $F_2^5$ | $F_2^4$ | $F_2^3$ | $F_2^2$ | $F_2^1$ | $F_2^0$ | $F_{IN}^{(2)}$ (PULSE) |
| $CR_D$ | 100D | $F_3^7$ | $F_3^6$ | $F_3^5$ | $F_3^4$ | $F_3^3$ | $F_3^2$ | $F_3^1$ | $F_3^0$ | $F_{IN}^{(3)}$ (SQUARE/ NOISE) |
| $CR_E$ | 100E | $C_A^3$ | $C_A^2$ | $C_A^1$ | $C_A^0$ | $A_3^3$ | $A_3^2$ | $A_3^1$ | $A_3^0$ | AMPLITUDE 3 |
| $CR_F$ | 100F | $C_B^3$ | $C_B^2$ | $C_B^1$ | $C_B^0$ | $C_E^3$ | $C_E^2$ | $C_E^1$ | $C_E^0$ | COLOR CONTROL |

**Note**
*These bits ignored when D = 1

**REGISTER DESCRIPTION**

There are sixteen eight-bit control registers within the 6562 which enable the microprocessor to control all the operating modes of VIC. The control and their functions are tabulated and explained below.

**EXPLANATION OF CONTROL REGISTER FUNCTIONS**

$CR_0$: Bits 0-6 determine how far from the left-hand side of the T.V. screen the first column of characters will appear. It is used to Horizontally center various sizes of video matrices on-screen. Bit 7 selects interlaced scan mode (I = 1).

$CR_1$: Determines how far from the top of the T.V. screen the first row of characters will appear. It is similarly used to Vertically center various sizes of video matrices on-screen.

$CR_2$: Bits 0-6 set the number of columns in the Video Matrix. Bit 7 is the Color Invert bit, as explained under $CR_F$.

$CR_3$: Bits 1-6 set the number of rows in the Video Matrix. Bit 0 is used to select either 8 x 8 character matrices (D = 0) or 32 x 8 character matrices (D = 1).* Bit 7 is part of the RASTER value found in $CR_4$.

$CR_4$: Contains the number of the line currently being scanned by the T.V. raster beam.

$CR_5$: Bits 1-3 determine the starting address of the character cell space. (Note that these bits from bits A13 through A11 of the actual address.) Bits 4-7 determine the starting address of the Video Matrix (these bits from bits A13 through A10 of the actual address). Bit 0 allows sound oscillator 3 to produce either variable frequency noise (N = 1) or a variable frequency square wave (N = 0).

$CR_6$: Contains the latched horizontal position of the light gun/pen.

$CR_7$: Contains the latched vertical position of the light gun/pen.

$CR_8$: Contains the digitized value of POTX.

$CR_9$: Contains the digitized value of POTY.

$CR_A$: Bits 0-3 set the amplitude of sound oscillator 1, bits 4-7 set the amplitude of oscillator 2.

$CR_B$: Bits 0-7 set the frequency of oscillator 1, (sawtooth waveform).

$CR_C$: Same as $CR_B$ for sound oscillator 2 (pulse waveform).

$CR_D$: Same as $CR_B$ for sound oscillator 3 (noise/squarewave).

$CR_E$: Bits 0-3 set the amplitude of oscillator 3. Bits 4-7 contain the Auxiliary color code used in conjunction with the "Multicolor" mode of operation.

$CR_F$: Bits 4-7 select 1 of 16 colors for the background common to all characters. (Essentially, they set the color of the background area within the Video Matrix.) Bits 0-3 select 1 of 16 colors for the exterior border area of the screen (all area outside the Video Matrix). The invert bit (R), found in $CR_2$, determines whether the Video Matrix will be displayed as different colored characters on a common background color (R = 1) or inverted (R = 0), that is, all characters will be the same color (the background color in $CR_F$) while each character's background will now be a different color, determined by the code in the Color RAM. Note that the R bit has no effect when Multicolor mode is selected and that $CR_F$ also functions differently in this mode. Refer to the section called "Operating Modes" for complete information.

**NOTE**

* The 32 x 8 character mode is designed primarily to allow bit-mapping the entire screen.

**COLOR OPERATING MODES**

VIC incorporates two modes of color operation. HI-RES (high resolution) mode and Multicolor mode. Basically, the operating mode affects how the Character Cell information will be translated into dots on the TV screen. The operating mode is determined by the MSB of the color pointer associated with each character location in the Video Matrix. If the MSB of a character's color pointer is zero, then that character will be displayed in HI-RES mode. Alternately, if the MSB is one, the character will be displayed in Multicolor mode.

With HI-RES mode selected, there is a one-to-one correspondence between Character Cell bits and the dots displayed on-screen. That is, all one bits of a character will be displayed in one color, and all zero bits in another color. The foreground color of the character is specified by the remaining 3 bits of the character's color pointer, while the character's background color is specified by Register F ($CR_F$).

With Multicolor mode selected, each TWO bits of a character cell correspond to ONE dot on-screen and the color of that dot is determined by the two-bit code. Unlike HI-RES mode, in which only two colors can be displayed in a single character, Multicolor mode allows four colors per character; however, since two bits of cell data now correspond to a single dot on-screen, the horizontal resolution is half that of the HI-RES mode. That is, each 8 x 8 Character Cell in memory maps onto an 8 x 4 character on-screen (8 lines of 4 dots each). Note that the amount of memory required for these 8 x 4 Multicolor characters is the same as that for 8 x 8 HI-RES characters, the data is simply mapped differently on-screen.

In Multicolor mode, the two bits which make up a dot select one of four colors for that dot. The four codes created by these two bits tell VIC where to find the color information for the dot. The color of the dot can be either the Background color (in $CR_F$), the Exterior Border color (in $CR_F$), the Auxiliary color (in $CR_E$) or the Foreground color (bits 0 thru 2 of the character's color pointer).

The Multicolor mode color select codes are:

00 – Background color ($CR_F$)
01 – Exterior Border color ($CR_F$)
10 – Foreground color (Color RAM)
11 – Auxiliary color ($CR_E$)

Note that the two-bit code is NOT itself a color code, rather it is a pointer to four different color codes, allowing greater color flexibility, as each code pointed to has either 3 or 4-bit resolution.

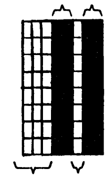
**EXAMPLE:**

| | | |
|---|---|---|
| Given: | $CR_F = 17$ | Character Background color is WHITE (1), Exterior Border color is YELLOW (7). |
| | $CR_2 = 8X$ | Invert is not selected (R = 1). |
| | $CR_E = 6X$ | Auxiliary color is BLUE (6). |

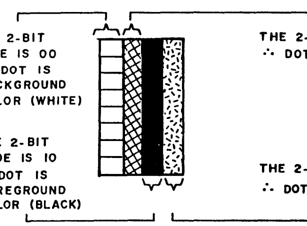
and a character definition of:

| | bit 76543210 | HEX |
|---|---|---|
| byte 0 | 00011011 | 1B |
| 1 | 00011011 | 1B |
| 2 | 00011011 | 1B |
| 3 | 00011011 | 1B |
| 4 | 00011011 | 1B |
| 5 | 00011011 | 1B |
| 6 | 00011011 | 1B |
| 7 | 00011011 | 1B |

If the color pointer nybble for that character is 0 (0000), then the Foreground color is BLACK (0) and HI-RES mode is selected (MSB = 0). The character will then appear on-screen as:




If the color pointer nybble for that character is 8 (1000), then the Foreground color is BLACK (0) and Multicolor mode is selected (MSB = 1). The character will then appear on-screen as:




**Note**
This is given solely as an example and due to color transition limitations of most TV sets, closely spaced dots of different colors will not appear sharply defined on-screen.

Since the mode of display for a character is selected by the character's color pointer and each character location on-screen has a unique color pointer, it is possible to freely intermix HI-RES and Multicolor characters. This provides great display flexibility, allowing HI-RES characters for alphanumerics, etc. and Multicolor characters for a wider array of colors available simultaneously.

**EXAMPLE OF VIC CONTROL REGISTER USE:**

For simplicity, assume all characters are in the HI-RES mode and the VIC Registers are loaded with the following values:

| Reg | Contents (HEX) | Binary | Results |
|---|---|---|---|
| $CR_0$ | 0B | 0/000 1011 | Moves Video Matrix over 11(x4) dot widths from the left side of the screen. Interlace is not selected (I = 0). |
| $CR_1$ | 32 | 0011 0010 | Moves Video Matrix down HEX 32 dot heights from top of screen. |
| $CR_2$ | A8 | 1/010 1000 | Sets HEX 28 (=40 base 10) columns in Video Matrix. Invert is not selected (R = 1). |
| $CR_3$ | 2E | X/010 111/0 | Sets 010111 (=23 base 10) rows in Video Matrix. 8 x 8 character matrices are selected (D = 0). |
| $CR_5$ | Should be set to access the proper memory locations of the specific system. Suppose it is desired to locate the Video Matrix starting at address HEX 0400, and the character matrices starting at address HEX 3000. In order to accomplish this, $CR_5$ is set: | | |
| $CR_5$ | 1D<br>This would create a 14-bit address of the form:<br>$CR_5$ BITS<br>76 54<br>00 01XX XXXX XXXX<br>0 4 0 0<br>for the Video Matrix.<br>It would also create a 14-bit address of the form:<br>$CR_5$ BITS<br>32 1<br>11 0XXX XXXX XXXX<br>3 0 0 0<br>for the character matrices. | 0001 110/1 | Noise is selected (N = 1). |
| $CR_A$ | 0F | 0000 1111 | Oscillator 1 is at full volume. Oscillator 2 is Off. |
| $CR_B$ | 1A | 0001 1010 | Oscillator 1 has a relative frequency of 1A. |
| $CR_C$ | 00 | 0000 0000 | Oscillator 2 has a relative frequency of 0. |
| $CR_D$ | 25 | 0010 0101 | Oscillator 3/Noise generator has a relative frequency of 25. |
| $CR_E$ | X3 | XXXX 0011 | Oscillator 3 has a relative volume of 3. |
| $CR_F$ | 06 | 0000 0110 | The background color common to all characters is black (0), the border color is dark blue (6) and since R = 1, each character is displayed in its own color on the black background. |

These register values will produce a screen with a properly centered Video Matrix of 23 x 40 characters, each character appearing in color on a black background, with a dark blue border surrounding the Video Matrix area. Additionally, the sound effects generator will be producing a pitched oscillation, along with white noise.

All of these registers can be modified to produce different effects.

For example: If the number in $CR_0$ is increased, the Video Matrix region will shift farther to the right.
If the number in $CR_B$ is reduced, the frequency of oscillator 1 will go down.
If $CR_2$ is changed to 28 (turning R OFF), the border will remain dark blue, but now the Video Matrix will appear as black characters on different colored backgrounds.

In order for VIC to produce a picture on-screen, the number of rows and columns and appropriate centering values must be loaded into the proper registers.

## 6562 PIN SIGNAL DESCRIPTION

### Address Bus—Pins 21 thru 34

The 14 bit address bus ($A_0$ thru $A_{13}$) is bidirectional. During $P\phi_2 = 1$, the address pins are in the input mode. In this mode the microprocessor can access any of the sixteen VIC Control Registers. The high order pins of the Address Bus ($A_8$ thru $A_{13}$) act as Chip Select pins in this input mode. A true chip select condition occurs when $A_{13} = A_{11} = A_{10} = A_9 = A_8 = 0$ and $A_{12} = 1$, which equates to a VIC chip select address of 1000 in HEX. The lower order 4 bits of the address bus ($A_0$ thru $A_3$) are used as the control register select portion of the input address.

During $P\phi_1 = 1$, the VIC address pins will be in the output mode if data (either Character Pointer or Character Cell) is to be fetched. In this mode, VIC will put out the address of the memory location to be fetched. The address form VIC will be valid 50 ns after the rising edge of $P\phi_1$ and remain valid until the rising edge of $P\phi_2$.

### Read/Write—Pin 4

This signal is an input only on the 6562 and controls the flow of data between VIC and the microprocessor. When the R/W signal is low and the VIC chip select conditions have been satisfied, the microprocessor can write data into the selected VIC Control Register. If the R/W signal is high and the chip select conditions have been met, the microprocessor can read data from the selected VIC Control Register.

It is important to note that all VIC/microprocessor data transfers can only occur when $P\phi_2 = 1$. During $P\phi_1$, VIC will be fetching data from memory for display and the R/W signal must be held high to insure that VIC will not write into any memory location.

### Data Bus—Pins 5 thru 16

The 12 bit data bus of the 6562, $DB_0$ thru $DB_{11}$, is divided into two sections. The lower order eight bits, $DB_0$ thru $DB_7$, are used both to interface to the microprocessor and fetch data needed for display, while the higher order 4 bits are used exclusively for retrieving color and mode information. The operation of the lower order eight bits ($DB_0$ thru $DB_7$) can also be separated into two categories: microprocessor interface and video data interface. During $P\phi_2 = 1$, $DB_7$ thru $DB_0$ are used exclusively for data transmission between the microprocessor and VIC. During $P\phi_1 = 1$, $DB_7$ thru $DB_0$ are used for fetching display data.

## CLOCKS

### Master Oscillator Clock Inputs—$\phi_1$ and $\phi_2$, Pins 39 and 38.

The 6562 requires a 14.31818 MHz (NTSC), TWO Phase Clock. The clock signals must be five (5) volts and non-overlapping. The 6563 requires an 8.867236 MHz clock for PAL standard.

### System Clocks—$P\phi_1$ and $P\phi_2$, Pins 35 and 36

These clocks are the master timing generator for the VIC System. They are five volt, non-overlapping 1.8 MHz clocks capable of driving the capacitance of the 6512A microprocessor.

### Analog to Digital Converters—POTX and POTY, Pins 17 and 18

These input pins are used to convert potentiometer position into a microprocessor readable 8 bit HEX number. This is accomplished by a simple RC time constant integration technique. The potentiometer is used to charge an external capacitor tied to the pot pin. Refer to application note No. 1 (Insert)

### Composite Sound—Pin 19

This pin provides the output of the sound synthesizer portion of the 6562 shown in the VIC Block Diagram. It is a high impedance output and must be buffered and amplified externally to drive a speaker.

### Composite Sync and Luminance—Pin 3

This pin is an open drain output which provides all the necessary video synchronization and luminance information required by a standard television. Refer to application note No. 1 (insert).

### Composite Color—Pin 2

This signal provides the necessary color information required by a standard television to receive a full color picture. The composite color pin is a high impedance output buffer which provides the reference burst signal plus the color encoded phase and amplitude information at the proper 3.579545 MHz frequency. Refer to application note No. 1 (insert).

### Reset—(Option), Pin 37

This input signal is used to synchronize the horizontal and vertical sync counter to an external signal.

**Bus Available—(Option), Pin 37**
This output signal indicates the state of VIC with respect to the video memory fetch. The pin will go low 1 $\mu$sec. before VIC performs any memory access and will remain low until the end of the current screen line. It is possible to access VIC registers or video RAM before and after an active screen line.

**Light Gun/Pen—(Option), Pin 37**
This input signal causes the current dot position being scanned onto the screen to be latched into control registers 6 and 7, upon a negative going edge. This pin would be used in conjunction with a photo detector for use in a "target shoot" type game or for light pen applications. Refer to application note No. 1 (insert).

**NOTE**
**OPTION ALTERNATIVES**
1 LIGHT PEN – Negative edge triggered latch of raster position/6562-101.
2 RESET – Reset Horizontal and Vertical counters to Vertical Sync./6562-201
3 BUS AVAILABLE – Pin is low when VIC is displaying data/6562-301

**AVAILABLE AUXILIARY/BACKGROUND/ BORDER COLORS**

| | |
|---|---|
| 0 BLACK | 8 ORANGE |
| 1 WHITE | 9 LIGHT ORANGE |
| 2 RED | A PINK |
| 3 CYAN | B LIGHT CYAN |
| 4 MAGENTA | C LIGHT MAGENTA |
| 5 GREEN | D LIGHT GREEN |
| 6 BLUE | E LIGHT BLUE |
| 7 YELLOW | F LIGHT YELLOW |

**AVAILABLE CHARACTER COLORS**
0 BLACK
1 WHITE
2 RED
3 CYAN
4 MAGENTA
5 GREEN
6 BLUE
7 YELLOW

**MCS6562 ELECTRICAL SPECIFICATION**

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Ambient Temperature under Bias | −10° to 80°C |
| Storage Temperature | −65°C to 150°C |
| Voltage on any Pin* | −0.5 V to + 7 V |
| Power Dissipation | 1.0 W |

*With respect to Ground

**COMMENT**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

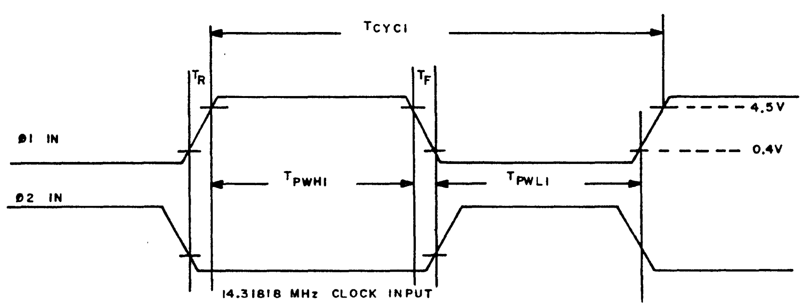
**D.C. CHARACTERISTICS** $T_A$ = 0°C to +50°C, $V_{DD}$ = 5 V ± 5% (unless otherwise specified)

| CHARACTERISTIC | MIN. | MAX. | TYP. | UNITS |
|---|---|---|---|---|
| Read/Write, Reset (Option), Address and Data-Input State | | | | |
| $V_{IL}$ | −0.2 | 0.4 | – | Volts |
| $V_{IH}$ | 2.4 | 5.6 | – | Volts |
| Input Capacitance | – | 8.0 | 5.0 | pF |
| Input Leakage (all outputs in high impedance state) | – | 10.0 | 1.0 | $\mu$A |
| Address and Data-Output State | | | | |
| $V_{OL}$ | – | 0.4 | – | Volts |
| $V_{OH}$ | 2.4 | – | – | Volts |
| $I_{OL}$ – Sink current $V_{OL}$ = 0.4 | 2.4 | – | – | mA |
| $I_{OH}$ – Source current $V_{OH}$ = 2.4 | 200 | – | – | $\mu$A |
| Impedance in Three State Condition | $1 \times 10^6$ | – | – | Ohms |
| Clock Input ($\phi_1$ and $\phi_2$ Input) | | | | |
| Frequency | – | – | 14.31818 | MHz |
| Capacitance | – | 10.0 | – | pF |
| $V_{IL}$ | −0.2 | 0.3 | – | Volts |
| $V_{IH}$ | 4.5 | – | 5.0 | Volts |
| Clock Outputs ($P\phi_1$, $P\phi_2$) | | | | |
| $V_{OL}$ | – | 0.3 V | – | Volts |
| $I_{OL}$ @ 0.3 Volts $V_{OL}$ | 1.6 | – | – | mA |
| $V_{OH}$ | $V_{DD}$−.2 | – | – | Volts |
| $I_{OH}$ @ 4.7 Volts $V_{OH}$ | 200 | – | – | $\mu$A |
| Loading | – | 120.0 | – | pF |
| Frequency | – | – | 1.8 | MHz |

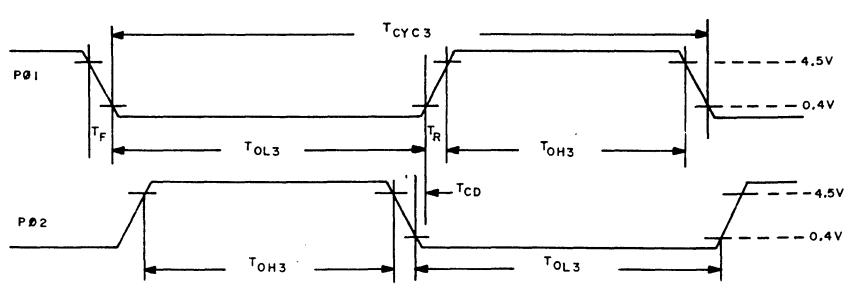
**MCS6562 ELECTRICAL SPECIFICATIONS (Continued)**

| CHARACTERISTIC | MIN. | MAX. | TYP. | UNITS |
|---|---|---|---|---|
| Composite Sound | | | | |
| Output Impedance | – | 2000 | 1000 | Ω |
| Max. Current (Sink or Source) | – | 500 | – | μA |
| Output Offset Voltage | 2.2 | 2.8 | 2.5 | Volts |
| $V_{OH}$ (Max. Amplitude-all oscillators) | 3.7 | – | 4.0 | Volts |
| $V_{OL}$ (Max. Amplitude-all oscillators) | – | 1.3 | 1.0 | Volts |
| $V_{OH}$ (Min. Amplitude-one oscillator) | 2.55 | – | 2.6 | Volts |
| $V_{OL}$ (Min. Amplitude-one oscillator) | – | 2.45 | 2.4 | Volts |
| Pot Inputs | | | | |
| $V_{TRIGGER}$ (Rising Edge) | 2.2 | 2.8 | 2.5 | Volts |
| Pot Reset | | | | |
| $V_{OL}$ | – | 0.2 | – | Volts |
| $I_{OL}$ @ $V_{OL} = 0.2$ | 500 | – | – | μA |
| Light Pen Input (Option) | | | | |
| $V_{TRIGGER}$ (Falling Edge) | 2.8 | 2.2 | 2.5 | Volts |
| Bus Available (Option) | | | | |
| $V_{OL}$ | – | 0.3 | – | Volts |
| $I_{OL}$ | 1.6 | – | – | mA |
| $V_{OH}$ | 2.4 | – | – | Volts |
| $I_{OH}$ | 10 | – | – | μA |
| $V_{DD}$ | 4.75 | 5.25 | 5.00 | Volts |
| $I_{DD}$ | – | 150 | 120 | mA |

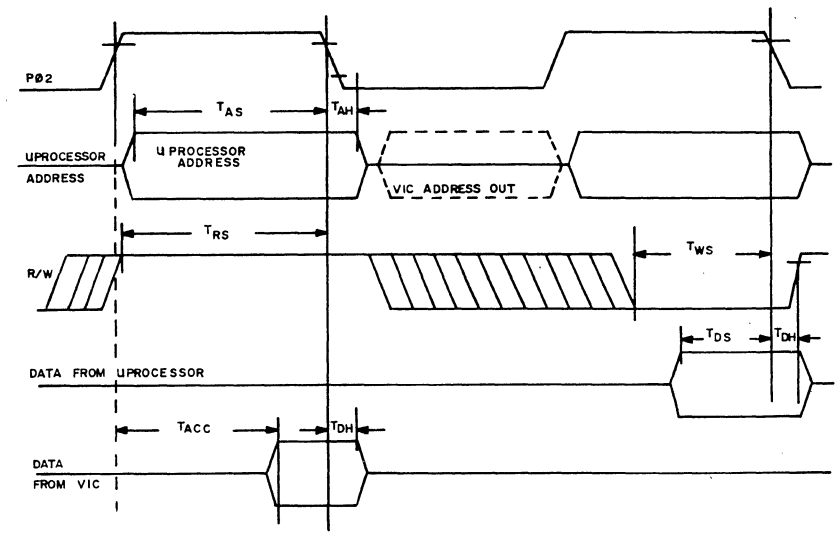
**VIC INPUT CLOCKS**



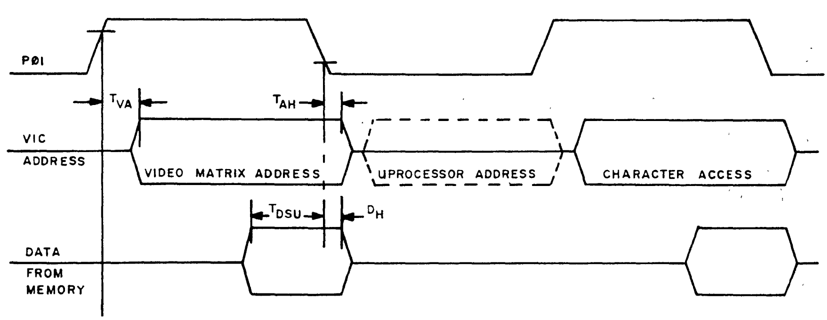

**VIC OUTPUT CLOCKS**



## MICROPROCESSOR READ/WRITE TIMING TO VIC




## VIC READ TIMING FROM MEMORY



## VIC SYSTEM TIMING

### VIC INPUT CLOCK TIMING

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| $T_{CYC1}$ | Input Clock Cycle Time | 69.82 | – | 69.84 | ns |
| $T_{PWH1}$ | Clock High | 20 | – | – | ns |
| $T_{PWL1}$ | Clock Low | 20 | – | – | ns |
| $T_R$, $T_F$ | Rise and Fall Time | – | – | 10 | ns |

### VIC OUTPUT CLOCK TIMING

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| $T_{CYC3}$ | 1.8 MHz μProcessor Clocks Cycle Time | 548 | – | 566 | ns |
| $T_{OL3}$ | $P\phi_1$, $P\phi_2$ Clocks Low | 240 | – | 286 | ns |
| $T_{OH3}$ | $P\phi_1$, $P\phi_2$ Clocks High | 240 | – | 286 | ns |
| $T_{CD}$ | Delay Time Between Clocks At .4 V | 5 | – | 20 | ns |
| $T_R$ | Rise Time, Max. $C_L$ | – | – | 40 | ns |
| $T_F$ | Fall Time, Max. $C_L$ | – | – | 20 | ns |

### MICROPROCESSOR READ/WRITE TIMING TO VIC

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| $T_{AS}$ | Address Set Up Time | 210 | – | – | ns |
| $T_{AH}$ | Address Hold Time | 5 | – | – | ns |
| $T_{RS}$ | Read Set Up Time | 210 | – | – | ns |
| $T_{WS}$ | Write Set Up Time | 150 | – | – | ns |
| $T_{DS}$ | Data In Set Up Time | 100 | – | – | ns |
| $T_{ACC}$ | Data Access Time | – | – | 200 | ns |
| $T_{DH}$ | Data Hold Time | 10 | – | – | ns |

### VIC READ TIMING FROM MEMORY

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| $T_{VA}$ | Time to Valid Address From $P\phi_1$ | – | – | 30 | ns |
| $T_{AH}$ | Address Hold Time | 10 | – | 20 | ns |
| $T_{DSU}$ | Data Set Up Time | 30 | – | – | ns |
| $D_H$ | Data Hold Time | 20 | – | – | ns |

### COMPOSITE SYNC, COLOR AND LUMINANCE TIMING

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| BLANKING | Blanking Period (No Video) | 10.0 | 11.0 | 12.0 | μs |
| $B_S$ | Breeze Way | .3 | .5 | .7 | μs |
| BURST | Color Burst Reference Signal | 4.0 | 5.0 | 6.0 | μs |

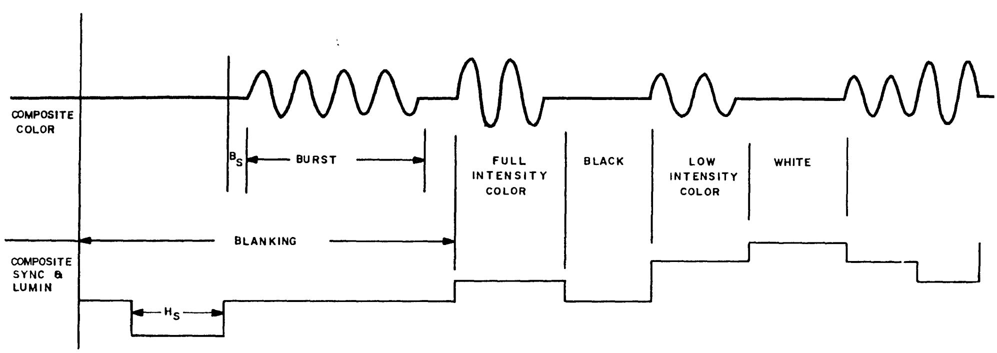
**Note**
The color burst signal is the 3.579545 MHz color phase reference from which all other color information is measured.
For Example: Full intensity blue is a 3.579545 MHz signal which has a relative delay of 135 ns from burst if the burst signal was available throughout the entire $H_L$ period.

## COMPOSITE SYNC OUTPUT TIMING

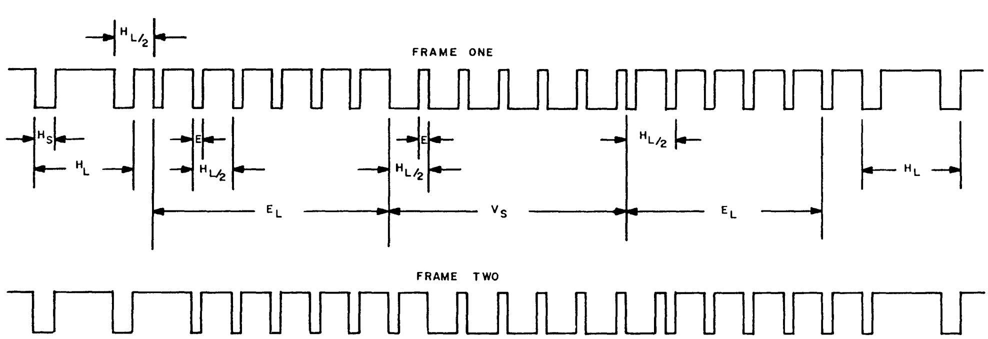
| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| $H_S$ | Horizontal Sync Pulse | 4.0 | 5.0 | 6.0 | µs |
| $H_L$ | Horizontal Line Period | 63.0 | 63.5 | 64.0 | µs |
| $H_{L/2}$ | One Half Horizontal Line Period | 30.0 | 31.5 | 32.5 | µs |
| E | Equalization Pulse | 2.0 | 2.5 | 3.0 | µs |
| $E_L$ | Equalization Time Period | 188.0 | 190.5 | 192.0 | µs |
| $V_S$ | Vertical Sync Period | 188.0 | 190.5 | 192.0 | µs |
| $V_S$ to $V_S$ | Vertical Sync to Vertical Sync Time Period | — | 16.66 | — | ms |

**Notes:**
1. The number of $H_L$ periods between $V_S$ periods is 262.5 in the interlace mode.
2. The number of $H_L$ periods between $V_S$ periods in the non-interlace mode is 262 per frame.
3. NTSC only.

## COMPOSITE SYNC, COLOR AND LUMINANCE




## COMPOSITE SYNC OUTPUT



**STANDARD SYSTEM CONFIGURATION**

A typical VIC System would consist of a microprocessor, VIC, ROM, RAM and I/O. The tasks involved in a system are divided between the $\mu$P and VIC. The $\mu$P controls the system functions (such as games) and VIC controls the Video Display.

VIC is designed to operate with 65XX microprocessors, generating the $\mu$P clocks directly (or through external dividers for slower systems). This allows the $\mu$P and VIC to alternate memory access through interleaved DMA.

A VIC System is divided into two sections; a standard speed section containing system RAM (optional), system ROM and system I/O; and a high-speed section, containing the shared high-speed (200 ns) RAM.

The shared subsystem must be isolated from the system busses via tri-state buffers whenever VIC takes control of the high-speed bus. Since the system busses are unaffected when VIC accesses the shared subsystem, all devices external to the shared subsystem can run at a slower speed, allowing standard speed system design.

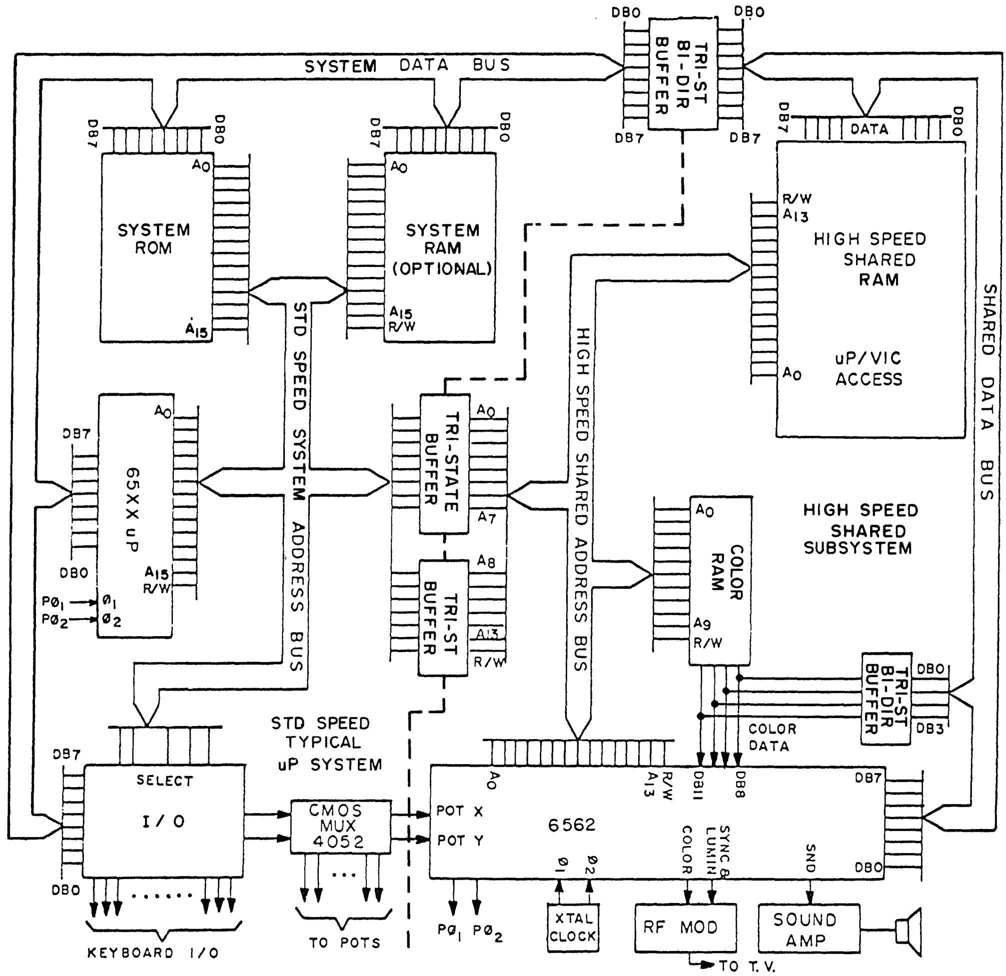
Although it is possible to incorporate all system RAM into the high-speed section of the system, it may be more cost effective to place only that RAM needed for video information in the high-speed subsystem and all other RAM outside.

Refering to the Standard System Diagram, the Tri-state buffers on the Address and Data busses allow the shared section to be isolated from the system busses during $P\phi_2$, the VIC busses tri-state and the buffers allow the $\mu$P to access the shared RAM or VIC registers.

During $P\phi_1$ the Color RAM is accessed in parallel with the Video Matrix, therefore, any VIC access of the Video Matrix also accesses the Color RAM. During $P\phi_2$ the tri-state buffer on the Color RAM allows the $\mu$P to access the Color RAM as a block of memory separate from the Video Matrix, (the Color RAM, therefore, resides in two different locations; at the same location as the Video Matrix during $P\phi_1$ and at some unique location during $P\phi_2$).

The 4052 CMOS MUX allows four joysticks to be connected to VIC. The I/O section determines which joystick will be digitized at any one time.

## STANDARD SYSTEM DIAGRAM



PRELIMINARY

# 65245
# Octal Bus Transceiver With 3-State Outputs

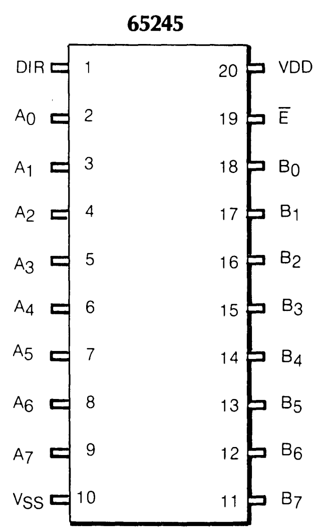
## DESCRIPTION

The 65245 is an octal bus transceiver designed for asynchronous, bi-directional communication between data busses.

The level of the Direction input (DIR) allows data transmission from bus A to bus B or from bus B to bus A. The Enable input ($\overline{E}$) can be used to provide isolation between the busses.

The device is fully TTL and CMOS compatible, and is pin-for-pin compatible with the 74LS245.

## PIN CONFIGURATION




## TRUTH TABLE

| $\overline{E}$ | DIR | Output |
|---|---|---|
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

NOTES
L = LOW level
H = HIGH level
X = Irrelevant

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | −0.3 to +7.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

## COMMENT

*This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.*

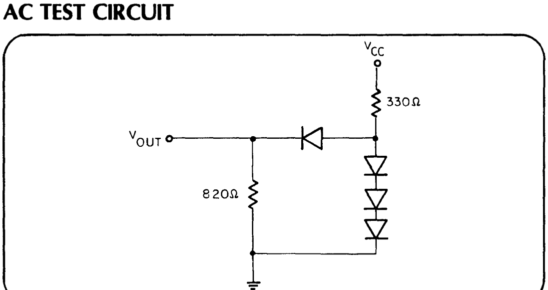
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = 0, $T_A$ = 0° to + 70°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | | V |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V |
| $V_{OH}$ | Output High Voltage<br>$V_{CC}$ = MIN, $V_{IH}$ = 2.0 V<br>$I_{OH}$ = −3 mA<br>$I_{OH}$ = −15 mA | <br><br>2.4<br>2.0 | | | V |
| $V_{OL}$ | Output Low Voltage<br>$V_{CC}$ = MIN, $V_{IL}$ = 0.8 V<br>$I_{OL}$ = 12 mA<br>$I_{OL}$ = 24 mA | | | <br><br>0.4<br>0.5 | V |
| $I_{OZH}$ | High-Impedance Output Current<br>$\bar{E}$ = 2.0 V, $V_{CC}$ = MAX, $V_{OUT}$ = 2.7 V | | | 50 | μA |
| $I_{OZL}$ | High-Impedance Output Current<br>$\bar{E}$ = 2.0 V, $V_{CC}$ = MAX, $V_{OUT}$ = −0.4 V | | | −50 | μA |
| $I_{IH}$ | High-Level Input Current<br>$V_{CC}$ = MAX, $V_{IH}$ = 2.7 V | | <br>20 | 100 | nA |
| $I_{IL}$ | Low-Level Input Current<br>$V_{CC}$ = MAX, $V_{IL}$ = 0.4 V | | <br>20 | −100 | nA |
| $I_{OH}$ | High-Level Output Current<br>$V_{CC}$ = NOM, $V_{OUT}$ = 2.4 V | | | <br>−15 | mA |
| $I_{OL}$ | Low-Level Output Current<br>$V_{CC}$ = NOM, $V_{OUT}$ = 0.4 V | | | <br>24 | mA |
| $I_{CC}$ | Power Supply Current<br>Outputs High<br>Outputs Low<br>Outputs Hi-Z | | <br>47<br>44<br>56 | <br>64<br>100<br>105 | mA |

**AC CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{SS}$ = 0 V, $T_A$ = +25°C)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Data to Output | | | 40<br>40 | ns<br>ns | |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time | | | 40<br>40 | ns<br>ns | Test Circuit |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time | | | 40<br>40 | ns<br>ns | |

**AC TEST CIRCUIT**



**commodore semiconductor group**

**NMOS**

# 2114
# Static RAM (1024 x 4)

| | 2114 | 2114L |
|---|---|---|
| Access Time (ns) | 450, 300, 200 | 450, 300 |
| Supply Current/Tolerance | 100 mA ±5% | 70 mA ±5% |

- **450, 300, Maximum Access Time**
- **Three-state Outputs for OR-Ties**
- **Directly TTL Compatible: All Inputs, Outputs and Power Supply**
- **400 mV Noise Immunity on Inputs**
- **Single 5 V Supply**
- **No Clocks or Strobes Required**
- **High-Density 18-Pin Package**
- **Identical Cycle and Access Times**

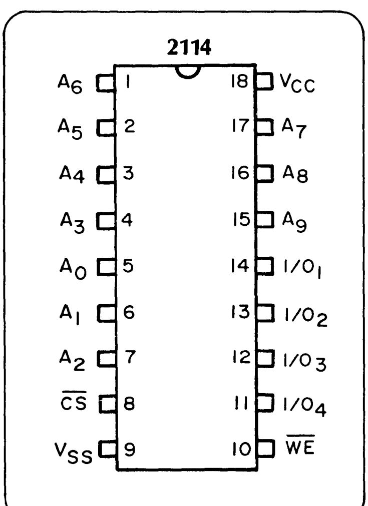
## DESCRIPTION

The MOS Technology 2114 is a 4096-bit Static Random Access Memory organized as 1024 words by 4 bits. It is fabricated using N-channel Silicon Gate technology. Because it is designed using fully DC stable (static) circuitry in both the memory array and the decoding, it requires no clock or refresh. Address setup times are not required and data is read nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of bus-oriented systems. Drive capability is 2 TTL loads.

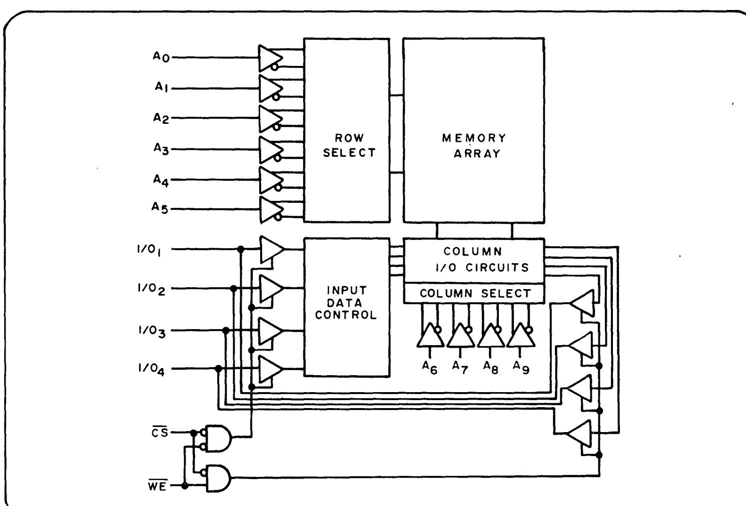
The 2114 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are important design objectives. It is totally TTL compatible in all respects. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are OR-tied.

Available in ceramic or molded packaging, the 2114 is offered in eight models. The 2114-45 (ceramic) and 2114-45 (molded) devices require a supply current of 100 mA, with a tolerance of ±5%. A 10% tolerance is obtained using the MCT (ceramic) and MPT (molded) 2114-45. Low-power models include the 2114L-45 (ceramic) and 2114L-45 (molded) devices with 70 mA supply current reuirements and ±5% tolerance as well as the ±10%-tolerance versions.

## PIN CONFIGURATION




## BLOCK DIAGRAM



**DC CHARACTERISTICS** $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$ (unless otherwise specified)

| Symbol | Parameter | MCS2114L-45 MPS2114L-45 | | MCS2114-45 MPS2114-45 | | MCT2114L-45 MPT2114L-45 | | MPT2114-45 MPT2114-45 | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| $I_{LI}$ | Input Load Current (all input Pins) | | 10 | | 10 | | 10 | | 10 | μA | $V_{IN}$ = 0 to 5.25V |
| $I_{LO}$ | I/O Leakage Current | | 10 | | 10 | | 10 | | 10 | μA | $\overline{CS}$ = 2.0 V, $V_{I/O}$ = 0.4 V to $V_{CC}$ |
| $I_{CC1}$ | Power Supply Current | | 65 | | 95 | | | | | mA | $V_{CC}$ = 5.25 V, $I_{I/O}$ = 0 mA, $T_A$ = 25°C |
| $I_{CC2}$ | Power Supply Current | | 70 | | 100 | | | | | mA | $V_{CC}$ = 5.25 V, $I_{I/O}$ = 0 mA, $T_A$ = 0°C |
| $I_{CC3}$ | Power Supply Current | | | | | | 65 | | 95 | mA | $V_{CC}$ = 5.5 V, $I_{I/O}$ = 0 mA, $T_A$ = 25°C |
| $I_{CC4}$ | Power Supply Current | | | | | | 70 | | 100 | mA | $V_{CC}$ = 5.5 V, $I_{I/O}$ = 0 mA, $T_A$ = 0°C |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | −0.5 | 0.8 | −0.5 | 0.8 | −0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V | $I_{OL}$ = 3.2 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | $I_{OH}$ = −400 μA |

**AC CHARACTERISTICS** $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$ (unless otherwise specified)

| Symbol | Parameter | MCS2114-45 MPS2114-45 MCS2114L-45 MPS2114L-45 | | MCT2114-45 MPT2114-45 MCT2114L-45 MPT2114L-45 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| | READ CYCLE | | | | | |
| $t_{RC}$ | Read Cycle Time | 450 | | 450 | | ns |
| $t_{ACC}$ | Access Time | | 450 | | 450 | ns |
| $t_{CO}$ | Chip Select to Output Valid | | 120 | | 120 | ns |
| $t_{CX}$ | Chip Select to Output Off | 0 | | 0 | | ns |
| $t_{OTD}$ | Chip Deselect to Output Off | 0 | 100 | 0 | 100 | ns |
| $t_{OHA}$ | Output Hold from Address Change | 50 | | 50 | | ns |
| | WRITE CYCLE | | | | | |
| $t_{WC}$ | Write Cycle Time | 450 | | 450 | | ns |
| $t_{AW}$ | Address to Write Setup Time | 0 | | 0 | | ns |
| $t_W$ | Write Pulse Width | 200 | | 200 | | ns |
| $t_{WR}$ | Write Release Time | 0 | | 0 | | ns |
| $t_{OTW}$ | Write to Output Off | 0 | 100 | 0 | 100 | ns |
| $t_{DW}$ | Data to Write overlap | 200 | | 200 | | ns |
| $t_{DH}$ | Data Hold | 0 | | 0 | | ns |

**CAPACITANCE** $T_A = 25°C$, f = 1.0 MHz

| Symbol | Test | Min | Max | Unit | Note | Conditions |
|---|---|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance | | 10 | pF | This parameter is periodically | $V_{I/O} = 0$ V |
| $C_{IN}$ | Input Capacitance | | 7 | pF | sampled and not 100% tested | $V_{IN} = 0$ V |

**AC CONDITIONS OF TEST**

| | |
|---|---|
| Input Pulse Levels | 0.8 V to 2.0 V |
| Input Rise and Fall Time | 10 ns |
| Timing Measurement Levels: | |
| Input | 1.5 V |
| Output | 0.8 V and 2.0 V |
| Output Load | 1 TTL Gate and 100 pF |

**ABSOLUTE MAXIMUM RATINGS**

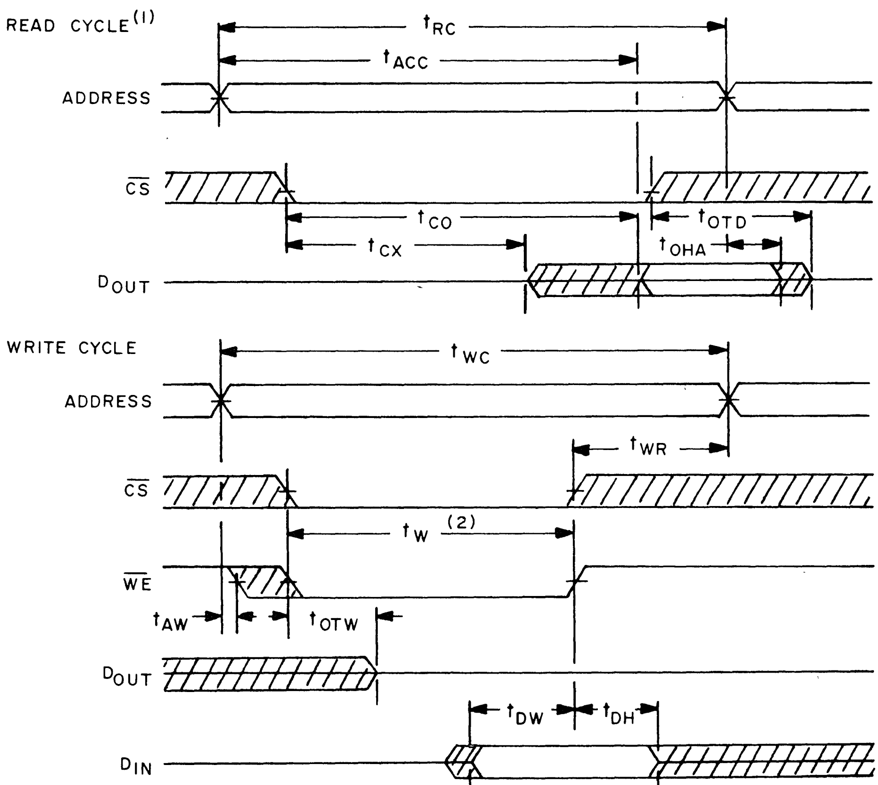
| | |
|---|---|
| Ambient Temperature under Bias | −10°C to +80°C |
| Storage Temperature | −65°C to +150°C |
| Voltage on any Pin* | −0.5 V to +7 V |
| Power Dissipation | 1.0 W |

*With respect to ground

**COMMENT**

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

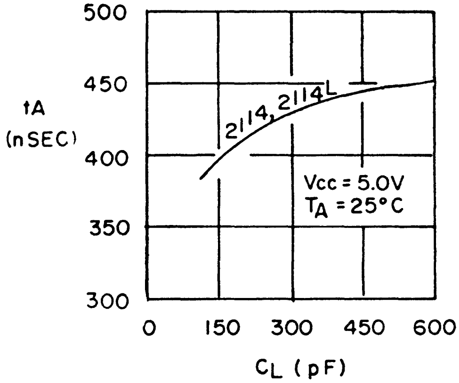
**TIMING DIAGRAMS**



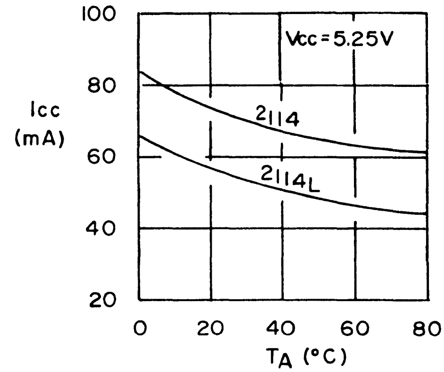

**NOTES**
1. WE is high for a Read Cycle
2. tW is measured from the latter of CS or WE going low to the earlier of CS or WE going high

## TYPICAL CHARACTERISTICS

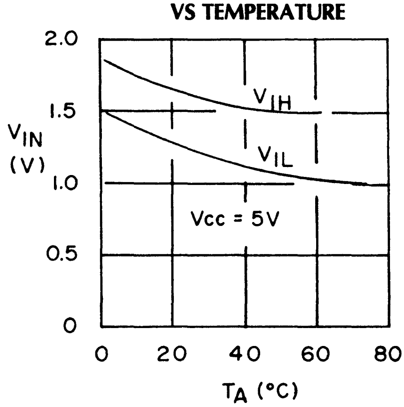
### ACCESS TIME VS CAPACITIVE LOAD



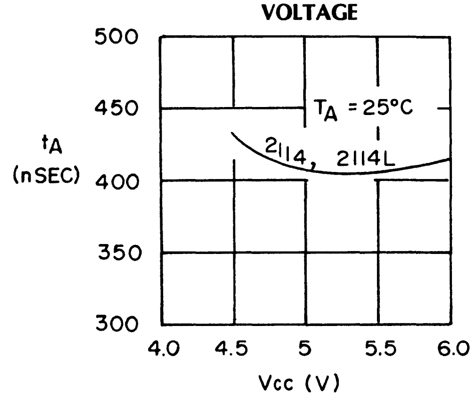

### SUPPLY CURRENT VS TEMPERATURE



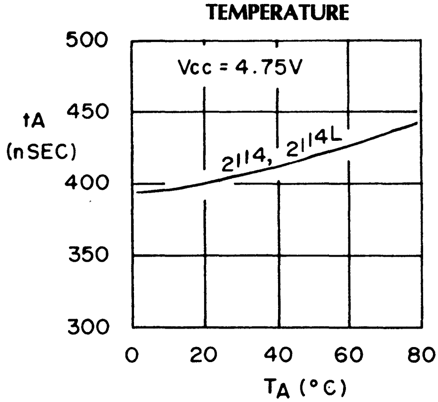

### INPUT VOLTAGE LIMITS VS TEMPERATURE



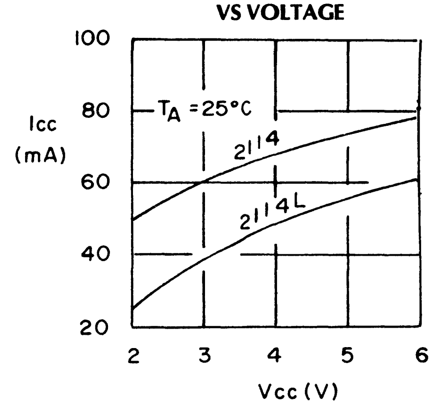

### ACCESS TIME VS VOLTAGE




### ACCESS TIME VS TEMPERATURE




### SUPPLY CURRENT VS VOLTAGE



# commodore semiconductor group

## NMOS

# 2316
# Static ROM (2048 x 8)

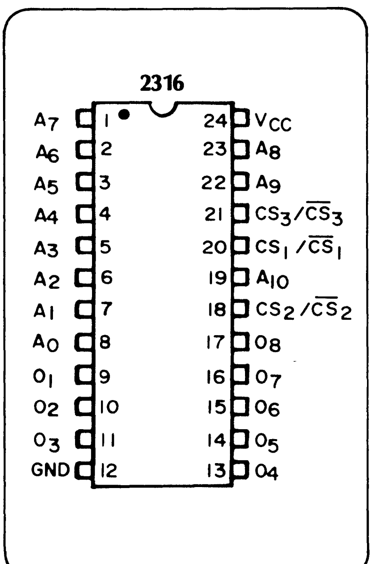
- Access Time 450 ns and 350 ns (maximum)
- Totally Static Operation
- Fully TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- Single 5 V Power Supply
- Pin Compatible With 2716 EPROM
- 400 mV Noise Immunity on Inputs
- 2708/2716 EPROMs Accepted as Program Data Inputs

### DESCRIPTION

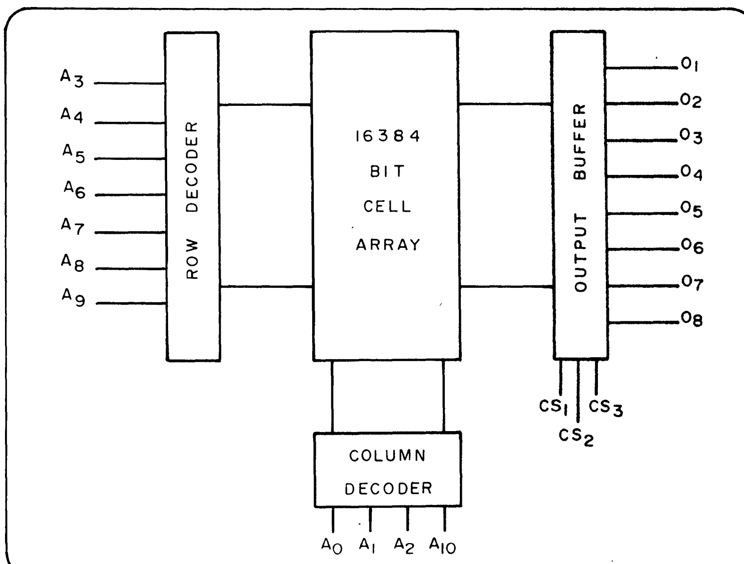
The MOS Technology 2316 is a 16,384-bit Static Read-Only Memory organized as 2048 x 8 bits. It features a fast access time (350 ns, maximum). It is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage capacity and simple interfacing requirements are important design considerations.

The 2316 operates totally asynchronously; no clock input is required. With three programmable chip select inputs, eight 16K ROMs can be OR-tied with no need for external decoding logic. Designed to replace two 2708 8K EPROMs, the 2316 can eliminate the need to redesign printed circuit boards for volume mask-programmed ROMs after prototyping is completed with EPROMs.

### PIN CONFIGURATION




### BLOCK DIAGRAM



**DC CHARACTERISTICS** $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0 V ±5% (unless otherwise specified)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $I_{CC1}$ | Power Supply Current | | 100 | mA | $V_{IN} = V_{CC}$, $V_O$ = Open, $T_A$ = 0°C |
| $I_{CC2}$ | Power Supply Current | | 95 | mA | $V_{IN} = V_{CC}$, $V_O$ = Open, $T_A$ = 25°C |
| $I_O$ | Output Leakage Current | | 10 | μA | Chip Deselected, $V_O$ = O to $V_{CC}$ |
| $I_I$ | Input Load Current | | 10 | μA | $V_{CC}$ = Max. $V_{IN}$ = O to $V_{CC}$ |
| $V_{OL}$ | Output Low Voltage | | 0.4 | Volts | $V_{CC}$ = Min. $I_{OL}$ = 2.1 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | Volts | $V_{CC}$ = Min. $I_{OH}$ = −400 μA |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | Volts | See note 1 |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$+1 | Volts | |

**AC CHARACTERISTICS** $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0 V ±5% (unless otherwise specified)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $t_{ACC}$ | Address Access Time | | 450 | ns | |
| $t_{CO}$ | Chip Select Delay | | 200 | ns | See Note 2 |
| $t_{DF}$ | Chip Deselect Delay | | 175 | ns | |
| $t_{OH}$ | Previous Data Valid After Address Change Display | 40 | | ns | |

**CAPACITANCE** $T_A$ = 25°C, f = 1.0 MHz, See Note 3

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 8 | pF | All Pins except Pin under Test Tied to AC Ground |
| $C_{OUT}$ | Output Capacitance | | 10 | pF | |

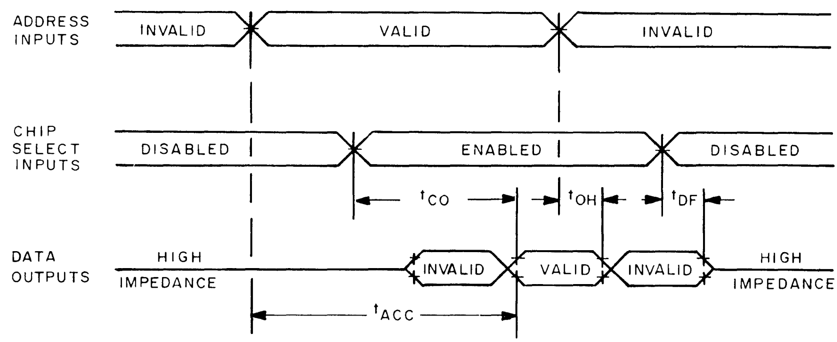
**Notes**
1. Input levels that swing more negative than −0.5 V will be clamped and may cause damage to the device.
2. Loading 1 TTL + 100 pF, input transition time: 20 ns. Timing measurement levels: input 1.5V, output 0.8V and 2.0V.
3. This parameter is periodically sampled and is not 100% tested.

**ABSOLUTE MAXIMUM RATINGS**

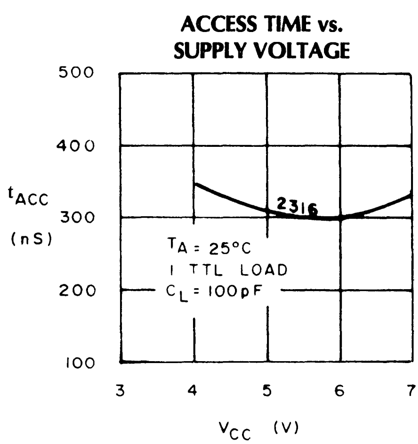
| | |
|---|---|
| Ambient Temperature Under Bias | 0° to +70°C |
| Storage Temperature | −65°C to +150°C |
| Supply Voltage to Ground Potential | −0.5v to +7.0V |
| Applied Output Voltage | −0.5V to +7.0V |
| Applied Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

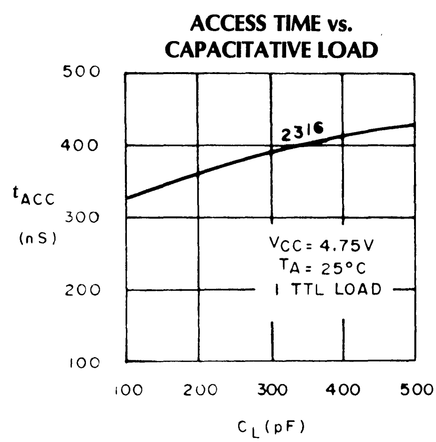
**COMMENT**
*Stresses above those listed under "Absolute Maximum Ratings" may cause permament damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

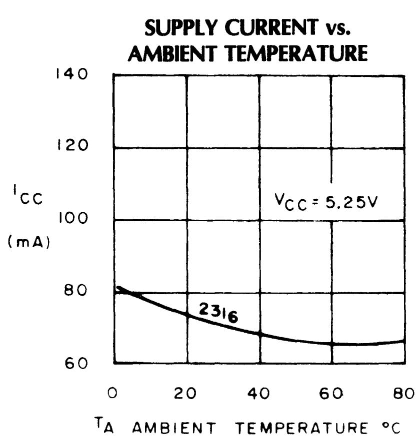
## TIMING DIAGRAM

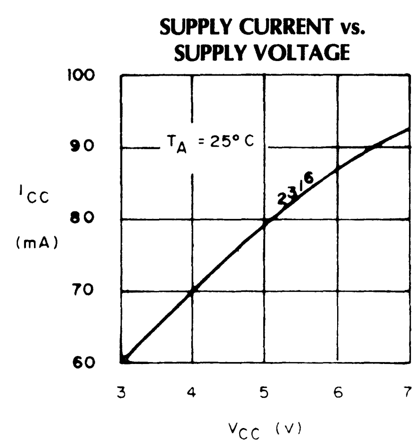



## TYPICAL CHARACTERISTICS



commodore semiconductor group

**NMOS**

# 2332
# Static ROM (4096 x 8)

| | 2332 | 2332A | 2332B |
|---|---|---|---|
| Maximum Access Time | 450 ns | 350 ns | 300 ns |

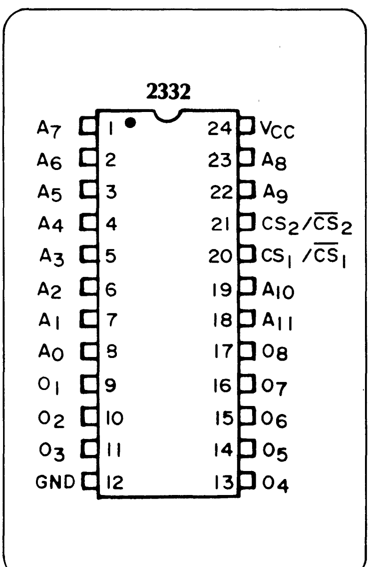
- Access Time Less Than 350ns
- Totally Static Operation
- Fully TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- Single 5V Power Supply
- Pin Compatible With 2716 & 2732 EPROMs
- 400 mV Noise Immunity on Inputs
- 2708/2716 EPROMs Accepted as Program Data Inputs

## DESCRIPTION

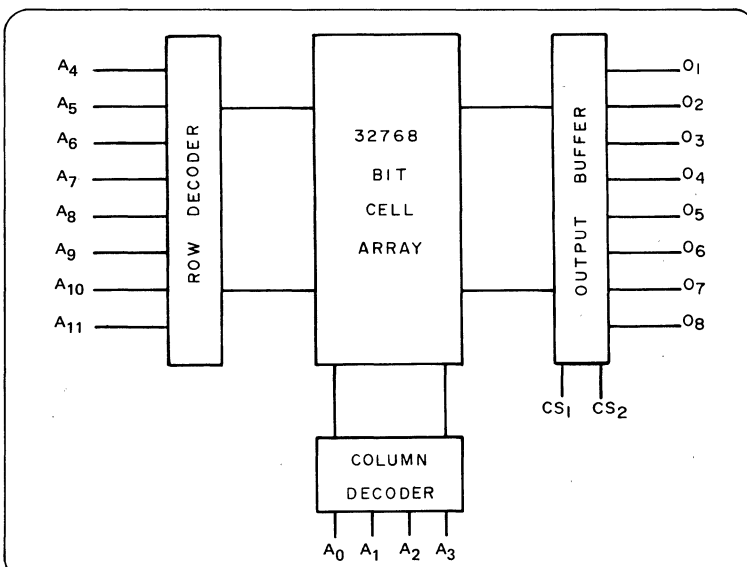
The MOS Technology 2332 is a 32,768-bit Static Read-Only Memory organized as 4096 x 8 bits. It features fast access time (450 ns maximum with the 2332, 350 ns maximum with the 2332A). The 2332 is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage capacity and simple interfacing requirements are important design considerations.

The 2332 operates totally asynchronously; no clock input is required. With two programmable chip select inputs, four 32K ROMs can be OR-tied with no need for external decoding logic. Designed to replace two 2716 16K EPROMs, the 2332 can eliminate the need to redesign printed circuit boards for volume mask-programmed ROMs after prototyping is completed with EPROMs.

## PIN CONFIGURATION




## BLOCK DIAGRAM



**DC CHARACTERISTICS** $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0 V ±5% (unless otherwise specified)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $I_{CC1}$ | Power Supply Current | | 125 | mA | $V_{IN} = V_{CC}$, $V_O$ = Open, $T_A$ = 0°C |
| $I_{CC2}$ | Power Supply Current | | 120 | mA | $V_{IN} = V_{CC}$, $V_O$ = Open, $T_A$ = 25°C |
| $I_O$ | Output Leakage Current | | 10 | μA | Chip Deselected, $V_O$ = O to $V_{CC}$ |
| $I_I$ | Input Load Current | | 10 | μA | $V_{CC}$ = Max. $V_{IN}$ = O to $V_{CC}$ |
| $V_{OL}$ | Output Low Voltage | | 0.4 | Volts | $V_{CC}$ = Min. $I_{OL}$ = 2.1 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | Volts | $V_{CC}$ = Min. $I_{OH}$ = −400 μA |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | Volts | See note 1 |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$+1 | Volts | |

**AC CHARACTERISTICS** $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0 V ±5% (unless otherwise specified)

| | | 2332 | | 2332A | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Units** | **Test Conditions** |
| $t_{ACC}$ | Address Access Time | | 450 | | 350 | ns | |
| $t_{CO}$ | Chip Select Delay | | 200 | | 200 | ns | See Note 2 |
| $t_{DF}$ | Chip Deselect Delay | | 175 | | 175 | ns | |
| $t_{OH}$ | Previous Data Valid After Address Change Display | 40 | | 40 | | ns | |

**CAPACITANCE** $T_A$ = 25°C, f = 1.0 MHz, See Note 3

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 8 | pF | All Pins except Pin under Test Tied to AC Ground |
| $C_{OUT}$ | Output Capacitance | | 10 | pF | |

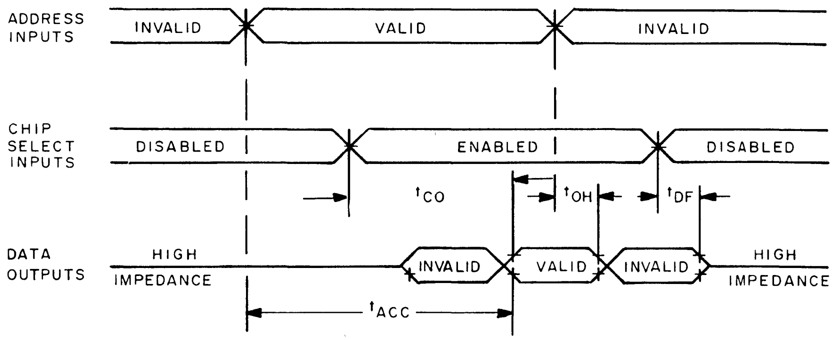
**Notes**
1. Input levels that swing more negative than −0.5 V will be clamped and may cause damage to the device.
2. Loading 1 TTL + pF, input transition time: 20 ns.
   Timing measurement levels: input 1.5V, output 0.8V and 2.0V.
   $C_L$ = 100pF.
3. This parameter is periodically sampled and is not 100% tested.

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Ambient Operating Temperature | 0° to +70°C |
| Storage Temperature | −65°C to +150°C |
| Supply Voltage to Ground Potential | −0.5V to +7.0V |
| Applied Output Voltage | −0.5V to +7.0V |
| Applied Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

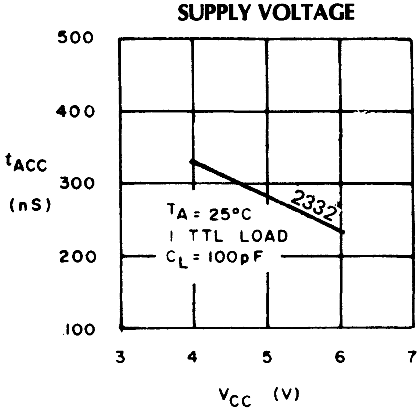
**COMMENT**
*Stresses above those listed under "Absolute Maximum Ratings" may cause permament damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## TIMING DIAGRAM

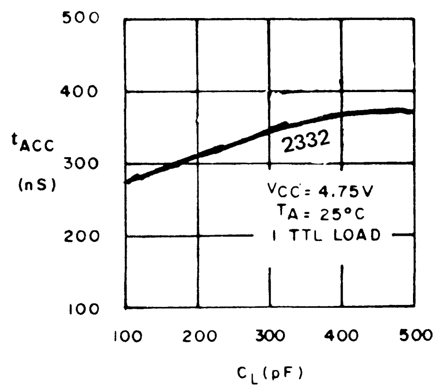



## TYPICAL CHARACTERISTICS

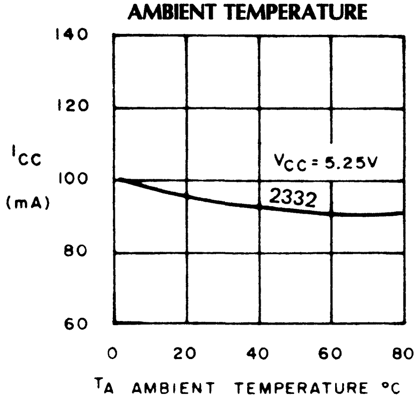
### ACCESS TIME vs. SUPPLY VOLTAGE



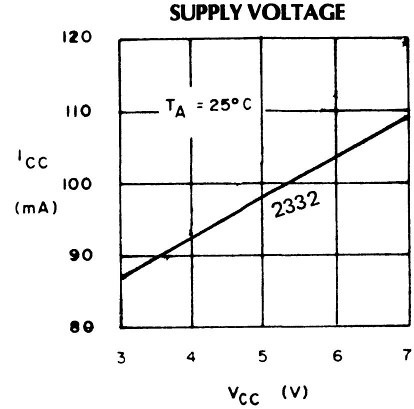

### ACCESS TIME vs. CAPACITATIVE LOAD




### SUPPLY CURRENT vs. AMBIENT TEMPERATURE




### SUPPLY CURRENT vs. SUPPLY VOLTAGE



commodore semiconductor group

NMOS

# 2364
# Static ROM (8192 x 8)

| | 2364 | 2364A | 2364B |
|---|---|---|---|
| Maximum Access Time | 450 ns | 350 ns | 300 ns |

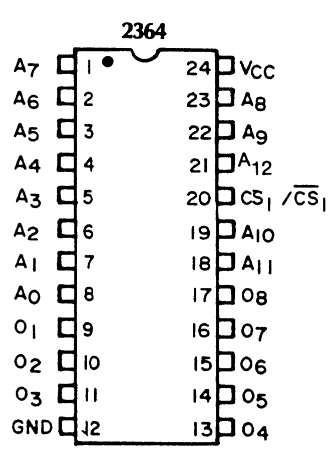
- Access Time 450 ns and 350 ns
- Totally Static Operation
- Fully TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Programmable Chip Select
- Single 5V Power Supply
- Pin Compatible With 2716 & 2732 EPROMs
- 400 mV Noise Immunity on Inputs
- 2716/2732 EPROMs Accepted as Program Data Inputs

## DESCRIPTION

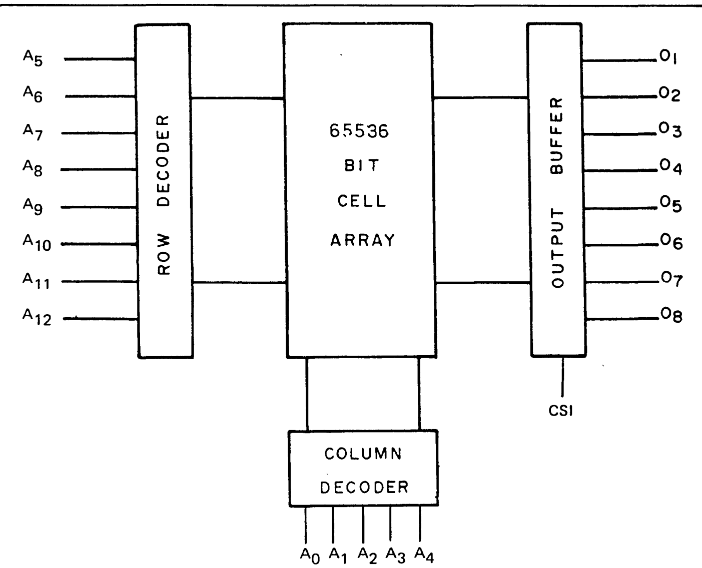
The MOS Technology 2364 is a 65, 536-bit Static Read-Only Memory organized as 8192 x 8 bits. It features fast access time (350 ns maximum). It is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage capacity and simple interfacing requirements are important design considerations.

The 2364 operates totally asynchronously; no clock input is required. With one programmable chip select input, two 64K ROMs can be OR-tied with no need for external decoding logic. Designed to replace two 2732 EPROMs, the 2364 can eliminate the need to redesign printed circuit boards for volume mask-programmed ROMs after prototyping is completed with EPROMs.

## PIN CONFIGURATION




## BLOCK DIAGRAM



**DC CHARACTERISTICS** $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0 V ±5% (unless otherwise specified)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $I_{CC1}$ | Power Supply Current | | 125 | mA | $V_{IN} = V_{CC}$, $V_O$ = Open, $T_A$ = 0°C |
| $I_{CC2}$ | Power Supply Current | | 120 | mA | $V_{IN} = V_{CC}$, $V_O$ = Open, $T_A$ = 25°C |
| $I_O$ | Output Leakage Current | | 10 | μA | Chip Deselected, $V_O$ = O to $V_{CC}$ |
| $I_I$ | Input Load Current | | 10 | μA | $V_{CC}$ = Max. $V_{IN}$ = O to $V_{CC}$ |
| $V_{OL}$ | Output Low Voltage | | 0.4 | Volts | $V_{CC}$ = Min. $I_{OL}$ = 2.1 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | Volts | $V_{CC}$ = Min. $I_{OH}$ = −400 μA |
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | Volts | See note 1 |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$+1 | Volts | |

**AC CHARACTERISTICS** $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0 V ±5% (unless otherwise specified)

| Symbol | Parameter | 2364 | | 2364A | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_{ACC}$ | Address Access Time | | 450 | | 350 | ns | |
| $t_{CO}$ | Chip Select Delay | | 200 | | 200 | ns | See Note 2 |
| $t_{DF}$ | Chip Deselect Delay | | 175 | | 175 | ns | See Note 2 |
| $t_{OH}$ | Previous Data Valid After Address Change Display | 40 | | 40 | | ns | |

**CAPACITANCE** $T_A$ = 25°C, f = 1.0 MHz, See Note 3

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 8 | pF | All Pins except Pin under Test Tied to AC Ground |
| $C_{OUT}$ | Output Capacitance | | 10 | pF | All Pins except Pin under Test Tied to AC Ground |

**Notes**

1. Input levels that swing more negative than −0.5 V will be clamped and may cause damage to the device.
2. Loading 1 TTL + pF, input transition time: 20 ns.
   Timing measurement levels: input 1.5V, output 0.8V and 2.0V.
   $C_L$ = 100pF.
3. This parameter is periodically sampled and is not 100% tested.

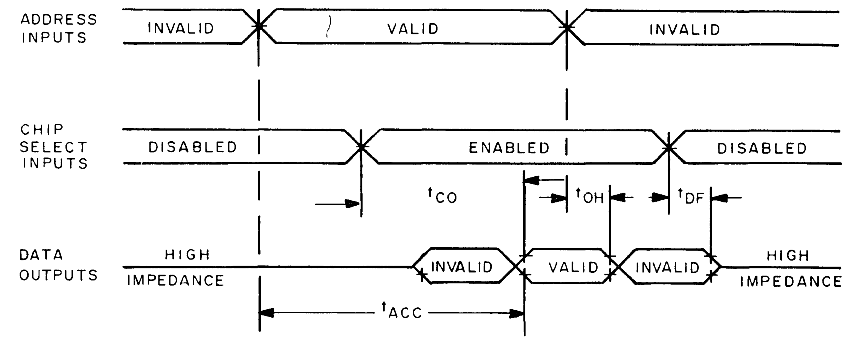
**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Ambient Operating Temperature | 0° to +70°C |
| Storage Temperature | −65°C to +150°C |
| Supply Voltage to Ground Potential | −0.5V to +7.0V |
| Applied Output Voltage | −0.5V to +7.0V |
| Applied Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

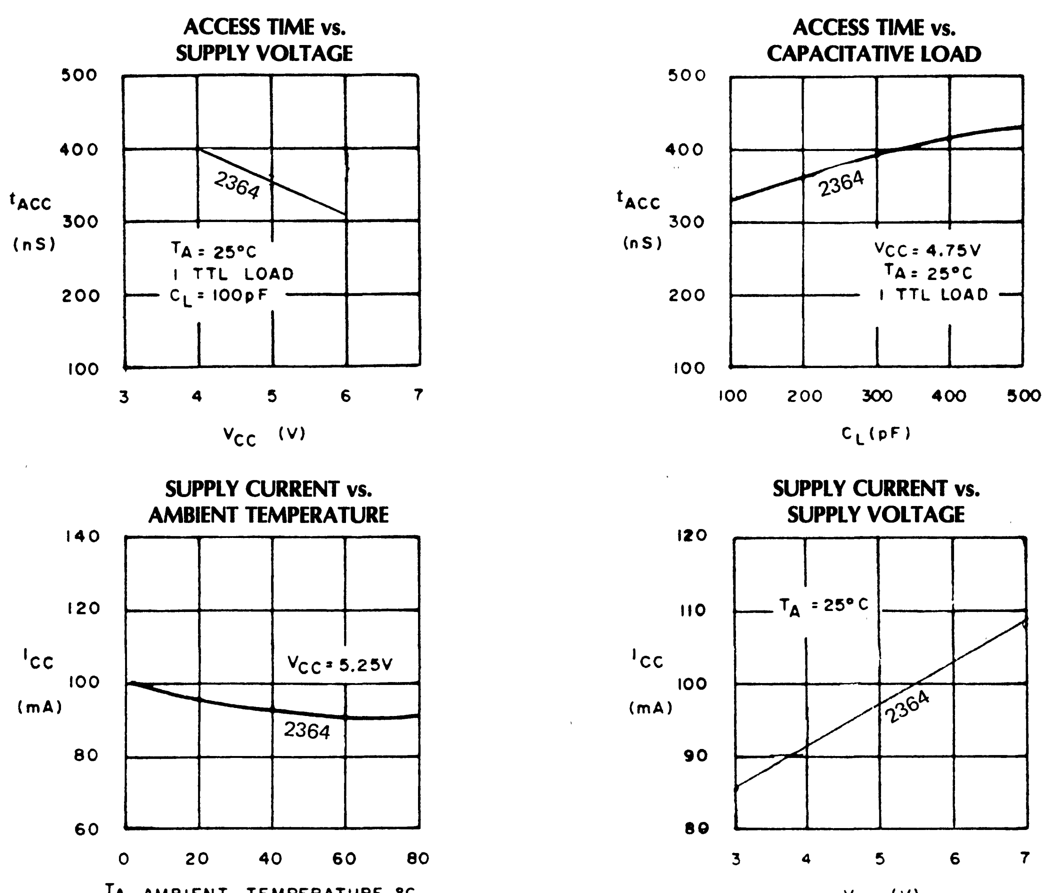
**COMMENT**

*Stresses above those listed under "Absolute Maximum Ratings" may cause permament damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

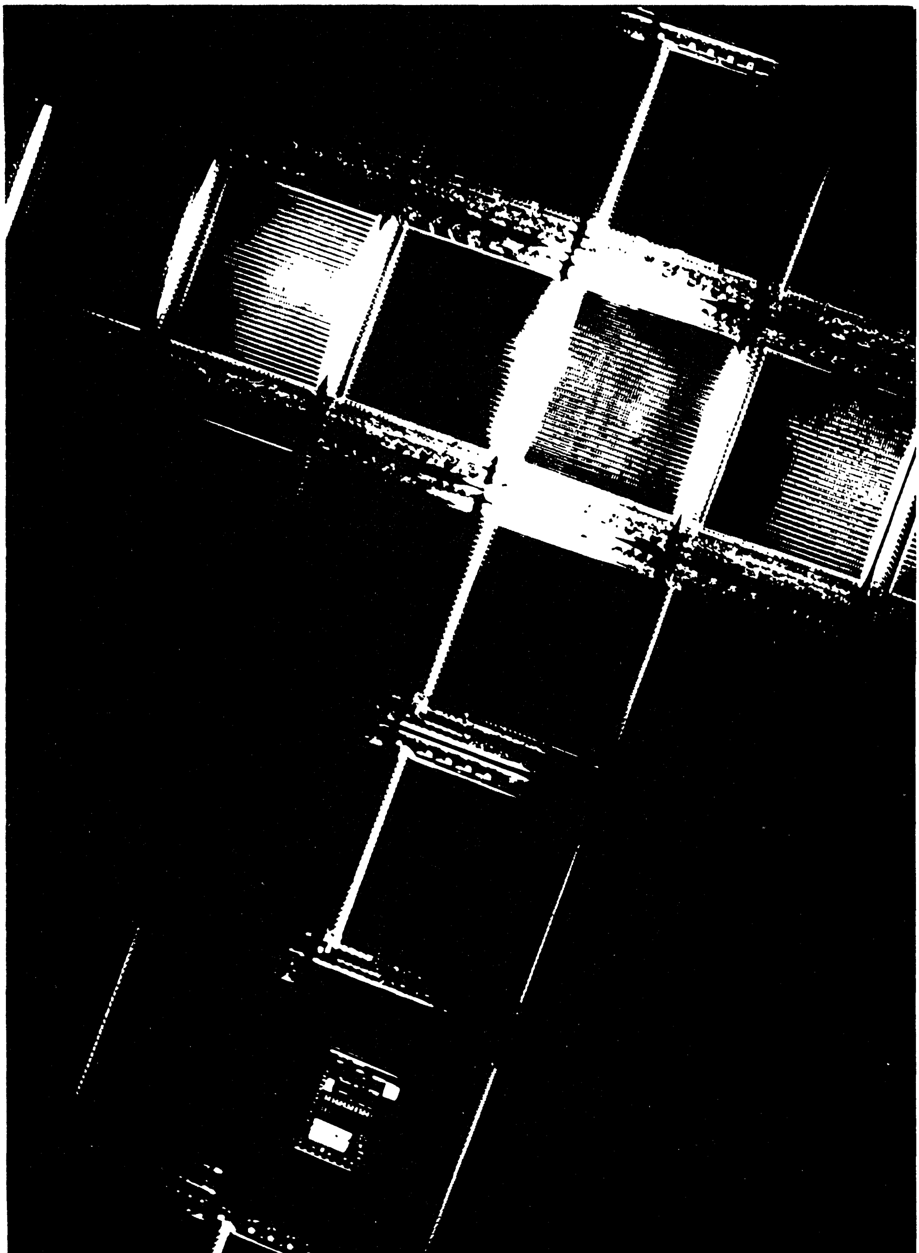
## TIMING DIAGRAM




## TYPICAL CHARACTERISTICS



# Section 3
# CMOS



# FR2060
# Alarm Watch With Snooze Stopwatch And Timer

- **24 Hours Settable Countdown Timer or . . .**
- **6 to 8 Digit Stopwatch (Autorange Capability in 6D Versions)**
- **Daily Alarm with Snooze—5 Minute Repeatable Reminder/Timer**
- **Executive Alarm Warning**
- **Alarm Feature Can be Set to Any Minute of the Day**
- **Many Display Formats Available with 6 to 8 Digits and Day Flags**
- **4 Year "Smart" Calendar**
- **Two Button Control of All Alarm Time, Normal Functions and Backlight**
- **Third Button Used ONLY When Accessing Timer or Stopwatch**
- **One Touch ±30 Second Error Correction**
- **Simple Setting Procedures**
- **Single 1.5 V Battery Operation**
- **Low Power Dissipation**
- **32768 Hz Quartz Crystal Operation**
- **Power-Up Reset**
- **On-Chip Oscillator Resistors**
- **High Speed Test Capability**
- **Designed For Use with Industry Standard Biplexed LCD Displays**
- **Multi-Tone Sound Outputs**
- **Lithium Battery Supply Option**
- **Chime Option**
- **7 Flag Day of the Week Indicators and Timer, Stopwatch and Alarm Flags**
- **Alarm and Lamp Test (Simultaneous Switch Depression)**
- **Efficient Voltage Doubler**
- **Option for 12 or 24 Hour Time Display**
- **Option for Month Date or Date Month Display**
- **Backlight/Function Switch Combination Option**

## DESCRIPTION

The FR2060 is a programmable CMOS/LSI circuit which contains all the logic necessary to implement a multi-function 6 or 8 digit biplexed liquid crystal display alarm watch with countdown timer and stopwatch. This device is fabricated with low-threshold, Ion-implanted CMOS metal gate technology for low voltage, low power operation. The circuit contains an oscillator-amplifier with an internal feedback resistor for use with 32768 Hz quartz crystals. The circuit operates from a single 1.5 volt battery and contains internal voltage multiplying circuitry that can be connected as a voltage doubler with a minimum of external components. Three switch inputs are required to control all operations. These switch inputs have pull-down resistors and debounce by internal circuitry. Date/Month and 24 Hour mode options are also provided. Switch control and display functions have been designed for flexibility and ease of operation.

## WATCH OPERATION:

The FR2060 has been designed with sufficient programming in its display circuitry to allow interfacing with almost any common 6 to 8 Digit dual backplane multiplexed LCD display including Day of Week and numerous indicator flags.

The following discussion outlines the operation of a 6-digit multi-function watch followed by a description of an 8-digit multifunction version. The programmability of the FR2060 switch and display controls allows this diversity.

Referring to Figure 1, note the following basic guidelines for the operation of the FR2060 6 Digit version:

A. S3 ("Select Button") is used as a selection switch to choose between the following states:
   1. Normal time display with Alarm
   2. Countdown Timer set/display
   3. Chronograph (Lap or Split Mode)

B. Within any of the above states, S2 ("Set Button") is basically used to select the information to be changed:
   1. In the Normal display state S2 is used to select Alarm or Real time for setting.
   2. In the Timer state, S2 is used for selecting the timer counters to be set.
   3. In the Chronograph state, S2 controls the display of the stopwatch vs. Lap/Split time.

C. S1 ("Display Button") is used to control the display options in the Normal display state as well as to control the actual changing of watch date as follows:
   1. In the Normal display state S1 controls the arming/disarming of the Alarm as well as the incrementing of timekeeping counters when setting.
   2. In the Timer state S1 is used for setting the desired countdown time as well as for start/stop.
   3. In the Stopwatch state S1 is used for controlling start/stop.

**NORMAL DISPLAY STATE—6 DIGIT WATCH**
The normal display for the watch is: Hours: Minutes Seconds or Hours: Minutes Date.

One push and release of the "Display" Button (S1) will display Month and Date for 3 seconds. If the display button is held depressed for longer than 3 seconds, Hours: Minutes Date will replace Hours: Minutes Seconds, or vice versa.

One of the seven day flags will indicate day of the week in all of the above modes.

Two sequential depressions of S1 will display Alarm time, and three depressions will alternately arm/disarm the Alarm.

**SETTING (Normal Display State)**
Depressing the Set Button (S2) one time will cause no action, however two successive depressions of the S2 will place the watch in the Alarm set mode. Alarm Hours: Minutes will appear with an "A" (AM) or "P" (PM) indication in the right most position. The Alarm Hours will be flashing and will advance with each depression of the "Display" Button or at a 2 Hz rate if the button is held. The display will return to normal mode 3 seconds after the last Set or Display input.

The next push of the Set Button before the 3 second timeout will cause the Alarm tens of Minutes to flash. Alarm tens of Minutes are advanced as above. The display will return to normal 3 seconds after the last Set or Display input.

The next push of the Set Button before the 3 second timeout will cause the Alarm units of minutes to flash. Alarm units of minutes are advanced as above. The display will return to normal 3 seconds after the last Set or Display input.

The next push of the Set Button will cause "CH" to display. If flashing, the Chime option is enabled, otherwise it is off. Depressing S1 will alternate the Chime status. The display will return to normal 3 seconds after the last Set or Display input.

The next push of the Set Button before the 3 second timeout will display Month Date Day with Month flashing. The month is advanced with S1 as above. There is NO automatic timeout return from this or any of the following set states.

The next push of the Set Button will cause the Date to flash; the Date is advanced as above.

The next push of the Set Button will cause the Day to flash. The Day of the week is advanced in the same manner as the month.

The next push of the Set Button will cause the display of Hours: Minutes Seconds with Seconds flashing. S1 depression will zero seconds; if Sec $\geq$ 30, Minutes will also advance by 1.

The next push of the Set Button causes the display of Hours: Minutes (actual time) with an "A" or "P" signifying AM or PM. The hour flashes and is advanced in the same way as other data.

The next push of the Set Button causes units of Minutes to flash with seconds counting. Units of minutes are advanced as above.

The next push of the Set Button causes units of Minutes to flash with seconds counting. Units of minutes are advanced as above.

The last push of the Set Button places the watch in the normal display without altering the seconds count.

Note that Alarm time is always distinguishable from actual time by the fact that ALL Alarm time displays have a 3 second timeout feature which returns the watch to normal time mode.

**ALARM OPERATION (Normal Display State)**
Two presses of the display button within 3 seconds will cause the Alarm Time (Hours: Minutes, AM or PM) to be displayed for 3 seconds.

A third push of the display button within 3 seconds will cause the alarm to change state from armed to disarmed or disarmed to armed. When the alarm is armed a flag appears in the display.

When the alarm is armed and the real time matches the alarm time, the alarm output will "beep" once; 3 and ¾ seconds later the alarm will beep at 1 Hz intervals for 26 seconds. A single push of the S1 button will cause the alarm to enter a 5 minute "snooze" mode. The snooze may be repeated as many times as desired. Once the Alarm turns on, the Snooze feature may thus be used as a 5 minute reminder/timer until disarmed. Two pushes of the display button (within 3 seconds) while the alarm is sounding will cancel the alarm. The alarm stays armed and will sound again in 24 hours.

**TIMER STATE**
Depressing the Select Button (S3) one time will place the watch in the last timer mode used. The timer will be in whatever state it was left in when this mode was last exited.

Timer state is indicated by the presence of the Timer flag.

In Timer state one push and release of the Set Button (S2) will place the watch in the Timer Set mode. Timer Hours:

Minutes Seconds will be displayed. The Timer Hours will be flashing and will advance with each depression of the display button or at a 2 Hz rate if the button is held.

The next push of the Set Button will cause the Timer tens of minutes to flash. Timer tens of minutes are advanced as above.

After the next push of the Set Button Timer units of minutes will flash. Timer units of minutes can then be advanced as above.

The next push of the Set Button will cause Timer tens of seconds to flash. The timer tens of seconds are advanced as above.

After the next push of the Set Button Timer units of seconds will flash. Timer units of seconds can then be advanced as above.

The next push of the Set Button will stop the flashing. The timer is then ready to count down from the time displayed. Pushing the Display Button will start the timer. When the timer reaches zero the alarm "beep" will be activated. While the timer is displayed and counting down the Display Button can be used to stop and restart the timer. When the timer reaches zero and beeps the Display Button is used to deactivate the timer. If there is no deactivation the timer will automatically go into SW mode and begin counting up from zero. This will occur even if the timer mode has been exited and the watch is displaying normal time. Exit timer state by S3 Button depression.

**STOPWATCH STATE**

Stopwatch state is indicated by the flashing of the Stopwatch flag. In Lap mode the word "LAP" will be displayed, and in the Split mode "SPL" will be displayed. Upon entering this state, by holding S3 depressed the watch will toggle between LAP and SPLIT modes. Release S3 for desired mode.

Upon entering the Stopwatch state, the contents of the Stopwatch are displayed. The mode of the Stopwatch (LAP vs. SPLIT) is that of the previous control sequence. In this state S1 (Display Button) is used to start or stop the Stopwatch and S2 (Set Button) is used to control Stopwatch vs. Lap/Split time display as well as Stopwatch reset.

In the SPLIT mode if the stopwatch is running pushing S2 will freeze the displayed time in the display. Internally the stopwatch continues to count; pushing S2 again will cause the display to show the counting stopwatch. If the Stopwatch is stopped pushing S2 will zero the Stopwatch.

In the LAP mode if the Stopwatch is running, pushing S2 will freeze the display time in the display. Internally the Stopwatch will zero and start counting again, pushing S2 again will transfer the current Stopwatch time to the display and restart the internal counter from zero. If the Stopwatch is stopped, pushing S2 will zero its contents.

The colon is used as a stopwatch running/stopped indicator. The colon flashes at a 1 Hz rate when the internal stopwatch is running and is steady when the counter is stopped.

Exit the Stopwatch state by S3 button depression to return to normal display.

**WATCH OPERATION—8 Digit Display**

The normal display for the 8-digit watch is: Hours: Minutes Seconds Date and Day Flags (Refer to Figure 2). Also active in this state are the following flags: PM, Alarm, Timer, Chrono, Date and Chime.

A single depression of S1 will display the Alarm Hour: Minutes with the letters "AL" to denote that Alarm information is being displayed. A double depression of S1 will toggle the Alarm status between armed and disarmed. The Alarm Flag is on when the Alarm is armed. The automatic 3 second return will occur in each of the above cases.

**SETTING**

The switch controls operate in a manner similar to the 6 digit version previously described. Depressing S2 twice will place the watch in the alarm set mode with Hours: Minutes "A" or "P" and "AL" showing. Hour and "A" or "P" will be flashing and Alarm Hours will advance with each S1 depression. The watch will return to normal mode 3 seconds after the last S1 or S2 input.

Another push of S2 before the timeout will cause the Alarm tens of Minutes of flash. This data is advanced by S1 as above.

The next push of S2 will cause the Alarm units of Minutes to flash. This is advanced as above.

The next push of S2 before the timeout will cause "CH" to display. Depressing S1 will alternate the Chime status between on and off. Flashing "CH" indicates Chime enabled.

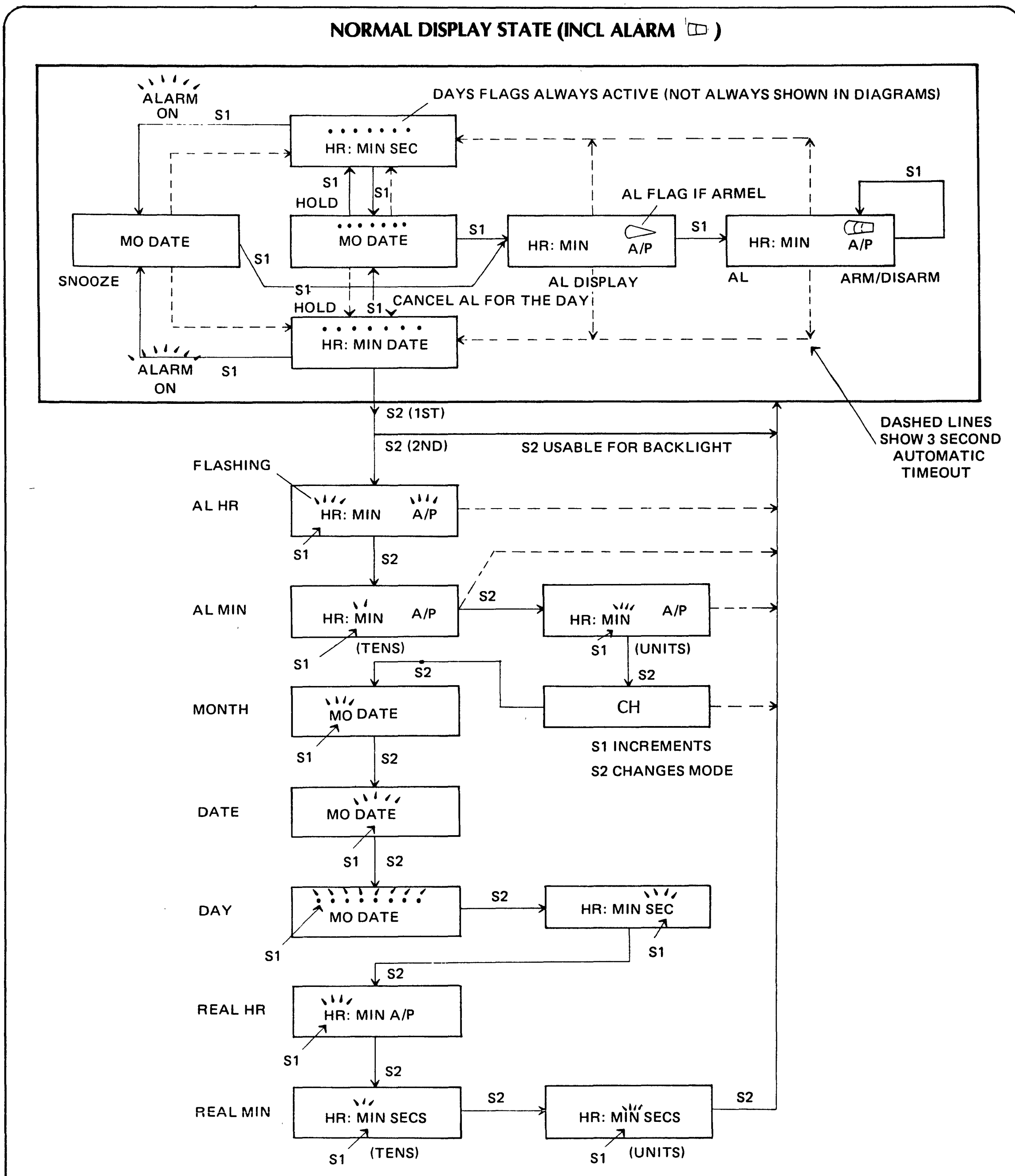
The next push of S2 before the timeout will display Hour: Minutes, Seconds with Seconds flashing. S1 depression will zero Seconds; if Seconds equal or exceed 30, Minutes will also advance by 1.

Subsequent pushes of S2 access the Real Time Hours, Minutes (tens and units), Month, Date, then Day of Week set states. In each case the data to be set flashes and is incremented by S1 depressions.

From the Set Day mode, S2 causes the return of normal time display.

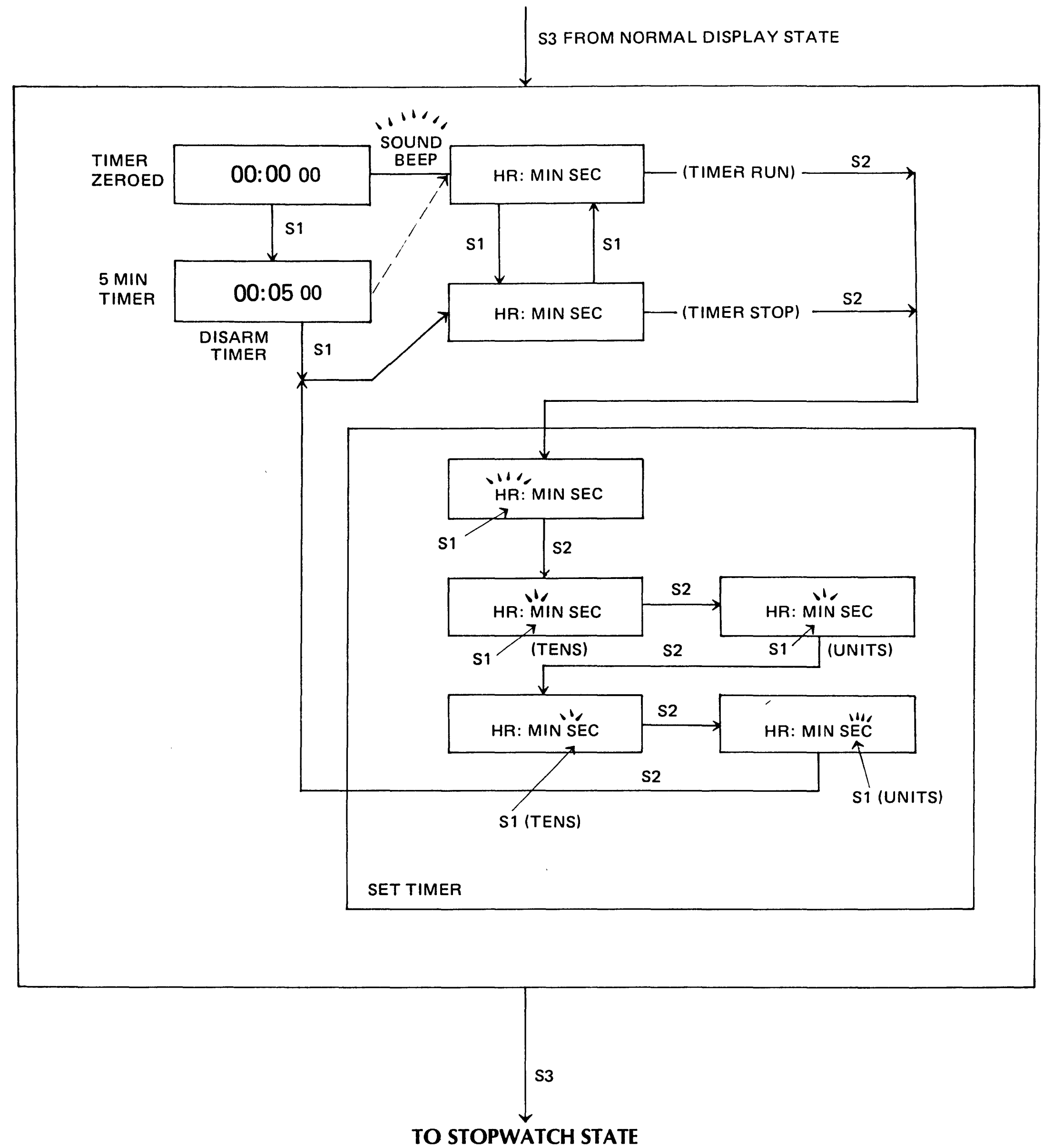
From the normal time display mode, S3 is used to select either the Timer or Stopwatch state as described previously. The operation within the Timer state is essentially identical to the 6 digit version. The stopwatch operation is also similar excepting that Hours: Minutes Seconds 1/100 are shown in the 8 digit version and no autoranging is required.

**FR2060 STATE DIAGRAM**



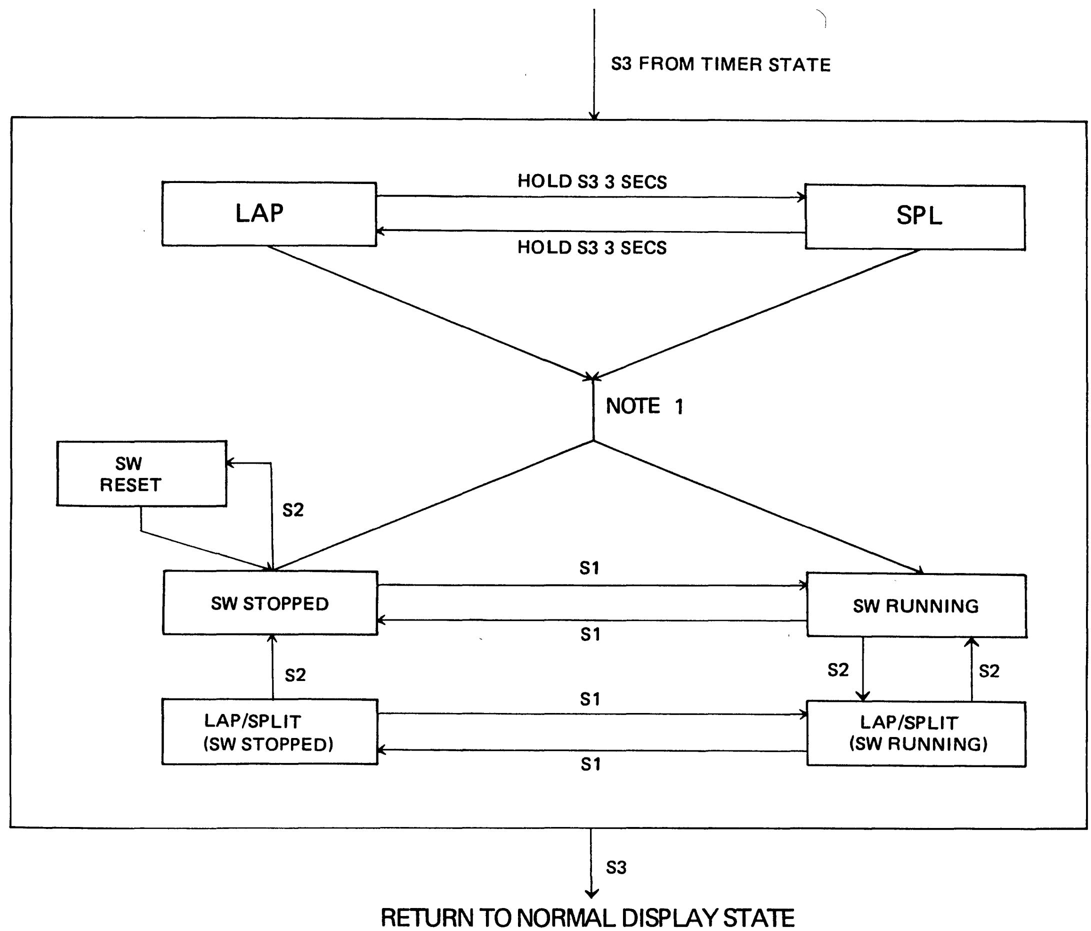

DEPRESS S3 TO GO TO TIMER STATE

## TIMER STATE




**NOTE**
Either Timer or Stopwatch May Be Active But Not Simultaneously.

## STOPWATCH STATE




**NOTES**

1. The NPN pad may be used to drive the base of an NPN transistor when used with a coil for amplified sound output. Direct drive on the piezo is accomplished using AL an $\overline{AL}$ (Ref. Fig. 2)
2. AL+ and AL− define the sense of the alarm input, i.e., if the alarm is normally low but goes high when the alarm sounds, connect AL+ to the alarm output from the watch chip. If AL is normally high, then connect AL−.

## FR2060 STATE DIAGRAM 8-DIGIT

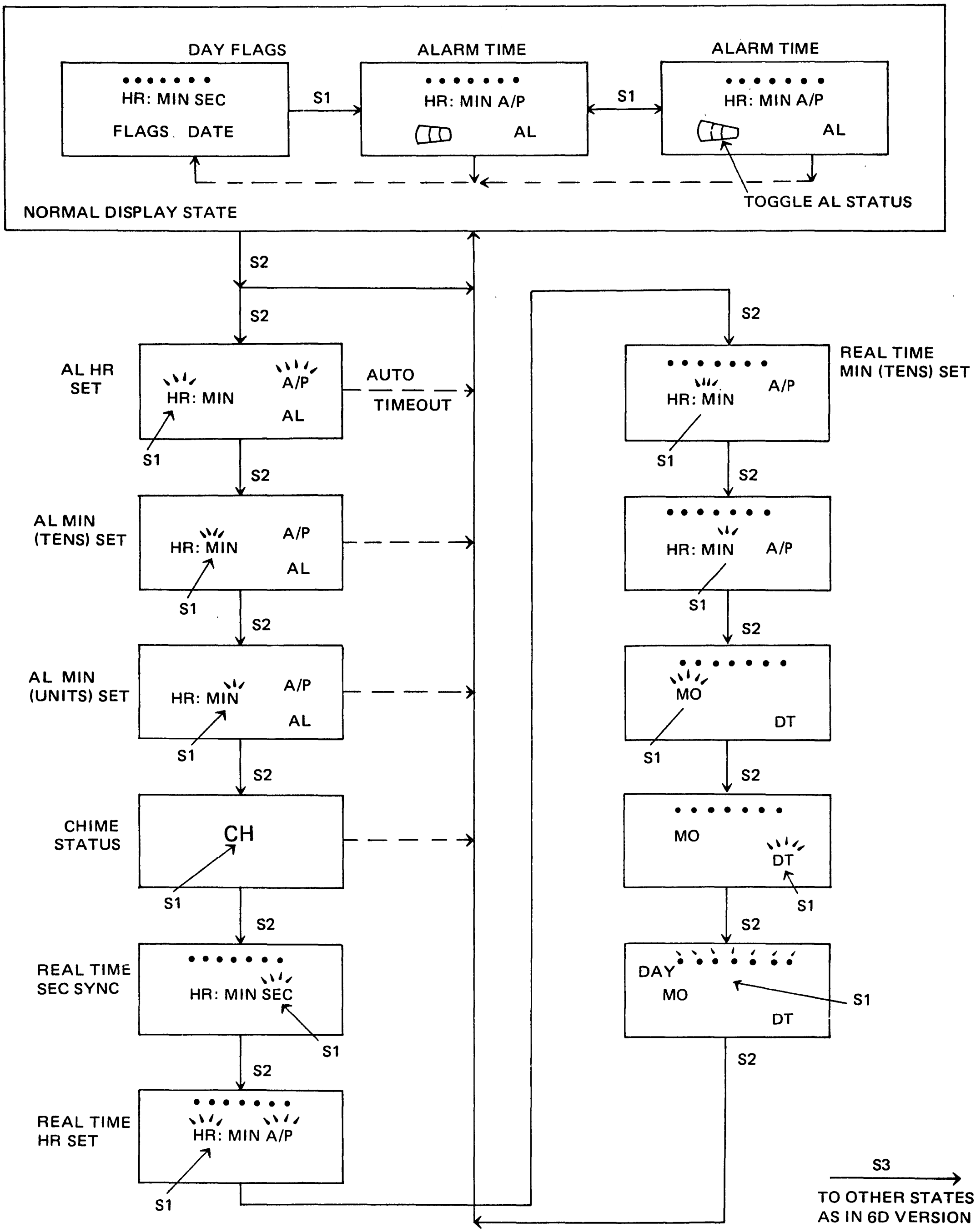



Figure 2

# FR2080
# Low Power CMOS Musical Tune Chip

- Gate Programmable up to 254 Notes of Tune (s)
- Prolonged Note Capability
- 3 Octave Range
- Direct Piezo Transducer Drive or Drive for NPN Transistor-Coil
- Oscillator Tuning Capacitors
- Low Standby Current
- Interfaceable with Many Common Alarm Watch Chips
- Small Size

## DESCRIPTION

The FR2080 is a low power 1.5 volt CMOS/LSI circuit which contains all the logic necessary to implement a musical alarm for an electronic watch, music box, or other musical application. The circuit is designed to drive a piezo electric transducer or a coil-transducer combination directly from the chip.

In addition to the sound generation circuitry the chip includes a selection of bonding pads with fixed capacitor values which may be used to tune a 32KHZ crystal oscillator.

## FUNCTIONAL DESCRIPTION

The FR2080 is a small musical tune chip which has been designed to operate utilizing a 32KHZ time base. In an alarm watch, the chip derives its timing by accepting a 32KHZ oscillator waveform from the timekeeping chip. While in a stand-alone application such as a music box, the timing is generated by using a 32KHZ crystal.

In an alarm watch the musical alarm may be implemented by as few as 7 signals as shown in Figure 2. Whenever the main chip energizes its Alarm Output, that signal enters the FR2080 and causes the chip to begin sequencing through its programmed tune (s).

The user shuts the alarm off via a single or multiple switch depression (s). If no switch is energized during the tune, the entire melody will be played to conclusion and the chip will return to its quiescent state. Note that the quiescent $I_{DD}$ is quite low.

Buffers on the chip allow for direct driving of a piezo device. This is advantageous in that piezo voltage feedback to the main timekeeping circuit is eliminated.

A selection of on-chip caps surround the oscillator pins allowing the user to selectively eliminate discrete fixed tuning capacitors and perhaps even the trim cap. Significant module cost and size savings may be realized by utilizing this circuitry.

## MUSICAL DETAILS

The FR2080 uses a 32KHZ time base to generate its notes. The range of notes available are:

Bc __________ bc′ __________ b′c″ __________ a″

C IN SECOND OCTAVE
BELOW MIDDLE C

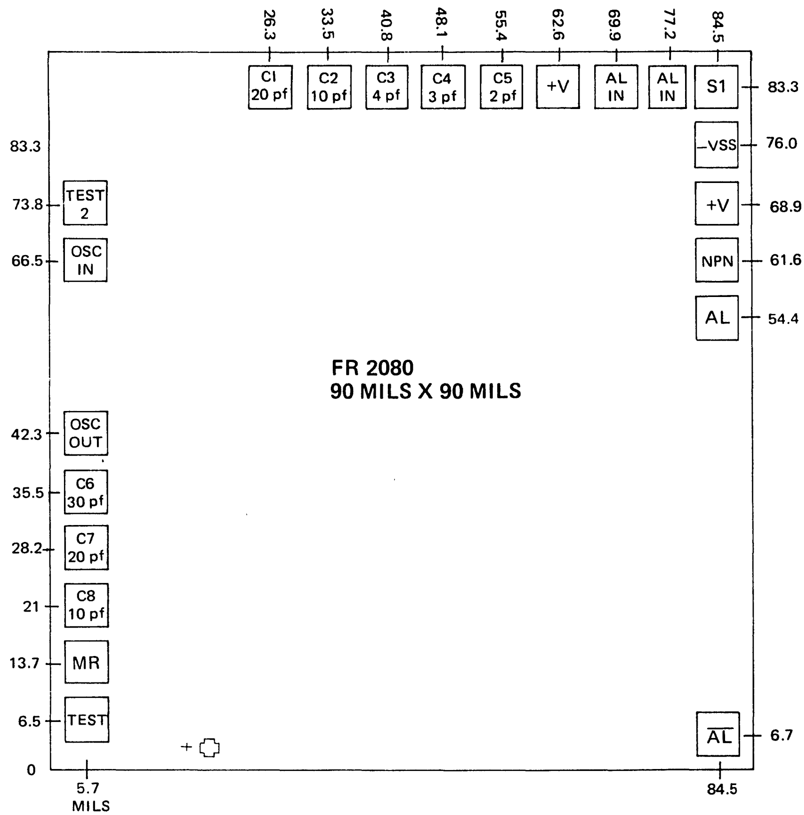
MIDDLE A F — MIDDLE A f: 431 Hz

**TOTAL OF 36 NOTES SPANS APPROXIMATELY 3 OCTAVES**

Once triggered the entire tune will be played unless interrupted by a switch input which will reset the circuit.

A tentative pinout is shown in Figure 1.

## PINOUT OF 2080




**NOTES**

1. The NPN pad may be used to drive the base of an NPN transistor when used with a coil for amplified sound output. Direct drive on the piezo is accomplished using AL an $\overline{AL}$ (Ref. Fig. 2)
2. AL+ and AL− define the sense of the alarm input, i.e., if the alarm is normally low but goes high when the alarm sounds, connect AL+ to the alarm output from the watch chip. If AL is normally high, then connect AL−.

**Figure 1**

## TYPICAL INTERCONNECTION OF 2080 WITH A WATCH CURCUIT

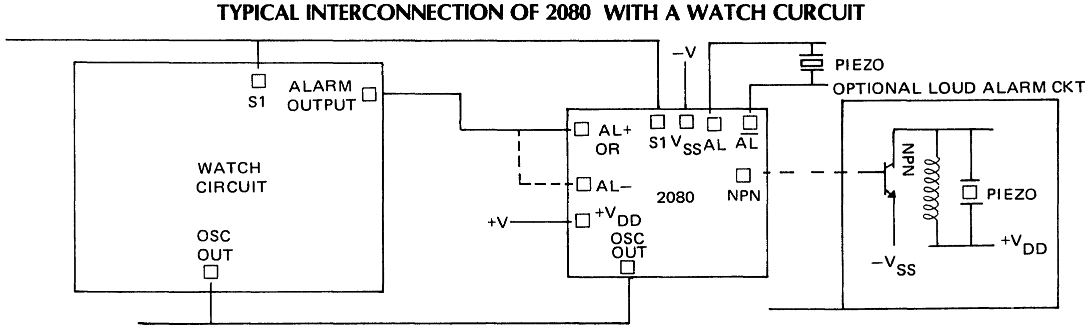



**Figure 2**

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Operating Temperature | 0° to 70°C |
| Storage Temperature | 25°C to 85°C |
| Voltage Any Pin | $V_{DD}$+.3V to $V_{SS}$−.3 V |
| Supply Voltage ($V_{DD}$ − $V_{SS}$) | 2.0 V |

**ELECTRICAL SPECIFICATIONS** $T_A$ = 25°C; $F_{osc}$ = 32,768 KHz; $V_{DD}$ = 1.6 V (Unless otherwise indicated)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 1.30 | 1.5 | 1.7 | Volt | |
| $I_{DD}$ | Power Supply Current | | 0.2 | 0.5 | μA | Standby mode |
| $I_{AL}$ | Alarm Output Current (push-pull) | | ±2 | | MA | $V_{DD}$ = 1.5 V, $V_{SAT}$ = 7 V |
| $I_{IN}$ | Switch Input Current | | −5 | −25 | μA | $V_{IN}$ = $V_{DD}$ |
| $V_{Start}$ osc. | Oscillator start Voltage (Stand alone mode) | 1.3 | | | Volt | |
| | Switch Debounce | | 62.5 | | mS | |
| $I_{NPN}$ | NPN Output Buffer current | | ±20 | | μA | $V_{DD}$ = 1.5 V, $V_{SAT}$ = −7 V |

# FR2222
# 5 Function 3½ Digit Biplex LCD Watch Circuit

- **5 Function Watch—Hours, Minutes, Seconds, Month and Date**
- **Biplex LCD Display Drive**
- **On Chip Oscillator Components**
- **Low Power Dissipation**
- **4 Year Calendar**
- **Efficient Voltage Doubler**
- **Simple Operating and Setting**
- **Single Input High Speed Test Capability**
- **32768 Hz Quartz Crystal Operation**
- **Small Die Size**
- **Date Flag**

## DESCRIPTION

The FR2222 is a CMOS/LSI circuit containing all the logic necessary to implement a five function watch interfaceable with a dual backplane multiplexed LCD display. The unique arrangement of the signals and the small die size allow for design and manufacture of extremely thin and compact watch modules.

The device is fabricated with low threshold, Ion-implanted CMOS metal gate technology for proven and reliable low power operation. The circuit contains an oscillator amplifier with internal feedback resistor elements for interfacing to 32768 Hz quartz crystals. The chip operates from a single 1.5 volt battery and contains an internal voltage doubler which operates with minimal external circuitry.

## OPERATION

The normal continuous display of the watch is Hours: Minutes.

If the Display Button is pushed and released, Month and Date will be displayed for approximately 1.5 seconds, then return to Hours: Minutes. If the button is pushed twice, Month and Date will be replaced by: Seconds. One further depression of the Display Button will return Hours: Minutes to the display.

## SETTING

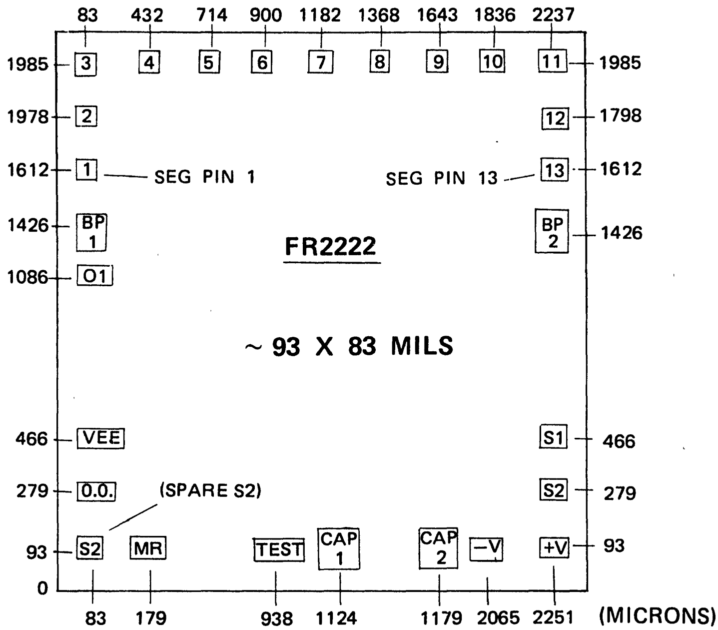
To set one or more timekeeping modes of the watch, the Set Button must be depressed. Month Date will now be displayed with Month flashing. To change the Month, the Display Button is pushed and held; Month will automatically increment at a 2Hz rate. If the Display Button is pushed and not held, the Month will be incremented each time the button is pushed.

The next push of the Set Button causes the Date to Flash. Date is advanced in the same manner as Month.

The next push of the Set Button displays the Hour, with an "A" or "P" signifying AM or PM. Hour is advanced in the same manner as Month.

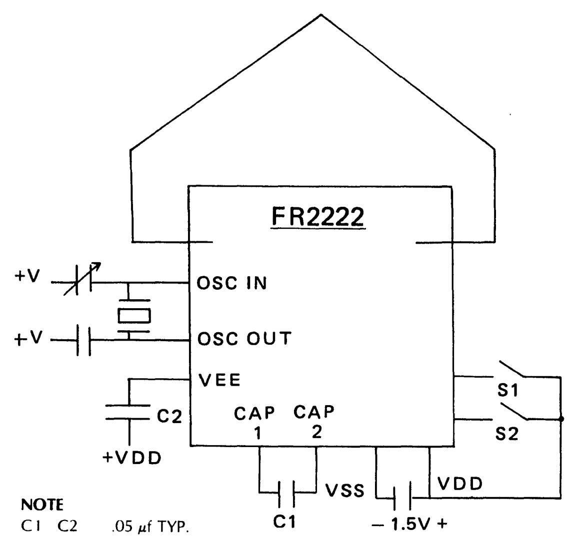
The next push of the Set Button displays Hours: Minutes, with the Minutes flashing. The Display Button advances Minutes in the same way as previously described. If Minutes are advanced, the watch stops counting, all displays retain the numbers as set, with the exception of Seconds, which is reset to "00". The last push of the Set Button restores normal counting from zero seconds. In this way, the watch may be synchronized with a time standard by the user. If Minutes were not advanced, the last push of the Set Button restores the normal Hours: Minutes display without altering the seconds count.

## COORDINATES OF PADS FOR FR2222 IN MICRONS




| SEG PIN | BP1 | BP2 |
|---|---|---|
| 1 | K | 1E |
| 2 | 1F | 1D |
| 3 | 1G | 1C |
| 4 | 1A | 1B |
| 5 | COL | 2E |
| 6 | 2F | 2D |
| 7 | 2G | 2C |
| 8 | 2A | 2B |
| 9 | OFF | 3E |
| 10 | 3F | 3D |
| 11 | 3G | 3C |
| 12 | 3A | 3B |
| 13 | FLAG (MO-DT) OFF | |

SEGMENT ASSIGNMENTS




NOTE
C1 C2 .05 μf TYP.

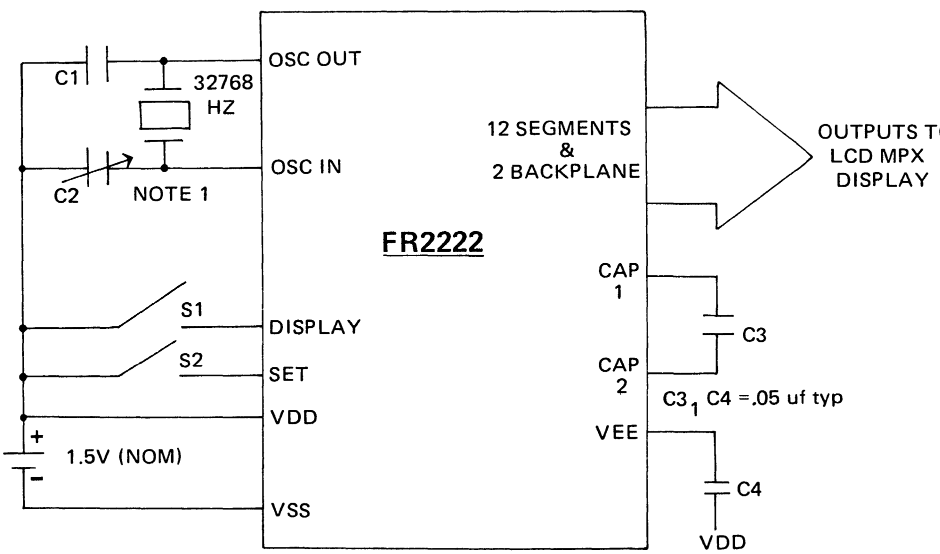
FR2222 SYSTEM DIAGRAM

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Operating Temperature | 0°C to 70°C |
| Storage Temperatures | 25°C to 85°C |
| Voltage Any Pin | $V_{DD}$ + 3V to $V_{SS}$ − .3V |
| Supply Voltage ($V_{DD} - V_{SS}$) | 2.0 V |

**ELECTRICAL SPECIFICATIONS** $T_A = 25°C$; $F_{OSC}$ = 32,768 KHz; $V_{DD}$ = 1.6 V (Unless Otherwise Indicated)

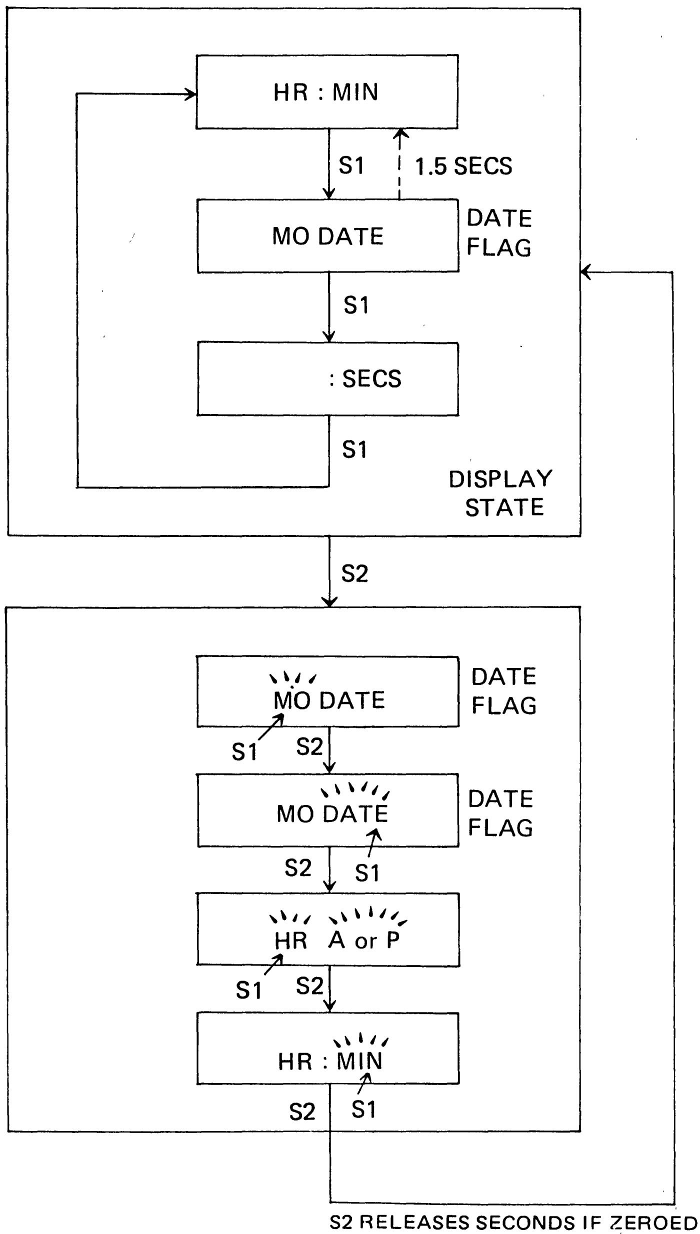
| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 1.35 | 1.5 | 1.7 | Volt | |
| $I_{DD}$ | Total Power Supply Current | | 1.8 | 3.0 | μA | Doubler connected but unloaded |
| $V_{EE}$ | Double Output Voltage | −1.15 | | −1.35 | Volt | $I_{EE}$ = 0.5 μA<br>$V_{DD}$ = 1.35 |
| $I_{IN}$ | Switch Input Current | | −5 | −25 | μA | $V_{IN} = V_{DD}$ |
| $V_{Start}$ osc. | Oscillator Start Voltage | 1.4 | | | Volt | |
| | Switch Debounce | | 62.5 | | mS | |




**NOTES**

1. $C_1$ and $C_2$ match chosen crystal for faster oscillator startup, $C_2$ should be adjusted to minimum capacitance setting.
2. As with all such semiconductor devices, care should be taken to insure no light is allowed to strike die. Predictably, light will increase $I_{DD}$ leakage and may cause malfunction. A non-transparent black coating is typically used to cover die and is highly recommended.

**FR2222 STATE DIAGRAM**



**commodore semiconductor group**

**CMOS**

# FR2268
# 5 Function, 3½/4 Digit LCD Alarm Watch Circuit

- Snooze Alarm—5 Minute Repeatable Reminder/Timer
- Alarm Feature Can Be Set to Any Minute of the Day
- Display of Hours: Minutes, Month Date or Seconds
- 4 Year "Smart" Calendar
- Two Button Control of All Functions
- Simple Setting Procedures
- Single 1.5 V Battery Operation
- Low Power Dissipation
- 32768 Hz Quartz Crystal Operation
- Power-Up Reset
- On-Clip Oscillator Resistors
- High Speed Test Capability
- Designed For Use With Industry Standard 3½ Digit LCD Displays or Other LCD Displays with AM, PM, and Alarm Flags
- Alarm Test (Simultaneous Switch Depression)
- Efficient Voltage Doubler

## DESCRIPTION

The FR2268 is a CMOS/LSI circuit which contains all the logic necessary to implement a five function 3½/4 digit liquid crystal display alarm watch. This device is fabricated with low-threshold, Ion-implanted CMOS metal gate technology for low voltage, low power operation. The circuit contains an oscillator-amplifier with an internal feedback resistor for use with 32768 Hz quartz crystals. The circuit operates from a single 1.5 volt battery and contains internal voltage multiplying circuitry that can be connected as a voltage doubler with a minimum of external components. Only two switch inputs are required to control all operations. These switch inputs have internal pull-down resistors and are debounced by internal circuitry.

## WATCH OPERATION

The normal display for the watch is: Hours: Minutes.

One push and release of the "Display" button (S1) will display Month and Date, for 3 seconds. If the display button is held depressed for longer than 3 seconds, Month Date will be replaced by: Seconds. One further depression of the display button will return Hours: Minutes to the display.

## ALARM OPERATION

Two presses of the display button within 3 seconds will cause the Alarm Time (Hours: Minutes, AM or PM flag) to be displayed for 3 seconds. If armed, the alarm will emit two "beeping" sounds per second while the switch is depressed.

A third push of the display button within 3 seconds will cause the alarm to change state from armed to disarmed or disarmed to armed. When the alarm is armed a flag output will also be activated.

When the alarm is armed and the real time matches the alarm time, the alarm output will "beep" at 1 Hz intervals for 60 seconds. A single push of the display button will cause the alarm to enter a 5 minute "snooze" mode. The snooze may be repeated as many times as desired. Two pushes of the display button will cancel the alarm.

It should be noted that the AM/PM state of the Alarm setting is easily obtained by a single depression of the set button. Interrogation of the Alarm time without the "beeping" indication is obtainable through a double depression of the Set switch. In each case the watch automatically returns to the normal time display mode.

## SETTING

Depressing the Set Button (S2) once will place the watch in the Alarm Hours set mode. The Alarm Hour will appear with an "A" (AM) or "P" (PM) indication in the right most position. The Alarm Hours will flash and will advance with each depression of the "Display" button or at a 2 Hz rate if the button is held. The display will return to normal mode 3 seconds after the last Set or Display input.

Two pushes of the Set Button before the 3 second timeout will cause the Alarm Minutes to flash. Alarm Minutes may be advanced as above. The display will return to normal 3 seconds after the last Set or Display input.

Three pushes of the Set Button before the 3 second timeout will cause Month Date display with Month flashing. The month is advanced with S1 as above. There is no automatic timeout return from this or any or the following three set states.

The next push of the Set Button will cause the Date to flash; the Date is advanced as above.

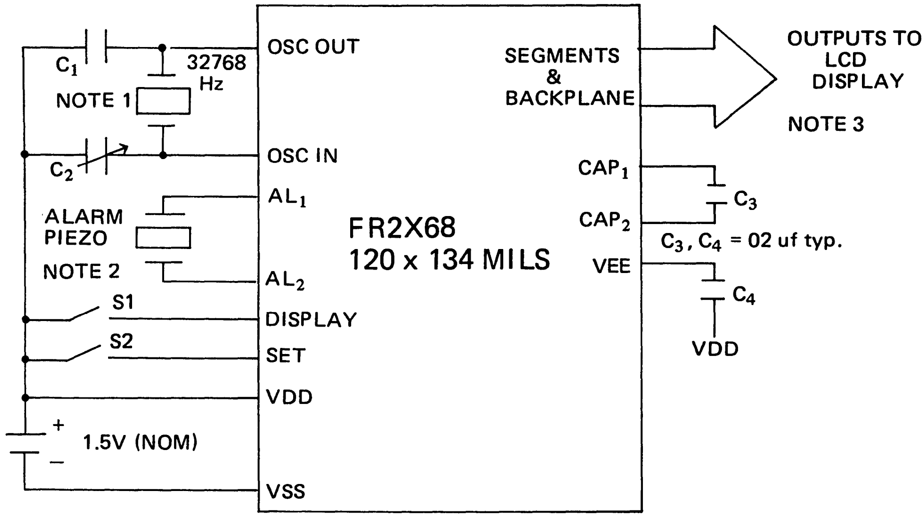
The next push of the Set Button causes the display of flashing Hours: (actual time) with an "A" or "P" signifying AM or PM. The hour is advanced in the same way as other data.

The next push of the Set Button displays Hours: Minutes with minutes flashing. Minutes are advanced as above. If minutes are advanced, the seconds become "00" and hold until the next depression of S2 which returns the watch to the normal display. If minutes were not advanced, the last push of the Set Button places the watch in the normal display without altering the seconds count.

**NOTE**

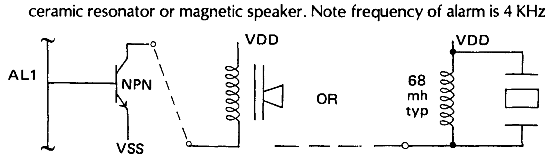
The setting and viewing of actual time is always distinguishable from Alarm time by the fact that all Alarm time displays have a 3 second timeout feature returning the watch to normal time mode.

### FR 2 x 68 SERIES SYSTEM DIAGRAM



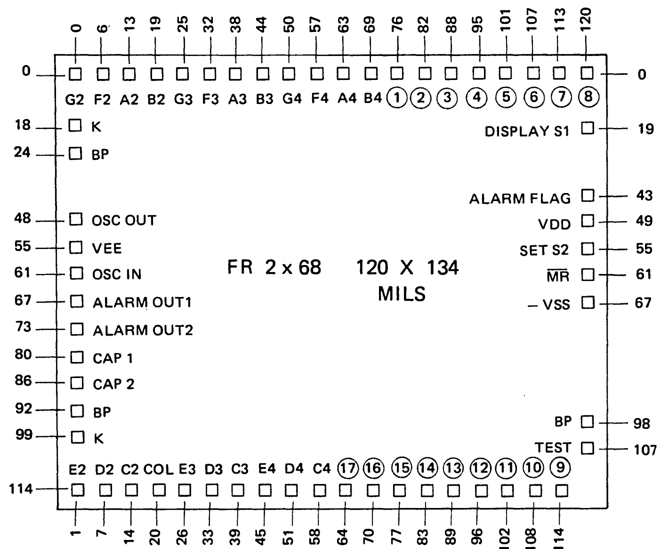

**NOTES**

1. $C_1$ and $C_2$ match chosen crystal. For faster oscillator startup, $C_2$ should be adjusted to minimum capacitance setting
2. For louder alarm output the following circuit may be used to drive a ceramic resonator or magnetic speaker. Note frequency of alarm is 4 KHz




3. Recommended commodore LCD displays:
   FR2268 5017, 5018 FR2368 5038 FR2568 5015, 5040, 5055
4. As with all semiconductor devices, care should be taken to insure that no light is allowed to strike the die. Predictably, light will increase $I_{DD}$ leakage and may cause malfunction. A non-transparent black coating is typically used and is recommended.

## FR 2 x 68 PINOUTS




| AN | FR 2568 | FR 2268 | FR 2368 |
|---|---|---|---|
| ① | G5 | – | MON |
| ② | F5 | – | SUN |
| ③ | H5 | – | – |
| ④ | A5 | – | TUE |
| ⑤ | B5 | – | WED |
| ⑥ | F6 | – | – |
| ⑦ | A6 | – | – |
| ⑧ | B6 | AM | – |
| ⑨ | G6 | PM | – |
| ⑩ | C6 | – | – |
| ⑪ | J6 | – | PM |
| ⑫ | D6 | – | – |
| ⑬ | E6 | – | – |
| ⑭ | C5 | – | SAT |
| ⑮ | D5 | – | FRI |
| ⑯ | J5 | – | – |
| ⑰ | E5 | – | THUR |

# FR2668
# LCD Watch Circuit

- **Display of Hours: Minutes-Seconds or Month-Date-Day**
- **4 Year "Smart" Calendar**
- **Two Button Control of All Functions**
- **Simple Setting Procedures**
- **Single 1.5 V Battery Operation**
- **Low Power Dissipation**
- **32,768 Hz Quartz Crystal Operation**
- **Power-Up Reset**
- **On-Chip Oscillator Resistors**
- **High Speed Test Capability**
- **Designed For Use with Industry Standard 5½ Digit LCD Displays**

## DESCRIPTION

The FR2668 is a CMOS/LSI circuit which contains all the logic necessary to implement a six function, 5½ digit liquid crystal display watch. This device is fabricated with low threshold, Ion implanted CMOS metal-gate technology for low voltage, low power operation. The circuit contains an oscillator-amplifier with an internal feedback resistor for use with 32,768 Hz quartz crystals. All die operate from a single 1.5 volt battery and contain internal voltage doubler circuitry which operate with a minimum of external components. Only two switch inputs are required to control all operations. These switch inputs have internal pull-down resistors and are debounced by internal circuitry.

## TIME AND DISPLAY SETTING

The normal display for the watch is: Hours, Minutes, Seconds. One push of the "Display" button will display Month, Date, Day for 3 seconds before returning the watch to normal display.

Depressing the "Set" Button will place the watch in the month set mode. Month, Date and Day will be display with Month flashing. The month will advance with each depression of the "Display" Button at a 2 Hz rate if the "Display" button is held.

The next push of the "Set" button causes the date to flash. The date is advanced in the same manner as the month.

The next push of the "Set" Button causes the day of the week to flash. The day of the week is advanced in the same manner as the month.

The next push of the "Set" Button displays Hours, Minutes with an "A" or "P" signifying AM or PM. The hour is advanced in the same way as the month.

The next push of the "Set" button displays Hours, Minutes with seconds counting and Minutes flashing. The "Display" button advances the minutes in the same way as the month. If minutes are advanced, the seconds become "00" and hold until the last push of the "Set" button which returns the watch to the normal time of day display with seconds starting at the push of the "Set" button. If minutes were not advanced, the last push of the "Set" button places the watch in the time of day display without altering the seconds count.

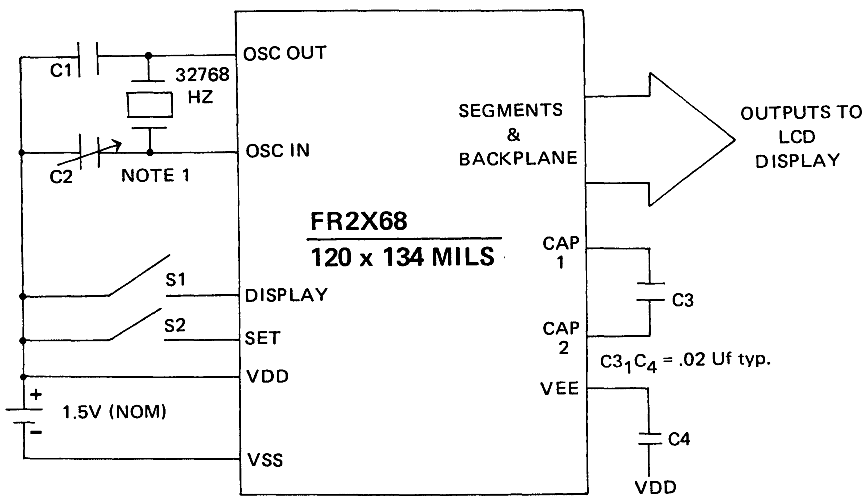
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Operating Temperature | 0°C to 70°C |
| Storage Temperature | 25°C to 85°C |
| Voltage Any Pin | $V_{DD}$ + .3 V to $V_{SS}$ − .3 V |
| Supply Voltage ($V_{DD} - V_{SS}$) | 2.0 V |

**Electrical Specifications** $T_A = 25°C$; $F_{OSC} = 32{,}768$ KHz; $V_{DD} = 1.6$ V (Unless otherwise indicated)

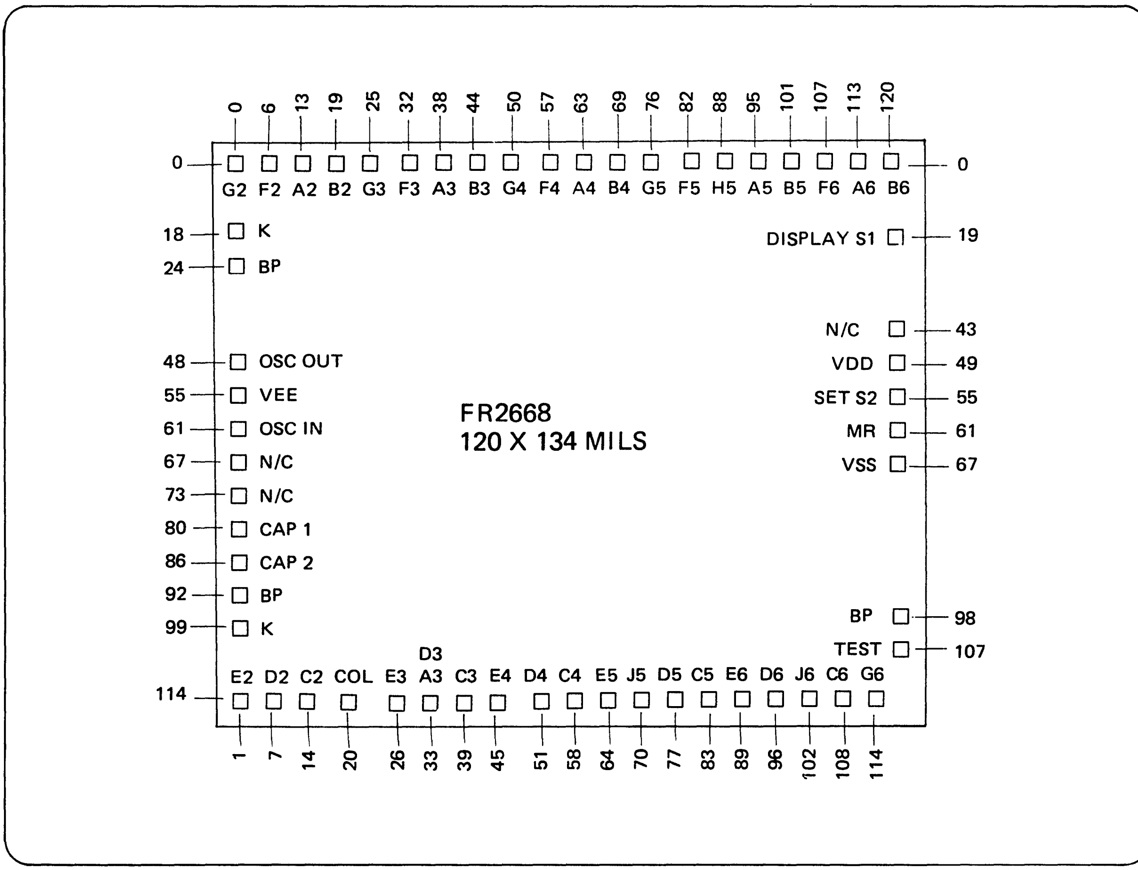
| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 1.35 | 1.5 | 1.7 | Volt |  |
| $I_{DD}$ | Power Supply Current $V_{DD} = 1.6$ V |  | 1.5 | 3 | μA | Doubler Connected but unloaded |
| $V_{EE}$ | Doubler Output Voltage | −1.3 |  |  | Volt | $I_{EE} = I_{\mu A}$ $V_{DD} = 1.5$ V |
| $I_{IN}$ | Switch Input Current ("Display" or "Set") |  | −5 | −25 | μA | $V_{IN} = V_{DD}$ |
| $V_{Start}$ osc. | Oscillator Start Voltage | 1.3 |  |  | Volt |  |
|  | Switch Debounce |  | 62.5 |  | mS |  |

**FR2668 SYSTEM**




NOTES
1. $C_1$ and $C_2$ Match Chosen Crystal.
2. Care should be taken to insure that no light is allowed to strike die. Light wll increase $I_{DD}$ and may cause malfunction. A non-transparent black coating is typically used and recommended.

## PINOUT DIAGRAM



# FR2368
# 6 Function, 3½/4 Digit LCD Alarm Watch Circuit With Day Flags

- **Snooze Alarm—5 Minute Repeatable Reminder/Timer**
- **Alarm Feature Can Be Set to Any Minute of the Day**
- **Display of Hours: Minutes, Day, Month-Date Day, or Seconds and Day**
- **4 Year "Smart" Calendar**
- **Two Button Control of All Functions**
- **Simple Setting Procedures**
- **Single 1.5 V Battery Operation**
- **Low Power Dissipation**
- **32768 Hz Quartz Crystal Operation**
- **Power-Up Reset**
- **On-Chip Oscillator Resistors**
- **High Speed Test Capability**
- **Alarm Test (Simultaneous Switch Depression)**
- **Efficient Voltage Doubler**
- **Day Flags**
- **PM Flag**

## DESCRIPTION

The FR2368 is a CMOS/LSI circuit which contains all the logic necessary to implement a six function 3½/4 digit liquid crystal display alarm watch. This device is fabricated with low-threshold, Ion-implanted CMOS metal gate technology for low voltage, low power operation. The circuit contains an oscillator-amplifier with an internal feedback resistor for use with 32768 Hz quartz crystals. The circuit operates from a single 1.5 volt battery and contains internal voltage multiplying circuitry that can be connected as a voltage doubler with a minimum of external components. Only two switch inputs are required to control all operations. These switch inputs have internal pull-down resistors and are debounced by internal circuitry.

## WATCH OPERATION

The normal display for the watch is: Hours: Minutes Day. Note that the day of week is indicated by the use of 7 flag outputs which are on, unless representing the particular day of the week in which case that flag turns off, allowing printed day of week to be visible.

One push and release of the "Display" button (S1) will display Month Date and Day for 3 seconds. If the display button is held depressed for longer than 3 seconds, Month Date will be replaced by: Seconds. One further depression of the display button will return Hours: Minutes and Day to the display. The Day flag and PM flags are always active.

## ALARM OPERATION

Two presses of the display button within 3 seconds will cause the Alarm Time (Hours: Minutes) to be displayed for 3 seconds. If armed, the alarm will emit two "beeping" sounds per second while the switch is depressed.

A third push of the display button within 3 seconds will cause the alarm to change state from armed to disarmed or disarmed to armed. When the alarm is armed a flag output will also be activated.

When the alarm is armed and the real time matches the alarm time, the alarm output will "beep" at 1 Hz intervals for 60 seconds. A single push of the display button will cause the alarm to enter a 5 minute "snooze" mode. The snooze may be repeated as many times as desired. Two pushes of the display button will cancel the alarm.

It should be noted that the AM/PM state of the Alarm setting is easily obtained by a single depression of the set button. Interrogation of the Alarm time without the "beeping" indication is obtainable through a double depression of the Set switch which will also provide PM information if a flag is available on the display. In each case the watch automatically returns to the normal time display mode.

## SETTING

Depressing the Set Button (S2) once will place the watch in the Alarm Hours set mode. The Alarm Hour will appear with an "A" (AM) or "P" (PM) indication in the right most position. The Alarm Hours will flash and will advance with each depression of the "Display" button or at a 2 Hz rate if the button is held. The display will return to normal mode 3 seconds after the last Set or Display input.

Two pushes of the Set Button before the 3 second timeout will cause the Alarm Minutes to flash. Alarm Minutes may be advanced as above. The display will return to normal 3 seconds after the last Set or Display input.

Three pushes of the Set Button before the 3 second timeout will cause Month Date Day display with Month flashing. The month is advanced with S1 as above. There is no automatic timeout return from this or any of the following three set states.

The next push of the Set Button will cause the Date to flash; the Date is advanced as above.

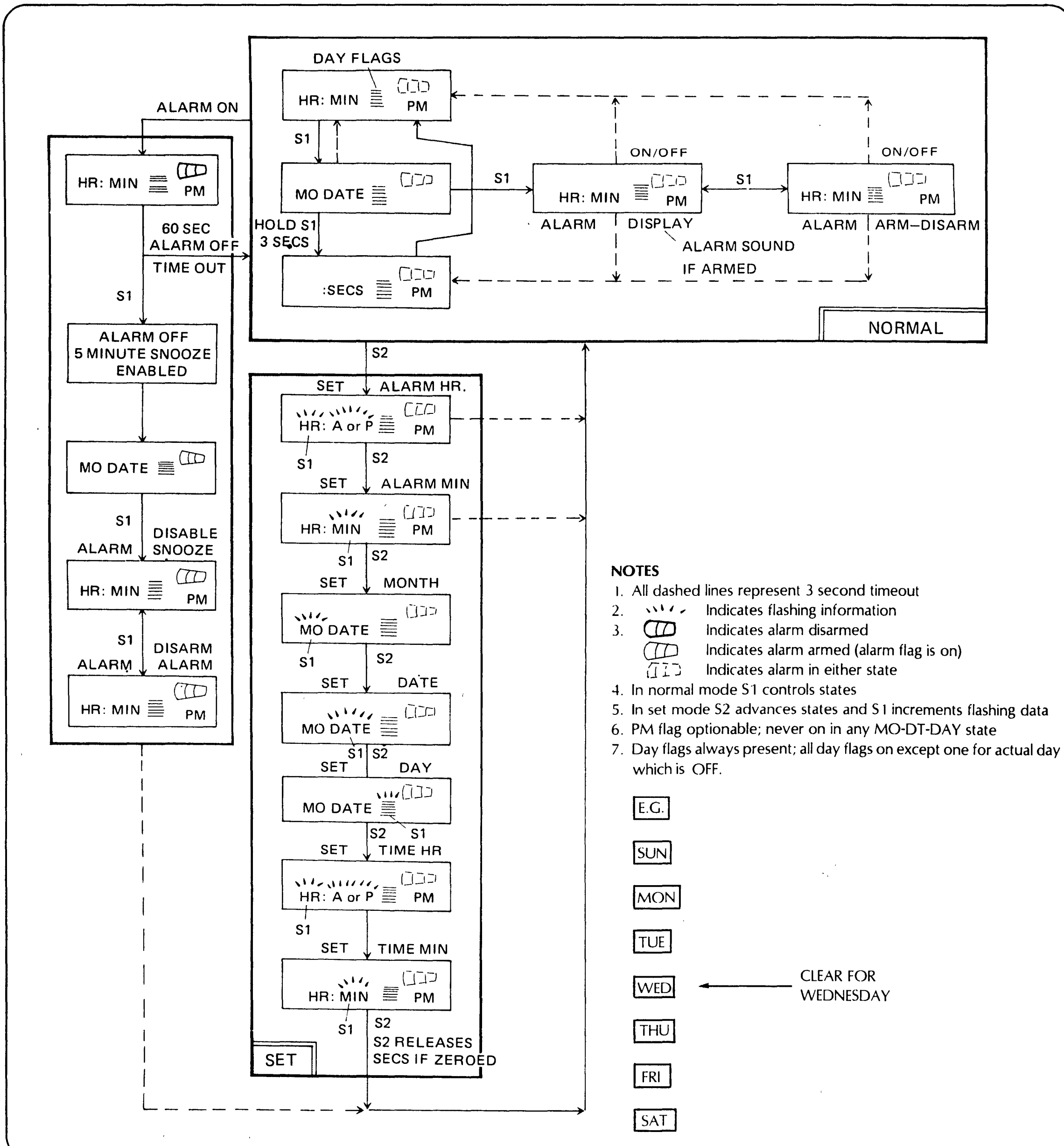
The next push of the Set Button causes the display of flashing Day Flag. The Day is advanced from one flag to the next by depressions of the Display button. The next push of the Set Button causes the display of flashing Hours: (actual time) with an "A" or "P" signifying AM or PM. The hour is advanced in the same way as other data.

The next push of the Set Button displays Hours: Minutes with minutes flashing. Minutes are advanced as above. If minutes are advanced, the seconds become "00" and hold until the next depression of S2 which returns the watch to the normal display. If minutes were not advanced, the last push of the Set Button places the watch in the normal display without altering the seconds count.

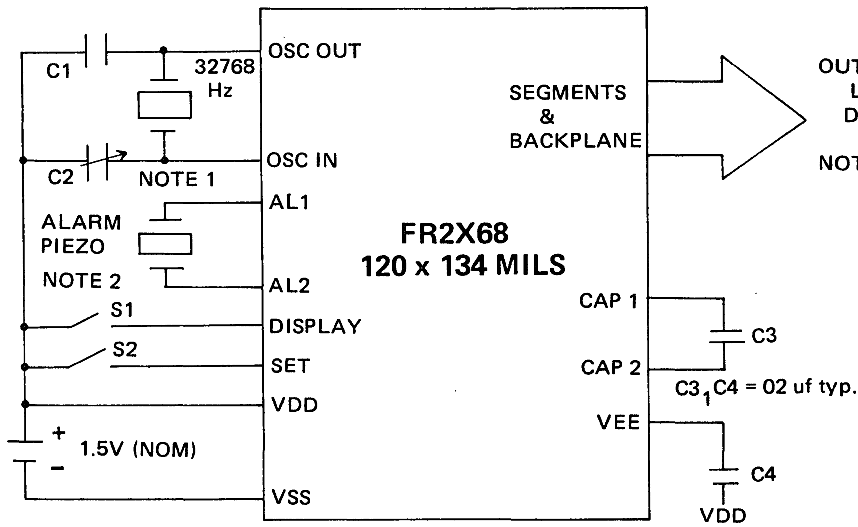
**NOTE**

The setting and viewing of actual time is always distinguishable from Alarm time by the fact that all Alarm time displays have a 3 second timeout feature returning the watch to normal time mode.

## FR2368 STATE DIAGRAM

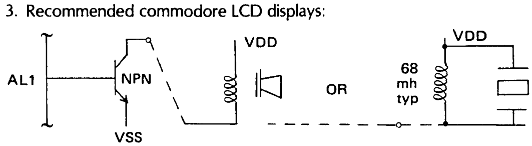


## FRONTIER FR2X68 SERIES SYSTEM DIAGRAM




**NOTES**

1. C1 and C2 Match chosen. Crystal. For faster oscillator startup C2 should be adjusted to minimum capacitance setting.
2. For louder alarm output the following circuit may be used to drive a ceramic resonator or magnetic speaker. Note frequency of alarm is 4 KHz.
3. Recommended commodore LCD displays:




FR2268 5017,5018 FR2368 5038 FR2568 5015,5040,5050.

4. As with all semiconductor devices, care should be taken to insure that no light is allowed to strike the die. Predictably light will increase $I_{DD}$ leakage and may cause malfunction. A non-transparent black coating is typically used and is recommended.

## FR2X68 ALARM OUTPUT NOTE

The FR2X68 series CMOS includes a number of alarm models which operate in an identical manner. All such die have been designed to drive typical piezo transducers directly from the chip. The basic circuit is shown in Figure 1.

It should be noted that ultimate loudness is, to a great extent, dependent upon such factors as appropriate mounting of the piezo, resonant frequency and other acoustic factors.

For applications requiring a significantly louder alarm, the circuit in Figure 2 has been used to amplify the voltage applied to the piezo. For best results, AL1 should be used to drive the NPN. This transistor should have a high collector-base breakdown voltage (e.g. 25 – 30 V) such as 2SC1623.

Figure 3 illustrates the use of a similar NPN transistor as a voltage clamping device to suppress externally generated voltage spikes from a piezo. Note that such spikes, when great enough in amplitude, may be able to overcome the chip protection circuity and possibly cause loss of data. The above circuit should not be needed in most cases, however if a very high degree of shock immunity is required, it has been effective in direct drive applications.

Direct Drive

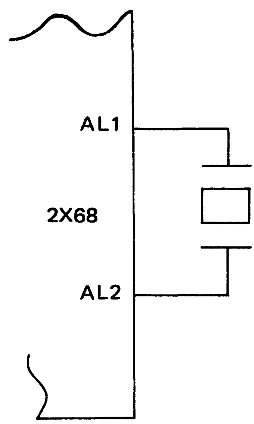



Figure 1

Loud Driven

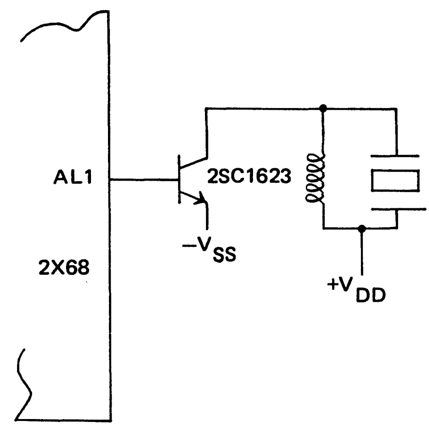



Figure 2

Shock Protection

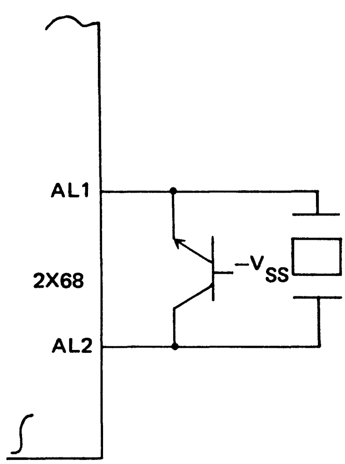
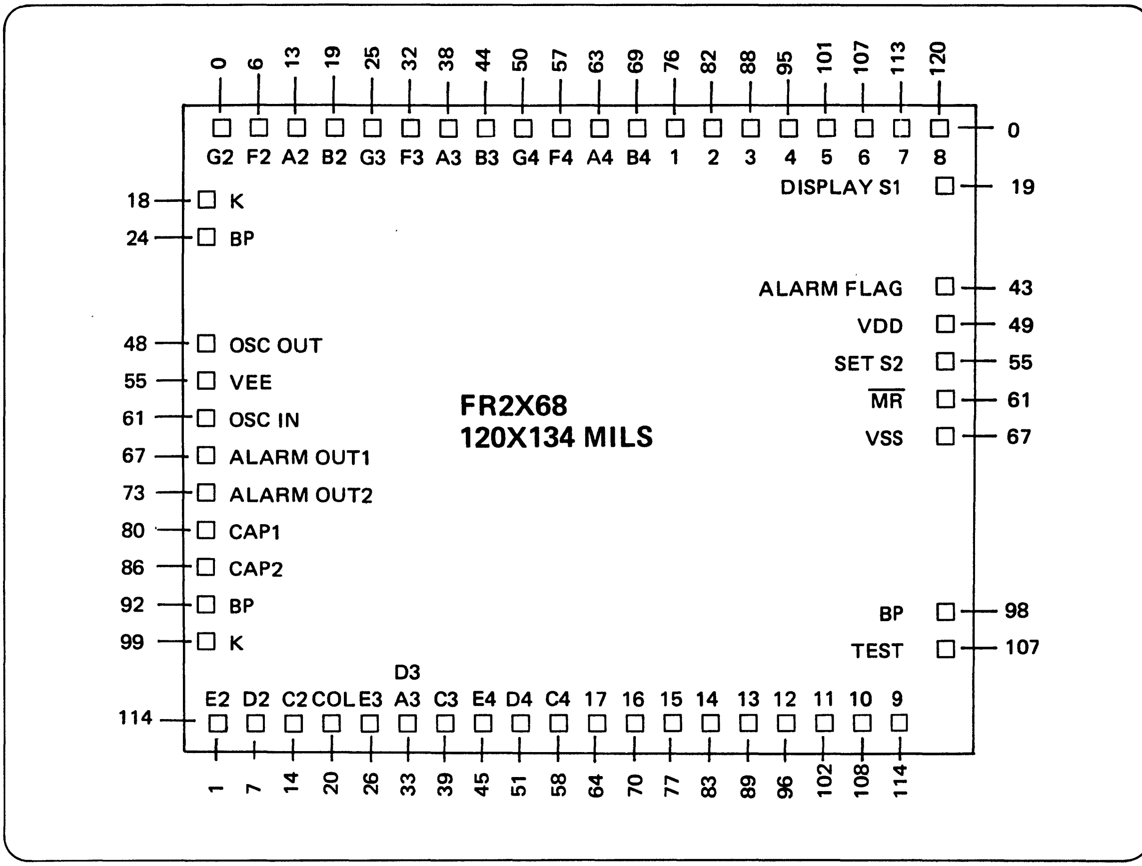



Figure 3

FR 2 X 68 PINOUTS




| PIN | FR 2068 | FR 2268 | FR 2368 | FR 2468 |
|---|---|---|---|---|
| 1 | G5 | – | MON | – |
| 2 | F5 | – | SUN | 5TH-10 |
| 3 | H5 | – | – | – |
| 4 | A5 | – | TUE | 6TH-10 |
| 5 | B5 | – | WED | 1ST-10 |
| 6 | F6 | – | – | – |
| 7 | A6 | – | – | – |
| 8 | B6 | AM | – | – |
| 9 | G6 | PM | – | – |
| 10 | C6 | – | – | – |
| 11 | J6 | – | PM | – |
| 12 | D6 | – | – | – |
| 13 | E6 | – | – | – |
| 14 | C5 | – | SAT | 2ND-10 |
| 15 | D5 | – | FRI | 3RD-10 |
| 16 | J5 | – | – | – |
| 17 | E5 | – | THUR | 4TH-10 |

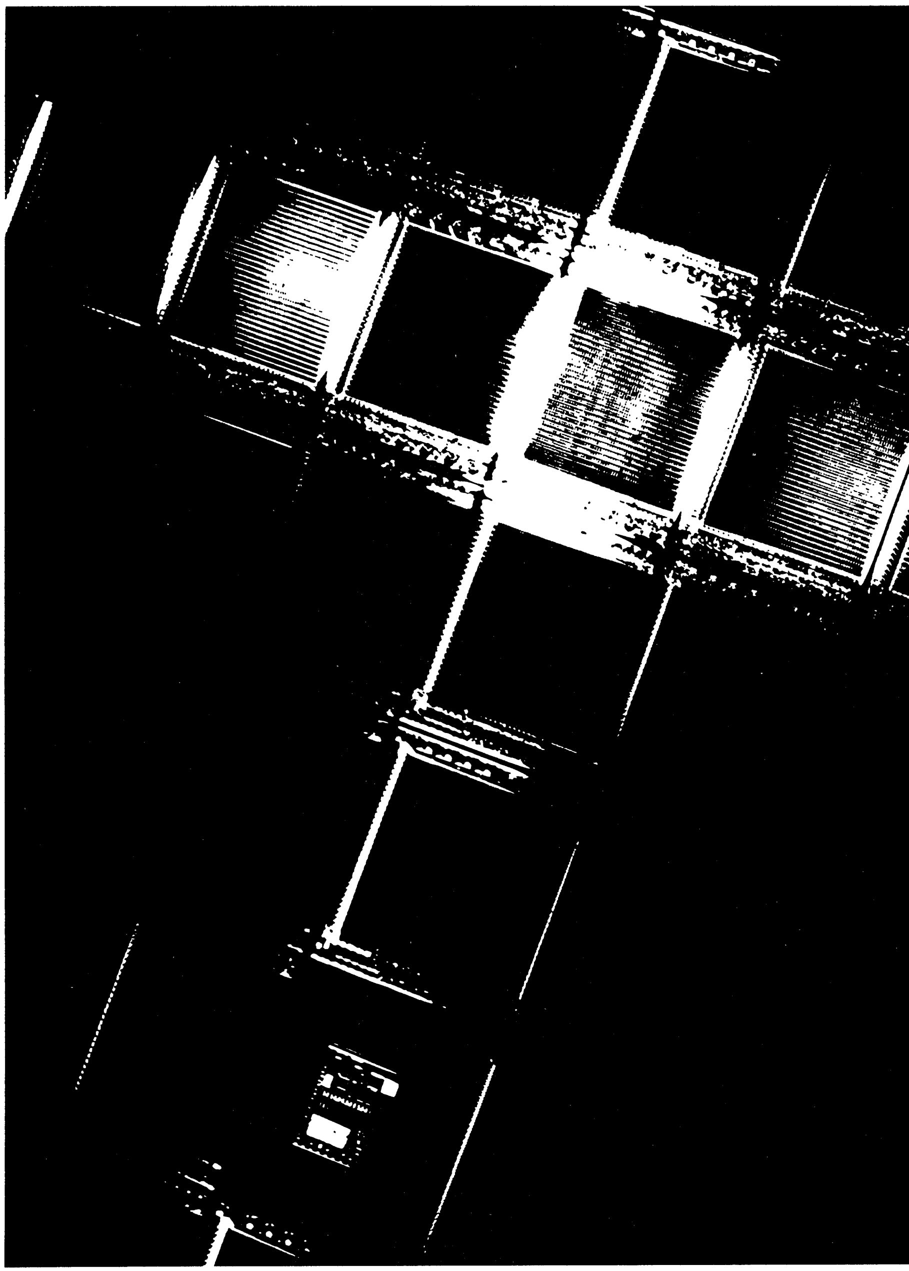
**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Operating Temperature | 0° to 70°C |
| Storage Temperatures | 25°C to 85°C |
| Voltage Any Pin | $V_{DD}$ + 3 V to $V_{SS}$ − .3 V |
| Supply Voltage ($V_{DD} - V_{SS}$) | 2.0 V |

**ELECTRICAL SPECIFICATIONS** $T_A$ = 25°C; $F_{OSC}$ = 32,768 KHz; $V_{DD}$ = 1.6 V (Unless Otherwise Indicated)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 1.35 | 1.5 | 1.7 | Volt | |
| $I_{DD}$ | Power Supply Current | | 1.5 | 3.0 | μA | Doubler connected but unloaded |
| $V_{EE}$ | Doubler Output Voltage (See Note) | −1.4 | | | Volt | $I_{EE}$ = 1 μA<br>$V_{DD}$ = 1.5 |
| $I_{IN}$ | Switch Input Current | | −2 | −25 | μA | $V_{IN} = V_{DD}$ |
| $V_{Start}$ osc. | Oscillator Start Voltage | 1.4 | | | Volt | |
| | Switch Debounce | | 62.5 | | mS | |
| | Alarm Output Resistance | | | 1.0 | KΩ | $V_{EE}$ = 1.4<br>$V_{Alarm} - V_{supply}$ = 0.5 V |
| | Avg. Alarm-On $I_{DD}$ | | 100 | | μA | |
| | Segment Output Current (Source or Sink) 1.0 | 1.0 | | | μA | $V_{EE}$ = −1.4<br>$V_{seg} - V_{supply}$ = 0.2 V |

# Section 4
# LCD



## LIQUID CRYSTAL DISPLAYS

Commodore offers a wide variety of standard liquid crystal displays for both mens and ladies watches. Superior surface technology employing low tilt angles, uniform LC thickness, and fast response times make these the most readable displays on the market today. Either direct drive or multiplexed, these displays are compatible with low voltage output CMOS with a peak voltage of 2.7 and as low as 1.5. Drive circuitry of this type is available from Commodore's Frontier division.

Commodore also offers LC displays for calculators, instruments, and a variety of custom applications. Our prototype facilities can take a customer's concept from spec sheet to finished displays in a matter of days.

Please contact the factory for details.

## ENVIRONMENTAL SPECIFICATIONS

| Test | Condition |
|---|---|
| Temperature Cycle | 10 cycles of 15 minute extremes at 0°C and 60°C in air with 15 seconds maximum transition time |
| Temperature Storage with polarizer — no bias[1] | 50°C for 96 hours including polarizer |
| Temperature Storage without polarizer — no bias | 1000 hours at 60°C-1000 hours at −20°C (operating current not to change by more than 50%) |
| UV Exposure | 500 hours direct sunlight at 25°C (operating current not to change by more than 50%) |

**NOTE**
1. Storage for extended periods or at higher temperatures may cause polarizer degradation.

## OPERATING CHARACTERISTICS

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Operating Voltage | 2.5 | 3.0 | 6.0 | Volts |
| Operating Frequency Range | 25.0 | 32.0 | 500 | Hz |
| Drive Current at 3 V — All Segments | | 350 | 800 | nA |
| Segment Capacitance | | | 15 | pF |
| Response Times: $t_{on}$ | | 100 | 130 | MSEC |
| $t_{off}$ | | 200 | 210 | MSEC |
| Operating Temperature | −10.0 | | 58 | °C |
| Storage Temperature | −20.0 | | 70 | °C |
| Viewing Angle | | 45 | | Degrees |
| Contrast Ratio (On Axis) | | 20:1 | | |
| Life Time | | 50000 | | Hours |

**NOTE**
Unless otherwise specified $T_A$ = 25°C and test voltages are 32 Hz square wave, 3.0 VAC.

**Rev 01**

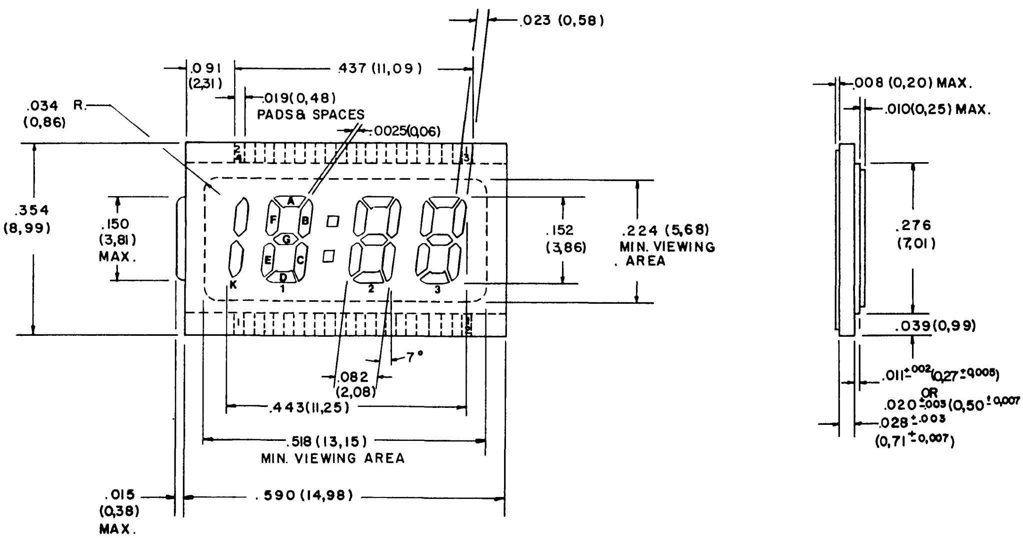
**DISPLAY AND CHIP GUIDE FOR COMMODORE OPTOELECTRONICS AND FRONTIER**

| | 2204 Basic 3½ or 4 Digit | 2222 3½ Digit-Biplex. Month/ Date Flags | 2268 3½ Digit With Alarm | 2268/2080 3½ Digit With Melody Alarm | 2368 3½ Digit With Alarm & Days of Week | 2668 Basic 6 Digit | *2068/2568 5½ Digit With Alarm | *2568/2080 5½ Digit With Melody Alarm | 2069 6 Digit With Chrono |
|---|---|---|---|---|---|---|---|---|---|
| **PEN** 320 x 550 | | 5075 | | | | | | | |
| **LADIES'** .354 x .590 | 5004 | 5060 | 5017 | | | | | | |
| .488 x .618 | | 5077 5063 | | 5067 | | | 5065 | 5059 | 5051 |
| .389 x .530 | | 5053 | | | | | | | |
| **UNISEX** .454 x .690 | 5007 | 5076 | 5036 | | | | 5042 | | |
| **MEN'S** .520 x .805 | 5012 | 5061 | 5018 | | 5038 | | | | |
| .454 x .827 | | | | | | | 5014 | | |
| .452 x .941 | | | | | | 5015 | 5015 | | |
| .637 x .806 | | 5064 | | | 5047 | | 5050 | 5066 | 5049 |
| .410 x .862 | | 5078 5052 | | | | | | | |
| .555 x .941 | | | | | | | | 5056 | |

*2068 Alarm Frequency = 2 kHz; 2568 Alarm Frequency = 4 kHz

## Model 5004 Ladies 3½ Digit Display

Outside Dimensions .354 (8,99) x .590 (14,98)
Digit Height .152 (3,86)

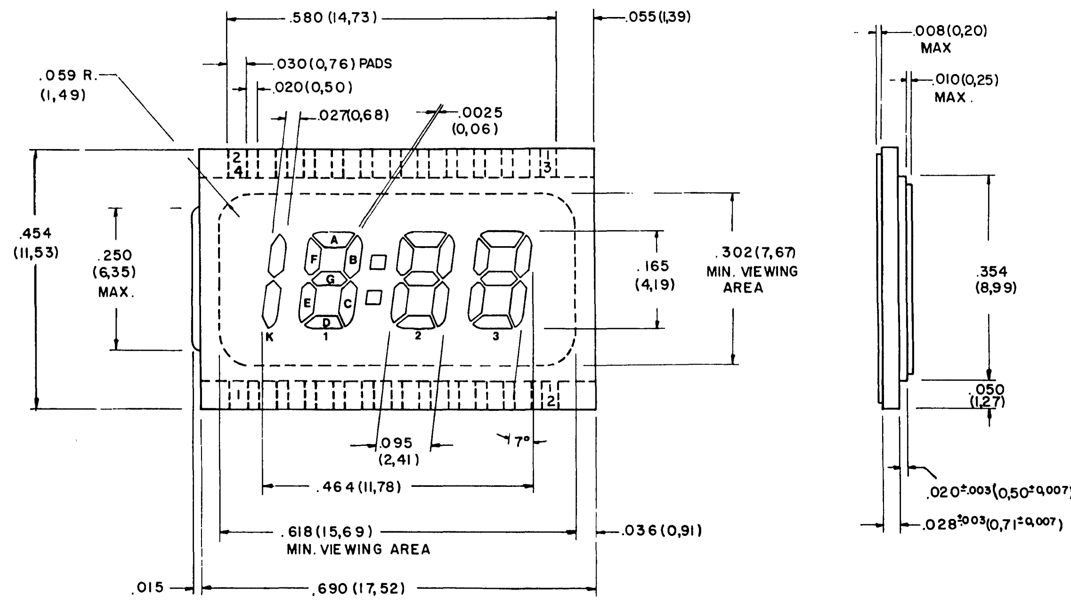



**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ± .005 (0,12)

### Pin Schedule

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Backplane | 7 | Seg $E_2$ | 13 | Seg $B_3$ | 19 | Seg $F_2$ |
| 2 | Half Digit | 8 | Seg $D_2$ | 14 | Seg $A_3$ | 20 | Seg $G_2$ |
| 3 | Seg $E_1$ | 9 | Seg $C_2$ | 15 | Seg $F_3$ | 21 | Seg $B_1$ |
| 4 | Seg $D_1$ | 10 | Seg $E_3$ | 16 | Seg $G_3$ | 22 | Seg $A_1$ |
| 5 | Seg $C_1$ | 11 | Seg $D_3$ | 17 | Seg $B_2$ | 23 | Seg $F_1$ |
| 6 | Colon | 12 | Seg $C_3$ | 18 | Seg $A_2$ | 24 | Seg $G_1$ |

**Model 5007 Unisex 3½ Digit Display**
Outside Dimensions .454 (11,53) x .690 (17,52)
Digit Height .165 (4,19)

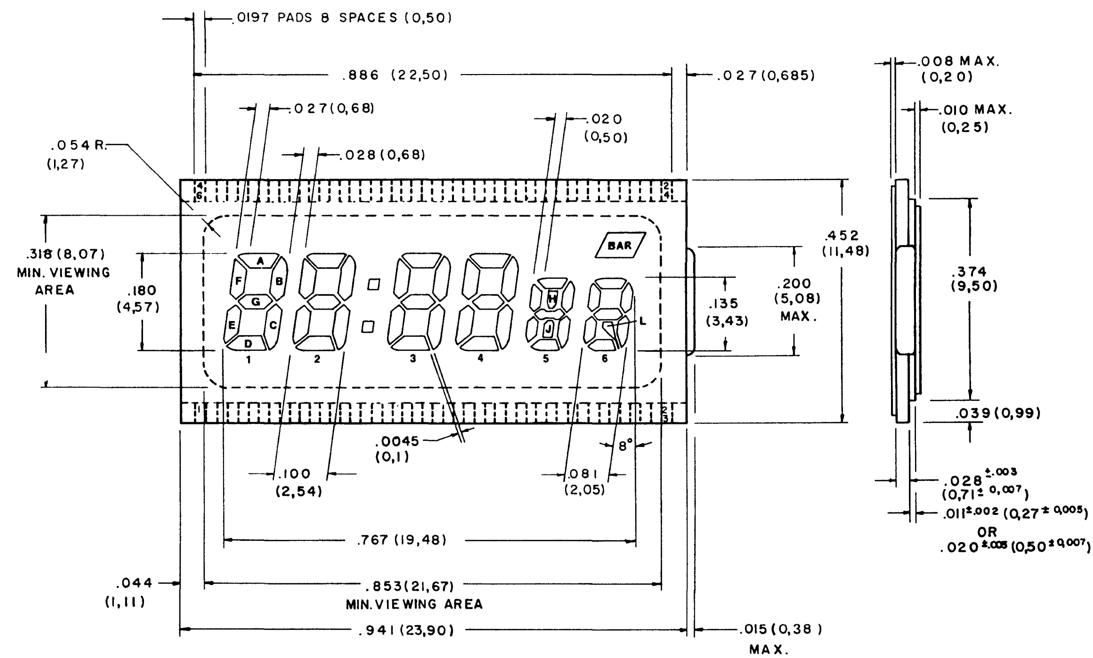



**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ±.005 (0,12)

**Pin Schedule**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Backplane | 7 | Seg $E_2$ | 13 | Seg $B_3$ | 19 | Seg $F_2$ |
| 2 | Half Digit | 8 | Seg $D_2$ | 14 | Seg $A_3$ | 20 | Seg $G_2$ |
| 3 | Seg $E_1$ | 9 | Seg $C_2$ | 15 | Seg $F_3$ | 21 | Seg $B_1$ |
| 4 | Seg $D_1$ | 10 | Seg $E_3$ | 16 | Seg $G_3$ | 22 | Seg $A_1$ |
| 5 | Seg $C_1$ | 11 | Seg $D_3$ | 17 | Seg $B_2$ | 23 | Seg $F_1$ |
| 6 | Colon | 12 | Seg $C_3$ | 18 | Seg $A_2$ | 24 | Seg $G_1$ |

**Model 5010 Men's 6 Digit Watch Display**
Outside Dimensions .452 (11,48) x .941 (23,90)
Digit Height .180 (4,57)
.135 (3,43)

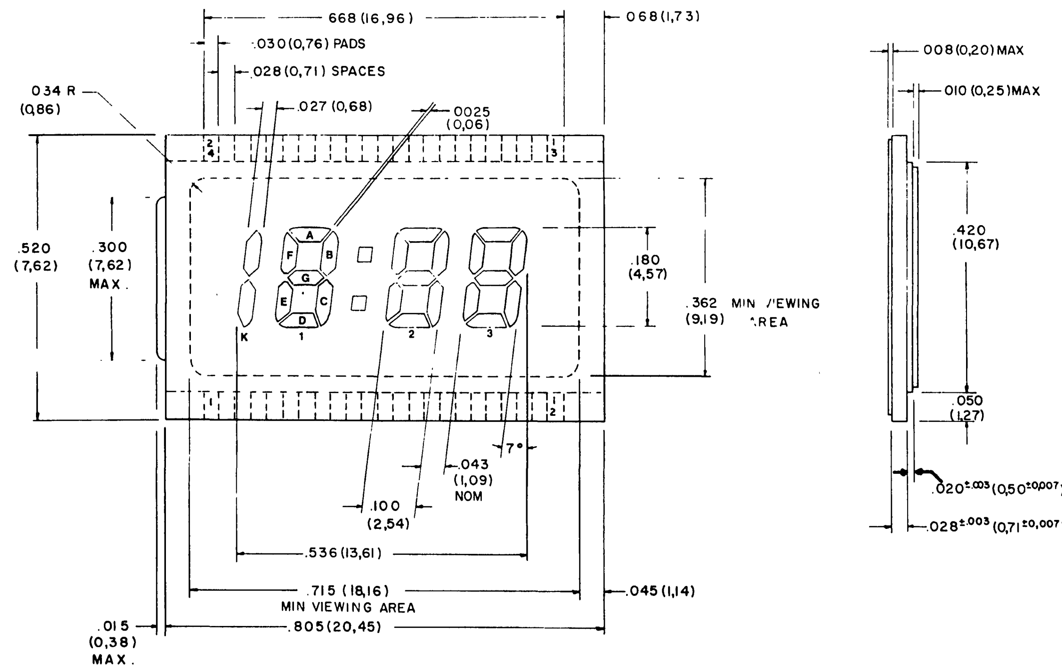



**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ± .005 (0,12)

**Pin Schedule**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Seg $E_1$ | 13 | Seg $C_4$ | 25 | Seg $B_6$ | 37 | Seg $B_3$ |
| 2 | Seg $D_1$, $A_1$ | 14 | Seg $E_5$ | 26 | Seg $A_6$ | 38 | Seg $F_3$ |
| 3 | Seg $C_1$ | 15 | Seg $J_5$ | 27 | Seg $F_6$ | 39 | Seg $G_3$ |
| 4 | Seg $E_2$ | 16 | Seg $D_5$ | 28 | Seg $B_6$ | 40 | Seg $B_2$ |
| 5 | Seg $D_2$ | 17 | Seg $C_5$ | 29 | Seg $A_5$ | 41 | Seg $A_2$ |
| 6 | Seg $C_2$ | 18 | Seg $E_6$ | 30 | Seg $H_5$ | 42 | Seg $F_2$ |
| 7 | Colon | 19 | Seg $D_6$ | 31 | Seg $F_5$ | 43 | Seg $G_2$ |
| 8 | Seg $E_3$ | 20 | Seg $L_6$ | 32 | Seg $G_5$ | 44 | Seg $B_1$ |
| 9 | Seg $A_3$, $D_3$ | 21 | Seg $C_6$ | 33 | Seg $B_4$ | 45 | Seg $F_1$ |
| 10 | Seg $C_3$ | 22 | Seg $G_6$ | 34 | Seg $A_4$ | 46 | Seg $G_1$ |
| 11 | Seg $E_4$ | 23 | Backplane | 35 | Seg $F_4$ | | |
| 12 | Seg $D_4$ | 24 | Bar | 36 | Seg $G_4$ | | |

**Model 5012 Men's 3½ Digit Watch Display**
Outside Dimensions .520 (7,62) x .805 (20,45)
Digit Height .180 (4,57)

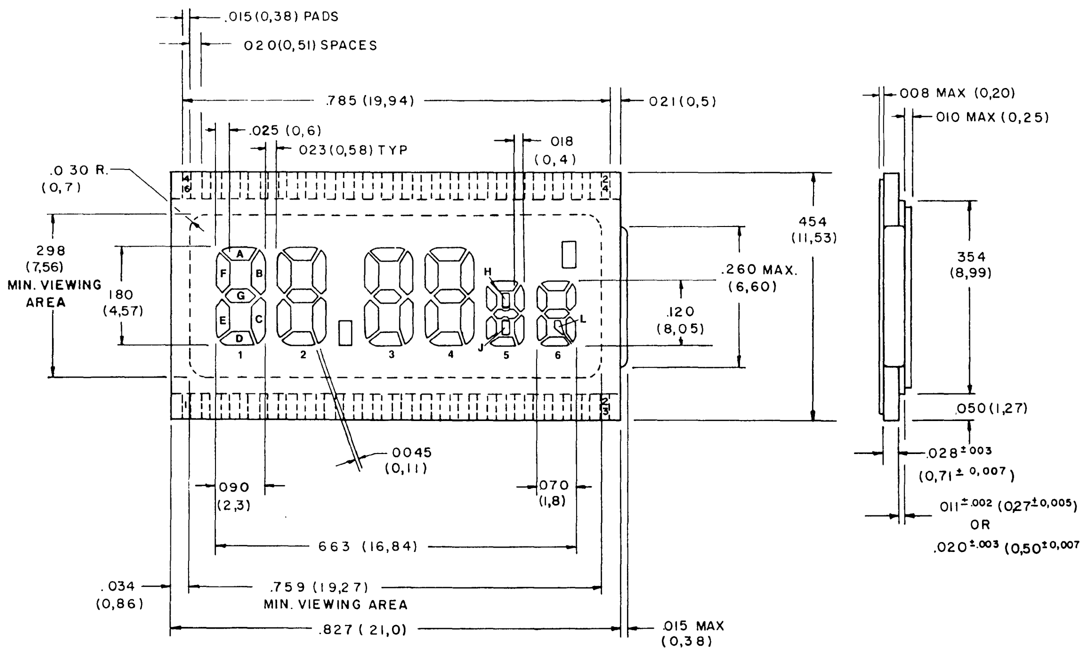



**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ± .005 (0,12)

**Pin Schedule**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Backplane | 7 | Seg $E_2$ | 13 | Seg $B_3$ | 19 | Seg $F_2$ |
| 2 | Half Digit | 8 | Seg $D_2$ | 14 | Seg $A_3$ | 20 | Seg $G_2$ |
| 3 | Seg $E_1$ | 9 | Seg $C_2$ | 15 | Seg $F_3$ | 21 | Seg $B_1$ |
| 4 | Seg $D_1$ | 10 | Seg $E_3$ | 16 | Seg $G_3$ | 22 | Seg $A_1$ |
| 5 | Seg $C_1$ | 11 | Seg $D_3$ | 17 | Seg $B_2$ | 23 | Seg $F_1$ |
| 6 | Colon | 12 | Seg $C_3$ | 18 | Seg $A_2$ | 24 | Seg $G_1$ |

**Model 5014 Men's 6 Digit Watch Display**
Outside Dimensions .454 (11,53) x .827 (21,0)
Digit Height .180 (4,5)
.120 (3,05)

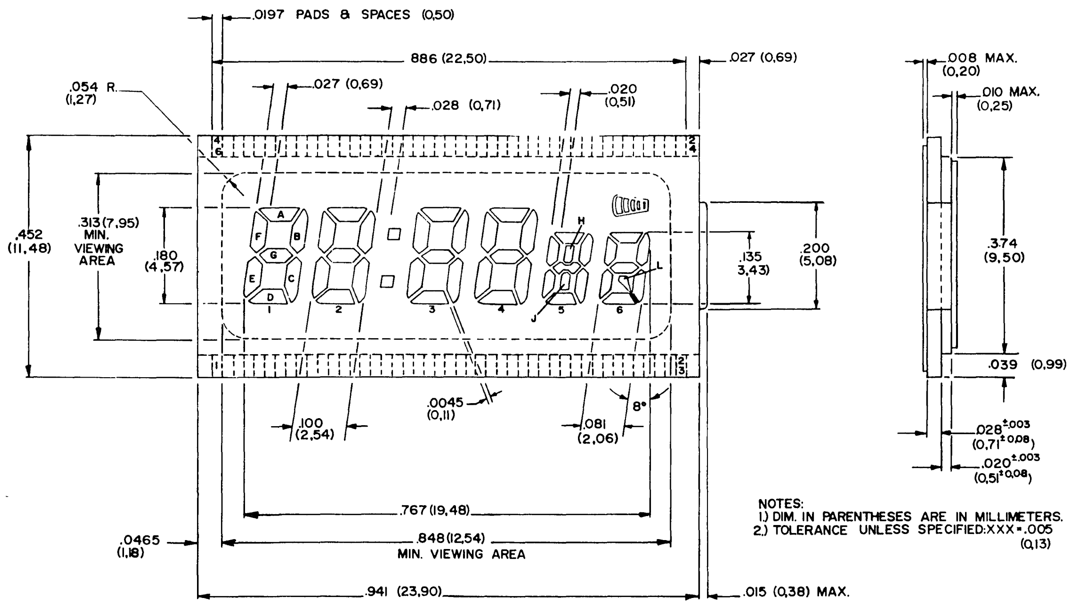



**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ±.005 (0,12)

**Pin Schedule**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Seg $E_1$ | 13 | Seg $C_4$ | 25 | Seg $B_6$ | 37 | Seg $B_3$ |
| 2 | Seg $D_1$, $A_1$ | 14 | Seg $E_5$ | 26 | Seg $A_6$ | 38 | Seg $F_3$ |
| 3 | Seg $C_1$ | 15 | Seg $J_5$ | 27 | Seg $F_6$ | 39 | Seg $G_3$ |
| 4 | Seg $E_2$ | 16 | Seg $D_5$ | 28 | Seg $B_5$ | 40 | Seg $B_2$ |
| 5 | Seg $D_2$ | 17 | Seg $C_5$ | 29 | Seg $A_5$ | 41 | Seg $A_2$ |
| 6 | Seg $C_2$ | 18 | Seg $E_6$ | 30 | Seg $H_5$ | 42 | Seg $F_2$ |
| 7 | Colon | 19 | Seg $D_6$ | 31 | Seg $F_5$ | 43 | Seg $G_2$ |
| 8 | Seg $E_3$ | 20 | Seg $L_6$ | 32 | Seg $G_5$ | 44 | Seg $B_1$ |
| 9 | Seg $A_3$, $D_3$ | 21 | Seg $C_6$ | 33 | Seg $B_4$ | 45 | Seg $F_1$ |
| 10 | Seg $C_3$ | 22 | Seg $G_6$ | 34 | Seg $A_4$ | 46 | Seg $G_1$ |
| 11 | Seg $E_4$ | 23 | Backplane | 35 | Seg $F_4$ | | |
| 12 | Seg $D_4$ | 24 | Bar | 36 | Seg $G_4$ | | |

**Model 5015 Men's 6 Digit Watch Display With Alarm**
Outside Dimensions .452 (11,48) x .941 (23,90)
Digit Height .180 (4,57)
.135 (3,43)



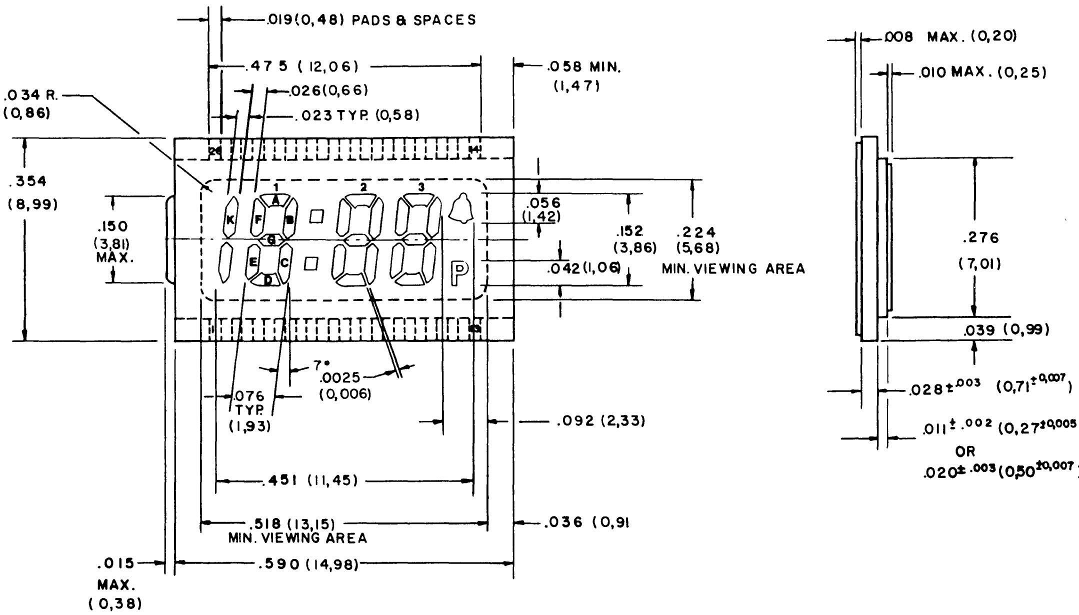

**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ± .005 (0,12)

## Pin Schedule

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Seg $E_1$ | 13 | Seg $C_4$ | 25 | Seg $B_6$ | 37 | Seg $B_3$ |
| 2 | Seg $D_1$, $A_1$ | 14 | Seg $E_5$ | 26 | Seg $A_6$ | 38 | Seg $F_3$ |
| 3 | Seg $C_1$ | 15 | Seg $J_5$ | 27 | Seg $F_6$ | 39 | Seg $G_3$ |
| 4 | Seg $E_2$ | 16 | Seg $D_5$ | 28 | Seg $B_5$ | 40 | Seg $B_2$ |
| 5 | Seg $D_2$ | 17 | Seg $C_5$ | 29 | Seg $A_5$ | 41 | Seg $A_2$ |
| 6 | Seg $C_2$ | 18 | Seg $E_6$ | 30 | Seg $H_5$ | 42 | Seg $F_2$ |
| 7 | Colon | 19 | Seg $D_6$ | 31 | Seg $F_5$ | 43 | Seg $G_2$ |
| 8 | Seg $E_3$ | 20 | Seg $L_6$ | 32 | Seg $G_5$ | 44 | Seg $B_1$ |
| 9 | Seg $A_3$, $D_3$ | 21 | Seg $C_6$ | 33 | Seg $B_4$ | 45 | Seg $F_1$ |
| 10 | Seg $C_3$ | 22 | Seg $G_6$ | 34 | Seg $A_4$ | 46 | Seg $G_1$ |
| 11 | Seg $E_4$ | 23 | Backplane | 35 | Seg $F_4$ | | |
| 12 | Seg $D_4$ | 24 | Alarm | 36 | Seg $G_4$ | | |

## Model 5017 Ladies 3½ Digit Watch Display With Alarm and PM Flags

Outside Dimensions .354 (8,99) x .590 (14,99)
Digit Height .152 (3,86)

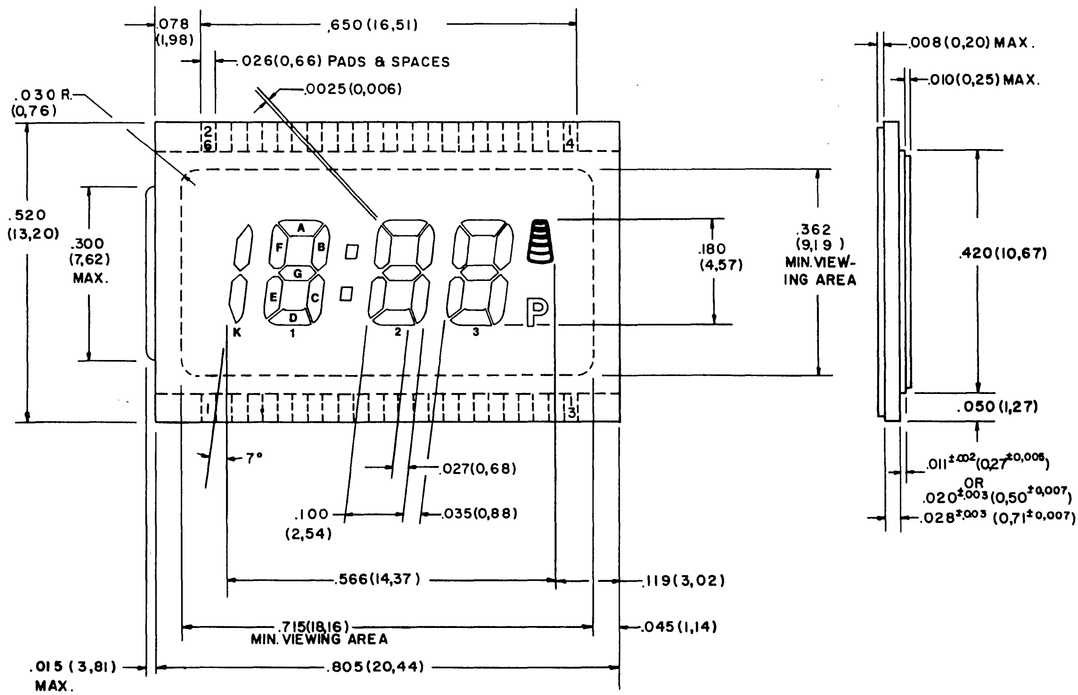



**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ± .005 (0,12)

### Pin Schedule

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Backplane | 8 | Seg $D_2$ | 15 | Seg $B_3$ | 22 | Seg $G_2$ |
| 2 | Half Digit | 9 | Seg $C_2$ | 16 | Seg $A_3$ | 23 | Seg $B_1$ |
| 3 | Seg $E_1$ | 10 | Seg $E_3$ | 17 | Seg $F_3$ | 24 | Seg $A_1$ |
| 4 | Seg $D_1$ | 11 | Seg $D_3$ | 18 | Seg $G_3$ | 25 | Seg $F_1$ |
| 5 | Seg $C_1$ | 12 | Seg $C_3$ | 19 | Seg $B_2$ | 26 | Seg $G_1$ |
| 6 | Colon | 13 | PM | 20 | Seg $A_2$ | | |
| 7 | Seg $E_2$ | 14 | Alarm | 21 | Seg $F_2$ | | |

**Model 5018 Men's 3½ Digit Display With Alarm/PM**
Outside Dimensions .520 (13,20) x .805 (20,44)
Digit Height .180 (4,57)




**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ± .005 (0,12)

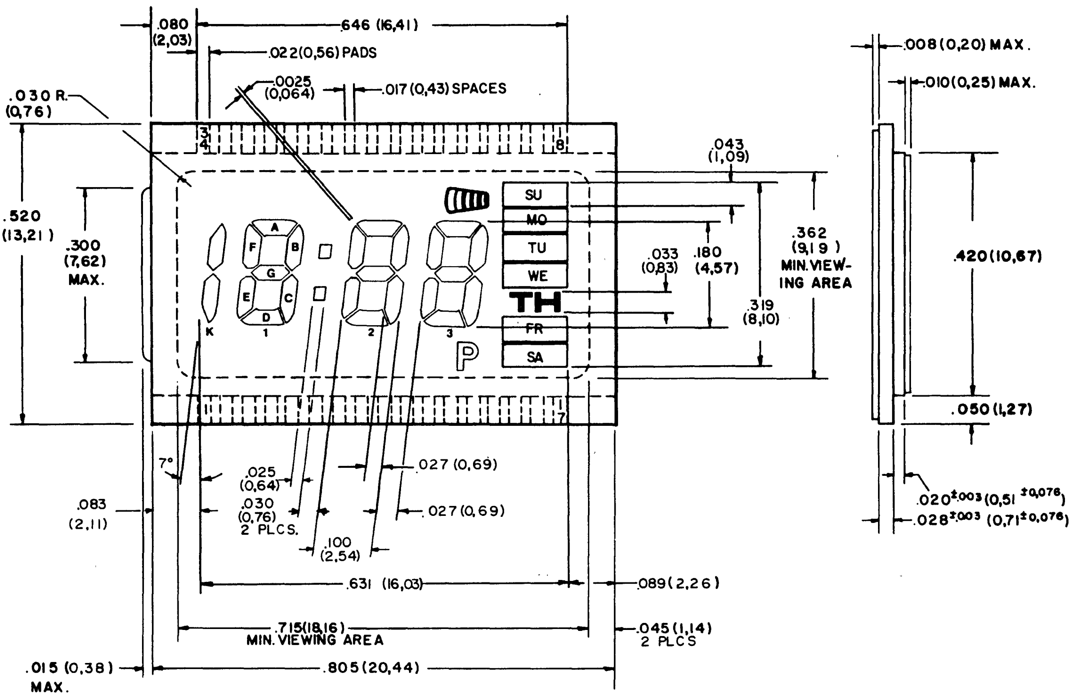
**Pin Schedule**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Backplane | 8 | Seg $D_2$ | 15 | Seg $B_3$ | 22 | Seg $G_2$ |
| 2 | Half Digit | 9 | Seg $C_2$ | 16 | Seg $A_3$ | 23 | Seg $B_1$ |
| 3 | Seg $E_1$ | 10 | Seg $E_3$ | 17 | Seg $F_3$ | 24 | Seg $A_1$ |
| 4 | Seg $D_1$ | 11 | Seg $D_3$ | 18 | Seg $G_3$ | 25 | Seg $F_1$ |
| 5 | Seg $C_1$ | 12 | Seg $C_3$ | 19 | Seg $B_2$ | 26 | Seg $G_1$ |
| 6 | Colon | 13 | PM | 20 | Seg $A_2$ | | |
| 7 | Seg $E_2$ | 14 | Alarm | 21 | Seg $F_2$ | | |

**Model 5038 Men's 3½ Digit Watch Display With Alarm, PM, and Day Flags**

Outside Dimensions .520 (13,21) x .805 (20,44)

Digit Height .180 (4,57)




**NOTE**

Dimensions in Parentheses are Millimeters.

Tolerance unless Specified: XXX = ± .005 (0,12)

**Pin Schedule**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Backplane | 10 | Seg $E_3$ | 19 | Tuesday | 27 | Seg $B_2$ |
| 2 | Half Digit | 11 | Seg $D_3$ | 20 | Sunday | 28 | Seg $A_2$ |
| 3 | Seg $E_1$ | 12 | Seg $C_3$ | 21 | Monday | 29 | Seg $F_2$ |
| 4 | Seg $D_1$ | 13 | PM | 22 | Alarm | 30 | Seg $G_2$ |
| 5 | Seg $C_1$ | 14 | Thursday | 23 | Seg $B_3$ | 31 | Seg $B_1$ |
| 6 | Colon | 15 | Friday | 24 | Seg $A_3$ | 32 | Seg $A_1$ |
| 7 | Seg $E_2$ | 16 | Saturday | 25 | Seg $F_3$ | 33 | Seg $F_1$ |
| 8 | Seg $D_2$ | 17 | (Blank) | 26 | Seg $G_3$ | 34 | Seg $G_1$ |
| 9 | Seg $C_2$ | 18 | Wednesday | | | | |

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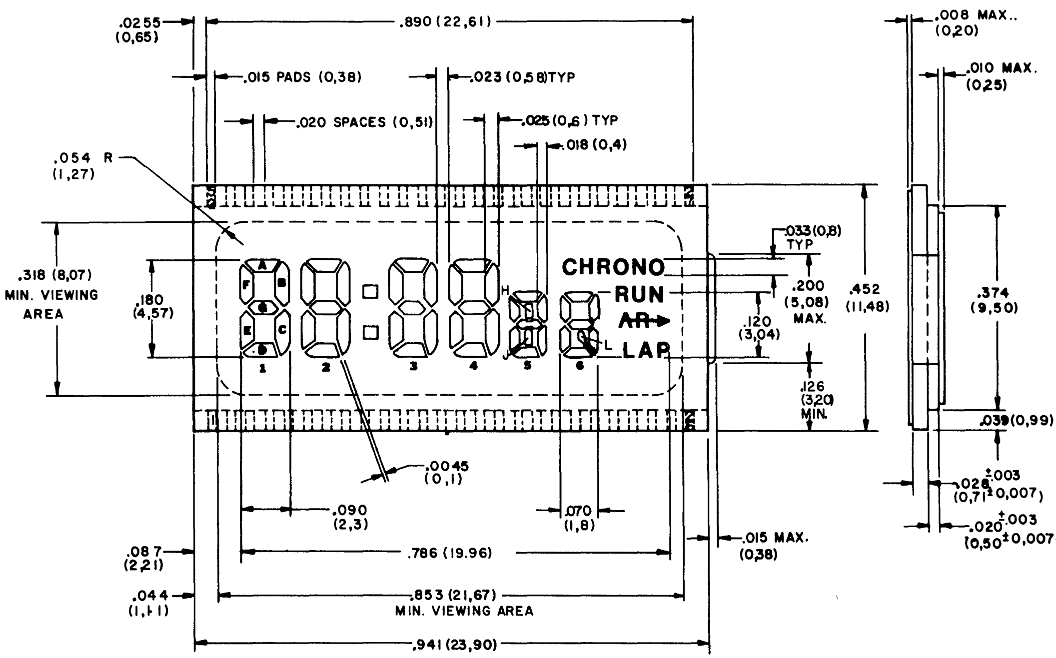
**LCD**

**Model 5039 Men's 6 Digit "Super Chrono" Watch Display With Chrono, Run, Auto Range and Lap Flags**
Outside Dimensions .452 (11,48) x .941 (23,90)
Digit Height .180 (4,57)
.120 (8,05)




**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ± .005 (0,12)

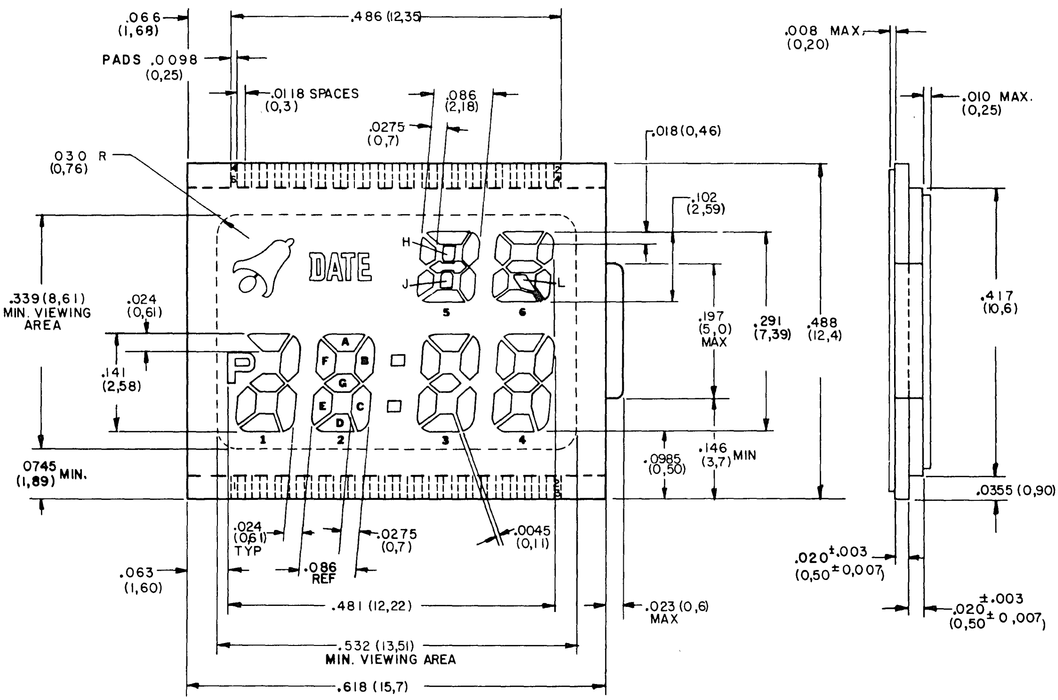
**Pin Schedule**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Seg $E_1$ | 14 | Seg $E_5$ | 27 | Chrono | 40 | Seg $A_4$ |
| 2 | Seg $D_1$, $A_1$ | 15 | Seg $J_5$ | 28 | Run | 41 | Seg $F_4$ |
| 3 | Seg $C_1$ | 16 | Seg $D_5$ | 29 | Auto Range | 42 | Seg $G_4$ |
| 4 | Seg $E_2$ | 17 | Seg $C_5$ | 30 | Lap | 43 | Seg $B_3$ |
| 5 | Seg $D_2$ | 18 | Seg $E_6$ | 31 | Seg $B_6$ | 44 | Seg $F_3$ |
| 6 | Seg $C_2$ | 19 | Seg $D_6$ | 32 | Seg $A_6$ | 45 | Seg $G_3$ |
| 7 | Colon | 20 | Seg $L_6$ | 33 | Seg $F_6$ | 46 | Seg $B_2$ |
| 8 | Seg $E_3$ | 21 | Seg $C_6$ | 34 | Seg $B_5$ | 47 | Seg $A_2$ |
| 9 | Seg $A_3$, $D_3$ | 22 | Seg $G_6$ | 35 | Seg $A_5$ | 48 | Seg $F_2$ |
| 10 | Seg $C_3$ | 23 | Backplane | 36 | Seg $H_5$ | 49 | Seg $G_2$ |
| 11 | Seg $E_4$ | 24 | (Blank) | 37 | Seg $F_5$ | 50 | Seg $B_1$ |
| 12 | Seg $D_4$ | 25 | (Blank) | 38 | Seg $G_5$ | 51 | Seg $F_1$ |
| 13 | Seg $C_4$ | 26 | (Blank) | 39 | Seg $B_4$ | 52 | Seg $G_1$ |

**Model 5040 Ladies 6 Digit Multipurpose Watch Display With Alarm, PM, and Date Flags.**

Outside Dimensions .488 (12,4 x .618 (15,7)

Digit Height .141 (3,6)
.102 (2,6)




**NOTE**
Dimensions in Parentheses are Millimeters.
Tolerance unless Specified: XXX = ±.004 (0,10)

## Pin Schedule

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Seg $E_1$ | 13 | Seg $C_4$ | 25 | Seg $A_6$ | 37 | Seg $F_3$ |
| 2 | Seg $D_1$, $G_1$, $A_1$ | 14 | Seg $E_5$ | 26 | Seg $F_6$ | 38 | Date |
| 3 | Seg $C_1$ | 15 | Seg $J_5$ | 27 | Seg $B_5$ | 39 | Seg $G_3$ |
| 4 | Seg $E_2$ | 16 | Seg $D_5$ | 28 | Seg $A_5$ | 40 | Alarm |
| 5 | Seg $D_2$ | 17 | Seg $C_5$ | 29 | Seg $H_5$ | 41 | Seg $B_2$ |
| 6 | Seg $C_2$ | 18 | Seg $E_6$ | 30 | Seg $F_5$ | 42 | Seg $A_2$ |
| 7 | Colon | 19 | Seg $D_6$ | 31 | Seg $G_5$ | 43 | Seg $F_2$ |
| 8 | Seg $E_3$ | 20 | Seg $L_6$ | 32 | Seg $B_4$ | 44 | Seg $G_2$ |
| 9 | Seg $A_3$, $D_3$ | 21 | Seg $C_6$ | 33 | Seg $A_4$ | 45 | Seg $B_1$ |
| 10 | Seg $C_3$ | 22 | Seg $G_6$ | 34 | Seg $F_4$ | 46 | PM |
| 11 | Seg $E_4$ | 23 | Backplane | 35 | Seg $G_4$ | | |
| 12 | Seg $D_4$ | 24 | Seg $B_6$ | 36 | Seg $B_3$ | | |

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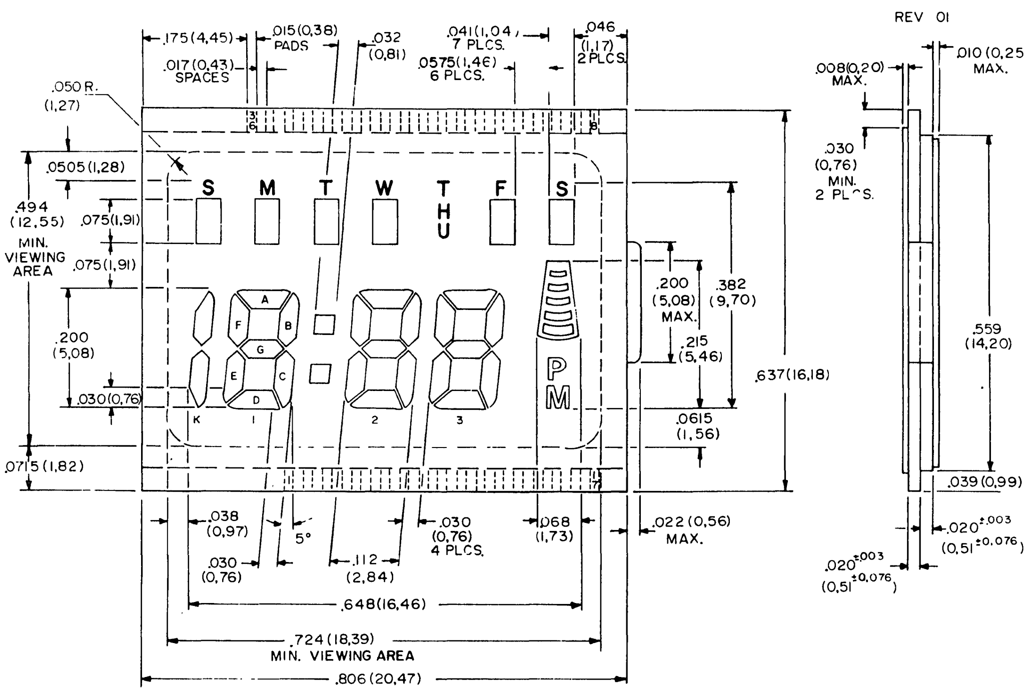
## LCD

**Model 5047 Men's 3½ Digit Direct Drive Watch Display With Days of Week, Alarm, and PM Flags**
Outside Dimensions .637 (16,18) x .806 (20,47)
Digit Height .200 (5,08)

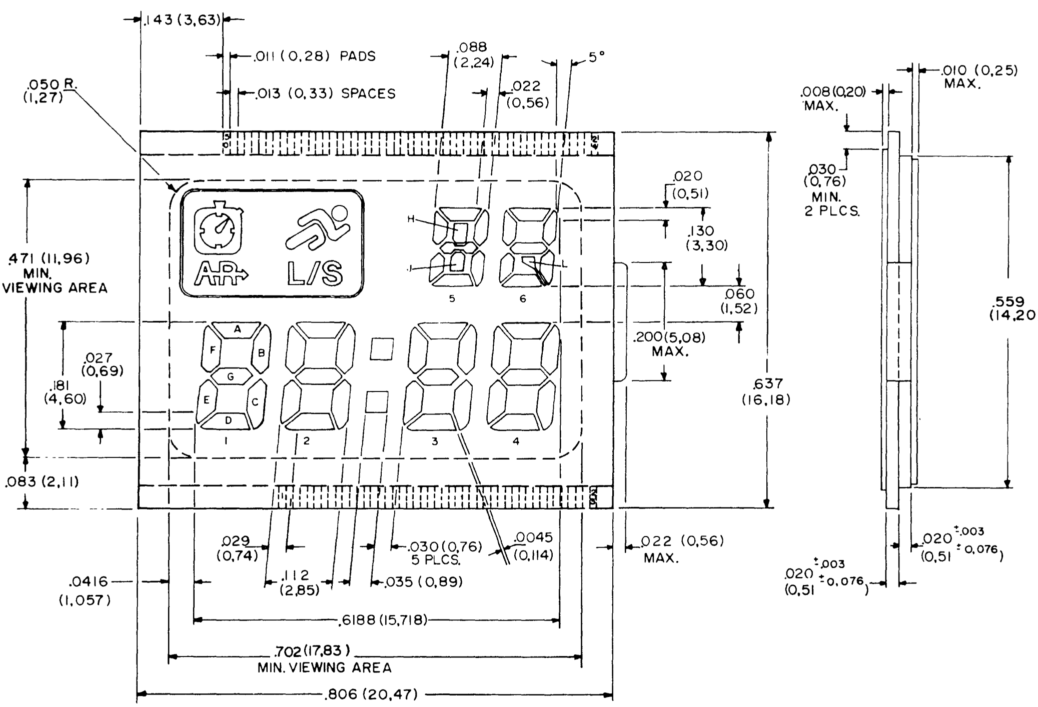



**Notes:**
1). Dimensions in parentheses are in millimeters.
2). Tolerances unless specified xxx = ±.004(0,10).
3). Days of week are permanently printed on display.

**PIN SCHEDULE**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Backplane | 10 | Seg $C_2$ | 19 | Blank | 28 | Seg $F_2$ |
| 2 | Blank | 11 | Seg $E_3$ | 20 | Blank | 29 | Seg $G_2$ |
| 3 | Seg K | 12 | Seg $D_3$ | 21 | Seg $B_3$ | 30 | Tuesday |
| 4 | Seg $E_1$ | 13 | Seg $C_3$ | 22 | Seg $A_3$ | 31 | Monday |
| 5 | Seg $D_1$ | 14 | Thursday | 23 | Seg $F_3$ | 32 | Seg $B_1$ |
| 6 | Seg $C_1$ | 15 | Friday | 24 | Seg $G_3$ | 33 | Seg $A_1$ |
| 7 | Colon | 16 | Saturday | 25 | Wednesday | 34 | Seg $F_1$ |
| 8 | Seg $E_2$ | 17 | PM | 26 | Seg $B_2$ | 35 | Seg $G_1$ |
| 9 | Seg $D_2$ | 18 | Alarm | 27 | Seg $A_2$ | 36 | Sunday |

**Model 5049 Men's 6 Digit "Super Chrono" Watch Display With Chrono, Run, Auto Range and Lap/Split Flags**
Outside Dimensions .637 (16,18) x .806 (20,47)
Digit Height .181 (4,60)
.130 (3,30)




**Notes:**
1). Dim. in parentheses are millimeters.
2). Tolerance unless specified: xxx = ± .005 (0.13).
3). Indicator frame is permanently printed on display.

**PIN SCHEDULE**

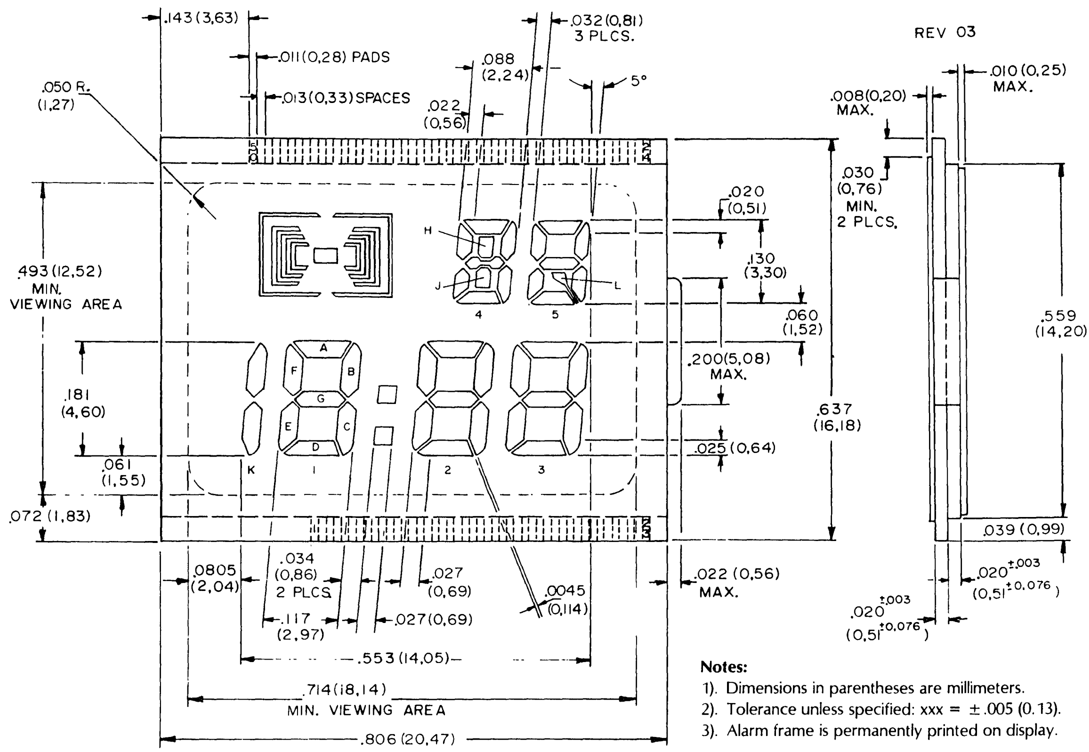
| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | Seg $E_1$ | 14 | Seg $E_5$ | 27 | Seg $B_5$ | 40 | AUTORANGE |
| 2 | Seg $A_1$, $D_1$ | 15 | Seg $J_5$ | 28 | Seg $A_5$ | 41 | LAP/SPLIT |
| 3 | Seg $C_1$ | 16 | Seg $D_5$ | 29 | Seg $H_5$ | 42 | RUN |
| 4 | Seg $E_2$ | 17 | Seg $C_5$ | 30 | Seg $F_5$ | 43 | CHRONO |
| 5 | Seg $D_2$ | 18 | Seg $E_6$ | 31 | Seg $G_5$ | 44 | Seg $B_3$ |
| 6 | Seg $C_2$ | 19 | Seg $D_6$ | 32 | Seg $B_4$ | 45 | Seg $A_2$ |
| 7 | COLON | 20 | Seg $L_6$ | 33 | Seg $A_4$ | 46 | Seg $F_2$ |
| 8 | Seg $E_3$ | 21 | Seg $C_6$ | 34 | Seg $F_4$ | 47 | Seg $G_2$ |
| 9 | Seg $D_3$ | 22 | Seg $G_6$ | 35 | Seg $G_4$ | 48 | Seg $B_1$ |
| 10 | Seg $C_3$ | 23 | Backplane | 36 | Seg $B_3$ | 49 | Seg $F_1$ |
| 11 | Seg $E_4$ | 24 | Seg $B_6$ | 37 | Seg $A_3$ | 50 | Seg $G_1$ |
| 12 | Seg $D_4$ | 25 | Seg $A_6$ | 38 | Seg $F_3$ | | |
| 13 | Seg $C_4$ | 26 | Seg $F_6$ | 39 | Seg $G_3$ | | |

**Model 5050 Men's 5½ Digit Direct Drive Watch Display With Alarm Flag**

Outside Dimensions .637 (16,18) x .806 (20,47)

Digit Height .181 (4,60)

.130 (3,30)




**Notes:**

1). Dimensions in parentheses are millimeters.

2). Tolerance unless specified: xxx = ± .005 (0.13).

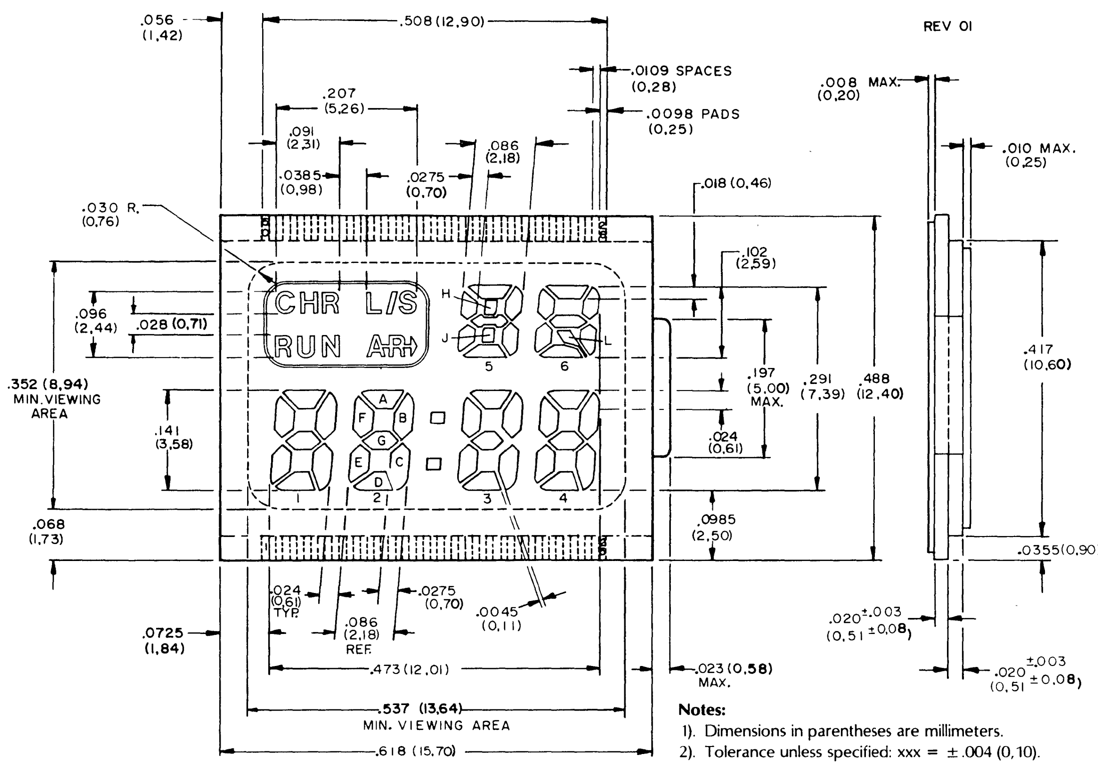
3). Alarm frame is permanently printed on display.

**PIN SCHEDULE**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | BLANK | 14 | Seg $E_4$ | 27 | Seg $B_4$ | 40 | ALARM |
| 2 | BLANK | 15 | Seg $J_4$ | 28 | Seg $A_4$ | 41 | BLANK |
| 3 | Seg K | 16 | Seg $D_4$ | 29 | Seg $H_4$ | 42 | BLANK |
| 4 | Seg $E_1$ | 17 | Seg $C_4$ | 30 | Seg $F_4$ | 43 | BLANK |
| 5 | Seg $D_1$ | 18 | Seg $E_5$ | 31 | Seg $G_4$ | 44 | Seg $B_1$ |
| 6 | Seg $C_1$ | 19 | Seg $D_5$ | 32 | Seg $B_3$ | 45 | Seg $A_1$ |
| 7 | Seg COLON | 20 | Seg $L_5$ | 33 | Seg $A_3$ | 46 | Seg $F_1$ |
| 8 | Seg $E_2$ | 21 | Seg $C_5$ | 34 | Seg $F_3$ | 47 | Seg $G_1$ |
| 9 | Seg $A_2$, $D_2$ | 22 | Seg $G_5$ | 35 | Seg $G_3$ | 48 | BLANK |
| 10 | Seg $C_2$ | 23 | BACKPLANE | 36 | Seg $B_2$ | 49 | BLANK |
| 11 | Seg $E_3$ | 24 | Seg $B_5$ | 37 | BLANK | 50 | BLANK |
| 12 | Seg $D_3$ | 25 | Seg $A_5$ | 38 | Seg $F_2$ | | |
| 13 | Seg $C_3$ | 26 | Seg $F_5$ | 39 | Seg $G_2$ | | |

## Model 5051 Ladies' 6 Digit Direct Drive Watch Display
## With Chrono, Run, Auto Range and Lap/Split Flags

Outside Dimensions .488 (12,40) x .618 (15,70)
Digit Height .141 (3,58)
.102 (2,59)

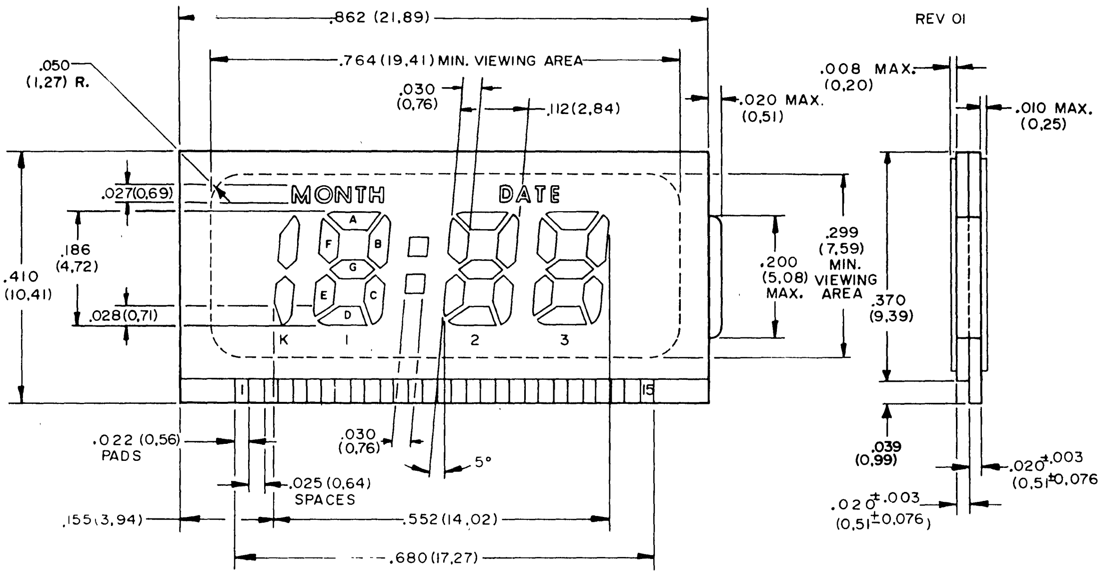



**Notes:**
1). Dimensions in parentheses are millimeters.
2). Tolerance unless specified: xxx = ± .004 (0,10).
3). Indicator frame is permanently printed on display.

**PIN SCHEDULE**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Seg $F_1$ | 14 | Seg $D_4$ | 27 | Seg $A_6$ | 40 | Seg $F_3$ |
| 2 | Seg $G_1$ | 15 | Seg $C_4$ | 28 | Seg $F_6$ | 41 | Seg $G_3$ |
| 3 | Seg $E_1$ | 16 | Seg $E_5$ | 29 | Seg $B_5$ | 42 | Autorange |
| 4 | Seg $A_1$, $D_1$ | 17 | Seg $J_5$ | 30 | Seg $A_5$ | 43 | Lap/Split |
| 5 | Seg $C_1$ | 18 | Seg $D_5$ | 31 | Seg $H_5$ | 44 | Run |
| 6 | Seg $E_2$ | 19 | Seg $C_5$ | 32 | Seg $F_5$ | 45 | Chrono |
| 7 | Seg $D_2$ | 20 | Seg $E_6$ | 33 | Seg $G_5$ | 46 | Seg $B_2$ |
| 8 | Seg $C_2$ | 21 | Seg $D_6$ | 34 | Seg $B_4$ | 47 | Seg $A_2$ |
| 9 | Colon | 22 | Seg $L_6$ | 35 | Seg $A_4$ | 48 | Seg $F_2$ |
| 10 | Seg $E_3$ | 23 | Seg $C_6$ | 36 | Seg $F_4$ | 49 | Seg $G_2$ |
| 11 | Seg $D_3$ | 24 | Seg $G_6$ | 37 | Seg $G_4$ | 50 | Seg $B_1$ |
| 12 | Seg $C_3$ | 25 | Backplane | 38 | Seg $B_3$ | | |
| 13 | Seg $E_4$ | 26 | Seg $B_6$ | 39 | Seg $A_3$ | | |

**Model 5052 Men's Biplexed 3½ Digit Watch Display**
Outside Dimensions .410 (10,41) x .862 (21,89)
Digit Height .186 (4,72)




**Notes:**
1). Dimensions in parentheses are in millimeters.
2). Tolerance unless specified: xxx = ± .005 (0.13).

**PIN SCHEDULE**

| | A | B | | A | A |
|---|---|---|---|---|---|
| 1 | Backplane | Seg $E_1$ | 9 | Seg $A_2$ | Seg $B_2$ |
| 2 | Half Digit | Seg $D_1$ | 10 | —OFF— | Seg $E_3$ |
| 3 | Seg $F_1$ | Seg $C_1$ | 11 | Seg $F_3$ | Seg $D_3$ |
| 4 | Seg $G_1$ | Seg $B_1$ | 12 | Seg $G_3$ | Seg $C_3$ |
| 5 | Seg $A_1$ | Seg $E_2$ | 13 | Seg $A_3$ | Seg $B_3$ |
| 6 | Colon | Seg $D_2$ | 14 | Month-Date | —OFF— |
| 7 | Seg $F_2$ | Seg $C_2$ | 15 | | Backplane |
| 8 | Seg $G_2$ | | | | |

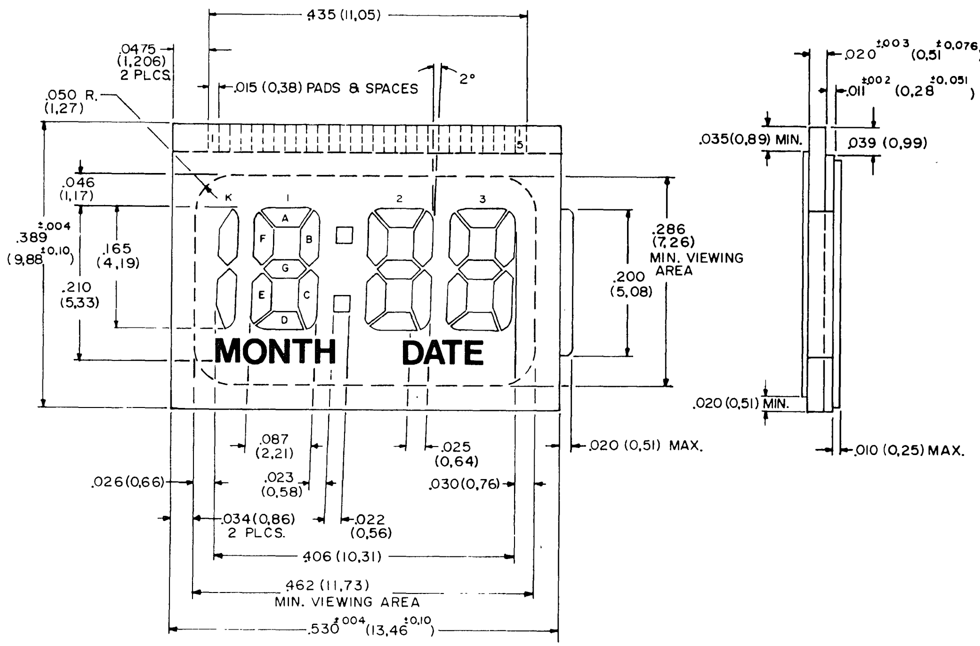
## commodore semiconductor group

## LCD

**Model 5053 Ladies Biplexed 3½ Digit Display**

Outside Dimensions .530 (13,46) x .389 (9,88)

Digit Height .165 (4,19)




**NOTE**

Dimensions in parentheses are in millimeters.

Tolerance unless specified: XXX = ±.005 (0,13).

**PIN SCHEDULE**

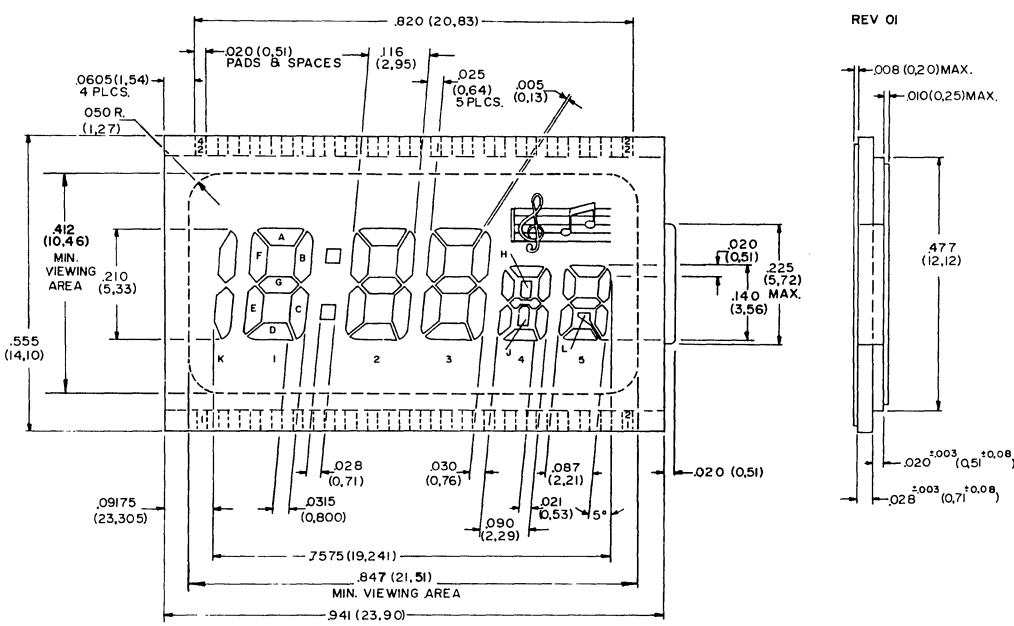
| | A | B | | A | B |
|---|---|---|---|---|---|
| 1 | Backplane | | 9 | Seg $A_2$ | Seg $B_2$ |
| 2 | Half Digit | Seg $E_1$ | 10 | –OFF– | Seg $E_3$ |
| 3 | Seg $F_1$ | Seg $D_1$ | 11 | Seg $F_3$ | Seg $D_3$ |
| 4 | Seg $G_1$ | Seg $C_1$ | 12 | Seg $G_3$ | Seg $C_3$ |
| 5 | Seg $A_1$ | Seg $B_1$ | 13 | Seg $A_3$ | Seg $B_3$ |
| 6 | Colon | Seg $E_2$ | 14 | Month-Date | –OFF– |
| 7 | Seg $F_2$ | Seg $D_2$ | 15 | | Backplane |
| 8 | Seg $G_2$ | Seg $C_2$ | | | |

**Model 5056 Men's 5½ Digit Watch Display with Melody**

Outside Dimensions .555 (14,10) x .941 (23,90)

Digit Height .210 (5,33)

.140 (3,56)



**NOTES**

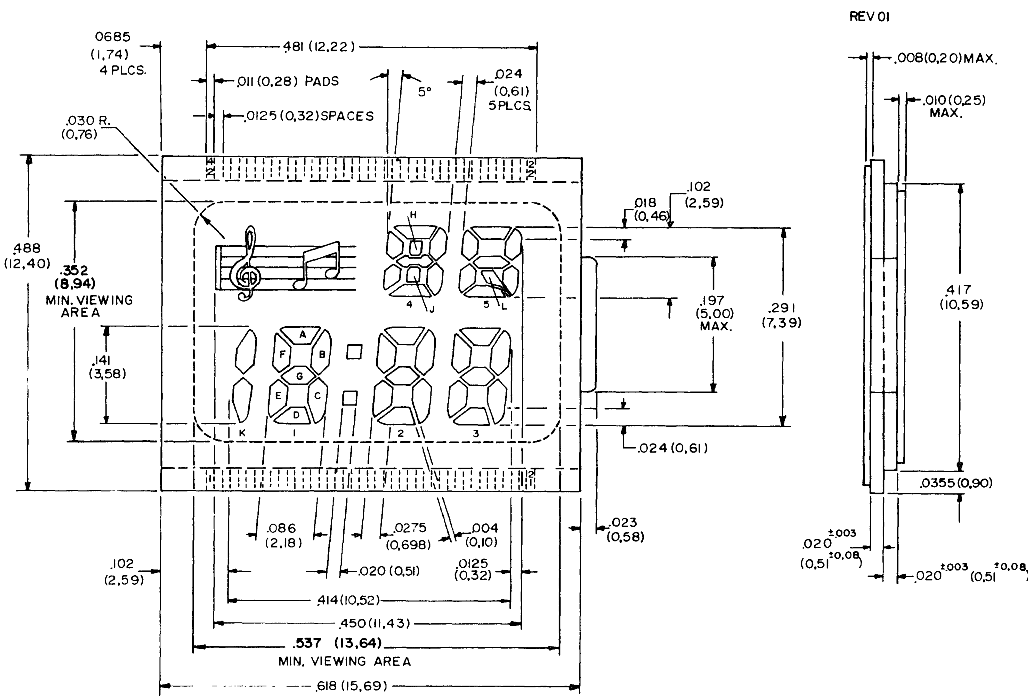
1. Dimensions in parentheses are in millimeters.
2. Tolerance unless specified: XXX = ± .005 (0,13).
3. Treble clef and scale are permanently printed on display.

**PIN SCHEDULE**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Half Digit | 12 | Seg $E_4$ | 23 | Seg $B_5$ | 34 | Seg $G_3$ |
| 2 | Seg $E_1$ | 13 | Seg $J_4$ | 24 | Seg $A_5$ | 35 | Seg $B_2$ |
| 3 | Seg $D_1$ | 14 | Seg $D_4$ | 25 | Seg $F_5$ | 36 | Seg $A_2$ |
| 4 | Seg $C_1$ | 15 | Seg $C_4$ | 26 | Seg $B_4$ | 37 | Seg $F_2$ |
| 5 | Colon | 16 | Seg $E_5$ | 27 | Seg $A_4$ | 38 | Seg $G_2$ |
| 6 | Seg $E_2$ | 17 | Seg $D_5$ | 28 | Seg $H_4$ | 39 | Seg $B_1$ |
| 7 | Seg $D_2$ | 18 | Seg $L_5$ | 29 | Seg $F_4$ | 40 | Seg $A_1$ |
| 8 | Seg $C_2$ | 19 | Seg $C_5$ | 30 | Seg $G_4$ | 41 | Seg $F_1$ |
| 9 | Seg $E_3$ | 20 | Seg $G_5$ | 31 | Seg $B_3$ | 42 | Seg $G_1$ |
| 10 | Seg $D_3$ | 21 | Backplane | 32 | Seg $A_3$ | | |
| 11 | Seg $C_3$ | 22 | Melody | 33 | Seg $F_3$ | | |

**Model 5059 Ladies 5½ Digit Multipurpose Watch Display With Melody Flag.**

Outside Dimensions .488 (12,40 ) x .618 (15,69)
Digit Height .141 (3,58)
.102 (2,59)



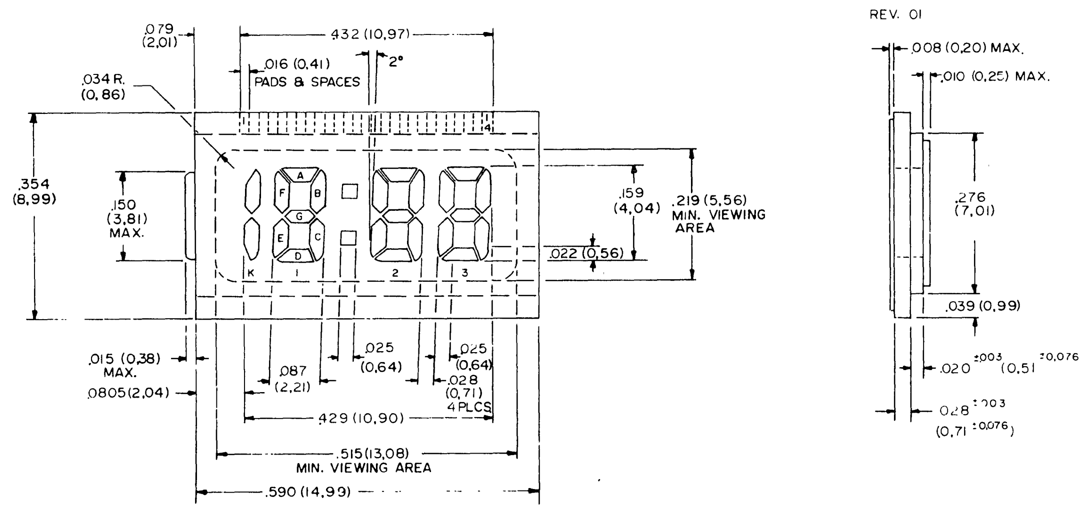

**NOTES**

1. Dimensions in parentheses are in millimeters.
2. Tolerances unless specified: XXX = ±.004 (0,10).
3. Treble clef and scale are permanently printed on display.

## PIN SCHEDULE

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Seg K | 12 | Seg $E_4$ | 23 | Seg $A_5$ | 34 | Seg $B_2$ |
| 2 | Seg $E_1$ | 13 | Seg $J_4$ | 24 | Seg $F_5$ | 35 | Seg $A_2$ |
| 3 | Seg $D_1$ | 14 | Seg $D_4$ | 25 | Seg $B_4$ | 36 | Seg $F_2$ |
| 4 | Seg $C_1$ | 15 | Seg $C_4$ | 26 | Seg $A_4$ | 37 | Seg $G_2$ |
| 5 | Colon | 16 | Seg $E_5$ | 27 | Seg $H_4$ | 38 | Melody |
| 6 | Seg $E_2$ | 17 | Seg $D_5$ | 28 | Seg $F_4$ | 39 | Seg $B_1$ |
| 7 | Seg $D_2$ | 18 | Seg $L_5$ | 29 | Seg $G_4$ | 40 | Seg $A_1$ |
| 8 | Seg $C_2$ | 19 | Seg $C_5$ | 30 | Seg $B_3$ | 41 | Seg $F_1$ |
| 9 | Seg $E_3$ | 20 | Seg $G_5$ | 31 | Seg $A_3$ | 42 | Seg $G_1$ |
| 10 | Seg $D_3$ | 21 | Backplane | 32 | Seg $F_3$ | | |
| 11 | Seg $C_3$ | 22 | Seg $B_5$ | 33 | Seg $G_3$ | | |

**Model 5060 Ladies Biplexed 3½ Digit Display**
Outside Dimensions .354 (8,99) x .590 (14,99)
Digit Height .159 (4,04)




**NOTES**
1. Dimensions in parentheses are in millimeters.
2. Tolerance unless specified: XXX = ±.005 (0,13).

**PIN SCHEDULE**

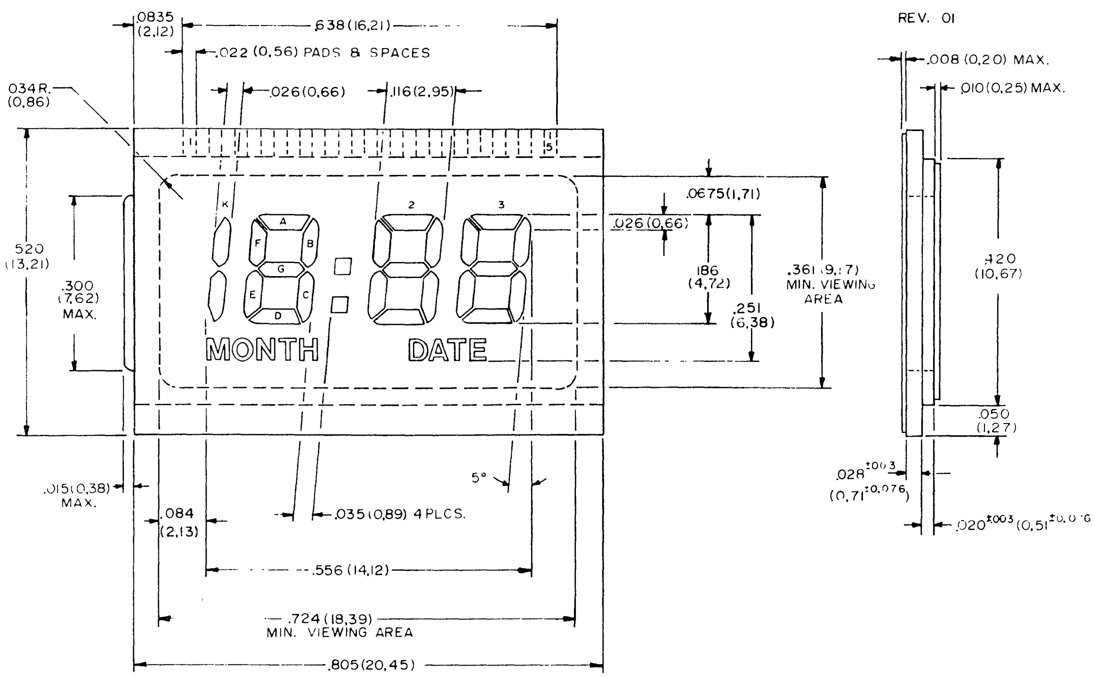
| | A | B |
|---|---|---|
| 1 | Backplane | |
| 2 | Half Digit | Seg $E_1$ |
| 3 | Seg $F_1$ | Seg $D_1$ |
| 4 | Seg $G_1$ | Seg $C_1$ |
| 5 | Seg $A_1$ | Seg $B_1$ |
| 6 | Colon | Seg $E_2$ |
| 7 | Seg $F_2$ | Seg $D_2$ |
| 8 | Seg $G_2$ | Seg $C_2$ |

| | A | B |
|---|---|---|
| 9 | Seg $A_2$ | Seg $B_2$ |
| 10 | –OFF– | Seg $E_3$ |
| 11 | Seg $F_3$ | Seg $D_3$ |
| 12 | Seg $G_3$ | Seg $C_3$ |
| 13 | Seg $A_3$ | Seg $B_3$ |
| 14 | | Backplane |

# commodore semiconductor group

## LCD

**Model 5061 Men's Biplexed 3½ Digit Watch Display**
Outside Dimensions .520 (13,21) x .805 (20,45)
Digit Height .186 (4,72)



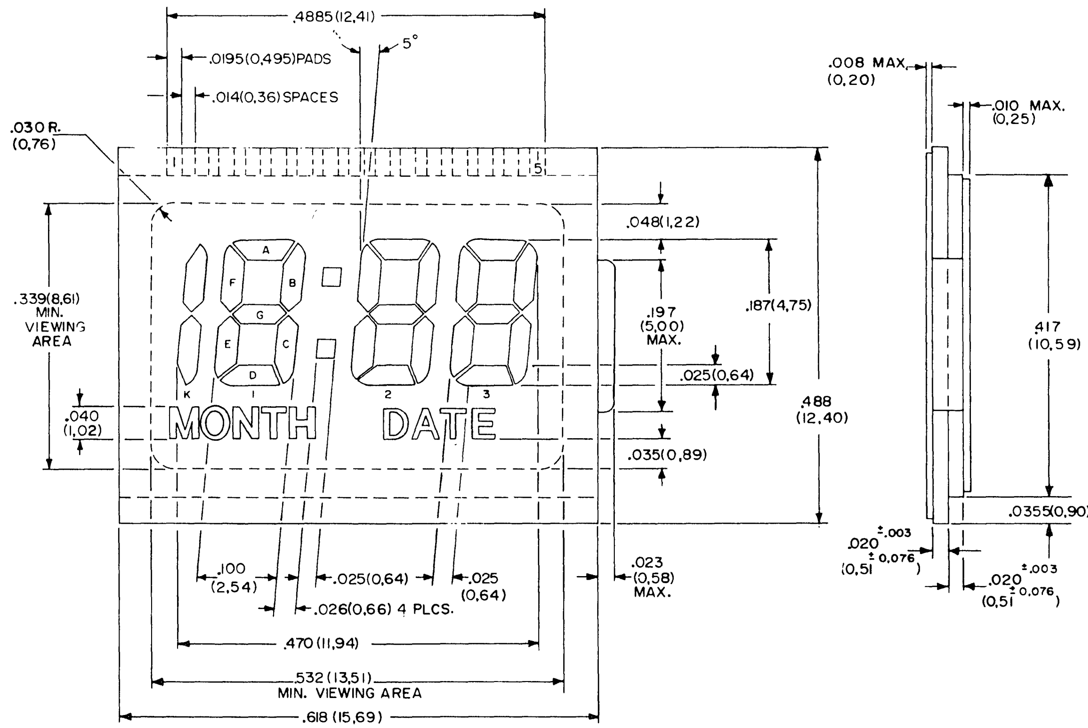

**PIN SCHEDULE**

| | A | B | | A | B |
|---|---|---|---|---|---|
| 1 | Backplane | | 9 | Seg $A_2$ | Seg $B_2$ |
| 2 | Half Digit | Seg $E_1$ | 10 | – OFF – | Seg $E_3$ |
| 3 | Seg $F_1$ | Seg $D_1$ | 11 | Seg $F_3$ | Seg $D_3$ |
| 4 | Seg $G_1$ | Seg $C_1$ | 12 | Seg $G_3$ | Seg $C_3$ |
| 5 | Seg $A_1$ | Seg $B_1$ | 13 | Seg $A_3$ | Seg $B_3$ |
| 6 | Colon | Seg $E_2$ | 14 | Month-Date | – OFF – |
| 7 | Seg $F_2$ | Seg $D_2$ | 15 | | Backplane |
| 8 | Seg $G_2$ | Seg $C_2$ | | | |

**Model 5063 Ladies Biplexed 3½ Large Digit Watch Display**

Outside Dimensions .488 (12,40) x .618 (15,69)

Digit Height .187 (4,75)




**Notes:**

1). Dimensions in parentheses are in millimeters.

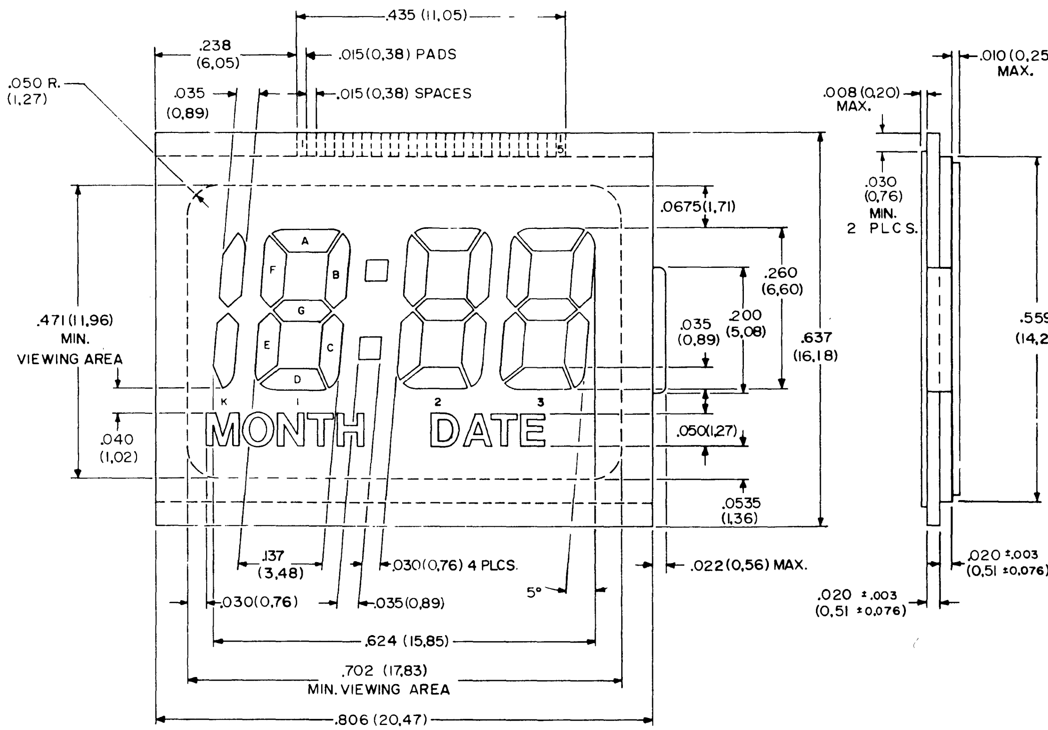
2). Tolerances unless specified: xxx = ± .004 (0.10).

**PIN SCHEDULE**

| | A | B | | A | B |
|---|---|---|---|---|---|
| 1 | Backplane | | 9 | Seg $A_2$ | Seg $B_2$ |
| 2 | Half Digit | Seg $E_1$ | 10 | —OFF— | Seg $E_3$ |
| 3 | Seg $F_1$ | Seg $D_1$ | 11 | Seg $F_3$ | Seg $D_3$ |
| 4 | Seg $G_1$ | Seg $C_1$ | 12 | Seg $G_3$ | Seg $C_3$ |
| 5 | Seg $A_1$ | Seg $B_1$ | 13 | Seg $A_3$ | Seg $B_3$ |
| 6 | Colon | Seg $E_2$ | 14 | Month-Date | —OFF— |
| 7 | Seg $F_2$ | Seg $D_2$ | 15 | | Backplane |
| 8 | Seg $G_2$ | Seg $C_2$ | | | |

**Model 5064 Men's Biplexed 3½ Large Digit Watch Display**

Outside Dimensions .806 (20,47) x .637 (16,18)
Digit Height .260 (6,60)



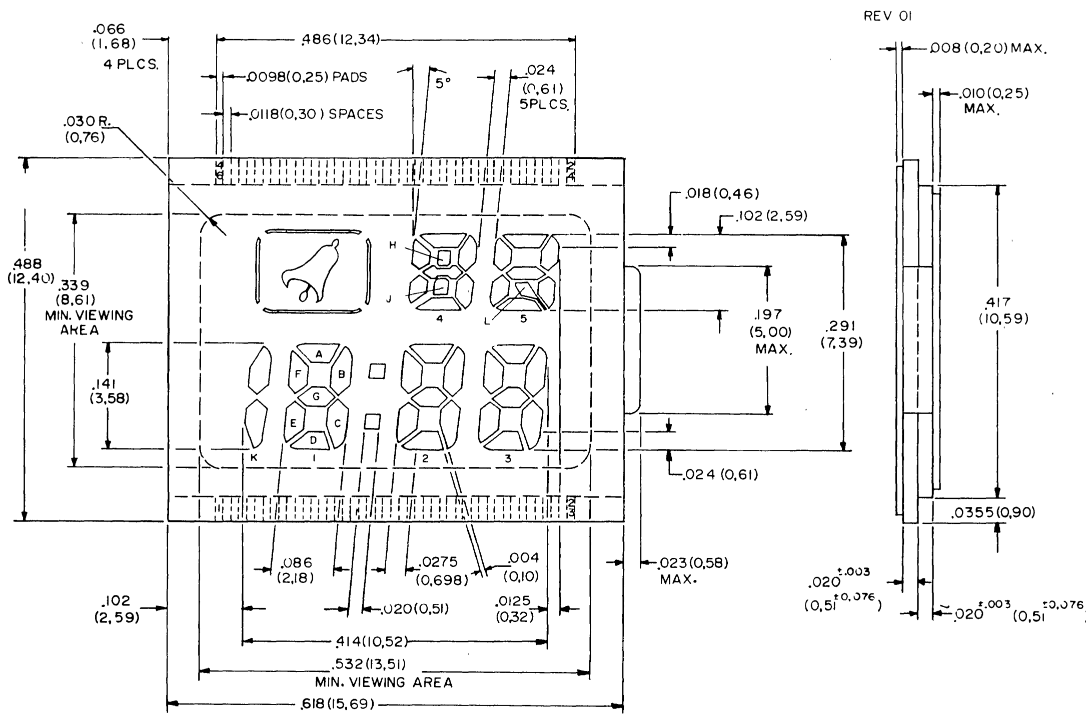

**Notes:**
1). Dimensions in parentheses are in millimeters.
2). Tolerances unless specified: xxx = ± .005 (0,13).

**PIN SCHEDULE**

| | A | B | | A | B |
|---|---|---|---|---|---|
| 1 | Backplane | | 9 | | Seg $B_2$ |
| 2 | Half Digit | Seg $E_1$ | 10 | Seg $A_2$ | Seg $E_3$ |
| 3 | Seg $F_1$ | Seg $D_1$ | 11 | —OFF— | Seg $D_3$ |
| 4 | Seg $D_1$ | Seg $C_1$ | 12 | Seg $F_3$ | Seg $C_3$ |
| 5 | Seg $A_1$ | Seg $B_1$ | 13 | Seg $G_3$ | Seg $B_3$ |
| 6 | Colon | Seg $E_2$ | 14 | Seg $A_3$ | —OFF— |
| 7 | Seg $F_2$ | Seg $D_2$ | 15 | Month-Date | Backplane |
| 8 | Seg $G_2$ | Seg $C_2$ | | | |

**Model 5065 Ladies 5½ Digit Watch Display With Alarm Flag**

Outside Dimensions .488 (12,40) x .618 (15,69)
Digit Height .141 (3,58)
.102 (2,59)




**Notes:**
1). Dimensions in parentheses are in millimeters.
2). Tolerances unless specified xxx = ± .004 (0.10).
3). Alarm is permanently printed on display.

**PIN SCHEDULE**

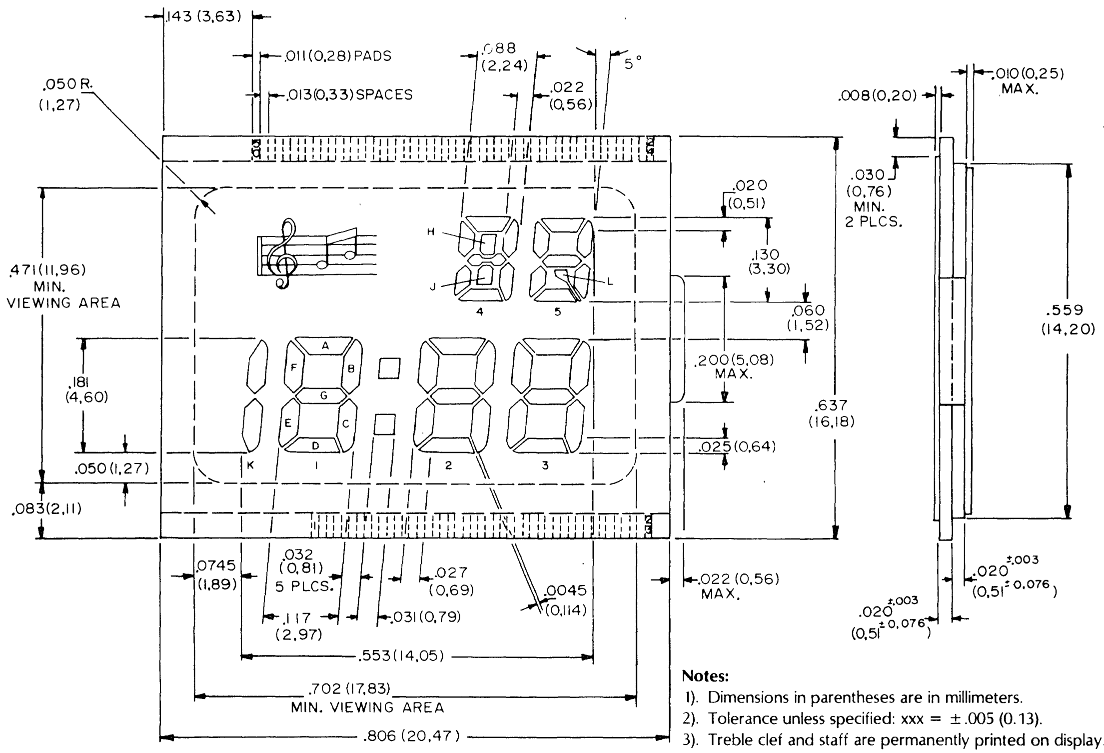
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | BLANK | 13 | Seg $C_3$ | 25 | Seg $A_5$ | 37 | Seg $A_2$ |
| 2 | BLANK | 14 | Seg $E_4$ | 26 | Seg $F_5$ | 38 | Seg $F_2$ |
| 3 | Seg K | 15 | Seg $J_4$ | 27 | Seg $B_4$ | 39 | Seg $G_2$ |
| 4 | Seg $E_1$ | 16 | Seg $D_4$ | 28 | Seg $A_4$ | 40 | ALARM |
| 5 | Seg $D_1$ | 17 | Seg $C_4$ | 29 | Seg $H_4$ | 41 | Seg $B_1$ |
| 6 | Seg $C_1$ | 18 | Seg $E_5$ | 30 | Seg $F_4$ | 42 | Seg $A_1$ |
| 7 | COLON | 19 | Seg $D_5$ | 31 | Seg $G_4$ | 43 | Seg $F_1$ |
| 8 | Seg $E_2$ | 20 | Seg $L_5$ | 32 | Seg $B_3$ | 44 | Seg $G_1$ |
| 9 | Seg $D_2$ | 21 | Seg $C_5$ | 33 | Seg $A_3$ | 45 | BLANK |
| 10 | Seg $C_2$ | 22 | Seg $G_5$ | 34 | Seg $F_3$ | 46 | BLANK |
| 11 | Seg $E_3$ | 23 | BACKPLANE | 35 | Seg $G_3$ | | |
| 12 | Seg $D_3$ | 24 | Seg $B_5$ | 36 | Seg $B_2$ | | |

# commodore semiconductor group

## LCD

**Model 5066 Men's 5½ Digit Watch Display With Melody Flag**

Outside Dimensions .637 (16,18) x .806 (20,47)
Digit Height .181 (4,60)
.130 (3,30)

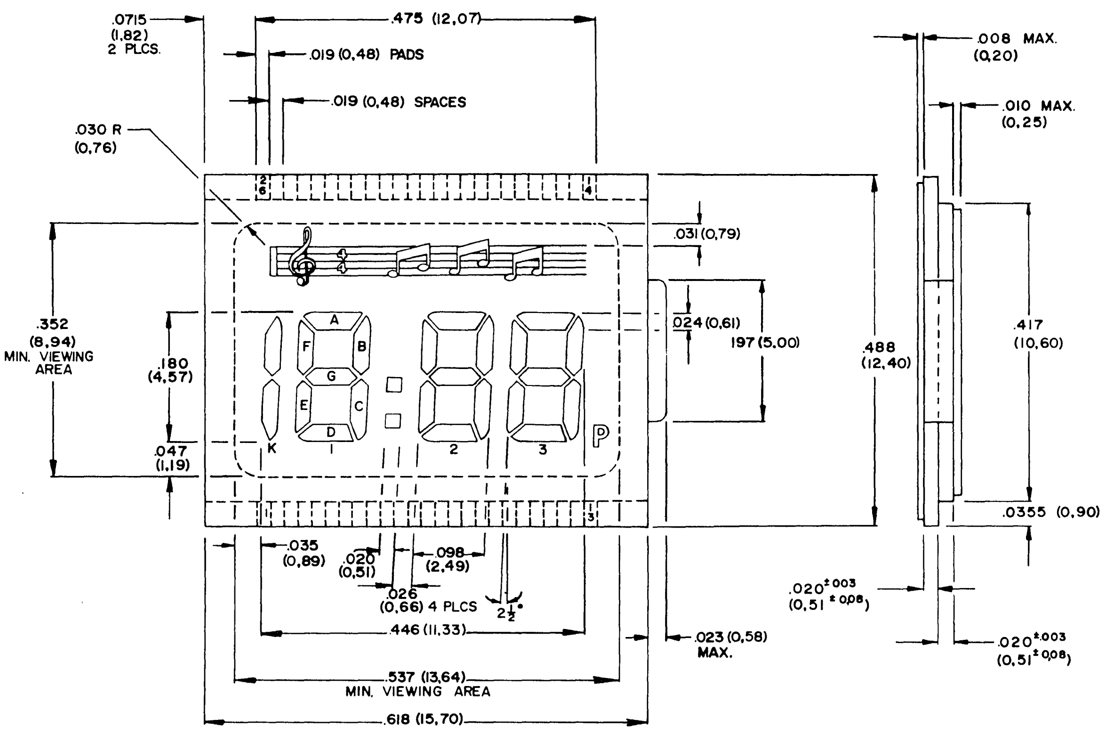



**Notes:**
1). Dimensions in parentheses are in millimeters.
2). Tolerance unless specified: xxx = ±.005 (0.13).
3). Treble clef and staff are permanently printed on display.

**PIN SCHEDULE**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | BLANK | 14 | Seg $E_4$ | 27 | Seg $B_4$ | 40 | MELODY |
| 2 | BLANK | 15 | Seg $J_4$ | 28 | Seg $A_4$ | 41 | BLANK |
| 3 | Seg K | 16 | Seg $D_4$ | 29 | Seg $H_4$ | 42 | BLANK |
| 4 | Seg $E_1$ | 17 | Seg $C_4$ | 30 | Seg $F_4$ | 43 | BLANK |
| 5 | Seg $D_1$ | 18 | Seg $E_5$ | 31 | Seg $G_4$ | 44 | Seg $B_1$ |
| 6 | Seg $C_1$ | 19 | Seg $D_5$ | 32 | Seg $B_3$ | 45 | Seg $A_1$ |
| 7 | Seg COLON | 20 | Seg $L_5$ | 33 | Seg $A_3$ | 46 | Seg $F_1$ |
| 8 | Seg $E_2$ | 21 | Seg $C_5$ | 34 | Seg $F_3$ | 47 | Seg $G_1$ |
| 9 | Seg $A_2$, $D_2$ | 22 | Seg $G_5$ | 35 | Seg $G_3$ | 48 | BLANK |
| 10 | Seg $C_3$ | 23 | BACKPLANE | 36 | Seg $B_2$ | 49 | BLANK |
| 11 | Seg $E_3$ | 24 | Seg $B_5$ | 37 | BLANK | 50 | BLANK |
| 12 | Seg $D_3$ | 25 | Seg $A_5$ | 38 | Seg $F_2$ | | |
| 13 | Seg $C_3$ | 26 | Seg $F_5$ | 39 | Seg $G_2$ | | |

**Model 5067 Ladies' 3½ Digit Direct Drive Watch Display With Melody Alarm and PM Flags**
Outside Dimensions .488 (12,40) x .618 (15,70)
Digit Height .180 (4,57)




**Notes**
1). Dimensions in parentheses are in millimeters.
2). Tolerances unless specified: xxx = ± .004 (0.10).
3). Treble clef and staff are permanently printed on display.

**PIN SCHEDULE**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | Backplane | 8 | Seg $D_2$ | 15 | Seg $B_3$ | 22 | Seg $G_2$ |
| 2 | Half Digit | 9 | Seg $C_2$ | 16 | Seg $A_3$ | 23 | Seg $B_1$ |
| 3 | Seg $E_1$ | 10 | Seg $E_3$ | 17 | Seg $F_3$ | 24 | Seg $A_1$ |
| 4 | Seg $D_1$ | 11 | Seg $D_3$ | 18 | Seg $G_3$ | 25 | Seg $F_1$ |
| 5 | Seg $C_1$ | 12 | Seg $C_3$ | 19 | Seg $B_2$ | 26 | Seg $G_1$ |
| 6 | Colon | 13 | PM | 20 | Seg $A_2$ | | |
| 7 | Seg $E_2$ | 14 | Melody | 21 | Seg $F_2$ | | |

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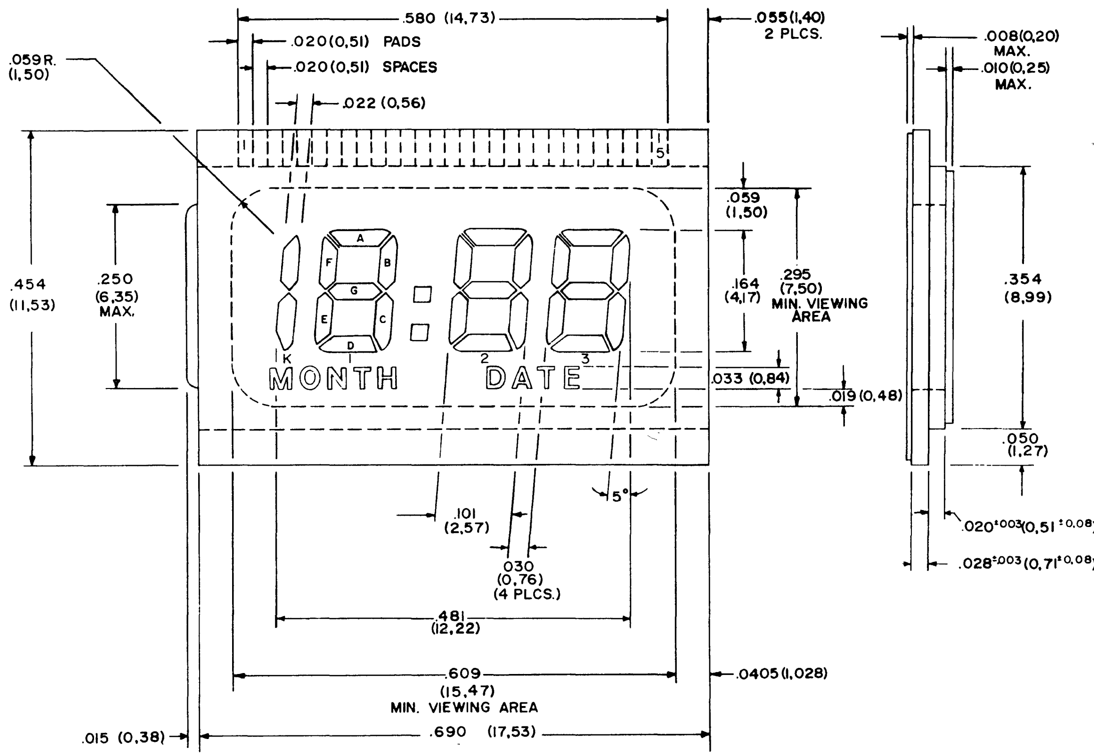
**LCD**

**Model 5076 Unisex 3½ Digit Biplexed Watch Display**
Outside Dimensions .454 (11,53) x .690 (17,53)
Digit Height .164 (4,17)

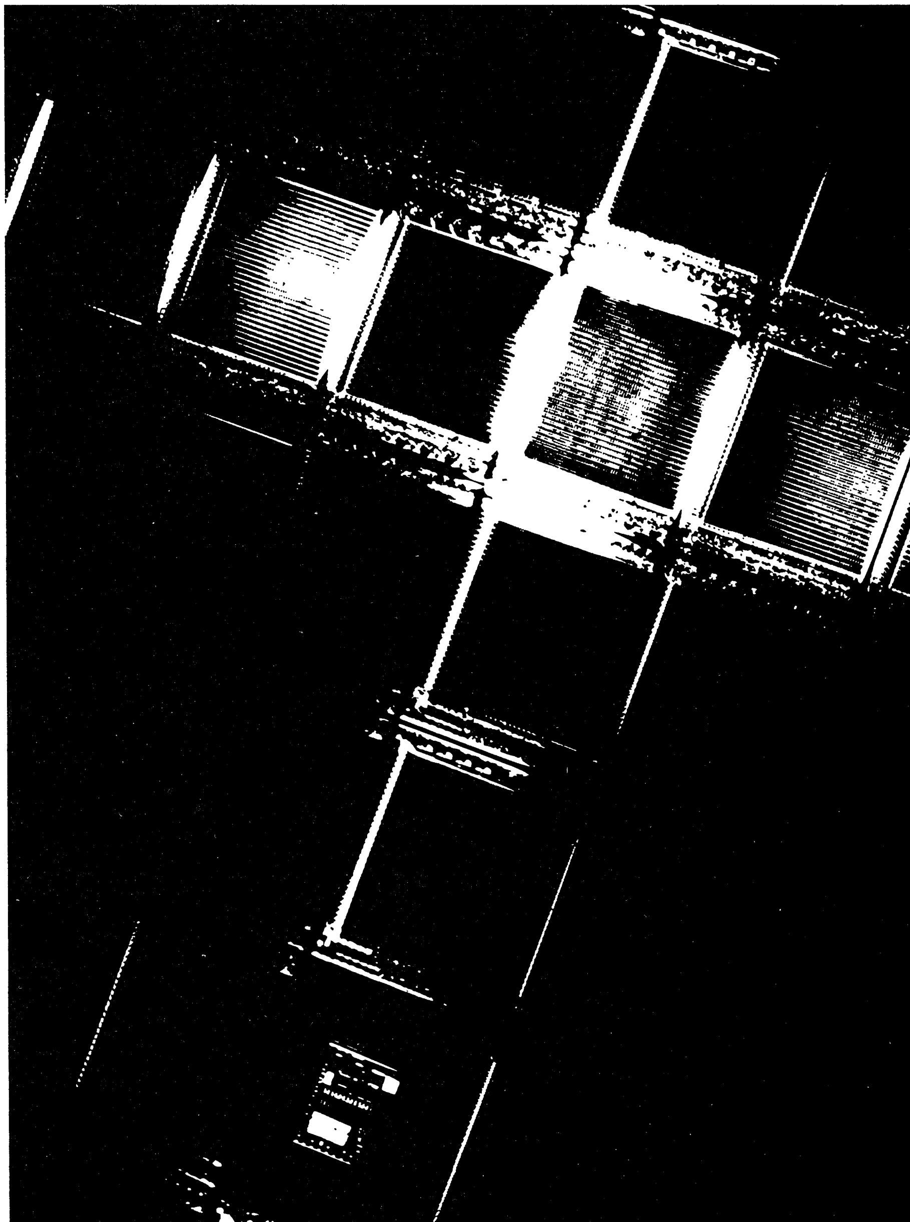



**Notes:**
1). Dimensions in parentheses are in millimeters.
2). Tolerance unless specified: xxx = ±.005 (0.13)

**PIN SCHEDULE**

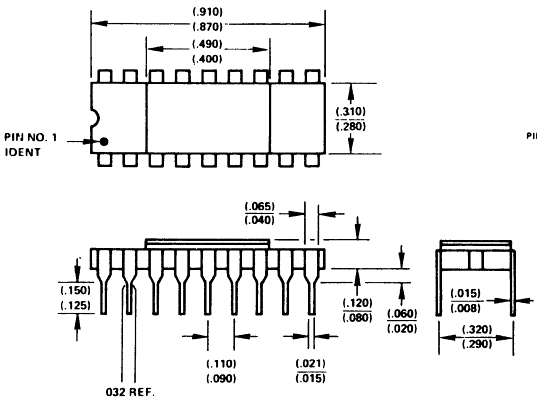
| | A | B | | A | B |
|---|---|---|---|---|---|
| 1 | Backplane | Seg $E_1$ | 9 | Seq $A_2$ | Seg $B_2$ |
| 2 | Half Digit | Seg $D_1$ | 10 | —OFF— | Seg $E_3$ |
| 3 | Seg $F_1$ | Seg $C_1$ | 11 | Seg $F_3$ | Seg $D_3$ |
| 4 | Seg $G_1$ | Seg $B_1$ | 12 | Seg $G_3$ | Seg $C_3$ |
| 5 | Seg $A_1$ | Seg $E_2$ | 13 | Seg $A_3$ | Seg $B_3$ |
| 6 | Colon | Seg $D_2$ | 14 | Month-Date | —OFF— |
| 7 | Seg $F_2$ | Seg $C_2$ | 15 | | Backplane |
| 8 | Seg $G_2$ | | | | |

# Section 5
# Packaging and Reliability Information

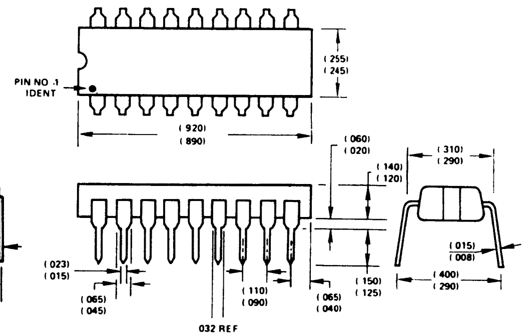


## 18-PIN PACKAGE

### Ceramic

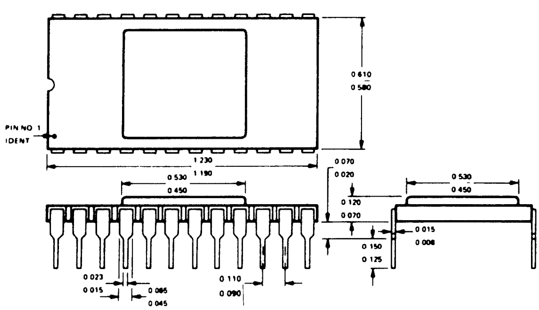



### Molded

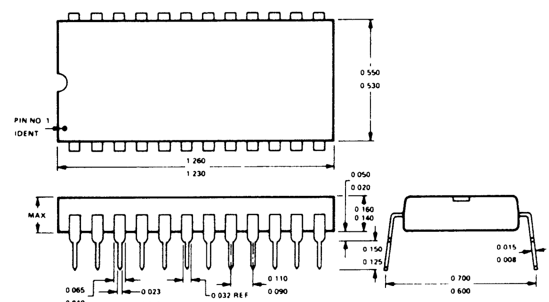



## 24-PIN PACKAGE

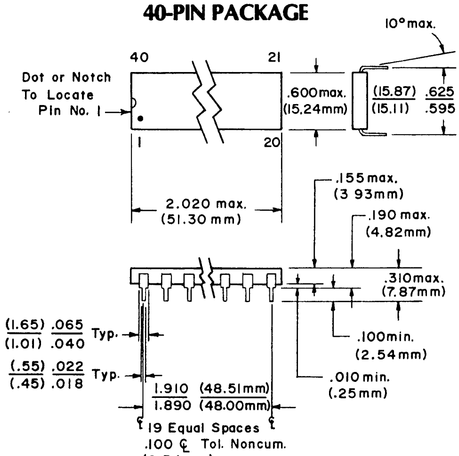
### Ceramic




### Molded




## 40-PIN PACKAGE



Device reliability is a function of design, of wafer processing and of packaging. MOS Technology products are characterized electrically and physically for an in-house qualification. Device reliability is verified by long-term, accelerated life testing. Life testing and characterization are then continuously checked in an ongoing monitor of reliability.

## ENVIRONMENTAL TESTING

No formal universal set of qualification standards exists for plastic encapsulated devices designed for non-military applications. However, modeled after the Military Standard 883, a series of environmental and general reliability tests were established to evaluate device reliability prior to new product introduction. These tests were as follows:

| TEST | MIL STD. 883 METHOD BASIS |
|---|---|
| Thermal Shock | 1011.1 |
| Immersion (Salt Solution) | 1002 |
| Moisture Resistance | 1004.1 |
| Steam High Pressure | 1004.1 |
| Centrifuge | 2001.1 |
| Burn-in and Long Term Life | 1015.1 |

### Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature.

### Procedure

This evaluation consisted of 1) preconditioning the sample for $>$5 minutes immersed in a liquid at $-55°C$; 2) transferring the sample rapidly ($<$10 seconds) to a second liquid at $+100°C$ and allowing stabilization for $>$5 minutes; 3) transfer of the sample back to the original container. The cycle was repeated 15 times.

Sample Size: 200 pieces, multiple lots, chosen at random.
Evaluation: Electrical Test
Results: 0 Failures

### Immersion

This test is performed to determine the effectiveness of the seal on microelectronic devices.

### Procedure

This evaluation consisted of: 1) 24-hour soak in salt solution at room temperature; 2) rinse in tap water; 3) bake dry.

Sample Size: 100 Parts
Evaluation: Electrical Test
Results: 0 Failures

### Moisture Resistance

The moisture resistance test is performed for the purpose of evaluating in an accelerated manner the resistance of component parts and constituent materials to the deteriorative effects of high humidity and heat conditions.

### Procedure

This evaluation consisted of two tests:

(a) The sample was subjected to 4 hours at 150°C 15 PSI saturated water vapor in a pressure chamber.

Sample Size: 100 Parts
Evaluation: Electrical Test
Results: 0 Failures

(b) The sample was subjected to 85°C 95% R.H. for 24 hours.

Sample Size: 100 Parts
Evaluation: Electrical Test
Results: 0 Failures

### Constant Acceleration

This test is used to determine the effects of constant acceleration on microelectronic devices. It is an accelerated test designed to indicate types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests.

### Procedure

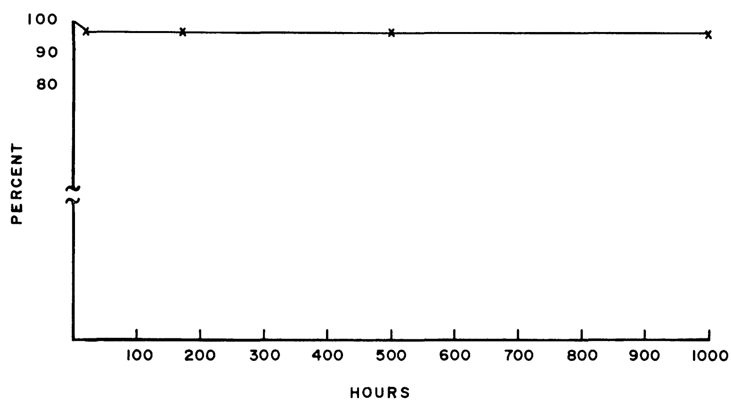
Parts were subjected to one-minute centrifuge at 30,000 G in $Y_1$ orientation.

Sample Size: 100 Parts
Evaluation: Electrical Test
Results: 1 Failure, open contact $A_0$ address lead due to open bond.

## LONG TERM LIFE

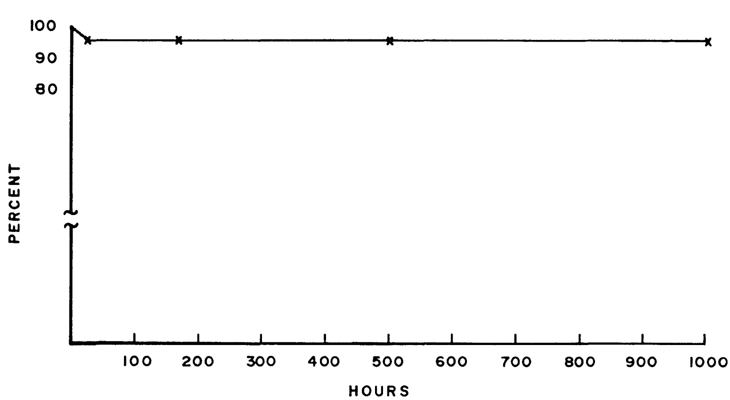
Elevated temperature is used to accelerate failure mechanisms such as mobile contamination, slow trapping and oxide pin holes. Burn-in ovens capable of continuously exercising devices are used to stress product at high voltage and temperature. Long term life testing is a continuous and ongoing procedure in order to detect any subtle reliability changes. Millions of device hours have been accumulated. The data presented in Figure 10 are typical 1000 hour performance characteristics at 125°C., 5.5v. Extrapolating to a 70°C operating ambient, the N-channel process demonstrates a reliability of .056%/1000 hours.

**LONG TERM RELIABILITY**




**ROM LONG TERM LIFE PERFORMANCE**

**SAMPLE N173-01 - N201-13**
**100 PIECES/SAMPLE**
**125°C**




**RAM LONG TERM LIFE PERFORMANCE**

**SAMPLE N166-02 - N171-01**
**100 PEICES/SAMPLE**
**125°C**

**Figure 10**

## MANUFACTURING PROCEDURES

The manufacturing process used at MOS Technology follows strictly documented procedures to ensure consistency in performance and reliability. Figure 11 is the product flow at the "back end" of the process. All production lots are burned-in and a constant monitor is made of losses. A high drop out at burn-in is an indication of a potential problem which can be immediately addressed. Any part shipped is traceable to burn-in, final test and fabrication yields. Quality assurance monitors prior to shipment verify electrical performance and mechanical standards.

**POST ASSEMBLY PRODUCTION FLOW**

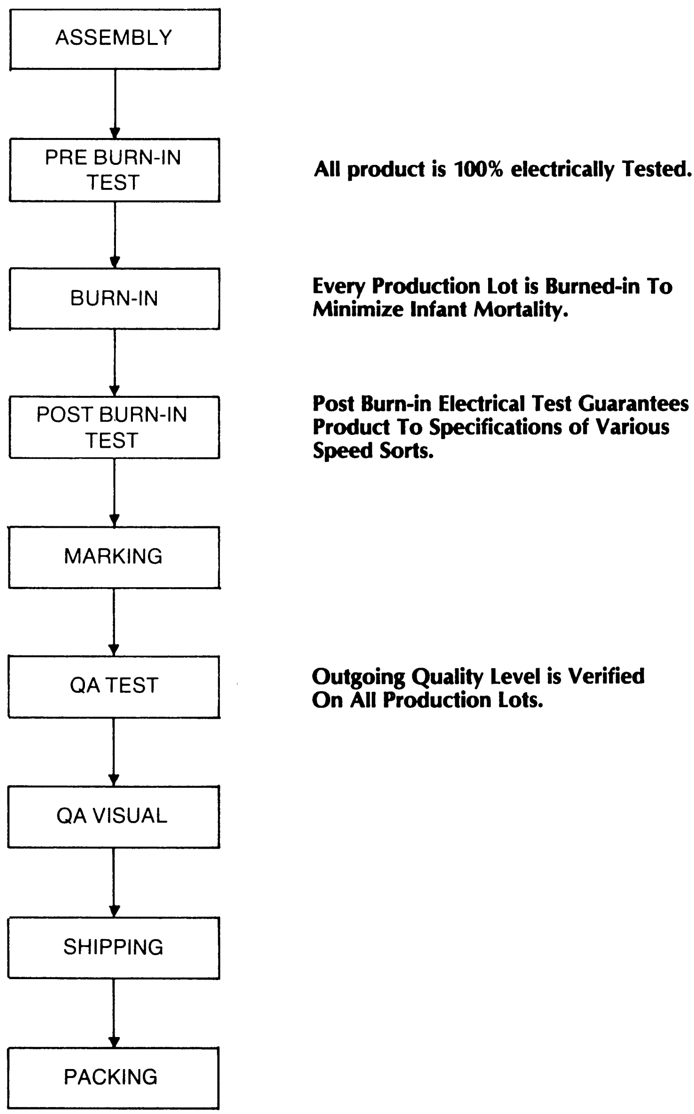



**Figure 11**

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