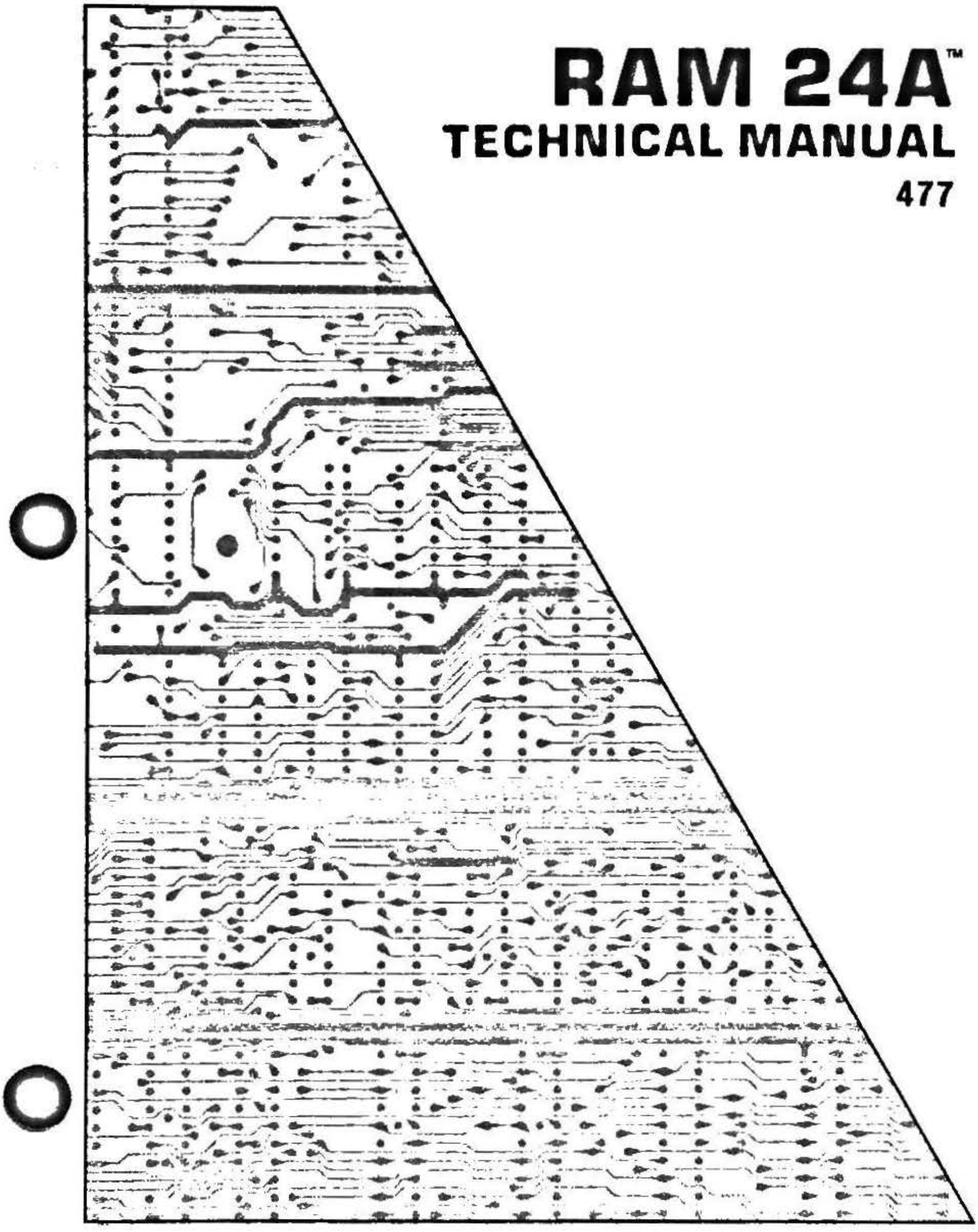
CompuPro™

RAM 24A™
TECHNICAL MANUAL
477



8261-0477

April 1988

RAM 24A
Technical Manual
High Speed Static Memory
for the IEEE 696 Bus

RAM 24A Technical Manual 477
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Contents

Preface

This manual describes the features and functions of the RAM 24A board. This is a reference manual for hardware engineers, programmers and anyone else who needs to understand how the RAM 24A functions in a CompuPro computer system. It is neither a troubleshooting guide nor a repair manual.

This manual begins with an overall description of the board and a detailed account of the jumper settings. Specifications and schematics are also included.

Overall Description

CompuPro's RAM 24A board is a high speed CMOS Static RAM board for S-100 Computers. The RAM 24A uses 32 high performance 32K by 8-bit CMOS RAM chips to provide a total of 1 Mb or 512K words of storage. The board works in "word wide" mode in 16-bit applications, as well as in "byte wide" mode in 8-bit applications. Supported by CompuPro's Concurrent DOS 8-16™ multi-user, multi-tasking operating systems, the RAM 24A is designed to work with our 12 MHz, two-cycle CPU 286™.

In addition, the RAM 24A has jumper selectable windows that can be blocked out for use in systems with SPIO, SP186 and/or SPUZ boards that overlap the RAM 24A memory space, thus eliminating the use of the S-100 PHANTOM* signal.

(continued)

Note: The RAM 24A was designed to run with the 12 MHz, two-cycle CPU 286™ and may not work with older processors. S100 pins 3 and 21 are grounded on the RAM 24A. Pin 3 is XRDY and pin 21 is an NDEF pin, previously used by CompuPro as Φdisable. Pins 3 and 21 are inputs on the CPU 8085/88™, CPU 8086™. Pin 3 is an input on DISK 3™ boards earlier than Rev. J. On the CPU 68K™, pin 21 is a jumperable input (J11) and pin 3 is used only on boards earlier than Rev. H.

To modify these boards for use with the RAM 24A, disconnect pins 3 and 21 from the IC inputs to which they go (or remove jumpers) and pull the disconnected inputs on the IC's on the board up to +5V. (This is not required if a jumper is present.)

See the specific board technical manual for location of IC's and jumpers.

Installing the RAM 24A

STATIC WARNING: Please observe these precautions:

- Store only in anti-static materials. Do not use non-conductive styrofoam or plastic trays or bags.
- Observe proper static discharge techniques when handling boards.
- Keep fabric and other static-generating materials away from boards and circuits.
- Turn off power when inserting or removing boards. Leave all power supplies off for several minutes to be certain no voltage is present.

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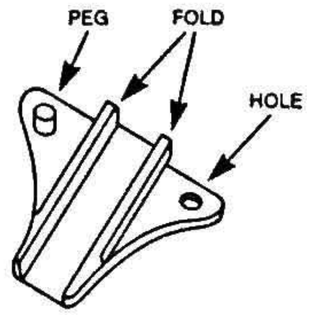
Basic Installation

Step 1. Unpack the RAM 24A Board.

Along with the board, you will find two card extractors in the anti-static plastic bag.



CARD EXTRACTOR

Step 2. Install Card Extractors.

1. Hold the board with the component side toward you.
2. Insert the peg on the card extractor into the hole in the right corner of the board. Fold the extractor over the board's edge until the extractor's hole snaps over the peg.

   NOTE: Make sure the long edge of the extractor is along the top edge of the board.
3. Repeat for the left extractor.

Step 3. Check Jumper Settings

For standard jumper settings for use with a CompuPro operating system, check your *Operating System Installation and Customization Guide Concurrent DOS 8-16*. Jumpers are described in detail under the **Jumper Summary** section.

(continued)

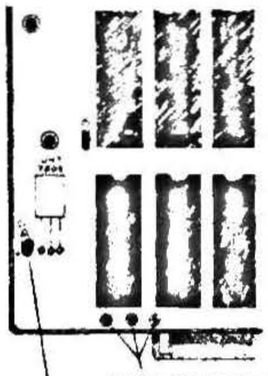
Installing the RAM 24A

Step 4. Insert the RAM 24A into the bus.

The power to the system must be off. Place the board into a slot near the CPU. The edge connector is offset, so the RAM 24A will fit only one way. **Push down GENTLY until the board is firmly installed.**

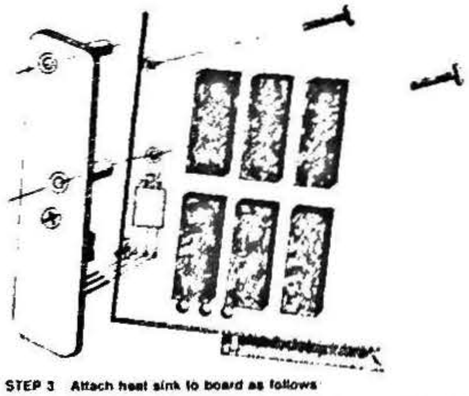
Caution: The RAM 24A without regulators is designed for use in systems with regulated power supplies (boards with 5V stickers). Do not attempt to adapt the board for use in systems with unregulated power supplies. Do not install a 5-volt regulator (7805) face up in U47. U47 requires an optional heat sink/regulator adapter, available from CompuPro (part number 1455-0049).

To install this adapter, use this illustration as a guide:



STEP 1 Drill out 3 holes with 141 (9/64) inch carbide drill

STEP 2 Solder 1.5 micro-farad capacitor in C1



STEP 3 Attach heat sink to board as follows

a) bend and solder regulator leads to supplied holes in board

b) insert anchor screws from solder side of board

Jumper Summary

JUMPERS J1 - J4 - Memory Address Select

Jumpers J1 - J4 are used to select the memory address bits A20-23. The address is set in a binary fashion with each jumper position representing an address bit. J1 represents A23, J2 represents A20, J3 represents A22 and J4 represents A21. A jumper connected to ground (B-C) represents a "zero" and a jumper connected to +5 Volts (A-C) represents a "one." These jumpers are connected via traces (B-C) on the board to ground selecting the lowest allowable 1 Mb boundary for memory (the starting address of the memory is 000000h and the ending address is 0FFFFF). To address the board at any other boundary, these traces must be cut and jumper wires connected between A and C.

For example, to set the memory to start at 400000h, cut the trace on J3 (B-C) and install a jumper wire from A-C on J3.

NOTE: The following jumpers (J5-J7) are used to disable areas of the RAM 24A memory space. These jumper selectable "windows" are used in systems with SPIO, SPUZ and/or SP186 boards that overlap the RAM 24A memory space, thus eliminating the need for the S-100 PHANTOM* signal. In CompuPro standard configurations, the SPIO memory space (4 Kbytes per SPIO) is set at the top of pages 0Dh, 0Eh or 0Fh. The SP186 memory space is all of 0Fh and the SPUZ memory space is all of 0Eh. The RAM 24A windows appear in these pages only. If the SPIO, SP186 and SPUZ are used at other memory locations, it is recommended that they be used without underlying system memory.

JUMPER J5 - SPIO Window Select

Jumper J5 is used to block out sections of the RAM 24A memory so it doesn't overlap the SPIO memory space. This jumper has positions A through L and is located in the lower center of the board. Positions A through E are set according to the number of SPIOs in the system and positions F through L are set according to the system configuration in which the RAM 24A will reside. A detailed discussion of positions A through E and F through L follows. **Note:** This position does not have an I jumper.

JUMPER J5

J5: Positions A through E: SPIO Window Size Select

Each SPIO employs a 4K block of memory space and standard CompuPro software supports up to two SPIOs. Positions A thru E of this jumper allow a 4 or 8K window (or no window) to be blocked out of the RAM 24A memory. For a system with a RAM 24A and without a SPIO (so no 4 or 8K window needs to be blocked out), place a shunt from C to D. If there is one SPIO in the system (and, therefore, a 4K window must be blocked out), shunt A-B and D-E. If there are two SPIOs in the system (8K block needed), shunt B-C and D-E. The following table summarizes these options.

Number of SPIOs in System	Shunt
0	C-D
1	A-B and D-E
2	B-C and D-E

J5 Positions F through L: SPIO Window Location Select

Positions F through L of Jumper 5 select in which page of memory (0Dh, 0Eh or 0Fh) the 4 or 8K window will appear. The location of the window depends on the system configuration. For instance, if there are SP186 boards in the system, they occupy page 0Fh (the full 64K) of the memory space. When an SP186 is present, (and without a SPUZ present) the SPIO resides in the upper 4K (upper 8K if two SPIOs) of page 0Eh. (See also J6.) In this configuration, the SPIO window must appear in page 0Eh. A description of the possible configurations and the appropriate jumper setting follows.

SPIO without a SPUZ or an SP186

In systems with a SPIO and without an SP186 or a SPUZ, the SPIO resides in the upper 4K (or 8K) of 0Fh. Therefore, the SPIO window must be set in page 0Fh. To do this, shunt G-H and J-K.

SPIO with 1-15 SPUZs and without an SP186

In systems with SPIO and SPUZ(s) but without an SP186, the SPIO resides in page 0Fh and the SPUZ in 0Eh. Therefore, the SPIO window must be set in page 0Fh. To do this, shunt G-H and J-K.

SPIO with 1-15 SP186s but without a SPUZ

In systems with SPIO and SP186(s) and without a SPUZ, the SPIO window must appear in page 0Eh since the SP186s reside in page 0Fh. To do this, shunt G-H and K-L.

SPIO with both SPUZ and SP186

In systems with SPIO and both SP186 and SPUZ boards, the SPIO window must appear in page 0Dh. To do this shunt F-G and J-K.

Jumper Summary

To summarize:

System Configuration:	SPIO Page:	Jumper:
SPIO/SP186/SPUZ	0Dh	F-G, J-K
SPIO/SP186	0Eh	G-H, K-L
SPIO alone or SPIO/SPUZ	0Fh	G-H, J-K

JUMPER J6: SP186 Window Select

Jumper J6 must have a shunt to window out the RAM space for the SP186(s). The SP186's memory space is in page 0Fh (the whole 64K). In systems with 1 to 15 SP186s, place a shunt in this jumper so the RAM24A and the SP186(s) will not have overlapping memory.

JUMPER J7: SPUZ Window Select

Jumper J7 must have a shunt in it to window out the RAM space for the SPUZs. The SPUZ's memory space is in page 0Eh (the whole 64K). In systems with 1 to 15 SPUZs, place a shunt in this jumper so the RAM24A and the SPUZ(s) will not have overlapping memory.

System Configuration Jumper Summary:

# of SPIOs	# of SP186s	# of SPUZs	J5	J6	J7
0	0	0	C-D	no shunt	no shunt
0	1-15	0	C-D	shunt	no shunt
1	0	0	A-B D-E G-H J-K	no shunt	no shunt
1	1-15	0	A-B D-E G-H K-L	shunt	no shunt
2	0	0	B-C D-E G-H J-K	no shunt	no shunt
2	1-15	0	B-C D-E G-H K-L	shunt	no shunt
0	0	1-15	C-D	no shunt	shunt
0	1-15	1-15	C-D	shunt	shunt
1	0	1-15	A-B D-E G-H J-K	no shunt	shunt

(continued)

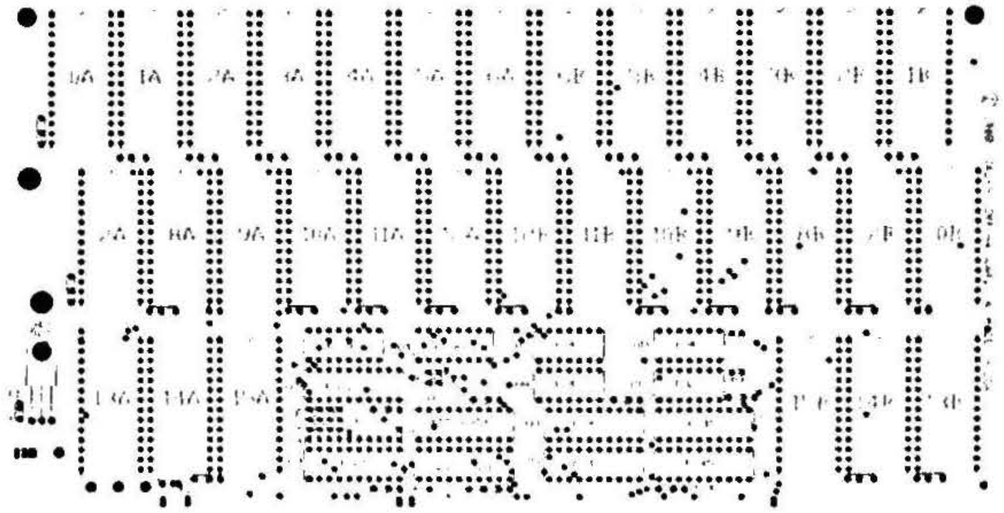
System Configuration Jumper Summary – continued

# of SPIOs	# of SP186s	# of SPUZs	J5	J6	J7
1	1-15	1-15	A-B D-E F-G J-K	shunt	shunt
2	0	1-15	B-C D-E G-H J-K	no shunt	shunt
2	1-15	1-15	B-C D-E F-G J-K	shunt	shunt

Locating RAM ICs by Address and Byte

The Component Layout below may be used as a map to locate specific RAM ICs by address and byte array. The following table lists the address within the board and what RAM chip corresponds to that address.

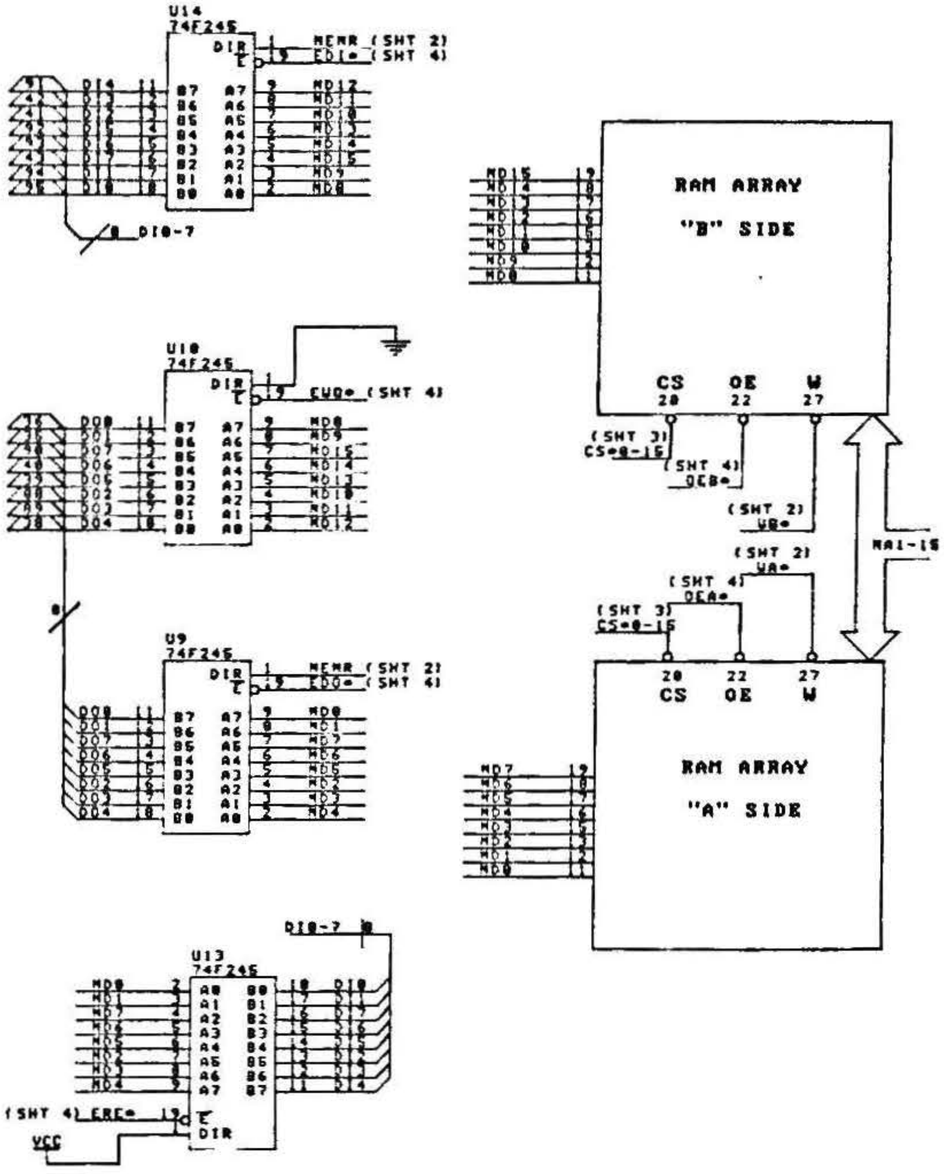
ADDRESS	EVEN BYTE	ODD BYTE
00000h-0FFFFh	0A	0B
10000h-1FFFFh	1A	1B
20000h-2FFFFh	2A	2B
30000h-3FFFFh	3A	3B
40000h-4FFFFh	4A	4B
50000h-5FFFFh	5A	5B
60000h-6FFFFh	6A	6B
70000h-7FFFFh	7A	7B
80000h-8FFFFh	8A	8B
90000h-9FFFFh	9A	9B
A0000h-AFFFFh	10A	10B
B0000h-BFFFFh	11A	11B
C0000h-CFFFFh	12A	12B
D0000h-DFFFFh	13A	13B
E0000h-EFFFFh	14A	14B
F0000h-FFFFFh	15A	15B

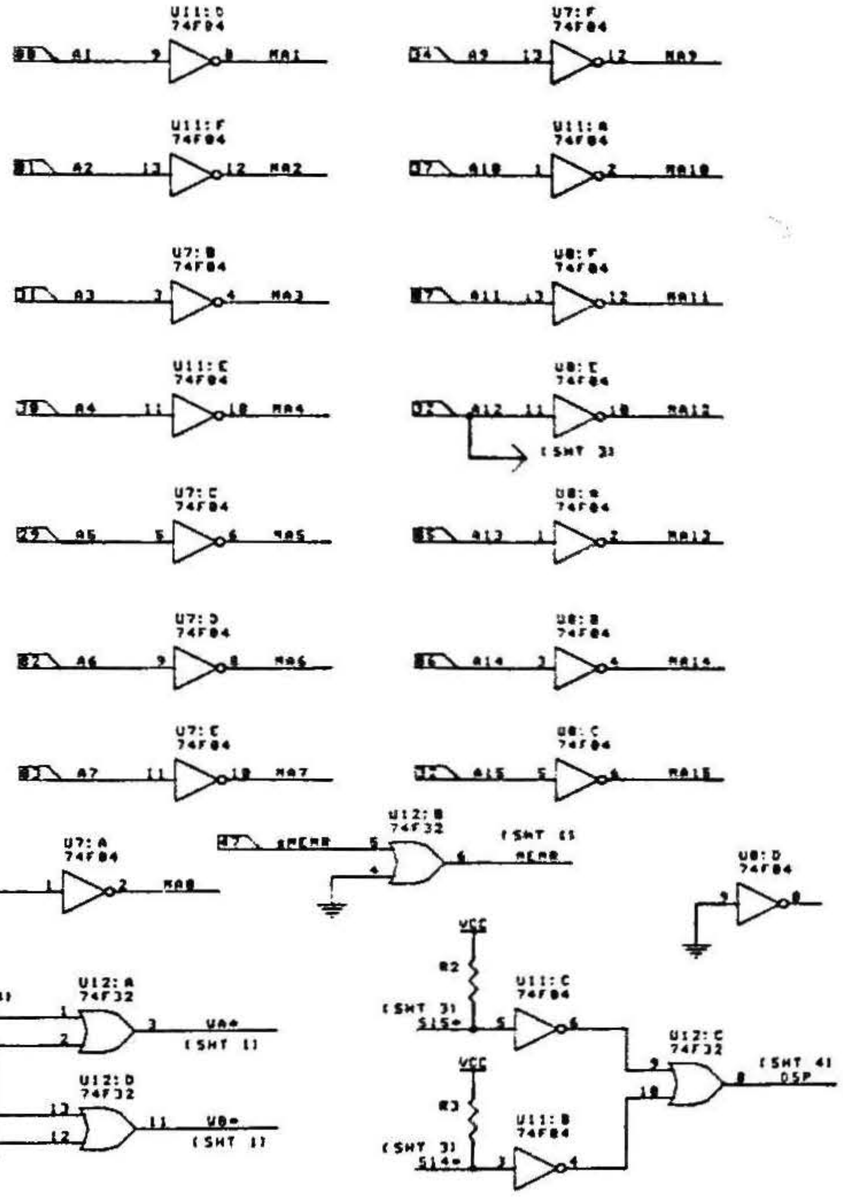


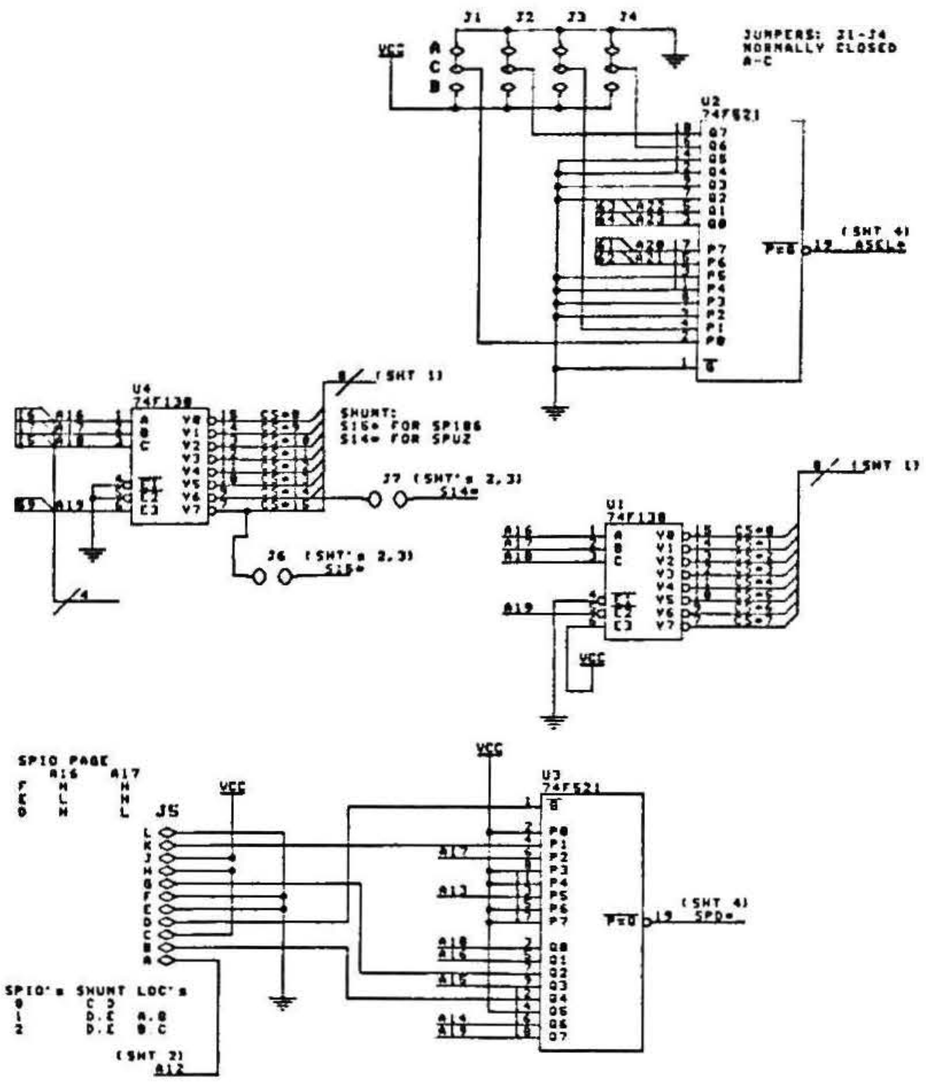
Specifications

Size:	
Length	253 mm (10 in)
Depth	13 mm (0.5 in)
Height	127 mm (5 in)
Weight:	308 g (10.8 oz.)
Timing:	Meets IEEE 696 timing including systems beyond 6 MHz. Meets requirements for two-cycle operation up to 12 MHz with CompuPro CPU 286.
Memory:	1 Mb (32, 32K by 8 Static RAM).
S-100 Address Space:	Factory set at lowest 1 Mb boundary. May be set in the field to any other 1 Mb boundary over the 16 Mb range.
Power Consumption:	758 mA typical at 5V 875 mA maximum.

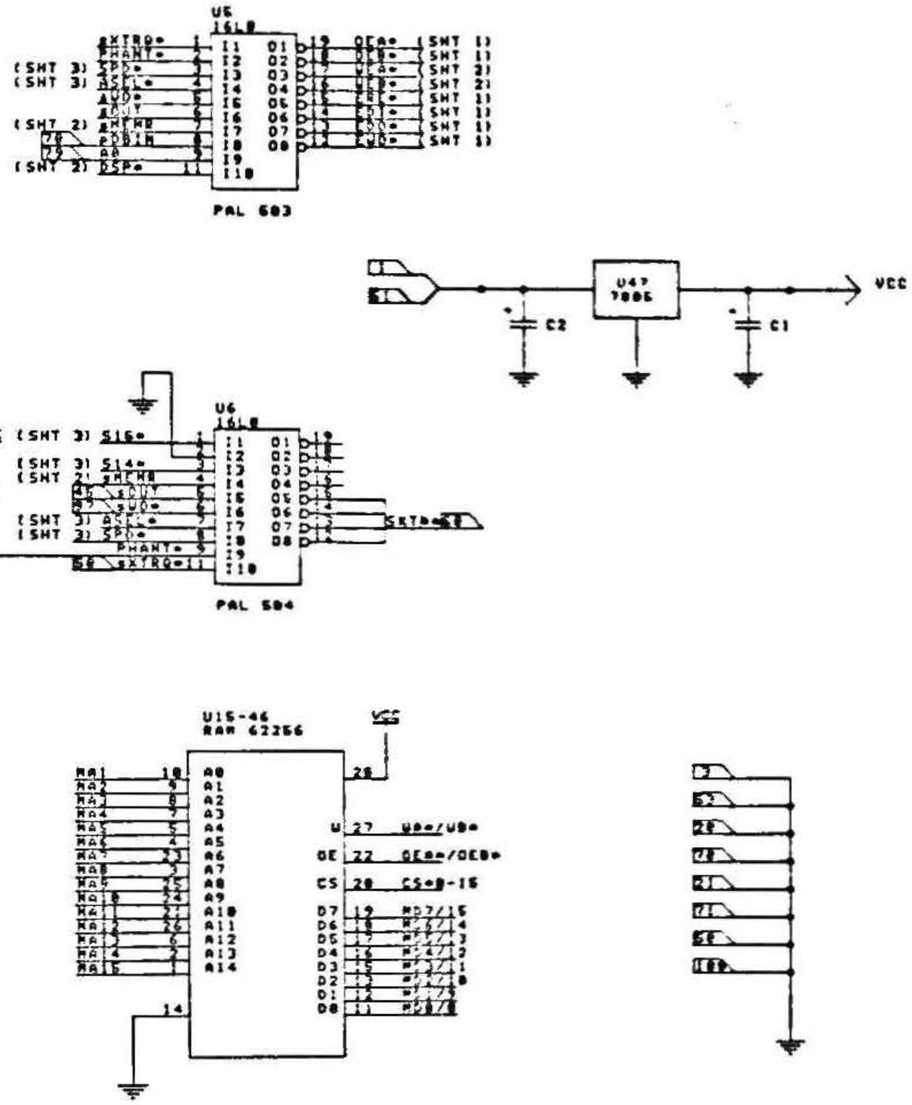
Schematics




U11:D
74F04
U7:F
74F04
U11:F
74F04
U11:A
74F04
U7:B
74F04
U8:F
74F04
U11:E
74F04
U8:E
74F04
U7:C
74F04
U8:A
74F04
U7:D
74F04
U8:B
74F04
U7:E
74F04
U8:C
74F04
U7:A
74F04
U12:B
74F32
U8:D
74F04
U12:A
74F32
U12:D
74F32
U11:C
74F04
U11:B
74F04
U12:C
74F32
VCC


J1 J2 J3 J4
JUMPERS: J1-J4
NORMALLY CLOSED
A-C
U2
74F621
U4
74F138
SHUNT:
S16* FOR SP1B6
S14* FOR SPU2
U1
74F138
U3
74F521
SPIO PAGE
SPIO'S SHUNT LOC'S
J5
VCC

Schematics


U6
16L8
PAL 503
U47
7805
VCC
C2
C1
U6
16L8
PAL 504
U15-46
RAM 62256
VCC

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