DTI-UM-2760-2

PRICE: $25.00

USER MANUAL FOR DATA TRANSLATION, INC. DEC DUAL HEIGHT ANALOG INPUT SYSTEMS

DT2762 DT2765

DT2764 DT2765-T

DATA TRANSLATION

4A STRATHMORE ROAD
NATICK, MASSACHUSETTS 01701.

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CHAPTER 1

PRODUCT DESCRIPTION

DT2762 - High level Analog input system with 16 single-ended or 8 differential input channels on a standard DEC dual height card.

DT2772 - High level input expander - Expands the DT2762 to 64 single ended or 32 differential inputs: Packaged on a standard DEC dual height card.

DT2764 - Wide range analog input systems with 16 single ended or 8 differential input channels as a standard DEC dual input card. Ranges are resistor selectable from 10mV FSR to 10V FSR.

DT2774 - Wide range input expander - Expands the DT2764 to 64 single ended or 32 differential input. Packaged on a standard DEC dual height card.

DT2765 - Isolated Wide Range analog inputs system containing 4 channels of isolated analog inputs with dry reed relay flying capacitor multiplexing. Packaged on a standard DEC dual height card.

DT2775 - Isolated input expander - Expands the DT2765 to 20 channels of analog inputs in groups of eight channels. Packaged on a standard DEC dual height card.

1.1 Options

1.1.1 DT2762 - optional features are as follows:

PG - programmable gain amplifier, gain controlled via software with gains of 1, 2, 4 and 8.

C - 100Khz data acquisition module provides 100Khz analog acquisition and concession throughput.

1.1.2 DT2764 R - resistor gain selection bit provides resistor for setting gains of 100, 200, 10, 2, 1.

1.1.3 DT2765

PG - Programmable gain amplifier, gains controlled via software with gains of 1, 10, 100 and 500.

T - Thermocouple input version, provides input for cold, reference junction compensation.

CHAPTER 2

DT2762 HIGH LEVEL INPUT SYSTEM SPECIFICATIONS

2.1 Analog Inputs

The DT2762 utilizes the DT5701 data acquisition module. This module will accept up to 16 single ended inputs or 8 differential inputs with 12 bit resolution. Expansion channels may be added by the addition of the DT2772 expander module for up to 64 single ended or 32 differential inputs.

2.2 Number of Analog Inputs

DT2762	- 8 channels Differential input (DI) -16 channels Single Ended inputs (SE)
DT2762 with DT2772	-32 channels Differential (DI) -64 channels Single Ended (SE)

2.2.1 Selection of SE/DI

Selection of SE or DI must be specified by the user and cannot be changed except by the factory.

2.3 Input Range

0-5V, ±5V, 0-10V, ±10V twos compliment, or offset binary notation.

2.4 Input Protection

Inputs are current limited and protected to ±35V overvoltage without damage.

2.5 Input Impedence

100 MOHM, 10pF - "OFF" Channels
100 MOHM, 100pF - "ON" Channels

2.6 Input Bias Current

15nA @ 25^{o}C

2.7 Maximum Input Signal

±10.5V Signal & Common Mode Voltage

2.8 Common Mode Rejection Ratio

80db @ 5V range
100db @ 10mV range

2.9 A/D Specifications

2.9.1 Resolution

12-bits Unipolar
11-bits + Sign Bipolar

2.9.2 Linearity

±½ LSB

2.9.3 Inherent Quantizing Error

±½ LSB

2.9.4 Stability

±25ppm/°C FSR

2.10 Sample and Hold Specification

2.10.1 Aperature Uncertainty

Less than 10nS

2.11 System Specifications

2.11.1 System Accuracy

±0.03% FSR

2.11.2 System Throughput

The throughput is defined as the time interval from a start A/D convert to an A/D Done bit set. It does not include overhead of program to retrieve data.

Throughput	=	35KHz	or	28.5 uSEC
	=	100KHz	or	10 uSEC optional

2.11.3 Input Noise

2uV RMS R.T.I.

2.12 Power Requirements

+5V @ 1.5A , 5%

2.13 System Compatibility

Standard DEC QBus compatible. DC Bus load = 1

2.14 Physical

Contained on a standard DEC dual height card for compatibility LSI-11, LSI-11/2 and LSI-11/23 systems.

CHAPTER 3

DT2764 WIDE RANGE INPUT SYSTEM SPECIFICATIONS

3.1 Analog Inputs

The DT2764 products utilize the Data Translation DT5702 12-bit data acquisition module. Expansion beyond 16 channels SE or 8 channels DI is accomplished with the DT2774 expander boards.

3.2 Number of Analog Inputs

DT2764 - 8 Channels DI, 16 Channels SE

DT2764 with DT2774 - Up to 32 Channels DI, 64 Channels SE

3.2.1 Analog Input Range

DT2764 - From 10mV to 10V Full Scale
From ±10mV to ±10V Full Scale

Ranger selectable via external resistor.

3.2.2 Analog Input Configuration

Analog inputs may be user selectable for Single Ended or Differential Input configuration. This selection is via jumpers on the board.

3.2.3 Input Protection

Inputs are current limited and protected to ±15V overvoltage without damage.

3.2.4 Input Impedence

100 MOHM, 10pF - "OFF" Channels
100 MOHM, 100pF - "ON" Channels

3.2.5 Input Bias Current

15nA @ 25°C

3.2.6 Maximum Input Signal

±10.5V Signal & Common Mode Voltage

3.2.7 Common Mode Rejection Ratio

80db @ 10V range
100db @ 10mV range

3.3 A/D Specifications

3.3.1 Resolution

12-bits Unipolar
11-bits + Sign Bipolar

3.3.2 Linearity

±½ LSB

3.3.3 Inherent Quantizing Error

±½ LSB

3.3.4 Stability

±25ppm/^{o}C FSR

3.4 Sample and Hold Specification

3.4.1 Aperture Uncertainty

10nSec

3.5 System Specification

3.5.1 System Accuracy

The system accuracy is dependent upon the gain of the system as follows:

GAIN	ACCURACY (BIPOLAR)	THROUGHPUT (KHz)
1	±0.03%	31
2	±0.03%	31
4	±0.03%	31
10	±0.03%	31
100	±0.05%	16.75
200	±0.07%	11.1
400	±0.08%	7.1
1000	±0.1%	3.7

(Table 3.5.1 Gain Parameters)

3.5.2 Throughput Rates

The system throughput is again dependent upon the gain of the system. Table 3.5.1 shows the throughput versus gain. This throughput is set via an external capacitor by the user.

3.5.3 Input Noise

2uV RMS

3.6 Power Requirements

3.6.1 DT2764 - +5V @ 1.5A, 5%

3.7 System Compatibility

Standard DEC Q-Bus compatible, DC Bus load =1.

3.8 Physical

Contained on a standard DEC dual height card for compatibility with LSI-11, LSI-11/2 and LSI-11/23 systems.

CHAPTER 4

DT2765 ISOLATED WIDE RANGE INPUT SYSTEM SPECIFICATIONS

4.0 General

The DT2765 series systems are Q-BUS compatible isolated wide range analog input systems. The input multiplexer is isolated via a flying capacitor technique utilizing dry reed relays. The system uses a DT5703 4 channel isolated data acquisition module. Expansion to 20 channels accomplished using the DT2775 expansion card.

4.1 Input Specification

4.1.1	Number of Analog Inputs		4 Differential, 12 channels with expander card.
4.1.2	Common mode voltage range		±250V DC max
4.1.3	Common mode rejection ratio		126db @ 60Hz with 1K unbalance
4.1.4	Input impedance	Power On Power Off	10 Megohms 100 Megohms
4.1.5	Zero offset channel to channel		±10uV
4.1.6	Input filter		1.5Hz
4.1.7	Throughput Rate	Random Mode	20 conversions per sec.
4.1.8	Differential Input Voltage		15V DC max, or 100V for 10mS max.

4.2 Amplifier

4.2.1	Offset voltage	Adjustable to Zero	
4.2.2	Offset voltage TC		±3uV/^{o}C
4.2.3	Gain TC		±10ppm/^{o}C
4.2.4	Gain Range	Gain of 1 to 1000 where, $G = 1 + \frac{20,000}{R_{ext.}}$	
4.2.5	Bias Current	@ 25^{o}C @ 70^{o}C	50pA 1.2nA
4.2.6	Input Noise	@ 15KHz BW	5uV rms

4.3 A/D Converter

4.3.1	Resolution		12 bits
4.3.2	Linearity		±½LSB
4.3.3	Quantizing Error		±½LSB
4.3.4	Range	Unipolar Bipolar	0 to +5V or 0 to 10V) ±5V ±10V)DT2725/15V
4.3.5	Temperature Coefficient	Zero Full Scale	±20uV/°C ±30ppm/°C

4.4 Power Requirements

4.4.1 DT2765 +5V @ 1.5A 5%

4.5 DT2765-T Thermocouple Input

4.5.1 Compensation Input Specification - DT2765-T

The DT2765-T version allows connection of a compensation circuit for providing thermocouple cold junction compensation.

4.5.2 Input Connection

The compensation inputs are connected at connector
J1 Pins 15 COMP IN HI
16 COMP IN LO

4.5.3 Input Impedence - 100 Ohms

4.5.4 Compensation Requirements

Type J	IRON/CONSTANTINE	50uV/°C
Type T	COPPER/CONSTANTINE	40uV/°C
Type K	Chromel/Alumel	40uV/°C

For application circuit see Appendix

4.6 System Compatibility - Standard DEC

Q-Bus compatible
DC Bus Load - 1

4.7 Physical

Standard DEC dual height card for compatibility with LSI-11, LSI-11/2 or LSI-11/23 systems.

CHAPTER 5

PROGRAMMING SPECIFICATIONS

Data Translation interfaces are designed to meet the requirements of standard DEC interfaces. As such they are structured around a Control and Status register for complete software control of the interface.

5.1 DT2762 and DT2764 Programming.

5.1.1 Modes of Operation.

This series can operate in a number of operating modes, as follows:

Program I/O - In this mode standard LSI-11 instructions can access and control the A/D components on the interface. A start A/D conversion can be accomplished by two ways:

1. Set A/D Start Bit (Bit Ø) ADCSR
2. External Triggers or Real Time Clock input.

Interrupt - In many real time applications the program does not want to dedicate itself to taking analog measurements. In this case the interface can be enabled to produce a program interrupt on the condition A/D Done. An interrupt may also be produced on the Error bit (Bit 15 ADCSR).

5.1.2 Device Address

The DT2762 device address is selectable via a dip switch. Device address may be assigned between 170000_8 and 177774_8. The order of address is as follows, once a base address has been set in the switch:

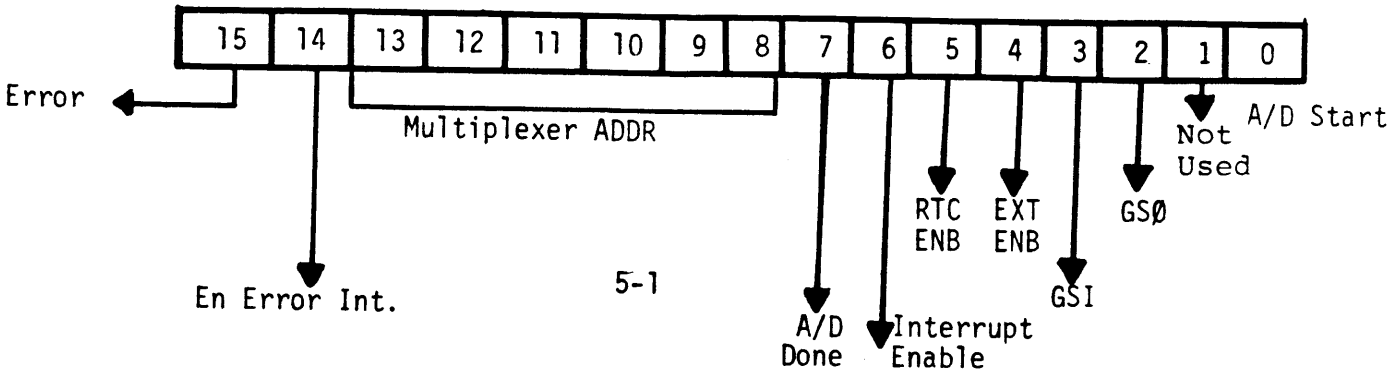
A/D Control and Status Register (ADCSR) - Base
A/D Data Buffer Register (ADDBR) - Base + 2 (Read Only)

5.1.3 Interrupt Vector Address

The vector address is set via a dip switch pack, they are selectable in increments of 10_8. There are two Interrupts A/D DONE, and ERROR. (See 5.1.4 CSR descriptions).

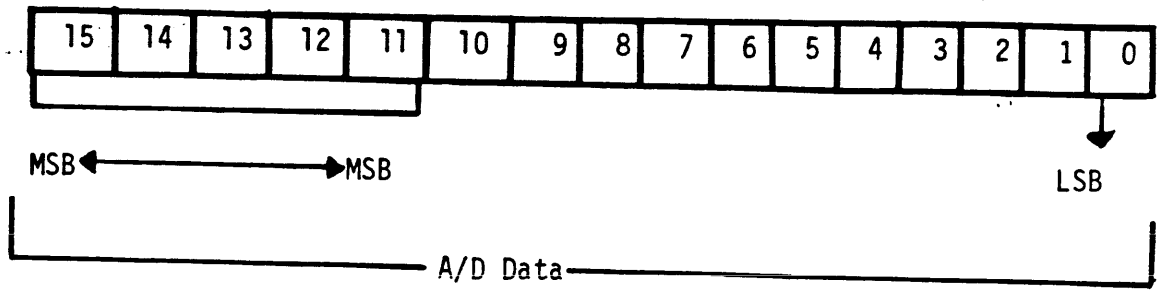
A/D DONE = BASE VECTOR
ERROR = BASE VECTOR + 4

5.1.4 Control and Status Register



5.1.5 A/D DATA BUFFER REGISTER (ADDBR) (READ ONLY)

This location contains the A/D data, the format is as follows:



CSR BIT DESCRIPTIONS: Note:

BIT #	NAME	DESCRIPTION
15	ERROR	READ/WRITE - Indicates an error set by one of the following conditions. 1. Attempting an external start or clock start during MUX settling. 2. Attempting a start while conversion in process. 3. Attempting any start while the A/D Done bit is set. Cleared by Processor and Init.
14	ERROR INT. ENABLE	READ/WRITE - When set enables an Interrupt on Error Bit. Cleared by INIT.
13-8	MULTIPLEXER ADDRESS	READ/WRITE - Six MUX channel address bits for addressing up to 64 channels.
7	A/D DONE	READ ONLY - Set by end of conversion reset by read A/D data. Cleared by INIT.
6	DONE INT. ENABLE	READ/WRITE - When set will enable interrupts from A/D done. Cleared by INIT.
5	RTC ENB	READ/WRITE - Real time clock enable when set this bit allows start conversion from the real time clock
4	EXT TRIG ENB	READ/WRITE - When set this bit allows start conversion from an external trigger source.
3-2	GAIN SELECT	READ/WRITE - These bits provide the gain select information.
Ø	A/D START	WRITE/ONLY - Initiates a conversion when set, cleared by internal logic after start conversion, will always read back as a Ø.

BIT 3 (GS1)	2 (GSØ)	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

5.2 DT2765 Programming

5.2.1 Modes of Operation

The DT2765 can operate in a number of operating modes, as follows.

5.2.2 Program I/O

In this mode standard LSI-11 instructions can access and control the A/D on the interface. Start A/D conversion is accomplished by loading the MUX channel in the CSR.

5.2.3 Interrupt Operation

In many real time applications the computer does not want to be dedicated to taking analog measurements. Then the Interrupt on A/D done bit is utilized.

5.2.4 Device Address

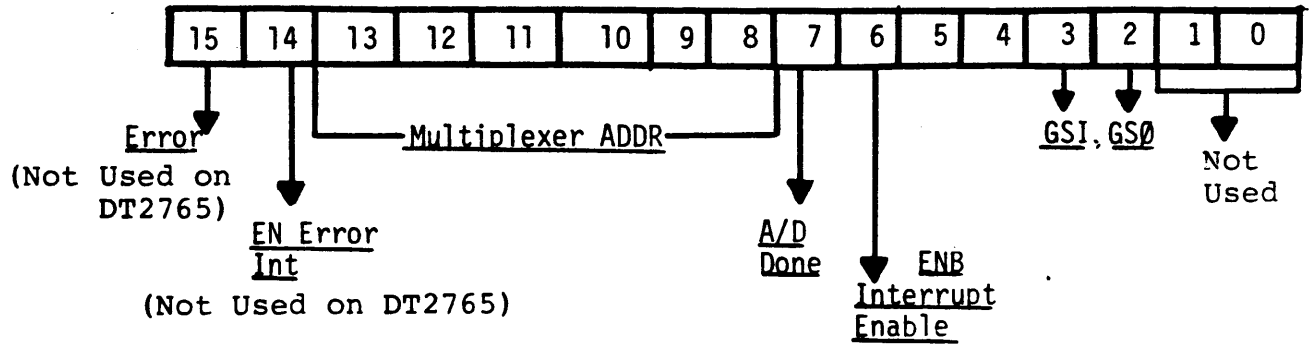
The DT2765 device address is selectable via a dip switch. Device Address may be assigned between 170000_8 and 177774_8. The order of the address is as follows, once a base address has been set in
A/D Control and Status Register (ADCSR) - Base
A/D Data Buffer Register (ADDBR) - Base + 2 (Read only).

5.2.5 Interrupt Vector Address

The vector address is set via a dip switch pack, and are selectable in increments of 10_8. There are two interrupts; A/D DONE, and ERROR.

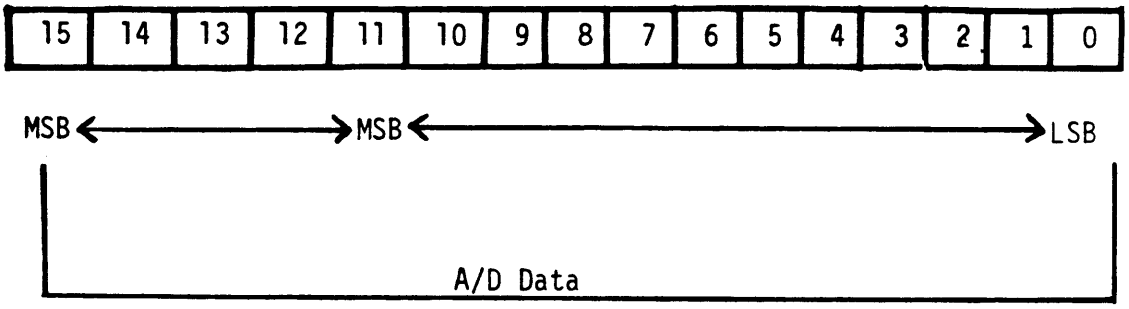
A/D DONE = BASE VECTOR
ERROR = BASE VECTOR + 4

5.2.6 Control and Status Register



5.2.7 A/D DATA BUFFER REGISTER (ADDBR) READ ONLY)

This location contains the A/D data, the format is as follows:



CSR BIT DESCRIPTIONS: NOTE:

BIT #	NAME	DESCRIPTION
15	ERROR (NOT USED IN DT2765)	Cleared by INIT
14	ERROR INT. ENABLE	READ/WRITE - When set Enables an Interrupt on Error Bit. Cleared by INIT
13-8	MULTIPLEXER ADDRESS	READ/WRITE - Six MUX channel address bits for addressing up to 64 channels. Will start an A/D conversion upon loading new MUX channel.
7	A/D DONE	READ ONLY - Set by end of conversion reset by read A/D data. Cleared by INIT.
6	EN INTERRUPT DONE	READ/WRITE - When set will enable interrupts from A/D done. Cleared by INIT
5,4	NOT USED ON DT2765	
3-2	GAIN SELECT	READ/WRITE - These bits provide the gain select information:
1,Ø	NOT USED	

BIT 3 (GS1)	2 (GSØ)	GAIN
0	0	1
0	1	10
1	0	100
1	1	500

NOTE: All instructions that modify the upper Byte of the CSR will cause a start A/D conversion.

CHAPTER 6

USER CONFIGURATION

6.1 Base Address Selection (DT2762, DT2764, DT2765)

The Base Address which is the I/O address assigned to the Control-Status Register (CSR) is user selectable by means of DIP switches SW1 and SW2 located near the bus interface logic as shown in Appendix E. The A/D Data Buffer Register address is then two locations greater than the CSR (Base) address. The DIP switches allow the user to set the base address anywhere in the 170000_8 - 177774_8 address space in increments of 4_8. The recommended base address for the DT2760 series is 177000_8 and is the address set at the factory. Figure 6.1 shows how switches SW1 and SW2 must be set to generate this base address.

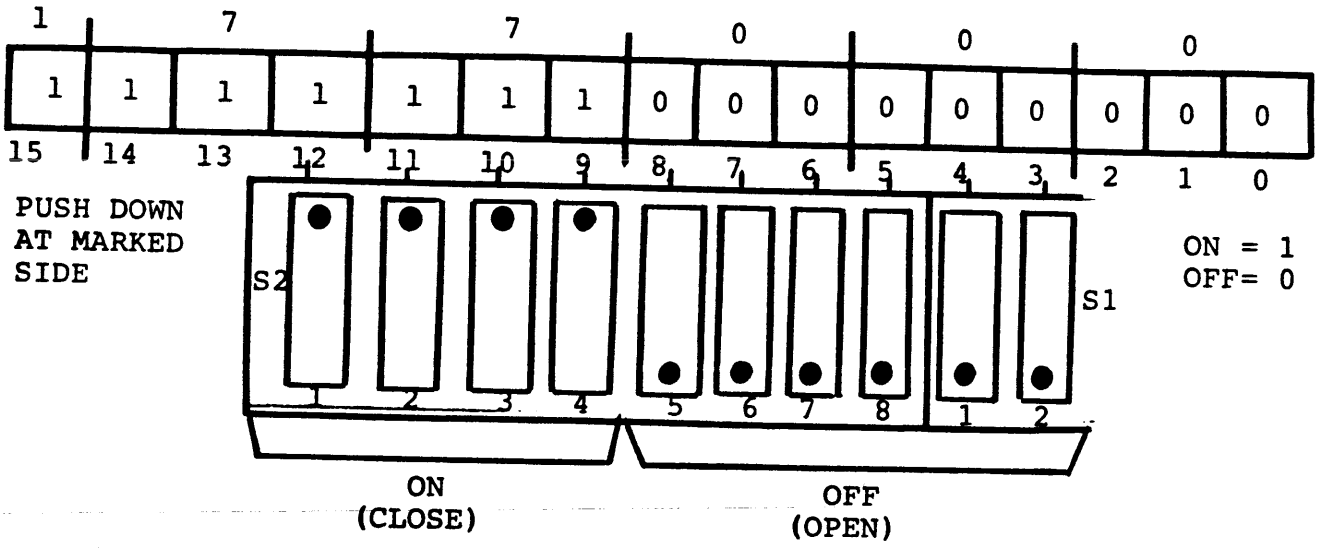


Figure 6.1

Switch Setting for Base Address of 177000_8

As shown in Figure 6.1 a switch in the "ON" position represents a "1" in the corresponding bit location and a switch in the "OFF" position represents a "0" in the corresponding bit location.

6.2 Vector Address Selection - DT2764, DT2765

The DT2760 series systems are capable of generating two distinct interrupt vectors to the LSI-11 processor. These interrupts can occur when:

1. A/D Done is set
2. Error is set

Each of these two events can generate a unique interrupt to the

6.2 processor with the internal priority being arranged such that the A/D Done interrupt has the higher priority of the two if both occur simultaneously and are both enabled. The interrupt vector address in the 000_8 - 770_8 vector address space in 10_8 increments. The interrupt vector of the Error Interrupt is then always 4_8 locations higher than the A/D Done interrupt vector address. The recommended interrupt vector address for the DT2760 series is 130_8 and is set to that value at the factory. Figure 6.2 shows how switch SW2 must be set to generate this address.

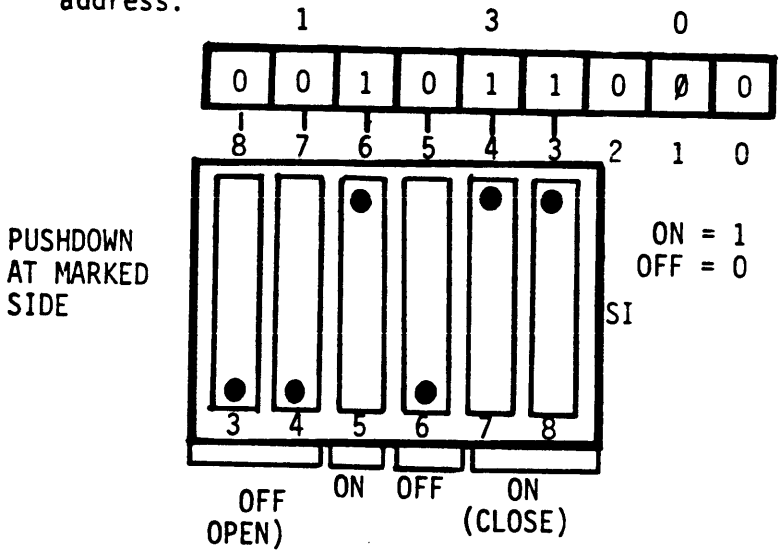


Figure 6.2

Switch Setting for Vector Address of 130_8

6.3 Analog Configuration DT2762

Factory Supplied Range - ±10V FSR 2's Complement Notation.

6.3.1 Ranges

The DT2762 is a high level system only and can be configured for the following ranges and data formats. The ranges are selectable via wire wrap posts and ±10V 2's complement is installed in etch on the board.

RANGE	CONNECT JUMPER
0-10V	1 and 2
±10V	2 and 4
0-5V	3 and 4
±5V	1 and 3

NOTE: The user must cut the jumpers which are already etched at pins 2, 4, 5 to change ranges from the factory supplied ±10V, 2's complement.

NOTE: The jumpers are located at the handle end of the board. Installing a jumper requires wire wrapping across a pair of pins as marked in Fig. 6.

6.3.1.1 PG Option

When the programmable gain option is installed the DT2762 must be set for ±10V or 0 to 10V coding only.

6.3.1.1 PG Option
(Cont.) Thus the ranges with PG option are:

GAIN = 1 - 10V
2 - 5V
4 - 2.5V
8 - 1.25V

6.3.2 Data Notation

Parallel digital outputs are provided in binary code. A unipolar input (0 to 10V, 0 to 5V) signal should be jumpered to produce a straight binary output. A Bipolar input (±5V, ±10V) can be jumpered to produce offset binary coding or 2's complement code.

CODING JUMPERS

BINARY NOTATION - CONNECT JUMPER 6
2's COMPLEMENT - CONNECT JUMPER 5

CODE	10V FULL SCALE	20V FULL SCALE	16 BIT OUTPUT CODE (OCTAL)
BINARY	+9.9976V 0.0000V		007777 000000
OFFSET BINARY	+4.9976V 0.0000V -5.0000V	+9.9951V 0.0000V -10.0000V	007777 004000 000000
2'S COMPLEMENT	+4.9976V 0.0000V -5.0000V	+9.9951V 0.0000V -10.0000V	003777 000000 174000

CODING TABLE

6.4 Analog Configuration DT2764

Factory Supplied - ±10mv FSR 2's Complement notation differential inputs.

6.4.1 DT2764 Single Ended or Differential Input

The DT2764 can be user configured for SE or DI operation as follows:

JUMPERS

SE (16 channels)	P1 to P2
DI (8 channels)	P2 to P3, P4 to P5.

NOTE: The user must cut the jumper in etch at P2 to P3, P4 to P5 to change from DI operation to SE operation

6.4.2 Gain Configuration - DT2764 - Gains from 1 to 1000

The INSTRUMENTATION AMPLIFIER may be programmed for a gain between 1 and 1000. Because the A/D has an input voltage range of either 0 to + 10V volts, or ± 10 volts, the gain of the INSTRUMENTATION AMPLIFIER will determine the input signal voltage range to be digitized. At a gain of 1000, the input signal range for full scale would be 10mV. For a gain of 1, no external resistor need be added, since the instrumentation amplifier has been set to this gain internally. The gain equation for the INSTRUMENTATION AMPLIFIER is:

$$G = 1 + \frac{20{,}000}{R_G} \quad \text{or} \quad R_G = \frac{20{,}000}{G-1}$$

The table shows a chart of resistors and capacitors for setting the gain and timing.

CHART OF INPUT RANGE PARAMETERS

INPUT RANGE	GAIN	Rg (Ohms)	Ct	AMP SETTLING TIME	SYSTEM ACCURACY	THROUGHPUT
±10mV	1000	20.02	0.015uf	250us	±0.1%	3.7KHz
±25mV	400	50.13	6800pf	120us	±0.08%	7.1KHz
±50mV	200	100.5	3300pf	70us	±.07%	11.1KHz
±100mV	100	202.0	150pf	40us	±.05%	16.75KHz
±1.0 Volt	10	2222	None	12us	±.03%	31KHz
±2.5 Volts	4	6667	None	12us	±.03%	31KHz
±5.0 Volts	2	20.0K	None	12us	±.03%	31KHz
±10.0 Volts	1	None	None	12us	±.03%	31KHz

NOTE: THROUGHPUT = AMP SETTLING TIME + 20 USEC A/D CONVERSION TIME.

6.4.3 Unipolar/Bipolar Selection - DT2764

The DT2764 can be configured for Unipolar (0 to F.S.) on Bipolar (±F.S.) operation.

	CONNECT JUMPERS
UNIPOLAR 0 TO F.S.	1 and 2
BIPOLAR ± F.S.	2 and 4

NOTE: The user must cut the jumper in etch at 2 and 4 to change the range from Bipolar to Unipolar.

6.4.4 Data Notation

Parallel digital outputs are provided in binary code. A unipolar input (0 to F.S.) should be jumpered to produce a straight binary output. A Bipolar input (±F.S.) can be jumpered to produce offset binary coding or 2's complement coding.

CODING JUMPERS

BINARY NOTATION - CONNECT JUMPERS 6

2's COMPLEMENT - CONNECT JUMPER 5

CODE	RANGE	16 BIT BINARY CODE
Binary	+ F.S.	007777
	0	000000
Offsett Binary	+ F.S.	007777
	0	004000
	- F.S.	000000
2's COMPLEMENT	+ F.S.	003777
	0	000000
	- F.S.	174000

6.5 Analog Configuration

DT2765 isolated wide range analog input system.

Factory Supplied ±10mV F.S.R. 2's complement notation unless PG option is installed then range is set by program control.

6.5.1 Number of Channels

The DT2765 is strictly a 4 channel isolated analog input system. The inputs are fully isolated via a flying capacitor dry reed multiplexer. Expansion beyond 4 channels is accomplished by the addition of the DT2775 dual height expander module. All inputs are fully differential.

6.5.2 Bipolar - Unipolar Selection

The DT2765 can be configured for Bipolar (±F.S.) or Unipolar (0 to F.S.) operation.

	CONNECT JUMPERS
UNIPOLAR 0 to F.S.	1 and 2
BIPOLAR ±F.S.	2 and 4

NOTE: The user must cut the jumper in etch at 2 and 4 to change the range from Bipolar to Unipolar.

6.5.3 Data Notation

Parallel digital outputs are provided in binary code. A Unipolar input should be jumpered to produce a straight binary output. A Bipolar input(±F.S.) can be jumpered to produce offset binary coding or 2's complement coding.

CODING JUMPERS

BINARY NOTATION - CONNECT JUMPER 6

2's COMPLEMENT - CONNECT JUMPER 5

CODE	RANGE	16 BIT BINARY CODE (OCTAL)
BINARY	+F.S.	007777
	0	000000
OFFSET BINARY	+F.S.	007777
	0	004000
	-F.S.	000000
2's COMPLEMENT	+F.S.	003777
	0	000000
	-F.S.	174000

6.5.4 Gain Configuration - DT2765 - Gains from 1 to 1000

The INSTRUMENTATION AMPLIFIER may be programmed for a gain between 1 and 1000. Because the A/D has an input voltage range of either 0 to +10V volts, or ±10 volts, the gain of the INSTRUMENTATION AMPLIFIER will determine the input signal voltage range to be digitized. At a gain of 1000, the input signal range for full scale would be 10mV. For a gain of 1, no external resistor need be added, since the instrumentation amplifier has been set to this gain internally. The gain equation for the INSTRUMENTATION AMPLIFIER is:

$$G = 1 + \frac{20{,}000}{R_G} \quad \text{or} \quad R_G = \frac{20{,}000}{G-1}$$

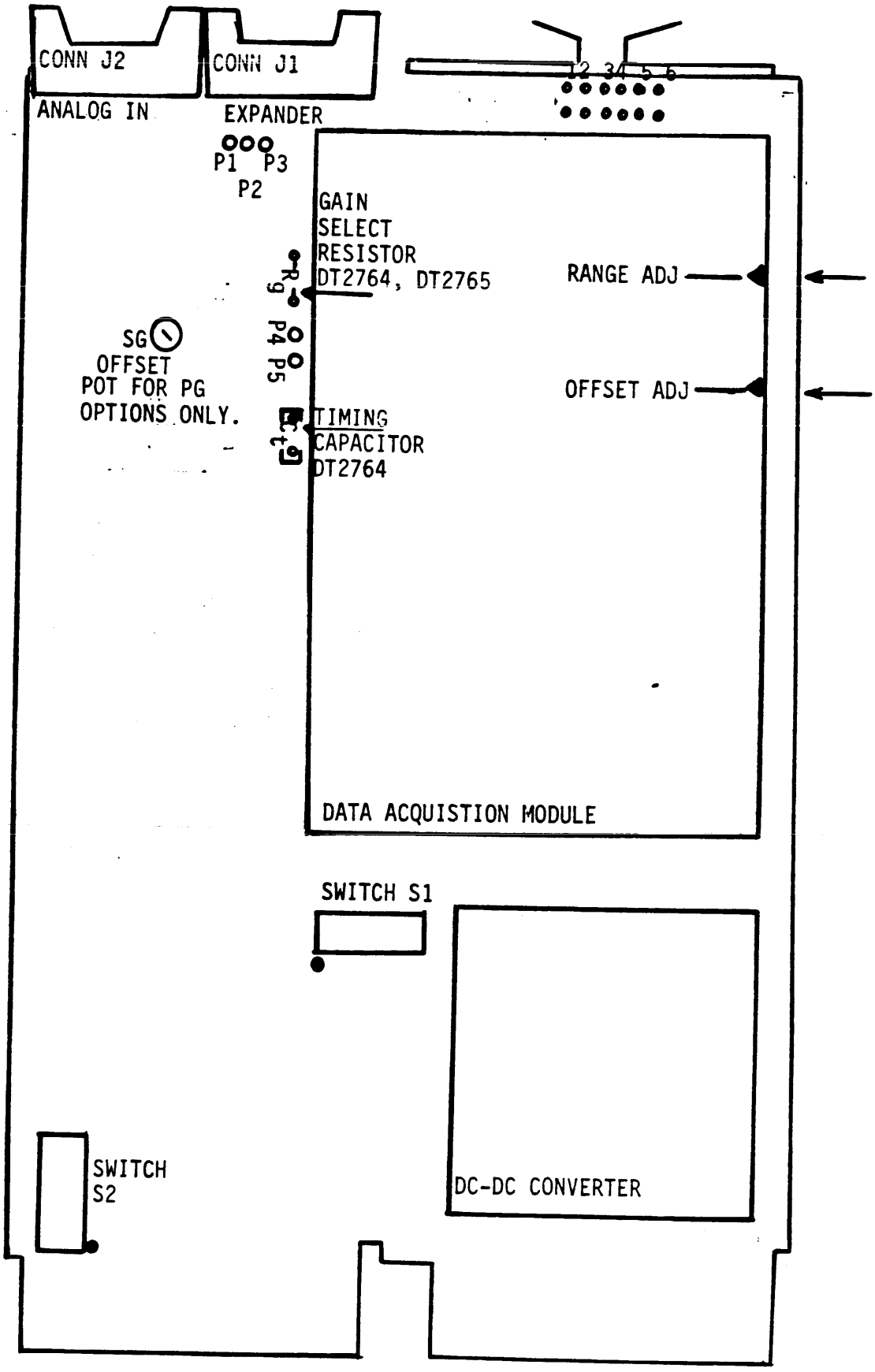
The table shows a chart of resistors for setting the gain.

INPUT RANGE	GAIN	OHMS	SYSTEM ACCURACY
±10mV	1000	20.02	+0.1%
±25mV	400	50.13	+0.08%
±50mV	200	100.5	+.07%
±100mV	100	202.0	+.05%
±1.0 Volt	10	2222	+.03%
±2.5 Volts	4	6667	+.03%
±5.0 Volts	2	20.0K	+.03%
±10.0 Volts	1	None	+.03%

6.5.5 Programmable gain option.

The DT2765 can be configured with a programmable gain amplifier. In this case the range must be set for 10V and the gains can be programmed as follows:

GAIN	RANGE
1	10V
10	1V
100	100mV
500	20mV



DT2762 CONFIGURATION DIAGRAM

Figure 6

CHAPTER 7

CONNECTION OF ANALOG INPUTS

Table 7.1 shows the various models and the connection schemes available.

MODEL	SE/DI JUMPER SELECTABLE	NUMBER OF INPUTS.
DT2762-SE	NO	16
DT2762 - DI	NO	8
DT2764	YES	16 SE 8 DI
DT2765	NO	4 DI (ISOLATED)

7.1 Single Ended Inputs - 16 Channels

Single ended analog inputs - Single ended connections are those which have a common side that is referenced back to analog common of the system. The advantage of this scheme is that the user gets twice the number of channels in the same space. The major disadvantage is that the user gives up any common mode rejection he might obtain from a differential system.

Recommendations:

High level inputs, greater than 1V.
Short lead lenghts, less than 15 ft.

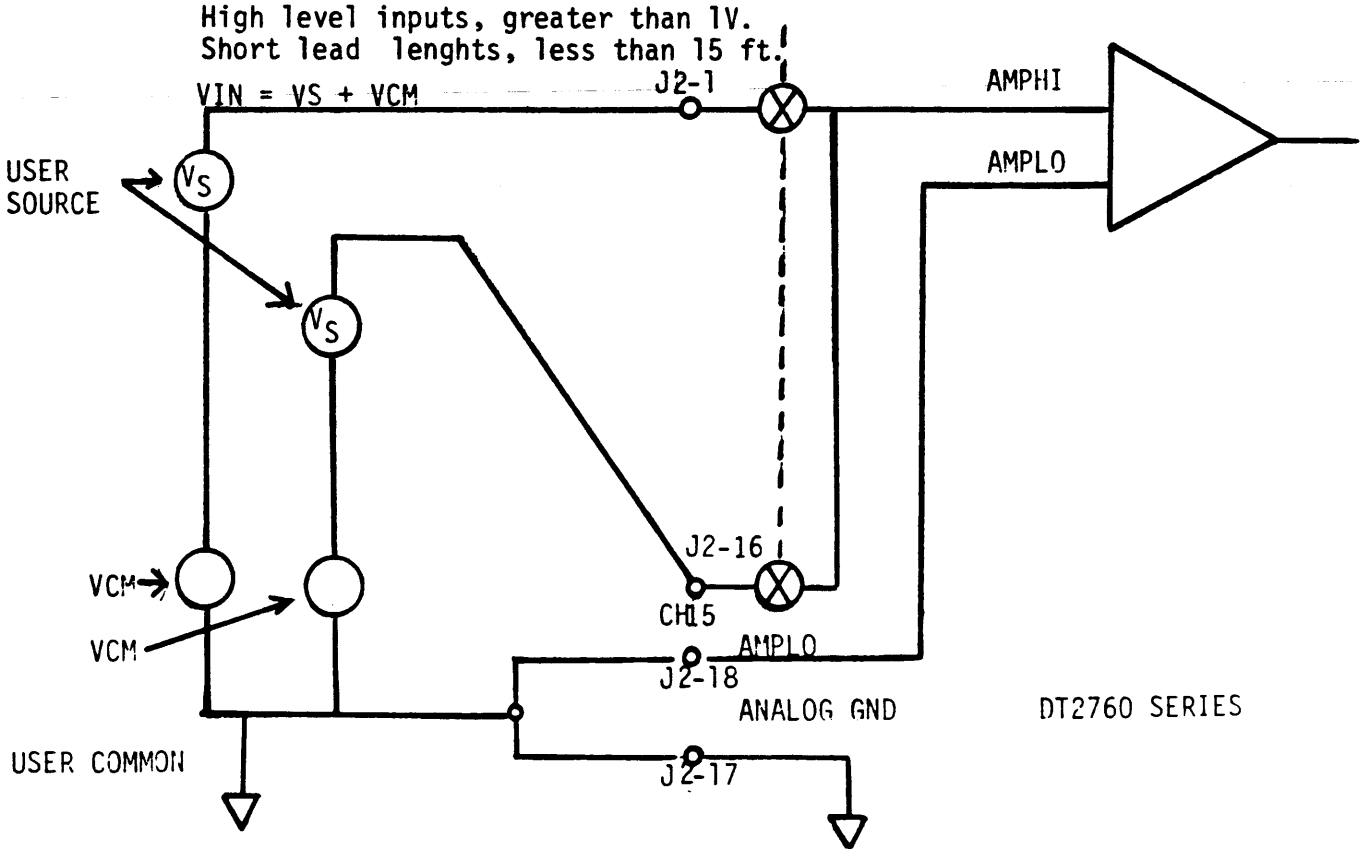


Fig 7.1 Single Ended Inputs

Fig. 7.1 Single Ended Inputs (continued)

Where VCM = Common Mode Voltage

7.2 Pseudo - Differential Inputs - 16 Channels.

Pseudo - Differential mode can be utilized with a single ended system if the user has all input sensors referenced to a common ground point. In this manner the input instrumentation amplifier can reject common mode noise. This is possible since the AMP LO input is brought out to connector J1 for user connection. The following diagram illustrates -

Recommendation:

Input Ranges: 100mV to 10V
Lead Lenghts- less than 25 ft.

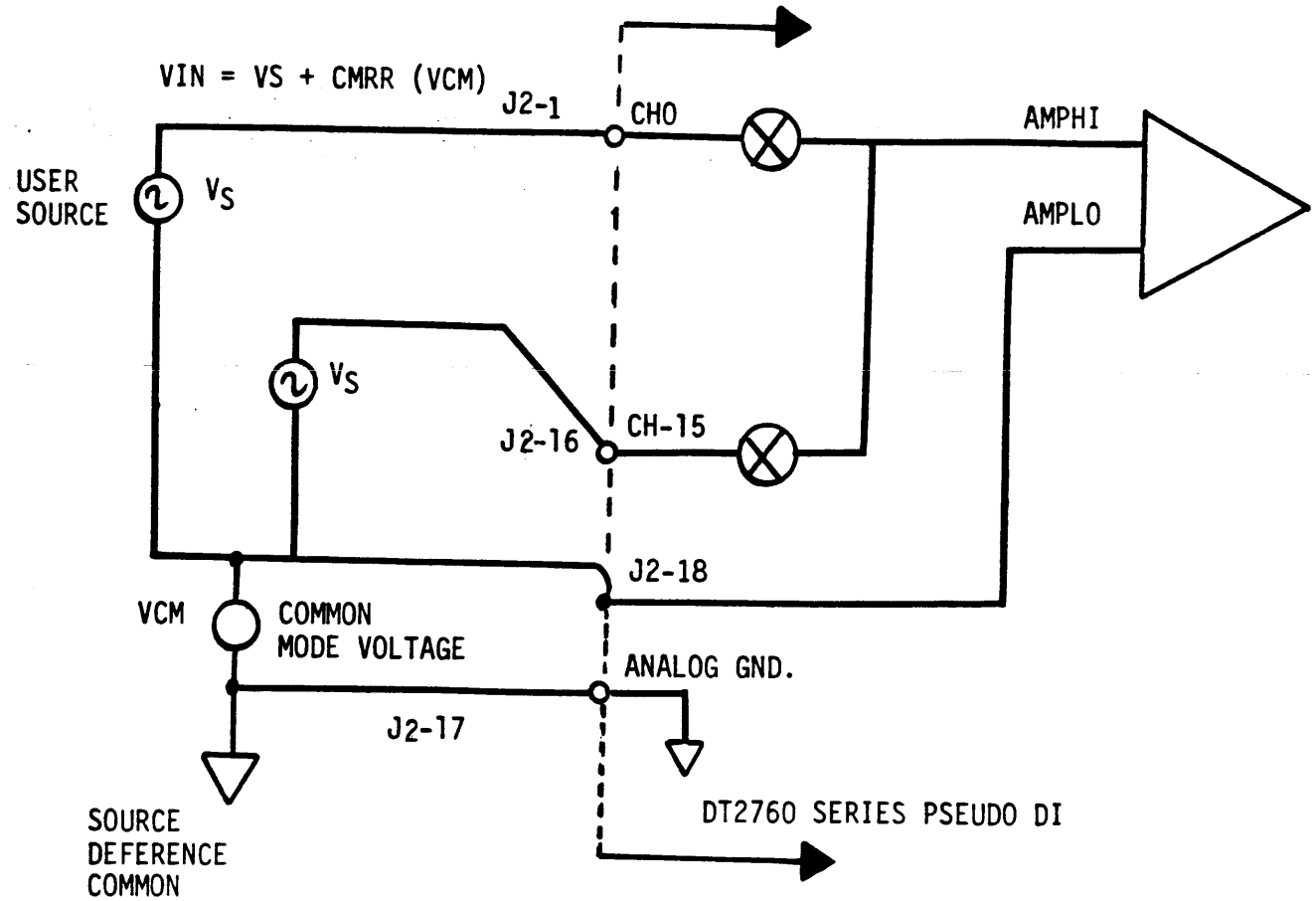


Fig. 7.2 PSEUDO-DIFFERENTIAL

7.3 Differential Inputs - 8 Channels

Differential Inputs - when the differential input scheme is utilized, there are two switches per channel, thus the number of channels are cut in half. The benefits are that common mode voltages, i.e. voltages appearing on both sides of the source simultaneously can be rejected by the differential input instrumentation amplifier. This CMR accounts for a much quieter system. The amount of CMRR depends on how well balanced the instrumentation amplifier is.

Recommendations:

Input Ranges:	10mV to 10V
Lead Lenghts:	As required by user
Lead Type:	Twisted Pair (Low Level) Shielded Input line.

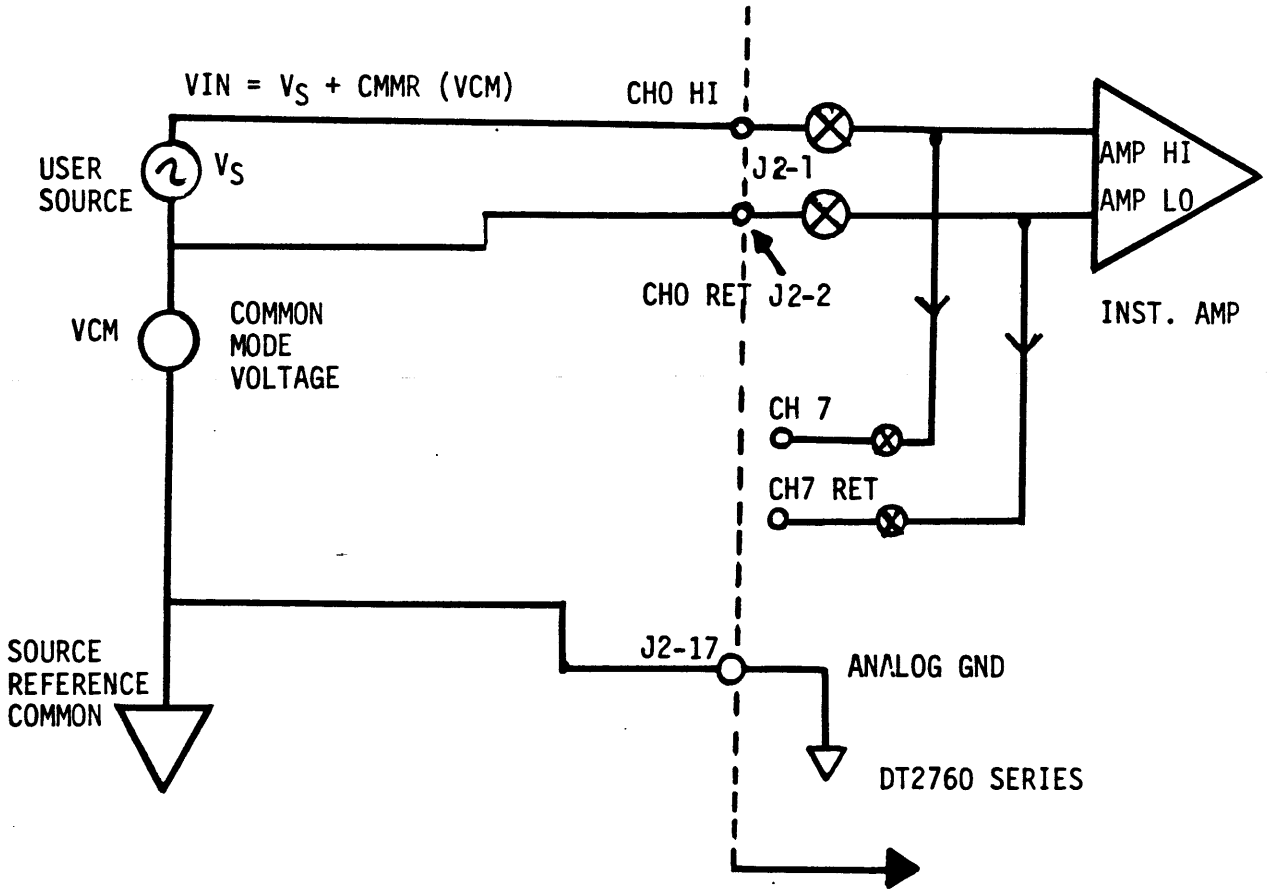


Fig. 7.3 DIFFERENTIAL INPUT CONNECTION

7.4 Isolated Analog Inputs - DT2765

The DT2765 provides four (4) isolated input channels via a dry reed flying capacitor multiplexer. Since the inputs are isolated there need not be any connection of system ground to input signal reference.

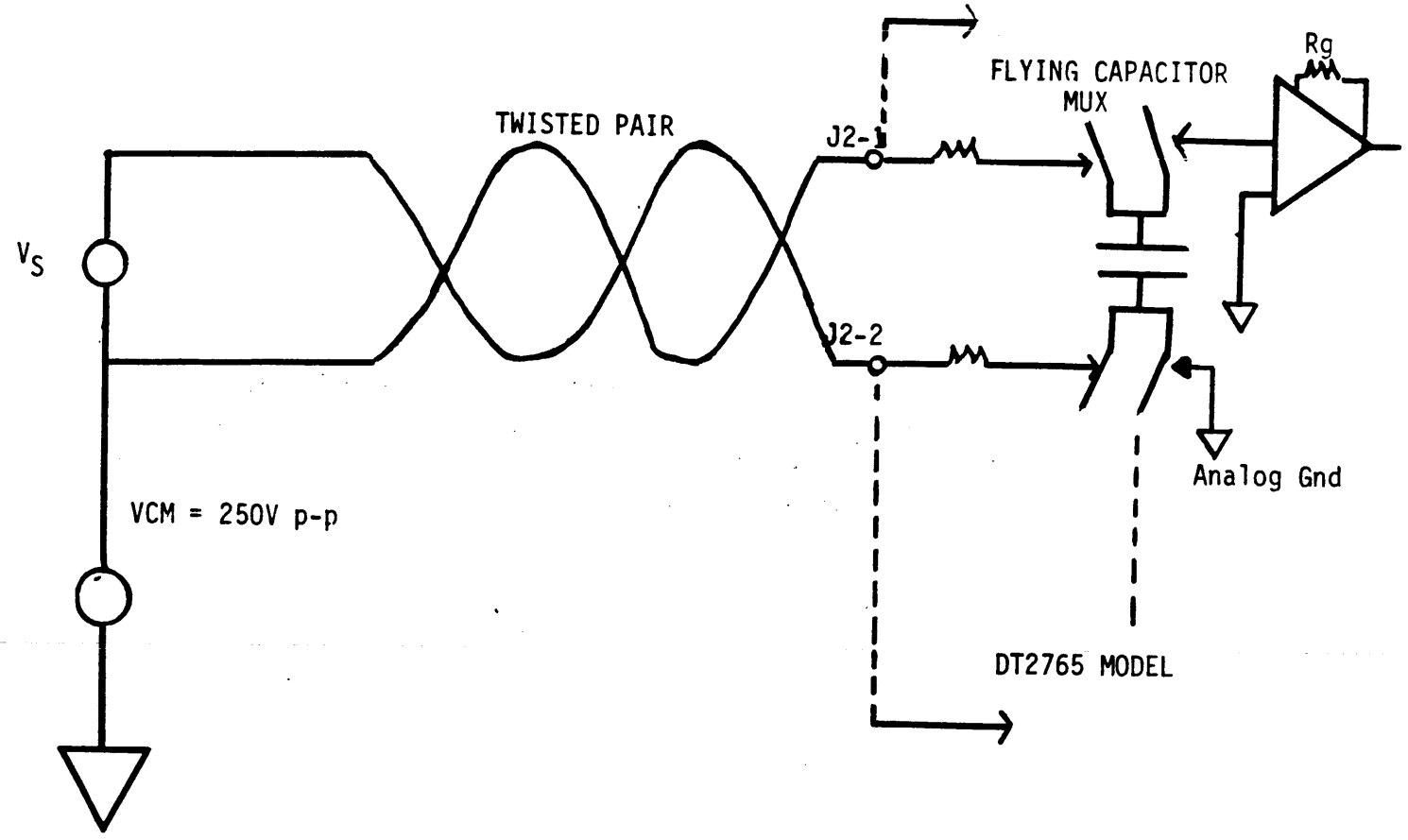


Fig 7.4 Isolated Analog Input.

7.5 Avoiding Spurious Signals

In order to obtain the best performance from a system, certain guidelines in connecting analog signals to the system should be utilized. These guidelines and precautions will minimize the pickup of electrical noise by measuring circuits.

7.5.1 Twisted Pair Input Lines

The effects of magnetic coupling on the input signals may be reduced for differential input configuration by twisting the signal and return lines. This is effective since the inductive pickup voltages on the two lines tend to match, thus not having an effect on the measurement. This is not the case for a ground referenced single ended system.

7.5.2 Shielded Input Lines

The effects of electrostatic coupling may be reduced by shielding the input lines. This becomes important if the source has a high impedance. The shield should only be tied to ground at the instrument end. This will prevent ground loop currents.

7.5.3 Input Settling with High Source Impedance

Solid state multiplexers inject a small amount of charge into the input lines when channels are switched. This can cause a transient error due to the input source impedance time constants. All Data Translation systems allow for input settling upon new channel selection. The settling time varies for the different input systems available.

Normally, the control logic allows sufficient time for this charge to settle to less than ½LSB of error (nine time constants to .012 percent). However, more time may be needed when the multiplexer is switching an input channel with high source impedance, particularly when large amounts of shunt capacitance exists in the interconnecting cables. Source impedance/cable shunt capacitance products greater than 1 uSec (1K-1000PF) on 30KHz units should be avoided for less than ½LSB error. Assuming a twisted pair cable capacitance of 50 PF/foot and 1K ohm source impedance this translates into a maximum run of twenty feet on 30KHz models. Note also that settling errors can be minimized by increasing the internal time out with an external capacitor C_t ($\approx$ 60PF per uSec).

7.6 Common Mode Rejection Ratio - (CMRR)

The CMRR of a system is defined as the ratio of output voltage from the instrumentation amplifier to the voltage which is common to both sides of the differential input amplifier. This ratio is given in units of decibels.

7.6 (Cont.) For example, the specification for CMRR on Data Translation's wide range interface is 100db at 60HZ at a gain of 1000. Thus with a CMV of 10 volts, the V out of the amplifier at a gain of 1000 should be:

$$CMRR = 20\log_{10} \left(\frac{CMV}{VOUT/A}\right)$$

Where CMRR = common mode rejection in db
CMV = common mode voltage
VOUT = The change in the amplifier output voltage due to the CMV.
A = Amplifier gain

$$100 = 20\log_{10} \left(\frac{CMV}{VOUT/A}\right)$$

$$\text{Antilog } \left(\frac{100}{20}\right) = \frac{10^4}{VOUT/1000}$$

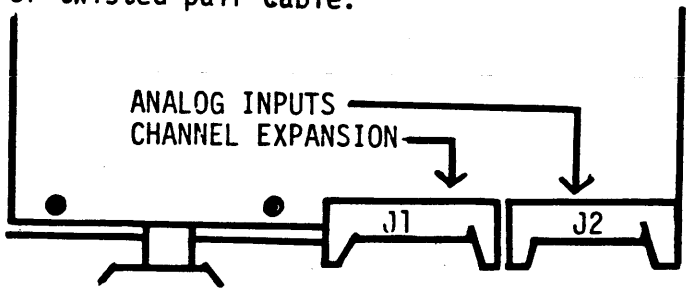
$$10^5 = \frac{10^4}{VOUT}$$

$$VOUT = 10^{-1} \text{ V.}$$

Thus with a CMV of 10 volts, the output of the instrumentation amplifier is 100 millivolts.

7.7 User Connections

User connections are via a 20 pin connector.
Mass terminated connections can be made to either flat ribbon cable or twisted pair cable.



7.7.1 CONN J1 - Channel Expansion - RTCIN

Connector J1 is utilized for expansion of input channels via expander loads DT2772, DT2774 and DT2775. Also contained on this connector is the Real Time Clock input RTCINL.

J1 CONNECTOR - EXPANSION CONNECTOR			
Pin	Signal Name	Pin	Signal Name
1	MXØH	2	MX1H
3	MX2H	4	MX3H
5	MX4H	6	MX5H
7	MXENB	8	SE/DI
9	RTC INL	10	D GND
11	DGND	12	
13	AGND	14	A GND
15	MXOUT HI	16	MXOUT LO
17	AGND	18	-15V
19	AGND	20	+15V

7.7.2 CONN - J2 Analog Inputs

CONN J2 - DT2762/DT2764 SINGLE ENDED INPUTS			
Pin	Signal	Pin	Signal
1	CH0	11	CH5
2	CH8	12	CH13
3	CH1	13	CH6
4	CH9	14	CH14
5	CH2	15	CH7
6	CH10	16	CH15
7	CH3	17	AGND
8	CH11	18	AMPLO
9	CH4	19	EXT TRIG L
10	CH12	20	D. GND.

CONN J2 - DT2762/DT2764 Differential Inputs			
Pin	Signal	Pin	Signal
1	CHØ	11	CH5
2	RETØ	12	RET5
3	CH1	13	CH6
4	RET1	14	RET6
5	CH2	15	CH7
6	RET2	16	RET7
7	CH3	17	AGND
8	RET3	18	AMPLO
9	CH4	19	EXT TRIG L
10	RET4	20	D. GND

7.7.2 DT2765/DT2765-T - User Inputs
(Cont.)

CONN J2 - ISOLATED DIFFERENTIAL INPUTS			
Pin	Signal	Pin	Signal
1	CH0 HI	11	
2	CH0 LO	12	
3		13	CH3 HI
4		14	CH3 LO
5	CH1 HI	15	COMPIN HI
6	CH1 LO	16	COMPIN LO
7		17	A. GND
8		18	AMP LO
9	CH2 HI	19	EXT. TRIG LO
10	CH2 LO	20	D. GND

7.8 External Trigger and RTC Inputs

This series of analog interfaces allow the user to externally trigger the conversion. Thus allowing synchronization of conversion to real word or a real time clock input. Data Translation can supply the user with a KWV11-A equivalent module, the DT2769 real time clock module.

7.8.1 Input Signal Characteristics

7.8.1.1 EP050 REVD.

For this revision the RTCIN inputs and the EXT TRIG inputs are different.

EXT TRIG L Input - CONN J2 PIN 19

DIGITAL GROUND - CONN J2 PIN 20

- TTL compatible, 1 unit LOAD
- Positive pulse, 100 MSEC to 2μSEC duration.
- Trigger on high to low transition.

RTC INL INPUT - CONN J1 PIN 9

DIGITAL GROUND - CONN J1 PIN 10

7.8.1.1 (Cont.)

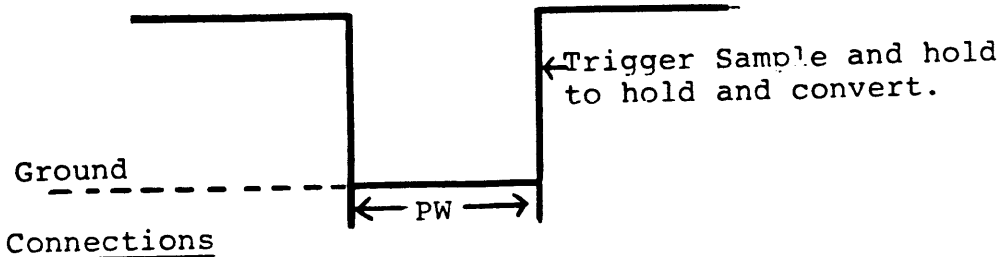
- TTL or CMOS input compatible
- Source current < 10uA
- Sink current < 10uA
- LO THRESHOLD < 0.8V
- HI THRESHOLD > 2.4V
- MAX HI VOLTAGE 11V MAX.
- Pulse input - Hi to low pulse duration 200NSEC to 2uSEC.
- Trigger on LO to HI transition.

7.8.1.2 EPO50 REV E

This revision has both inputs with identical electrical characteristics.

Electrical Characteristics

- TTL or CMOS compatible
- Source current, less than 10μA
- Sink current, less than 10μA
- LOW THRESHOLD, less than Ø.8V
- HIGH THRESHOLD, greater than 2.4V
- MAX. HIGH VOLTAGE, 11V
- Pulse input, High to low pulse with a duration between 200NSEC and 2μSEC.
- Trigger on Low to High transition.



Connections

RTCINL - CONN J1 PIN 9, or Wire Wrap Pin (see appendix E)

EXTTRIGL - CONN J2 PIN 19, or Wire Wrap Pin (see appendix E)

A special wire is supplied with every DT2769 real time clock board to allow easy connection between the DT2769 output and the DT2760 series analog input board.

CHAPTER 8

CALIBRATION AND TESTING

8.1 Equipment and System Requirements

In order to assist the user in testing the operation of the DT2760 series interfaces, Data Translation has developed a comprehensive software diagnostic aid designated SP0023. This software is provided in either of the two media: Paper pape for minimum, paper tape based LSI-11 Systems, or Floppy Disks for more sophisticated RT-11 Systems. The system and test equipment requirements for this software are given below:

SP0023 - DT2762
DT2764
SP0029 - DT2765

SP0023/SP0029 System Requirements

Paper Tape:

KD11-F (LSI-11) processor, ECO #10 or greater

or

KD11-HA (LSI-11/2) processor

Minimum of 4K words RAM
Serial Interface at Standard DEC console address
Paper tape reader
Data Translation DT2760 series interface.

Floppy Disk

KD11-F (LSI-11) processor, ECO #10 or greater

or

KD11-HA (LSI-11/2) processor

Minimum of 8K words RAM
System console terminal at standard DEC console address
DEC compatible dual floppy disc drive system
RT-11 operating system (Version 2 or Version 3)
Data Translation DT2760 series interface

Test Equipment Requirements

10MHz or greater bandwidth oscilloscope
Laboratory quality voltage standard.

8.2 Loading SP0023/SP0029 from Paper Tape

This software is supplied in PDP-11 absolute loader format. To load this release into memory the following steps must be taken:

1. Load the LSI-11 absolute loader (see DEC documentation for information on this.)
2. Place the paper tape in the paper tape reader.
3. Start the absolute loader at location XXX500 where XXX is determined by the following table: (See 8-2)

8.2 (Cont.) Loading SP0023/SP0029 from Paper Tape

SYSTEM MEMORY SIZE	XXX
4K	017
8K	037
12K	057
16K	077
20K	017
24K	137
28K or greater	157

Following this procedure will cause SP0023 to be loaded into memory and executed.

8.2.1 Loading Floppy Disk

The SP0023 on SP0029 diskette contain an RT-11 memory image file called SP0023.SAV. This is a linked and executable version of SP0023. To load and execute SP0023 the user should boot up RT-11 in the usual way with the system disk in drive Ø. When RT-11 comes up the user should insert the SP0023 disk into drive 1 and type the following command string to the RT-11 monitor;

.RUN DX1:SP0023 (Return)

This will cause SP0023 to be loaded and executed, at this time the SP0023 monitor will have control of the system and RT-11 will be prevented from interfacing.

8.3 Using SP0023 /SP0029

SP0023/SP0029 is a stand-alone software diagnostic package that allows the user to test Data Translation's dual-height series of LSI-11 interface cards. The test program does not need RT-11 once it has been loaded and in fact it flushes RT-11 from the system after it has loaded. To allow the user to control the testing procedure a monitor has been included that interfaces to the user. When SP0023/SP0029 is brought up this monitor is automatically entered. On start up the resident monitor prints out the directory of the various Data Translation interface boards that can be tested followed by the monitor prompt character ">" (a right angle-bracket). At this point the user should set the desired model number to be tested using the MODEL command, for example:

>Model (Space) DT2762 (Return)

would set up the program to test the DT2762 Analog Input Board. The monitor would then invoke all the necessary initialization routines to test this board and confirm the board model by printing out a confirmation message followed by the default base and vector addresses that will be used. These base and vector addresses have

8.3 (Cont). been preset at the factory and need not be changed. If for some reason however a change in the base or vector address is required the user can modify locations 542 (base address) and 544 (vector address) to the new address. In order to easily facilitate this change the SP0023/SP0029 monitor also has some subset capabilities of ODT. In particular the user can use the slash and back-slash characters to open and modify memory locations just as in ODT. Therefore if the user needs to change any location he should type the address followed by a slash (/) or back-slash (\), the monitor will then open that location just as in ODT. The user can roll up or down sequentially in memory by using the line feed or carat (^) keys. The SP0023/SP0029 monitor is reentered from the ODT mode by typing a carriage return. Like ODT a memory location will only be modified if a valid octal number is typed before any of the ODT terminator characters. For example, to change the base and vector address of the DT2762 tests one would type:

```
>542/17700 170400 (line-feed)
000544/000300 400 (return)
>
```

to change the base address to 170400 and vector address to 400. Note that this change is only temporary and the default addresses will be reloaded if the model number is retyped or if SP0023 is reloaded. In addition to these commands the SP0023 test executive allows the user to ask for the model directory, to start tests, to loop or halt on tests or even to reboot RT-11. The commands available to the user under the SP0023 test executive are listed on the following page.

Example: User wants to run a scope loop on Test 2 because an error is encountered. Type:

```
>IL TEST (Space) 2
```

In this case the program will loop on Test 2 and inhibit error printouts.

If a test is run and no errors occur the test will return to the SP0023 command level without any other messages. If however, an error does occur then the test will print out the test number and error code. The user may look up the meaning of each error code in the program listings given in Appendix A.

8.4 Test Descriptions

All descriptions of the tests and the set up requirements needed for any particular test are described in detail in the program listings at the beginning of each test.

8.5 SP0023/SP0029 Program Description

SP0023/SP0029 consists of two groups of tests. The first group contains a series of tests which test all the logic of the interface board. These tests contain scope loops for debug purposes and will provide an error message if a problem exists. The second set of tests test the analog operation and calibration of the boards.

A listing of all the tests for testing DT2760 series boards can be found at the beginning of the program listings.

Note that the user can run all the logic tests by using the monitor ALL command. Calibration tests, however, must be run individually.

COMMAND	FUNCTION
ALL	Runs all logic tests that are present for current device. Generates an error if there is no current device.
BOOT	Jumps to the standard hardware bootstrap (173000). Generates an error if there is no bootstrap present.
DIRECTORY	Displays the contents of the current directory.
EXIT	Halts the processor
MODEL	Displays the parameters associated with the current device. Generates an error if there is no current device.
MODEL (space) DTXXXX	Searches the current directory for the given model number. If found, makes that model the current device. Generates an error if there is no current directory or if the model number cannot be found.
TEST	Runs the last test executed.
TEST (space) ⟨octal number⟩	Runs the indicated test

Test Command prefixes - The following command prefixes are to be used with the TEST command to control the execution of the various tests.

COMMAND PREFIXES TO TEST EXECUTION COMMANDS

R	(TEST command only)	repeat this test continuously
L	(both TEST and ALL)	loop on this test if an error is detected.
H	(both TEST and ALL)	halt test stream if an error is detected.
I	(both TEST and ALL)	inhibit error printout

A control-C will terminate any test.

Example: User wants to run a scope loop on Test 2 because an error is encountered. Type:

ILTEST (space) 2

In this case the program will loop on test 2 and inhibit error printouts.

SP0023/SP0029 Error Codes - SP0023/SP0029 will print an error code when a specific error is encountered. All codes are in the program listing and show the error and what test the program was in when a failure occured. Use the table of contents printed at the front of the listing to quickly find the pages in the listing associated with the test that generates the error.

8.6 SP0023 Tests

Logic Tests

TEST 1:	BRPLY FROM ALL REGISTERS
TEST 2:	CHECK ADCSR BITS
TEST 3:	BINITL ACTION
TEST 4:	BYTE OPERATION OF ADCSR
TEST 5:	A/D DONE BIT AND INTERRUPT
TEST 6:	ERROR BIT AND INTERRUPT
TEST 7:	END OF LOGIC TESTS
TEST 10:	A/D CALIBRATION
TEST 11:	A/D INPUT CHANNEL SCAN
TEST 12:	A/D INPUT GAIN/CHANNEL SCAN

SP0029 TESTS

TEST 1:	BRPLY FROM ALL REGISTERS
TEST 2:	CHECK ADCSR BITS
TEST 3:	BINITL ACTION
TEST 4:	BYTE OPERATION OF ADCSR
TEST 5:	A/D DONE AND INTERRUPT
TEST 6:	END OF LOGIC TESTS
TEST 7:	A/D CALIBRATION
TEST 10:	A/D INPUT CHANNEL SCAN
TEST 11:	A/D INPUT GAIN/CHANNEL SCAN.

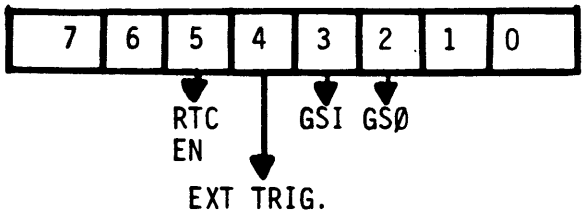
8.6.1 Test Description

All description of tests are located in the program listing at the beginning of each test.

8.6.2 Modes of Operation

Test 10, 11 and 12 will ask for a MODE input when they are called. This MODE input is the lower byte of the CSR.

8.6.2 (Cont.) When a user wants to run an interface under RTC control or EXT TRIG he can set these bits when the program asks for MODES. If a user wants to run under EXT TRIG he will set the MODES as 20_8,



MODE BITS FOR USE IN TEST 10, 11 AND 12.

8.6.3 Calibration

Calibration of the system requires a voltage standard for highly accurate analog inputs and a DVM for calibration of analog inputs.

Equipment Required:

Voltage standard - EDC Model MV-100 or equivalent
- Data Technology Model 40 or equivalent.

8.6.3.1 Calibration of Analog Inputs

Configuration ±10V FS, 2's complement notation:

1. Connect a Voltage Standard to CHØ input
2. Set standard to -2.4mV
3. Start A/D Calibration test at CHØ, Mode Ø.
4. Adjust A/D offset for the printout between 177777 and ØØØØØ
5. Set voltage standard to +9.9927V
6. Adjust A/D range control for printout between 003776 and 003777

NOTE: For ±10mV systems (DT2765, DT2764) divide above voltage values by 1000. (Octal values remain the same.)

8.6.3.2 Calibration of Analog Inputs with Programmable Gain Amplifier

1. Adjust the A/D offset and range as in section 8.4.3.1
2. Set voltage standard to -600mV
3. Start A/D Calibration Test at CHØ Mode 14_8
4. Adjust the Programmable gain offset pot for a printout between 177777 and ØØØØØØ

For other ranges please see 8.0 Adjustment Values.

8.7 Adjustment Values

8.7.1 Notes on Full Scale (FS)

Full Scale (FS) is the amount of input voltage required to turn on all the bits of the A/D converter. For a D/A converter, the inverse is true: Full Scale is the voltage that results when all bits of the converter are turned on.

In a 12 bit converter there are 4096 possible states (2^{12}). Because one of these states is given to zero, the converter lacks one state at its high or positive FS end. Hence even though the converter is rated at 1Ø volts Full Scale, the positive Full Scale value will actually be 1 state (1 least significant bit value) below 1Ø volts. For example, a 0-10 volt range converter has a least significant bit value of 2.44V (1Ø volts / 4069 states). The positive Full Scale will be reached at 1Ø volts -2.44 mV or 9.99756 volts. The negative full scale (in this instance taken to mean the voltage associated with all converter bits OFF) will be Ø volts.

The Full Scale Range is the difference in voltage between positive Full Scale (all converter bits ON) and negative full scale (all converter bits OFF). Thus a Ø-1Ø volt converter has a Full Scale Range of 1Ø volts while a ±1Ø volt converter has a FSR of 2Ø volts.

8.7.2 Computing Calibration Values

(Note: LSB (least significant bit) = FSR ÷ 4096

8.7.3 A/D Offset Adjustment Valves

Unipolar Ranges 0-n Volts, $n \leq 1Ø$

		Adjust for Printout Between	
Input Range	Input Voltage	Low Value	High Value
any	+½LSB	Ø	1 LSB
any, Octal output.	+½LSB	0000	0001
Ø-1Ø	+1.22Ø7mV	0000	0001
0-5V	+Ø.61Ø4mV	0000	0001
0-10mV	+1.22Ømv	0000	0001

Bipolar Ranges (+n Volts, n ≤ 10)

		Adjust for Printout Between	
Input Range	Input Voltage	Low Value	High Value
any	Ø volts -½ LSB	Ø volts -1 LSB	Ø volts
any, OCTAL output	Ø volts -½ LSB	177777	ØØØØØØ (two's complement.)
±1ØV	-2.4414mV	008777	004000 (offsett binary)
±5V	-1.22Ø7mV		
±1ØmV	-2.4414uV		

8.7.4 A/D Range Adjustment Valves

Unipolar Ranges (Ø-n Volts, n 1Ø)

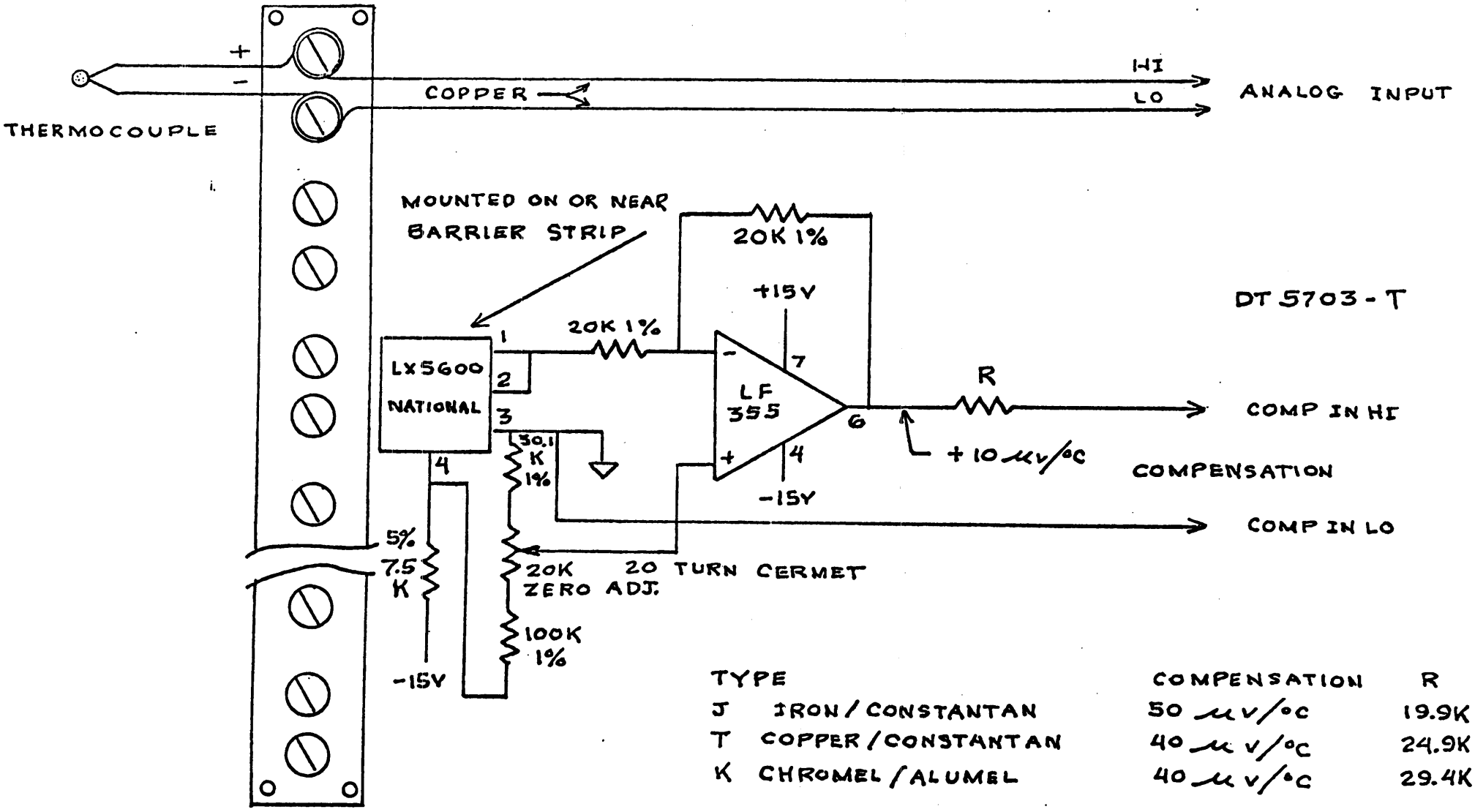
		Adjust for Printout Between	
Input Range	Input Voltage	Low Value	High Value
any	+FS-1½LSB	+FS-2LSB	+FS-1 LSB
Any, OCTAL output	+FS-1½LSB	007776	007777
Ø-1Ø	+9.9963V		
Ø-5V	+4.9982V		
Ø-1ØmV	+9.9963mV		

Bipolar Ranges (±n Volts, N 1Ø)

		Adjust for Printout between	
Input Range	Input Voltage	Low Value	High Value
any	+FS - 1½ LSB	+FS-2 LSB	+FS - 1 LSB
any, octal output	+FS - 1½ LSB	003776	003777 (two's complement)
±10V	+9.9927	007776	007777 (offset binary)
±5V	+4.9964		
±10mV	+9.9927mV		

APPENDIX A

4-20MA INPUT OPTIONS



TYPE		COMPENSATION	R
J	IRON / CONSTANTAN	50 μv/°C	19.9K
T	COPPER / CONSTANTAN	40 μv/°C	24.9K
K	CHROMEL / ALUMEL	40 μv/°C	29.4K

$$R = \left(\frac{10\,\mu V}{COMP} - 1\right) .100$$

ANBIENT TEMPERATURE COMPENSATION CIRCUIT

THERMOCOUPLE COLD JUNCTION COMPENSATION CIRCUIT.

A.1 4-20 mA Inputs are supplied on the DT2762 and DT2765 by ordering (4-20). This option is configured by Data Translation by adding precision 250 ohm resistor on the interface board. A modified data acquisition module is also utilized providing a 1 to 5V input - thus the user just supplies us current input and will receive full 12 bit resolution of his signal.

DT2762 (4-20) - 8 Channels input

DT2765 (4-20) - 4 channels input

A.2 CODING

DT2765	DT2762	VIN(V)	IiN (mA)
000Ø	7777	1.000	4.000
0001	7776	1.0010	4.004
0002	7775	1.0020	4.008
0004	7773	1.0039	4.015
0010	7767	1.0078	4.031
0020	7757	1.0156	4.062
0040	7737	1.0313	4.125
0100	7577	1.0625	4.250
0200	7577	1.1250	4.500
0400	7377	1.2500	5.000
1000	6777	1.5000	6.000
2000	5777	2.0000	8.000
4000	3777	3.0000	12.000
6000	1777	4.0000	16.000
7000	0777	4.5000	18.000
7400	0377	4.7500	19.000
7600	0177	4.8750	19.500
7700	0077	4.9375	19.750
7740	0037	4.9688	19.875
7760	0017	4.9844	19.938
7770	0007	4.9922	19.969
7774	0003	4.9961	19.984
7776	0001	4.9980	19.992
7777	0000	4.9990	19.996

APPENDIX B

TEMPERATURE COMPENSATION CIRCUIT

FOR

DT2765-T

AMBIENT TEMPERATURE COMPENSATION CIRCUIT

When the termocouple wire is connected to copper wire at the barrier strip an additional thermocouple is made with an output that would cancel the measurement thermocouple's output if the barrier strip was at the same temperature.

To compensate for this error a National Semiconductor LX5600 temperature transducer should be mounted on the center of the barrier strip or near the most critical thermocouple connection. The output at pin 1 as shown is -10 millivolts per degree Kelvin. Following this the amplifier is utilized to remove the -2.7 volt offset due to ambient temperature and reference the output to 0 millivolts for $0^{o}C$ with +10 millivolts per + degree C and -10 millivolts per -degree C.

The millivolts per degree C can now be scaled by calculating the value of R to produce the correct compensation voltages for the thermocouple utilized. Note that once a thermocouple has been compensated it will remain compensated through the entire gain range with the PG option. (PG = programmable gain).

To calibrate the system place the thermocouple in a beaker of crushed ice and adjust the 20K ohm potentiometer for zero volts out of the system. Now transfer the thermocouple into a known high temperature medium and adjust the fullscale scale of the DT5703-T for the appropriate reading.

APPENDIX C
SP-0023 PROGRAM LISTINGS
SP-0029 PROGRAM LISTINGS

```
                        .LIST   TTM
                        .ENABL  LC
                        .TITLE  DT2760  TST-11 MODULE
                        .IDENT  /V03.01/
000000                  .PSECT  DT2760
                .NLIST  BIN
        ;
        ;
                .SBTTL  GENERAL INFORMATION
        ;
        ;
        ; COPYRIGHT (C) 1979, DATA TRANSLATION INCORPORATED.  ALL
        ; RIGHTS RESERVED.NO PART OF THIS PROGRAM OR PUBLICATION
        ; MAY BE REPRODUCED WITHOUT THE PRIOR WRITTEN PERMISSION
        ; OF  DATA TRANSLATION INCORPORATED,  4 STRATHMORE ROAD,
        ; NATICK, MASS.  01760.
        ;
        ;
        ; THE INFORMATION IN THIS DOCUMENT IS SUBJECT TO CHANGE
        ; WITHOUT  NOTICE  AND  SHOULD  NOT  BE  CONSTRUED AS A
        ; COMMITMENT BY DATA TRANSLATION INCORPORATED.
        ;
        ;
        ; DATA TRANSLATION CANNOT ASSUME ANY RESPONSIBILITY FOR
        ; THE USE OF ANY PORTION OF THIS SOFTWARE FOR OTHER THAN
        ; ITS INTENDED  DIAGNOSTIC  PURPOSE  IN CALIBRATING AND
        ; TESTING  DATA  TRANSLATION  MANUFACTURED  ANALOG  AND
        ; DIGITAL INTERFACE BOARDS.
        ;
        ;
        ;
        ; VERSION V03-01
        ;
        ; EDWIN KROEKER 6-JAN-79
        ; PHILLIP MARTINEZ 17-AUG-79
        ;
        ;
        ; THIS PROGRAM MODULE CONTAINS ROUTINES TO TEST AND
        ; CALIBRATE DTI DT2760 SERIES ANALOG INTERFACE SYSTEMS
        ; FOR THE LSI-11.  A COMPLETE LISTING OF THE MODELS
        ; TESTED BY THIS CODE MODULE WILL BE FOUND ON THE
        ; FOLLOWING PAGES.  THIS MODULE IS DESIGNED TO OPERATE
        ; UNDER TST-11 SUPERVISION.
        ;
```

```
                        .SBTTL  LIST OF CHANGES
                ;
                ;
                ;       DESCRIPTION OF CHANGES:
                ;
                ;       THE DIFFERENCES BETWEEN V02-01 AND V03-01 ARE:
                ;       1).  THE 2765 BOARD TESTS HAVE BEEN TAKEN OUT
                ;       2).  TEST 10 HAS BEEN CHENGED TO ALLOW ODD MUX
                ;            ADDRESSES
                ;       3).  THE TEST NOW COMPUTES ITS OWN TIME DELAY
                ;            FOR DIFFERENT SPEED MODULES
                ;
                ;
                ;
                                .LIST   BIN
```

```
                        .SBTTL  TEST PARAMETER BLOCK (TPB)
                ;
                ; TEST-11 DECLARATION
                ;
                        .MCALL  TST11
000000                  TST11
                ;
                ;
                ; ADDITIONAL PARAMETERS USED BY THIS DIAGNOSTIC
                ;
                ;
        000546  DELAY   =546            ; A/D DELAY COUNT STORAGE
                ;
        000522  ERRCNT  =522            ; ERROR COUNTER
                ;
                ;
                ; TEST PARAMETER BLOCK
                ;
                .NLIST  BIN
        ;
000000  TPB:    .WORD   PARAM           ; ADDRESS OF PARAMETER
                                        ; PRINT-OUT ROUTINE
000002          .BYTE   377             ; RESERVED
000003          .BYTE   12              ; # OF TESTS
        ;
        ; TEST ADDRESS TABLE FOR USE BY TST-11
        ;
000004          .WORD   TEST1,PR7
000010          .WORD   TEST2,PR7
000014          .WORD   TEST3,PR7
000020          .WORD   TEST4,PR7
000024          .WORD   TEST5,PR7
000030          .WORD   TEST6,PR7
000034          .WORD   TEST7,PR7
000040          .WORD   TEST10,0
000044          .WORD   TEST11,0
000050          .WORD   TEST12,0
        ;
                        .LIST   BIN
```

```
                        .SBTTL  INITIALIZATION
                ;
000054  005037  INIT62: CLR     @#SWR           ; INPUT ONLY MODE!
        000540
000060  012737          MOV     #400.,@#DELAY   ; SET DELAY CONSTANT
        000620
        000546
000066  000406          BR      INIT            ; GO TO COMMON INIT.
                ;
000070  012737  INIT64: MOV     #BIT4,@#SWR     ; LOW LEVEL INPUT ONLY
        000020
        000540
000076  012737          MOV     #800.,@#DELAY   ; SET LOW LEVEL DELAY
        001440
        000546
                ;
                ;
000104          INIT:   PRINT   <# OF A/D INPUT CHANNELS (IN OCTAL): >
000154          GETOCT                          ; GET OCTAL INPUT
000156  103352          BCC     INIT            ; NO CR - ASK AGAIN
000160  105737          TSTB    @#ODTACC        ; ZERO?
        000514
000164  001747          BEQ     INIT            ; ASK AGAIN
000166  113737          MOVB    @#ODTACC,@#SWR+1
        000514
        000541
000174  012737          MOV     #177000,@#BASE  ; SET DEFAULT ADDRESS
        177000
        000542
000202  012737          MOV     #130,@#VECTOR   ; SET DEFAULT VECTOR
        000130
        000544
000210  000207          RETURN                  ; ALL DONE
```

NITIALIZATION

```
                        QUERY:  PUSH    R1              ; SAVE POINTER
                                PRINTS                  ; PRINT PROMPT
                                PRINT   < (Y OR N)? >
                                TTYIN
                                CMPB    #'Y,R0          ; A "Y"?
                                BEQ     2$
                                CMPB    #'N,R0          ; A "N"?
                                BEQ     1$              ; YES
                                CRLF
                                PRINTC  <SEE MANUAL FOR ASSISTANCE.>
                                POP     R1              ; RESTORE POINTER
                                BR      QUERY
                        ;
                        1$:     SEC                     ; SET CARRY FLAG
                                BR      3$
                        2$:     CLC                     ; CLEAR CARRY FLAG
                        3$:     TTYOUT                  ; ECHO CHARACTER
                                CRLF
                                POP     R1              ; RESTORE R1
                                RETURN
                        ;
                        ;
                        ;
                        ;
                                .SBTTL  DISPLAY PARAMETERS
                        ;
                        ;       THIS ROUTINE DISPLAYS THE CURRENT SETTING
                        ;       OF 'BASE' AND 'VECTOR' ON THE SYSTEM CONSOLE
                        ;       TERMINAL.
                        ;
                        PARAM:  PRINT   <  BASE ADDRESS = >
                                MOV     @#BASE,R0       ; GET BASE ADDRESS
                                OCT16                   ; DISPLAY
                                CRLF
                                PRINT   <VECTOR ADDRESS = >
                                MOV     @#VECTOR,R0     ; GET VECTOR ADDRESS
                                OCT16                   ; DISPLAY
                                CRLF
                                RETURN                  ; ALL DONE
```

```
                        .SBTTL  ERROR REPORTERS
                ;
                ;
                ; THIS ROUTINE PROVIDES ERROR REPORTING FOR BUS
                ; TIME-OUT ERRORS (NO RPLY FROM INTERFACE).
                ;
000426          NORPLY: PRINT   <NO RPLY WHEN ACCESSING LOCATION >
000472  010100          MOV     R1,R0
000474                  OCT16                   ; DISPLAY ADDRESS
000476                  CRLF
000500  000207          RETURN                  ; DONE
                ;
                ;
                ; THIS ROUTINE PROVIDES ERROR REPORTING FOR REGISTER
                ; BIT ERRORS (ONE OR MORE INCORRECT BITS IN A REGISTER)
                ;
000502          REG:    PRINTC  <REGISTER ERROR>
000524                  PRINT   <ADDRESS: >
000540                  PUSH    R0              ; SAVE R0
000542  010100          MOV     R1,R0           ; GET ADDRESS
000544                  OCT16
000546                  CRLF
000550                  PRINT   <EXPECTED:>
000564  010200          MOV     R2,R0           ; GET EXPECTED VALUE
000566                  OCT16                   ; DISPLAY
000570                  CRLF
000572                  PRINT   <FOUND:    >
000606  011600          MOV     (SP),R0         ; GET BAD BITS
000610  074200          XOR     R2,R0           ; GENERATE SNAPSHOT
000612                  OCT16                   ; DISPLAY
000614                  CRLF                    ; FORMATTING
000616                  PRINT   <BITS:     >
000632                  POP     R0              ; GET ERROR BITS
000634                  OCT16                   ; DISPLAY
000636                  CRLF
000640  000207          RETURN                  ; DONE
```

```
                        .SBTTL  MODEL TESTING INFORMATION
                .NLIST  BIN
        ;
        ; THIS CODE MODULE CONTAINS THE ROUTINES NECESSARY
        ; TO TEST THE FOLLOWING DTI INTERFACE MODELS:
        ;
        ;
        ;
        ;
        ;       DT2762  HIGH LEVEL ANALOG INPUT
        ;
        I2762   ==INIT62
        T2762   ==TPB
        ;
        ;
        ;       DT2764  LOW LEVEL ANALOG INPUT
        ;
        I2764   ==INIT64
        T2764   ==TPB
        ;
        ;
                        .LIST   BIN
                ;
                ;
                ; SOFTWARE SWITCH REGISTER BIT RESERVATIONS
                ;
                ; BITS 13-8:    # OF A/D CHANNELS
                ; BIT 6-5:      UNUSED
                ; BIT 4:        DT5702 A/D MODULE PRESENT
                ; BIT 3:        UNUSED
                ; BITS 2-0:     RESERVED
```

```
                        .SBTTL  LOGIC TESTS
                        .SBTTL  TEST 1:  BRPLY FROM ALL REGISTERS
                ;
                ; THIS TEST VERIFIES THAT THE INTERFACE SYSTEM RESPONDS
                ; WITH A BUS REPLY SIGNAL DURING A BUS DATIO BUS CYCLE
                ; ALL REGISTERS AVAILABLE ON THE BOARD ARE CHECKED.
                ;
                ;
000642  010602  TEST1:  MOV     SP,R2           ; SAVE SP
000644                  RELMOV  #3$,R0          ; SET UP TRAP TO 4
000652  010037          MOV     R0,@#4
        000004
000656  013701  2$:     MOV     @#BASE,R1       ; GET ADDRESS
        000542
000662                  SCOPE                   ; DECLARE LOOP POINT
000664  005011          CLR     (R1)            ; DATIO BUS CYCLE
000666  062701          ADD     #2,R1           ; NEXT REGISTER
        000002
000672                  SCOPE                   ; DECLARE LOOP POINT
000674  005011          CLR     (R1)            ; DATIO BUS CYCLE
000676                  EXIT
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 1 - BUS TIMEOUT
                ;
                ; ********************************************************
                ;
000700  011603  3$:     MOV     (SP),R3         ; GET OFFENDING PC
000702  010206          MOV     R2,SP           ; RESTORE STACK
000704                  ERROR   1,NORPLY        ; REPORT ERROR
000710  000113          JMP     (R3)            ; CONTINUE TEST
```

```
                        .SBTTL  TEST 2:  CHECK ADCSR BITS
                ;
                ; THIS TEST CHECKS MOST OF THE BITS IN ADCSR.
                ; BITS ARE CHECKED FOR BOTH SET AND RESET CAPABILITY
                ; BITS THAT ARE NOT CHECKED ARE THE A/D DONE BIT
                ; AND THE ERROR BIT (BOTH CHECKED IN OTHER TESTS).
                ;
 8 000712 013701 TEST2:  MOV     @#BASE,R1       ; GET ADDRESS
          000542
 9 000716 005002         CLR     R2              ; INIT TEST REG.
10 000720 012703         MOV     #40,R3          ; SET # OF STATES
          000040
11 000724                SCOPE                   ; DECLARE LOOP POINT
12 000726 010211 1$:     MOV     R2,(R1)         ; SET BITS
13 000730 011100         MOV     (R1),R0         ; GET BITS
14 000732 042700         BIC     #177600,R0      ; IGNORE HIGH BYTE
          177600
15 000736 074200         XOR     R2,R0           ; TEST BITS
16 000740 001402         BEQ     2$              ; NO ERROR - SKIP
17                      ;
18                      ; ***************************************************
19                      ;
20                      ;       ERROR CODE 2 - BIT ERROR, ADCSR
21                      ;                       BITS 0-6
22                      ;
23                      ; ***************************************************
24                      ;
25 000742                ERROR   2,REG           ; REPORT ERROR
26                      ;
27 000746 062702 2$:     ADD     #4,R2           ; NEXT STATE
          000004
28 000752 077313         SOB     R3,1$           ; LOOP UNTIL DONE
29 000754 005002         CLR     R2              ; INIT TEST REG.
30 000756 012703         MOV     #200,R3         ; SET # OF STATES
          000200
31 000762                SCOPE                   ; DECLARE LOOP POINT
32 000764 010211 4$:     MOV     R2,(R1)         ; SET BITS
33 000766 011100         MOV     (R1),R0         ; GET BITS
34 000770 042700         BIC     #100377,R0      ; IGNORE LOW BYTE
          100377
35 000774 074200         XOR     R2,R0           ; TEST BITS
36 000776 001402         BEQ     5$              ; NO ERROR - SKIP
37                      ;
38                      ; ***************************************************
39                      ;
40                      ;       ERROR CODE 3 - BIT ERROR, ADCSR
41                      ;                       BITS 8-14
42                      ;
43                      ; ***************************************************
44                      ;
45 001000                ERROR   3,REG           ; REPORT ERROR
46                      ;
47 001004 062702 5$:     ADD     #400,R2         ; NEXT STATE
          000400
48 001010 077313         SOB     R3,4$           ; LOOP UNTIL DONE
49 001012                EXIT
```

```
                        .SBTTL  TEST 3:  BINITL ACTION
                ;
                ; THIS TEST VERIFIES THAT THE BINITL SIGNAL CLEARS
                ; THE PROPER ADCSR BITS.
                ;
                ;
001014  013701  TEST3:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001020  012711          MOV     #40101,(R1)     ; SET BITS
        040101
001024  013700          MOV     @#DELAY,R0      ; WAIT FOR A/D DONE
        000546
001030  077001  2$:     SOB     R0,2$
001032  105211          INCB    (R1)            ; SET ERROR BIT
001034  005002          CLR     R2              ; CLR TEST REG.
001036                  SCOPE                   ; DECLARE LOOP POINT
001040  000005          RESET                   ; ISSUE BINITL
001042  011100          MOV     (R1),R0         ; GET BITS
001044  042700          BIC     #37476,R0       ; IGNORE SOME BITS
        037476
001050  074200          XOR     R2,R0           ; TEST BITS
001052  001402          BEQ     3$              ; OK - SKIP ERROR
                ;
                ; **************************************************
                ;
                ;       ERROR CODE 4 - PROPER BIT(S) NOT CLEARED
                ;                      BY BINITL
                ;
                ; **************************************************
                ;
001054                  ERROR   4,REG           ; REPORT ERROR
                ;
001060          3$:     EXIT                    ; ALL DONE
```

```
                        .SBTTL  TEST 4:  BYTE OPERATION OF ADCSR
                ;
                ; THIS TEST VERIFIES HIGH AND LOW BYTE OPERATIONS
                ; INVOLVING THE ADCSR.
                ;
                ;
001062  013701  TEST4:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001066  005011          CLR     (R1)            ; CLEAR ADCSR
001070  005002          CLR     R2              ; INIT. TEST REGISTER
001072                  SCOPE                   ; DECLARE LOOP POINT
001074  112711          MOVB    #-1,(R1)        ; SET R/W BITS
        177777
001100  011100          MOV     (R1),R0         ; GET ADCSR AS WORD
001102  042700          BIC     #100377,R0      ; IGNORE LOW BYTE
        100377
001106  074200          XOR     R2,R0           ; TEST BITS
001110  001402          BEQ     1$              ; OK - SKIP ERROR
                ;
                ; ***************************************************
                ;
                ;       ERROR CODE 5 - HIGH BYTE LOADED DURING
                ;                       A LOW BYTE OPERATION
                ;
                ; ***************************************************
                ;
001112                  ERROR   5,REG           ; REPORT ERROR
                ;
001116  005011  1$:     CLR     (R1)            ; CLEAR ADCSR
001120  005002          CLR     R2              ; INIT. TEST REGISTER
001122  005201          INC     R1              ; POINT TO HIGH BYTE
001124                  SCOPE                   ; DECLARE LOOP POINT
001126  112711          MOVB    #-1,(R1)        ; SET R/W BITS
        177777
001132  016100          MOV     -1(R1),R0       ; GET ADCSR AS WORD
        177777
001136  042700          BIC     #177600,R0      ; IGNORE HIGH BYTE
        177600
001142  074200          XOR     R2,R0           ; TEST BITS
001144  001402          BEQ     2$              ; OK - SKIP ERROR
                ;
                ; ***************************************************
                ;
                ;       ERROR CODE 6 - LOW BYTE LOADED DURING
                ;                       A HIGH BYTE OPERATION
                ;
                ; ***************************************************
                ;
001146                  ERROR   6,REG           ; REPORT ERROR
                ;
001152          2$:     EXIT
```

```
                        .SBTTL  TEST 5:  A/D DONE BIT AND INTERRUPT
                ;
                ; THIS TEST VERIFIES THAT THE A/D DONE BIT CAN
                ; BE SET PROPERLY AND THAT THE INT ENB BIT
                ; FUNCTIONS PROPERLY.
                ;
                ;
001154  013701  TEST5:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001160  013702          MOV     @#VECTOR,R2     ; GET VECTOR ADDRESS
        000544
001164  005761          TST     2(R1)           ; CLEAR A/D DONE BIT
        000002
001170  005011          CLR     (R1)            ; CLEAR ADCSR
001172                  SCOPE                   ; DECLARE LOOP POINT
001174  105211          INCB    (R1)            ; SET A/D DONE BIT
001176  013700          MOV     @#DELAY,R0      ; WAIT FOR A/D DONE
        000546
001202  077001  1$:     SOB     R0,1$
001204  105711          TSTB    (R1)            ; IS BIT SET?
001206  100402          BMI     2$              ; YES - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 7 - A/D DONE BIT NOT SET
                ;
                ; ********************************************************
                ;
001210                  ERROR   7               ; REPORT ERROR
001212  000460          BR      8$              ; CAN'T CONTINUE
                ;
001214          2$:     SCOPE                   ; DECLARE LOOP POINT
001216  005761          TST     2(R1)           ; READ ADDBR
        000002
001222  105711          TSTB    (R1)            ; DONE BIT CLEAR?
001224  100002          BPL     3$              ; YES - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 10 - A/D DONE BIT NOT CLEARED
                ;                       AFTER A/D DATA WAS READ
                ;
                ; ********************************************************
                ;
001226                  ERROR   10              ; REPORT ERROR
001230  000451          BR      8$              ; CAN'T CONTINUE
```

TEST 5: A/D DONE BIT AND INTERRUPT

```
 1 001232  005003  3$:     CLR     R3              ; PREPARE STATUS WORDS
 2 001234  012704          MOV     #PR7,R4
           000340
 3 001240                  RELMOV  #5$,R0          ; GET ISR ADDRESS
 4 001246  010012          MOV     R0,(R2)         ; STORE
 5 001250  010462          MOV     R4,2(R2)        ; STORE STATUS TOO
           000002
 6 001254                  SCOPE                   ; DECLARE LOOP POINT
 7 001256  105211          INCB    (R1)            ; SET A/D DONE
 8 001260  013700          MOV     @#DELAY,R0      ; WAIT FOR DONE
           000546
 9 001264  077001  4$:     SOB     R0,4$
10 001266  052711          BIS     #100,(R1)       ; ENABLE INTERRUPTS
           000100
11 001272  106403          MTPS    R3              ; ENABLE CPU INTERRUPTS
12 001274  000240          NOP                     ; STALL TIME
13 001276  106404          MTPS    R4              ; TURN OFF CPU
14                 ;
15                 ; ***************************************************
16                 ;
17                 ;       ERROR CODE 11 - NO INTERRUPT ON A/D DONE
18                 ;
19                 ; ***************************************************
20                 ;
21 001300                  ERROR   11              ; REPORT ERROR
22 001302  000424          BR      8$              ; CAN'T CONTINUE
23                 ;
24 001304  062706  5$:     ADD     #4,SP           ; ADJUST STACK
           000004
25 001310                  SCOPE                   ; DECLARE LOOP POINT
26 001312  005761          TST     2(R1)           ; READ ADDBR
           000002
27 001316  105711          TSTB    (R1)            ; A/D DONE CLEAR?
28 001320  100002          BPL     6$              ; YES - EXIT
29                 ;
30                 ; ***************************************************
31                 ;
32                 ;       ERROR CODE 12 - A/D DONE BIT NOT CLEARED
33                 ;                       AFTER A/D DATA WAS READ
34                 ;
35                 ; ***************************************************
36                 ;
37 001322                  ERROR   12              ; REPORT ERROR
38 001324  000413          BR      8$              ; CAN'T CONTINUE
```

```
                        6$:     SCOPE                   ; DECLARE LOOP POINT
001330  005761 000002          TST     2(R1)           ; CLEAR DONE
001334  005011                 CLR     (R1)            ; CLEAR ADCSR
001336  005211                 INC     (R1)            ; START CONVERSION
001340  013700 000546          MOV     @#DELAY,R0      ; WAIT -
001344  077001          7$:     SOB     R0,7$
001346  005711                 TST     (R1)            ; ERROR BIT SET?
001350  100001                 BPL     8$              ; NO - EXIT
                        ;
                        ; ***********************************************
                        ;
                        ;       ERROR CODE 13 - ERROR BIT SET AFTER NORMAL
                        ;                       A/D TRIGGERING SEQUENCE
                        ;
                        ; ***********************************************
                        ;
001352                          ERROR   13              ; REPORT ERROR
                        ;
001354  005761 000002   8$:     TST     2(R1)           ; CLEAR DONE
001360  005011                 CLR     (R1)
001362  005000                 CLR     R0              ; INITIALIZE COUNTER
001364  105211                 INCB    (R1)            ; START CONVERSION
001366  005200          9$:     INC     R0              ; BUMP COUNTER
001370  105711                 TSTB    (R1)            ; WAIT FOR DONE
001372  100375                 BPL     9$
001374  006300                 ASL     R0              ; FORM NEW DELAY
001376  006300                 ASL     R0
001400  006300                 ASL     R0
001402  010037 000546          MOV     R0,@#DELAY      ; STORE NEW DELAY
001406  005761 000002          TST     2(R1)           ; CLEAR DONE
001412  005011                 CLR     (R1)
001414                          EXIT
```

```
                        .SBTTL  TEST 6:  ERROR BIT AND INTERRUPT
                ;
                ; THIS TEST VERIFIES THAT THE ERROR BIT CAN BE SET
                ; PROPERLY AND THAT THE ERR INT ENB BIT FUNCTIONS
                ; CORRECTLY.
                ;
                ;
001416  013701  TEST6:  MOV     @#BASE,R1       ; GET ADDRESS
        000542
001422  013702          MOV     @#VECTOR,R2     ; GET VECTOR ADDRESS
        000544
001426  062702          ADD     #4,R2           ; ADJUST VECTOR
        000004
001432  005761          TST     2(R1)           ; CLEAR A/D DONE BIT
        000002
001436                  SCOPE                   ; DECLARE LOOP POINT
001440  005011          CLR     (R1)            ; CLEAR ADCSR
001442  005711          TST     (R1)            ; ERROR CLEAR?
001444  100002          BPL     1$              ; YES - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 14 - ERROR BIT NOT CLEAR
                ;
                ; ********************************************************
                ;
001446                  ERROR   14              ; REPORT ERROR
001450  000442          BR      5$              ; CAN'T CONTINUE
                ;
001452          1$:     SCOPE                   ; DECLARE LOOP POINT
001454  105211          INCB    (R1)            ; SET A/D DONE BIT
001456  013700          MOV     @#DELAY,R0      ; WAIT FOR A/D DONE
        000546
001462  077001  2$:     SOB     R0,2$
001464  105211          INCB    (R1)            ; SET ERROR BIT
001466  005711          TST     (R1)            ; IS BIT SET?
001470  100402          BMI     3$              ; YES - SKIP ERROR
                ;
                ; ********************************************************
                ;
                ;       ERROR CODE 15 - ERROR BIT NOT SET
                ;
                ; ********************************************************
                ;
001472                  ERROR   15              ; REPORT ERROR
001474  000430          BR      5$              ; CAN'T CONTINUE
```

```
    1 001476  005003  3$:     CLR     R3                  ; PREPARE STATUS WORDS
    2 001500  012704          MOV     #PR7,R4
              000340
    3 001504                  RELMOV  #4$,R0              ; GET ISR ADDRESS
    4 001512  010012          MOV     R0,(R2)             ; STORE
    5 001514  010462          MOV     R4,2(R2)            ; STORE STATUS TOO
              000002
    6 001520                  SCOPE                       ; DECLARE LOOP POINT
    7 001522  052711          BIS     #40000,(R1)         ; ENABLE INTERRUPTS
              040000
    8 001526  106403          MTPS    R3                  ; ENABLE CPU INTERRUPTS
    9 001530  000240          NOP                         ; STALL TIME
   10 001532  106404          MTPS    R4                  ; TURN OFF CPU
   11                     ;
   12                     ; ***************************************************
   13                     ;
   14                     ;       ERROR CODE 16 - NO INTERRUPT ON ERROR
   15                     ;
   16                     ; ***************************************************
   17                     ;
   18 001534                  ERROR   16                  ; REPORT ERROR
   19 001536  000407          BR      5$                  ; CAN'T CONTINUE
   20                     ;
   21 001540  062706  4$:     ADD     #4,SP               ; ADJUST STACK
              000004
   22 001544                  SCOPE                       ; DECLARE LOOP POINT
   23 001546  005011          CLR     (R1)                ; CLEAR ERROR BIT
   24 001550  005711          TST     (R1)                ; CHECK BIT
   25 001552  100001          BPL     5$                  ; CLEAR - SKIP ERROR
   26                     ;
   27                     ; ***************************************************
   28                     ;
   29                     ;       ERROR CODE 17 - ERROR BIT NOT CLEAR
   30                     ;
   31                     ; ***************************************************
   32                     ;
   33 001554                  ERROR   17                  ; REPORT ERROR
   34                     ;
   35 001556  005761  5$:     TST     2(R1)               ; CLEAR DONE
              000002
   36 001562  005011          CLR     (R1)                ; CLEAR ADCSR
   37 001564                  EXIT
```

```
                        .SBTTL  TEST 7:  END OF LOGIC TESTS
                ;
                ; THIS TEST IS PRESENT TO INFORM THE TST-11 MONITOR
                ; THAT THERE ARE NO MORE ADDITIONAL LOGIC TESTS
                ; TO BE EXECUTED.  WHEN THE "ALL" COMMAND IS USED,
                ; THIS TEST WILL FORCE A RETURN TO THE COMMAND
                ; LEVEL OF TST-11 WHEN THE TEST SEQUENCER REACHES
                ; THIS TEST.
                ;
                ;
001566          TEST7:  ESCAPE
                ;
                ;
                        .SBTTL  CALIBRATION INITIALIZATION
                ;
                ; THIS ROUTINE PERFORMS INITIALIZATION FUNCTIONS
                ; FOR SOME OF THE CALIBRATION TESTS.
                ;
                ;
001570          GETCH:  PRINT   <CHANNEL? >             ; OUTPUT PROMPT
001604                  GETOCT                          ; GET VALUE
001606  103422          BCS     1$                      ; CR AT END - CONT.
001610                  PRINTC  <ENTER AN OCTAL CHANNEL ADDRESS.>
001652  000746          BR      GETCH                   ; TRY AGAIN
                ;
001654  013701  1$:     MOV     @#BASE,R1               ; GET ADDRESS
        000542
001660  013702          MOV     @#ODTACC,R2             ; GET VALUE
        000514
001664  000302          SWAB    R2                      ; ADJUST
001666          2$:     PRINT   <MODE BITS? >           ; OUTPUT PROMPT
001704                  GETOCT                          ; GET VALUE
001706  103420          BCS     3$                      ; CR AT END - CONT.
001710                  PRINTC  <ENTER AN OCTAL BYTE VALUE.>
001746  000747          BR      2$
                ;
001750  042702  3$:     BIC     #377,R2                 ; CLEAR LOW BYTE,R2
        000377
001754  013700          MOV     @#ODTACC,R0             ; GET VALUE
        000514
001760  042700          BIC     #177400,R0              ; CLEAR HIGH BYTE,R0
        177400
001764  060002          ADD     R0,R2                   ; ADD IN MODE BYTE
001766  005761          TST     2(R1)                   ; CLEAR DONE
        000002
001772  005011          CLR     (R1)                    ; CLEAR BOARD
001774  000207          RETURN
```

```
                        .SBTTL  DISPLAY A/D DATA
                ;
                ; THIS ROUTINE TAKES THE DATA FROM ADDBR AND DISPLAYS
                ; IT FOR THE USER AS A 16 BIT OCTAL VALUE.
                ;
001776 016100   DISPLY: MOV     2(R1),R0        ; GET DATA
       000002
002002                  OCT16                   ; PRINT
002004 005711           TST     (R1)            ; ERROR BIT SET?
002006 100015           BPL     1$              ; NO - RETURN
002010 112700           MOVB    #'E,R0          ; PRINT 'E'
       000105
002014                  TTYOUT
002016 042711           BIC     #40000,(R1)     ; CLEAR ERROR BIT
       040000
002022 005237           INC     @#ERRCNT        ; INC. COUNT
       000522
002026 005737           TST     @#ERRCNT        ; OVERFLOW?
       000522
002032 001003           BNE     1$              ; NO - SKIP
002034 012737           MOV     #-1,@#ERRCNT    ; YES - FORCE VALUE
       177777
       000522
002042 000207   1$:     RETURN
                ;
                ;
                        .SBTTL  TEST 10: A/D CALIBRATION
                ;
                ; THIS TEST ACCEPTS A CHANNEL ADDRESS FROM THE USER
                ; AND DISPLAYS THE DATA FROM THAT CHANNEL CONTINUOUSLY
                ;
                ;
002044          TEST10: PRINTC  <A/D CALIBRATION>
002066 004767           CALL    GETCH           ; GET CHANNEL ADDRESS
       177476
002072                  KBEXIT                  ; SET UP KEYBOARD
002074 042702           BIC     #140303,R2      ; CLEAR SOME BITS
       140303
002100 032702           BIT     #60,R2          ; EXTERNAL?
       000060
002104 001002           BNE     1$              ; YES - NO START BIT
002106 052702           BIS     #1,R2           ; SET START BIT
       000001
002112 112704   1$:     MOVB    #10,R4          ; LINE COUNTER
       000010
002116                  CRLF
002120 010211   2$:     MOV     R2,(R1)         ; START CONVERSION
002122 105711   3$:     TSTB    (R1)            ; WAIT FOR DONE
002124 100376           BPL     3$
002126 004767           CALL    DISPLY          ; DISPLAY DATA
       177644
002132 105304           DECB    R4              ; LINE OVER?
002134 001766           BEQ     1$              ; YES - NEW LINE
002136                  TAB
002140 000767           BR      2$              ; NEXT CONVERSION
```

```
                        .SBTTL  TEST 11: A/D INPUT CHANNEL SCAN
                ;
                ; THIS TEST SCANS THE INPUT CHANNELS WHILE
                ; DISPLAYING THE A/D DATA ON THE TERMINAL
                ;
                ;
002142          TEST11: PRINTC  <A/D INPUT CHANNEL SCAN>
002174                  KBEXIT                          ; SET UP KEYBOARD
002176  013701                  MOV     @#BASE,R1       ; GET ADDRESS
        000542
002202  005761                  TST     2(R1)           ; CLEAR DONE
        000002
002206  005011                  CLR     (R1)            ; CLEAR CSR
002210  005002                  CLR     R2              ; INIT. CHANNEL COUNT
002212          1$:     CRLF
002214  112703                  MOVB    #10,R3          ; LINE COUNTER
        000010
002220                  PRINT   <CH=>                   ; DISPLAY ADDRESS
002226  010200                  MOV     R2,R0
002230                  OCT8
002232  010200                  MOV     R2,R0           ; GET CHANNEL ADDRESS
002234  000300                  SWAB    R0              ; PUT IN HIGH BYTE
002236  010011                  MOV     R0,(R1)         ; SET UP CHANNEL
002240  105211  2$:     INCB    (R1)                    ; TRIGGER CONVERTER
002242  105711  3$:     TSTB    (R1)                    ; WAIT FOR DONE
002244  100376                  BPL     3$
002246                  TAB
002250  004767                  CALL    DISPLY          ; DISPLAY DATA
        177522
002254  105303                  DECB    R3              ; LINE DONE?
002256  001370                  BNE     2$              ; NO - CONTINUE
002260  005202                  INC     R2              ; INC. CHANNEL
002262  123702                  CMPB    @#SWR+1,R2      ; END OF RANGE?
        000541
002266  001351                  BNE     1$              ; NO - CONTINUE
002270  005002                  CLR     R2              ; YES
002272                  CRLF
002274  000746                  BR      1$
```

```
                        .SBTTL  TEST 12: A/D INPUT GAIN/CHANNEL SCAN
                ;
                ; THIS TEST SCANS THE INPUT CHANNELS WHILE
                ; CHANGING THE GAIN OF THE CONVERTER.  THE
                ; A/D DATA IS DISPLAYED ON THE TERMINAL.
                ;
                ;
002276          TEST12: PRINTC  <A/D INPUT GAIN/CHANNEL SCAN>
002334                  KBEXIT                          ; SET UP KEYBOARD
002336  013701          MOV     @#BASE,R1               ; GET ADDRESS
        000542
002342  005761          TST     2(R1)                   ; CLEAR DONE
        000002
002346  005011          CLR     (R1)                    ; CLEAR CSR
002350  005002          CLR     R2                      ; INIT. CHANNEL COUNT
002352  005003          CLR     R3                      ; INIT. GAIN
002354          1$:     CRLF
002356  112704          MOVB    #7,R4                   ; LINE COUNTER
        000007
002362                  PRINT   <CH=>                   ; DISPLAY ADDRESS
002370  010200          MOV     R2,R0
002372                  OCT8
002374  112700          MOVB    #',,R0                  ; DISPLAY GAIN
        000054
002400                  TTYOUT
002402  112700          MOVB    #'0,R0
        000060
002406  032703          BIT     #10,R3                  ; GS1 SET?
        000010
002412  001401          BEQ     2$                      ; NO - SKIP
002414  105200          INCB    R0
002416          2$:     TTYOUT                          ; DISPLAY BIT
002420  112700          MOVB    #'0,R0
        000060
002424  032703          BIT     #4,R3                   ; GS0 SET?
        000004
002430  001401          BEQ     3$                      ; NO - SKIP
002432  105200          INCB    R0
002434          3$:     TTYOUT                          ; DISPLAY BIT
```

```
    1 002436  010200          MOV     R2,R0           ; GET CHANNEL ADDRESS
    2 002440  000300          SWAB    R0              ; PUT IN HIGH BYTE
    3 002442  050300          BIS     R3,R0           ; SET GAIN BITS
    4 002444  010011          MOV     R0,(R1)         ; SET UP CHANNEL
    5 002446  105211  4$:     INCB    (R1)            ; TRIGGER CONVERTER
    6 002450  105711  5$:     TSTB    (R1)            ; WAIT FOR DONE
    7 002452  100376          BPL     5$
    8 002454                  TAB
    9 002456  004767          CALL    DISPLY          ; DISPLAY DATA
              177314
   10 002462  105304          DECB    R4              ; LINE DONE?
   11 002464  001370          BNE     4$              ; NO - CONTINUE
   12 002466  005202          INC     R2              ; INC. CHANNEL
   13 002470  062703          ADD     #4,R3           ; INCREMENT GAIN
              000004
   14 002474  042703          BIC     #177763,R3      ; CLEAR EXTRA BITS
              177763
   15 002500  123702          CMPB    @#SWR+1,R2      ; END OF RANGE?
              000541
   16 002504  001323          BNE     1$              ; NO - CONTINUE
   17 002506  005002          CLR     R2              ; YES
   18 002510                  CRLF
   19 002512  000720          BR      1$
   20
   21         000001          .END
```

```
DT:760  TST-11 MODULE   MACRO V03.0B     31-AUG-79 03:27:32 PAGE 21-1
SYMBOL TABLE

BA:E   = 000542          ERRNUM= 000521          SWR    = 000540
BIT0   = 000001          FF     = 000014          TEST1   000642R      002
BIT1   = 000002          GETCH   001570R      002 TEST10  002044R      002
BIT10  = 002000          HLTERR= 000004          TEST11  002142R      002
BIT11  = 004000          INHERR= 000100          TEST12  002276R      002
BIT12  = 010000          INIT    000104R      002 TEST2   000712R      002
BIT13  = 020000          INIT62  000054R      002 TEST3   001014R      002
BIT14  = 040000          INIT64  000070R      002 TEST4   001062R      002
BIT15  = 100000          I2762 = 000054RG     002 TEST5   001154R      002
BIT2   = 000004          I2764 = 000070RG     002 TEST6   001416R      002
BIT3   = 000010          LF     = 000012          TEST7   001566R      002
BIT4   = 000020          LPERR = 000002          TPB     0000000R     002
BIT5   = 000040          LPTST = 000001          TSTALL= 000010
BIT6   = 000100          NEWFLG= 010000          TSTCSR= 000500
BIT7   = 000200          NORPLY  000426R      002 TSTNUM= 000520
BIT8   = 000400          ODTACC= 000514          TSTONE= 000040
BIT9   = 001000          PARAM   000334R      002 TSTSEQ= 000020
CR     = 000015          PR7    = 000340          T2762 = 000000RG     002
CTRLC  = 000003          QUERY   000212R      002 T2764 = 000000RG     002
CTRLI  = 000011          RBUF   = 177562          VECTOR= 000544
DELAY  = 000546          RCSR   = 177560          XBUF   = 177566
DISPLY  001776R      002 REG     000502R      002 XCSR   = 177564
ERRCNT= 000522           SPACE = 000040

  ABS.   000000      000
         000000      001
ODT2760  002514      002
ERRORS DETECTED:  0

VIRTUAL MEMORY USED:  2128 WORDS  ( 9 PAGES)
DYNAMIC MEMORY AVAILABLE FOR  67 PAGES
.DO 1:2760.=DX0:TST11.ML/M,DX1:2760.V01
```

```
RT-11 LINK  V05.04A      LOAD MAP          FRI 31-AUG-79 13:56:16
SP0023.LDA       TITLE:  SP0023  IDENT:  V03.01

SECTION  ADDR    SIZE     GLOBAL  VALUE    GLOBAL  VALUE    GLOBAL  VALUE

  ABS.   000000  001000    (RW,I,GBL,ABS,OVR)
SP0023   001000  000060    (RW,I,LCL,REL,CON)
                          DIRECT  001000
OT2760   001060  002514    (RW,I,LCL,REL,CON)
                          T2762   001060  T2764   001060  I2762   001134
                          I2764   001150
OT2769   003574  003342    (RW,I,LCL,REL,CON)
                          T2769   003574  I2769   003740
TST11    007136  006434    (RW,I,LCL,REL,CON)
                          START   007136

TRANSFER ADDRESS = 007136, HIGH LIMIT = 015572 =  3517. WORDS
```

```
T-11 LINK  V05.04A      Load Map        Thu 16-Aug-79 14:05:27
P0029.LDA       Title:  TST11   Ident:  V02.06

Section  Addr    Size    Global  Value   Global  Value   Global  Value

. ABS.   000000  001000    (RW,I,GBL,ABS,OVR)
TST11    001000  006434    (RW,I,LCL,REL,CON)
                         START   001000
 P0029   007434  000040    (RW,I,LCL,REL,CON)
                         DIRECT  007434
 T2765   007474  002234    (RW,I,LCL,REL,CON)
                         T2765   007474  I2765   007544

Transfer address = 001000, High limit = 011730 =  2540. words
```

TABLE OF CONTENTS

```
                        .LIST   TTM
                        .ENABL  LC
                        .TITLE  DT2765  TST-11 module
                        .IDENT  /V01.02/
000000                  .PSECT  DT2765
                .NLIST  BIN
        ;
        ;
                .SBTTL  General Information
        ;
        ;
        ; Copyright (C) 1979, Data Translation Incorporated. All
        ; rights reserved.No part of this program or publication
        ; may be reproduced without the prior written permission
        ; of  Data Translation Incorporated,  4 Strathmore Road,
        ; Natick, Mass. 01760.
        ;
        ;
        ; The information in this document is subject to change
        ; without  notice  and  should  not  be  construed as a
        ; commitment by Data Translation Incorporated.
        ;
        ;
        ; Data Translation cannot assume any responsibility for
        ; the use of any portion of this software for other than
        ; its intended  diagnostic  purpose  in calibrating and
        ; testing  Data  Translation  manufactured  analog  and
        ; digital interface boards.
        ;
        ;
        ;
        ; Version 01-02
        ;
        ; Phillip Martinez 19-Apr-79
        ; Edwin Kroeker 6-Jan-79
        ; Phillip Martinez  16-Aug-79
        ;
        ;
        ; This program module contains routines to test and
        ; calibrate DTI DT2765 series analog interface systems
        ; for the LSI-11. A complete listing of the models
        ; tested by this code module will be found on the
        ; following pages. This module is designed to operate
        ; under TST-11 supervision.
        ;
```

```
1           ;
2           ;
3           ;       The differences between V01-01 and V01-02
4           ;       are as follows.
5           ;       1). test 7 now supports even and odd
6           ;           mux addresses.
7           ;       2). general cleanup of various small
8           ;           inconsistent coding sequences.
9                       .LIST   BIN
```

```
                                .SBTTL  Test Parameter Block (TPB)
                        ;
                        ; Test-11 Declaration
                        ;
                                .NCALL  TST11
000000                          TST11
                        ;
                        ;
                        ; Additional parameters used by this diagnostic
                        ;
                        ;
000546          DELAY   =546                    ; A/D delay count storage
                        ;
000522          ERRCNT  =522                    ; error counter
                        ;
                        ;
                        ; Test Parameter Block
                        ;
                        .NLIST  BIN
                ;
000000  TPB:    .WORD   PARAM                   ; address of parameter
                                                ; print-out routine
000002          .BYTE   377                     ; reserved
000003          .BYTE   11                      ; # of tests
                ;
                ; Test Address Table for use by TST-11
                ;
000004          .WORD   TEST1,PR7
000010          .WORD   TEST2,PR7
000014          .WORD   TEST3,PR7
000020          .WORD   TEST4,PR7
000024          .WORD   TEST5,PR7
000030          .WORD   TEST6,PR7
000034          .WORD   TEST7,0
000040          .WORD   TEST10,0
000044          .WORD   TEST11,0
                ;
                                .LIST   BIN
```

```
                        .SBTTL  Initialization
                ;
                ;
000050  012737  INIT65: MOV     #BIT3,@#SWR     ; isolated module
        000010
        000540
000056  012737          MOV     #21000.,@#DELAY ; big delay
        051010
        000546
                ;
000064          INIT:   PRINT   <# of A/D input channels (in octal): >
000134                  GETOCT                  ; get octal input
000136  103352          BCC     INIT            ; no CR - ask again
000140  105737          TSTB    @#ODTACC        ; zero?
        000514
000144  001747          BEQ     INIT            ; ask again
000146  113737          MOVB    @#ODTACC,@#SWR+1
        000514
        000541
000154  012737          MOV     #177000,@#BASE  ; set default address
        177000
        000542
000162  012737          MOV     #130,@#VECTOR   ; set default vector
        000130
        000544
000170  000207          RETURN                  ; all done
```

```
 1
 2
 3                              .SBTTL  Display Parameters
 4                      ;
 5                      ;       This routine displays the current setting
 6                      ;       of 'BASE' and 'VECTOR' on the system console
 7                      ;       terminal.
 8 000172               ;
 9 000216  013700       PARAM:  PRINT   <Base address =   >
           000542               MOV     @#BASE,R0       ; get base address
10 000222                       OCT16                   ; display
11 000224                       CRLF
12 000226                       PRINT   <Vector address = >
13 000252  013700               MOV     @#VECTOR,R0     ; get vector address
           000544
14 000256                       OCT16                   ; display
15 000260                       CRLF
16 000262  000207               RETURN                  ; all done
```

```
                        .SBTTL  Error reporters
                ;
                ;
                ; This routine provides error reporting for bus
                ; time-out errors (no BRPLY from interface).
                ;
000264          NORPLY: PRINT   <No BRPLY when accessing location >
000330  010100          MOV     R1,R0
000332                  OCT16                   ; display address
000334                  CRLF
000336  000207          RETURN                  ; done
                ;
                ;
                ; This routine provides error reporting for register
                ; bit errors (one or more incorrect bits in a register).
                ;
000340          REG:    PRINTC  <Register Error>
000362                  PRINT   <Address: >
000376                  PUSH    R0              ; save R0
000400  010100          MOV     R1,R0           ; get address
000402                  OCT16
000404                  CRLF
000406                  PRINT   <Expected:>
000422  010200          MOV     R2,R0           ; get expected value
000424                  OCT16                   ; display
000426                  CRLF
000430                  PRINT   <Found:    >
000444  011600          MOV     (SP),R0         ; get bad bits
000446  074200          XOR     R2,R0           ; generate snapshot
000450                  OCT16                   ; display
000452                  CRLF                    ; formatting
000454                  PRINT   <Bits:     >
000470                  POP     R0              ; get error bits
000472                  OCT16                   ; display
000474                  CRLF
000476  000207          RETURN                  ; done
                ;
                ;  This routine provides for house keeping upon
                ;  leaving a routine.
                ;
000500  013700  WAIT:   MOV     @#DELAY,R0
        000546
000504  077001  1$:     SOB     R0,1$
000506  005761          TST     2(R1)
        000002
000512  000207          RETURN
```

```
                        .SBTTL  Model testing information
                .NLIST  BIN
        ;
        ; This code module contains the routines necessary
        ; to test the following DTI interface models:
        ;
        ;
        ;
        ;               DT2765  Isolated wide range input
        ;
        I2765   ==INIT65
        T2765   ==TPB
        ;
                        .LIST   BIN
                ;
                ;
                ; Software switch register bit reservations
                ;
                ; bits 13-8:    # of A/D channels
                ; bit 6:        DT5710 A/D module present
                ; bit 5:        DT5701 A/D module present
                ; bit 4:        DT5702 A/D module present
                ; bit 3:        DT5703 A/D module present
                ; bits 2-0:     reserved
```

```
                        .SBTTL  Logic Tests
                        .SBTTL  Test 1:  BRPLY from all registers
                ;
                ; This test verifies that the interface system responds
                ; with a bus reply signal during a bus DATIO bus cycle.
                ; All registers available on the board are checked.
                ;
                ;
000514  010602  TEST1:  MOV     SP,R2           ; save SP
000516          RELMOV  #3$,R0          ; set up trap to 4
000524  010037          MOV     R0,@#4
        000004
000530  013701  2$:     MOV     @#BASE,R1       ; get address
        000542
000534          SCOPE                           ; declare loop point
000536  105011          CLRB    (R1)            ; DATIO bus cycle
000540  062701          ADD     #2,R1           ; next register
        000002
000544          SCOPE                           ; declare loop point
000546  005011          CLR     (R1)            ; DATIO bus cycle
000550  004767          CALL    WAIT
        177724
000554          EXIT
                ;
                ; ************************************************
                ;
                ;       Error Code 1 - Bus timeout
                ;
                ; ************************************************
                ;
000556  011603  3$:     MOV     (SP),R3         ; get offending PC
000560  010206          MOV     R2,SP           ; restore stack
000562          ERROR   1,NORPLY        ; report error
000566  000113          JMP     (R3)            ; continue test
```

```
                        .SBTTL  Test 2:  check ADCSR bits
                ;
                ; This test checks most of the bits in ADCSR.
                ; Bits are checked for both set and reset capability.
                ; Bits that are NOT checked are the A/D DONE bit
                ; and the ERROR bit (both checked in other tests).
                ;
000570  013701  TEST2:  MOV     @#BASE,R1       ; get address
        000542
000574  005002          CLR     R2              ; init test reg.
000576  012703          MOV     #40,R3          ; set # of states
        000040
000602                  SCOPE                   ; declare loop point
000604  110211  1$:     MOVB    R2,(R1)         ; set bits
000606  011100          MOV     (R1),R0         ; get bits
000610  042700          BIC     #177600,R0      ; ignore high byte
        177600
000614  074200          XOR     R2,R0           ; test bits
000616  001402          BEQ     2$              ; no error - skip
                ;
                ; ************************************************
                ;
                ;       Error Code 2 - bit error, ADCSR
                ;                      bits 0-6
                ;
                ; ************************************************
                ;
000620                  ERROR   2,REG           ; report error
000624  062702  2$:     ADD     #4,R2           ; next state
        000004
000630  077313          SOB     R3,1$           ; loop until done
000632  005002          CLR     R2              ; init test reg.
000634  012703          MOV     #200,R3         ; set # of states
        000200
000640                  SCOPE                   ; declare loop point
000642  010211  4$:     MOV     R2,(R1)         ; set bits
000644  011100          MOV     (R1),R0         ; get bits
000646  042700          BIC     #100377,R0      ; ignore low byte
        100377
000652  074200          XOR     R2,R0           ; test bits
000654  001402          BEQ     5$              ; no error - skip
                ;
                ; ************************************************
                ;
                ;       Error Code 3 - bit error, ADCSR
                ;                      bits 8-14
                ;
                ; ************************************************
                ;
000656                  ERROR   3,REG           ; report error
000662  062702  5$:     ADD     #400,R2         ; next state
        000400
000666  077313          SOB     R3,4$           ; loop until done
000670  004767          CALL    WAIT
        177604
000674                  EXIT
```

```
                        .SBTTL  Test 3:  BINITL action

                        ;
                        ; This test verifies that the BINITL signal clears
                        ; the proper ADCSR bits.
                        ;
                        ;
000676  013701  TEST3:  MOV     @#BASE,R1       ; get address
        000542
000702  012711          MOV     #40100,(R1)     ; set bits
        040100
000706  013700          MOV     @#DELAY,R0      ; wait for A/D DONE
        000546
000712  077001  2$:     SOB     R0,2$
000714  052711          BIS     #0,(R1)         ; set error bit
        000000
000720  005002          CLR     R2              ; clr test reg.
000722                  SCOPE                   ; declare loop point
000724  000005          RESET                   ; issue BINITL
000726  011100          MOV     (R1),R0         ; get bits
000730  042700          BIC     #37476,R0       ; ignore some bits
        037476
000734  074200          XOR     R2,R0           ; test bits
000736  001402          BEQ     3$              ; OK - skip error
                        ;
                        ; ************************************************
                        ;
                        ;       Error Code 4 - proper bit(s) not cleared
                        ;                      by BINITL
                        ;
                        ; ************************************************
                        ;
000740                  ERROR   4,REG           ; report error
                        ;
000744  004767  3$:     CALL    WAIT                    ; all done
        177530
000750                  EXIT
```

```
                        .SBTTL  Test 4:  byte operation of ADCSR
                ;
                ; This test verifies high and low byte operations
                ; involving the ADCSR.
                ;
                ;
000752  013701  TEST4:  MOV     @#BASE,R1       ; get address
        000542
000756  105011          CLRB    (R1)            ; clear ADCSR
000760  005002          CLR     R2              ; init. test register
000762                  SCOPE                   ; declare loop point
000764  112711          MOVB    #-1,(R1)        ; set R/W bits
        177777
000770  011100          MOV     (R1),R0         ; get ADCSR as word
000772  042700          BIC     #100377,R0      ; ignore low byte
        100377
000776  074200          XOR     R2,R0           ; test bits
001000  001402          BEQ     1$              ; ok - skip error
                ;
                ; ************************************************
                ;
                ;       Error Code 5 - high byte loaded during
                ;                           a low byte operation
                ;
                ; ************************************************
                ;
001002                  ERROR   5,REG           ; report error
                ;
001006  105011  1$:     CLRB    (R1)            ; clear ADCSR
001010  005002          CLR     R2              ; init. test register
001012  005201          INC     R1              ; point to high byte
001014                  SCOPE                   ; declare loop point
001016  112711          MOVB    #-1,(R1)        ; set R/W bits
        177777
001022  016100          MOV     -1(R1),R0       ; get ADCSR as word
        177777
001026  042700          BIC     #177600,R0      ; ignore high byte
        177600
001032  074200          XOR     R2,R0           ; test bits
001034  001402          BEQ     2$              ; ok - skip error
                ;
                ; ************************************************
                ;
                ;       Error Code 6 - low byte loaded during
                ;                           a high byte operation
                ;
                ; ************************************************
                ;
001036                  ERROR   6,REG           ; report error
                ;
001042  004767  2$:     CALL    WAIT
        177432
001046                  EXIT
```

```
                        .SBTTL  Test 5:  A/D DONE bit and interrupt
                ;
                ; This test verifies that the A/D DONE bit can
                ; be set properly and that the INT ENB bit
                ; functions properly.
                ;
                ;
001050  013701  TEST5:  MOV     @#BASE,R1       ; get address
        000542
001054  013702          MOV     @#VECTOR,R2     ; get vector address
        000544
001060  005761          TST     2(R1)           ; clear A/D DONE bit
        000002
001064  005011          CLR     (R1)            ; clear ADCSR
001066                  SCOPE                   ; declare loop point
001070  052711          BIS     #0,(R1)         ; set A/D DONE bit
        000000
001074  013700          MOV     @#DELAY,R0      ; wait for A/D DONE
        000546
001100  077001  1$:     SOB     R0,1$
001102  105711          TSTB    (R1)            ; is bit set?
001104  100402          BMI     2$              ; yes - skip error
                ;
                ; ************************************************
                ;
                ;       Error Code 7 - A/D DONE bit not set
                ;
                ; ************************************************
                ;
001106                  ERROR   7               ; report error
001110  000457          BR      8$              ; can't continue
                ;
001112          2$:     SCOPE                   ; declare loop point
001114  005761          TST     2(R1)           ; read ADDBR
        000002
001120  105711          TSTB    (R1)            ; done bit clear?
001122  100002          BPL     3$              ; yes - skip error
                ;
                ; ************************************************
                ;
                ;       Error Code 10 - A/D DONE bit not cleared
                ;                       after A/D data was read
                ;
                ; ************************************************
                ;
001124                  ERROR   10              ; report error
001126  000450          BR      8$              ; can't continue
```

```
 1 001130  005003  3$:     CLR     R3              ; prepare status words
 2 001132  012704           MOV     #PR7,R4
           000340
 3 001136                   RELMOV  #5$,R0          ; get ISR address
 4 001144  010012           MOV     R0,(R2)         ; store
 5 001146  010462           MOV     R4,2(R2)        ; store status too
           000002
 6 001152                   SCOPE                   ; declare loop point
 7 001154  005011           CLR     (R1)            ; set A/D DONE
 8 001156  013700           MOV     @#DELAY,R0      ; wait for DONE
           000546
 9 001162  077001  4$:      SOB     R0,4$
10 001164  152711           BISB    #100,(R1)       ; enable interrupts
           000100
11 001170  106403           MTPS    R3              ; enable CPU interrupts
12 001172  000240           NOP                     ; stall time
13 001174  106404           MTPS    R4              ; turn off CPU
14                 ;
15                 ; ***************************************************
16                 ;
17                 ;       Error Code 11 - no interrupt on A/D DONE
18                 ;
19                 ; ***************************************************
20                 ;
21 001176                   ERROR   11              ; report error
22 001200  000423           BR      8$              ; can't continue
23                 ;
24 001202  062706  5$:      ADD     #4,SP           ; adjust stack
           000004
25 001206                   SCOPE                   ; declare loop point
26 001210  005761           TST     2(R1)           ; read ADDBR
           000002
27 001214  105711           TSTB    (R1)            ; A/D DONE clear?
28 001216  100002           BPL     6$              ; yes - exit
29                 ;
30                 ; ***************************************************
31                 ;
32                 ;       Error Code 12 - A/D DONE bit not cleared
33                 ;                       after A/D data was read
34                 ;
35                 ; ***************************************************
36                 ;
37 001220                   ERROR   12              ; report error
38 001222  000412           BR      8$              ; can't continue
```

TEST 5: A/D DONE BIT AND INTERRUPT

```
 1 001224           6$:     SCOPE                   ; declare loop point
 2 001226  005761           TST     2(R1)           ; clear DONE
           000002
 3 001232  005011           CLR     (R1)            ; clear ADCSR
 4 001234  013700           MOV     @#DELAY,R0      ; wait
           000546
 5 001240  077001   7$:     SOB     R0,7$
 6 001242  005711           TST     (R1)            ; error bit set?
 7 001244  100001           BPL     8$              ; no - exit
 8                  ;
 9                  ; ***************************************************
10                  ;
11                  ;       Error Code 13 - Error bit set after normal
12                  ;                       A/D triggering sequence
13                  ;
14                  ; ***************************************************
15                  ;
16 001246                  ERROR   13              ; report error
17                  ;
18 001250  005761   8$:     TST     2(R1)           ; clear DONE
           000002
19 001254  005011           CLR     (R1)
20 001256  004767           CALL    WAIT
           177216
21 001262                  EXIT
```

```
                        .SBTTL  Test 6:  End of logic tests
                ;
                ; This test is present to inform the TST-11 monitor
                ; that there are no more additional logic tests
                ; to be executed. When the "ALL" command is used,
                ; this test will force a return to the command
                ; level of TST-11 when the test sequencer reaches
                ; this test.
                ;
                ;
001264          TEST6:  ESCAPE
                ;
                ;
                        .SBTTL  Calibration initialization
                ;
                ; This routine performs initialization functions
                ; for some of the calibration tests.
                ;
                ;
001266          GETCH:  PRINT   <Channel? >     ; output prompt
001302                  GETOCT                  ; get value
001304  103422          BCS     1$              ; CR at end - cont.
001306                  PRINTC  <Enter an octal channel address.>
001350  000746          BR      GETCH           ; try again
                ;
001352  013701  1$:     MOV     @#BASE,R1       ; get address
        000542
001356  013702          MOV     @#ODTACC,R2     ; get value
        000514
001362  000302          SWAB    R2              ; adjust
001364          2$:     PRINT   <Mode bits? >   ; output prompt
001402                  GETOCT                  ; get value
001404  103420          BCS     3$              ; CR at end - cont.
001406                  PRINTC  <Enter an octal byte value.>
001444  000747          BR      2$
                ;
001446  042702  3$:     BIC     #377,R2         ; clear low byte,R2
        000377
001452  013700          MOV     @#ODTACC,R0     ; get value
        000514
001456  042700          BIC     #177400,R0      ; clear high byte,R0
        177400
001462  060002          ADD     R0,R2           ; add in mode byte
001464  005761          TST     2(R1)           ; clear DONE
        000002
001470  005011          CLR     (R1)            ; clear board
001472  105711  4$:     TSTB    (R1)
001474  100376          BPL     4$
001476  005761          TST     2(R1)
        000002
001502  000207          RETURN
```

```
                        .SBTTL  Display A/D data
                ;
                ; This routine takes the data from ADDBR and displays
                ; it for the user as a 16 bit octal value.
                ;
001504 016100   DISPLY: MOV     2(R1),R0        ; get data
       000002
001510                  OCT16                   ; print
001512 005711           TST     (R1)            ; error bit set?
001514 100015           BPL     1$              ; no - return
001516 112700           MOVB    #'E,R0          ; print 'E'
       000105
001522                  TTYOUT
001524 042711           BIC     #40000,(R1)     ; clear error bit
       040000
001530 005237           INC     @#ERRCNT        ; inc. count
       000522
001534 005737           TST     @#ERRCNT        ; overflow?
       000522
001540 001003           BNE     1$              ; no - skip
001542 012737           MOV     #-1,@#ERRCNT    ; yes - force value
       177777
       000522
001550 000207   1$:     RETURN
                ;
                ;
                        .SBTTL  Test 7: A/D Calibration
                ;
                ; This test accepts a channel address from the user
                ; and displays the data from that channel continuously.
                ;
                ;
001552          TEST7:  PRINTC  <A/D Calibration>
001574 004767           CALL    GETCH           ; get channel address
       177460
001600                  KBEXIT                  ; set up keyboard
001602 042702           BIC     #140363,R2      ; clear all but gain bi
       140363
001606 112704   1$:     MOVB    #10,R4          ; line counter
       000010
001612                  CRLF
001614 010211   2$:     MOV     R2,(R1)         ; start conversion
001616 105711   3$:     TSTB    (R1)            ; wait for DONE
001620 100376           BPL     3$
001622 004767           CALL    DISPLY          ; display data
       177656
001626 105304           DECB    R4              ; line over?
001630 001766           BEQ     1$              ; yes - new line
001632                  TAB
001634 000767           BR      2$              ; next conversion
```

```
                                .SBTTL  Test 10: A/D input channel scan
                        ;
                        ; This test scans the input channels while
                        ; displaying the A/D data on the terminal.
                        ;
                        ;
001636                  TEST10: PRINTC  <A/D Input channel scan>
001670                          KBEXIT
001672  013701                  MOV     @#BASE,R1       ; set up keyboard
        000542                                          ; get address
001676  005761                  TST     2(R1)           ; clear DONE
        000002
001702  005011                  CLR     (R1)            ; clear CSR
001704  004767                  CALL    WAIT
        176570
001710  005002                  CLR     R2              ; init. channel count
001712                  1$:     CRLF
001714  112703                  MOVB    #10,R3          ; line counter
        000010
001720                          PRINT   <CH=>           ; display address
001726  010200                  MOV     R2,R0
001730                          OCT8
001732  010200                  MOV     R2,R0           ; get channel address
001734  000300                  SWAB    R0              ; put in high byte
001736  010011                  MOV     R0,(R1)         ; set up channel
001740  000167                  JMP     3$
        000004
001744  052711          2$:     BIS     #0,(R1)         ; trigger converter
        000000
001750  105711          3$:     TSTB    (R1)            ; wait for DONE
001752  100376                  BPL     3$
001754                          TAB
001756  004767                  CALL    DISPLY          ; display data
        177522
001762  105303                  DECB    R3              ; line done?
001764  001367                  BNE     2$              ; no - continue
001766  005202                  INC     R2              ; inc. channel
001770  123702                  CMPB    @#SWR+1,R2      ; end of range?
        000541
001774  001346                  BNE     1$              ; no - continue
001776  005002                  CLR     R2              ; yes
002000                          CRLF
002002  000743                  BR      1$
```

```
                        .SBTTL  Test 11: A/D input gain/channel scan
                ;
                ; This test scans the input channels while
                ; changing the gain of the converter.  The
                ; A/D data is displayed on the terminal.
                ;
                ;
002004          TEST11: PRINTC  <A/D Input gain/channel scan>
002042                  KBEXIT                  ; set up keyboard
002044  013701          MOV     @#BASE,R1       ; get address
        000542
002050  005761          TST     2(R1)           ; clear DONE
        000002
002054  005011          CLR     (R1)            ; clear CSR
002056  105711  6$:     TSTB    (R1)
002060  100376          BPL     6$
002062  005761          TST     2(R1)
        000002
002066  005002          CLR     R2              ; init. channel count
002070  005003          CLR     R3              ; init. gain
002072          1$:     CRLF
002074  112704          MOVB    #7,R4           ; line counter
        000007
002100                  PRINT   <CH=>           ; display address
002106  010200          MOV     R2,R0
002110                  OCT8
002112  112700          MOVB    #',,R0          ; display gain
        000054
002116                  TTYOUT
002120  112700          MOVB    #'0,R0
        000060
002124  032703          BIT     #10,R3          ; GS1 set?
        000010
002130  001401          BEQ     2$              ; no - skip
002132  105200          INCB    R0
002134          2$:     TTYOUT                  ; display bit
002136  112700          MOVB    #'0,R0
        000060
002142  032703          BIT     #4,R3           ; GS0 set?
        000004
002146  001401          BEQ     3$              ; no - skip
002150  105200          INCB    R0
002152          3$:     TTYOUT                  ; display bit
```

```
    1 002154  010200            MOV     R2,R0           ; get channel address
    2 002156  000300            SWAB    R0              ; put in high byte
    3 002160  050300            BIS     R3,R0           ; set gain bits
    4 002162                    PUSH    R0
    5 002164  011611    4$:     MOV     (SP),(R1)       ; trigger conversion
    6 002166  105711    5$:     TSTB    (R1)            ; wait for DONE
    7 002170  100376            BPL     5$
    8 002172                    TAB
    9 002174  004767            CALL    DISPLY          ; display data
              177304
   10 002200  105304            DECB    R4              ; line done?
   11 002202  001370            BNE     4$              ; no - continue
   12 002204                    POP     R0
   13 002206  005202            INC     R2              ; inc. channel
   14 002210  062703            ADD     #4,R3           ; increment gain
              000004
   15 002214  042703            BIC     #177763,R3      ; clear extra bits
              177763
   16 002220  123702            CMPB    @#SWR+1,R2      ; end of range?
              000541
   17 002224  001322            BNE     1$              ; no - continue
   18 002226  005002            CLR     R2              ; yes
   19 002230                    CRLF
   20 002232  000717            BR      1$
   21                   ;
   22         000001            .END
```

SYMBOL TABLE

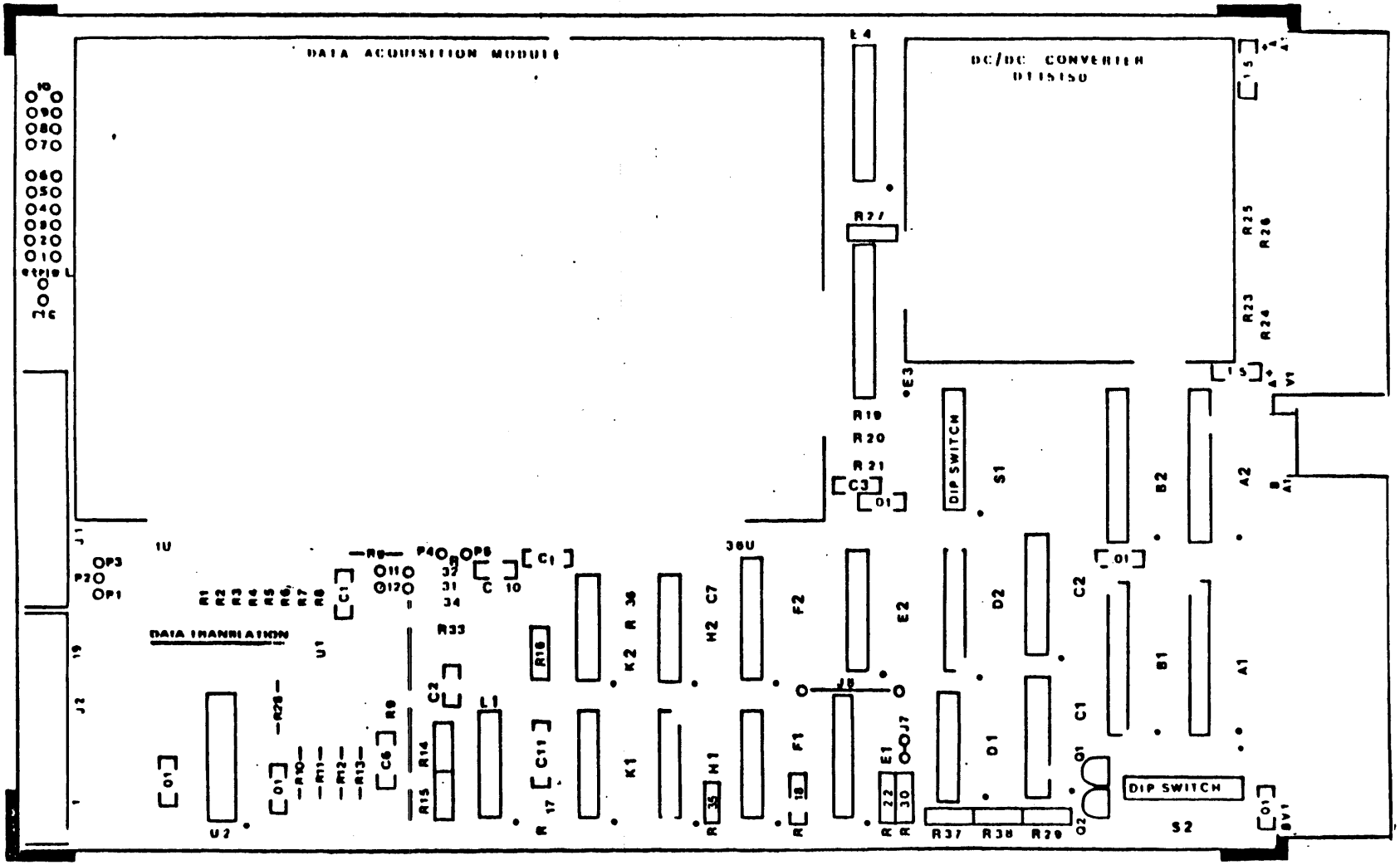
```
BASE  = 000542          ERRCNT= 000522          SWR   = 000540
BIT0  = 000001          ERRNUM= 000521          TEST1   000514R     002
BIT1  = 000002          FF    = 000014          TEST10  001636R     002
BIT10 = 002000          GETCH   001266R     002 TEST11  002004R     002
BIT11 = 004000          HLTERR= 000004          TEST2   000570R     002
BIT12 = 010000          INHERR= 000100          TEST3   000676R     002
BIT13 = 020000          INIT    000064R     002 TEST4   000752R     002
BIT14 = 040000          INIT65  000050R     002 TEST5   001050R     002
BIT15 = 100000          I2765 = 000050RG    002 TEST6   001264R     002
BIT2  = 000004          LF    = 000012          TEST7   001552R     002
BIT3  = 000010          LPERR = 000002          TPB     000000R     002
BIT4  = 000020          LPTST = 000001          TSTALL= 000010
BIT5  = 000040          NEWFLG= 010000          TSTCSR= 000500
BIT6  = 000100          NORPLY  000264R     002 TSTNUM= 000520
BIT7  = 000200          ODTACC= 000514          TSTONE= 000040
BIT8  = 000400          PARAM   000172R     002 TSTSEQ= 000020
BIT9  = 001000          PR7   = 000340          T2765 = 000000RG    002
CR    = 000015          RBUF  = 177562          VECTOR= 000544
CTRLC = 000003          RCSR  = 177560          WAIT    000500R     002
CTRLI = 000011          REG     000340R     002 XBUF  = 177566
DELAY = 000546          SPACE = 000040          XCSR  = 177564
DISPLY  001504R     002

  ABS.  000000      000
        000000      001
  I2765 002234      002
ERRORS DETECTED:  0

VIRTUAL MEMORY USED:  2128 WORDS  ( 9 PAGES)
DYNAMIC MEMORY AVAILABLE FOR  67 PAGES
,DX1:2765,=DX1:TST11.ML/M,DX1:2765.V01
```

APPENDIX D
SCHEMATIC DRAWINGS

REDUCE TO 9.500



SILK-SCREEN
EP050

COMPONENT DESIGNATIONS

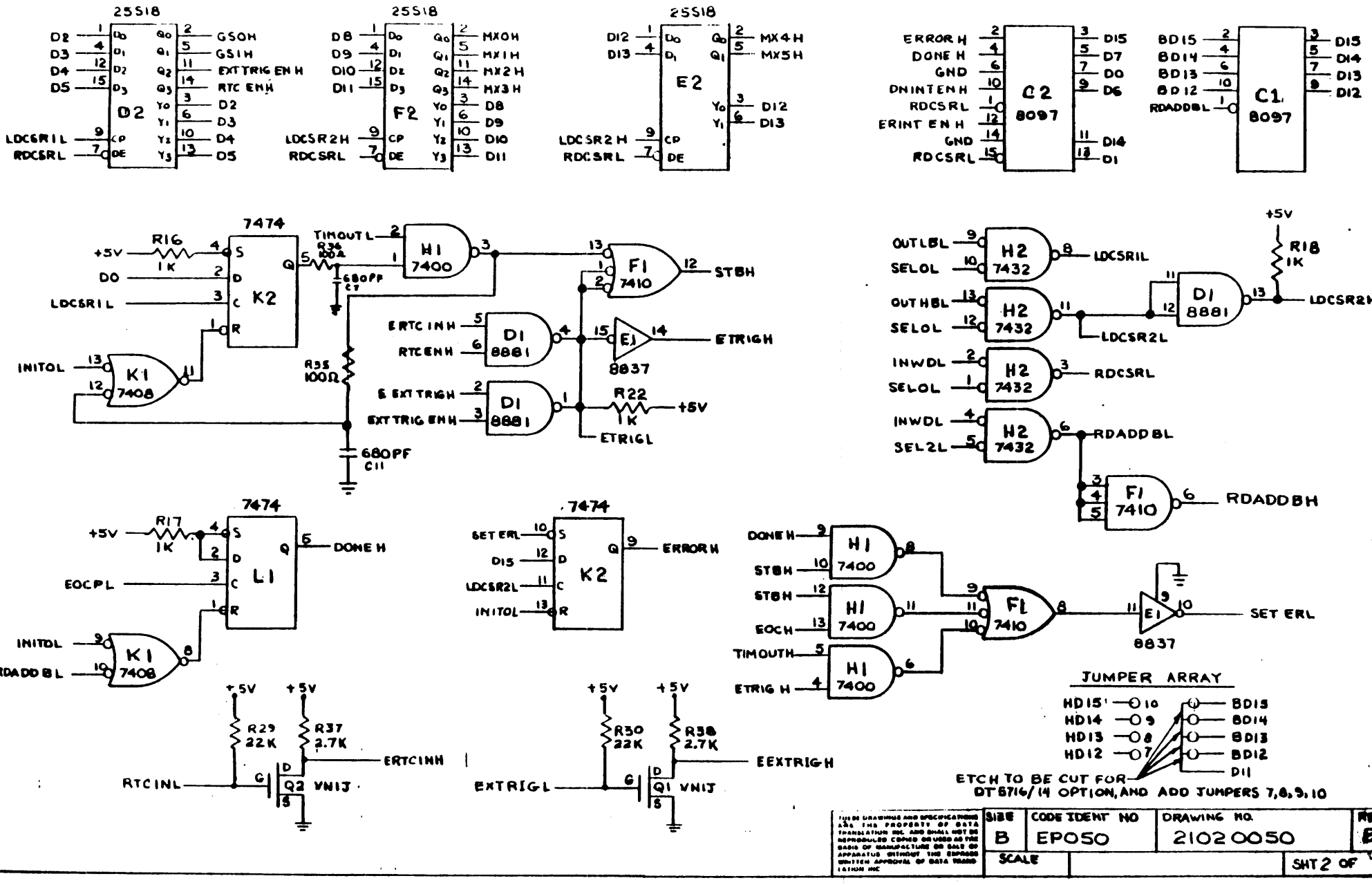
THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DATA TRANSLATION, INC. AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS OF MANUFACTURE OR SALE OF APPARATUS WITHOUT THE EXPRESS WRITTEN APPROVAL OF DATA TRANS-	SIZE A	CODE IDENT NO. EP050	DRAWING NO. 11070050	REV F
	SCALE			SHEET 1 OF 1

REVISION	ECO NO.	DATE	DWN	ENG
F1	# 227	1-3-80	K.E.D	
F	# 177	9-11-79	K.F.C.	K.E.D.
E	# 146	1-18-79	K.F.C.	K E.D.
D	# 127	11-14-78	K F.C	K E.D.

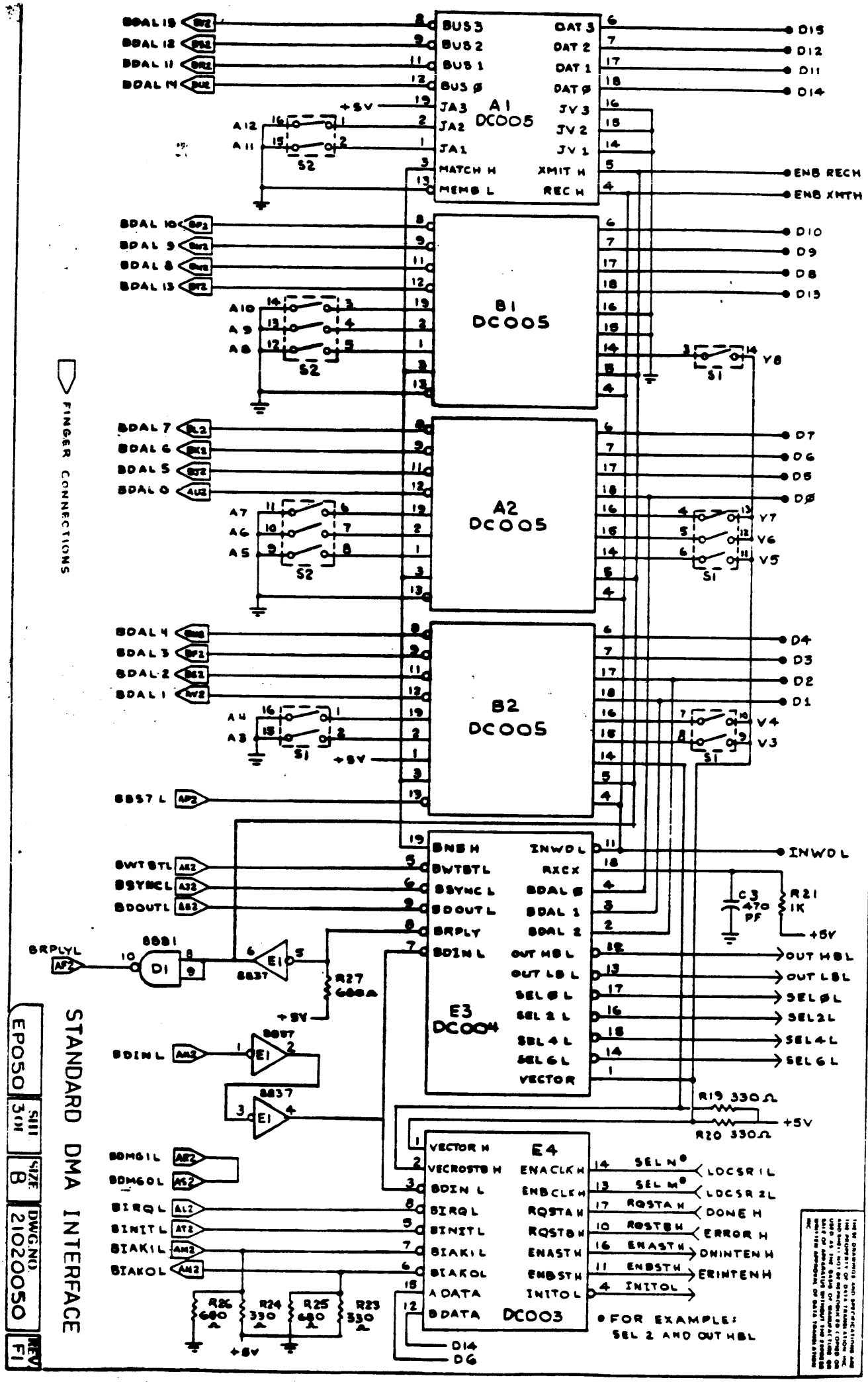
DATA TRANSLATION INC

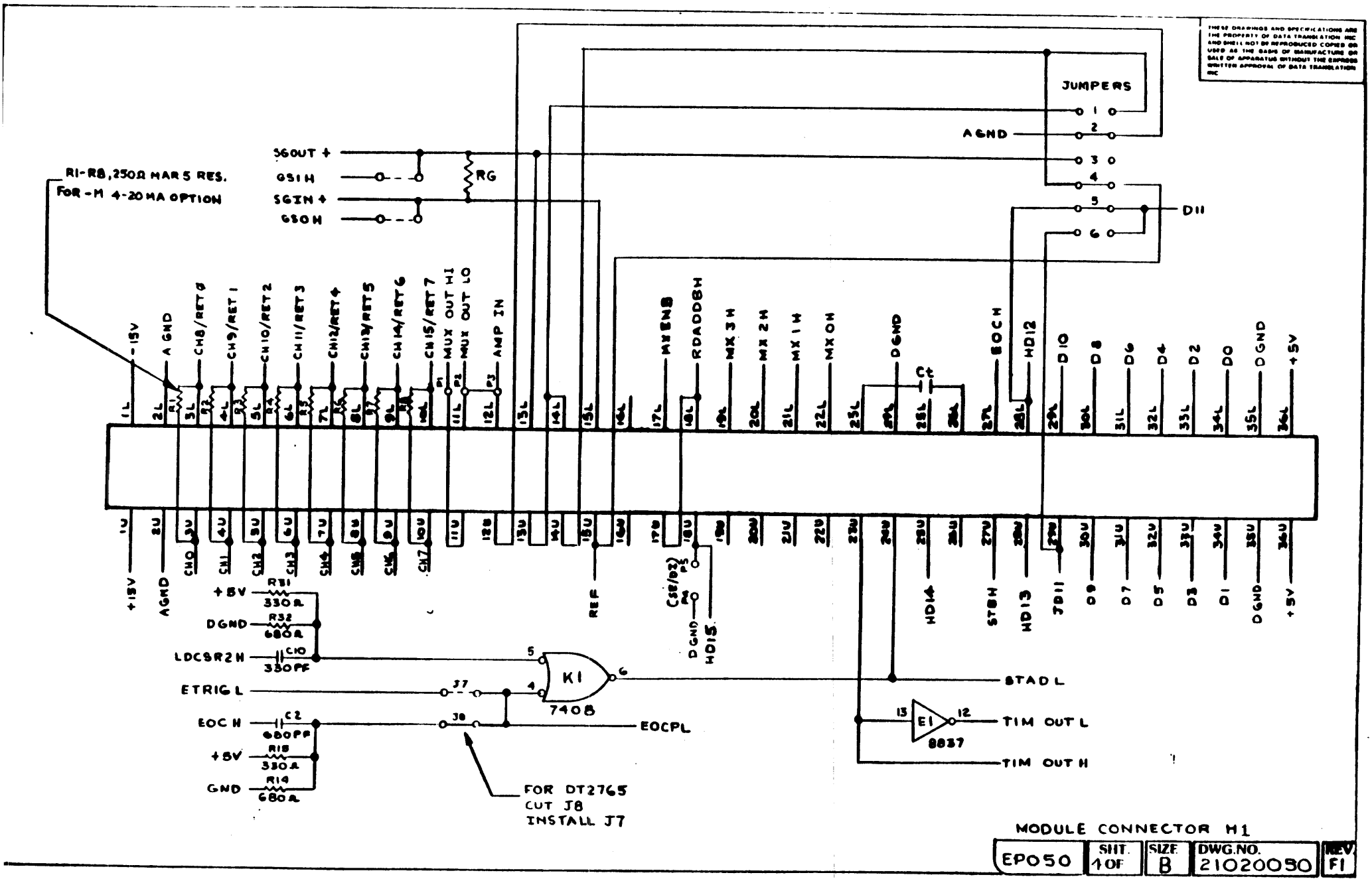
DRAWN: K.E.D.	DATE: 4-10-78	TITLE: LSI-11 ANALOG INPUT BOARDS DT2762 DT2762/571X DT2764 DT2764/571X DT2765
CHECKED: K.E.D.	DATE: 6-29-78	
ENG: P.J.S.	DATE: 6-30-78	

EPOSO	SHT. 1 OF 10	SIZE B	DWG.NO. 21020050	REV. F1



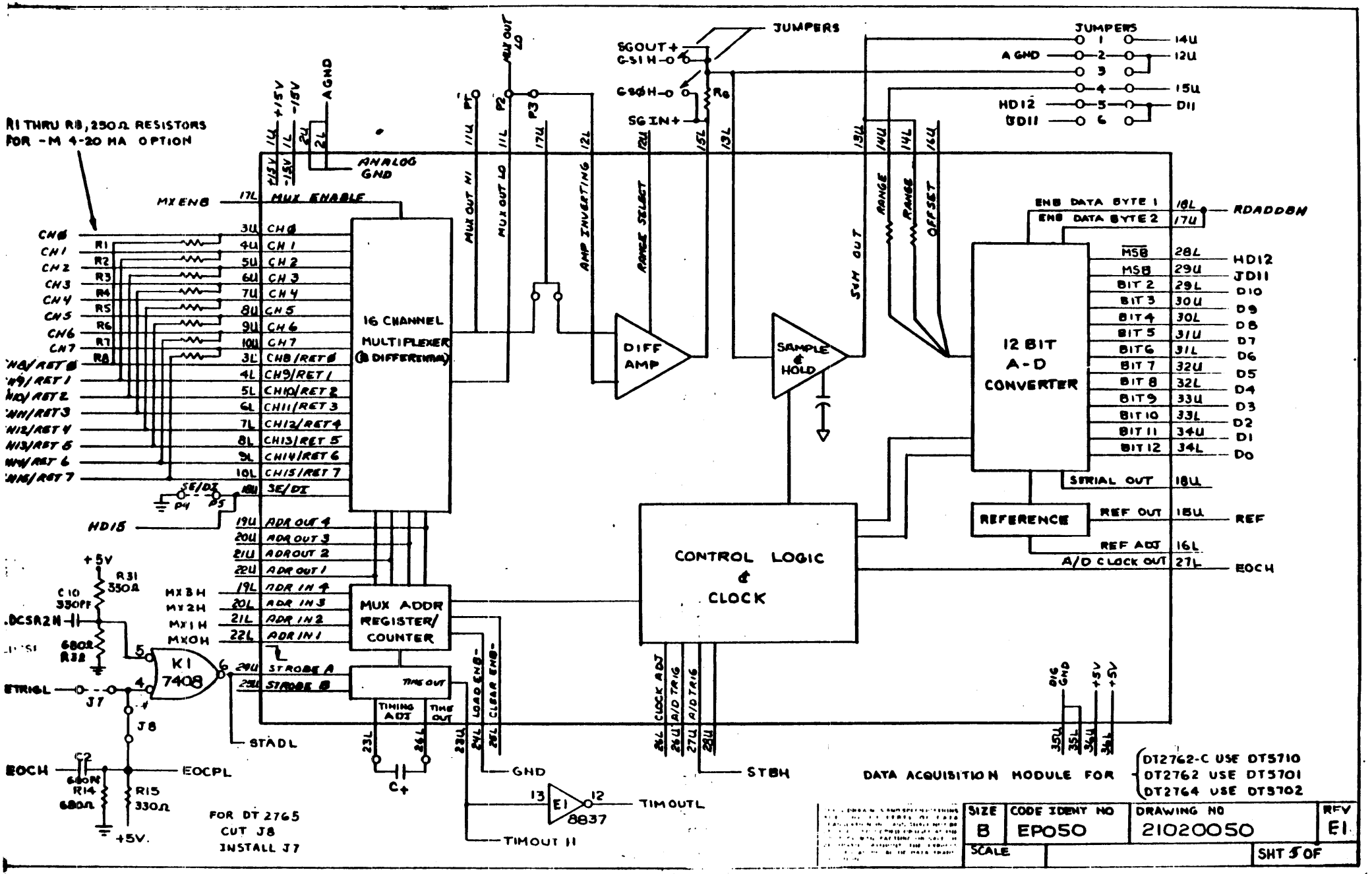
SIZE	CODE IDENT NO	DRAWING NO.	REV
B	EP050	21020050	E1
SCALE			SHT 2 OF

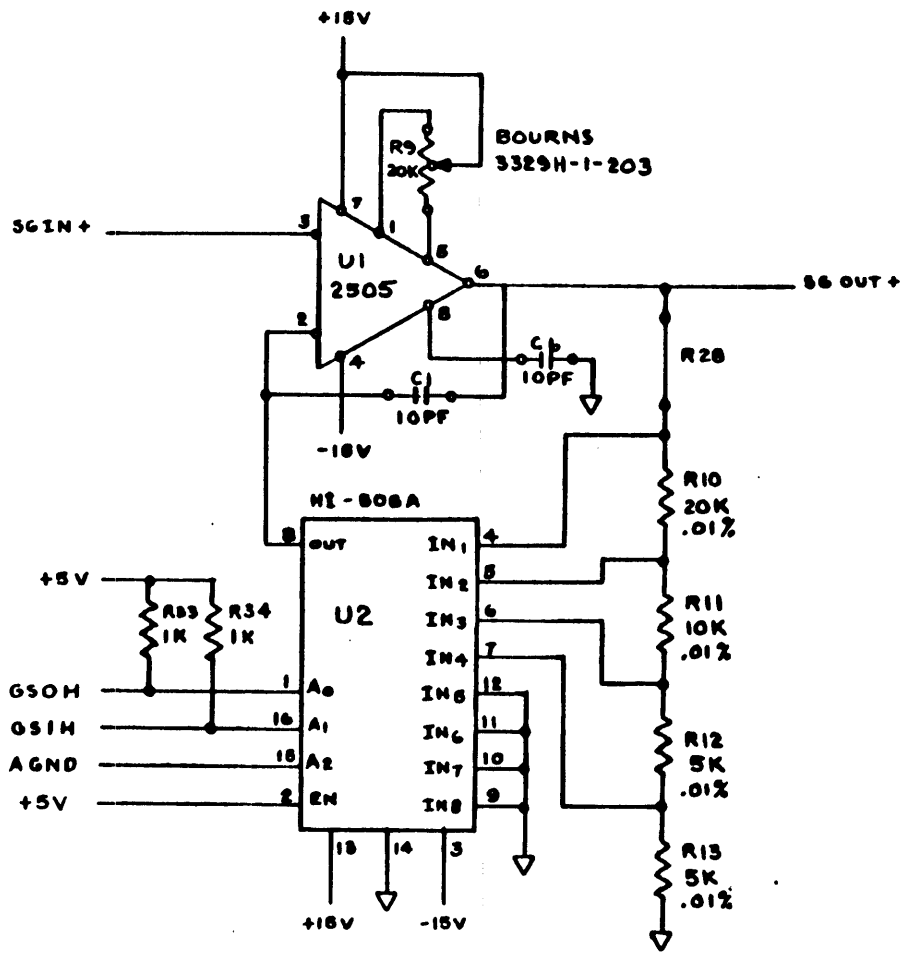

STANDARD DMA INTERFACE
FINGER CONNECTIONS
A1 DC005
B1 DC005
A2 DC005
B2 DC005
E3 DC004
E4
DC003
BUS3
BUS2
BUS1
BUS Ø
JA3
JA2
JA1
MATCH H
MEMB L
DAT 3
DAT 2
DAT 1
DAT Ø
JV 3
JV 2
JV 1
XMIT H
REC H
BDAL 15
BDAL 12
BDAL 11
BDAL 14
BDAL 10
BDAL 9
BDAL 8
BDAL 13
BDAL 7
BDAL 6
BDAL 5
BDAL Ø
BDAL 4
BDAL 3
BDAL 2
BDAL 1
BBS7 L
+5V
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
S1
S2
D15
D12
D11
D14
D10
D9
D8
D13
D7
D6
D5
DØ
D4
D3
D2
D1
V8
V7
V6
V5
V4
V3
ENB RECH
ENB XMTH
BWTBTL
BSYNCL
BDOUTL
BRPLY L
8881
D1
8837
E1
R27 680Ω
BDIN L
BDMGIL
BDMGOL
BIRQL
BINITL
BIAKIL
BIAKOL
R26 680Ω
R24 330Ω
R25 680Ω
R23 330Ω
BNSB H
BWTBTL
BSYNC L
BDOUT L
BRPLY
BDIN L
INWD L
RXCX
BDAL Ø
BDAL 1
BDAL 2
OUT HBL
OUT LBL
SEL ØL
SEL 2 L
SEL 4 L
SEL 6 L
VECTOR
C3 470 PF
R21 1K
R19 330Ω
R20 330Ω
VECTOR H
VECROSTB H
ENACLK H
ENBCLK H
RQSTA H
RQSTB H
ENASTH
ENBSTH
INITOL
A DATA
B DATA
SEL N*
SEL M*
RQSTA H
RQSTB H
ENASTH
ENBSTH
INITOL
LOCSR1L
LOCSR2L
DONE H
ERROR H
DNINTENH
ERINTENH
* FOR EXAMPLE:
SEL 2 AND OUT HBL
EP050
SIII
3 OF
SIZE
B
DWG NO.
21020050
REV
F1



MODULE CONNECTOR H1

EP050	SHT. 1 OF	SIZE B	DWG.NO. 21020050	REV F1

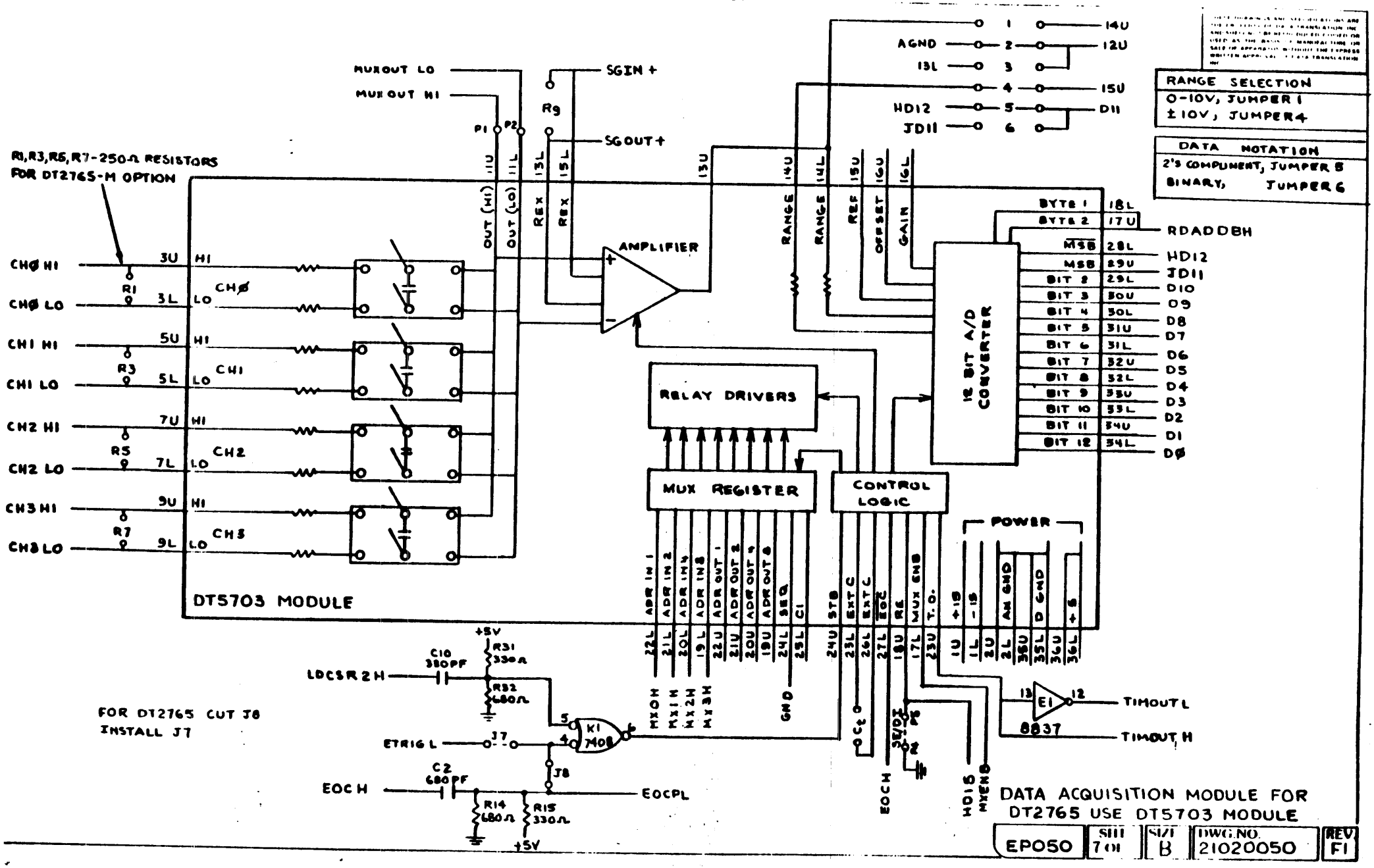

R1 THRU R8, 250Ω RESISTORS FOR -M 4-20 MA OPTION
+15V
-15V
AGND
ANALOG GND
MUX OUT LO
MUX OUT HI
AMP INVERTING
RANGE SELECT
SAH OUT
RANGE
RANGE
OFFSET
JUMPERS
SGOUT+
SGIN-
SGØH-
SGIN+
R6
AGND
HD12
JD11
MXENB
MUX ENABLE
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
16 CHANNEL MULTIPLEXER (8 DIFFERENTIAL)
DIFF AMP
SAMPLE & HOLD
12 BIT A-D CONVERTER
ENB DATA BYTE 1
ENB DATA BYTE 2
RDADDBH
MSB
MSB
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
HD12
JD11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
SERIAL OUT
REFERENCE
REF OUT
REF ADJ
A/D CLOCK OUT
REF
EOCH
SE/DI
HD15
ADR OUT 4
ADR OUT 3
ADR OUT 2
ADR OUT 1
ADR IN 4
ADR IN 3
ADR IN 2
ADR IN 1
MX8H
MX2H
MX1H
MX0H
MUX ADDR REGISTER/ COUNTER
CONTROL LOGIC & CLOCK
+5V
R31 330Ω
C10 330PF
680Ω R32
K1 7408
ETRIGL
J7
J8
STROBE A
STROBE B
TIME OUT
TIMING ADJ
TIME OUT
LOAD ENB-
CLEAR ENB-
STADL
GND
C+
E1 8837
TIMOUTL
TIMOUT 11
C2 680PF
R14 680Ω
R15 330Ω
EOCPL
+5V.
FOR DT 2765 CUT J8 INSTALL J7
CLOCK ADJ
A/D TRIG
A/D TRIG
STBH
DIG GND
+5V
+5V
DATA ACQUISITION MODULE FOR
DT2762-C USE DT5710
DT2762 USE DT5701
DT2764 USE DT5702
SIZE
B
CODE IDENT NO
EP050
DRAWING NO
21020050
REV
E1
SCALE
SHT 5 OF

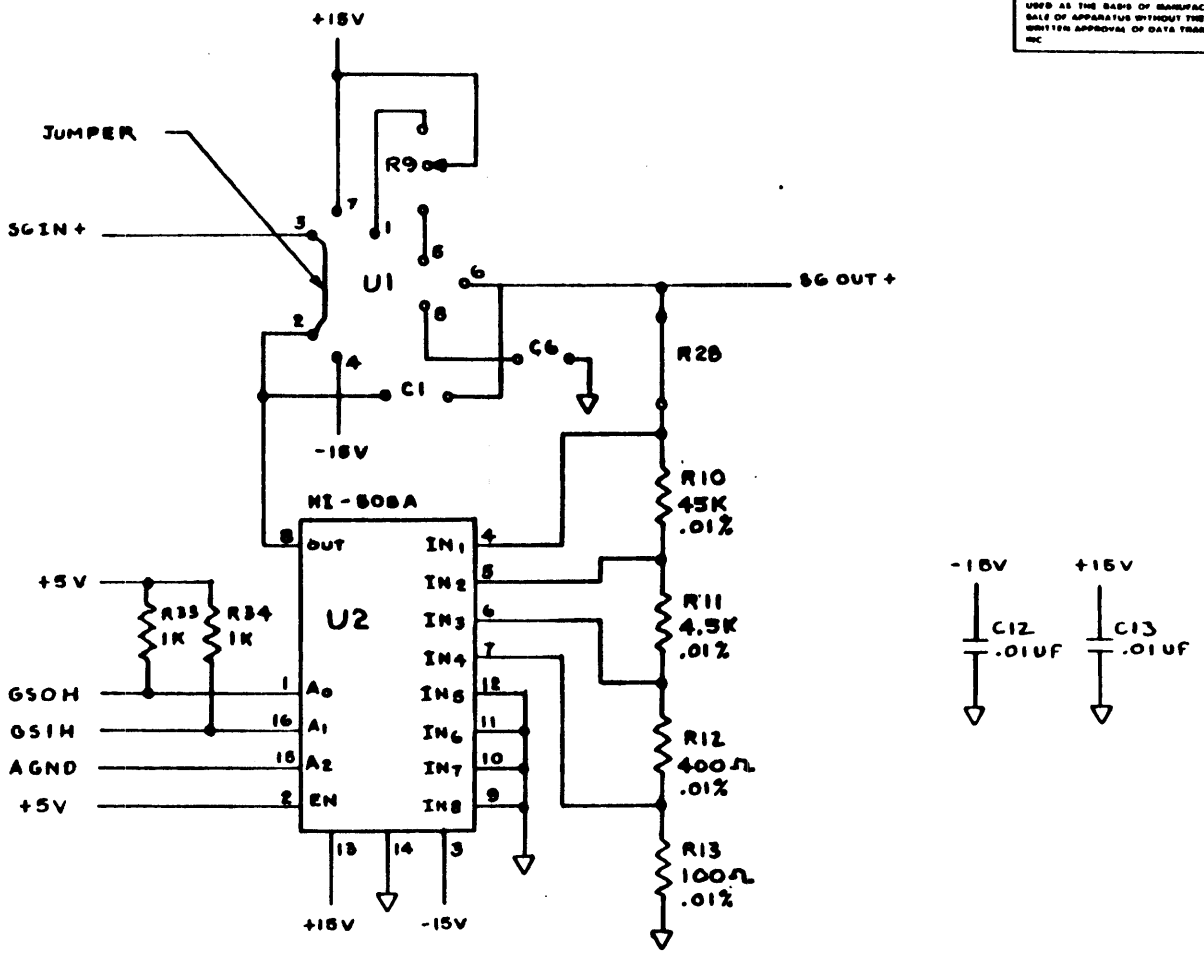


MODEL DT2762

PROGRAMMABLE GAIN OPTION

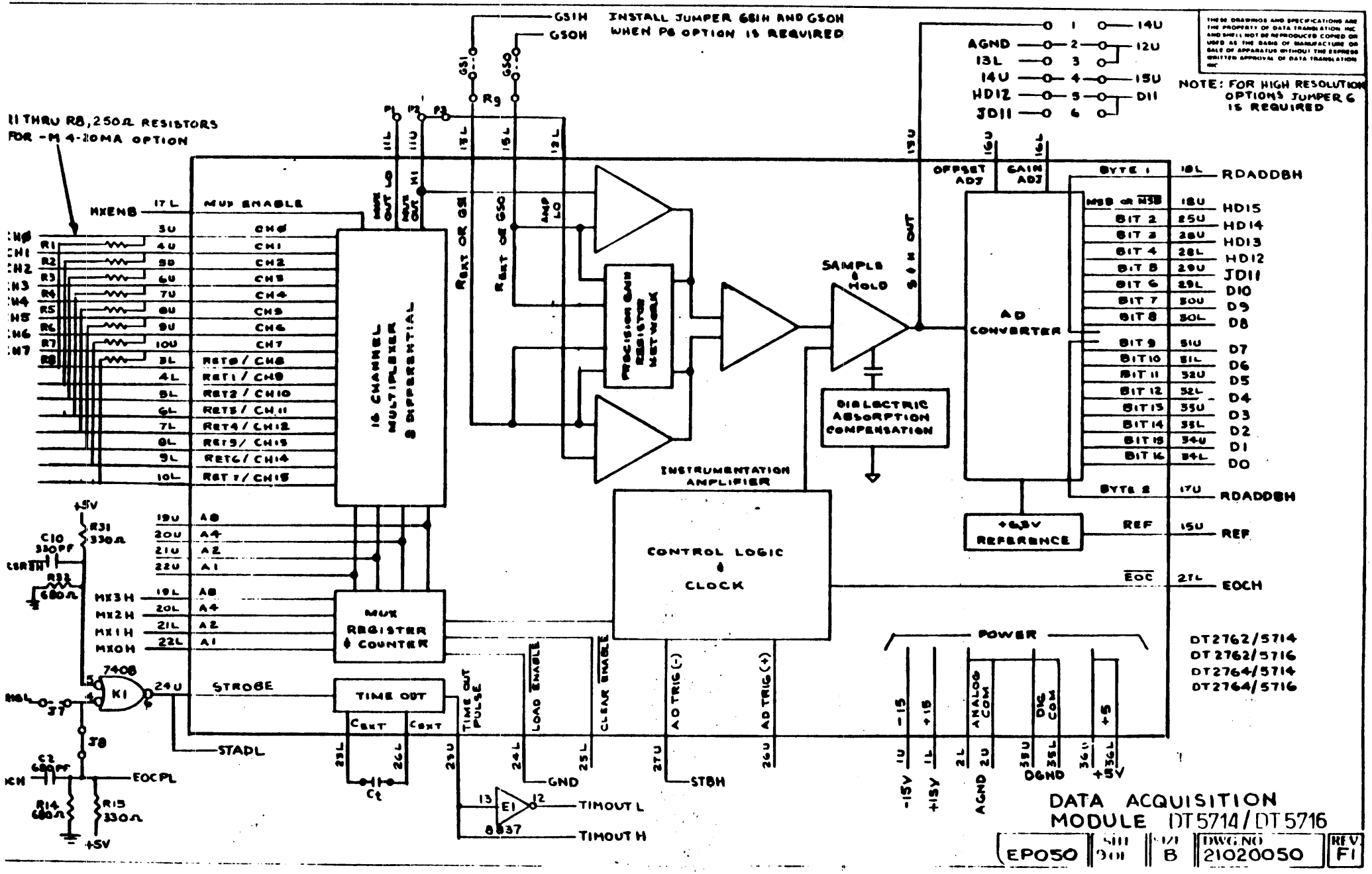
EP050	SHT 6 OF	SIZE B	DWG NO 21020050	REV F1


R1,R3,R5,R7-250Ω RESISTORS FOR DT2765-M OPTION
MUXOUT LO
MUXOUT HI
SGIN +
SGOUT +
R9
P1
P2
CH0 HI
CH0 LO
CH1 HI
CH1 LO
CH2 HI
CH2 LO
CH3 HI
CH3 LO
R1
R3
R5
R7
CH0
CH1
CH2
CH3
HI
LO
OUT (HI)
OUT (LO)
REX
REX
AMPLIFIER
RANGE
RANGE
REF
OFFSET
GAIN
AGND
13L
HD12
JD11
RELAY DRIVERS
MUX REGISTER
CONTROL LOGIC
12 BIT A/D CONVERTER
BYTE 1
BYTE 2
MSB
MSB
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
RDADDBH
HD12
JD11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
POWER
DT5703 MODULE
ADR IN 1
ADR IN 2
ADR IN4
ADR IN8
ADR OUT 1
ADR OUT 2
ADR OUT 4
ADR OUT 8
SEQ
CI
STB
EXTC
EXTC
EOC
RE
MUX ENB
T.O.
+15
-15
AN GND
D GND
+5
MXOH
MX1H
MX2H
MX3H
GND
EOCH
HD15
MXENB
+5V
C10
330PF
R31
330Ω
LDCSR2H
R32
680Ω
K1
7408
ETRIG L
J7
J8
EOC H
C2
680PF
R14
680Ω
R15
330Ω
EOCPL
FOR DT2765 CUT J8
INSTALL J7
E1
8837
TIMOUT L
TIMOUT H
RANGE SELECTION
0-10V, JUMPER 1
±10V, JUMPER 4
DATA NOTATION
2'S COMPLIMENT, JUMPER 5
BINARY, JUMPER 6
DATA ACQUISITION MODULE FOR DT2765 USE DT5703 MODULE
EP050
SHT 1 OF 1
SIZE B
DWG NO. 21020050
REV F1



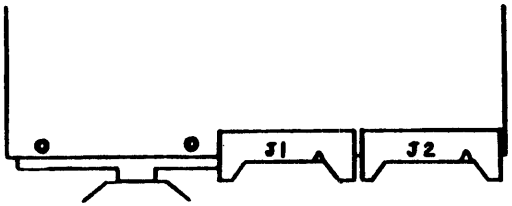
MODEL DT2765
PROGRAMMABLE GAIN OPTION

EP050	SHT 8 of 8	SIZE B	DWG.NO. 21020050	REV. F1



DATA ACQUISITION MODULE DT5714/DT5716

EP050	SHT 1 OF 1	REV B	DWG NO 21020050	REV F1



EXPANSION
CONNECTIONS FOR ALL MODELS

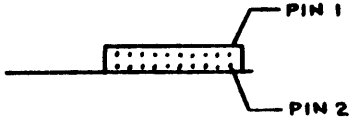
J1 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	MX ØH	2	MX 1H
3	MX2H	4	MX3H
5	MX4H	6	MX5H
7	MXENB	8	SE/DI
9	RTC INL	10	D GND
11	D GND	12	STADL
13	A GND	14	AGND
15	MX OUT HI	16	MX OUT LO
17	A GND	18	-15V
19	A GND	20	+15V

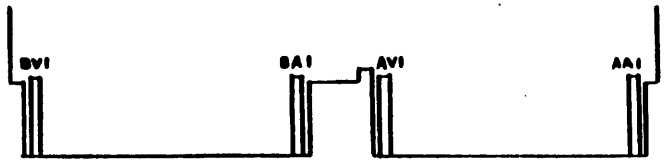
CONNECTIONS FOR DT2762 + DT2764

J2 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	CHØ	2	CH8/RET Ø
3	CH1	4	CH9/RET 1
5	CH2	6	CH10/RET 2
7	CH3	8	CH11/RET 3
9	CH4	10	CH12/RET 4
11	CH5	12	CH13/RET 5
13	CH6	14	CH14/RET 6
15	CH7	16	CH15/RET 7
17	A GND	18	AMP IN
19	EXT TRIG L	20	D GND

CONNECTIONS FOR DT2765

J2 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	CHØ HI	2	CHØ LO
3		4	
5	CH1 HI	6	CH1 LO
7		8	
9	CH2 HI	10	CH2 LO
11		12	
13	CH3 HI	14	CH3 LO
15		16	
17	A GND	18	AMP IN
19	EXT TRIG L	20	D GND





BOTTOM EDGE CONNECTOR							
COMPONENT SIDE		SOLDER SIDE		COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
BA1		BA2	+5V	AA1		AA2	+5V
BB1		BB2		AB1		AB2	
BC1		BC2	D GND	AC1		AC2	D GND
BD1		BD2		AD1		AD2	
BE1		BE2	BDAL 2L	AE1		AE2	BDOUTL
BF1		BF2	BDAL 3L	AF1		AF2	BRPLYL
BH1		BH2	BDAL 4L	AH1		AH2	BDINL
BJ1	D GND	BJ2	BDAL 5L	AJ1	D GND	AJ2	BSYNCL
BK1		BK2	BDAL 6L	AK1		AK2	BWTBTL
BL1		BL2	BDAL 7L	AL1		AL2	BIRQL
BM1	D GND	BM2	BDAL 8L	AM1	D GND	AM2	BIAKIL
BN1		BN2	BDAL 9L	AN1		AN2	BIAKOL
BP1		BP2	BDAL 10L	AP1		AP2	BBS7L
BR1		BR2	BDAL 11L	AR1		AR2	BDMGIL
BS1		BS2	BDAL 12L	AS1		AS2	BDMGOL
BT1	D GND	BT2	BDAL 13L	AT1	D GND	AT2	BINITL
BU1		BU2	BDAL 14L	AU1		AU2	BDALOL
BV1	+5V	BV2	BDAL 15L	AV1		AV2	BDALIL

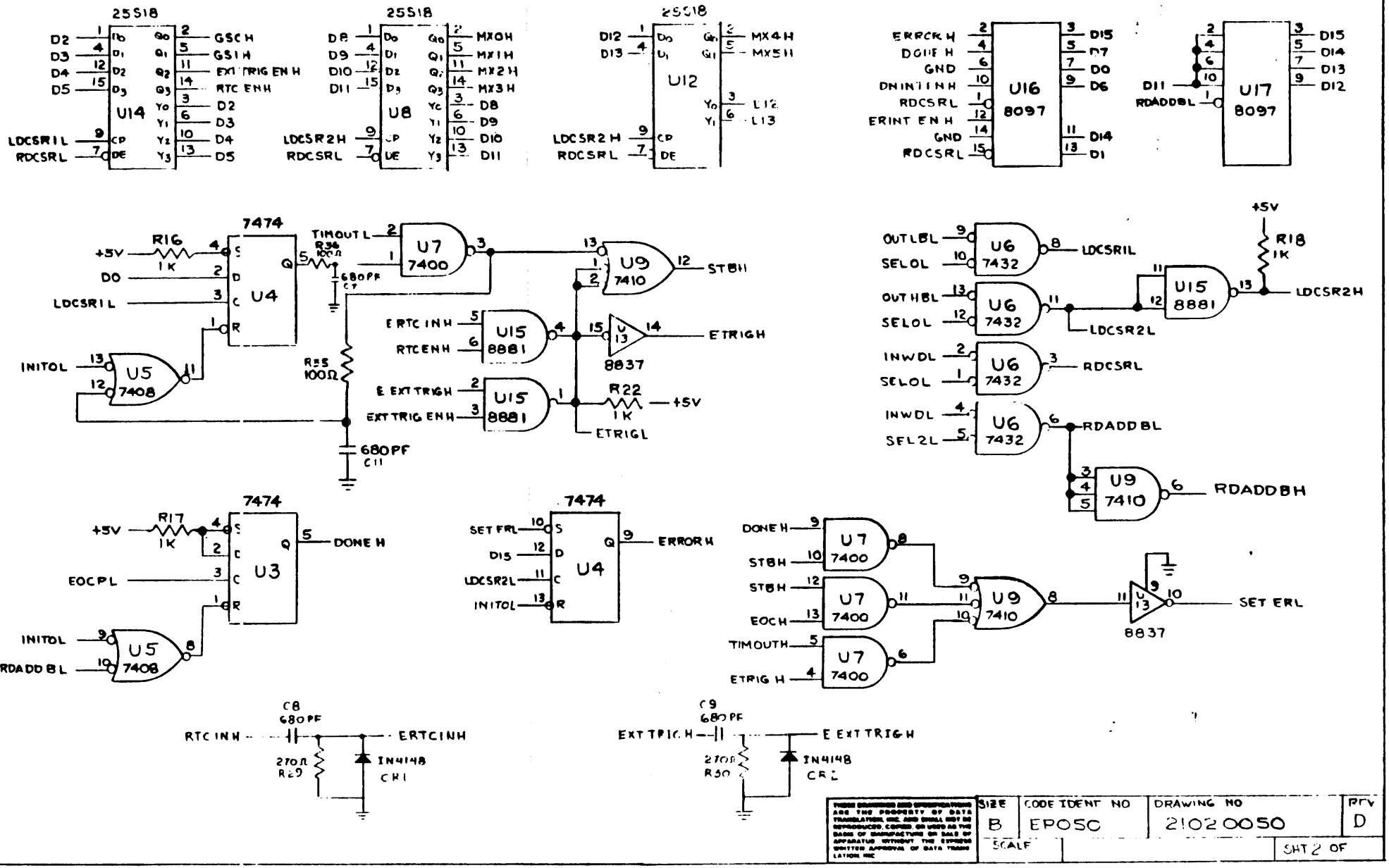
EP050	SHT. 10 OF 10	SIZE B	DWG.NO. 21020050 -	REV. F1

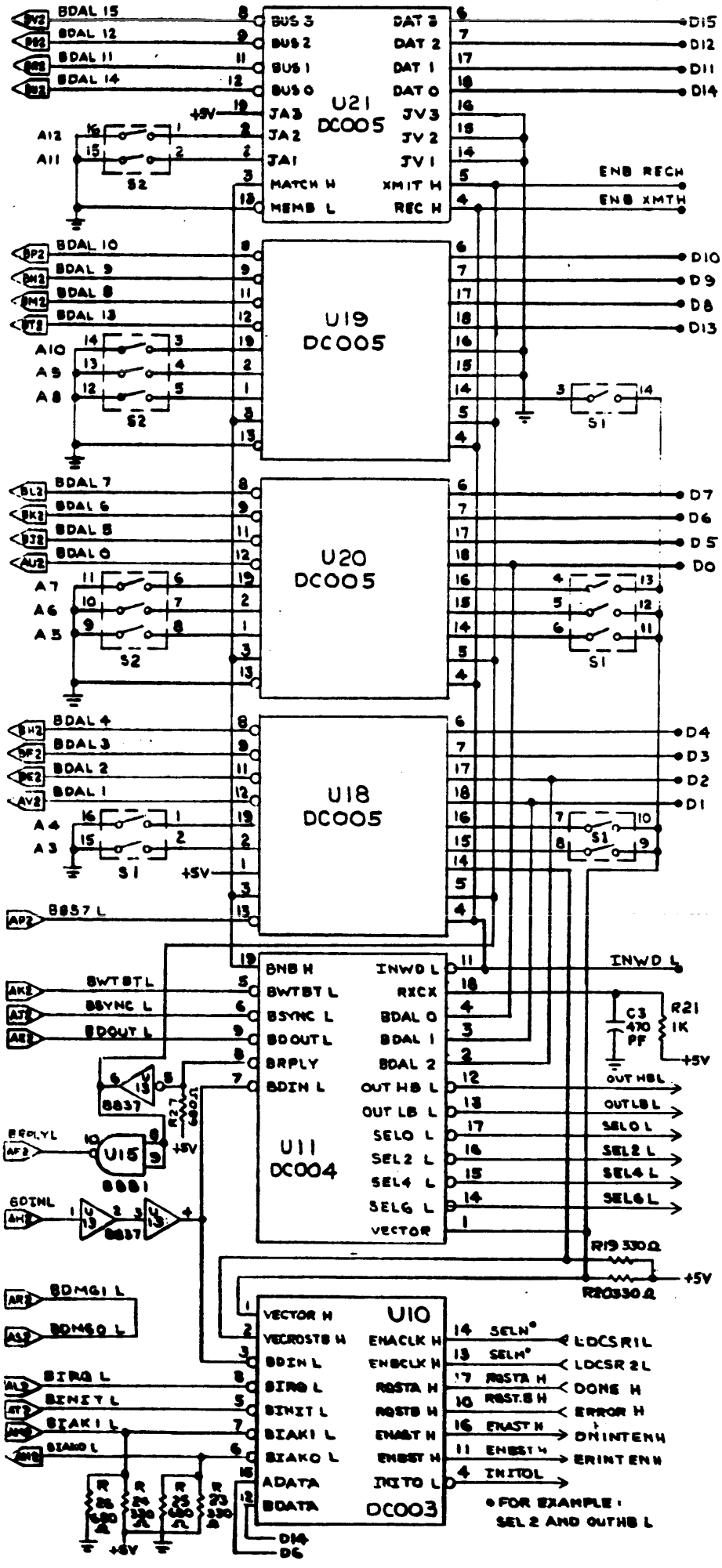
REVISION	ECO NO.	DATE	DWN	ENG
D	# 127	11-14-78	K.F.C.	

DATA TRANSLATION INC

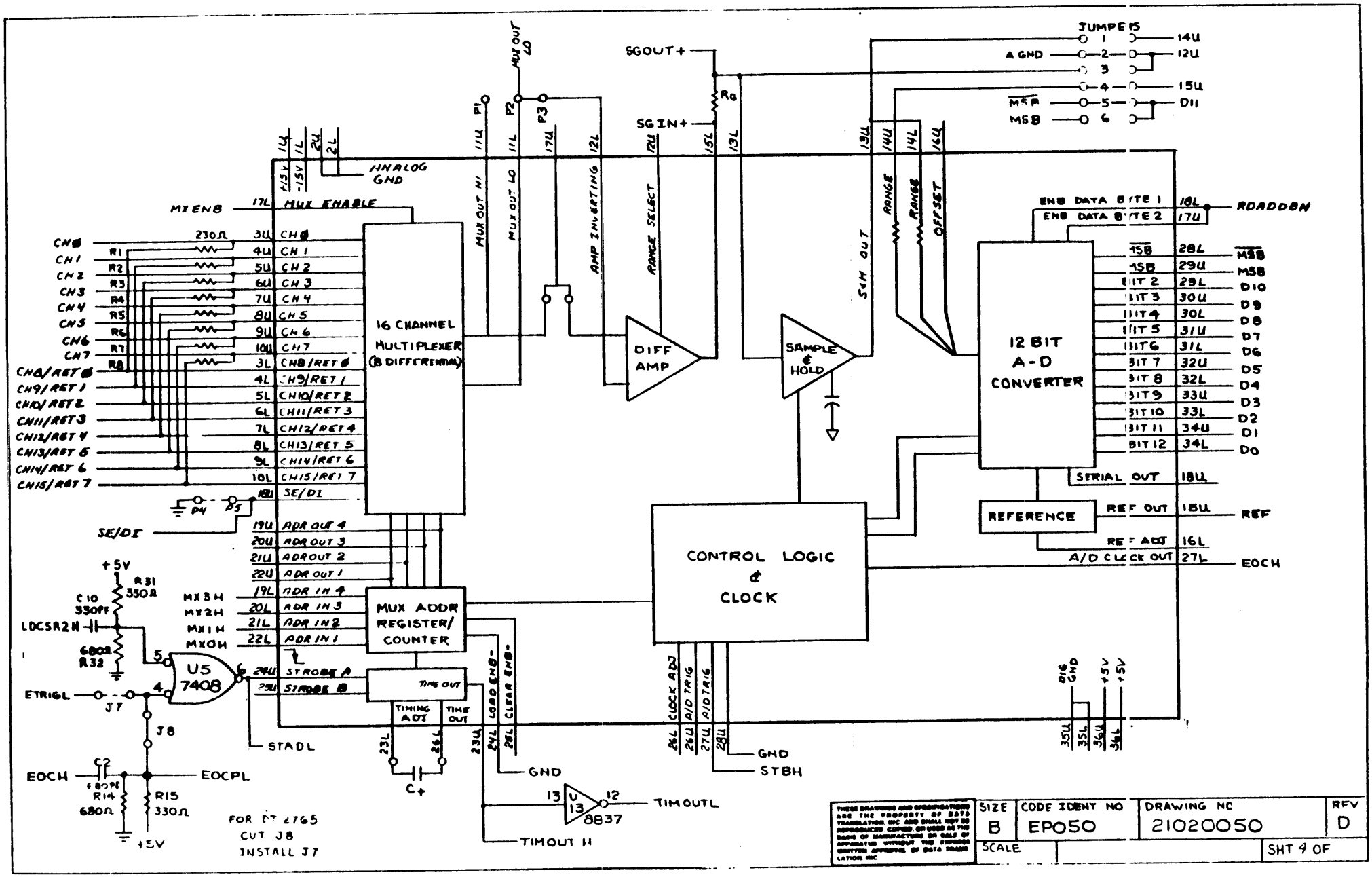
4 Strathmore Rd., Natick MA 01760
(617) 655-5300 Telex 948574

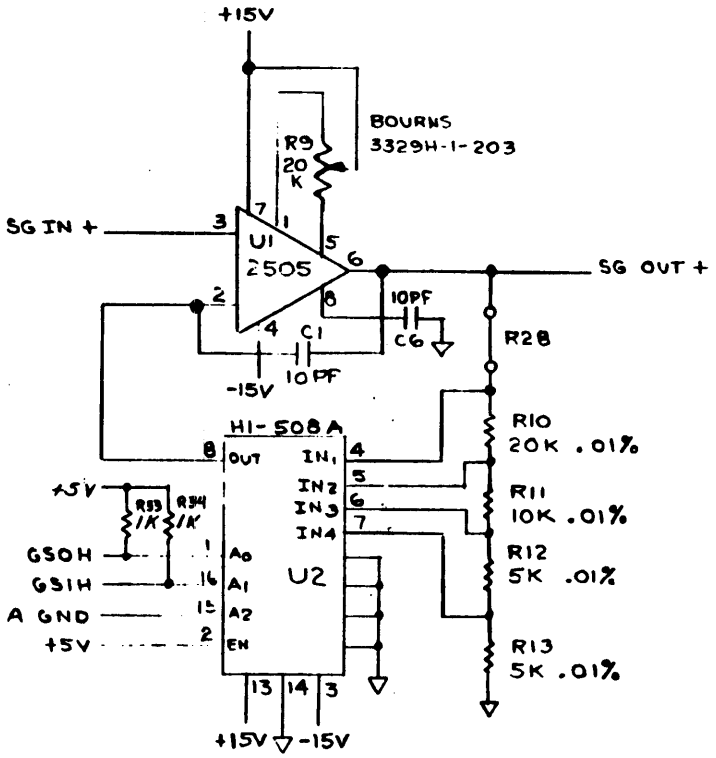
DRAWN: K.F.C.	DATE: 11-10-78	TITLE: SCHEMATIC ANALOG INPUT SYS. DT2762
CHECKED:	DATE: 6-27-78	
ENG: J. V. J.	DATE: 6-26-78	
EP050	SHT 1 OF 6	SIZE B
		DWG NO. 21020050
		REV D

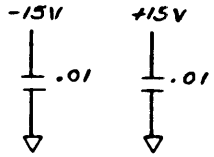

25S18
U14
D2
D3
D4
D5
LDCSR1L
RDCSRL
GSCH
GS1H
EXT TRIG ENH
RTC ENH
D2
D3
D4
25S18
U8
D8
D9
D10
D11
LDCSR2H
RDCSRL
MX0H
MX1H
MX2H
MX3H
D8
D9
D10
D11
25S18
U12
D12
D13
LDCSR2H
RDCSRL
MX4H
MX5H
L12
L13
U16
8097
ERRCRH
DONEH
GND
DNINTINH
RDCSRL
ERINT ENH
GND
RDCSRL
D15
D7
D0
D6
D14
D1
U17
8097
D11
RDADDBL
D15
D14
D13
D12
7474
U4
+5V
R16
1K
D0
LDCSR1L
INITOL
TIMOUT L
R34
100Ω
680PF
C7
U7
7400
U9
7410
STBH
ERTC INH
RTCENH
U15
8881
8837
ETRIGH
R35
100Ω
E EXT TRIGH
EXT TRIG ENH
U15
8881
R22
1K
+5V
ETRIGL
680PF
C11
U5
7408
OUTLBL
SELOL
OUTHBL
SELOL
INWDL
SELOL
INWDL
SEL2L
U6
7432
LDCSR1L
LDCSR2L
RDCSRL
RDADDBL
+5V
R18
1K
U15
8881
LDCSR2H
U9
7410
RDADDBH
7474
U3
+5V
R17
1K
EOCPL
DONE H
INITOL
RDADDBL
U5
7408
7474
U4
SETFRL
D15
LDCSR2L
INITOL
ERROR H
DONE H
STBH
STBH
EOCH
TIMOUTH
ETRIG H
U7
7400
U9
7410
8837
SET ERL
C8
680PF
RTC INH
ERTCINH
270Ω
R29
IN4148
CR1
C9
680PF
EXT TRIG H
E EXT TRIGH
270Ω
R30
IN4148
CR2
SIZE
B
CODE IDENT NO
EP05C
DRAWING NO
21020050
REV
D
SCALE
SHT 2 OF



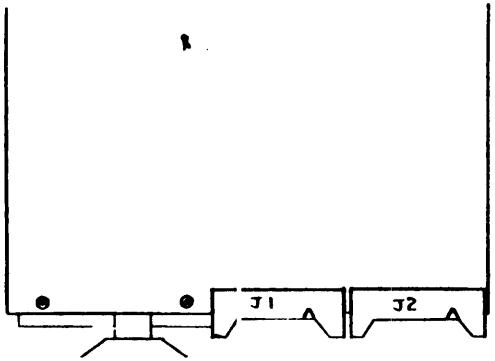
FINGER CONNECTIONS


JUMPERS
AGND
MSB
MSB
14U
12U
15U
D11
MUX OUT LO
MUX OUT HI
AMP INVERTING
RANGE SELECT
SGOUT+
SGIN+
RG
ANALOG GND
+15V
-15V
MUX ENABLE
MUX ENB
230Ω
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8/RET 0
CH9/RET 1
CH10/RET 2
CH11/RET 3
CH12/RET 4
CH13/RET 5
CH14/RET 6
CH15/RET 7
SE/DI
16 CHANNEL MULTIPLEXER (8 DIFFERENTIAL)
DIFF AMP
SAMPLE & HOLD
SAM OUT
RANGE
RANGE
OFFSET
12 BIT A-D CONVERTER
ENB DATA BYTE 1
ENB DATA BYTE 2
RDADDBN
MSB
MSB
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
SERIAL OUT
REFERENCE
REF OUT
REF ADJ
A/D CLOCK OUT
REF
EOCH
CONTROL LOGIC & CLOCK
ADR OUT 4
ADR OUT 3
ADR OUT 2
ADR OUT 1
ADR IN 4
ADR IN 3
ADR IN 2
ADR IN 1
MUX ADDR REGISTER/ COUNTER
MX3H
MX2H
MX1H
MX0H
STROBE A
STROBE B
TIME OUT
TIMING ADJ
TIME OUT
LOAD ENB-
CLEAR ENB-
CLOCK ADJ
A/D TRIG
A/D TRIG
STBH
GND
STADL
+5V
R31 330Ω
C10 330PF
LDCSR2H
680Ω R32
U5 7408
ETRIGL
J7
J8
EOCH
C2
EOCPL
R14 680Ω
R15 330Ω
+5V
FOR DT 2765
CUT J8
INSTALL J7
C+
GND
TIMOUTL
U 13 8837
TIMOUT H
DIG GND
+5V
+5V
SIZE
B
CODE IDENT NO
EP050
DRAWING NO
21020050
REV
D
SCALE
SHT 4 OF



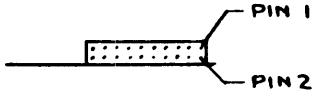


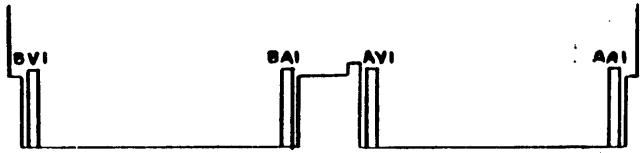
SIZE	CODE IDENT NO.	DRAWING NO	REV
B	EP050	21020050	D
SCALE		SHT 5 OF	



J1 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	MX ØH	2	MX 1H
3	MX 2H	4	MX 3H
5	MX 4H	6	MX 5H
7	MX ENB	8	SE/ DI
9	RTC INL	10	D GND
11	D GND	12	STADL
13	A GND	14	A GND
15	MX OUT HI	16	MX OUT LO
17	A GND	18	-15V
19	A GND	20	+15V

J2 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	CHØ	2	CH8/RET Ø
3	CH1	4	CH9/ RET 1
5	CH2	6	CH10/ RET 2
7	CH3	8	CH11/ RET 3
9	CH4	10	CH12/RET 4
11	CH5	12	CH13/ RET 5
13	CH6	14	CH14/ RET6
15	CH7	16	CH15/ RET 7
17	A GND	18	MX OUT LO
19	EXT TRIG L	20	D GND





BOTTOM EDGE CONNECTOR							
COMPONENT SIDE		SOLDER SIDE		COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
BA1		BA2	+5V	AA1		AA2	+5V
BB1		BB2		AB1		AB2	
BC1		BC2	D GND	AC1		AC2	D GND
BD1		BD2		AD1		AD2	
BE1		BE2	BDAL 2L	AE1		AE2	BDOUTL
BF1		BF2	BDAL 3L	AF1		AF2	BRPLYL
BH1		BH2	BDAL 4L	AH1		AH2	BDINL
BJ1	D GND	BJ2	BDAL 5L	AJ1	D GND	AJ2	BSYNC L
BK1		BK2	BDAL 6L	AK1		AK2	BWTBTL
BL1		BL2	BDAL 7L	AL1		AL2	BIRQL
BM1	D GND	BM2	BDAL 8L	AM1	D GND	AM2	BIAKIL
BN1		BN2	BDAL 9L	AN1		AN2	BIAKOL
BP1		BP2	BDAL 10L	AP1		AP2	BBS7L
BR1		BR2	BDAL 11L	AR1		AR2	BDMGIL
BS1		BS2	BDAL 12L	AS1		AS2	BDMGOL
BT1	D GND	BT2	BDAL 13L	AT1	D GND	AT2	BINITL
BU1		BU2	BDAL 14L	AU1		AU2	BDALOL
BV1	+5V	BV2	BDAL 15L	AV1		AV2	BDALIL

SIZE	CODE IDENT NO	DRAWING NO	REV
B	EP050	21020050	D
SCALE			SHT 6 OF 6

DATA TRANSLATION
INC
4 Strathmore Rd., Natick MA 01760
(617) 655-5300 Telex 948474