Document UM-00049-A

User Manual

for

DT1742/57XX SERIES

DT1742/57XX, DT1744/57XX, DT1751/57XX, DT1755/57XX

HIGH RESOLUTION

ANALOG INTERFACES

For MULTIBUS Systems

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MAXIMUM INPUT VOLTAGE WITHOUT DAMAGE FOR DATA TRANSLATION A/D CONVERSION BOARDS

The multiplexers used in Data Translation A/D converters can be damaged if the input voltages applied to the A/D input connections exceed certain threshold values.

Figure 1 contains the maximum voltage values, both normal mode and common mode, which various Data Translation A/D converter modules can tolerate (Common mode voltages apply only to differential modules, or modules (like the DT5712) jumpered to operate in differential mode.). Note that the maximum voltage which these inputs can tolerate is greatly reduced when the modules are powered down.

Users of Data Translation analog input boards should note the model number of the A/D converter module or input expander module used on their board and check the "MAX VOLTAGE W/O DAMAGE" values listed in Figure 1. The A/D converter or expander module is housed in a 3" long by 4.6" high black steel package. Each is labelled with a model number on the top of the module housing.

WARNING

Applying input voltages to a Data Translation A/D board in excess of the values specified in Figure 1 for the module used on that board will cause irreparable damage to the module, and will void the warranty on the board.

MAXIMUM INPUT VOLTAGE VALUES FOR DATA TRANSLATION MODULES

A/D MODULE	MAX VOLTAGE W/O DAMAGE (POWER ON)	MAX VOLTAGE W/O DAMAGE (POWER OFF)
DT5701	+/-16V	+/-1V
DT5702	+/-35V	+/-20V
DT5703/03EX	+/-15V*	+/-250V
DT5704/04EX	+/-31V	+/-16V
DT5710/10A	+/-16V	+/-1V
DT5712/02EX	+/-35V	+/-20V
DT5716A	+/-16V	+/-1V
DT16EX/48EX	+/-16V	+/-1V
DT5722	+/-16V	+/-1V

*Common mode voltages can be +/-250V without damage. Differential voltage an be 100V for 10ms maximum.

FIGURE 1

NOTES ON USING DATA TRANSLATION A/D BOARDS:

When making connections to Data Translation A/D boards, a few matters should be considered to assure proper operation. PLEASE READ THE FOLLOWING COMMENTS BEFORE OPERATING THE BOARD.

UNUSED ANALOG INPUTS

All unused analog input channels should be connected to Analog Common. Failure to do this can result in inaccurate A/D conversions on channels adjacent to the unused channels.

DIFFERENTIAL INPUTS

The low end of each differential input must be referenced to Analog Common. This can be done by connecting a 10 kilohm resistor between the low end of each differential input and Analog Common.

If all inputs share a common ground, a single 1 kilohm resistor can be connected between the input signal common and the board Analog Common.

SINGLE-ENDED AND PSEUDO-DIFFERENTIAL INPUTS

When single-ended or pseudo-differential inputs are used, you must always reference Amp Low to Analog Common. This can be accomplished by connecting Amp Low to Analog Ground at the point of connection of the user signal.

DATA TRANSLATION

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DATA TRANSLATION

SECTION 1

Data Translation provides high resolution interfaces for the Multibus in various configurations. These subsystems are contained on a single printed circuit board which is exactly plug compatible with Multibus systems. These units are also compatible with the Intel MDS development system.

1.1 Model Configuration

1.1.1 Analog Input Systems - High Level

DT1742 – XX XX / 5716A–B

Number of channels

SE or DI

The DT1742 interface contains a high level analog input system providing 16 bit resolution with the DT5716A module. The interface also contains up to 64 single ended channels or 32 differential channels. Input ranges are from 0 to 10V or ±10V.

1.1.2 High Level Analog I/O System

DT1751 – XX/5716A–B

SE or DI

The DT1751 interfaces contain a high level analog I/O system providing 16 bits of resolution on the analog inputs. Two channels of analog inputs of 16 single ended or 8 differential channels are available. Analog input range is 0 to 10V unipolar or ±10V bipolar.

1.1.3 Options for DT1742, DT1751

PGH - High Level Programmable gain. This option allows the use of software programmable gain with ranges of 1, 2, 4 and 8. Specify with suffix "PGH" onto model number above.

1.2 Wide Range Analog Input System

1.2.1 DT1744–XX XX / 5716A–B

Number of Channels

SE or DI

1.2.1 cont. The DT1744 allows up to 64 single ended or 32 differential inputs with 16 bit resolution.. Input ranges from 10mV to 10V are available by the use of a resistor gain selection.

1.2.2 Wide Range Analog I/O System

DT1755 – XX/5716A–B

The DT1755 is a wide range analog I/O system. The analog inputs can be configured for 16 single ended or 8 differential inputs with 16 bit resolution. The analog outputs are provided as two 12 bit D/A outputs with ranges jumper selectable for 0–10V, ±10V, 0–5V and ±5V.

Analog input ranges are selectable from 10mV to 10V via a precision resistor.

1.2.3 Options for DT1755, DT1744

Precision Resistor Gain Kit - DT13 -10501-4. This kit supplies 7 resistors to set the gain of the system from 10mV Full Scale to 10V Full Scale.

PGL - Low Level Programmable gain - This option allows the unit to be programmed via software. The gains available are 1, 10, 100 and 500. Specify with suffix "PGL" onto model number above.

SECTION 2

HIGH LEVEL INPUT SPECIFICATIONS

2.1 Analog Inputs - DT1742
DT1751

2.1.1 Accuracy /5716A

Resolution	16 bits (1 part in 65,536)
Linearity	±0.003%
Differential Linearity	0.0015% of FSR
Inherent Quantizing Error	±1/2 LSB
Accuracy Gain–1	±0.0075%FSR
A/D Range	±10V
Power Supply Sensitivity	±0.002% FRS/%

2.1.2 STABILITY (TEMPCO)

2.1.2.1	Gain = 1	/5716A
	Gain TC for A/D	±10ppm/°C FSR
2.1.2.2	Differential Linearity TC	±2ppm/°C FSR
2.1.2.3	Gain TC for Instrumentation AMP	±5ppm/°C FSR
2.1.2.4	Zero TC Unipolar for A/D	±8uV/°C
	Zero TC Bipolar for A/D	±12uV/°C
2.1.2.5	Instrumentation Amp Zero TC (RTI)	±10uV/°C
2.1.2.6	Instrumentation Amp Output TC (Zero)	±10uV/°C

2.1.3 ANALOG INPUTS

2.1.3.1 DT1742 - available up to 64 single ended or 32 differential inputs as follows:

16SE	or	8DI
32SE		16DI
64SE		32DI

2.1.3.2 DT1751 - available as 16SE or 8DI inputs

2.1.3.3 INPUT IMPEDANCE - 100 MEGOHMS 10pF "OFF"
100 MEGOHMS 100pF "ON"

2.1.3.4 BIAS CURRENT 10nA

2.1.3.5	Common Mode Input Voltage, max	±11V
2.1.3.6	Maximum Input Voltage with out damage	(Power on) ±27V (Power off) ±12V
2.1.3.7	Amplifier Input Offset Voltage max.	±20uV
2.1.3.8	Amplifier Input Offset Voltage Change over time	±20uV per month ±10uV per year
2.1.3.9	Amplifier Input Noise	1.0 uV rms (Voltage) 2.0 pA rms (Current)
2.1.3.10	Channel to Channel Input Voltage Error	±5uV

2.1.4 DYNAMIC ACCURACY

2.1.4.1	Channel Acquisition Time	30 u DT5716A
2.1.4.2	Throughput Rate	20kHz (400uS/Channel) DT 5716A
2.1.4.3	Sample/Hold Aperture Uncertainty Sample/Hold Aperture Time	50nS 150nS
2.1.4.4	Sample & Hold Feedthrough Attenuation	94 dB down @ 1KHz
2.1.4.5	CMRR (Gain =1)	80db @ 60Hz 1 kohm unbalance
2.1.4.6	A/D Conversion Time	20uS DT5716A
2.1.4.7	Channel Cross Talk	94dB @ 1kHz
2.1.4.8	Sample/Hold Droop Rate	.19 uV/us

2.1.5 PGH - HIGH LEVEL PROGRAMMABLE GAIN

2.1.5.1	Ranges	1 -	10V F.S.	
		2 -	5V F.S.	F.S: Full Scale
		4 -	2.5V F.S.	
		8 -	1.25V F.S.	
2.1.5.2	Gain Accuracy		±0.01%	
2.1.5.3	Gain TC		±5ppm/°C	
2.1.5.4	Zero Accuracy (RTI)		±10uV	
2.1.5.5	Zero TC (RTI)		±2uV/°C	

2.2 Power Requirements

DT1742/571X - +5V @ 1.5A

SECTION 3

PROGRAMMING

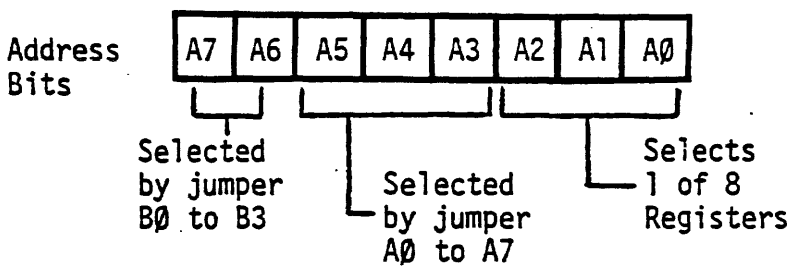
Data Translation interfaces are designed for efficient programming. The interfaces are designed around a control and status register to select operating modes and provide a snapshot of the status of the device. I/O addressing is also utilized so that possible conflicts of present memory utilization or future use of more memory intensive software, such as higher level language and real time operating systems does not produce a conflict with I/O peripherals.

Programming compatibility - DTI interfaces are designed as much as possible to be software compatable within each product line. In this manner the user may utilize one software package for all his applications. This next section describes the programming specifications for the following interfaces:

DT1742/5716A
DT1744/5716A
DT1751/5716A
DT1755/5716A

3.1 General — This series of interfaces are programmed via standard INport and OUTport instructions. Each interface also has the ability to provide an interrupt to the processor for ease of systems programming in real time application.

3.2 Device Address Selection - The I/O address parts for this series are completely jumper selectable in groups of 8 as follows:

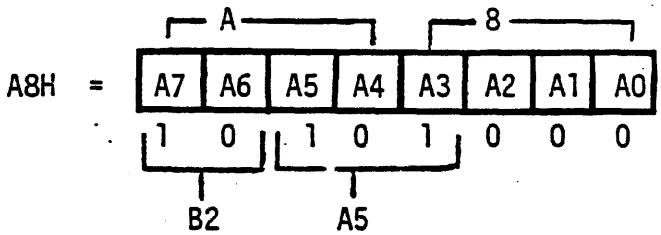


JUMPER	A7	A6
B0	0	0
B1	0	1
B2	1	0
B3	1	1

JUMPER	A5	A4	A3
AØ	0	0	0
A1	0	0	1
A2	0	1	0
A3	0	1	1
A4	1	0	0
A5	1	0	1
A6	1	1	0
A7	1	1	1

REGISTER	A2	A1	A0
MUX-Gain	0	0	0
CSR	0	0	1
ADDB1	0	1	0
ADDB2	0	1	1
DADB1	1	0	0
DADB2	1	0	1
Not used	1	1	0
Not used	1	1	1

JUMPER SELECTION: Selecting the "B" field and the "A" field select a group of eight addresses. For example standard DTI interfaces are configured with a base address of A8H.



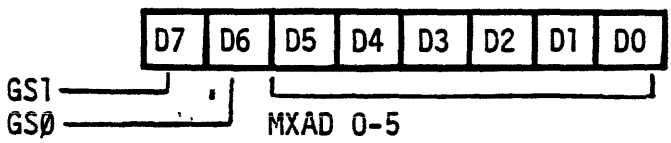
For actual jumper locations see Fig. 3-1

3.3 Register Definitions

3.3.1 Multiplexer - Gain Register MXG

BASE address

A2	A1	A0
0	0	0



An A/D start is initiated upon an out MXG instruction.

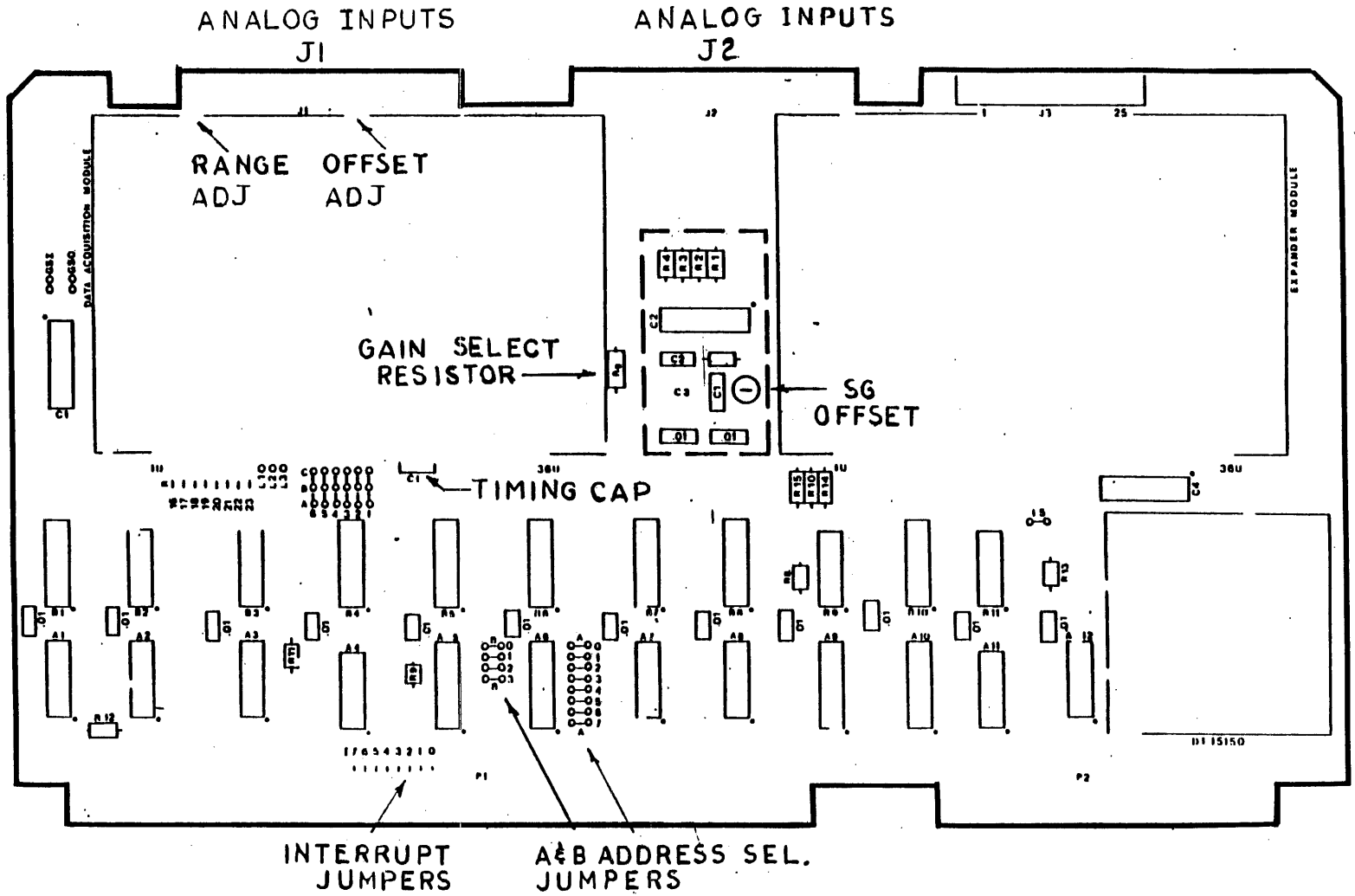


Figure 3–1 JUMPER AND ADJUSTMENT LOCATIONS FOR DT1742/5716A AND DT1744/5716A

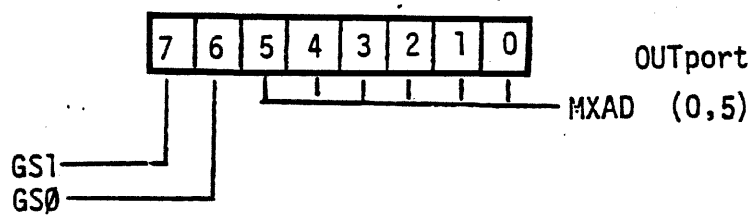
EP040 REV. E

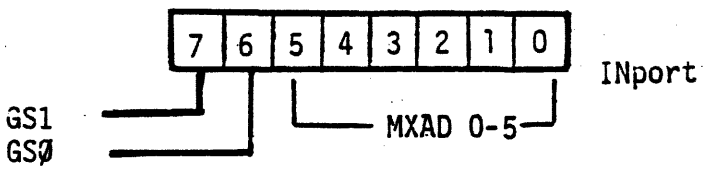
BIT	NAME	DESCRIPTION
7,6	GS1, GSØ	Gain Select Bits - These bits select the gain of the programable gain amplifier option (available on high level systems only).
5 to Ø	MXAD5,0	Multiplexer selection bits. Selects one of 64 mux channels. READ/WRITE

READ / WRITE

GS1	GSO	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

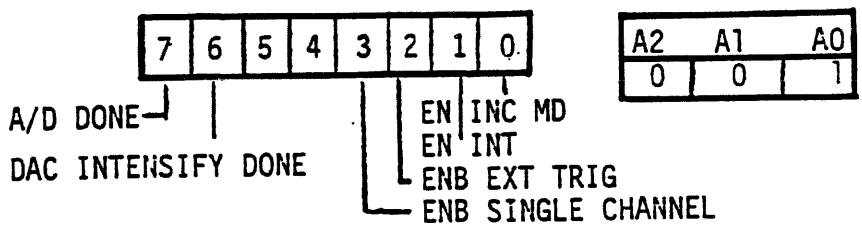
MUX - Gain Register





3.3.2 System Control and Status Register CSR

Address



BIT	NAME	DESCRIPTION
Ø	EN INC MD	Enable Increment Mode - When this bit is set by an OUTport instruction, the converter multiplexer will automatically increment through the channels. See Sec4 for complete operation Set/Reset under Program Control.
1	EN INT	Enable Interrupt - This bit will enable the AN interrupt on the condition A/D DONE. Set/Reset under Program Control.
2	ENB EXT TRIG	Enable External Trig - This bit allows the converter to be triggered via an external source Set/Reset under Program Control.
3	EN SINGLE CH	This bit when set allows the converter to be run on a single channel most efficiently. A channel is set up by the load MUX-GAIN OUTport instruction. Then EN Single CH bit is set and when the conversion is done, a read data buffer is issued. Upon issuing the read ADDB Byte 2 instruction the next conversion is initiated. Set/Reset by Program Control.
6	DAC INTENSIFY DONE	This bit is controlled by the Z output signal. When set bit 6 indicates that the previous intensify is done and the next point can be set up for intensification. This bit is set by the trailing edge of the Z output, it is reset upon loading of the DAC date Byte 2.

BIT	NAME	DESCRIPTION
7	A/D DONE	This bit indicates that the A/D conversion cycle is done and that data in the buffer is valid. It is set by the end of conversion signal from the DATAX module. The A/D DONE bit will produce a program interrupt if bit 1 EN INT in the CSR is set; This bit is reset upon reading Byte 2 of the ADDB, A-D data buffer.

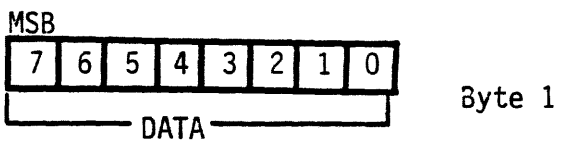
NOTE: All bits in the CSR are cleared by system initialize.

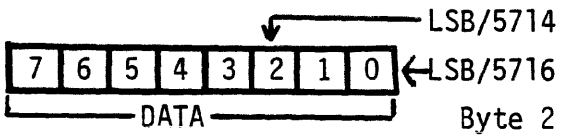
3 3.3 Analog to Digital Converter Data Buffer (ADDB)

Address

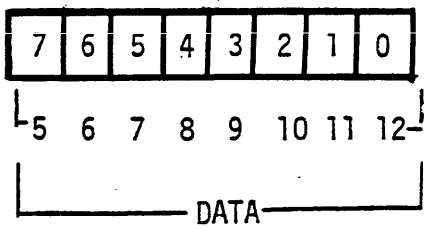
A2	A1	A0	
0	1	0	ADDB1
0	1	1	ADDB2

The A/D converter output is larger than 8 bits, requiring that two (2) Inport instructions be issued to input the full data word. The format for these words is shown as follows:





DADB2



DADB1 Description:

BIT	NAME	DESCRIPTION
7	X-Y SEL	This bit will select whether the X or Y DAC is loaded. Bit 7 = 1 X DAC Bit 7 = Ø Y DAC Set/Reset under Program Control
6	INTENSIFY	This bit will make the Z output of the Scope control logic go true. This bit can only be set by the program, it is reset upon completion of intensity timing.
5-4	MODE	These bits are utilized by the Scope control logic. However, they can be used for any digital output function. They provide four Mode outputs to the user as follows:
3-0	DAC DATA	These bits are the four most significant DAC bits.

Bit 5	Bit 4	Output
0	0	DAC MDØ
0	1	DAC MD1
1	0	DAC MD2
1	1	DAC MD3

Data Format

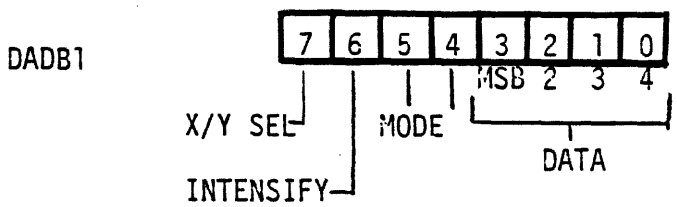
The output coding of the converter depends on whether it is a unipolar or bipolar configuration. The following table illustrates the proper coding for a gain of 1.

		DATA WORD	
CODE	ANALOG RANGE	ADDB1	ADDB2
		7 6 5 4 3 2 1	7 6 5 4 3 2 1 0
UNIPOLAR BINARY NOTATION	0.0000V	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	F.S. - 1LSB	1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
BIPOLAR 2's COMPLEMENT NOTATION	+FS-1LSB	0 1 1 1 1 1 1	1 1 1 1 1 1 1 1
	0.0000V	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	- F.S.	1 0 0 0 0 0 0	0 0 0 0 0 0 0 0

3.3.4 DAC Data Buffer (DADB)

Address	A2	A1	A0
	1	0	0 - DADB1
	1	0	1 - DADB2

The DAC Data word is 12 bits long. Thus two OUTport instructions are required to load the DAC. The DAC input data is buffered so as to prevent the DAC output from spiking upon loading data in 8 bit length. DADB1 however should be loaded first - followed by DADB2. The DAC buffers have the following formats:



DADB2 Description:

BIT	NAME	DESCRIPTION
7-Ø	DAC DATA	The least significant 8 bits of the DAC data word.

Both DACDB Byte 1 and Byte 2 are not provided as INport functions.

DAC Timing

Since the DAC output requires a two word transfer, the DAC and Intensify (Z outputs) are updated at the transfer of Byte 2. Mode bits are updated at the transfer of Byte 1. Thus in normal operation the sequence of instructions must be OUT DAC Byte 1 followed by OUT DAC Byte 2. Since Byte 1 (DADB1) is buffered the DAC outputs and the intensify do not change until an OUT DADB2 is accomplished. However, mode bits will change at load DADB1.

3.4 Modes of Operation

The following section will cover the various modes of operation of the interfaces including programming examples. It will be noted that certain routines are used in many places, such as testing the A/D done bit. These routines can be written and assessed with a call instruction. For convenience the A/D Done test will be shown now and calls to it will be utilized.

A/D DONE BIT TEST:

```
DNE     IN CSR      INPUT CSR
        ORI $ØØ     OR WITH ØØ
        JM DNO      IF DONE SET GO TO DNO
        JMP DNE     IF DONE NOT SET RETEST

DNO     RET
```

Program Controlled Random Address Mode

In this mode the user supplies a gain and MUX channel address. Upon loading this information, a conversion is initiated. Data is available upon receipt of A/D DONE. This can be tested via an INport CSR and J condition address conditional jump or by providing an interrupt on A/D DONE.

```
PROGRAM EXAMPLE:    MVI A, XX       Set up channel #
                    OUT MXG         Load Ch # and Start A/D
                    CAll DNE        Test Done Bit
                    IN AD1          Input ADDB1
                    STAX BC         Store A in location
                                    contained in REG B + C
                    IN AD2
                    INX BC
                    STAX BC         Store ADDB2 in memory
```

This program will start a conversion on the specified channel, test for A/D done bit set and then read data and put it in memory.

Program Controlled Single Channel Mode

The sequence of events in this mode is as follows: First the channel and gain information is loaded via OUTport MUX-Gain instruction. This causes a conversion with the specified parameters. The Enable Single Channel Mode bit should now be set in the CSR. Upon receipt of an A/D DONE the INport A-DDB1 and A-DDB2 instructions are issued bringing in A/D data. Upon the issuance of Inport A-DDB2 the next conversion is initiated. Thus samples can be taken on single channel by just issuing the INport data instructions.

```
PROGRAM EXAMPLE:    MVI D, ØØ        Set conv. counter to Ø
                    MVI A, XX        Load mux-gain and start A/D
                    OUT MXG
                    MVIA, Ø8         Load CSR with Sing CH mode
                    OUT CSR
          TDN       CALL DNE         Test Done
                    IN ADDB1         Input ADDB1
                    STAX BC          Store Data in Memory
                    IN ADDB2         Input ADDB2 and Start A/D
                    INX BC           Increment Reg. B, C
                    STAX BC          Store DATA in next Memory Loc.
                    INR D            INC. Conv. Counter
                    MOV A,D
                    CPI FF           Compare with FF
                    JZ NEXT          If equal go to next routine
                    JMP TDN          If not equal repeat
          NEXT      -
```

This routine will take 256 conversions on the same channel and store them in 256 sequential memory locations.

Program Controlled Sequential Mode

The sequential mode follows the same programming sequence as the Single Channel Mode. The exception is that instead of setting the Single Channel Mode bit in the CSR, the ENINCMD bit is set. Thus upon reading the A/D data buffer, the MUX channel is incremented and a new conversion is initiated.

External Trigger Mode

When the Enable External Trigger bit is set in the CSR, conversion will be initiated by a user supplied trigger pulse. This is especially useful in applications where data must be taken in sync with a real time event.

EXTERNAL TRIGGER CHARACTERISTICS:

The external trigger inputs are available on all interfaces with analog input capability. This input is used to synchronize an A/D conversion with an external event.

Electrical Characteristics

TTL compatable, 1 unit load

Timing Characteristics

Triggering is accomplished on a edge going from plus to minus. The timing diagram shows how this is accomplished.

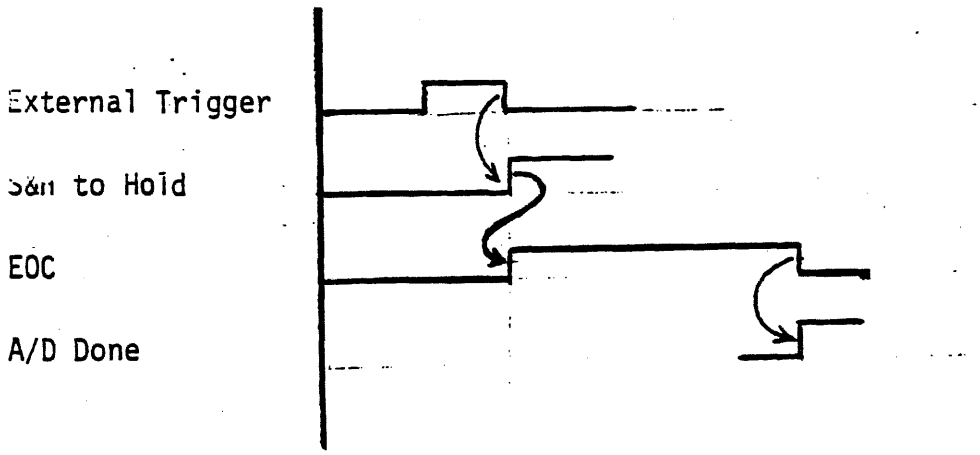


Figure 4.4 External Trigger Timing

As can be seen when external trigger is received, the sample and hold is switched to hold and an A/D conversion proceeds. It should be noted that the mux channel must be settled when this trigger is received.

Programming Considerations:

When the interface is put into external trigger mode, single channel mode need not be utilized. However, increment mode may be used in the following manner.

```
        MVI A, ØØ       Set up channel Ø
        OUT MXG         Output to mux gain & start A/D
        MVI A, 05       Set up increment mode and external trigger
        OUT CSR         Output to control & status reg
A       Call DNE        Wait for DONE
        IN ADI          Input ADDB1
        STAX BC         Store Data in location pointed
                        to BY B&C
        INAD2           Input ADDB2 and increment CH#
        INXBC           Increment memory pointer
        STAX BC         Store Data
        JMP A           JMP to A and wait for external trigger
                        to start a conversion
```

This program will start at CHØ. Then increment through the channels as the external trigger signals come in to start the A/D conversion.

SECTION 4

USER CONFIGURATION/CONNECTIONS

4.1 I/O Port Address Selection

I/O port address selection is explained in Section 3.

4.2 For DT1742 and DT1751 products the configuration is set at the factory by specification of the user at the time of order. For example: DT1742-32DI/5716-B. This specified a high level analog input system with 32 differential input channels, 16 bit resolution and 0-10V unipolar input.

4.3 User Connections

User connections are via a 50 pin edge card connector. Compatible connectors are as follows:

Connector Type	Vendor	Part Number
Flat Cable	3M AMP	3415-0001 2-86792-3
Soldered	AMP VIKING TI	2-583715-3 3VH25/1JV-5 H312125
Wire-wrap	TI VIKING CDC ITT	H311125 3VH25/1JND-5 VPB01B25D00A1 EC4A050A1A
Crimp	AMP	1-583717-1

4.3.1 Input/Output Connection

4.3.1.1 DT1751, DT1755 User Connection Pin Summary
DT1841

ANALOG INPUT		ANALOG OUTPUT	
CONNECTOR J1		CONNECTOR J2	
PIN	SIGNAL	PIN	SIGNAL
1	CHØ	1	X DAC OUT
2	CH8/RETØ	2	X RETURN
3	CH1	3	ANALOG GND
4	CH9/RET1	4	ANALOG GND
5	CH2	5	Y DAC OUT
6	CH10/RET2	6	Y RETURN
7	CH3	7	ANALOG GND
8	CH11/RET3	8	ANALOG GND
9	CH4	9	UNUSED
10	CH12/RET4	|	|
11	CH5	|	|
12	CH13/RET5	|	|
13	CH6	40	UNUSED
14	CH14/RET6	41	Z OUT
15	CH7	42	DIG GND
16	CH15/RET7	43	DAC MDØ
17	ANALOG GND	44	DIG GND
18	ANALOG GND	45	DAC MD1
19	UNUSED	46	DIG GND
|	|	47	DAC MD2
|	|	48	DIG GND
|	|	49	DAC MD3
47	UNUSED	50	DIG GND
48	EXT TRIG		
49	DIG GND		
50	DIG GND		

4.3.2 DT1741, DT1742, DT1744, User Connections, Single Ended

Connector J1				Connector J2			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CHØ	26		1	Analog GND	26	CH36
2	CH8	27		2	Analog GND	27	CH43
3	CH1	28		3	CH63	28	CH35
4	CH9	29		4	CH55	29	CH42
5	CH2	30		5	CH62	30	CH34
6	CH10	31		6	CH54	31	CH41
7	CH3	32		7	CH61	32	CH33
8	CH11	33		8	CH53	33	CH40
9	CH4	34		9	CH60	34	CH32
10	CH12	35		10	CH52	35	CH31
11	CH5	36		11	CH59	36	CH23
12	CH13	37		12	CH51	37	CH30
13	CH6	38		13	CH58	38	CH22
14	CH14	39		14	CH50	39	CH29
15	CH7	40		15	CH57	40	CH21
16	CH15	41		16	CH49	41	CH28
17	Analog GND	42		17	CH56	42	CH20
18	Analog GND	43		18	CH48	43	CH27
19		44		19	CH47	44	CH19
20		45		20	CH39	45	CH26
21		46		21	CH46	46	CH18
22		47		22	CH38	47	CH25
23		48	EXT. TRIG	23	CH45	48	CH17
24		49	DIG. GND	24	CH37	49	CH24
25		50	DIG. GND	25	CH44	50	CH16

4.3.3 DT1741, DT1742, DT1744 User Connections, Differential Inputs

Connector J1				Connector J2			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CHØ	26		1	Analog GND	26	CH20
2	RETØ	27		2	Analog GND	27	RET19
3	CH1	28		3	RET31	28	CH19
4	RET1	29		4	CH31	29	RET18
5	CH2	30		5	RET30	30	CH18
6	RET2	31		6	CH30	31	RET17
7	CH3	32		7	RET29	32	CH17
8	RET3	33		8	CH29	33	RET16
9	CH4	34		9	RET28	34	CH16
10	RET4	35		10	CH28	35	RET15
11	CH5	36		11	RET27	36	CH15
12	RET5	37		12	CH27	37	RET14
13	CH6	38		13	RET26	38	CH14
14	RET6	39		14	CH26	39	RET13
15	CH7	40		15	RET25	40	CH13
16	RET7	41		16	CH25	41	RET12
17	Analog GND	42		17	RET24	42	CH12
18	Analog GND	43		18	CH24	43	RET11
19		44		19	RET23	44	CH11
20		45		20	CH23	45	RET10
21		46		21	RET22	46	CH10
22		47		22	CH22	47	RET9
23		48	EXT TRIG	23	RET21	48	CH9
24		49	DIG GND	24	CH21	49	RET8
25		50	DIG GND	25	RET20	50	CH8

Calibration

Calibration of the system is always done at a gain of 1. The calibration is accomplished utilizing a Calibration Test.

Equipment Required:

Voltage Standard - EDC MV-100 or equivalent.
- SP-028 Data Translation Calibration and Test routine.
- MULTIBUS SYSTEM WITH SYSTEM CONSOLE.

Procedure

1. Apply a calibration standard to the proper input channel

Zero Calibration

For unipolar units (-U models) set the input voltage precisely to 0 volts +½LSB and adjust the zero adjust potentiometer until the converter is just switching from all zeros to plus 1 LSB.

For bipolar units (-B models) set the input voltage precisely to minus full scale +½LSB. Adjust the zero adjust potentiometer until the LSB is just switching from a zero to a one with a one at the MSB position and the remaining bits zero.

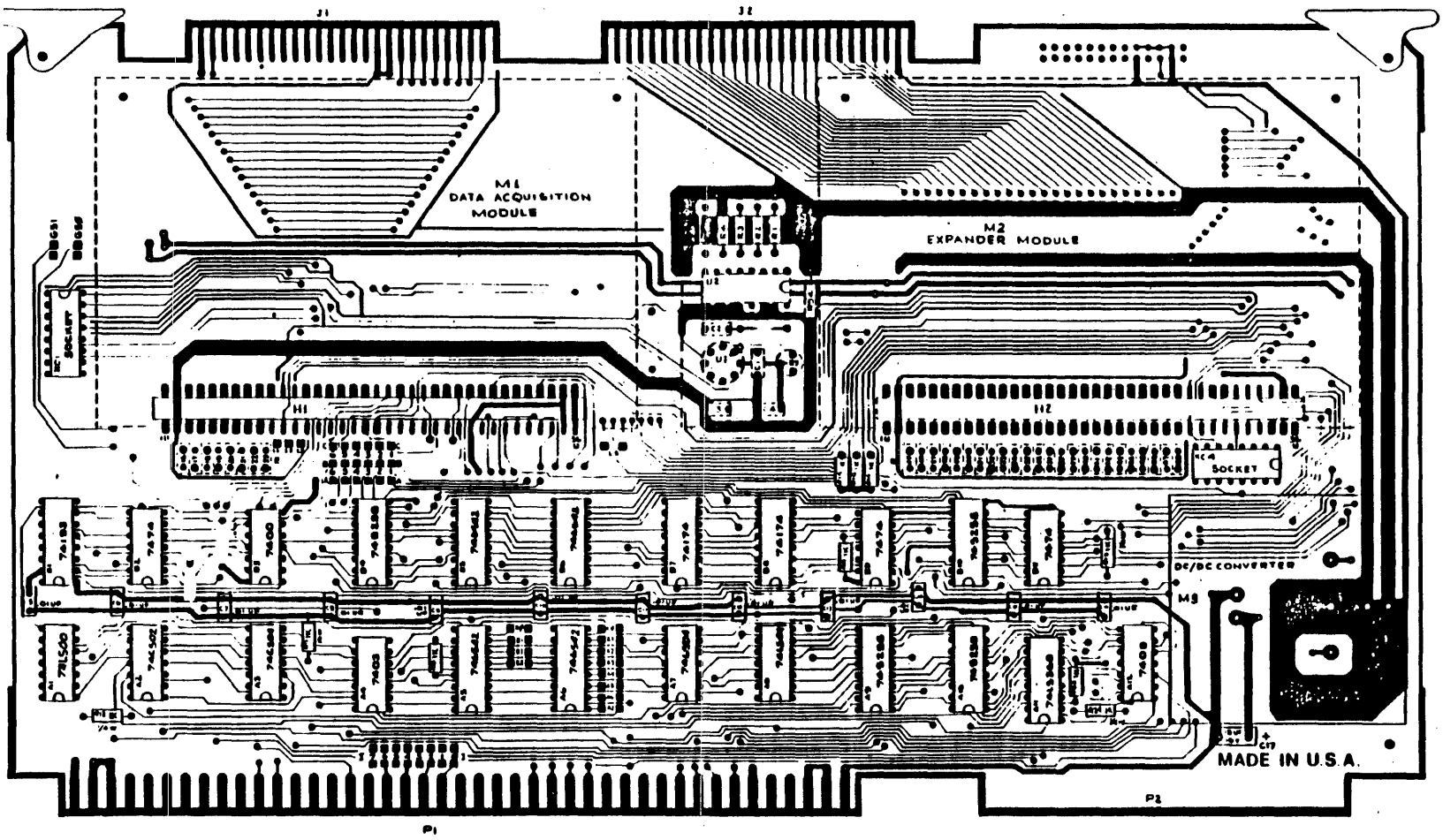
Full Scale Calibration (all models)

Set the input voltage precisely to the plus full scale voltage minus 1½LSB. Adjust the full scale potentiometer until the LSB just switches on with all other bits a 1 with unipolar models and the MSB a 0 and all other bits a 1 with bipolar models.

Table of LSB Values

MODEL	LSB	RANGE
5716-B	305.2 Microvolts	± 10V

ENGINEERING DRAWINGS



NOTE:

1) UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/8 W ±10%.
2) ALL UNIDENTIFIED ITEMS CAN BE DETERMINED BY REFERRING TO TABULATED LIST OF MATERIALS DWG. NO. 00630.
3) FOR SOCKET CONFIGURATION AND OPTIONS SEE SHEET 2.
4) R54 IS NOT INSTALLED FOR -PG OPTIONS.

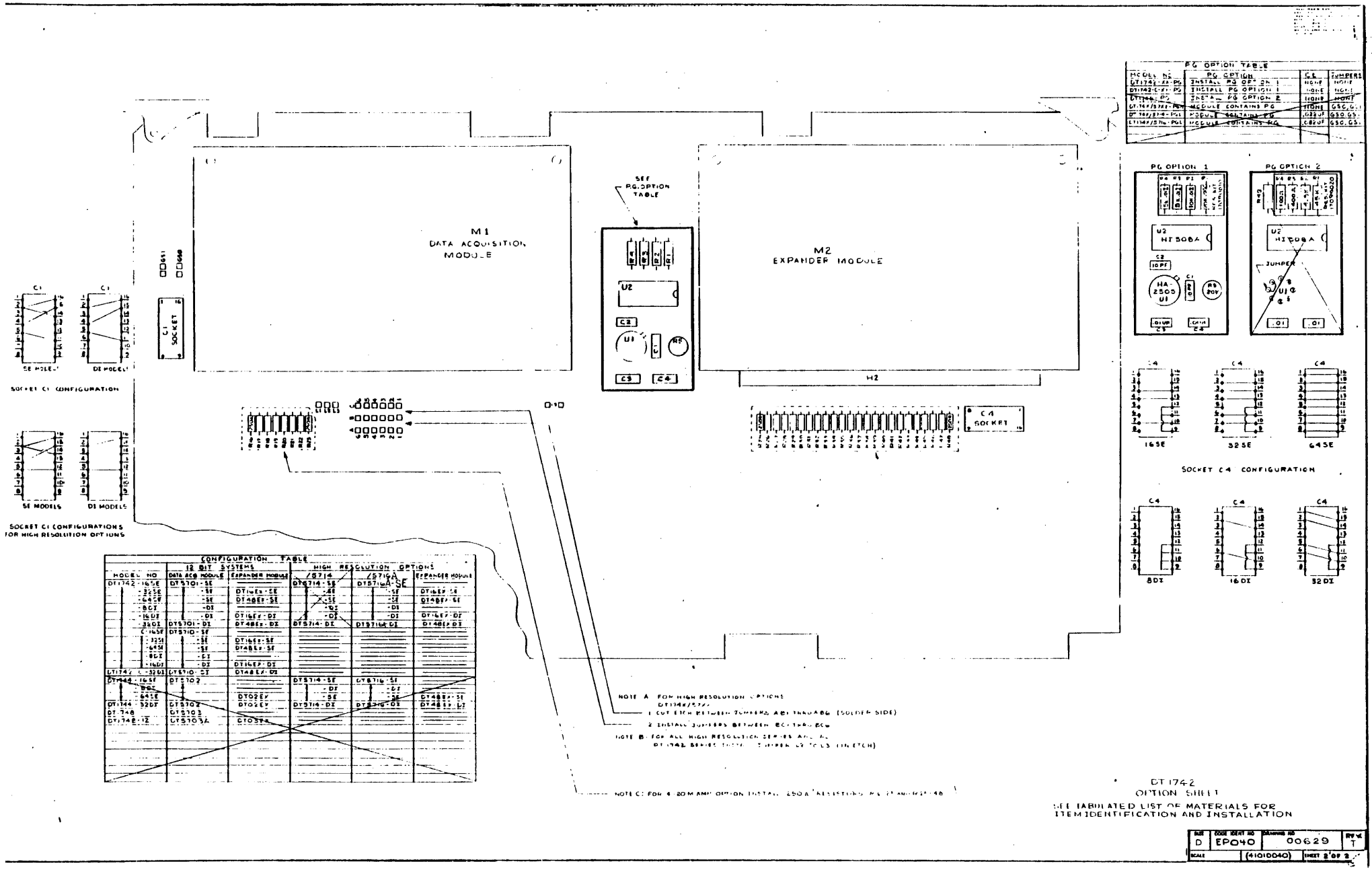
REVISION	ECO NO	DATE	DWN	ENG.
T	.3227		CAR	
S	2277			
R	2067	1-6-85		
P	1772	3-23-84	SL	
N	1738	2-13-84		
M	1638	11-16-83		
L	1092, 1706	11-7-83		
K	593	6-10-82		
J	355	6-8-81		

DATA TRANSLATION INC

DRAWN R.F.C.	DATE 7-11-79	TITLE: ASSEMBLY DWG DT 1742 64 CHANNEL ANALOG INPUT SYS. MULTIBUS
CHECKED R.B.B.	DATE 7-9-79	
ENG. P.J.S.	DATE 7-18-79	
EP040	SHT 1 OF 2	SIZE D

DWG NO 00629 REV T

(4101084-44)



DT1742
OPTION SHEET

SEE TABULATED LIST OF MATERIALS FOR ITEM IDENTIFICATION AND INSTALLATION

SIZE	CODE IDENT NO	DRAWING NO	REV
D	EP040	00629	T
SCALE	(41010040)	SHEET 2 OF 2	

INTRODUCTON TO "INTERFACE BOARD A/D CALIBRATION PROCEDURE"

The following document provides detailed information on calibrating the following Data Translation A/D converters:

1. DT2009
2. DT5701
3. DT5702
4. DT5703
5. DT5704
6. DT5710
7. DT5711
8. DT5712
9. DT5716
10. DT5720
11. DT5722
12. DT5740
13. DT6812

This calibration procedure is divided into discussions of the following: single-ended (section 5.000) versus differential mode (section 6.000); calibration (section 7.000) for unipolar and bipolar ranges; applications (section 8.000), which indicates a number of recommended procedures for improving A/D performance; and troubleshooting (section 9.000). Coding charts and a list of recommended test equipment are also given.

INTERFACE BOARD A/D CALIBRATION PROCEDURE

1.000 INTRODUCTION

1.010 This procedure will cover the calibration of a typical A/D converter, unipolar or bipolar, 12 or 16 bit, using a microcomputer.

1.020 In addition it will provide the hook-up diagrams for single ended and differential operation along with recommended ground connections.

2.000 ASSUMPTIONS

2.010 Calibration will be done on channel 0 with all other channels returned to analog common.

2.020 The input cable is less than 3 meters long.

2.030 Software is available to provide continuous readings of channel 0 and display them on a CRT.

3.000 EQUIPMENT REQUIRED

3.010 Precision voltage source, Electronic Development Corporation model 501J, or equivalent.

3.020 Miscellaneous cables and connectors.

4.000 PRECAUTIONS

4.010 Switch the computer power off when installing or removing the interface board.

4.020 Switch the reference signal (which connects to the analog multiplexer) on only when the board is under power. This will prevent damage to interface boards without multiplexer input protection. A 510 ohm resistor may be installed in series with the input to provide multiplexer protection to ±10 volts with the power off.

5.000 SINGLE ENDED OPERATION (SE)

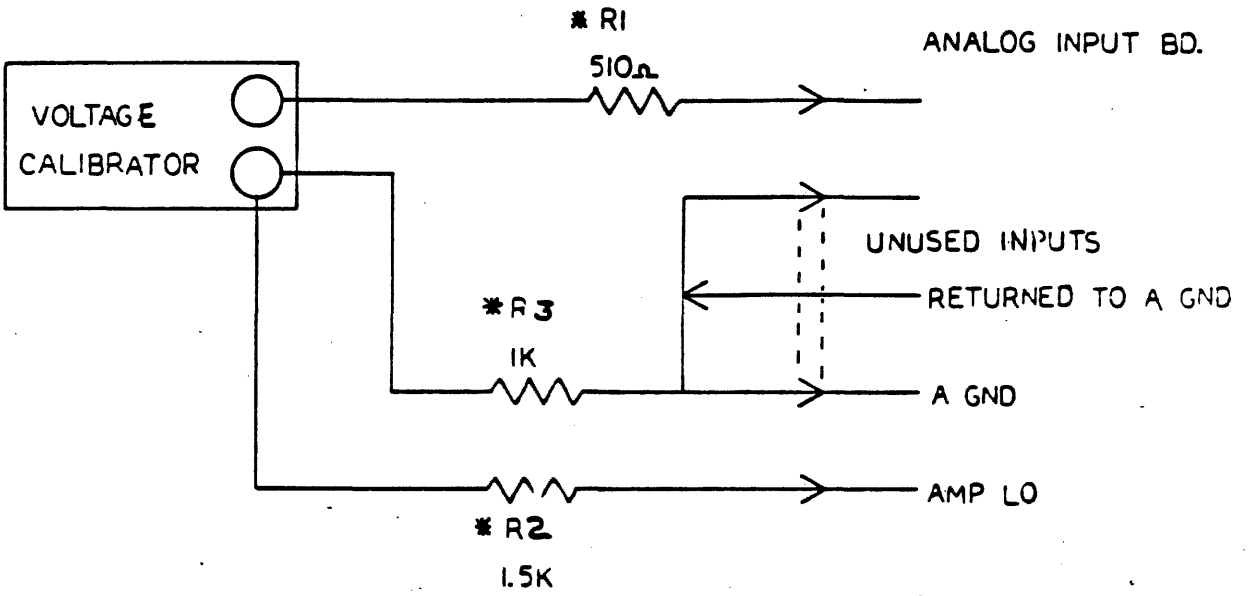
5.010 In the SE mode, all the analog inputs are referenced to a single ground potential.

5.020 If the input has provision for pseudo-differential operation the amplifier lo can be used as a remote ground sense connection to reject a single common mode voltage on all inputs.

5.021 For proper operation the amplifier lo input must be connected to the signal common as close to the signal as possible.

5.022 Note that the input can be balanced by placing the same impedance in series with the amplifier lo input as there is in the signal paths. (Typically, 1 kilohm for the multiplexer plus 1 kilohm for signal source impedances or 2 kilohms total.) Additionally the 2 kilohm resistor will provide current limiting for over voltage conditions.

5.030 HOOK-UP SE



* R1,R2+R3 OPTIONAL AND MAY BE REPLACED WITH A DIRECT CONNECTION

5.031 R1 is used for input protection.

5.032 R2 is used to balance the amplifier input and represents 1 kilohm for the multiplexer plus 500 ohms for the input protecton resistor R1.

5.033 R3 isolates the calibrator lo signal from the analog ground.

6.000 DIFFERENTIAL INPUT OPERATION (DI)

6.010 In the differential mode of operation each input has a hi (ch0) and a lo (ch0 Ret) connection. The measurement taken is the difference between the two inputs, thereby rejecting any noise common to both inputs.

6.020 With non-isolated systems, care must be taken to insure that the inputs are referenced to analog common.

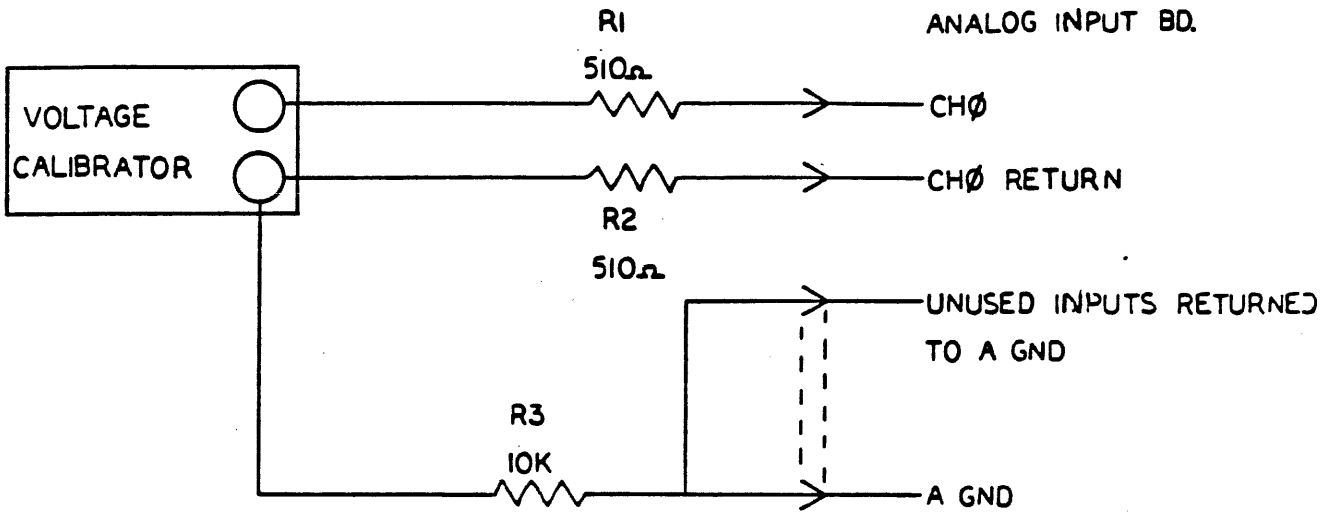
6.021 If the signal to be measured is isolated, a return path for the bias current must be provided back to analog

common. This may be done by connecting a 1 kilohm to 100 kilohm resistor from the signal lo to analog common.

6.022 If all analog inputs are referenced to a single analog common, only one resistor will be required.

6.023 A direct connection could be made; however, this could cause large ground currents to flow if the computer ground potential is several volts different from the input signal ground potential. Even if the signal inputs are isolated from earth ground AC currents could flow due to stray capacitance.

6.030 HOOK-UP DI



R1,R2+R3 OPTIONAL AND MAY BE REPLACED WITH A DIRECT CONNECTION

6.031 R1 and R2 are used for input protection.

6.032 R3 is used to reference the inputs to analog common. Otherwise, they may drift due to bias currents out of the common mode voltage range.

7.000 CALIBRATION

7.001 Allow one hour for the entire system to warm up and stabilize before calibration.

7.010 With software programmable gains the calibration must be done at the gain of 1 first.

7.020 With resistor programmable gain, the calibration is done after the resistor to determine the gain has been installed.

7.030 With jumper selectable gain, the calibration will be done on the selected range.

7.040 When adjusting the potentiometers, center the code on the proper value by noting where the adjacent codes are. That is, mechanically center the pot between the position that yields the desired value plus 1 LSB and the desired value minus 1 LSB.

7.041 A second calibration must be done to eliminate interaction between the adjustments.

7.042 When calibrating an isolated system with PGL gain, the high level (gain of 1) must be done on one channel and

the low level (gain greater than 10) done on another. Otherwise, up to 1 hour could be required to discharge the capacitor when the gain is switched from 1 to 500.

7.060 On a ±10 volt input, the range is 20V. (Range equals the upper input voltage minus the lower input voltage. For ±10V, that is +10V - (-10V) = 20V range.)

7.070 LSB TABLE

INPUT RANGE*	1 LSB SIGNAL FOR: 12 BITS	14 BITS	16 BITS
20V (+/-10V)	4.88 mV	1.221 mV	305.2 uV
10V (+/-5V)	2.44 mV	610.4 uV	152.6 uV
5V (+/-2.5V)	1.22 mV	305.2 uV	76.29 uV
1.25V (+/-.625V)	305 uV	76.29 uV	19.07 uV
.625V (+/-.3125V)	152 uV	38.15 uV	9.537 uV
.100V (+/-50 mV)	24.4 uV	6.104 uV	1.526 uV
20 mV (+/-10 mV)	4.88 uV	1.221 uV	305.2 nV
10 mV (+/-5 mV)	2.44 uV	610.4 nV	152.6 nV
4 mV (1-5V)	976 uV	244.1 uV	61.04 uV
16 Ma (4-20mA)	3.91 uA	976.6 nA	244.1 nA

7.080 ±FULL SCALE -2 LSB VOLTAGE

INPUT RANGE*	12 BIT A/D	16 BIT A/D
20V (+/-10V)	9.9902V	9.99939V
10V (0 to +10V)	9.9951V	9.99969V
5V (0 to +5V)	4.9976V	4.99985V
2.5V (0 to +2.5V)	2.4988V	2.49992V
1.25V (0 to +1.25V)	1.2494V	1.24996V
.635V (0 to +.625V)	.62469V	.624981V
.100V (0 to +.100V)	99.951 mV	99.9969 mV
20 mV (0 to +20 mV)	19.990 mV	19.9994 mV
10 mV (0 to +10 mV)	9.9951 mV	9.99969 mV
4V (1-5V)	4.9980V	4.99988 mV
16 mA (4-20mA)	19.992 mA	19.9995 mA

7.090 FULL SCALE -2 LSB OUTPUT CODE STRAIGHT BINARY CODE

BITS	BINARY	OCTAL	HEX
12	111 111 111 110	007776	OFFE
16	1 111 111 111 111 110	177776	FFFE

7.091 2'S COMPLEMENT CODE

BITS	BINARY	OCTAL	HEX
12	011 111 111 110	003776	07FE
16	0 111 111 111 111 110	077776	7FFE

*See 7.060 for a definition of range

7.100 UNIPOLAR ZERO

7.110 Input 1 LSB of signal (note table 7.070) and adjust the offset or zero adjust potentiometer for 1 count on the digital output.

7.120 On the higher gain ranges, especially at 16 bits, the input can be increased to 10 LSBs to center up the outputs around 10 LSB's due to the noise level.

7.200 UNIPOLAR FULL SCALE

7.210 Input plus full scale minus 2 LSB's and adjust the range or full scale potentiometer for the proper code per 7.080.

7.220 On the higher gain ranges, especially at 16 bits, the input can be reduced 10 LSBs to center up the outputs around full scale minus 10 LSBs.

7.300 PGL AND PGH ZERO

7.310 To calibrate the zero on software programmable gain models (PGL and PGH), first calibrate the zero and full scale at a gain of 1.

7.320 Switch the gain to maximum and apply an input of 1 LSB of the range. For example, at a gain of 8, the full scale range would be 1.25 volts. Thus the input would be 305uV for a 12-bit converter.

7.330 Adjust the amplifier or auxiliary offset for 1 digital count. (Note 7.120)

7.400 BIPOLAR ZERO (2'S COMPLEMENT CODE)

There are two different zero adjustment procedures on bipolar units. Care must be taken to insure that the correct procedure is used. Otherwise, there will be excessive interactions between the zero and full scale adjustments.

7.402 The difference between the two adjustments is that one type is adjusted with zero volts at the input where the other is adjusted with minus full scale plus 1 LSB at the input.

7.403 The following is a list of modules that may be installed on an interface board that requires zero volts at the input for zero calibration:

DT5701	DT5740
DT5702	DT5722
DT5703	DT6812
DT5710	DT2009
DT5720	

7.404 The following is a list of modules that may be installed on an interface board that requires minus full scale plus 1 LSB at the input for zero calibration:

DT5711	DT5716A
DT5712	DT5704

7.410 ZERO CALIBRATION (NOTE 7.4030)

7.411 Input zero volts and adjust the zero potentiometer for all zeros output.

7.420 ZERO CALIBRATION (NOTE 7.404)

7.421 Input minus full scale plus 1 LSB voltage and adjust the zero potentiometer for the correct output code per the table 7.440.

7.430 Minus full scale + 1 LSB output code.

7.431 2'S COMPLEMENT CODE (-FS + 1 LSB) (SIGN EXTENDED)

BITS	BINARY	OCTAL	HEX
12	1 111 100 000 000 001	174001	F801
14/16	1 000 000 000 000 001	100001	8001

7.440 MINUS FULL SCALE + 1 LSB VOLTAGE

INPUT RANGE	12 BIT A/D	16 BIT A/D
20V (+/-10V)	-9.9951V	-9.99969V
10V (+/-5V)	-4.9976V	-4.99985V
5V (+/-2.5V)	-2.4988V	-2.49992V
2.5V (+/-1.25V)	-1.2494V	-1.24996V
1.25V (+/-.625V)	-.62469V	-.624981V
.625V (+/-.312V)	-.31235V	-.312490V
.2V (+/-.1V)	-99.950 mV	-99.9969 mV
.1V (+/-.05V)	-49.976 mV	-49.9985 mV
40 mV (+/-20 mV)	-19.990 mV	-19.9994 mV
20 mV (+/-10 mV)	-9.9951 mV	-9.99969 mV
10 mV (+/-5 mV)	-4.9976 mV	-4.99985 mV

7.500 BIPOLAR FULL SCALE

7.510 Input plus full scale minus 2 LSB's and adjust the range on full scale potentiometer for the proper code per 7.080.

7.511 On the higher gain ranges, especially at 14 or 16 bits, the voltage input can be reduced 10 LSB's to center the output around full scale minus 10 LSB's.

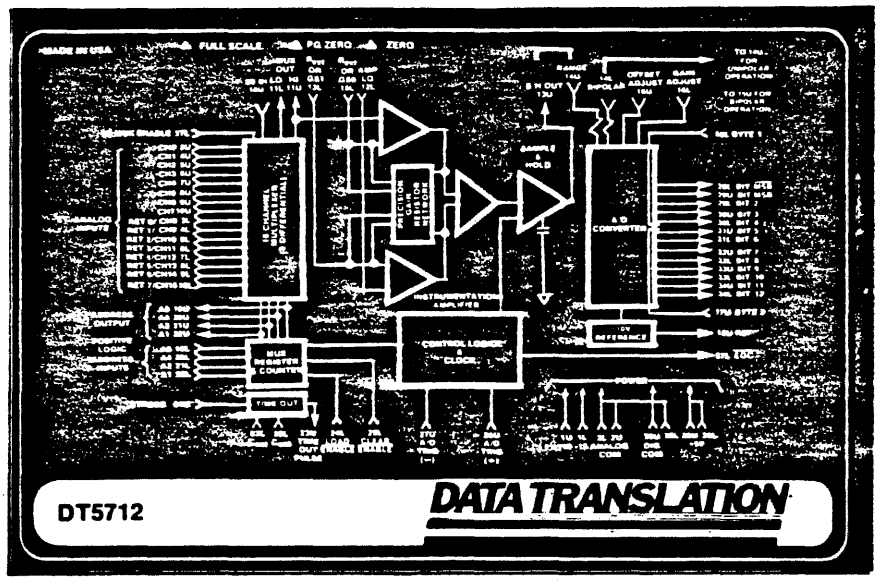
7.600 PGL AND PGH ZERO

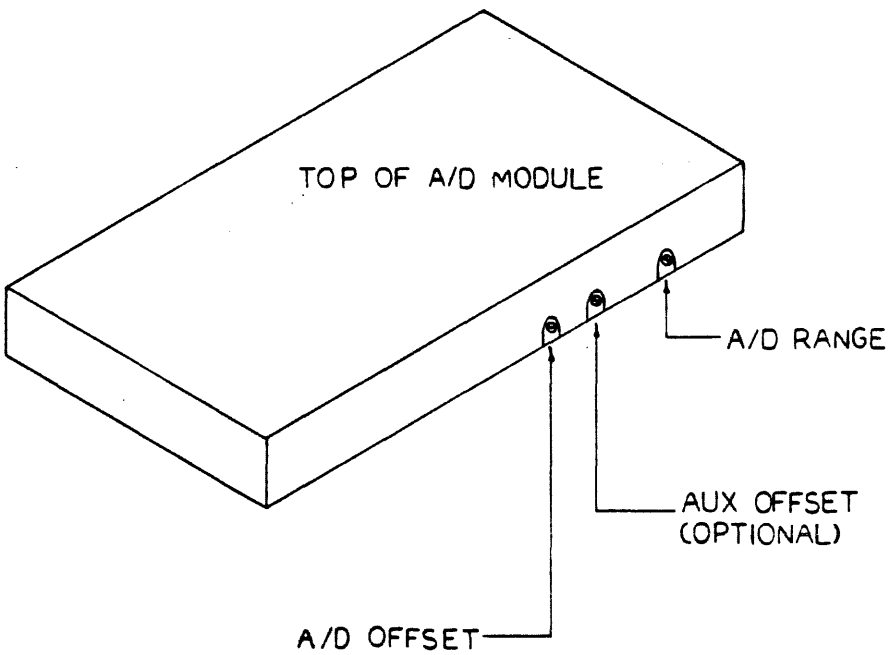
7.610 To calibrate the zero on software programmable gain models (PGL, PGH), first calibrate the zero and full scale at a gain of 1.

7.620 At a gain of 1, apply 0 volts at the input and note the digital output code. It must be all zeros ±1 LSB.

7.630 Set the software programmable gain to maximum and adjust the PG zero or auxiliary zero for all zeros on the digital output.

7.800 POTENTIOMETER LOCATIONS





8.000 APPLICATIONS

8.010 Noise is the major problem with A/D converters. In addition to the accuracy specifications, there is an added noise specification of .2 LSB rms at a gain of 1. In addition, the input amplifier has a noise specification that is multiplied by gain. (3 uV for 12 bits and 1 uV rms for 16 bits.)

8.011 To determine the peak to peak spread of the noise to the 3-sigma points (99.7%), the rms value is multiplied by 6.

8.012 COUNT SPREAD DUE TO NOISE (±10V A/D RANGE)

GAIN	12 BIT A/D	16 BIT A/D
AV = 1	1.2	1.2
8	1.2	1.2
100	1.2	2.3
500	2.2	9.9
1,000	3.9	19.7

8.020 Single ended operations for gains up to 10, A/D conversion rates to 40kHz with a low single source impedance and cable lengths less than 3 meters are usually fine.

8.021 Other than the previous conditions in 8.020, differential inputs should be used.

8.022 All cables must be routed away from switching power supplies and digital signals.

8.023 In high noise environments, the inputs must be differential with shielded twisted pairs for the signal.

8.024 The shield should only be connected at one end.

8.025 Unused inputs should be returned to analog common.

8.026 RC filters can be added at the inputs to remove high frequency noise pick-up.

8.027 Digital averaging of the data can be done simply by adding 16 12-bit A/D conversions and then shifting right 4 times (divided by 16). This is especially useful to minimize the rms noise in high gain applications.

8.100 Input settling time can be a problem if the input cable is over 3 meters in length or the source impedance over 1 kilohm.

8.110 With the following modules, a capacitor can be installed on the board (CT) to allow additional settling time. Note that source impedances greater than 10 kilohms are not recommended due to input impedance errors and bias current errors.

DT5702	DT5722
DT5712	DT5704
DT5716A	

8.111 A typical DT5712 hook-up with 3 meters of cable and a source impedance of 10 kilohms requires a 1 nF capcitor in the CT position. This reduces the maximum throughput to approximately 20kHz.

8.200 GROUNDING

8.210 DIFFERENTIAL INPUTS

When the differential input scheme is utilized, there are two switches per channel. Thus the number of channels is cut in half. The benefits are that common mode voltages, i.e., voltages appearing on both sides of the source simultaneously can be rejected by the differential input instrumentation amplifier. This Common Mode Rejection (CMR) results in a much quieter system. The amount of CMR depends on how well balanced the impedances are on the instrumentation amplifier inputs. (Typical spec. of 80dB at @ 60Hz with 1 kilohm unbalanced.)

8.211 One problem that the user must realize is that even though you have a differential input, the inputs must be referenced back to the analog common of the system. This is because the signal plus common mode voltage range of the input is ±11 volts and if the input is not referenced back to analog common, leakage currents on the input will drive the inputs out of the common mode voltage range thereby saturating the amplifier.

8.212 This ground reference need not be a hard connection but some impedance from 1 kilohm to 100 kilohms.

8.213 It is recommended that this connection be made with a 1 kilohm to 100 kilohm impedance rather than a direct connection to minimize potential ground current through the analog system. For example, the computer analog ground system eventually would be connected back to earthground at a different location, several volts of ground potential between the two could result. If the connections are connected directly, several amps of current could flow through the analog path creating noisy data. If the connection is made through a 1 kilohm impedance, one volt ground difference will only cause one milliamp of current through the analog path thereby creating the minimum disturbance to the analog measuring system. Note hook-up at 6.030, (R3).

8.214 If all the analog inputs have a common connection, the resistor need only be installed once between the two commons.

8.220 SINGLE ENDED INPUTS

8.221 With single ended inputs it is recommended that the inputs be isolated from earthground.

8.222 All the signal commons then would be connected separately to analog common of the board.

8.230 PSEUDO-DIFFERENTIAL

8.231 This mode of operation allows one common mode voltage for all inputs.

8.232 The amplifier low input is used as a remote ground sense wire.

8.233 For example, a metal panel could be used with BNC connectors mounted on it with a common ground. A 1 kilohm resistor could be connected between the panel and analog common to prevent the ground from floating out of the common mode voltage range due to bias currents if the ground is floating. Then the amplifier lo signal could be connected to the panel to sense the panel ground. See note 5.030.

8.240 LOW LEVEL INPUTS (GAIN GREATER THAN 10)

8.241 With low level inputs, it is important to operate differentially and to keep both inputs balanced.

8.242 Shielded twisted pairs with equal resistance and capacitive filtering will minimize noise. However, care must be taken to minimize thermal voltages developed due to connectors in each signal path.

8.243 If the signals pass through a connector, they should be routed through adjacent pins to minimize temperature differences of the contacts.

8.244 Additionally, great care must be taken when selecting the resistors in the input filter. Precision metal film resistors can generate a thermoelectric voltage due to the metal film and copper leads. Generally, Allen Bradley carbon composition resistors have a low thermal voltage.

9.000 TROUBLESHOOTING GUIDE

9.010 Before calling the factory with a problem, the following items should be checked:

9.011 The board should be checked in the factory shipped configuration with the factory shipped diagnostic.

9.020 Make sure the address and vector are set to the proper locations.

9.030 The +5 volt supply must be between +4.75 and +5.25 volts.

9.040 All jumper straps are in the proper locations.

9.050 All cables are connected properly (note pin 1 position).

9.060 No components are making contact to an adjacent card.

9.200 SYMPTOMS AND SOLUTIONS

9.210 NO BOARD RESPONSE

9.211 Check steps 9.010 through 9.060

9.212 Clean board connector fingers with a soft pencil eraser.

9.220 DIGITAL OUTPUT CODE IN PLUS OR MINUS FULL SCALE STOPS

9.221 Check for floating inputs per 8.211.

9.222 Check for floating inputs per 5.021.

9.223 Make sure that the input is not greater than the range that the A/D is on.

9.224 Make sure that none of the other inputs is above the plus and minus power supplies. (±15 volts or ±12 volts on/12 models).

9.230 FIRST READING ON A CHANNEL IS INCORRECT

9.231 Settling time problems due to source impedance over 1 kilohm, or CT not installed for higher gains.

9.232 Note step 8.100.

9.233 Input settling time is budgeted from one linear region to another. If the sample and hold is saturated due to overvoltage on an open channel, the first reading on a valid channel could be in error.

9.240 ZERO WILL NOT CALIBRATE

9.241 The total adjustment range of the zero adjust potentiometer is approximately 50 LSB'S. If there are offsets in the system, such as bridge imbalances, they cannot usually be removed with the A/D zero control.

9.242 Check for the floating input per 5.021.

9.245 With high gains, offsets in the signal path due to thermal voltages can cause zero error that cannot be adjusted out. Note steps 8.240.

9.250 FULL SCALE WILL NOT CALIBRATE

9.251 The total adjustment range of the A/D converter range potentiometer is approximately 50 LSB'S. If there are other gain errors in the system, they cannot usually be adjusted out with the A/D converter potentiometer.

9.252 On resistor programmable gain models, the resistor must have an absolute tolerance of ±.02% or the range potentiometer may not calibrate.

9.260 EXCESSIVE NOISE

9.261 Note 8.010.

Reader's Comment Form

Please use this form to let us know about your experience using this manual. Your suggestions will help us continue to improve the accuracy, organization and overall quality of our user publications.

Manual title: _____

Document UM– _____

What is your general reaction to this manual?

Accuracy	☐ excellent	☐ very good	☐ good	☐ fair	☐ poor
Completeness	☐ excellent	☐ very good	☐ good	☐ fair	☐ poor
Usability	☐ excellent	☐ very good	☐ good	☐ fair	☐ poor

What parts of the manual do you use most:

1. _____ 2. _____

3. _____ 4. _____

What errors have you found?

_____

_____

_____

Additional comments or suggestions:

_____

_____

_____

If we have questions about your comments, may we call you?

____ Yes ____ No

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