Datapoint 3300/Maintenance

Note: this unit does not contain a speed buffer. Reliable operation limited to 600 baud!

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LIST OF ILLUSTRATIONS

INTRODUCTION

This manual is for use by persons with the responsibility to repair and maintain the Datapoint 3300.

The manual is arranged to provide a detailed explanation of the Theory of Operation in a logical sequence.

The theory of operation details all functions within the Datapoint 3300. Review of this section in conjunction with the associated diagrams should thoroughly acquaint the technician with the designed operational characteristics of the equipment.

Extreme caution must be used in replacing a component on any of the printed circuit cards. Recommended tools and techniques to preclude serious damage to the cards are provided in the maintenance section of this manual.

DESCRIPTION

The Datapoint 3300 is a data terminal, incorporating the most advanced electronic engineering, modern design and compatibility with all time sharing services.

To become familiar with the functions of the Datapoint 3300, refer to the Operators Instruction Manual supplied with the equipment.

Table 1-1 provides a listing of dimensions, electrical and interface specifications for the Datapoint 3300.

Table 1-1. Specifications

DIMENSIONS

Width	18 inches
Height	13 inches
Depth	18 inches
Weight	48 pounds

ELECTRICAL

Power Input	200 Watts, 115 VAC, Single Phase, 60 HZ
Heat Dissipation	683 BTU/hr.
Operating Temperature Range	40°F to 100°F
Humidity Limits	0% to 95%
Display Size	10 1/8" to 7 5/8"
Active Display Size	8" x 6"
Spot Diameter	0.01 inches
Repeatability	±0.001 inches
Characters per Line	72
Number of Lines	25
Number of Characters Displayable	1800
Intensity	Adjustable
Brightness	75 ft. Lamberts/Min.
Contrast Ratio	12:1
Types of Phosphor	P31
Character Size	0.11" x 0.18"
Character Generation Method 5 x 7	Dotmatrix
Deflection Type	Magnetic
Deflection Method	Modulated Scan
Character Generator	Read Only Memory
Type of Memories	MOS
Memory Size:	
ROM	2240 Bits
Circulating	10,800 Bits 1800 Characters
Display Refresh Rate	60 Times/Sec.
Character Set	Upper Case ASC II
Cursor	Non-Destructive, Blinking

Table 1-1. Specifications (Cont)

INTERFACE

Serial (Input and Output)	EIA RS-232-B
Bit Rates	110, 220, 440, 880, 1760 150, 300, 600, 1200, 2400
Parallel (Input Only)	Logic Level

SIGNAL CHARACTERISTICS:

(EIA RS-232-B Code)

1. RECEIVE
   a. MARK -3 TO -25 VOLTS
   b. SPACE +3 TO +25 VOLTS

2. TRANSMIT
   a. MARK -10 VOLTS WITH 3K LOAD
   b. SPACE +6 VOLTS WITH 3K LOAD

MAXIMUM SHORT CIRCUIT CURRENT	500 MA
TERMINATING IMPEDANCE	3K to 7K
CONNECTOR TYPE	17-10250-1 Amphenol (or equivalent)

PIN ASSIGNMENTS

PIN NO.	FUNCTION
1	Protective Ground
2	Transmitted Data
3	Receive Data
4	Request to Send
7	Signal Ground
8	Data Carrier Detector
11	Reverse Channel Transmitted Data
12	Reverse Channel Receive Data
18	Read Only Data (See Note)
20	Data Terminal Ready
25	Use for Computer Terminal Test

NOTE

This data may be used to drive a read only copy device and has the same signal characteristics as the normal transmitted data.

Table 1-2 provides the ASC II code assignments for all of the characters and functions used in the Datapoint 3300.

Table 1-2. ASC II Code Assignments

BIT #	7	0	0	0	0	1	1	1	1
	6	0	0	1	1	0	0	1	1
4 3 2 1	5	0	1	0	1	0	1	0	1
0 0 0 0				SP	Ø	@	P		
0 0 0 1			X on	!	1	A	Q		
0 0 1 0				"	2	B	R		
0 0 1 1			X off	#	3	C	S		
0 1 0 0				$	4	D	T		
0 1 0 1		WRU		%	5	E	U		
0 1 1 0				&	6	F	V		
0 1 1 1		BELL		'	7	G	W		
1 0 0 0			c →	(	8	H	X		
1 0 0 1			c ←	)	9	I	Y		
1 0 1 0		LINE FEED	c ↑	*	:	J	Z		
1 0 1 1		c ↓	ESC	+	;	K	[		
1 1 0 0			HOME DOWN	,	<	L	\		
1 1 0 1		RE-TURN	HOME UP	–	=	M	]		
1 1 1 0		SPOW LATCH	ERASE EOL	.	>	N	↑		
1 1 1 1		SPOW UN LATCH	ERASE EOF	/	?	O	←		RUB OUT

c Cursor

DIAGRAM SYMBOLISM

SCHEMATIC AND LOGIC DIAGRAMS

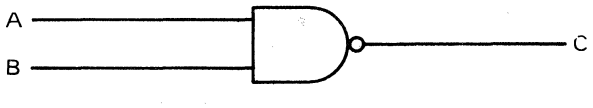
Symbols used on schematic and logic diagrams are generally Military Specification symbols. However, no attempt has been made to conform to Military standards.

The 7400 series, TTL logic family is used. A "one" is high (+5v); a "zero" is low (0v).

Only two types of gates, NAND and NOR are employed.

The small circle used at the input or output of the symbols indicates that the active level is a low.

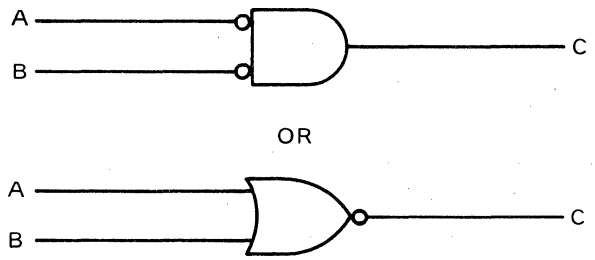
The NAND gate is used in two, three, four, and eight input configurations. The symbol and truth table for the NAND gate are shown in figure 1-1.



AB	C
00	1
01	1
10	1
11	0

Figure 1-1. NAND Gate

The NOR gate is used only in the two input configuration. The symbols and truth table for NOR gates are shown in figure 1-2.



AB	C
00	1
01	0
10	0
11	0

Figure 1-2. NOR Gates

D and JK are the only two types of flip flops used.

The symbol and truth table for the D flip-flops are shown in figure 1-3. The input at D determines which state the Q output will go on the ascending edge of the next clock. The preset and reset lines are not related to clock time and will override any D input at clock time. A low going pulse on the preset will result in a high output at Q. A low going pulse on the reset will result in a high output at $\overline{Q}$.

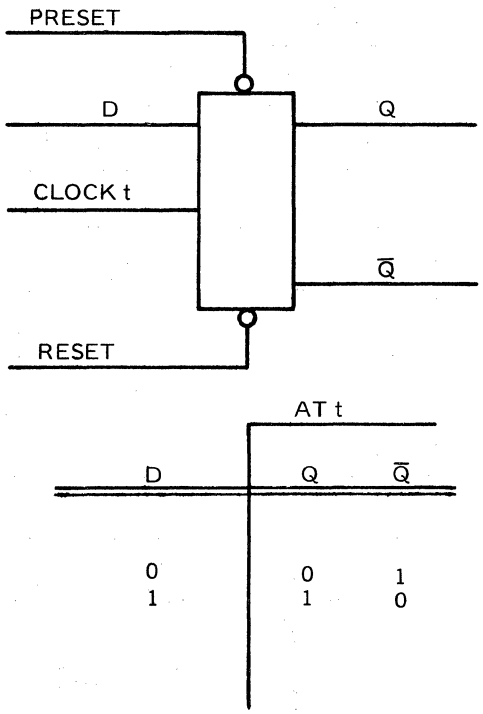
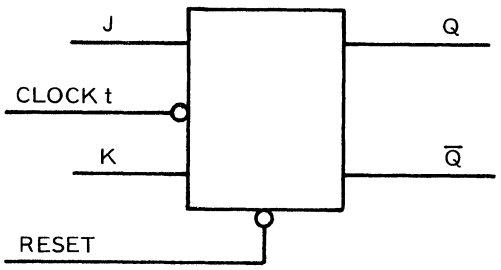


Figure 1-3. D Flip-Flop

The symbol and truth table for the JK flip-flops are shown in figure 1-4. The JK flip-flop utilizes the descending edge of the clock to provide two inputs for control. The J input controls the next state of the Q output and the K input controls the next state of the $\overline{Q}$ output. The J and K inputs are usually complements of each other, however, this is not a requirement. When the J and K inputs are both low, no change will occur at the outputs at clock time. When the J and K inputs are both high, the outputs will complement at clock time. Two variations are used for

inputs to the JK flip-flops. The first provides for one J input and one K input while the second variation provides for three J inputs and three K inputs. The three inputs function as an AND gate and all three J inputs or all three K inputs must be high to reflect a high on the output being controlled.



AT t (DESCENDING EDGE OF CLOCK)

JK	Q	$\overline{Q}$
01	0	1
10	1	0
11	$\overline{Q}$	$\overline{\overline{Q}}$
00	Q	Q

Figure 1-4. JK Flip-Flop

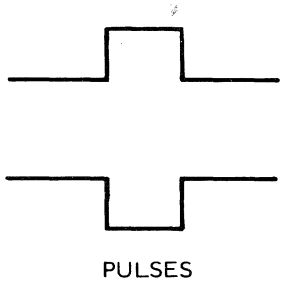
Other special circuits used, such as dividers, counters and one-shots are symbolized by a rectangle with all of the inputs and outputs marked.

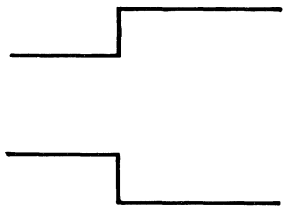
BLOCK DIAGRAMS

The functional block diagrams are composed of circuit elements connected by lines to indicate the direction of information flow. The elements are represented by rectangles with no significance to size. Each rectangle contains a letter designator which represents the general type of circuit. The letter designators are:

G . . . . . Gate
L . . . . . Latch
D . . . . . D flip-flop
JK . . . . . JK flip-flop

The most significant waveforms are shown adjacent to appropriate pins. Figure 1-5 is typical of pulses and levels generally shown in waveforms.





LEVELS, TRANSITION SHOWS DIRECTION OF INITIAL MOVEMENT. LEVEL REMAINS UNTIL OTHER ACTION IS TAKEN.

Figure 1-5. Typical Waveforms

ILLUSTRATIONS

Figures 1-6 through 1-9 show the printed circuit cards used in the Datapoint 3300.

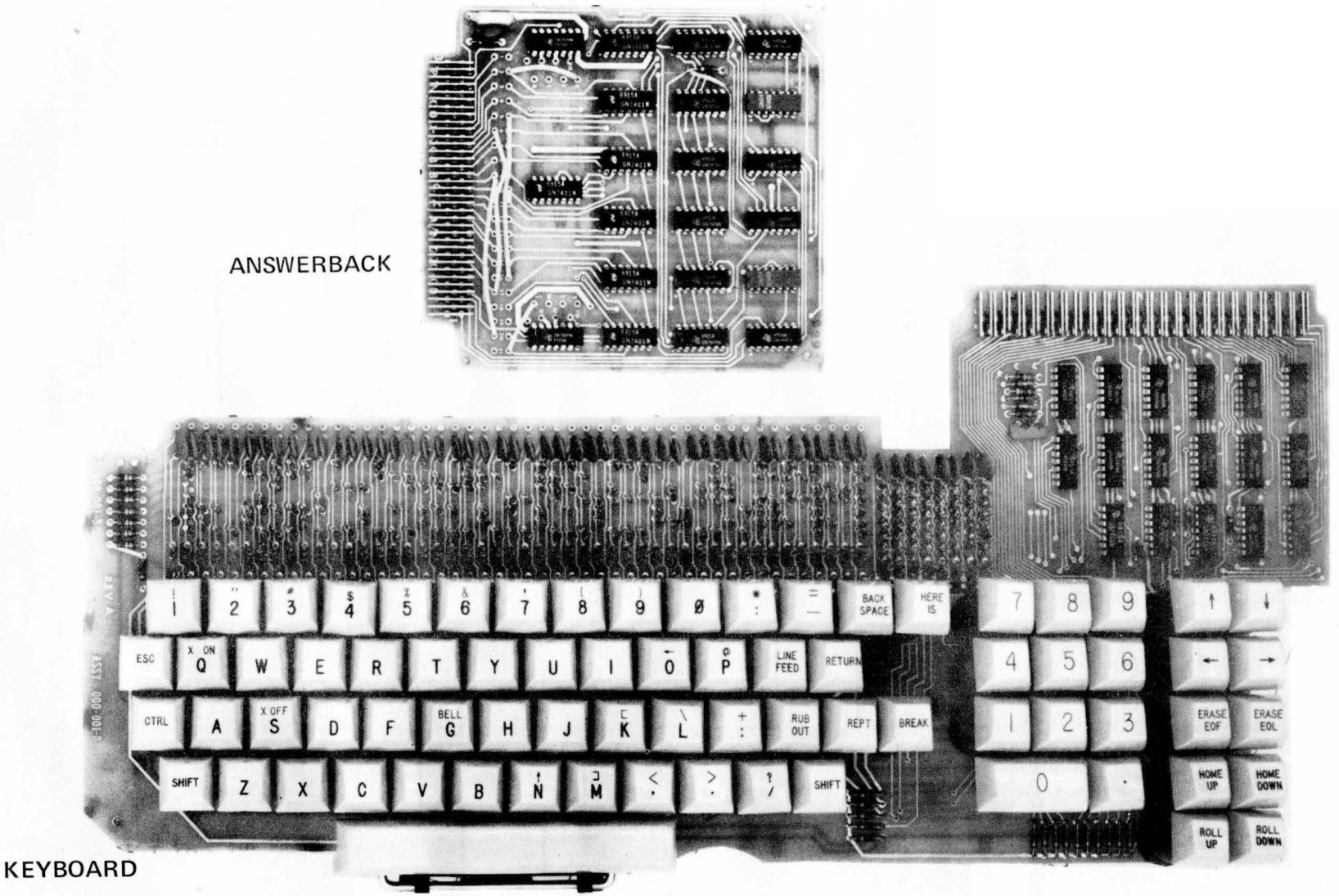
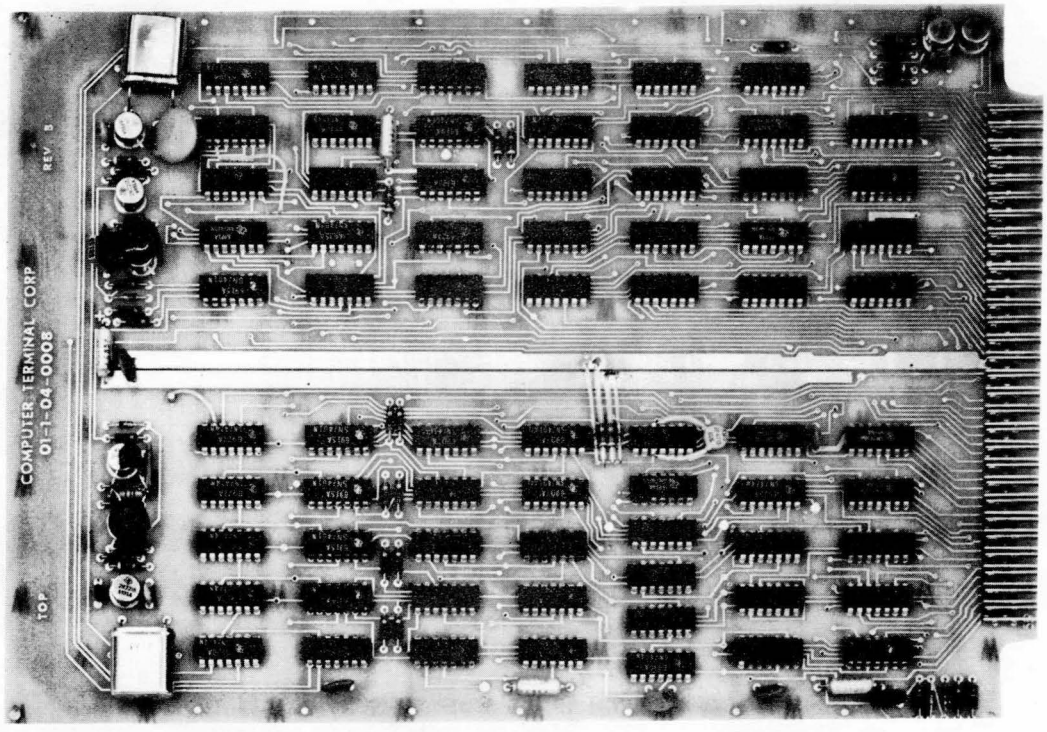
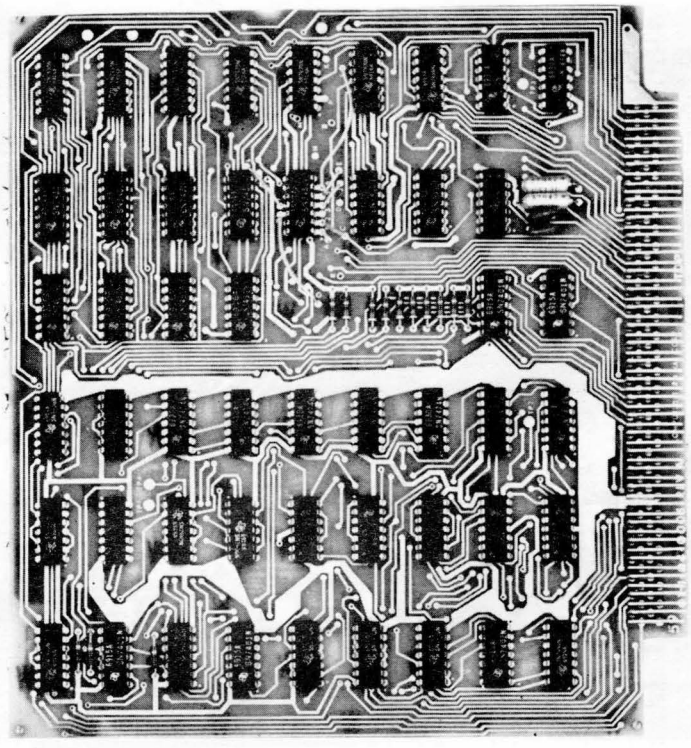


Figure 1-6. Keyboard and Answer-Back Cards

INTERFACE 2

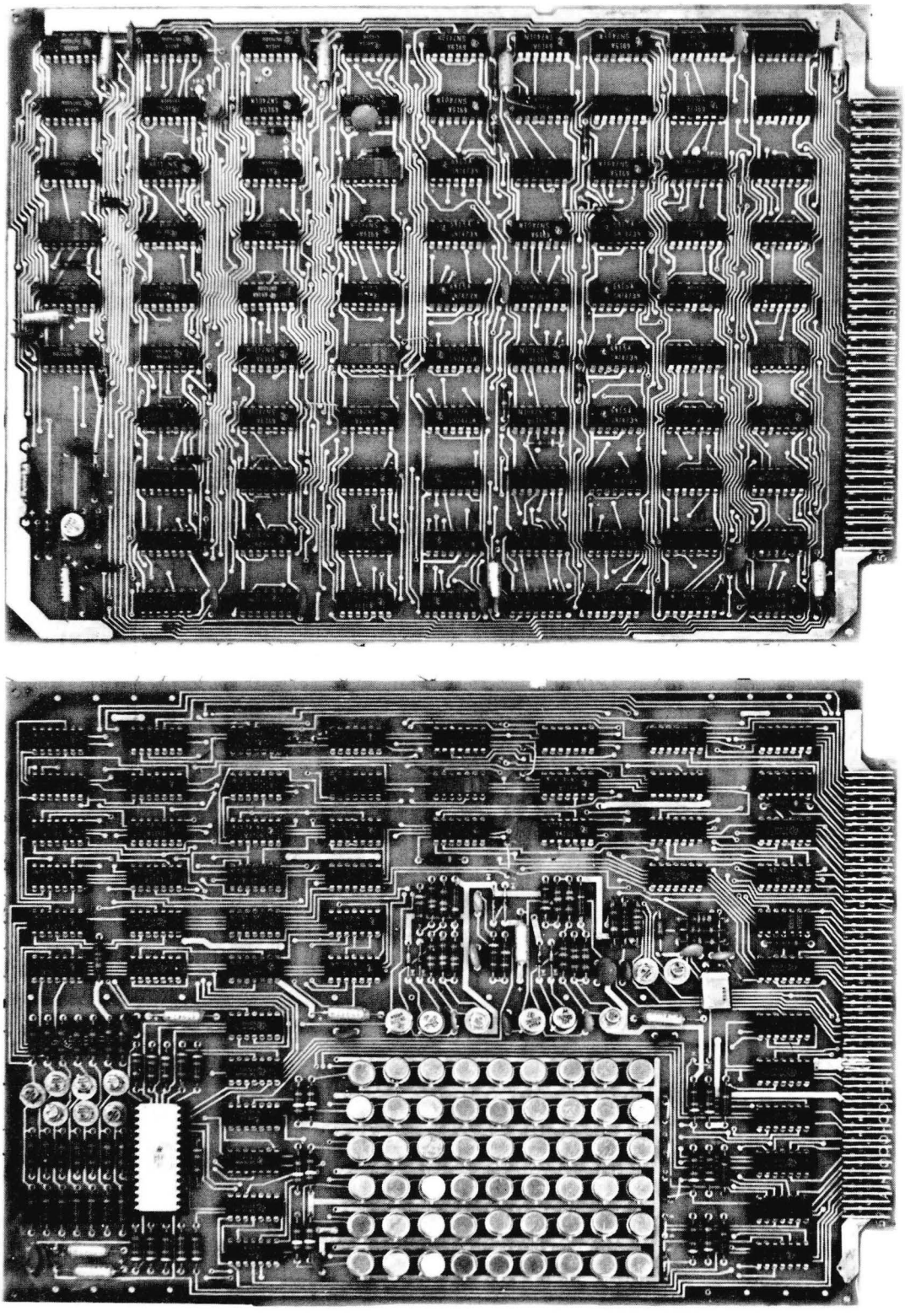




INTERFACE 1

Figure 1-7. Interface 1 and Interface 2 Cards

CONTROL LOGIC



MOS

Figure 1-8. Control Logic and MOS Cards

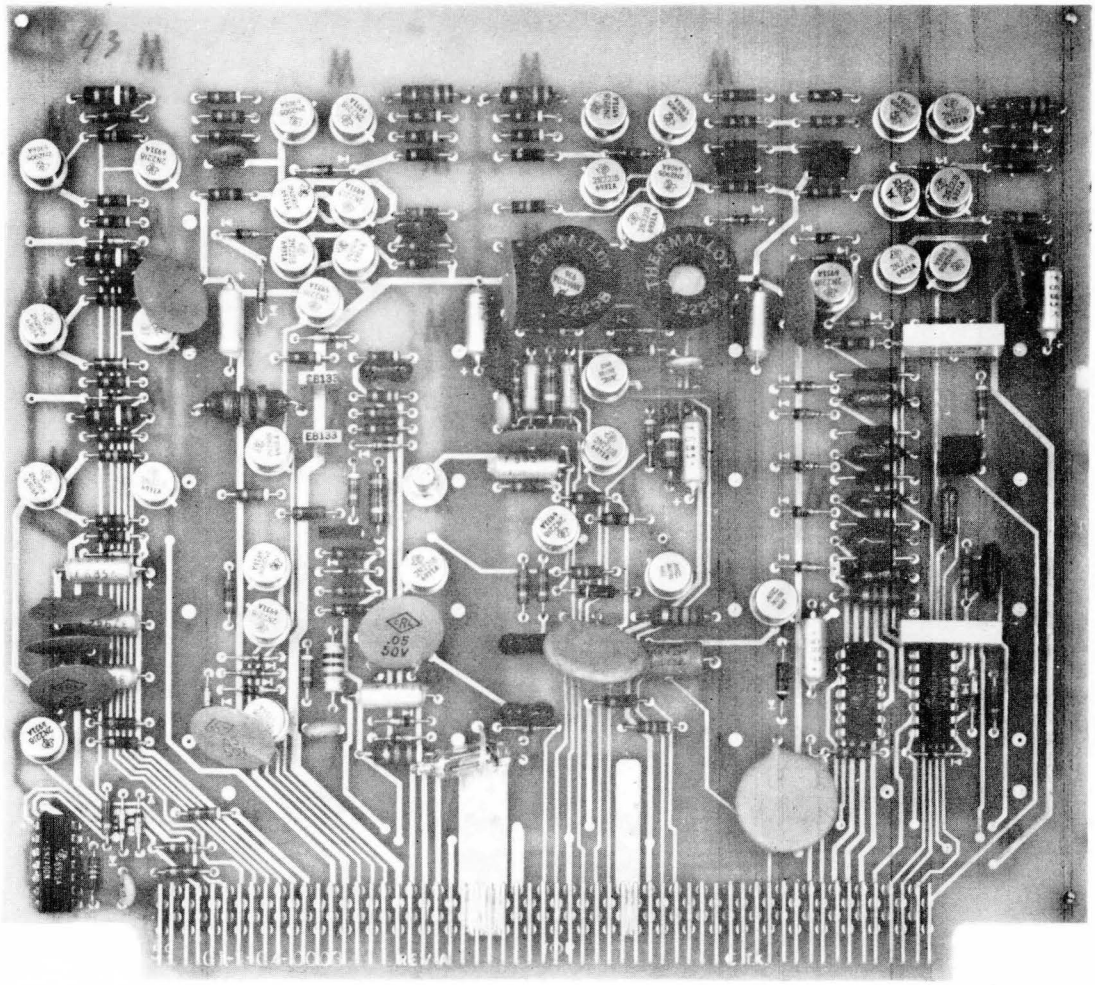


Figure 1-9. Deflection Amplifier Card

DIFFERENCE DATA FOR 50 CYCLE OPERATION

For 50 cycle, 230 volt, operation of the Datapoint 3300, no changes are required on the following cards:

a. Deflection Amplifier
b. Interface I
c. Interface II
d. Control Logic

On the keyboard, a 47K ohm resistor is installed in series with the ON/OFF light bulb.

On the MOS card, install a 24.9 MHz crystal in place of the 26.6 MHz crystal.

The primary power fuse is a 1.25A slo-blow.

Changes necessary in the power supply are:

a. Remove jumpers on transformer T2 from terminals 1 to 3 and 2 to 4.

b. Jumper terminals 2 and 3 together.

c. Check to ensure fan motor is now connected across terminals 1 and 2 of T2.

d. A 15KV high voltage supply designed for 110V 50 cycle input is connected across terminals 3 and 4 of T2. (See figure 1).

The existing filament transformer T1 must be replaced with a UTRAD Corporation transformer, Part Number 5714 revision A. This transformer has a 230VAC input with 6.3VAC output.

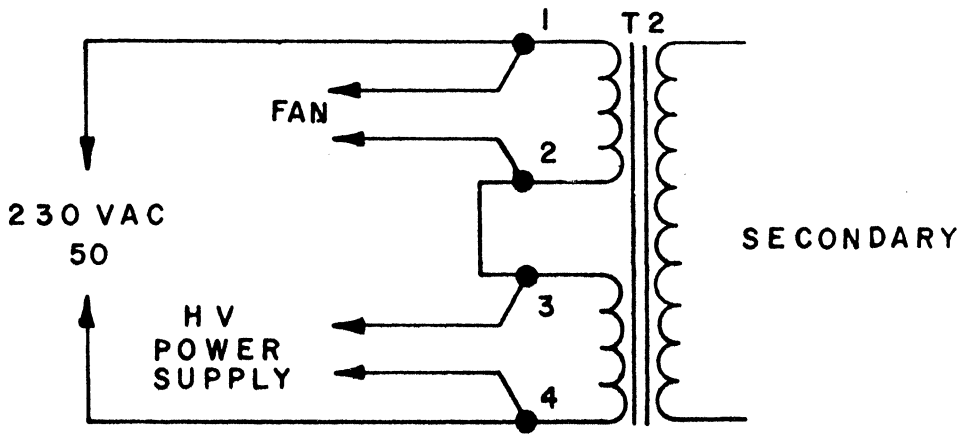


Figure 1

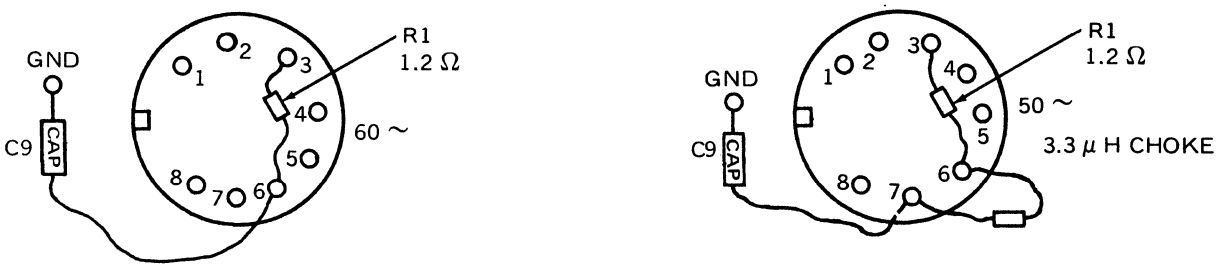


Figure 3

This completes the changes necessary for 50 cycle operation of the Datapoint 3300.

THEORY OF OPERATION

SECTION II

General

The Theory of Operation presented in this section is provided to acquaint the technician with the overall functions and then explain, in detail, functions contained on each card of the terminal. References to particular block diagrams, logic diagrams or schematics should further aid in understanding the operation being explained.

The Data Logic portion will primarily deal with those circuits used in processing data. The Control Logic portion will primarily deal with all of the control functions. References to other sections are noted where inter-relation with another function is explained.

DATA LOGIC

General

The Datapoint 3300 as a complete operational unit consists of two main sections (transmit and receive), power supplies and interface timing. The transmit and receive functions will be covered as separate functions to familiarize the technician with the overall operation of the data terminal. Interface timing and power supplies will be explained in the detailed explanations of the various circuits and printed circuit cards. Reference to figure 2-1 will assist in better understanding the transmit and receive functions.

TRANSMIT FUNCTION

The keyboard is normally considered the source of data to be transmitted, however, provisions have been incorporated to permit parallel data entry from any other auxiliary source, e.g. the Datapoint 3300T. The keyboard or auxiliary source provides seven parallel data bits and a strobe pulse. The strobe occurs after the data bits are stable on the output lines, typically about 600 micro-seconds. The strobe pulse starts the output clock generator that counts down the 8 times selected rate clock provided by the interface oscillator. The output of the clock generator, loads the start space and data into the output shift register, clocks the shift register each bit time and clocks the parity generator during each bit time. During the eighth bit time, the proper parity bit is inserted to produce an even parity followed by either one or two stop marks, depending upon the speed selected. The data is fed serially to the line buffer, located on the deflection card. This circuit converts the digital data signal into the bipolar signal defined in EIA RS-232-B. (See Table 1-1)

Digital data is tapped off the Output Buffer input and connected to the LOCAL/REMOTE and DUPLEX switches. When in Local or Half Duplex mode, digital data is sent to the Receive section and ORed with the data, if any, from the Input Buffer. Transmitted data appears on pin 2 of connector J9.

The Answer-Back optional feature is considered a part of the transmit function. Answer-Back consists of an eleven bit shift register that cycles two times when triggered by receipt of a control "E" or by depressing the HERE IS key on the keyboard. The output of the Answer-Back card is wired to the keyboard matrix to produce a sequential output the same as if the keys were depressed in that sequence.

Depressing the BREAK key generates a space condition on the output line. On early models, the space condition was maintained on the output line as long as the BREAK key was held depressed, however the later models will only provide approximately a 200 milli-second break on the output line for each time the BREAK key is depressed.

In order to repeat a character, the REPEAT key and any other alpha or numeric key must be depressed. This action starts the Repeat Generator which creates keyboard strobes at 7.5 PPS. These repeat pulses are ORed through the same path as the normal keyboard strobe pulses.

RECEIVE FUNCTION

The bipolar EIA RS-232-B signal enters the Datapoint 3300 at Pin 3 of connector J9. The Input Buffer converts this bipolar data to standard logic levels. (1 = high or +5V, 0 = low or 0 volts).

The negative going transition of the start space causes the input bit chopper to start shifting the data into the input shift register. When a full character has been shifted into the register, a flag is raised to the comparator and the data is passed in parallel through the Speed Buffer, if available, into the input hold register.

The Speed Buffer is a circulating memory to provide temporary storage for characters while the trace is returning to the compare or cursor position. The Speed Buffer is only necessary when the input character time is less than the frame time or 16.6 milli-seconds. The Speed Buffer would be required for all data rates above 60 char/sec.

When the compare does occur, the contents of the input hold register is loaded into the circulating memory. When a compare is generated in response to a flag from the input shift register, the circulating data is inhibited at the OR gate to the memory and replaced by the new data.

The circulating memory is driven by a two phase clock at a 135 KHz rate. The two clocks are derived from the cycle generator and converted to MOS compatible levels by the MOS clock drivers. The period between clocks is 7.5 microseconds; therefore, the six parallel bits in the circulating memory are present for this period at the address input to the Read Only Memory (ROM). The six bit character actually defines a block address in the memory or a starting address from which five sequential addresses will be read. The cycle generator provides five sequential pulses to the ROM which causes the five 7 bit words to be read out. Each word represents one column of the 5 x 7 character matrix. While each 7 bit word is present at the ROM output, the dot generator scans each bit position and produces a digital pulse for each "one" present in the word. This pulse is applied to the video amplifier and becomes a visible dot on the cathode ray tube (CRT).

The dots are positioned on the CRT by three yoke windings. The horizontal winding controls the lateral position of the character and is modulated by the minor vertical sweep which controls the individual dot positions. The vertical sweep controls the line position on the CRT. Digital pulses from the memory character counter supply the input for the horizontal ramp generator. The horizontal ramp is generated on the control logic board and passed to the horizontal amplifier on the deflection card. The actual power drivers for each deflection winding are located on heat sinks on the rear panel assembly. A 950 KHz digital signal is the source of the minor vertical deflection which is sometimes referred to as the WRITE deflection. The output of the vertical amplifier for any given line is a constant current level. The current level is controlled by the Digital-to-Analog (D/A) converter which receives its digital input from the memory line counter on the control logic card.

The source for all timing is the master oscillator located on the MOS card. The circuit is a crystal controlled 26.6 MHz oscillator. The output of the oscillator is burst synched to the line e.g. the output is shut off at the end of the frame and is not started again until the power line passes through zero volts going in the positive direction. This technique eliminates any apparent flicker in the display due to a beat between the refresh 60 Hz and the room lighting.

The special character decode monitors the input data for special control characters. The output of this gate array causes various functions to occur, such as CARRIAGE RETURN, LINE FEED, BACKSPACE, BELL, etc.

The cursor control and repeat circuitry located on the control logic card receives the inputs from the various cursor control keys located on the keyboard. This circuitry controls the cursor line and character counters.

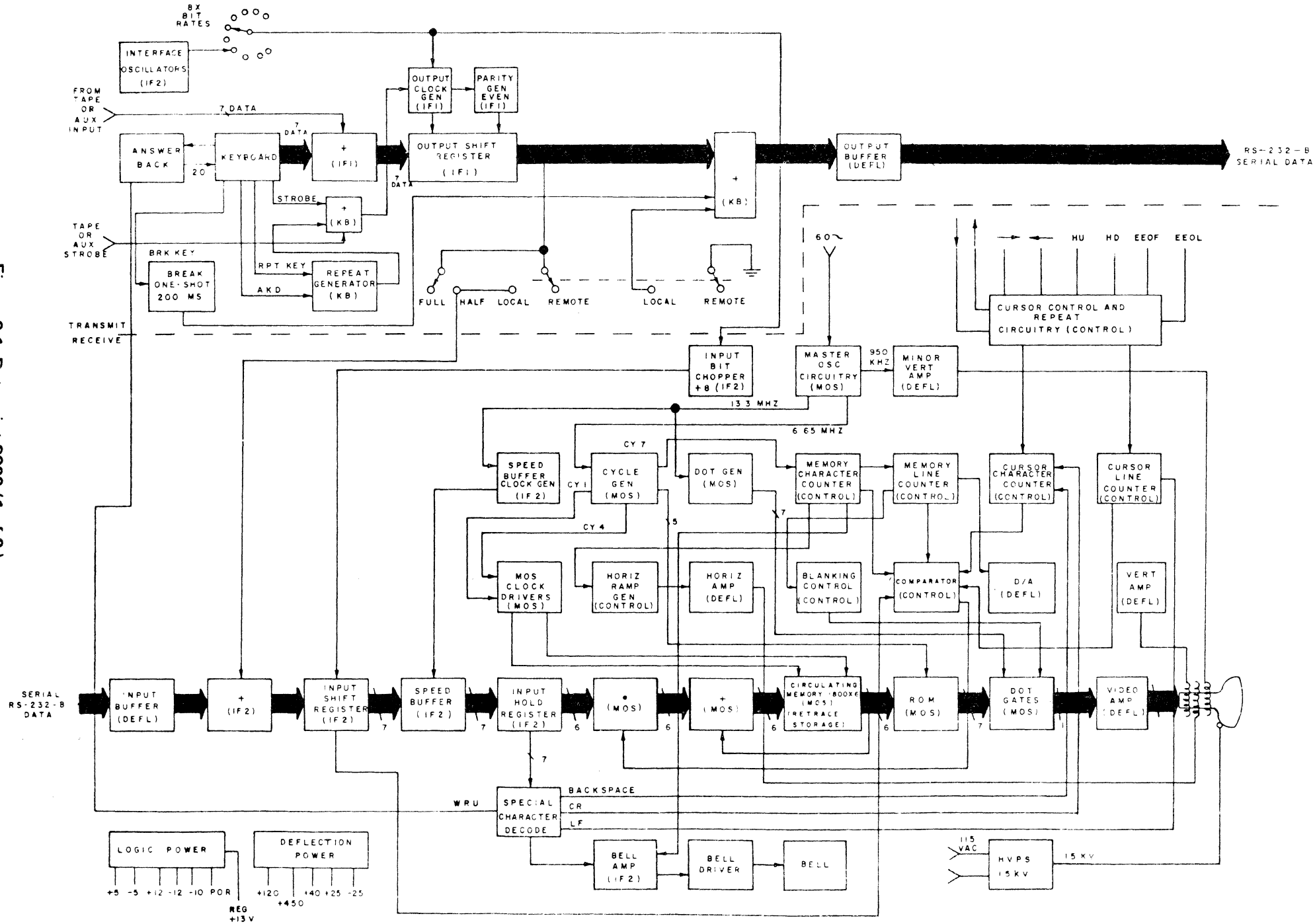


Figure 2-1. Datapoint 3300 (1 of 2)

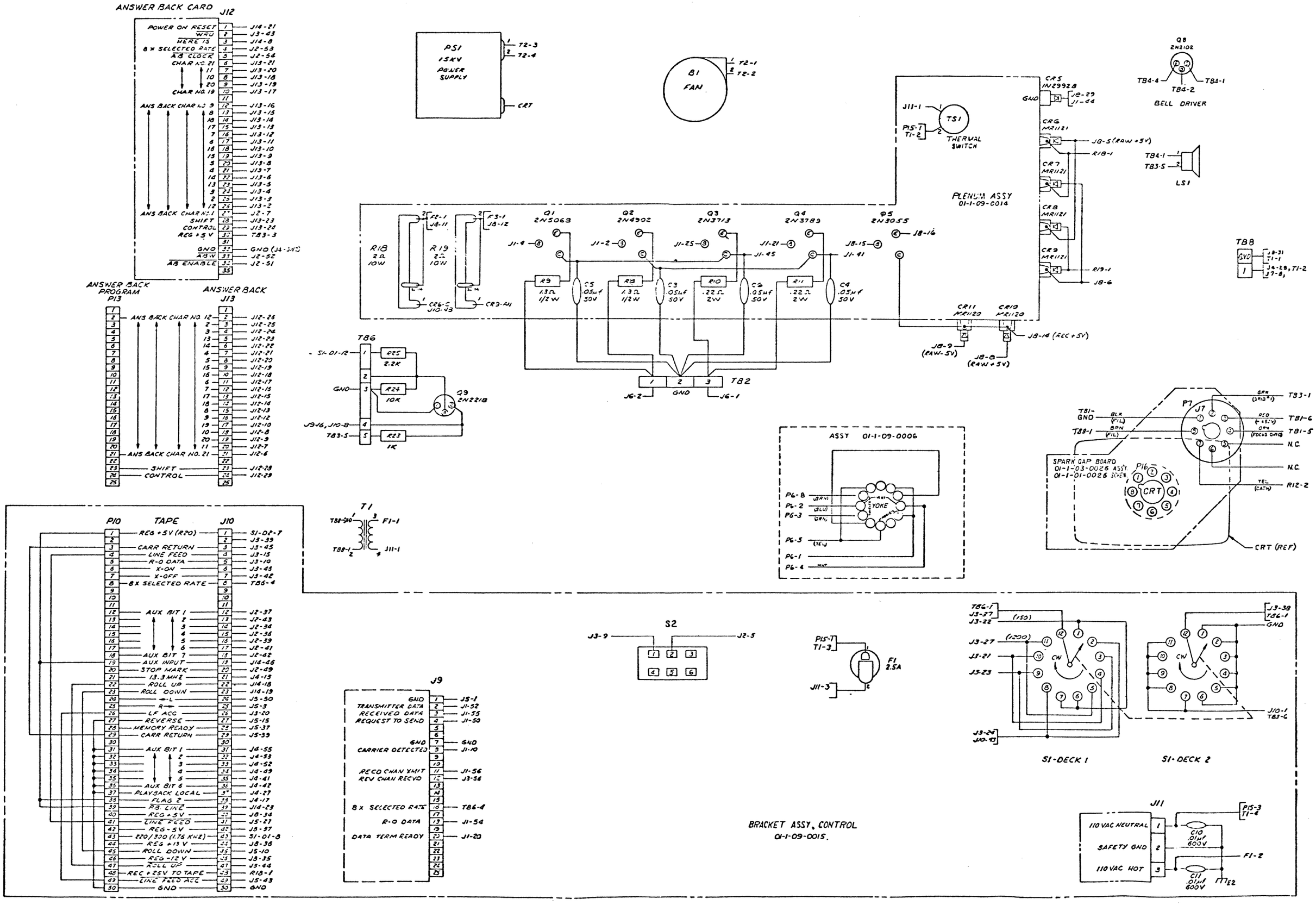


Figure 2-1 Datapoint 3300 (2 of 2)

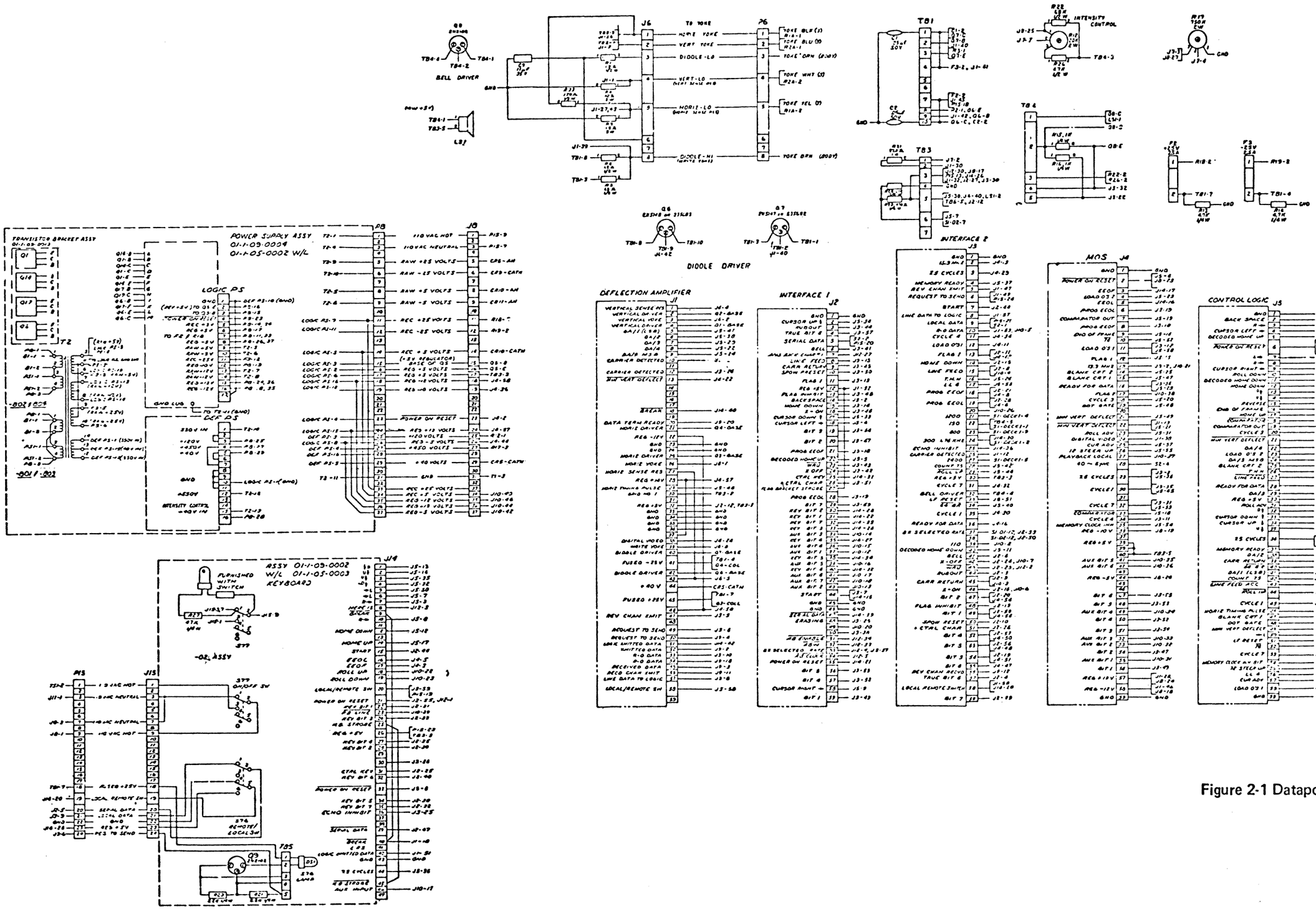


Figure 2-1 Datapoint 3300 (2 of 2)

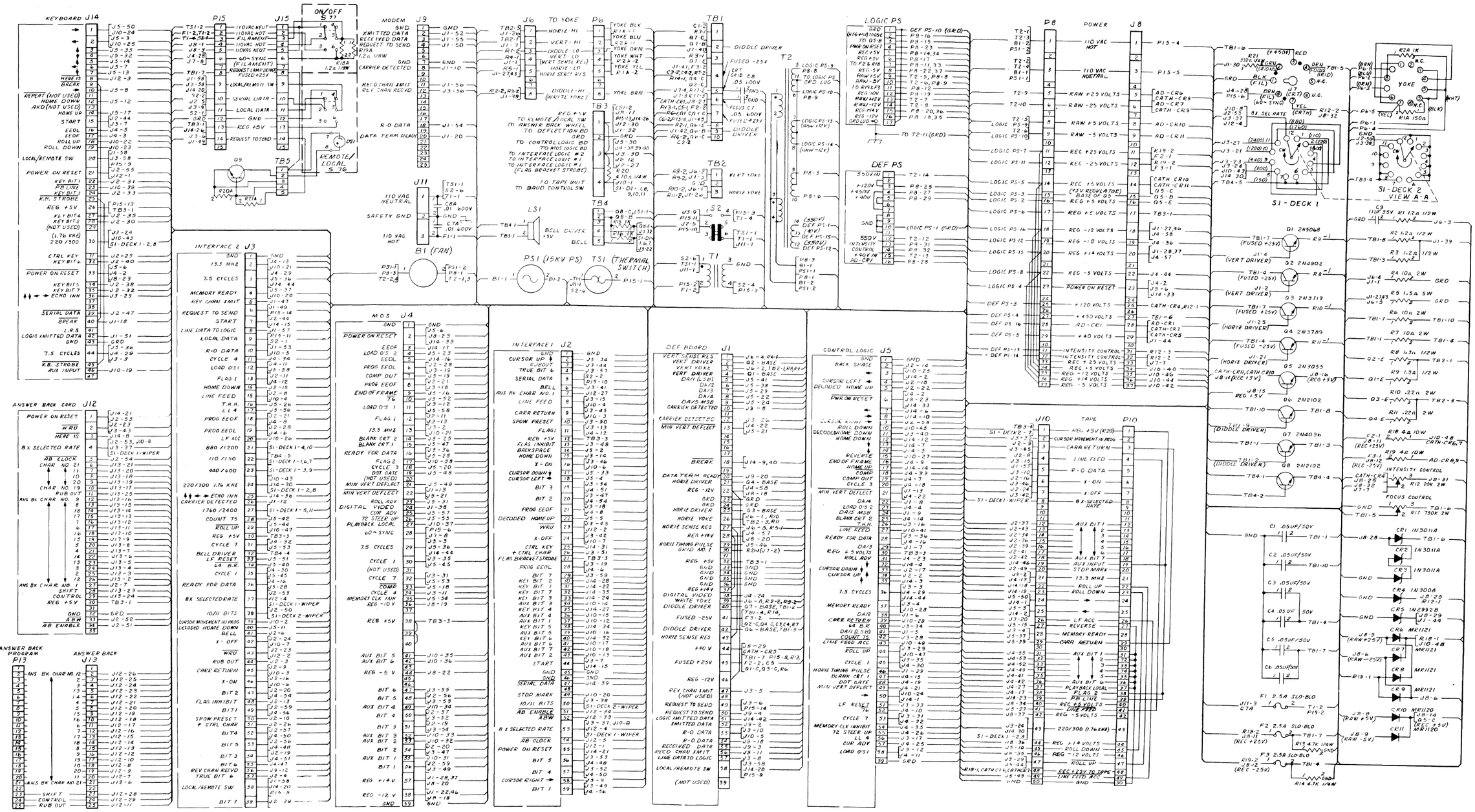


Figure 2-1. Datapoint 3300 (2 of 2)

KEYBOARD

The keyboard consists of 75 hermetically sealed magnetic reed switches that initiate the generation of numbers, letters or control function signals. The magnetic reed switches, the diode matrix and the other associated circuitry are mounted on the Keyboard printed circuit card.

The unique roll-over feature, which allows characters to be printed on the downward movement of the key is accomplished by capacitively coupling the switch closure into the diode matrix. A typical switch circuit is shown in figure 2-2.

When the key is depressed, the voltage on the capacitor at the key side is changed from 5V to 0V; therefore, there is a 5V change on the matrix side of the capacitor. The two diodes in series ensure that the 5V change will drive the resulting pulse below ground. This will compensate for the diode drop in the matrix.

Refer to the Keyboard Block Diagram figure 2-3 to follow the keyboard theory of operation. Figure 2-4, Keyboard Schematic Diagram, is provided for details of the keyboard circuit.

There are seven data bit lines coming out of matrix. The pulses on the bit lines are negative going pulses when the line is active or when the bit is a "one". The pulse duration is approximately 400 micro-seconds. These bit lines are applied to a latching register. The purpose of this register is to eliminate the effects of switch contact bounce. At the same time that the bounce register is latching, Z13 is starting the timing generator, Z16.

The timing generator is driven by the 1.76 KHz clock and produces two sequential pulses that are spaced approximately 570 micro-seconds apart. The first pulse, created by Z7 and inverted and driven by Z14, loads the contents of the bounce register into the holding register. The hold register is loaded on the rising leading edge of the first pulse. The second pulse occurs approximately 570 micro-seconds later and is gated through Z15, Z17 and Z14 to become the output strobe pulse. This pulse goes to the interface circuitry indicating that new data is available in the hold register. The OR gate, Z17 is used to combine possible strobes from the keyboard, tape cassette unit or the repeat generator, Z12. The repeat generator (Z12) generates continuous strobes at 7.5 PPS whenever it is enabled by Z6 which is the NAND of the Repeat key and the AKD signal from Z7.

The second pulse occurs a minimum of 570 micro-seconds after the first pulse (long after the switch bounce has decayed) and resets the bounce register. This is accomplished by Z15. The timing generator is now in its static condition awaiting the depression of another key to restart the operation.

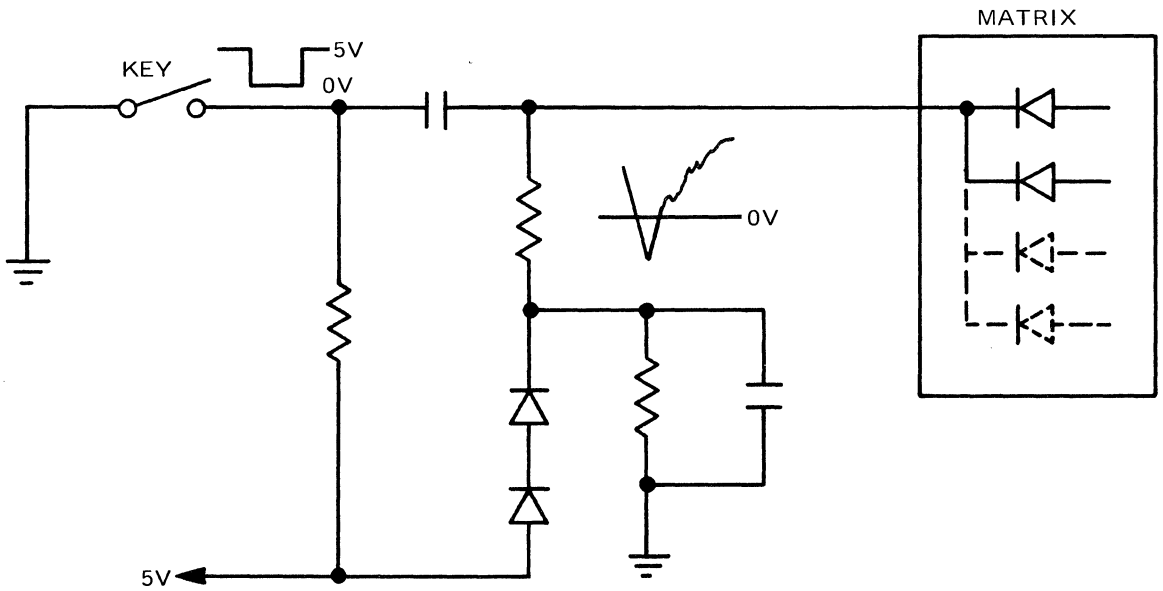


Figure 2-2. Typical Switch Circuit

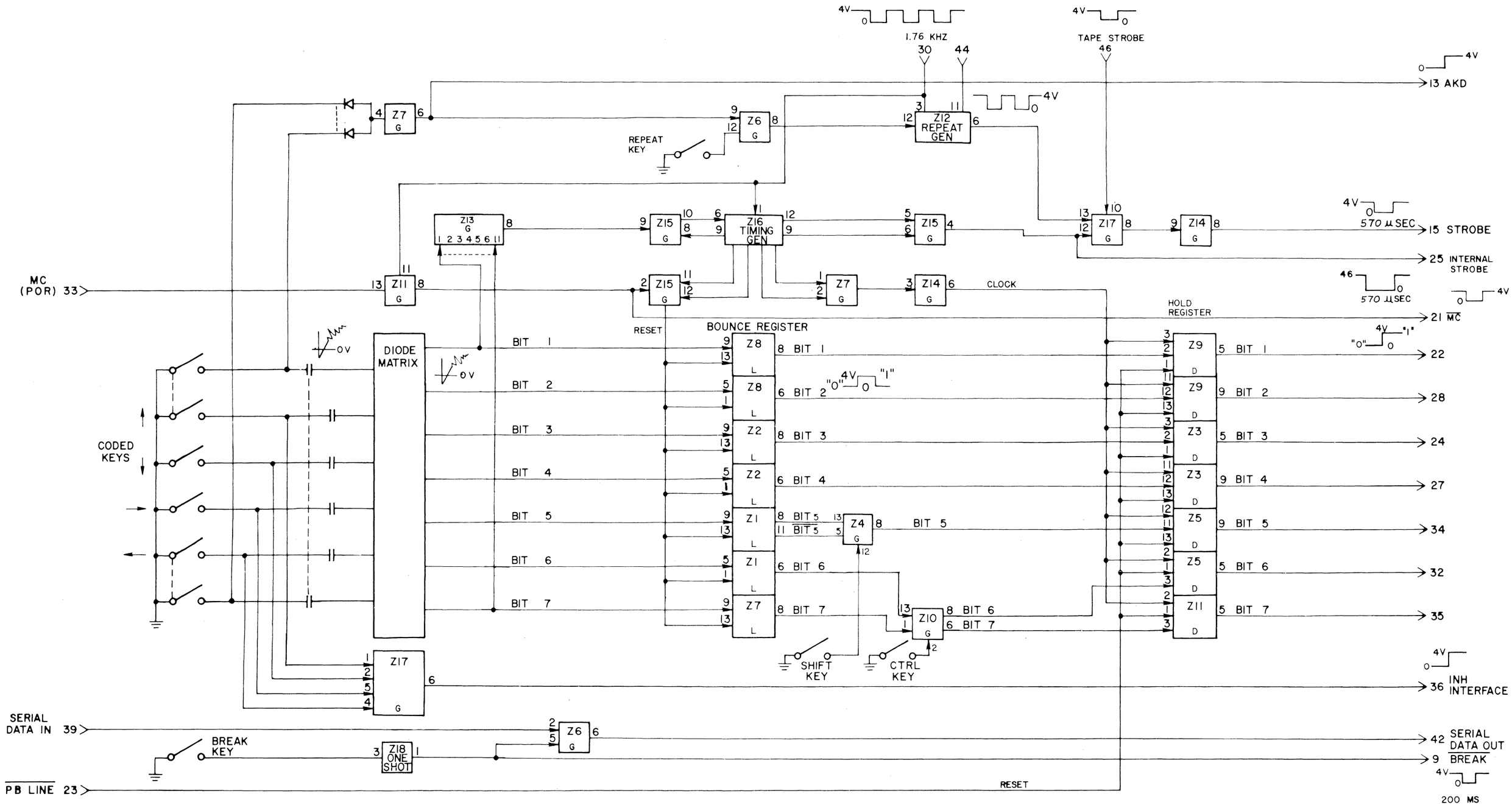
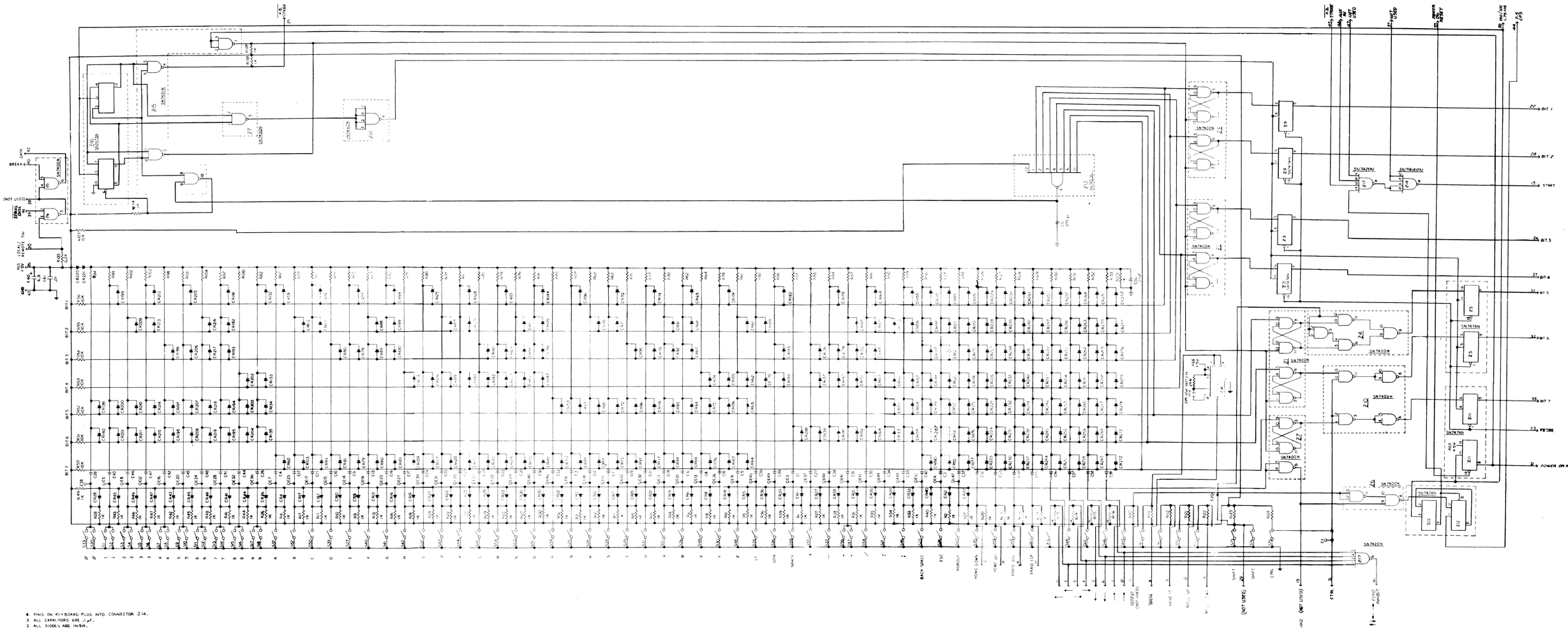


Figure 2-3. Block Diagram, Keyboard



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE 4.7 K, 1/4 W, 5%.
2. ALL DIODES ARE 1N914.
3. ALL CAPACITORS ARE .1 μF.
4. PINS ON KEYBOARD PLUG INTO CONNECTOR J14.

Figure 2-4. Schematic Diagram, Keyboard

When the contents of the bounce register is transferred to the hold register, bits 1 through 4 are transferred direct. Bits 5, 6 and 7 pass through gate arrays for possible modification. If the shift key is depressed, bit 5 is complemented by Z4 before it is stored in the hold register, thus creating the shifted character code. If the CTRL key is depressed, Z10 causes bits 6 and 7 to be stored into the hold register as "zeros", thus creating the control code.

The four cursor directional arrow keys are ORed through Z17 and driven to the interface circuitry on pin 36 to provide echo inhibit when these keys are depressed. When the coded cursor option is incorporated, this signal ensures that the cursor will not move more than one position due to echo-back of the same character from the computer.

The one-shot, Z18, is used to create a timed break pulse of approximately 200 milli-seconds. This pack is not present on all keyboards. When this pack is not present, the break signal remains as long as the key is held down. The break signal is ORed with serial data from the interface card by Z6 and is driven out on pin 42 to the interface buffer located on the deflection card.

ANSWER-BACK

Answer-Back is a 21 character message option used for automatic terminal identification. The Answer-Back is similar to the mechanical answer-back wheel available on some teleprinter devices.

Twenty of the characters are programmable to establish the code for each specific terminal. The functional block diagram explained here is shown in figure 2-5. Figure 2-6 Answer-Back Schematic shows the details of this function.

The Answer-Back is started by the depressing of the HERE IS key causing a low at pin 3 or the receipt of a WRU (Control E) causing a pulse at pin 2. Either of these will cause Z6 pin 3 to go low, which clocks the first JK flip-flop of the start control. The start control issues the "start initialize pulse" from Z20 pin 4. This pulse ensures that the circuit is ready to begin in the correct sequence and issues character number one by setting the D flip-flop Z7. The first character of the Answer-Back is always a suppress character.

The output of the JK flip-flop Z4 pin 13 is gated with the AB ENABLE clock from the Interface 1 card by Z1. The output of Z1 pin 3 is inverted by Z2 to enable the first ten (actually characters 2 thru 11) character gates. The shift register is clocked, from the Interface 1 card, once each character time by AB CLOCK. The phasing of AB ENABLE and AB CLOCK is such that after each shift time, the JK flip-flop Z4 is clocked. When the shift register reaches the last stage, Z12 pin 9 enables Z4 and the flip-flop changes state. The output of Z4 at pin 12 is gated with the AB ENABLE by Z1 and inverted by Z2 to enable the second set of characters (characters 12 through 21). When the shift register reaches the end and Z12 pin 9 allows Z4 to change states, pin 13 will enable Z13 pin 13 so that on the next AB CLOCK, Z13 pin 12 goes low and is ORed with the master clear (MC), which is the same as power on reset (POR). The output of Z6 pin 6 goes low and resets the start control at Z3 pin 2.

Programming the Answer - Back

Programming the Answer-Back is a two part operation:

1. Programming the Answer-Back card.

2. Programming the cable from the Answer-Back card to the Keyboard.

Figure 3-8 is an example of the Answer-Back Coding Table used to determine where the jumpers should be installed for a particular Answer-Back program. Referring to figure 3-8, assume the Answer-Back to be programmed will read: return, Computer * Terminal, return, control J. Enter this in the fifth blank line down, marked customer fill-in.

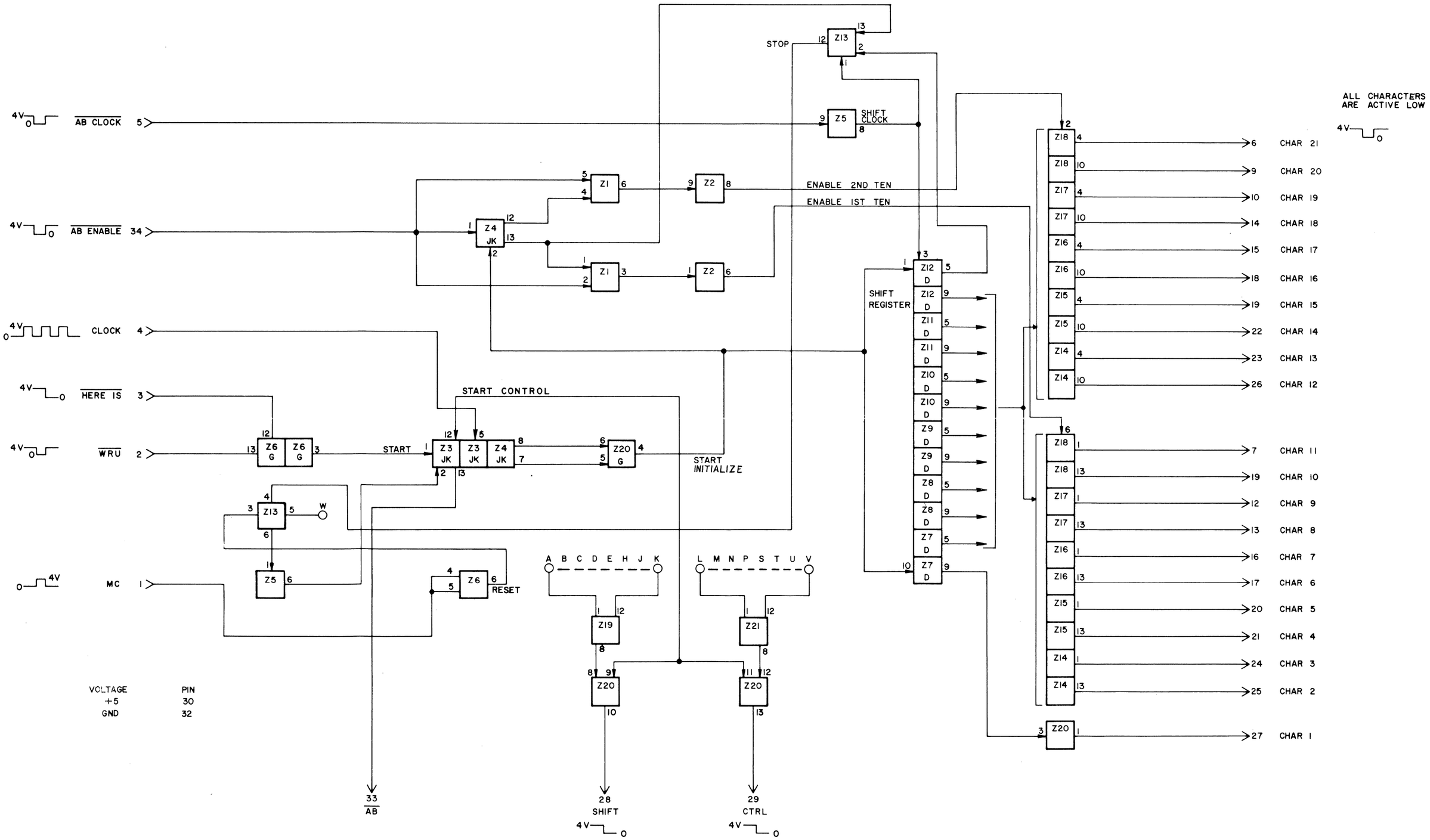


Figure 2-5. Block Diagram, Answer-Back

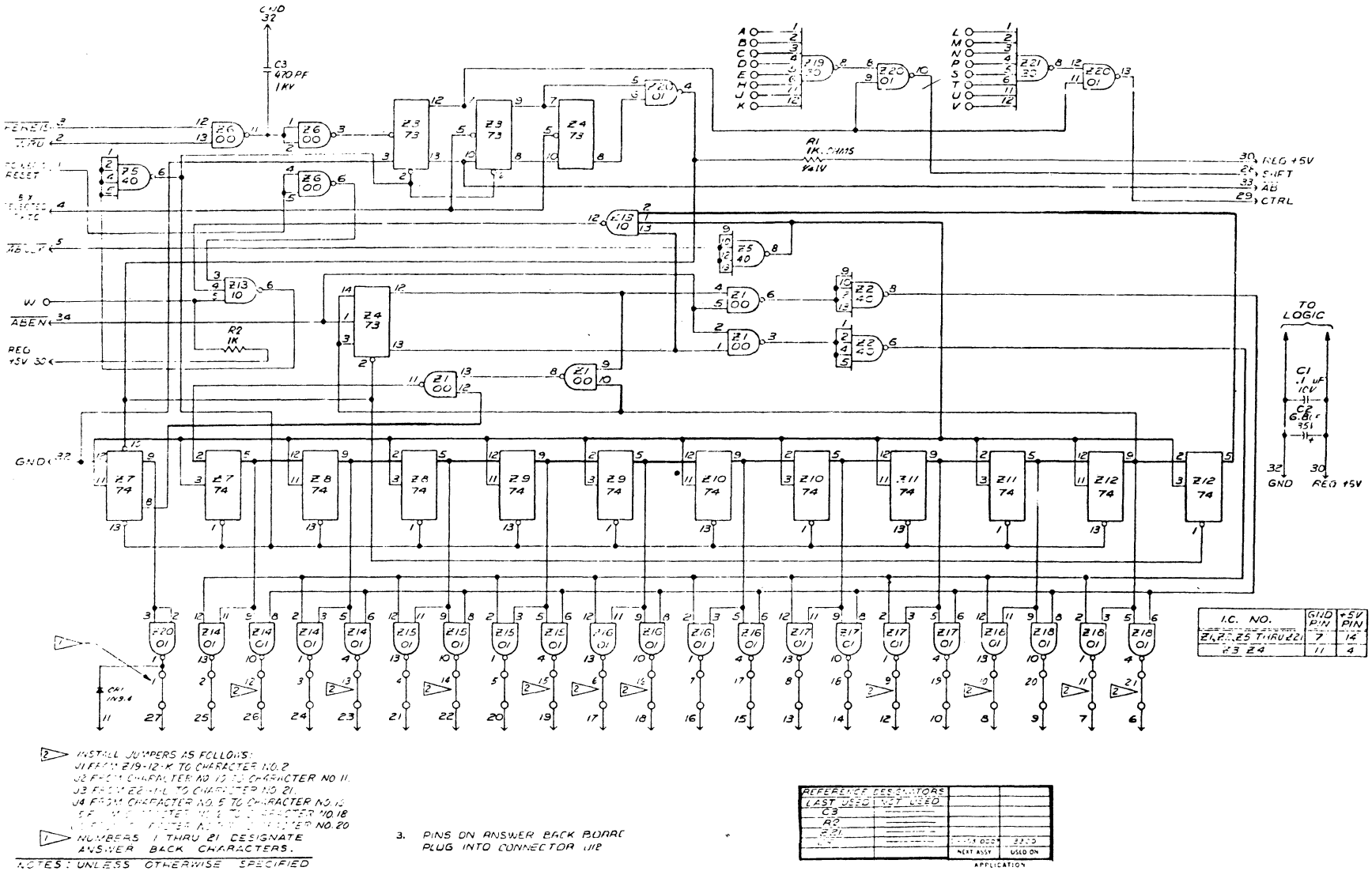


Figure 2-6. Schematic Diagram, Answer-Back

Physically examine the Answerback card and determine the numbering sequence etched on the card near the connector. The numbering sequence will determine whether the card is the "OLD" type, as follows:

TYPE CARD	NUMBERING SEQUENCE
OLD	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21
NEW	1, 12, 2, 3, 13, 14, 4, 5, 15, 16, 6, 7, 17, 18, 8, 9, 19, 10, 20, 11, 21

The coding above the "customer fill-in" line pertains to the coding that must be done on the Answer-Back card and everything below this line applies to the cable hook-up between the Answer-Back card and the Keyboard.

The first line moving up the form is for repeated characters. In the example, the first repeated character is "return". In the E row at the bottom of the form place a dash, and in the repeated character row place the character number of the first "return" (3) over the second "return", in this case, character number 19. This same procedure is repeated for each repeated character. A character may be repeated any number of times by strapping the proper numbers together. On the card, jumper plug in pads are available on the character number lines.

The next row up is used for shifted characters. In the example, the "*" is a shifted character. In the shifted character row, directly above the "*" place an A, B, C, D, E, H, J or K. These are all inputs to the shift gate Z19 on the card. If another shifted character were present, another one of the letters in the group would be chosen.

The next row up the form is for control characters. The "J" is a control character in the above example. In the CTRL CHAR row directly above the "J" place L, N, M, P, S, T, U or V. These are inputs to the control gate Z21 on the card.

This completes the card coding portion of the form. The following jumpers may now be placed on the Answer Back card.

FROM PAD	TO PAD
2	15
5	16
6	18
9	8
19	3
20	A
21	L

The lower portion of the form may now be completed. In the example the first character that requires an entry on the last row of the form, marked "keyboard E row", is the character "C". The procedure is to look up the character "C" in the table located below the coding form. From this table it can be determined that the character "C" corresponds to E-17 on the keyboard. Write the number 17, directly below the character "C" in the "keyboard E row" of the form. After every character has been assigned an "E" number, the cable portion of the form will be complete.

The pin numbers on the row marked "25 pin connector" are the pin numbers on an amphenol 17-304-01 or equivalent connector. This connector will mate with the male connector on the Answer-Back assembly. From the form it can be seen that the following connections must be made.

FROM CONNECTOR PIN	TO KEYBOARD E NUMBER
25	47
4	17
7	40
11	42
12	30
20	44
2	22
5	14
6	18
9	33
10	34
13	29
14	7
17	39
19	49
21	31
23	2
24	1

In the above example all 20 characters were used: however, it is not necessary to use all character positions. When the full 20 characters are not used the character position following the last character of the Answer-Back must be jumpered to pad W or pin 5 of Z13.

The Interface 1 card contains the transmit circuitry, which is basically a parallel to serial converter and the special character decode matrix. The functional block diagram explained here, is shown in figure 2-7. Figure 2-8 is the schematic of the Interface 1 card.

Data appears from the keyboard or tape cassette at the inputs of Z43 and Z49. After a delay of 570 micro-seconds the start strobe at pin 44 occurs. The start pulse presets the D flip-flop Z48 so that Z48 pin 9 enables the gate Z13 allowing the eight times selected rate signal at pin 53 to pass through and clock the clock generator, which is a divide by eight counter. There are four decodes off of the clock generator T1, T4, T6 and T8. The sequence of events are as follows: At T1, the bit counter is advanced and the parity generator is clocked at Z42 pin 11, if the last bit in the shift register has a one output at Z42 pin 5. T1 is inverted at pin 6 of Z25 and applied to the NAND gate Z25 pin 9. If the above conditions are met the output at Z25 pin 8 goes low. Because the parity generator is a D flip-flop, the actual clocking does not occur until the ascending edge of T1. This sequence repeats once per bit time at T1.

At T4, the data is loaded into the output shift register, if the bit counter is in the first count position. At this time, the NAND gate Z35 will be satisfied and pin 11 will be low. The inverted T4 satisfied the NOR gate Z40 causing a high output at pin 13 which loads the data through Z43 and Z49. Also at T4, the NOR gate Z40 at pin 9 is enabled. If it is bit 8 time (parity bit time), either Z19 pins 8 and 9 or 5 and 6 will be satisfied causing pin 8 of Z40 to be enabled. The 10/11 bit input at connector pin 50 is gated with the outputs of Z30 to determine the parity bit time. If an eleven bit code is being generated, the input at pin 50 will be high. This high causes the second stop bit to be added at Z25 pin 1 when the data is loaded. Also, the bit counter sequence is controlled by this high through gate Z7. The output at Z7 pin 1 causes the counter to count eleven bits and the output at Z7 pin 4 will cause a ten bit count, if the input at pin 50 was low.

Returning to the NOR gate Z40, the output at pin 10 will go high. If the output of Z42 pin 9 (the parity generator) is high, indicating that an odd number of ones have been detected at the output of the shift register, Z35 pin 8 will go low, setting a "one" into the last bit position of the shift register at Z42 pin 4, thus creating the even parity.

At T6, the shift register is advanced. T6 is generated by Z20 pin 6 and inverted by the power inverter Z14. The output of Z14 at pin 8 clocks the D flip-flops in the output shift register on the leading edge of T6. As data is shifted out of Z48 pin 5, it is inverted by Z7 so that the serial data output appears at connector pin 5 and the inverted data at pin 47.

This sequence repeats until the bit counter reaches the last count (either 10 or 11). The output of Z40 pin 1 will be high when the last count is reached. If another strobe from the keyboard or tape cassette has not been received while the previous character was being shifted out, Z8 pin 8 will be high. This allows Z13 pin 8 to go low which puts a low on the D input of Z48. When T8 occurs, Z48 pin 9 goes low and inhibits the 8 times selected rate signal from clocking the clock generator.

In the event that a second strobe did occur while the first character was being processed, the output of Z25 at pin 11 would have clocked Z8 causing pin 8 to go low. When Z8 pin 8 is low, Z48 does not receive a clock, and the input clock is not inhibited and the clock generator goes into another cycle immediately. This condition may occur during a fast two character typing sequence, e.g. T-H.

The seven data bits from the input hold register are hard wired through the decode matrix to the various gates to sense particular control characters. The backspace gate Z30 is a programmable gate. Any backspace code may be selected by jumpering the numbered pads at the input of Z30 to the proper lettered pads at the decode matrix input.

The rubout, SPOW, backspace and all of the control characters are not loaded into the memory therefore, the flag to the MOS memory must be inhibited. The output of Z39 at pin 8 is ORed with the control character outputs on the

Interface 2 board to inhibit the flag during any of the special characters.

The automatic Space Overwrite (SPOW) is a special feature of the Datapoint 3300 and functions as follows: With each line feed character, the D flip-flops Z50 are reset and the latch Z39 is set. The first flag from the interface appearing at connector pin 11, indicating that a printable character has occurred, will reset the latch Z39 causing Z39 pin 6 to go low. This low is inverted by Z45 and clocks D flip-flop Z50 so that Z50 pin 5 goes high enabling the D flip-flop Z50 at pin 12. When the next carriage return occurs, it will clock Z50 at pin 11 on its ascending edge. This will cause Z50 pin 9 to go high enabling Z29. If the next character is a line feed, the circuit will be reset through Z45; however, if no line feed does occur, the next space character will satisfy Z29. The output of Z29 at pin 8 inhibits the flag to the memory; therefore, no new character is entered. This output is also ORed with the right arrow decode by Z3. The result is that the space character, which is destructive, is converted to the right arrow character which also advances the cursor, but does not destroy the memory contents.

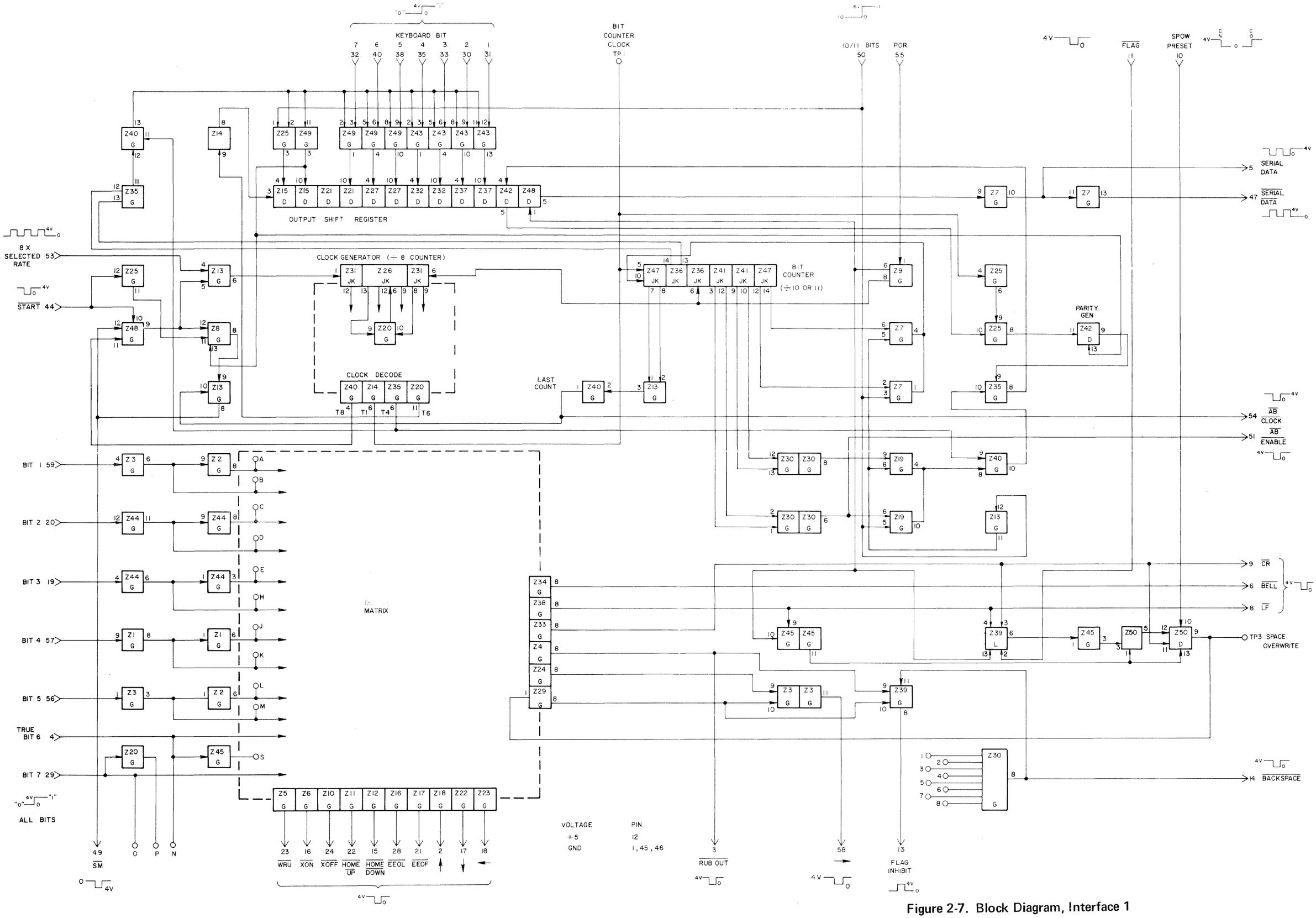


Figure 2-7. Block Diagram, Interface 1

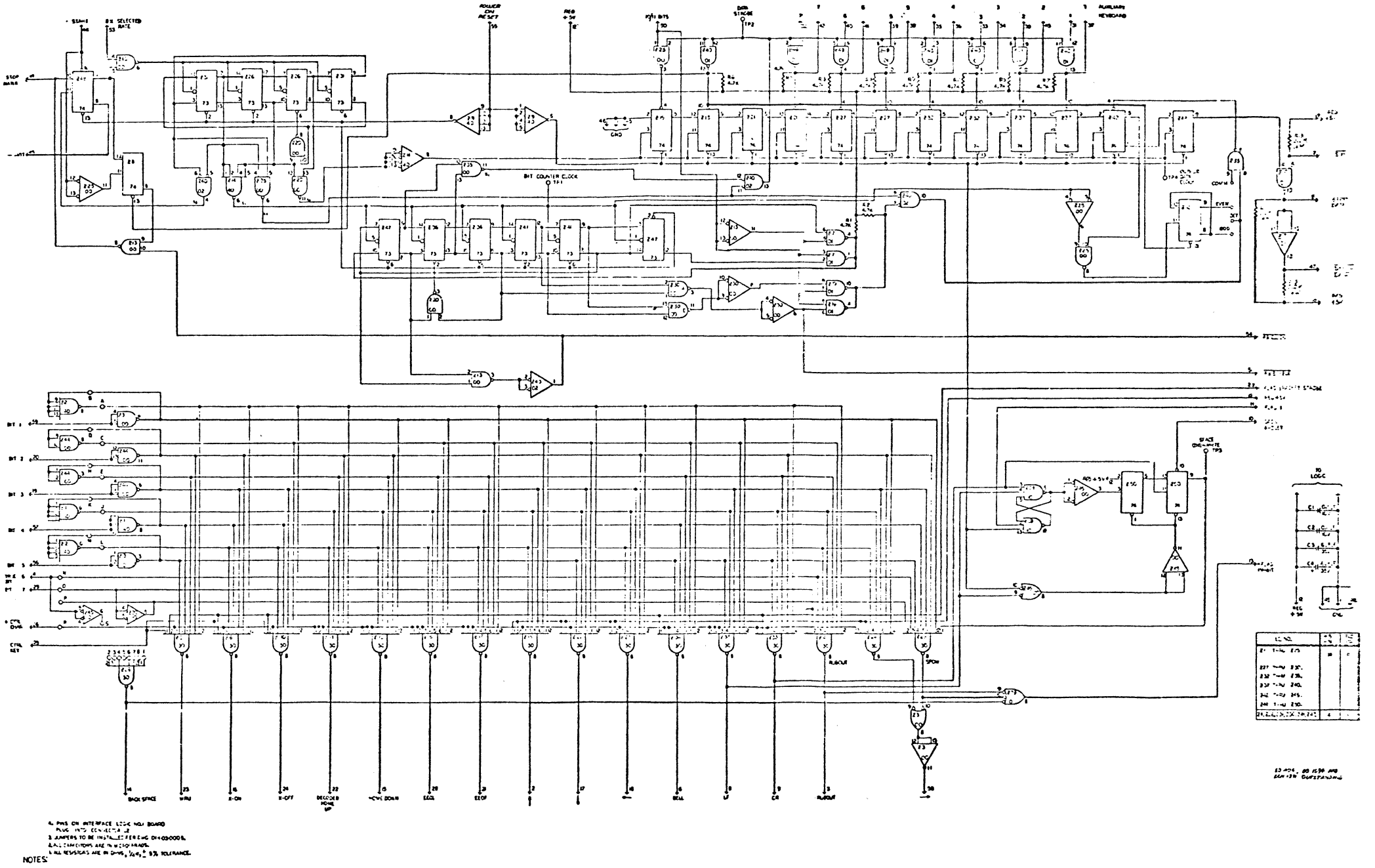


Figure 2-8. Schematic Diagram, Interface 1

INTERFACE 2

The Interface 2 card consists primarily of the data receiver for the Datapoint 3300. Serial data being received is presented to the display memory and the function matrix as parallel characters. Other functions located on the Interface 2 card are the two bit-rate oscillators/dividers, the request to send latch with high speed data turnaround circuit,Space Overwrite preset, bell driver and a control-character reset circuit. Also, included on some Interface 2 cards is the optional speed buffer and its associated control circuits.

Figure 2-9 is a functional block diagram of the Interface 2 card without Speed Buffer. A block diagram of the Speed Buffer is shown in figure 2-10. Figure 2-11 shows the Interface 2 card with Speed Buffer and all associated circuitry. Figure 2-12 shows the Interface 2 card without the Speed Buffer.

Input data is routed through Z29 to the input shift register, Z61-Z65. The start space sets the start latch, Z28, which removes the reset from the input register and gates the 8x Bit Rate Clock to the input bit chopper, Z68 and Z69. The input bit chopper, a radix-eight Johnson counter, reduces the input clock to bit rate. The fourth count is decoded by Z46 and is used to clock the input register on its rising edge. The rising edge occurs half-way through each bit time, thus sampling the incoming data in the middle of each bit.

The presence of the start space at Z65 pin 5 (after 10 shift clocks) enables succeeding timing pulses to be gated through Z57 pins 4, 10 and 13. The output of Z57 pin 4 occurs at "time 5" of the radix-eight bit chopper and is gated through Z56 pin 8 and Z15 pin 8 to clock the data now present in the input register into the input hold register, Z11 pin 14. The output of Z57 pin 10 (time 6) will be gated through Z18 pin 8 as $\overline{\text{FLAG}}$ unless the character that has been transferred is a control character. The output of Z1 pin 8 detects control characters and inhibits the $\overline{\text{FLAG}}$ through Z26 pin 6 and Z36 pin 8. The outputs of Z57 pin 13 and Z57 pin 1 (time 7) provide resets to both the control character reset latch, Z28 pin 11, and the start latch, Z28 pin 3.

Word sync is maintained by gating the reset timing pulse, Z57 pin 1, with the start space, Z56 pin 6, and the first stop mark, Z61 pin 9. These three inputs are gated through Z67 pins 9, 10 and 11. The rising edge of Z67 pin 8 will clock the start latch, Z28 to the reset condition.

If the character present in the input hold register is decoded as any of the functions brought back to Z5 pins 3, 4, 5, 6, 11 or 12, the control character reset latch, Z28 pins 8 and 9, immediately resets the input hold register. The resulting decoded outputs, excepting HOME DOWN, are only present for approximately 125 nanoseconds. A decoded HOME DOWN sets latch Z17, Z27 and allows divider Z38 to count out a "time window" ($\geqslant$ 600 micro-seconds) to allow the control logic timer enough time to execute HOME DOWN. HOME DOWN is not executed in speed ranges over 440 bits/seconds due to the time required.

The two bit-rate oscillators are two-transistor, crystal controlled circuits with a discrete buffer on each. The 225.28 KHz oscillator provides the basic frequency for all 11-bit code data rates, e.g. 110, 220, 440, 880 and 1760, while the 307.20 KHz oscillator provides all 10-bit code data rates, e.g.150,300, 600, 1200 and 2400. The output of each oscillator is gated into Z66. A single 10/11 control line is brought into Z66 to allow one of the oscillators to be gated into Z16 and Z7, the dividers. Outputs from the dividers (actual frequency is eight times the data rate) are routed to the rotary switch for baud rate selection.

TheSpace Overwrite consists of Z3, Z4 and one Z14 flip-flop. The output of Z3 presets Z14 pin 5 to "zero" upon decoding a "control N". A "zero" on Z14 pin 5 is sent to the Interface 1 card to lock its circuit intoSpace Overwrite. The output of Z4, upon receipt of a "control 0", presets Z14 pin 5 to a "one" thereby releasing the Space Overwrite circuit.

The bell-driver consists of Z20, two Z19 gates and a discrete output driver. When either a decoded BELL or count 64 is received, Z19 and Z20 supply an output to the discrete driver, the width of a 7.5 Hz clock pulse, thereby gating the tone generator for a period great enough to be audible.

The request-to-send latch is Z9. In the REMOTE mode, depressing any key provides a START pulse which sets the latch and raises the request-to-send line. When operating with any data set other than a 202, the request-to-send latch will remain engaged until the LOCAL/REMOTE switch is moved to the LOCAL position. When operating high-speed with 202 data sets, the remote computer may control the status of the request-to-send latch through the "carrier detected" and "reverse channel received" inputs.

If the remote terminal or remote computer lowers its reverse channel, the change is gated through the Schmitt Trigger, Z1 pin 3, Z19 pin 3 and appears as a clipped, differentiated pulse at Z1 pin 6. This pulse is gated through Z2 pin 4 to reset the request-to-send latch, thereby lowering the request-to-send line to the data set. If the remote terminal or remote computer has completed its transmission, it may raise the request-to-send line by lowering its carrier or main channel. The change is gated through Z6 pin 11 thereby clocking the request-to-send latch back to the "send" mode.

Speed Buffer

The purpose of the Speed Buffer is to temporarily store incoming high-speed (>600 bits/second) characters, until synchronization with the display is achieved. Characters may then be written in rapid succession at the display memory stepping rate of 130 KHz.

The Speed Buffer consists of a clock divider, load control circuits, the high-speed circulating registers (memory), a temporary holding register and the unload control circuits.

This explanation will refer to the block diagram figure 2-10 and details of the Interface 2 card with the Speed Buffer are shown in the schematic figure 2-11.

The clock divider is a radix-six Johnson counter, Z70 and Z60, that divides the 13.3 MHz master clock to 2.22 MHz. The high speed circulating registers, Z31 - Z35, Z41, Z43 and Z45 are clocked from Z50 pin 11 which decodes count 1. Shift occurs on the rising edge of count 1.

Referring to the input shift register and input bit chopper clock, the presence of the start space at Z65 pin 5 arms Z48 pin 12. One output of the "TAG" high-speed register Z35 pin 14, is tied to Z48 pin 11 so that if data is presentin the registers, the new character will be loaded only when the falling edge of the TAG occurs. If a TAG is present, Z48 pin 8 will be clocked "low" thereby starting the load sequence. If no TAG is detected by time 5 of the input bit chopper, the output of Z56 pin 6 initiates the load sequence through Z58 pin 11.

Either of these load commands clocks Z59 pin 5 high which will allow the next speed buffer clock time 4 to clock Z59 pin 9 high and also be gated through Z58 pin 3. (This is a latching circuit to permit only one, time 4 pulse to be gated through.) This time 4 pulse is decoded at Z50 pin 6 and inverted through Z58 pin 8. This gated time 4 pulse clocks Z48 pin 6 low. Z49 pins 4 and 10 invert this output to enable all "load" gates contained in Z52 - Z55 that are tied to this line. The "recirculate" gates, also contained in Z52 - Z55, are tied to Z49 pin 1 and 13 are now inhibited. Data present in the input shift register will now be entered into the speed buffer on the rising edge of the next speed buffer clock (rising edge of time 1). A TAG bit will also be entered into Z35.

The next speed buffer time 2 pulse that occurs, gated through Z50 pin 3, will apply a reset at Z48 pin 1 and Z59 pin 13 thereby returning the buffer to the "recirculate" mode and restoring the load circuits to their original states. The input register data has now been entered into the Speed Buffer which allows the input register to be reset.

Since the Speed Buffer data must be maintained in first-in, first-out order, the unload sequence must begin on the rising edge of the TAG, which represents the first character entered Z24 pin 5 to clocked high on the rising edge of TAG applied to Z24 pin 3. Z24 pin 5 enables Z40 pin 6 to allow the next time 4 Speed Buffer clock to clock the data into the temporary holding register Z21 - Z24, through Z25 pin 6. At the same time, Z30 pin 5 was preset to the "one" state,

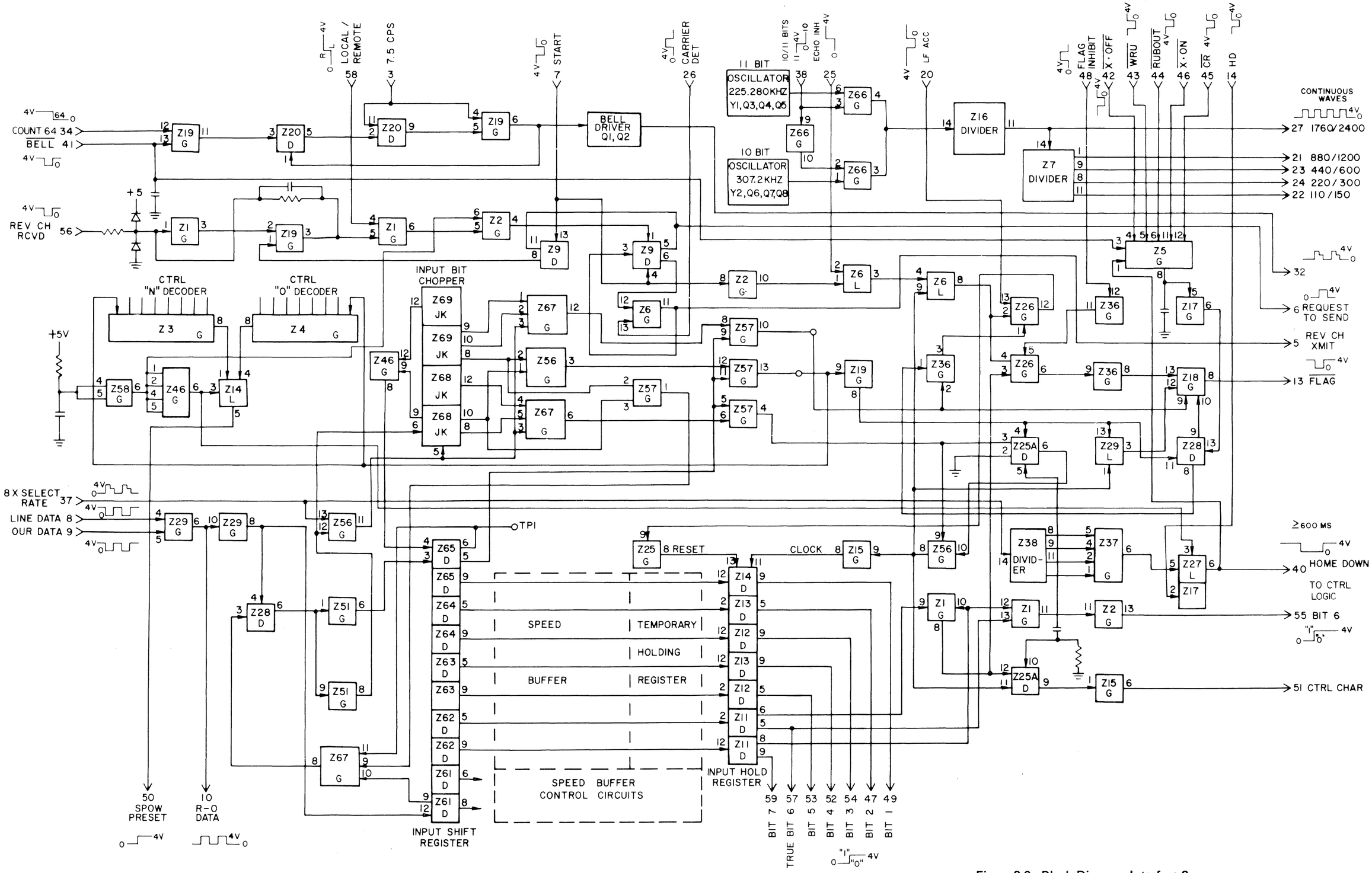


Figure 2-9. Block Diagram, Interface 2

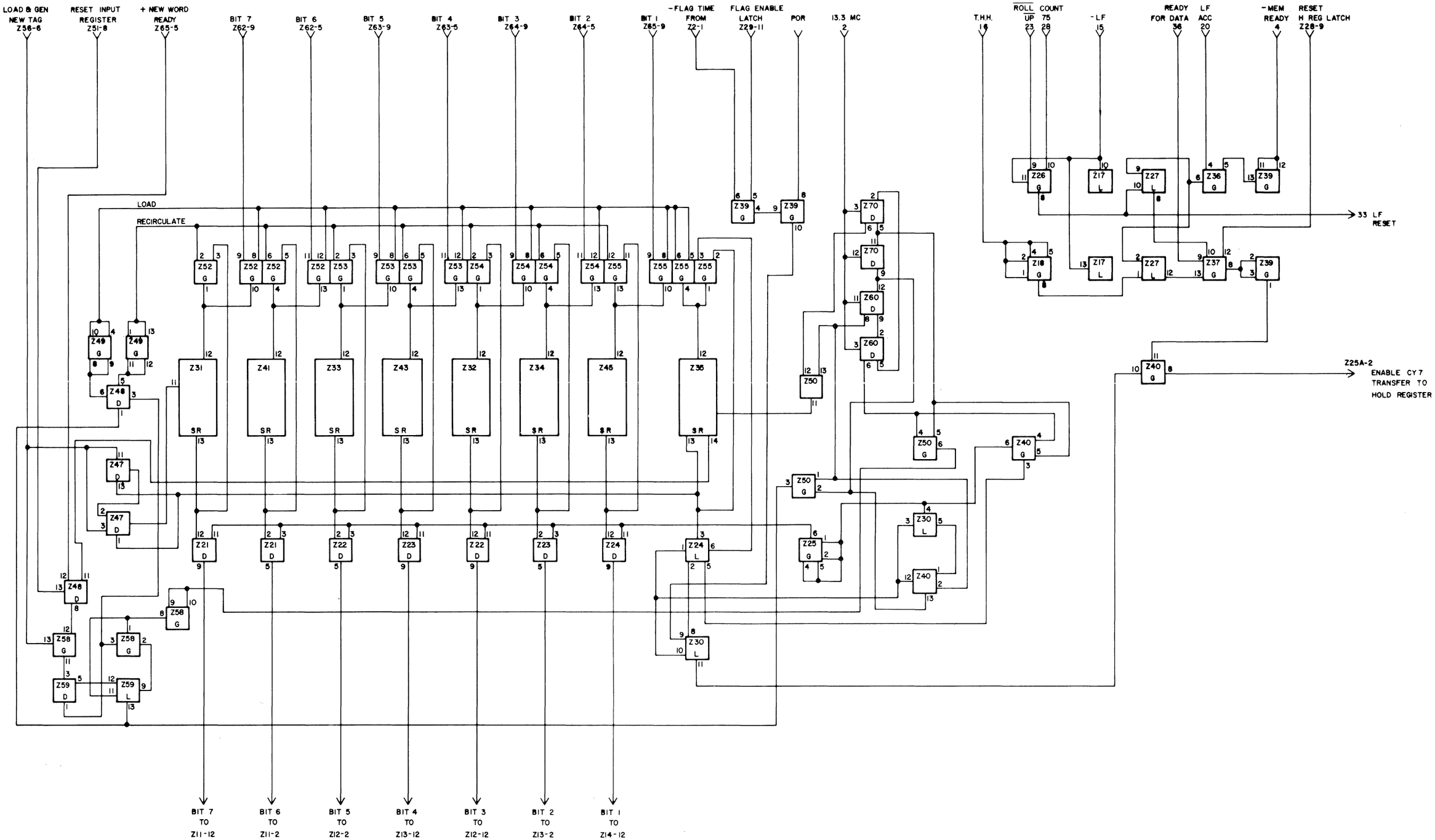


Figure 2-10. Block Diagram, Speed Buffer

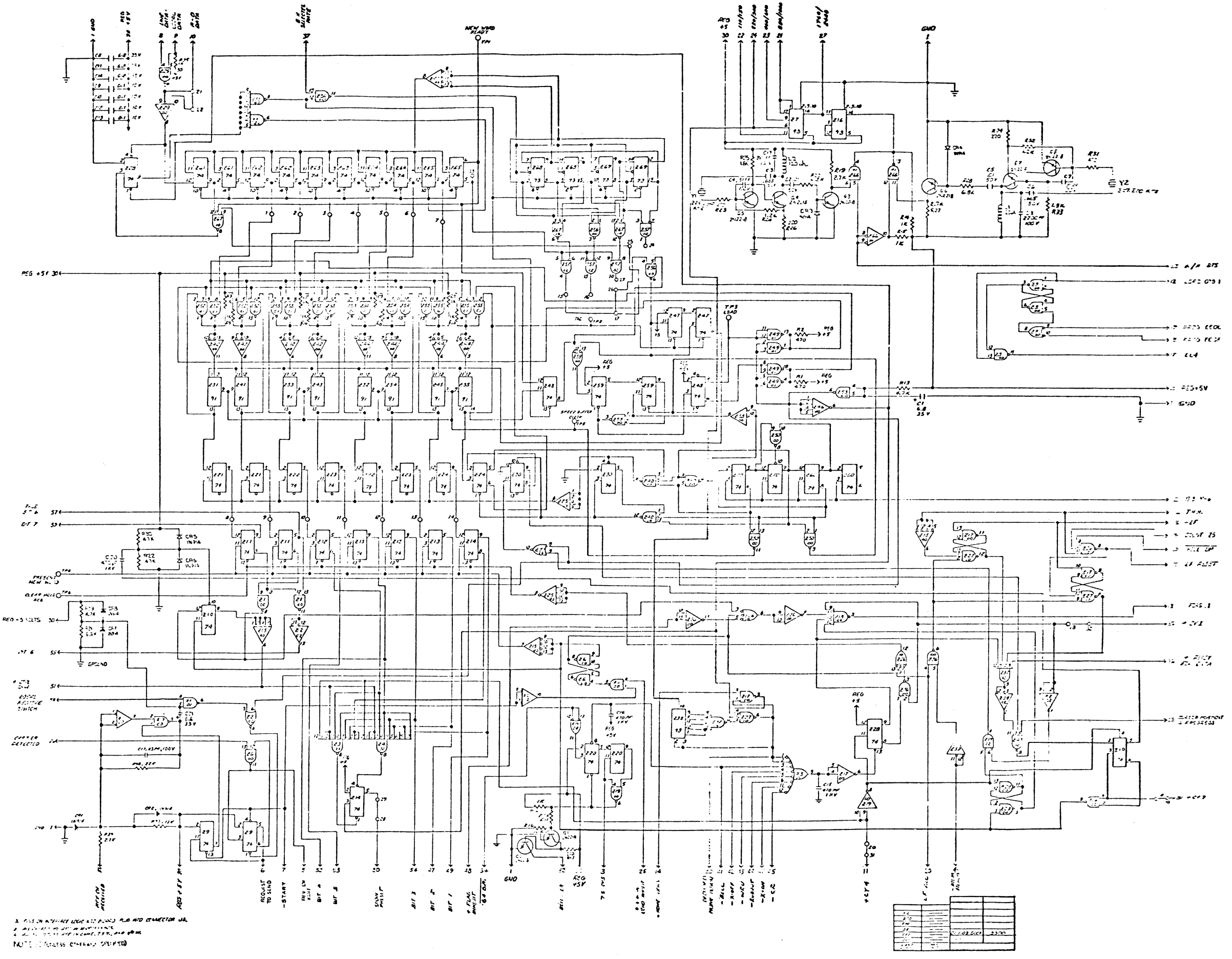


Figure 2-11. Schematic Diagram, Interface 2

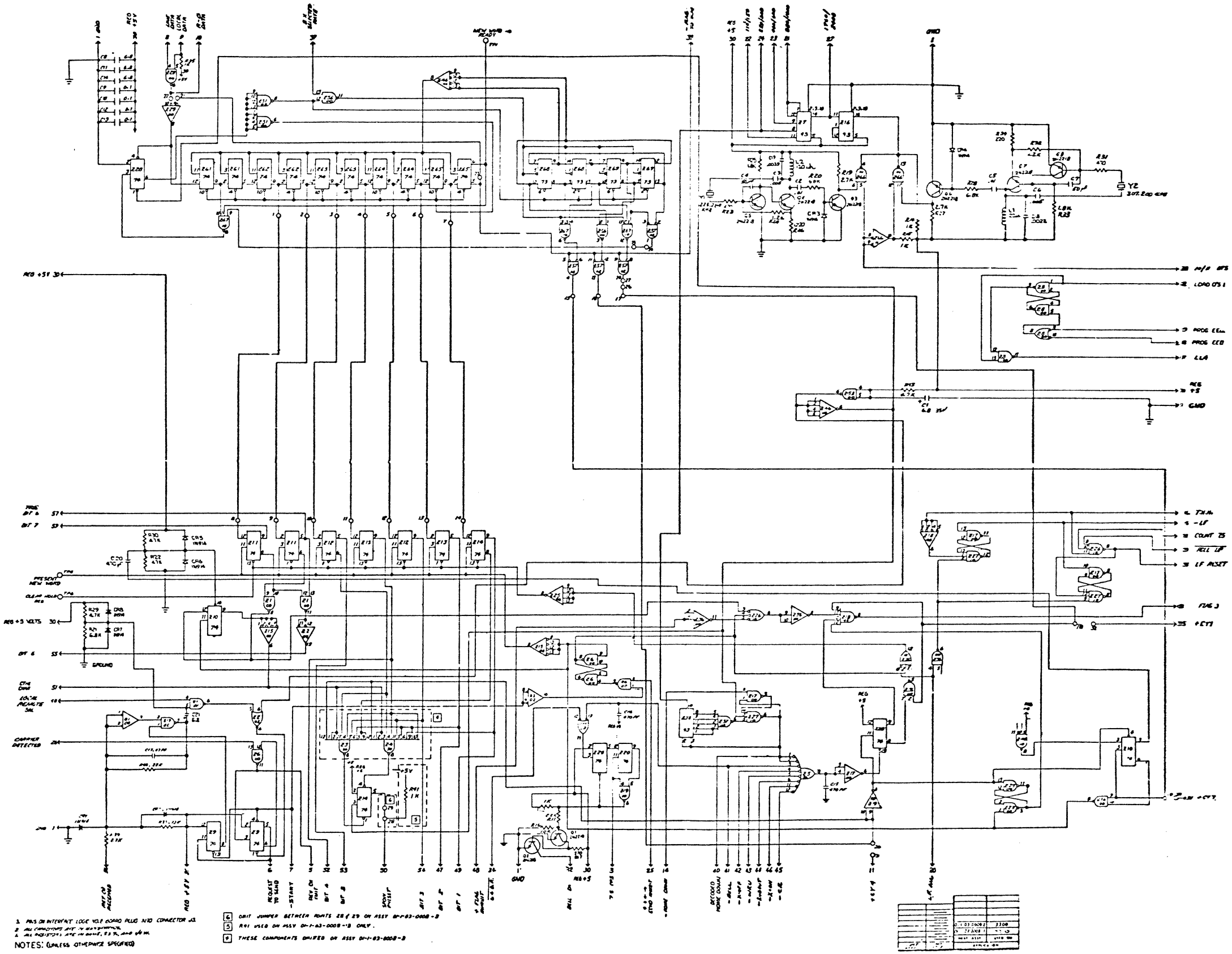


Figure 2-12. Schematic Diagram, Interface without Speed Buffer

thus allowing Z40 pin 12 to reset and clock respectively, Z24 pin 5 and Z30 pin 5 to their original states. During this period, Z24 pin 6 has been routed back to Z55 pin 3 which enters a "zero" in the TAG, representing this character, that has been removed from the Speed Buffer. Before this character can be transferred to the "input hold register", six conditions must be met. They are:

1. A ROLL UP must not be in progress, denoted by Z27 pin 12 being high. (Latch formed by Z17 pin 11, Z27 pin 12, reset by Z18 pin 6.)

2. A LINE FEED must not be in progress, denoted by Z27 pin 8 being high. (Latch formed by Z17 pin 8, Z27 pin 8, reset by Z26 pin 8.)

3. No holding register reset must be present, denoted by Z27 pin 8 being high.

4. Data must be present in the temporary holding register, Z30 pin 9 high.

5. The ready-for-data line, pin 36, must be high.

6. The memory ready line, pin 4, must be low and the LF accepted line, pin 20, must have returned high.

When all of these conditions have been met, Z40 pin 8 will go low thus enabling the next cycle 7 clock to change Z25 pin 6 high and gate through one cycle 7 pulse. The cycle 7 pulse is gated through Z15 pin 8, which clocks the data in the temporary holding register into the input hold register.

If the character transferred is a printable character, cycle 1 will be gated through Z18 pin 8 and sent to the display memory as a FLAG. If it is a control character, Z1 pin 8 will inhibit the flag and the matrix on Interface 1 will decode the character. After execution of the control character, it will either be reset by the control character latch or be reset from the Control Logic via the LF accepted line, pin 20.

At the time the transfer occurred, (Cycle 7 through Z56 pin 8), latch Z29 pin 3 and Z29 pin 11 enabled Z18 pin 12 to pass the next cycle 1 (FLAG). After this latch set, cycle 1 was also gated through Z39 pin 4 and Z39 pin 10 to clock Z30 pin 8 back to the "ONE" state, thus denoting the character had been taken from the temporary holding register. This initiates an immediate search for the next character in the Speed Buffer.

The completion of the unload cycle occurs on the following cycle 4. The cycle 4 input at pin 11, gated through Z19 pin 8, resets the Z29 pin 11, Z29 pin 3 latch and resets Z25 pin 6 to its original state.

Now that snychronization with the display memory has been achieved, the Ready-for-Data line will return high on the following cycle 6. Since the temporary holding register will have another character by this time, the unload cycle will repeat on the following cycle 7 until the Speed Buffer is empty.

MOS

The MOS card contains the Circulating Memory, the Read Only Memory (ROM) and the Master Oscillator Circuitry. This explanation makes reference to the Block Diagram in figure 2-13. Figure 2-14 is the MOS Schematic Diagram providing additional details of the circuits.

The Master Oscillator is a dual transistor 26.6 MHz crystal controlled circuit. JK flip-flop, Z19, serves as a buffer and a divide-by-two counter for the oscillator output. The output of Z19 is present at connector pin 13 and is connected to NAND gate Z22 pin 1. The NAND gate Z22 is not satisfied until pin 11 of the latch Z22 is high. This occurs each time the 60 Hz line tap at connector pin 28 goes positive. Latch Z22 is reset by the End of Frame (EOF) signal from the control logic. The output of Z22 pin 3 is a 13.3 MHz burst starting with each cycle of the line voltage and ending with the display frame. This technique prevents any flicker in the display due to a difference beat between the line frequency and the frame rate.

The synchronized 13.3 MHz drives the dot generator which is a divide-by-seven synchronous counter. Gates Z35 and Z36 decode the seven dot times from the counter.

The dot times are the seven vertical dots of the 5 x 7 dot matrix. Dot number one appears at Z35 pin 11 and the dots are decoded sequentially with dot seven appearing at Z36 pin 3. Adjacent dot times occur 75 nanoseconds apart and the dot width is approximately 37.5 nanoseconds.

Dot seven enables the JK flip-flop Z18 which is being clocked by the 13.3 MHz clock. The output at Z18 pin 6 is the 950 KHz signal used for the minor vertical deflection freuqency. The inverted 950 KHz is present at Z8 pin 6. This signal is used to drive the cycle generator which is another divide-by-seven synchronous counter.

The cycle generator is the heart of the master timing system. Decoded signals from the cycle generator control the ROM read cycles and the phase clock generation for the Circulating Memory and clock pulses for the memory character counter on the control logic card. Gates Z34 and Z33 decode five counts which cause the ROM to access five sequential words. The two counts connected to Z13 pins 8 and 12 are the input gates to the phase clock generator or clock drivers. The transistors Q1 through Q6 convert the logic level cycle clocks into MOS compatible signals.

The Circulating Memory consists of fifty-four 200 bit shift registers. The memory is configured in six tracks of nine packs each, providing the 1800 character length and the six bit width. All tracks operate identically therefore, only bit 1 or track 1 will be discussed.

Data is normally recirculating in the memory at a 135 KHz rate. The collectors of Q3 and Q6 provide the two phase 135 KHz clock pulses. As data passes through the eighteen hundredth position, it is passed from Z61 pin 6 through gate Z29 to the recirculating gate Z1 pin 6. In the recirculating mode, pin 5 of Z1 will be high, thus allowing the data to re-enter the circulating memory through Z1. If new data is to be entered in place of the circulating data, the bit will be present at connector pin 56 and Z1 pin 11. A flag will occur at connector pin 12 causing the output of the D flip-flop, Z9 pin 5, to go high. When the compare point is reached, the pulse occurring at connector pin 7 will cause latch Z17 pin 6 to go low, thus, causing the latch Z17 pin 11 to go low.

The low from Z17 pin 11 is applied to Z7 pin 8 and Z7 pin 11. The resulting high output at Z7 pin 9 enables the "new data gate" Z1 pin 12 and allows the new bit to be entered. The resulting low at Z6 pin 10 disables the recirculating gate Z1 at pin 5. The gate Z5 output at pin 1 serves to enable and disable the auxiliary inputs in the same manner as Z7 pin 9 output does for the receive bits.

The cursor is advanced after the character is loaded into the memory. The latch, Z17, was set during the load time, making Z17 pin 3 high. This high enables Z21 and Z20. The output at Z21 pin 6 occurs at cycle 5 and advances the cursor one character position. The output at Z21 pin 8 is passed through the inverter Z14 and produces the roll advance strobe at connector pin 23. The output of Z20 pin 6 resets the first Z17 latch at cycle 6. The second Z17 latch is reset by cycle 7 from Z50 pin 12. At this time, the input gates return to the recirculating mode.

The memory is cleared by loading zeros into the bit positions. The gates, Z12 pins 4 and 5 and Z16 pins 1, 2 and 13, receive the various functions that require zeros to be loaded. The functions are: ERASE END OF LINE (EEOL), ERASE END OF FRAME (EEOF) and POWER ON RESET (POR). The outputs of Z10 pins 1 and 4 occur at compare time and are connected to the OR gate Z12 pin 1. The other input to Z12 at pin 2 comes from the control logic card and occurs when the frame is being rolled down. The output of Z12 pin 3 is a high which causes Z6 pin 13 to go low, thus inhibiting the recirculating gates and zeros are placed in the memory.

A character is present at the Circulating Memory output for approximately 7.5 micro-seconds, due to the clock rate, before it is shifted around and replaced by the next character. Gates Z30 and Z33 present the six data bits to the ROM during this time and define one of 64 unique blocks of five addresses. The cycle counter pulses the ROM approximately once every micro-second until five words have been read out. The output of the ROM is a seven bit word. The first word corresponds to the first column of seven dots, the second word corresponds to the second column of seven dots, etc.

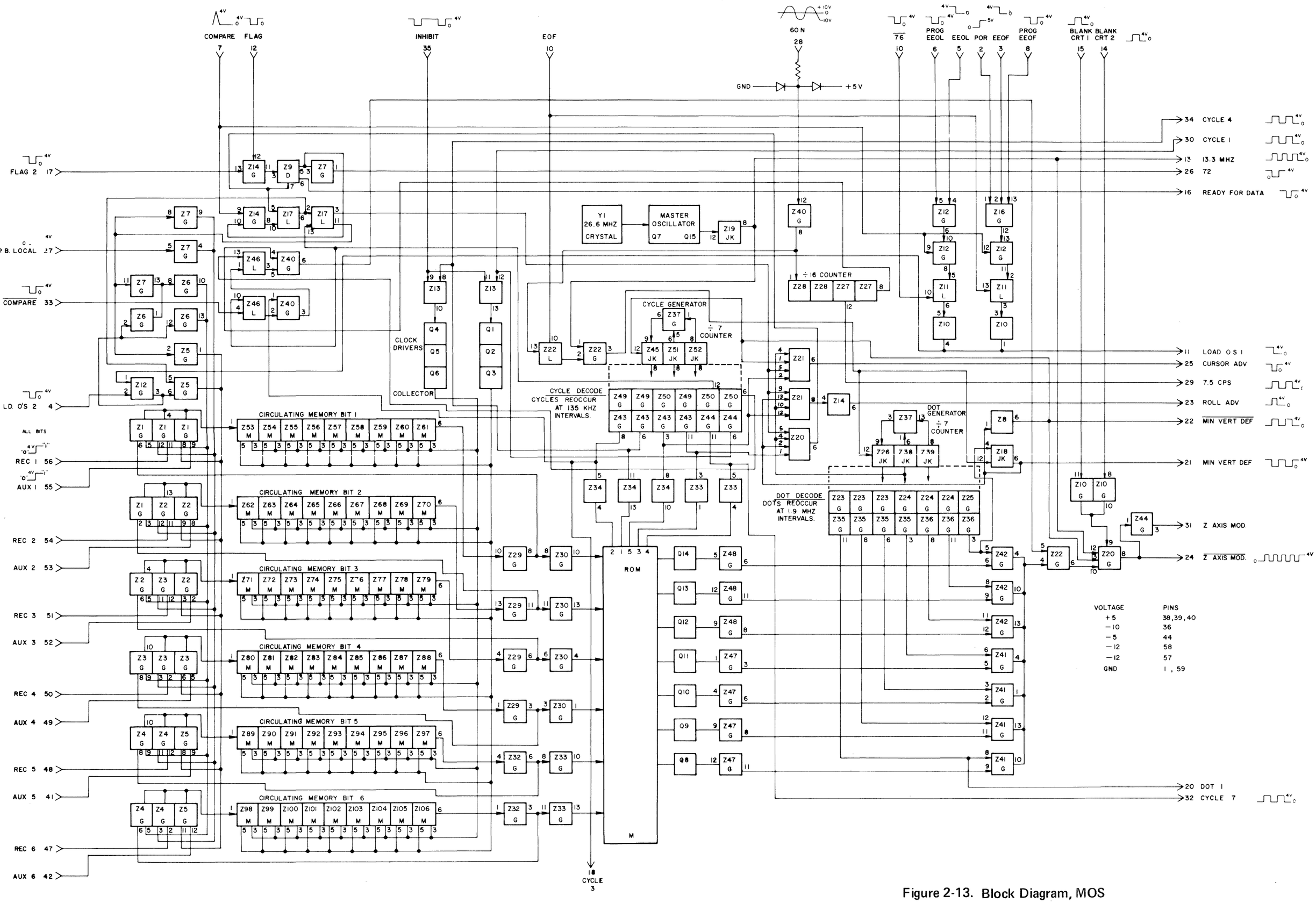


Figure 2-13. Block Diagram, MOS

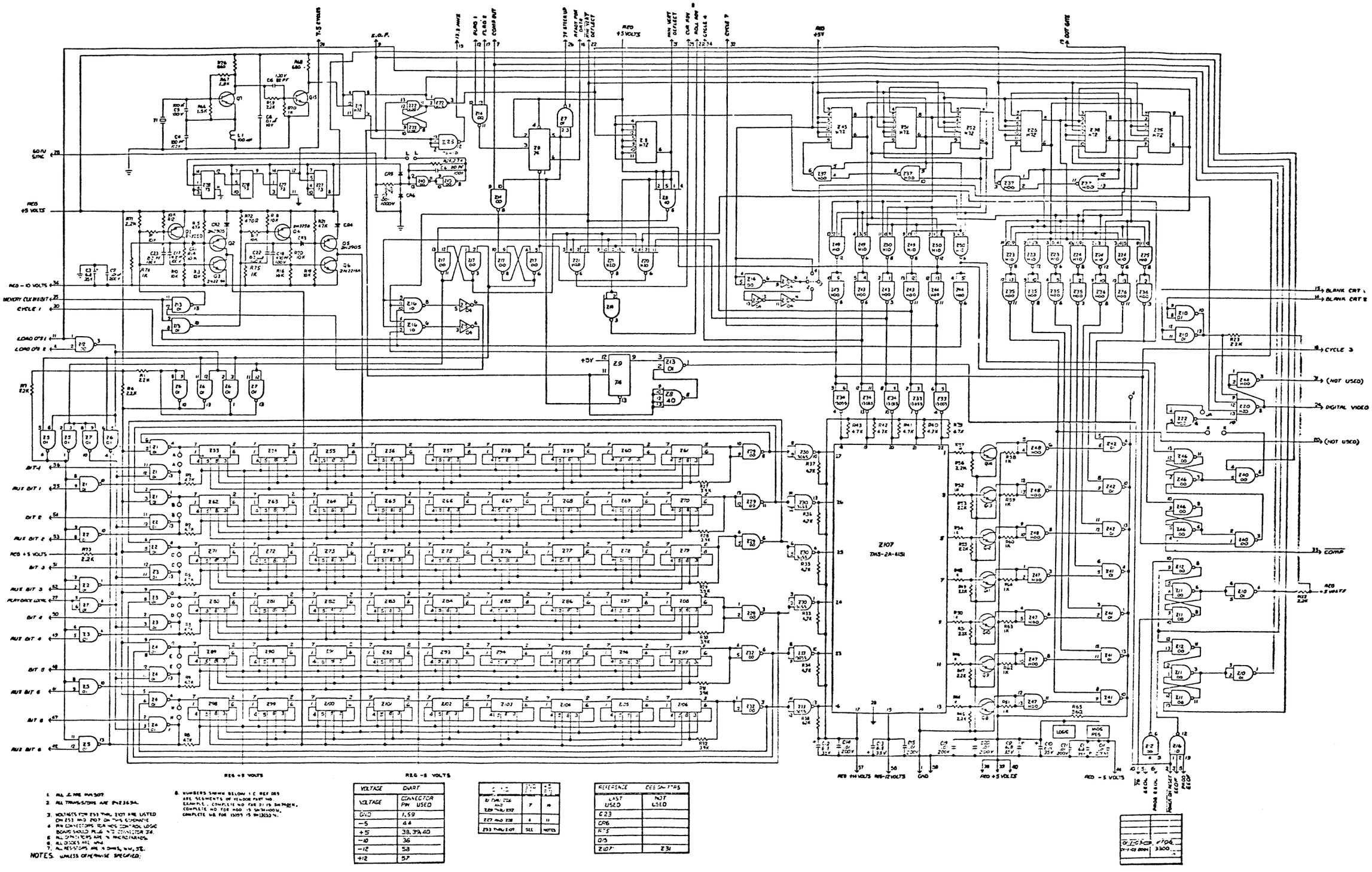


Figure 2-14. Schematic Diagram, MOS

The transistors Q8 through Q14 convert MOS LEVELS to logic levels and passes them through gates Z47 and Z48. The outputs of Z47 and Z48 enable the dot gates Z41 and Z42 when a "one" is present. While each seven bit word is present, the dot generator scans each gate in sequence. The outputs of Z41 and Z42 are collector ORed (wire ORed) together so that if any one gate is satisfied, a pulse appears at Z22 pin 4. The dot pulses are ORed with cursor pulses by Z22. The cursor occurs at compare time and consists of all 35 dots. A 3.75 Hz signal from Z27 pin 8 is gated with the cursor enable at Z40 pin 4. The output of Z40 pin 6 is a 35 dot burst occuring approximately every 20 frames, thus giving the cursor a blink rate of about three times per second. The output of Z22 pin 6 is gated with the 13.3 MHz clock, Cycle 1 and the CRT blanking ihhibits at gate Z20. The output of Z20 at pin 8 is the minor vertical deflection modulation. The inverter Z44 provides the compliment of the minor vertical deflection modulation at Z44 pin 3. The dot times occur at 75 nano-second intervals with each dot being 37.5 nano-seconds wide. The 5 x 7 dot matrix generation for the character "A" is shown in figure 2-15.

A malfunctioning MOS is indicated by a character changing when a displayed line of characters is rolled up or down the screen.

To identify a faulty MOS in LOCAL mode, momentarily depress HOME UP key and then ERASE EOF key. Type alternately the @ symbol and the question mark (?) until the first display line is filled, e.g. @ ? @ ? @ ? @ ?, etc. This loads characters into the MOS which will exercise maximum change within the MOS, since the @ symbol is a binary code of 1000 000 and the question mark (?) is a binary code of 0111 111. (Only the first six bits are significant to character display and are stored in MOS.)

If this displayed line is now moved down the screen, using the ROLL DOWN key, any character change in the displayed line is indicative of a faulty MOS at that point in the memory. Identify on which line the character changed and which character it is in the displayed line.

By using the code assignments shown in Table 1-2, identify which of the six bits in the symbol is changing, e.g. the 39th character changed from the @ symbol to a B when moved to the 12th line. The binary code change was from a zero to a one in Bit 2.

Using this example, refer to figure 2-17, and locate the changing character position in the 39th vertical column of spaces and the 12th line down. This space location shows the changing character is stored in the MOS cans located in the 5th column on the MOS card. Refer to the MOS locater in figure 2-16 and the faulty MOS is in the Bit 2 row under the 5th column.

To completely check every MOS, repeat the procedure but this time start typing the display line with the question mark (?) and then the @ symbol, e.g. ? @ ? @ ? @ ? @ etc.

To preclude rolling the displayed line off the screen, use the cursor HOME UP prior to ROLL UP or the cursor HOME DOWN prior to ROLL DOWN and the cursor will indicate the 1st display line or the 25th display line, respectively.

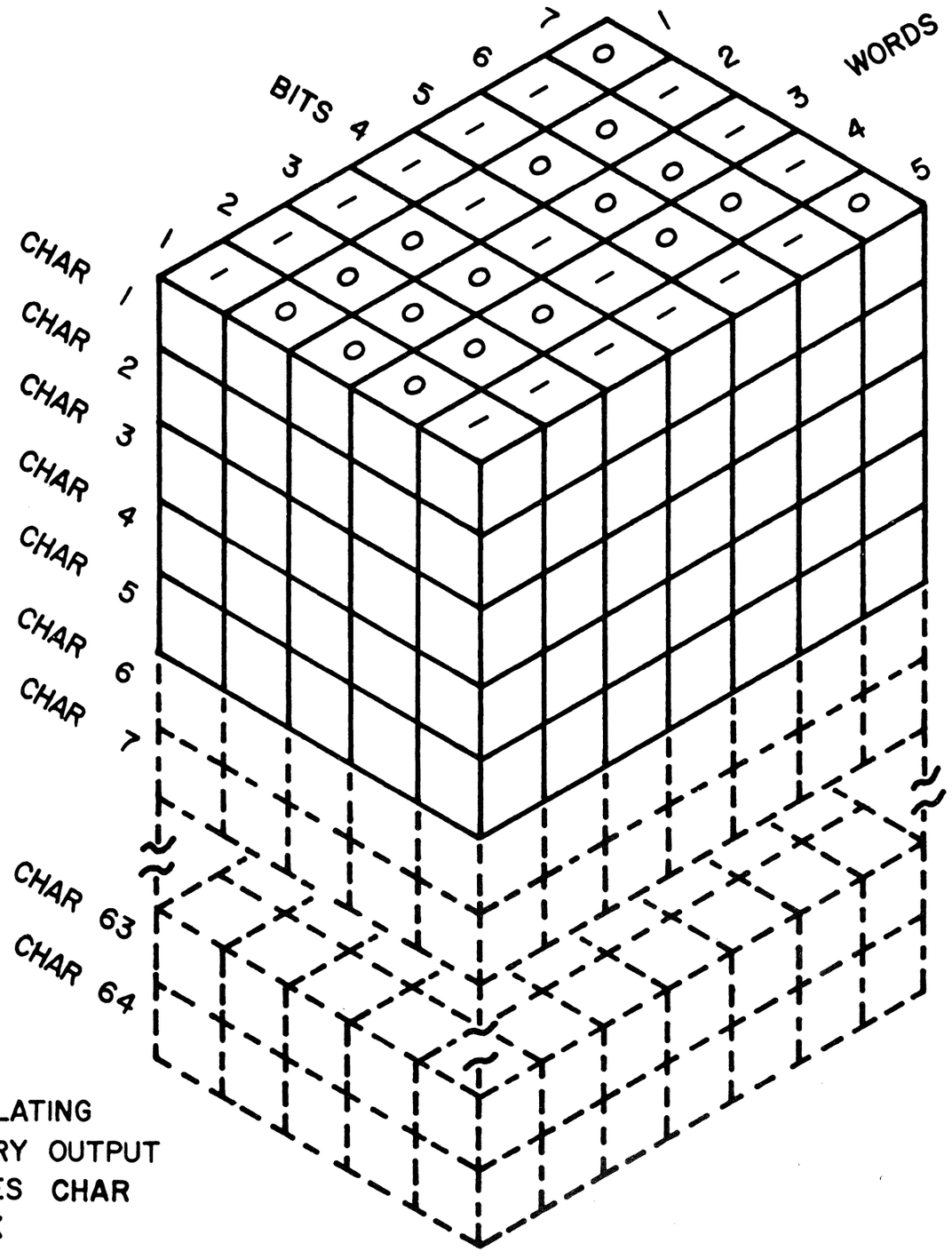
DEFLECTION AMPLIFIER

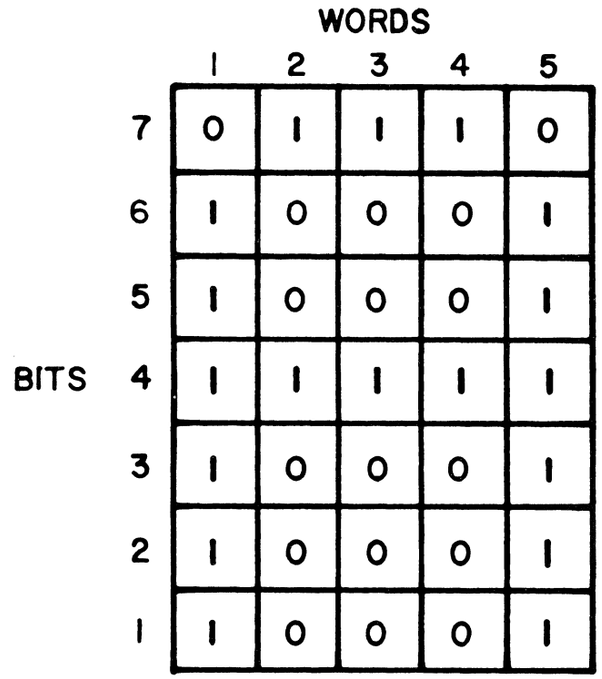
The Deflection Amplifier card contains the write, vertical and horizontal deflection amplifiers, the video amplifier and the RS-232-B converters.

Figure 2-20 is a functional block diagram and figure 2-21 is a schematic diagram. This explanation makes reference to figure 2-21.

The 950 KHz minor vertical delfection square wave from the MOS card enters the deflection board at connector pin 13. Transistor Q6 provides isolation of the logic on the MOS card from the higher DC voltages present in the write amplifier. The output of Q6 is clamped by diode CR7 and passed through the filter consisting of C5, C6 and L2. The filter circuit removes the DC component of the wave and makes the waveform symetrical around ground. Transistors Q7 and Q8 form a differential input to the operational amplifier formed by Q7 through Q13. Transistors Q9 and Q10 form a current source for the output base drivers. As the voltage at the base of Q7 increases in the positive direction, Q7 begins to conduct, shunting some of the current that

ROM
FORMAT





CYCLE COUNTER STROBES OUT FIVE WORDS FROM SELECTED BLOCK.

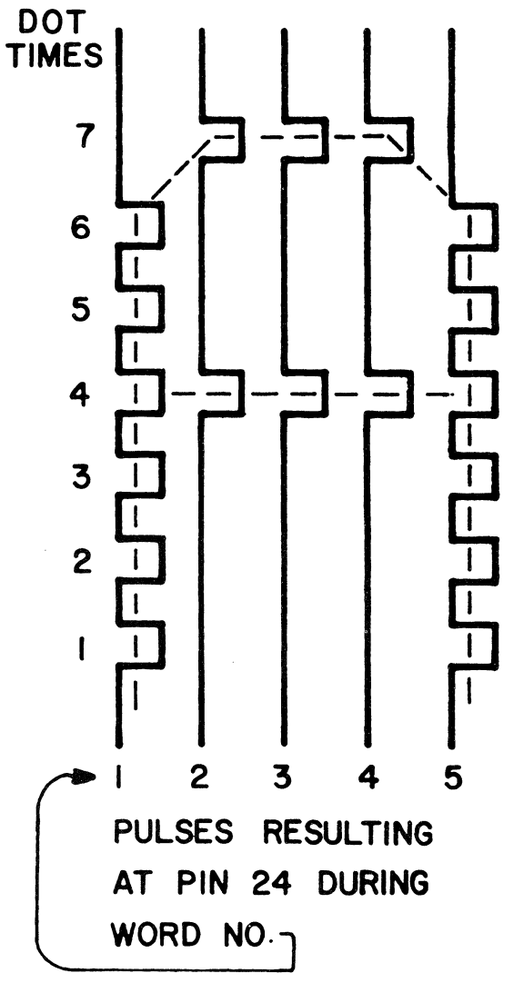


Figure 2-15. Dot Matrix Generation

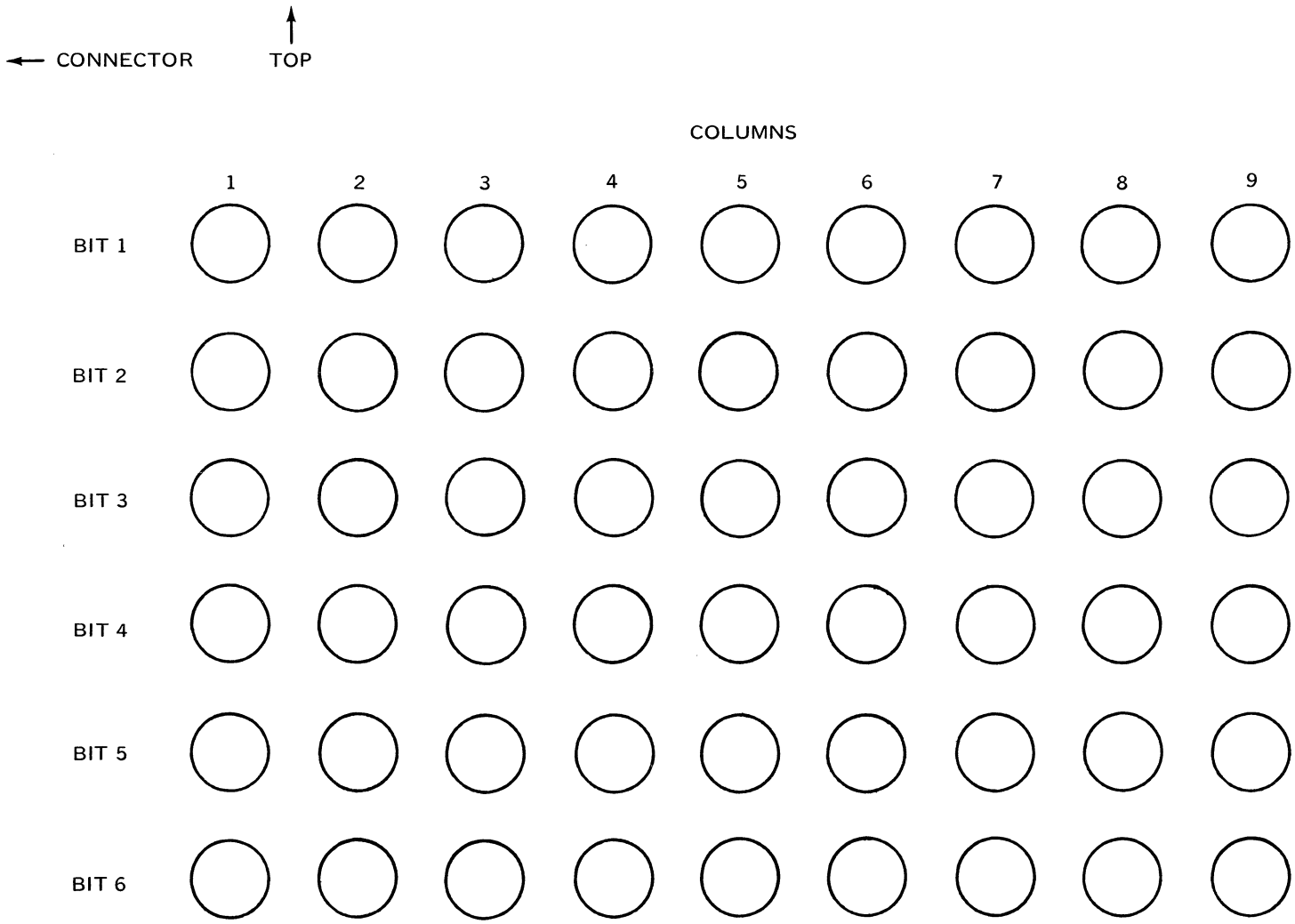


Figure 2-16. MOS Locator

CHARACTER SPACES

10 20 30 40 50 60 70

DISPLAY LINES

1 COLUMN 1 72
73 COLUMN 1 144
145 COLUMN 1 200 201 COLUMN 2 216
217 COLUMN 2 288
5 289 COLUMN 2 360
361 COLUMN 2 400 401 COLUMN 3 432
433 COLUMN 3 504
505 COLUMN 3 576
577 COLUMN 3 600 601 COLUMN 4 648
10 649 COLUMN 4 720
721 COLUMN 4 792
793 COLUMN 4 800 801 COLUMN 5 864
865 COLUMN 5 936
937 COLUMN 5 1000 1001 COLUMN 6 1008
15 1009 COLUMN 6 1080
1081 COLUMN 6 1152
1153 COLUMN 6 1200 1201 COLUMN 7 1224
1225 COLUMN 7 1296
1297 COLUMN 7 1368
20 1369 COLUMN 7 1400 1401 COLUMN 8 1440
1441 COLUMN 8 1512
1513 COLUMN 8 1584
1585 COLUMN 8 1600 1601 COLUMN 9 1656
1657 COLUMN 9 1728
25 1729 COLUMN 9 1800

Figure 2-17. Character Display

had been going through Q9. As Q7 conducts, Q8 conducts less, due to the increasing positive voltage at its emitter. This causes more current to flow through Q10, which is inverted by Q12. This action decreases the drive to the bases of Q11 and Q13 and the output drive of their emitters is decreased. The output transistors Q11 and Q13 drive the bases of the power drivers that are mounted on the air duct on the back panel. (See figure 3-14).

Figure 2-18 shows the general connection from all three of the deflection amplifiers to the power drivers on the rear panel. The diodes CR8, CR9 and CR10 are connected between the base of Q11 and Q13 to approximately match the four base-emitter junctions of the base drivers, Q11 and Q13 and the power drivers on the rear panel. This diode arrangement prevents any distortion of the output due to zero crossover.

All three sweep amplifiers are identical except for the feed-back source. The write amplifier uses voltage feed-back while the vertical and horizontal amplifiers use a current feed-back taken from the sense resistor on the particular yoke.

The geometry of the CRT is such that the characters are distorted at the sides of the tube, both in height and width. The characters tend to be short and wide at each side and uniform in size at the center of the tube. To correct for this geometric distortion, the horizontal current is monitored from the sense resistor and brought into Q2 and Q3. These transistors provide a steady current through CR13, which develops a voltage across R9 in proportion to the horizontal sweep position. The voltage at R9 is connected through R39 to control the charging rate of the horizontal sweep capacitor, C18.

The output of Q2 and Q3 is also inverted by Q4 and passed through the emitter follower, Q5. The output of Q5 sets the clamp voltage on CR7. This results in the output of Q6 being clamped at a higher voltage at the beginning and end of the sweep than it is clamped to at the center of the sweep. This allows the characters that are normally smaller on the sides of the CRT to have more gain than those in the center. The net result is characters of uniform height across the entire sweep.

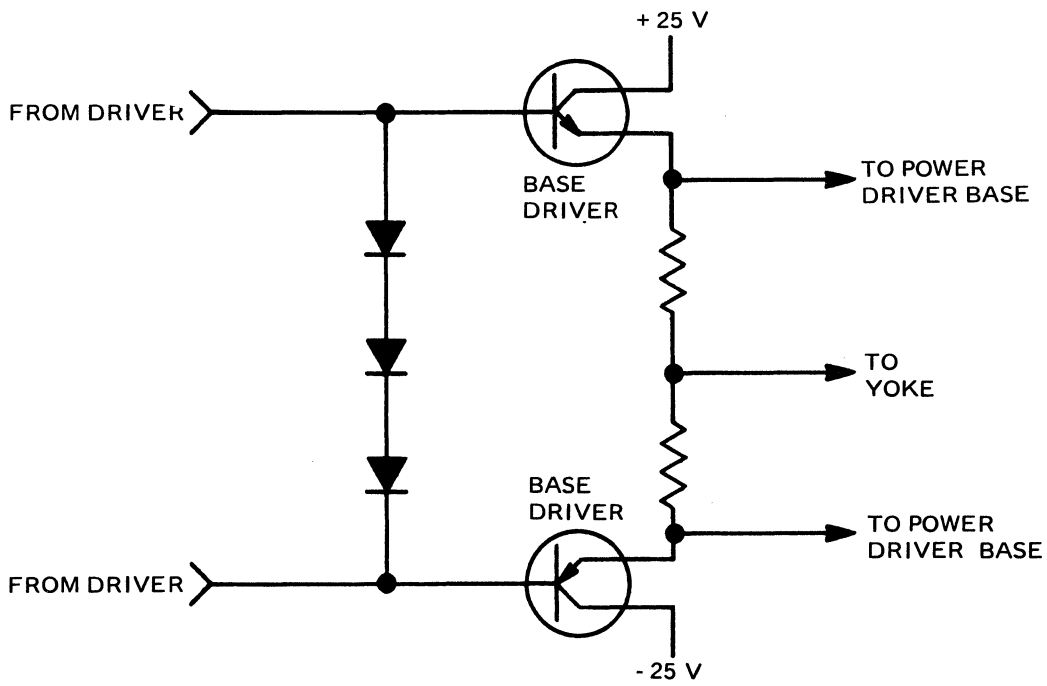


Figure 2-18. Driver Connection

The horizontal ramp frequency from the control logic enters the card at pin 29. Transistor Q14 is an inverter to control the conducting time of Q15. Transistor Q15 is a current generator to charge the sweep capacitor C18. The base of Q15 is held at a constant voltage by VR1 and the charging current at the collector is controlled by the emitter circuit. The correction voltage is connected to the emitter of Q15 and controls the voltage at this point. At the beginning and end of the horizontal sweep, more current is drawn through R39 than is drawn through it at the center of the sweep. The result is a slower rate of charge on capacitor C18 at the ends of the sweep than in the center. The changing charge rate of capacitor C18 throughout the sweep compensates for the geometric distortion and results in characters of uniform size during the entire sweep.

The voltage ramp from C18 is passed through the emitter followers Q16 and Q17 to buffer the capacitor from the amplifier input. Two emitter followers are used (one NPN and one PNP)to compensate for the junction drops in the transistors which would cause an offset in the generated sweep.

Transistors Q18 through Q24 form the horizontal amplifier which is identical to the write amplifier previously described.

The vertical sweep is controlled by the output of the line counter on the control logic card. The inverted inputs from the counter enter the deflection card on pins 5 through 9. Gates Z1 and Z2 form the input to a digital to analog converter. The base of Q26 is the summing junction for the converter. When all of the outputs of Z1 and Z2 are at ground, the only current available at the summing junction is through R72 which has a resistance value chosen to place the first line of the sweep in the desired position.

Resistors R67 through R71 have chosen resistances that will allow current flow in a binary magnitude, e.g., with the same source voltage, each resistor will pass two times the current as the one before. The output of the line counter is a binary count, therefore, the current at the summing junction increases in a binary progression.

The voltage source for resistors R67 through R71 is held at 5V through matched diodes CR18 through CR22. The transistor Q25 is a regulator used to hold the 5V generated across VR2 at a constant level. The values of R60 through R64 are chosen to provide a constant current from each circuit when the corresponding gate input is not active.

The current summing junction is the input to the vertical amplifier which is identical to the write amplifier previously described.

Digital video pulses from the MOS card enter the deflection card at pin 38. The resistor R3 and diodes CR1 and CR2 are a terminating network that supresses any overshoot or undershoot that is commonly present on high-speed pulsed lines. The pulses are coupled to Q1 through C1. The collector of Q1 contains the peaking coil L1 which ensures a sharp video pulse of approximately 40 V amplitude. The diodes CR3, CR4, CR5 and CR6 protect Q1 from either excessive saturation current or from the inductive kick developed by L1.

In order to protect the video amplifier from internal CRT arcs to the grid, the output of Q1 is AC coupled by C3 to the output, pin 30. Diodes CR12 and CR34 restore the coupled signal to near ground level. The Transorb and Driver diode serves as an arc suppressor to protect the circuit.

There are two identical RS-232-B receive circuits on the deflection board, the receive data circuit consisting of Z3 and the carrier detect circuit consisting of Z1. The RS-232-B carrier detect signal enters the deflection card at pin 10 where diodes CR32 and CR33 clip the input at 5V and ground respectively. Gate Z1 produces a logic level out while R2 and C30 prevent any oscillation of the circuit caused by poor rise times of the input signal. The receive data circuit is identical in operation.

There are three identical RS-232-B transmit circuits on the deflection card. The RO Data Circuit consisting of Q33 and Q34, the Transmit Data Circuit consisting of Q35 and Q36 and the Request-to-Send Circuit consisting of Q37 and Q38. The data to be transmitted enters the

circuit at pin 51. The input is pulled up by R99 and clamped to 5V by CR31. When the input at pin 51 is positive, indicating that a mark is present, Q35 conducts, furnishing base drive to Q36 which conducts, causing the output at pin 52 to approach -12V. When the input at pin 51 is ground, indicating a space, Q35 does not conduct and Q36, having no base current, does not conduct. The output at pin 52 at this time is +13V. The resistor, R111, protects the output transistor Q36 from externally applied short circuits to ground.

The circuit consisting of Z3 and Q39 normally is the circuit used for the reverse channel transmit circuit, however, it may be used to provide a current loop interface circuit. The reverse channel signal from the Interface 2 card enters the deflection card at pin 47. The level at pin 18 is from the keyboard and is high, except when the BREAK key is depressed. When the output of Z3 pin 3 is low, the transistor Q39 does not conduct and the output at pin 56 is +13V. When Z3 pin 3 is high, the output at pin 56 is ground. When the BREAK key is depressed, the input at pin 18 goes low forcing Z3 pin 3 high and the output at pin 56 goes to ground.

A current loop interface, referred to earlier, may be provided if the circuit for Z3 and Q39 is modified. Using an Elco pin pusher, remove the contacts from connector locations 18, 47 and 56. Tape these wires and turn them back into the harness. Push the pin out of location 51 and insert it into position 47. Push the pin out of location 52 and insert it in position 56. If the computer furnishes drive from a voltage source greater than 5V, the preceeding modification is all that is required. If the computer drive is from a voltage source less than 5V, on the deflection card, resistor R88 must be shorted and a 10K ohm resistor added from connector pin 55 to a -12V source. With this modification, the transmitted data is available on J9 pin 3. Connector pins 1 and 7 are ground points.

LOGIC POWER SUPPLY

The Logic Power Supply consists of six separate supplies, operating from one common transformer. The voltages provided are:

1. +5VDC
2. −5VDC
3. −12VDC
4. +13VDC
5. +25VDC
6. −25VDC

The negative going pulse used for POWER ON RESET is developed from the REG +5VDC circuit within the Logic Power Supply.

On early models of the Datapoint 3300, an over-voltage protection circuit was incorporated to disable the +5VDC output if an over-voltage condition occurred.

The theory of operation deals with the +13 VDC supply The same theory will apply to the +5 VDC supply. The -5VDC and -12VDC supplies are complements of the positive supplies.

The block diagram in figure 2-19 is typical of the functions within the 5, 12 and 13 volt supplies.

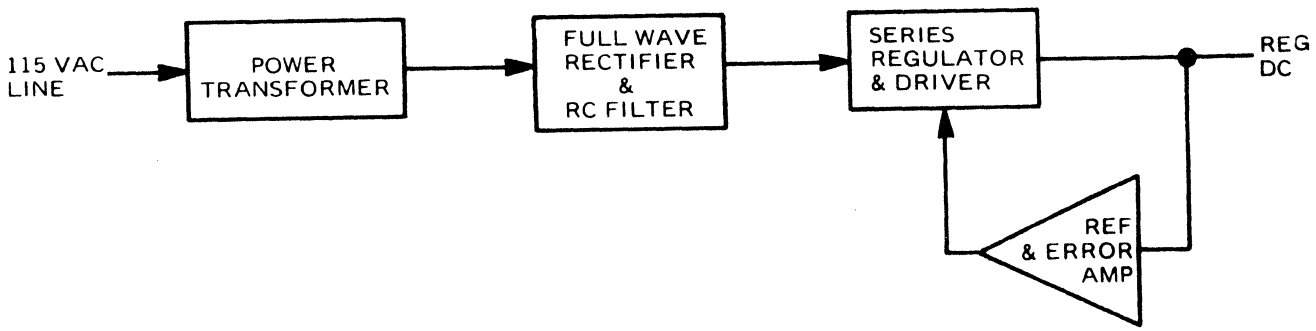


Figure 2-19. Typical Power Supply Block Diagram

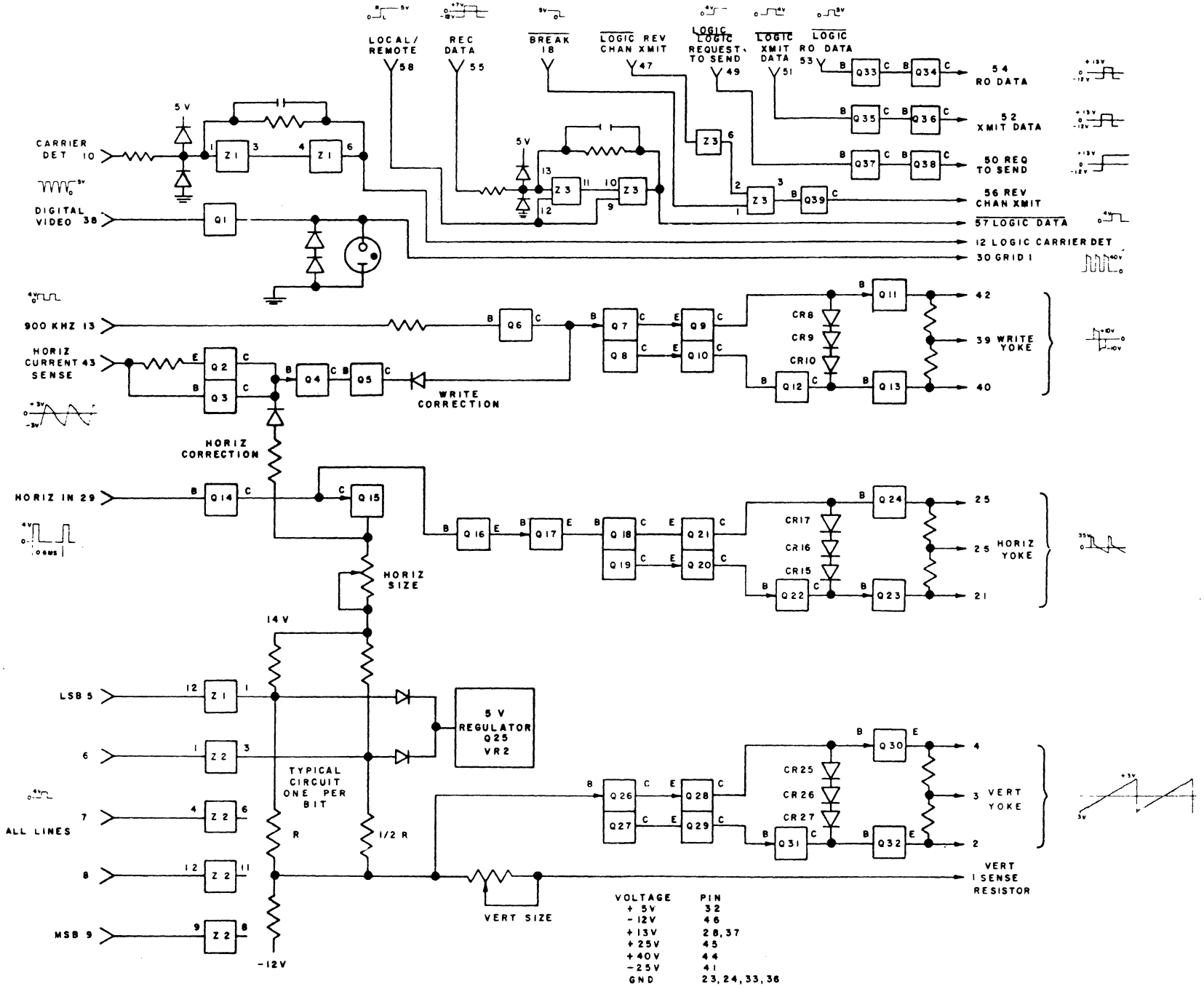
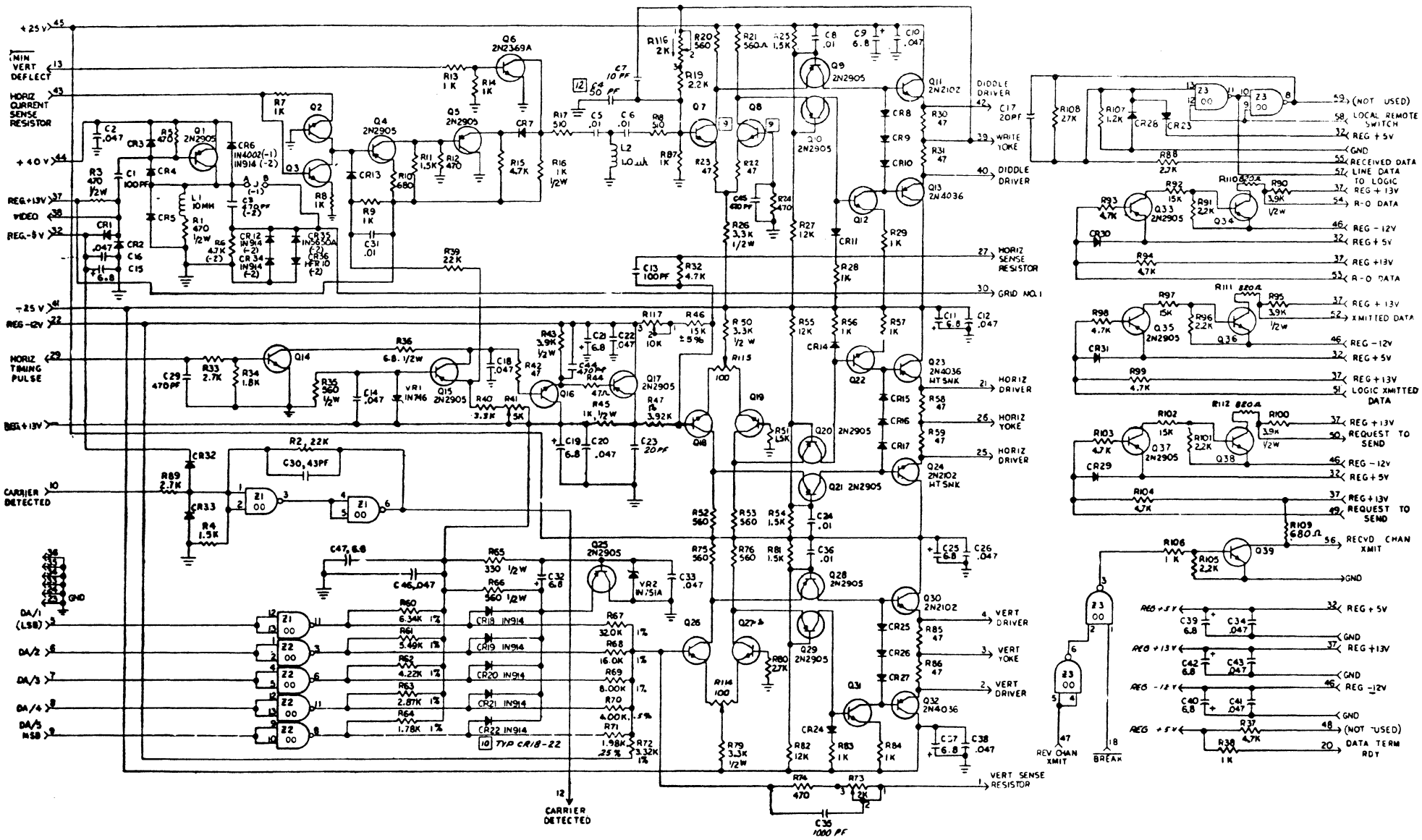


Figure 2-20. Block Diagram, Deflection Amplifier



7. ALL TRANSISTORS ARE 2N2219A
6. ALL DIODES ARE IN914
5. ALL CAPACITANCE VALUES ARE IN MICROFARADS,
4. ALL RESISTOR VALUES ARE IN OHMS, ± 5 %, 1/4 W
3. LOGIC SYMBOLS PER MIL-STD-806, ELECTRONIC SYMBOLS PER USA-STD-Y32.2-67
2. NUMBERS SHOWN BELOW REFERENCE DESIGNATION WITHIN LOGIC SYMBOLS ARE SEGMENTS OF VENDOR PART NUMBERS DESCRIBED IN PARTS LIST
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND / OR ASSEMBLY DESIGNATION

NOTES: (UNLESS OTHERWISE SPECIFIED)

[12] C4 IS 100PFD ON BOARDS PRIOR TO J REV

11 PINS ON DEFLECTION AMPLIFIER BD PLUG INTO CONN. J1

[10] CR18 THRU CR22 MATCHED TO 10MV

[9] Q7 & Q8 MUST HAVE MATCHED BETA

8. POTENTIOMETER R114 & R115 ARE SPECTROL P/N 62-1-1-101

VR2	
L2	
Z3	
R117	
Q39	
CR36	

Z1-Z3	3	7
I.C	+5V DW	GN. DW

Figure 2-21. Schematic Diagram, Deflection Amplifier

The three major sub-circuits of the +13VDC power supply (See figures 2-22 and 2-23) are as follows:

1. Diodes CR3 and CR4, CR17 and CR18 and capacitor C2 comprise the rectifier-filter circuit. Pins 13 and 14 from the power transformer provide in excess of 14VAC to rectifiers CR 3 and CR4, CR17 and CR18 with respect to ground. The pulsating DC from CR3 and CR4 is smoothed by the RC filtering action of C2.

2. The series regulator and driver circuit consists of series regulator Q1 and driver transistor Q2, resistor R1, Zener diode CR21 and capacitor C22. The series regulator circuit controls all current to the load from the rectifier-filter circuit in response to signals from the error amplifier. A driver circuit is provided in the base of the series regulator to increase the current gain of the error signal. All current to the load must flow through the series regulator Q1. Therefore, the voltage drop across Q1 for a given current will determine the voltage across the load. The drop across Q1 is solely dependent upon the feed-back signal from the error amplifier within the limits of regulator Zener diode, CR21 and resistor R1 limit the voltage drop across Q1 to a safe value. These two components do not appear in the 5 volt power supplies since a 5 volt drop is entirely within the capability of the series regulator transistor. Capacitor C22 in the base of Q1 assures a smooth and well damped response of Q1 to signals to the error amplifier.

3. The Reference and Error Amplifier is a common mode differential amplifier, consisting of transistors Q3 and Q4; resistors R2, R3, R4, R11, R33; Zener diode CR5 and capacitors C1 and C3. Since the amplifier is differential, many of the effects of heat and component aging are cancelled. Zener diode CR5 provides the reference potential on the base of Q3. When the potential at the base of Q4 is identical to that on the base of Q3, the amplifier is considered to be in balance, and no error signal results. Any deviation of the base of Q4 from the reference level of Q3 would result in an unbalanced condition. The resultant signal from the error amplifier would cause a change in base voltage on driver Q2 and would ultimately vary the drop across Q1 to compensate for the deviation in supply voltage

To clearly understand the operation of the 5, 12 and 13 volt power supplies, assume the +13 volts power supply to be operating at the nominal +13 volts DC level. Assume that due to variations of line or load or both, the voltage across the load exceeds +13VDC. Since the voltage to the load exceeds pre-set level the base of Q4 will become more positive. The drop across Q4 will decrease causing its emitter and therefore the emitter of Q3 to go more positive. Since the emitter of Q3 is now more positive with respect to its base (which is held at the reference potential), the current through Q3 will be diminished. The drop across R33 in the collector of Q3 will be less, causing the base of Q2 to go more positive. Q2, being a PNP transistor, will decrease its current to the base of Q1. When the base of Q1 goes less positive, the drop across Q1 will increase such that the voltage appearing on the output terminal of the power supply will again be the nominal 13 volts, and the voltage at the base of Q4 will return to the pre-set level.

Now assume that due to line or load variations the potential at the output terminal of the +13 volts power supply should drop below the nominal 13VDC value. The base of Q4 would go less positive decreasing the current thru Q4. The emitter of Q4 would then become less positive. Since Q3 and Q4 share a common emitter resistor, R4, the emitter of Q3 would also become less positive. Again, since the base of Q3 is held at a fixed reference potential, if the emitter becomes less positive the current through Q3 would increase, causing a greater drop across collector resistor R33. The base of driver, Q2, would therefore go less positive, increasing the current to Q1. The drop across Q1 would decrease, thus increasing the potential at the power supply output terminal to the nominal 13 volts.

Capacitor C1 provides additional filtering at the output terminal and minimizes variations in voltage which would exceed the response time of the regulator circuit. R11 provides a means of adjusting the output voltage to a nominal 13±1VDC.

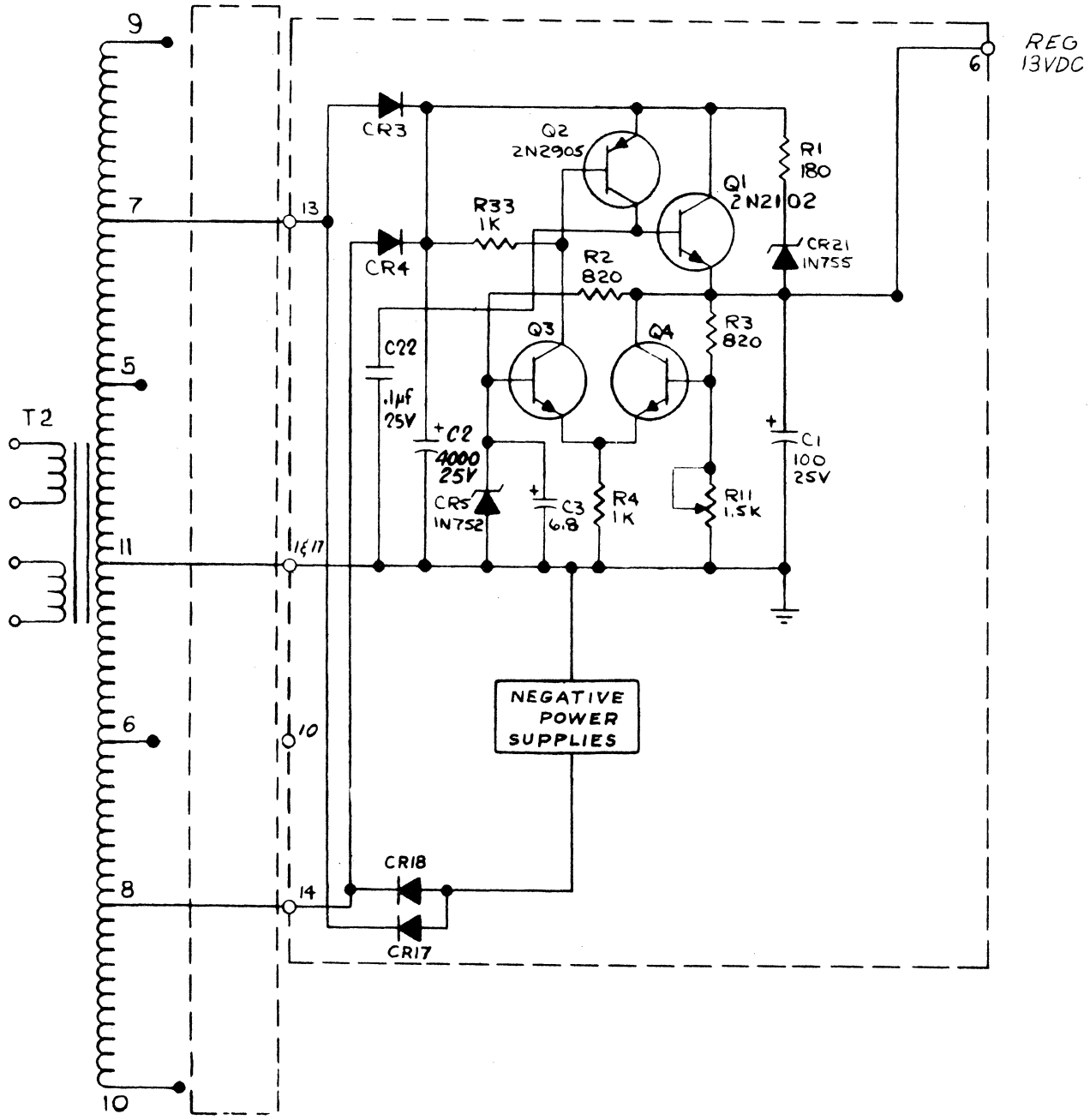


Figure 2-22. +13VDC Power Supply

The +25VDC and -25VDC used for the deflection drivers is obtained from transformer T2. Plus 25 volts is obtained by rectifying the output of T2 pins 9 and 10 across CR6 and CR7, CR8 and CR9. Filtering is accomplished with C17. The output is to the +25VDC fuse F2. Negative 25 volts is a complement of the +25VDC supply with filtering accomplished by C18. The output is to the -25VDC fuse F3.

Power On Reset

The power on reset circuit consists of R13, C8, R17, Q15, R14, C7, R15, R16, Q18, R18, R19, R34 and Q16. (See figure 2-23.)

The purpose of the circuit is to provide a negative going pulse to the POWER ON RESET BUS during a brief interval following turn-on of the +5VDC supply, thus assuring a resetting of all logic elements each time power is recycled.

When power is first applied to the reset circuit, capacitors C8 and C7 will be discharged (C8 by R17 and C7 by R14, R15 to the +5VDC bus). The base of Q18 will immediately go sufficiently positive to turn off Q18. As a result, Q16 will be turned off.

Meanwhile, after a time constant determined by values of C8 and R13, C8 will charge to a value sufficiently positive to saturate Q15 bringing the negative side of capacitor C7 to approximately ground potential. For a brief time interval (determined by the values of C7 and R15), Q18 will saturate and remain in this state until C7 has charged, thus driving Q16 into saturation and providing a negative going pulse to the Power On Reset bus. As C7 charges, the base of Q18 will then become sufficiently positive to cut off Q16, thereby restoring the conditions which existed immediately following application of power.

DEFLECTION POWER SUPPLY

The Deflection Power Supply provides additional voltages for the deflection circuits. Figure 2-24 shows the +40VDC portion of the Deflection Power Supply.

Approximately 40VAC from transformer T2 is applied to the bridge rectifier, CR3 - CR6. The full wave rectified output is filtered by C2, R5 and C7 and is clamped by Zener diode CR5 to produce a +40VDC output at pin 6.

Figure 2-25 shows the circuitry which provides +120VDC and +450VDC to the deflection circuits. Approximately 550VAC from the secondary of T2 is applied to the power supply on pin 1. A +450VDC output on pin 4 is provided by rectifier CR1 operating in the RC filter R8 with C3 and C4. The +120VDC supply is derived from the +450VDC supply through divider R1 and R22. R2 and R3 are the bleeder resistors for the Deflection Power Supply.

Figure 2-26 is the schematic diagram of the complete Deflection Power Supply circuitry.

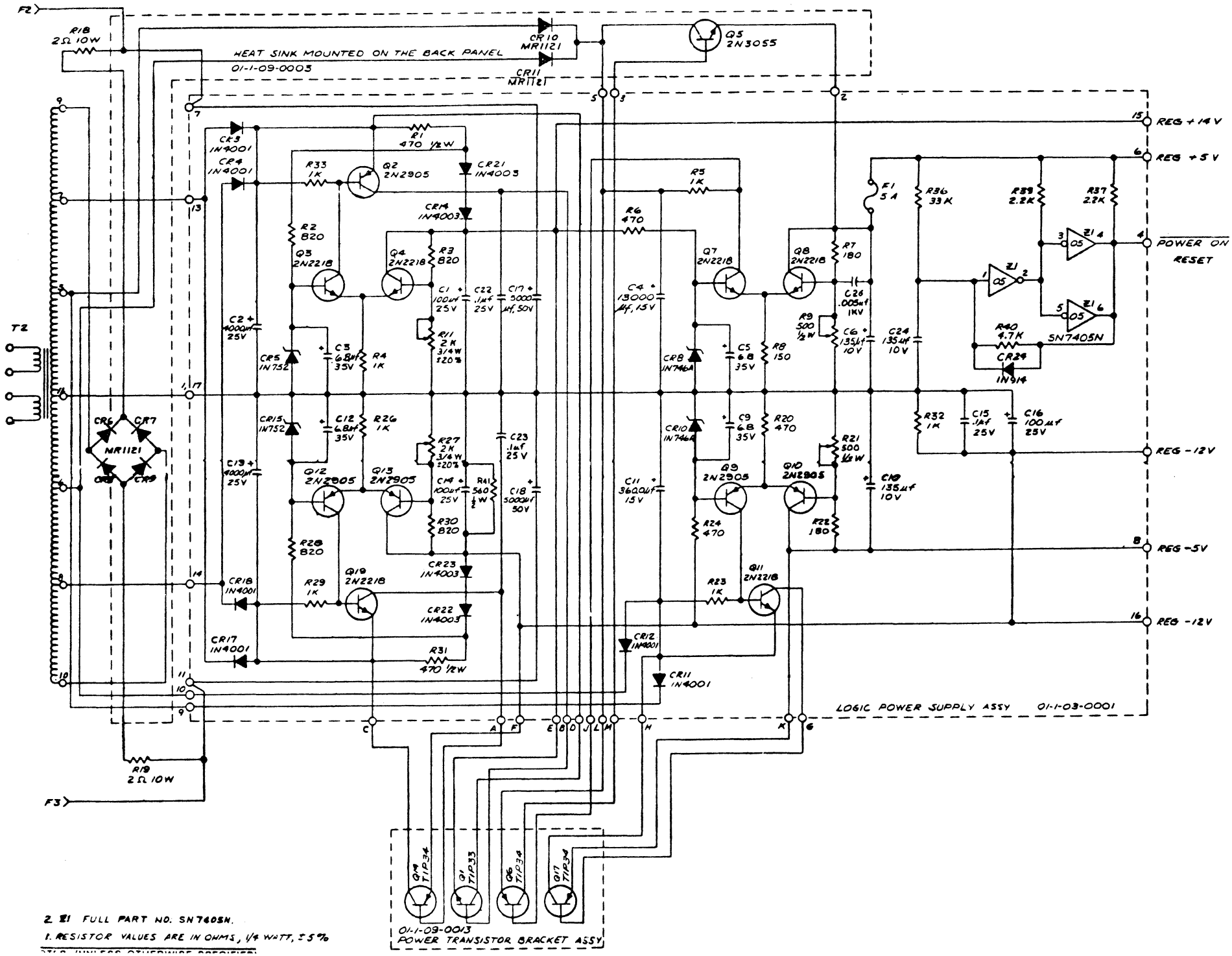


Figure 2-23. Schematic Diagram, Logic Power Supply

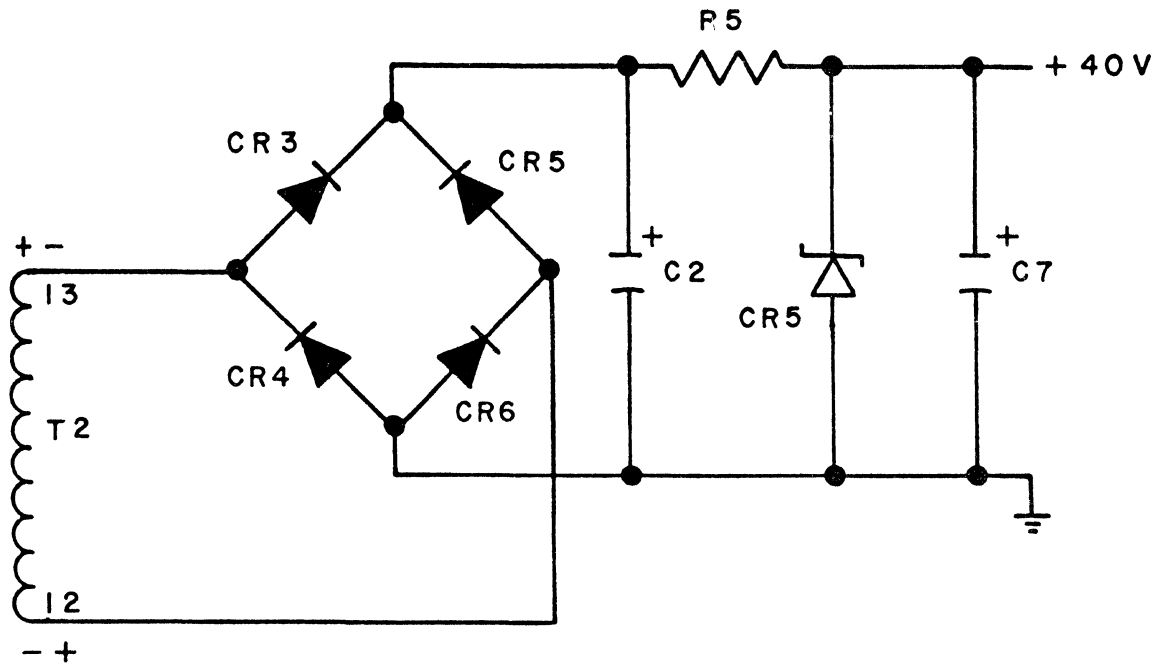


Figure 2-24. +40VDC Circuit

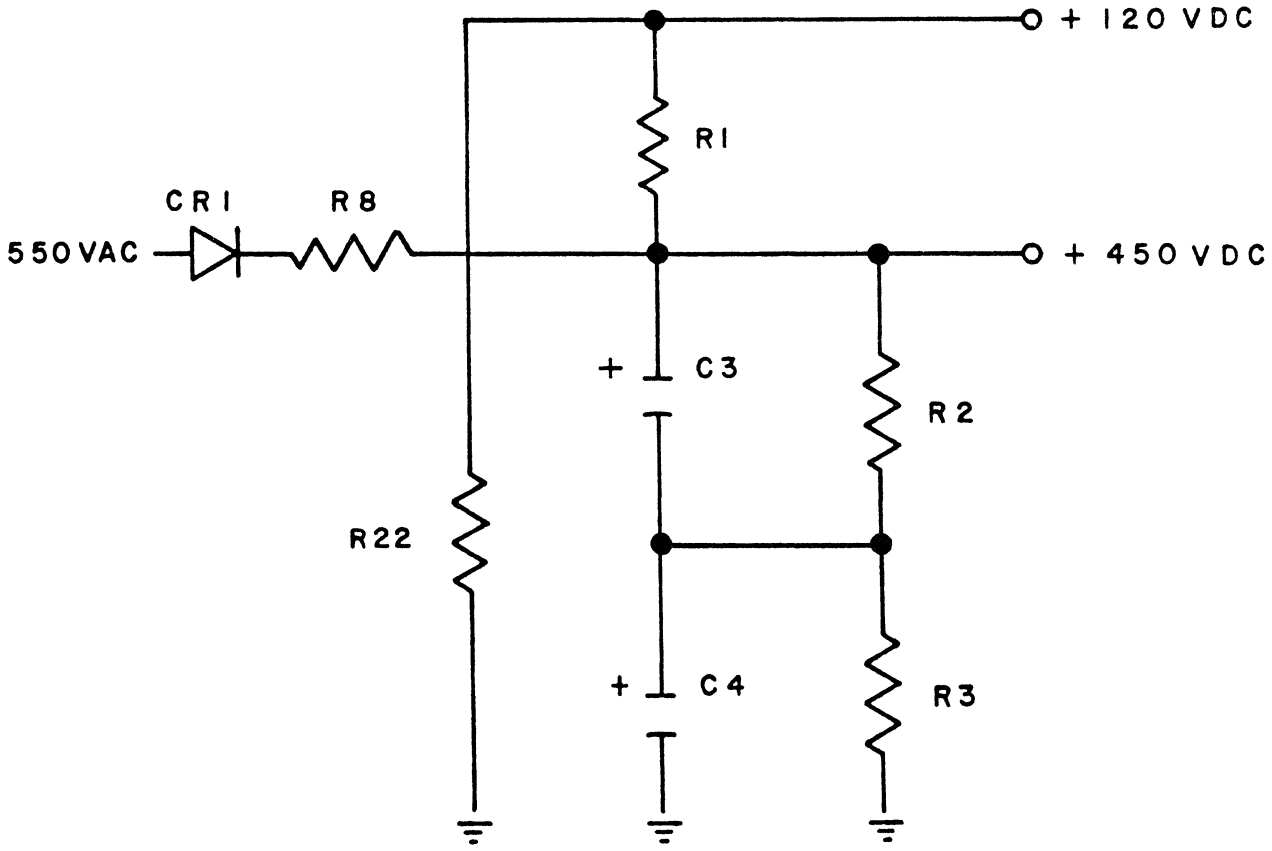
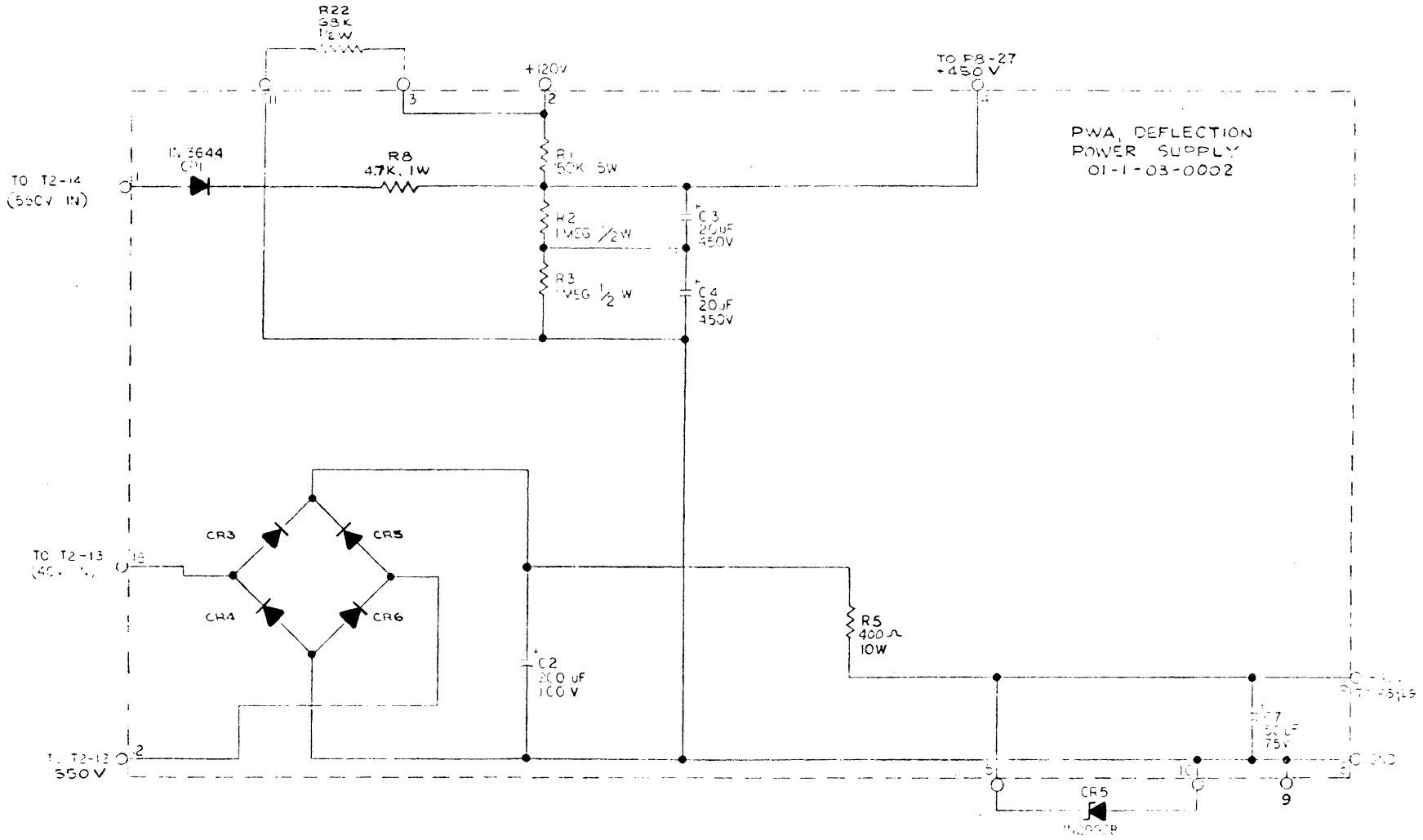


Figure 2-25. +120VDC and +450VDC Circuit



[illegible]	330Ω
[illegible]	VTO2
NEXT ASSY	USED ON
APPLICATION	

2. RESISTANCE VALUES ARE IN OHMS.

1. ALL DIODES ARE IN4003.

NOTES: (UNLESS OTHERWISE SPECIFIED)

Figure 2-26. Schematic Diagram, Deflection Power Supply

HIGH VOLTAGE POWER SUPPLY

The High Voltage Power Supply is a sealed unit. When 95 - 135VAC, at 60 Hz, is applied to the input tab sockets, 15,000 VDC will be present at the output high voltage lead. If input voltage is correct and 15 KVDC is not present, replace the High Voltage Power Supply.

CONTROL LOGIC

General

The functions of the Control Logic card are
(1) Generate the horizontal and vertical timing pulses.
(2) Provide blanking pulses for horizontal and vertical retrace.
(3) Control the cursor movements (i.e. left arrow, right arrow, up arrow and down arrow).
(4) Provide line feed, carriage return roll up and roll down functions.
(5) All compare circuitry for data entry into circulating memory.
(6) All address counters for memory and cursor.

Horizontal Deflection Timing (See Figures 2-27 and 2-28.)

The horizontal deflection timing pulses are generated by a synchronous binary counter, consisting of Z62 through Z65, referred to as the Character Counter. The Character Counter Clock and cycle 7 pulses to the input pins of Z65 will increment the counter each character time. The Character Counter counts to 82 although there are only 72 characters displayed per line. The ten extra counts are to allow for horizontal retrace and recovery of the yoke after retrace. The Character Counter has a normal radix of 128, therefore Z86, Z76 and Z75 provide the necessary feedback to turn the Character Counter around at count 82. Z86 decodes a count of 82 (a binary count of 81 is actually the 82nd count, since the first count is zero) and returns the Character Counter to the zero state with the next clock pulse.

The N jumper at pin 6 of Z86 is provided to aid in isolating a malfunction within the Character Counter and feedback circuit. With the N jumper removed, the feedback path is broken and the Character Counter will cycle through its radix of 128. The output of each succeeding flip-flop in the counter chain will be twice the period of the preceding flip-flop. It is then a matter of determining whether the malfunction is in the counter chain or in the feedback path.

The horizontal ramp clock is generated by Z33, which is connected in a standard latch configuration. Z84 decodes the 72nd count and the output at pin 8 of Z84 is connected to pin 9 of Z33. When the 72nd count is detected, Z84 pin 8 drives Z33 pin 9 low, setting Z33 pin 8 high. At this point, Z63 pin 8 which connects to Z33 pin 13 is high. On the 80th count, Z63 pin 8 will go low, setting Z33 pin 11 to a high and resetting Z33 pin 8 to a low. The horizontal ramp is generated when Z33 pin 8 goes from a high to a low and is terminated when Z33 pin 8 goes from a low to a high. The horizontal sweep begins (left hand margin of the CRT) with the 81st count and ends (right hand margin of the CRT) with the 72nd count. The 81st and 82nd counts are not used to display information but do allow time for the horizontal yoke to gain speed. The function of the Clock Inhibit signal is to inhibit the clock pulses to the MOS recirculating register during horizontal retrace. Z66 pin 1 goes low on count 72 and remains in this state until the Character Counter cycles to the first count (zero state).

Vertical Deflection Timing

The vertical deflection sweep is generated by a synchronous binary counter which consists of Z60 through Z62 and is referred to as the Line Counter. Feedback is provided to change the Line Counter natural radix of 32 to a radix of 26. Z79 pin 12 goes low on the 26th count (binary count of 25 since zero is the first count) and in conjunction with Z70 pin 11 and Z13 pin 4, steer the counter-back to the zero state on the next clock pulse. The clock pulse to the Line Counter is generated by the Character Counter. Z84 decodes the 72nd count of the Character Counter and this count is inverted by Z75 to be applied to pin 2 of Z13. (Pin 3 of Z13 and pin 10 of Z12 will be considered at this time to be in the high state.) The pulse is gated through Z13 and Z12 and applied to Z82 which is an inverting buffer. Z82 has an extended fan-out capability and applies a low going clock pulse to the Line Counter.

The D/A 1 through D/A 5 outputs of the Control Logic card are the Q outputs of the Line Counter flip-flops. These outputs are used to drive the Digital-to-Analog converter which generates the vertical sweep signal. The End-of-Frame signal which leaves the Control Logic card on connector pin 16 is generated by JK flip-flop Z39 pin 8. The K input, pin 10 of Z39, is steered by Z79 pin 12 which is the decoded 26th count. The output of Z79 pin 12 is inverted by Z70. Pin 11 of Z70 drives the J input, pin 7 of Z39. The following clock pulse which sets the Line Counter to the zero state, clocks Z39 pin 8 low. Z39 pin 9 connects to Z66 pin 12. Z66 pin is wire-ORed with Z66 pin 1 which is the horizontal retrace clock inhibit signal. Z39 pin 9 stops high during the vertical retrace until the end of the first horizontal sweep. This forces Z66 pin 13 low during this period of time to inhibit the recirculating memory clock. In order to allow time for the recovery of the horizontal yoke after vertical retrace, the first horizontal sweep is not used to display information. This is why the Line Counter has a radix of 26 rather than a radix of 25. The End-of-Frame signal and the Clock Inhibit signal are gated together by Z12. The output, pin 11 of Z12, leaves the deflection card on connector pin 47 and is referred to as the Blank CRT 1 signal. This signal is used to blank the CRT display during the horizontal retrace and the vertical retrace. The 76th count of the Character Counter is decoded by Z83, inverted by Z72 and leaves the Control Logic card on connector pin 42. This signal is used on the MOS card to perform the Erase-End-of-Line function. The End-of-Frame signal is used to perform the Erase-End-of-Frame function.

Cursor Positioning

The positioning of the cursor on the CRT display is controlled by the Cursor Character Counter and the Cursor Line Counter. The Cursor Character Counter is an up-down 72 count counter, consisting of flip-flops Z43, Z44, Z45 and Z46 with their associated steering gates. The Cursor Line Counter is an up-down 25 count counter, consisting of Z40, Z41 and Z42 with their associated steering gates. The outputs of these two counters are compared to the outputs of the Memory Character Counter and the Memory Line Counter. These four counters are compared by Z50, Z51, Z52, Z54 and Z55 whose outputs are wire-ORed. The binary outputs of the Cursor Character Counter and the Cursor Line Counter indicates the location of the cursor in the CRT display. The output of the digital comparator, pin 9 of Z69, will remain low as long as the four counters are not in agreement. When the two sets of counters compare, the comparator output will go high for a single character time. The pulse width of the digital comparator is narrowed by gating it with three signals from the MOS card. The digital comparator, Cycle 1, Dot gate and the Character Counter Clock are ANDed together by Z69. The digital comparator output is inverted by Z69 and the pulse width is reduced to a single dot time. The output of Z69 on pin 8 leaves the card on connector pin 18 and this same output is inverted by Z59 pin 13 to provide the Comparator Output from the card on connector pin 19.

The first character position on a line is represented by the zero state of the Cursor Character Counter. In order to move the cursor to the right on the display, the Cursor Character Counter is incremented up, to move the cursor to the left the Cursor Character Counter is incremented down. The steer up and steer down lines of the Cursor Character Counter are jumpers A and L respectively. These lines are normally high. To steer the counter up, jumper A remains high while jumper L is pulled low. To steer the counter down, jumper A is pulled low while jumper L remains high. Jumpers A, L and K are provided into the counter so that trouble-shooting the counter may be simplified. By removing these jumpers, external steering controls and an external clock may be applied to the counter. The Cursor Line Counter is implemented in a similar manner to the Cursor Character Counter. Jumpers E and B represent the steer up and steer down lines respectively, of the counter. By removing jumpers E, B and C, external steering controls and an external clock may be applied to the Cursor Line Counter. It was noted earlier that the Line Counter used to generate the vertical deflection is a divide by 26 counter. The

first horizontal line after vertical retrace, is used to allow time for the horizontal yoke to recover rather than to display information on the CRT. The outputs of the first flip-flop, Z42 pins 9 and 8 in the Cursor Line Counter, are reversed from the normal configuration in that the $\overline{Q}$ output of Z42 is wired into the digital comparator as the Q input. This prohibits a comparator output for the first horizontal deflection line and allows a comparator output for the second horizontal deflection line. This means that the home up position is actually the first character in the second horizontal sweep. This allows time for the horizontal yoke to recover and gain speed after vertical retrace.

The Cursor Right, Cursor Left, Cursor Up and Cursor Down functions are decoded commands from the computer to increment the Cursor right, left, up or down. These commands are decoded on the Interface 1 card and are inputs to the Control Logic card. The Left Arrow, Right Arrow, Up Arrow and Down Arrow function are switch closure commands from the keyboard to move the cursor left, right, up or down. The Left Arrow, Right Arrow, Up Arrow and Down Arrow commands out of the Control Logic card are functions that indicate a keyboard switch has been closed. These outputs are wired back to the keyboard where they are encoded and then transmitted to the computer.

The Cursor Right function enters the Control Logic card on connector pin 9 and follows two paths. The first path is through Z78 pin 2, which inverts the signal and applies the inverted signal to Z57 pins 11 and 12, Z57 pin 13 is connected to jumper L, the steer down line and goes low to steer the counter up. The second path followed by the Cursor Right signal is to Z78 pin 4 where the signal is gated and inverted. Z78 pin 6 then connects to Z78 pin 9 and uprights the signal. Z78 pin 8 connects to Z28 pin 4. Z28 is a four input NAND gate. The other three inputs to the gate at this time are high, therefore with Z28 pin 4 going low, Z28 pin 6 goes high. Z28 pin 6 connects to Z7 pin 10 where it is gated with count 76 from the Character Counter. The output of Z7 pin 8 sets a latch, consisting of Z8 pins 1, 2 and 3 and Z7 pins 1, 2, 12 and 13. The output, Z8 pin 3, of the latch is gated with count 82 by Z8 pins 11, 12 and 13. Z8 pin 11 sets a second latch which resets Z8 pin 3 to a low. The output of the first latch now has a pulse on it which lasts from count 76 of the Character Counter until count 82. This pulse is inverted by Z16 pins 11, 12 and 13 and then gated, by Z16 pins 8, 9 and 10, with the normally high Cursor Advance Signal from connector pin 57. Z16 pin 8 is gated by Z26 with Z15 pin 8. Z15 decodes the zero state of the Cursor Character Counter and its output is high when clocking the Cursor Character Counter up. The output of Z26 is inverted by Z32 which drives the Clock line to the Cursor Character Counter. Since the steer down line had previously been pulled low, the application of the clock to the Cursor Character Counter by Z32 will now clock the counter up by one. The second latch, consisting of Z8, pins 4, 5, 6 and 8, 9 and 10, which was set by count 82, will be reset by Z28 pin 6 on the trailing edge of the data pulse. The output, Z8 pin 8 of this latch is inverted and buffered by Z86 and Z82 and leaves the Control Logic Board on connector pin 43. This signal, referred to as Line Feed Accepted, clears the holding register on the Interface 2 card and informs the Interface 2 card that the desired function has been completed. The Cursor Left function is performed in a similar manner to the Cursor Right function. The difference being that the steer up line (jumper A) is pulled to ground and the steer down line (jumper L) remains high. The Cursor Left clock path is also through Z28 pin 6. The clock pulse may be checked at Test Point 2.

The Cursor Up function enters the Control Logic Card on connector pin 34 and is normally high. The steering path for the Cursor Up function is through Z77 pin 12 and Z57 pins 5 and 6. Upon application of the Cursor Up signal, Z57 pin 4 drives the steer up line, jumper E, of the Cursor Line Counter low. The clock path for the Cursor Up function is through Z77 and Z28 pin 9. Upon application of the Cursor Up signal, Z28 pin 8 (Test Point 1), is driven high. The logic high signal on Test Point 1 is gated by Z17 with count 76 of the Character Counter. The output, Z17 pin 8, sets a latch which is reset by a second latch at count 82 of the Character Counter. (This technique is similar to that used for Cursor Right and Cursor Left.) The output of the first latch, Z58 pin 3, is wired through Z59 pins 4 and 5. The signal is passed by Z20 and presented to Z1 pin 11. Z1 pin 9 is connected to Z21 pin 8. Z21

decodes the zero state of the counter and inhibits clock pulses to the counter when the all zero state and a steer up signal are detected. Z1 pin 10 is connected to Z69 pin 6 which decodes the 25th count, corresponding to the 25th line. Z69 inhibits clock pulses to the counter when the 25th count and a steer up command are detected. If neither one of these states is detected by Z21 or Z69, Z1 pin 8 will present the pulse to Z32 to drive the clock line to the Cursor Line Counter. The Cursor Line Counter will then be incremented down by a single count.

The Cursor Down function is accomplished in a similar manner to that of Cursor Up. The steering path is through Z77 and Z57 pin 1. Z57 pin 1 drives jumper B low thus allowing the Cursor Line Counter to be incremented up. The clock path is through Z28 pin 8, Test Point 1, and may be checked at Test Point 1.

Switch bounce protection circuitry for allowing automatic repeating of the function after a slight delay are provided for these signals. The switch closure corresponding to the Cursor Right movement enters the card on connector pin 8 and is normally high. The steering path for this function is through Z78 and Z57. Upon application of the Right Arrow signal, Z57 pin 13 drives the steered down line, jumper L, low, thus allowing the Cursor Line Counter to be incremented up. The clock path for the Right Arrow signal is through Test Point 2. The switch closure is inverted by Z67, pin 11 the output, is connected to Z37 pin 11. The signal is still "bouncy" at this point and is inhibited by Z37 pin 10. The inverted switch closure from Z67 pin 11 is applied to Z47 pin 11. This forces Z47 pin 13 low, thereby setting a latch consisting of Z48 pins 11, 12 and 13 and Z48 pins 8, 9, 10. Z48 goes low and is connected to the input of Z38 pins 8 and 9 in 01 gate. The output, Z38 pin 10, is connected to an RC filter, consisting of R19 and C2, which smoothes out the switch bounce. After the filtering action, C2 charges up and forces Z49 pin 6 to go low. Z49 pin 6 sets a latch consisting of Z49 pins 8, 9 and 10 and Z49 pins 1, 2 and 3, forcing Z49 pin 8 to go high. Z49 pin 8 connects to Z37 pin 10. Since Z37 pin 9 is normally high, the bounceless switch closure is gated out of Z37 pin 8 which connects to Z28 pin 2. This forces Test Point 2 to go to a logic 1 state. From Test Point 2, the generation of the clock pulse for the Cursor Character Counter follows the identical path for the Cursor Right and Cursor Left functions.

If the Cursor Control switch is depressed and held, Z38 pin 13, will begin to charge C1. After a short delay, the charge on C1 is sufficient to forward bias CR1 and Q1. The collector of Q1 is connected to Z27 pin 5. Q1 going into saturation forces Z27 pin 6 high. Z27 pin 6 is connected to Z27 pin 12 where it is gated with a 7.5 Hertz signal which enters the Control Logic card on connector pin 36. The 7.5 Hertz will then be passed through to either Test Point 1 or Test Point 2, where continuous clock pulses for either the Cursor Character Counter or the Cursor Line Counter will be generated.

Carriage Return

The Carriage Return function is performed by clearing the Cursor Character Counter to the zero state. The Carriage Return signal enters the card on connector pin 39 and normally is a logic one. When connector pin 39 is pulsed, Z29 pin 8 is driven to a logic zero through a series of inverters and wired OR connections. Z29 pin 8 is connected to the Clear Inputs of the Cursor Character Counter and clears the counter.

Home Up

The Home Up function is performed by clearing both the Cursor Character Counter and the Cursor Line Counter to the zero state. There are three command signals which will home the cursor display up. These are:

1. The Power On Reset pulse.
2. The Decoded Home Up command.
3. The Home Up key switch closure.

The Power On Reset pulse enters the card on connector pin 6, the Decoded Home Up command enters the card on connector pin 5 and the Home Up key switch closure enters the card on connector pin 17. These three signals are normally a logic one and are gated together by Z68. If any of the signals are pulsed, Z68 pin 12 goes high and through a series of inverters and

wired OR gates, drives Z29 pin 8 low and clears the Cursor Character Counter to the zero state. Z29 pin 6 is also driven low, thus clearing the Cursor Line Counter to the zero state.

Home Down

The Home Down function is performed by clearing the Cursor Character Counter to the zero state and by counting the Cursor Line Counter to the 25th line with a burst of high speed clock pulses. Connector pin 11 is wired to the decoded home down command and connector pin 12 is wired to the Home Down key switch closure. These inputs are gated by Z78 and normally are a logic one state. When either of these inputs is pulsed, Z29 pin 8 is driven low and clears the Cursor Character Counter. Z59 pin 1 is connected to the steer down line of the Cursor Line Counter and is driven low. Z59 pin 8 is driven high and enables Cycle 3, a high speed clock, to be gated out on Z59 pin 10 which is the clock path for the Cursor Line Counter.

Line Feed and Reverse

The Line Feed function has two standard operating modes. When the Datapoint 3300 is not operated in conjunction with the 3300T (companion magnetic tape cassette unit), Line Feed steps the cursor down to the 25th line of the display, one line at a time. Upon reaching the bottom line, each succeeding Line Feed will perform the Roll Up function. When the Datapoint 3300 is operated with the Tape Cassette 3300T in the read reverse mode, the Line Feed steps the cursor up the screen to the first line, one line at a time. Each succeeding Line Feed rolls the information down. These two modes of operation are controlled by the reverse line which enters the Control Logic card on connector pin 15. When the Datapoint 3300 is not operating with the 3300T, the reverse line is grounded through the 50 pin Tape Cassette Unit connector on the back panel of the Datapoint 3300. This explanation will consider the Reverse line to always be at ground level. The Line Feed signal enters the Control Logic card on connector pin 27 and is normally a logic one state. The Line Feed signal connects to Z28 pin 10 and when pulsed, drives Z28 pin 8, Test Point 1, high. A pulse applied to Test Point 1 will generate a clock signal to the Cursor Character Counter.

The logic zero level of the reverse line is inverted by Z10 and applied to Z9 pin 3. Z9 pin 2 in connected to the inverted Line Feed pulse. The output, Z9 pin 1, is connected to the steer down line of the Cursor Character Counter. When Line Feed is pulsed, the steer down line of the Cursor Line Counter will be lowered and a clock pulse will be generated to increment the counter up, this will move the cursor down on the display. The clock pulse will be applied to Z1 pin 11. Z69 detects whether or not the cursor is on the 25th line. If the cursor is not on the 25th line, the output, Z69 pin 6, will be high and the clock pulse will be gated through Z1. This will increment the Cursor Line Counter by 1. If, however, the cursor is on the 25th line, Z69 pin 6 will be low and the clock will be inhibited. The output of Z69 is inverted by Z20 and gated by Z19 with a not reverse line. Z19 pin 8 goes low forcing Z19 pin 6 high. Z19 pin 6 is connected to Z7 pin 3. Z7 pin 5 is connected to the inverted line feed pulse. Z7 pin 4 is connected to Z33 pin 6 which is a clock pulse generated from Test Point 1. The clock pulse is gated through Z7 and inverted by Z10. The output, Z10 pin 8, is gated by Z9 with the not reverse line. The clock pulse is gated out of Z9 on pin 13 and applied to Z6 pin 10. By applying this pulse to Z6, the Roll Up function is initiated.

Roll Up

The function of rolling up information displayed on the CRT is performed by slipping sync between the vertical deflection and the MOS recirculating memory. The clock pulses to the Memory Character Counter are inhibited for a particular count while the MOS recirculating memory clock pulses are continued. This has the effect of holding the horizontal sweep in the same vertical position for two horizontal line times, while the information contained in the memory is advanced two line times.

The Roll Up signal enters the Control Logic card on connector pin 44 and is normally a logic high. This signal connects to Z6 pin 9. Z6 pin 10 is activated by the Line Feed function. If either of these input pins to Z6 is pulsed, the output, Z6 pin 8, is forced to a logic high. The signal is then gated by Z6 with the 82nd count of the Character Counter and the $\overline{\text{End of Frame}}$ signal. $\overline{\text{End of frame}}$ goes to a logic 1 at the beginning

of vertical retrace and gates count 82 through Z6. This forces the output, Z6 pin 6 low, setting a latch consisting fo Z5 pins 1, 2 and 3 and Z2 pins 8, 9, 10 and 11. One output of the latch, Z2 pin 8, is set to a logic 0 and gated by Z13 with the clock pulse for the line counter. This condition is maintained until the following count 82 of the Character Counter is gated through Z4 pin 8, which resets the latch circuitry. Since Z13 pin 3 was held at a logic 0 for a complete line time, the clock pulse to the Line Counter was inhibited and the Line Counter remained in the all zero state. Following vertical retrace, the recirculating memory clock is inhibited during the first horizontal sweep since this line position is not used for displaying data. The memory clocks are inhibited by wired OR gates Z66 pin 13. Z2 pin 8 however, holds Z66 pin 13 at a logic 1 during the Roll Up process thus allowing the memory clocks to continue. The recirculating memory then has advanced the information one line time while the Line Counter has remained in the same state for two counts. Information displayed on the first line of the CRT prior to the Roll Up command must be erased. This is accomplished on the MOS board by the load 0's 1 pulse which leaves the Control Logic card on connector pin 58. This signal is the inversion of Z2 pin 8, by Z13 pin 10.

Roll Advance

Roll Advance enters the Control Logic card on connector pin 31. This signal is used as a Roll Up command when the cursor is located on the 72nd character of the 25th line. Roll Advance is gated by Z1 with two control lines to detect that the 72nd character of the 25th line has been written. The Roll Advance pulse is gated through Z11 and applied to Z6 pin 12. This initiates the Roll Up function.

Roll Down

The Roll Down key switch closure enters the Control Logic card on connector pin 10. The switch bounce is filtered out by R19 and C2 before the signal is gated through Z18. Z18 pin 13 is wire ORed with Z9 pin 10 (a function of the line feed signal on the Datapoint 3300 when it is operated with the 3300T). These signals connect to Z2 pin 3, a three input gate connected in a latch configuration with Z11 pins 8, 9 and 10. Z2 pin 3 going low, forces Z2 pin 6 to a logic one. This signal is gated by Z4 with count 76 from the Character Counter and the End of Frame signal. End of Frame is high except during the time of vertical retrace and therefore allows count 76 to be gated through Z4 at any time except vertical retrace. The output of Z4 pin 6 sets a latch consisting of Z3 pins 1, 2 and 3 and Z1 pins 3, 4, 5 and 6. One output of the latch, Z3 pin 3, is inverted by Z13 and wired with Z13 pin 1 which is the clock pulse for the line counter. The second latch consisting of Z3 pins 8, 9 and 10 and Z3 pins 4, 5 and 6 is set on count 82 and resets Z13 pin 13 to a high. The remaining latch circuitry is reset on the following count 72 of the Character Counter. By adding an additional clock pulse to the Line Counter, sync is momentarily lost while the vertical sweep moves one full line time ahead of the recirculating memory. When Z4 pin 6 went low, following count 76, a latch consisting of Z80 pins 8, 9 and 10 and Z80 pins 4, 5 and 6 was set. Z80 pin 8 leaves the Control Logic card on connector pin 25 and is referred to as the Blank CRT2 signal. This signal is initiated at the beginning of the Roll Down function and is used to blank the CRT during the Roll Down process. Z80 pin 8 is gated with count 72 and Z39 pin 12 by Z79, Z39 pin 12 goes high at the beginning of the second horizontal sweep (first horizontal sweep display). This gates Z79 pin 8 low, setting a latch consisting of Z80 pins 1, 2 and 3 and Z70 pins 1, 2 and 3. The output of this latch, Z70 pin 3, leaves the Control Logic card on connector pin 23 and is referred to as the Load 0's 2 signal. This signal is used to erase information in the recirculating memory that has been positioned on the bottom line prior to the Roll Down signal. The latch circuitry is reset on count 72 by Z80 pin 11.

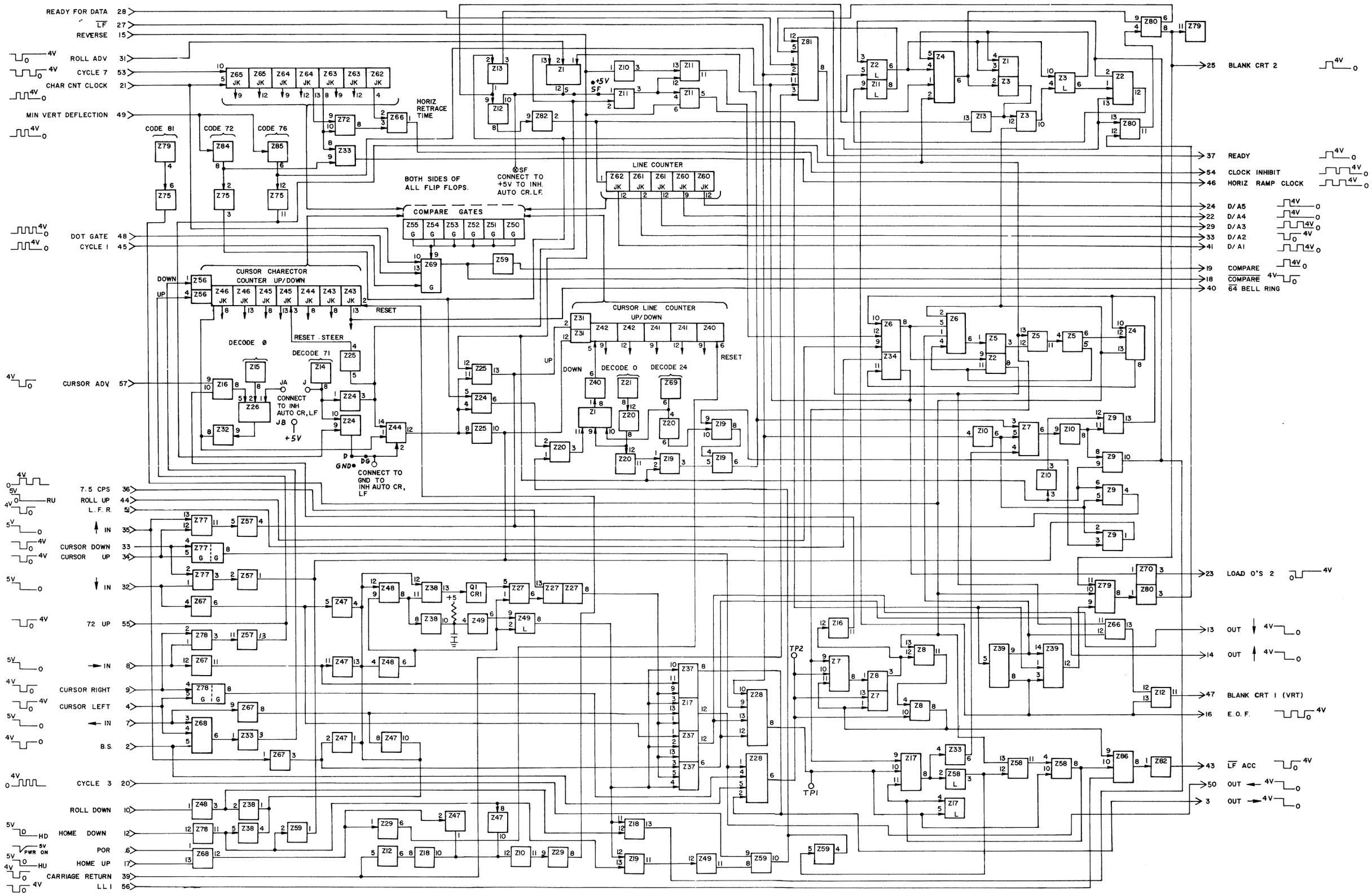
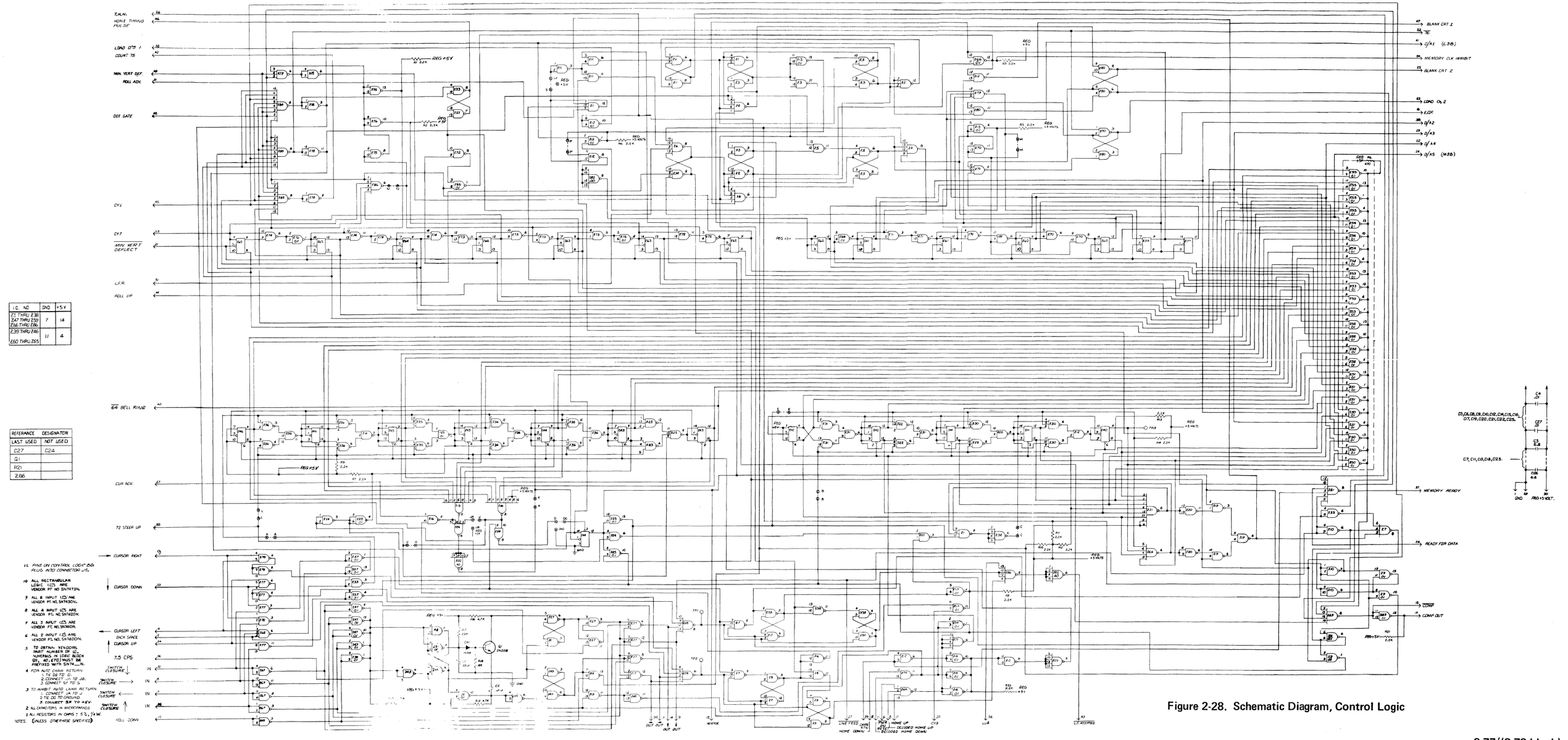


Figure 2-27. Block Diagram, Control Logic



I.C. NO	GND	+5 V
Z1 THRU Z38	7	14
Z47 THRU Z59		
Z66 THRU Z86		
Z39 THRU Z46	11	4
Z60 THRU Z65		

REFERANCE DESIGNATOR	
LAST USED	NOT USED
Q27	Q24
Q1	
R121	
Z86	

NOTES. (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS IN OHMS ± 5%, ¼W.
2. ALL CAPACITORS IN MICROFARADS.
3. TO INHIBIT AUTO LAMP RETURN:
   1. CONNECT JA TO J.
   2. TIE DC TO GROUND.
   3. CONNECT SW TO +8V.
4. FOR AUTO CARR. RETURN:
   1. TIE DB TO D.
   2. CONNECT JA TO JB.
   3. CONNECT SW TO S.
5. TO OBTAIN VENDORS PART NUMBER OF IC, NUMERALS IN LOGIC BLOCK (Q1, 40, ETC) MUST BE PREFIXED WITH SN74....N.
6. ALL 2 INPUT LCS ARE VENDOR PT. NO. SN7400N.
7. ALL 3 INPUT LCS ARE VENDOR PT. NO. SN7410N.
8. ALL 4 INPUT LCS ARE VENDOR PT. NO. SN7420N.
9. ALL 8 INPUT LCS ARE VENDOR PT. NO. SN7430N.
10. ALL RECTANGULAR LOGIC LCTS ARE VENDOR PT NO SN7473N.
11. PINS ON CONTROL LOGIC BD. PLUG INTO CONNECTOR J-5.

Figure 2-28. Schematic Diagram, Control Logic

MAINTENANCE

SECTION III

General

Become familiar with the various functions and data flow through the Datapoint 3300 by referring to Section II of this manual and the Operators Manual provided with the equipment. To gain access to the equipment for maintenance, it is necessary to remove the housing from the base plate and if any of the printed circuit cards require replacement, it will be necessary to remove the keyboard from the terminal base plate.

WARNING

With the housing removed and power on, 15,000 volts is present at the CRT.

REMOVAL

Housing Removal From Base

The terminal housing is secured to the base plate by 3 Allen head screws. One is located on each side of the base plate, 3-1/2 inches from the rear and the third is located in the front center of the base plate. A 5/32 inch Allen wrench is required to remove these screws. After removing the screws, lift the housing (not including the back panel) straight up until it is clear of the unit and the back panel. This will provide access to the keyboard and the printed circuit cards without removing the back panel.

If it is necessary to remove the back panel, proceed as follows:

1. Remove the two Phillips head screws securing the Data Set connector and unplug the connector.

2. Remove the two Phillips head screws securing the Recorder Model 3300T connector and unplug the connector.

3. Disconnect the AC Power cord from the 115 VAC 60 Hz connector.

4. Remove the fuse holder cap and fuse.

NOTE

Turn Baud Rate Switch knob to a point where the index mark points straight down. This places the switch in the null position for ease in re-indexing and also makes the knob set screw easily accessible.

5. Using a 1/16 inch Allen wrench, loosen the set screw in the knob on the Baud Rate Switch and remove the knob.

Tilt the back panel toward the rear and lift the panel off the base plate.

NOTE

Before operating with the cover removed, the fuse and cap, Baud Rate Switch knob, 3300T connector and AC power cord must be replaced. The null position of the Baud Rate Switch will display a cursor however no data can be displayed.

Keyboard Removal From Terminal

The Keyboard must be removed from the terminal in order to remove any of the other printed circuit cards. The Keyboard is held in place by four Phillips screws located on the bottom of the terminal base plate, two on each end of the Keyboard. The screw holes through the terminal base plate are slotted to facilitate forward and backward adjustment of the keyboard. Once the mounting screws are removed, unplug the main connector on the right hand side of the keyboard, and lift the keyboard out.

Keyswitch Disassembly

Remove the Keyboard assembly from the terminal baseplate. The keyswitch is secured to the printed circuit card by two spring tabs on the keyswitch housing and a 6-32 nut. Remove the nut with a 3/16 inch socket wrench. Insert a 1/16 inch diameter piece of piano wire through the holes in the plungers. Use special keycap removing tool to remove the keycap. Pull straight up to avoid damage to the keycap.

Remove the spring and keyswitch gasket. Two pairs of needle nose pliers are required to remove the keyswitch housing. Compress the two spring tabs on the sides of the housing with one pair of needle nose pliers and use the other pair to grasp the plunger, and pull up. Remove the magnet assembly retainer for access to the magnet and focusing plates. When replacing the magnet, the north pole (positive) must be at the top. Reassemble in the reverse order. Make sure that the plunger gasket is installed, or faulty operation of the switch will result. When replacing the keycap, push it straight down onto the plunger. Do not rock it or the keycap can be damaged. Remove the 1/16 inch rod from the plungers. Replace the 6/32 inch nut.

Reed Replacement

To replace a defective reed, remove the keyswitch and break the reed lead where it is soldered to the reed bracket. Unsolder the lower lead from the Keyboard printed circuit board. Cut 0.5 inch off the contact side of the reed lead. Position the reed on the reed support so that the flat side of the reed is 90 degrees to the flat side of the reed bracket. The top of the contact lead must be flush with the top of the reed bracket. Hold the reed in position with an alligator clip and solder the bottom lead to the keyboard printed circuit board. Remove alligator clip and solder top lead to reed support. Replace keyswitch assembly.

Printed Circuit Card Removal

After the keyboard has been removed, the other five printed circuit cards may be removed by pulling the card straight forward out of it's connector. The cards when viewed from the front, starting from the top, are:

Deflection Amplifier Card
Interface 1 Card
Interface 2 Card
MOS Card
Control Logic Card

Logic Power Supply Removal

The Logic Power Supply is secured to the terminal by five Phillips head screws. If it is necessary to gain access to the Logic Power Supply for trouble-shooting or repair, remove the two Phillips head screws on the bottom of the terminal base plate (on the right hand side about half-way toward the rear of the plate). Remove the two Phillips head screws that secure the Logic Power Supply bracket to the right hand side of the CRT bracket. Remove the one Phillips head screw that secures the Logic Power Supply bracket to the back bracket. Using caution to avoid breaking or shorting together any of the connecting wires; lift the Logic Power Supply and bracket to clear the terminal base plate and move it out to the right hand side of the terminal.

NOTE

If power is to be turned on for trouble-shooting, check first to ensure that no wires were broken or shorted together in moving the power supply out.

High Voltage Power Supply Removal

CAUTION

Before attempting to remove the High Voltage Power Supply, ensure that the post accelerator has been discharged by shorting the post accelerator connection to ground. The post accelerator connector is located under the rubber cap on the right rear of the CRT. Use extreme caution in grounding this connection since a 15,000 volt potential may be present.

After the post accelerator has been discharged, disconnect the spring clip connector (under the rubber cap) from the side of the CRT. Disconnect the two input leads on the side of the High Voltage Power Supply. Loosen the screw on top of the power supply enough to permit removal of the spade lug on the CRT ground wire.

Support the power supply while removing the four Phillips head screws that secure the High Voltage Power Supply to the rear panel. Lift the power supply out of the terminal.

CRT Removal

Disconnect the octal plug on the rear panel near the left side. Disconnect the socket on the rear of the CRT

CAUTION

Discharge the post accelerator and disconnect the high voltage lead to the post accelerator connection. Remove the ground spring across the back of the CRT. Support the CRT and deflection yoke while removing the four Phillips head screws that secure the CRT faceplate to the CRT brackets. Lift out the CRT and deflection yoke.

Figures 3-1 through 3-4 show views of the Datapoint 3300 with the housing removed.

Figure 3-5 shows the Logic and Deflection Power Supply cards moved out to the side to provide access to the cards for trouble shooting.

Assembly drawings are provided to facilitate locating components during trouble shooting.

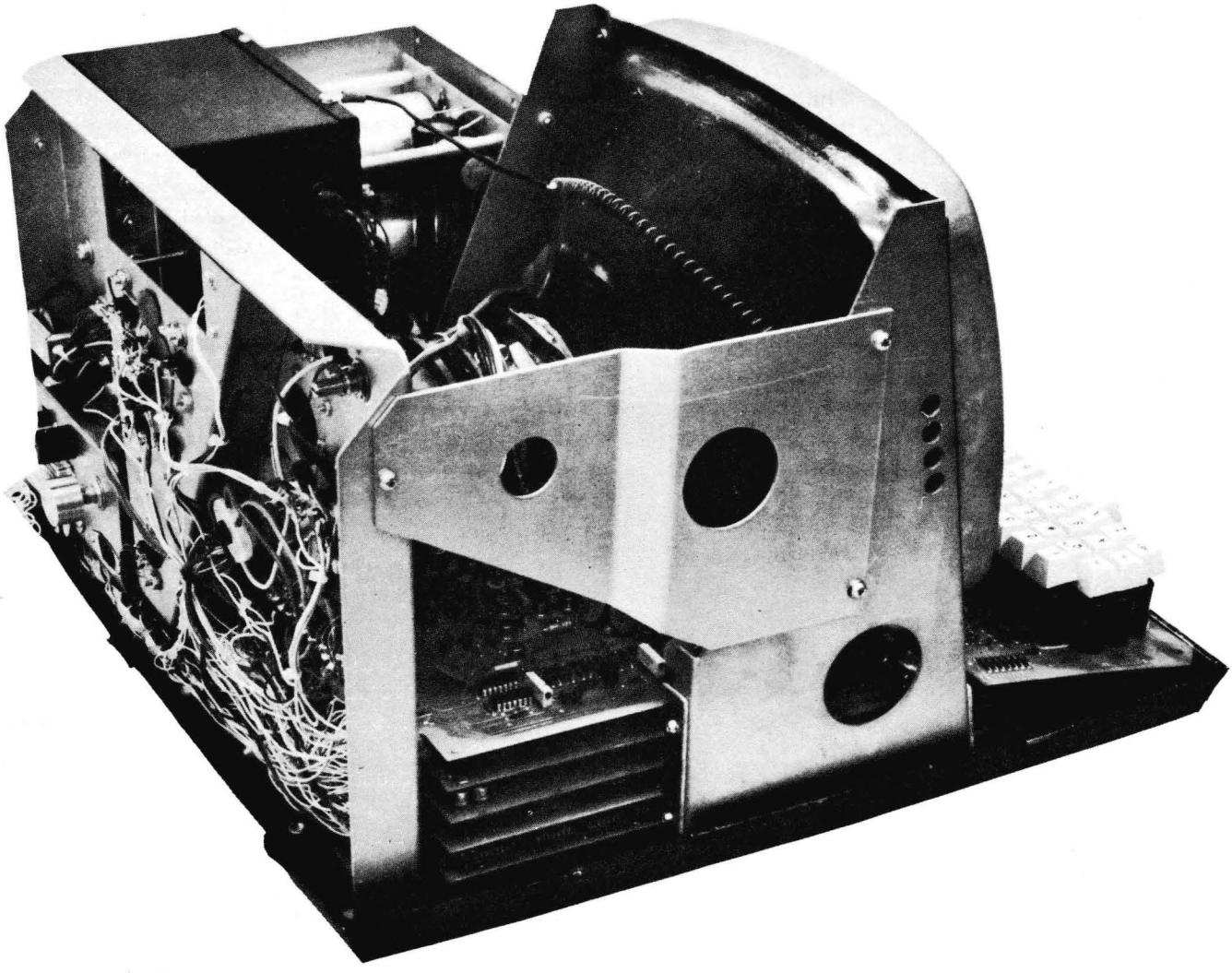


Figure 3-1. Datapoint 3300 with Cover Removed

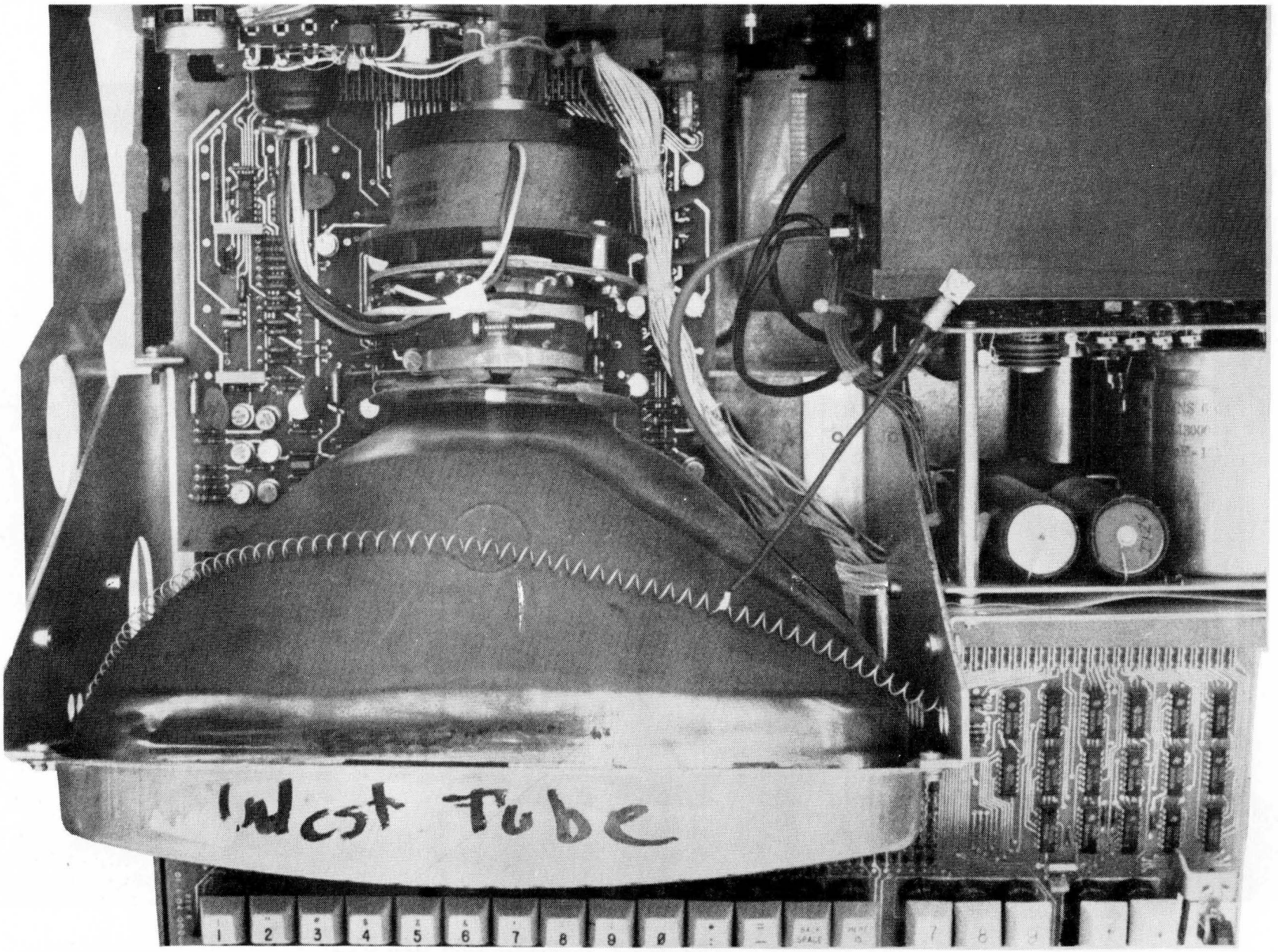


Figure 3-2. Datapoint 3300, Top View

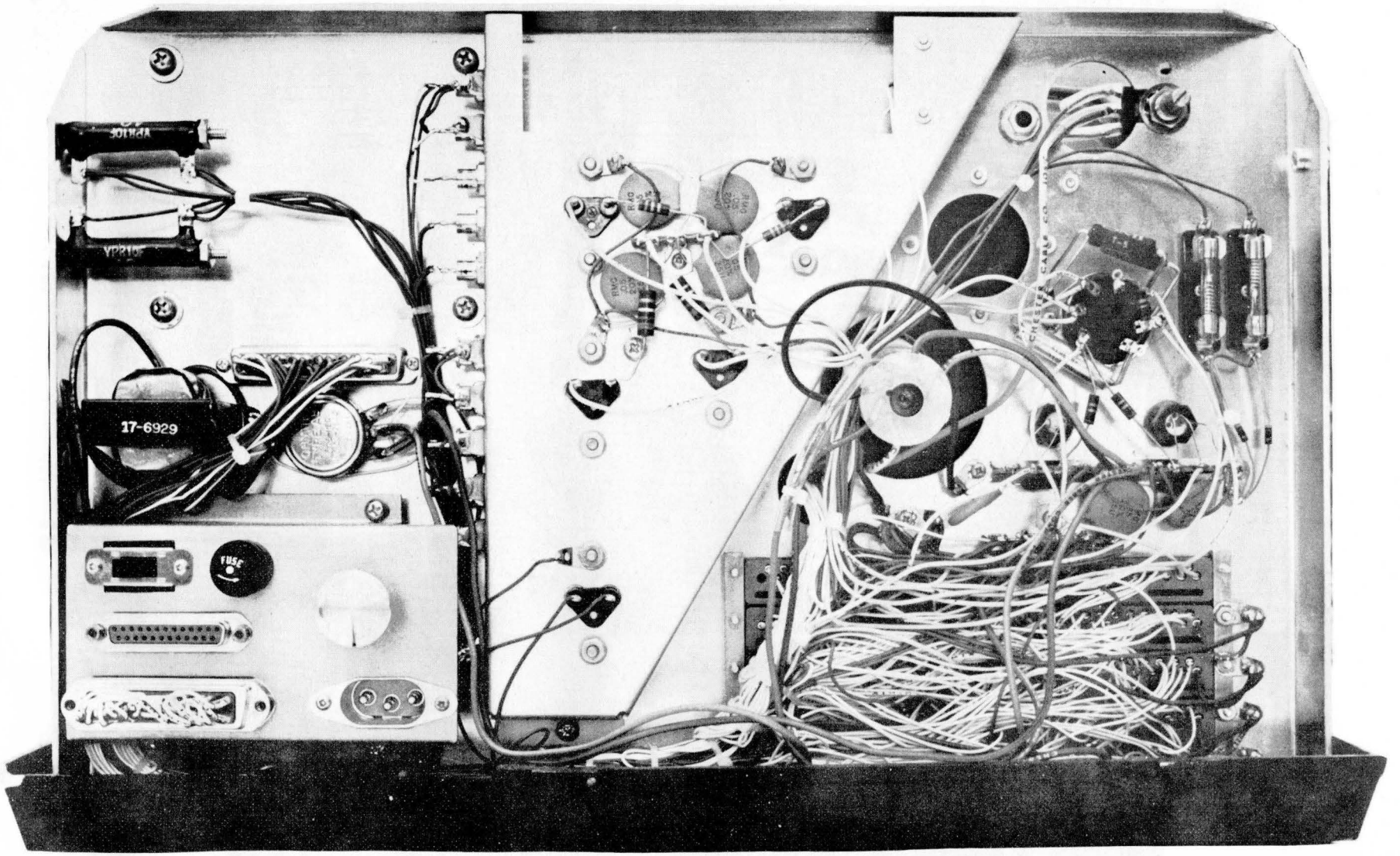


Figure 3-3. Datapoint 3300, Rear View

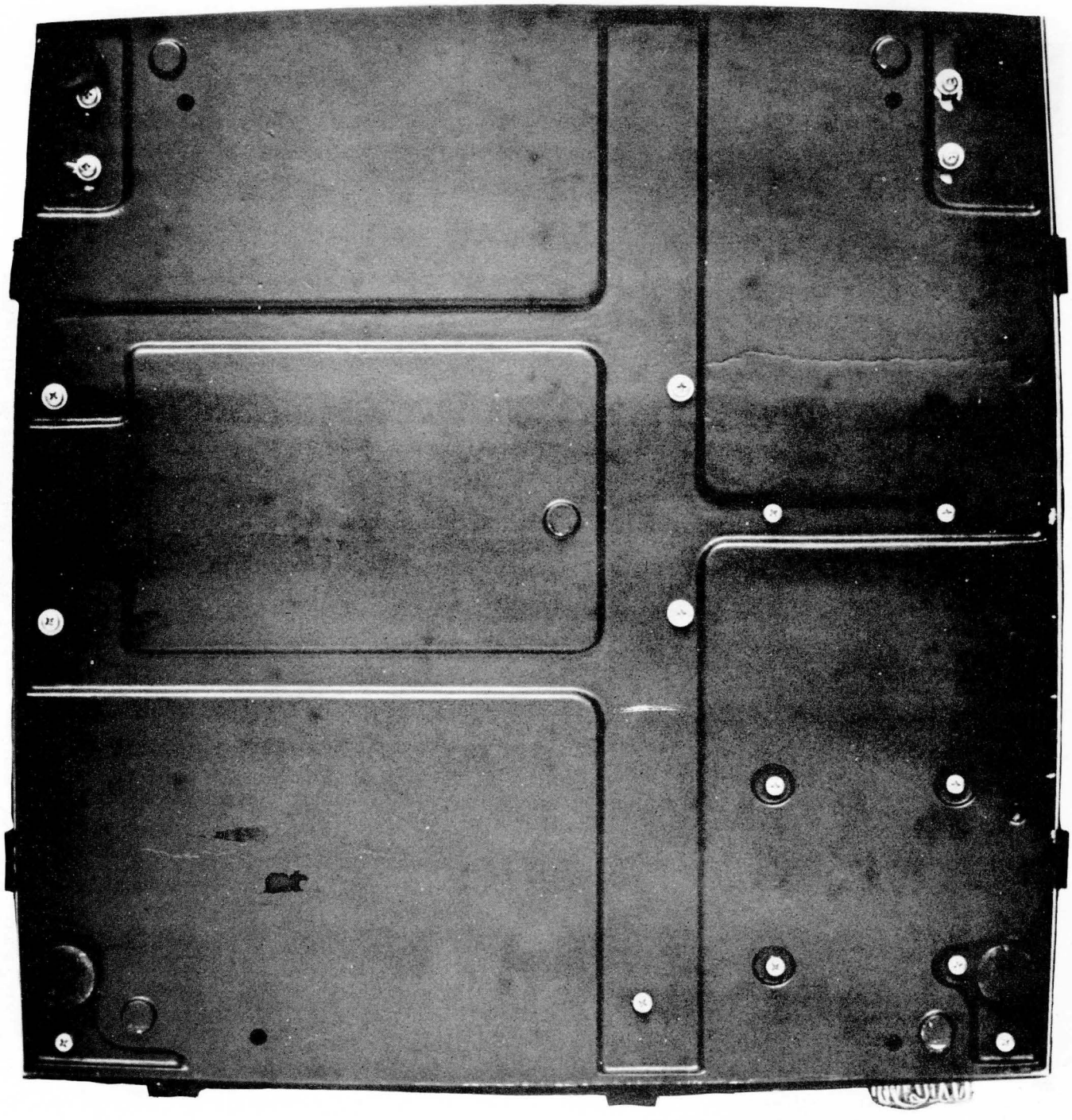


Figure 3-4. Datapoint 3300, Bottom Panel

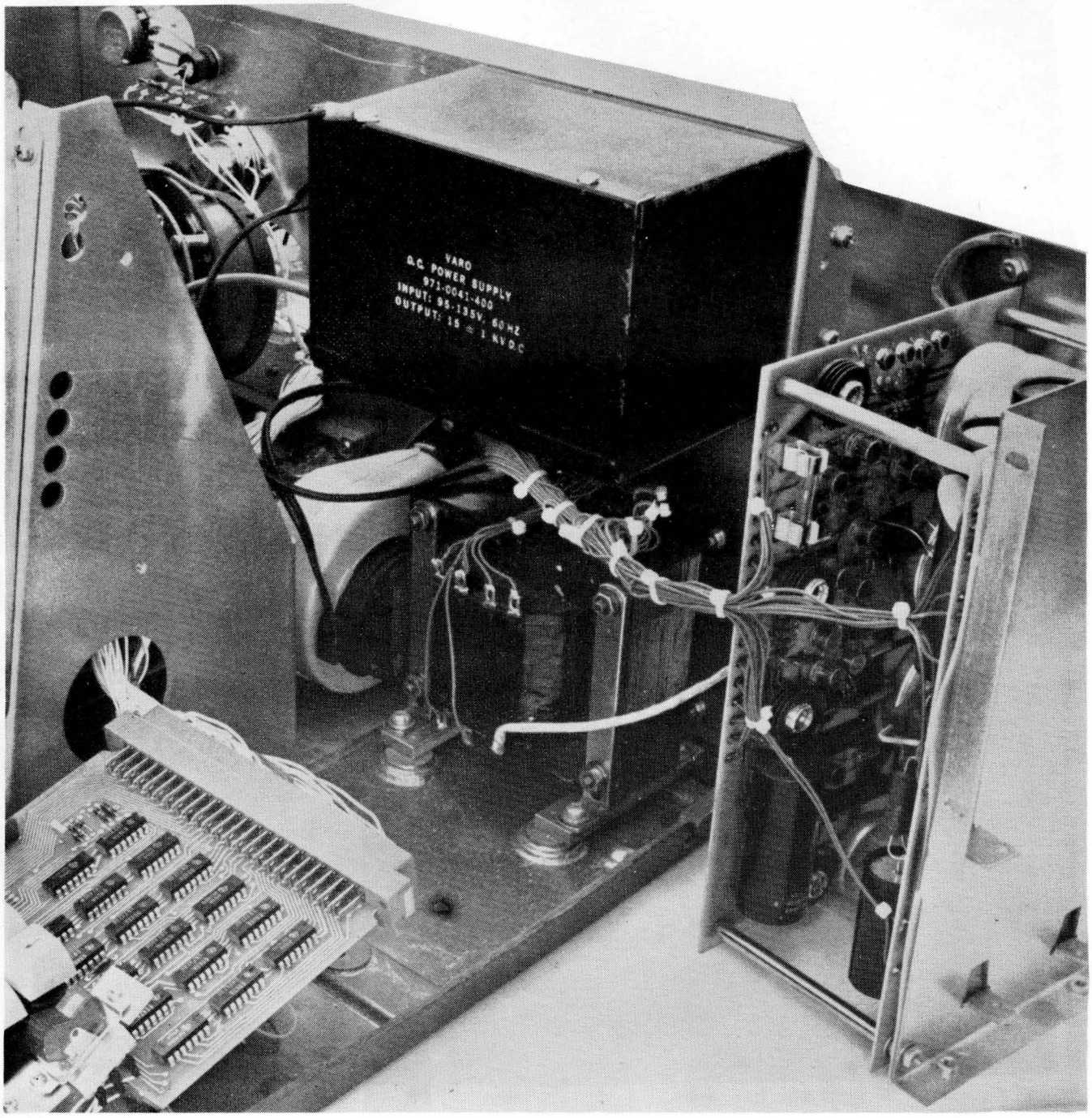


Figure 3-5. Logic and Deflection Power Supplies

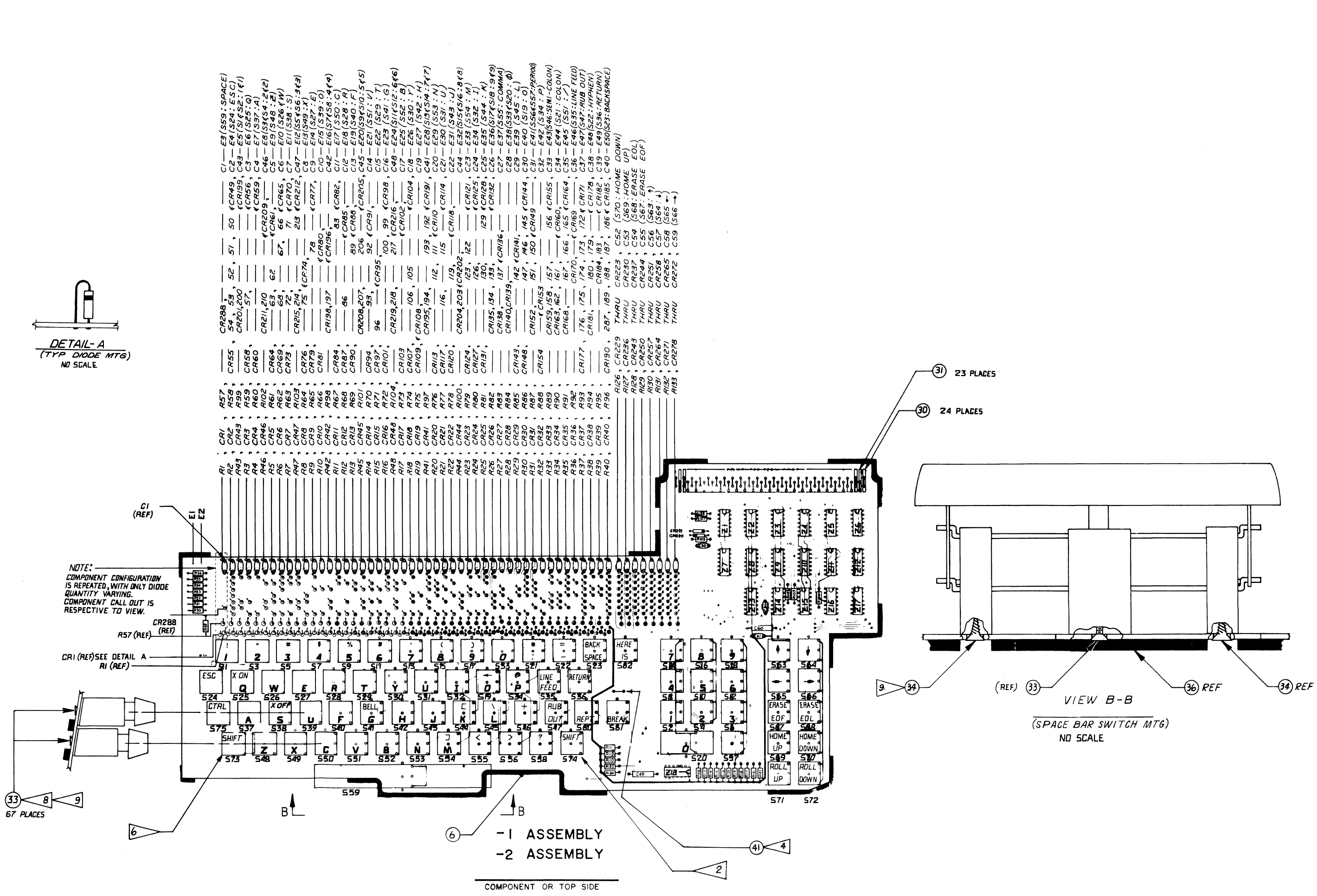


Figure 3-6. Keyboard Assembly (NAVCOR)

-2	-1	CTC PART NO	NOMENCLATURE	VENDOR PART NO	VENDOR	REF DES	ITEM
23	23	000-024-41	CONTACT, UPPER TIER	60-7001-05-13	ELCO		31
24	24	000-025-41	CONTACT, LOWER TIER	60-7001-15-13	ELCO		30
1	1	000-021-71	INTEGRATED CIRCUIT	SN7412IN	T.I.		29
1	1	000-011-71	INTEGRATED CIRCUIT	SN7420N	T.I.		28
5	5	000-006-71	↑	SN7474N	↑		27
1	1	000-007-71		SN7473N			26
1	1	000-009-71		SN7440N			25
1	1	000-010-71		SN7430N			24
1	1	000-014-71	↓	SN7401N	↓		23
7	7	000-015-71	INTEGRATED CIRCUIT	SN7400N	T.I.		22
							21
279	279	000-008-70	DIODE	IN914	T.I.		20
1	1		CAPACITOR, TANTALUM - 10 uF, 20 VOLT	T110B106M020AS	KERMET		19
1	1		CAPACITOR, CERAMIC - 470 uuF, 600 V	DD471G	CENTRAL LAB		18
1	1		↑ TANTALUM - 6.8 uF, 35 V	T110B685M035AS	KERMET		17
48	56		↓ CERAMIC - .1 uF, 10 V	UK10-104	CENTRAL LAB		16
2	2		CAPACITOR, CERAMIC - .01 uF, 50 V	UK50-103	CENTRAL LAB		15
1	1	000-004-65	RESISTOR, CARBON COMP - 27K 1/4W 5%	RC07GF273J	AB		14
8	8	000-001-65	RESISTOR, CARBON COMP-10K OHM, 1/4W, 5%	RC07GF103J	AB		13
56	56	000-021-65	↑ 4.7K OHM, 1/4 W, 5%	RC07GF472J	↑		12
			↓		↓		11
69	69	000-030-65	RESISTOR, CARBON COMP-1K OHM, 1/4W, 5%	RC07GF102J	AB		10
75	75		REED ASSEMBLY				9
							8
							7
1	1	000-046-59	PRINTED-WIRING BOARD	01-1-02-0017-1	ENGINEERING		6
							5
							4
							3
X		000-036-10	BOARD ASSEMBLY, KEYBOARD	01-1-03-0017-2	ENGINEERING		2
	X	000-035-10	BOARD ASSEMBLY, KEYBOARD	01-1-03-0017-1	ENGINEERING		1

CODED KEY OPTIONS

STANDARD KEYBOARD CODING SHOWN

BACKSPACE

BIT	REMOVALS STANDARD	REMOVALS OPTIONAL
1	CR 185	CR 185
2	CR 186	CR 186
3	CR 187	CR 187
4	CR 188	CR 188
5	CR 189	CR 189
6	~~CR 227~~	CR 237
7	CR 190	CR 190

CURSOR KEYS

STANDARD BIT	CODE	HO	HU	ERASE EOL	ERASE EOF	↑	↓	←	→
1	1	CR 223	CR 230	CR 237	CR 244	CR 251	CR 258	CR 265	CR 272
2	1	CR 224	CR 231	CR 238	CR 245	CR 252	CR 259	CR 266	CR 273
3	1	CR 225	CR 232	CR 239	CR 246	CR 253	CR 260	CR 267	CR 274
4	1	CR 226	CR 233	CR 240	CR 247	CR 254	CR 261	CR 268	CR 275
5	1	CR 227	CR 234	CR 241	CR 248	CR 255	CR 262	CR 269	CR 276
6	1	CR 228	CR 235	CR 242	CR 249	CR 256	CR 263	CR 270	CR 277
7	1	CR 229	CR 236	CR 243	CR 250	CR 257	CR 264	CR 271	CR 278

ESCAPE

BIT	REMOVALS STANDARD	REMOVALS OPTIONAL
1	CR 49	CR 49
2	CR 50	CR 50
3	~~CR 51~~	CR 51
4	CR 52	CR 52
5	CR 53	CR 53
6	~~CR 54~~	CR 54
7	~~CR 55~~	CR 55

NOTE: ALL DIODE REMOVALS WILL BE MARKED WITH AN "X". AN "X" IN A PARTICULAR BIT POSITION INDICATES A ZERO.

CODING

STANDARD: WILL BE SPECIFIED BY MARKETING AND WILL BE CODED PRIOR TO INSTALLATION INTO DATAPOINT 3300

OPTIONAL: WILL BE SUPPLIED BY MARKETING AND WILL BE CODED PRIOR TO INSTALLATION INTO DATAPOINT 3300.

REF DESIGNATOR	ITEM
R1 THRU R49, R105, R108 THRU R124, R134, R135	10
R57 THRU R104, R126 THRU R133	12
R50 THRU R56, R107	13
R106	14
C50 C61	15
C1 THRU C48 C52 THRU C59	16
C60	17
C51	18
C49	19
CR1 THRU CR221 CR223 THRU CR278, CR287, CR288	20
Z1,2,4,6,8,10,7	22
Z15	23
Z13	24
Z14	25
Z16	26
Z3,5,9,11,12	27
Z17	28
Z18	29

5. AFTER ASSEMBLY IS COMPLETE, STAMP ASSEMBLY PART NO., REVISION LEVEL, AND SERIAL NO. ON TOP SIDE. CHARACTERS ARE TO BE .12 INCH HIGH, GOTHIC STYLE, COLOR BLACK. THE ASSEMBLY NO. SHALL BE PREFIXED WITH "ASSY".
4. TO BUILD A -2 CONFIGURATION, DELETE C52 THRU C59 AND MASK AREA USED BY C52 THRU C59 PRIOR TO WAVE SOLDERING.
3. FOR SCHEMATIC DIAGRAM, REFER TO DRAWING 01-1-01-0006.
2. REFERENCE DESIGNATIONS SHOWN MAY OR MAY NOT APPEAR ON ASSY.
1. EQUIVALENT VENDORS' PARTS MAY BE UTILIZED WITH COMPUTER TERMINAL CORP ENGINEERING APPROVAL.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 3-7. Keyboard Assembly (1 of 2)

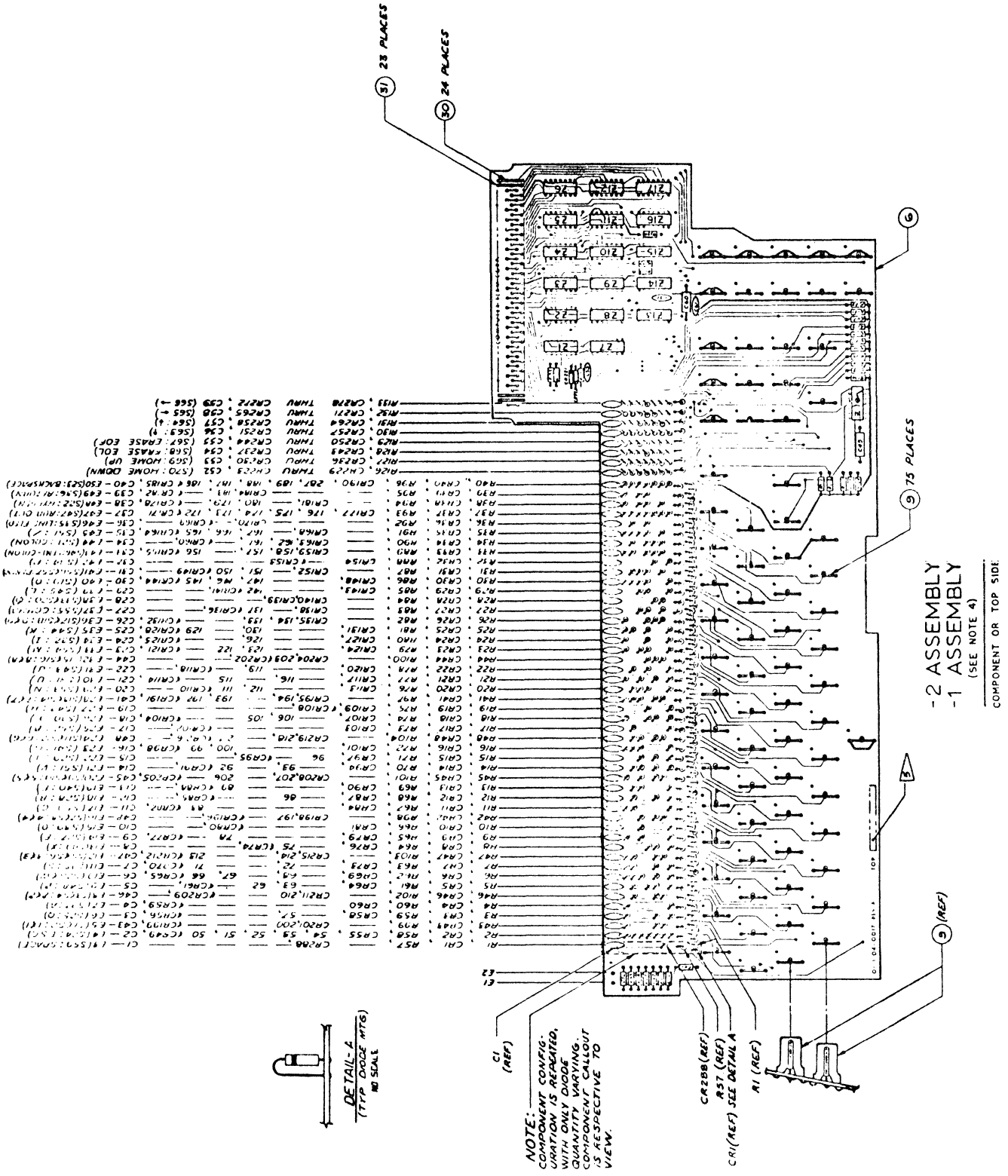
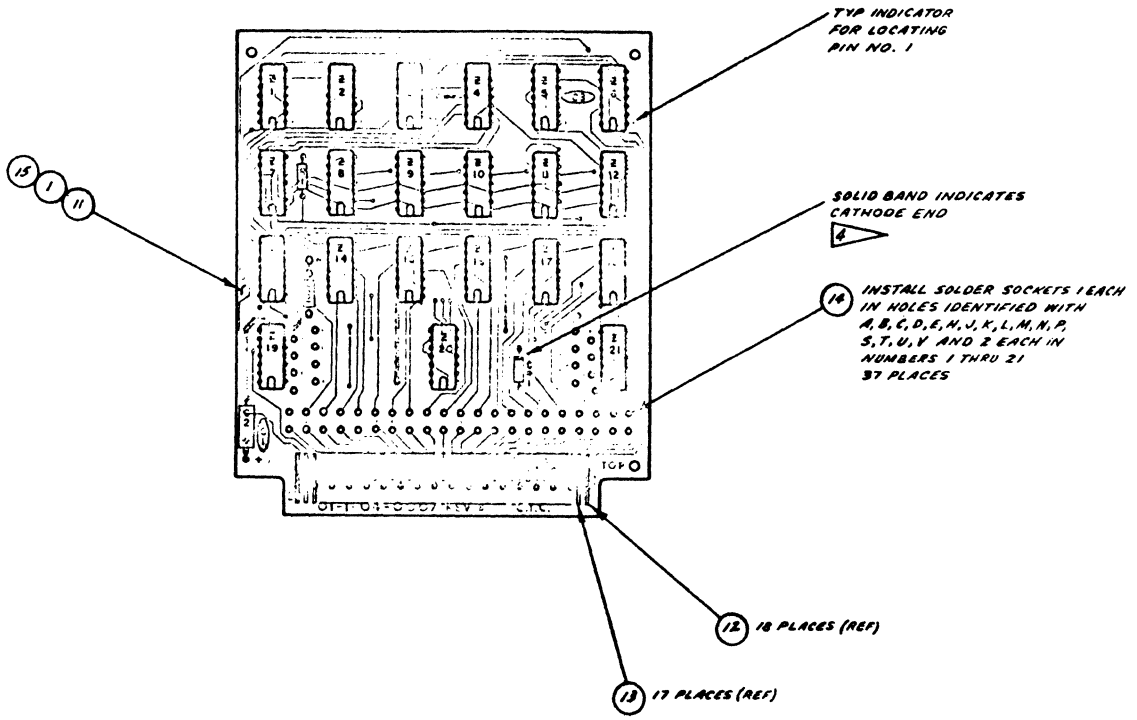


Figure 3-7. Keyboard Assembly (2 of 2)

ASSEMBLY
COMPONENT OR TOP SIDE

REF DESIGNATOR	ITEM
C1	18
C2	19
C3	20
CR1	22
R1, R2	24
Z1, 6	26
Z2, 5	27
Z3, 4	28
Z7-12	29
Z13	30
Z19, 21	31
Z14-18, 20	32



4 THE CATHODE END OF ALL DIODES IS INDICATED BY EITHER A COLOR BAND, A DOT, OR THE END FROM WHICH THE BANDS ORIGINATE.

3. AFTER ASSEMBLY IS COMPLETE, STAMP ASSEMBLY PART NUMBER, REVISION LEVEL AND SERIAL NUMBER ON BOTTOM SIDE. CHARACTERS ARE TO BE 1/16 INCH HIGH AND COLOR WHITE. THE ASSEMBLY NUMBER SHALL BE PREFIXED WITH "ASSY".

2. EQUIVALENT VENDORS PARTS MAY BE UTILIZED WITH COMPUTER TERMINAL CORP. ENGINEERING APPROVAL.

1. FOR SCHEMATIC DIAGRAM REFER TO DRAWING 01-1-01-0007.

NOTES: (UNLESS OTHERWISE SPECIFIED)

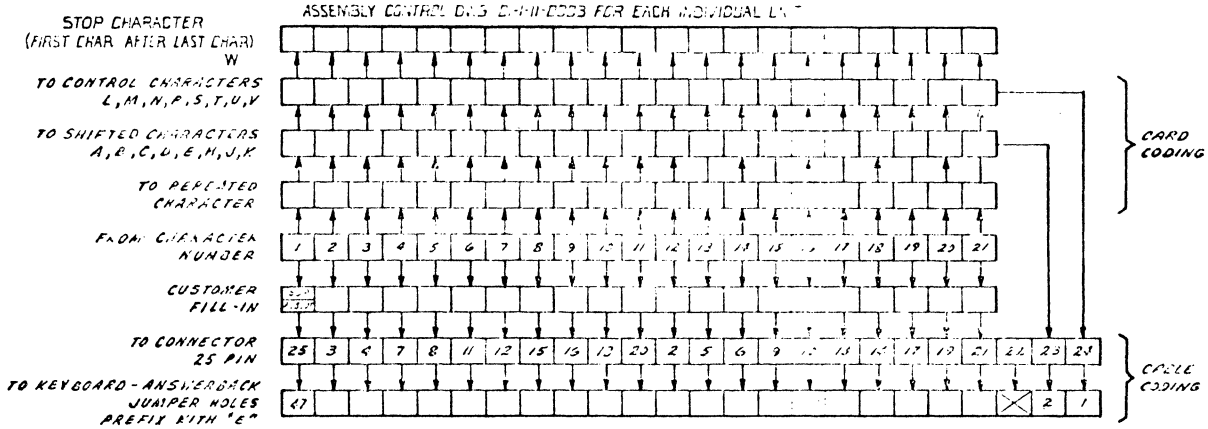
Figure 3-8. Answer-Back Assembly (1 of 2)

6	000-014-71	INTEGRATED CIRCUIT-QUADRUPLE 2-INPUT NAND	SN7400N	T.I.		32
2	000-010-71	-8 INPUT POS NAND	SN7430N			31
1	000-012-71	-TRIPLE 3-INPUT POS NAND	SN7410N			30
6	000-006-71	-DUAL D EDGE TRIG F-F	SN7474N			29
2	000-007-71	-DUAL J-K F-F	SN7473N			28
2	000-009-71	-DUAL 4-INPUT NAND BUF	SN7440N			27
2	000-015-71	INTEGRATED CIRC. QUADRUPLE 2-INPUT NAND	SN7400N	T.I.		26
						25
2	000-031-05	RESISTOR-CARBON COMP, 1K OHMS, 1/2W, ±5%	RC07GF10	A.B.		24
						23
1	000-008-70	DIODE	IN914	T.I.		22
						21
1	000-084-25	CAPACITOR-CERAMIC, 470 PF, 1 KV	D0471G	CENTRALAB		20
1	000-011-35	CAPACITOR-TANTALUM, 6.8 UF, 35 V	T110B685M035AS	KEMET		19
1	000-012-35	CAPACITOR-MICA, .1 UF, 10 V	UK10-104	CENTRALAB		18
						17
A/R		WIRE-26 AWG, SOLID COPPER, TINNED				16
1		ASSEMBLY CONTROL DRAWING	01-1-11-0003	MARKETING		15
58	000-020-42	SOCKET-SPRING	6330808-0	AMP		14
17	000-024-41	CONTACT-UPPER TIER	60-7001-05-13	ELCO		13
18	000-025-41	CONTACT-LOWER TIER	60-7001-15-13	ELCO		12
1	000-016-50	PRINTED WIRING BOARD (ASY B)	01-1-02-0007-1	ENGINEERING		11
						10
						9
						8
						7
						6
						5
						4
						3
						2
X	000-002-10	ASSEMBLY-ANSWERBACK	01-1-03-0007-1	ENGINEERING		1
-1	DTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	REF DES	

ANSWERBACK CODING TABLE

SHOWN FOR REFERENCE ONLY

FOR VARIATION IN ANSWER BACK JUMPER INSTALLATION REFER TO ASSEMBLY CONTROL DWG 01-1-11-0003 FOR EACH INDIVIDUAL UNIT



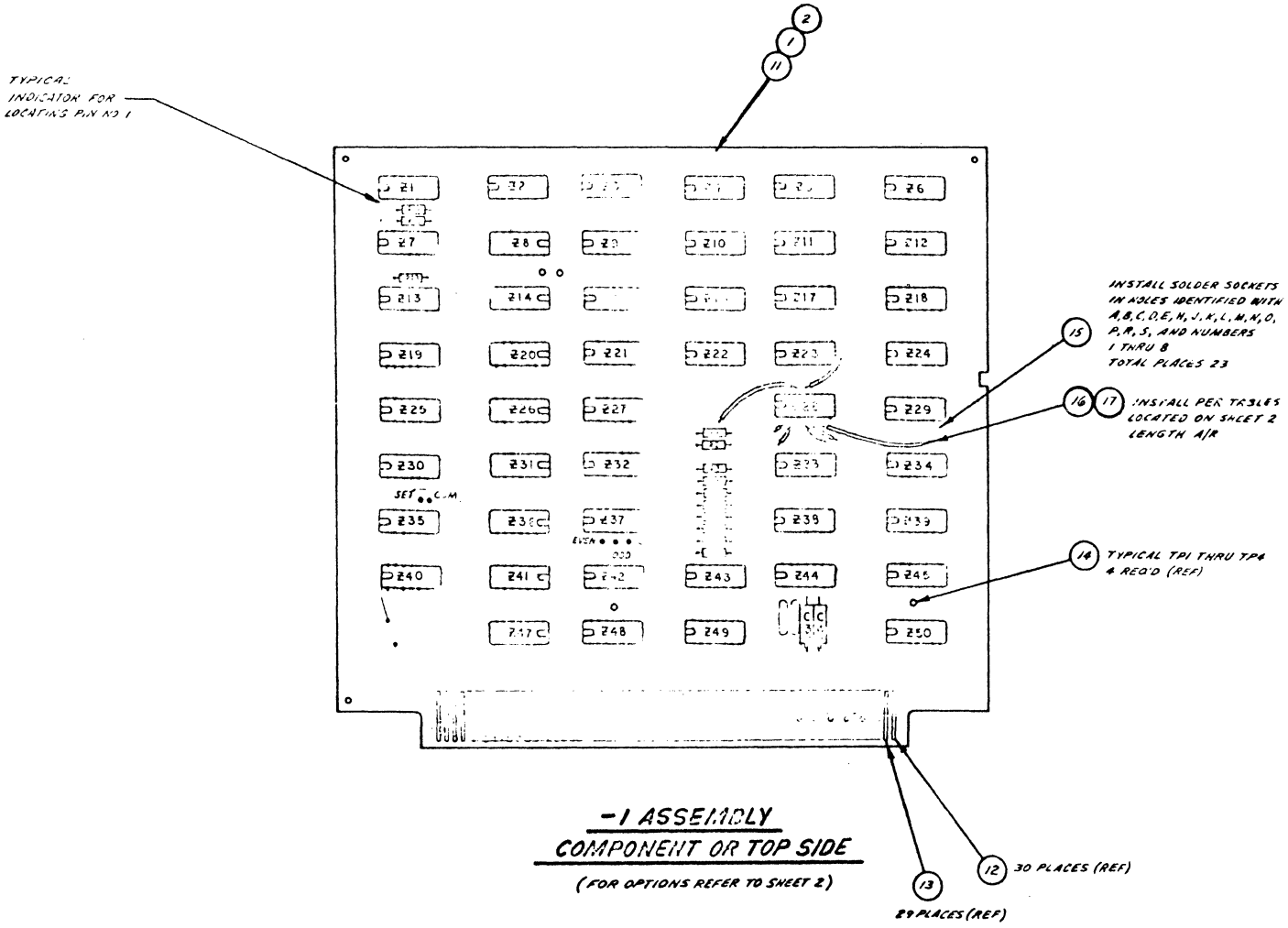
KEYTOPS FUNCTION	SOCKETS PREFILLED WITH "E"
CTRL	1
SHIFT	2
1 !	5
2 "	8
3 #	12
4 $	16
5 %	33
6 &	24
7 '	28
8 (	32
9)	36
β	38
A	7
B	25
C	17
D	15

KEYTOPS FUNCTION	SOCKETS PREFILLED WITH "E"
E	14
F	19
G BELL	23
H	27
I	34
J	31
K [	35
L \	39
M]	33
N ↑	29
O ←	43
P @	42
Q ↓ON	6
R	18
S ↓OFF	11
T	22

KEYTOPS FUNCTION	SOCKETS PREFILLED WITH "E"
U	30
V	21
W	10
X	13
Y	26
Z	9
: X	44
- =	48
SP	3
; +	43
LF	46
RTN	49
AUX OUT	47
) <	37
. >	41
/ ?	45

Figure 3-8. Answer-Back Assembly (2 of 2)

REF DESIGNATOR	ITEM
C1, 2	20
C3, 4	19
R1-10	23
R11-13	24
R14-21	25
Z3, 13, 20, 25, 30, 35, 44, 45	27
Z7, 19, 43, 49	28
Z40	29
Z39	30
Z4-6, 10-12, 15-18, 22-26, 33, 29, 33, 34, 38	31
Z1, 2, 9, 14	32
Z26, 31, 36, 41, 47	33
Z15, 21, 27, 32, 37, 42, 48, 53, 8	34



3. [illegible] ASSEMBLY IS COMPLETED, SERIAL ASSEMBLY PART NUMBER, REVISION LEVEL, AND SERIAL NUMBER ON BOTTOM SIDE. CHARACTERS ARE TO BE 1/16 INCH HIGH, GOTHIC STYLE, COLOR WHITE. THE ASSEMBLY NUMBER SHALL BE PREFIXED WITH "ASSY".
2. FOR SCHEMATIC DIAGRAM REFER TO DRAWING 01 1-01-0005.
1. EQUIVALENT VENDORS PARTS MAY BE UTILIZED WITH COMPUTER TERMINAL CORP. ENGINEERING APPROVAL.

NOTES: (UNLESS OTHERWISE SPECIFIED)

Figure 3-9. Interface 1 Assembly (1 of 2

-2 QTY	-1 QTY	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	USED ON	ITEM NO.
9	9		INTEGRATED CIRCUIT - DUAL D FLIP-FLOP	SN7474N	T.I.		27
5	5		-DUAL J-K FLIP-FLOP	SN7473N			26
4	4		-DUAL 4 INPUT NAND	SN7420N			25
9	17		-8 INPUT NAND	SN7430N			24
1	1		-TRIPLE 3 INPUT NAND	SN7410N			23
1	1		-QUAD UPLE 2 INPUT NOR	SN7402N			22
4	4		-QUAD UPLE 2 INPUT NAND	SN7400N			21
8	8		INTEGRATED CIRCUIT - QUAD 2 INPUT NAND	SN7400N	T.I.		20
							19
8	—		RESISTOR - CARBON COMP, 1.0K OHMS, 1/4W, 5%	RCR07G102J	A.B.		18
3	3		RESISTOR - CARBON COMP, 22K OHMS, 1/4W, 5%	RCR07G223J	A.B.		17
10	10		RESISTOR - CARBON COMP, 6.2K OHMS, 1/4W, 5%	RCR07G622J	A.B.		16
							15
							14
2	2		CAPACITOR - CERAMIC, 0.1 UF, 10 V	UK10-104	CENTRALAB		13
2	2		CAPACITOR - TANTALUM, 6.8 UF, 35 V	T110B685M035AS	KEMET		12
							11
A/R	A/R		SLEEVING - 26 AWG, THIN WALL, TEFLON				10
A/R	A/R		JUMPER - 26 AWG BUSS, COPPER, TINNED				9
23	23		SOCKET - SPRING	48-330803-0	AMP		8
4	4		TERMINAL - SOLDER	1004-2	C.T.C.		7
29	29		CONTACT - UPPER TIER	60-1001-05-13	ELCO		6
30	30		CONTACT - LOWER TIER	60-1001-15-13	ELCO		5
1	1		PRINTED WIRING BOARD	01-1-02-0005-1	ENGINEERING		4
1	1		ASSEMBLY CONTROL DRAWING	01-1-11-0001	MARKETING		3
							2
X	—		ASSEMBLY - INTERFACE LOGIC NO. 1	01-1-03-0005-2	ENGINEERING		1
—	X		ASSEMBLY - INTERFACE LOGIC NO. 1	01-1-03-0005-1	ENGINEERING		

PARTS LIST

DASH NO.	DESCRIPTION	DELETIONS	ADDITIONS
-1	ALLOWS REMOTE CURSOR CONTROL (RECEIVE) AS SHOWN SHEET 1	—	—
-2	REMOVES REMOTE CURSOR CONTROL CAPABILITY (RECEIVE)	INTEGRATED CIRCUITS: 211, 12, 16, 17, 18, 22, 23 AND 24	INSTALL A 1K OHM, 1/4W, ±5%, CARBON COMP RESISTOR IN THE SPACE WHERE EACH INTEGRATED CIRCUIT HAS BEEN REMOVED. INSERT ONE END OF THE RESISTOR IN PIN NO. 14 AND THE OTHER INTO PIN NO. 8 (ITEM NO. 25). HAND FORM THE LEADS

OPTION TABLE

BACKSPACE STANDARD

SHIFT "0"

INSTALL JUMPERS	
FROM SOCKET	TO SOCKET
A	1
C	2
J	4
E	5
S	6
L	7
O	8

INSTRUCTIONS:
LIST THE REQUIRED BACKSPACE CODE IN BINARY IN THE COLUMN BELOW.
START THE COLUMN WITH BIT 1, THE LEAST SISNIFICANT BIT, AT THE TOP.

MANUFACTURING USE ONLY
REF DWG NO. 01-1-03-0005
TITLE: INTERFACE LOGIC NO. 1

FROM SOCKET	TO THIS SOCKET IF THE CODE AT THE RIGHT IS A "1"	TO THIS SOCKET IF THE CODE AT THE RIGHT IS A "0"	BACKSPACE CODE
1	A	B	____ LSB
2	C	D	____
4	E	H	____
8	J	K	____
6	L	M	____
7	N	S	____
8	O	P	____ MSB

REMARKS:

SHOWN FOR REFERENCE ONLY

FOR VARIATIONS IN BACKSPACE JUMPER INSTALLATION REFER TO ASSEMBLY CONTROL DRAWING 01-1-11-0001 FOR EACH INDIVIDUAL UNIT.

Figure 3-9. Interface 1 Assembly (2 of 2

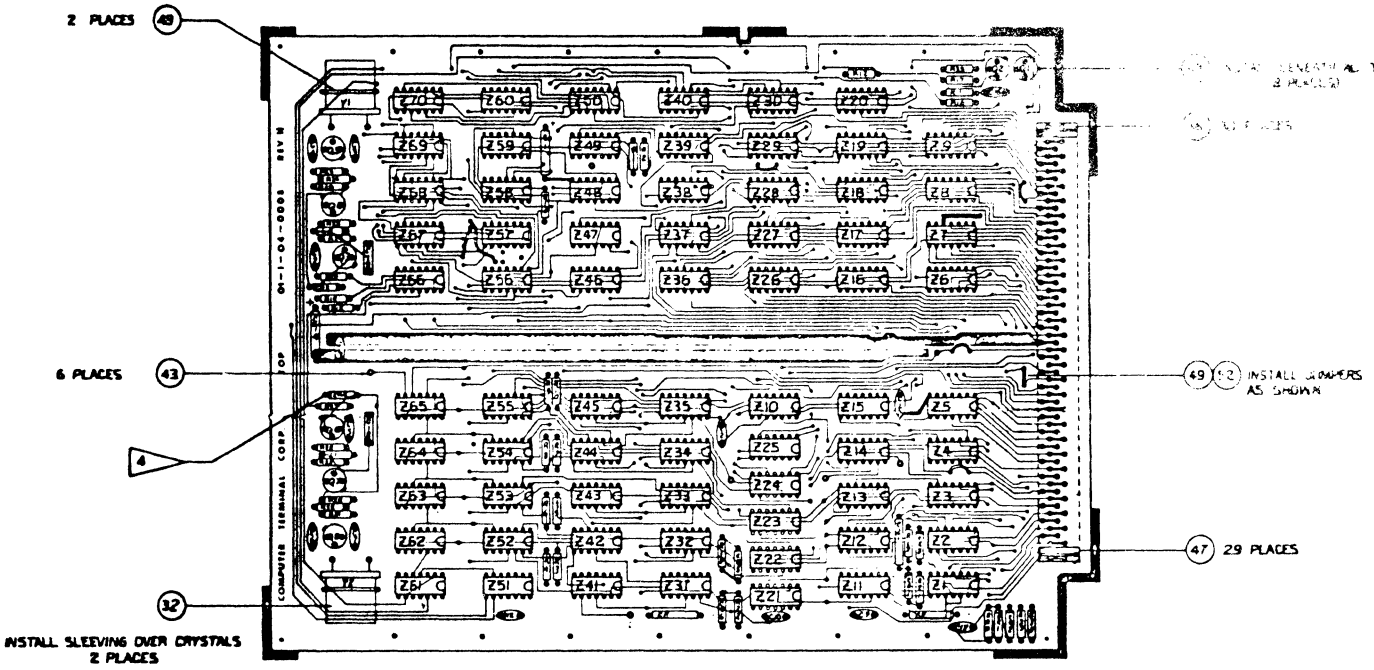
-4	-3	-2	-1	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	REF DES	ITEM
6	6	6	6	000-009-71	INTEGRATED CIRCUIT	SN7440N	TEXAS INST		42
3	3	3	3	000-005-71		SN7493N			41
8	-	-	8	000-018-71		SN7491N			40
23	13	13	23	000-006-71		SN7474N			39
2	2	2	2	000-007-71		SN7473N			38
1	1	3	3	000-010-71		SN7430N			37
4	4	4	4	000-012-71		SN7410N			36
3	2	2	3	000-013-71		SN7402N			35
6	1	1	6	000-014-71		SN7401N			34
12	9	9	12	000-015-71	INTEGRATED CIRCUIT	SN7400N	TEXAS INST		33
A/R	A/R	A/R	A/R	000-005-90	SLEEVING, VINYL, 1/2 IN DIA				32
8	8	8	8	000-001-73	TRANSISTOR	2N2218			31
2	2	2	2	000-005-56	INDUCTOR, 120 uh, ± 10%	9230-70	MILLER		30
8	8	8	8	000-008-70	DIODE	IN914			29
1	1	1	1	000-040-35	CAPACITOR, MICA, 3900 PF, 100V	DM19-392J	ELMENCO		28
2	2	2	2	000-076-35	, MICA , 51 PF, 100V	DM15-510J	ELMENCO		27
3	3	3	3	000-084-35	, CERAMIC, 470 PF, 1 KV	DD471G	CENTRALAB		26
1	1	1	1	000-075-35	, MICA , 43 PF, 100V	DM15-430J	ELMENCO		25
5	3	3	5	000-011-35	, .6.8 uf, 35V	T110B685M035AS	KEMET		24
4	4	4	4	000-012-35	, .1uf, 10V	UK10-104	CENTRALAB		23
2	2	2	2	000-090-35	, CERAMIC, .005 uf, 50V	CK502	CENTRALAB		22
2	2	2	2	000-021-35	, CERAMIC, .01 uf, 50V	UK50-103	CENTRALAB		21
1	1	1	1	000-026-35	CAPACITOR, MICA, 2200PF, 100V	DM19-222J	ELMENCO		20
1	1	1	1	000-008-65	RESISTOR, CARBON, 22K OHM, 1/4W ±5%	RC07GF223J	ALLEN BRADLEY		19
3	3	3	3	000-021-65	, 4.7K	472J			18
2	2	2	2	000-011-65	, 220	221J			17
2	2	2	2	000-009-65	, 1.8K	182J			16
2	2	2	2	000-031-65	, 1.2K	122J			15
4	4	4	4	000-033-65	, 6.8K	682J			14
									13
3	3	3	3	000-028-65	, 2.7K	272J			12
1	1	1	1	000-048-65	, 270	271J			11
2	2	2	2	000-001-65	, 10K	103J			10
1	1	1	1	000-029-65	, 2.2K	222J			9
13	5	4	12	000-030-65	, 1K	102J			8
4	2	2	4	000-014-65	RESISTOR, CARBON, 470 Ω, 1/4 W, ±5%	RC07GF471J	ALLEN BRADLEY		7
									6
									5
/	-	-	-	000-009-10	ASSY, INTERFACE LOGIC NO. 2				4
-	/	-	-	000-018-10	ASSY,				3
-	-	/	-	000-019-10	ASSY,				2
-	-	-	/	000-020-10	ASSY, INTERFACE LOGIC NO. 2				1

PARTS LIST

-4	-3	-2	-1	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	REF DES	ITEM
A/R	A/R	A/R	A/R	000-001-90	SLEEVING, TEFLON				52
1	1	1	1	000-017-59	PRINTED WIRING BOARD	01-1-02-0023-1	CTC ENGRG		51
-	20	20	-	000-020-42	SOCKET, SPRING	6-330808-2	AMP		50
A/R	A/R	A/R	A/R		WIRE, 26 AWG BUS, COPPER TINNED				49
8	8	8	8	000-015-42	TRANSIPAD, NYLON, GREEN	7717-16	THERMALLOY		48
29	29	29	29	000-024-41	CONTACT, UPPER TIER	60-7001-55-13	ELCO		47
30	30	30	30	000-025-41	CONTACT, LOWER TIER	60-7001-15-?	ELCO		46
1	1	1	1	000-007-46	CRYSTAL , 307.200 KHZ				45
1	1	1	1	000-008-46	CRYSTAL , 225.280 KHZ				44
6	6	6	6	000-019-42	TERMINAL, SOLDER	1604-2	CAMBION		43

PARTS LIST

Figure 3-10. Interface 2 Assembly (1 of 5)



-1 ASSEMBLY

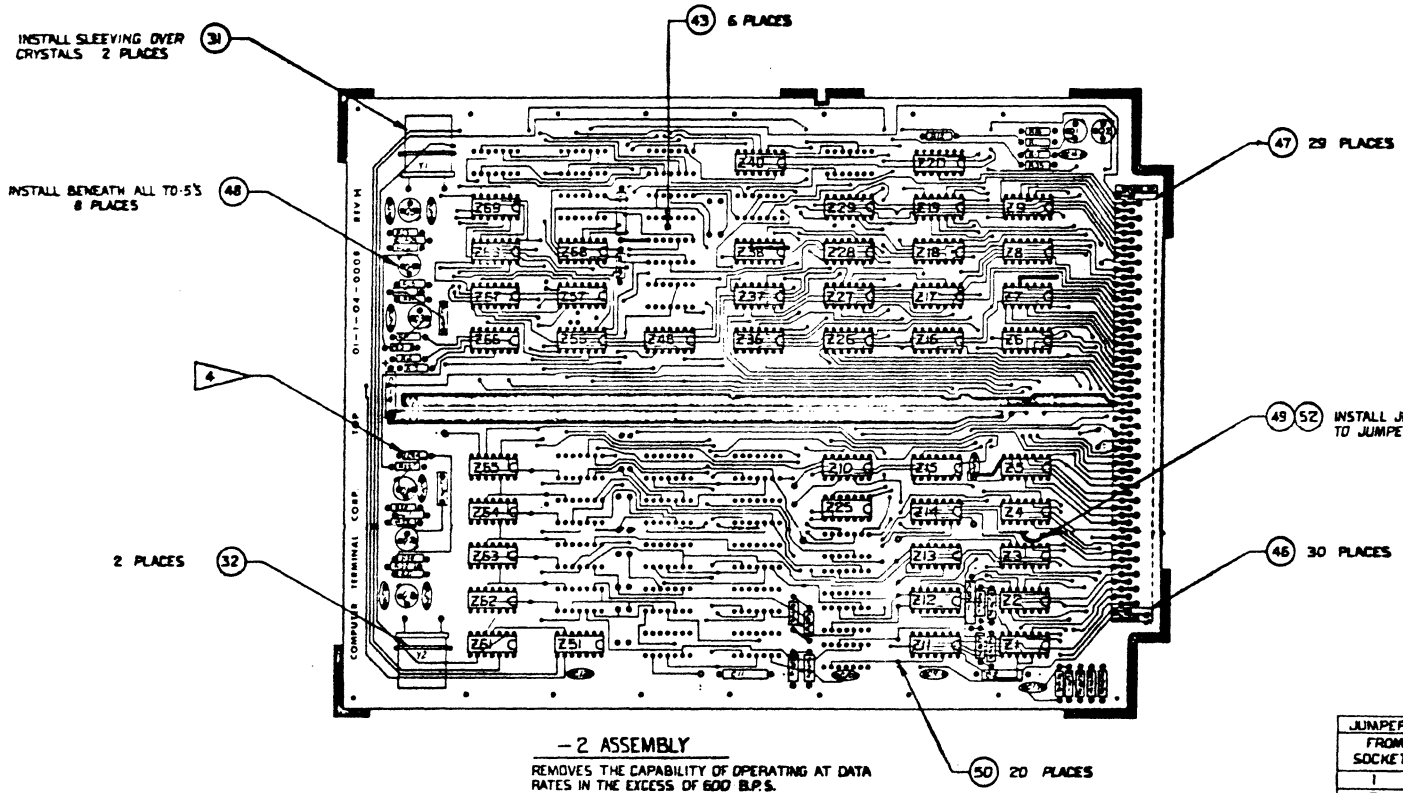
1. ALLOWS OPERATION AT DATA RATES UP TO 2400 BPS.
2. ALLOWS PRESETTING AND CLEARING OF THE SPACE BAR-OVERWRITE FEATURE.

4. CATHODE END OF ALL DIODES IS INDICATED BY EITHER A COLOR BAND, A DOT, OR THE END FROM WHICH THE BANDS ORIGINATE.
3. AFTER ASSEMBLY, STAMP ASSEMBLY PART NO., REVISION LEVEL, AND SERIAL NO ON BOTTOM SIDE. CHARECTORS ARE TO BE 1/16 HIGH (MIN) GOTHIC STYLE, COLOR BLACK, PREFIX ASSEMBLY NO. WITH "ASSY."
2. FOR -1, REFER TO SCHEMATIC DIAGRAM 01-1-01-0008.
1. EQUIVALENT VENDORS PARTS MAY BE USED WITH COMPUTER TERMINAL CORP ENGINEERING APPROVAL.

NOTES UNLESS OTHERWISE SPECIFIED

REF DESIGNATOR	ITEM
R1 R2 R23 R31	7
R3 THRU R10 R12 R14 R15 AND R35	8
R11	9
R16 R38	10
R17	11
R19 R27 R39	12
R20 R21 R22 R28	14
R24 R32	15
R25 R33	16
R26 R34	17
R13 R29 R30	18
R40	19
C18	20
C2 C5	21
C3 C6	22
C9 C10 C12 C13	23
C1 C8 C11 C14 C21	24
C17	25
C15 C16 C20	26
C4 C7	27
C19	28
CR1 THRU CR8	29
Q1 THRU Q8	31
Z2 Z39 Z57	35
Z1 Z5 Z8 Z17 Z19 Z29 Z36 Z44 Z42 Z50 Z56 Z58	33
Z48 Z52 THRU Z55 Z66	34
Z26 Z27 Z40 Z67	36
Z5 Z3 Z4	37
Z68 Z69	38
Z9 THRU Z14 Z20 THRU Z24 Z28 Z30 Z47 Z48 Z59 Z60 THRU Z65 Z70	39
Z31 THRU Z35 Z41 Z43 Z45	40
Z7 Z16 Z38	41
Z15 Z18 Z25 Z37 Z46 Z51	42
TP1 THRU TP6	43
Y1	44
Y2	45
L1 L2	30

Figure 3-10. Interface 2 Assembly (2 of 5)



-2 ASSEMBLY

REMOVES THE CAPABILITY OF OPERATING AT DATA RATES IN THE EXCESS OF 600 B.P.S.

ALLOWS PRESETTING AND CLEARING OF THE SPACE BAR-OVERWRITE FEATURE.

JUMPER WIRE TABLE	
FROM SOCKET	TO SOCKET
1	8
2	9
3	10
4	11
5	12
6	13
7	14
15	19
16	20
17	18

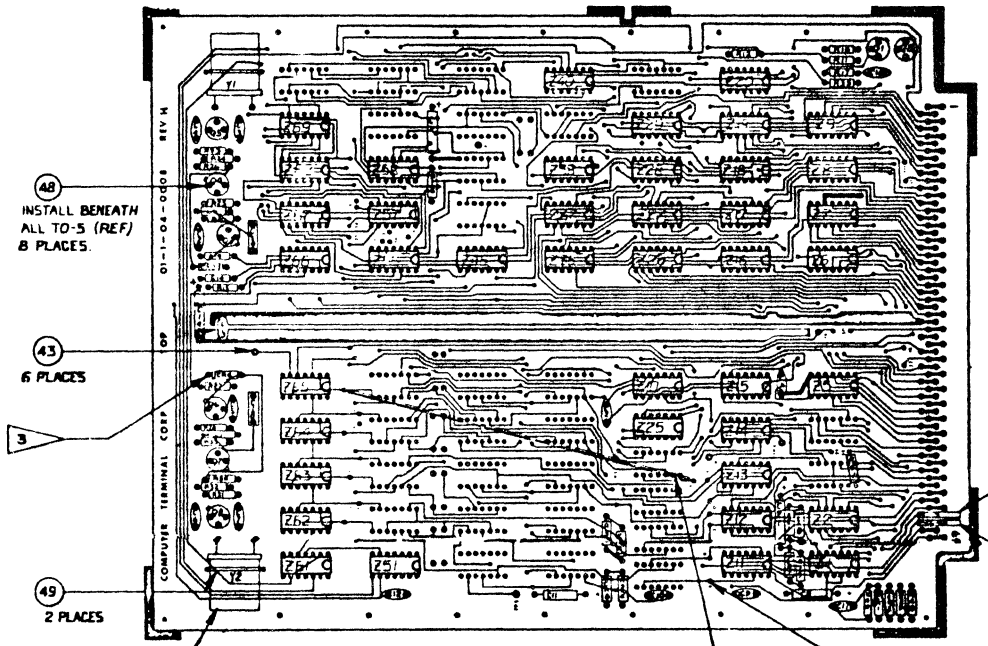
REF DESIGNATOR	ITEM
R23 R31	7
R12 R14 R15 R35	8
R11	9
R16 R38	10
R17	11
R5 R27 R39	12
R20 R21 R22 R28	14
R24 R32	15
R25 R33	16
R26 R34	17
R13 R29 R30	18
R40	19
C18	20
C2 C5	21
C3 C6	22
C9 C10 C12 C13	23
C1 C8 C11 C14 C21	24
C17	25
C15 C16 C20	26
C4 C7	27
C19	28
CR1 THRU CR8	29
Q1 THRU Q8	31
Z1 Z6 Z8 Z17 Z19 Z29 Z36 Z56 Z58	33
Z66	34
Z2 Z57	35
Z28 Z27 Z40 Z67	36
Z3 Z4 Z5	37
Z68 Z69	38
Z9 THRU Z14 Z20 Z28 Z61 THRU Z65	39
Z7 Z16 Z38	41
Z15 Z18 Z25 Z37 Z46 Z51	42
TP1 THRU TP6	43
Y1	44
Y2	45
U1 U2	30
1 THRU 20	50

4 CATHODE END OF ALL DIODES IS INDICATED BY EITHER A COLOR BAND, A DOT, OR THE END FROM WHICH THE BANDS ORIGINATE.

3. AFTER ASSEMBLY, STAMP ASSEMBLY PART NO., REVISION LEVEL, AND SERIAL NO ON BOTTOM SIDE. CHARACTORS ARE TO BE 1/16 HIGH (MIN), GOTHIC STYLE, COLOR BLACK. PREFIX ASSEMBLY NO WITH "ASSY"
2. FOR -2 REFER TO SCHEMATIC DIAGRAM 01-1-01-0013.
1. EQUIVALENT VENDORS PARTS MAY BE USED WITH COMPUTER TERMINAL CORP ENGINEERING APPROVAL.

NOTES UNLESS OTHERWISE SPECIFIED

Figure 3-10. Interface 2 Assembly (3 of 5)



JUMPER WIRE TABLE	
FROM SOCKET	TO SOCKET
1	8
2	9
3	10
4	11
5	12
6	13
7	14
15	19
16	20
17	18
22	23
24	25
26	27

—3 ASSEMBLY—

1. REMOVES THE CAPABILITY OF OPERATING AT DATA RATES IN THE EXCESS OF 600 B.P.S.
2. REMOVES THE CAPABILITY TO PRESET AND CLEAR THE SPACE BAR-OVERWRITE FEATURE.

FOR _3 REFER TO SCHEMATIC DIAGRAM 01-1-01-0013.

3 CATHODE END OF ALL DIODES IS INDICATED BY EITHER A COLOR BAND, A DOT, OR THE END FROM WHICH THE BANDS ORIGINATE.

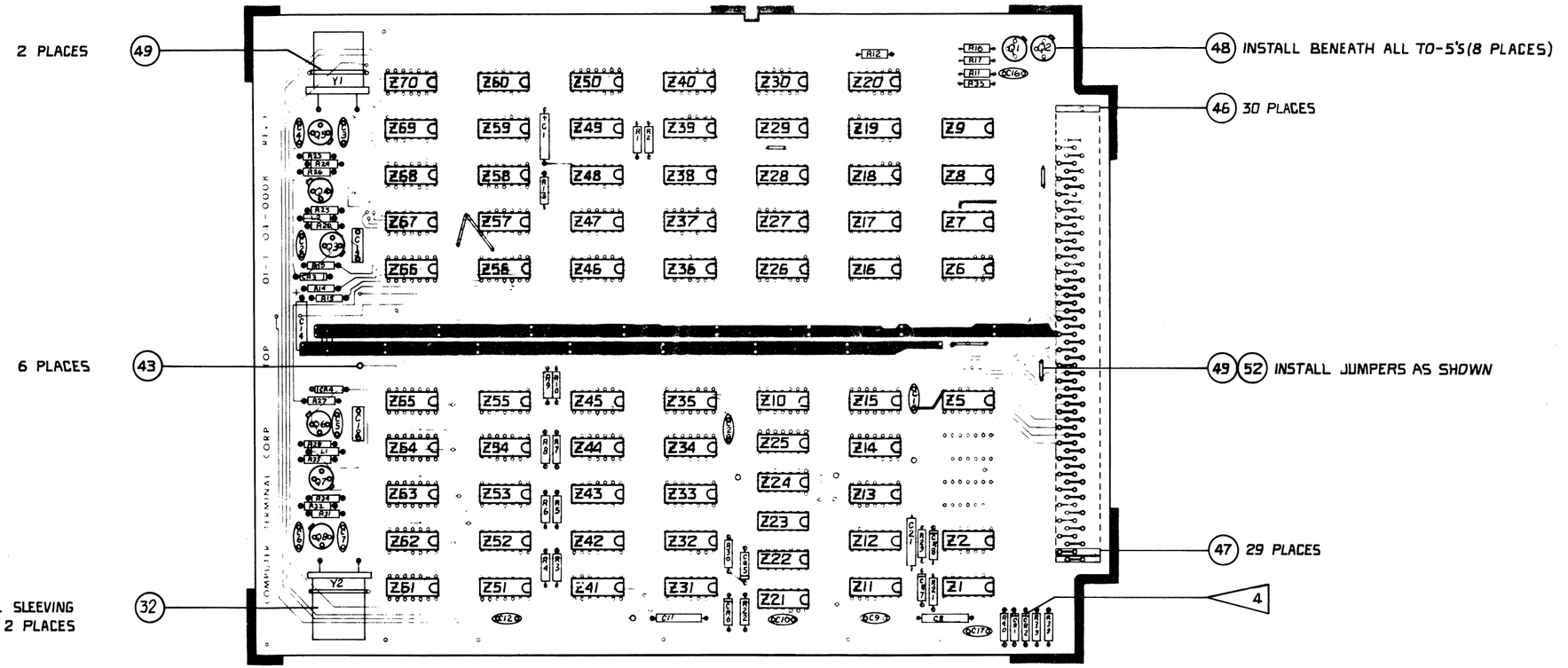
2. AFTER ASSEMBLY, STAMP ASSEMBLY PART NUMBER, REVISION LEVEL AND SERIAL NO ON BOTTOM SIDE. CHARACTORS ARE TO BE 1/16 HIGH (MIN), GOTHIC STYLE, COLOR BLACK. PREFIX ASSEMBLY NO. WITH "ASSY."

1. EQUIVALENT VENDORS PARTS MAY BE USED WITH COMPUTER TERMINAL CORP ENGINEERING APPROVAL.

NOTES: UNLESS OTHERWISE SPECIFIED.

REF DESIGNATOR	ITEM
R23 R31	7
R12,R14,R15,R35,R41	8
R11	9
R16 R38	10
R17	11
R19 R27 R39	12
R20,R21,R22,R28	14
R24 R32	15
R25 R33	16
R26 R34	17
R13,R29,R30	18
R40	19
C18	20
C2 C5	21
C3 C6	22
C9 C10 C12 C13	23
C1 C8 C11 C14 C21	24
C17	25
C15 C16 C20	26
C4 C7	27
C19	28
CR1 THRU CR8	29
Q1 THRU Q8	31
Z1 Z6 Z8 Z17 Z19 Z29 Z58	—
Z56 Z58	33
Z65	34
Z2 Z57	35
Z26 Z27 Z40 Z67	36
Z5	37
Z68 Z69	38
Z9 THRU Z14 Z20 Z28 Z61 THRU Z65	39
Z7 Z16 Z38	41
Z15 Z25 Z18 Z37 Z46 Z51	42
TP1 THRU TP6	43
Y1	44
Y2	45
U L2	30
1 THRU 20	50

Figure 3-10. Interface 2 Assembly (4 of 5)



−4 ASSEMBLY

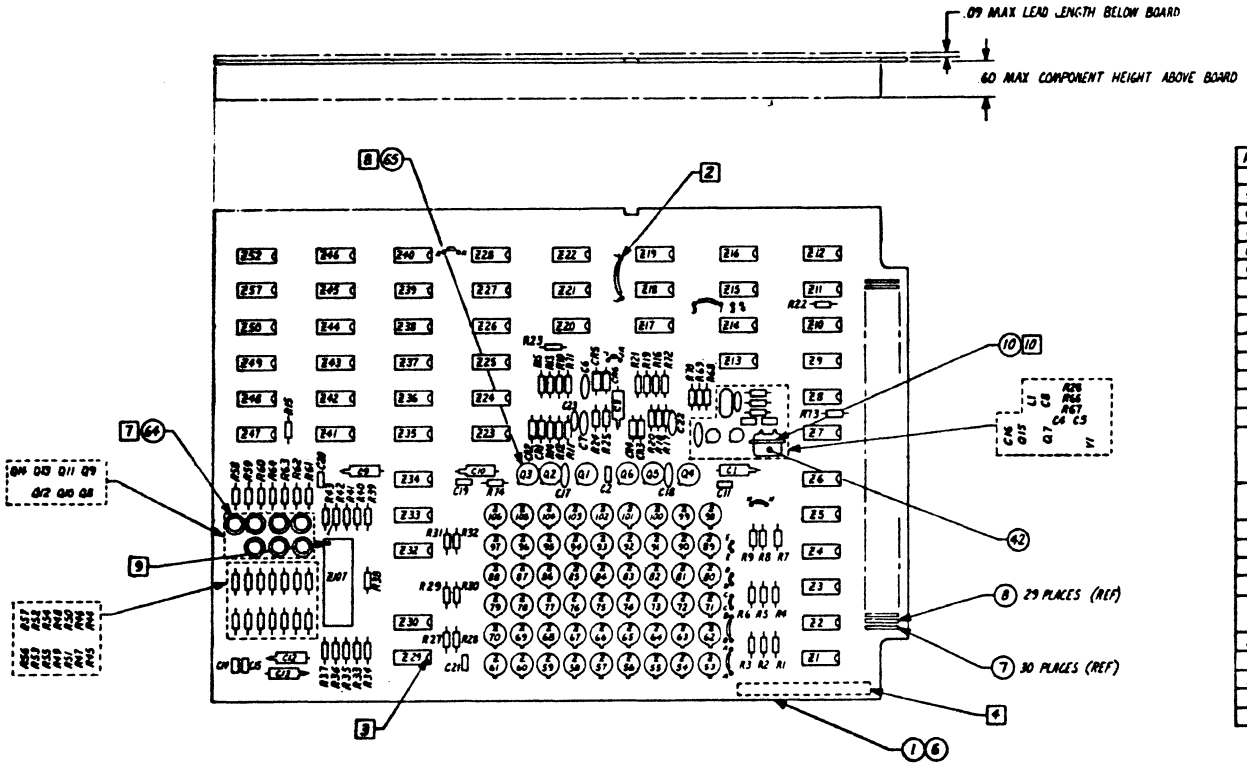
1. ALLOWS OPERATION AT DATA RATES UP TO 2400 B.P.S.
2. REMOVES THE CAPABILITY OF PRESETTING AND CLEARING THE SPACE BAR-OVERWRITE FEATURE.

REF DESIGNATORS	ITEM
R1 R2 R23 R31	7
R3 THRU R10 R12 R14 R15 R35	8
R11	9
R16 R38	10
R17	11
R19 R27 R39	12
R24 R32	15
R25 R33	16
R26 R34	17
R13 R29 R30	18
R40	19
R20 THRU R22 R28	14
C18	20
C2 C5	21
C3 C6	22
C9 C10 C12 C13	23
C1 C8 C11 C14 C21	24
C17	25
C15 C16 C20	26
C4 C7	27
C19	28
CR1 THRU CR8	29
Q1 THRU Q8	31
Z2, Z39, Z57	35
Z1, Z6, Z8, Z17, Z19, Z29, Z36, Z42, Z44, Z50, Z58, Z56	33
Z49, Z52 THRU Z55, Z66	34
Z26, Z27, Z40, Z67,	36
Z5	37
Z68, Z69	38
Z9 THRU Z14, Z20, Z21, Z22, Z23, Z24, Z28, Z30, Z47, Z48, Z59, Z60 THRU Z65, Z70	39
Z31 THRU Z35, Z41, Z43, Z45,	40
Z7, Z16, Z38	41
Z15, Z18, Z25, Z37, Z46, Z51	42
TP1 THRU TP6	43
Y1	44
Y2	45
L1, L2	30

4. CATHODE END OF ALL DIODES IS INDICATED BY EITHER A COLOR BAND, A DOT, OR THE END FROM WHICH THE BANDS ORIGINATE.
3. AFTER ASSEMBLY STAMP ASSEMBLY PART NO. REVISION LEVEL AND SERIAL NO. ON BOTTOM SIDE CHARACTORS ARE TO BE 1/16" HIGH (MIN), GOTHIC STYLE, COLOR BLACK. PREFIX ASSEMBLY NO. WITH "ASSY."
2. FOR −4 REFER TO SCHEMATIC DIAGRAM 01-1-01-0008.
1. EQUIVALENT VENDORS PARTS MAY BE USED WITH COMPUTER TERMINAL CORP. ENGINEERING APPROVAL.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 3-10. Interface 2 Assembly (5 of 5)



REFERENCE DESIGNATOR	ITEM
C1,C3,C9,C10,C12,C13	16
C2,C11,C14,C15,C19,C20,&C21	15
C4,C5	20
C6	19
C7	13
C8	14
C16,C22,C23	17
C17,C18	18
CR1-CR6	22
L1	24
R1,R4,R7,R22,R23,R45,R47, R49,R51,R53,R55,R56,R69, R71,R72,R73	30
R2,R3,R5,R6,R8,R9,R15,R21, R33-R43	33
R10-R14,R16-R20	34
R24,R25	31
R26,R65	26
R27-R32	32
R44,R46,R48,R50,R52,R54, R57-R64,R70,R74,R75	28
R66	29
R67	35
R68	27

REFERENCE DESIGNATOR	ITEM
Q1,Q4	41
Q2,Q5	40
Q3,Q6	38
Q7-Q15	39
Z1-Z7,Z10,Z13,Z41,Z42	45
Z8	50
Z9	52
Z11,Z12,Z14,Z17,Z29,Z32, Z40,Z46	44
Z15	46
Z16	47
Z18,Z19,Z26,Z38,Z39,Z45, Z51,Z52	56
Z20	55
Z21	48
Z22,Z35-Z37,Z43,Z44, Z47,Z48	53
Z23-Z25,Z49,Z50	54
Z27,Z28	51
Z30,Z33,Z34	49
6 Z53-Z106	57
Z107	58
Y1	60-62

6

JUMPER SCHEDULE	
FROM POSITION	TO POSITION
Z61-2	Z61-7
Z70-2	Z70-7
Z79-2	Z79-7
Z88-2	Z88-7
Z97-2	Z97-7
Z106-2	Z106-7

10 INSTALL ITEM 10 (JUMPER) TO SECURE CRYSTAL LENGTH AS REQUIRED

9 BLACK DOT ON ITEM 58 INDICATES PIN NO 1

8 INSTALL ITEM 65 (TRANSIPAD) BENEATH ALL TO-9's, ITEMS 38 & 40

7 INSTALL ITEM 64 (TRANSIPAD) BENEATH ALL TO-18's, ITEMS 39 & 41

6 CHKT Z61, Z70, Z79, Z88, Z97 & Z106 ON 803 ASSY INSTALL JUMPERS PER JUMPER SCHEDULE

5 CATHODE END OF DIODE IS INDICATED BY A COLOR BAND OR A DOT

4 MARK "ASSY ON 11-03-3004 REV F" 12 HIGH CHARACTER COLOR BLACK LOCATE APPROX AS SHOWN

3 COMPONENTS ARE ORIENTATED AS SHOWN

2 INSTALL SOLDER SOCKETS IN HOLES IDENT WITH A,B,C,D,E,M,J,H,R,K,1,2,3,4, BEFORE INSTALLING JUMPERS

1 EQUIVALENT VENDOR PARTS MAY BE USED WITH COMPUTER TERMINAL ENGINEERING APPROVAL

NOTES UNLESS OTHERWISE SPECIFIED

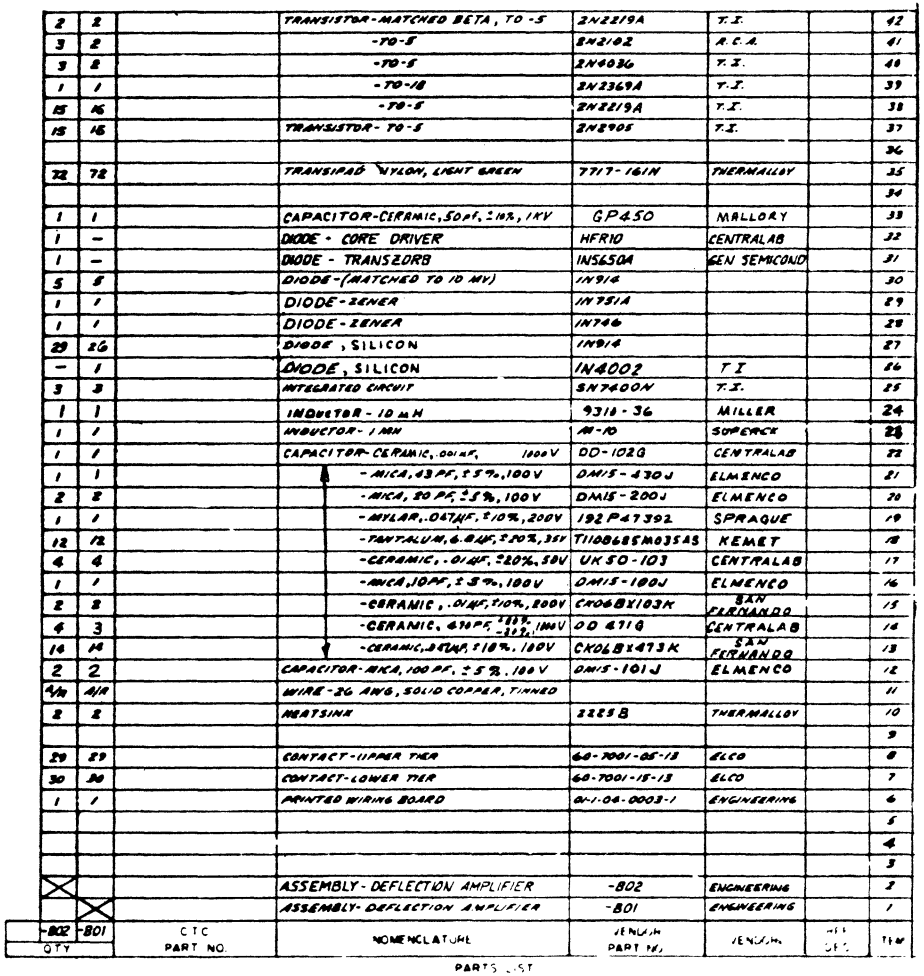
REF								
	REF	803	10-1-01-0004	SCH. DIA. MOS CONTROL LOGIC		CTC ENGR		69
			01-1-01-0005	SCH. DIA MOS CONTROL LOGIC		CTC ENGR		67
4	4	4						66
11	11	11		TRANSIPAD-NYLON LIGHT GREEN	7717-161N	THERMALLOY		65
				TRANSIPAD-NYLON LIGHT GRN	7717-137N	THERMALLOY		64
								63
1				CRYSTAL-25.2 MHZ		SENTRY		62
	1			CRYSTAL-24.9 MHZ		SENTRY		61
		1		CRYSTAL-26.3 MHZ		KNIGHT		60
								59
1	1	1		INTEGRATED CIRCUIT	TMS-28-4151	T.I		58
48	54	54			MM507	NATIONAL		57
8	8	8			SN74H72N	T.I		56
1	1	1			SN74H20N			55
5	5	5			SN74H10N			54
8	8	8			SN74H00N			53
1	1	1			SN7474N			52
2	2	2			SN7473N			51
1	1	1			SN7440N			50
3	3	3			SN13055N			49
1	1	1			SN7420N			48
1	1	1			SN7410N			47
1	1	1			SN7409N			46
11	11	11			SN7401N			45
8	8	8		INTEGRATED CIRCUIT	SN7400N	T.I		44
A/R	A/R	A/R		SLEEVING, VINYL, HEATSHRINK	HVX 3/4	CO RALLY		42
2	2	2		TRANSISTOR - TO-18	2N3250	T.I		41
2	2	2		- TO-5	2N2905			40
9	9	9		- TO-18	2N2369			39
2	2	2		TRANSISTOR - TO-5	2N2219A	T.I		38
								37
-803 QTY	-802 QTY	-801 QTY	CTC PART NO	NOMENCLATURE	VENDOR PART NO	VENDOR	REF DES	ITEM

PARTS LIST

2	1	1		RESISTOR - CARBON COMP, 18K Ω, 1/4W, 5%	RC07GF182J		AB	35
10	10	10		10K Ω, 1/4W, 5%	RC07GF103J			34
19	19	19		47K Ω, 1/4W, 5%	RC07GF472J			33
6	6	6		39K Ω, 1/4W, 5%	RC07GF392J			32
2	2	2		27K Ω, 1/4W, 5%	RC07GF272J			31
16	16	16		2.2K Ω, 1/4W, 5%	RC07GF222J			30
1	1	1		1.5K Ω, 1/4W, 5%	RC07GF152J			29
17	17	17		1.8K Ω, 1/4W, 5%	RC07GF132J			28
1	1	1		680 Ω, 1/4W, 5%	RC07GF681J			27
2	2	2		RESISTOR - CARBON COMP, 560 Ω, 1/4W, 5%	RC07GF560J		AB	26
								25
1	1	1		INDUCTOR - 100 UH		9230-68	J.W. MILLER	24
								23
6	6	6		DIODE		IN914		22
								21
2	2	2		CAPACITOR - CERAMIC 100 PF 100 V		DM15-101J	ELMENCO	20
1	1	1		- CERAMIC 20 PF 100 V		DM15-200J		19
2	2	2		- CERAMIC 470 PF 100 V		DM15-471J		18
3	3	3		- CERAMIC 82 PF 100 V		DM15-820J	ELMENCO	17
6	6	6		- TANTALUM 6.8 μF 35V		T110B685M035AS	KEMET	16
7	7	7		- CERAMIC .01 μF 200 V		CK06BX103K	SPRAGUE	15
1	1	1		- CERAMIC .01 μF 10 V		UK10-104	CENTRALAB	14
1	1	1		CAPACITOR - CERAMIC .001 μF 200 V		DD-102G	CENTRALAB	13
								12
A/R	A/R	A/R		SLEEVING, TEFLON, NO 22		C545	PENN TUBE	11
A/R	A/R	A/R		JUMPER, SOLID, TINNED, 24 AWG		8022	BELDEN	10
20	20	20		SOCKET - SPRING		6-330808-0	AMP	9
29	29	29		CONTACT - UPPER TIER		60-7001-05-13	ELCO	8
30	30	30		CONTACT - LOWER TIER		60-7001-15-13	ELCO	7
1	1	1	01-1-02-0004-1	PWB MOS CONTROL LOGIC			CTC ENGR	6
								5
			-803	PWA MOS CONTROL LOGIC (338C)		-803	CTC ENGR	4
			-802	PWA MOS CONTROL LOGIC		-802	CTC ENGR	3
			-801	PWA MOS CONTROL LOGIC		-801	CTC ENGR	2
-803 QTY	-802 QTY	-801 QTY	CTC PART NO	NOMENCLATURE	VENDOR PART NO	VENDOR	REF DES	ITEM

PARTS LIST

Figure 3-11. MOS Assembly



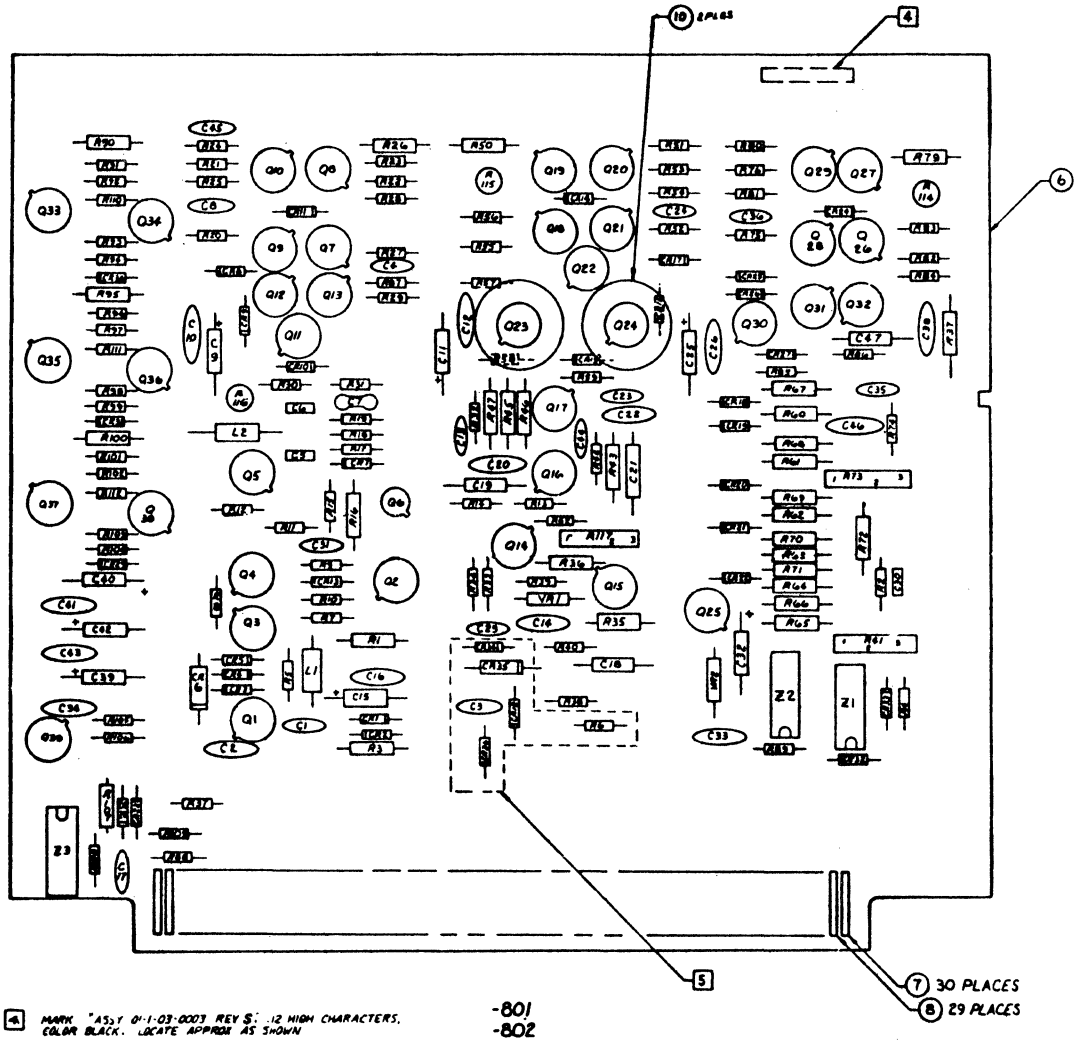
-802 QTY	-801 QTY	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	REF DES	ITEM
2	2		TRANSISTOR-MATCHED BETA, TO-5	2N2219A	T.I.		42
3	2		-TO-5	2N2102	R.C.A.		41
3	2		-TO-5	2N4036	T.I.		40
1	1		-TO-18	2N2369A	T.I.		39
15	16		-TO-5	2N2219A	T.I.		38
15	16		TRANSISTOR-TO-5	2N2905	T.I.		37
							36
72	72		TRANSIPAD NYLON, LIGHT GREEN	7717-161N	THERMALLOY		35
							34
1	1		CAPACITOR-CERAMIC, 50pf, ±10%, 1KV	GP450	MALLORY		33
1	—		DIODE - CORE DRIVER	HFR10	CENTRALAB		32
1	—		DIODE - TRANSZORB	1N6650A	GEN SEMICOND		31
5	5		DIODE-(MATCHED TO 10 MV)	1N914			30
1	1		DIODE-ZENER	1N751A			29
1	1		DIODE-ZENER	1N746			28
29	26		DIODE, SILICON	1N914			27
—	1		DIODE, SILICON	1N4002	T I		26
3	3		INTEGRATED CIRCUIT	SN7400N	T.I.		25
1	1		INDUCTOR - 10 mH	9318-36	MILLER		24
1	1		INDUCTOR - 1 MH	M-10	SUPERCK		23
1	1		CAPACITOR-CERAMIC, .001uF, 1000V	DD-102G	CENTRALAB		22
1	1		-MICA, 43 PF, ±5%, 100V	DM15-430J	ELMENCO		21
2	2		-MICA, 20 PF, ±5%, 100V	DM15-200J	ELMENCO		20
1	1		-MYLAR, .047uF, ±10%, 200V	192P47392	SPRAGUE		19
12	12		-TANTALUM, 6.8uF, ±20%, 35V	T110B685M035AS	KEMET		18
4	4		-CERAMIC, .01uF, ±20%, 50V	UK50-103	CENTRALAB		17
1	1		-MICA, 10PF, ±5%, 100V	DM15-100J	ELMENCO		16
2	2		-CERAMIC, .01uF, ±10%, 200V	CK06BX103K	SAN FERNANDO		15
4	3		-CERAMIC, 470PF, +80% -20%, 1KV	DD 471G	CENTRALAB		14
14	14		-CERAMIC, .047uF, ±10%, 100V	CK06BX473K	SAN FERNANDO		13
2	2		CAPACITOR-MICA, 100 PF, ±5%, 100V	DM15-101J	ELMENCO		12
4/in	4/in		WIRE-26 ANG, SOLID COPPER, TINNED				11
2	2		HEATSINK	22858	THERMALLOY		10
							9
29	29		CONTACT-UPPER TIER	60-7001-05-18	ELCO		8
30	30		CONTACT-LOWER TIER	60-7001-15-13	ELCO		7
1	1		PRINTED WIRING BOARD	01-1-08-0003-1	ENGINEERING		6
							5
							4
							3
X			ASSEMBLY-DEFLECTION AMPLIFIER	-802	ENGINEERING		2
	X		ASSEMBLY-DEFLECTION AMPLIFIER	-801	ENGINEERING		1

PARTS LIST

-802 QTY	-801 QTY	CTC PART NO.	NOMENCLATURE	VENDOR PART NO.	VENDOR	REF DES	ITEM
1	1		POTENTIOMETER - 2K 1/2W ± 5%	53-1-2-202	SPECTROL		86
2	2		POTENTIOMETER - 100Ω, 1/4W ± 5%	62-1-1-101	SPECTROL		85
1	1		POTENTIOMETER - 10K	61-2-1-103	SPECTROL		84
1	1		POTENTIOMETER-2K	61-2-1-202	SPECTROL		83
1	1		POTENTIOMETER-5K	61-2-1-502	SPECTROL		82
3	3		RESISTOR, CARBON COMP, 820Ω, 1/4W ± 5%				81
1	1		RESISTOR-METAL FILM, 4.0K OHMS, 1/4W, ±.5%	RN60D4001	A.B.		80
1	1		1.98K ±.25%	1981			79
1	1		3.32K ±1%	3321F			78
1	1		8.0K	8001F			77
1	1		16.0K	1602F			76
1	1		32.0K	3203F			75
1	1		1.78K	1781F			74
1	1		2.87K	2871F			73
1	1		4.32K	4321F			72
1	1		5.49K	5491F			71
1	1		6.34K	6341F			70
1	1	-METAL FILM, 3.92K	1/4W, ±1%	RN60D3921F			69
1	1	-CARBON COMP, 15K	1/4W, ±5%	RC07GF153J			68
4	4	-CARBON COMP, 3.9K	1/2W, ±5%	RC20GF392J			67
3	3	3.3K		332J			66
2	2	1.0K		102J			65
1	1	330		331J			64
2	2	560		561J			63
2	2	470	1/2W	RC20GF471J			62
1	1	27K	1/4W	RC07GF273J			61
1	1	1.2K		122J			60
8	9	15K		153J			59
2	2	22K		223J			58
1	1	1.8K		182J			57
4	4	2.7K		272J			56
3	3	12.0K		123J			55
1	1	3.3K		332J			54
14	14	1.8K		182J			53
10	9	4.7K		472J			52
5	5	2.2K		222J			51
6	6	1.5K	1/4W	152J			50
							49
1	1	6.8	1/2W	6R8J			48
10	10	47	1/4W	470J			47
4	6	560		561J			46
2	2	510		511J			45
2	2	680		681J			44
4	4	RESISTOR-CARBON COMP, 470 OHMS, 1/4W, ±5%		RC07GF471J	A.B.		43

PARTS LIST

Figure 3-12. Deflection Amplifier Assembly (1 of 2)



REFERENCE DESIGNATOR	ITEM
C1, 13	12
C2, 10, 12, [illegible] 20, 22, 24, 33, 34, 38, 41, 43, 46	13
5 C3, [illegible] 16, 45	14
C30	21
C5, 6	15
C7	16
C8, 29, 31, 36	17
C9, 11, 15, [illegible] 25, 32, 37, 39, 40, 42, [illegible]	9
C17, 28	20
C18	19
C35	22
L1	24
L2	23
C4	33
Z1, 2, 3	25
5 CR1-17, 23-34	27
CR18-22	30
CR35	31
CR36	32
VR1	28
VR2	29
Q1, 4, 5, 9, 10, 15, 17, 20, 21, 25, 28, [illegible] 33, 35, 37	37
Q2, 3, 12, 14, 16, 18, 19, 22, 26, 27, 31, 34, 36, 38, 39	38
Q6	39
Q7, 8	42
Q13, 23, 32	40
Q11, 24, 30	41
R1, 3	62
R2, 39	58
R4, 11, 25, 51, 54, 81	52
R5, 12, 24, 76	43
R7, 9, 14, 28, 29, 35, 45, 51, 83, 84, 87, 88, 104	53
R10, 109	44

REFERENCE DESIGNATOR	ITEM
R16, 45	65
R6, 15, 32, 37, 91, 94, 95, 99, 103, 104	52
R17, 18	45
R40	54
R20, 21, 52, 53, 75, 76	46
R22, 23, 30, 31, 42, 44, 48, 57, 85, 86	47
R26, 50, 79	66
R27, 55, 82	55
R33, 80, 88, 89	56
R34	57
R35, 66	63
R117	84
R36	48
R19, 31, 96, 101, 105	51
R41	82
R43, 90, 95, 100	67
R46	68
R47	69
R60	70
R61	71
R62	72
R63	73
R64	74
R65	64
R67	75
R68	76
R69	77
R70	80
R71	78
R72	79
R73	81
R92, 97, [illegible]2	59
R107	60
R108	61
R110, 111, 112	91
R114, 115	85
R116	86

4. MARK "ASSY 01-1-03-0003 REV S" .12 HIGH CHARACTERS, COLOR BLACK. LOCATE APPROX AS SHOWN

3. COMPONENTS ARE ORIENTED AS SHOWN

2. REF DWG: SCHEMATIC DIAGRAM FOR -801 ASSY: 01-1-01-0003

1. EQUIVALENT VENDOR PARTS MAY BE USED WITH CTC ENGR APPROVAL

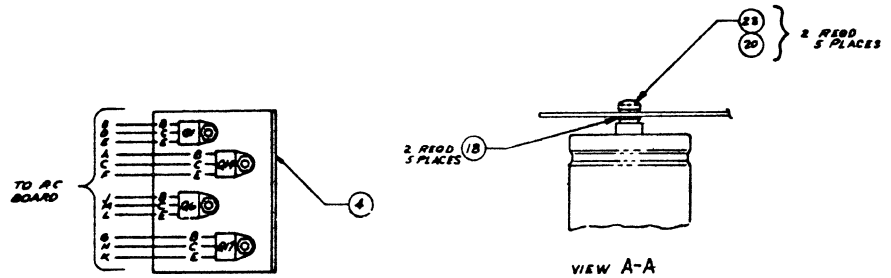
-801
-802

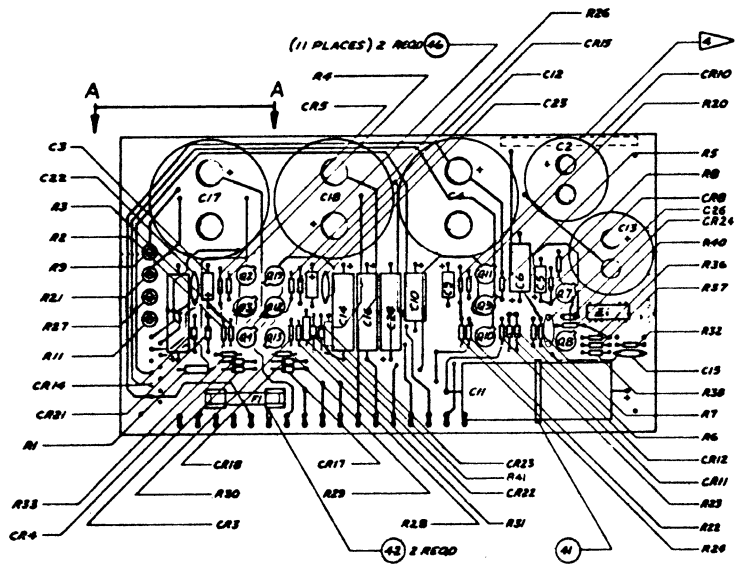
5. THE FOLLOWING COMPONENTS WILL NOT BE USED IN -801 ASSY C3, CR12, CR34, CR35, CR36 & R6. IN LIEU OF C3 ACQ INSULATED JUMPER WIRE

7. 30 PLACES

8. 29 PLACES

Figure 3-12. Deflection Amplifier Assembly (2 of 2)





-801 ASSY

REFERANCE DESIGNATOR	ITEM
F1	43
Q3, Q4, Q7, Q8, Q11, Q19	39
Q2, Q9, Q10, Q12, Q13	40
CR14, CR20, CR22, CR23	38
CR8, CR10	35
CR9, CR15	36
CR3, CR4, CR11, CR13, CR17, CR18	37
CR24	33
21	34
C26	24
C17, C19	31
C15, C22, C23	25
C11	29
C6, C10, C24	28
C4	32
C3, C5, C9, C12	26
C2, C13	30
C1, C14, C16, C..	27
R40	17
R37, R38	14
R36	15
R41	16
R11, R27	22
R9, R21	21
R8	8
R7, R22	9
R6, R30, R24	11
R4, R5, R25, R26, R27, R32, R33	13
R2, R3, R28, R30	12
R1, R31	19

A/R		WIRE, 22 GA. STRANDED, RED				47
22	15-42	TRANSIPAD	7717-161	THERMALLOY		46
A/R		SILICONE COMPOUND	340			45
A/R		SOLDER, SN60-40				44
1	8-47	FUSE 5A				43
2	24-42	FUSEHOLDER				42
1		STRAP, NYLON	SST31M	PANDUIT		41
5	5-73	TRANSISTOR	2N2905	T.I		40
6	1-73	TRANSISTOR	2N2218			39
4	4-70	DIODE	IN4003			38
6	3-70	DIODE	IN4001			37
2	7-70	DIODE	IN752			36
2	6-70	DIODE	IN746A			35
1	26-71	INTEGRATED CIRCUIT	SN7405N	T.I		34
1	31-70	DIODE	IN914	T.I.		33
1	6-36	CAPACITOR, ELECTROLYTIC, 13000 µF. 15 V	3-85CL13000-15	CALLINS		32
2	5-36	5000 µF, 50 V	3-85CL 5000-50			31
2	7-36	4000 µF, 25 V	2-85CL4000-25			30
1	9-36	3600 µF, 15V	12-85 PSD3600-15			29
3	1-36	135 µF, 10V	4-85PSD135-10	CALLINS		28
3	3-36	ELECTROLYTIC, 100 µf, 25 V	6-85PSD100-25	CALLINS		27
4	11-35	TANTALUM, 6.8 µF, 35 V	T110B685M035AS	KEMET		26
3	1-35	CAPACITOR, CERAMIC, .1 µF, 25 V	UK25-104	CENTRALAB		25
1	6-35	CAPACITOR .005 µF 1KV (CERAMIC)	DD 5022	CENTRALAB		24
10	48-50	SCREW, PAN HEAD, 10-32 x 1/2				23
2	6-66	RESISTOR, POT. 2 K, 3/4 W ± 20%	62-1-1-202	SPECTROL		22
2	9-66	RESISTOR, POT. 500 OHM, 1/2 W ± 5%				21
10	18-50	WASHER, SPLIT LOCK #10				20
2	58-65	RESISTOR - 470 OHM, 1/2 W ± 5%	RC20GF471J			19
10		WASHER, LOCK, EXT. TOOTH #10				18
1	21-65	RESISTOR - 4.7K OHM, 1/4W ± 5%	RC07GF472J	A.B.		17
1	60-65	RESISTOR - 560 OHM, 1/2 W ± 5%	RC20GF561J			16
1	5-65	RESISTOR - 33K OHM, 1/4W ± 5%	RC07GF333J	A.B.		15
2	29-65	-2.2K	222J			14
7	30-65	-1K	102J			13
4	25-65	-820	821J			12
3	14-65	-470	471J			11
						10
2	18-65	-180	181J			9
1	13-65	RESISTOR - 150 OHM, 1/4W. ± 5%	RC07GF151J			8
						7
1		PWB, LOGIC POWER SUPPLY	01-1-02-0001-1	CTC ENGR.		6
						5
1		ASSEMBLY, POWER TSTR BRACKET	01-1-09-0013-1	CTC ENGR.		4
						3
						2
		PWA, LOGIC POWER SUPPLY	01-1-03-0001-801	CTC ENGR		1
QTY	CTC PART NO	NOMENCLATURE	VENDOR PART NO	VENDOR	REF DES	ITEM

-801

PARTS LIST

3. COMPONENTS ARE ORIENTATED AS SHOWN

2. REF DWG, SCHEMATIC DIAGRAM FOR - 801 ASSY 01-1-01-0001

1. EQUIVALENT VENDOR PARTS MAY BE USED WITH COMPUTER TERMINAL ENGINEERING APPROVAL

NOTES (UNLESS OTHERWISE SPECIFIED)

4 MARK ASSY 01-1-03-0001-801 REV P 12 HIGH CHARACTER, COLOR BLACK, LOCATE APPROX AS SHOWN

Figure 3-13. Logic Power Supply Assembly

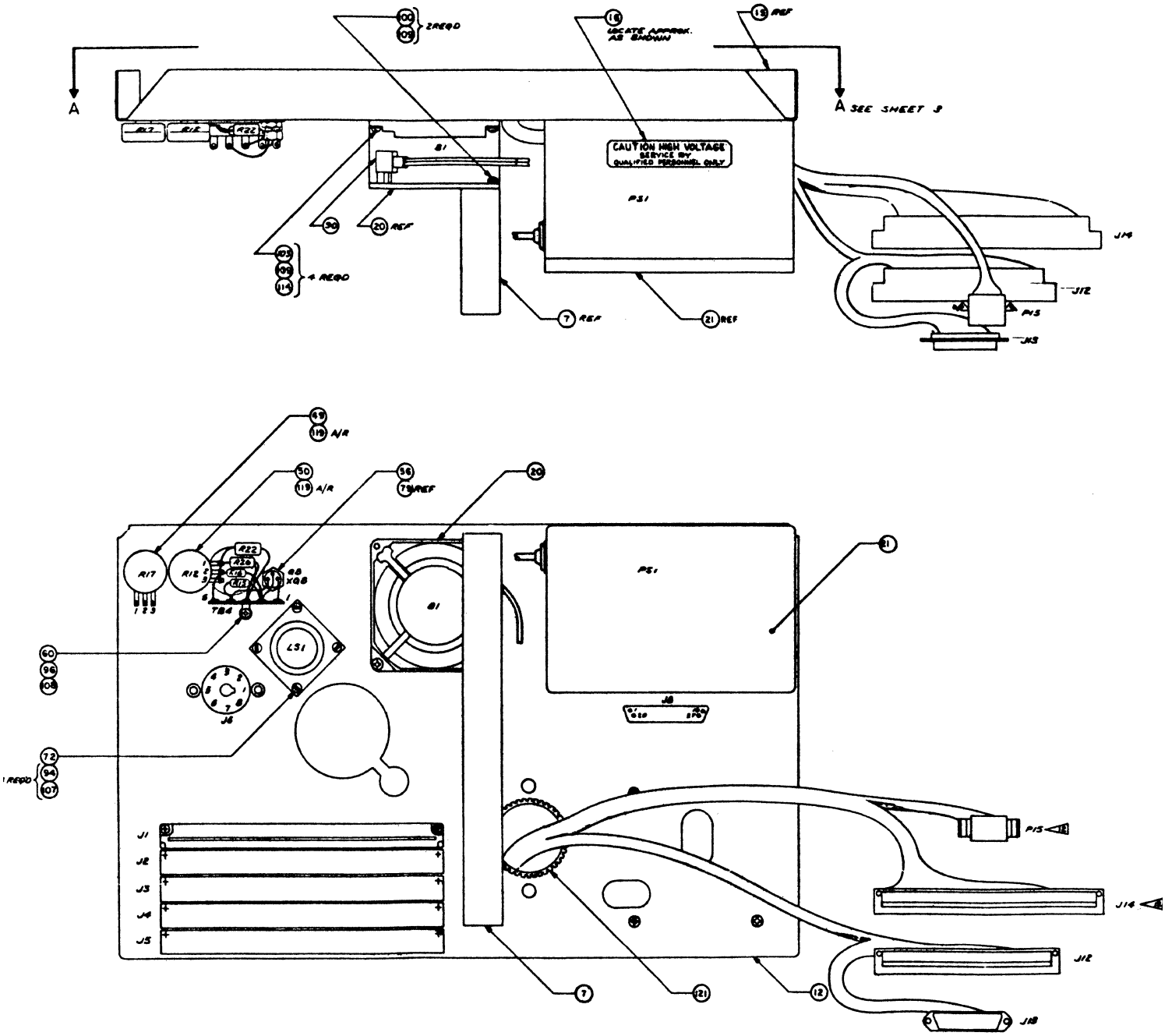
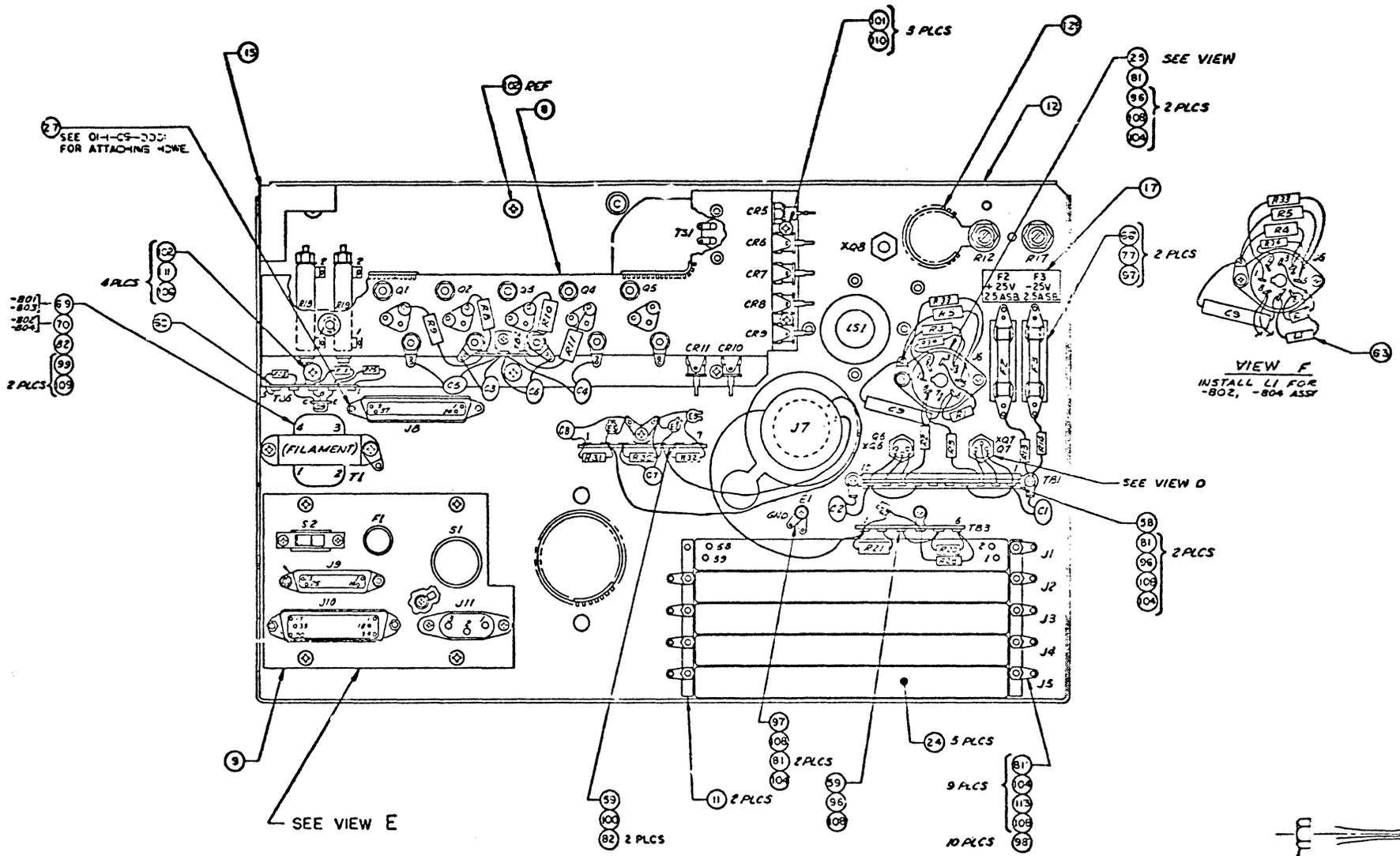
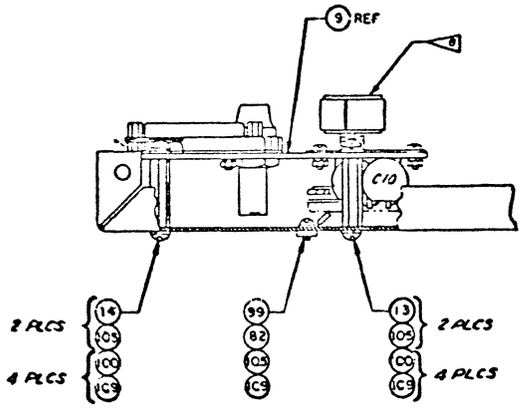
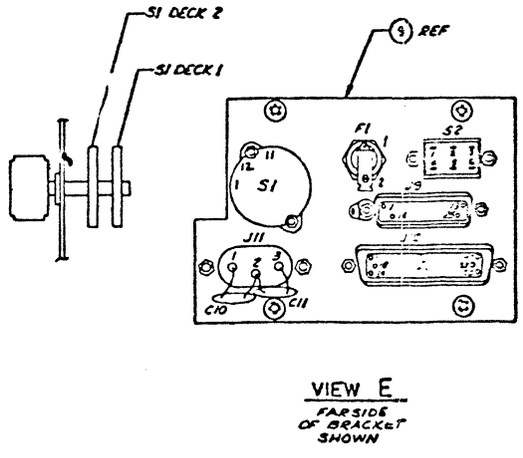


Figure 3-14. Rear Panel Assembly (1 of 3)

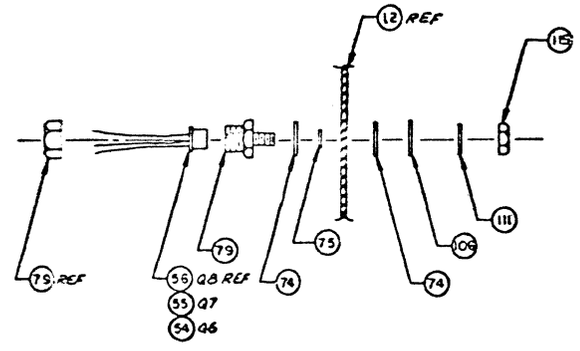




VIEW A-A
SEE SHT 2



VIEW E
FAR SIDE OF BRACKET SHOWN



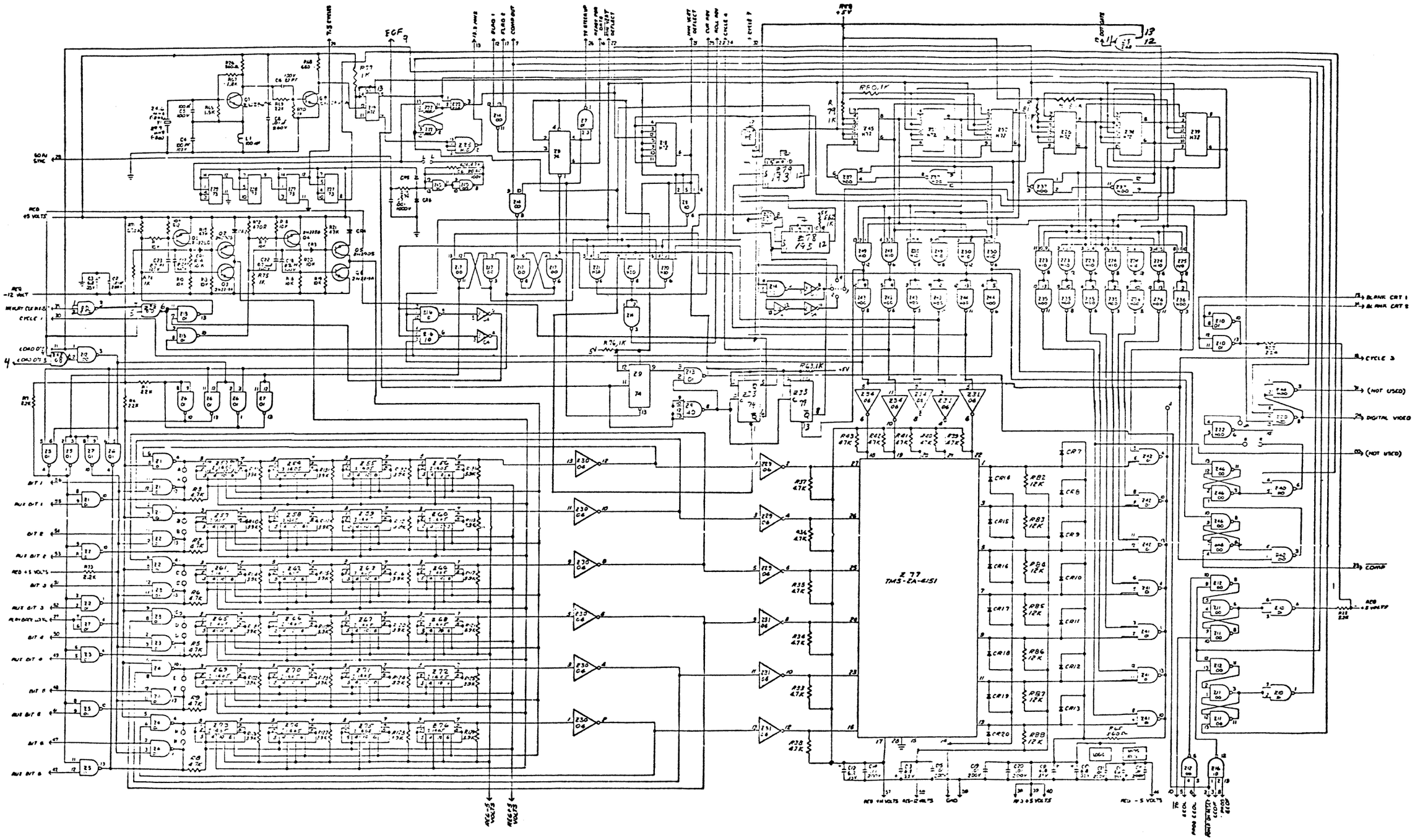
VIEW D
TYP TRANSISTOR MTG FOR Q6, Q7, Q8

Figure 3-14. Rear Panel Assembly (2 of 3)

Figure 3-14. Rear Panel Assembly (3 of 3)

RECOMMENDED SPARE PARTS LIST
(Quantities shown are per 100 Terminals)

QTY	CTC PART NO.	DESCRIPTION		
2	000-002-70	Diode,	IN3644,	CR1
12	000-004-70	Diode	IN4003,	CR 3,4,5,6,
12	000-006-71	IC	SN7474	
12	000-007-71	IC	SN7473	
12	000-009-71	IC	SN7440	
12	000-010-71	IC	SN7430	
12	000-012-71	IC	SN7410	
12	000-013-71	IC	SN7402	
12	000-014-71	IC	SN7401	
12	000-015-71	IC	SN7400	
24	000-016-71	MOS CAN	MM507	
1	000-002-46	Crystal	263 MHZ Y1	
12	000-002-71	IC	SN74H20N	
12	000-001-71	IC	74H72N	
4	000-008-70	Diode	1N914	CR1-6
6	000-001-73	Transistor	2N2219A	
6	000-004-73	Transistor	2N2369	
6	000-003-73	Transistor	2N2905	
6	000-007-73	Transistor	2N3205	
12	000-011-71	IC	SN7420	
12	000-004-71	IC	SN74H00N	
12	000-003-71	IC	SN74H10N	
24	000-001-78	Key Switch		
6	000-002-78	Space Bar		
12	000-005-70	Diode	IN746	
6	000-007-70	Diode	IN752	
4	000-007-70	Diode	IN752A	
2	000-009-70	Diode	IN755	
12	000-003-70	Diode	IN4001	
4	000-005-73	Diode	2N681	
6	000-010-73	Diode	2N4036	
24	000-002-47	Fuse	5A F1	
4	000-006-70	Diode, Zener	IN751A	
6	000-011-73	Transistor	2N2102	
1	000-008-46	Crystal	225-280 KHZ	
1	000-007-46	Crystal	307-200 KNZ	
4	000-002-73	Transistor	2N4902	
4	000-006-73	Transistor	2N5068	
2	000-005-78	Slide Switch		
2	000-004-78	Rotary Switch		
2	000-003-78	Thermal		
24	000-001-47	Fuse 25AMP		
6	000-011-70	Diode	MR 1120	
6	000-001-70	Diode	MR 1121	
6	000-012-70	Diode	IN 2992	
6	000-013-70	Diode	IN 3008	



4. All diodes are in 914

3. Logic symbols per mil—std—806, electronic symbols per USA—std—Y32.2 —67

2. Numbers shown below reference designation within logic symbols are segments of vendor part numbers described in parts list

1. Partial reference designations are shown; for complete designation prefix with unit and/or assembly designation

VOLTAGE CHART	
VOLTAGE	CONNECTOR PIN USED
GND	1, 59
-5	44
+5	38, 39, 40
-12	58
+14	57

I.C NO	GND PIN	+5 PIN	-5 PIN	-12 PIN	+14 PIN
Z1-Z26 Z29-Z46	7	14			
Z48-Z52	7	14			
Z53-Z76	8	16			
Z78, Z79	8	16			
Z77	14, EE			15	17

REF. DES.	
LAST USED	NOT USED
R88	R64
C23	
Z79	Z47
CR20	
Q8	
L1	
Y1	

NOTES: (UNLESS OTHERWISE SPECIFIED)

Figure 3-15. Schematic Diagram MOS Control Logic

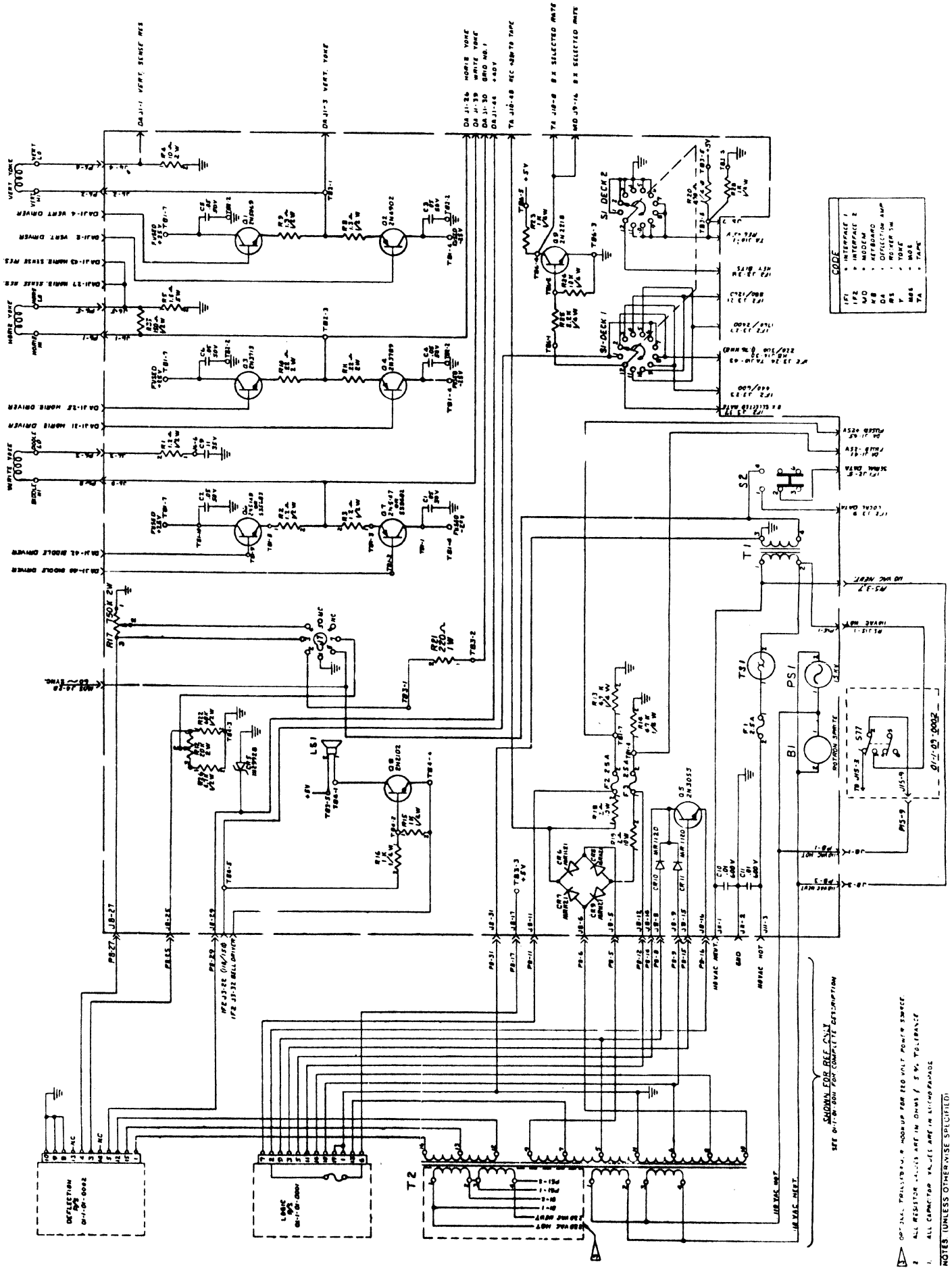


Figure 3-16. SCHEMATIC DIAGRAM REAR PANEL 3300