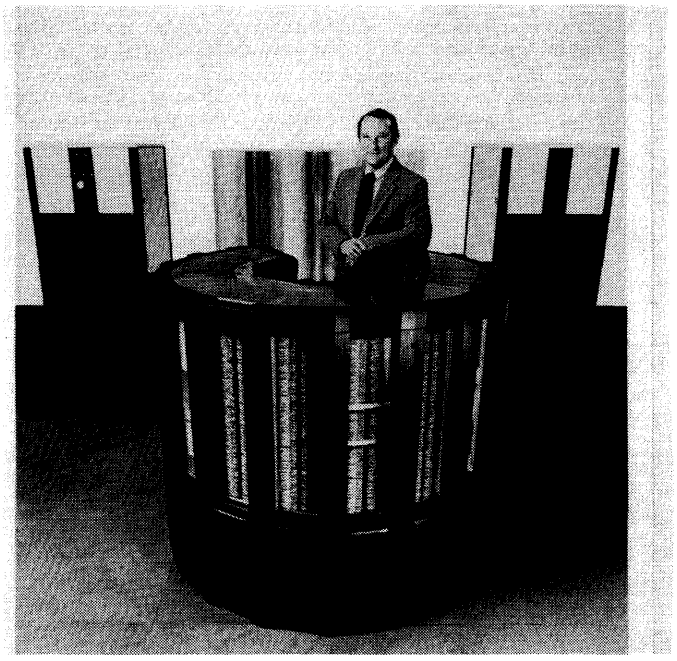
Cray Research Supercomputers

MANAGEMENT SUMMARY

Founded in 1972, Cray Research is currently the leading supplier of supercomputers. The Cray-1, which was introduced in 1976, was the first commercially successful vector processor and has become the standard for scientific supercomputers. However, the Cray-1 has been superseded by the X-MP Series, introduced in 1982, and the top-of-the-line Cray-2, introduced in 1985. The X-MP Series is architecturally very similar to the Cray-1, while the Cray-2 is a new design.

The Cray systems are specifically designed for computationally intensive applications, such as physical simulation and modeling. The systems perform both conventional scalar processing and vector processing. In scalar processing, the computer starts an instruction, handles one operand or operand pair, and produces a single result. A vector instruction operates on a series of elements, repeating the same function and producing a series of results. The main advantage of vector processing is that it eliminates instruction start-up time for all but the first operand.

All Cray systems except the X-MP/1 systems are multiprocessor systems that permit several programs to execute simultaneously on the processors within the system. The systems also perform multitasking, a feature that enables a ➢



The Cray-2 is the fastest computer system currently available. The system includes four 4.1-nanosecond central processors and 2 gigabytes of main memory. One compact circular unit houses the memory, computer logic, and DC power supplies. The Cray-2 occupies only 16 square feet of floor space.

The Cray X-MP Series and Cray-2 supercomputers perform high-speed vector and scalar processing for a variety of scientific, engineering, and industrial applications. The systems can be linked to other vendors' general-purpose mainframes, which can serve as front-end systems to the Crays.

MODELS: X-MP/1 Series, X-MP/2 Series, X-MP/4 Series, and Cray-2.
CONFIGURATION: The X-MP Series include 1, 2, or 4 central processors, from 8 to 128 megabytes of main memory, up to 4 I/O processors, and from 4 to 10 I/O channels. The Cray-2 contains 4 central processors, a foreground processor, 2 gigabytes of main memory, and 4 high-speed channels.
COMPETITION: ETA Systems (Control Data) Cyber 205.
PRICE: Purchase prices for basic systems range from $5,000,000 to $17,000,000.

CHARACTERISTICS

MANUFACTURER: Cray Research, Inc., 608 Second Avenue South, Minneapolis, MN 55402. Telephone (612) 333-5889. In Canada: Cray Canada Inc., 4141 Yonge Street, Toronto, Ontario M2P 2A8. Telephone (416) 229-2729.

MODELS: X-MP/11, X-MP/12, X-MP/14, X-MP/18, X-MP/24, X-MP/28, X-MP/216, X-MP/48, X-MP/416, and Cray-2.

DATA FORMATS

BASIC UNIT: Each word consists of 64 data bits and 8 check bits.

FIXED-POINT OPERANDS: On the X-MP Series, integer addition and subtraction operations produce either 24-bit or 64-bit results in twos complement mode. An integer multiply operation produces 24-bit results. A 64-bit multiply operation or an integer divide operation can be performed through a software algorithm that uses the floating-point hardware.

The Cray-2 performs 32-bit or 64-bit integer arithmetic in twos complement mode.

FLOATING-POINT OPERANDS: One single-precision 64-bit word, consisting of a 1-bit sign, a 15-bit exponent, and a 48-bit normalized coefficient. The floating-point format allows the accurate expression of numbers to about 15 decimal digits. The Cray hardware does not provide for double-precision operations, but software routines provide double-precision computations with 95-bit accuracy.

INSTRUCTIONS: Divided into parcels of 16 or 32 bits on X-MP Series processors. Instructions are packed 4 parcels per word. A 2-parcel instruction begins in any parcel of a word and continues across the word boundary. Any parcel position can be addressed in branch instructions. ➢

Cray Research Supercomputers

TABLE 1. SYSTEM COMPARISON

MODEL	X-MP/11	X-MP/12	X-MP/14	X-MP/18	X-MP/24
SYSTEM CHARACTERISTICS					
Date announced	1984	1984	1984	September 1985	1982
Date first delivered	—	—	—	2nd Quarter 1986	—
Field upgradable to	X-MP/12	X-MP/14	X-MP/18	Not applicable	X-MP/28
Relative performance*	1.5 to 2.5	1.5 to 2.5	1.5 to 2.5	1.5 to 2.5	3.0 to 5.0
Number of processors	1	1	1	1	2
Cycle time, nanoseconds	9.5	9.5	9.5	9.5	9.5
Word size, bits	64	64	64	64	64
Operating systems	COS, Unicos	COS, Unicos	COS, Unicos	COS, Unicos	COS, Unicos
MAIN MEMORY					
Type	MOS	MOS	MOS	MOS	MOS
Minimum capacity, bytes	8M	16M	32M	64M	32M
Maximum capacity, bytes	8M	16M	32M	64M	32M
Increment size, bytes	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Cycle time, nanoseconds	76	76	76	76	76
BUFFER STORAGE					
Minimum capacity	Not available	Not available	Not available	Not available	Not available
Maximum capacity	—	—	—	—	—
Increment size	—	—	—	—	—
INPUT/OUTPUT CONTROL					
Number of channels:					
Byte multiplexer	0	0	0	0	0
Block multiplexer	4 to 12 per XIOP	4 to 12 per XIOP	4 to 12 per XIOP	4 to 12 per XIOP	4 to 12 per XIOP
Word	0	0	0	0	0
Other	4 to 7	4 to 7	4 to 7	4 to 7	7

**Compared to a Cray-1.*

program to be divided into multiple parts or tasks that can be executed in parallel. In the Cray systems, the central processors are dynamically assigned to perform multiple tasks. Data and communications travel very rapidly between the CPUs.

The Cray X-MP Series consists of 9 models that vary primarily in the number of central processors and the amount of main memory configured. All X-MP Series systems have a machine cycle time of 9.5 nanoseconds, compared to the 12.5-nanosecond Cray-1. According to Cray, the X-MP Series systems provide from 1.5 to 10 times the performance of a Cray-1.

The X-MP/1 systems are uniprocessors that support from 8 to 64 megabytes of shared main memory and from 4 to 7 I/O channels. The X-MP/2 systems are dual-processor systems supporting from 32 to 128 megabytes of shared main memory and 7 I/O channels. The X-MP/4 systems include 4 central processors, 64 or 128 megabytes of shared main memory, and 10 I/O channels. Memory upgrades are available to upgrade models within the X-MP/1, X-MP/2, and X-MP/4 series, but models cannot be field upgraded from an X-MP/1 to an X-MP/2, or from an X-MP/2 to an X-MP/4. The X-MP Series systems are not upgradable to a Cray-2.

All X-MP Series systems are housed in columns arranged in an arc, with a bench-like projection at the base of the arc. This circular arrangement keeps wire lengths short and reduces floor space requirements.

The Cray-2, with a cycle time of 4.1 nanoseconds, is currently the fastest computer available. It also boasts the

The background processors in the Cray-2 translate instructions into 16-bit parcels packed 4 per word.

INTERNAL CODE: ASCII.

MAIN MEMORY

In multiprocessor X-MP systems, main memory is shared among the processors. Memory is organized into 16 or 32 interleaved banks on the X-MP/1 and X-MP/2, and into 32 or 64 banks on the X-MP/4. Each CPU in an X-MP/2 or X-MP/4 system has 4 memory access ports: 3 used for CPU register transfers and 1 used for input/output operations. On the X-MP/1, there are 2 I/O ports and 3 CPU ports. Each port can make one reference per clock period.

Common Memory on the Cray-2 consists of 128 banks divided into quadrants of 32 banks each. Each memory quadrant has a data path to each of 4 memory ports. A background processor and a foreground communication channel are connected to each port. Total memory bandwidth is 64 billion bits per second.

STORAGE TYPE: Metal oxide semiconductor (MOS) or emitter coupled logic (ECL) bipolar random-access memory (RAM).

CAPACITY: From 1 million to 256 million words (8 million to 2 billion bytes). Please refer to Table 1 for the capacities of each model.

CYCLE TIME: See Table 1.

CHECKING: All Cray systems feature single error correction and double error detection codes. Eight check bits are added to each 64-bit data word before the data is written to memory. The check bits are generated as even parity bits for a specific group of data bits.

Cray Research Supercomputers

TABLE 1. SYSTEM COMPARISON (Continued)

MODEL	X-MP/28	X-MP/216	X-MP/48	X-MP/416	Cray-2
SYSTEM CHARACTERISTICS					
Date announced	September 1985	September 1985	1984	September 1985	June 1985
Date first delivered	3rd Quarter 1986	3rd Quarter 1986	—	4th Quarter 1986	4th Quarter 1985
Field upgradable to	X-MP/216	Not applicable	X-MP/416	Not applicable	Not applicable
Relative performance*	3.0 to 5.0	3.0 to 5.0	5.0 to 10.0	5.0 to 10.0	6.0 to 12.0
Number of processors	2	2	4	4	4
Cycle time, nanoseconds	9.5	9.5	9.5	9.5	4.1
Word size, bits	64	64	64	64	64
Operating systems	COS, Unicos	COS, Unicos	COS, Unicos	COS, Unicos	Unicos
MAIN MEMORY					
Type	MOS	MOS	ECL Bipolar	ECL Bipolar	MOS
Minimum capacity, bytes	64M	128M	64M	128M	2G
Maximum capacity, bytes	64M	128M	64M	128M	2G
Increment size, bytes	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Cycle time, nanoseconds	76	76	38	38	—
BUFFER STORAGE					
Minimum capacity	Not available	Not available	Not available	Not available	128KB
Maximum capacity	—	—	—	—	128KB
Increment size	—	—	—	—	Not applicable
INPUT/OUTPUT CONTROL					
Number of channels:					
Byte multiplexer	0	0	0	0	0
Block multiplexer	4 to 12 per XIOP	4 to 12 per XIOP	4 to 12 per XIOP	4 to 12 per XIOP	0
Word	0	0	0	0	0
Other	7	7	10	10	4

**Compared to a Cray-1.*

largest available memory size, offering 2 gigabytes of directly addressable memory. The Cray-2 includes 4 CPUs that Cray calls Background Processors, plus a Foreground Processor that supervises the Background Processors and all I/O operations. Four 4-gigabit communications channels connect the various components of the system. The Cray-2 offers a performance of 6 to 12 times that of a Cray-1.

The Cray-2 is designed around 3-dimensional logic modules that are immersed in an inert fluorocarbon cooling liquid. It is housed in a transparent cabinet that is arranged in an arc.

Peripherals for the Cray systems include the DD-39 and DD-49 disk subsystems and the Solid-State Storage Device (SSD). Both disk drive models provide 1.2 gigabytes of storage, but the DD-49 is a faster unit. The X-MP Series systems support up to 32 disk drives, while the Cray-2 supports up to 36. The SSD adds fast, random-access storage to the X-MP Series systems. Memory capacity is 256, 512, or 1,024 megabytes.

Cray now offers two operating systems: the original Cray Operating System (COS) and the new Unix-based Unicos operating system. Unicos was introduced for the Cray-2, but it can also be used with the X-MP Series systems. Both operating systems have been optimized to support the power of the Cray processors. The Cray systems support the Fortran, C, and Pascal programming languages. Various utilities are also available.

COMPETITIVE POSITION

Cray Research currently holds about 70 percent of the supercomputer market, a market that even Cray originally underestimated. The company states that at one time, it identified about 86 potential customers worldwide. With at least 115 systems currently installed at 79 customer sites, the company now feels that the potential is far greater.

RESERVED STORAGE: Not specified.

CENTRAL PROCESSORS

The *X-MP Series* consists of 9 models based on the same 9.5-nanosecond central processor. Cray uses high-speed 16-gate array integrated logic circuits with 300 to 400 picosecond propagation delays in the X-MP central processors. A basic X-MP system includes one or more central processors and an input/output (I/O) subsystem, supported by condensing units for refrigeration, motor generators for system power, and separate power distribution units for the CPU, I/O subsystem, and optional Solid-State Storage Device (SSD).

The X-MP central processors are organized into a control section and a computation section. The control section contains registers and instruction buffers for instruction issue and control. An exchange mechanism is used for switching instruction execution from program to program.

A 24-bit Program Address (P) register indicates the next parcel of program code to enter the Next Instruction Parcel (NIP) register. The 16-bit NIP register holds a parcel of code until it enters the Current Instruction Parcel (CIP) register, which holds the parcel waiting to issue for execution. If an instruction is 2 parcels long, the CIP register holds the first parcel and the Lower Instruction Parcel (LIP) register holds the second parcel.

Each X-MP CPU includes 4 instruction buffers, each with 128 sixteen-bit instruction parcels. Instruction parcels are held in the buffers before they are delivered to the NIP or CIP registers.

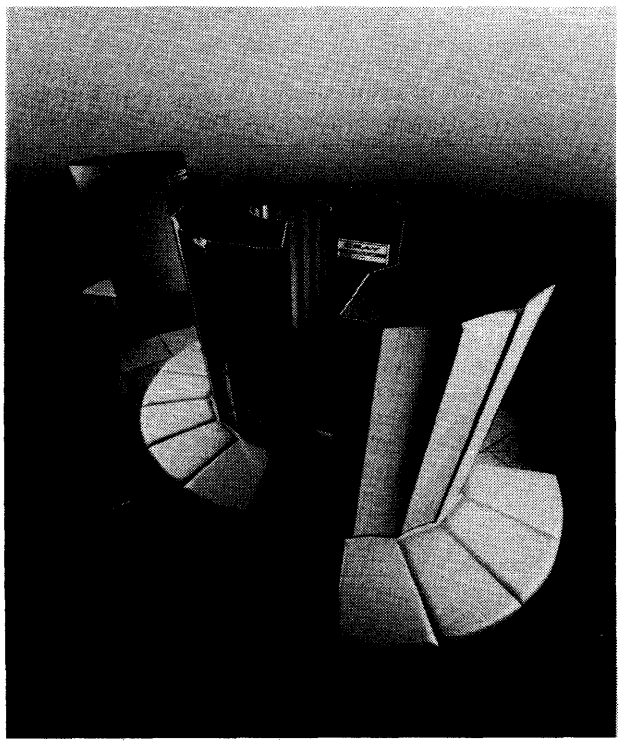
Associated with each program in the system is a 16-word block of data called an exchange package that contains the parameters used in executing the program. The exchange sequence causes program parameters for the next program to be exchanged with the current information in the operating registers. Exchange sequences may be initiated automatically during an interrupt condition or they may be initiated by the software.

Other control registers include the Instruction Base Address (IBA) register, which holds the base address of the user's

Cray Research Supercomputers

Many industry analysts share Cray's optimism about the supercomputer market. Some experts have predicted an annual growth rate of 60 percent through 1990. The increasing need for faster computation and the improved price/performance ratios of the newer supercomputers have spurred on this growth. Probably the biggest reason for the increased demand for supercomputers, though, is the acceptance of the use of simulation and modeling in place of physical experimentation. Many organizations are finding that it is more cost-effective to have a supercomputer simulate conditions in the real world than to conduct an actual experiment. For example, if simulations enable an oil company to avoid a few dry holes, the money saved may more than offset the cost of the supercomputer.

Some of the traditional mainframe vendors offer vector processing capabilities for their systems, but currently the only direct competition for the Cray systems is the Cyber 205, now marketed by ETA Systems, a Control Data spin-off. The Cyber 205, with a 20-nanosecond cycle time, is not as fast as the Cray systems. Control Data has installed about 33 Cyber 205s worldwide, so the system has not sold as well as the Cray models, either. However, ETA is reportedly working on a new system, the ETA^{10}, which will be much more powerful than the Cyber 205. The new system may offer more competition for Cray, but Cray isn't standing still, either. The Cray-3 is already under development, and so is an upgraded version of the X-MP Series.



The X-MP/4 systems include 4 central processors with 64 or 128 megabytes of main memory. In this photograph, the mainframe is in the center. To the left is the I/O subsystem and to the right is a Solid-State Storage Device.

instruction field; the Instruction Limit Address (ILA) register, which holds the limit address of the user's field; the Data Base Address (DBA) register, which holds the base address of the user's data field; and the Data Limit Address (DLA) register, which holds the upper limit address of the user's data field.

The computation section of the X-MP central processors comprises operating registers and functional units used for address, scalar, and vector processing. Address processing operates on internal control information such as addresses and indices, while scalar and vector processing operate on data. Data flow is from central memory to the operating registers and from the operating registers to the associated functional units. Results flow from the functional units to the registers and from the registers to central memory or back to the functional units.

Each X-MP computation section contains eight 24-bit Address (A) registers plus sixty-four 24-bit Intermediate Address (B) registers. The A registers are used for addressing and counting operations; the B registers perform the role of a data cache. There are eight 64-bit Scalar (S) registers that serve as the source and destination for operands that execute scalar arithmetic and logical instructions, plus sixty-four 64-bit Intermediate Scalar (T) registers that serve as a cache memory for the S registers. The X-MP systems contain eight 64-element (4096-bit) Vector (V) registers for vector processing. Successive elements from a V register enter a functional unit in successive clock periods. The effective length of a Vector register for any operation is controlled by a program-selectable Vector Length (VL) register. A Vector Mask (VM) register allows for the logical selection of particular elements of a vector.

The X-MP functional units are specialized hardware units that perform instructions other than simple transmit or control operations. Each CPU has four groups of functional units: address, scalar, vector, and floating-point. The address, scalar, and vector units act in conjunction with the address, scalar, and vector registers, respectively. The floating-point functional units support both scalar and vector operations. Each functional unit operates independently of the other units and implements algorithms for a specific portion of the instruction set. A functional unit operates in a fixed period of time called functional unit time. A new set of operands can enter a functional unit each clock period even though the functional unit time may be longer than one clock period. All functional units can operate concurrently.

There are 2 address functional units, the Address Add unit and the Address Multiply unit. The functional unit time is 2 clock periods for the Add unit and 4 clock periods for the Multiply unit.

The scalar functional units are as follows: the Scalar Add unit, the Scalar Shift unit, the Scalar Logical unit, and the Scalar Population/Parity/Leading Zero unit. The Scalar Add unit performs 64-bit integer addition and subtraction in a functional unit time of 3 clock periods. The Scalar Shift unit shifts the entire 64-bit contents of an S register or the 128-bit contents of 2 concatenated S registers. The functional unit time is 2 clock periods for single-shift instructions and 3 clock periods for double-shift instructions. The Scalar Logical unit performs bit-by-bit manipulation of 64-bit quantities obtained from S registers. The functional unit time is 1 clock period. The Scalar Population/Parity/Leading Zero unit performs various counting functions in 3 or 4 clock periods.

The X-MP processors have 5 vector functional units: Vector Add, Vector Shift, Full Vector Logical, Second Vector Logical, and Vector Population/Parity. The vector functional units are basically the same as their scalar counterparts, except that they perform vector operations using the V

Cray Research Supercomputers

New would-be competitors are entering the market at the low end. The new "minisupercomputers" have brought entry-level supercomputer performance to customers who could not yet justify a larger, more expensive system. The minisupercomputers have been dubbed "Crayettes," a clear indication that Cray is indeed the leader in the world of supercomputing. Although it is possible that Cray could lose some sales because customers choose the smaller, less expensive systems, it is just as likely that in the end Cray will benefit from the Crayettes. Once users get a taste of the power of even a small supercomputer, they may find more and more applications that need the additional power of a Cray. Thus far, Cray has stated that it intends to stick with the high end of the supercomputer industry.

ADVANTAGES AND RESTRICTIONS

The Cray X-MP Series and Cray-2 are very fast, powerful systems that are especially suited to computationally intensive scientific and engineering applications. All of the systems except the X-MP/1 are multiprocessor systems that offer multiprogramming and multitasking capabilities. All Cray systems perform both scalar and vector processing, and the Cray Fortran compiler automatically vectorizes codes as appropriate.

The Cray systems can be linked to a variety of general-purpose mainframes and minicomputers from such vendors as IBM, Control Data, Digital Equipment, Data General, Honeywell, and Sperry. The smaller systems serve as front-end computers to the larger Crays.

One possible disadvantage to the Cray systems is the lack of field upgradability. The uniprocessor X-MP/1 cannot be field upgraded to a dual-processor X-MP/2, nor can the X-MP/2 be field upgraded to an X-MP/4. None of the X-MP Series systems can be upgraded to a Cray-2. □

registers. The Second Vector Logical unit provides additional logic functions; it is mutually exclusive with the floating-point functional units. The functional unit times in clock periods for each vector unit are as follows: Vector Add, 3; Vector Shift, 3 or 4; Full Vector Logical, 2; Second Vector Logical, 4; Vector Population/Parity, 5.

There are 3 floating-point functional units: Floating-Point Add, Floating-Point Multiply, and Reciprocal Approximation. All 3 units operate on both S and V registers. The Floating-Point Add functional unit performs addition or subtraction of 64-bit operands in floating-point format. The functional unit time is 6 clock periods. The Floating-Point Multiply unit provides for full- and half-precision multiplication of 64-bit operands. The functional unit time is 7 clock periods. The Reciprocal Approximation unit finds the approximate reciprocal of a 64-bit operand in floating-point format. The functional unit time for this unit is 14 clock periods.

Data is referenced on a word basis; however, branch instructions reference parcels within words. The lower 2 bits of an address identify the location of an instruction parcel in a word. Depending on the model, the X-MP systems address from 21 to 24 bits in memory. Systems with 8 or 16 million words (64 or 128 megabytes) of memory feature an expanded addressing capability that uses 24-bit direct word addressing of data elements and 24-bit parcel addressing for instruction references.

Each multiprocessor X-MP system also includes an inter-CPU communication section that provides for a realtime clock and for communication and control among CPUs. There are 3 clusters of shared registers on X-MP/2 systems and 5 clusters on X-MP/4 systems. Each cluster of shared registers includes eight 24-bit Shared Address (SB) registers, eight 64-bit Shared Scalar (ST) registers, and thirty-two 1-bit Semaphore (SM) registers. Each central processor has a Cluster Number (CLN) register that determines which set of shared registers is accessed by a processor. The SB and ST registers pass address and scalar information from one central processor to another. Only one read or one write operation can occur during one clock period. The SM registers are used for control among the processors. Loading or reading the SM registers or setting or clearing an SM register can occur at any time from any or all CPUs. The test and set instruction is the only operation on the SM registers that includes a hardware interlock to prevent simultaneous access to the same SM register.

Under operating system control, a cluster of shared registers can be allocated to 0, 1, 2, 3, or 4 processors, depending upon the system configuration. The cluster may be accessed by any processor to which it is allocated in either user or system mode.

The X-MP systems contain one Realtime Clock (RTC) register that is shared by all central processors. Programs can be timed by using the clock period counter, which advances one count each 9.5-nanosecond clock period.

The X-MP systems also contain 8 performance monitors that track such hardware events as the number of specific instructions issued, hold issue conditions, and the number of fetches, I/O references, and vector references. The performance monitors allow users to select the events to be monitored, read the results into a scalar register, and test the operation of the performance counters.

The *Cray-2 Computer System* includes four 4.1-nanosecond central processors termed Background Processors, plus a Foreground Processor that controls and coordinates the data flow between the Common Memory, the Background Processors, and all peripheral devices. A maintenance control console provides for on-site maintenance of the system. The computer logic, memory, and DC power supplies are housed in one compact, circular cabinet. The Cray-2 uses 16-gate array logic chips packaged in 3-dimensional modules, which are cooled by liquid immersion cooling technology.

The 4 Background Processors operate independently on separate jobs or concurrently on the same job. Each Background Processor consists of a control section, a computation section, and a high-speed Local Memory. The control section contains registers and instruction buffers for instruction issue and control. The computation section contains registers and functional units that work together to execute instructions stored in memory. The Local Memory is used to temporarily store scalar and vector data during computations.

Each Cray-2 control section contains a 32-bit Program Address (P) register that indicates the address of the program instruction parcel currently awaiting issue. The Foreground Processor loads the P register with data at the beginning of the computational period. As each parcel issues from the instruction queue, the content of the P register advances by 1.

Each Background Processor includes an instruction buffer with 8 independent fields that allow program loops to execute without additional references to memory. Programs can loop within the buffer by using any of the branch instructions. Each independent field contains 16 words (128 bytes), for a total instruction buffer size of 128 words (1024 bytes).

Cray Research Supercomputers

TABLE 2. MASS STORAGE

MODEL	DD-39 Disk Storage Unit	DD-49 Disk Storage Unit
Cabinets per subsystem	Up to 4	Up to 4
Disk packs/HDAs per cabinet	3	1
Capacity	1.2 gigabytes	1.2 gigabytes
Tracks/segments per drive unit	12,600	7,088
Average seek time, msec.	18	16
Average access time, msec.	—	—
Average rotational delay, msec.	—	—
Data transfer rate	5.9M bytes/sec. at user job level	9.8M bytes/sec. at user job level
Controller model	DCU-5	DCU-5
Comments	For use on the X-MP/1, which supports up to 32 disk storage units.	Designed for X-MP/2, X-MP/4, and Cray-2. The X-MP systems support up to 32 disk storage units; the Cray-2, up to 36.

The next sequential instruction or a branch out of the instruction buffer discards the oldest data field and replaces it with 16 words of new data.

The Cray-2 Background Processors also contain a 32-bit Base Address (BA) register and a 32-bit Limit Address (LA) register. The BA register defines the lower boundary of the memory address, while the LA register defines the upper boundary. Eight semaphore flags are provided to synchronize references to Common Memory when 2 or more Background Processors are executing a single job. One semaphore flag is assigned to each currently active job in the background system. When a Background Processor is assigned to a job, it is also assigned a semaphore flag.

The computation section in each Background Processor contains operating registers and functional units that perform the arithmetic and logic operations for the Cray-2 system. The Cray-2 includes 3 types of operating registers: eight 32-bit Address (A) registers, eight 64-bit Scalar (S) registers, and eight 64-element Vector (V) registers with 64 bits per element. The A registers calculate memory locations for Local Memory and Common Memory references, and are used for 32-bit integer calculations and for moving data directly from Local Memory. The S registers are used for operands executing scalar arithmetic and logical instructions; they can also furnish one operand in vector instructions. The V registers are the primary computational registers in the Cray-2 system. The length of each vector to be processed is set in the 6-bit Vector Length (VL) register. The 64-bit Vector Mask (VM) register provides for the implementation of vector branch operations.

The Cray-2 functional units receive operands from registers and deliver the result to a register when the function has been performed. Each Background Processor contains the following functional units: Address Add, Address Multiply, Scalar Integer, Scalar Shift, Scalar Logical, Vector Integer, Vector Logical, Floating-Point Add, and Floating-Point Multiply. In addition, the Background Processors contain the Local Memory that serves as a buffer for the data in the A, S, and V registers.

The Address Add and Address Multiply functional units perform 32-bit integer addition, subtraction, and multiplication of two A register operands. The units can accept address operands as fast as the instructions can issue.

The Scalar Integer functional unit performs 64-bit integer addition and subtraction of S register operands, as well as population count, population count parity, and leading zero. The Scalar Shift functional unit shifts the entire 64-bit contents of an S register or the double 128-bit contents of 2 concatenated S registers. The Scalar Logical functional unit manipulates bit-by-bit the 64-bit quantities obtained from the S registers. In all scalar functional units, scalar operands are accepted as fast as the instructions can issue.

The Vector Integer functional unit performs vector shifts, vector integer arithmetic, vector population count, vector leading zero count, and compressed iota. The Vector Logical functional unit manipulates bit-by-bit the 64-bit quantities from two V registers or from V and S registers. Both vector functional units can accept operands each clock period and, after a transmit time delay, deliver a result each clock period.

The Floating-Point Add functional unit performs addition and subtraction of 64-bit operands in floating-point format for both scalar and vector operations. The unit also performs conversion between integer and floating-point arithmetic. The Floating-Point Multiply functional unit performs full multiplication of 64-bit operands in floating-point format on both scalar and vector operations. It also performs reciprocal approximation, reciprocal square root approximation, reciprocal iteration, and reciprocal square root iteration. Both floating-point functional units are reserved for the time of a vector stream during execution of vector addition instructions. The units can accept vector operand data each clock period and, after a transmit time delay, deliver a result each clock period. Scalar references are accepted as fast as they issue if the unit is not processing vector data.

Each Cray-2 Background Processor includes 16K words (128K bytes) of Local Memory that takes the place of the B and T registers found in the X-MP systems. The access time for Local Memory is 4 clock periods. Accesses to Local Memory can overlap accesses to Common Memory. The Local Memory can store scalar or vector operands during computation.

Each Background Processor also contains a 64-bit Realtime Clock register that counts continuously at the clock period rate of 4.1 nanoseconds. The clocks in all 4 Background Processors are synchronized at deadstart.

SPECIAL FEATURES: All Cray supercomputers perform vector processing as well as scalar processing. All systems have 8 vector registers, which are associated with vector functional units as described above. Working in conjunction with the hardware, the Cray Fortran compiler automatically vectorizes inner DO loops, unless instructed not to do so. In general, vector loops are faster than scalar loops, but more preparation time is needed for vector registers, so DO loops executed a few times may actually be executed faster in scalar mode.

The Cray systems include a full indexing capability that allows matrix operations in vector mode to be performed on rows, columns, diagonals, and any set of data that is stored

Cray Research Supercomputers

in memory with regular spacing between elements. The gather/scatter instructions allow a vector of indices to be used to reference a random pattern of data in memory. The systems can also generate a compressed index that contains only those items that correspond to some testable condition.

PHYSICAL SPECIFICATIONS: All Cray computers are compact systems made up of vertical columns arranged in an arc. The X-MP/1 consists of 6 vertical columns arranged in a 135-degree arc that occupies 32 square feet of floor space. The X-MP/2 system is composed of 8 vertical columns arranged in a 180-degree arc occupying 43 square feet of floor space. The X-MP/4 models consist of 12 vertical columns in a 270-degree arc that takes up 64 square feet of space. The X-MP Series mainframes weigh approximately 11,300 pounds. The systems use 400-hertz power from motor generators. Power supplies are located in bench-like projections at the base of the columns. The X-MP I/O Subsystem (IOS) resides in 4 vertical columns arranged in a 90-degree arc that occupies 24 square feet of floor space. The IOS can be located up to 19 feet from the mainframe.

The Cray-2 consists of 14 columns arranged in a 300-degree arc occupying 16 square feet of floor space. The Cray-2 is 45 inches high, measures 53 inches in diameter, and weighs 5,500 pounds. The system uses 400-hertz power from motor generators.

CONFIGURATION RULES

The X-MP Series systems are available in 9 models that differ primarily in the number of central processors and the amount of main memory supplied with each system. The X-MP/1 models have one central processor. The X-MP/11 includes 1 million words (8 megabytes) of main memory, the X-MP/12 includes 2 million words (16 megabytes) of memory, the X-MP/14 includes 4 million words (32 megabytes) of memory, and the X-MP/18 includes 8 million words (64 megabytes) of memory. All X-MP/1 models can have 2, 3, or 4 I/O Processors (IOPs) and from 4 to 7 I/O channels. Memory upgrades are available to upgrade an X-MP/11 to an X-MP/12, et cetera, but the X-MP/1 cannot be field upgraded to an X-MP/2 or X-MP/4.

The X-MP/2 models are dual-processor systems. The X-MP/24 includes 4 million words (32 megabytes) of shared main memory, the X-MP/28 contains 8 million words (64 megabytes) of memory, and the X-MP/216 includes 16 million words (128 megabytes) of memory. The X-MP/2 systems support 2, 3, or 4 IOPs and 7 I/O channels. As with the X-MP/1 systems, memory upgrades are available for the X-MP/2 models, but an X-MP/2 system cannot be field upgraded to an X-MP/4 system.

The X-MP/4 systems contain 4 central processors. The X-MP/48 includes 8 million words (64 megabytes) of main memory, and the X-MP/416 includes 16 million words (128 megabytes) of memory. Both models support 4 IOPs and 10 I/O channels. The X-MP/48 can be upgraded to an X-MP/416 with the addition of the required main memory. However, the X-MP/4 systems cannot be field upgraded to a Cray-2.

The Cray-2 is equipped with 4 central processors called Background Processors, 256 million words (2 billion bytes) of Common (main) Memory, and a Foreground Processor that supervises the Background Processors and all I/O operations. The Cray-2 includes 4 high-speed channels.

INPUT/OUTPUT CONTROL

The X-MP Series I/O Subsystem (IOS) is housed in a separate cabinet and is shared by all CPUs on the system. The IOS has a buffer memory, available in 32-megabyte and 64-megabyte versions, that is shared by all I/O Processors (IOPs). The IOS provides fast data transfer between its buffer memory and the system's main memory, front-end computers, disk storage devices, and other peripheral devices.

The X-MP systems support 3 types of channels, operating at 6 megabytes, 100 megabytes, or 1250 megabytes per second. The X-MP/1 models include two or four 6-megabyte channels, one or two 100-megabyte channels, and one 1250-megabyte channel. The X-MP/2 systems have four 6-megabyte channels, two 100-megabyte channels, and one 1250-megabyte channel. On the X-MP/4, there are four 6-megabyte channels, four 100-megabyte channels, and two 1250-megabyte channels.

The X-MP I/O Subsystem supports 4 types of IOPs: a Master IOP (MIOP), a Buffer IOP (BIOP), a Disk IOP (DIOP), and an auxiliary IOP (XIOP). All IOSs must include at least one MIOP and one BIOP. The number of DIOPs and XIOPs is installation-dependent. Each IOP has a local memory section, a control section, a computation section, and an I/O section. Each IOP also has 6 direct memory access (DMA) ports to its local memory.

The MIOP connects to the mainframe over a 6-megabyte-per-second channel pair. One DMA port connects to buffer memory. The MIOP also controls the front-end interfaces and station peripherals. (See the Communications section for a description of the front-end interfaces.)

The BIOP serves as the main link between the central processors' main memory and the mass storage devices. Data from mass storage devices is transferred through the BIOP's local memory to the system's main memory over a 100-megabyte-per-second channel pair.

The DIOP is used for additional disk storage units. Up to 4 disk controllers with up to 16 disk drives are supported. Each IOS supports a maximum of 32 disk drives. The DIOP uses one DMA port for each controller, one DMA port to connect to buffer memory, and one DMA port to connect the 100-megabyte channel pair to the mainframe's main memory.

The XIOP is used for multiplexer channels. It interfaces to a maximum of 3 block multiplexer controllers supporting up to 4 block multiplexer channels each. Up to 48 magnetic tape units can be connected to the block multiplexer channels. The XIOP uses one DMA port for each controller and one to connect with the buffer memory.

The 1250-megabyte channels are used to connect the Solid-State Storage Device (SSD) to the central processor. The SSD can also be directly connected to the IOS via a 100-megabyte channel.

The X-MP IOS permits simultaneous data transfers between the MIOP, BIOP, DIOP, or XIOP and the system's main memory.

On the Cray-2, I/O operations are controlled by the Foreground Processor, which is connected to four 4-gigabit communications channels. Each channel connects to one Background Processor port, one group of peripheral controllers, one Common Memory port, and the Foreground Processor. Each channel supports up to 4 front-end interfaces.

The communications channels interconnect the Foreground Processor, disk controllers, front-end interfaces, Background Processor port, and Common Memory port in a continuous channel loop. Each member of the loop is called a channel node. Each channel node receives data during each clock period and transmits that data to the next node during the next clock period.

Cray Research Supercomputers

The Cray-2 supports up to 40 I/O devices, including a maximum of 36 disk storage units. Disk controllers are usually divided equally among the channels. The disk units can be addressed individually, or they can operate synchronously with all disks running in parallel in a lockstep mode.

MASS STORAGE

Disk subsystems provided by Cray are listed in Table 2.

Cray also offers the Solid-State Storage Device (SSD) for the X-MP systems. The SSD incorporates high-density MOS memory, but it is used much like a conventional disk subsystem. Datasets are logically identical to those on disk storage, and no programming changes are required to access the SSD.

The SSD provides 256, 512, or 1024 megabytes of storage. Since the unit is not constrained by seek and latency delays, the access time is essentially zero. The SSD connects to the 1000-megabyte-per-second channels on the X-MP systems. It can also connect directly to the I/O Subsystem on the 100-megabyte channels, thus bypassing main memory.

The SSD is housed in 4 columns arranged in a 90-degree arc. It requires 24 square feet of floor space.

INPUT/OUTPUT UNITS

Cray does not provide its own magnetic tape drives and printers. However, the Cray systems support IBM 3420 and 3480 tape subsystems.

TERMINALS

Terminals are not available from Cray.

COMMUNICATIONS

All Cray systems can be interfaced to front-end computers to form a network. The front-end computers are self-contained systems that operate under the control of their own operating system. Computers from IBM, Control Data Corporation, Data General, Digital Equipment Corporation, Honeywell, and Sperry can serve as a front end to a Cray system. The Cray systems can also be connected to Apollo and Sun workstations via Network Systems Corporation (NSC) network adapters.

The front-end computer interfaces are housed in a separate cabinet located near the Cray host computer. The front-end system can serve the Cray system as a master operator station, a local operator station, a local batch entry station, a remote batch entry station, a data concentrator for multiplexing several other stations into a single Cray channel, or an interactive communication station.

SOFTWARE

OPERATING SYSTEM: The X-MP systems run under the *Cray Operating System (COS)*, which was developed for the Cray-1. The X-MP processors also support the new Unicos operating system announced with the Cray-2. Unicos is described below.

COS is a multiprogramming, multiprocessing, multitasking operating system that monitors and controls the flow of work presented to the X-MP system in the form of jobs. Multitasking enables a program to be partitioned into separate tasks that can execute in parallel on a multiprocessor system. The operating system optimizes resource usage and resolves conflicts when more than one job needs resources. Jobs are presented to the Cray system by one or more front-end computers, or stations, which run under the control of their own operating systems. COS includes links for the initiation and control of interactive jobs and the transfer of data between the Cray system and the front-end system.

COS is loaded into central memory and activated through a system start-up procedure performed at the I/O Subsystem. Nearly all information maintained by COS is organized into quantities of information known as datasets that reside in memory, on mass storage, or on magnetic tape drives. At start-up, linkage to the Permanent Dataset Catalog (DSC) is reestablished on mass storage. All permanent mass storage datasets are recorded in the DSC.

Central memory is shared by COS, jobs running on the Cray mainframe, dataset I/O buffers, and system tables associated with the jobs. COS allocates resources to each job, as needed, when the resources become available.

COS occupies 2 areas of main memory. The Exchange Packages, the System Executive, the System Task Processor, and, optionally, the Control Statement Processor reside in the lower portion of memory. The station I/O buffers, the system log buffer, and the DSC information and buffers reside in the upper portion of memory.

Every job is assigned to a user area in memory that consists of a Job Table Area (JTA) and a user field. The JTA contains the parameters and information required for monitoring and managing the job. The JTA is not accessible to the user. The user field is a block of memory immediately following the job's JTA. It is always a multiple of 512 words. The beginning or base address and the end or limit address of the user field are set by the operating system. The maximum user field size is set by parameters on one of the job control statements or by installation-defined default.

Compilers, assemblers, system utility programs, and user programs are loaded from mass storage into the user field and are executed in response to control statements on the job deck.

The *Unicos Operating System*, which is based on AT&T's Unix System V, was introduced for the Cray-2, but it is also available for the X-MP Series. Like Unix, Unicos is written in C language and contains a kernel and a set of utilities and programs. The kernel supports a small number of system call primitives that library and application programs can use to perform more complex tasks. The kernel is procedure-oriented and includes many processes that dynamically share a common data area used to control the Cray system. The operating system is oriented toward an interactive environment with a hierarchical file structure featuring directories, user ownership, and file protection. A batch processing capability is also provided.

The Unicos kernel has been enhanced to support the computational power of the Cray-2 system. Enhancements have been made in I/O processing, the use of very large data files, support for asynchronous I/O, improved file system reliability, and support for multiprocessing and multitasking. Users can initiate asynchronous processes to communicate with one another and to pass data among them. A variety of command structures, or shells, are possible. Unicos provides a standard shell, but others can be created. The user interface to the multitasking capability is through a set of Fortran-callable library routines.

PROGRAMMING LANGUAGES: The following languages are supported on all Cray systems: Cray Assembler Language (CAL), ANSI X3.9-1978 Fortran, and C. The X-MP Series also supports ISO Level 1 Pascal.

Cray Research Supercomputers

DATA BASE MANAGEMENT: Not available from Cray.

DATA MANAGEMENT: Not available from Cray.

DATA COMMUNICATIONS: In addition to the hardware interfaces to front-end systems, Cray offers station software that provides a connection between its computers and those of other vendors. Cray software is available for the IBM MVS and VM, Control Data NOS and NOS/BE, Digital Equipment VAX/VMS, Data General RDOS, and AT&T Unix operating systems. Station software for Honeywell and Sperry operating systems is available from third-party sources.

The Cray MVS and Cray VM Station Software Services enable IBM MVS and VM users to take advantage of the processing power of the Cray supercomputers by connecting the IBM operating systems with the Cray operating system. The MVS and VM Station Software Services provide the following capabilities to the IBM user: submission of jobs to the Cray system, dataset transfer between the IBM and Cray systems, monitoring and control of Cray jobs, interactive execution of Cray JCL statements and procedures, provision of user exits to meet specific user requirements, and, for VM users only, direct data transfer from the Cray operating system file base to VM user memory.

The Superlink Integrated Support Processor enables Cray Fortran users to have record-level access to data on an IBM MVS system. A Cray Fortran program may read and write IBM dataset records as if the IBM dataset were resident on the Cray.

Cray also offers the Apollo Station Software Service, which provides for communications between Apollo Domain workstations and a Cray system. The Apollo software includes a subset of the Apollo graphics primitives as Fortran-callable routines residing in a library on the Cray, as well as a graphics library residing on the Apollo. A dataset staging feature permits jobs running on the Cray to access and create files on the Apollo. Both interactive and batch processing are supported. A Cray system can be connected to a variety of Apollo Domain configurations by using the Network Systems Corporation (NSC) Hyperchannel.

PROGRAM DEVELOPMENT: Program development facilities are provided by the Unicos operating system.

UTILITIES: A variety of utility programs are available for the X-MP Series systems, including a text editor, symbolic interactive debug package, segment loader, sort package, and a number of dataset utilities. For the Cray-2, a set of operational support facilities are provided for proper system management, and software tools for efficient system use support both interactive and batch processing.

OTHER SOFTWARE: A wide variety of third-party application programs were developed for the Cray-1, many of which have been adapted for the newer X-MP Series and the Cray-2. Applications include fluid dynamics, mechanical engineering, nuclear safety, circuit design, seismic processing, image processing, molecular modeling, and artificial intelligence.

PRICING AND SUPPORT

POLICY: The Cray X-MP Series and Cray-2 are available for purchase or on a 1-year or 3-year lease. The accompanying price list includes purchase prices only; contact Cray for lease charges and for maintenance service prices.

SUPPORT: Cray provides preinstallation site planning and on-going, on-site engineering and software support. Additional assistance is available from technical centers throughout the United States. Preventive maintenance identifies potential problems. Diagnostics can be invoked locally at the customer's site or remotely by Cray technical support personnel. Cray's philosophy is to repair and replace modules on-site to keep downtime to a minimum.

EDUCATION: Training is available at the customer's site or at Cray's training facilities.

TYPICAL CONFIGURATION: Because Cray does not sell a full line of peripherals and communications equipment, we have not included typical configuration prices.

Cray Research Supercomputers

EQUIPMENT PRICES

		Purchase Price ($)
PROCESSORS		
X-MP/11	Basic system; includes one CPU, 1M words (8M bytes) of memory, I/O processor, motor generator, condensing unit, power distribution unit, COS operating system, utilities, and Fortran, C, and Pascal compilers	5,000,000
X-MP/12	Same components as X-MP/11, but with 2M words (16M bytes) of memory	6,000,000
X-MP/14	Same components as X-MP/11, but with 4M words (32M bytes) of memory	7,000,000
X-MP/18	Same components as X-MP/11, but with 8M words (64M bytes) of memory	8,000,000
X-MP/24	Basic system; includes two CPUs, 4M words (32M bytes) of memory, I/O processor, motor generator, condensing unit, power distribution unit, COS operating system, utilities, and Fortran, C, and Pascal compilers	8,500,000
X-MP/28	Same components as X-MP/24, but with 8M words (64M bytes) of memory	9,500,000
X-MP/216	Same components as X-MP/24, but with 16M words (128M bytes) of memory	11,500,000
X-MP/48	Basic system; includes four CPUs, 8M words (64M bytes) of memory, I/O processor, motor generator, condensing unit, power distribution unit, COS operating system, utilities, and Fortran, C, and Pascal compilers	14,000,000
X-MP/416	Same components as X-MP/48, but with 16M words (128M bytes) of memory	16,000,000
Cray-2	Basic system; includes one Foreground Processor and four Background Processors, 256M words (2G bytes) of common memory, maintenance control console, Unicos operating system, utilities, CAL assembler, Fortran and C compilers, and multitasking libraries	17,600,000
	I/O Subsystem Buffer Upgrade; from 32MB to 64MB	75,000
MASS STORAGE		
DD-39	Disk Storage Unit for X-MP/1 systems; 1.2 gigabytes	100,000
DD-49	Disk Storage Unit for X-MP/2, X-MP/4, and Cray-2; 1.2 gigabytes	125,000
DCU-5	Disk Control Unit for DD-39 and DD-49	60,000
SSD	Solid-State Storage Device; 256MB	2,000,000
SSD	Solid-State Storage Device; 512MB	3,000,000
SSD	Solid-State Storage Device; 1024MB	4,000,000 ■

Cray Research Supercomputers

Product Enhancement

Recent enhancements to the Cray product line include improved performance of the X-MP Series, the addition of two new models to the X-MP family, reduced prices on all single-processor and dual-processor X-MP models, and a fiber optic link for connecting other manufacturers' computers to a Cray system. In addition, Cray introduced two high-capacity Solid-State Storage Device (SSD) models and reduced prices on the previous SSD models.

The overall performance of the X-MP Series processors has been improved by speeding up the cycle time. All new X-MP Series processors will have an 8.5-nanosecond clock period, compared to the 9.5-nanosecond clock period of the previous models. According to Cray, existing user programs can run on the faster processors without modification.

Entry-level models were added to the X-MP/2 and X-MP/4 series. The new X-MP/22 is a dual-processor system with 2 million words (16 million bytes) of main memory. The new X-MP/44 system includes 4 central processors and 4 million words (32 million bytes) of main memory. Previously, the minimum X-MP/2 system had 4 million words of memory, and the minimum X-MP/4 system had 8 million words.

Cray has reduced the purchase prices of all X-MP/1 and X-MP/2 models by $500,000 to $1,000,000. Current prices are listed in the price list below. Prices for the X-MP/48 and X-MP/416 have not changed.

The new SSD models include two and four gigabytes of RAM. The previous maximum was one gigabyte. Purchase prices for other models were reduced from 25 to 33 percent. The latest prices are listed below.

Cray also announced a new 3-megabyte-per-second fiber optic link that allows a front-end system connected to a Cray system to be located as much as 0.621 mile (one kilometer) away. Previously, the systems could not be located more than 450 feet (137 meters) from each other.

EQUIPMENT PRICES

		Purchase Price ($)
PROCESSORS		
X-MP/11	Basic system; includes one CPU, 1M words (8M bytes) of memory, I/O processor, motor generator, condensing unit, power distribution unit, COS operating system, utilities, and Fortran, C, and Pascal compilers	4,000,000
X-MP/12	Same components as X-MP/11, but with 2M words (16M bytes) of memory	5,000,000
X-MP/14	Same components as X-MP/11, but with 4M words (32M bytes) of memory	6,000,000
X-MP/18	Same components as X-MP/11, but with 8M words (64M bytes) of memory	7,000,000
X-MP/22	Basic system; includes two CPUs, 2M words (16M bytes) of memory, I/O processor, motor generator, condensing unit, power distribution unit, COS operating system, utilities, and Fortran, C, and Pascal compilers	7,000,000
X-MP/24	Same components as X-MP/22, but with 4M words (32M bytes) of memory	8,000,000
X-MP/28	Same components as X-MP/22, but with 8M words (64M bytes) of memory	9,000,000
X-MP/216	Same components as X-MP/22, but with 16M words (128M bytes) of memory	10,500,000
X-MP/44	Basic system; includes four CPUs, 4M words (32M bytes) of memory, I/O processor, motor generator, condensing unit, power distribution unit, COS operating system, utilities, and Fortran, C, and Pascal compilers	12,000,000
X-MP/48	Same components as X-MP/44, but with 8M words (64M bytes) of memory	14,000,000
X-MP/416	Same components as X-MP/44, but with 16M words (128M bytes) of memory	16,000,000
MASS STORAGE		
SSD	Solid-State Storage Device; 256MB	750,000
SSD	Solid-State Storage Device; 512MB	2,000,000
SSD	Solid-State Storage Device; 1024MB	3,000,000
SSD	Solid-State Storage Device; 2048MB	4,000,000
SSD	Solid-State Storage Device; 4096MB	6,000,000 □