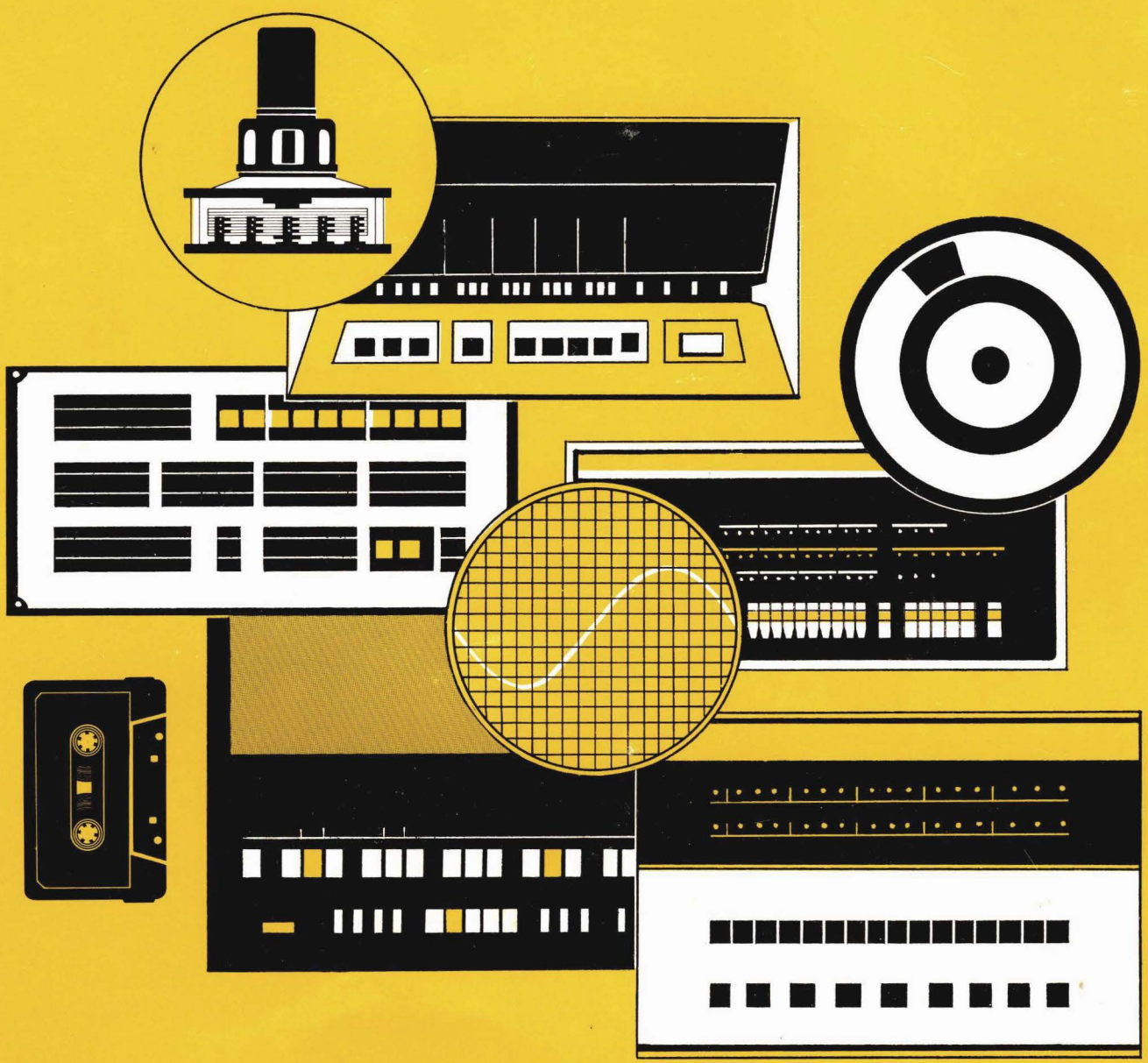
DATUM

PERIPHERAL EQUIPMENT
DIVISION

INSTRUCTION MANUAL

MODEL 5094-101
TWO-PORT
MULTIPLEXER

PUBLICATION NO. 1802.3



PERIPHERAL EQUIPMENT
DIVISION

INSTRUCTION MANUAL

MODEL 5094-101
TWO-PORT
MULTIPLEXER

PUBLICATION NO. 1802.3

SEPTEMBER 1974

DATUM INC.
1363 South State College Boulevard
Anaheim, California 92806

TABLE OF CONTENTS

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This technical manual contains operating, installation, and maintenance information for the DATUM Model 5094-101 Multiplexer. The manual is organized in five sections. Section I contains general physical and functional information, Section II contains information for installing and operating the Multiplexer, and Section III includes Multiplexer theory at the block diagram and logic level. Sections IV and V, respectively, contain maintenance information and the reference drawings.

1.2 PURPOSE OF EQUIPMENT

The Model 5094-101 Multiplexer allows the connection of two peripheral devices to the IBM 1130 SAC channel. A typical application would be the connection of a magnetic tape system and a high-speed line printer to the IBM 1130.

1.3 PHYSICAL DESCRIPTION

The Multiplexer (Drawing 5094-101) consists of a printed circuit card and a power supply mounted in a 19" x 3.5" x 13" box. The box is furnished with standard RETMA hole spacing for the 3.5" high front panel. The front panel contains the power on-off pushbutton, and the

rear panel contains the connectors for interfacing the computer and peripheral devices.

1.4 FUNCTIONAL DESCRIPTION

The Model 5094-101 Multiplexer receives and repowers all the signals to and from the computer and peripheral devices. It controls and determines the priority of the cycle steal operations of the two peripheral devices. Connectors J102 and J103 are identical to the IBM SAC channel.

SECTION II

INSTALLATION AND OPERATION

2.1 GENERAL

This section of the manual describes the installation and operation of the Model 5094-101 Multiplexer.

2.2 INSTALLATION

The Multiplexer is shipped fully assembled and ready for operation. No assembly is required other than connection of the Multiplexer to a source of AC power and connection of the computer and peripheral device interface cables.

2.2.1 Power

The Multiplexer operates on 120/230-volt, 60 Hz, single-phase power. Connect the AC source to the Hubbel connector provided on the rear panel of the Multiplexer. Ensure that a 2-ampere Slo-Blo fuse is installed in the fuse socket.

2.2.2 Interface Connectors

The functions of the interface connectors located at the rear of the Multiplexer are listed in Table 2.1.

The signal cable from the IBM 1130 SAC channel is plugged into connector J101.

The signal cable from the higher priority device connects to J102, and the signal cable from the lower priority device connects to J103.

2.3 OPERATION

If only one device is to be operated, the connector for the second device must be left open. It makes no difference which connector is used for a single device.

Table 2.1. Interface Connector Functions

CONNECTOR	FUNCTION
J101	Interface to the computer
J102	Channel '1' — highest priority
J103	Channel '2' — lowest priority

SECTION III

THEORY OF OPERATION

3.1 GENERAL

The theory of operation describes the detailed functions of the Model 5094-101 Multiplexer. The descriptions begin at the block diagram level and then proceed through descriptions of the logic diagram.

3.2 BLOCK DIAGRAM DESCRIPTION (DRAWING 800526)

The block diagram shows the flow of the data to and from the computer and peripheral devices. The arrows show the direction of the data flow.

The sheet numbers shown in each box refer to the sheet numbers of Drawing 76085 where that particular logic is shown.

The control lines (out of the control logic) which control some of the gating functions are now shown.

The block diagram shows the IBM 1130 SAC channel on the right-hand side of the drawing; the two peripheral devices are shown on the left-hand side. The SAC Device #1 is the higher priority device.

3.3 LOGIC DESCRIPTION

3.3.1 Control Logic (76085, Sheet 1)

This logic handles the priority of the cycle steal requests from the two peripheral devices.

Flip-flop REQ is the channel cycle steal request. B is used to synchronize the incoming cycle steal request with the phase A signal from the computer when the computer is in the wait mode and no T clocks are available. SEL1 determines which device is to be serviced.

3.3.2 Data Input Bus (76085, Sheet 2)

This logic receives the 16-bit data words from the two peripheral devices and OR's them to drive the data input bus of the SAC channel.

3.3.3 Address Bus (76085, Sheet 3)

This logic receives the 16-bit address words from the two peripheral devices and gates one of them, depending on which is being serviced at the time, out onto the address bus of the SAC channel.

3.3.4 Data Output Bus (76085, Sheet 4)

This logic receives the 16-bit data word from the SAC channel and repowers it for the two peripheral devices.

3.3.5 Control Signals Repowering (76085, Sheets 5 and 6)

This logic receives the control signals from the SAC channel and repowers them for the two peripheral devices.

3.4 LOGIC ELEMENTS

All logic elements are Signetics TTL or Utilogic integrated circuits in dual-inline packages. Logic diagrams for these elements can be found at the back of this section.

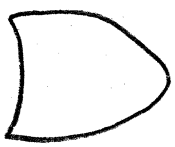
The logic elements are mounted in wire-wrap sockets on printed circuit cards. All circuit interconnections are made by wire-wrap connections. Circuit elements are easily replaceable by removing them from their sockets and replacing them with equivalent elements.

Integrated circuits are used throughout wherever possible. Exceptions are relay and lamp drivers.

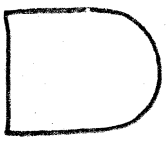
3.5 LOGIC SYMBOLS

The logic symbols are derived from MIL-STD-806B, and they are utilized in such a manner that signals can be traced through the logic in terms of "high" and "low" (+2.5 to +5V) and (0V) by examination of the logic symbols without the need to memorize the electrical characteristics (NAND, NOR, AND, OR, etc.) of the circuits (which most other logic drawing schemes require).

The "high" and "low" signal level indication is illustrated by a straight line for a "high" signal and a small circle for a "low" signal level. The following symbol shapes are used:



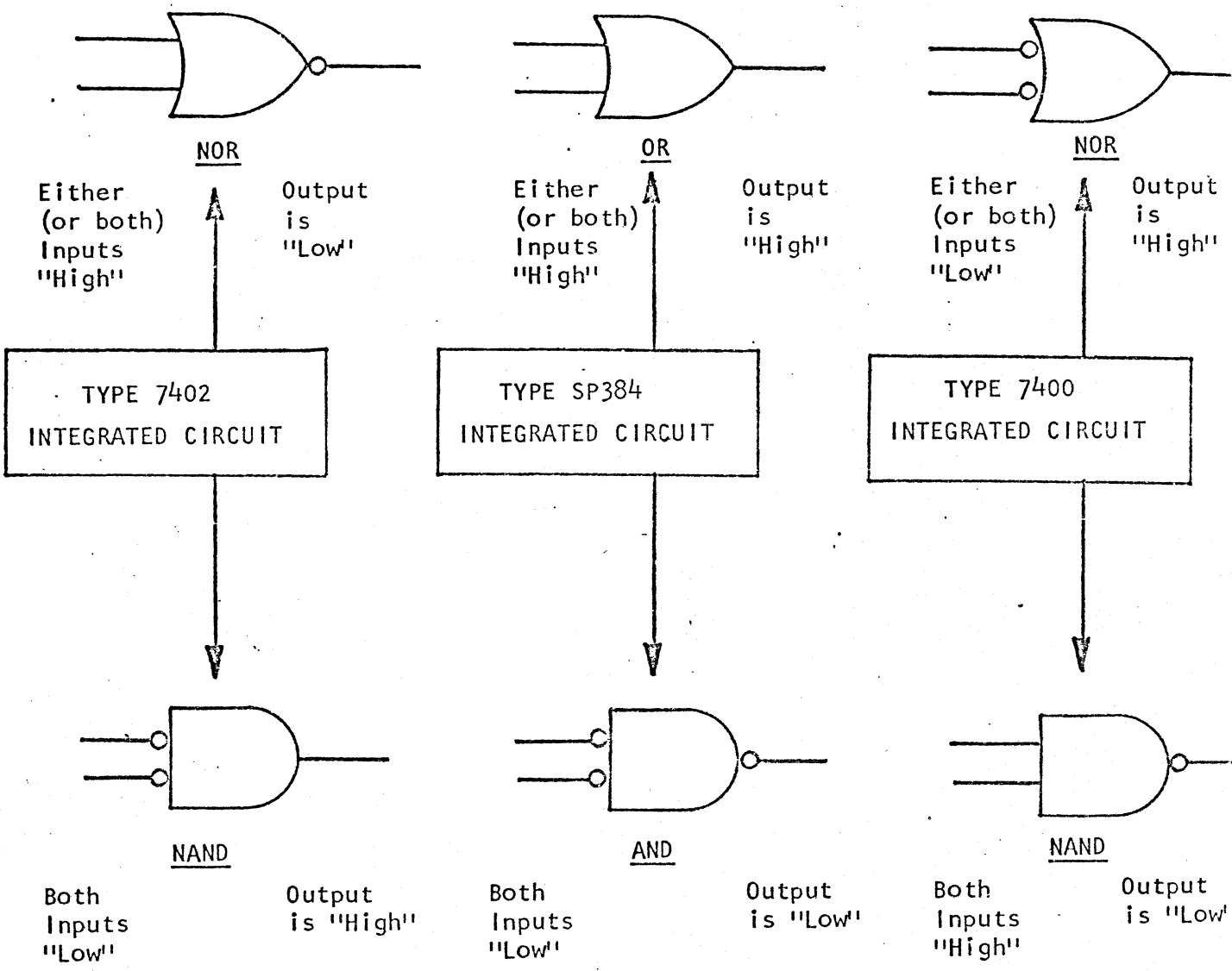
"OR" SYMBOL



"AND" SYMBOL

The use of straight lines or circles at inputs and outputs of these basic symbols completely defines the function the circuit performs, the input signal levels required to activate the circuit, and the output signal level when the circuit is activated.

Some examples follow:

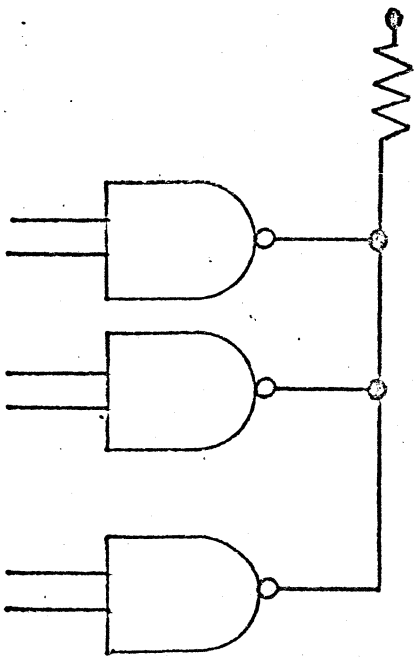


Note that the Type 7402 integrated circuit can be used as a "high" input NOR or a "low" input NAND.

Note also that the Type 7400 integrated circuit can be used as a "low" input NOR or a "high" input NAND.

Note that the Type SP 384 integrated circuit can be used as a "high" input OR or a "low" input AND.

A "low wired OR" or a "high wired AND" function can also be implemented with certain integrated circuits by tying the outputs together and adding an external discrete resistor "pull up."



+5

"Pull Up" Resistor

1. <u>"Low Wired OR"</u>

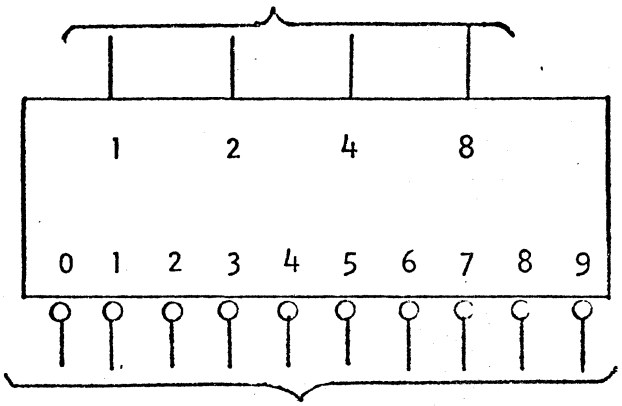
   (Any NAND gate output goes "low" the bus goes "low.")

2. <u>"High Wired AND"</u>

   <u>All</u> NAND gate outputs must be "high" in order for the bus to be "high."

Four-To-Ten-Line Decoder

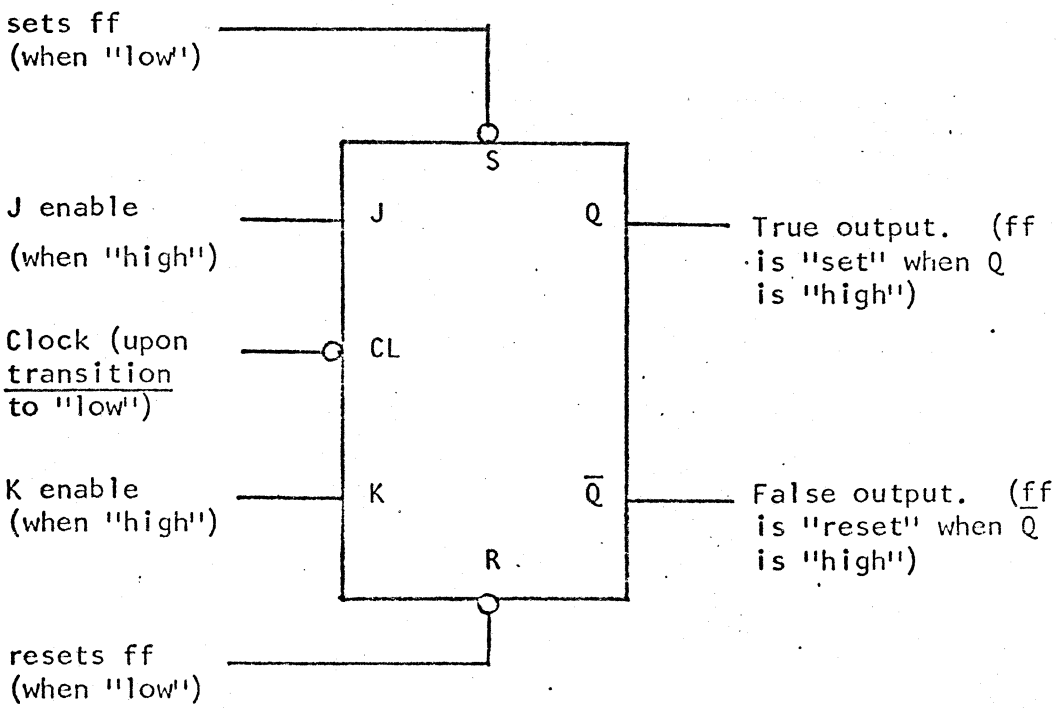
Decodes "High" 8-4-2-1 BCD Inputs



Decoded Output Goes "Low"

"4-TO-10-LINE DECODER" SYMBOL

J-K Flip-Flop



J-K FLIP-FLOP TRUTH TABLE

Input Levels Before Clock		Flip-Flop State After Clock
J	K	
Low	Low	Same as Before Clock
Low	High	Reset
High	Low	Set
High	High	Opposite of Before Clock

As illustrated in the Truth Table, the J-K flip-flop has no "forbidden" combination for its J and K inputs. If both inputs are enabled, the clock merely causes the flip-flop to toggle to the opposite state.

SECTION IV

MAINTENANCE

4.1 GENERAL

This section contains corrective and preventive maintenance information for the Model 5094-101 Multiplexer. Effective maintenance of the Multiplexer requires an adequate understanding of the logic theory.

4.2 MAINTENANCE AIDS

The maintenance aids associated with the Multiplexer are the drawings in Section V.

4.2.1 Drawings

The drawing complement consists of the following:

a. Top Assembly Drawing 5094-101
b. Block Diagram 800526
c. Logic Diagrams 76085
d. Card Assembly Drawings 76085
e. Power Supply Schematic 940015
f. Power Supply Assembly 940015
g. AC Wiring Diagram 800918

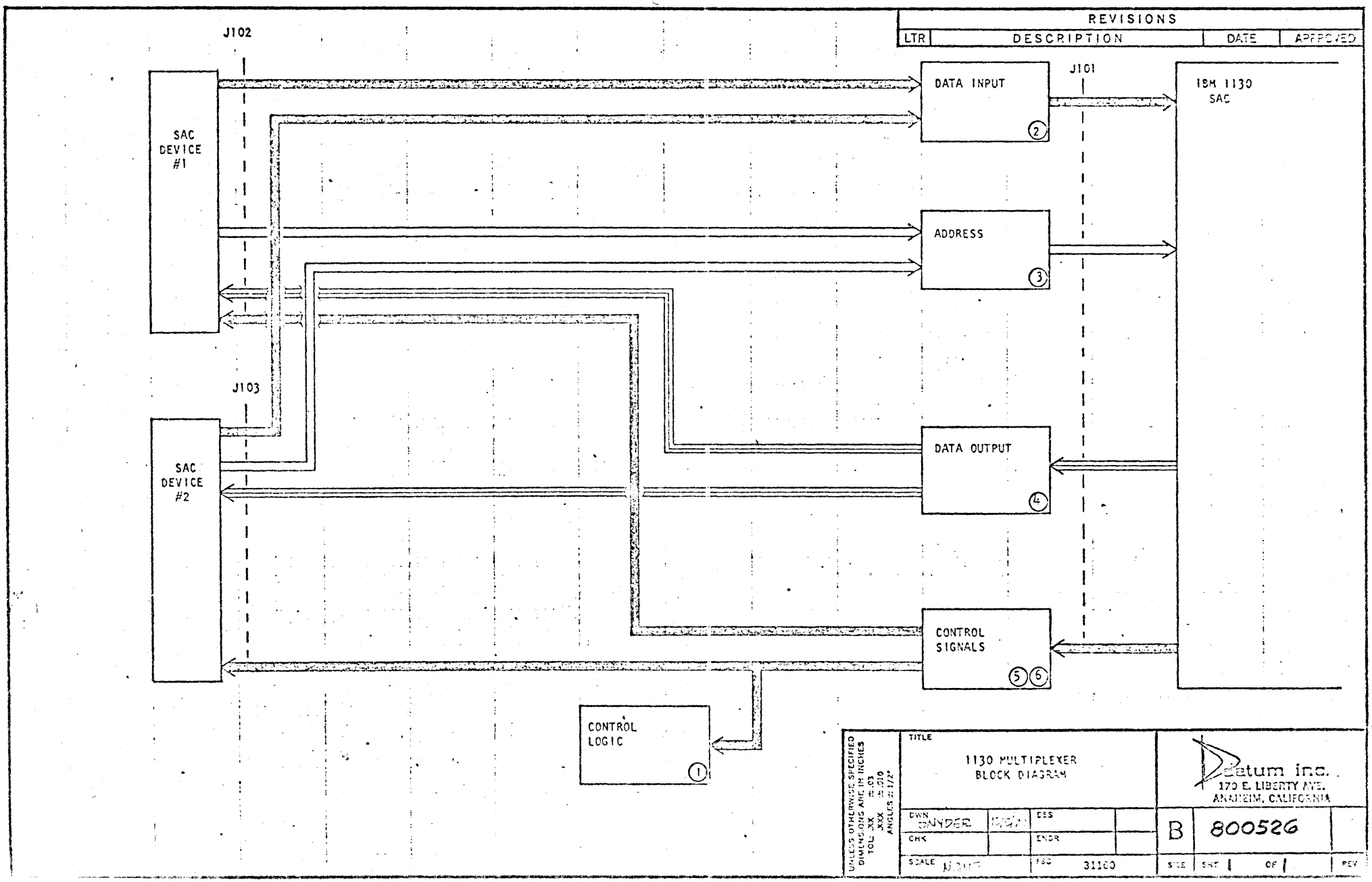
The block diagram illustrates the system in terms of each functional logic block. The sheet number in each block refers to the sheet number of Drawing 76085 where that logic is located.

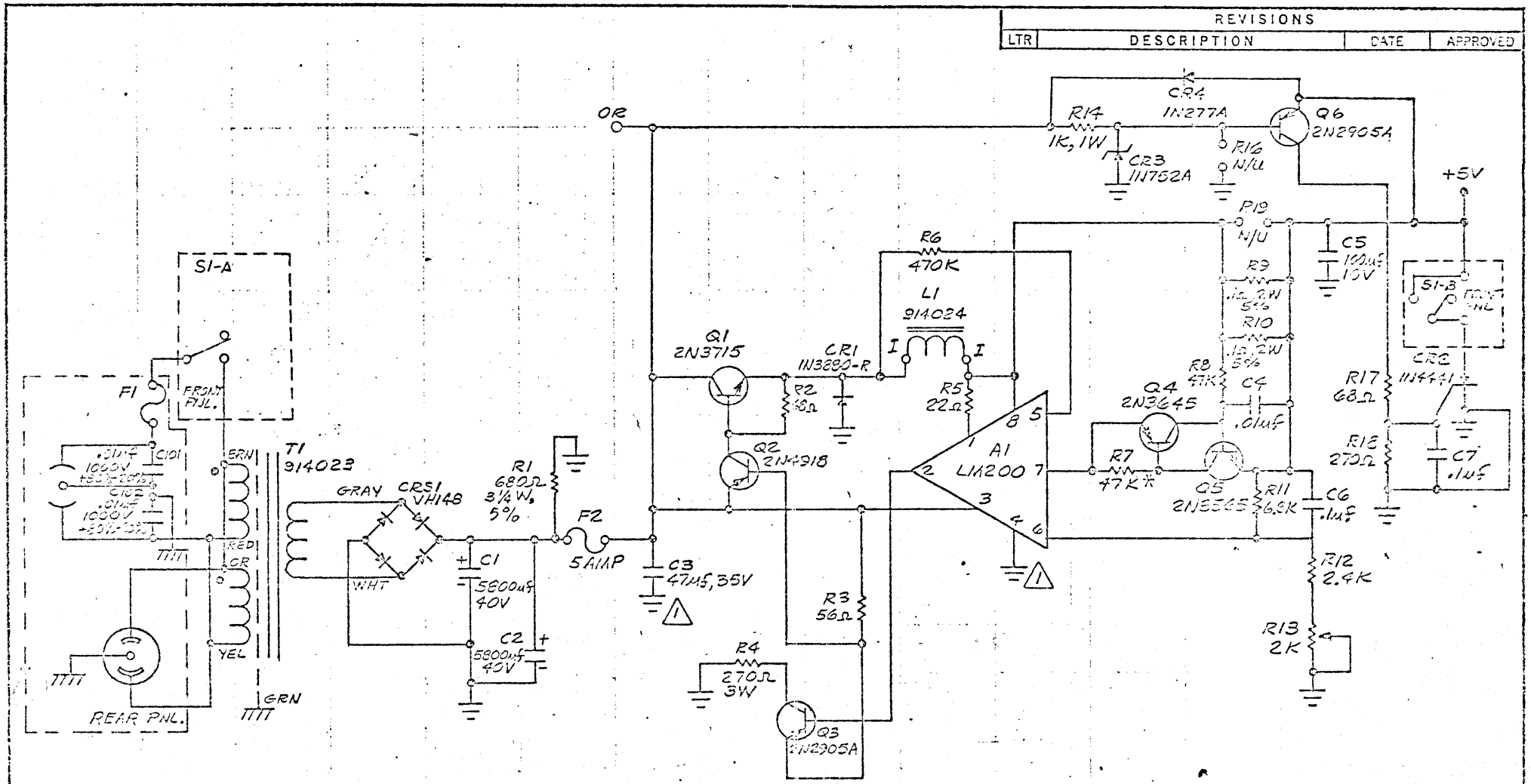
The logic diagrams furnish the logic mechanization details of the Multiplexer. The physical location of each logic element is designated on the diagrams by chip location on the card. The chip location designation corresponds to the column (A through N) and row (1 through 6) in which the chip is located on the card. The IC chip type can be determined either by examination of the chip on the card in the column/row given, or by inspection of the assembly drawing for the card.

SECTION V

DRAWINGS

Drawing Number	Rev.	Title
800526	None	1130 Multiplexer Block Diagram
940015	C	Power Supply Assembly
940015	C	Power Supply Schematic
5094-101	A	Top Assembly, 1130 Multiplexer
76085, 1 of 7	C	1130 Multiplexer
76085, 2 of 7	C	Control 1130 Multiplexer
76085, 3 of 7	C	Data Input Bus
76085, 4 of 7	C	Address Bus
76085, 5 of 7	C	Data Output Bus Re-Powering
76085, 6 of 7	C	Control Signals Re-Powering
76085, 7 of 7	C	Control Signals Re-Powering
800918	None	AC Wiring Diagram


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
J102
J101
J103
SAC DEVICE #1
SAC DEVICE #2
DATA INPUT
2
ADDRESS
3
DATA OUTPUT
4
CONTROL SIGNALS
5 6
CONTROL LOGIC
1
IBM 1130 SAC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
TITLE
1130 MULTIPLEXER BLOCK DIAGRAM
DWN CANNDER 12/67
CHK
ENGR
SCALE NONE
FSC 31100
Datum inc.
170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA
B
800526
SIZE
SHT 1 OF 1
REV



3. * DENOTES FACTORY SELECT.
2. ITEMS WITHIN DOTTED AREAS ARE EXTERNALLY MOUNTED
1. ALL RESISTORS ARE ¼W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

6-15-77

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ±.03
.XXX ±.010
ANGLES ±1/2°

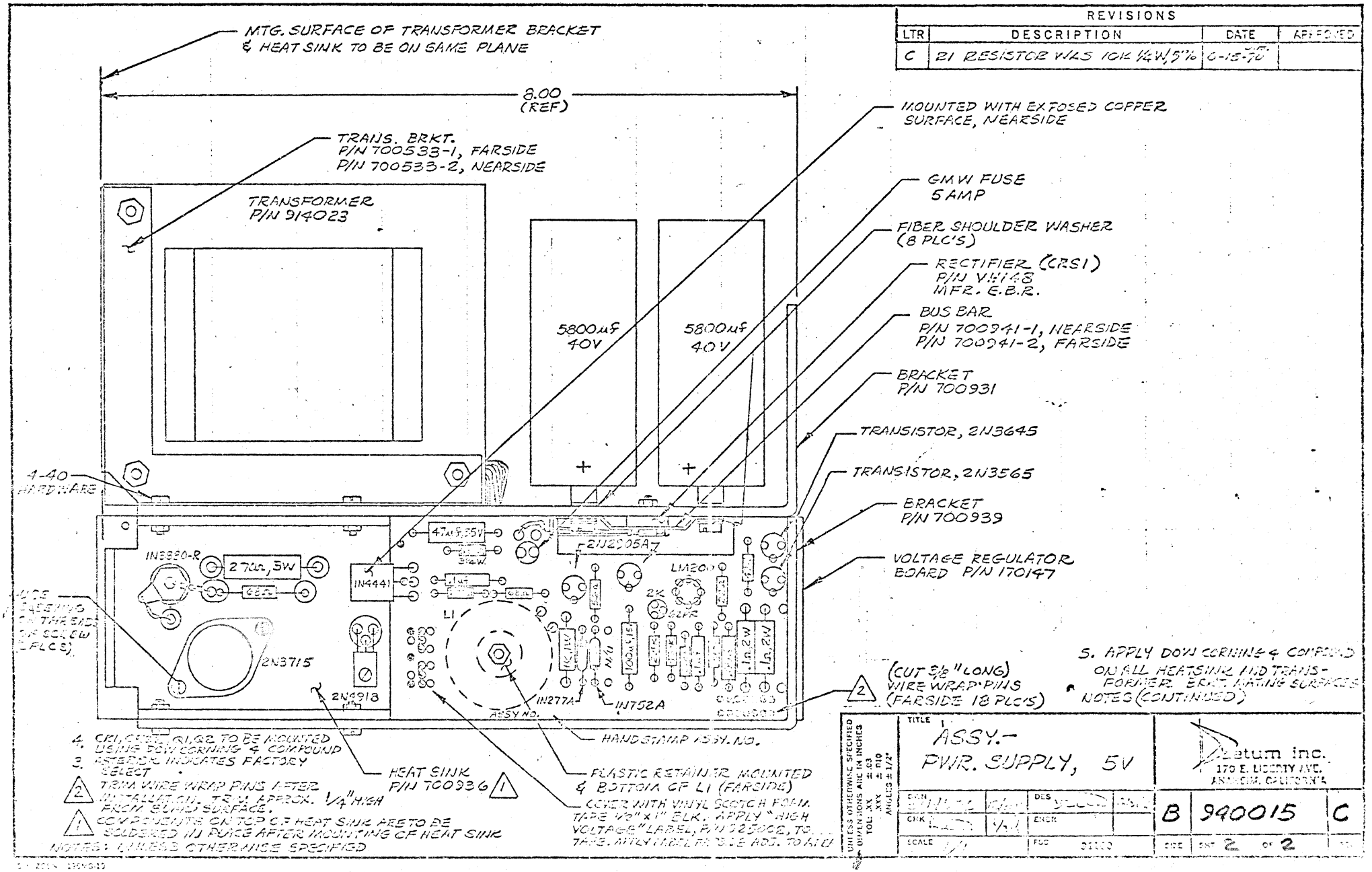
TITLE
POWER SUPPLY
+5V

DWN
CHK
SCALE NONE
DES
ENGR
ISS
DATE

Datum inc.
179 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B 940015 C

SIZE
SHT 1 OF 2
REV



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
C	R1 RESISTOR WAS 10K 1/4W 5%	6-15-70	

4. CR1, CR2, CR3, CR4 TO BE MOUNTED USING DOW CORNING 4 COMPOUND
3. ASTERISK INDICATES FACTORY SELECT
2. TRIM WIRE WRAP PINS AFTER INSTALLATION. TRIM APPROX. 1/4" HIGH FROM BOARD SURFACE.
1. COMPONENTS ON TOP OF HEAT SINK ARE TO BE SOLDERED IN PLACE AFTER MOUNTING OF HEAT SINK

NOTES: UNLESS OTHERWISE SPECIFIED

5. APPLY DOW CORNING 4 COMPOUND ON ALL HEATSINK AND TRANSFORMER MATING SURFACES

NOTES (CONTINUED)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ± .03
XXX ± .010
ANGLES ± 1/2°

TITLE: ASSY.- PWR. SUPPLY, 5V

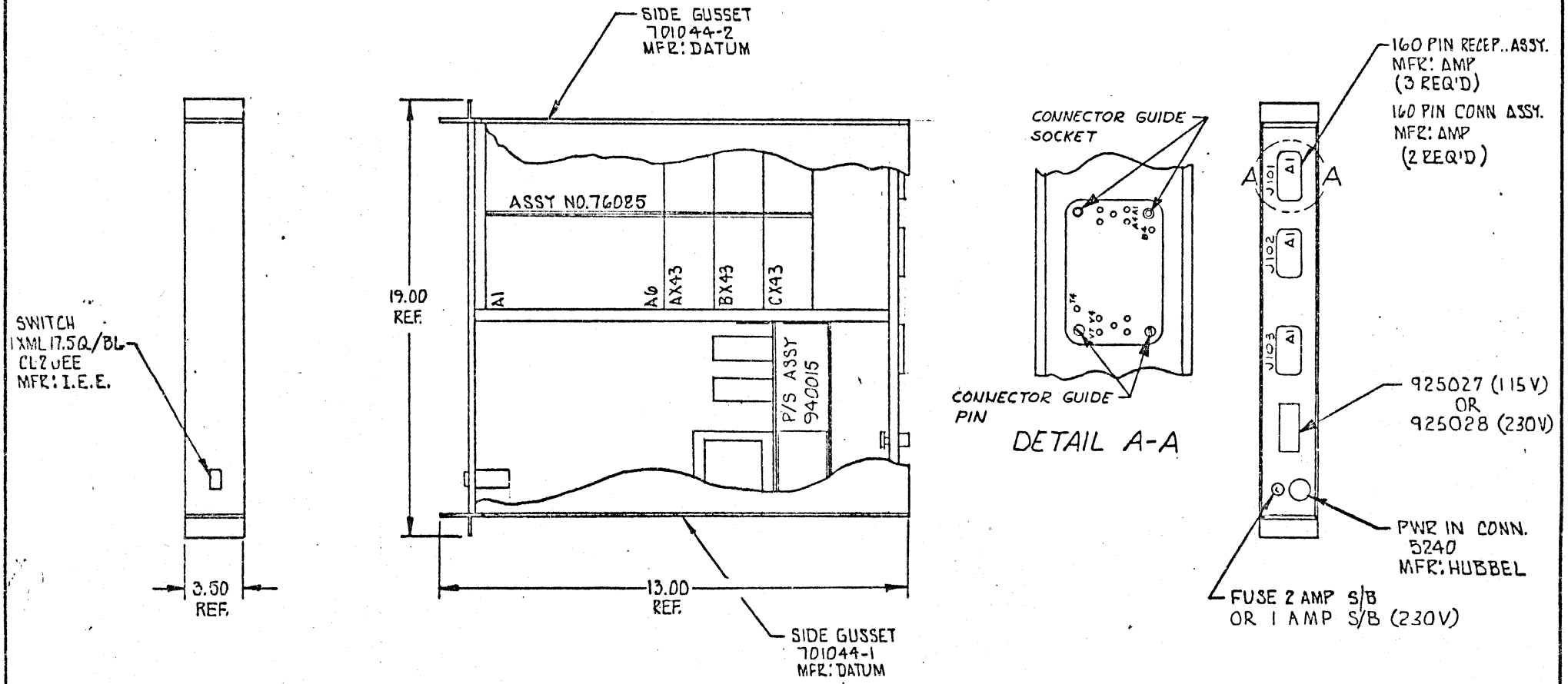
Tetum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN		DES	
CHK		ENGR	
SCALE		FSC	01100

B | 940015 | C

SIZE | SHT 2 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ADD 115 VAC LABEL & 1A S/B FUSE CO.1580 MWJ.	9-24-74	



NOTES: UNLESS OTHERWISE SPECIFIED

6-21-72

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

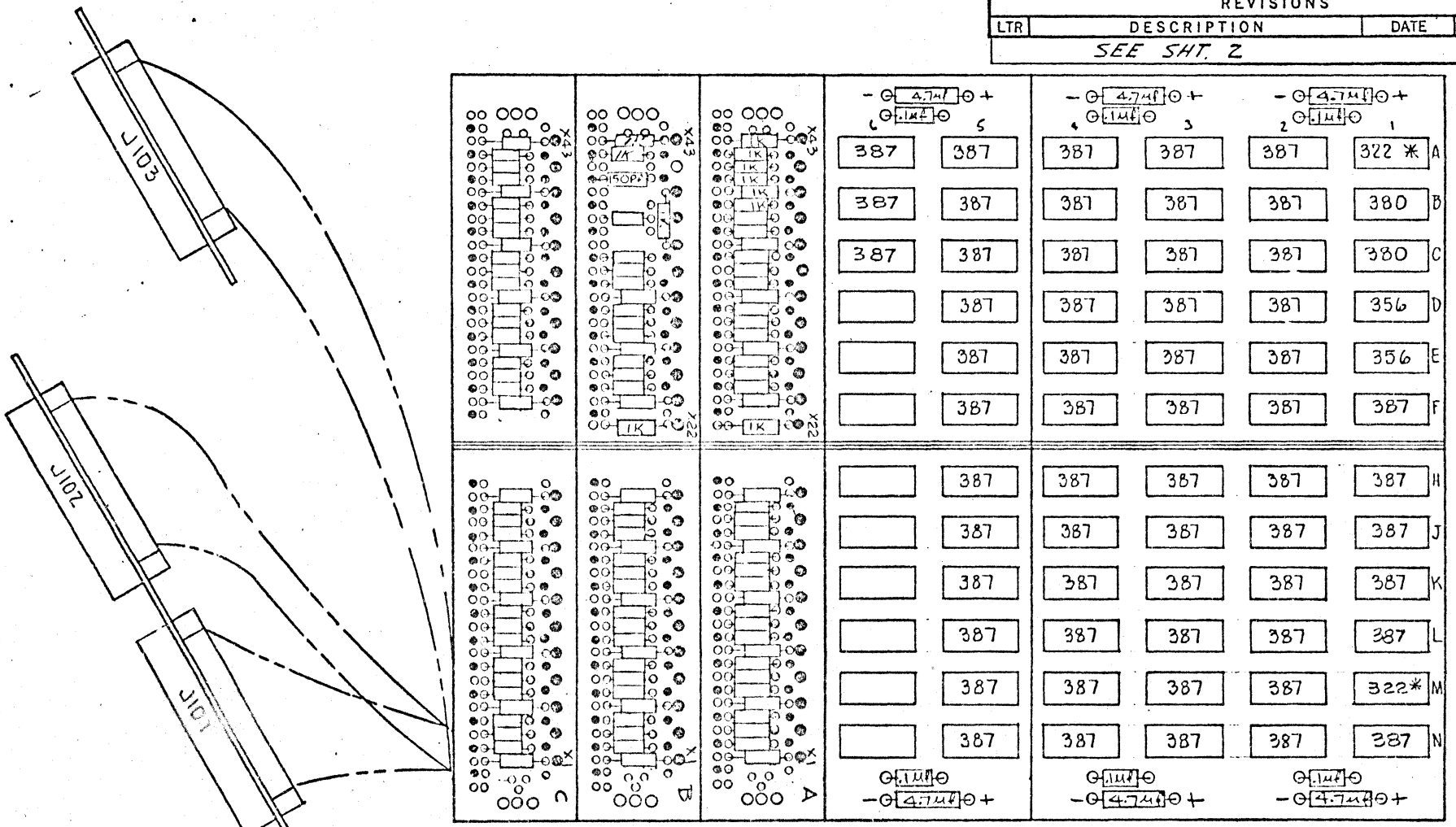
TITLE
TOP ASSEMBLY—
1130 MULTIPLEXER
2 PORT

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	CHK	DES	ENGR	SIZE	DRAWING NO.	REV
BORGER 5-19-70				B	5094-101	A

SCALE NONE FSC 31160 SHT 1 OF 1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	SEE SHT. 2		



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 150Ω 1/4W, 5%
2. WIRE PER WIRELIST 800440
3. ● DENOTES WIRE WRAP PIN

1-3-73

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03, .XXX ±.010, ANGLES ±1/2°

TITLE: 1130 MUX.

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	BORGER	DES		B	76085	C
CHK		ENGR				
SCALE	NONE	FSC	31160	SIZE	SHT 1 OF 7	REV

REVISIONS			
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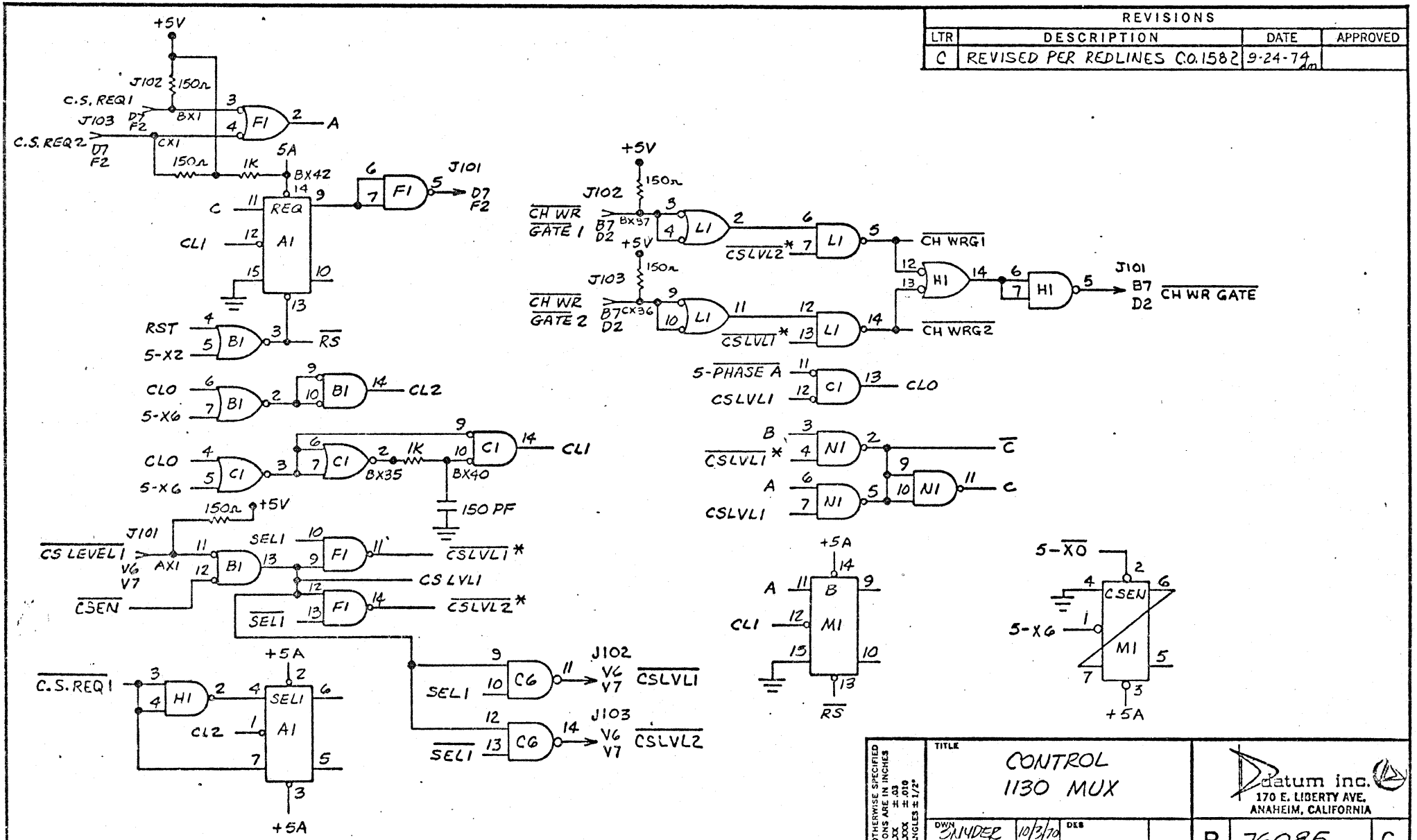
C	REVISED PER REDLINES CO. 1582	9-24-74	



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: CONTROL 1130 MUX

DWN SNYDER 10/3/70 DES

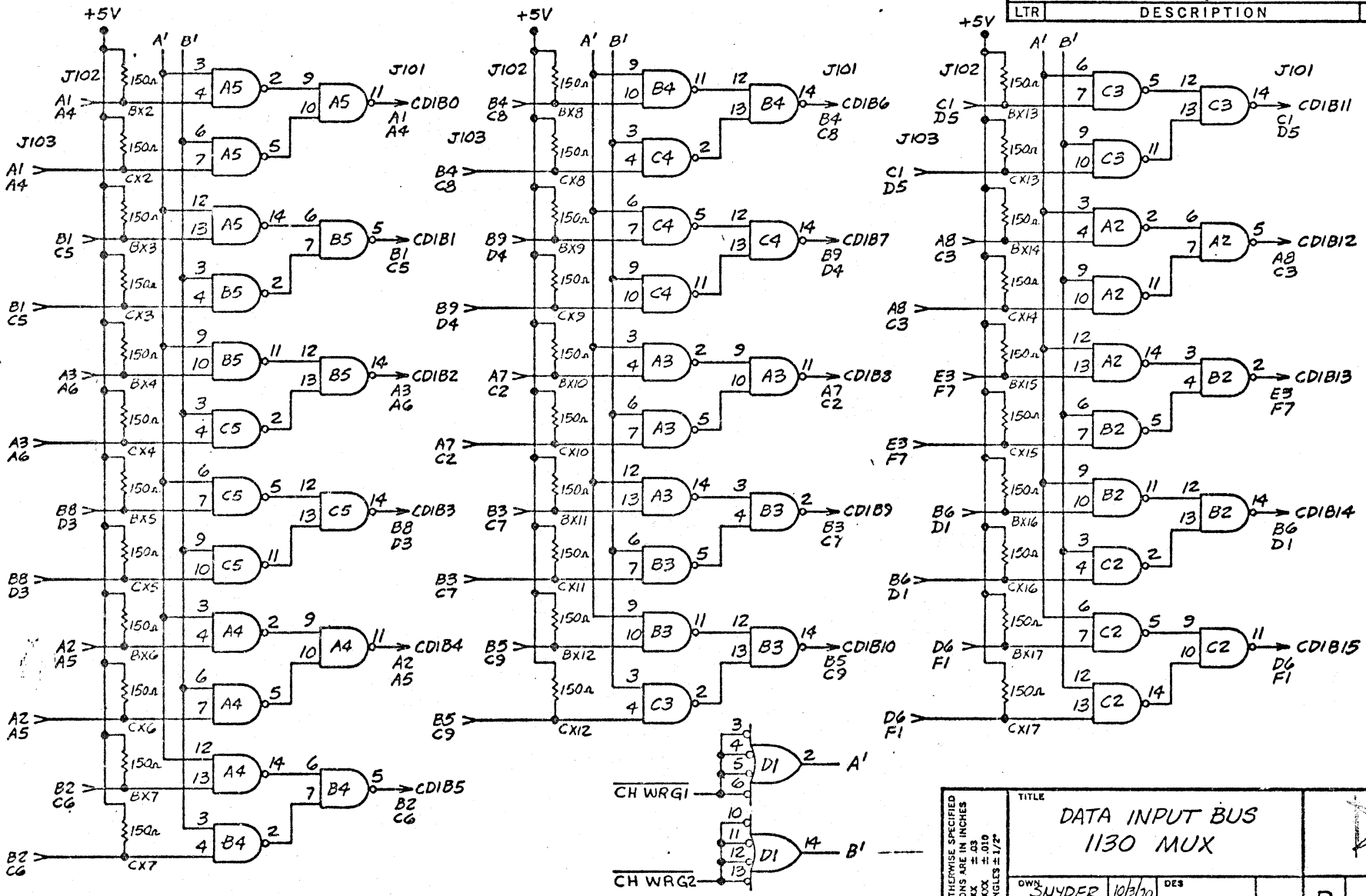
CHK ENGR

SCALE FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 76085 | C

SIZE | SHT 2 OF 7 | REV



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

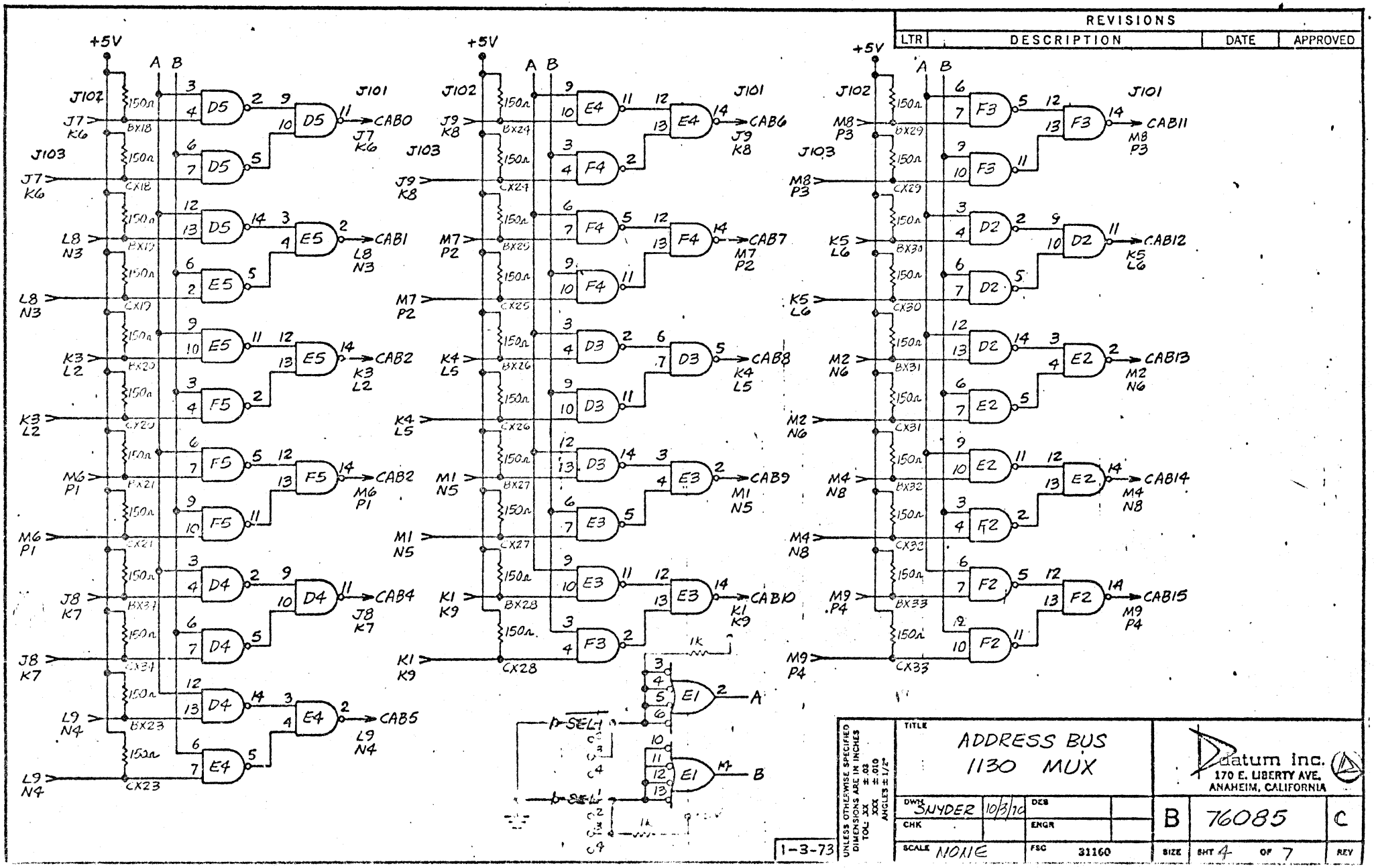
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ± .03
XXX ± .010
ANGLES ± 1/2°

TITLE
DATA INPUT BUS
1130 MUX

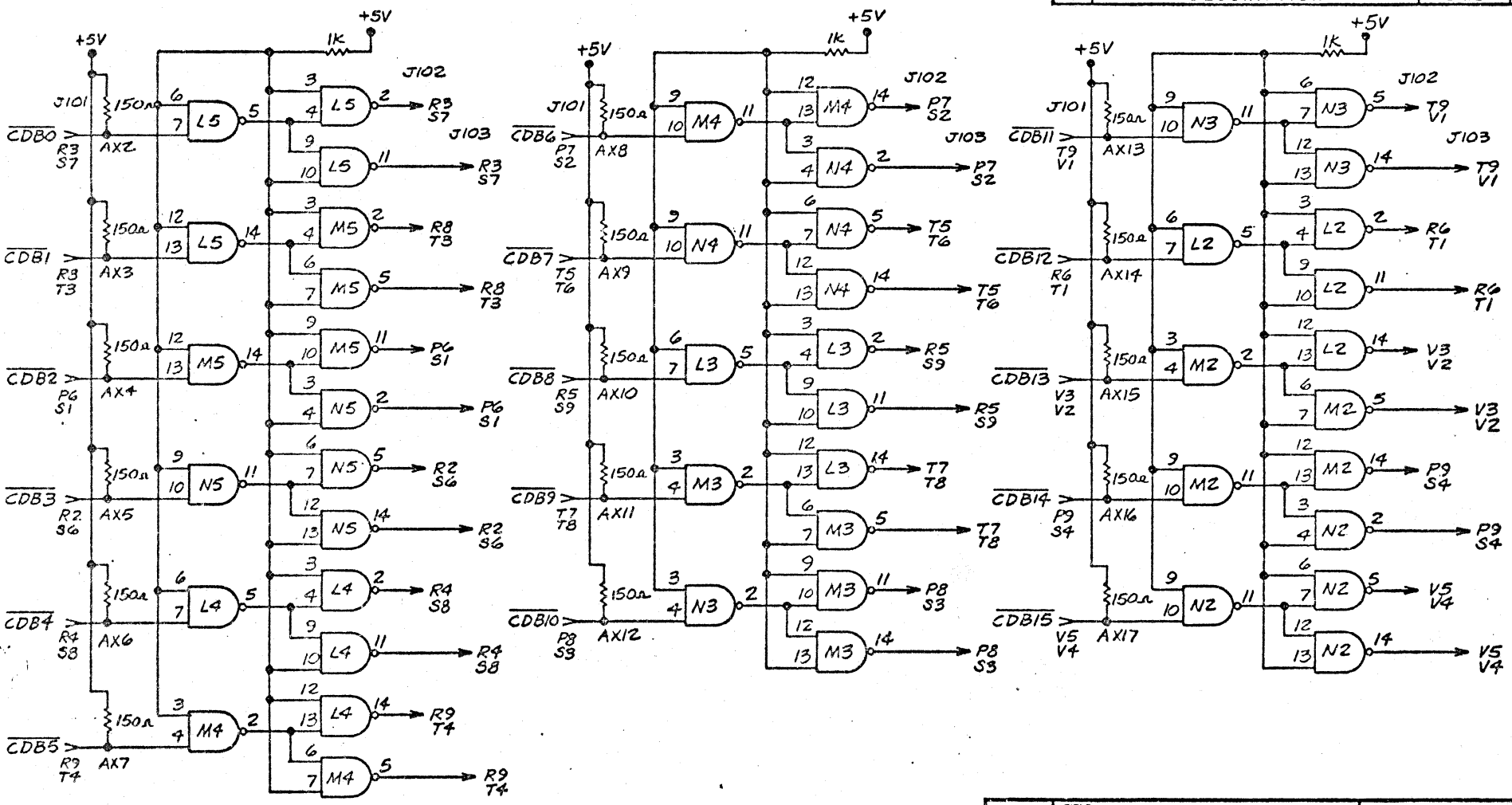
datum inc
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN SNYDER	10/3/70	DES		B	76085	C
CHK		ENGR				
SCALE NONE		FSC 3[illegible]		SIZE	SHT 3 OF 7	REV

1-3-73


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
+5V
A B
J102
J103
J101
J7 K6
J8 K7
J9 K8
L8 N3
L9 N4
K3 L2
K4 L5
K5 L6
M1 N5
M2 N6
M4 N8
M6 P1
M7 P2
M8 P3
M9 P4
K1 K9
150Ω
1K
D5
D4
E5
E4
F5
F4
D3
E3
F3
D2
E2
F2
E1
CAB0
CAB1
CAB2
CAB4
CAB5
CAB6
CAB7
CAB8
CAB9
CAB10
CAB11
CAB12
CAB13
CAB14
CAB15
A
B
SEL1
SEL2
SEL3
SEL4
1-3-73
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
TITLE
ADDRESS BUS
1130 MUX
Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
DWN SNYDER 10/3/72
DES
CHK
ENGR
SCALE NONE
FSC 31160
B
76085
C
SIZE
SHT 4 OF 7
REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



1-3-73

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°

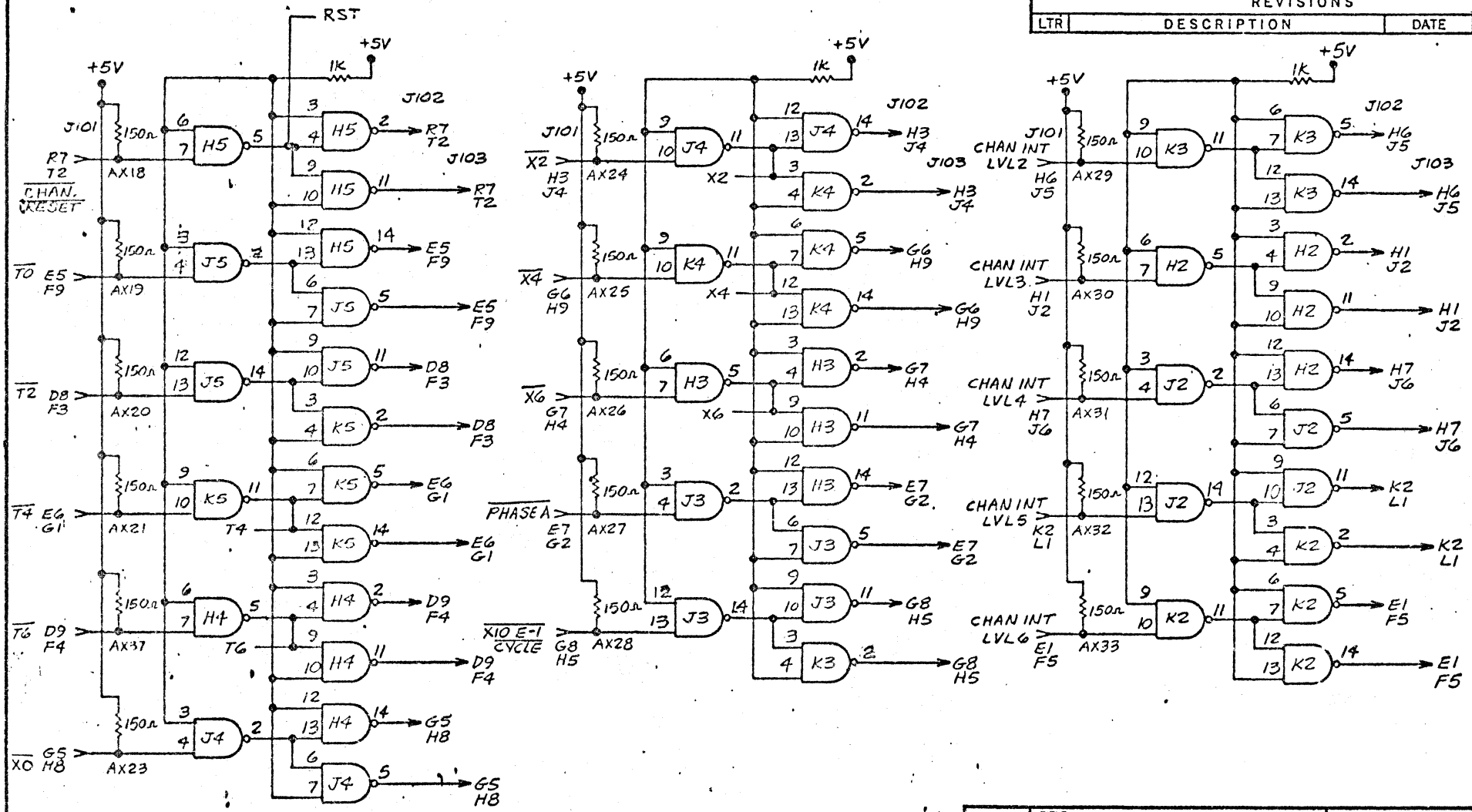
TITLE
DATA OUTPUT BUS
RE-POWERING
1130 MUX

DWN SNYDER	10/7/72	DES.	
CHK		ENGR	
SCALE 1/1 1/15		FSC 31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE	DWG NO.	REV
B	76085	C

SHT 5 OF 7



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

1-3-73

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE
CONTROL SIGNALS
RE-POWERING
1130 MUX

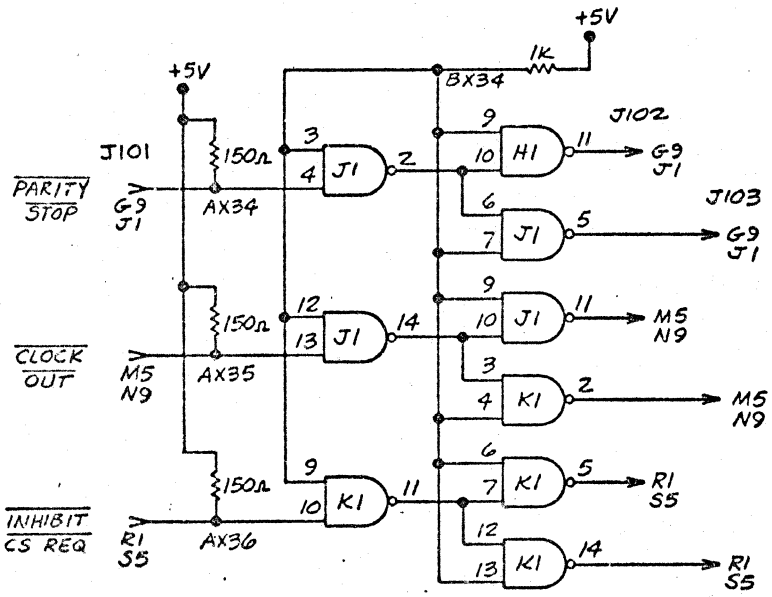
datum inc
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

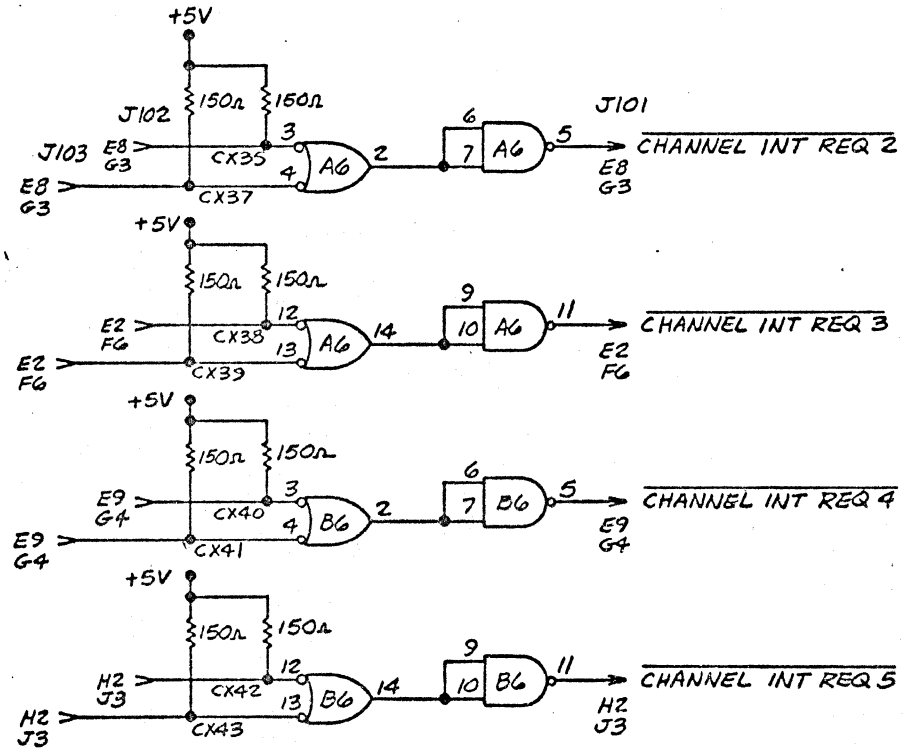
DWN	DES
SNYDER 10/4/72	
CHK	ENGR
SCALE NONE	FSC 31160

B | 76085 | C

SIZE | SHT 6 OF 7 | REV

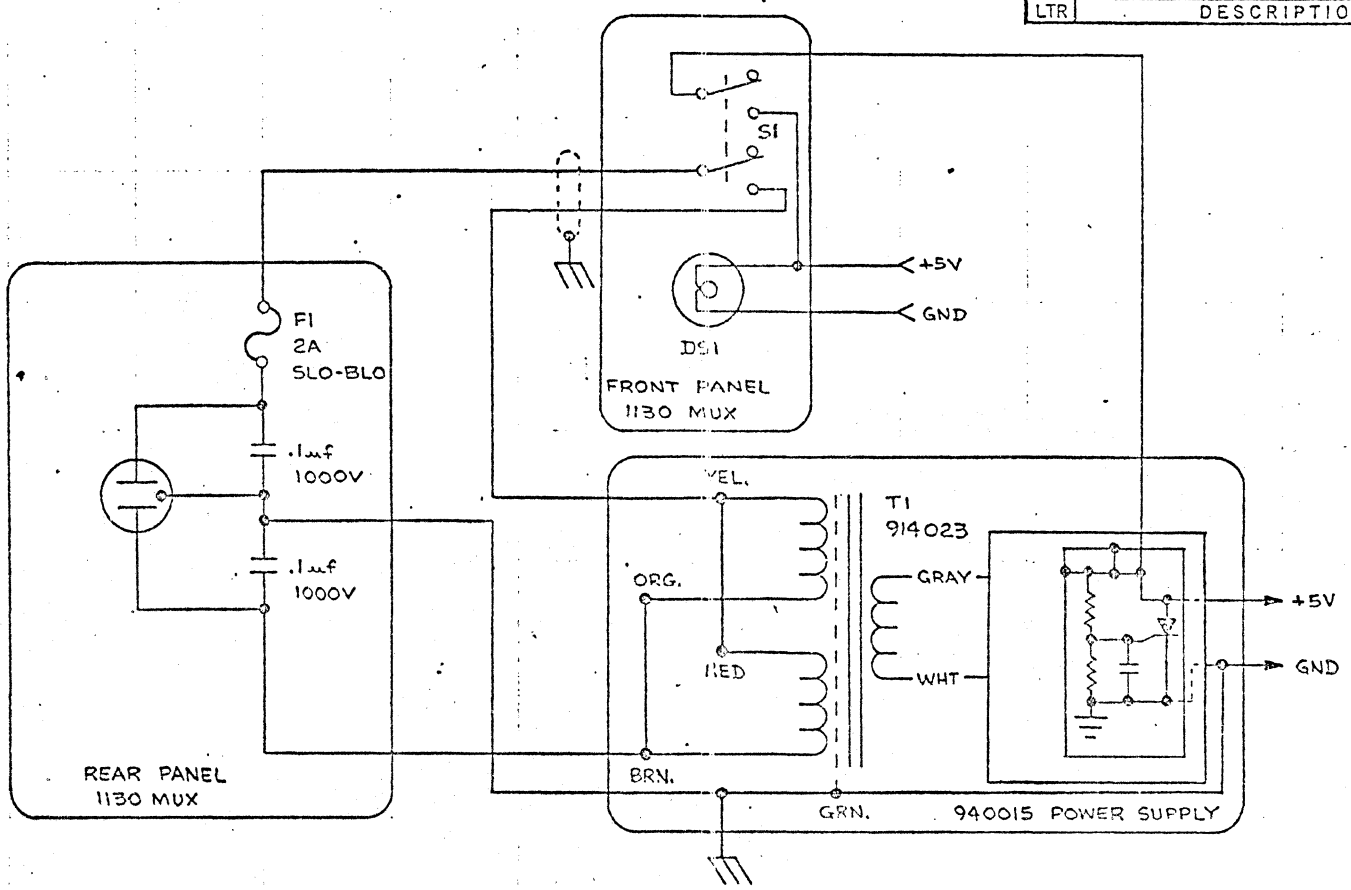
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°	TITLE: CONTROL SIGNALS RE-POWERING 1130 MUX	datum inc 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA	
1-3-73	DWN SNYDER 10/3/70 DES CHK ENGR SCALE NONE FSC 31160	B 76085 C SIZE SHT 7 OF 7 REV	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



1. FOR CONVERSION TO 230 VAC 50HZ
   DELETE BRN-ORG. JUMPER AND RED-YEL. JUMPER;
   ADD RED-ORG. JUMPER.
   HANDSTAMP REAR PANEL: 230VAC 50HZ

NOTE:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE
AC WIRING DIAGRAM 1130 MULTIPLEXER

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	M.CARINO	6-19-72	DES		B	800918
CHK			ENGR			
SCALE	NONE		FSC	31150	SIZE	SHT 1 OF 1