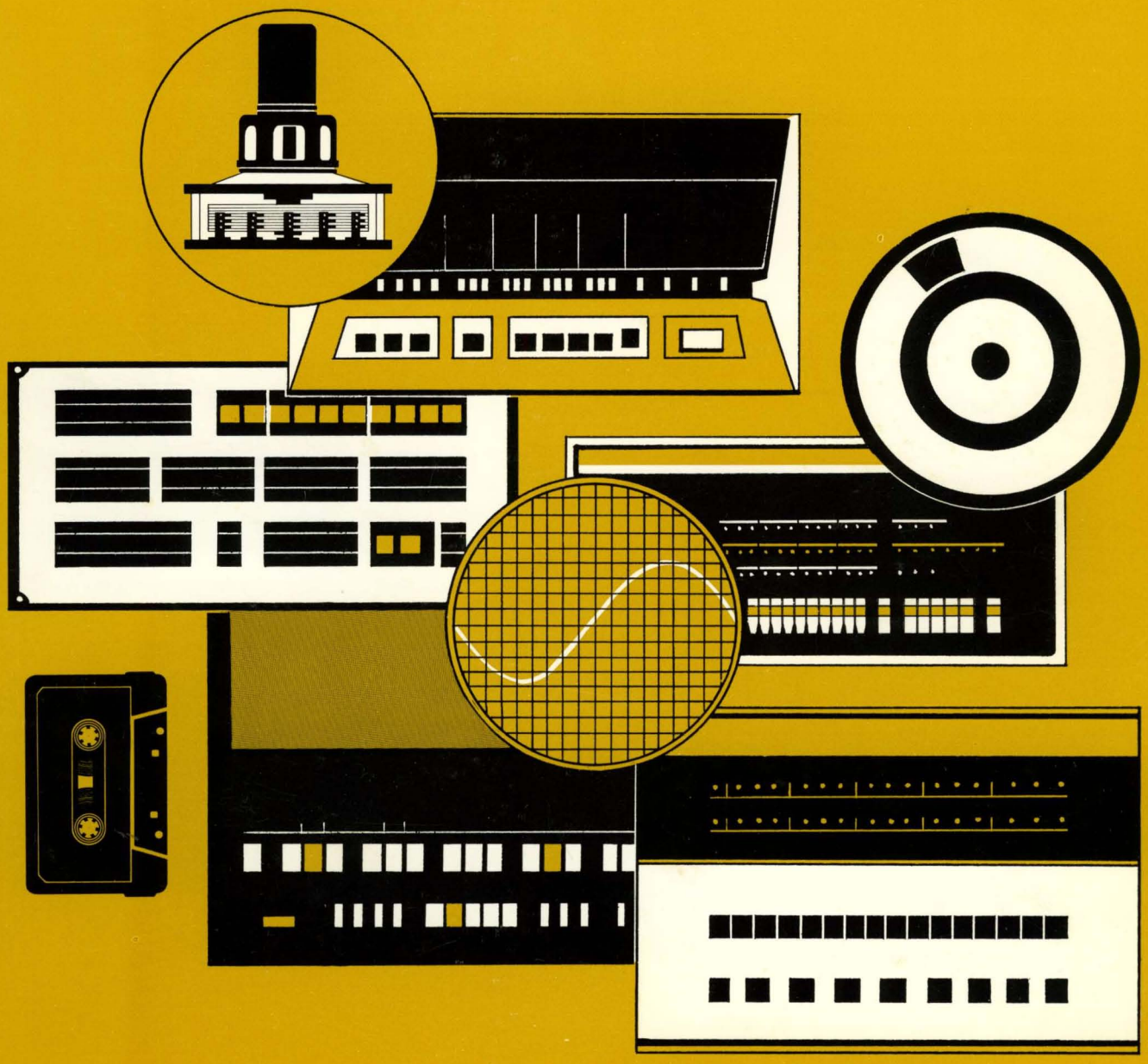
DATUM

5091-P8e

MAGNETIC TAPE SYSTEM

TECHNICAL DESCRIPTION

PUBLICATION NO. SM-06



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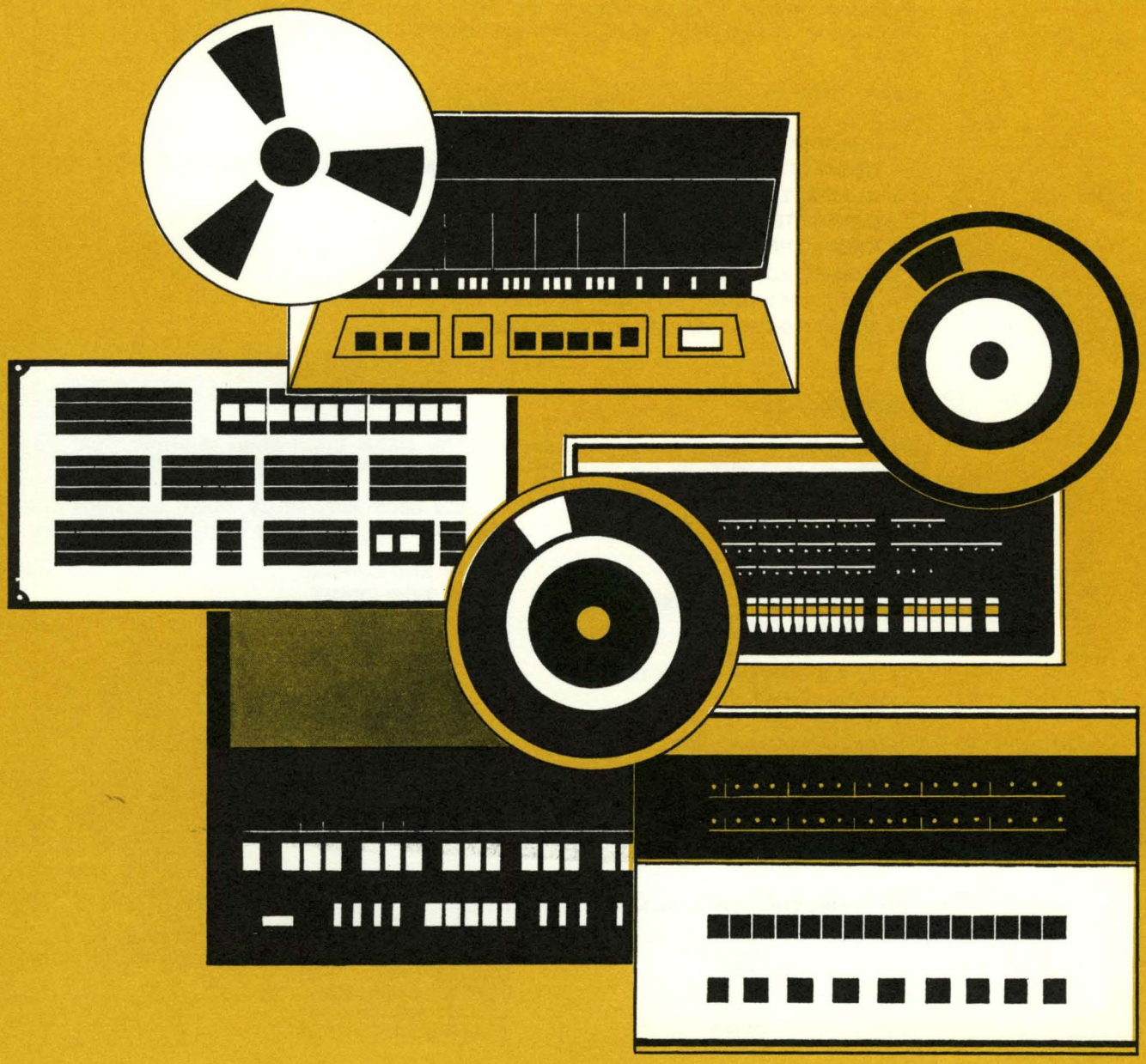
TECHNICAL DESCRIPTION

PUBLICATION NO. SM-06

DATUM INC.
1363 S. State College Blvd.
Anaheim, California 92806

DATUM PERIPHERAL EQUIPMENT DIVISION

SERIES 5091 MAGNETIC TAPE INPUT/OUTPUT SYSTEMS FOR MINI-COMPUTERS



OPTIONS

SEVEN/NINE CHANNEL

The standard controller accommodates either seven (dual-density) *or* nine-channel, magnetic tape recorders. This option offers both seven *and* nine-channel operation. The device selection and command set is augmented to provide program selection of low or high BPI recording density. Also, character parity (VRC) may be selected by program control as even or odd parity (7-channel only).

CABINETS

Both single-bay and dual-bay cabinets are available.

TAPE UNIT ADDRESS SWITCH

The Series 5091 system may include from one to four tape recorders, designated A, B, C and D. Logically these are identified as 0, 1, 2 and 3. In the standard controller, recorder A corresponds to logic unit 0, recorder B to logic unit 1, etc. This option provides four front-panel switches allowing any recorder to be assigned any logical identity.

TERMINATION CARD

By providing a single termination card, this option allows interchangeability of the tape units at will in a multiple-tape unit system.

SPECIFICATIONS

Weight:	Single tape system—less than 100 lbs.
Power:	117V 60 Hz single phase, regular outlet power, 300 watts per tape unit.
Number of Tracks:	7 or 9 IBM compatible.
Data Density:	9 track—800 BPI 9 track — 1600 BPI 7 track—800/556, 800/200, 556/200 BPI
Rewind Speed:	150 IPS (10-1/2 inches) 50 IPS (7 inches)
Reel Size:	10-1/2 inches 7 inches
Operating Temperature:	35° to 122°F (10-1/2 inches) 41° to 113°F (7 inches)
Mounting:	User-supplied standard RETMA rack mount. Optional cabinet can be supplied by DATUM, Inc.

Standard Series 5091 Systems, with software, are available for the following computers:

HP2114	**PDP-9**	**Honeywell 124A**
HP2115	**PDP-9/L**	**Honeywell 316**
HP2116	**PDP-11**	**Honeywell 416**
PDP-8	**PDP-15**	**Honeywell 516**
PDP-8E	**IBM 1130**	**SDS CE16**
PDP-8/L	**Varian 620i**	**SDS CF16**
PDP-8/I	**CAI 816**	**Micro-Systems 810**
Univac 1107	**NOVA**	**Univac 1616**

Designs for other computers are being produced continually.

DATUM 5091-P8e

MAGNETIC TAPE SYSTEM DESCRIPTION

FEATURES

a. TC58-compatible.

b. Stand-alone driver and diagnostics provided.

c. Controller mounts within the mainframe.

d. Drives — Rack Mount

1. Pertec

(a) Speeds of 12.5 ips to 75 ips

(b) Reel sizes 7" to 10-1/2"

(c) Read-after-write is standard (single gap optional).

2. Wangco

(a) Speeds of 12.5 ips to 75 ips

(b) Vacuum column available on 10-1/2" reel models at 25, 37.5, 45, or 75 ips

(c) Read-after-write is standard (single gap optional).

e. Write or read on-the-fly (continuous tape motion).

f. Edit mode (if transport is so equipped).

FEATURES (continued)

g. Memory extension.

h. Mixed 7- or 9-track.

i. Up to four drives.

j. Three-cycle data break.

SECTION I

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 FUNCTIONAL DESCRIPTION

The DATUM PDP8e Controller provides interface between the DEC PDP8e computer and 9-track, 800 BPI and/or 7-track 800/556/200 BPI tape machines, enabling computer-control of writing and reading IBM- or USACCII-compatible magnetic tapes.

All major operations are performed automatically under command of the Controller. Individual selection and operation with up to four "Daisy-Chained" tape transports is provided. Either single- or dual-gap machines can be accommodated.

Tape transport motion control, Cyclic Redundancy Check Character (CRCC) and Longitudinal Redundancy Check Character (LRCC) generation and checking, inter-record-gap generation and status reporting are included. All Write clocks and delay times are derived from a crystal-controlled oscillator. No "one-shots" or RC delays are utilized.

The unit plugs directly into the computer omnibus and uses computer power.

"On the Fly" operation (continuous read or write at maximum tape speed without stopping in each inter-record gap) is provided.

The IBM-compatible file mark (7- or 9-track formats) is written and recognized.

The "Edit" feature (allows a record anywhere on a previously recorded tape to be replaced with an updated record of equal size) is provided.

No calibration or adjustment potentiometers in the Formatter. All timing is derived from a crystal oscillator.

Compatible to entire 12.5 to 75-ips tape-speed range without changing crystals. A single field-changeable jumper selects the frequencies needed for the tape speed.

1.2 PHYSICAL DESCRIPTION

The DATUM Model 5091 NRZI Controller, complete on three large circuit boards, is designed to be installed in the PDP8e computer mainframe. Figure 1-1 shows this installation.

1.3 SPECIFICATIONS

Inter-record gap (7 track)	.75 inch nominal (.69 inch minimum)
Inter-record gap (9 track)	.6 inch nominal (.54 inch minimum)
Circuits	All silicon
Operating Temperature	0° to 50° C
Storage Temperature	-40° to +70° C
Altitude	0 to 20,000 feet
Relative Humidity	10 to 95% (non-condensing)
Interface Voltages (DTL 900 series or TTL 7400 series compatible)	low = 0V ±.4V high = 3.9V ±1.5V

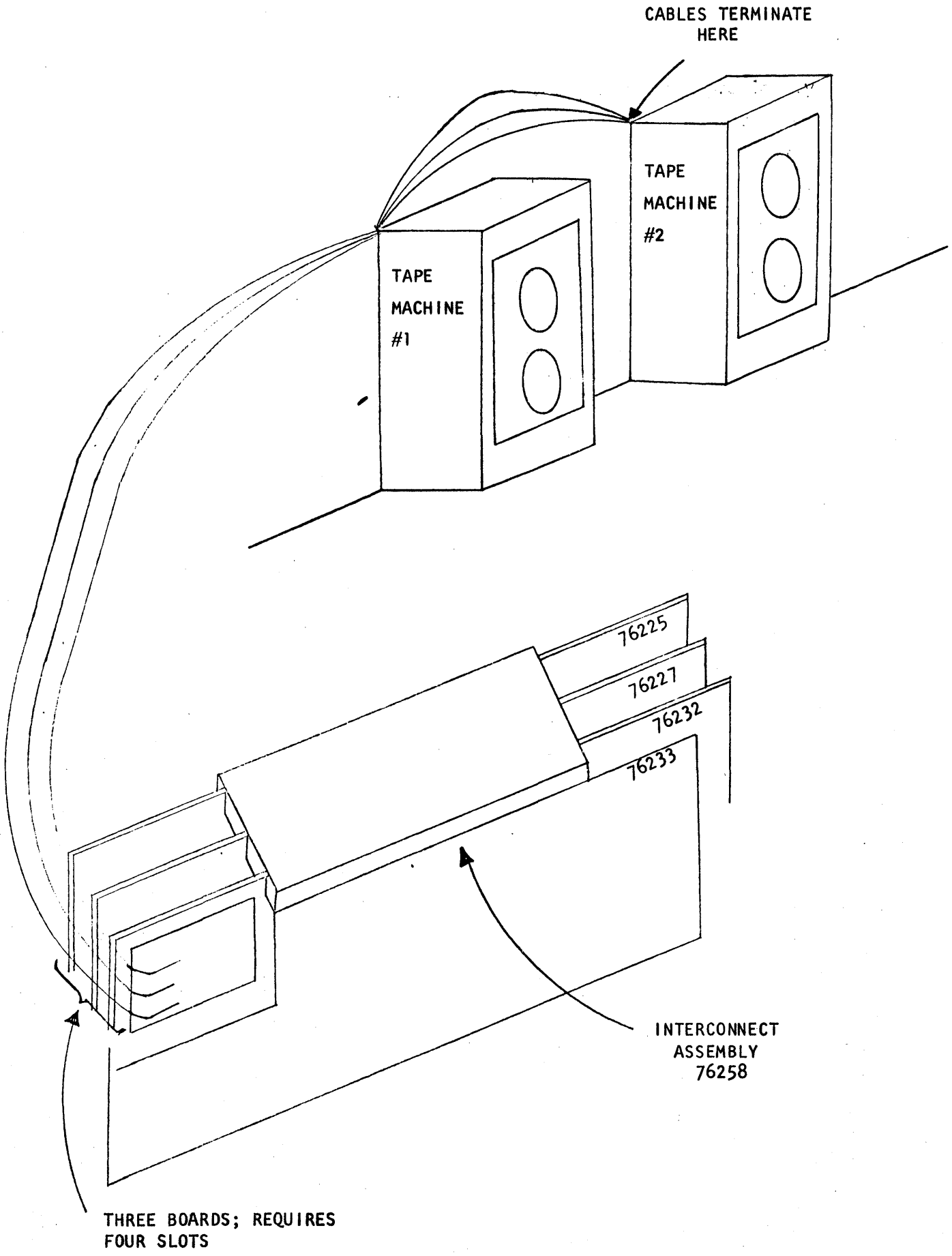


Figure 1-1. Installation of Model 5091 NRZI Controller

The interface is designed such that an open circuit is interpreted as a "high" signal.

Figure 1-3 illustrates the configuration for which the interface has been designed.

1.4 MAGNETIC TAPE FORMATS

Figures 1-4 and 1-5 illustrate the IBM and USASCII magnetic tape formats for 7-track and 9-track tapes, respectively.

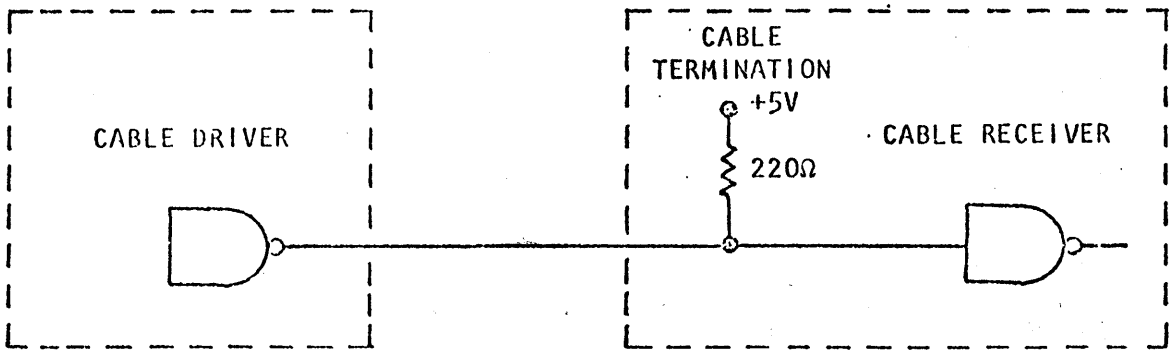
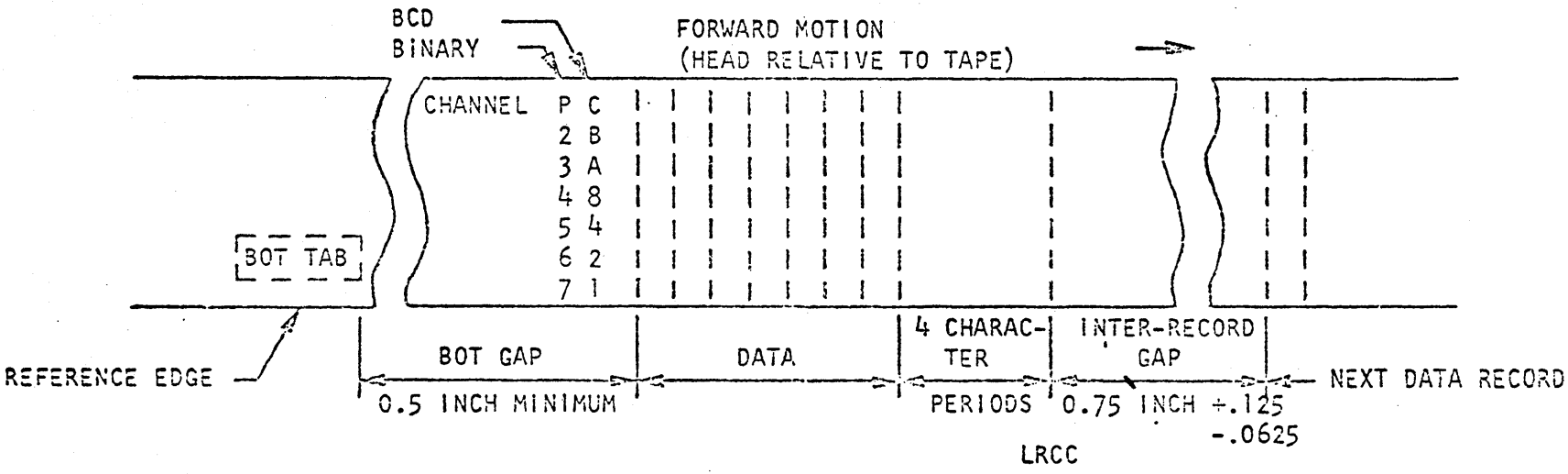


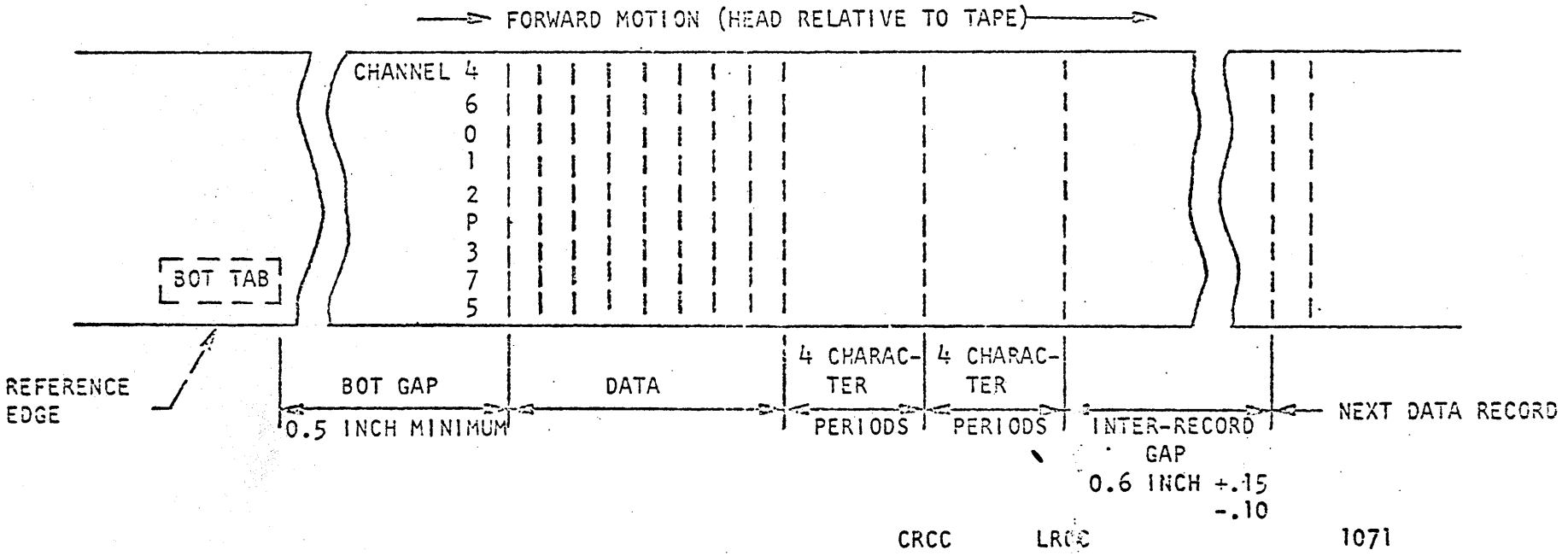
Figure 1-3. Interface Circuits



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) CONTAINS ODD DATA PARITY FOR BINARY TAPES, OR EVEN PARITY FOR BCD TAPES.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE LRCC) IS EVEN. IT IS POSSIBLE IN THE 7-TRACK FORMAT FOR THIS CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
5. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 4, 5, 6 AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE FILE MARK IS SEPARATED BY NORMAL IRG's (.75 INCH) FROM THE PREVIOUS AND FOLLOWING RECORDS. OPTIONALLY, A 3.5-INCH GAP CAN BE ERASED PRIOR TO WRITING THE FILE MARK.
6. DATA PACKING DENSITY MAY BE 200, 556, or 800 BITS PER INCH.

Figure 1-4. 7-Track Format



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRCC AND THE LRCC) IS EVEN. IN THE 9-TRACK FORMAT THE LRCC WILL NEVER BE AN ALL-ZEROES CHARACTER.
5. IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL ZEROES. THE FILE MARK IS SEPARATED BY NORMAL IRG's (.6 INCH) FROM THE PREVIOUS AND FOLLOWING RECORDS. OPTIONALLY, A 3.5 INCH GAP CAN BE ERASED PRIOR TO WRITING A FILE MARK.

Figure 1-5. 9-Track Format

SECTION II

INTERFACE

2.1 INTRODUCTION

There are two interfaces to the Controller Formatter section, one to the computer adapter section and one to the tape units (76232 A1, A2, C1 and C2).

Individual, stranded, 22-26-gauge twisted-pair wires should be used. Maximum length should be twenty feet (total) for the tape-unit "Daisy-Chain" bus.

The twisted-pair wire should have at least one twist per inch and a minimum insulation thickness of .01 inch.

The ground wire of each twisted pair should be terminated to ground as close to the origin or destination of the signal as possible (within 6 inches maximum) to minimize ground-loop-current "crosstalk" effects.

2.2 FORMATTER/TRANSPORT(s) INTERFACE

2.2.1 Formatter to Transport

2.2.1.1 Transport Address

$\overline{\text{SELECT A}}$ through $\overline{\text{SELECT D}}$ - Transport Select Lines. Four select lines to select one of the "daisy-chained" transports. Developed by decoding CR1 and CR2 from the command register.

2.2.1.2 Control

The control lines activate the selected transport when it is "READY" and "ON LINE".

$\overline{SFC}$ - Synchronous Forward Command. A levelwhich, when low, causes the selected transport to "ramp" up to speed and drive forward at the rated speed until the level goes back high. When switches to the high level, the transport "ramps" down to halt.

$\overline{SRC}$ - Synchronous Reverse Command. A level which, when low, causes the same action as $\overline{SFC}$ except in reverse tape motion.

$\overline{RWC}$ - Rewind Command. A negative-going pulse which causes the selected transport to rewind to load point.

$\overline{OFC}$ - Offline Command. A negative-going pulse which causes the selected transport to revert to manual control. Transport must be manually placed "ON LINE" before it can again be operated.

The offline command can be transmitted to a tape transport that is rewinding (even though the transport status indicates NOT READY).

$\overline{SWS}$ - Set Write Status. The level of this signal is inspected within 20 microseconds after an SFC or SRC command is initiated to set the selected transport to the write or read mode. This mode is maintained until the next SFC or SRC command is initiated.

The write mode within the transport is also switched to read mode if:

a) An RWC or OFC command is received.
b) Loss of interlock occurs.
c) The transport is manually switched offline.

$\overline{\text{EDIT}}$ – (Over Write). – This signal is a level that causes the transport write current enable/disable to "ramp" on and off to minimize rate of change of recorded inter block gap magnetism when rewriting a record in the EDIT mode.

This signal level also causes the DC erase head current to be turned off immediately after rewriting the new record (to keep from erasing the beginning of the next record).

$\overline{\text{WARS}}$ – Write Amplifiers Reset. This signal controls the early ramp down of write and early turn off of erase currents after rewriting a record in the EDIT mode.

The negative-going transition of this signal initiates the write current ramp down. In NRZI transports, this signal also generates the LRC character.

$\overline{\text{DDS}}$ – Select High Density. Low = select high density (for NRZI Formatter only) for 7-track transport.

2.2.1.3 Write Data

$\overline{\text{WDS}}$ – Write Data Strobe. This is a clock used to copy the write data ($\overline{\text{WDP}}$ and $\overline{\text{WD0}}$ through $\overline{\text{WD7}}$) into the selected transport write flip-flops. The data levels must be static during $\overline{\text{WDS}}$ and the trailing edge (positive-going) of $\overline{\text{WDS}}$ is used to clock the flip-flops. The clock rate is at the character rate for NRZI.

$\overline{\text{WDP}}$, $\overline{\text{WD0}}$ through $\overline{\text{WD7}}$ – Write Data. $\overline{\text{WDP}}$ is the parity bit, $\overline{\text{WD0}}$ is the most significant bit, and $\overline{\text{WD7}}$ is the least-significant bit. $\overline{\text{WD0}}$ and $\overline{\text{WD1}}$ are not used for 7-track NRZI operation.

These signals are presented to the selected transport along with the $\overline{\text{WDS}}$ clock. The write data is presented in a logic-level form (low = logic 1, high = logic 0).

2.2.2 Transport to Formatter

2.2.2.1 Status Lines.

$\overline{\text{RDY}}$ - Ready. A level that is low only when the selected transport is:

a) Interlocked

b) Through the initial load or rewind-to-load point sequence.

c) On line

d) Not rewinding

Note: A transport may go NOT Ready for approximately .5-second after reversing into load point and does not go Ready until approximately .5-second after termination of a Rewind.

$\overline{\text{ONLINE}}$ - On line. A level that is low when the selected transport is manually switched on line (to place it under remote control).

$\overline{\text{REWINDING}}$ - Rewinding. A level that is low while the selected transport is rewinding. The level remains low until the transport completes the automatic "return to load point" sequence but the transport does not become Ready until approximately .5 second after the $\overline{\text{RWD}}$ signal terminates.

$\overline{\text{FPT}}$ - File Protect. A level that is low when the selected transport has a supply reel of tape mounted that does not have a write-enable ring installed.

$\overline{\text{LDP}}$ - Load Point. A level that is low when the selected transport's beginning-of-tape reflector is located under the photo sensor, interlocks are made, and the initial load or rewind sequence is completed.

$\overline{\text{EOT}}$ - End of Tape. A level that is low when the end-of-tape reflector is under the photo sensor in the selected transport. This signal is not staticised and neither the positive nor negative-going transition is "clean".

$\overline{\text{SINGLE}}$/DUAL – Head Stack. A level that reports the selected transport head type. Low for single stack, high for dual stack "read while writing".

7 TRK/9 TRK – Transport Type

Low = 9-track
High = 7-track

$\overline{\text{DDI}}$ – Data Density Indicator

Low = High Density Selected
High = Low Density Selected

2.2.2.2 Read Data & Read Clock

$\overline{\text{RDP}}$, $\overline{\text{RD0}}$ through $\overline{\text{RD7}}$ – Read Data

2.2.2.3 Read Data & Clock

The read data is completely "buffered" in a special register. The data is allowed to change until just before the leading edge of the read strobe pulse ($\overline{\text{RSTROBE}}$) and is static throughout $\overline{\text{RSTROBE}}$ and until a minimum of 1 μs after $\overline{\text{RSTROBE}}$.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section contains information on the operation of the NRZI Magnetic Tape Controller.

The information in this section is divided into two major topics. A discussion of the block diagram (Figure 3-1) is presented first, to provide an overall functional description and to illustrate the relationship between the formatter portion, the adapter portion and a discussion of the command execution, illustrated by timing diagrams, describes operation of the Controller circuitry during execution of computer-originated instructions.

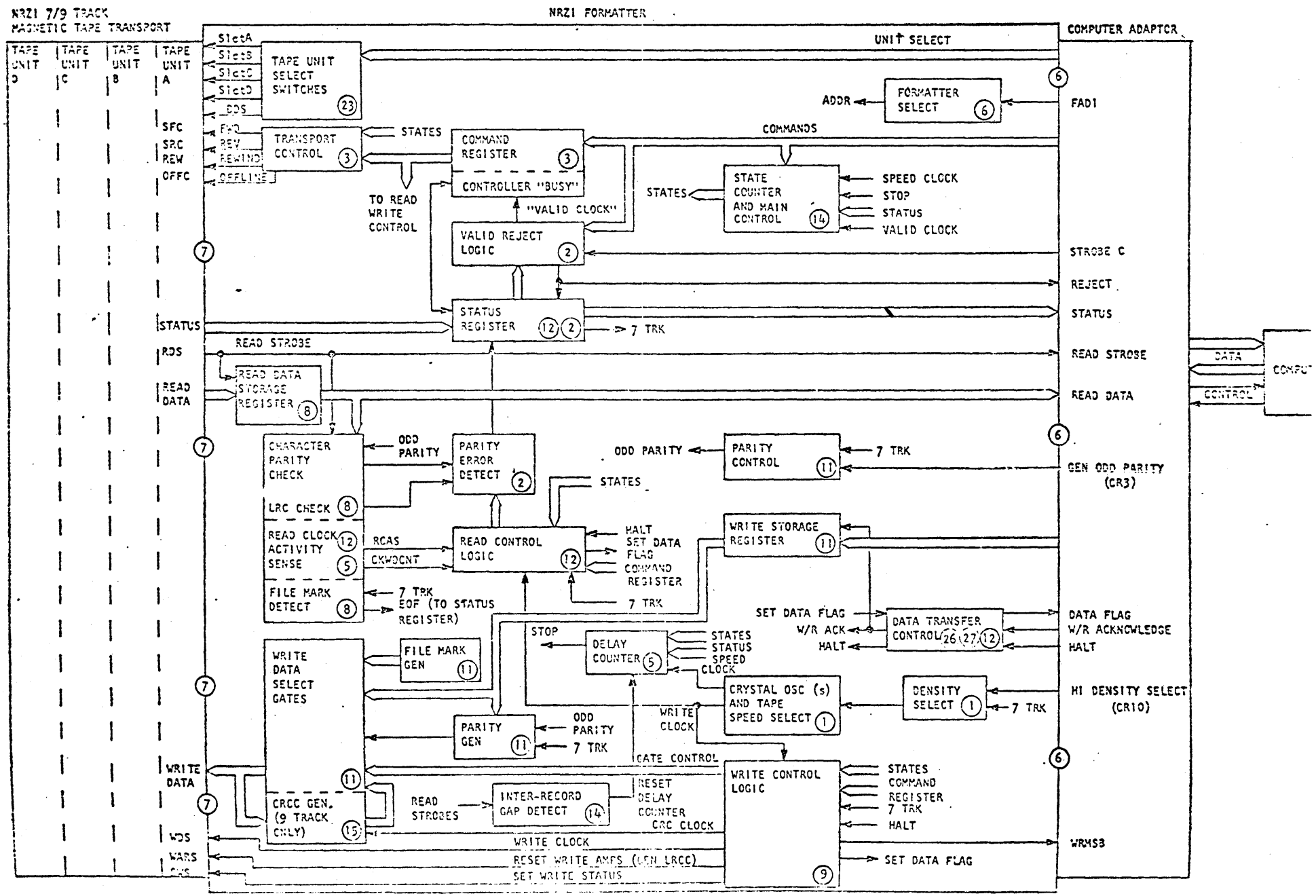
The Controller performs three basic functions. These are:

1. Control
2. Write
3. Read

The Controller provides control over the selected tape unit including all timing necessary to perform automatically all Write, Read, Rewind, Space Forward or Backward, and Rewind commands.

Upon completion of the commanded operation, status is provided so that the computer can ascertain whether the operation was performed correctly.

The Controller performs all the Write functions for erasing tape, writing a file mark or writing a record of data. A 3.5-inch gap is automatically erased before the first record when starting from beginning of tape (BOT). The correct timing delays for erasing the inter-record gap (IRG) are provided and the file-mark code is developed by the formatter portion of the Controller.


NRZI 7/9 TRACK
MAGNETIC TAPE TRANSPORT
NRZI FORMATTER
COMPUTER ADAPTOR
TAPE UNIT D
TAPE UNIT C
TAPE UNIT B
TAPE UNIT A
SletA
SletB
SletC
SletD
RDS
TAPE UNIT SELECT SWITCHES
23
UNIT SELECT
FWD
REV
REWIND
OFFLINE
SFC
SRC
REW
OFFC
TRANSPORT CONTROL
STATES
TO READ WRITE CONTROL
COMMAND REGISTER
CONTROLLER "BUSY"
"VALID CLOCK"
COMMANDS
ADDR
FORMATTER SELECT
FAD1
STATE COUNTER AND MAIN CONTROL
SPEED CLOCK
STOP
STATUS
VALID CLOCK
VALID REJECT LOGIC
STROBE C
REJECT
STATUS REGISTER
7 TRK
STATUS
READ STROBE
RDS
READ DATA STORAGE REGISTER
READ DATA
DATA
CONTROL
CHARACTER PARITY CHECK
ODD PARITY
PARITY ERROR DETECT
LRC CHECK
READ CLOCK ACTIVITY SENSE
RCAS
CKWDCNT
READ CONTROL LOGIC
HALT
SET DATA FLAG
COMMAND REGISTER
FILE MARK DETECT
EOF (TO STATUS REGISTER)
PARITY CONTROL
GEN ODD PARITY (CR3)
WRITE STORAGE REGISTER
SET DATA FLAG
W/R ACK
HALT
DATA TRANSFER CONTROL
26
27
12
DATA FLAG
W/R ACKNOWLEDGE
HALT
STOP
DELAY COUNTER
STATUS
SPEED CLOCK
WRITE DATA SELECT GATES
FILE MARK GEN
CRYSTAL OSC (s) AND TAPE SPEED SELECT
DENSITY SELECT
HI DENSITY SELECT (CR10)
PARITY GEN
WRITE CLOCK
GATE CONTROL
WRITE DATA
CRCC GEN. (9 TRACK ONLY)
READ STROBES
INTER-RECORD GAP DETECT
RESET DELAY COUNTER
CRC CLOCK
WRITE CONTROL LOGIC
WRMSB
WDS
WDRS
WRITE CLOCK
RESET WRITE AMPS (GEN LRCC)
SET WRITE STATUS
SET DATA FLAG

The task of writing is reduced to mere transfer of the characters on a demand-response basis for the computer-adapter logic.

The Controller also reduces the reading and spacing operations to a minimum by performing all parity checks and positioning of the head in the IRG's automatically. The task of reading is reduced to transfer of the characters on a demand-response basis.

The Controller can accommodate as many as four magnetic tape transport units simultaneously. All input/output signal lines are daisy-chained to the tape transports. Only the selected tape transport unit will respond to the Formatter commands. Select is determined by unit-select switches located on each tape unit.

3.2 BLOCK DIAGRAM

A simplified block diagram of the NRZI Formatting logic is shown by Figure 3-1. The block diagram illustrates the various functions performed by the standard 7-track, 9-track NRZI Controller and shows the relationship between the control, the tape transport units, and the computer adapter section.

3.2.1 Command Register & Valid/Reject Logic

When a command is output from the computer, the command and a strobe pulse are delivered from the computer-adapter segment to the Controller valid-command-detect logic. If the command is acceptable, a "valid" clock is generated to enable the command to be loaded into the command register. If the command is not valid, a "reject" pulse is returned to the computer adapter. Each "valid" clock initiates a system reset (SRS) pulse, which is, in turn, used to reset the Formatter to initial conditions.

3.2.2 CBUSY

The "valid" clock also sets the controller-busy flip-flop. The controller-busy flip-flop normally is used by the computer adapter to signal termination of all commands. The transport control logic resets the controller-busy flip-flop after all tape motion has ceased for the commanded function. If "on-the-fly" writing or reading is desired, the Data Busy status must be utilized by the computer to initiate the next command as soon as Data Busy terminates.

3.2.3 Transport Control

The transport control logic develops the forward, reverse, rewind and offline commands to the selected tape transport unit under control of the command register and the state counter.

3.2.6 State Counter and Main Control

The State Counter breaks the major operations (such as write and read) down into successive sub "states" that are sequentially stepped-through to perform the operation. These states are:

State Count	Function
0	Reset
1	Predelay (not BOT and not 3-inch gap)
2	Predelay (BOT or 3-inch gap)
3	Write or Read execution
4	Postdelay
5	Forward Motion Halt time out
6	Reverse Motion Halt time out
7	Rewind or Clear execution

The "delay" and "time out" states all use the Delay Counter to determine when the state count should terminate and the next state count entered. These delay count times vary, depending upon such factors as:

1. Tape speed
2. Single or dual-stack head
3. Edit or normal mode
4. Reverse or Forward motion
5. Seven or nine track tape unit selected

The pre and post delays are used to erase the inter-record gaps (IRG) and to halt the head in the correct position in the IRG when reading.

State 0 (the "rest" state) is the state the Controller enters after completing an operation.

State 1 (Predelay) is used to wait for the tape unit to get up to speed and to erase part of the IRG when writing. State 1 is used for predelay when not starting from BOT or not erasing a 3-inch gap.

State 2 (Predelay) is similar to State 1 except a longer delay is implemented to handle the 3-inch gap erased automatically at BOT and the Erase-3-Inch-Gap command.

State 3 (Write or Read Execution) is the State during which the record is written or read. When reading, State 3 is terminated when no more Read strobes occur (indicating the IRG has been reached).

IRG detection also terminates State 3 for Write operations when using a dual-stack read-after-write tape unit (so that the written record can be checked for correct parity). For single-stack writes, State 3 is terminated as soon as the LRC character is written at the end of the record.

State 4 (Postdelay) halts the head in the correct position in the IRG when reading. When writing, State 4 postdelay erases a portion of the IRG.

State 5 (forward motion halt time out) retains memory of the forward direction of motion during the time between the command to stop and the actual stop time. This delays termination of the CBUSY signal until the tape unit has completely halted in the IRG.

The DBUSY status terminates when State 5 is entered. Thus, successive "Writes" or successive "Reads" may be executed on-the-fly, without stopping in the IRG's.

State 6 (reverse motion halt time out) is similar to State 5 except for reverse motion commands. When performing on-the-fly operations, successive commands issued after DBUSY terminates but before CBUSY terminates must be of the same type. A Read cannot follow a Write and a forward motion command cannot follow a reverse motion command (or vice versa). There is, of course, no such restriction if the commands are not issued until after CBUSY terminates.

State 7 (Rewind or Clear) is entered upon issuance of a Rewind or Clear command by the computer. The state is terminated when the tape unit finishes rewinding.

3.2.7 Status Register

The Status Register stores both the tape unit the the Controller status. This makes it possible for the computer to inspect the results of an operation to find out whether it was completed correctly or if some other action must be taken.

The status of the selected tape unit and the Controller are available for access by the computer at any time.

3.2.8 Parity Control

The Parity Control logic provides manual or program control over selection of odd or even parity for 7-track tape units. Odd parity is automatically selected for 9-track tape units. The output (odd parity) is used by the Parity Generator and Check logic.

3.2.9 Parity Error Detect

The Parity Error Detect logic searches for one or more parity errors in each tape record. Any detected errors cause the Parity Error Status bit to be set.

The Read Control logic uses the Read Clock Activity Sense logic (RCAS) output to enable the Parity Error Detect logic to inspect the Character Parity Check output only during the data portion of a record (since CRCC (9-track) and LRCC (7-track) can exhibit either odd or even parity).

The output of the LRC Check logic is inspected only after the entire record (including CRCC and LRCC) has been read.

3.2.10 Character Parity Check :

The Character Parity Check logic checks each character read from tape for either odd or even parity.

3.2.11 LRC Check

The Longitudinal Redundancy Character Check logic checks for an even number of 1's for each individual track down the length of the record, including the CRC and LRC characters.

3.2.12 Read Data Storage Register

The Read Data Storage Register stores each tape character at the leading edge of the Read Strobe in such a manner that the Read Data is static to the computer adapter interface throughout the entire period until the leading edge of the next Read strobe occurs. This deletes the requirement for a storage register in the computer adapter section. This register would otherwise be required to retain the data for the maximum possible time after the Data Flag is set, to give the computer the maximum amount of time to accomplish the data transfer.

The outputs of the Read Data Storage Register are routed to the rest of the logic where Read data is utilized on the Controller.

3.2.13 Read Clock Activity Sense

The Read Clock Activity Sense logic separates the data portion of each record from the CRC and/or LRC characters in the forward direction. Thus, the Set Data Flag (in the Read Control logic) is allowed to operate only for the data portion of the record, which "strips" off the CRC and/or LRC characters.

The check word count (CKWDCNT) pulse occurs just after the last data character but before the CRC or LRC character's Read Strobe destroys the contents of the Read Data Storage Register. The CKWDCNT pulse is delivered to the Computer Adapter interface, where it may be used to create an extra data transfer request to the computer for the case where an odd number of characters were read from tape and the "Pack" mode of operation is being used. The CKWDCNT pulse is also typically used by the Computer Adapter to determine if the expected number of characters were read from tape to create status bits which can inform the computer that the record was too long, too short and/or contained an odd number of tape characters.

3.2.14 File Mark Detect

The File Mark Detect logic checks for 7-track or 9-track file marks, depending upon which type of tape is selected. The EOF status bit is developed if a file mark is detected in a forward or backword direction.

3.2.15 Read Control Logic

The Read Control logic controls data transfer during State 3 until the IRG is detected, at which time the Postdelay (State 4) or one of the Halt delays (State 5 or 6) is entered.

The Set Data Flag signal is generated for each Read Strobe that occurs as long as RCAS indicates that the data portion of the record is present and the Halt signal hasn't occurred.

When the IRG is detected or the computer generates the Halt signal (to indicate that it doesn't want any more data), there are no more Data Flag signals generated even though there may be more data in the record.

The Read Control logic also controls the forward and reverse space operations. These operations are identical to reading forward or reverse except that the Data Flag is not set for data transfer requests. All parity checks are valid for the spacing operations as well as for the reading operations and for read-after-write operations when a dual-stack head is employed on the selected tape unit.

In the special, Test Read, mode, the CRC and/or LRC characters are not separated from the data in the Forward Read operation. This mode is used to check the CRC and LRC generator logic with diagnostic programs.

3.2.16 Write Storage-Register

The Write Storage-Register is provided so that the Computer Adapter does not need a register to store computer output data. The Data Transfer logic operates on a request/response basis via the Data Flag and Write/Read Acknowledge (W/R ACK) signals. Each data character is requested a full write-clock-period before it is needed. The computer can respond any time within this period with a W/R ACK strobe pulse to load the Write Data into the Write Storage Register.

3.2.17 Parity Generator

The Parity Generator creates odd or even parity for each character presented from the Write Storage Register and sends the parity bit to the Write Data Select Gates. The Parity Control logic determines whether odd or even parity is generated.

3.2.18 Write Data Select Gates

The Write Data Select Gates consist of three sets of gates that are enabled by the Write Control logic to gate the Write data (and parity bit) or the File Mark code or the CRC Character onto the write data bus to the tape units.

3.2.19 File Mark Generator

The File Mark Generator generates the appropriate file mark. This may be a normal 9-track file mark, a special 9-track file mark or a 7-track file mark. The Write Control logic gates the file mark code onto the write data bus at the appropriate time and generates a Write Clock to write the file mark.

The special 9-track file mark is an option that writes the 7-track file mark code to provide compatibility with some computer manufacturer's hardware and software when writing in the "unpack" mode on a 9-track tape.

3.2.20 CRCC Generator

The Cyclic Redundancy Check Character (CRCC) Generator calculates the CRC Character while writing each record as each data character while writing each record as each data character appears on the write-data bus.

At the end of the record (9-track only) the Write Control logic gates the CRCC onto the bus and generates a Write clock pulse to write the CRC Character. The LRC Character is then written to finish the record. The CRCC may be all zeros and may exhibit odd or even parity.

3.2.21 Write Control Logic

The Write control logic operates during State 3 for write, erase and write-file-mark operations. The Write control logic controls the Data Transfer logic for write operations by developing the Set Data Flag pulse to request each character to be written until the Write operation is terminated by the Halt signal from the Computer Adapter.

Upon receiving the Halt signal, the CRC and/or LRC character is automatically appended to the record and part of the IRG is then erased. If a single-stack (read/write) tape unit is selected, the Write Control logic triggers the State Counter to the State 4 postdelay when it finishes writing the LRC Character at the end of the record. If a dual-stack (read after write) tape unit is selected, the Inter-Record Gap Detect logic is utilized to exit State 3 to State 4 postdelay in order to allow all of the record to be read-after-write parity checked.

The data rate is developped from the write clock frequency (from the Crystal Oscillators) and the tape-speed-select logic.

The Write Control logic also sends the Write Most Significant Byte (WRMSB) signal to the Computer Adapter. This enables the odd/even characters to be separated when "unpacking" a computer word into two sequential tape characters.

3.2.22 Crystal Oscillators and Tape Speed Select

The Crystal Oscillators provide stable precision clock frequencies for packing densities of 800/556/200 bits per inch. One set of crystals covers the standard tape speeds from 12.5 to 75 ips. The Tape Speed Select and Density Select logic divides down the clock rates to the appropriate frequencies and selects the write clock frequency as determined by tape speed and packing density.

The Speed Clock signal is used by the Delay Counter to provide all the precise time delays for the Formatter. The Speed Clock is dependent only on tape speed.

3.2.23 Density Select

The Density Select logic provides control over selection of Hi or Low density for 7-track tape units. Nine-track tape units are automatically operated at only 800 BPI. The Density Selection is controlled by the computer program via the Hi Density Select signal.

3.2.24 Data Transfer Control

The Data Transfer Control operates in conjunction with the Read or Write Control logic depending upon whether a Read or a Write operation is active.

The Read or Write Control logic generates the Set Data Flag pulse to signal that Read data is ready for input or to request a Write Data character. The Computer Adapter returns the W/R ACK signal, which clears the Data Flag and is used to strobe the Write data into the Write Storage Register for write operations. When the Computer Adapter desires to halt data transfer, it generates the HALT signal and the Data Flag signal is disabled.

3.2.25 Delay Counter

The Delay Counter is a flip-flop divider chain that counts the Speed Clock pulses to provide precise time intervals for Pre-, Post-, and Halt delays. The time interval begins when the counter starts counting (from a reset condition) and ends when the STOP signal is generated by the gates that decode various counts from the Delay Counter. The gate selected for a particular time interval depends upon which state the Controller is in as well as its configuration and the selected tape unit (provided by the STATUS signals to the Delay Counter).

3.2.26 Inter Record Gap Detector

The IRG Detector triggers the Formatter from State 3 to the Post Delay State 4, of Halt Delay State 5 or 6 when completing any Read or Space operation or any Write operation with a dual-stack, read-after-write tape unit. The IRG Detector resets the Delay Counter with each Read strobe. After the Read strobes stop, the Delay Counter is allowed to count for a prescribed interval until the STOP time is reached, at which time State 3 is terminated.

3.3 COMMANDS

3.3.1 Basic Commands

Basic Commands provided by the Formatter are:

1. Read (one record)
2. Write (one record)
3. Space
4. Write File Mark
5. Erase 3-inch gap
6. Rewind
7. Offline
8. Clear

3.3.1.1 Read and Space

The Space operations can be a single or multiple record under control of the STOP SPACE Computer Adapter signal. In addition, the backspace operation can be conducted in the EDIT mode. This is to position the Write head correctly in the IRG preceeding a record that is to be replaced with an equal length but updated record. BOT will halt backspacing automatically.

3.3.1.2 Write, Erase 3 Inch Gap and Write File Mark

The Erase-3-Inch-Gap command can be performed by itself or combined with the Write or Write File Mark commands to cause a 3-inch gap to be erased prior to writing the record or file mark. A Write command can be performed in the Edit mode (if the record to be replaced has first been backspaced over in the Edit mode to position the head correctly) to replace a record with an equal length record of updated information.

3.3.1.3 Rewind and Offline

The Rewind command causes the selected tape unit to rewind to Load Point (Beginning of Tape). The Controller goes "Busy" until the rewind is terminated (to provide a means of interrupting the computer upon termination of the operation).

The Offline command never sets the Formatter to the "Busy" state and may be sent to a selected tape unit even if the tape unit is "Not Ready" because it is performing a rewind operation.

3.3.2 Command and Mode Combinations

The list of possible commands executable by the Formatter depends upon the "mode" lines and are listed in Table 3-1.

NOTE 1 The GEN ODD PARITY and HIGH DENSITY mode lines are ignored for 9-track tape units. The GEN ODD PARITY line controls whether odd or even parity is written or checked for. The HI DENSITY line controls the written character packing density and the period of time allowed between read strobes in the Read Clock Activity Sensor Circuits.

TABLE 3-1. COMMAND & MODE COMBINATIONS

FORMATTER	"SET XXX" COMMAND SIGNALS									"MODE" SIGNALS					
	REV	WCC	WFM	GAP	FSR	RCC	CLR	REW	OFL	GEN ODD PARITY	HI DENSITY	EDIT	TRD	STOP SPACE	CD
1. Test Read Forward						X				1	1		X		5
2. Read Forward						X				1	1				5
3. Write 1 Record (normal)		X								1	1				
4. Write 1 Record (edit)		X								1	1	X			
5. Space Forward 1 Record					X					1	1				5
6. Space Forward "n" Records					X					1	1			4	5
7. Space Reverse 1 Record	X									1	1				5
8. Space Reverse "n" Records	X									1	1			4	5
9. Space Reverse (edit mode)	X									1	1	X			5
10. Write File Mark			X							1	1	6			5
11. Erase 3 Inch Gap				X											
12. Erase 3" then Write File Mark			X	X											
13. Erase 3" then Write 1 Record		X		X						1	1				
14. Rewind								X							
15. Off-line									X						
16. Initiate Rewind then Offline								X	X						

SEE NEXT PAGE FOR NOTES 1-4

3.9.3 Input/Output Transfer (IOT) Control Pulses

The memory extension register allows the three least-significant bits of the computer AC register to be stored in the computer adapter memory-extend register to provide a three-bit extension of the address to the computer. Control and status information is transferred via IOT instructions by the program. In order to effect transfer of the control and status information, the IOT decoder is utilized to gate the three IOP pulses (IOP1, IOP2, and IOP4) to the various logic elements of the computer adapter when the six-bit device-select address code for the tape controller is present on the computer MB register bus. The IOT control pulses are referenced on the block diagram by the actual octal IOT instruction code. The following gives the basic uses of the IOT's by octal code.

OCTAL CODE	INSTRUCTION
-6701	Skip on Error Flag or MTF set
-6702	Clear AC
-6706	Status —▷ AC
-6711	Skip on Controller Ready
-6712	Clear Flags and Control Register
-6714	Inclusive -OR AC—▷ Control Register
-6716	AC—▷ Control Register and Clear Error Flag/MTF
-6717	AC— ▷ Control Extension Register (Mode, Offline, Memory Ext.)

AC

6	7	8	9	10	11	
1	X	X	X	X	X	= Offline Mode
X	X	1	X	X	X	= Edit Mode
X	X	X	0	0	0	= 1st 4K of core memory
X	X	X	0	0	1	= 2nd 4K of core memory
X	X	X	0	1	0	= 3rd 4K of core memory
X	X	X	0	1	1	= 4th 4K of core memory
X	X	X	1	0	0	= 5th 4K of core memory
X	X	X	1	0	1	= 6th 4K of core memory
X	X	X	1	1	0	= 7th 4K of core memory
X	X	X	1	1	1	= 8th 4K or core memory

-6721	Skip on Tape Unit Ready
-6722	MTGO (initiate command)

3.9.4 AC Outputs

The twelve outputs of the Computer Accumulator (AC) register are wired to the inputs of the Computer Adapter control register, the Control Register Extension and the Prog. I/O option to the Write storage register. IOT 6714 will "inclusive-OR" the AC register into the control register. IOT 6716 will replace the contents of the control register with the contents of the AC regi ter. IOT 6712 will clear the control register and the MTF or the EF. IOT 6717 will load the AC register into the control Extension register.

3.9.5 AC Inputs

IOT 6706 first clears the AC register, then gates the contents of the status register through the input gates to the AC register. Since the AC register is cleared automatically by IOT 6706, there is no need for the program to clear the AC register first.

3.9.6 Interrupt/Skip

Control register bit 9 enables the interrupt logic so that the computer is interrupted if either the EF or MTF flag is set. The program may test for the tape controller Interrupt by generating OPT 6701. IOT 6701 will cause a skip pulse to be generated if either the EF or MTF flag is set. IOT 6712 may then be used by the interrupt subroutine to clear the interrupt flags. The computer program may also test for Tape Transport Unit and/or Tape Controller Ready by using IOT 6721 to test for Transport Ready status, and IOT 6711 to test for Controller Ready status.

Once the control codes have been transferred into the computer adapter control register, the tape-transport controller can be signalled to initiate the operation defined by the decoded commands by execution of IOT 6722 (Mag Tape Go). IOT 6722 causes the STROBEC pulse to be generated. The STROBEC pulse then transfers the decoded command into the tape transport controller command register (if the command is a "valid" one) and initiates the operation. When the operation is complete, the status lines may be sampled by the computer program to test for satisfactory completion of the operation. The computer program is signalled that the operation is complete by the EF or MTF flags. These two flags are set from the tape transport controller 2-CBUSY flip-flop, and generate an interrupt if bit 9 is set in the control register. If the command is not a valid one, the "Reject" status bit is set and the Error Flag is set.

Actual data transfer into or out of core memory is controlled by the data transfer logic. The data transfer logic operates the data break mode.

3.9.7 Data Transfer

The data transfer logic interfaces with the tape transport controller via the Data flag and the HALT and Write/Read Acknowledge (W/RACK) signals. The data transfer logic interfaces with the computer via the OMNIBUS and the control lines called BREAK REQ, XFER DIRECTION IN, THREE-CYCLE, WC OVERFLOW, and ADDRESS ACCEPTED, etc.

The THREE-CYCLE control line is always set to the three-cycle state because all transfers are in the three-cycle data break mode.

The XFER DIRECTION IN line indicates to the computer data-break facilities whether the data transfer is to be into core memory (in the case of a Read operation) or out of core memory (in the case of a Write operation).

The BREAK REQ signal is used for each twelve-bit data transfer to be made. The Data flag sets the BREAK REQ for each twelve-bit word transfer into core memory during the Read operation; the Data flag sets the BREAK REQ for each twelve-bit word transfer out of core memory during the write operation.

For write operations, the data output from the computer MB register is split into two successive six-bit characters for 7-track or 9-track core dump operations by the unpack gates. The unpack gates deliver the two successive characters to the Controller on the Write Data bus. For 9-track operations (not in the core dump mode), only the eight least-significant bits of the twelve-bit computer words are utilized. Similarly, for Read operations, two successive six-bit characters are packed into the twelve-bit Read storage register by the pack gates in 7-track or 9-track core-dump modes before inputting to the computer MB register. For normal 9-track operations, the eight-bit tape characters, plus the parity bit, are gated to the nine least-significant bits of the computer MB register bus.

3.9.7.1 Break Requests

When a break request has been initiated by a device, the device at time-state 4 must verify that it is the highest-priority break request device for that particular cycle. This is done by enabling the accumulator bits for all priority levels higher than the priority assigned to the requesting device, and checking time-state 4 to see if any of the higher-priority devices are also breaking. If not, a "go" signal is given to the break device and the break is continued with the requesting device.

When a break request cycle is initiated, a latch is set that tells the computer that there is a break in progress. This also enables a signal called CPMA DISABLE, which takes the control of the memory-address bus away from the CPU and allows the breaking device to control the address bus from the memory address register. As soon as the break device has this capability, a three-cycle break is initiated.

During the word count portion of the three-cycle break, the memory address bus allows the hard-wired address (which is pre-wired using chip G6) f or the current address number. This hard-wired address is gated on the bus less the least significant bit, to show the computer where the word count is located.

Again, a priority check is made at the end of the word count cycle to see if another, higher-priority, device has made a break request. If not, the device will continue with cycle 2 and the hard-wired address, with the least-significant bit, will go to the current address on the address bus.

At time 3 of the second cycle, the memory data on the bus is stored in the register to give the current address location that will be used for the third cycle of the break. During the third cycle, the data will be transferred to the address that is stored in the buffer either to put data into the core during a Read mode, or take it out of core for a Write operation.

During the word count and current-address portions of the break cycles, the data that is brought out of the word count and current address locations is incremented before being restored into memory by a signal called INCR. This incrementing is done at the beginning of the cycle to increment the location before the transfer is completed. If, during the word count portion of the cycle, the word count in the location overflows to zero, a word count overflow signal is generated that terminates the data-transfer portion and halts transfer until the next Write or Read operation is commanded by the computer.

If, during a Read mode, the Word Count Overflow is initiated before the end of the record, the record will continue to be read but no more data will be placed into the core. This Word Count Overflow signal also generates the Halt signal, which shuts off the data gate and, in a Write mode, causes the controller to start the countdown for writing the CRC and LRC character.

On a nine-track machine the CRC will be valid; on a seven-track machine the CRC will not be written. If, during any three-cycle operation, it is determined at time 4 of the computer cycle that a higher-priority device is also requesting, the controller will hand in its present state, holding all data and control functions, until the next computer cycle, and at time-state 4 will again check to see if it has priority. When there are no priority-request devices of a higher priority requesting, then the device will continue and complete the three-cycle break.

3.9.9 IOT Instructions

3.9.9.1 Skip on Error Flag (EF) or Mag Tape Flag (MTF)

MTSF - Octal 6701

The state of the EF and MTF status bits is sampled. If either (or both) is set, a pulse is returned on the skip bus to skip the next sequential instruction. This instruction allows the program (when interrupted) to test the tape controller to ascertain if the tape controller is generating the interrupt. The EF- and MTR-generated interrupt is not cleared until either a "Clear Register and Flags" or "Load Control Register" (MTLC) IOT instruction is executed; hence, the LON LOT instruction (octal 6001) should not be executed to enable interrupts until after the MTAF or MTLC instruction is executed in the magnetic tape interrupt service subroutine.

3.9.9.2 Clear AC

Octal 6702

Clears AC register.

3.9.9.3 Read Status

MTRS - Octal 6706

Status register is loaded into AC.

3.9.9.4 Skip on Tape-Controller-Ready

MTCR — Octal 6711

This instruction allows the computer program to test the tape transport controller status (busy or not busy).

3.9.9.5 Clear Register and Flags

MTAF — Octal 6712

This instruction clears the status and control registers (including EF and MTF interrupt flags) if the tape controller is ready. If the tape controller is not ready, this instruction clears only the EF and MTF flags.

3.9.9.6 Inclusive-OR AC Into Control Register

MTCM — Octal 6714

This instruction transfers three command bits (AC_6, AC_7, and AC_8) and three select bits (AC_0, AC_1, and AC_2) into the control register and "inclusive-OR's" the rest of the AC into the control register.

3.9.9.7 Load Control Register

MTCL — Octal 6716

The load control register instruction produces different results, depending upon the status of the tape-transport controller (i.e., busy or not busy).

a. Controller Not Busy - The EF and MTF flags are cleared. The contents of the AC register are loaded into the control register, thereby selecting the designated tape transport unit.

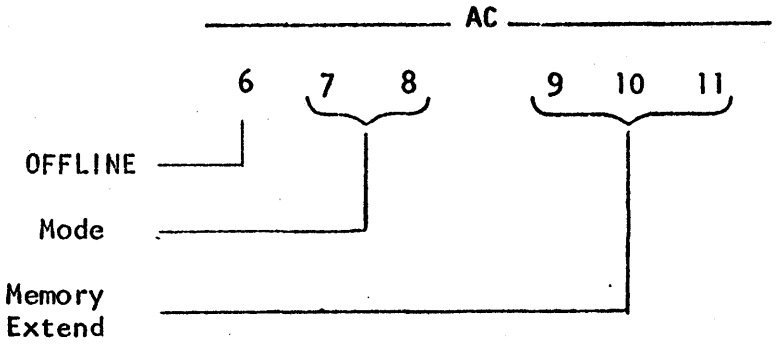
b. Controller Busy - The EF amd NTF flags are cleared. Bits 3, 4, 5 and 9, 10, 11 of the AC register are "inclusive-OR'ed" into the corresponding bits of the control register, while bits 0, 1, 2, 6, 7 and 8 (select and command code) replace corresponding bits of the control register.

3.9.9.8 Load Control Register Extension

Octal 6717

This instruction causes the least-significant six bits of the computer AC register to be loaded into the control extension register. The control extension register extends the most-significant end of the CA to allow addressing of up to 32K memory. It also provides mode control over the EDIT function, the marginal-read threshold for single-gap read-checking of each record after it is written (THR1), and the low data recovery read threshold Z (THR2). The OFFLINE command bit is also located in the control extension register.

Control Register Extension Format



Mode		
7	8	
0	0	Normal
0	1	Edit
1	0	THR1
1	1	THR2

NOT USED

Memory Extend			4K Core Addressed
9	10	11	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

The computer START switch causes the tape controller to reset the extension register to 000 (baskc 4K memory).

3.9.9.9 Skip on Tape-Transport-Ready

MTTR — Octal 6721

This instruction allows program to test the selected tape transport unit status (ready or not ready).

3.9.9.10 Mag Tape GO

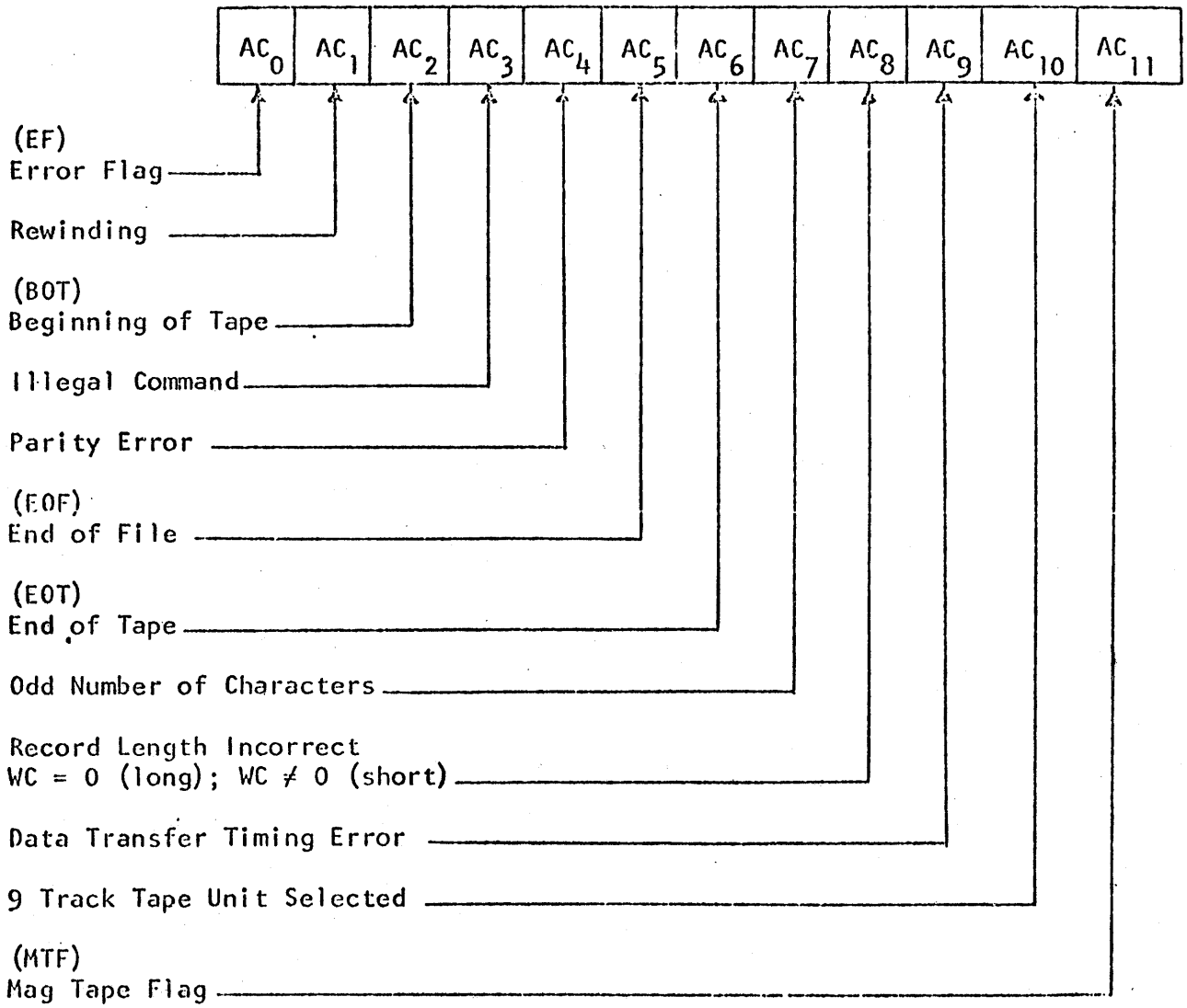
MTGO — Octal 6722

This instruction causes the controller to execute the command present in bits 6, 7, and 8 of the control register (if a legal command). It also causes bit 5 (Erase 3" Gap) of the control register to be reset to zero if on. MTGO can be jumper-selected to load the control extension register from the AC register instead of IOT 6717. This gives control over the OFF-line command, edit mode, RTHR1 and RTHR2 modes and memory extension with MTGO.

3.9.10 STATUS WORD FORMAT

The status word is input to the computer AC register with an MTRS (Mag Tape Read Status) IOT instruction, octal 6706.

STATUS WORD INPUT TO THE COMPUTER AC REGISTER



3.9.11 Error Flag (AC_0)

The Error Flag (EF) sets if any error status bit (AC_4, AC_6, AC_8, or AC_9) is on when MTF is set at the conclusion of an operation, or if an illegal command is attempted. MTF is not set for the illegal command case. EF causes an interrupt if bit 9 is set in the control register. The status or MTF or EF can be tested with IOT instruction 6701 (MTSF) Mag Tape Skip on Flag Set. EF may be reset (to clear the interrupt condition) by IOT MTLC (Load Control Register) or MTAF (Clear Registers and Flags).

3.9.12 Rewinding (AC_1)

Set while selected tape transport unit is in rewind mode.

3.9.13 Beginning-Of-Tape (AC_2)

Set while selected tape transport unit is on the beginning-of-tape (BOT) marker.

3.9.14 Illegal Command (AC_3)

Illegal commands are:

a. MTGO command is issued when tape controller is busy

b. MTGO command is issued to a tape transport unit that is not ready (even though tape controller may be ready).

c. Write-One-Record or Write EOF command is issued when no write-enable ring is in reel.

d. Space-reverse command is issued when at BOT. If the tape requires movement to reach BOT on a space reverse, then the result is not an illegal command.

e. An MTGO command when bits 6, 7, and 8 of the control register are set to 000.

The EF (AC_0) status flag is set, but MTF (AD_{11}) does not set for an illegal command.

3.9.15 Parity Error (AC_4)

The parity error detection is for both vertical odd parity checks on each character and upon longitudinal even parity checks on each track throughout the entire record for an NRZI tape unit.

Once a parity error is detected, the status bit remains set until either the MTAF (6712) or MTLC (6716) instruction is issued to clear the status and control registers. Parity is checked for a Read-One-Record, a Write-One-Record, a Space Forward or a Space Reverse operation.

3.9.16 End-of-File (AC_5)

The EOF status bit is set if an end-of-file mark is encountered during any tape movement operation except Rewind.

The EOF status bit is also set if an end-of-file mark is encountered on a Space Forward or a Space Reverse. When the space commands are terminated due to a file mark, the program can interrogate WC to determine the number of records spaced over prior to encountering the end-of-file mark. The end-of-file mark is counted as a record.

3.9.17 End-of-Tape (AC_6)

The EOT status bit sets when the EOF foil is initially sensed (however, the operation is completed). At completion, both the EF and MTF status bits are set and the interrupt is generated (if enabled). The EOT status does not clear until the tape transport is commanded to Rewind or Space Reverse.

3.9.18 Odd Number of Characters (AC_7)

For 7-track or 9-track core dump Read operations, if an odd number of characters is contained within a record, this status bit is set as well as the "Record Length Incorrect" (AC_8) status bit. This occurs because there are normally two 6-bit tape characters packed into each 12-bit computer word. For odd-character record lengths, the least-significant half of the last 12-bit computer word must be discarded by the software.

3.9.19 Record Length Incorrect (AC_8)

During a Read operation, this status bit is set whenever the WC overflow does not agree with the number of words actually read. The EF is set when MTF is set upon completion of the Read operation and the Interrupt is generated (if enabled).

3.9.20 Data Transfer Timing Error (AC_9)

This status bit sets whenever a word is not transferred in time in either a Write or a Read cycle. The EF status bit is set when the MTF is set at the completion of the operation and an interrupt is generated (if enabled).

3.9.21 9-Track (AC_{10})

This status bit is set whenever a 9-track tape-unit is selected.

3.9.22 Magnetic Tape Flag (AC_{11})

The magnetic tape flag (MTF) status bit is set whenever the tape controller has completed an operation and is ready to accept the next command.

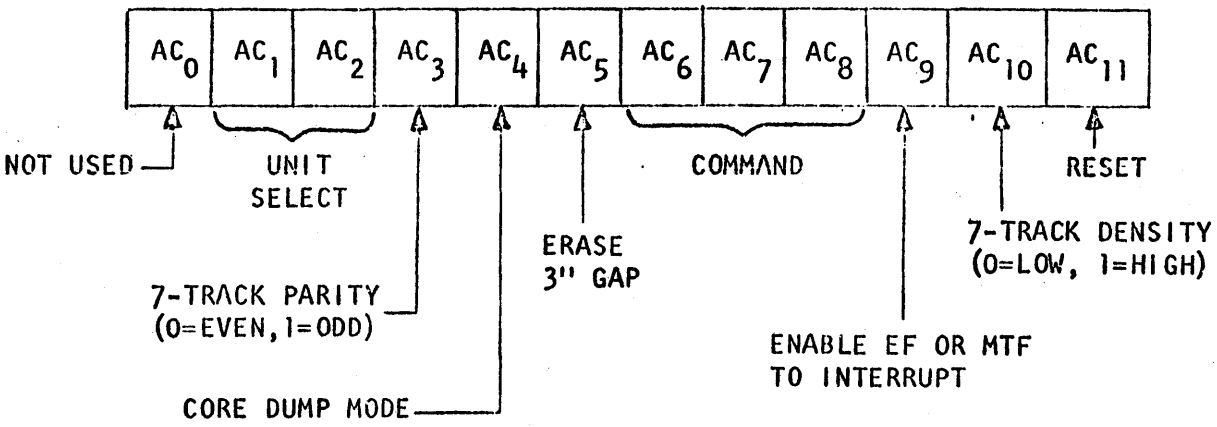
MTF causes an interrupt if bit 9 is set in the control register, When MTF goes set, the Error Flag (EF) will set if any errors are present.

MTF or EF can be tested with IOT instruction 6701 (MTSF) Magnetic Tape Skip on Flag Set.

MTF may be reset (to clear the interrupt condition) by IOT MTLC (load Control Register) or MTAF (Clear Register and Flags).

3.9.23 Control Word Format

The control register bits are illustrated in conjunction with the bits of the computer AC register:



Tape Unit Select Code		Tape Unit Selected
AC_1	AC_2	
0	0	0
0	1	1
1	0	2
1	1	3

The specified tape transport unit is selected when the control register is loaded, regardless of command.

Command Codes			
AC_6	AC_7	AC_8	
0	0	0	No operation
0	0	1	Rewind
0	1	0	Read One Record
0	1	1	Test Read
1	0	0	Write One Record
1	0	1	Write File Mark
1	1	0	Space Forward
1	1	1	Space Reverse

The NO-OP command will cause an illegal-command error. The illegal-command error sets status bit AC_3 and EF to cause an Interrupt (if enabled), if an MTGO instruction is executed while NO-OP code is present in the command register.

The control register is loaded or modified by the computer program, using either MTLC or MTCM IOT instructions. See Section 3.9.11 for commands explanation.

3.9.23.1 Erase 3" Gap (AC_5)

This causes three inches of tape to be erased. This bit may be used by itself or in conjunction with a Write or Write EOF to erase a bad section of tape. A gap will be erased on the tape if MTGO is executed and the command is Read One Record or Space Forward giving an erroneous result. This bit is always reset automatically by the tape controller upon the execution of an MTGO instruction.

3.9.23.2 Reset (AC_{11})

This bit "forces" a reset to the Formatter when IOT 6716 is generated and the jumper is installed between 23X1 and 23Y1 (see logic 22). This is useful for test purposes to halt a "runaway" tape condition and loop on one command sequence for trouble shooting.

3.9.23.3 Enable Interrupt (AC_9)

The computer will be interrupted if this bit is set, and either MTF (Magnetic Tape Flag) or EF (Error Flag), or both MTF and EF are set. MTSE IOT is used to determine whether MTF or EF caused the interrupt.

3.9.23.4 7-Track Parity (AC_3)

When the NRZI Formatter is in the "Remote" mode, this bit controls the Write/Read parity selection for 7-track tape units (0 = even parity, 1 = odd parity).

3.9.23.5 7-Track Density (AC_{10})

When the NRZI Formatter is in the REMOTE mode, this bit controls the selection of Write/Read density (0 = low density, 1 = high density).

3.9.23.6 Unit Select (AC_{1-2})

These two bits select the tape transport unit. Switches are provided on the Formatter for switching tape transport units to any of the four logical unit numbers.

3.9.23.7 Core Dump Mode (AC_4)

This mode allows complete twelve-bit memory words to be transferred as two six-bit tape characters for 9-track tape units. Bits 0 through 5 form character number 1 and bits 6 through 11 form character number 2. When employing the Read One Record command or Write One Record command in core dump mode, it is necessary to load the WC with the negative of the number of twelve-bit words (half the number of tape characters) to be transferred. The core dump mode is ignored unless the operation is a Read or Write One Record.

3.9.24 Commands (AC_{6-8})

3.9.24.1 Rewind

The Rewind command causes the selected tape transport unit to rewind to the beginning of tape. The program may initiate rewind on one unit and then immediately select a different unit and continue operating while the original unit is rewinding.

a. If the program does not execute either an MTLC (6716) or an MTCM (6714) to select a different tape transport unit prior to the termination of the rewind to the original unit, the MTF will be set on the completion of Rewind to cause an Interrupt (if enabled). The selected tape transport unit and the tape controller remain not ready until the rewind is complete so that the program can use MTSF (6701), MTCR (6711), MTTR (6721) or Interrupt to ascertain when the tape controller and tape transport unit are ready.

b. If the program executes an MTLC (6716) or MTCM (6714) to select a different tape transport unit prior to the termination of the rewind operation, the MTF will set a

short time after execution of MTLC or MTCM (providing the second tape transport unit is ready). At this time, an Interrupt will occur (if enabled) and the tape controller is ready for another command. The rewinding tape transport unit will remain Not Ready until the rewind is complete.

NOTE: This is the only time that MTF is set after execution of an MTLC or MTCM that is not followed by an MTGO (6722).

3.9.24.2 Read-One-Record

The Read-One-Record command causes the next record to be read into core memory. Records may be read forward or reverse, and both computer CA and WC core memory three-cycle data break control registers must be set up before issuing the command. The CA register must be set to the initial buffer address, minus one; the WC register must be set to the twos-complement of the number of twelve-bit computer words to be used.

If WC is set to less than the actual record length, the indicated number of words is read in and data transfer halts, although the tape continues moving until it reaches the next inter-record gap. If WC is set to greater than the actual record length, the entire record is input.

In either case, the parity checks are performed on the entire record and the MTF is set to interrupt (if enabled) when the tape transport unit halts in the next inter-record gap. If the record length does not match the WC on completion, bit 8 of the status word is set to 1, the EF is set, and the WC can be interrogated to determine if the record was longer or shorter than expected.

When reading forward, the CRC and LRC characters are stripped off by the NRZ Formatter.

3.9.24.3 Write-One-Record

The Write-One-Record command requires that the CA and WC core locations be set up before execution.

The CA register must be set to the initial core address, minus one; the WC register must be set to the two's complement of the number of twelve-bit computer words or eight-bit tape characters to be transferred (depending on whether the core dump mode is utilized). For 9-track operations, when WC overvlows (indicating the last word to be written), the three-cycle data break transfer ceases, the CRC character is written after three blank characters, the LRC character is written after three more blank characters (per IBM 9-track specifications), and a portion of the inter-record gap (IRG) is erased. The tape transport unit halts and the MTF is set to interrupt the program (if enabled. The Read-After-Write logic performs both vertical (character) and longitudinal parity checks on the written record. For 7-track operations, the CRC character is deleted and the LRC character is generated after three blank characters. If a single-gap tape unit is used, the program should backspace and read the record in threshold 1 mode to perform a marginal check on each record written. If there is a parity error, the program should backspace and erase that section of tape, then rewrite the record.

3.9.24.4 Write EOF

For 9-track NRZI operations, the Write EOF command causes an octal 023 character to be writtin on tape, seven blank characters (no CRCC), then the LRC character (which in this case is another octal 023 character). This format is per IBM 9-track specification.

The tape transport unit erases a portion of the IRG and then halts. The MTF is then set and the interrupt is generated (if enabled). The Read-After-Write logic should cause the EOF status bit to be set to indicate that the EOF has been successfully written. For 7-track NRZI operations, two even-parity octal 17's are written four character-spaces apart per IBM 7-track specification. There will not be a parity error indication for 7-track odd parity mode file marks unless the Controller enable jumper for file-mark parity errors is installed.

3.9.24.5 Space Forward

The Space Forward command requires that the computer WC core location be loaded with the two's complement of the number of records to be spaced over. The computer CA core location need not be set up since it is ignored. When WV overflows, or when EOF or EOT is detected, the tape transport unit is halted in the IRG and MTF is set to interrupt the program (if enabled). Records are spaced-over continuously without stopping in the inter-record gaps. Parity is checked and the EOF status bit is set if an EOF terminates the Space-Forward operation. A file mark is counted as a record.

3.9.24.6 Space Reverse

The Space Reverse command requires that the computer WC core location be loaded with the two's complement of the number of records to be spaced over before execution. The CA register is ignored as in the Space Forward command. When WC overflows, or EOF is detected, the tape transport unit is halted in the IRG and the MTF is set to interrupt the program (if enabled). Records are spaced-over continuously without stopping in the inter-record gap.

Detection of BOT while spacing in reverse will terminate tape movement on the BOT marker with the BOT status bit set. When BOT is detected in a space reverse operation, the tape transport unit becomes not ready for approximately 0.5 second.

The EOF status bit is set if an EOF terminates the space reverse operation. A file mark is counted as a record.

3.9.24.7 Test Read

This function is identical to a Read-One-Record command, with the exception that the tape controller will also input the LRC and CRC (NRZI only) characters to the computer in the forware mode. The WC register should be set to the two's-complement of the number of tape characters plus two (9-track) or plus one (7-track). The command is included for maintenance purposes and should not be used in the core dump mode.

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