H-552

INSTRUCTION MANUAL

DECTAPE CONTROL

552

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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TYPE 552
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CHAPTER 1
INTRODUCTION

1-1 GENERAL DESCRIPTION

The Type 552 DECtape Control transfers binary data between one of two types of DEC digital computers (i.e., PDP-5 or PDP-8) and up to eight transport drives (e.g., four Type 555 transports, eight TU55 transports or any 8-drive combination). A Type 555 DECtape transport contains two independent tape drives with relay logic to select and control the tape motion of each drive; a Type TU55 contains a single drive with solid-state logic.

Binary information is transferred between the tape transport and the computer as one 12-bit computer word approximately every 133-1/3 μsec. In writing, the Type 552 DECtape Control disassembles 12-bit computer words so that they are written in four successive lines on tape. Transfers between the computer and the control always occur in parallel for a 12-bit word. Data transfers use the data-break (high-speed channel) facility of the computer. As the start and end of each block are detected by the mark-track detection circuits, the control raises a DECtape (DT) flag which causes a computer program interrupt. The program interrupt is used by the computer program to determine the block number. When it determines that the forthcoming block is the one selected for a data transfer, it selects the read or write control mode. Each time a word is assembled or DECtape is ready to receive a word from the computer, the control raises a data flag. This flag is connected to the computer data-break facility to signify a break request. Therefore, when each 12-bit computer word is assembled, the data flag causes a data break and initiates a transfer. By using the mark-channel decoding circuits and data-break facility in this manner, computation in the main computer program can continue during tape operations. The functions performed by the Type 552 DECtape Control in these operations are described in detail in Chapters 2, 3, and 4.

1-2 TYPE 552 CHARACTERISTICS

Table 1-1 contains a summary of the characteristics of the Type 552 DECtape Control plus its associated transport equipment.

TABLE 1-1 SUMMARY OF EQUIPMENT CHARACTERISTICS FOR THE TYPE 552 DECTAPE CONTROL

552 Control	21 inches high, 19 inches wide for equipment which operates four Type 555 or eight Type TU55 transports or any combination thereof, up to eight drives.

TABLE 1-1 SUMMARY OF EQUIPMENT CHARACTERISTICS
FOR THE TYPE 552 DECTAPE CONTROL (continued)

555 Transport	10-1/2 inches high, 19 inches wide
TU55 Transport	10-1/2 inches high, 19-1/2 inches wide
Cabinet	69-1/8 inches high, 22-1/4 inches wide, 27-1/16 inches deep. Will hold a maximum of one Type 552 Control and three Type 555 Dual Transports.
Weight	
552 Control	30 pounds
555 Transport	65 pounds (rack mounted)
TU55 Transport	65 pounds (rack mounted)
Cabinet	555 pounds
Power Requirements	
552 Control	115v, 60 cps, 4 amp.
	A Type 728 and a Type 734 Power Supply are included in the Type 552 Control.
555 Transport	115v, 60 cps, 3.2 amp maximum, 1.5 amp idle.
TU55 Transport	115v ± 10%, 60 cps, 2.0 amp maximum, 1.5 amp idle.
Cabinet	115v, 60-cps source capable of delivering 20 amp.

Tape Characteristics

a. 260 feet of 0.75 inch, 1.0 Mylar tape per 3.5-inch reel.

b. 350 ± 55 lines per inch.

c. 849,036 usable lines per tape.

d. 60 lines per control zone.

e. 4096 is the maximum number of addressable blocks per reel.

f. Number of words in a block must be divisible by 3.

g. $N_B = \frac{212112}{N_W + 15} - 2$ N_B = decimal number of blocks

N_W = number of words per block

h. Capacity for 190, 000 12-bit words in blocks of 129 words.

Word Transfer Rate

a. One tape line is read or written every 33-1/3 μsec.

b. A 12-bit word is read and assembled or disassembled and written in 133-1/3 μsec.

c. In reverse direction, the transfer rate varies by 20% as the effective reel diameter changes.

TABLE 1-1 SUMMARY OF EQUIPMENT CHARACTERISTICS
FOR THE TYPE 552 DECTAPE CONTROL (continued)

Word Transfer Rate (continued)	
d. Transfers require 4.5% of PDP-5 cycles after the initial 200-msec start time.	
e. Transfers require 1.2% of PDP-8 cycles after the initial 200-msec start time.	
Addressing	
a. Mark and timing channels allow searching for a particular block.	
b. Start time is <200 msec, stop time is <150 msec, turn-around time is <200 msec.	
c. Start and stop distances are approximately 8 inches.	
d. When a command to reverse direction is issued at a given tape location, the system is up to speed when that same location passes the head after turnaround.	
Input Signals to Transport from Control	
Commands*	FORWARD, REVERSE } normally complementary levels
	GO, STOP } normally complementary levels
	ALL HALT stops transport when computer halts.
Unit Select*	Select 1 through select 8
Control	POWER CLEAR is a standard DEC negative pulse to prevent tape motion when computer power is turned on.
Output Signal from Transport to Control	
Control	WRITE ENABLE (ground level assertion)
Thermal Dissipation	2150 Btu/hour
Operating Temperature	50-95°F ambient
Humidity	10-90% relative humidity

NOTE: The magnetic tape manufacturer recommends 40-60% relative humidity and 60°-80°F as an acceptable operating environment for DECtape.

*These signals are approximately −3v or floating when supplied by a control unit designed to operate the Type 555 Dual DECtape transport which uses relay switching logic circuits; or are standard DEC logic levels of ground and −3v when supplied by a control unit designed specifically to drive the TU55.

1-2.1 Physical Details

The Type 552 DECtape Control is mounted in the lower three panels of a standard DEC computer cabinet. This arrangement requires three module mounting panels plus three standard 50-terminal interface connectors. When so mounted, up to three Type 555 or Type TU55 DECtape transports may be installed in the same cabinet.

The standard DEC computer cabinet is constructed with a welded steel frame and sheet steel covering. Double doors on the front and rear are held closed by magnetic latches. Power supplies and controls are mounted inside the rear double doors on a full-width plenum door latched by a spring-loaded pin at the top. Module mounting panels are mounted behind the double door in front with the wiring side facing outward. Fans at the bottom of the bay draw cooling air through dust filters, pass it over the electronic components, and exhaust it through the wiring and other openings in the front and top of the cabinet. Four casters provide mobile support for the system. The rear plenum door contains blank panels in the space not used by components. Control equipment used with the PDP-5 requires a Type 728 Power Supply mounted near the bottom of the door. AC power for this supply is furnished through a utility outlet which is controlled by the PDP-5 power control. A Type 734 Power Supply mounted at the top rear of the PDP-5 provides marginal-check power for the control equipment. Control equipment used with the PDP-8 requires two Type 728 Power Supplies and one Type 834 Power Control. These units are mounted near the bottom of the plenum door and a Type 734B Power Supply for marginal-check power is mounted at the top.

Standard DEC computer cabinets have access doors which extend 8-3/4 inches to the front of the cabinet and a plenum door which extends 13-3/4 inches to the rear. At least 3 feet should be allowed at both front and rear for access and maintenance. Cabinets may be bolted together at the sides to form contiguous units.

1-2.2 Electrical Details

A cable rated at 6.5 amp (8 amp surge) at 115v, 60 cps furnishes power for the Type 552 DECtape Control. This cable is terminated by a Hubbell Twist Lock plug rated at 30 amp, 25 vac.

Signal connections to and from the tape drives are made through 22-pin Amphenol connectors (similar to those used for the logic modules). When viewed from the rear, the connectors at the left of the top logic panel are for the head bus, the pair at the right of the center panel are for the control and selection buses. Signal connections from PDP-5 are made through two cables terminated by 50-pin Amphenol plugs. Three 50-pin receptacles are mounted wiring-side out at the right front of the panel just above the logic panel. A standard PDP-5 programmed in/out transfer cable plugs into the left receptacle, a data-break transfer cable plugs into the right. The center receptacle is bused to the left, allowing the programmed transfer bus to extend to other peripheral devices. PDP-8 signals are connected through eight twisted-pair cables which terminate in DEC FLIP CHIP Type W021 Cable Terminations. These terminations

plug directly into the upper sockets at the left of the connector panel above the logic. The lower FLIP CHIP sockets are bused to the upper, so that both the programmed-transfer bus and the data-break bus may extend to other peripheral devices. Either a PDP-5 or PDP-8 may be connected to the Type 552 DECtape Control, but not simultaneously. No logic or wiring changes are required to adapt the control equipment to either computer.

Signals between the Type 552 DECtape Control and the computer are the standard voltage levels for the DEC 4000-series modules, as stated in the DEC System Modules Catalog. Control and selection signals between the Type 552 and the tape transport are designed to operate relays. The energizing signal is −15v at 30 ma maximum; the common return is at ground level. During writing, the head bus carries 200 ma in either direction with a 20v peak-to-peak waveform symmetrical with respect to ground. When reading, the peak-to-peak head-voltage waveform is between 4 and 6 mv when the tape is up to speed. The internal logic for the Type 552 consists of DEC 4000-series logic modules, except for two 1000-series diode modules (which act as pulse gates for the standard 400 nsec pulses), and two 6000-series inverter modules required for fast rise-time applications. All internal signals are standard 4000-series levels and pulses, except those for the read/write amplifiers and relay drivers. Power for the Type 552 is the conventional −15v collector supply, +10v base bias supply.

The types and number of FLIP CHIP modules used in the Type 552 DECtape Control are listed in DEC engineering drawing ML-A-552-0-15 of Chapter 6. Module locations in the three mounting panels are shown in DEC drawing UML-D-552-0-18. An explanation of the conventions in this drawing is given in Chapter 5.

1-3 SCOPE OF MANUAL

This manual is intended to aid personnel in the maintenance of the Type 552 DECtape Control. The equipment is discussed primarily from a maintenance point of view, but some information is given on operation and associated controls and indicators. Pertinent documents listed in the following subsection give more complete information on operation from a programmer's viewpoint. Since the DECtape control is one element of a computer/control/transport system, the reader is advised to become familiar with the internal operations of both the computer and the appropriate transports. Of special importance are sections concerning program interrupts, programmed in/out transfers and the data-break facility in the computer; and the select and motion-control logic in the tape transport. Detailed descriptions of the instruction repertoire and programming practice for a particular computer can be found in the PDP-5 and PDP-8 handbooks. Information on the logic and motion control of the Type 555 and Type TU55 DECtape transports can be obtained from the maintenance manuals for the particular transport.

1-4 PERTINENT DOCUMENTS

The following DEC documents contain material which supplements information in this manual. These documents may be obtained from the nearest DEC office or from:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts

1-4.1 Manuals

Digital FLIP CHIP Modules (C105) - Specifications and descriptions of each FLIP CHIP module, plus simplified explanation of selection and use of these modules in numerous applications.

System Modules (C100) - Specifications and descriptions of basic system modules, plus simplified explanation of selection and use of these modules in numerous system applications.

PDP-5 Handbook (F-55) - Detailed information on the function, instructions, and programming of the three major system elements of the computer.

PDP-5 Software Package - Perforated program tapes and descriptive matter for the program assembly language (PAL) utility subroutine and maintenance programs.

PDP-8 Handbook (F-85) - Programming and operating information for the computer, including brief instructions on the Type 552 DECtape Control.

PDP-8 Maintenance Manual (F-87) - Complete information on the internal operations of PDP-8 logic, memory, basic in/out, and processor options.

PDP-8 Programming Manual (Digital-8-27-U) - Programs for PDP-8. These programs can also be used without change on PDP-5. Complete descriptions of DECtape subroutines designed for assembly with an object program, the DECtape library system, and the DECtog utility routines.

Type 555 DECtape Transport Maintenance Manual - Transport drive logic and internal operations, plus preventive and corrective maintenance instructions.

Type TU55 DECtape Transport Maintenance Manual - Transport drive logic and internal operations, plus preventive and corrective maintenance instructions.

1-4.2 Engineering Drawings

Drawing Number	Title
FPL-C-552-0-1	552 DECtape
PL-A-552-0-1	552 DECtape Parts List
BS-D-552-0-3	Status Timing and Mark-Track Decoding
BS-D-552-0-4	Flag, Error Detection, and Write Enable

Drawing Number	Title
BS-D-552-0-5	Longitude Parity Buffer and Memory Address Control
BS-D-552-0-6	Read/Write Buffer, Data Buffer, and Read/Write Amplifiers
BS-D-552-0-7	RWB,DB,WB Controls
BS-D-552-0-8	Motion and Function Control
WL-B-552-0-16	Wiring List Type 552 DECtape Control
UML-D-552-0-14	Utilization Module Location
UML-D-552-0-18	Utilization Module Location
ML-A-552-0-15	Module List

1-4.3 Replacement Schematics

Drawing Number	Title
RS-728-5	Power Supply 728
RS-B-734B-2	Variable Power Supply 734B
RS-B-1033-1	Microtape Attenuator 1033
RS-B-1113-6	Diode 1113
RS-1501-5	Level Standardizer 1501
RS-1982-5	Inhibit Driver 1982
RS-B-4102-4	Inverter 4102
RS-B-4113-9	Diode 4113
RS-B-4114-7	Diode 4114
RS-B-4115-7	Diode 4115
RS-B-4117-7	Diode 4117
RS-B-4127-6	Capacitor Diode Inverter 4127
RS-B-4129	Capacitor Diode Inverter 4129
RS-4151-8	Binary-to-Octal Decoder 4151
RS-4215-8	4-Bit Counter 4215
RS-4217-4	4-Bit Counter 4217
RS-D-4260-1	Mark-Track Decoder 4260
RS-B-4303-17	Integrating One-Shot 4303
RS-B-4401-12	Clock 4401
RS-C-4523-7	Manchester Reader and Writer 4523
RS-4671-4	BCD Light Driver 4671

In addition to the above documents, complete sets of library programs are available for each computer using DECtape systems.

A complete set of reduced engineering drawings and replacement schematics for the Type 552 DECtape Control is in Chapter 6. The engineering drawings are in addition to the complete set of full-size drawings forwarded with each DECtape control. As explained in Chapter 6, all maintenance personnel should use only the full-size engineering drawings for work on the equipment, because the full-size drawings include variations peculiar to an individual installation.

CHAPTER 2
PRINCIPLES OF OPERATION

This chapter describes the principles of operation of the Type 552 DECtape Control System by giving functional descriptions of each system element and then summarizing the programmed operation of the control system containing these elements. Brief descriptions of DECtape format, instructions, and control modes provide a background for understanding the functional operation of the system. The pertinent documents listed in Chapter 1 contain more detailed information on these programming features.

2-1 DECTAPE FORMAT

Format of the DECtape used in the DECtape transport is an important factor in the operation of the Type 552 DECtape Control. DECtape provides for ten tracks, of which three pairs are available for data and two pairs for timing and mark information (see Figure 2-1). A 10-track recording head reads and writes the five duplexed channels of the DECtape. Duplication of each track by nonadjacent read/write heads, wired in series, eliminates most dropouts due to noise and dust, and minimizes skew problems. The location of the redundant head eliminates most cross talk between tracks. In addition, the location of the timing tracks along the edges of the tape permits strobing on the analog sum of the timing-track signals and guarantees reading of the data tracks when they are in the most favorable position. The location of the data tracks in the middle of the tape also minimizes the effects of skew.

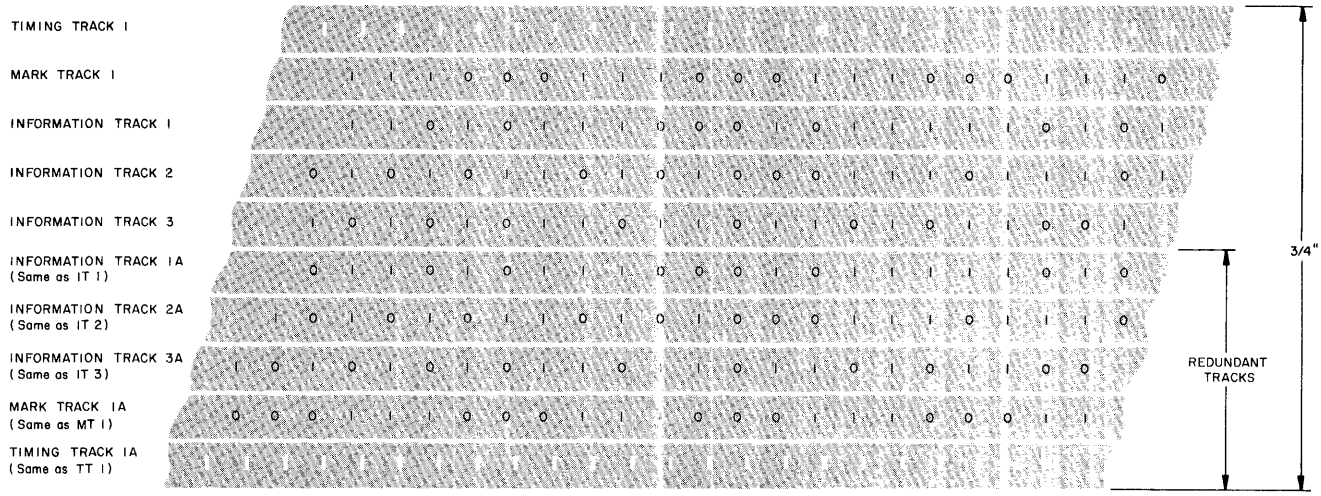


Figure 2-1 DECtape Track Allocation
Showing Redundantly Paired Tracks

Information is stored on the tape in block form (see Figure 2-2). Block length is flexible and determined by information on the mark channel. A complete reel of tape (849,036 lines) can be divided into any number of blocks up to 4096. Usually, a uniform block length is established over the entire length of a reel of tape by a program which writes mark and timing information at specific locations. However, the ability to write variable-length blocks is useful for certain data formats; for example, where small blocks containing index or tag information need to be alternated with the large blocks of data.

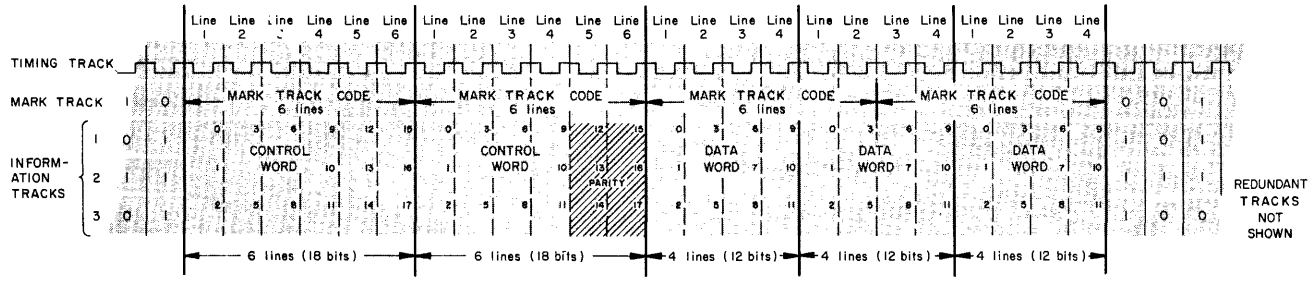


Figure 2-2 Basic Six Line DECtape Unit

Each block contains two types of words which are assembled by the Type 552 DECtape Control --data and control words (see Figure 2-3). Because DECtape has no inter-record gaps, control words separate the data portions of adjacent blocks. Although control words usually occupy six lines, only the last four lines are used for the PDP-5 and PDP-8. Control words record address and checking information. They provide compatibility between DECtape written on any DEC 12-, 18-, or 36-bit computer. Data words contain stored information and occupy four lines on tape (12 bits). To maintain compatibility with the mark-channel format, data words are recorded in 12-line segments (12 being the lowest common multiple of 6-line marks and 4-line data words) which correspond to three 12-bit data words.

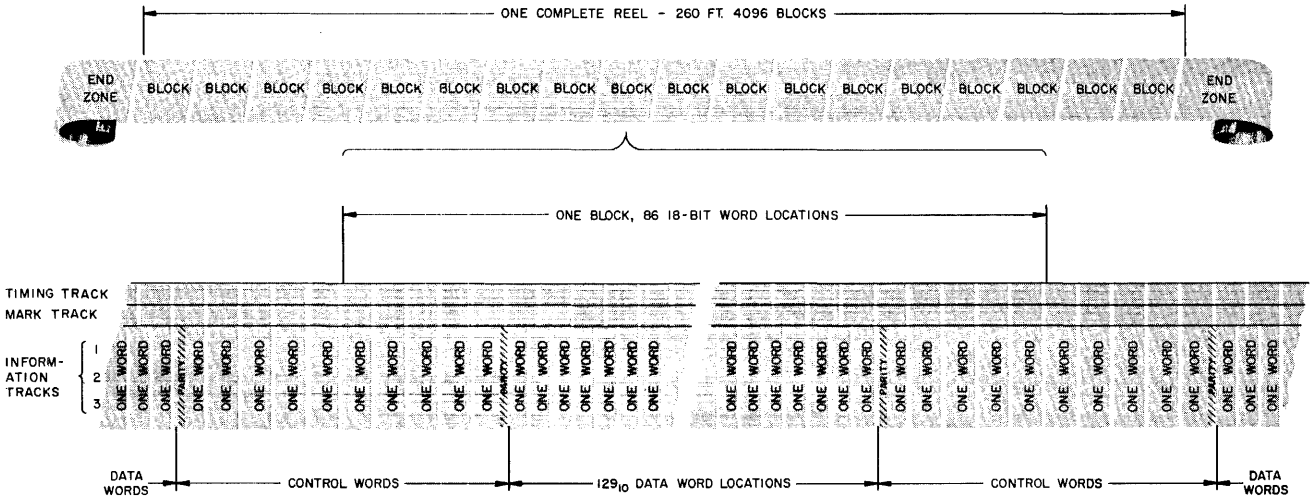


Figure 2-3 DECtape Control and Data Word Assignments

Block numbers normally occur in sequence from 1 to N. There is one block numbered 0 and one block N + 1. Programs are entered with a statement of the first block number to be used and the total number of blocks to be read or written. The maximum number of blocks is determined by the following equation in which N_B = decimal number of blocks, and N_W = decimal number of words per block. (N_W must be divisible by 3.)

$$N_B = \frac{212112}{N_W+15} - 2$$

2-1.1 Mark-Channel Format

The mark channel is the key to the overall computer system. Six-bit serially stored codes (called marks) on the mark track initiate controls which raise flags in the program, create sequence breaks, detect block mark numbering and block ends, and protect control portions of the tape (see Figure 2-4). The DECtape control unit automatically identifies these codes. The mark track also provides for automatic bidirectional compatibility, variable block formatting, and end-of-tape sensing.

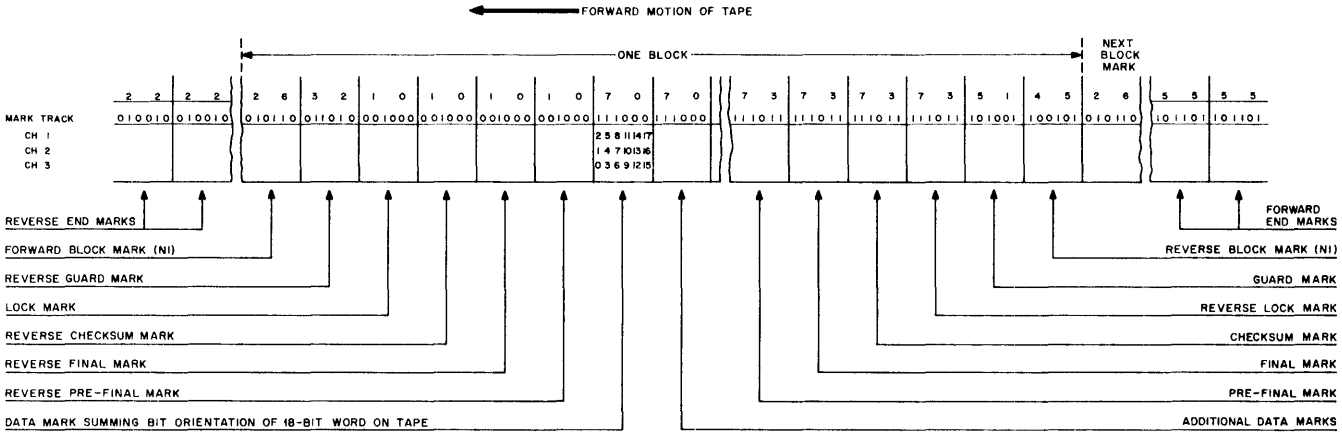


Figure 2-4 DECtape Mark Track Format
(Assumes 256_{10} Data Words Per Block)

Because the DECtape system allows searching as well as reading and writing in both directions of tape motion, the mark track is often read in reverse. In the reverse case, not only are the mark-track bits read serially in reverse order, but also (since the polarity of pulses is reversed when the tape moves

backward) the complement is read. The complement of a number with the bits reversed is defined as the complement obverse. The mark-track format has been carefully selected to be symmetrical so that the logic for reading in the reverse direction is exactly the same as that for forward reading. The complement obverse of the end-of-tape mark becomes the beginning-of-tape mark, and the end-of-data mark becomes the beginning-of-data mark.

The standard mark track uses the serial code of 6-bit characters to divide the tape into words. Codes are written on the mark track opposite word locations to identify the type of information stored at that location on tape. Block addresses are written for both forward and reverse directions and identified by two types of mark codes. A checksum is written at each end of the block. The first checksum written is -0 (-777777_8). This information is stored in a register in the computer. As each succeeding data word is read from the block, a total is kept that represents the sum of the words in the block. (Data words are added to -0.) Since the second checksum is the complement of the total, the addition of this number to the register should cause the appearance of -0. The control uses the final marks to establish synchronism and raise block-end flags. Data marks locate data words.

2-2 DECTAPE INSTRUCTIONS

The ten basic instructions used for the operation of the Type 552 DECtape Control system are summarized in Table 2-1. A more detailed description of these instructions, equally applicable to the PDP-5 and PDP-8, is in the PDP-8 Programming Manual (Digital-8-27-U).

Included in the basic instructions are those for eight modes of operation which are loaded into the function register (see Figure 2-5) during the MMLF command. These control modes are described briefly in the following subsection. Also included are the status-bit assignments which are loaded into status register during the MMRS command. Table 2-2 lists the meanings of these bit assignments.

TABLE 2-1 DECTAPE INSTRUCTION LIST

Mnemonic	Octal	Operation
MMLS	6751	Load select register from contents of AC bits 2-5 and clear DECtape (DT) flag. DT flag is automatically set approximately 70 msec after this IOT.
MMLM	6752	Load motion register from contents of AC bits 7-8 and clear DT flag. DT flag is automatically set approximately 70 msec after this IOT.
MMLF	6754	Load function register from contents of AC bits 9-11, then clear the AC. The octal code of these three bits 9-11 establishes the following DECtape control modes:

TABLE 2-1 DECTAPE INSTRUCTION LIST (continued)

Mnemonic	Octal	Operation
		0 = Move 1 = Search 2 = Read data 3 = Read all bits 4 = Write data 5 = Write all bits 6 = Write mark and timing 7 = Move and examine mark channel.
MMSF	6761	Skip if DT flag is a 1.
MMCC	6762	Clear memory address counter (MAC).
MMLC	6764	Load MAC from content of AC bits 0-11 and then clear the AC. (1's transfer).
MMML	6766	Clear and load MAC from content of AC bits 0-11 and then clear the AC.
MMSC	6771	Skip if error flag is a 1.
MMCF	6772	Clear error flag and DT flag.
MMRS	6774	Read status bits into the content of AC bits 0-7. The bit assignments are: AC0 = DT flag AC1 = Error flag AC2 = End (selected tape at end point) AC3 = Timing error AC4 = Reverse tape direction AC5 = Go AC6 = Parity or mark channel error AC7 = Select error

2-3 CONTROL MODES

The eight modes of operation which are loaded into the function register during the MMLF command (see Table 2-1) are described briefly in the following subparagraphs.

a. Move - Initiates motion of the selected transport tape in either direction. Mark-channel errors are inhibited in this mode.

b. Search - As the tape is moved in either direction, the sensing of a block mark causes both the data flag and the DECtape (DT) flag to rise. The data flag requests a computer data break for depositing the block number in the core memory at the

address held in the memory address register (MAC). The DT flag initiates a program interrupt which causes the program to jump to a particular subroutine; e.g., a subroutine which is responsible for checking the block numbers by using either the block number stored during this operation or by counting the number of times the DT flag rises.

c. Read Data - This mode reads a block of data in either direction, raises the data flag to cause a data break each time a 12-bit word is to be transferred, and raises the DT flag to initiate a program interrupt at the end of the data block. The program is responsible for controlling tape motion at the end of a block transfer and must stop motion or change the contents of the function register when the DT flag rises. The transport continues reading until taken out of the read-data mode.

d. Read All Bits - In this mode, the three information channels are continuously read and transferred to the computer. This mode is similar to the read-data mode except that the DT flag rises each time the data flag rises. The read-all-bits mode is used to read an unusual tape format which is not compatible with the read-data mode. The DT flag does not cause an interrupt when in this mode.

e. Write Data - This mode writes a block of data on tape in either direction, raises the data flag to effect each transfer, and raises the DT flag at the end of the block as in the read-data mode.

f. Write All Bits - This special mode of operation is used to write information at all positions without regard to blocks (such as in writing block numbers). Except that it applies to writing, this mode is similar to the read-all-bits mode. The DT flag does not cause an interrupt in this mode.

g. Write Mark and Timing - This mode is used to write on the timing and mark channels for establishing or changing block length.

h. Move and Examine Mark Channel - This mode is similar to the move mode mentioned above except that the control examines the mark channel and causes a program interrupt whenever an expected mark is absent.

2-4 FUNCTIONAL DESCRIPTION

The basic functional elements of the Type 552 DECtape Control (plus its PDP-5/8 computer and 555/TU55 transport interfaces) are shown in Figure 2-5. In this figure, numerals in the lower right corner of the blocks indicate bit-capability of the device, while numerical subscripts on the signal flow lines indicate the bit assignments in the signal; e.g., AC_{9-11} indicates that accumulator bits 9-11 are assigned for use in the signal. Brief descriptions of the functional elements in Figure 2-5 are given in the following subsections.

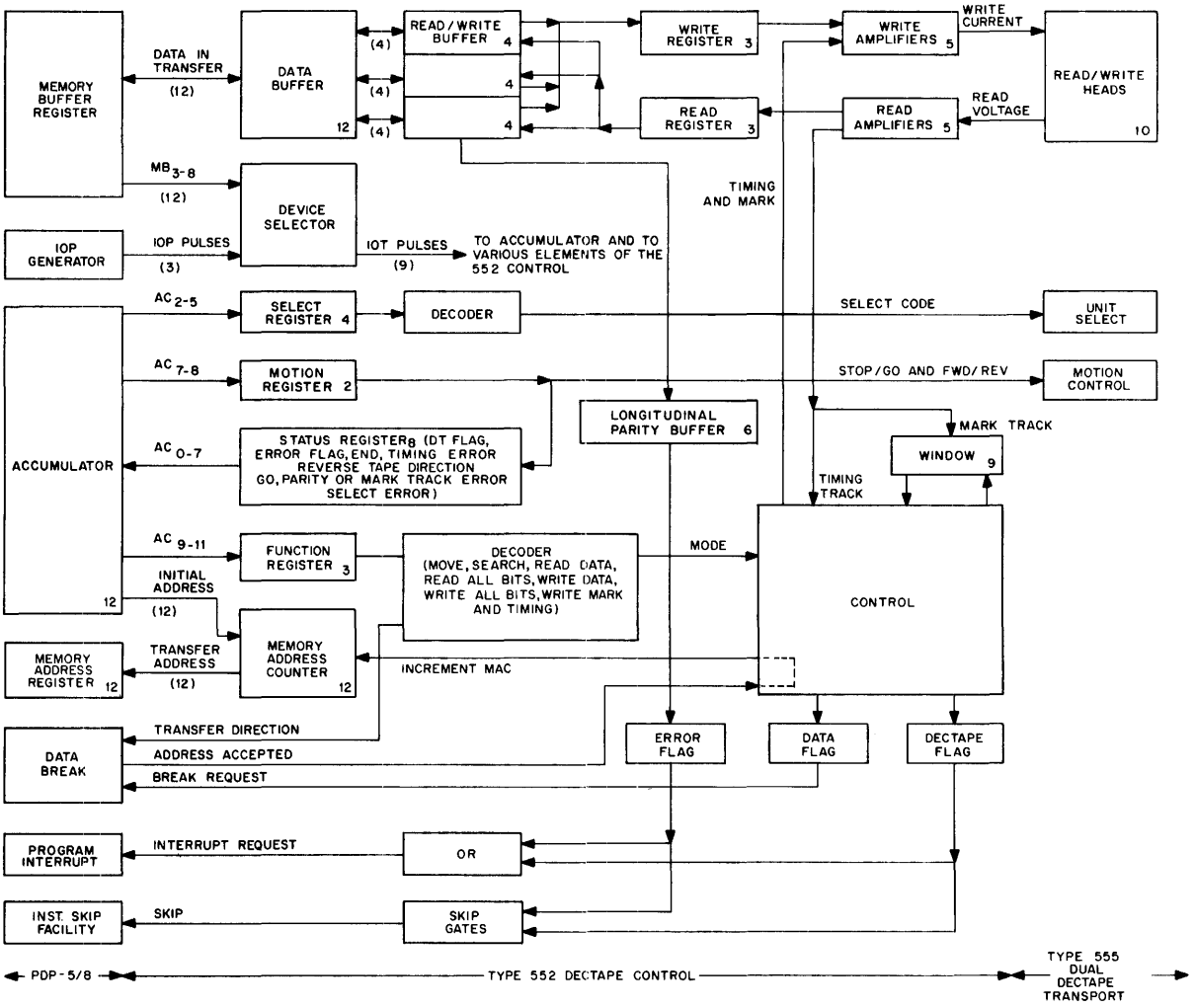


Figure 2-5 Block Diagram of Type 552 DECtape Control
Plus PDP-5/8 and Transport Interface Elements

2-4.1 Data Buffer (DB)

This 12-bit register serves as a storage buffer for data to be transferred between DECtape and the computer memory buffer register. During a read operation, information sensed from the tape is

transferred into the DB from the read/write buffer for subsequent transfer to the computer during a data-break cycle. During a write operation, the DB receives information from the computer and transfers it to the read/write buffer for disassembly and recording on tape. The DB, therefore, synchronizes data transfers by allowing transfers between the computer and the read/write buffer as a function of the tape timing.

2-4.2 Read/Write Buffer (R/WB)

This 12-bit register is composed of three 4-bit shift registers. During reading, one bit from each information channel is read into a separate segment of the R/WB and shifted right or left as a function of the direction of tape movement. When four tape positions have been read, the contents of the R/WB are set into the DB as an assembled 12-bit computer word. During writing, the contents of each segment of the R/WB are shifted serially to the write register (one bit from each of the three segments of the R/WB is transferred into the write register at a time to provide the data to be written at one line) for recording on tape.

2-4.3 Write Register

This 3-bit register is alternately loaded from the R/WB and complemented to write the phase-coded information on tape.

2-4.4 Read Register

During reading, this 3-bit register is loaded with one bit from each of the three information channels of the read head and transferred to the R/WB.

2-4.5 Device Selector (DS)

The device selector is a gating circuit which produces in/out transfer (IOT) pulses necessary to initiate operation of the DECtape system and to strobe information into the computer. This selector accepts all three in/out pulses (IOP) from the computer and decodes the contents of bits 3-8 of the IOT instruction in the computer memory buffer to determine whether the IOPs are addressed to DECtape control. When the control is addressed, the selector generates an IOT pulse for each IOP sent from the computer.

2-4.6 Select Register

This 4-bit register is loaded under the program control to specify the particular DECtape drives (eight tape drives available) selected for operation by the DECtape control. A 4-bit code in accumulator octal bits 2-5 is used for the selection and is decoded by the decoder at the right of the select register.

2-4.7 Decoder

Thirty-five msec after receipt of a select command from the select register, this decoder develops a signal for the unit relays of the selected DECtape transport. When enabled by a go command from the motion register, the decoder (to the right of the function register) asserts one of the seven function signals in the FR for use by control.

2-4.8 Motion Register

This 2-bit register contains a GO/STOP flip-flop and a FORWARD/REVERSE flip-flop which control the motion of the selected tape drive. The register is set under program control.

2-4.9 Status Register

This register contains eight gates which produce load pulses for bits 0-7 of the accumulator upon receipt of a read-status instruction addressed to control. The instruction generates an in/out transfer (IOT) pulse which drives all eight gates. Appropriate setting of the accumulator bits is effected according to the DECtape and error flags, the four error conditions, and two additional levels (GO and REVERSE), which assert tape-motion commands to the selected drive. The GO flip-flop is loaded from the motion register to initiate tape motion 35 msec after an instruction loads the motion register. Simultaneously the REVERSE flip-flop is loaded. Table 2-2 contains a summary of the meanings of accumulator bits 0-7.

TABLE 2-2 SIGNIFICANCE OF ACCUMULATOR BITS 0-7

AC Bit	Condition	Significance
AC0	DECtape flag	Control has completed a processing operation, or has recognized a new motion or select command and is requesting an interrupt.
AC1	Error flag	One of the four error conditions has occurred; thus a 1 is in accumulator bits 2, 3, 6, or 7 and control is requesting a program interrupt.
AC2	End	Tape at the selected drive is in the end zone.
AC3	Timing Error	Computer has failed to honor a program interrupt or data-break request, or new motion or select commands were issued before the last command could be executed.

TABLE 2-2 SIGNIFICANCE OF ACCUMULATOR (continued)
BITS 0-7

AC Bit	Condition	Significance
AC4	Reverse	Last tape motion command specifying GO also specified REVERSE.
AC5	Go	Control currently commands selected-tape drive to move tape.
AC6	Parity or Mark-Track Error	An error occurred in the timing or mark channels, or when reading in the data mode, a parity error was detected at the end of the last block.
AC7	Select Error	Control is unable to address one and only one tape drive, or has been commanded to write at a drive set to WRITE LOCK.

2-4.10 Function Register

This 3-bit register specifies the function to be performed by the control in any tape operation. Upon receipt of DECtape instructions, the function register is loaded from bits 9-11 of the accumulator. The octal code of these three bits establishes the eight DECtape control modes listed in Table 2-1. Any instruction that loads the function register also clears the accumulator.

2-4.11 Memory Address Counter (MAC)

This 12-bit register specifies an address in computer core memory to be used for each word transfer. During program initialization, the starting address of a transfer is set into MAC from the accumulator. During the transfer, the address in MAC is transferred into the computer memory address register for each data word. The contents of MAC are incremented by 1 at the conclusion of each word transfer, so that transfers occur between successive addresses of computer core memory and tape, regardless of tape direction.

2-4.12 Window (W)

This 9-bit register serves as a control signal generator for the DECtape system. The mark-channel data is stored in the W, and control signals are generated as a function of the mode of operation

in progress and the contents of the W. For example, in the search mode, when the W detects a block mark, control signals are generated to raise the DECtape (DT) flag to indicate the presence of a block number in the DB and signal the start of data block to the computer.

2-4.13 Longitudinal Parity Buffer (LPB)

This 6-bit register performs a parity check of the information in the three information channels. Essentially, the check reads the number of binary 0's in each half of a 12-bit data word and forms a parity bit to be recorded in the checksum control word at the end of the data block. This operation is performed by setting the information read from two consecutive tape positions into the LPB, and then complementing a bit of the LPB if the corresponding bit of the R/WB contains a 0. After reading a block of data, the LPB holds a number which indicates the parity of bits 0 and 6, 1 and 7, etc. A 1 in the LPB at this time indicates odd parity, and a 0 indicates even parity. This information is compared with the data stored in the checksum control word during reading and generates the checksum during writing. If the data read is not equal to the checksum, the parity or mark-channel-error flip-flop is set to 1.

2-4.14 Error Flag

Four error conditions raise this flag. When the flag rises, it initiates a program interrupt to allow the computer interrupt subroutine to determine the condition of Type 552 DECtape Control by means of a read status command. The four error conditions indicated are:

Condition	Meaning
End	The tape of the selected transport is in the end zone and tape motion is stopped automatically. Under these conditions, end is an error if it is not expected by the program in process, or it is a legitimate signal used to indicate the end of a normal operation (such as rewind) if it is anticipated by the program. If the transport is not selected when the tape enters the end zone, this end signal is not given, tape motion is not stopped automatically, and the tape can run off the end of the reel.
Timing Error	The program is not able to keep pace with the tape transfer rate, or a new motion or select command was issued before the previous command was completely executed.

Condition	Meaning
Parity or Mark-Track Error	Indicates that during the course of the previous block transfer a data parity error was detected, or one or more bits have been picked up or dropped out from either the timing track or the mark track.
Select Error	Signifies that a tape-transport unit select error has occurred (for example, more than one transport in the system has been assigned the same select code), or that no transport has been assigned the programmed select code.

In summary, a select error indicates an error by the operator; a timing error is a program error; and a parity or mark-track error indicates an equipment malfunction. Under certain conditions, the end may also be an indication of equipment malfunction.

2-4.15 DECtape Flag (DT)

This flip-flop serves as an indicator of DECtape system operation to the computer and is connected to the computer program interrupt facility. The control mode in operation at the time determines the function of the DT flag as follows:

a. In the search mode, the DT flag rises each time a block mark (block number) is read to indicate the beginning of a new block and to allow programmed determination of the block number which just passed the read/write head.

b. In read-data or write mode, the DT flag rises at the end of each block to indicate the end of a data block. Under these conditions, the computer program can sense for this flag to determine when the transfer is complete.

c. In read-all-bits or write-all-bits mode, the DT flag rises to indicate completion of each 12-bit word transfer. Since block marks are not observed in these modes, the computer program can use this flag to count the number of words transferred as a means of determining tape location.

2-4.16 Data Flag

This flag is raised each time the DECtape system is ready to transfer a 12-bit word with the computer. When raised, the flag produces a computer data break.

2-5 PROGRAMMED OPERATION

The prerecording of a reel of DECtape (prior to its use for data storage) is accomplished in two passes. During the first pass, the timing and mark channels are placed on the tape. During the second pass, the forward and reverse block-mark numbers, the standard data pattern, and the automatic parity checks are written. The DECTOG program (see PDP-8 Programming Manual) performs these functions. Prerecording utilizes the write-timing-and-mark-channel control mode plus a manual switch in the DECtape control to write on the timing and mark channels, to activate a clock which produces the timing-channel recording pattern, and to enable flags for program control. Unless this control mode and switch are used simultaneously, the writing on the mark or timing channels is physically impossible. A red indicator lights on all transports associated with the control when the manual switch is in the ON position. Only under these conditions does the write register and the write amplifier (which writes on information channel 1, bits 0, 3, 6, and 9) write on the mark channel.

Two PDP-8 in/out transfer (IOT) DECtape instructions initiate operation of the DECtape. The first instruction (MMMM) loads the select register, motion register, and function register by means of instruction 6757 (combining MMLS, MMLM, and MMLF). A second instruction MMML 6766 (combining MMCC and MMLC), loads the memory address counter (MAC) with the core memory address for use in storing the block number during searching. After initiating DECtape operation, the program always checks immediately for errors using the MMSC instruction. This instruction is also used at the end of each transfer. A program always starts the DECtape system in the search mode to locate the block number selected for transfer. When the block number has been located, the transfer is accomplished by loading the function register with the read-data or write-data mode.

In searching, the transport reads each block number and transfers it to the control. The control raises the DT flag upon receipt of each block number and stores the number in the computer core memory at the address in MAC. The computer program then samples the DT flag and either counts the number of blocks passed or reads the block number from core memory and compares it with the number it is seeking. The results of data obtained in this way are used to further control the search operation. Upon determining that the forthcoming block is the one selected for a data transfer, the program loads the function register with either the read-data or write-data mode. Entering another mode discontinues the search mode. The computer then sets into the MAC the starting address to be used for the first core memory address of the transfer.

When the start of the data position of the block is detected, the data flag is raised to initiate a data break each time the DECtape system is ready to transfer a 12-bit word. Therefore, the main computer program continues running but is interrupted approximately every 133-1/3 μsec during a data break for the transfer of a word. Transfers occur between DECtape and successive core memory locations, commencing at the address previously set into MAC. The size of the selected tape block determines the

number of words transferred. At the conclusion of the block transfer, the DT flag is raised, and a program interrupt occurs. The interrupt subroutine checks the DECtape error flag to determine the validity of the transfer and either initiates a search for the next information to be transferred or returns to the main program.

During all normal writing transfers, a checksum (the 6-bit exclusive OR of the words in the data block) is computed automatically by the control and is automatically recorded as one of the control words immediately following the data portion of the block. This same checksum is used during reading to determine that the data playback and recognition take place without error.

The program can select any one of the eight tape drives. After using a particular drive, the program can stop the drive currently being used and select a new drive, or can select another drive while permitting the original selection to continue running. Because several transports may be used simultaneously, this is a particularly useful feature when rapid searching is desired. Caution must be exercised, however, because, although the earlier drive continues to run, no tape-end detection or other sensing takes place. Automatic end sensing that stops tape motion occurs in all modes, but only in the selected tape drive.

Whenever either the motion or select code is changed, the program must wait until the DT flag is set to 1 before giving another motion or selection command. In other words, to prevent a timing error, all operations of the currently selected drive must be completed before issuing a new select code.

2-6 AVAILABLE SOFTWARE

PDP-5/8 software (see PDP-8 Programming Manual Digital-8-27-U) includes the following:

a. Subroutines which the programmer may easily incorporate into a program for data storage, logging, data acquisition, data buffering (queueing), etc.

b. A library calling system for storing named programs on DECtape and calling them with a minimal size loader.

c. Programs for preformatting tapes controlled by the content of the switch register to write the timing and mark channels, to write block formats, to exercise the tape and check for errors, and to provide ease of maintenance.

The series of subroutines will read or write any number of DECtape blocks; read any number of 129-word blocks as 128 words (or one memory page) in which 200 octal locations equal 126 decimal locations; or search for any block (used by read and write, or to position the tape). These programs are assembled with the user's program and are called by a jump-to-subroutine (JMS) instruction. The program interrupt detects the setting of the DECtape (DT) flag, allowing the main program to proceed while the

DECtape operation is being completed. A program flag is set when the operation has been completed. The program may thus effectively allow concurrent operation of several input/output devices with the DECtape. These programs occupy two memory pages ($400_8 = 256_{10}$ words).

Several design features are included in the library system. First and perhaps foremost, the system leaves the state of the computer unchanged when it exits. Second, it is capable of calling programs by name from the keyboard and allowing for expansion of the program file stored on the tape. Finally, it conforms to existing system conventions; namely, that all of memory, except the last memory page (7600_8-7777_8), is available to the programmer. This convention permits the binary loader (paper tape), and/or future versions of this loader, to reside in memory at all times. The skeleton library tape for the library system contains the following programs:

INDEX	Typing this program causes the names of all programs currently on file to be typed out.
UPDATE	Allows the user to add a new program to the files. UPDATE queries the operator about the program's name, its starting address, and its location in core memory.
GETSYS	Generates a skeleton library tape on a specified DECtape unit.
DELETE	Causes a named file to be deleted from the tape.

Starting with the skeleton library tape, the user can build up a complete file of his active programs and continuously update it.

The last group of programs, a collection of short routines controlled by the contents of the switch register, is called DECTOG. It provides for the recording of timing and mark channels and permits block formats to be recorded for any block length. Patterns may be written in these blocks, then read and checked. Specified areas of tape may be "rocked" for specified periods of time. A given reel of tape may thus be thoroughly checked before it is used for data storage. These programs may also be used for maintenance and check-out purposes.

CHAPTER 3
CONTROL LOGIC

3-1 INTRODUCTION

Control logic for the Type 552 DECtape Control is explained by reference to pertinent timing diagrams and to DEC engineering drawings BS-D-552-0-3 through BS-D-552-0-8. In this chapter, the engineering drawings will be referenced only by the last number and where applicable a colon and the zone. Circuit locations on the drawings will be referenced by a numeral-letter-numeral symbol; the first numeral designates the last digit of the drawing number, while the following letter-numeral combination designates the location of the circuit on the drawing (see Chapter 6).

Reduced engineering drawings, with applicable symbol conventions, are in Chapter 6. These symbol conventions should be thoroughly understood before proceeding because they are used in the text and timing diagrams as well as in the engineering drawings.

In the text and timing diagrams, the circuit location symbols defined above cross-reference each event of the program with its associated hardware on the engineering drawings. This cross-referencing forms the basis of the discussion in this chapter.

3-2 COMPUTER INTERFACE

The interface between the computer and its DECtape control includes the following:

a. Decoding pulse amplifiers which generate in/out transfer (IOT) pulses from computer instructions.

b. Five registers used for computer-DECtape control communications. These registers are the unit, motion, and function registers shown on BS-8; the data buffer (DB) at bottom of BS-6; and the memory address counter (MAC) at the bottom of BS-5.

c. Status bits for the tape end, timing error, parity or mark error, and select error flip-flops at top of BS-4. The 1 outputs of the REV and GO flip-flops (8:B4,5) are also available as status levels, but the computer cannot set or clear these two flip-flops directly.

d. Data flag and data transfer (DT) flag (4:A2,3).

3-2.1 In/Out Control

The control operations initiated by specific computer instructions are illustrated by the flow diagram of Figure 3-1. In this flow diagram, the shapes of the enclosures indicate the following:

Shape	Enclosure for
Ellipse	True pulses (e.g., pulse amplifier outputs).
Rectangle	Gating levels or changes in the state of the flip-flop.
Pair of horizontal lines	Delays specified between lines by duration (e.g., 500 nsec) and condition (e.g., wait for positive overshoot).

As in timing diagrams, events on the flow chart are keyed to their associated hardware by the circuit location symbols.

The 4605 Gated PA (2L01) for the 675 instructions (MMLS, MMLM, and MMLF) is shown on drawing 8:C1. All three instructions pertain to the jam-transfer of disjunct groups of accumulator (AC) bits into the unit, motion, and function registers. Loading the function register (like loading the MAC) clears the AC through a gate (8:C6) and loads the function register through a pulse inverter (PI) (8:B6). The capacitor-diode (C-D) gates below motion register $MOTION_1$ (8:B6) are permanently disabled by the 10K resistor to −15v; consequently, the PI only affects the three function-register bits. As long as $MOTION_1$ is set, the 4151 Binary-to-Octal Decoder (8:A7,8) is fed by the function register and generates the seven tape function levels. The read-all, write-all, and write-timing and-mark (WRTM) functions are ORed together to develop the ALL BITS level (4:C2).

The AC —J→ MOTION pulse generated by the MMLM (6752) instruction transfers AC bits 7 and 8 into $MOTION_1$ through the C-D gates (8:B5,6) and simultaneously triggers 35-msec delay (8:D3). When this delay times out, it triggers the SELECT delay (8:C3) and the turn-around-and-start-acceleration (TA&SA) delay (8:C3); and simultaneously transfers the contents of $MOTION_1$ into the REV and GO flip-flops (8:B4,5) through their C-D gates. The transfer into GO is unconditioned, but REV is loaded only if GO becomes 1; hence the direction of a prior tape movement is always available to a transport that is commanded to stop. These REV and GO flip-flops directly control the tape motion at the selected transport through the indicator drivers (ID) (8:B4,5); consequently, tape motion is governed by the contents of AC bits 7 and 8, 35 msec after the MMLM instruction.

The MMLS (6751) instruction generates an AC —J→ UNIT pulse (8:C2). The leading edge of this pulse triggers the lower 35-msec delay (8:D2); and 400 nsec later, the trailing edge triggers a PA (8:C1). This PA develops a 1-msec pulse whose trailing edge transfers the contents of AC bits 2-5 into

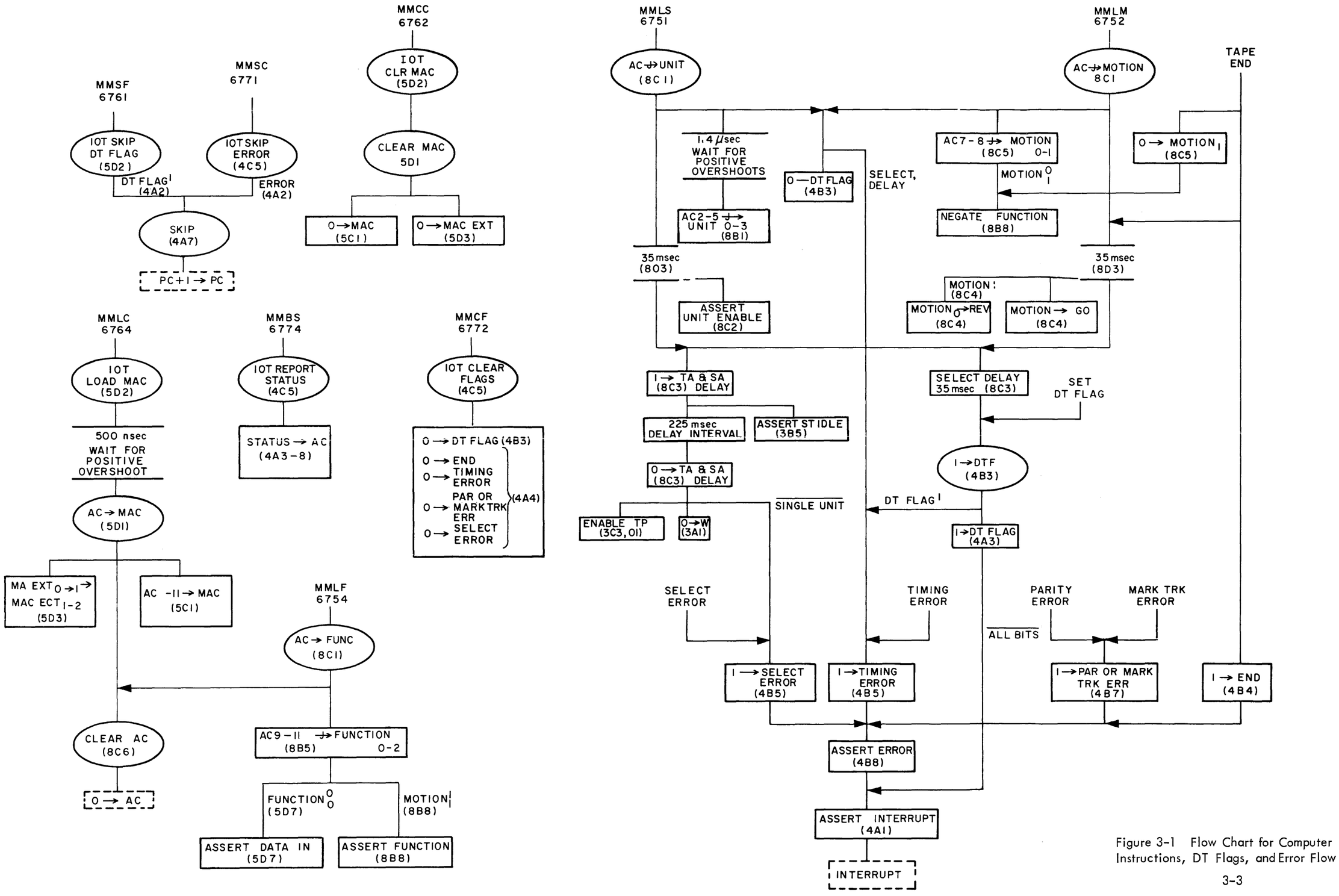


Figure 3-1 Flow Chart for Computer Instructions, DT Flags, and Error Flow

the unit register. Because of the cascaded trailing-edge triggers, the transfer occurs 1.4 μsec after the computer's IOP 1 pulse. Such a delay is required because PDP-8 accumulator bits may be indeterminate up to 0.5 μsec before IOT 1, and this is insufficient time to enable the C-D gates at the unit register flip-flop. In the NAND gates of the 4112 module (8:C4) the 35-msec delay negates both outputs of $UNIT_3$, disabling the 4671 Binary-to-Decimal Decoder (8:B1,2,3). The MMLS (6751) instruction, therefore, deselects the previous transport 35 msec before selecting another. This delay interval allows for all deselected transport relays to drop before picking up relays of the newly selected transport. While the delay enables the new selection, it also triggers SELECT and TA & SA delays (8:C3). The ground return for the 4671 Decoder is connected through a 5-ohm resistor (8:A1). If unit register (8:B1,2,3) is loaded with a code that addresses more than one drive, the decoder draws double (or more) the normal current; hence, the drop across the return resistor is doubled. If the unit register cannot address any drive, no decoder current is drawn and the drop across the return resistor is zero. The two adjacent 1501 Difference Amplifiers (8:A1) sample the drop across the return resistor and assert $\overline{\text{SINGLE UNIT}}$ in response to either select error.

When the SELECT delay (8:C3) times out, it sets the DT flag (4:A3). Unless the function register specifies one of the all-bits functions, the DT flag asserts the interrupt level (4:A1) causing a program interrupt. The TA & SA delay (8:C3) clears the state generator prior to beginning new tape operations. When the delay terminates, its 0 output clears the window register and enables the production of timing pulses. If a null or multiple selection has been made, the TA & SA delay signals the program when it times out by setting the select-error flip-flop through the C-D gate (4:B8). A selection or motion instruction repeated while the select delay is set (i.e., between 35 and 70 msec) causes a timing error through C-D gates (4:B6). All error flip-flops assert the ERROR level (4:B8) which requests a program interrupt (4:A1). A timing error also results if the control sets either flag while it is already 1, indicating that the computer has failed to service a data-break request or a program interrupt.

The 4605 Gated Pulse Amplifier (4:C5) is used for the MMSC (6671), MMCF (6772), and MMRS (6774), instructions. An MMSC (6771) generates a pulse that samples the ERROR at gate (4:A2), and a pulse out at the SKIP line adds 1 to the computer program counter (in addition to the increment that is normally part of each cycle). A clear-flags pulse generated on the MMCF (6772) instruction clears all four error flip-flops through the PI(4:A4), and the DT flag through gate (4:D3). The report-status pulse generated by MMRS (6774) drives the row of gates (4:A-3), setting AC bits that correspond to asserted status levels.

The last three instructions are decoded by the 4605 Gated-Pulse Amplifier (5:D2). The SKIP DT-flag pulse from instruction MMSF (6761) pulses SKIP line (4:A2) when the DT flag is 1. The other two pulses clear and load the MAC and MAC EXT (5:D3). The load pulse generated by MMLC (6764) functions as a trailing-edge trigger for the PA(5:D1); the PA output loads MAC (5:C1), clears AC (8:C6) and loads

MAC EXT (5:D3) from the data-field register in the computer memory-extension control. DECtape controls (designed for use with computers having more than four 4K memory modules) have an additional MAC EXT flip-flop. The 1 outputs of MAC and its extension are made available to the computer through buffers at ground assertion, and specify the address for a data transfer during data-break cycles initiated by this control.

3-2.2 Data Transfers

Full-word 12-bit transfers are made between the memory buffer (MB) and data buffer (DB) shown at the bottom of drawing 6. DB is not available to the program; transfers take place only to or from the memory location specified by MAC in a computer data-break cycle requested by DECtape data flag (DT). The direction of information flow is determined by $FUNCTION_0$ (5:D7), and is 1 for all write operations. A negative 0 output asserts the DATA IN signal (5:D7) to the computer for move and read operations; data breaks then transfer the information into memory. The data flag asserts the BREAK REQ signal through an inverter (4:A1). MAC has its own increment logic, so that the address-increment request level (4:A1) to the computer is permanently disabled at ground. When the address in MAC and its extension have been transferred to computer memory address and extension registers, the computer returns the ADDRESS ACCEPTED pulse which clears the data flag. Except in the search mode, this pulse also increments MAC through a gate (5:C8) to obtain the address for the next transfer.

DB (6:C1) receives MB 1 outputs (5:D8) asserted at ground; internal inverters generate the corresponding 0 levels to allow a jam-transfer of information. For writing, the MB —J▶ DB pulse is generated by the logic at the lower right of BS-5. During the break cycle, the level (B(1) is asserted from the computer and C-D gate (5:D6) is enabled. Timing pulse T5 (5:D6) from PDP-5 or T2B from PDP-8 generates the MB strobe pulse for the DB through the C-D gate and PA(5:D8). In reading, read/write buffer (RWB) on drawing 6 accepts read amplifier levels at one end of each 4-bit shift segment. Four successive shifts assemble in RWB a full word, which is then transferred to DB as data flag (7:C2) is set. While RWB assembles the next word from tape, the contents of DB are available to memory through the buffers shown above the register.

3-3 READ/WRITE LOGIC

The basic circuit for read/write logic, and pertinent waveforms are shown in Figure 3-2. In this figure, the flip-flop below the write amplifier may be a bit of the write buffer (WB) in drawing 6 or it may be the timing-track buffer (TMB) (3:C1) or the mark-track buffer (MKB) (3:B4). For all channels, the hardware is identical with each read/write module, containing a flip-flop and input gates, a write amplifier

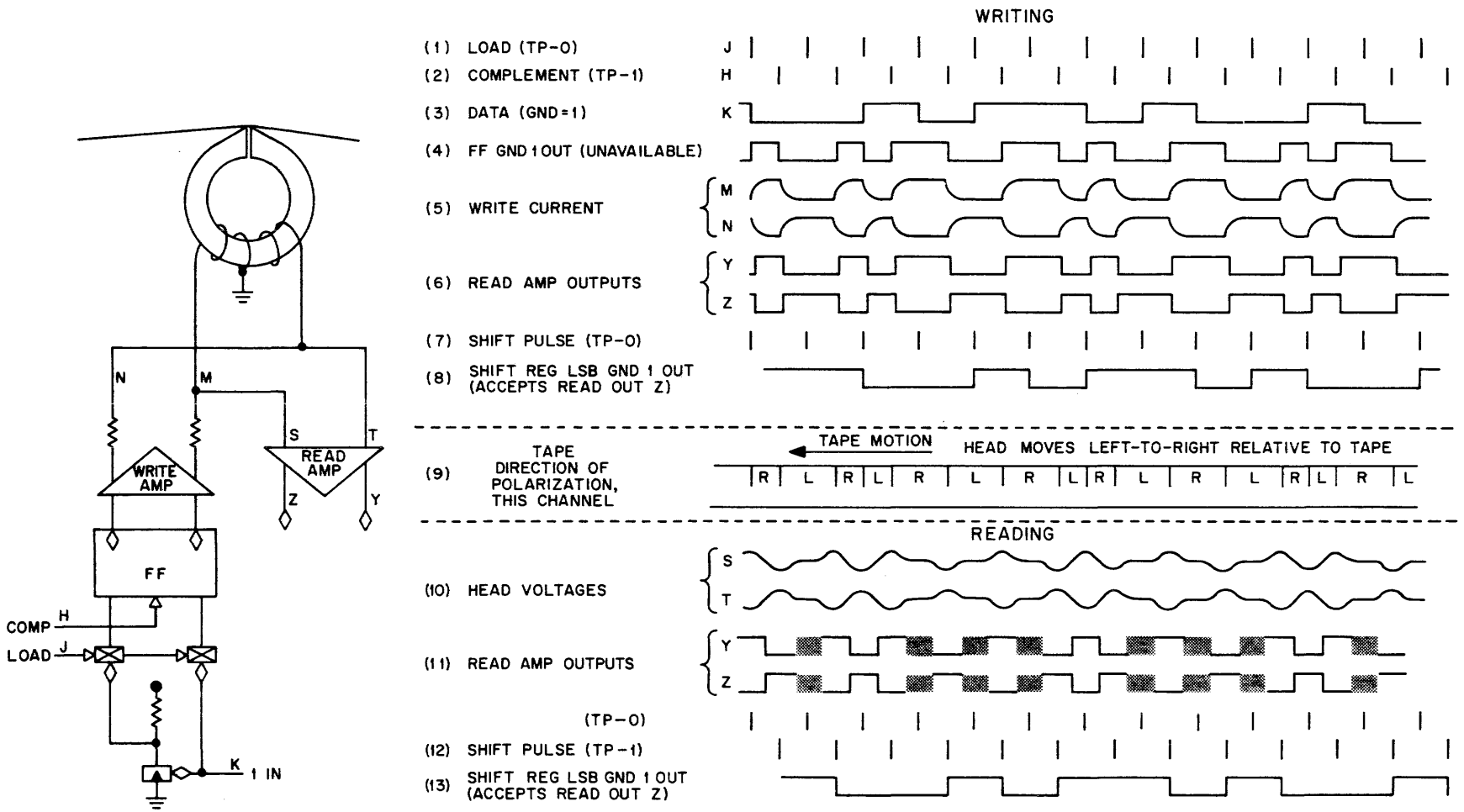


Figure 3-2 Read/Write Waveforms

governed by the flip-flop outputs, and a read amplifier. Read inputs are paralleled with the write-amplifier outputs across the head. Hence, the read amplifier responds to signals from both the head and the write amplifier.

The read amplifier is a three-stage differential amplifier having extremely high (uncontrolled) gain, augmented by a transient positive feedback that is effective over a delay of approximately 10 μsec. The feedback amplitude with reference to the input is nearly 1 mv, as compared to head signals of 5 mv peak-to-peak. The read amplifier, therefore, is a decision-making device in which (when a signal of either polarity is sensed by the head) the amplifier outputs switch immediately and are asserted unambiguously regardless of noise. This design prevents head cross talk resulting from simultaneous writing in the data channels and the timing and mark channels. The read amplifier outputs Z and Y are standard DEC logic levels of −3v and ground. When input S is more positive than T, the output Y is asserted at ground and Z is negative; when T is more positive, the output levels are reversed. Due to the positive feedback, the read amplifier oscillates in the absence of input signals. Hence, the read-amplifier output waveforms are rectangular whenever the differential input signal is indeterminate.

The write amplifier is a saturated grounded-emitter push-pull amplifier with its output collectors connected through resistances to pins M and N. If the enable level is asserted negative, the write amplifier is governed entirely by the state of the flip-flop. When the flip-flop is 1, M floats while N is returned through the resistance and saturated output collector to −13v. When the flip-flop is 0, N floats while M is negative. In the two tracks corresponding to each channel on tape, information is recorded in a manner that makes read signals from the two head inductors reinforce on playback. The two inductors can be considered as a single head inductor whose winding is center-tapped to ground, reading and writing in a single track (see Figure 3-2).

When the write flip-flop contains 0, current flows from ground through the head inductor into M, and the polarization of the head core is oriented clockwise. Then the tape polarization as the tape moves across the head is oriented toward the left regardless of the direction of tape motion. Similarly when the flip-flop contains 1, tape polarization is oriented to the right regardless of the direction of tape motion. When reading, the current induced in the head by a change in polarization flows opposite to the current which would be required to cause the same change; consequently, the current induced by a left-to-right (L-R) tape polarization change is a current flowing out of the head toward pin S. Now the head is a source, and when a terminal is a current source it is positive. Thus an L-R tape polarization change causes the read-amplifier input S to be positive; consequently, Y is ground and Z is negative. By the same reasoning, the right-to-left (R-L) polarization change induces a positive signal at T and results in Y being asserted negative and Z at ground.

In the Manchester recording system, two pulses are required to write each bit in a channel. The first pulse loads the write flip-flop with the value of the bit to be written; the second pulse complements

the flip-flop. Depending on the state of the flip-flop, the pulse that loads the flip-flop may or may not cause a polarization change on the tape. The complement pulse, however, causes a tape polarization change because the complement always changes the state of the flip-flop. When reading, therefore, the value of a recorded bit is detected by observation of the head inductor output as the polarization change (corresponding to the complement) passes over the head. The complement pulse produces a R-L tape polarization change when the flip-flop is loaded with 1, and produces a L-R change when the flip-flop is loaded with 0.

In the circuits of Figure 3-2, the LOAD and COMP pulses alternate. The first pulse always makes the flip-flop correspond to the assertion of the 1 IN level, the second pulse always makes the flip-flop assume the opposite state. The complement pulse always follows a load pulse by 16.6 μsec and the next load pulse follows the complement after the same interval. This relationship is shown in lines 1 and 2 of Figure 3-2. Since the flip-flop is loaded through capacitor-diode (C-D) gates, the data input is free to change at each load pulse; line 3 shows a string of consecutive bits to be written on tape. The write flip-flop in line 4 receives each bit at a load pulse, then assumes the opposite state on a complemer pulse. The output shown in line 4 is not obtainable in the hardware unless the module is plugged into a module extender; however, outputs at M and N in line 5 can be observed with a current probe. During writing, the read-amplifier output waveforms at Y and Z of line 6 follow the write-current waveforms at M and N, respectively.

Information to be written in a data channel comes from RWB_0 (6:C1). Each pulse that loads WB causes RWB to shift simultaneously one place to the left; successive shift pulses therefore cause the information in RWB bits 3, 6, and 9 to be applied to the WB input gate. The RWB shift pulses also shift the read-amplifier information into the RWB_9 which accepts output Z of the read amplifier and receives the written information displaced one bit. Line 9 in Figure 3-2 shows the direction of tape polarization, labeled R and L for right and left, respectively. The R-L and L-R transitions are detected by the read amplifier as negative and positive half sinusoids at pin S (opposite polarity at T). If the tape is read in the same direction as written, the tape positions, corresponding to the time the write flip-flop was complemented, will show an R-L change as a 1, an L-R change as a 0. The head voltages at read-amplifier inputs S and T are shown in line 10; the read-amplifier outputs, at line 11. In reading, the shift pulses in line 12 for RWB coincide with those in line 2 which complemented the write flip-flop in writing. The R-L polarization change, representing a 1, results in a ground level at Z at the time of the shift pulse; consequently, as shown in line 13, a 1 is shifted into the shift register as the first bit read.

If the tape is read opposite to the direction in which it was written, the polarizations reach the head gap in reverse order; that is, the head senses an L-R change where a 1 was written, etc. The contents of the mark channel are selected to take advantage of this condition. For data, however, the RWB

must accept the read-amplifier outputs Z when reading in the same direction as the information was written, and the outputs Y when reading in the opposite direction. For simplification, the polarization change denoting a 1 is standardized as an R-L change when reading forward. RWB_{9-11} accept the read-amplifier Z outputs (READ -n levels (6:A2,6)) as RWB shifts left when reading forward; RWB_{0-2} accept the Y outputs (RAMP-n levels) as RWB shifts right when reading reverse. The appropriate READ and RAMP channel is denoted by n.

The logic is standard while writing forward; loading a WB bit with 1 and complementing it correctly produces an R-L change on tape at the complement pulse; complementing a 0 produces an L-R change. However, to make a 1 written in reverse appear to be written forward, the head must first write left polarization, then right. When reading this forward, the head senses an R-L change which is a 1. When writing in reverse, reversal is obtained by loading WB with 0 to write 1, and loading 1 to write 0.

3-4 TIMING AND MARK CHANNELS

In writing, two logical functions are required for access to the timing and mark channels. The computer supplies one function when it loads the function register with the code for WRTM. The other is the RELTM level asserted through relay contacts V-J (4:D6) which are closed when the WRTMR toggle switch is on (up). In addition to energizing the relay, the switch provides a ground return at pin L of connectors 2L28-29 (4:D8) lighting red indicators on all transports connected to the control. The relay contacts for developing RELTM are shown on drawing 4:D7; other contacts are shown on drawing in which they are more significant.

All operations in the write timing and mark mode are timed by an 8.33 μsec clock (3:C1) which is enabled by the RELTM relay. Each clock governs the clock counter CK (3:C2), and, at the same time, transfers the contents of CK_1 into the timing-channel write buffer TMB (3:C1). The complement pulse for CK_1 passes through a unidirectional enabling gate so that when the level at pin M is ground, CK_1 may be complemented in either direction; when M is negative, the flip-flop may be complemented only to the 0 state. The complement pulse is enabled by a gate (3:D1) only when writing is enabled by the WRTMR switch, or when the tape is in motion and up to speed in the WRTM mode. The clock that changes the state of CK_1 redundantly strobes its previous contents into TMB; the first subsequent clock changes TMB according to the new state of CK_1. TMB, therefore, changes state every 16.6 μsec which is 90° out of phase with CK_1, and hence equally out of phase with the timing pulses.

Each time CK_1 becomes 1, it produces timing pulse TP-0 through the PA(3:C5); 16.6 μsec later (when CK_1 becomes 0), TP-1 is produced through a PA(3:C4). Since TP-0 is produced when TMB is 0, TP-0 marks the center of an interval during which left polarization occurs in the timing channel. Similarly, TP-1 marks the center of right polarization on the timing channel.

Whenever writing is enabled in the WRTM mode, TP-0 loads mark-write buffer MKB (3:B4) as well as WB_0 (6:A1), and TP-1 complements it through the gates (3:D4). Information for MKB comes from the most significant bit of read/write buffer RWB_0 (6:C1). TP-0 shifts RWB to present new information at the same time that MKB accepts the previous bit. Since the timing pulses govern MKB, this buffer is loaded with new information at the center of left polarization in the timing channel; complemented in the center of right polarization in the timing channel. Hardware timing relationships in the WRTM mode are shown at the top of Figure 3-3. Line 7 of this figure shows the tape polarizations in the timing and mark channels as a result of the above writing operations.

The read-amplifier waveforms are shown at the bottom of Figure 3-3. These waveforms illustrate the behavior of signals for both forward and reverse tape motion. For forward motion, the chart is read from left to right along lines labeled at the left; for reverse, from right to left along lines labeled at the right. Line 8 is the timing channel read voltage at the read-amplifier input pins (3:B1). For an L-R transition, pin S is positive as in line 8. The same position on tape is read as an R-L transition in reverse; consequently input T is positive at this point when reading backwards. Line 9 shows the timing-channel read-amplifier output; the waveform represents the output at Z when reading forward; at Y, in reverse. These outputs drive the C-D gates below the PA(3:C4,5) producing TP-0 and TP-1. When the gates are enabled, the fall in TT0 in line 9 produces a TP-0 through the lower PA(3:C5), while the upper PA(3:C4) generates TP-1 from a fall in TT1.

The timing pulses themselves disable the two gates directly through Type 6102 Inverters (3:C5), and trigger the 10-μsec cross-talk delay (3:D3). The TP ENABLE level therefore drops at the leading edge of either timing pulse, and remains negated for 10 μsec while the cross-talk delay times out. These circuits prevent generation of a second spurious timing pulse from timing-channel noise due to simultaneous writing in the data channels. The TT levels must be prevented from affecting generation of timing pulses when writing in the timing channel; so RELTM grounds TP ENABLE (3:C4). In all other functions, the enable is asserted as soon as the tape is up to speed (i.e., when TA & SA (8:C3) clears with GO^1). In writing, the write-enable flip-flop enables timing pulses, until cleared to allow a complete word to be written on tape. The occurrence of the timing pulses in line 10 of Figure 3-3 takes place at identical tape positions regardless of the direction of motion. A TP-0 always occurs in the middle of a left polarization on tape, a TP-1 in the middle of a right polarization, thus duplicating the relationship created by the hardware when writing on the timing and mark channels.

The mark-channel read-amplifier output MT (3:A4) is the first of the three traces in line 12 of Figure 3-3. This output level is sampled at every TP-1 to load W9, the least significant bit of the window register (3:A4). The contents of W9 are shifted to the left as new information enters W9; consequently, the center trace of line 12 (which shows the state of W9 with respect to time) also indicates the contents

of the last eight bits of the W register in order from left to right. For example, during the interval from the TP-1 before and after the center vertical chart division, W contains 01 010 110, i.e., octal 126, corresponding to the block mark. The W BLK MK level (top trace at line 13) is asserted during the interval.

Reading from right to left on the chart, the center and lower traces of line 13 indicate the mark-channel read-amplifier output and the behavior of W9 when reading backward. Since the order of polarization change is reversed when the tape moves backward, the MT waveform is of opposite polarity from that existing when reading forward. Consequently, the complement obverse of the mark-read-forward is shifted into W9. From the TP-1 before and after the center vertical chart division (reading right to left), W contains 11 101 001, i.e., octal 351, corresponding to the guard mark. The digital group is decoded as W GUARD (3:A2) and is shown as the top trace of line 13. Notice that the assertion of a decoded window output is not displaced when changing tape direction. Note also that the mark intervals on the tape are bounded by every sixth TP-0 and that decoded window outputs always assert the marks from the TP-1 before and after the mark boundary.

3-5 ALL-BITS MODE

The control operates in the all-bits mode whenever the function register specifies read-all, write-all, or write timing and mark. When writing on the timing and mark channels, the RELTM level disables the window register by inhibiting the TP-1's; thus the window remains clear. In the read-all or write-all functions, the window does assemble mark-channel information but data is written or read continuously, regardless of the window contents. When reading, no checks for parity occur. When writing, the block numbers are erased and replaced by data. Data transfers occur at 12-bit (4-line) intervals (whether writing or reading) as long as the tape is in motion.

3-5.1 Control Pulses and Data Transfers

Timing pulse TP-1 drives a 4.5-μsec delay (3:C6) which, in turn, produces TP-2 through a PA (3:C7). This delayed pulse initiates and terminates the various control functions that depend on decoded marks from the window register and times the transfer of information to or from the computer. TP-2 increments the data-timing-gate counter (DTG) (3:D7) in standard binary fashion. To guarantee synchronization, the DTG is cleared by ST BLK MK, a level asserted at TP-2 time, just before the end of the forward block mark on the tape. When DTG_0 becomes 1, PA(3:C7) produces the DTP-2 pulse which coincides with every fourth TP-2. The next TP-0, gated by the condition that DTG contains 2, generates DTP-0 through PA(3:C6). If the tape is allowed to continue through interblock zones after DTG is synchronized, the subsequent block-mark clears are redundant. This condition arises because DTG becomes 0 at the end of every second mark frame, and the number of frames in a block is an even number (assuming that the computer words in the data portion are a multiple of three as required).

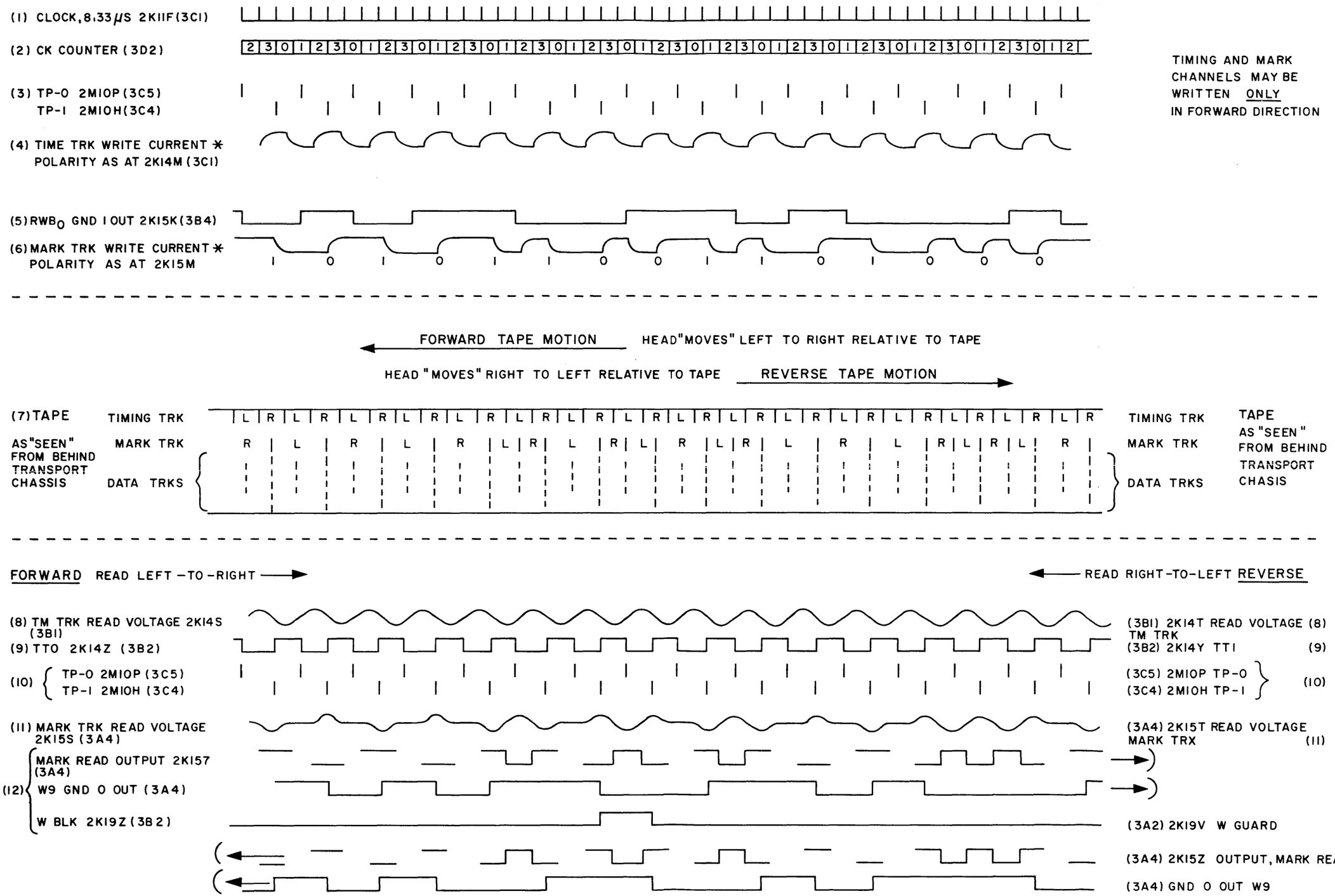


Figure 3-3 Timing and Mark Channels

3-5.2 Tape Operations

The tape operations initiated by specific computer instructions are illustrated in Figure 3-4. Control operations begin when the TA & SA delay (8:C3) clears, 215 msec after any 675-instruction that includes MMLM (6752). When reading forward, every TP-1 shifts RWB left through a network (7:A4,5). RWB_{9-11} receive the READ levels, and the information shifted out of RWB_{0-2}(6:C1,6) is lost. When reading in reverse, TP-1 shifts RWB(7:A2,3) right and the RAMP levels load RWB_{0-2}; the information shifted out of RWB_{9-11} is lost. When DTG becomes 2 (signifying that RWB has assembled a 4-line computer word) DTP-2 sets the data and DT flags through C-D gates (4:B1,3). In the all-bits mode, the DT flag-interrupt is inhibited at the gate (4:A1), but a timing error (caused by either flag being set at DTP-2) does cause an interrupt. The 1 ⟶ DF pulse (4:B2) simultaneously exchanges the contents of RWB and DB in order to make the just-read word available. The next four TP-1's assemble another word in RWB, after which DTP-2 again sets the data and DT flags (4:A2) to initiate another data break. This cycle repeats itself until the contents of the unit, motion, or function registers are changed. Reading all bits in reverse is identical to the forward procedure except that TP-1 shifts RWB to the right and the RAMP outputs of the read amplifiers (top of drawing 6) provide information for the most significant ends of the three RWB segments.

Writing in all-bits mode may begin anywhere on tape. The operation should preferably begin after detection of a block mark, since DTG is synchronized at that point. If writing is begun before synchronization, the DTG CLEAR at the end of the block could cause loss of information due to premature data transfer. Reading all bits should also begin after DTG synchronization, otherwise information read before the DTG CLEAR may be assembled out of registration by some multiple of three bits. Consequently, the program should start in the search mode, and the resulting DT-flag program interrupt should be allowed to initiate the change to the all-bits mode.

In writing all-bits forward, the initial operations following the end of the TA & SA delay are identical to those for reading above. The first DTP-2 sets the data and DT flags and exchanges the contents of RWB and DB. The contents of DB prior to this exchange will be the first word written on tape. The subsequent data break strobes new information from the computer into DB, where it remains while the first word is written, awaiting the next exchange. Unless there is a selection error resulting from the specification of a unit set to write lock (or from the simultaneous selection of more than one unit), write-enable flip-flop WREN (4:C4) is set by DTP-0 (4:D3,4) approximately 12 μsec after the data flag becomes 1. The assertion rise of the $WREN^1$ output simultaneously loads RWB_{0-3} into WB and shifts RWB left (7:A2). Thus, the first three bits of the first word are in WB, ready to be written on tape at TP-1 by the C ⟶ WB pulse (7:C2). From this time on, all subsequent RWB shift pulses and concurrent RWB_{0-2} ⟶ WB pulses (7:A5) are generated by TP-0 (7:B1), each followed by the C ⟶ WB pulse generated by TP-1 (7:C2). By this time, the data break has loaded DB with the second word; after four lines are written, DTP-2

again sets the data flag, which exchanges the contents of DB and RWB and initiates a data break to obtain the third word. This cycle repeats itself until the program makes a change in unit motion or function selection, or the tape ends.

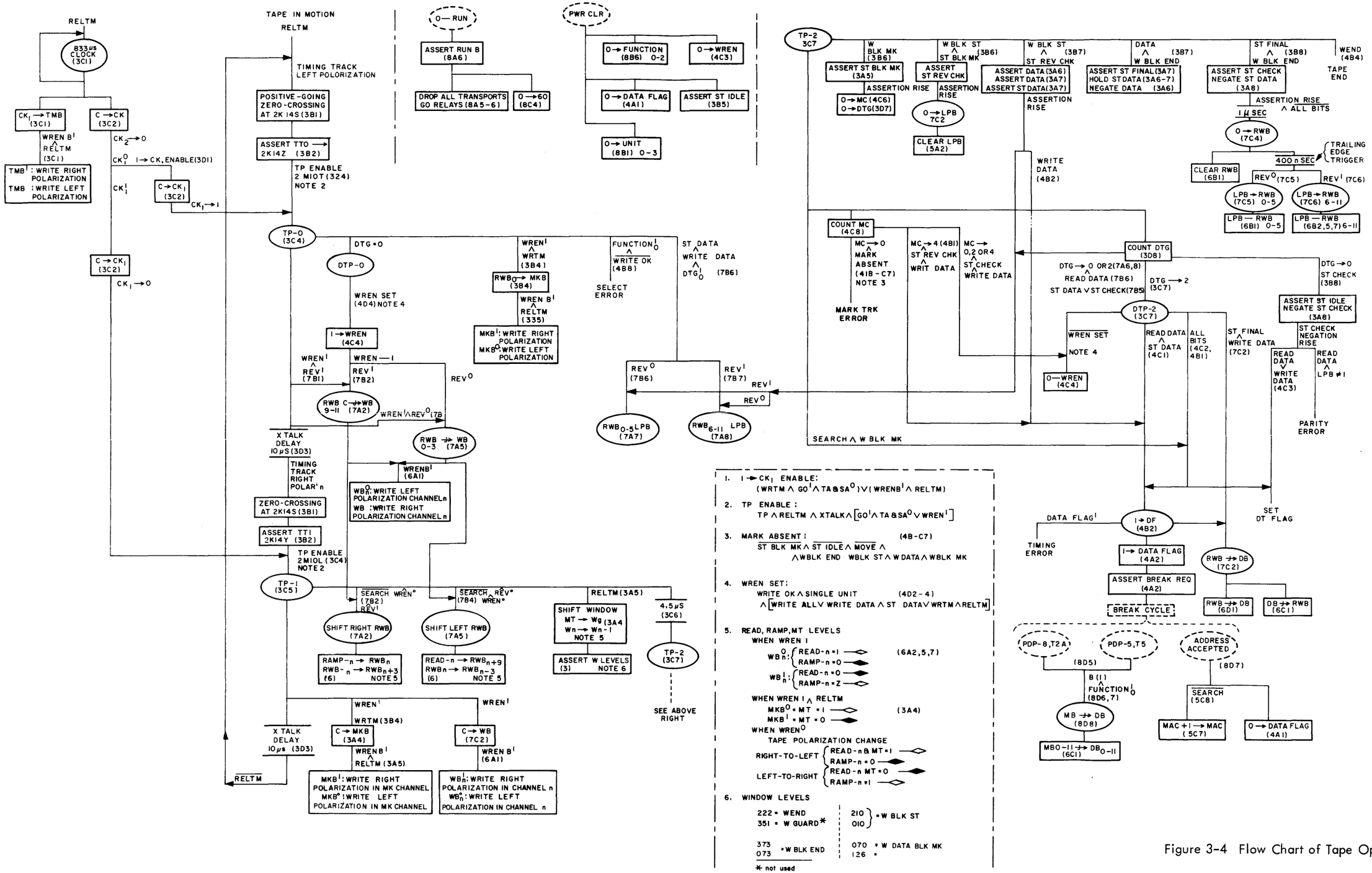
In the WRTM mode, this data-transfer procedure provides the information to be written in the mark track (all operations are identical except that TP-0 loads the contents of RWB_0 into MKB (3:B4) as well as into WB_0) and TP-1 complements MKB as well as WB.

Writing in reverse uses the same procedure, except that TP-0 loads WB with the complement of the information in RWB_{9-11}, and simultaneously shifts RWB to the right. Since the contents of RWB are shifted right in reverse, it is impossible to write the timing and the mark tracks backward (information coming into RWB_0 during right shifts depends upon the RAMP-0 level and hence is spurious).

Figure 3-5 shows the timing relationships between the various timing and control pulses and the information transferred during reading and writing. The pulses and the states of DTG are shown in lines 2, 3, and 4. Lines 6 and 7 show how words are read and assembled in the RWB and transferred into DB when the data flag is set. Line 8 shows the writing of all bits, and line 9 the timing of the write-enable flip-flop with respect to assertion of the write-all function. From line 12, notice that in writing, RWB_{9-11} accept the information being written on tape via the read-amplifier outputs. Notice also that when the data flag goes up, RWB_{0-2} contain the last three bits of the previously written word while RWB_{3-11} contain bits 0-8 of the word just written. If the function is changed from write all to read all in midstream, the first subsequent data break transfers this displaced information to the computer as the first word "read" from the tape. After this false start, subsequent RWB-DB exchanges present properly assembled information read from tape. However, the first word assembled in RWB after the function switch (i.e., the second transmitted to the computer) is quite likely to have errors in the first two lines due to incomplete recovery of the read amplifiers.

The DECtape (DT) flag is set with the data flag for every word transfer but is inhibited from causing a program interrupt in the all-bits mode. Hence, the program must either enter an MMSF loop to sense the DT flag continuously, or it must depend upon the timing error programming interrupt caused by DT flag set pulses occurring while the flag is still 1 (see Figure 3-1). One of the two methods must be used to count words in read all, because MAC has no overflow detection; consequently, an unchecked control continues to read even into locations used by the program itself.

If the tape end mark is detected by the window register, assertion of W END clears motion register bit 1 at the first subsequent TP-2 through a gate (8:C5). At the same time, TP-2 triggers the upper 35 msec delay (8:D3). MOTION $\begin{smallmatrix}0\\1\end{smallmatrix}$ disables function register decoder (8:B8) so that the write-enable flip-flop clears at the next DTP-2 (4:D3). If a new motion command is not given within the 35-msec delay period, the delay termination clears GO, stopping the tape; immediately halts operations by triggering TA & SA delay (8:C3) which inhibits the production of timing pulses; and triggers the SELECT delay,



1. 1 → CK1 ENABLE:
   (WRTM ∧ GO1 ∧ TA&SA0) ∨ (WRENB1 ∧ RELTM)
2. TP ENABLE :
   TP ∧ RELTM ∧ XTALK ∧ [GO1 ∧ TA&SA0 ∨ WREN1]
3. MARK ABSENT : (4B-C7)
   ST BLK MK ∧ ST IDLE ∧ MOVE ∧ ∧ WBLK END WBLK ST ∧ W DATA ∧ WBLK MK
4. WREN SET:
   WRITE OK ∧ SINGLE UNIT (4D2-4)
   ∧ [WRITE ALL ∨ WRITE DATA ∧ ST DATA ∨ WRTM ∧ RELTM]
5. READ, RAMP, MT LEVELS
   WHEN WREN 1
   WB0n: { READ-n = 1 ◇ RAMP-n = 0 ◆ (6A2,5,7)
   WB1n: { READ-n = 0 ◆ RAMP-n = Z ◇
   WHEN WREN 1 ∧ RELTM
   MKB0 = MT = 1 ◇ (3A4)
   MKB1 = MT = 0 ◆
   WHEN WREN0
   TAPE POLARIZATION CHANGE
   RIGHT-TO-LEFT { READ-n & MT = 1 ◇ RAMP-n = 0 ◆
   LEFT-TO-RIGHT { READ-n MT = 0 ◆ RAMP-n = 1 ◇
6. WINDOW LEVELS
   222 = WEND
   351 = W GUARD*
   210, 010 = W BLK ST
   373, 073 = W BLK END
   070 = W DATA BLK MK
   126 =
   * not used

Figure 3-4 Flow Chart of Tape Operations

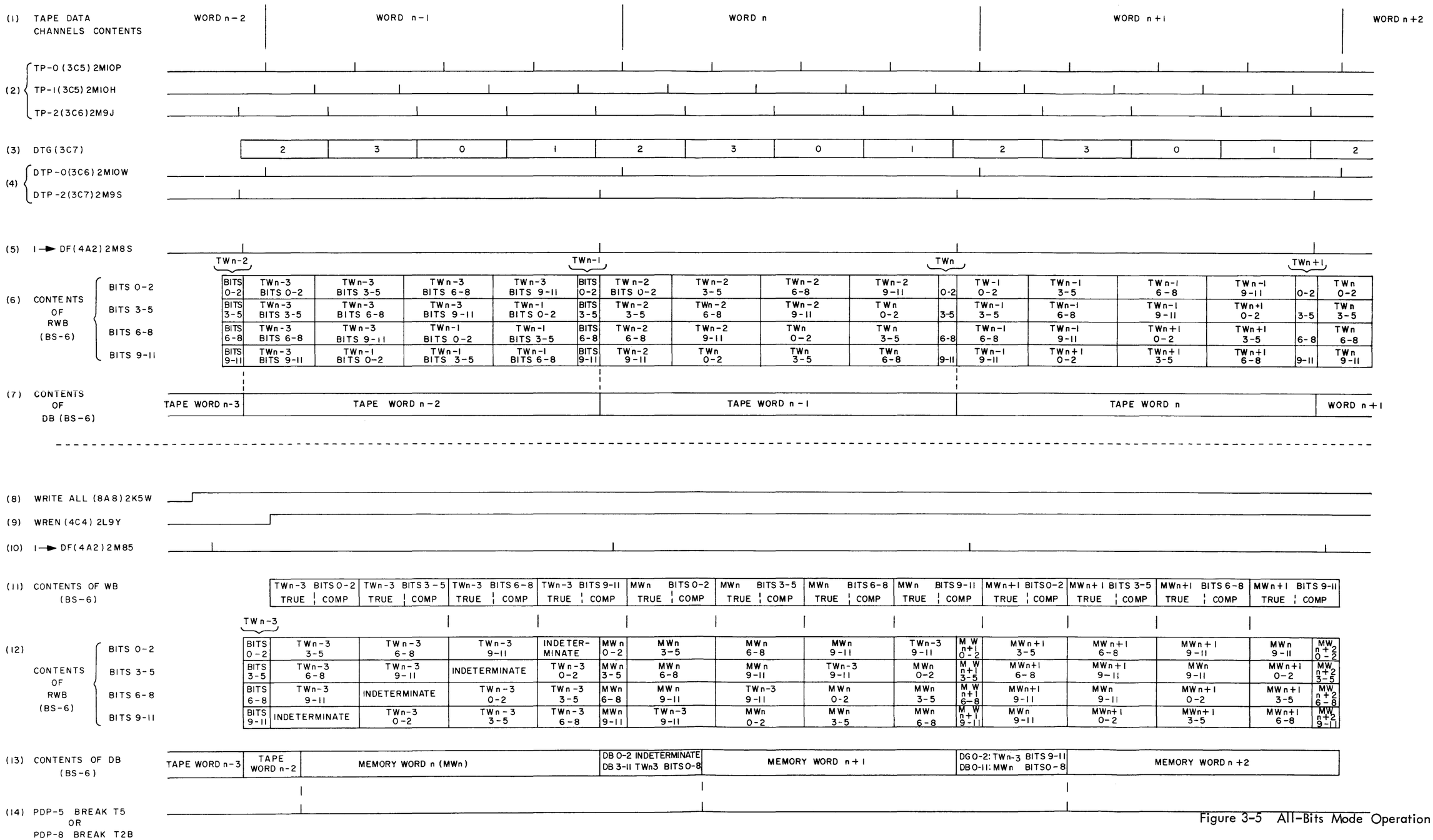


Figure 3-5 All-Bits Mode Operation

resulting in a DT-flag interrupt at the end of another 35 msec. When the program changes the unit or motion selection before the end-of-tape, the same delay chain is initiated but $MOTION_1$ is not cleared first. All data transfers stop when the TA & SA delay is triggered. In WRTM, the control is writing end marks in the mark channel near the physical end of the tape, and the window is clear because RELTM inhibits reading into it. Consequently the end-of-tape detection circuits cannot function, and the program must provide for stopping the tape to prevent it from running off the supply reel. The transport is not interlocked to stop on this condition (or on broken tape), so the rotating take-up reel whips the tape until the operator stops the transport or halts the computer.

A computer halt, caused either by the program or the operator, clears the computer RUN flip-flop. The group of five paralleled indicator drivers (8:A5-6) normally provides a ground return for all transports at connector pin M (8:A5). When RUN B^0 is asserted from the computer, the two inverters (8:A6) disable the indicator driver inputs so that all transports stop. The level also clears GO (8:B5,C5) which disables generation of timing pulses in reading. RUN B^0 does not disable the function decoder, however; so WREN remains 1 in writing, and timing pulses are generated as long as the selected transport-head relay contacts are closed (from 15 to 25 msec). If tape is moving across the head during this interval, the last word received from memory is written repeatedly. Each repetition is three bits out of registration from the previous one.

3-6 SEARCH AND DATA MODES

Tape operations in these modes depend on levels from the status generator (3:A6,7,8). Within the control, data flows just as in the all-bits modes. However, transfers to and from the computer occur only at specific times within a block and are governed by the contents of the window register. Except in search, parity is generated in writing and checked in reading for all information within the data portion of each block.

3-6.1 Control States

The status generator is a 6-stage ring counter composed of interlocking NAND gates. Each gate output can be asserted only when the other five are negated; the assertion at any gate in turn maintains the other five at cutoff. The state of this generator is changed by grounding the selected collector at TP-2 time through one of six PIs (3:B6,7,8). When new tape motion or selection commands are asserted for transports, the TA & SA delay (8:C3) holds the generator in ST IDLE while the transport reacts to the new motion command. At the end of this interval, timing pulses are generated from the tape timing track. TP-2's are then available to adjust the status generator according to the decoder window output. Except for the first, the transition to each state is conditioned by the state just to the left of the gates shown on drawing 3:B6-8; e.g., the reverse check state can be entered only from the MK BLK ST (3:B2).

Since IDLE is the initial state, the only decoded window output that can affect the status generator (after the TA & SA falls) is the W BLK MK. At the last TP-1 of the mark frame containing the forward block number, this level is asserted, and gates TP-2 to assert ST BLK MK (3:B5). Hence, operations governed by the status generator cannot begin until the start of a new block on tape even though timing pulses may have begun during the previous block. At the last TP-1 of the L frame on tape, the window decoder asserts the first of four block-start levels (3:B3). The first block start gates TP-2 to assert the reverse check state (3:B6); during which the reverse parity check group is read from tape and transferred to the longitudinal parity buffer. In the second block state, TP-2 simultaneously asserts DATA (3:A6) and ST DATA (3:A7); thus the control enters the data state about 12 μsec before the beginning of the F frame on tape (this frame contains the first data word of a block). As the end of a block approaches, the first of four block-end marks allows TP-2 to assert ST FINAL (3:B7). This assertion negates DATA but holds ST DATA. The final state inhibits further data flags when writing the last word. To write parity, or to check it when reading, the second block end causes assertion of ST CHECK. Two tape lines later, at the end of the 6-bit reverse parity check group, the DTG counter becomes 0, and the next TP-2 returns the control to the ST IDLE (3:B8).

Mark counter MC is shown at the lower right of drawing 4. Like DTG, this counter is cleared by the assertion of ST BLK MK at the beginning of a tape block. Each TP-2 counts MC in straightforward binary fashion until the count of 5. The sixth TP-2 then clears the counter, because MC_0^1 prevents the MC_2 carry output from setting MC_1. Thus the counter clears in synchronism with the generation of decoded window levels from the mark track. Just above MC is a gate that accepts four window levels; BLK END, BLK ST, DATA, and BLK MK. Except in the ST BLK MK or ST IDLE or in the MOVE function, one of these four window levels must be asserted at the TP-1 just before the TP-2 that clears MC. Otherwise, when the counter clears, MC_0 sets the parity-or-mark-track-error flip-flop through the C-D gate (4:D7). The error is inhibited in ST IDLE because the decoded window levels for the guard, REV BLK MK, and the extend marks are not used by the control. The error must be inhibited in the BLK MK ST because, similarly, the REV GUARD MK is unused. The error network actually does not check for the FWD BLK MK or for the first BLK ST since window levels for both of these marks are required at the status generator to enable the error-checking logic. If either is absent, the control remains in the ST IDLE or BLK MK ST, either of which maintains the error-check inhibit. (The window register, a Type 4260 Mark Track Decoder, recognizes the unused register configurations and asserts decoded outputs at unconnected pins. A complete description of the Type 4260 is given in Chapter 4.)

3-6.2 Search

Figure 3-6 shows the behavior of the control when initiated by the search mode to locate a specific block and then switched to the write-data mode after the selected block number is found. The

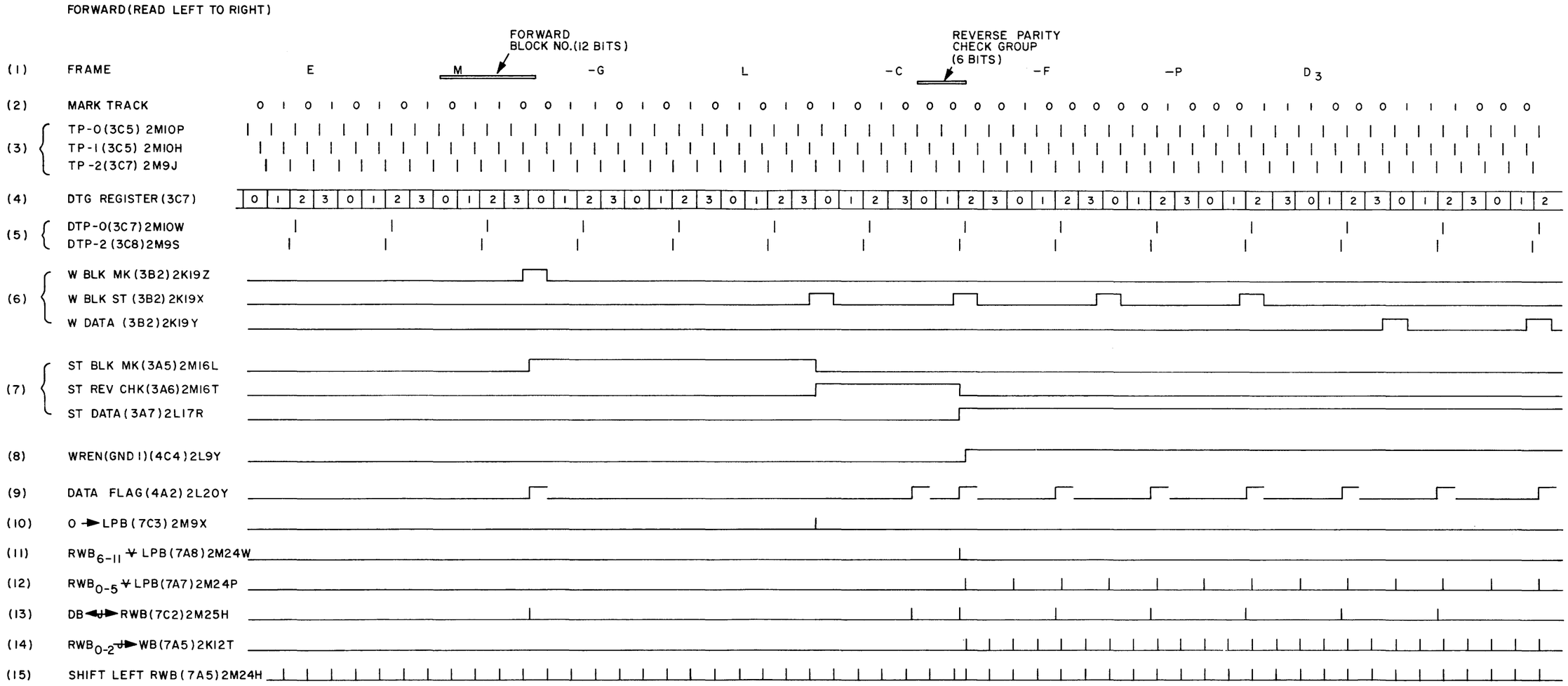


Figure 3-6 Search and Data Mode Timing
Block Start

upper left of Figure 3-6 indicates the relative timing of logical functions in the search mode. Lines 1 and 2 of the chart show the designation and binary contents of the mark-track control information. Lines 3, 4, and 5 show the timing pulses, and the DTG counts as in Figure 3-5. The three decoded window levels that govern operations at the beginning of a block are shown in line 6, and the control states assumed in response to these window levels in line 7.

As soon as the TA & SA delay times out, TP-1's shift RWB left to assemble 12-bit words from the information in the data channels. The window block-mark level, signifying that the 12-bit block number is in RWB, enables the C-D (4:C2) allowing the next TP-2 to set the data and DT flags at the same time the control enters the block-mark state. The 1 ⟶ DF causes the DB-RWB exchange, making the block number available in DB for transfer to the computer during the ensuing data break. The program then compares this block number with the one desired and takes appropriate action.

In the search mode, the RWB shift logic (upper left of drawing 7) causes left shifts on every TP-1, regardless of the direction of tape motion. This means that lines from the tape data channels are assembled in reverse order when searching backward. In other words, if the octal contents of four successive lines in the tape data channels are 1234, these lines will be assembled in the RWB as 4321 when searching backward. Note that the order of 3-bit groups is changed, not the order of bits; i.e., when searching backward, the lines are read from the tape in the reverse order, but the order of bits is not reversed within each line. The program has three options. It may write forward block numbers conventionally and reverse block numbers with the order of lines on tape reversed; it may construct the correct block number when searching backward by reversing the order of 3-bit groups received from the control; or it may simply elect never to search backward.

3-6.3 Write Data

The control function may be switched to write data at any time (see Section 3-6.5). However, to write a complete block of information into a selected block on tape, the function must be changed within 533 μsec after the specified block number is found. The end of this permissible interval is shown as the vertical line in the upper center of Figure 3-3. The behavior of the logic to the right of this division takes place if the program selects write data forward.

The transition of the MC contents of 4 in the reverse check state sets the data flag (4:A1) to call from memory the first word to be written and exchanges the contents of DB and RWB. The contents of DB will be replaced by the information transfer from memory during the data break. During the second block-start level, the ST DATA assertion rise again sets the data flag, loading the first word into RWB and calling the second out of memory. Because the control is now in the data state, the first DTP-0 (about 12 μsec later) sets the write enable flip-flop (4:C4). When WREN becomes 1, it immediately transfers the first line from RWB_{0-3} into WB and shifts RWB left (7:A5). This first shift must be accomplished by

WREN because the C-D gate (7:B3) that allows TP-0 to perform the same function requires 1 μsec to enable the pulse input. All subsequent shifts left and concurrent RWB_{0-2} ⟶ WB pulses are generated by TP-0 through the C-D gate (7:B3). Throughout the data portion of the block, the control proceeds exactly as in the write-all function, with data flags and RW-DB exchanges occurring on every DTP-2 pulse. In write data, however, the DT flag is not raised with the data flag.

Figure 3-7 shows tape operations near the end of a block when writing data forward. Since the data flag set pulse at DTP-2 is gated by the DATA level (4:C1), the last data flag occurs toward the end of the P frame on tape. During the subsequent data break, the memory loads DB with the last word of the block to be written in the last four lines of the F frame. To write this last word, however, the DB-RWB exchange must occur once more. This is accomplished by DTP-2, during the assertion of ST FINAL, through gate (7:C2). Transfers into WB and concurrent RWB shifts left occur on TP-0 as long as ST DATA is asserted, also twice more (while the control is in the check state immediately following) in order to write the forward parity-check group. When ST CHECK falls, it sets the DT flag (4:B3), causing a program interrupt at the end of the block.

The parity check group is generated in the longitudinal parity buffer (LPB) shown at the top of drawing 5. The entire register may be cleared, and individual bits may be complemented, according to the contents of either the left or right half of RWB. An LPB bit is complemented if the corresponding RWB bit contains a 0. The complement pulse may be concurrent with the pulse that shifts RWB, but the prior contents govern the complement through the C-D gates.

Timing pulses that affect the LPB are shown in lines 8-15 of Figure 3-7. At the beginning of the block, the register is cleared when the machine goes into ST REV CHK through the PA (P7:C3). The last two RWB-left shifts before WREN becomes 1 read the 6-bit reverse parity check group into RWB_{6-11}. When the machine goes into the ST DATA, the C-D gate (7:B7) loads the complement of this check group into LPB by producing the RWB_{6-11} ∀ LPB pulse. The first word to be written is concurrently loaded into RWB by the 1 ⟶ DF (7:C1). From this point on, the initial TP-0 and the third TP-0 of each word produce the RWB_{0-5} ∀ LPB pulse (7:A7). At the time of the first, the full word is in RWB, so the left half of the word governs the complements into LPB. At the time of the third, RWB has shifted left twice, so the right half of the word, now in RWB_{0-5}, governs the complements. Hence, throughout the data written in each block, a 1 in LPB bits 0, 1, or 2 represents odd parity for the information written in odd-numbered lines on tape; a 1 in LPB bits 3, 4, or 5 represents odd parity for the information written in even-numbered lines.

Near the end of the block (see Figure 3-7), the last LPB complement pulse is generated when RWB_{0-5} contain the last six bits to be written on tape. At the end of the F frame, the control goes into the check state. The assertion of ST CHECK triggers a 1 μsec delay (7:C4) which in turn triggers a PA.

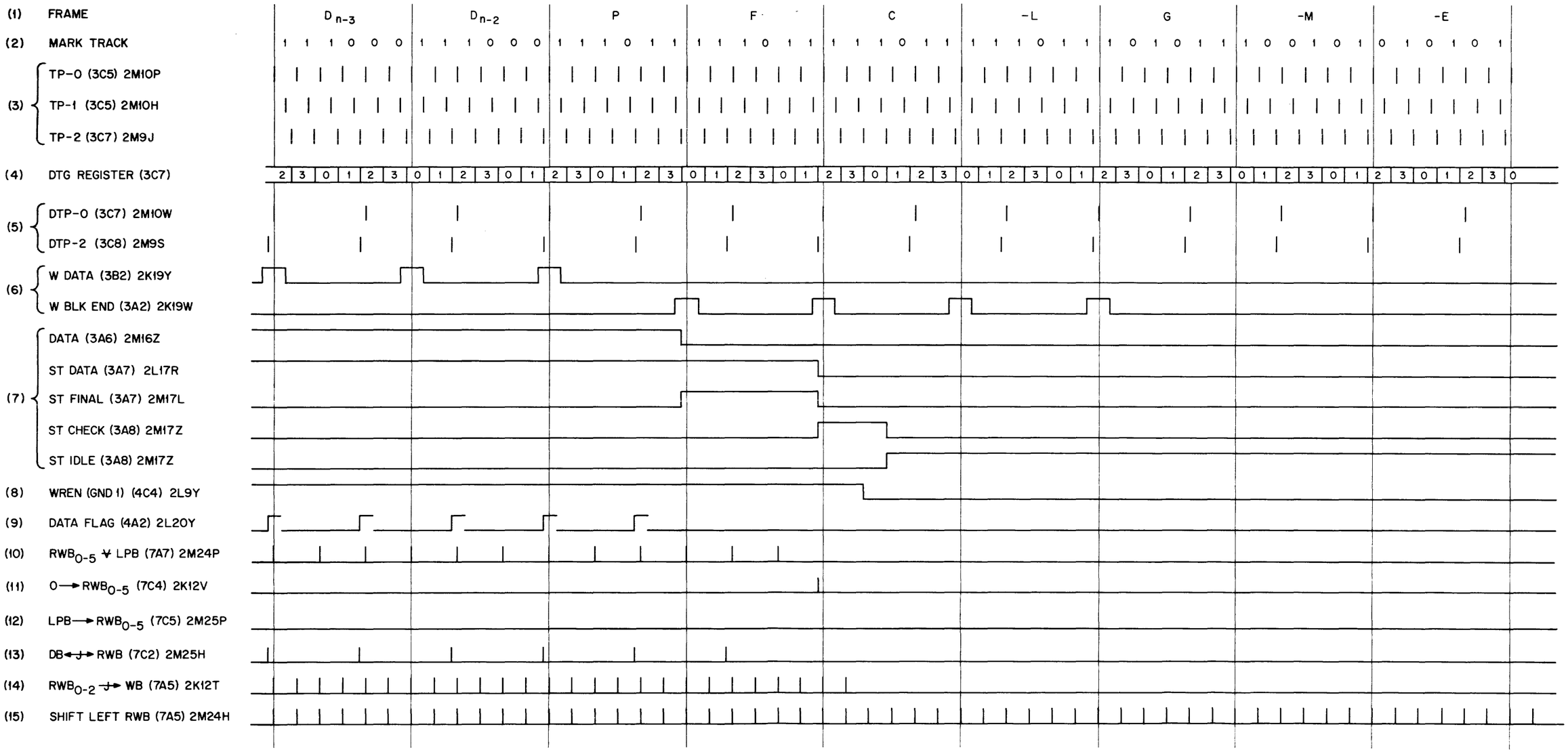


Figure 3-7 Data Mode Timing

The leading edge of the output pulse clears RWB, and the trailing edge loads the left half of RWB with the contents of LPB. The next two TP-0's transfer this information to the write buffer as the 6-bit forward parity-check group.

On the second TP-2 in the C frame, DTG becomes 0, and the contents of MC become 2; the $MC_2 \longrightarrow 0$ transition clears the write-enable flip-flop through C-D gate (4:C2). The left shifts for RWB are now again generated by TP-1 (the control reads continuously whenever it is not writing). The next TP-2 asserts ST IDLE, and the control remains inactive until the W BLK MK level at the beginning of the next block.

Writing data backward is essentially the same procedure, except that LPB is initially loaded from the left half of RWB; because the check group is read in at the left in reverse, RWB is always shifted right, and WB is loaded with the complement of the information in RWB_{9-11}. Parity is checked in LPB from the right half of RWB, and is transferred to the right half to write the check group at the end of the block.

3-6.4 Read Data

In reading, the timing of the RWB shifts never changes. Although the direction of shift depends upon the direction of tape motion, shifts always occur on TP-1 throughout a block. Other differences between reading and writing concern the timing of the data flag and the behavior of the parity-check logic.

Each DTP-2 in the data state signifies that a full word is properly registered in RWB, and consequently sets the data flag. Unlike the writing operation, no information transfer is necessary during the reverse check state. The DT flag is not concurrently set as in the all-bits mode. Pulses that complement LPB according to information in RWB must occur after each 6-bit group is read from tape; thus, they occur when the contents of DTG become 0 or 2, i.e., on the DTG_1^0 transition (7:B6, 7:A8). The last data flag occurs at the end of the F frame, when ST DATA falls. Since the data state is no longer asserted, no transfers to the computer take place after the last word in the data portion of the block, i.e., the last word in the F frame. However, RWB continues to shift throughout the interblock frames, and the register continues to assemble words from whatever is written in the data channels. The first six bits read from the C frame are the forward parity-check group; the first two TP-1's in the check state load this information into the right half of RWB when reading forward, the left half in reverse. The DTG count to 0 complements LPB bits that correspond to the 0's in this check group, the same as if the check group were data read from tape. But the 0's in the check group represent even parity for the data written in the block; and LPB already contains 1's representing odd parity corresponding to the 1's in the check group. After the final complement pulse for LPB, therefore, LPB must contain all 1's. If this is not the case, the negation of ST CHECK on the following TP-2 sets the parity-or-mark-track-error flip-flop, causing a program interrupt.

3-6.5 Read/Write Function Switching

Switching from read data to write data within the data portion of a block causes a control operation similar to switching from read to write in the all-bits mode. The last complete word read from tape before the switch is duplicated as the first word written, followed by the new words transferred from memory. Similarly, after switching from write to read, the first word available is the last word written and is presented three bits out of registration. The following words read from tape are presented properly, although the first line may have an error due to incomplete read-amplifier recovery. Correct parity is impossible to retain through a switch in function in the data mode. Due to read-amplifier recovery-time requirements, an error is likely to occur in the first line read from tape after a write-to-read switch. Then, parity will probably be disturbed. On a switch from read to write, the parity buffer not only generates parity on the same word twice (once reading, the second writing), but also misses one 6-bit group, unless the computer has carefully timed the function switch to occur within the 12-μsec interval between the DTG_1 clear and the following DTP-0. If the switch occurs before this interval, the group is missed because the read-data function is negated at the time of the DTG_1 clear. Consequently, no complement pulse for LPB is generated until the following TP-0, at which time new information has replaced the last word read in RWB.

CHAPTER 4
CIRCUIT DESCRIPTION

4-1 INTRODUCTION

Type 552 DECtape Control logic contains two classes of circuits. One class performs the conventional logic functions such as the acceptance and production of DEC logic levels and pulses. This class of circuits includes inverters, flip-flops, gates and pulse amplifiers. The second class performs special functions which apply particularly to the Type 552 or similar applications. This special class includes solenoid or indicator drivers, read/write amplifiers, and block-format decoders.

Conventional DEC circuits are fully described in DEC catalogs Digital FLIP CHIP Modules (C-105) and System Modules (C-100). Brief descriptions of the basic circuits of these modules are given in the next subsection. The special circuits (some of which are described in DEC catalogs) are also discussed in this chapter. In this discussion, reference is made to the replacement schematics in Chapter 6. As stated in Chapter 6, the replacement schematics are furnished only for test and maintenance purposes.

All module components are mounted on a dip-soldered epoxy board surrounded by an aluminum frame 1/2 inch thick and 4-1/8 inches high when in the mounting panel. The module may be 7 or 10 inches long depending on the space required to contain all circuit components. Logic and power connections are made through 22-pin Amphenol plugs, connected to the circuits by flexible wiring to minimize strain. Four connector pins on each module are reserved for supply voltages: pins A and B carry +10v (duplicated for submodular marginal checking), pin C supplies −15v, and pin D is grounded. Additional pins may be used for ground as necessary. Modules that generate standard negative logic levels have an internal −3v supply.

4-2 CONVENTIONAL CIRCUITS

4-2.1 Clamped Loads

The diode in the clamped load of Figure 4-1 limits the negative-level excursion at a module input or output so that it supplies the current necessary to maintain the output at −3v. With a 1.5K load resistor, the maximum diode current is 8 ma under no-load conditions and decreases to 0 as the current increases to the 8-ma maximum. Drawing more than maximum current creates an excessive drop across the load resistor, breaking the clamp. Then, the output voltage becomes more positive and may cause marginal driving conditions in fan-out. In most modules, jumpers connect clamped loads to inverter

collectors or to inputs driven by external inverter collectors. The −3v supply is established by forward drops of 0.75v each across four series-connected silicon diodes. The resistor accepts enough current to regulate the supply under all load conditions.

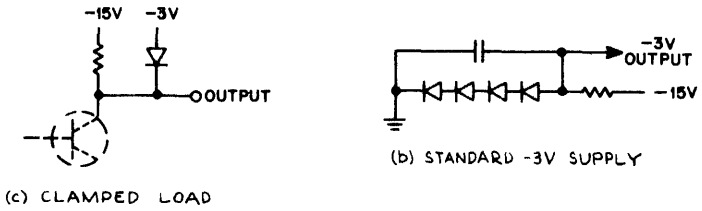


Figure 4-1 Clamped Load and Standard Power Supply

4-2.2 Inverter

An inverter (see Figure 4-2) may be used either as a level gate or a pulse gate. PNP transistors are always used in these inverters and are operated either in saturation or in cutoff. If the emitter is grounded and the collector connected to a negative load, the collector output is inverted with respect to the base input (both are standard DEC logic levels or negative pulses). Base input loading is furnished by the 3K resistor so that a saturating base current of 1 ma flows through the transistor when −3v is present at the input. A bypass capacitor at the input provides overdriving current which speeds switching. The more positive input to an inverter is usually derived from the collector of a saturated transistor (approximately −0.4v). Base bias at 0v is supplied by a resistor returned to +10v; cutoff-bias resistors allow marginal checking base leakage or dc gain of the inverter.

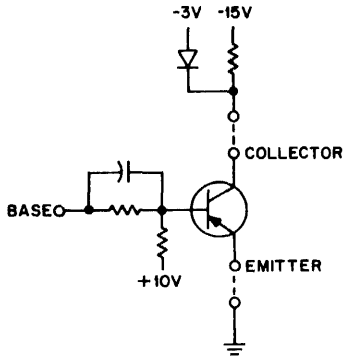


Figure 4-2 Basic Inverter

4-2.3 Gates

Diode modules include simple networks for general-purpose pulse and level gating, capacitor-diode gates (C-D gates), and decoders. Diode modules contain two or more logic gating circuits consisting

of a number of diode-coupled inputs driving an inverter. Usually, a clamped load is available for each inverter. Input diodes provide either the AND or the OR function depending upon the polarity of the input assertion level (see Figure 4-3). Since the transistor amplifies and inverts the diode network output, the combination is properly termed a NAND or NOR, hence the symbols $\sim\Lambda$, $\sim V$. In the negative NAND gate of Figure 4-3(a), the transistor is driven into conduction only if inputs A, B, and C are all negative (−3v), allowing R1 to forward-bias the transistor emitter-base junction. With ground at any input, R2 reverse-biases the junction and cuts off the transistor. In this gate, the two silicon diodes between the gating diodes and the inverter base compensate for the slightly negative offset in an input ground level caused by the saturation drop across a preceding inverter. The two diodes shift the level at the inverter base approximately 1.4v to ensure reliable cutoff when any nominally ground input is applied to the gate. The positive diode NAND gate of Figure 4-3(b) saturates the transistor through input resistor R4 when either D, E, or F is negative; consequently, a negative voltage can appear at the output only when all three inputs are ground. Except for the input diodes, this circuit is identical to the standard DEC inverter circuit.

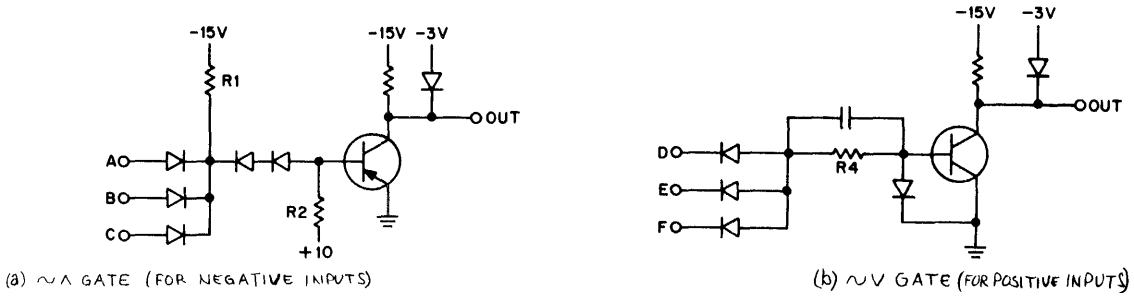


Figure 4-3 NAND Gates

Decoder circuits are simply diode gates in which an additional level of input diodes precedes the inputs discussed above. In most decoders this additional bank of diodes simply provides isolation between three or four NANDs on a module. Common inputs (e.g., the three or four bits of a register) may then drive all circuits on the board at different assertion levels so that one decoder output is asserted for each configuration of register contents.

4-2.4 Capacitor-Diode (C-D) Gates

In the basic positive C-D gate of Figure 4-4(a), a positive pulse or level change at A produces a positive pulse out whenever a ground-enabling level has been present at B for at least 800 nsec before

the pulse. The ground-enabling level discharges the capacitor, allowing a positive-input pulse to forward-bias the output diode and be coupled through to the output. When the enable input falls to −3v, the capacitor charges, and the anode of the output diode becomes negative so that a positive-input pulse is superimposed on the negative level. Since the waveform never exceeds ground, the output diode cannot become forward-biased and the pulse is blocked by subsequent logic. In the basic negative C-D gate of Figure 4-4(b), the diode polarity is reversed and the pulse input, enabling input, and output are negative.

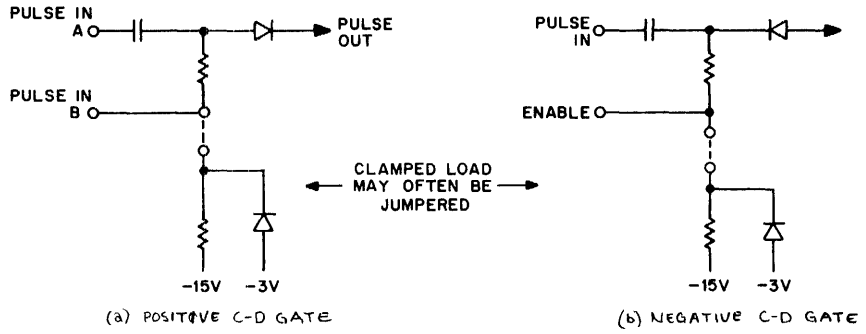


Figure 4-4 Capacitor-Diode (C-D) Gates

The positive C-D circuit appears as shown at the inputs of flip-flops. Self-contained C-D modules have one or a number of negative C-D gates for driving output inverters, providing positive-output pulses suitable for the direct-set or clear inputs to flip-flops. Since the enabling input to a C-D gate charges or discharges a capacitor, the enable input may be the output of a flip-flop whose state changes on the gated pulse. Even though the enable input deteriorates as the pulse is coupled through, the capacitor maintains the enable throughout the pulse width.

4-2.5 Flip-Flops

The flip-flop, or bistable multivibrator, is a 2-state device used primarily for short-term storage of logical conditions within a digital system. Simple flip-flops may be constructed by interconnecting two grounded-emitter inverters as shown in Figure 4-5. When one inverter is cut off, its negative output holds on the other transistor. This operation, in turn, holds off the first transistor. Driving either the base of the conducting transistor or the collector of the cut-off transistor with a positive pulse changes the state of the flip-flop by turning off the conducting inverter. This turnoff, in turn, establishes conduction in the other.

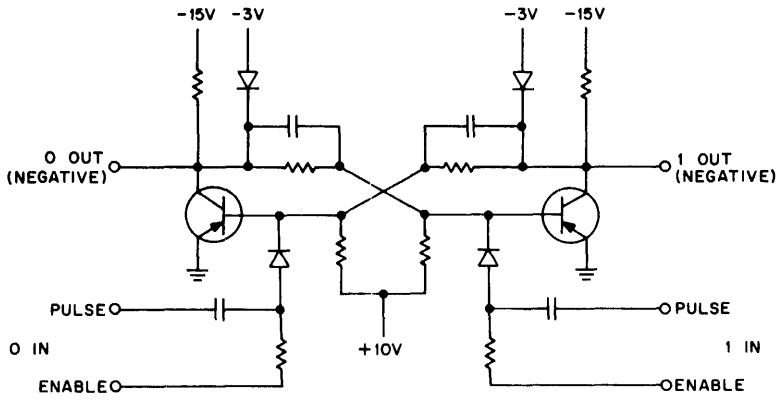


Figure 4-5 Basic Flip-Flop

Positive input pulses for the inverter bases may be applied through C-D gates as in the Type 4215 flip-flop. Positive-going pulses for flip-flop collectors must be supplied from additional internal or external inverters. In most flip-flops, a complement input internally gates a positive pulse to the base of the conducting transistor. Such an input always changes the state of the flip-flop. Some modules have an input-pulse inverter common to many flip-flops on the board; e.g., the Type 4217 flip-flop contains a pulse inverter which drives four C-D gates to set individual bits; and the Type 4227 flip-flop contains two pulse inverters which clear combinations of flip-flops selected by jumpers. In shift registers and assembly modules, input pulses can set or clear some flip-flops according to the state of others on the same board, even though the gating flip-flops may be unavailable at output pins. Type 4228 and 42281 flip-flop assembly circuits have this capability.

4-2.6 Pulse Amplifiers

The three types (i.e., 4604, 4605, and 4606) of pulse amplifiers used in the DECtape control perform the power amplification and pulse standardization necessary to meet DEC requirements. Each type contains three pulse amplifiers, and each amplifier uses six of the eighteen module connector pins available for signals (see Figure 4-6). The output pulse length is standardized by a multivibrator which applies a 0.4-μsec or a 1-μsec pulse to an output transistor whose collector is transformer-coupled to the output pins. Both ends of the transformer secondary are available, and either may be grounded. Hence, positive pulses are available at one pin or negative pulses at the other.

A negative pulse or level change triggers the multivibrator through a permanently enabled C-D gate. Amplifiers on each module type contains an NPN input inverter that accepts positive or positive-going level changes through another permanently enabled C-D gate. On the Type 4604, the remaining two pins allow connection of an external capacitor to lengthen output-pulse duration; any pulse length up to 1 μsec may be obtained. On the Type 4606, the remaining two pins are the pulse and enable inputs to a second negative C-D gate which passes conditioned inputs to the amplifier circuit.

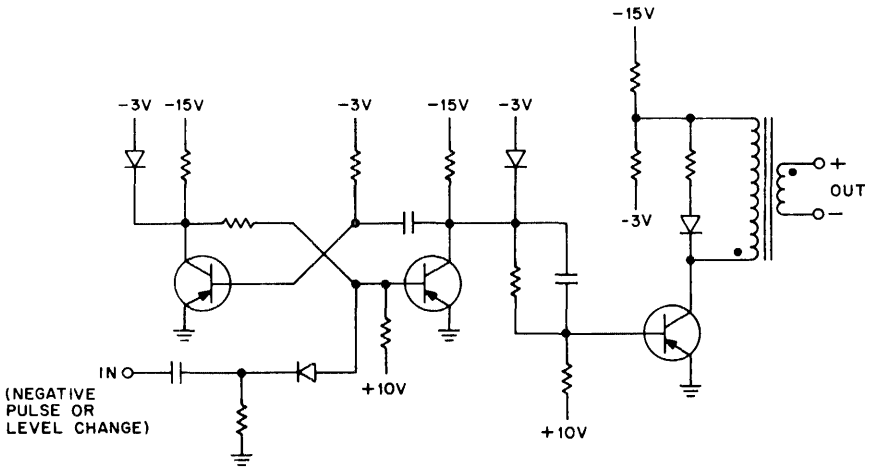


Figure 4-6 Basic MV-Type Pulse Amplifier

The Type 4605 is the decoding pulse-amplifier module used in the logic of the device selector. A 6-input AND gate for negative levels receives jumper-selected inputs from pins M to Z. When all six inputs are negative, the gate inverter saturates and enables all three PA circuits on the module. Each circuit receives one of the three in/out pulses (IOPs) from the computer and produces an in/out transfer (IOT) at the output when the module is enabled. Except for certain circuit values, the output stage of each 4605 PA is identical to that in the 4604-4606 circuits. Instead of a multivibrator, the Type 4605 uses a single inverter which is transformer-coupled to the output state (see Figure 4-7). Pulse timing is standardized by an R-L net consisting of a clamped-load return resistor and the inductance of the interstage transformer primary.

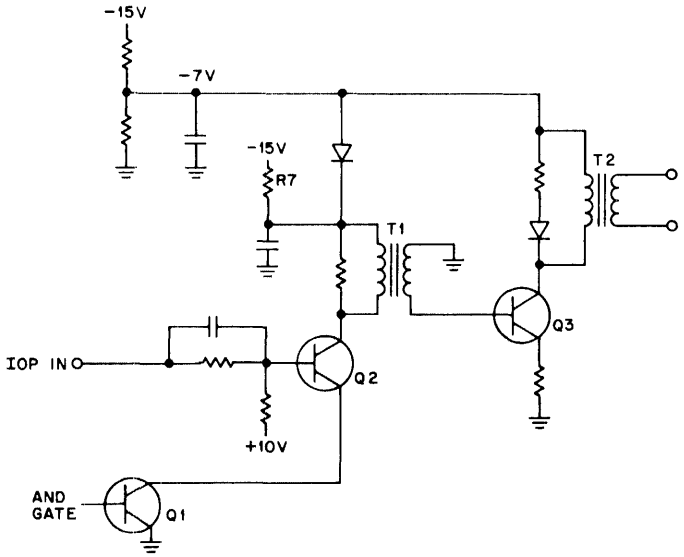


Figure 4-7 Basic Transformer-Coupled Pulse Amplifier

When an IOP saturates Q1, approximately 7v is applied across the T1 primary until the primary current causes too great a drop across clamped-load return resistor R7. At this point the clamp breaks, and the voltage across the T1 primary falls rapidly. Circuit values are selected to make the pulse 0.4 μsec long; this pulse drives the Q3 base to generate a similarly standardized pulse at the output pin through T2.

Either positive or negative pulses are available from the T2 secondary; but internal jumpers select the pulse polarity instead of module-connector wiring. All Type 4605 Pulse Amplifiers in the 552 DECtape Control are jumpered to produce negative pulses, but sometimes the positive overshoot is used as the trigger in subsequent logic.

4-3 SPECIAL CIRCUITS

4-3.1 Level Standardizer Type 1501

This module (see reference schematic RS-1501-5) contains three identical difference-amplifier circuits plus a −3v supply; hence a description of the first amplifier Q1-Q2 applies to all three. The Q1-Q2 amplifier compares the input level at pin J with a fixed-reference level at pin H. When the J level is more negative than the H level, Q1 conducts, and the current passing through R3 holds the common-emitter junction at a voltage sufficiently negative to cutt off Q2; under this condition a little more than 1 ma passes through R4 and R7. The bias thus established at the base of output inverter Q3 causes Q3 to saturate. Since pin F is grounded, pin E becomes grounded through Q3. As the J level becomes more positive than the H level, the current through Q1 decreases and Q2 starts to conduct. When the current through Q2 reaches approximately 2 ma, the collector of Q2 is approximately at ground level; under this condition the voltage drop through R5 and R6 holds Q3 at cutoff and pin E floats.

In the DECtape control, the external resistances shown on BS-8:A1 hold pin H at 0.31v and pin M of the center amplifier at 0.87v. Pins J and N are returned through a 5-ohm resistor to ground level. This 5-ohm resistor must provide all current for the selection relays in the transports through the BCD decoder associated with the select register. The selection relay requires approximately 130 ma, creating a drop of approximately 0.65v across the 5-ohm resistor. The two output inverters for the left and the center difference amplifiers are connected in series; consequently, if either cuts off, the output at pin L becomes −3v. If the operator fails to set the transport address selectors to correspond with addresses used by the program, one of two conditions may occur. The select register contents may not correspond to the address of any transport selector so that no transport is selected; or, two or more selectors may correspond to the address so that multiple selection occurs. When no transport is selected, no load is applied to any output of the Type 4671 Decoder; consequently, no drop occurs across the 5-ohm resistor. As a result, pin J is more negative than H, and output inverter Q3 cuts off. If more than one transport is selected, the decoder must supply approximately 260 ma, causing a 1.3v drop across the 5-ohm resistor. Then, pin M is more negative then N, and output stage Q6 cuts off. In either case the output at L becomes −3v, asserting a selection error.

4-3.2 BCD Light Driver Type 4671

This module contains ten identical stages (see reference schematic RS-4671-4), each consisting of a diode AND gate for negative levels, an emitter follower, and a high-current output inverter. The AND gates contain only the number of diodes necessary to decode the conventional 4-bit BCD or excess-three decimal codes; no interlock exists to prevent simultaneous assertion of two or more outputs in response to illegal input codes. For example, code 1010 causes a simultaneous assertion at outputs S and Y. Except for diode connections, all stages are identical; hence, a description of Q1-Q11 stage applies to all.

The emitter of emitter follower Q1 is returned through R11 to +10v; any ground level input to the AND gate D1-D4 causes the Q1 emitter to assume a level close to ground. The emitter of Q11, the output inverter, is clamped at approximately −1v by diodes D34-D35. When the Q1 emitter is more positive than −1.2v, Q11 is cut off. However, when negative levels appear at all diodes of the input AND gate, the Q1 emitter voltage drops and the base current of Q11 flows through Q1 and is returned to −15v through R21. As Q11 saturates, the output P is returned to the −1v clamp level. In the DECtape control, pin D is connected to the ground through one end of the 5-ohm current-sampling impedance associated with the Type 1501 Level Standardizer (see BS-8:A1).

4-3.3 Integrating Delay Type 4303

This module contains a positive C-D gate (Q1), two monostable multivibrators (Q2-Q3 and Q10-Q11), two difference amplifiers (Q5-Q6 and Q7-Q8), three inverters (Q1,Q4, and Q9), and a negative dc supply (see reference schematic RS-B-4303-17). Voltage levels of −0.75, 1.5, −3, −4.5, −5.25, and −6v are tapped from the internal negative supply. The three inputs are applied to pins K, S, and R. Input K may be a DEC standard 0.4-μsec negative pulse or a negative level. Input S may be either a DEC standard 0.4-μsec positive pulse or a positive-going level change. This pulse is gated to the Q2 base by a ground at pin T. Input R requires a positive pulse such as the output of a positive C-D gate (e.g., C1-R1-D1). The 1 and 0 outputs appear at pins W and U.

When the multivibrator circuits are in the 1 state, the 1-output levels are at −3v and the 0-output levels are at ground. In the 0 state, the output levels are reversed. Multivibrator (Q2-Q3) assumes a 1 state when any of the three inputs at pins K, S, and R are pulsed. The circuit returns to the 0 state after a selected delay which begins at the termination of the input signal. The delay is variable from 3.4 μsec-0.9 sec in five overlapping ranges. Connection of one of five internal capacitors (C6-C10) determines the delay range. C7 is permanently connected and gives the shortest range. Connecting C6, C8, C9, or C10 (E, F, H, or J) to ground (D) increases the range by successive factors of approximately 10. Potentiometer R10 determines the delay within each range if Y is jumpered to X. Alternately, an external potentiometer connected between Z and X may control fine delay.

In the quiescent state, Q1, Q3, Q4, Q5, Q8, Q9, and Q10 are off; Q2, Q6, Q7, and Q11 are on. Voltage divider R2-R3 shifts the ground level at input K positive, biasing Q1 off. Multivibrator Q2-Q3 is in its stable state, with Q2 held on by base current flowing through R5, and Q3 held off by voltage divider R8-R9. With the Q2 collector at ground, voltage divider R11-R12 biases Q4 off.

In the first difference amplifier (slicer), Q5 is off and Q6 is conducting. D6 clamps the Q6 collector at −0.75v to hold Q6 out of saturation. The common emitter connection of NPN transistors Q5 and Q6 follows the voltage (−1.5v) at the base of Q6, cutting off Q5. Slicer transistors Q7 and Q8 are on and off, respectively. The series combination of R13, R14, and potentiometer R10 draws sufficient current from the Q7 base to saturate Q7 even if potentiometer R10 is set at maximum resistance. Saturation of Q7 holds the common emitter connection of Q7 and Q8 at −5.25v (the Q7 collector voltage), and the more positive voltage (−4.5v) at the Q8 base holds Q8 at cutoff. Q9, therefore, is back-biased through R19 and cut off. Q10 is held off by the voltage dividers R23, R21, and R24. Multivibrator Q10-Q11 is in its stable state with Q10 off and Q11 on.

The overall circuit is triggered from its quiescent state when an appropriate input at K, R, or S drives the Q2 base positive. Then multivibrator Q2-Q3 shifts its state so that Q2 is off and Q3 on. Diode D4 clamps the Q2 collector at −3v and this level, coupled to the Q4 base by R11 and C5, drives Q4 into saturation. The grounded collector of Q4 drives the bases of Q5 and Q7 positive; Q7, in turn, drives output multivibrator Q10-Q11 to its temporary state. Q5 is part of the feedback loop that returns the signal to input multivibrator Q2-Q3 and causes it to revert to its stable state.

As the Q7 base goes positive, Q7 turns off and Q8 turns on, and their common emitter connection rises to the Q8 base voltage. Q8 does not saturate because its rising collector voltage is clamped at −5.25v by the Q9 turnon. (Q9 saturates and its collector drops to −5.25v). The Q9 collector voltage is connected through R20 to the Q10 base, causing a turnon of Q10. Then multivibrator Q10-Q11 flips to the temporary state, with Q10 on and Q11 off. The circuit output is now in the 1 state (W at −3v, U at ground).

In the feedback loop to input multivibrator Q2-Q3, the voltage drop through R14 causes C7 (and any capacitor C6, C8, C9, or C10 in parallel with it) to approach ground. When this feedback voltage reaches approximately −1.5v, Q5 becomes saturated. Most of the Q5 base current flows to its collector, cutting off Q6. When the Q6 collector goes positive, D5 is forward-biased and Q3 cuts off. Then Q2 turns on provided it is not held off by a continuing positive level at R. As a result, the Q4 base becomes grounded, cutting off Q4 and initiating the discharge of the timing capacitors. Before the Q7 collector can return to its quiescent state, C7 (and any additional capacitor in parallel with it) must discharge through R13 and potentiometer R10. As C7 begins to discharge, Q5 turns off and Q6 turns on. Then D5 becomes back-biased, disconnecting R16 and R17 from the Q3 base. From this time on (although the full delay interval is not yet over), the circuit can be retriggered by a positive pulse at S or a negative input at K.

When the Q7 base becomes more negative than −4.5v, Q7 turns on and Q8 turns off. The −6v supply back-biases Q9 via R19 and turns off Q9. The rise in voltage at the Q9 collector cuts off Q10, returning the output multivibrator (Q10-Q11) to its stable state. The output returns to the 0 state (W at ground, U at −3v), indicating the end of the delay.

If the Q1 input is held at −3 vdc, C7 charges up to −1.5v and stays there. The output, therefore, remains in the 1 state. Return to the 0 state occurs at a fixed interval after removal of the negative Q1 input. When input pulses arrive at shorter intervals than the delay period, output remains in the 1 state and returns to the 0 state at a fixed interval after the last pulse.

4-3.4 Clock Type 4401

The Type 4401 Clock is briefly described in DEC System Modules Catalog, C-100. This module contains an astable multivibrator (Q1-Q2), a pulse amplifier-shaper (Q3), and an output pulse amplifier (Q4) (see reference schematic RS-B-4401-12). A Type 4401 Clock generates DEC 0.4-μsec pulses at pins E and F in any frequency from 5 cps to 500 kc. The output frequencies are divided into five overlapping ranges with provision for adjusting to any frequency within each range. Output pulse trains are inhibited by applying −3 vdc to a disconnected diode which has its anode connected to pin V.

Capacitance inserted between pins T and V determines the frequency range. An internal jumper can select any one of the five capacitors (C3 through C7) for this purpose. The range of 5 to 50 cps can be selected by jumpering pin T to pin M. Range increases by a factor of 10 can be made by connecting pin T in succession to pins R, P, N, or V respectively. Connecting an external capacitor between pins V and T can extend the frequency range of the multivibrator. When X and Y are jumpered, potentiometer R4 adjusts the frequency within the selected range. An external fine-control potentiometer may also be connected between pins Y and Z.

Diodes D1-D6 determine operating voltages of the multivibrator. A tap between D3 and D4 holds the Q1 base at −2.25 vdc; a tap between D4 and D6 provides −3-vdc collector supply for Q1 and Q2. Because the Q1 operating point can be varied over a wide range by R4, a dual collector load is provided for Q1. R3 is the principal load for low operating current. At higher currents, D5 conducts and the load is shared by R2.

The rate at which Q1 and Q2 alternate is a function of the RC time constant of the frequency-determining capacitor (one of C3-C7) and the series combination of R1 and R4. An output pulse is generated at Q2 turnoff during each cycle of the multivibrator. Assume that Q1 is turning off and Q2 is turning on. The Q2 emitter voltage follows the negative-going voltage at the Q1 collector, and C3 (if T is jumpered to M) couples the negative transient to the Q1 emitter. This feedback rapidly triggers the

multivibrator to its first state of Q1 off and Q2 on. The positive pulse generated by the T1 secondary is applied to the Q3 base and serves to drive Q3 further into cutoff. Therefore, the output pulse amplifier is not affected.

The multivibrator remains in the state of Q1 off and Q2 on while C3 charges through R4, R1, Q2, and the T1 primary. This charging pulls the Q1 emitter toward ground. When the emitter voltage becomes more positive than −2.25v (Q1 base potential), the transistor turns on; and the Q1 collector-emitter feedback triggers the multivibrator to its second state of Q1 on and Q2 off. Note that if V is held at −3 vdc, Q1 cannot turn on. Turnoff of primary current in T1 generates a negative pulse at T1-3. This pulse saturates Q3, grounding T2-2 and turning on Q4 with a negative pulse at the base. The output-pulse amplifier (Q4) generates a DEC standard 0.4-μsec pulse across E and F. This pulse is positive at F if E is grounded, negative at E if F is grounded. C8 flattens the top of the output pulse by maintaining the high rate of change of the T3-primary current for a longer time. R8 and D7 serve to dampen the overshoot of the T3 primary. The multivibrator remains in the second state while C3 discharges through R5, Q1, and the Q1 collector load. When the discharge current decreases to about 6 ma, the Q2 emitter becomes more positive than its base. Then Q2 begins to turn on and Q1 to turn off, thus starting a new cycle.

4-3.5 Mark Track Decoder Type 4260

As shown in replacement schematic RS-D-4260-1, the Mark Track Decoder Type 4260 contains a pulse inverter (Q1), a 9-bit register (Q2-A17 and Q20-Q21), two pulse amplifiers (Q18-Q19 and Q22-Q23), and nine decoders (Q24-Q33). The circuit is shown in the logic diagram at the upper left of engineering drawing BS-3 in Chapter 6. In this drawing the flip-flops are numbered W1-W9 in order of decreasing significance. In RS-D-4260-1, flip-flops W9-W2, respectively, are shown at the top of the schematic, starting at the left with flip-flop Q2-Q3. The most significant flip-flop W1 contains transistors Q20 and Q21, and is shown at the lower left of the schematic. Pulse amplifiers for the shift and clear inputs are Q18-Q19 and Q22-Q23 at the extreme lower left of the schematic.

The ground-asserted 1 input at pin M represents information to be shifted into W9 (see BS-3). A negative shift input is applied at pin J, and the entire register may be cleared by a negative pulse or negative-going level change at pin H. The 1 and 0 outputs of W1 (Q20-Q21) are available at pins L and K; the W2 (Q16-Q17) outputs at pins P and E. These are the only register outputs available at external pins.

Operation of the shift-pulse amplifier (Q18-Q19) and the clear-pulse amplifier (Q22-Q23) is identical. A negative input pulse saturates the right transistor (e.g., Q19), generating base current for the emitter follower (e.g., Q18). The Q18 emitter rises to ground, providing a low-impedance positive-going level transition for the shift bus. When the input pulse terminates, the Q18 emitter falls to −3v

and is held at the level by clamp diode D142. The shift bus is connected to shift information conventionally through the eight flip-flops at the top of RS-D-4260-1, but can shift only a 1 into W1 (Q20-Q21). All shift gates at the flip-flops are conventional C-D gates for positive pulses similar to those described for Figure 4-4. Transistor Q22 drives the clear bus through C3. This bus is connected to turn off the left transistor in all flip-flops through isolating diodes, e.g., D33.

The outputs for the decoders (Q24-Q23) are explained in Table 4-1 and are shown in both BS-3 and RS-D-4260-1. The decoder transistors are driven by a large 2-stage diode AND network in the center of RS-D-4260-1. Each section of the network is a standard AND gate for negative-levels similar to the one described for Figure 4-3(a). The clamped returns (e.g., R7-D133) for all sections and level-shifting pairs of silicon diodes (e.g., D112-D123) are shown in the replacement schematic. The output at pin W is at ground level only when Q31 and Q33 are both conducting. Q31 conducts when window bits W4-W9 contain octal 73; Q33 conducts when W2 and W3 contain octal 0 or 3. Pin W, therefore, is at ground level for window contents 073 or 373. All other decoder outputs are asserted by single inverters.

TABLE 4-1 DECODER OUTPUTS FOR MARK TRACK DECODER TYPE 4260

Output Pin	Window Contents	Mark	Output Logic Signal
R	X25	-E, E	Not used
S	232	-G	Not used
T	145	-M	Not used
U	222	END	W END
V	351	G	Test point
W	073 V 373	P, F, C, -L	W BLK END
X	010 V 210	L, -C, -F, -P	W BLK START
Y	070	DATA	W DATA
Z	126	M	W BLK MK

Notes:

a. Output pins are shown on replacement schematic RS-D-4260-1 and engineering drawing BS-D-552-0-3 (BS-3) in Chapter 6.

b. Three numerals in the second column indicate the octal contents of the window (W) which cause assertion of corresponding output. The letter X in any numeral represents any number from 0-3.

c. The third column lists the mark-channel position corresponding to the output.

d. The fourth column lists the logic signals (BS-3) generated in the output of the Type 552 DECtape Control.

4-3.6 Manchester Reader and Writer Type 4523

This module (see RS-C-4523-7) contains two input gating-level inverters (Q3,Q4), several C-D gates, a flip-flop (Q1-Q2), a write amplifier (Q5-Q8), and a read amplifier (Q9-Q18). A logic diagram of the Type 4523 Reader and Writer is shown in engineering drawing BS-D-552-0-6 (BS-6) of Chapter 6.

The flip-flop (Q1-Q2) is one bit of the write buffer (WB) in BS-6, or of the timing-or-mark-channel write flip-flops (TMB or MKB respectively) in BS-3. Positive input-load pulses at pins F and J, and a complement input at pin H set or clear the flip-flop through standard positive C-D gates. Input enabling levels for the load pulses are connected at pins E and K. An inverter creates the opposite polarity for each input so that the load is a jam-transfer. Information at pin E governs the flip-flop for pulses at pin F; information at pin K gates the pulses at pin J.

The write amplifier, consisting of transistors Q5-Q8, is governed by flip-flop outputs whenever write-enable input at pin L is negative. When the flip-flop output is 1, the anode of D14 is negative, and R21 turns on Q6. Base current for Q8 then flows through D18, Q6, and R25. A conduction path for current through one side of the head inductor is established at pin N through R27, Q8, and diodes D15-D16, to −15v. When the write flip-flop contains 0, the anode of D10 is negative, and write-amplifier transistors Q5 and Q7 conduct. This establishes a current path (similar to the above) for the other side of the head inductor at pin M. For this operation Q6 and Q8 cut off simultaneously. The head inductance (o.110 μh) is driven through the series 68-ohm resistors R26 and R27. The time constant for current flow through the head is approximately 5.5 μsec. This interval is slightly more than the time taken by tape to travel from the center to the edge of the effective write gap. Polarization is written on tape at the edge of the gap, whereas a change in polarization (e.g., in the timing channel) is detected as it passes the center of the gap. Selection of this particular time constant ensures that changes in tape polarization always occur at precisely the same tape position and are governed by the timing-channel information.

The read amplifier includes transistors Q9-Q18. Inputs at pins S and T are connected directly to the write-amplifier outputs and to the head-inductor leads. Consequently, the read amplifier functions (although overloaded) even while writing is taking place. The read amplifier is a 3-stage difference amplifier; the first stage is Q9; the second is Q13, Q14, and Q16; and the third is Q11, Q12, Q17, and Q18. The first two stages are biased by current sinks Q10 and Q15. Q10 draws a constant current of a little less than 1 ma from the emitters of Q9; Q15 draws constant-current bias from the emitters of Q14 and the collectors of Q13 and Q16. This bias current for the second stage is adjustable by varying R2, which controls the operating point of the second stage by controlling the total current through the resistance (R1, R8, R9, R11, and R16) network at the Q14 collectors. Overload protection for the circuit is provided by three pairs of paralleled diodes connected back-to-back; namely, D17-D19 at the bases of Q9, D20-D21 at the bases of Q14, and D26-D27 at the bases of Q12 and Q17.

An input signal causes higher conduction in one side of Q9 and a lower conduction in the other side. The resulting differential across R31-R33 is coupled to the bases of Q14 through C3-C4. Then Q14 establishes assymetrical conduction which directly drives emitter followers Q13-Q16. Diodes D23-D24 and D28-D29 couple the emitter followers to the Q12-Q17 bases of the third stage. The third stage collectors directly drive conventional inverters Q11 and Q18. The inverter outputs provide standard DEC ground and −3v logic levels at Y and Z, according to the polarity of the input signal. When input S is positive, Y is ground and Z is negative; when input T is positive, the output polarities are reversed. RC networks R40-C10 and R39-C9 provide positive feedback from outputs Y and Z to inputs S and T. The feedback has a time constant of approximately 0.3 μsec, and is effective at the input for approximately 10 μsec. Feedback is approximately 1 mv peak-to-peak at the input, superimposed on the read signal of approximately 5 mv peak-to-peak. In the absence of signal input, this feedback causes the amplifier to oscillate. For normal connections, feedback prevents noise superimposed on a legitimate read signal from affecting the state of the amplifier outputs after they have responded to a differential input. The amplifier is sensitive to a differential input of 20 μv.

CHAPTER 5
MAINTENANCE

5-1 INTRODUCTION

The maintenance procedures in this section are based on the assumption that the reader is familiar with the operation of the Type 552 DECtape Control as described in the preceding chapters.

Maintenance activities servicing the Type 552 DECtape Control require use of the equipment listed in Table 5-1 (or the equivalent) as well as standard hand tools, cleansers, test cables, and probes.

TABLE 5-1 RECOMMENDED MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Model
Potentiometric dc voltmeter	John Fluke	801 H(0.025%)
Multimeter	Triplett or Simpson	630-MA or 260
Oscilloscope	Tektronix	Series 540 or 580, with Type CA Differential Amplifier
System module extender*	DEC	1954
System module puller*	DEC	1960
Filter Kote (aerosol spray)	Research Products Corp., Madison, Wisconsin	Order by name
Attenuator modules (2 required)	DEC	Type 1033 (See RS-B-1033-1)
Small thin-bladed screwdriver	Any quality brand	
Phillips-head screwdriver	Any quality brand	All four standard sizes

*One supplied with Type 552 DECtape Control.

5-2 WIRING

5-2.1 Interface

The interface connector panel for connections between the Type 552 DECtape Control and the PDP-5/8 computer is represented in DEC drawing UML-D-552-0-18. This panel is located just above the three logic panels in the lower section of the cabinet. In DEC drawing UML-D-552-0-18 the FLIP CHIP receptacles labelled W021 accept the in/out cables from the PDP-5/8. The W021's in blocks H1 through H10 are bussed pin-for-pin to the W021's in blocks J1 through J10. Each block contains the cable designation and the type of information carried from the PDP-5/8 to the panel.

5-2.2 Module Location

The types and number of FLIP CHIP modules used in the Type 552 DECtape Control are listed in DEC drawing ML-A-552-0-15. A diagram showing the module location in each of the three mounting panels containing Type 552 logic is shown in DEC drawing UML-D-552-0-14. In this drawing, each module is represented by a rectangle with the module type designation (e.g., 4422) at the top. Each rectangle, in turn, is subdivided by dashed lines to show the number of circuits on the module. These subdivisions contain two lines of information. The top line is an abbreviation of the logic signal produced at the circuit output; the lower line is the block schematic location of the circuit in its appropriate logic diagram (see Chapter 6 for the convention indicating block locations on DEC drawings).

5-2.3 Wiring List

Detailed wiring information for all internal wiring in the Type 552 DECtape Control is in the Wiring List in DEC engineering drawing WL-B-552-0-16. This list includes signal name, wire number, pin number, and color code. A general wiring sheet for the 50-pin Amphenol plugs to FLIP CHIP 2N in/out bus and data-break connection) is in DEC engineering drawing WS-A-552-0-19.

5-3 MODULE HANDLING

The type and number of DEC modules used in the Type 552 DECtape Control System are listed in DEC engineering drawing ML-A-552-0-15. Information on the removal and replacement of these modules from the Type 552 equipment is given in the following subparagraphs.

5-3.1 Module Removal

When necessary to remove modules, a Type 1960 System Module Puller should be used as follows:

a. Turn off all power to the DECtape control.

b. Carefully hook the small flange of the module puller over the center of the module rim.

c. Gently pull the module from the mounting panel. Use a straight even pull to avoid damage to plug connections and the printed-wiring board. Since the puller is not secured to the module, grasp the module rim to prevent dropping.

Signal tracing can be performed by replacing the module with a Type 1954 Module Extender and then plugging the module into the extender.

5-3.2 Module Replacement

When the DECtape control modules listed below require replacement, the replacement module must be connected by jumpers on the circuit board to conform with the logic requirements. The proper jumper connections are made as follows:

Type 4222 - Six of seven flip-flops located on this flip-flop counter have jumper-selected 1 or 0 outputs available at the module connector. Jumper the 1 outputs with 100-ohm, 1/4w resistors to pins J, L, N, R, T, and V.

Type 4151R in 2K05 - This binary-to-octal decoder includes jumper-selected clamped loads for the decoder outputs, and a ground jumper between P and D for enabling the entire module. Since the module is to be enabled by external logic at P, the jumper from P to ground must be clipped out.

Type 4228 - This assembler contains three bits of the data buffer (DB). Jumpers are required to select either the 1 or 0 outputs for driving an output inverter. All three 0 sides should be jumpered.

Type 4228-1 - This assembler contains a single bit of the RWB and the DB. The 0 side of the DB flip-flop must be connected to drive the output inverter in the same manner as in the Type 4228.

Type 4605 - This gated pulse amplifier produces IOT pulses which govern programmed control operations. The device address is connected to this module through jumpers to a 6-diode AND gate for negative levels. The 1 and 0 outputs of memory buffer bits 3-8, asserted negative, are connected directly from the interface plugs to pins M to Z, respectively, of this module. The 0 sides drive pins M, P, S, U, W, and Y; the 1 sides drive the alternate pins from N to Z. Jumpers on the board near the connector determine the MB-bit sides used to drive the diodes. The module is shipped with all jumpers connected. Jumpers which connect the unwanted side of an MB bit must be clipped out. For example the pulse amplifier in 2L01, which accepts address 75, should be prepared by clipping the jumpers at M, P, S, U, X, and Y. Thus, the AND gate is driven by the 1 sides of all MB bits from 3-8 (except bit 7).

Type 4227 - This set-reset flip-flop module includes eight flip-flops and two clear pulse inputs at P and R. Jumpers on flip-flops 5, 6, and 7 are used to select which of the two pulse inputs is to clear the flip-flop. All jumpers must be clipped out in the DECtape control, because neither input should affect any of the three flip-flops.

Inverters, Diodes, and Gates - The presence of a jumper is indicated by a 1 in a binary number of n bits, where n is the number of clamped loads in the module. Bits from left to right correspond to the alphabetical order of the circuit outputs at the connector. The number is written in octal as a suffix to the type number on the utilization module list (see DEC engineering drawing B-552-0-14). For example, the Type 6102 in 2L15 has the suffix 061 or binary 00 110 001. Thus the clamped-load jumpers at outputs F, J, L, T, V, and X are clipped out. The jumpers remaining at N, R, and Z correspond to the 1's in the above binary number. An R in place of a number indicates that all clamped loads are connected.

5-4 PREVENTIVE MAINTENANCE

Preventive maintenance tasks consist of visual inspections, cleaning, mechanical checks, and checks of specific circuit elements. A log book should be made available for recording pertinent information noticed during the various tasks. The recommended schedule for preventive maintenance includes the following:

a. Daily

Clean tape handling surfaces using Freon and a soft cloth.

Clean dust from inside the cabinet.

b. Weekly

Conduct a test program (DECtog 8 or the DEC-8-33-U maintenance routine) to exercise all transports and control logic in all modes.

c. Every 300 Hours

Inspect tape guides to ensure that tape is not rubbing against guides.

Check each spool during its use as a takeup spool to ensure tape is wound evenly.

Check pin-loaded pins on all hubs to ensure proper operation.

d. Every 1000 Hours (or every six months, whichever first)

Perform mechanical checks and indicated corrective actions outlined in the PDP-5 Maintenance Manual, page 9-5, or the PDP-8 Maintenance Manual, page 9-7. Then perform all the following check/adjustment procedures.

5-4.1 Type 728 Power Supply Check

Check the output voltage and ripple content of the Type 728 Power Supply (see RS-728-5) and ensure that it is within tolerance. Use a multimeter to make the output voltage measurements without disconnecting the load. Use the oscilloscope to measure the peak-to-peak ripple content on the dc-supply outputs. This power supply is not adjustable; hence, if the output voltage or ripple content is not within the tolerance specified, the supply should be considered defective and troubleshooting procedures should be undertaken. When used with the PDP-8, be sure to check both Type 728 Power Supplies in the Type 552 DECtape Control. Acceptable voltage and ripple tolerances are as follows:

Outputs	Color Code	Tolerance
+10v output	black (-) and red (+)	9.5 - 11v; ripple <800 mv p-p
-15v output	black (+) and blue (-)	14.5 - 16v; ripple <400 mv p-p

5-4.2 Type 4303 Delay Check

A DECtape flag (requesting a program interrupt) occurs approximately every 225 msec during this check procedure. If desired, a small subroutine may be deposited to clear the DECtape flags on each interrupt. Otherwise the computer may be turned off and the Type 552 DECtape Control switched to LOCAL. Proceed as follows:

a. Connect a jumper between pins W and S on the module located at 2L13, i.e., 13th module from the left in mounting panel L.

b. Connect the oscilloscope to terminal 2L13W, i.e., pin W of same module. A correct indication is a short positive pulse every 180 msec, superimposed on a −3v ambient.

If the indication is incorrect, turn the adjustment screw (accessible through a hole in the handle of the Type 4303 Delay) to obtain the specified pulse-repetition rate.

c. Remove the jumper at 2L13.

5-4.3 Type 4306 Delay Check

This adjustment procedure must be carried out for each of the three delays in each of the two delay check modules. Normally, the delay has a range between 0 and 10 μsec; but external capacitors may be added at pins J-H, R-P, and X-W to lengthen the delay. As shown in engineering drawing

BS-8:D3, the module at 2L14 contains three 6.8-μsec capacitors. Refer to previous subparagraph "Module Locations" in this chapter for location of modules on engineering drawings. Proceed as follows:

a. Deposit the following program in consecutive memory locations, starting at the beginning of a page:

Page address	Instruction	Function
00	6002	IOF
01	6753	MMLS & MMLM
02	6761	MMSF
03	5202	JUMP BACK TO IOT SKIP
04	5201	JUMP BACK TO LOAD REGISTERS

Start the computer at 00 of the same page.

b. Connect the oscilloscope to terminal 2L14Z. The correct indication at this point is a −3v level of 35-msec duration followed by a ground level of same duration. If the duration of the negative level is incorrect, turn the lower adjustment screw (accessible through bottom hole in aluminum frame of module) to reset the delay.

c. Connect an oscilloscope probe to 2L14P. The correct indication is a −3v level of 35-msec duration, followed by a ground level of same duration. If the duration of the negative level is incorrect, turn the center adjustment screw to reset the delay.

d. Shift the oscilloscope probe to terminal 2L14L. The correct indication is a negative 35-msec level, followed by a ground level of same duration. If the duration of the negative level is incorrect, turn the top adjustment screw to obtain the correct delay.

e. Stop the computer and remove the probes.

f. Turn on the WRTMR maintenance switch.

g. Connect a jumper between pins X and Y of 2K11, and another jumper between terminal 2M07M and ground.

h. Using an oscilloscope, observe the indication at 2L08L. The correct indication is a 10-μsec negative level occurring every 16.6 μsec. If the duration of the negative level is incorrect, turn the upper adjustment screw of the delay module in 2L08 to achieve the correct delay.

i. Observe the level at 2L08P. The correct indication is a 4.5-μsec negative level occurring every 33 μsec. If the duration of the negative level is incorrect, turn the center adjustment screw on the same module to achieve the correct delay.

j. Connect a third jumper from 2L08V to ground, and a fourth from 2K11F to 2L08U.

k. Observe the level at 2L08Z. The correct indication is a negative level of 1 μsec or less duration, occurring every 8.3 μsec. If the duration of the negative level is incorrect, turn the bottom adjustment screw to achieve the correct delay.

l. Remove all jumpers. Leave the WRTMR switch on and proceed with the clock adjustment below.

5-4.4 Type 4401 Variable Clock Check

Proceed as follows:

a. With the WRTMR switch on, observe 2K11F with an oscilloscope. The correct indication is a 400-nsec positive pulse occurring every 8-1/3 μsec. If the duration between pulses is incorrect, turn the clock adjustment screw (available through the access hole in the aluminum frame of the module at 2K11) to achieve the correct repetition rate.

b. Remove the probes; turn off WRTMR.

5-4.5 Type 4523 Manchester Reader and Writer Check

The following procedure for checking and adjusting any of the five Type 4523's should only be performed by an experienced maintenance technician. Proceed as follows:

a. Remove the jumper plugs at locations 2K47 and 2K48, and replace them with Type 1033 Attenuator modules.

b. Deposit a test program (e.g., one of DECtog programs) which will rock the tape for periods of approximately 4 sec.

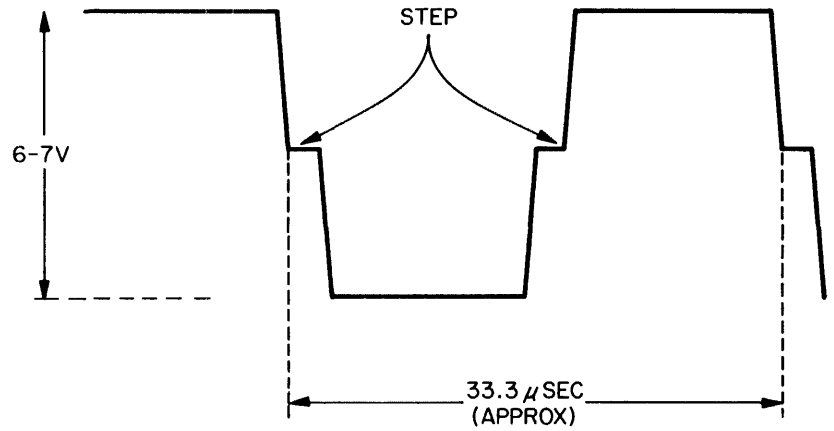
c. Test each Manchester reader and writer module using location 2K14, which normally contains the read/write module for the timing track. First, check the module in the timing track; then remove it and substitute modules from other locations (2K15-18) for the one in 2K14.

d. Turn the mode switch of the oscilloscope differential preamplifier to the position at which signals are added algebraically. Invert the polarity of one input to reject common mode signals.

e. Connect one channel of the differential preamplifier to terminal 2K14Y, the other channel to 2K14Z.

NOTE: To obtain the correct indication in step f, it may be necessary to replace one or both Type 1033 Attenuator modules with the jumper plugs in connectors 2K47 and 2K48. Vernier adjustments, however, should always be made with both Type 1033 modules installed.

f. Observe the points in step e with an oscilloscope. The correct indication is a square wave with an amplitude of 6 - 7v and a period of approximately 33.3 μsec. If the correct indication is not obtained, turn the sensitivity potentiometer (accessible through the lower hole in the aluminum frame at 2K14) in one direction until a step appears in the square wave as shown below. Turn the potentiometer in the opposite direction until the step disappears and then reappears. Determine the range of potentiometer settings for which no step appears by rocking the adjustment between the two limits which produce a step in the square wave. Permanently set the potentiometer to the center of this range. This position is the one least likely to allow the step under marginal conditions.



NOTE: The normal pulse period indicated in step g will vary with the speed of the tape. Vernier measurements and adjustments should be performed with the tape advancing in the forward direction.

g. If the correct square-wave duty cycle of 50% is not obtained, adjust the duty-cycle potentiometer (accessible through top hole in aluminum frame of module in 2K14) for correct indication. Since the sensitivity and the duty-cycle adjustments interact, this adjustment requires a repetition of steps f and g until correct indications are obtained for both steps.

h. Return any of the Type 4523 Manchester Reader and Writer modules removed during this procedure to their original locations. Leave the Type 1033 Attenuators installed for the read/write circuit checks below.

5-4.6 Read/Write Circuit Checks

Run a program which uses all read/write circuits. Parts of the Digital-8-33-U DECtape Maintenance Package contain several routines which perform write and read check operations in all channels. Directions for operation are supplied with the routines. Attenuated signals produced by installation of Type 1033 Attenuator modules will cause marginal read/write circuits to fail. When the component fails, it is often detected by the program which types appropriate error messages. Otherwise, oscilloscope signal-tracing techniques must be used to detect marginal components.

To check that the head and control signals are performing the proper functions, the diagnostic routines should be run at every tape drive connected to the DECtape control. Figure 5-1 shows normal waveforms at various test points of the Manchester reader and writer module. Voltage waveforms for write amplifier output pins M and N are shown in Figure 5-1(a). Peak-to-peak voltage is 20v, and is symmetrical with respect to ground. Current waveforms at the same pins are shown in Figure 5-1(b). The peak current should be 185 ma into the pin; the current in the opposite direction represents leakage and should be quite low. Figure 5-1(c) shows the differential read-head waveform at pins S and T.

NOTE: Replace the jumper plugs at locations 2K47 and 2K48 when finished with the checking routines.

5-5 MARGINAL CHECKS

Marginal checks are performed to aggravate borderline conditions within the logic circuits, thereby revealing observable faults. Such conditions can be corrected during corrective maintenance schedules, forestalling future failure. Marginal checks can also be used as a troubleshooting aid for locating marginal or intermittent components, e.g., faulty transistors. Checks are performed by operating the equipment logic circuits from an adjustable power source such as the DEC Type 734B Variable Power Supply (see RS-B-734B-2). This supply is installed at the top of the rear plenum door in Type 552 DECtape

systems used with the PDP-5/8. The supply panel contains a 2-position toggle switch marked -15/+10 for selecting the polarity of the power used for the check; a 0 - 20 voltmeter which presents the voltage at the panels switched to marginal power; and a control knob for adjusting the voltage.

(to be supplied)

a. Voltage at Pins M and N

(to be supplied)

b. Current at Pins M and N

(to be supplied)

c. Differential Read-Head Waveform at Pins S and T

Figure 5-1 Read/Write Waveforms of Type 4523 Manchester Reader and Writer

Raising the bias voltage above +10v is equivalent to lowering the amount of base drive on a particular inverter. This, in turn, simulates a lower gain in the transistor which drives the inverter under test. Lowering the bias voltage below +10v simulates a condition where the saturation voltage drop across the previous driving transistor has increased. This condition tends to indicate a high saturation drop in transistors which drive the logic being tested, or a high leakage in transistors within the logic being tested.

Raising or lowering the −15v supply allows checks of the collector supply voltage for the delay circuits and the pulse amplifiers. The −15v margin bus is connected only to the delay and amplifier modules. Making the collector supply of a pulse amplifier more negative results in increased pulse amplitudes and serves as a check for the proper operation of elements (e.g., flip-flops and C-D gates) driven by the pulse amplifier.

Lowering the negative power to a pulse amplifier produces lower pulse amplitudes and serves as a check for inverter and flip-flop transistor gains, and for marginal transition delay. Changing the negative voltage to delay modules allows observation of the change in the delay interval under marginal power conditions.

CAUTION

Reducing the −15v power to a value more negative than −18v will cause damage within the logic circuits.

Recordings of bias voltage levels at which circuits fail permit the plotting of progressive deterioration and the predicting of expected failure dates. Marginal checks, therefore, provide for planning periodic replacement to ensure minimum downtime.

A color-coded connector at the right side of each module mounting panel (seen from the module side) provides connections for the normal and marginal operating voltages. Power sources for all modules in a panel are selected by switches at the left end of each panel on the wiring side. These switches apply power from the marginal check bus when switched on (up); and apply normal power when switched off. The first two switches control positive power for terminals A and B of all modules in the panel; the bottom switch controls negative power for pulse amplifiers and delays. The normal and marginal power buses are common to all panels and are connected to the Types 728 and 734B Supplies (see RS-728-5 and RS-B-734B respectively) in the systems for the PDP-8. The Type 734B has no switching which guarantees normal power to panels in a polarity other than that being checked. For example, when the supply is set to +10v, the lifting of the −15v toggle switch cuts off negative power to the panel. Normal power for systems used with PDP-5 also comes from a Type 728 Supply, but marginal check power is furnished by a variable power supply mounted in the computer bay. The color coding of bus connections (at the ends of the panels on the module side) is as follows:

Green: +10v margin power bus

Red: +10v normal power bus

Black: ground

Blue: −15v normal power bus

Yellow: −15v margin power bus

CAUTION

After marginal check procedures, make certain that all marginal check on/off switches (at the left of every logic panel) are off.

5-6 CORRECTIVE MAINTENANCE

If a malfunction should occur, the condition should be analyzed and corrected by the procedure set forth in the computer maintenance manuals (PDP-5, pp. 9-24; PDP-8, pp. 9-27). The most useful tools for this purpose are the oscilloscope and the multimeter, plus a thorough understanding of the physical and electrical characteristics of the equipment.

The flow charts in Figures 3-2 and 3-4, are very useful in corrective maintenance procedures. These charts illustrate every event that occurs in any operation of the control, and all gating levels required to condition each event. The locations of the logic on DEC engineering drawings -3 through -8 are called out on the flow charts for each condition or event. When an event does not take place at the proper moment, all possible conditions leading up to its scheduled occurrence can be located on the flow charts. Then, the existence of the conditioning levels specified along flow lines can be used to trace the pulse or level-transition triggers of preceding events. All such information can be related to individual logic elements by cross references in the flow diagrams to the engineering drawings.

5-7 SPARE PARTS

For minimum system downtime, at least one spare module should be stocked for each type listed in DEC engineering drawing ML-A-552-0-15. To avoid duplication in carrying out this instruction, consideration should be given to the total module complement of the PDP-5/8 computers.

The following miscellaneous mechanical spares should be stocked in all cases where the Type 552 DECtape Control is housed only in the standard DEC bay accompanying the computer:

Quantity	Item	Part No.	Vendor
1	Toggle switch for margin power application		
1	Rotron fan	53E168, Type CFG	Rotron Mfg. Co.
1	Rotron filter	34-X1431	Rotron Mfg. Co.
1	Indicator lamp	GE327	General Electric

CHAPTER 6
ENGINEERING DRAWINGS

6-1 INTRODUCTION

This section contains reduced copies of the engineering drawings and replacement schematics (see "Pertinent Documents" Chapter 1) required for understanding and maintaining the Type 552 DECtape Control System. The engineering drawings are in addition to the complete set of full-size drawings forwarded with each Type 552. Only the full-size drawings should be used by maintenance personnel for work on the units; the full-size drawings show variations peculiar to an individual installation. Replacement schematics are furnished only for test and maintenance purposes. These circuits are proprietary in nature and should be treated accordingly.

6-2 CIRCUIT SYMBOLS

Block schematics of DEC equipment are multipurpose drawings that combine signal flow, logical function, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using special symbols that define the circuit operation. These symbols are similar to those appearing in the FLIP CHIP Modules Catalog but are often simplified. Figure 6-1 illustrates some of the symbols used in the DEC engineering drawings for the Type 552 DECtape Control.

6-2.1 Logic Signal Symbols

DEC standard logic signal symbols are shown at the input of most circuits to specify the enabling conditions required to produce a desired output. These symbols represent either standard DEC logic levels or standard FLIP CHIP pulses.

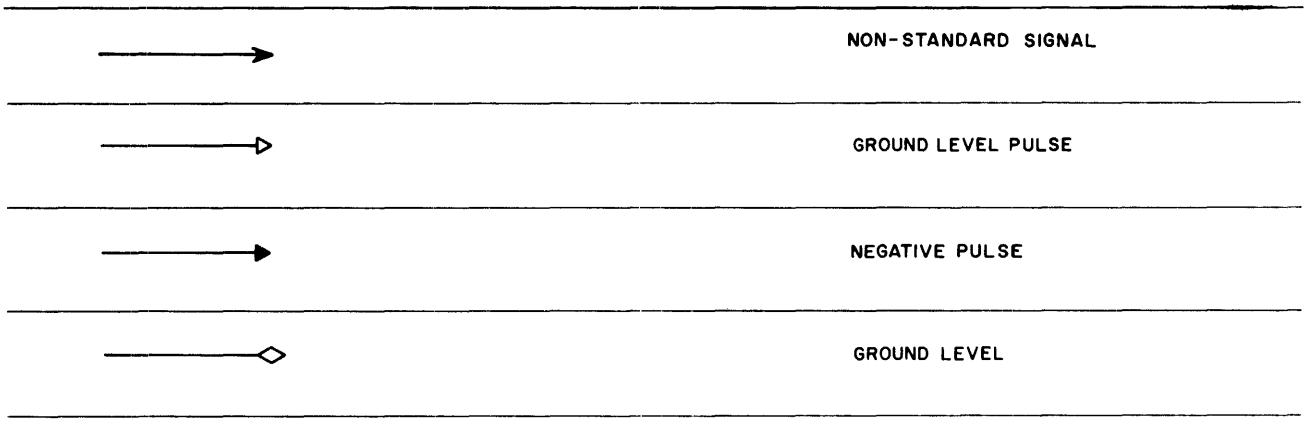


Figure 6-1 DEC Symbols

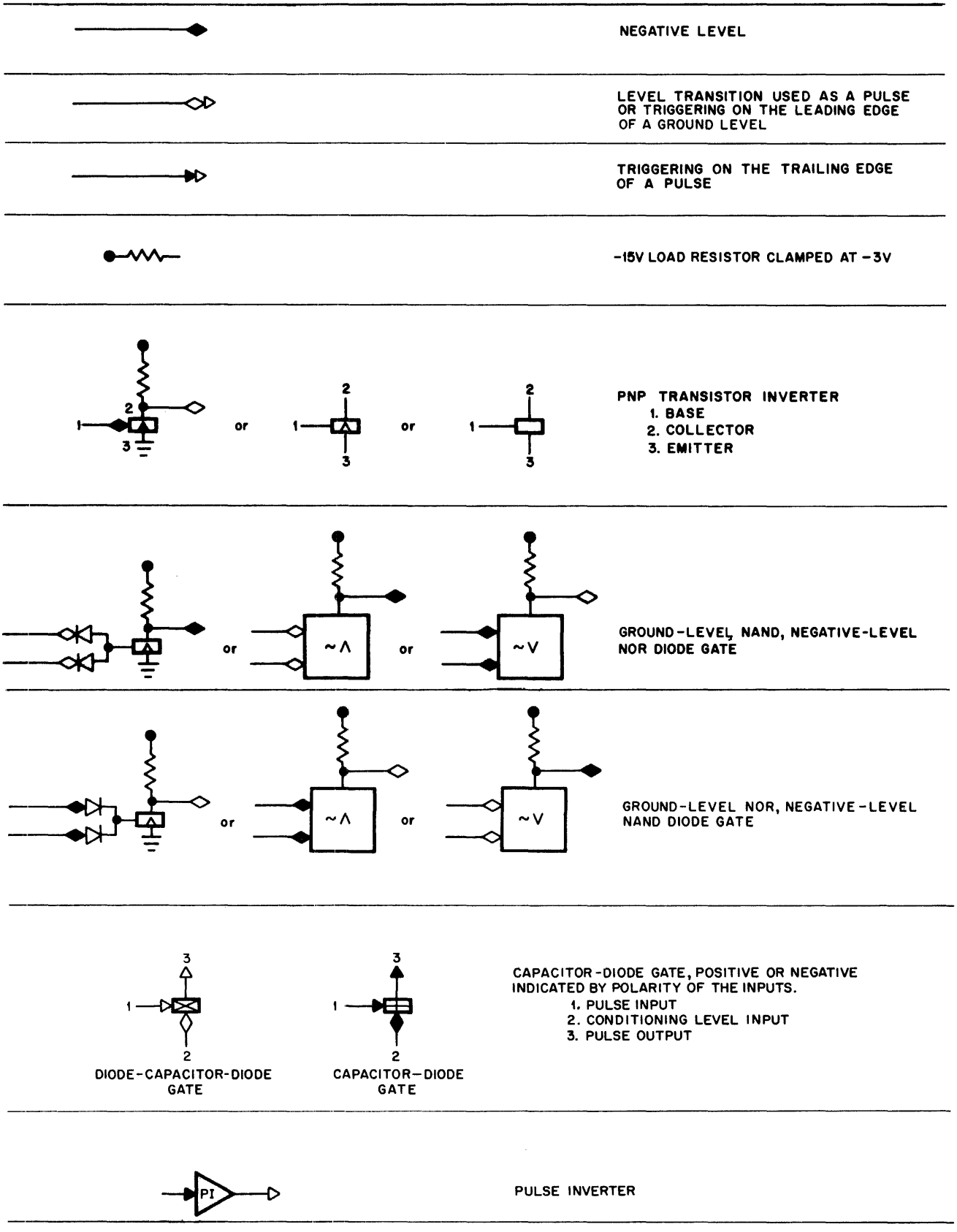
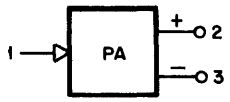
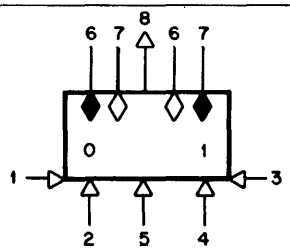


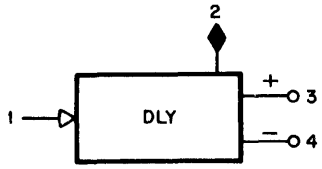
Figure 6-1 DEC Symbols (continued)



PULSE AMPLIFIER
1. PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL
2,3. TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):
1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. COMPLEMENT INPUT
6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1
8. CARRY PULSE OUTPUT, UPON BEING CLEARED



DELAY (ONE-SHOT MULTIVIBRATOR)
1. INPUT PULSE
2. OUTPUT LEVEL, -3V DURING DELAY
3,4. TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED

$\wedge$	Logical AND
V	Logical OR
superscript 1 or 0	Denotes condition for assertion, e.g., $WREN^1$ is asserted when the write-enable flip-flop is set.
subscript numerals	Denote particular register flip-flops in sequence from greater to lesser significance; e.g., DB_0 and DB_{11}, respectively, are the most and least significant bits of the data buffer. DB_0^1 is 1 output of most significant data buffer bit.
overbar (e.g., $\overline{RELTM}$)	Negation of signal level (but not when derived from flip-flop; e.g., negation of $WREN^1$ is $WREN^0$).
(⟶)	Transfer of 1's. Sets all destination register bits that correspond to source register bits containing 1.
(⟶J⟶)	Jam transfer. Sets or clears destination register bits to make the contents equal to the source register contents.
(⟷J⟶)	Jam-exchange. A 2-way transfer. Each register is made equal to the prior contents of the other.

Figure 6-1 DEC Symbols (continued)

∀	A pulse that complements the destination register bits corresponding to source bits containing 0.
0 ⟶ (device symbol)	All bits of the designated device are cleared.
1 ⟶ (device symbol)	All bits of the designated device are set.
C ⟶ (device symbol)	All bits of the designated device are complemented.
(device symbol) ⟶	Events occur only when device (e.g., memory counter) is cleared from some other state. If the memory counter is already 0, clear pulses have no effect on subsidiary flow.

Figure 6-1 DEC Symbols (continued)

6-2.2 Logic Levels

The standard DEC logic level is either at ground (0 to −0.3v) or at −3v (−2.5 to −3.5v). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (⟶◇) indicates that the signal is a DEC logic level and that ground represents assertion; a solid diamond (⟶◆) indicates that the signal is a DEC logic level and that −3v represents assertion. All logic signals applied to the conditioning level inputs of diode-capacitor-diode gates must be present for a minimum of 400 nsec before an input pulse will trigger operation of the gate.

6-2.3 FLIP CHIP Pulses

FLIP CHIP circuit operation uses two types of pulses, R series and B series. The pulse produced by R-series modules starts at −3v, goes to ground (−0.2v) for 100 nsec, then returns to −3v. This pulse is shown in Figure 6-2.

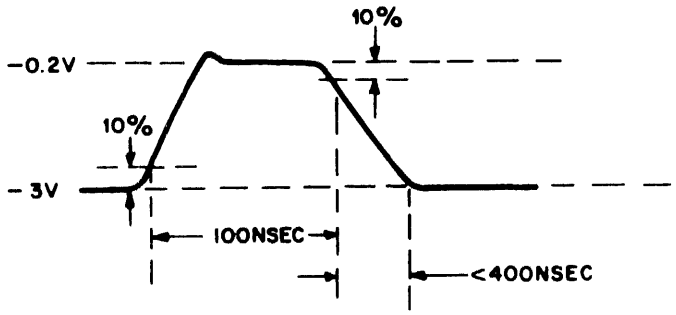


Figure 6-2 FLIP CHIP R-Series Pulse

The B-series negative pulse is 2.5v in amplitude and 40 nsec in width as shown in Figure 6-3. If this pulse is applied to the base of an inverter, the inverter output will be a narrow pulse, similar in shape to the R-series standard pulse. The B-series positive pulse, which goes from ground to +2.5v, is the inverse of the B-series negative pulse.

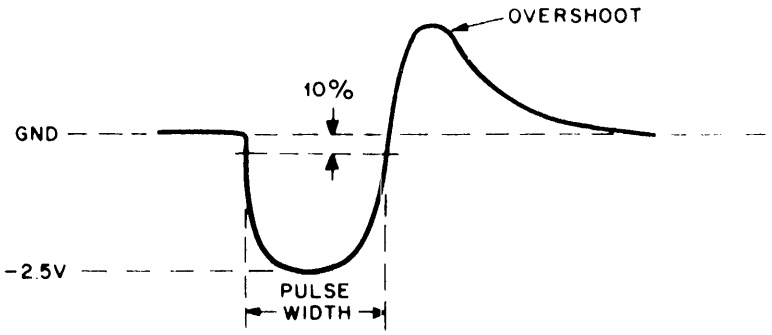


Figure 6-3 FLIP CHIP B-Series Pulse

6-3 DEC ENGINEERING DRAWING CONVENTIONS

DEC engineering drawings are subdivided into zones bounded by horizontal sections A-D and vertical sections 1-8. Circuit locations are referenced by a letter-numeral combination prefixed by the drawing number. For example, 3:A8 refers to the logic shown on drawing BS-D-552-0-3 zone A8. The source or destination of a signal is also called out by zone; e.g., STOP B3 is a STOP signal developed or applied to logic in zone B3.

Engineering drawing circuits are labelled by two 4-character designations. The upper 4-digit number specifies the module type of circuit as listed in the DEC System Modules Catalog, C-100. The first numeral in the lower 4-character designation is the number of the bay which contains the equipment. For Type 552 DECtape equipment this number is always 2. The second character is a letter which indicates the mounting panel. The third and fourth characters are numerals indicating the module location from left to right within the specified panel. Individual module pins are labelled from top to bottom by the letters A-Z (excluding G, I, O, and Q). Pin letters on logic diagrams are written near their respective terminals. On flow charts and timing diagrams, pin designations are formed by adding the pin letter to the module location code; e.g., 2M10H indicates pin H of module 10 in panel M of bay 2.

6-4 REPLACEMENT SCHEMATICS

Drawing numbers for replacement schematics are formed by a letter-numeral combination as follows: RS-(letter) - (3 or 4 numerals). The letter indicates the drawing size and the numerals indicate

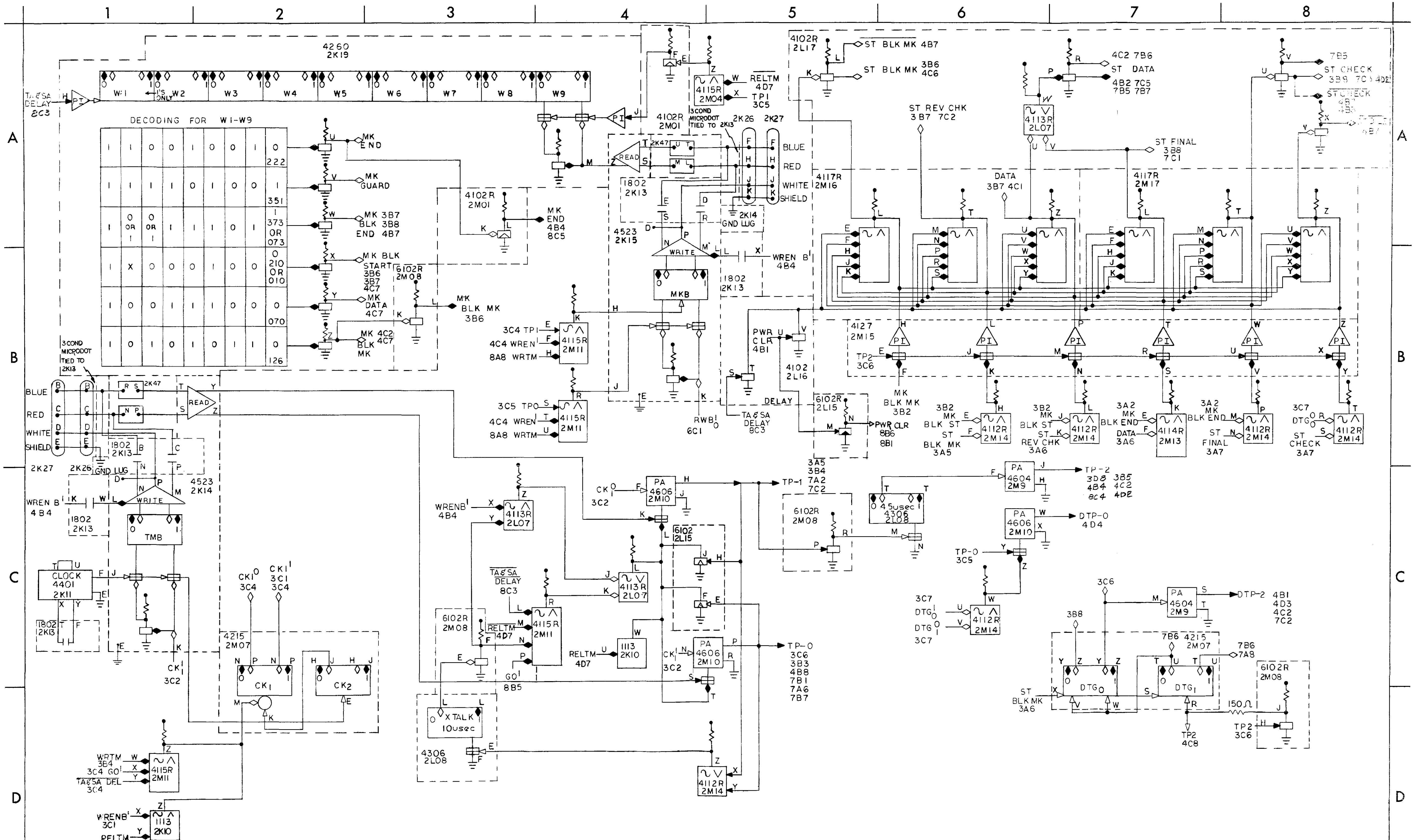
the circuit type. Another numeral to the right of these numerals indicates the number of the revision, and a letter to the left indicates the circuit-board revision. This revision letter is etched on the circuit board and embossed after the type numbers on the aluminum frame of the module.

6-5 SEMICONDUCTOR SUBSTITUTION

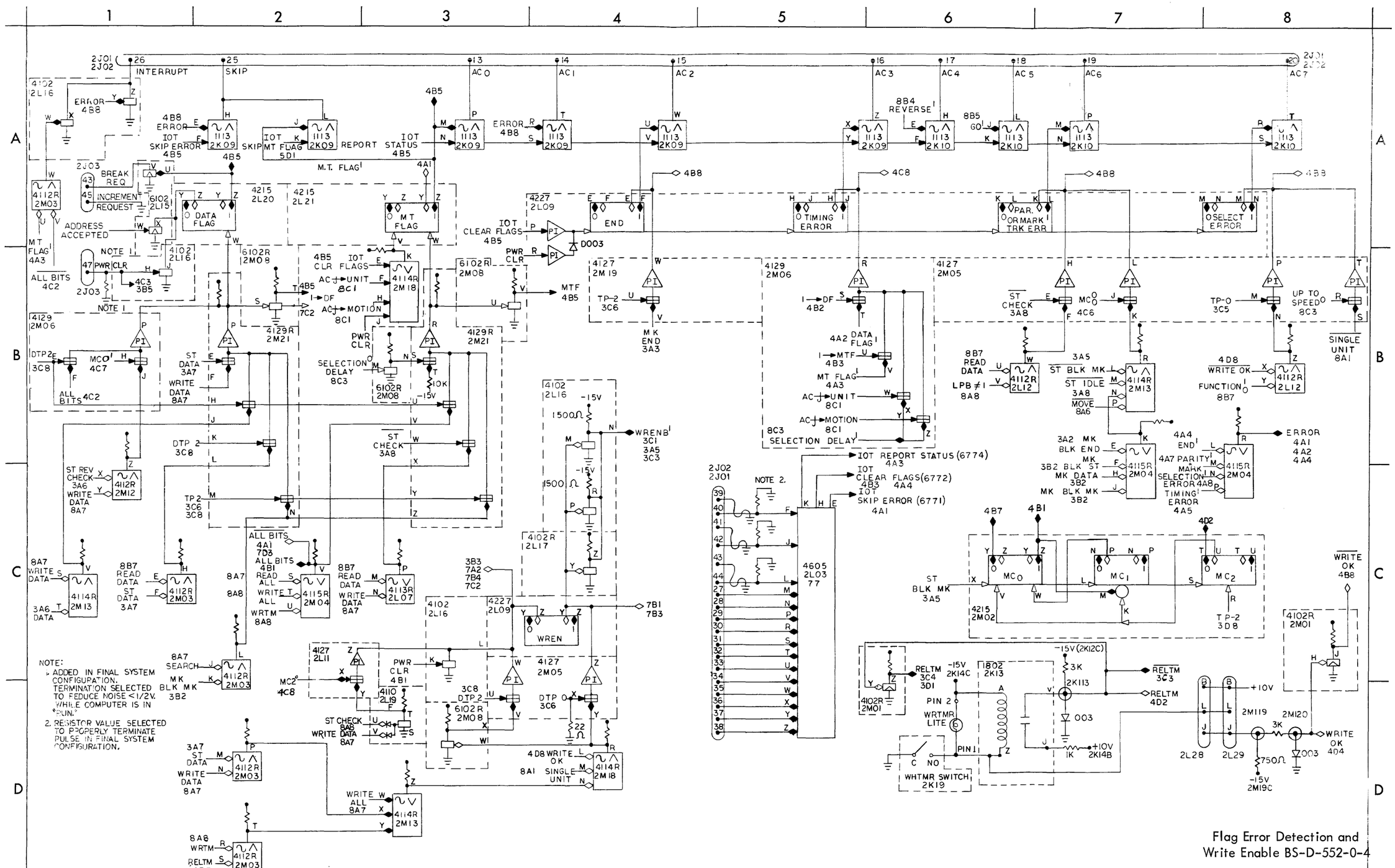
Standard EIA components specified in Table 6-1 can replace the majority of DEC semiconductions used in modules of the Type 552 DECtape Control, and shown on the RS drawings for the control. Exact replacement is recommended for semiconductors not listed.

TABLE 6-1 SEMICONDUCTOR SUBSTITUTION

DEC	EIA	DEC	EIA
D-001	1N276	DEC 1754	2N1499A (or 2N1754)
D-003	1N994	DEC 2894-1	2N2894
D-007	1N277	DEC 2894-4	DEC 2894
D-662	1N645	DEC 3009	2N3009
D-664	1N914 (or 1N3606)	MD94	2N2488
D-668	Two 1N3606 in Series	4JX1C741	2N527

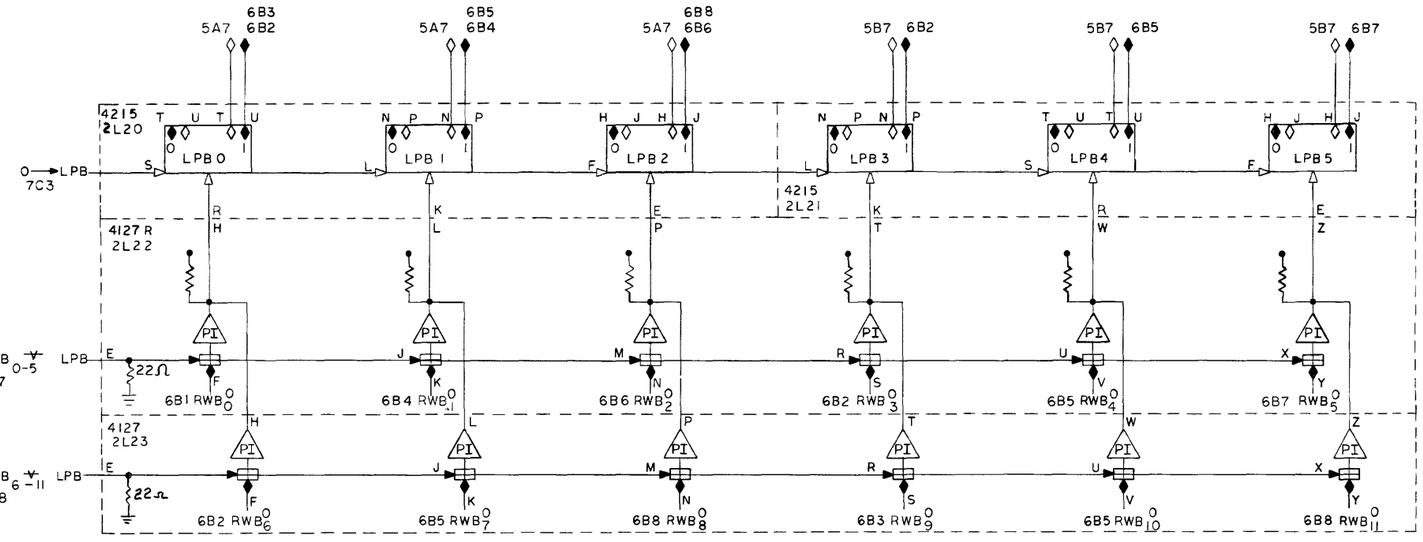


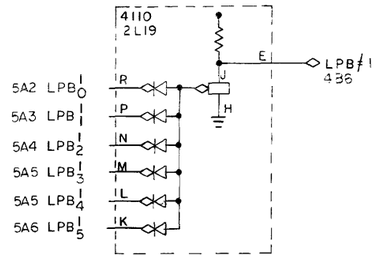
Status Timing and Mark Track Decoding BS-D-552-0-3

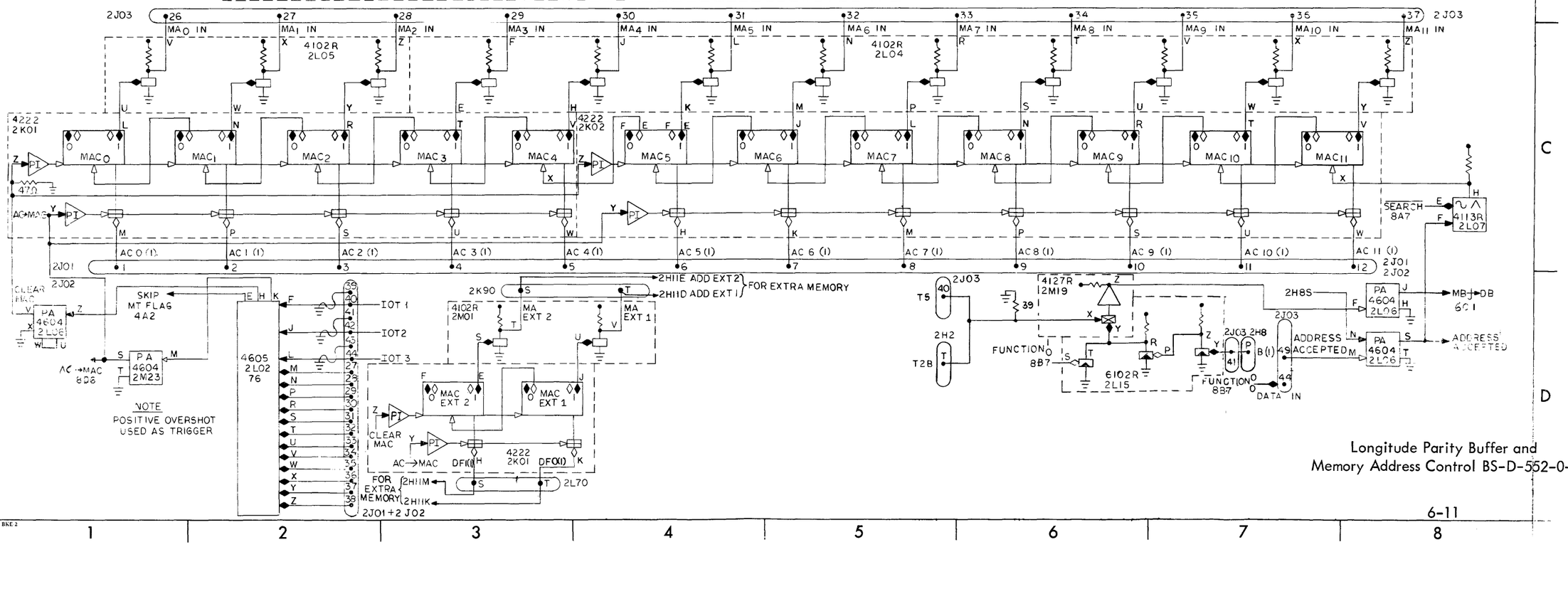


Flag Error Detection and
Write Enable BS-D-552-0-4

BKE-2

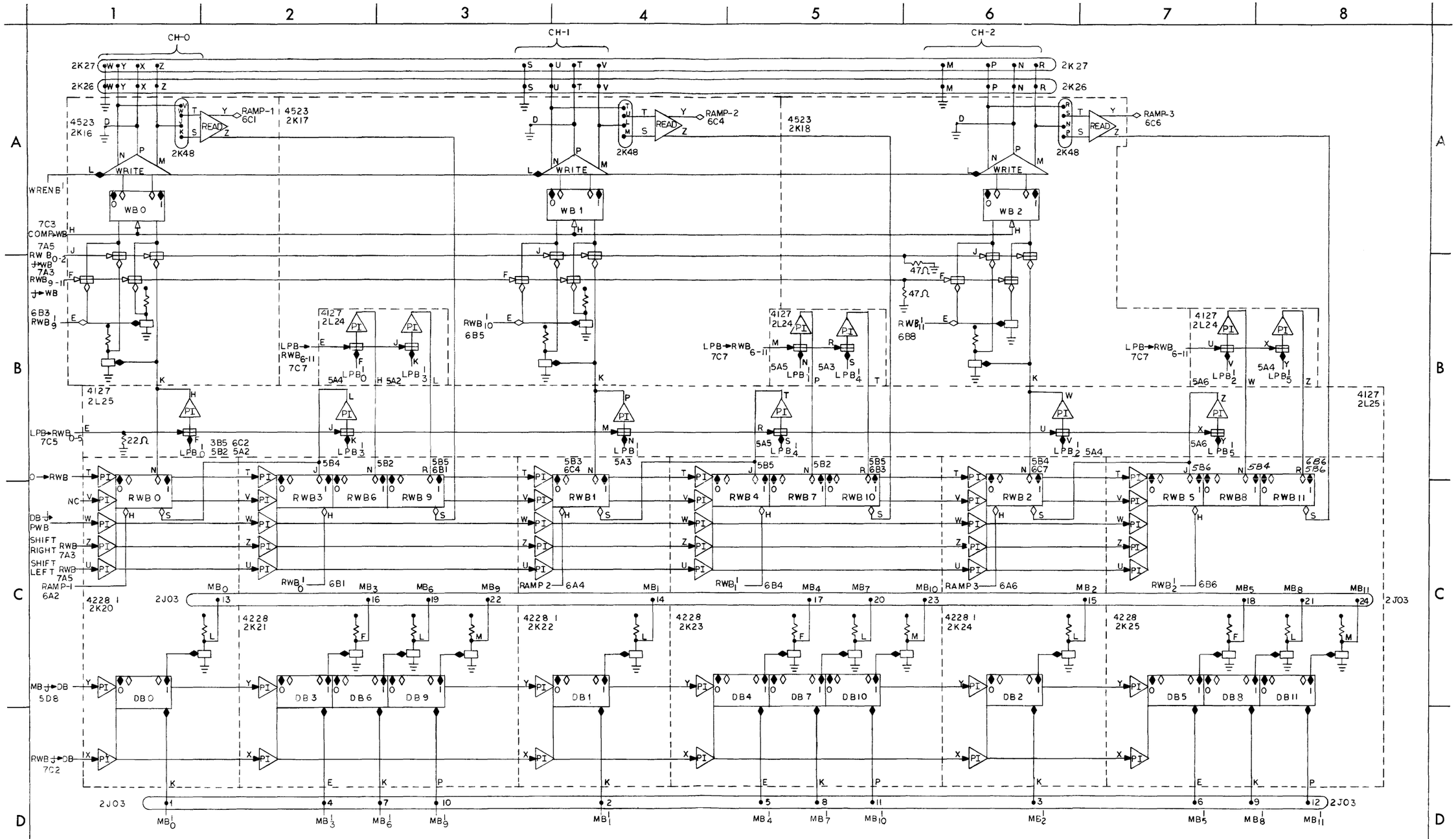






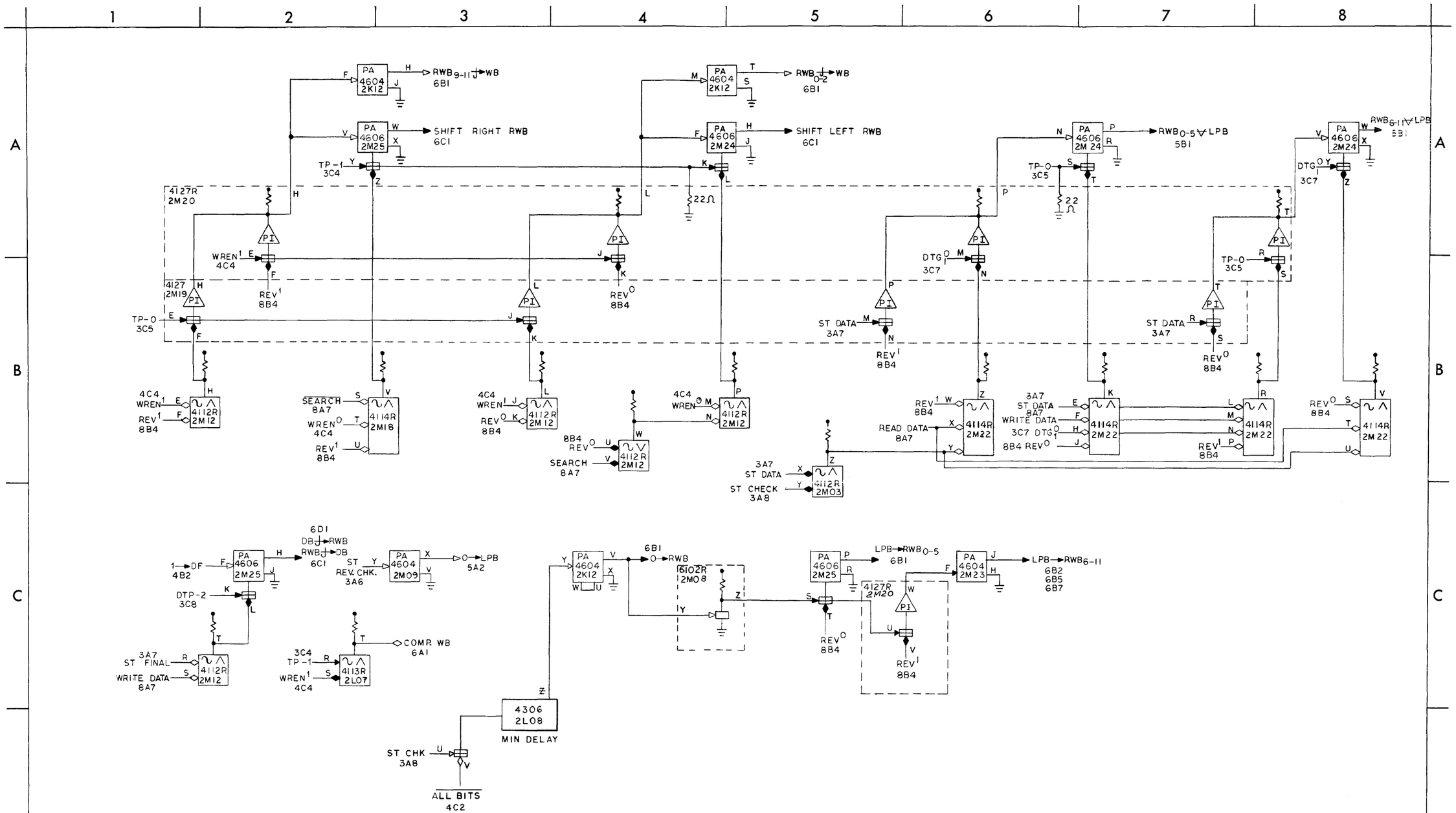
Longitude Parity Buffer and
Memory Address Control BS-D-552-0-5

BKE 2



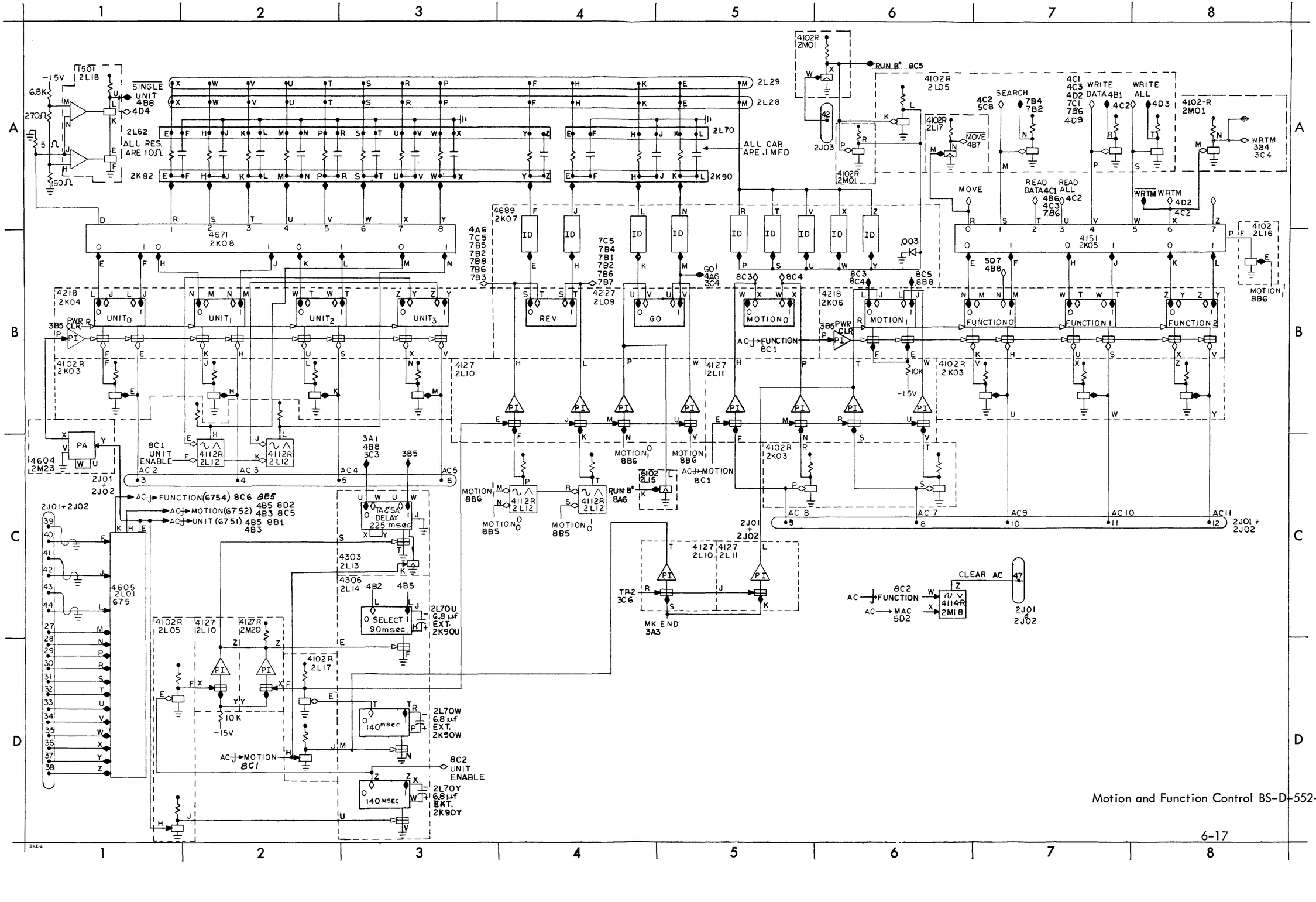
NOTE:
CHECK FOR PROPER JUMPERS ON THE 4228 OUTPUTS

Read/Write Buffer, Data Buffer and Read/Write Amplifiers BS-D-552-0-6



RWB, DB, and WB Controls BS-D-552-0-7

BKE-2



Motion and Function Control BS-D-552-0-8

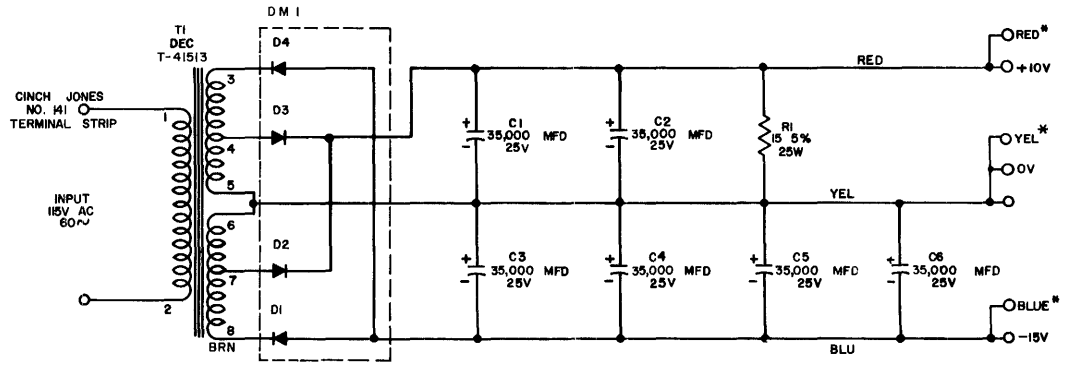
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	4222[1]	4222[1]	4102R	4218	4151R[3]	4218	4689	4671	1113	1113	4401	4604[6]	1802	4523	4523	4523	4523	4523	4260	4228-1[2]	4228[2]	4228-1[2]	4228[2]	4228-1[2]	4228[2]
2K	MAC EXT 2 D-5-D3	MAC 5 D-5-C4	CLR. UNIT 0 D-8-B1	UNIT 0	MOVE D-8-A7	MOTION 1	REV D-8-A4	SINGLE UNIT D-8-A1	SKIP D-4-A2	AC4 D-4-A6		RWB 9-11 → WB	READ	WRITE READ	WRITE READ	WRITE READ	WRITE READ	WRITE READ	W1 D-3-A1		DB3 D-6-C2		DB4 D-6-C5		DB5 D-6-C7
	MAC EXT 1 D-5-D3	MAC 6 D-5-C4	CLR. UNIT 1 D-8-B2	D-8-B1	SEARCH D-8-A7	D-8-B6	REV D-8-A4	SELECT 1 D-8-A1	SKIP D-4-A2	AC5 D-4-A6		D-7-A3	D-3-C1 READ						W2 D-3-A1	DB0 D-6-C1	DB6 D-6-C2	DB1 D-6-C3	DB7 D-6-C5	DB2 D-6-C6	DB6 D-6-C7
	MAC 0 D-5-C1	MAC 7 D-5-C5	CLR. UNIT 2 D-8-B2	UNIT 1	READ DATA D-8-A7	FUNCTION 0	GO D-8-A4	SELECT 2 D-8-A2	ACO D-4-A3	AC6 D-4-A7		RWB 0-2 → WB	D-3-A4 CLOCK D-3-C1						W3 D-3-A2						
	MAC 1 D-5-C2	MAC 8 D-5-C6	CLR. UNIT 3 D-8-B3	D-8-B2	READ ALL D-8-A7	D-8-B6	GO D-8-A4	SELECT 3 D-8-A2	AC1 D-4-A4	AC7 D-4-A8	CLOCK	D-7-A5	REL TM D-4-D6						W4 D-3-A2		DB9 D-6-C2		DB10 D-6-C5		DB11 D-6-C7
	MAC 2 D-5-C3	MAC 9 D-5-C6	MOTION 0 D-8-B5	UNIT 2	WRITE DATA D-8-A7	FUNCTION 1	RUN D-8-A5	SELECT 4 D-8-A2	AC2 D-4-A4	RELTM D-3-C4		0 → RWB	WREN B1 D-3-C1						W5 D-3-A2		RWB3 D-6-B2		RWB4 D-6-C5		RWB5 D-6-C7
	MAC 3 D-5-C3	MAC 10 D-5-C6	MOTION 1 D-8-B6	D-8-B2	WRITE ALL D-8-A7	D-8-B7	RUN D-8-A5	SELECT 5 D-8-A2	AC3 D-4-A6	WREN B + RELTM D-3-D1		D-7-4C	WREN B1 D-3-B5						W6 D-3-A3	RWB0 D-6-B1	RWB6 D-6-B2	RWB1 D-6-B4	RWB7 D-6-C5	RWB2 D-6-C6	RWB6 D-6-C7
	MAC 4 D-5-C3	MAC 11 D-5-C7	CLR. FUNCTION 0 D-8-B7	UNIT 3	WRT M D-8-A7	FUNCTION 2	RUN D-8-A6	SELECT 6 D-8-A3											W7 D-3-A3		RWB9 D-6-B2		RWB10 D-6-C5		RWB11 D-6-C7
			CLR. FUNCTION 1 D-8-B7				RUN D-8-A6	SELECT 7 D-8-A3											W8 D-3-A3						
			CLR. FUNCTION 2 D-8-B7	D-8-B3		D-8-B8		SELECT 8 D-8-A3											W9 D-3-A4						
	4605[6]-75	4605[6]-76	4605[6]-77	4102R	4102R	4604[6]	4113R	4306	4227X[5,7]	4127	4127	4112R	4303	4306	6102-061	4102	4102R	1501	4110	4215[4]-2	4215[4]-2	4127R	4127	4127	4127
	AC → UNIT	SKIP MT FLAG	IOT SKIP ERROR	MA3 D-5-C3 MA4 D-5-C4 MA5 D-5-C4 MA6 D-5-C5 MA7 D-5-C5 MA8 D-5-C6 MA9 D-5-C6 MA10 D-5-C7 MA11 D-5-C7	SET SELECT D-8-D2 UNIT ENABLE D-8-D2 RUN D-8-A6 SEARCH D-8-A7 WRITE DATA D-8-A7 WRITE ALL D-8-A8 MA0 D-5-C2 MA1 D-5-C2 MA2 D-5-C2	MB → DB	COMP. MAC11 TP-1 1 → MFT D-4-C3 COMP. WB D-7-3C DATA + ST. FINAL D-3-A7 TP-1 D-3-C3	TALK TP-2 D-3-D3 D-3-C6	END D-4-A4 TIMING ERROR D-4-A5 PARITY OR MRK TRK ERROR D-4-A6 SELECT ERROR D-4-A8 REV D-8-B4 GO D-8-B4 MOTION 0 D-8-B5 WREN D-4-C3	REV D-8-B3 REV D-8-B4 GO D-8-B4 GO D-8-C4 GO D-8-B5 SET SELECT D-8-D2	MOTION 0 D-8-B5 MOTION 1 D-8-C5 MOTION 1 D-8-B6 MOTION 1 D-8-B6 WREN D-4-D2	UNIT 1 D-8-C2 REV D-8-C3 PARITY OR MARK TRK ERR D-4-A6 SELECT ERROR D-4-A8	MOTION D-8-C3	SELECT D-8-C3 SELECT D-8-D3 UNIT ENABLE D-8-D3	TPO D-3-C4 TPI D-3-C4 GO[0] D-8-C5 PWR CLR MB + DB MB + DB BR REQ D-4-A1 0 → DATA FLAG D-4-A1 MB + DB D-5-D7	MOTION D-8-D8 DATA FLAG D-4-A1 WREN D-4-C3 WREN B1 D-4-B4 WREN B1 D-4-B4 ST BLK MK D-3-B5 ST BLK MK D-3-B5 INTERRUPT D-4-A1 INTERRUPT D-4-A1	SET SELECT D-8-D2 SET SELECT D-8-D2 ST BLK MK D-3-A5 MOVE D-8-A7 ST DATA D-3-A7 ST FINAL D-3-A7 ST CHK D-3-A8 ST IDLE D-3-A8 WREN B1 D-4-C4	SINGLE UNIT D-8-A1 D-8-A1	LPB=0 D-5-A8 WREN D-4-D3	LPB2 D-5-A4 LPB1 D-5-A3 LPB0 D-5-A2 DATA FLAG D-4-A2	LPB5 D-5-A6 LPB3 D-5-A5 LPB4 D-5-A5 MT FLAG A-4-A3	LPB0 D-5-B2 LPB1 D-5-B3 LPB2 D-5-B4 LPB3 D-5-B4 LPB4 D-5-B5 LPB5 D-5-B6	LPB0 D-5-B2 LPB1 D-5-B3 LPB2 D-5-B4 LPB3 D-5-B4 LPB4 D-5-B5 KPB5 D-5-B6	RWB6 D-6-B2 RWB9 D-6-B3 RWB7 D-6-B5 RWB10 D-6-B5 RWB8 D-6-B7 RWB11 D-6-B7	SET WBO D-6-B1 RWB3 D-6-B2 RWB4 D-6-B4 RWB5 D-6-B6 RWB2 D-6-B7 RWB5 D-6-B7
2L	D-8-C1 AC → MOTION D-8-C1 AC → FUNCTION D-8-C1	D-5-D1 CLEAR MAC D-5-C7 AC → MAC D-5-C1	D-4-B5 IOT CLR FLAGS D-4-B5 IOT REPORT STATUS D-4-B5			D-5-D8 COMP. MAC11 D-5-C8 CLEAR MAC D-5-C1		TP-2					MOTION												
	4102R	4215[4]-1	4112R	4115R	4127	4129	4215[4]-1	6102R	4604[6]	4605[6]	4115R	4112R	4114R	4112R	4127	4117R	4117R	4114R	4127-01	4127R	4129R	4114R	4604[6]	4606[6]	4606[6]
2M	SHIFT WIN. D-3-A4 WRITE OK D-4-C8 MK END D-3-A3 WRTM. D-8-A8 RUN D-8-B6 MA EXT 2 D-5-D3 MA EXT 1 D-5-D4 RUN D-8-A6 RELTM D-4-C7	MC2 D-4-C8 MC1 D-4-C7 MC0 D-4-C6	ST DATA READ DATA D-4-C1 1 → DF D-4-C2 WREN D-4-D2 MT. INTERR. D-4-A1 RWB 0-5 LPB D-7-B4	PARITY OR MRK TRK ERR D-4-B7 ERROR D-4-B8 ALL BITS D-4-C2 SHIFT WIN MT. DECODER D-3-A5	PARITY OR MRK TRK ERR. D-4-B6 PARITY OR MRK TRK ERR. D-4-B7 SELECT ERROR D-4-B8 SELECT ERROR D-4-B8 WREN D-4-C3 WREN D-4-C3	1 → DF D-4-B2 TIMING ERROR D-4-B5 D-4-C6	CK2 D-3-C2 CK1 D-3-C2 DTG1 D-3-C7 DTGO D-3-C7	TP-1 D-3-C3 TP-2 D-3-D8 MK BLK MK D-4-B3 MT FLAG D-4-B3 TP-2 D-3-C5 1 → DF D-4-B3 1 → MFT D-4-B3 WREN D-4-D3 LPB → RWB 0-5 D-7-C4	TP-2 D-3-C7 DTP-2 D-3-C7 0 → LPB D-7-C3	TP-1 D-3-C4 TP-0 D-3-C5 DTP-0 D-3-C6	COMP. MKB D-3-C4 CLR. MKB D-3-B4 TP-1 D-3-C3 CK ENABLE D-3-D1 D-3-C6	SHIFT RIGHT RWB D-2-1B SHIFT LEFT RWB D-7-4B SHIFT LEFT RWB D-7-4B DB → RWB RWB → DB D-7-2C SHIFT LEFT RWB D-7-4B 1-DF AT ST.REV.CHK. D-4-B1	ST FINAL D-3-B7 PARITY OR MARK TRK ERR D-4-B7 1 → DF D-4-C1 WREN D-4-D3	ST REV CHK D-3-B6 DATA D-3-B7 ST CHECK D-3-B8 ST IDLE D-3-B8 DTP-0 D-3-C6 X TALK D-3-D5	ST BLK MK D-3-B6 ST REV CHK D-3-B6 ST DATA D-3-B7 ST FINAL D-3-B7 ST CHK D-3-B8 ST IDLE D-3-B8	ST BLK MK D-3-A5 ST REV CHK D-3-A6 ST DATA NO LOAD D-3-A6	ST FINAL D-3-A7 ST CHK D-3-A8 ST IDLE D-3-A8	MT FLAG D-4-A3 WREN D-4-D4 SHIFT RIGHT RWB D-7-2B CLEAR AC. D-8-D6	SHIFT RIGHT RWB D-7-B1 SHIFT LEFT RWB D-7-B5 RWB 0-5 LPB D-7-B5 RWB 6-11 LPB D-7-B7 END D-4-B4 MB → DB	SHIFT RIGHT RWB D-7-2A SHIFT LEFT RWB D-7-4A RWB 0-5 LPB D-7-5B RWB 6-11 LPB D-7-8A LPB → RWB 6-11 D-7-C5 SET SELECT D-8-D2	DATA FLAG D-4-B2 MT FLAG D-4-B3	RWB 0-5 LPB D-7-B6 RWB 6-11 LPB D-7-B7 RWB 6-11 LPB D-7-B8 RWB 0-5 LPB D-7-B6	LPB → RWB 6-11 D-7-C6 AC → MAC D-5-D1 DB 31 AC → UNIT	SHIFT LEFT RWB D-7-A5 RWB 0-5 LPB D-7-A7 RWB 6-11 LPB D-7-A8	DB → RWB RWB → DB D-7-C2 LPB → RWB 0-5 D-7-C5 SHIFT RIGHT RWB D-7-A3

NOTE:
1. JUMPER "1" OUTPUTS WITH 100Ω 1/4W RESISTORS (4222 MODULE)
2. 4228 & 4228-1 JUMPER ZERO SIDE
3. 4151 - CUT OUT JUMPER BETWEEN P & D ONLY CLAMP LOADS REMAIN
4. 4215 - INHIBIT CONNECTION IDENTIFIED BY -1; NORMAL LOADING CONNECTION BY -2
5. INDICATES NO JUMPERS.
6. -15V DC. MARGINAL CHECK SUPPLY IS WIRED TO THESE PACKAGES.
7. THE 4227 IN 2L9 HAS A D003 DIODE WIRED BETWEEN THE PI OUTPUT LINES, THE CATHODE IS CONNECTED TO THE PIN P PI OUTPUT LINE.

Utilization Module Location
UML-D-552-0-14

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	* W021														
I	IN-OUT CONN ACO(1) TO AC8(1)	I-O AC9(1) TO AC11(1) IOP 1,2,4 T1, T2 PWR CLR	I-O MB0(1) TO MB5(1)	I-O MB6(1) TO MB11(1)	I-O IM 0 TO IM 8	I-O IM 9 TO IM 11 SKIP INTER, AC,CL RUN	DATA ADDR 0(1) TO 8(1)	DATA ADDR 9(1) TO 11(1) ADDR ACK, BK,REG, TRD INC MB	DATA BIT 0(1) TO 8(1)	DATA BIT 9(1) TO 11(1)	DF0(1) DF1(1) DF2(1) ADD EXT 1 ADD EXT 2 ADD EXT 3													
	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021															
J	IN-OUT CONN. ACO(1) TO AC8(1)	I-O AC9(1) TO AC11(1) IOP 1, 2, 4 T1,T2 PWR CLR	I-O MB0(1) TO MB5(1)	I-O MB6(1) TO MB11(1)	I-O IM 0 TO IM 8	I-O IM 9 TO IM 11 SKIP INTER, AC,CL RUN	DATA ADDR 0(1) TO 8(1)	DATA ADDR 9(1) TO 11(1) ADDR ACK, BK, REG, TRD	DATA BIT 0(1) TO 8(1)	DATA BIT 9(1) TO 11(1)															

* FOR EXTRA MEMORY



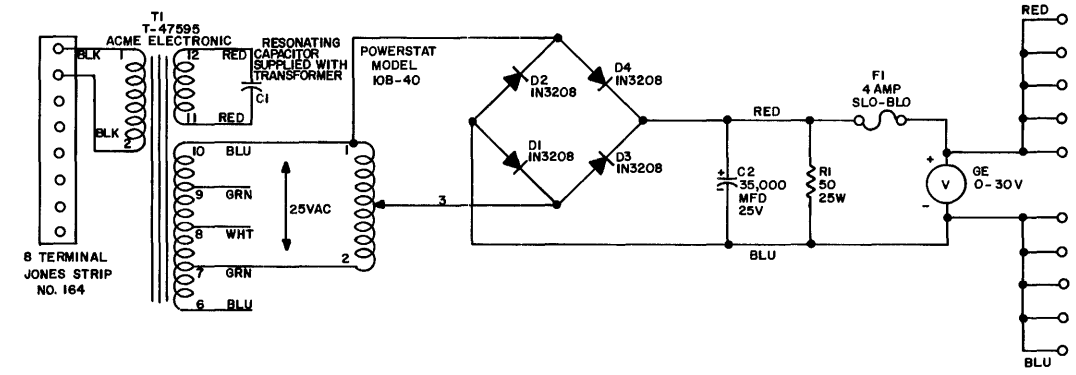
* HEYMAN MFG. CO.
TAB TERMINALS

NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES	+10 V	0	TO	7.0	AMPS
LOADED	-15 V	1.0	TO	8.0	AMPS
ONE SIDE	+10 V	0	TO	7.5	AMPS
LOADED	-15 V	1.0	TO	8.5	AMPS

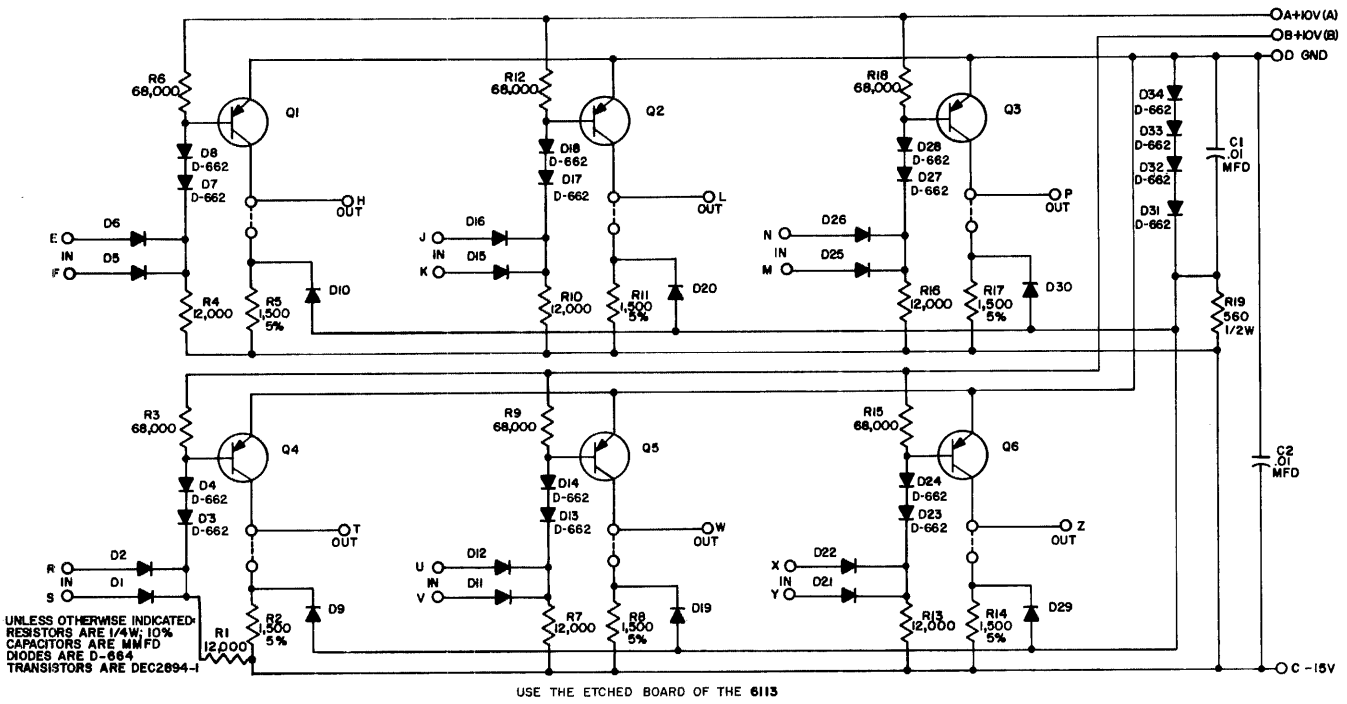
SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE FOLLOWING EQUATION: $5I_{10} + 6I_{15} \leq 53$

Power Supply RS-B-728

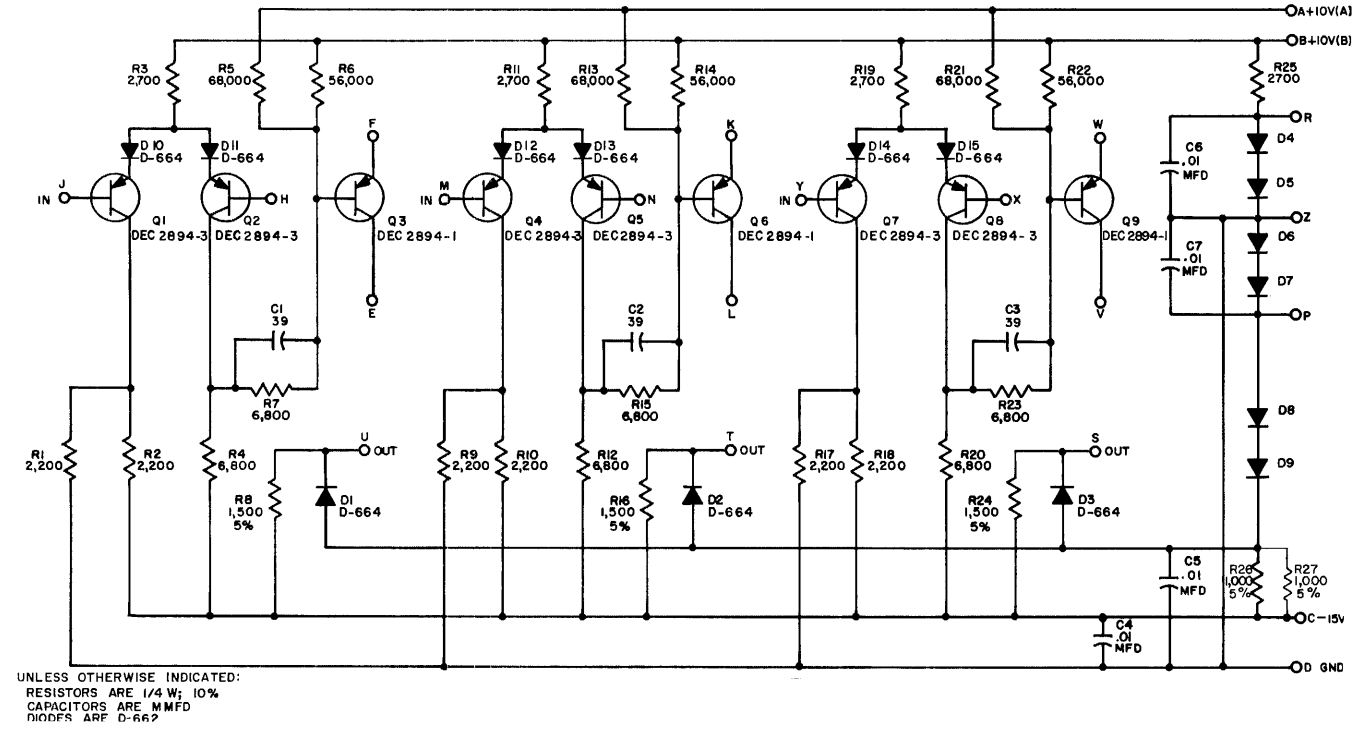


NOTE:
OUTPUT IS CONNECTED THROUGH
HEYMAN TAB TERMINALS

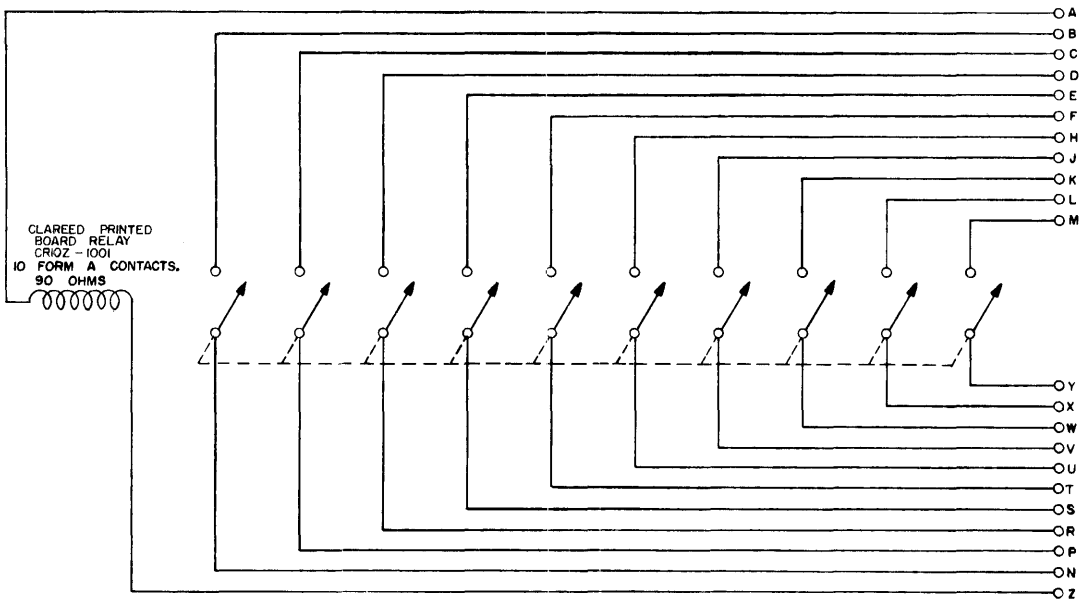
20v Variable Power Supply RS-B-734



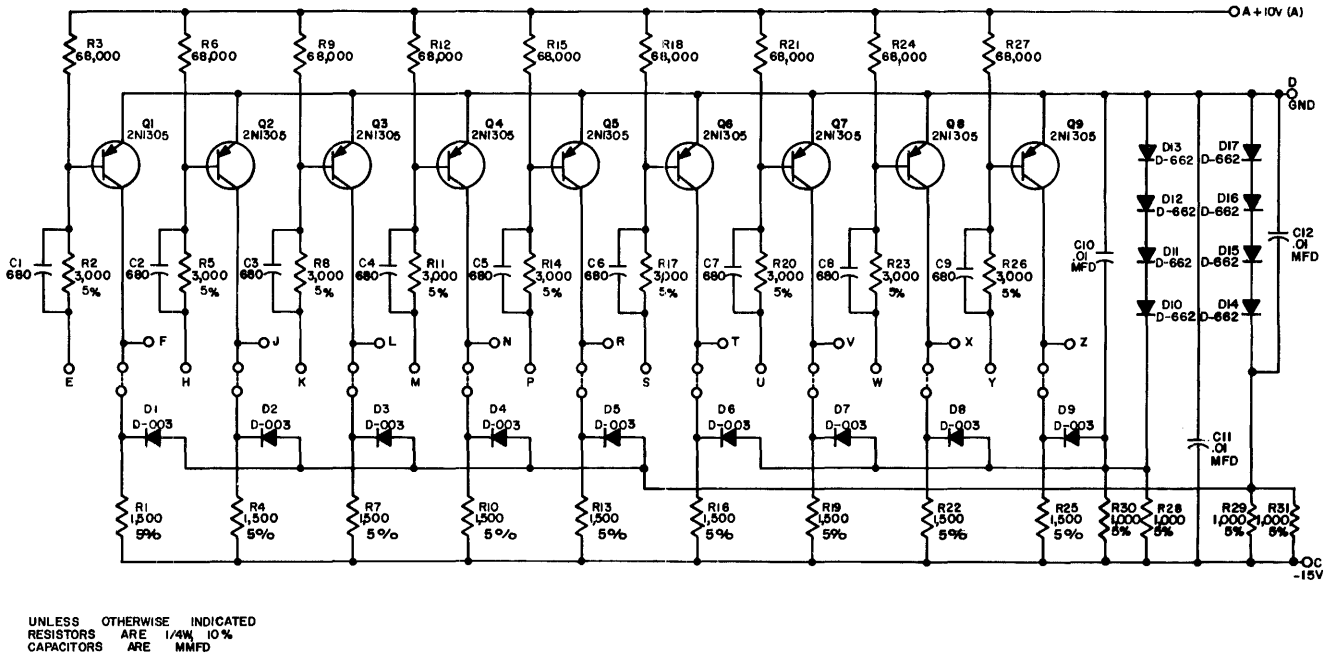
Diode RS-B-1113



Level Standardizer RS-B-1501

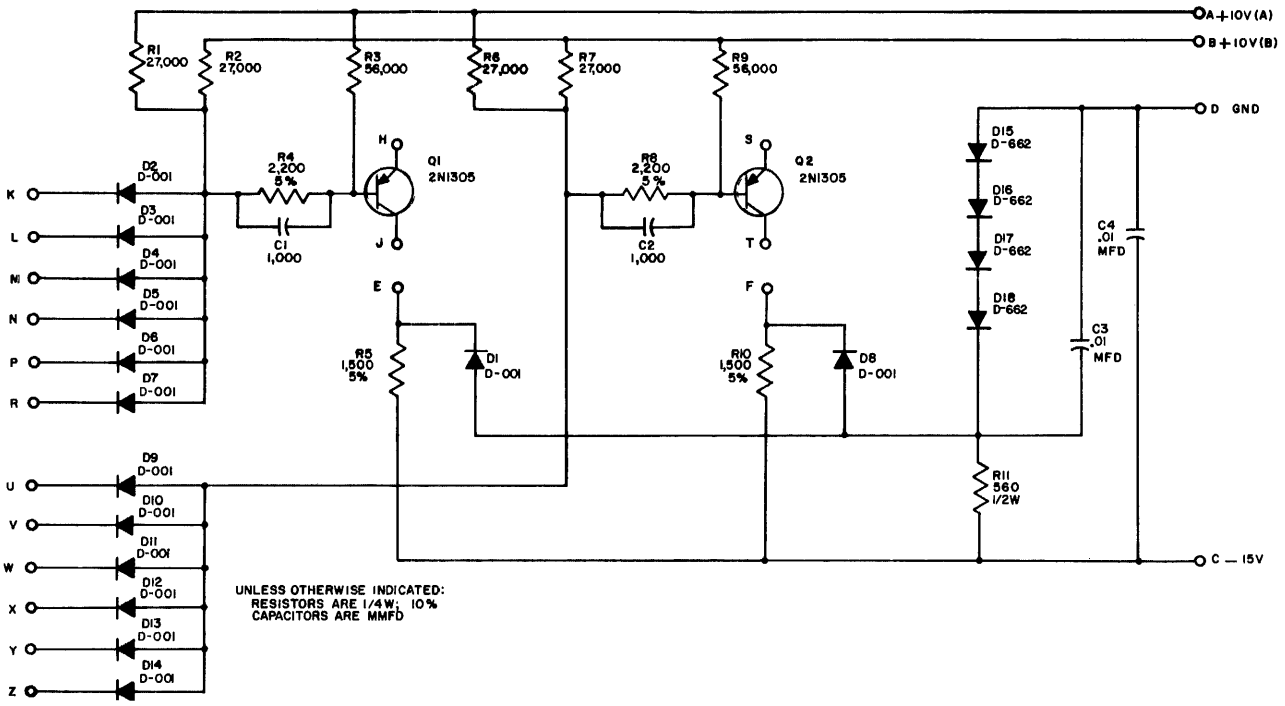


Relay RS-B-1802

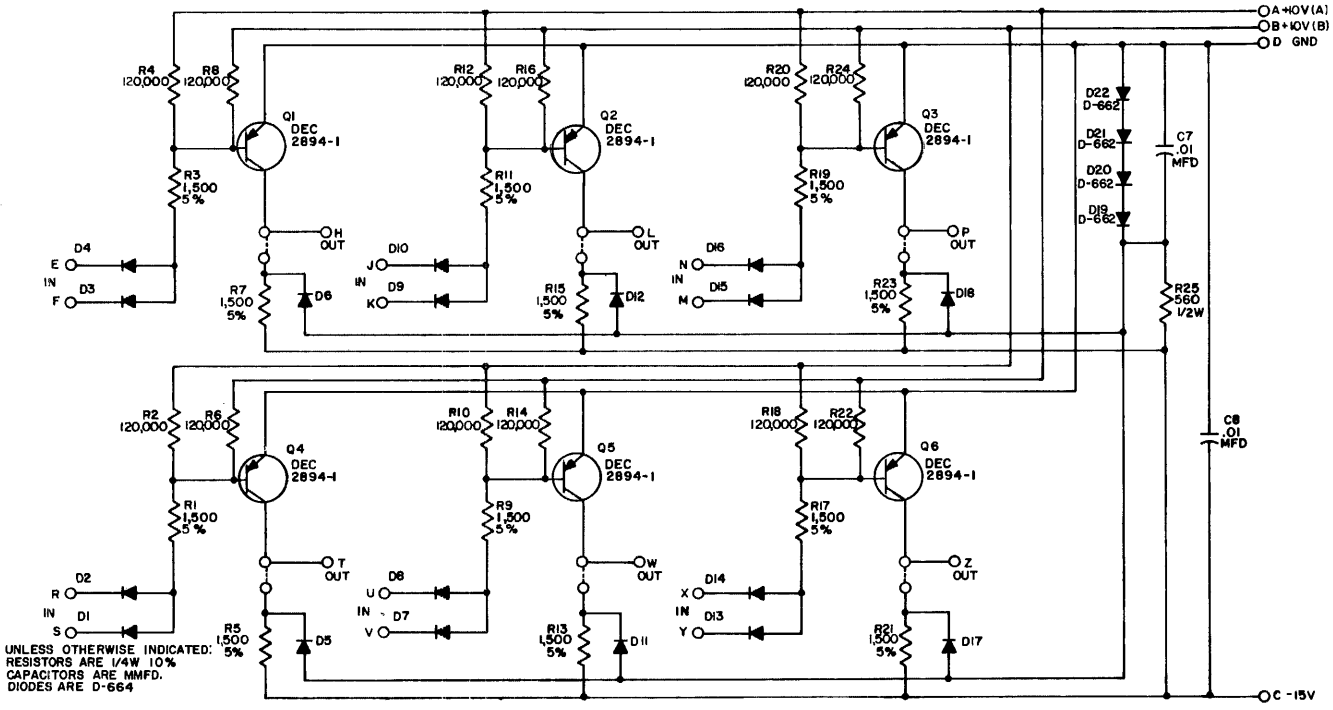


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

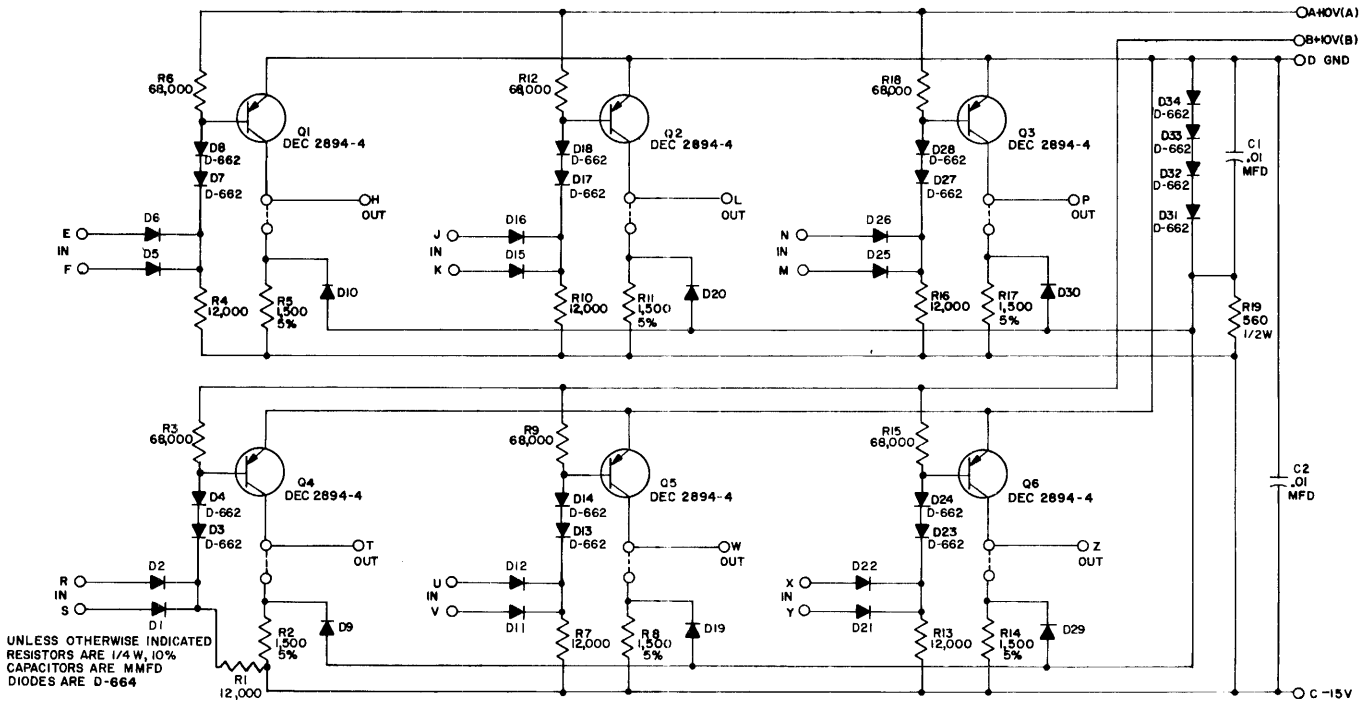
Inverter RS-B-4102



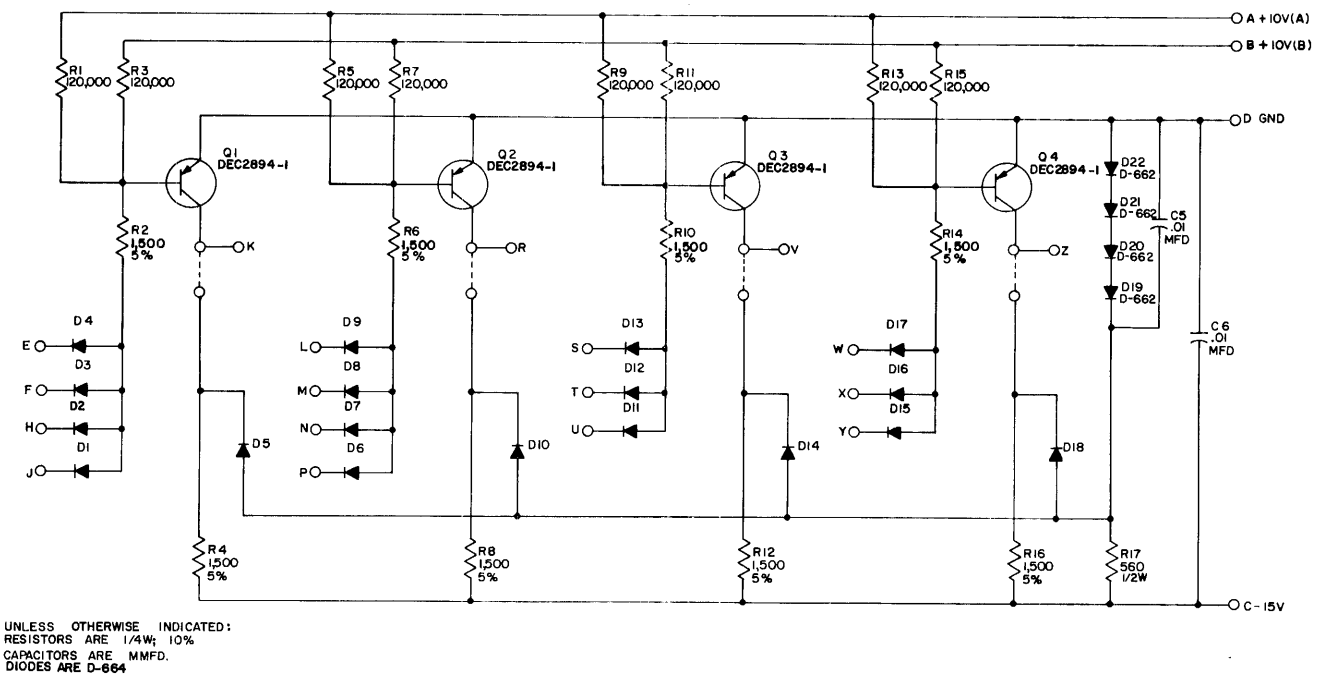
Diode Unit RS-B-4110



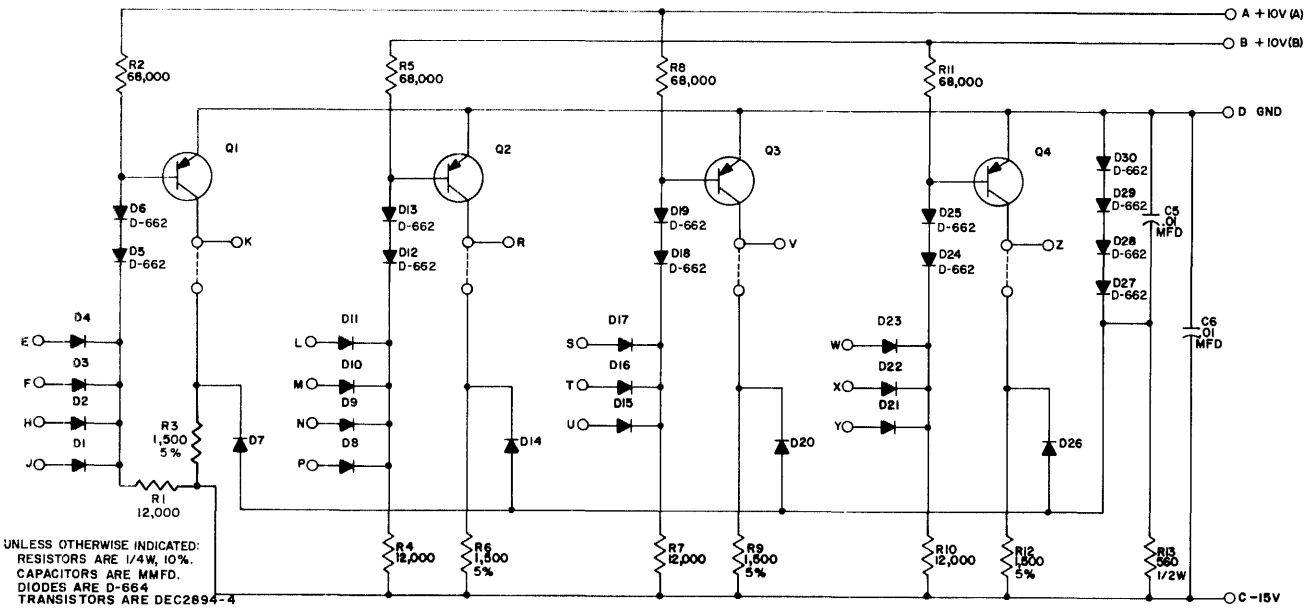
Diode RS-B-4112-R



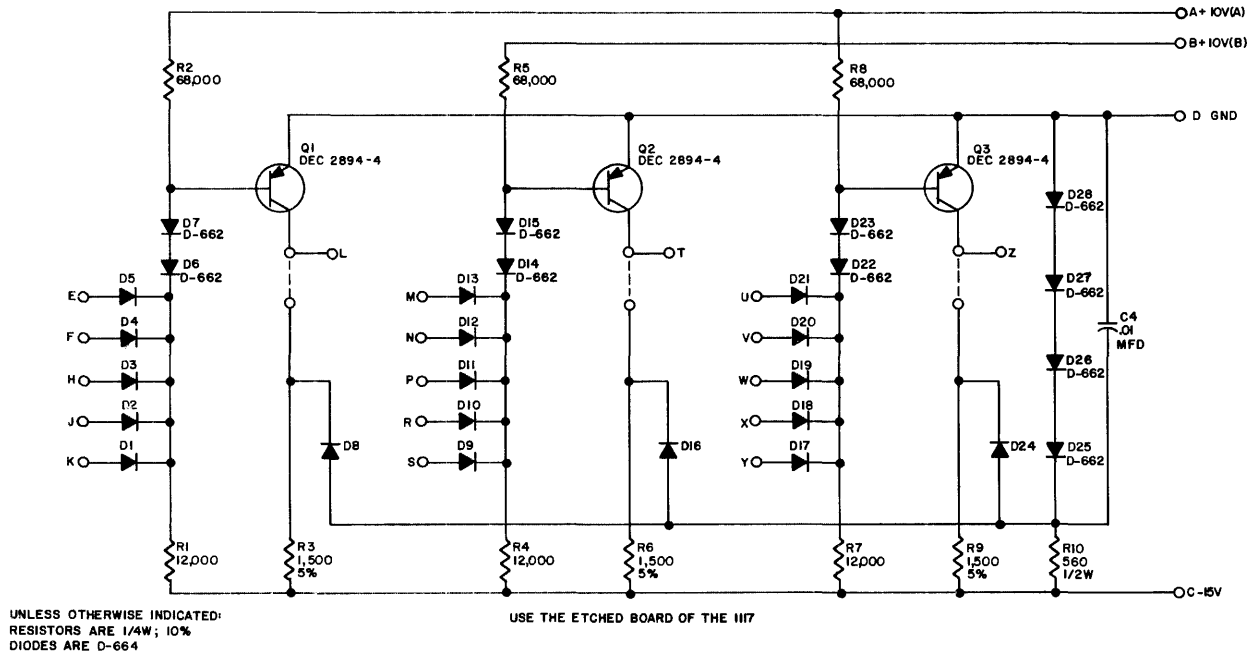
Diode RS-B-4113-R



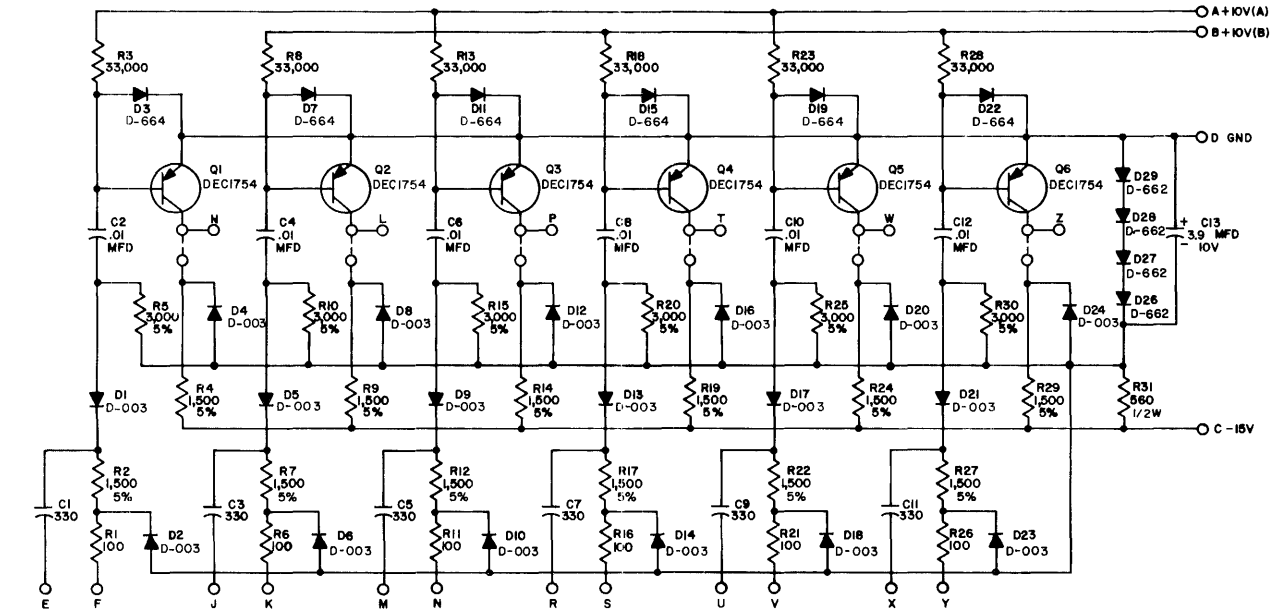
Diode RS-B-4114



Diode RS-B-4115

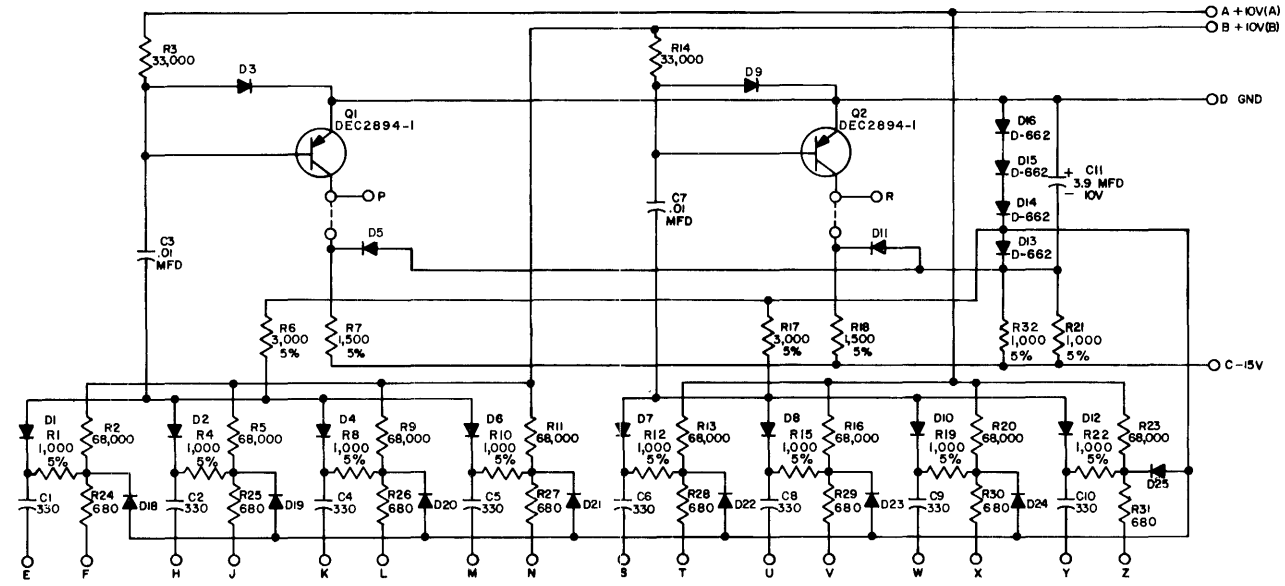


Diode RS-B-4117



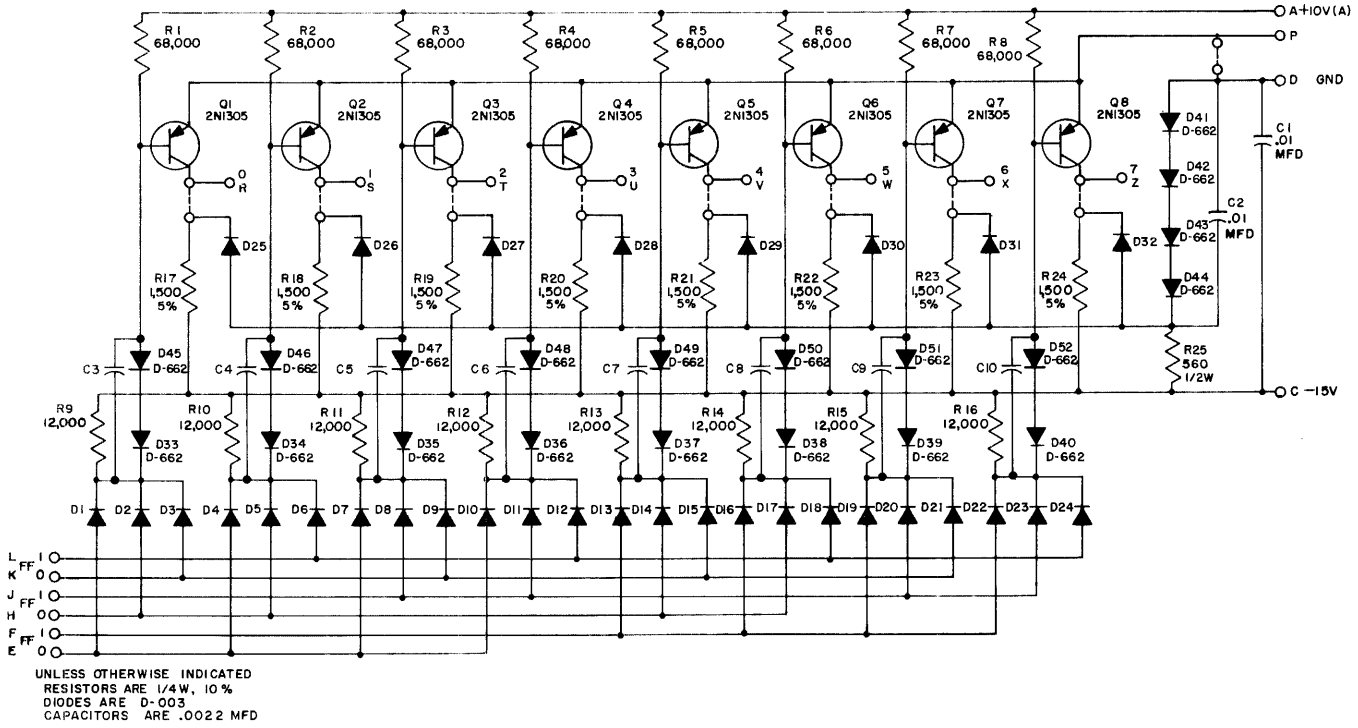
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

Capacitor Diode Inverter RS-B-4127

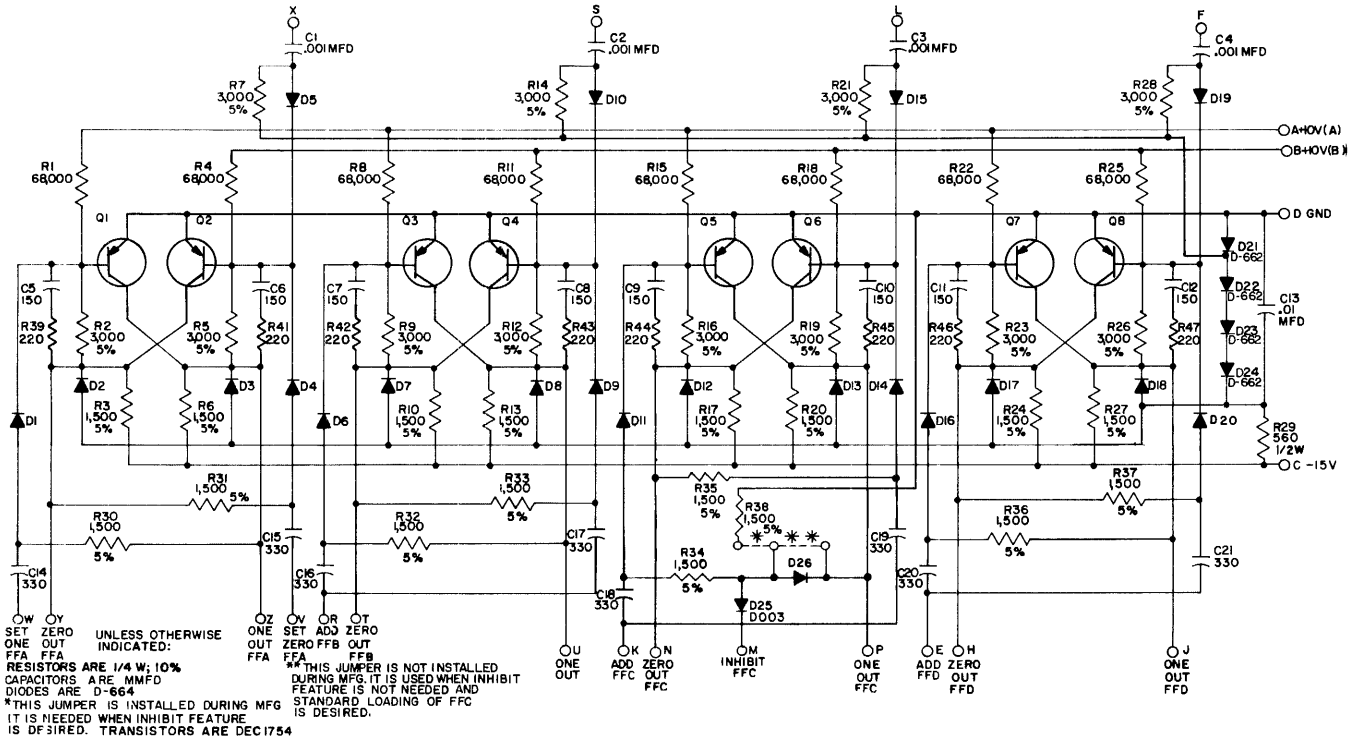


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W ; 10%
CAPACITORS ARE MMFD
DIODES ARE D-664

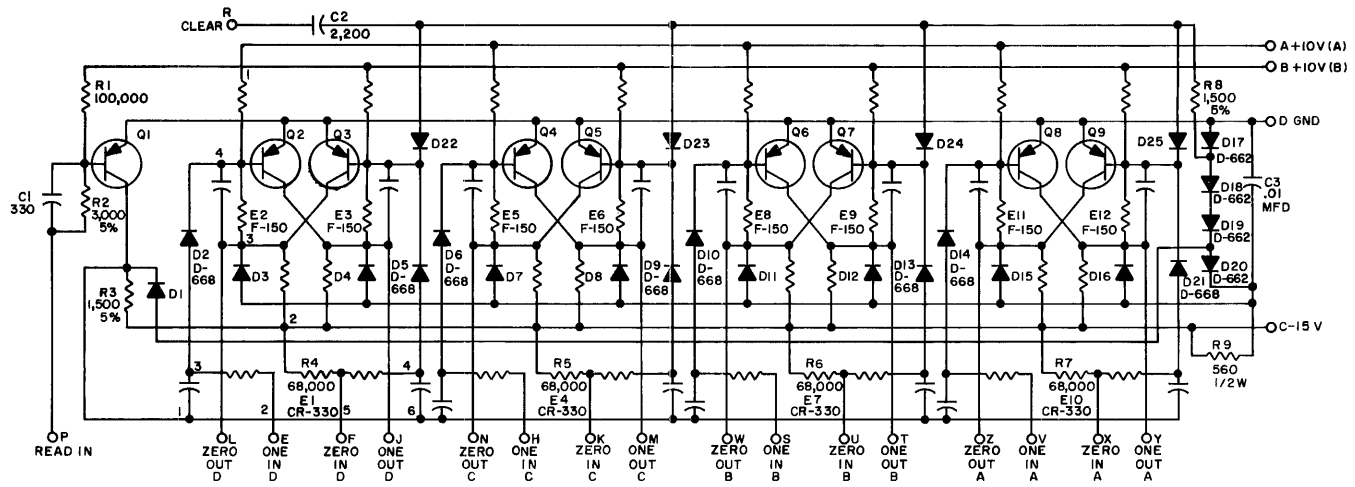
Capacitor Diode Inverter RS-B-4129



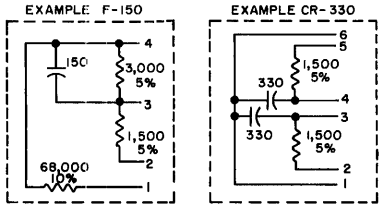
Binary-to-Octal Decoder RS-B-4151



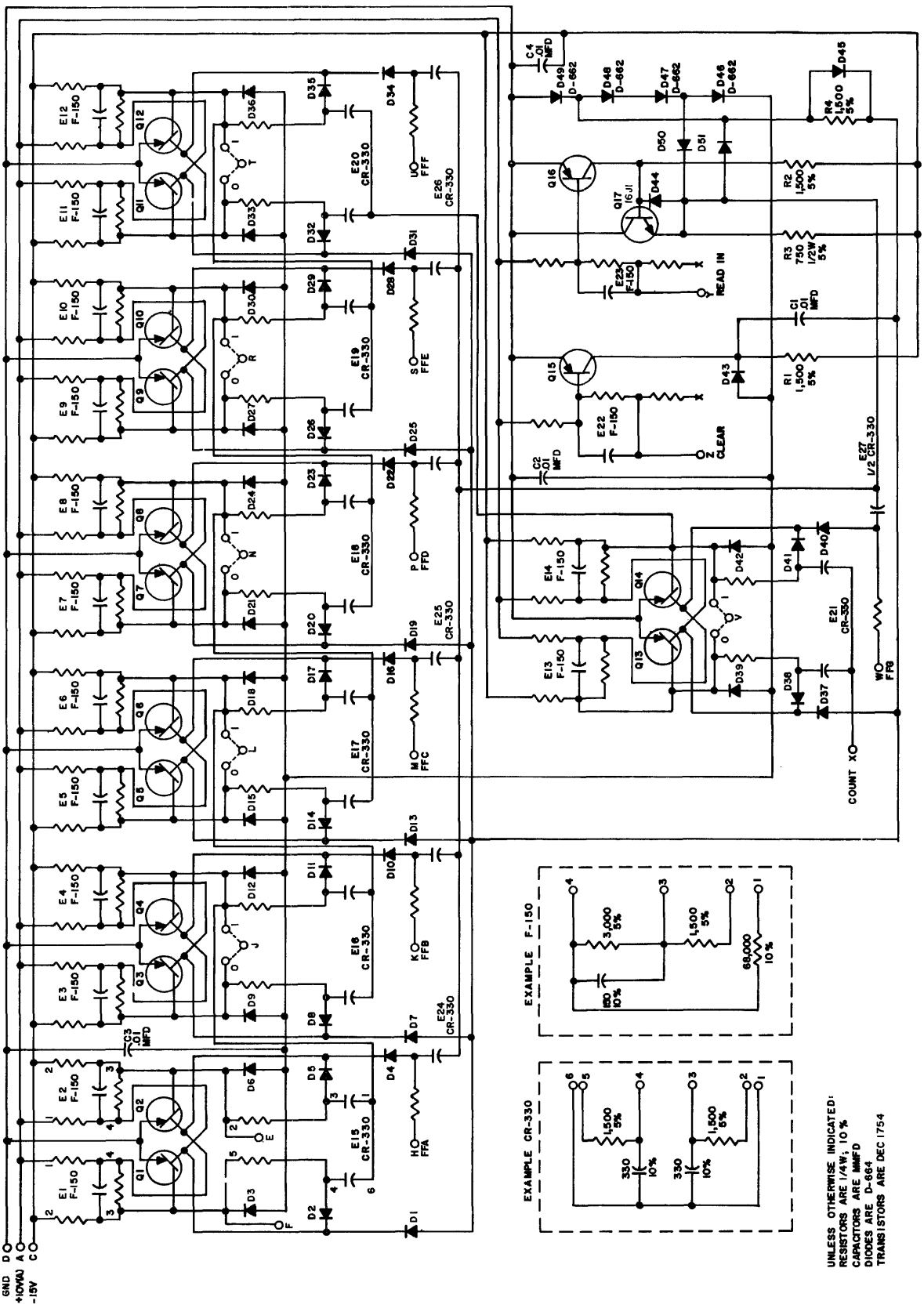
4-Bit Counter RS-B-4215



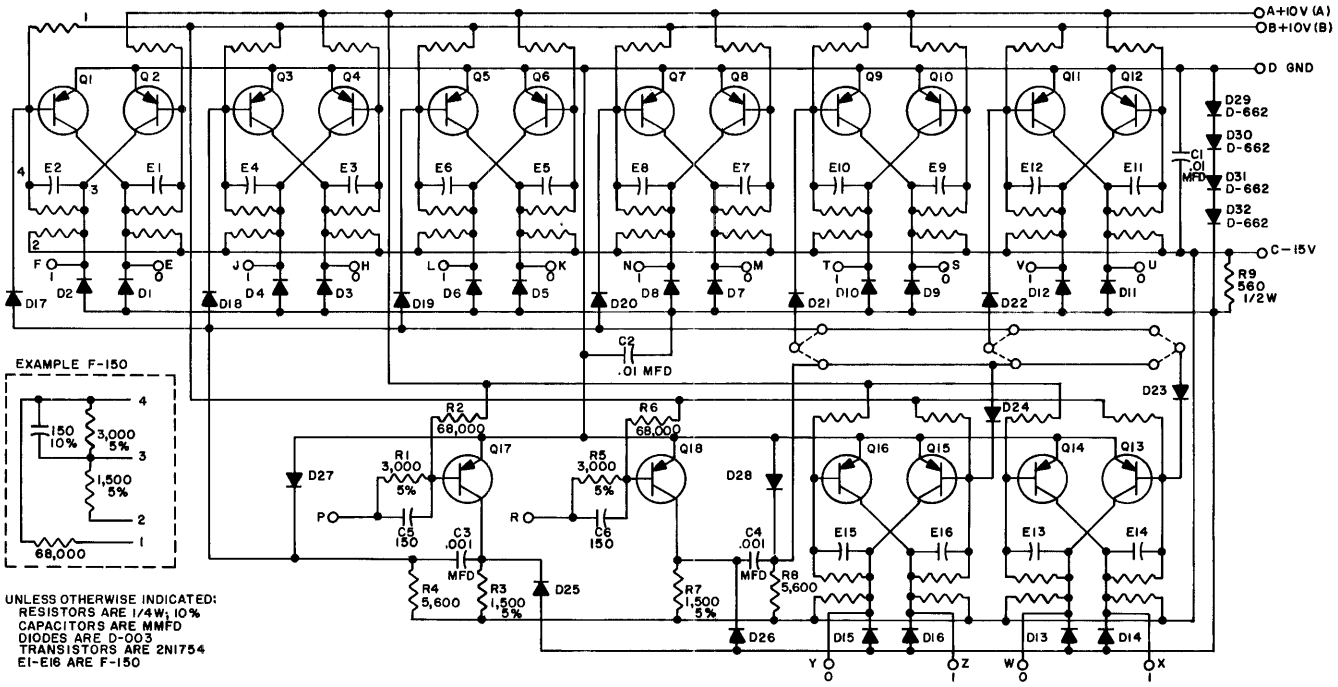
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD.
DIODES ARE D-664
TRANSISTORS ARE DEC 2894-4



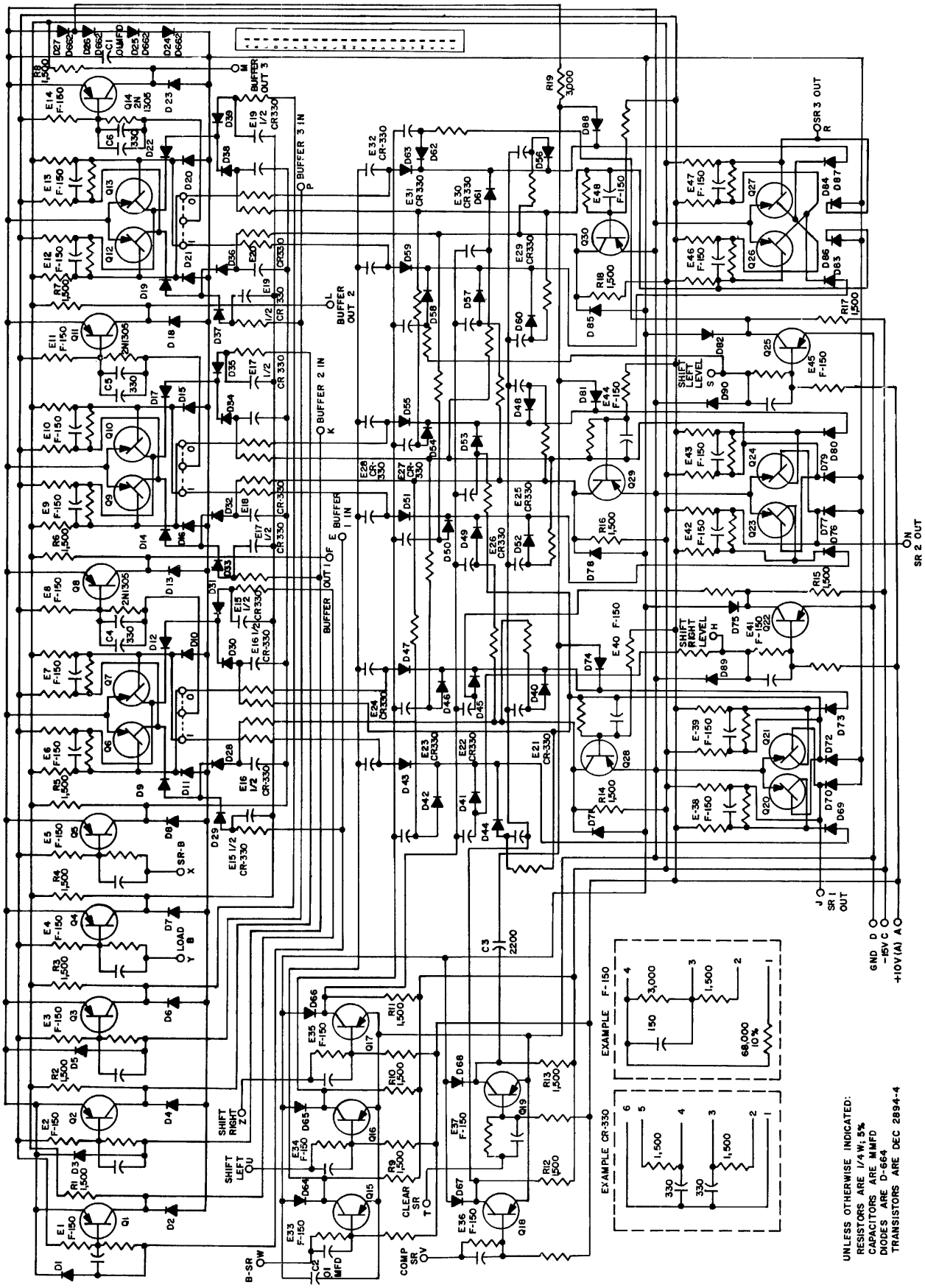
Quadruple Flip-Flop RS-B-4218



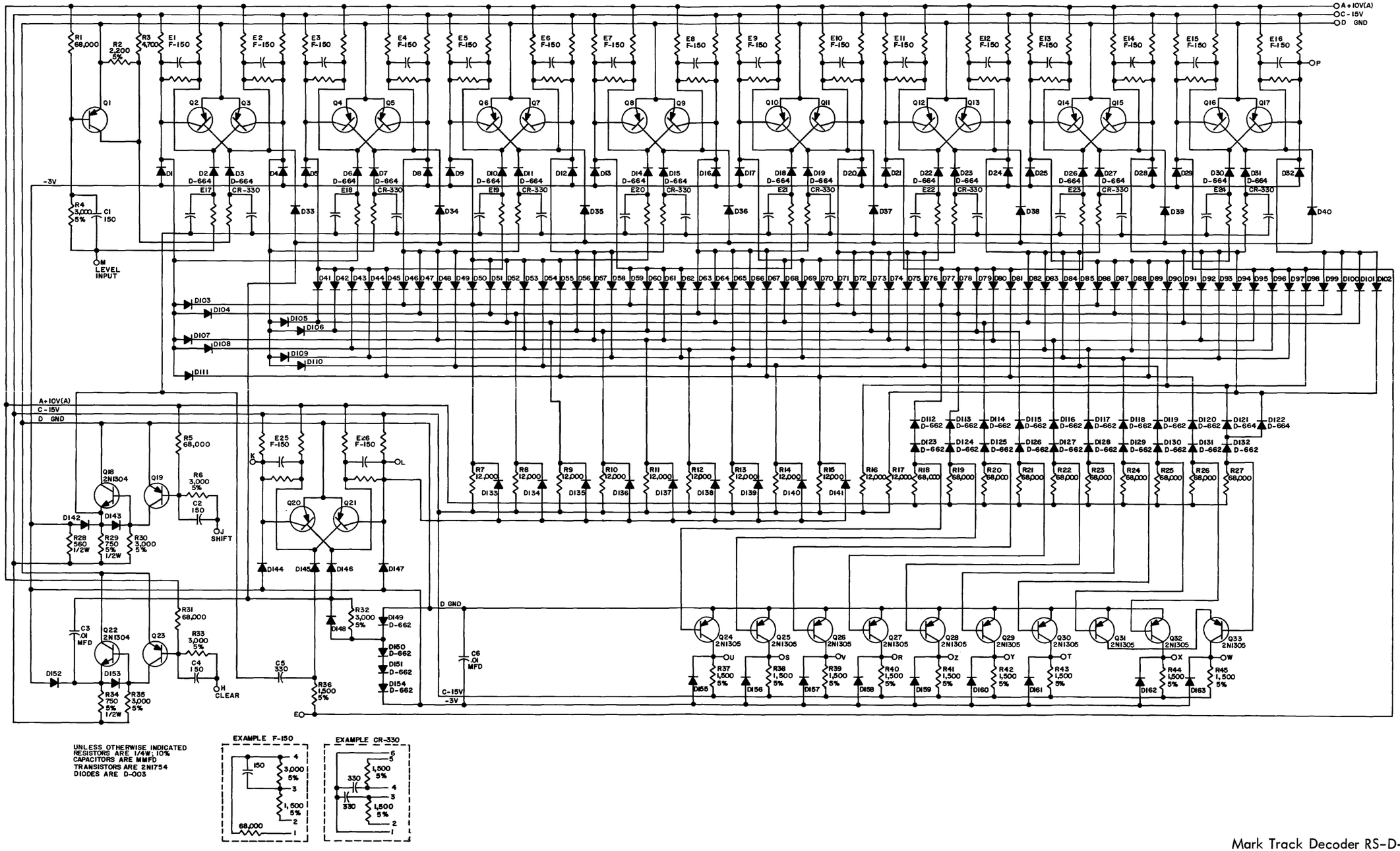
7-Bit Counter with Readin Gates RS-C-4222



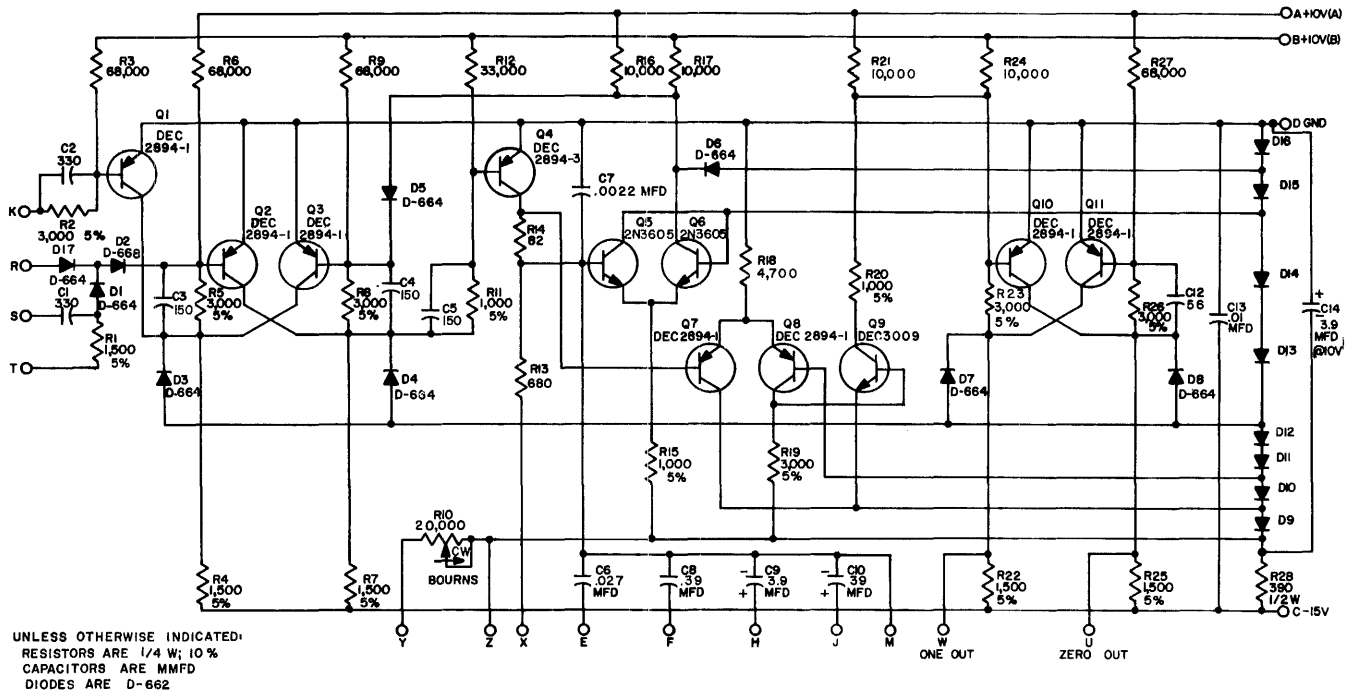
8 Unbuffered Flip-Flops RS-B-4227



3-Bit Shift Register with Buffer Register RS-C-4228

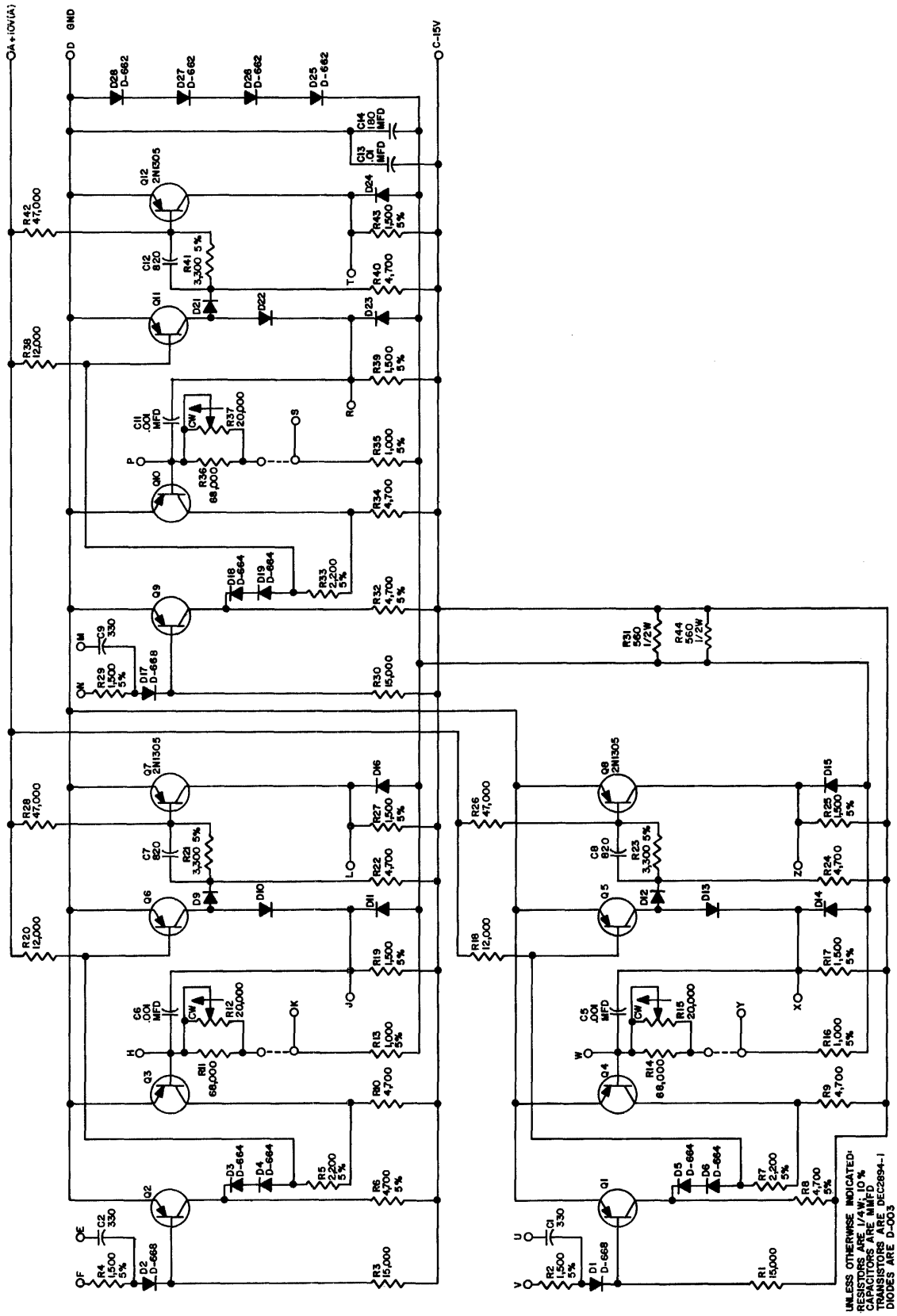


UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE 2N1754
DIODES ARE D-003

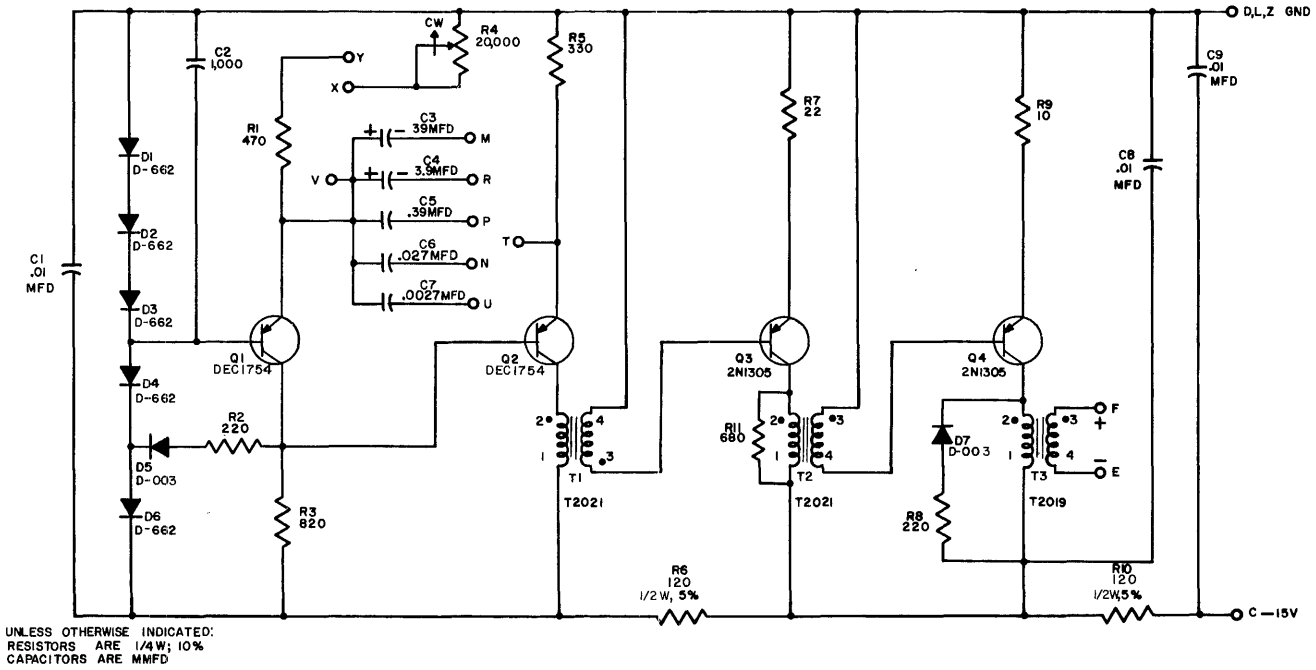


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10 %
CAPACITORS ARE MMFD
DIODES ARE D-662

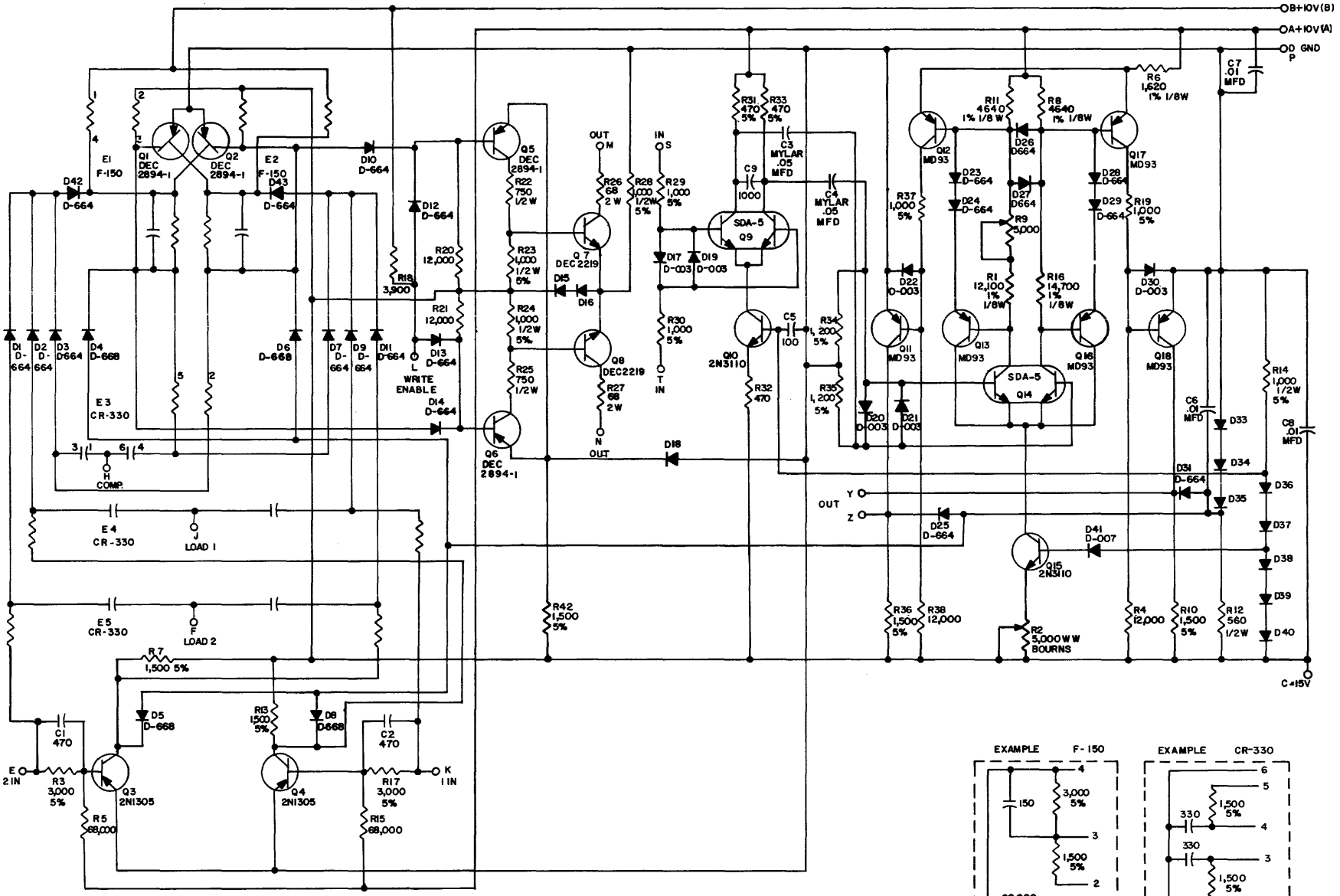
Integrating One-Shot RS-B-4303

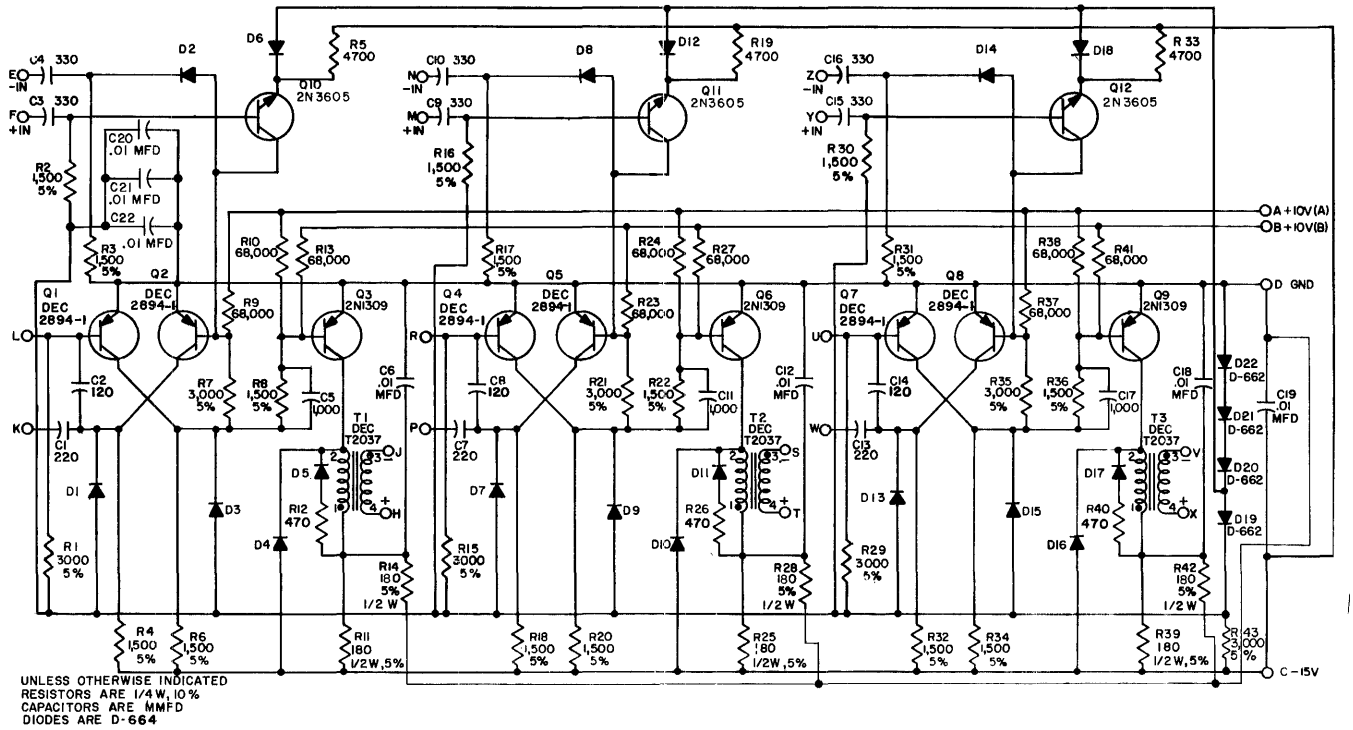


Delay RS-C-4306

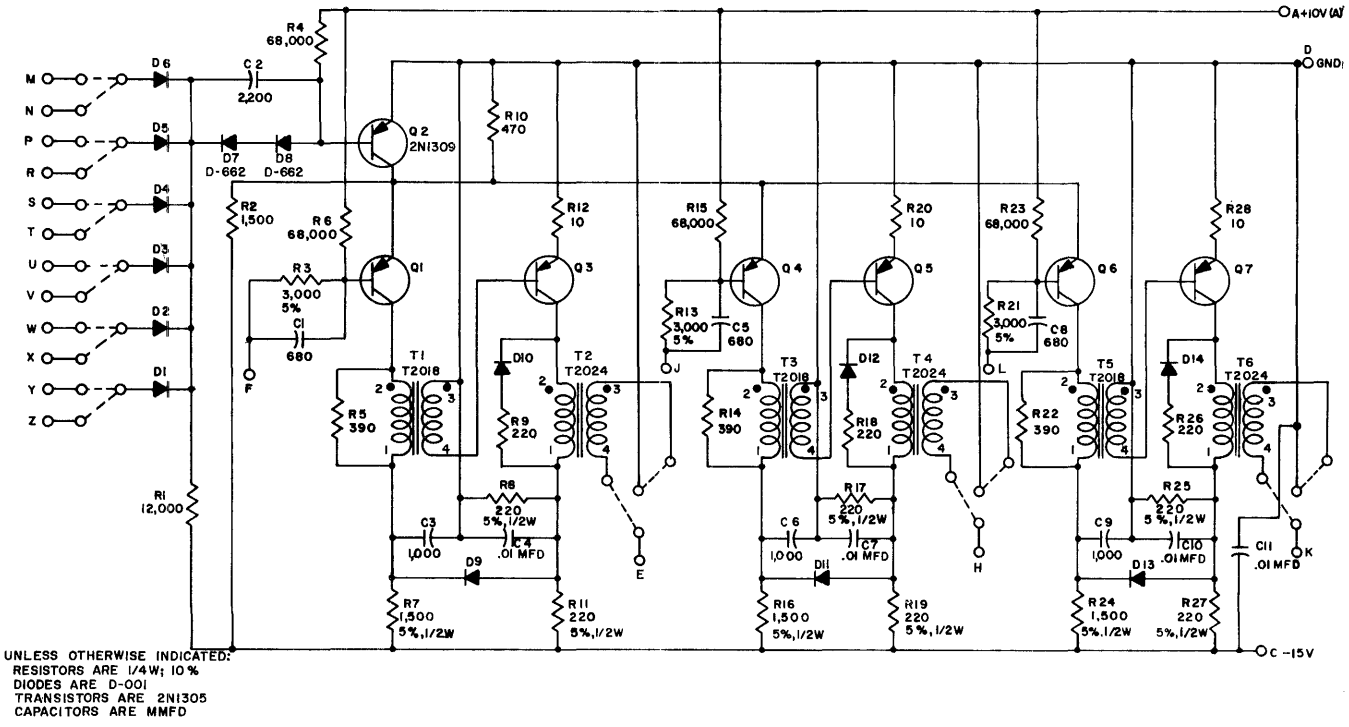


Clock RS-B-4401

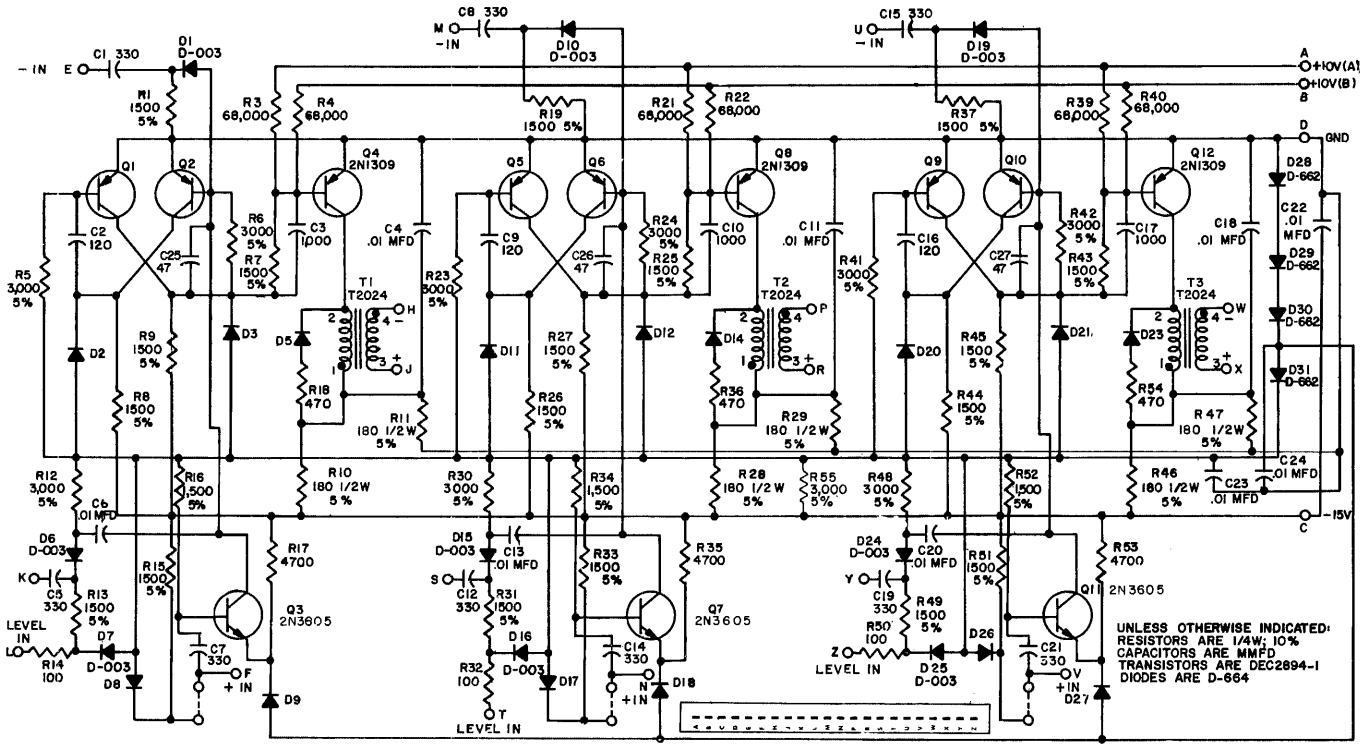

B+10V(B)
A+10V(A)
D GND
P
C+15V
E1 F-150
E2 F-150
E3 CR-330
E4 CR-330
E5 CR-330
Q1 DEC 2894-1
Q2 DEC 2894-1
Q3 2N1305
Q4 2N1305
Q5 DEC 2894-1
Q6 DEC 2894-1
Q7 DEC 2219
Q8 DEC 2219
Q9 SDA-5
Q10 2N3110
Q11 MD93
Q12 MD93
Q13 MD93
Q14 SDA-5
Q15 2N3110
Q16 MD93
Q17 MD93
Q18 MD93
WRITE ENABLE
H COMP.
LOAD 1
LOAD 2
OUT M
IN S
T IN
N OUT
OUT Y
Z
E 2 IN
K 1 IN
R9 5,000
R2 5,000 WW BOURNS
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE MMFD
DIODES ARE D-662
RESISTORS ARE 1/4W; 10%.
R1, R6, R8, R11, R16, ARE LOW TEMP. COEF. MF; 50PPM/°C
R9 IS A C.T.S. METAL FILM POT.
EXAMPLE F-150
EXAMPLE CR-330



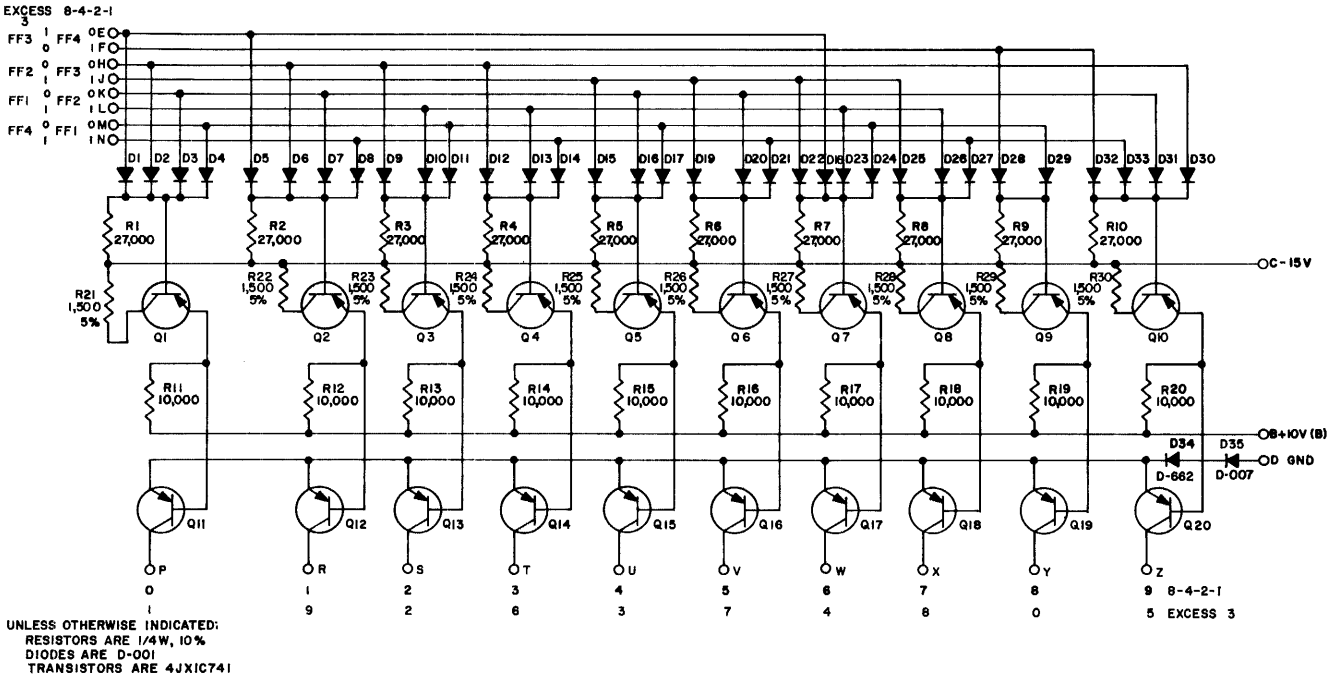
Pulse Amplifier RS-B-4604



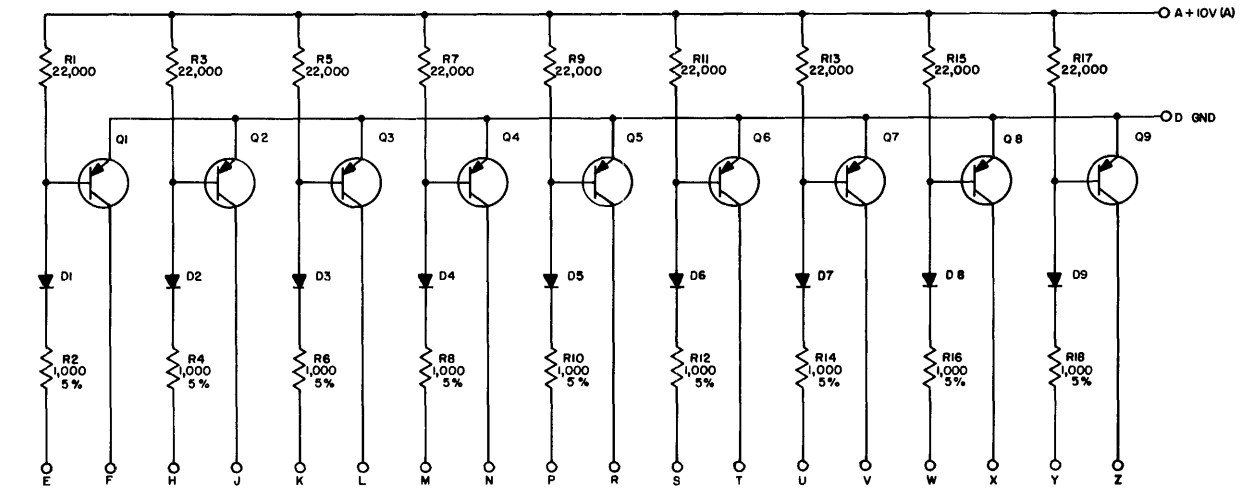
Pulse Amplifier RS-B-4605



Pulse Amplifier RS-B-4606

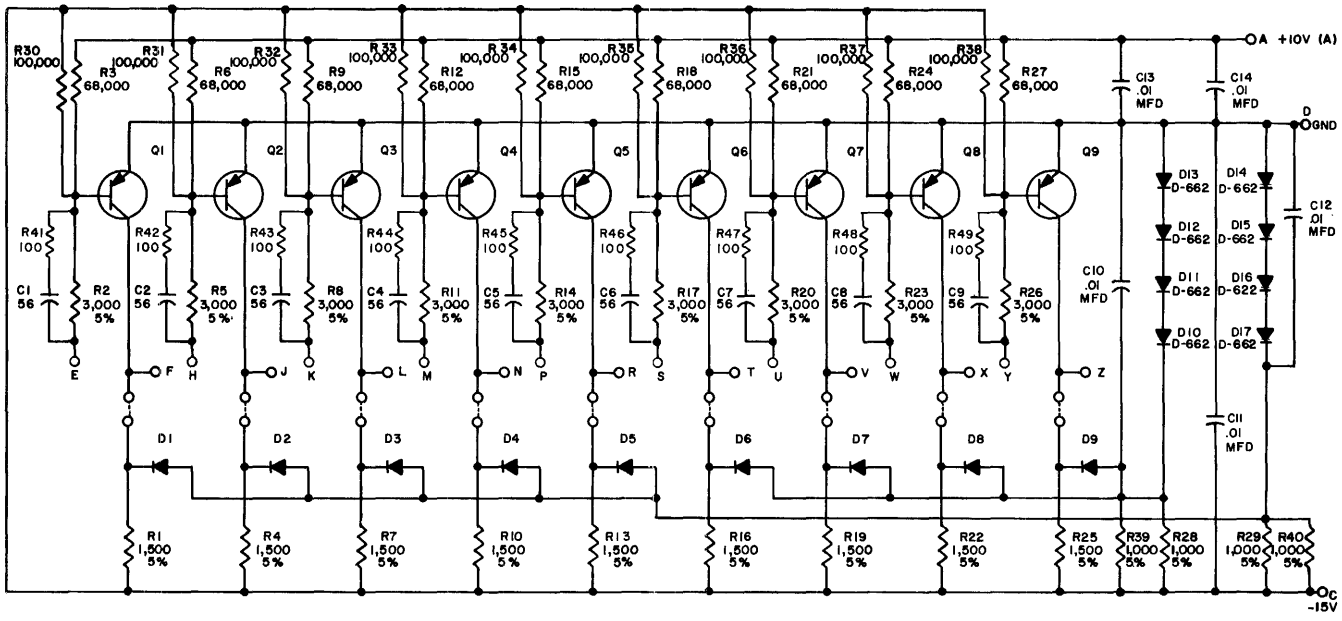


BCD Light Driver RS-B-4671



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
TRANSISTORS ARE 4JXIC741
DIODES ARE D-662

Indicator Driver RS-B-4689



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-I
DIODES ARE D-664

Inverter RS-B-6102

5551

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2.5-4/66