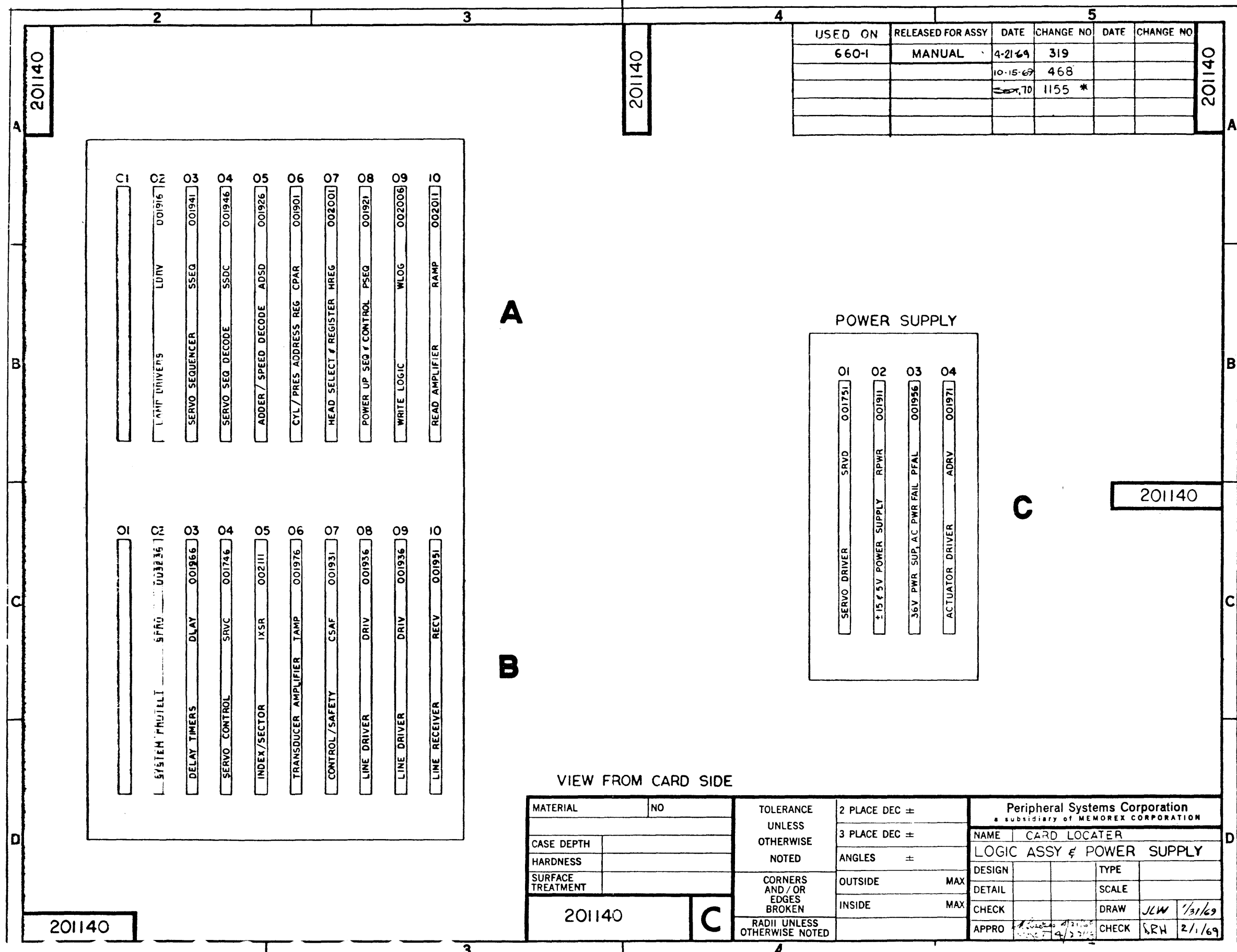




2



201140

201140

201140

201140

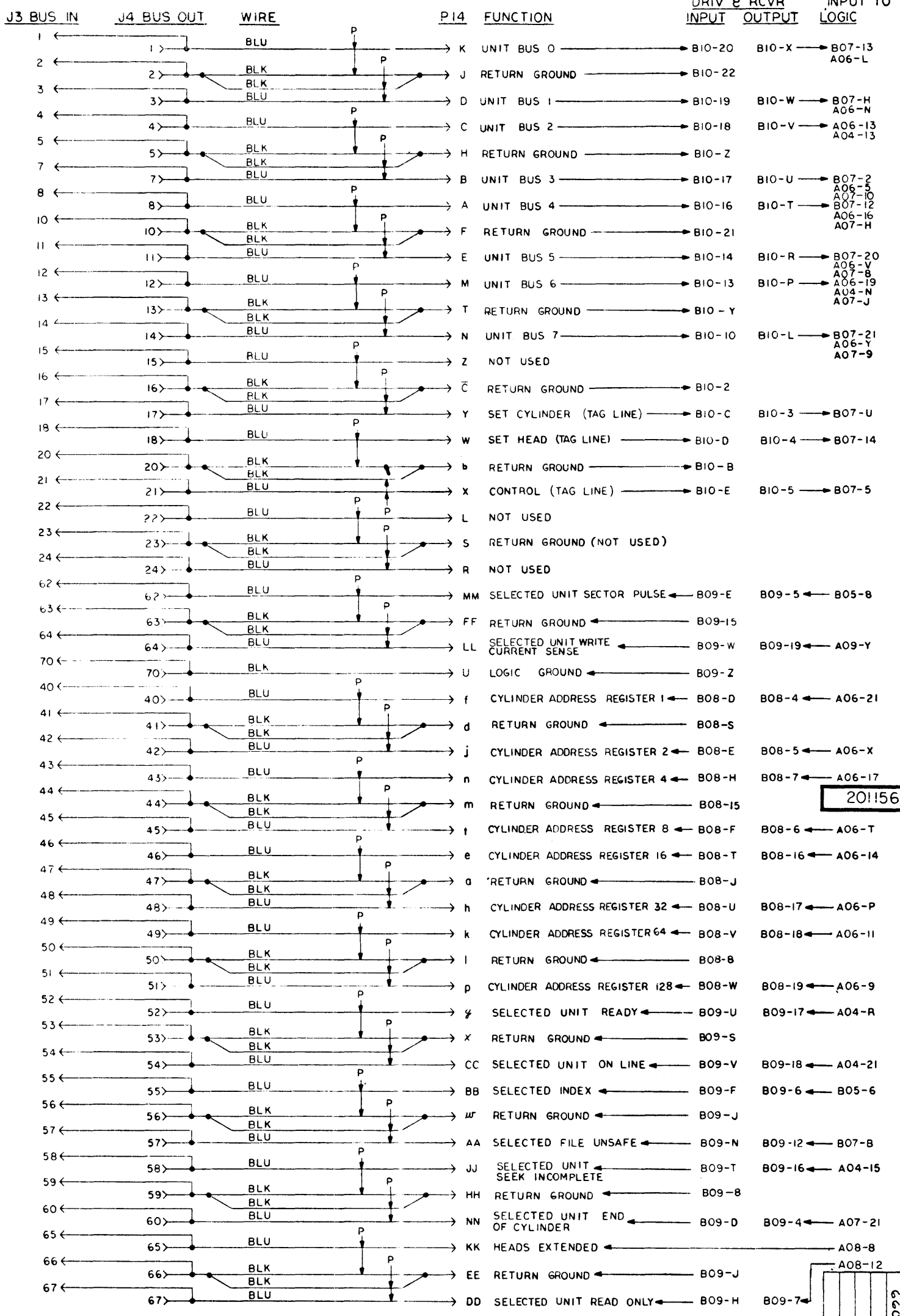
201140

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660-1	MANUAL	4-21-69	319		
		10-15-69	468		
		10-17-70	1155 *		

VIEW FROM CARD SIDE

MATERIAL	NO	TOLERANCE	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH		UNLESS OTHERWISE NOTED	3 PLACE DEC ±	NAME	CARD LOCATER
HARDNESS			ANGLES ±	LOGIC ASSY & POWER SUPPLY	
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
			INSIDE MAX	DETAIL	SCALE
		RADIi UNLESS OTHERWISE NOTED		CHECK	DRAW JLW 1/31/69
				APPRO	CHECK SRH 2/1/69

LOGIC PRINT REF



NOTES:  
 1. PINS 73, 74, 75 & PINS 25 THRU 39 ARE SPARES  
 2. FOR CIRCUITRY ASSOCIATED WITH PINS 71, 76, 77 AND 78 SEE DRAWING NO. 201112.  
 3. PINS 6, 9, 19, 61, 68, 69 & 81 ARE NON EXISTENT.  
 4. FOR CIRCUITRY ASSOCIATED WITH PINS 72 & 79 SEE DRAWING NO. 201157.

201156

2

3

4

5

6

7

8

9

MATERIAL		NO	
CASE DEPTH		TOLERANCE	
HARDNESS		UNLESS OTHERWISE NOTED	
SURFACE FINISH		3 PLACE DEC =	
DIMENSION		ANGLES =	
CORNERS AND/OR EDGES BROKEN		DESIGN SCALE	
MAX DETAIL		TYPE	
MAX CHECK		SCALE	
APPRO		DRAW	

201156

D

201156

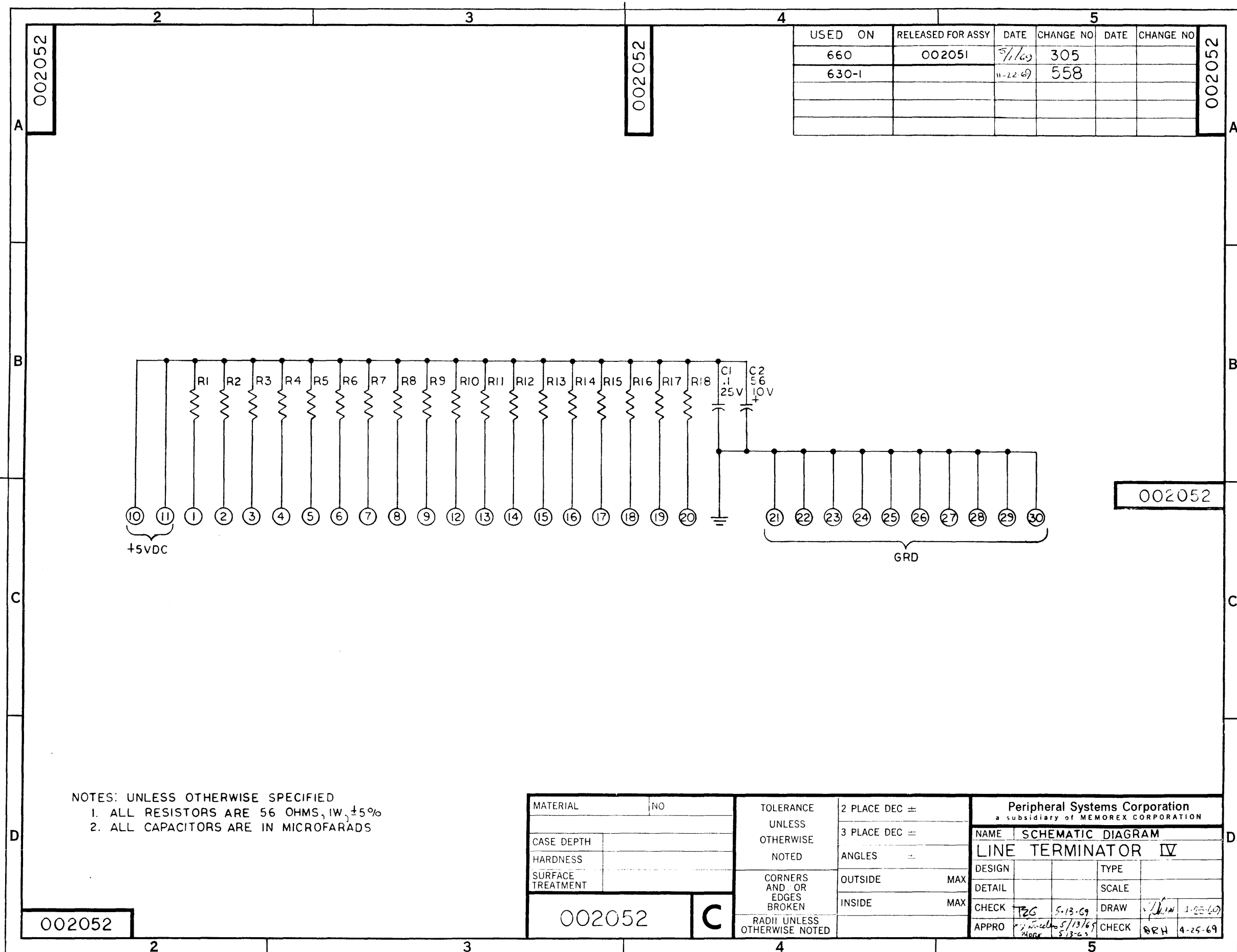
D

201156

USED ON	640-1	RELEASED FOR ASSY	201061	DATE	6/6/69	CHANGE NO	364	DATE		CHANGE NO	
					10-2-69		452				
					11-22-69		537				
					APR 70		845				

201156

D



USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	002051	5/1/69	305		
630-1		11-22-69	558		

NOTES: UNLESS OTHERWISE SPECIFIED  
 1. ALL RESISTORS ARE 56 OHMS, 1W, ±5%  
 2. ALL CAPACITORS ARE IN MICROFARADS

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH		CORNERS AND/OR EDGES BROKEN	3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM	
HARDNESS		RADI UNLESS OTHERWISE NOTED	ANGLES ±	LINE TERMINATOR IV	
SURFACE TREATMENT			OUTSIDE MAX	DESIGN	TYPE
			INSIDE MAX	DETAIL	SCALE
				CHECK	DRAW
				APPRO	CHECK

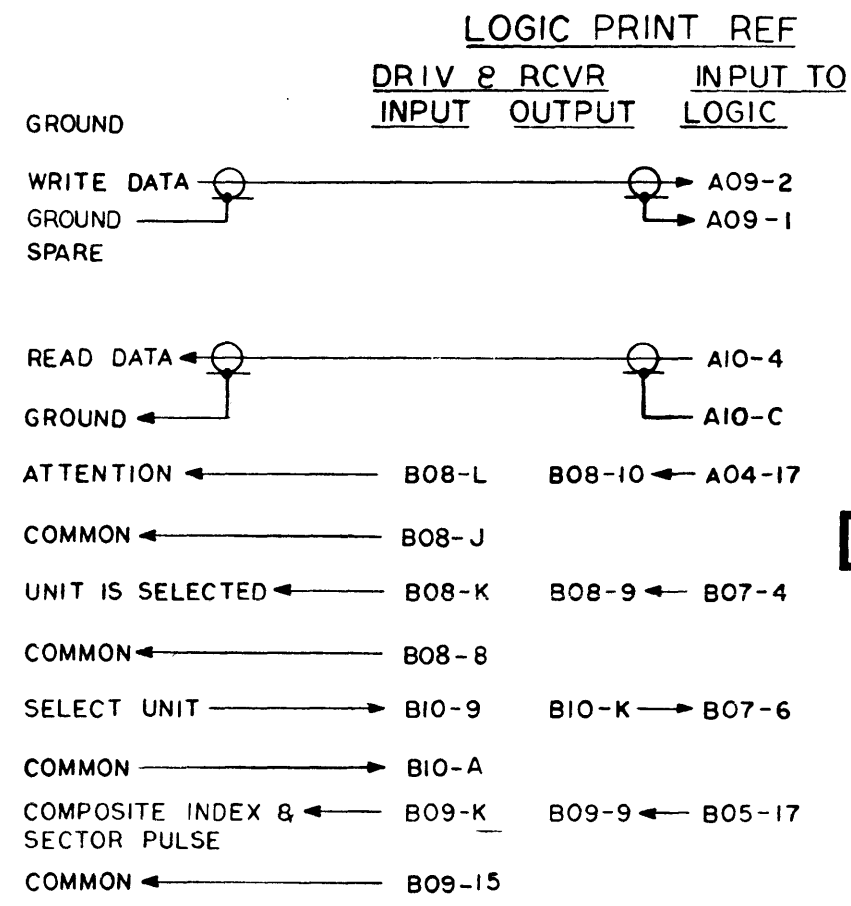
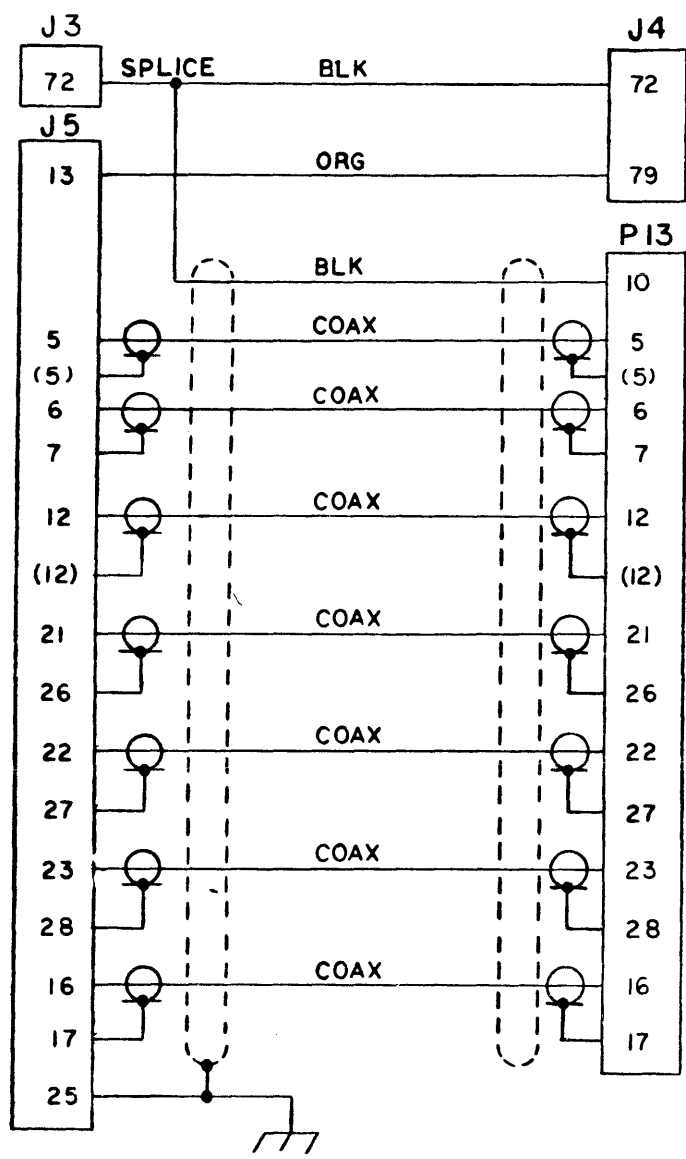
002052

002052

C

002052

USED QN	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660-1	201062	6/6/69	364		
		11-21-69	537		
		APR 9, 70	865		



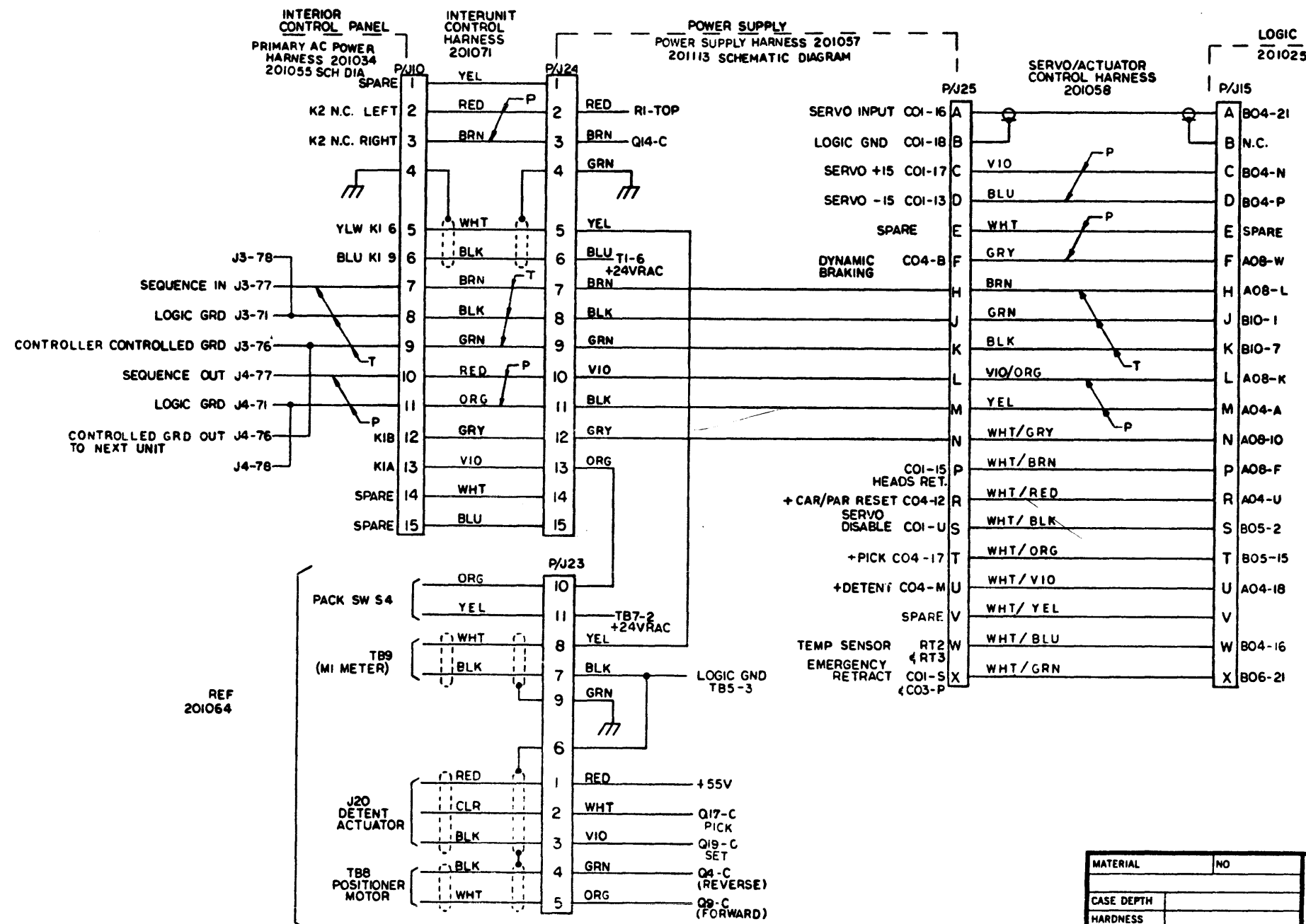
201157

**NOTES:**  
 1. ALL OTHER PINS IN J5 ARE NOT USED INCLUDING PIN G.

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION			
CASE DEPTH			3 PLACE DEC ±				
HARDNESS		CORNERS AND/OR EDGES BROKEN	ANGLES ±	NAME SCHEMATIC DIAGRAM			
SURFACE TREATMENT			OUTSIDE MAX	UNIT INPUT			
		RADI UNLESS OTHERWISE NOTED	INSIDE MAX	DESIGN		TYPE	
				DETAIL		SCALE	
				CHECK		DRAW	JLW 2-4-69
				APPRO		CHECK	Hand 6/6/69

201157

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	MANUAL	6/6/69	364		
		AUG 9 70	865		
		OCT 70	1525		



SERVO/ACTUATOR HARNESS 201076  
201064 SCHEMATIC DIA

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMORE CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME SCHEMATIC DIAGRAM	
HARDNESS			ANGLES ±	INTERUNIT CONTROL	
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
		RADI UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL	SCALE NONE
20112		D		CHECK	DRAW
				APPRO	CHECK

20112

20112

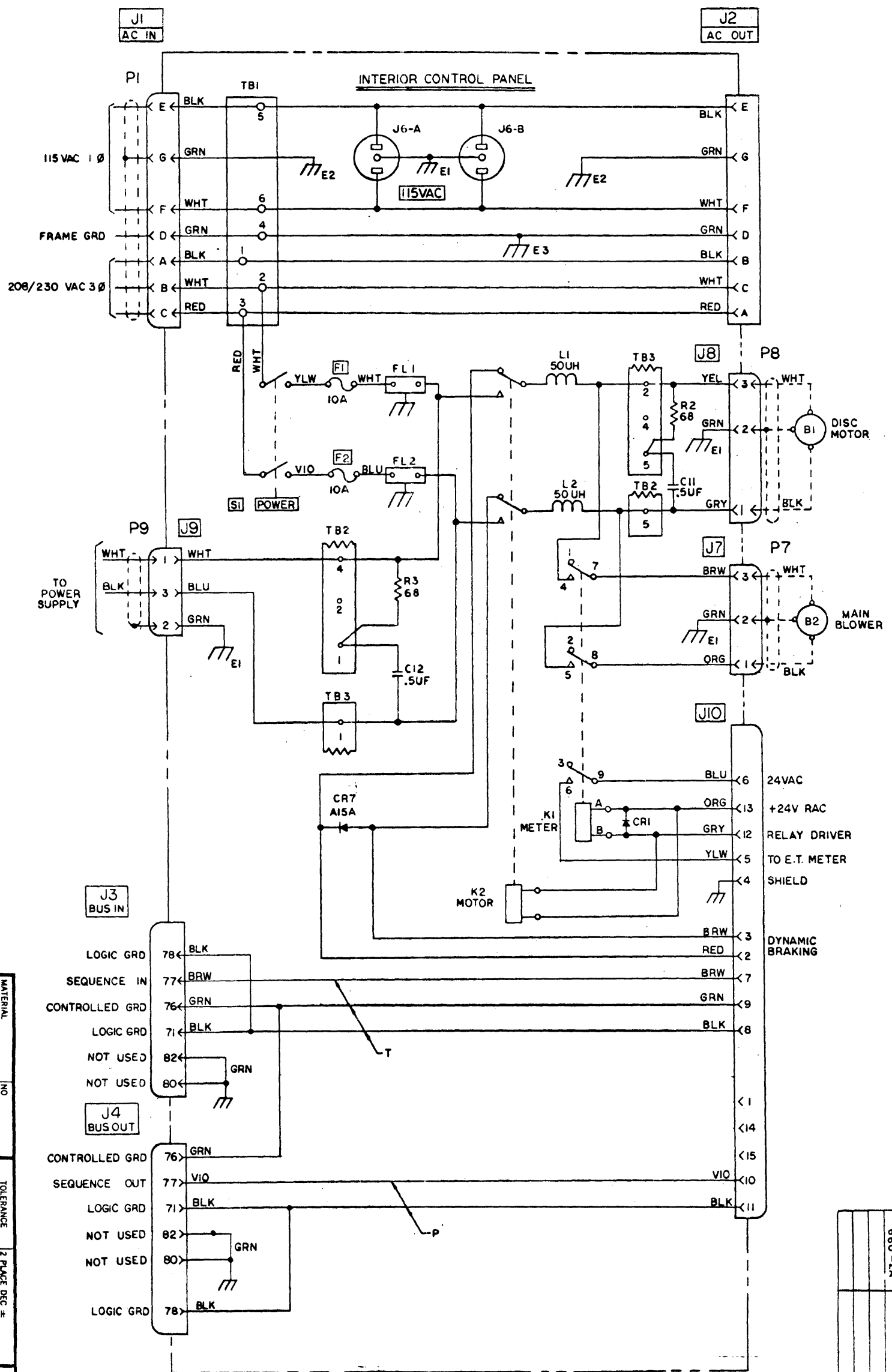
20112

20112

20112

201055

201055



NOTES

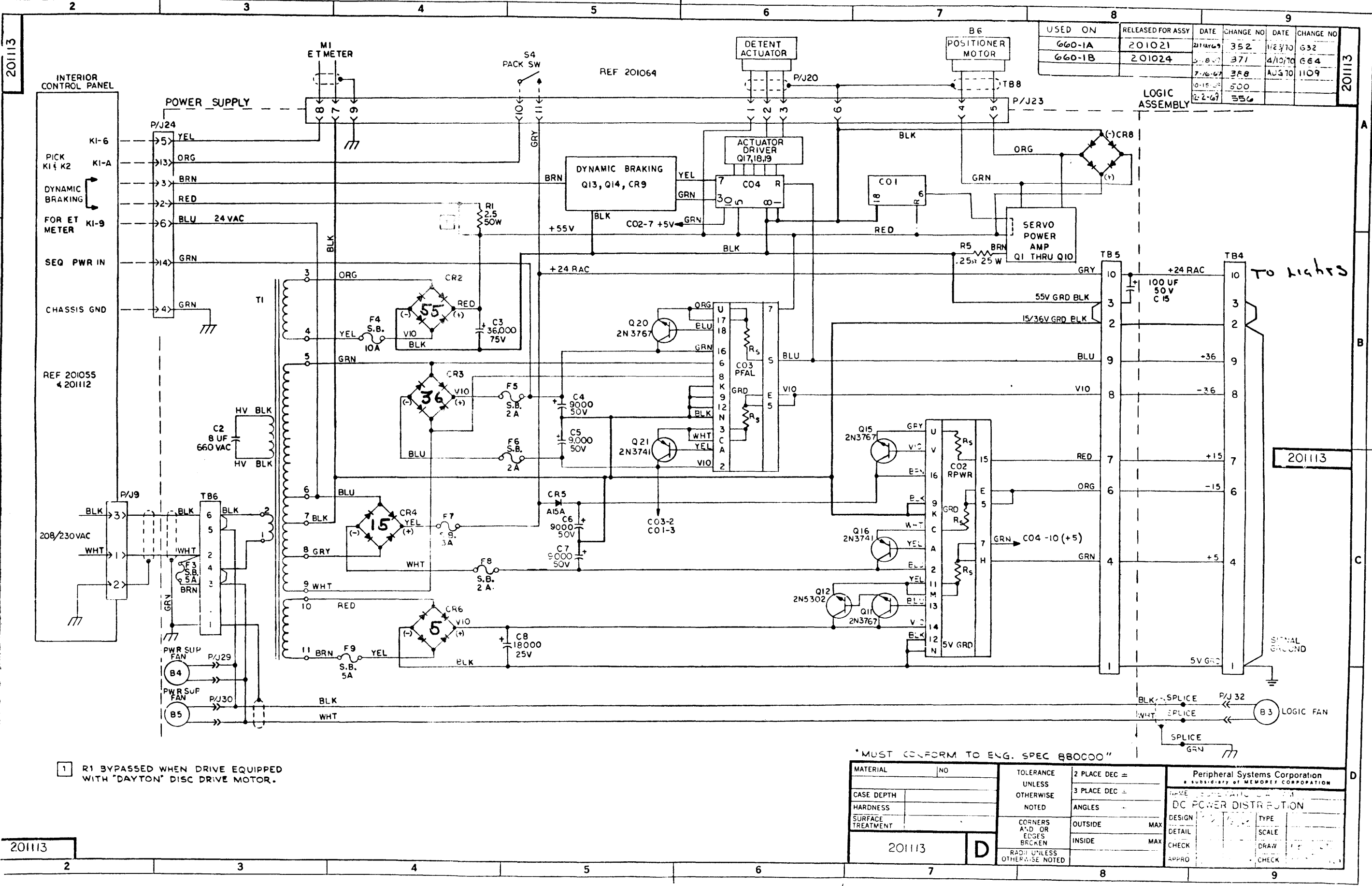
1. REF SCHEMATIC 201945 FOR 50HZ POWER.
2. SEE BUS INPU SCHEMATIC 201156 FOR BALANCE OF J3 J4 CONNECTIONS

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	3 PLACE DEC ±	NAME	DATE	SCALE
CASE DEPTH					Peripheral Systems Corporation		
HARDNESS					SCHEMATIC DIAGRAM		
SURFACE TREATMENT					AC POWER DISTRIBUTION 60 HZ		
					DESIGN	2/24/68	1/16"
					CORNER AND/OR EDGES BROKEN	2/24/68	1/16"
					INSIDE	2/24/68	1/16"
					MAX CHECK	2/24/68	1/16"
					APPRO	2/24/68	1/16"

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660-1A	201034	6-30-67	352		
660-2A		2-8-70	376		
			774		
			1065		

201055

201055



USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660-1A	201021	2/14/69	352	1/23/70	632
660-1B	201024	5-8-69	371	4/10/70	664
		7-16-69	368	AUG 70	1109
		0-15-69	500		
		12-2-69	556		

1 R1 BYPASSED WHEN DRIVE EQUIPPED WITH "DAYTON" DISC DRIVE MOTOR.

\*MUST CONFORM TO ENG. SPEC 880000"

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC =	Peripheral Systems Corporation A SUBSIDIARY OF MEMOREX CORPORATION			
CASE DEPTH			3 PLACE DEC =	DC POWER DISTRIBUTION			
HARDNESS			ANGLES =	DESIGN	TYPE	SCALE	
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	CHECK	SCALE	DRAW	
		RADI UNLESS OTHERWISE NOTED	INSIDE MAX	APPRO		CHECK	
201113		D					

201113

201113

201113

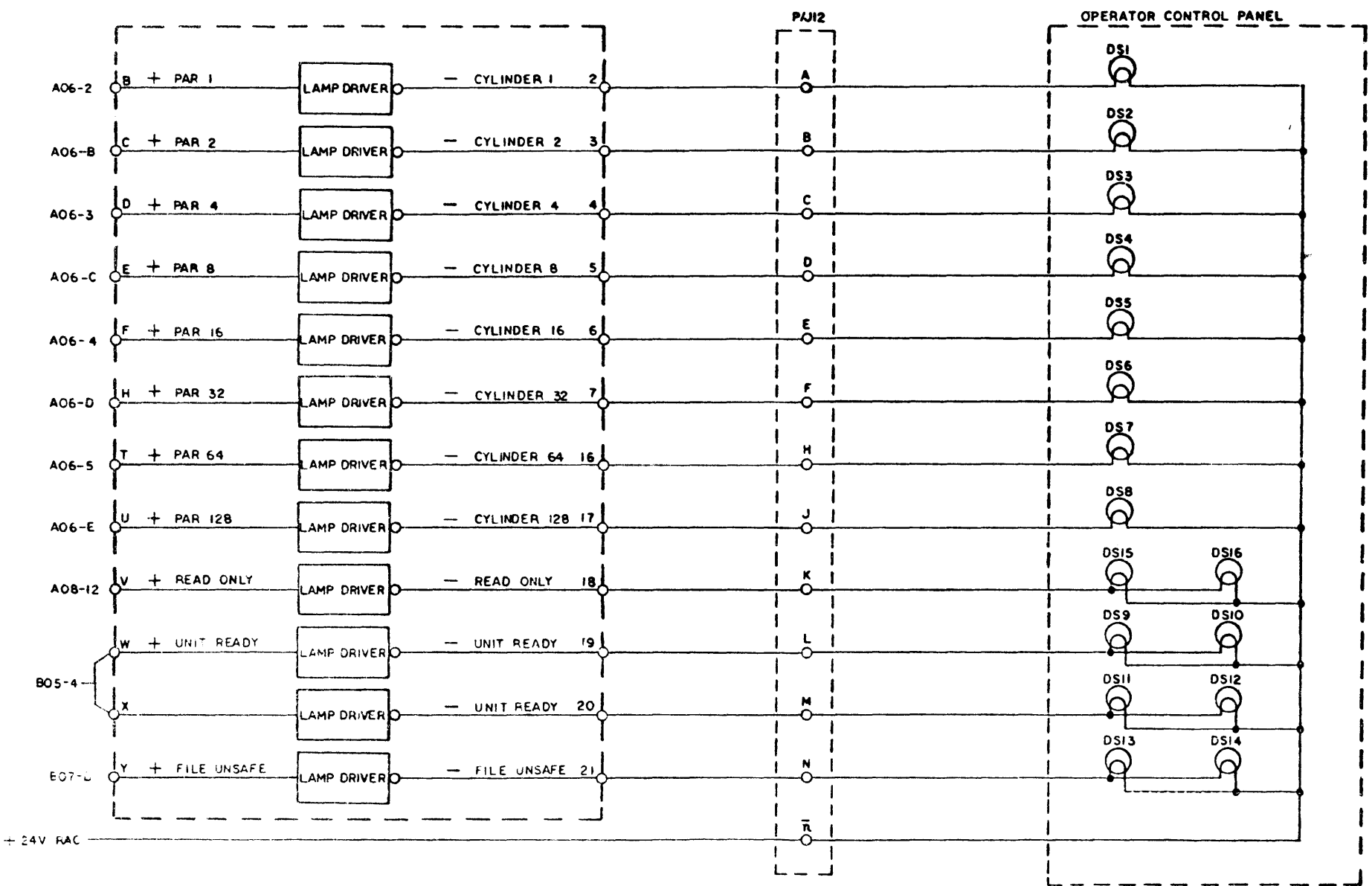
D

8



201327

201327



NOTES: UNLESS OTHERWISE SPECIFIED  
1. ON MACHINES WITH TAMP P.C. BOARD OF EC LEVEL 487 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10 VOLTS ± .04 VOLTS.

A02  
(LDRV)

DATE	CHANGE NO.	DATE	CHANGE NO.	TECHNICAL APPROVAL	MEMOREX EQUIPMENT GROUP
7-29-69	416				NAME SYSTEM LOGIC DIAGRAM
12-2-69	556				LAMP DRIVERS 660-1
APR 9, 70	865				DESIGN
AUG 70	1158				DETAIL
					CHECK
					APPRO

201327

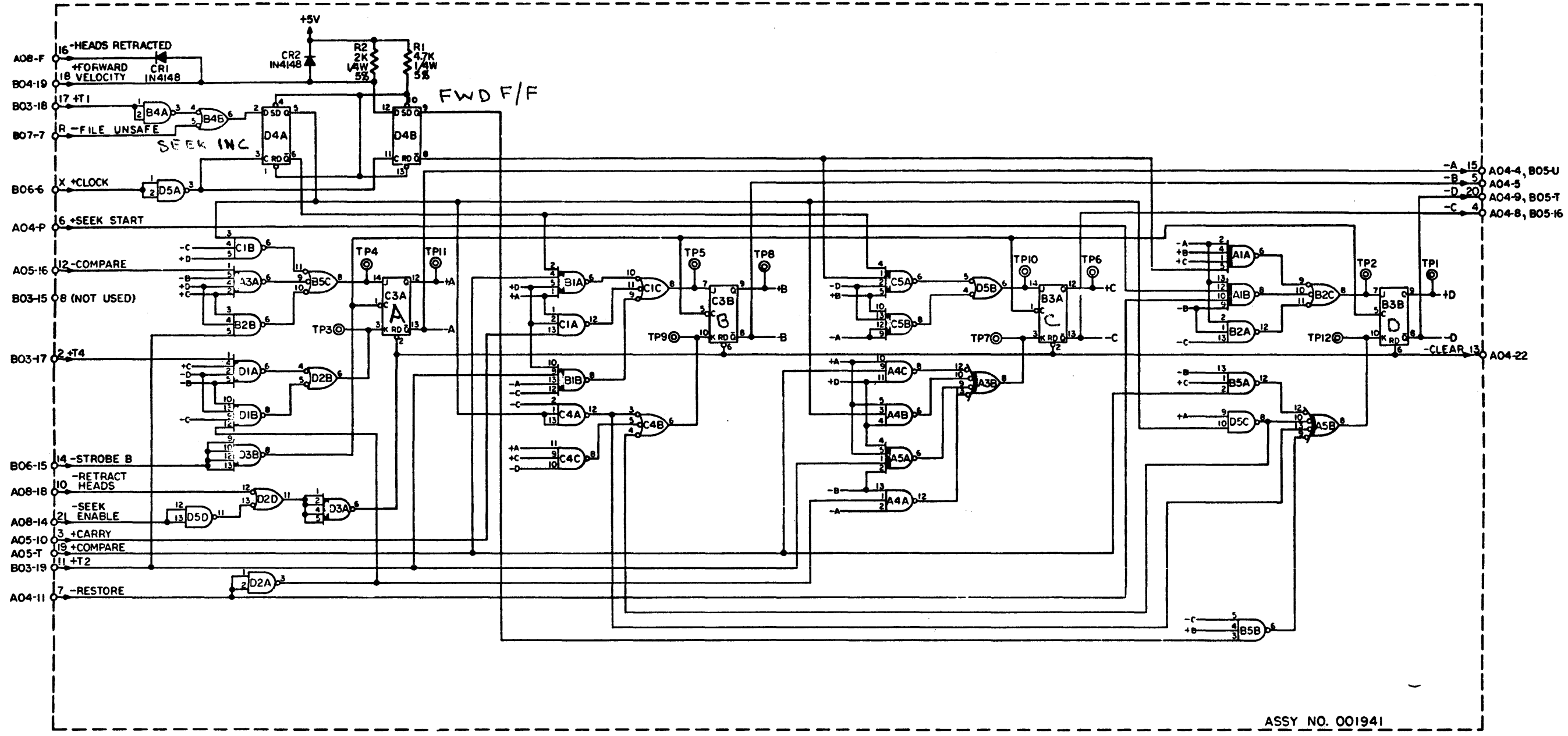
201327

201142

201142

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	MANUAL	4-29-68	319H		
		8-2-69	417		
		7-25-69	429		
		12-11-69	429C		
		UN91	846		

201142



ASSY NO. 001941

NOTES:

1. IC'S B3 & C3 ARE SN7473N, DUAL JK FLIP-FLOP.
2. IC D4 IS A SN7474N, DUAL D-TYPE FLIP-FLOP.
3. FOR MACHINES WITH TAMP P.C. BOARD AT EC LEVEL 487 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS + 5.10 V

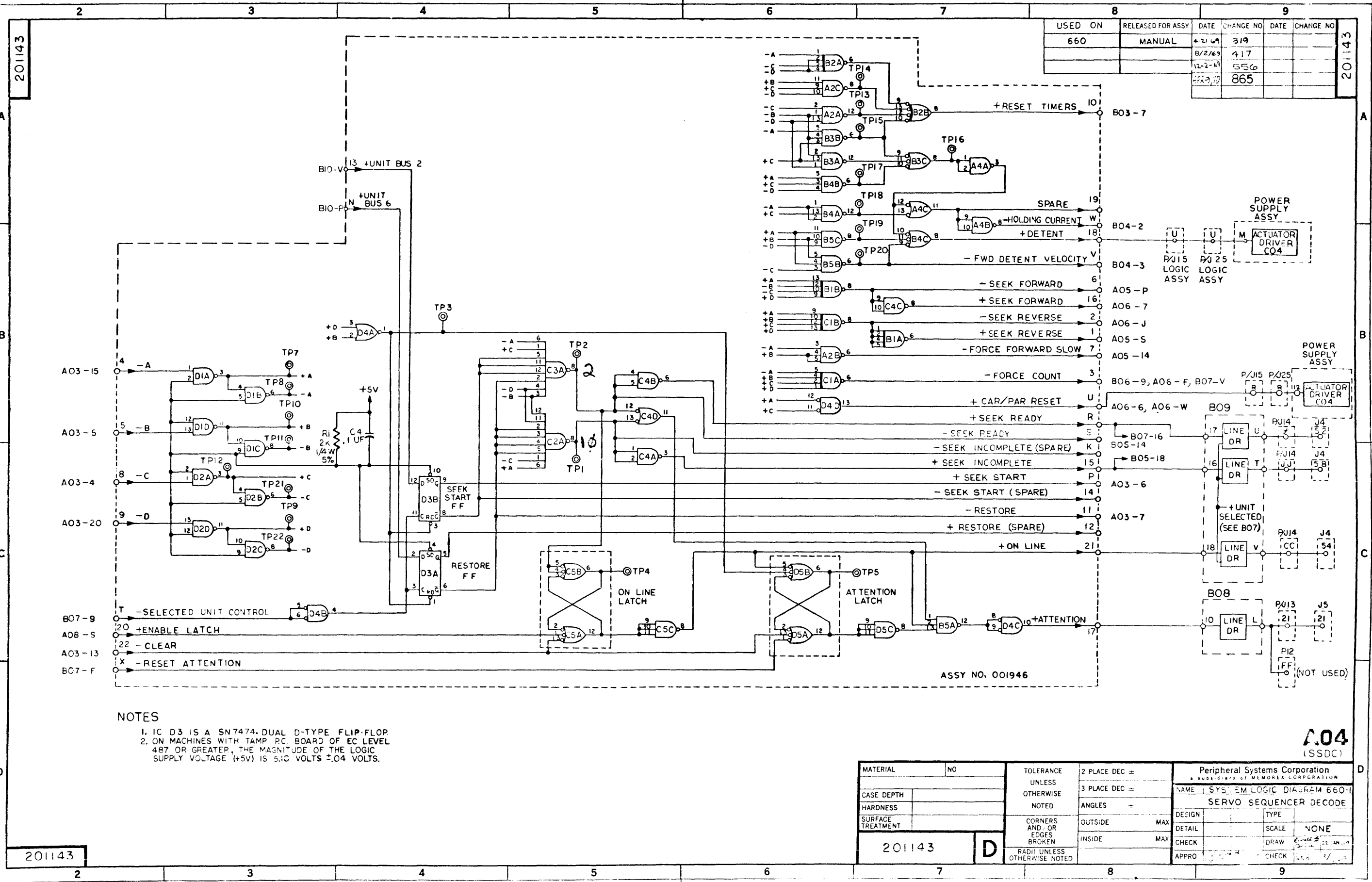
201142

A03 (SSEQ)

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH		NOTED	3 PLACE DEC ±	NAME SYSTEM LOGIC DIAGRAM 660-1	
HARDNESS			ANGLES ±	SERVO SEQUENCER	
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
		RADI UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL	SCALE NONE
				CHECK	DRAW
				APPRO	CHECK

201142

10



USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	MANUAL	4-21-69	319		
		8/2/69	417		
		12-2-69	556		
		11-27-70	865		

**NOTES**

- IC D3 IS A SN7474-DUAL D-TYPE FLIP-FLOP
- ON MACHINES WITH TAMP PC BOARD OF EC LEVEL 487 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10 VOLTS ±.04 VOLTS.

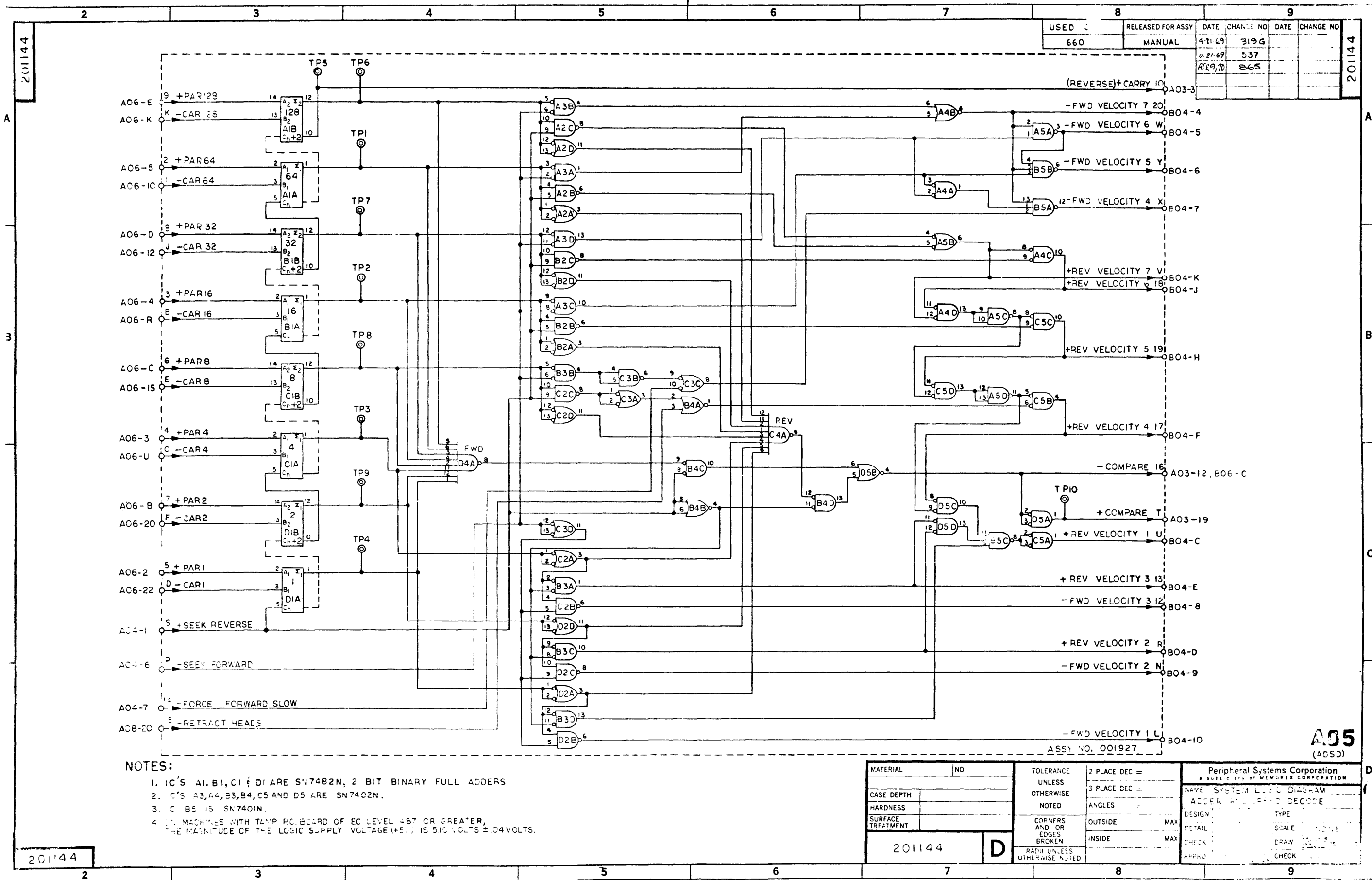
**A04**  
(SSDC)

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	3 PLACE DEC ±	ANGLES ±	Peripheral Systems Corporation A SUBSIDIARY OF MEMOREX CORPORATION		
CASE DEPTH						NAME: SYS EM LOGIC DIAGRAM 660-1		
HARDNESS						SERVO SEQUENCER DECODE		
SURFACE TREATMENT						DESIGN	TYPE	
						DETAIL	SCALE	NONE
						CHECK	DRAW	
						APPRO	CHECK	

201143 D

201143

201143



USED	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	MANUAL	4-11-69	319 G		
		11-21-69	537		
		11-19-70	865		

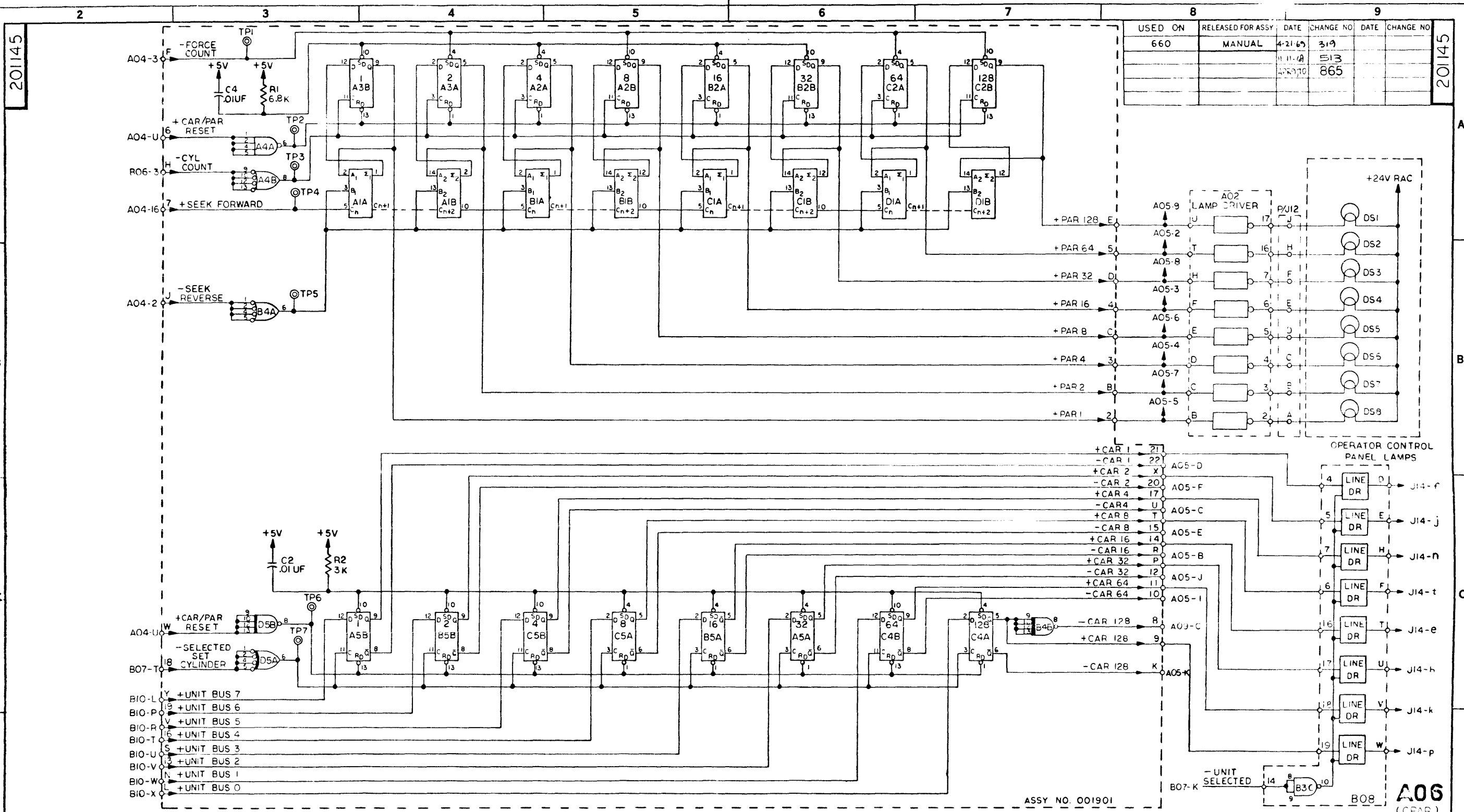
- NOTES:
- IC'S A1, B1, C1 & D1 ARE SN7482N, 2 BIT BINARY FULL ADDERS
  - IC'S A3, A4, B3, B4, C5 AND D5 ARE SN7402N.
  - C & B5 IS SN7401N.
  - ON MACHINES WITH TAMP PC BOARD OF EC LEVEL 487 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5.1) IS 510 VOLTS ±.04 VOLTS.

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC =	Peripheral Systems Corporation A SUBSIDIARY OF MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC =	NAME SYSTEM LOGIC DIAGRAM	
HARDNESS			ANGLES =	ADDER AND DECODE	
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
		RADI UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL	SCALE
201144	D			CHECK	DRAW
				APPROV	CHECK

201144

A05  
(A050)

12



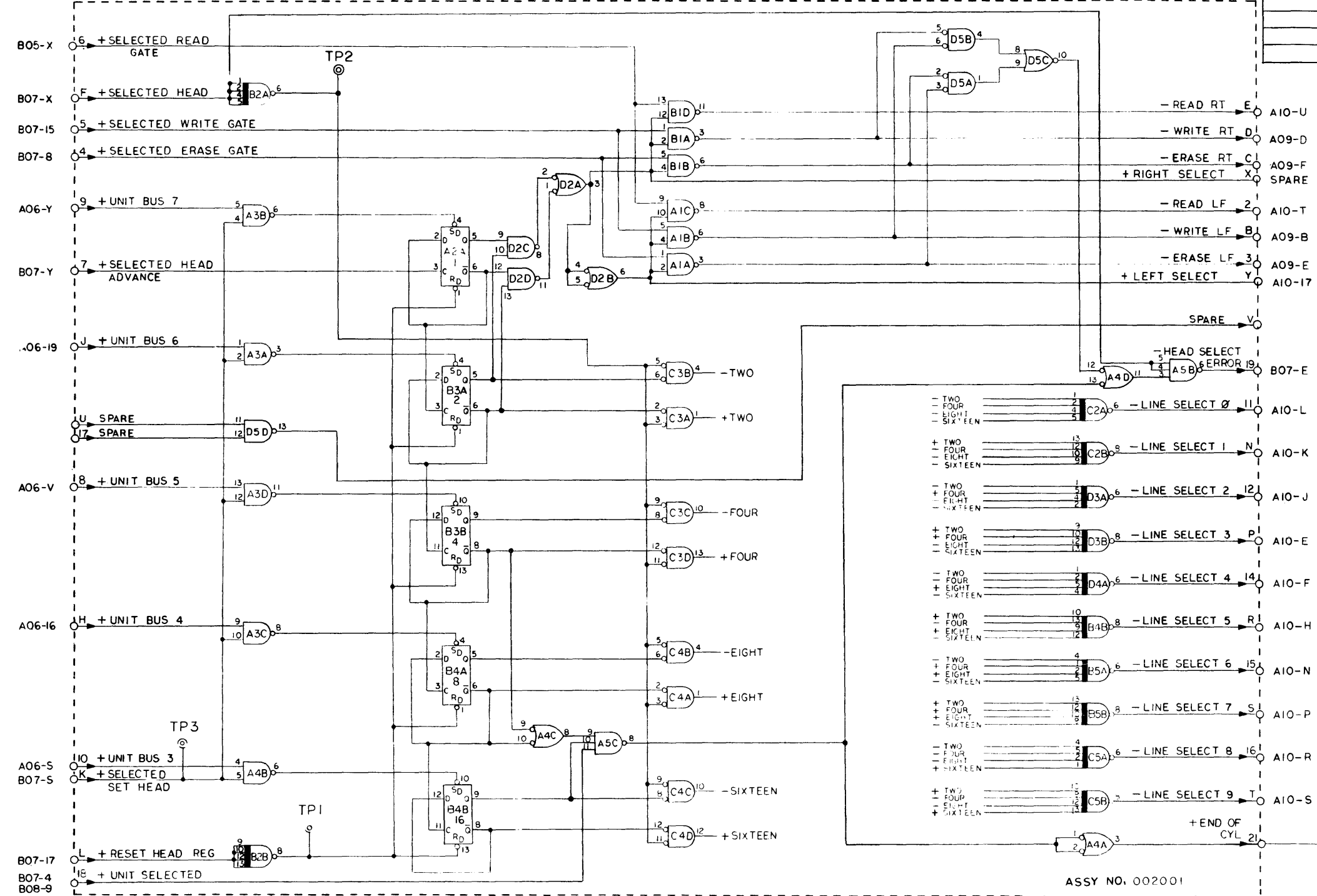
USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	MANUAL	4-21-69	319		
		11-11-68	513		
		12-30-70	865		

- NOTES**
- IC'S A1, B1, C1 & D1 ARE SN7482N, 2 BIT BINARY FULL ADDERS
  - IC'S A2, A3, A5, B2, B5, C2, C4 & C5 ARE SN7474N, DUAL D-TYPE FLIP-FLOPS
  - ON MACHINES WITH TAMP PC BOARD OF EC LEVEL 487 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 510 VOLTS ±.04 VOLTS

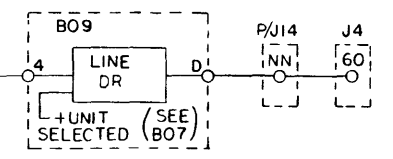
MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation A SUBSIDIARY OF MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME SYSTEM LOGIC CIRCUIT M. 660-1	
HARDNESS			ANGLES ±	CYLINDER PRESENT ADDRESS REG.	
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
		RADIUS UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL	SCALE
201145				CHKD	DRAW
				APPRO	CHECK

201145

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660-1	MANUAL	4-21-69	319		
		4-22-69	321		
		5-13-69	323		



- NOTES:
- IC'S A2, B3 & B4 ARE SN7474N, DUAL D FLIP-FLOP.
  - IC D5 IS A SN7402N QUADRUPLE 2-INPUT NOR GATE.



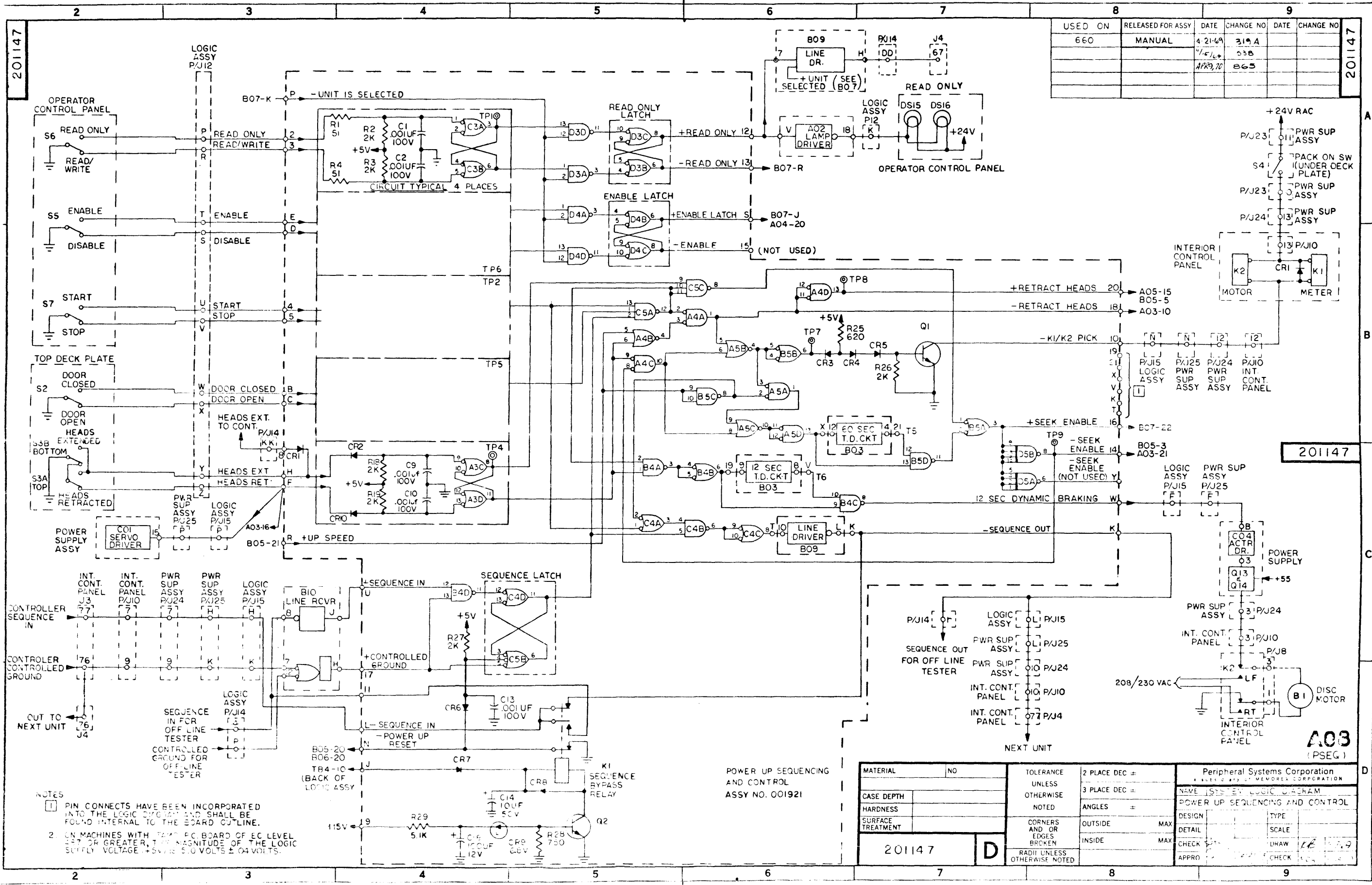
MATERIAL NO		TOLERANCE UNLESS OTHERWISE NOTED		Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
CASE DEPTH		2 PLACE DEC ±		NAME SYSTEM LOGIC DIAGRAM 660-1	
HARDNESS		3 PLACE DEC ±		HEAD SELECTION AND REGISTER	
SURFACE TREATMENT		ANGLES		DESIGN	TYPE
		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DETAIL	SCALE NONE
		RADII UNLESS OTHERWISE NOTED	INSIDE MAX	CHECK	DRAW
201146	D			APPRO	CHECK

201146

201146

A07  
(HREG)

14



USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	MANUAL	4-21-69	31A		
		1/1/70	33B		
		APR 9, 70	665		

201147

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	3 PLACE DEC ±	ANGLES ±	Peripheral Systems Corporation A SUBSIDIARY OF MEMOREX CORPORATION	
CASE DEPTH						NAME: SYSTEM LOGIC DIAGRAM	
HARDNESS						POWER UP SEQUENCING AND CONTROL	
SURFACE TREATMENT		CORNERS AND OR EDGES BROKEN	OUTSIDE MAX	INSIDE MAX		DESIGN	TYPE
	201147	RADII UNLESS OTHERWISE NOTED				DETAIL	SCALE
						CHECK	DRAW
						APPRO	CHECK

NOTES  
 1. PIN CONNECTS HAVE BEEN INCORPORATED INTO THE LOGIC DIAGRAM AND SHALL BE FOUND INTERNAL TO THE BOARD OUTLINE.  
 2. ON MACHINES WITH 7540 PC BOARD OF EC LEVEL 337 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE +5V IS 5.0 VOLTS ± 0.4 VOLTS.

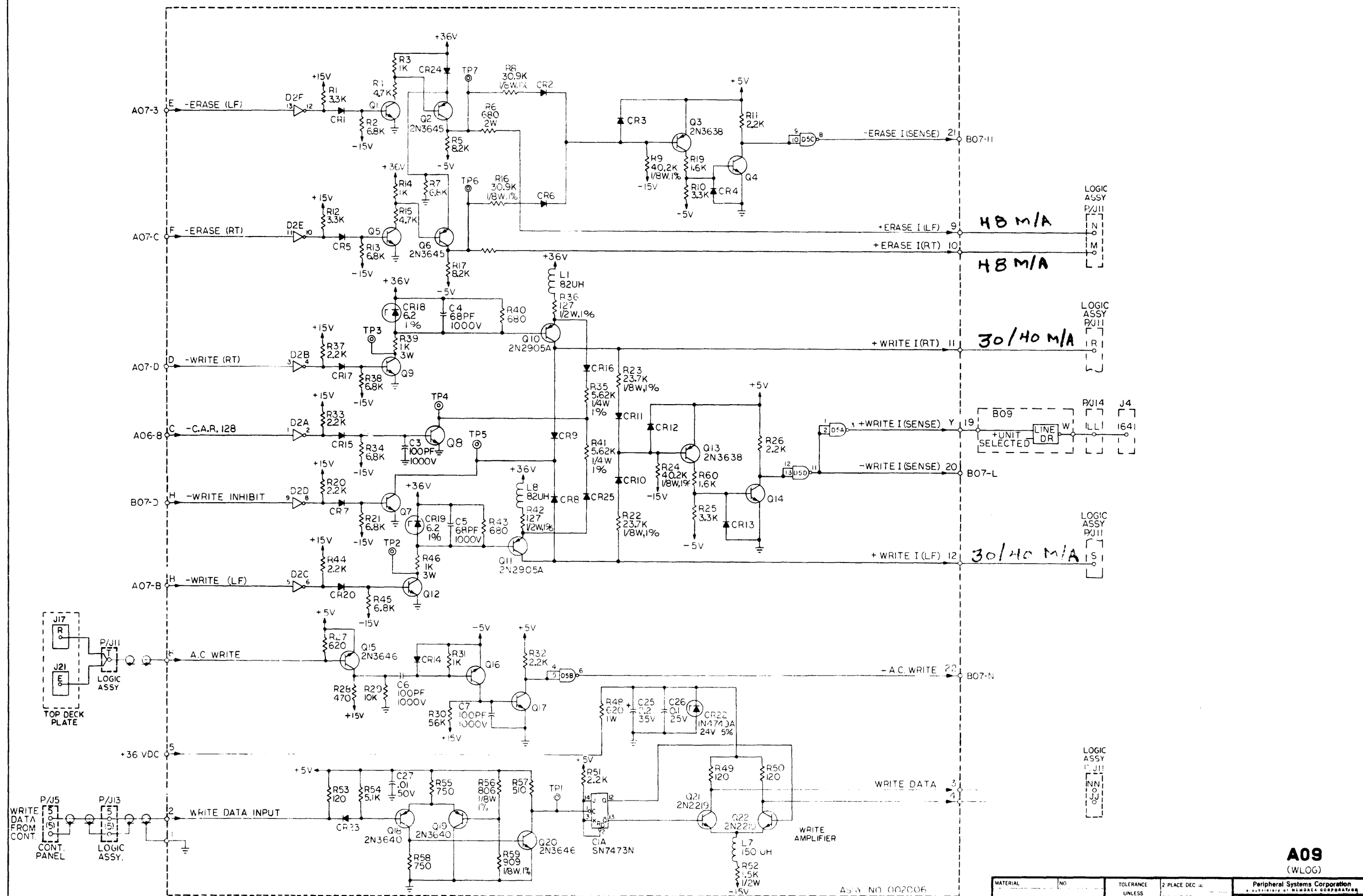
POWER UP SEQUENCING AND CONTROL  
 ASSY NO. 001921

A08  
 (PSEG)

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO.	DATE	CHANGE NO.
660-1	MANUAL	12-11-66	315		
		12-11-66	416		

201148

201148



NOTES: UNLESS OTHERWISE SPECIFIED  
 I C D2 IS A MC835P HEX INVERTER

ASSY NO 002006

**A09**  
(WLOG)

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC	Peripheral Systems Corporation
CASE DEPTH			3 PLACE DEC	PERIPHERAL SYSTEMS CORPORATION
HARDNESS			ANGLES	NAME SYSTEM LOGIC HARDWARE
SURFACE TREATMENT				WRITE LOGIC
				DESIGN TYPE
				DETAIL SCALE
				CHECK
				APPRO

201148

201148

E

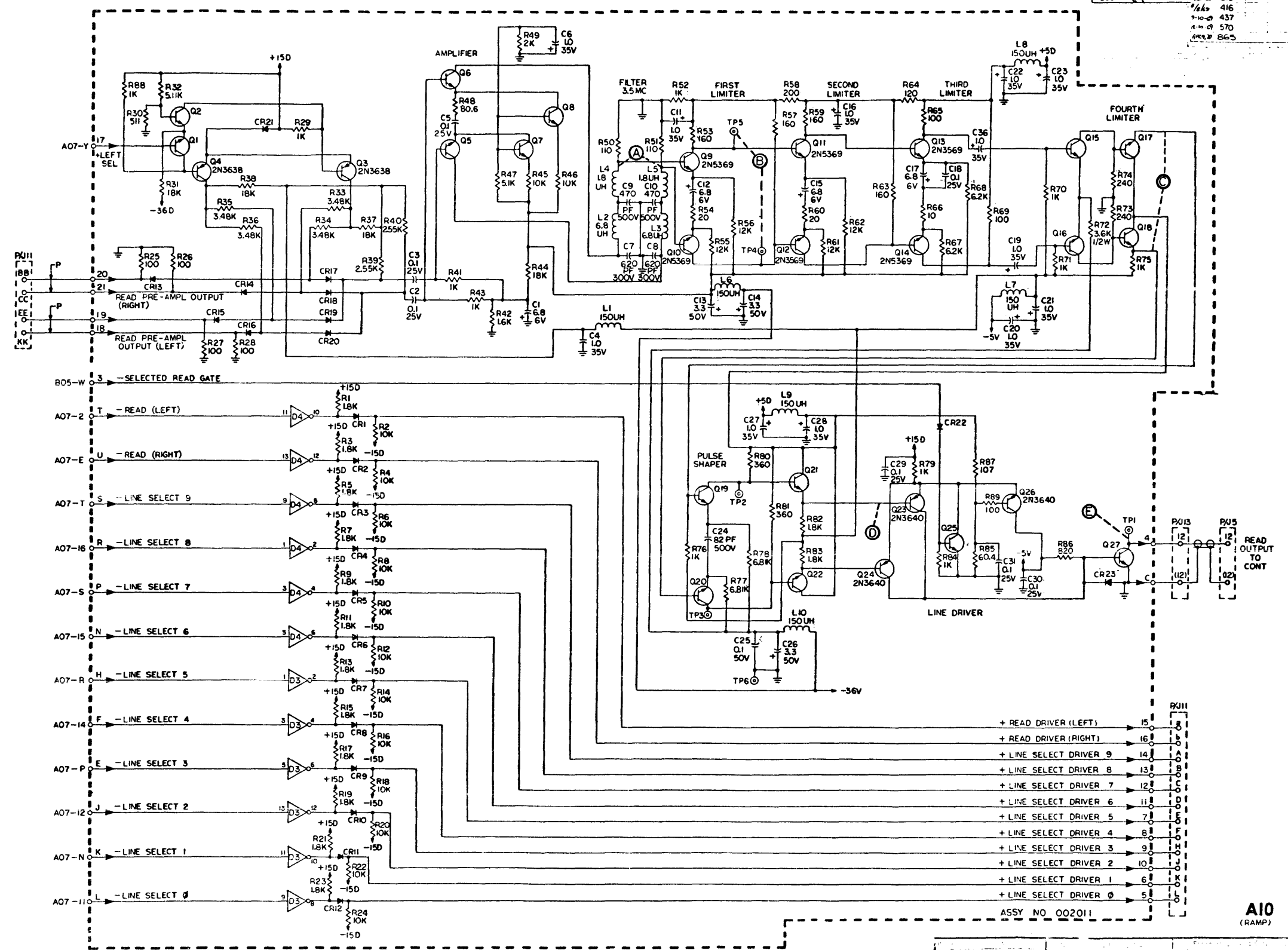
16



201164

USED ON	MANUAL	319
660		416
		437
		570
		865

201164

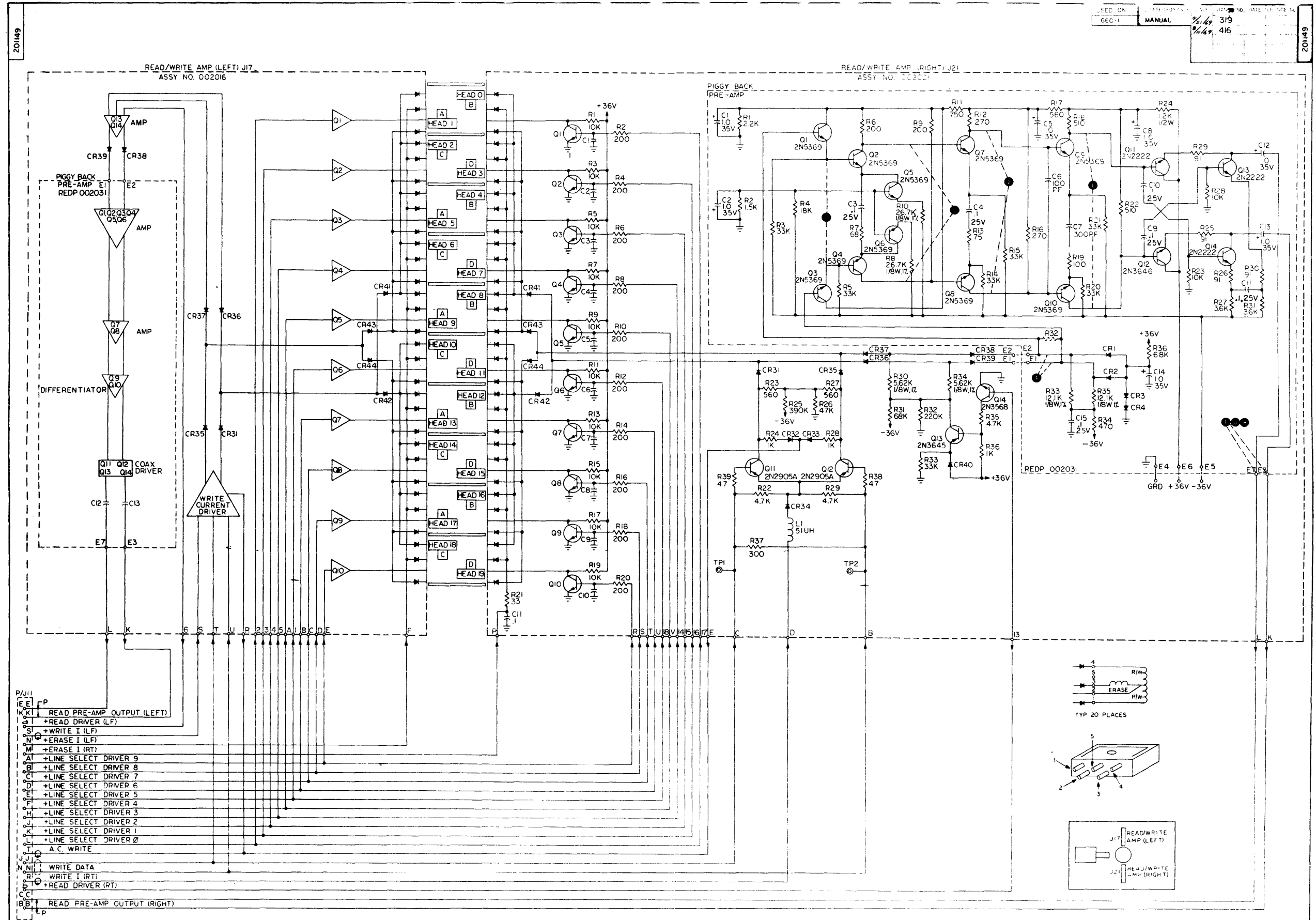


NOTES  
 1. ON MACHINES WITH TAMP PC BOARD OF PC LEVEL 4E7 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (#5V) IS 5.10 VOLTS ± 0.4 VOLTS.

201164	ASSY NO 002011	A10 (RAMP)
SYSTEM LOGIC DIAGRAM 6604		READ AMPLIFIER

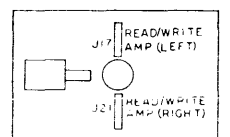
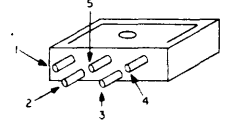
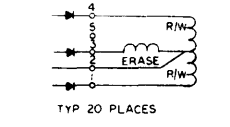
201164

17

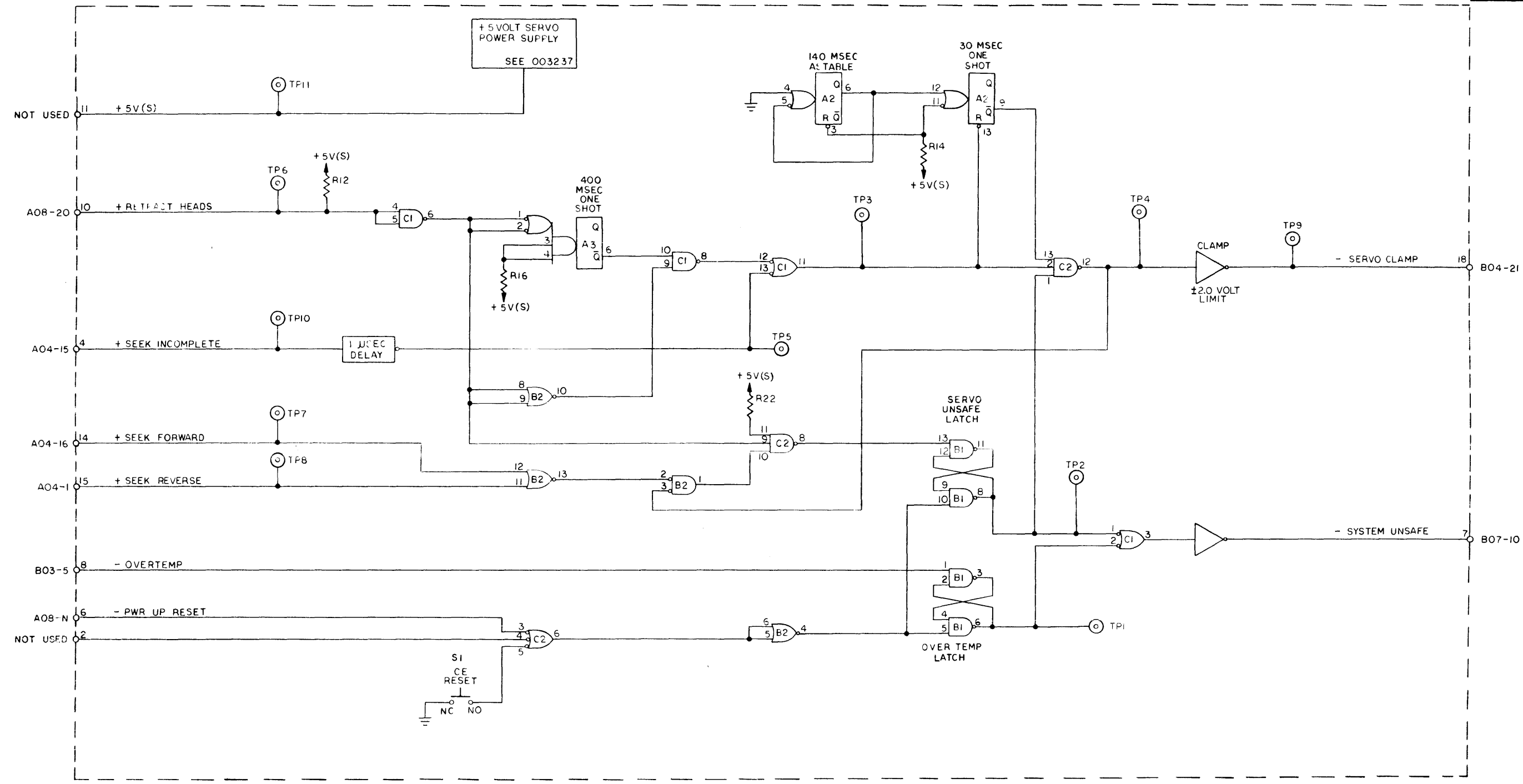


- P/J11  
 E/E1 P  
 K/K1 READ PRE-AMP OUTPUT (LEFT)  
 G1 +READ DRIVER (LF)  
 S1 +WRITE I (LF)  
 N1 +ERASE I (LF)  
 M1 +ERASE I (RT)  
 A1 +LINE SELECT DRIVER 9  
 B1 +LINE SELECT DRIVER 8  
 C1 +LINE SELECT DRIVER 7  
 D1 +LINE SELECT DRIVER 6  
 E1 +LINE SELECT DRIVER 5  
 F1 +LINE SELECT DRIVER 4  
 H1 +LINE SELECT DRIVER 3  
 J1 +LINE SELECT DRIVER 2  
 K1 +LINE SELECT DRIVER 1  
 L1 +LINE SELECT DRIVER 0  
 T1 A.C. WRITE  
 N/N1 WRITE DATA  
 R/R1 WRITE I (RT)  
 S/S1 +READ DRIVER (RT)  
 C/C1  
 B/B1 READ PRE-AMP OUTPUT (RIGHT)  
 L/L1 P

- NOTES: UNLESS OTHERWISE SPECIFIED.
1. TRANSISTORS Q1 THRU Q10 ARE 2N3568
  2. ALL CAPACITORS ARE IN MICROFARADS.
  3. CAPACITORS C1 THRU C10 ARE .001MF, 1000V, ±10%.
  4. LEFT AND RIGHT AMPLIFIERS HAVE IDENTICAL CIRCUITS. LEFT IS SHOWN LOGICALLY, RIGHT IS SHOWN IN FULL SCHEMATIC.



201149	E	Peripheral Systems Corporation SYSTEM LOGIC DIAGRAM 660-1 READ/WRITE AMP LEFT & RIGHT
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BO 2

201776

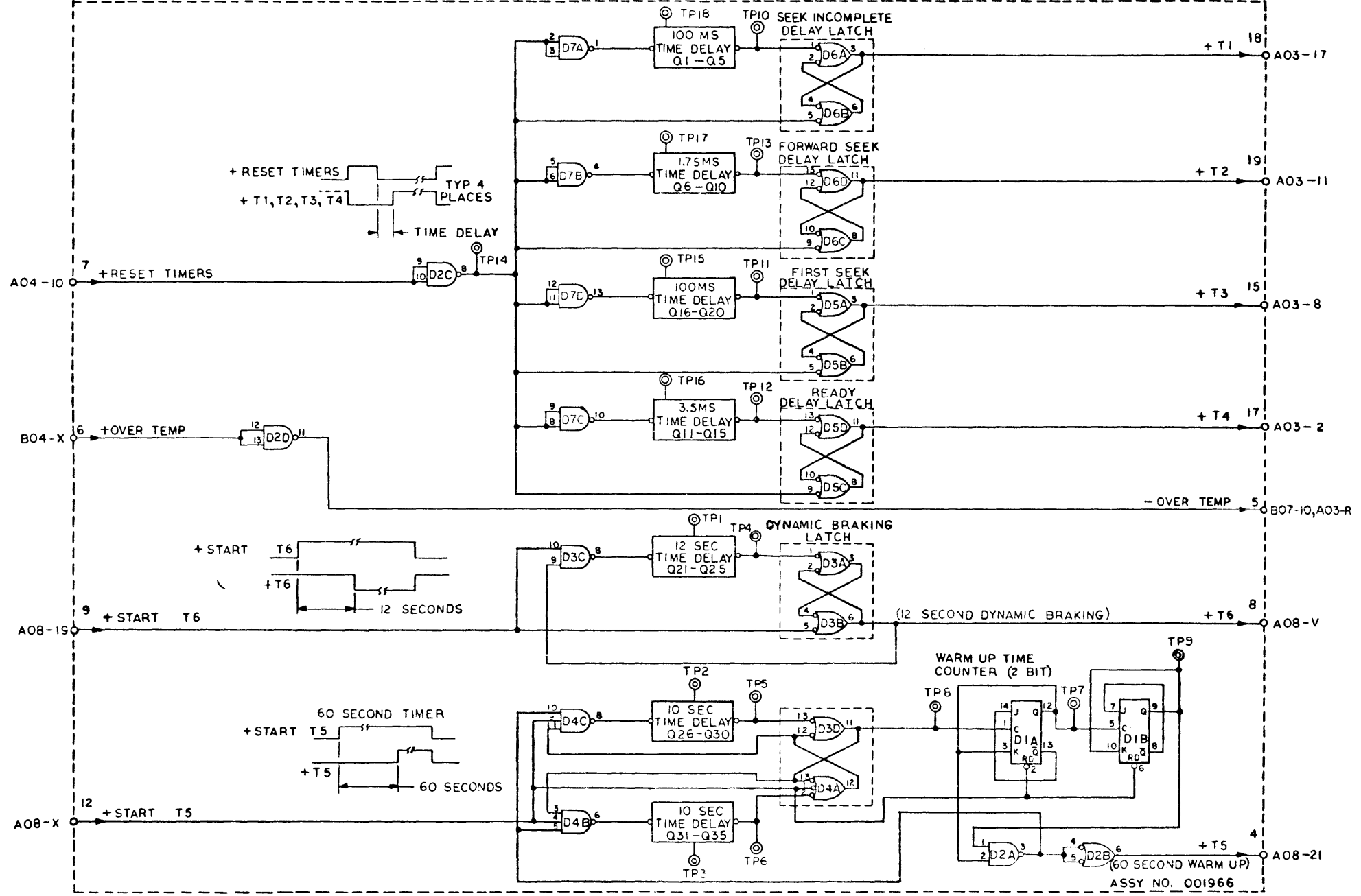
D

DATE	CHANGE NO.	DATE	CHANGE NO.	TECHNICAL APPROVAL	MEMOREX EQUIPMENT GROUP
JULY 70	1268				NAME: SYSTEM LOGIC DIAGRAM SYSTEM PROTECTION
					DESIGN: DMYERS JULY 24, 70
					CHECK: [Signature] JUL 31, 70
					APPRO: [Signature] JUL 31, 70

201776

19

201150	2	3	4	5	6	7	8	9	201150
	USED ON		RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO		
	660		MANUAL	4-21-69	319				
				6-19-69	366				
			10-23-69	481					
			APR 9, 70	865					



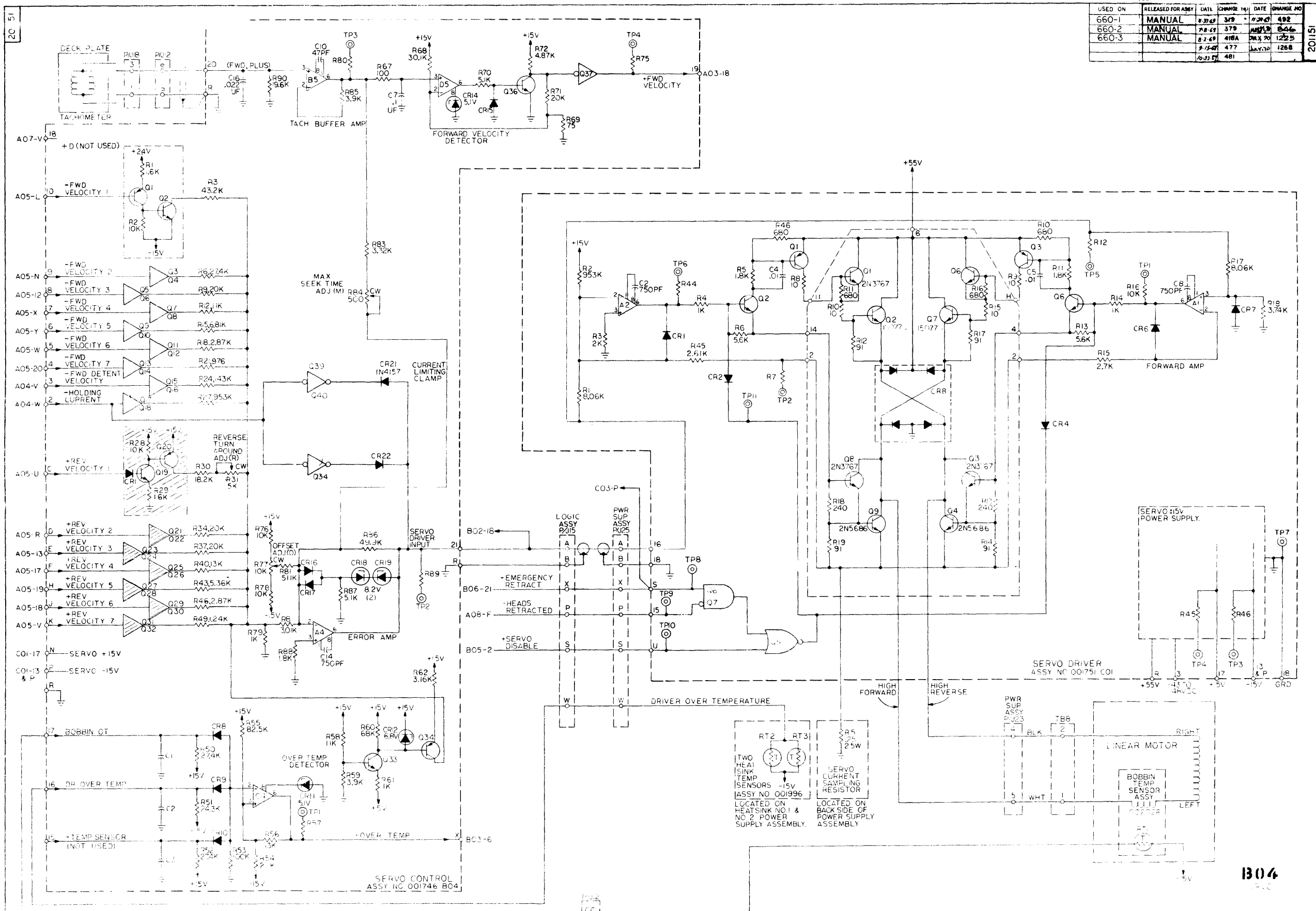
- NOTES:
- IC D1 IS A SN7473, DUAL J-K FLIP-FLOP
  - ON MACHINES WITH TAMP PC BOARD OF EC LEVEL 4:7 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10 VOLTS ± .04 VOLTS.

**D03**  
(DELAY)

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation A SUBSIDIARY OF MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME SYSTEM LOGIC DIAGRAM 660-1	
HARDNESS			ANGLES =	DELAY TIMERS	
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
	201150	RADI UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL	SCALE NONE
	D			CHECK	DRAW 25 JAN 69
				APPRO	CHECK 1/27/69

201150

USED ON	RELEASED FOR ASBY	DATE	CHANGE NO	DATE	CHANGE NO
660-1	MANUAL	8-31-69	379	8-31-69	492
660-2	MANUAL	8-31-69	379	8-31-69	492
660-3	MANUAL	8-31-69	418A	8-31-69	1225
		8-15-69	477	8-15-69	1268
		10-21-57	481		



NOTES: UNLESS OTHERWISE SPECIFIED:  
 1. FITTING DIMENSIONS WITH TYPICAL BOARD AT EC LEVEL 4-7. R GREATER, THE  
 MAXIMUM OF THE TYPICAL SUPPLY VOLTAGE (15V) IS 15.10 TO 0.04 VOLTS.

MATERIAL		TOLERANCE		PERIPHERAL SYSTEMS CORPORATION	
NO		UNLESS OTHERWISE NOTED		2 PLACE DEC.	3 PLACE DEC.
CASE DEPTH				DESIGN	TYPE
HARDNESS				CORNERS AND OR LOGS	SCALE
SURFACE TREATMENT				INSIDE	MAX
20151	E	RADI UNLESS OTHERWISE NOTED		CHECK	SCALE NONE
APPRO		DATE		DRAW	
APPRO		DATE		DRAW	

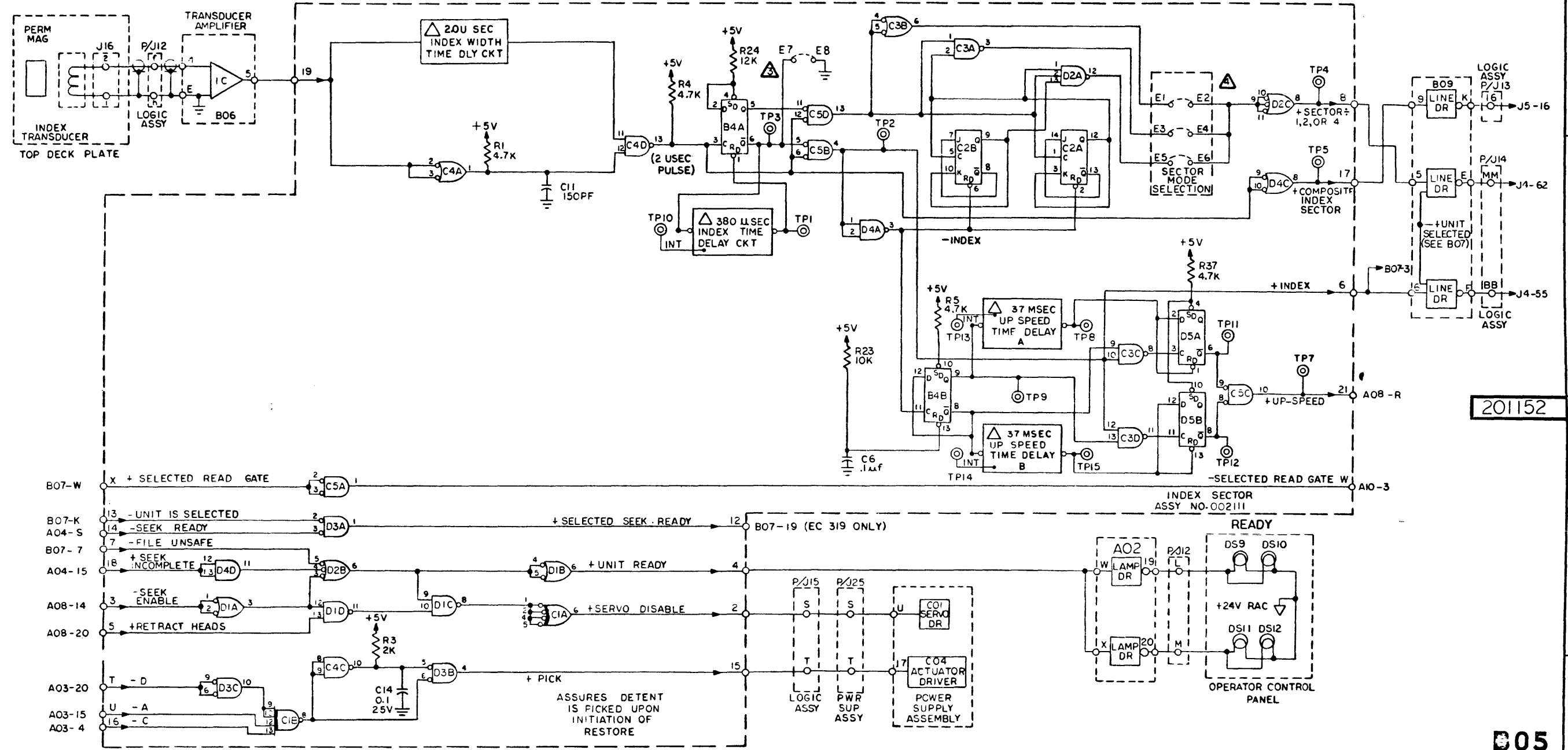
21

201152

201152

201152

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660-1	MANUAL	4-21-69	319	APR 29, 70	865
660-2		5-11-69	320		
		8-19-69	320C		
		10-15-69	468		
		11-14-69	468A		



201152

05 (1 X SR)

- NOTES: UNLESS OTHERWISE SPECIFIED
- IC'S B4 & D5 ARE SN7474N, DUAL D FLIP-FLOP
  - IC C2 IS A SN7473N, DUAL J-K FLIP-FLOP FOR STANDARD INDEX ONLY MODE OF OPERATION. INSERT JUMPER TO GRD. FOR INDEX-SECTOR MODE LEAVE OPEN
  - CUSTOMER OPTION:  
JUMPER E1 TO E2 FOR SECTOR +1 OPERATION  
JUMPER E3 TO E4 FOR SECTOR +2 OPERATION  
JUMPER E5 TO E6 FOR SECTOR +4 OPERATION
  - IC C4 IS A SN7401N OPEN COLLECTOR GATE
  - IC'S D3 & C5 ARE SN7402N, 2-INPUT NOR GATE
  - ON MACHINES WITH TAMP. P.C. BOARD OF EC LEVEL 487 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10 VOLTS ± .04 VOLTS.

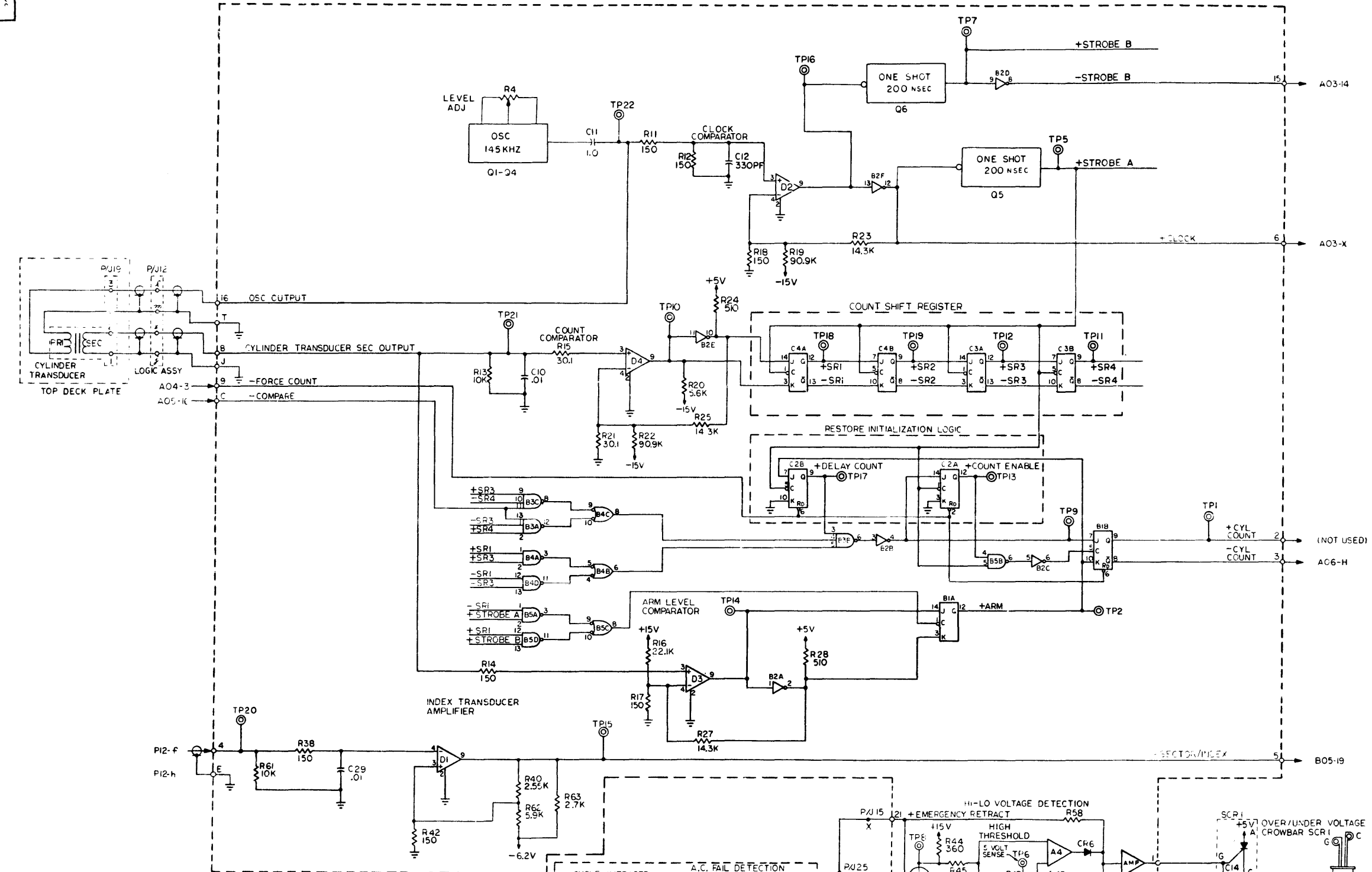
MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	3 PLACE DEC ±	ANGLES ±	OUTSIDE MAX	INSIDE MAX	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION		
CASE DEPTH								DESIGN		TYPE
HARDNESS								DETAIL		SCALE
SURFACE TREATMENT								CHECK		DRAW
201152		D						APPRO		CHECK

201152

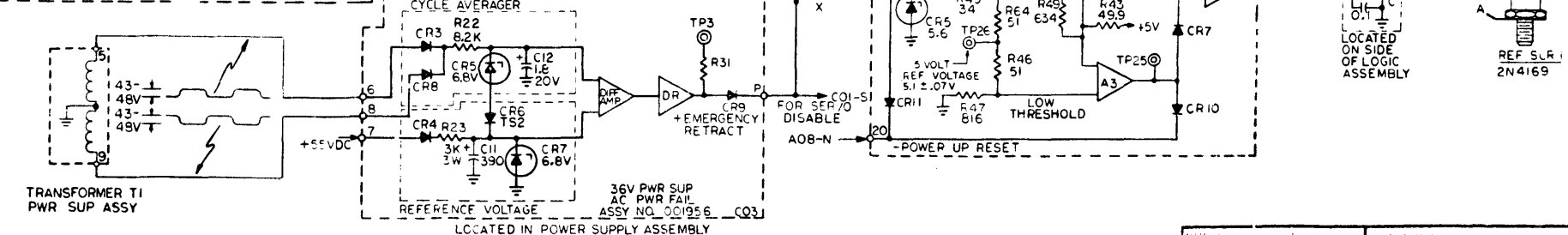
22

66	MA	42	319	1089
		6-13-69	363	
		7-31-69	411	
		10-1-69	451	
		1-1-70	497	

201153



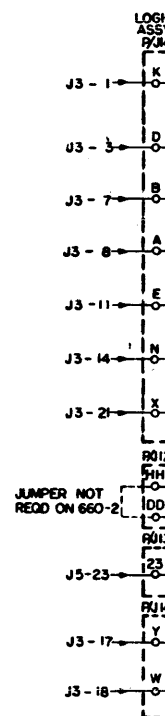
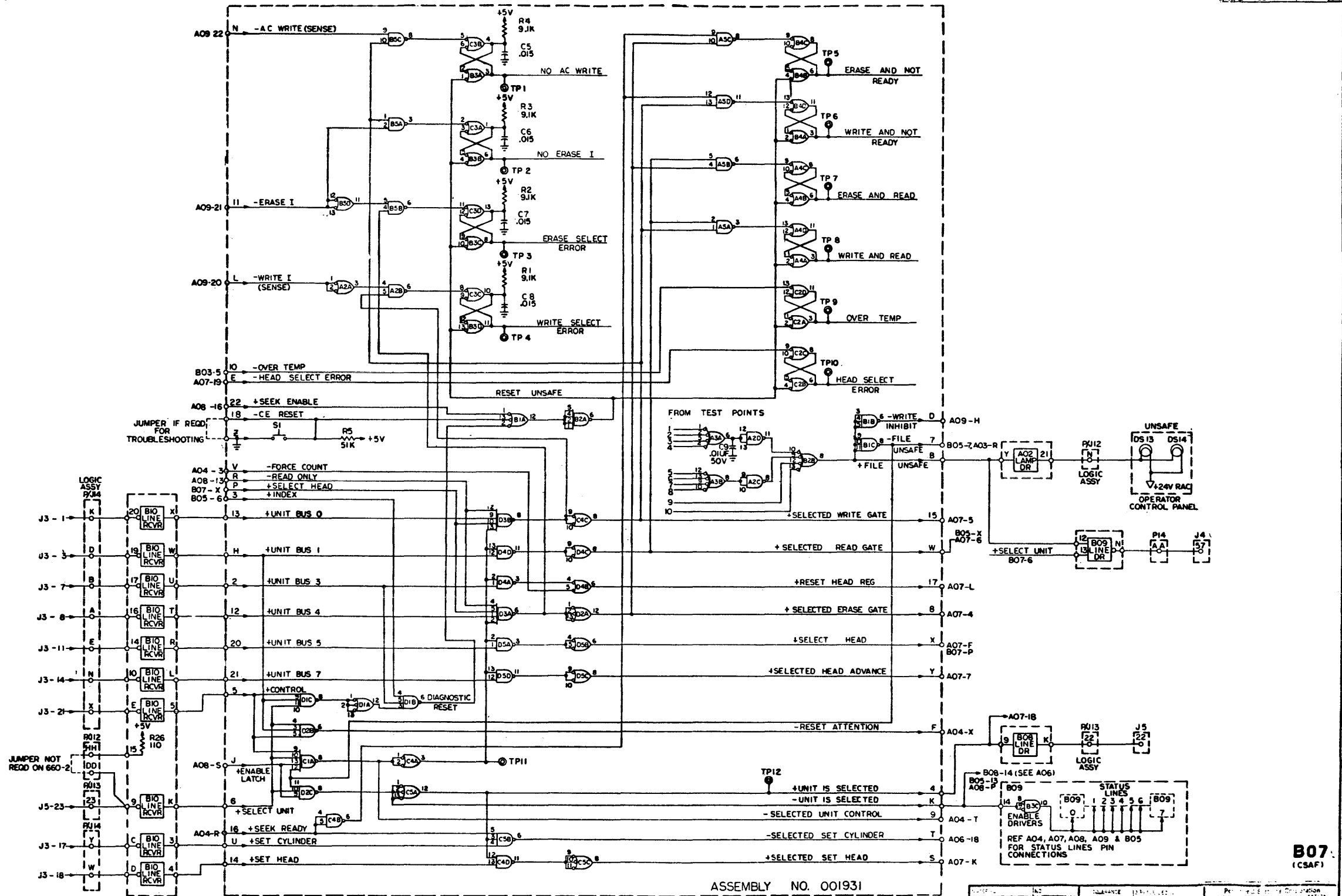
- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE IN MICROFARADS.
  2. ALL RESISTORS ARE IN OHMS.
  3. IC B4 & B5 ARE QUAD 2 INPUT SN7400N.
  4. IC B3 IS TRIPLE 3 INPUT SN7410N.
  5. IC B2 IS HEX INVERTER SN7404N.
  6. IC'S A3 & A4 ARE LM201.
  7. IC'S B1, C2, C3 & C4 ARE DUAL JK SN7473N.
  8. IC'S D1, D2, D3 & D4 ARE MCI710CP COMPARATOR.
  9. THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10 ± .04V.



B06 (TA 10)

201153	E	SYSTEM LOGIC TRANS-DUCER AMPLIFIER	NONE
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23



NOTES  
 1. C3 IS A SN7401N, OPEN COLLECTOR GATE.  
 2. THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10 VOLTS ± 0.4 VOLTS.

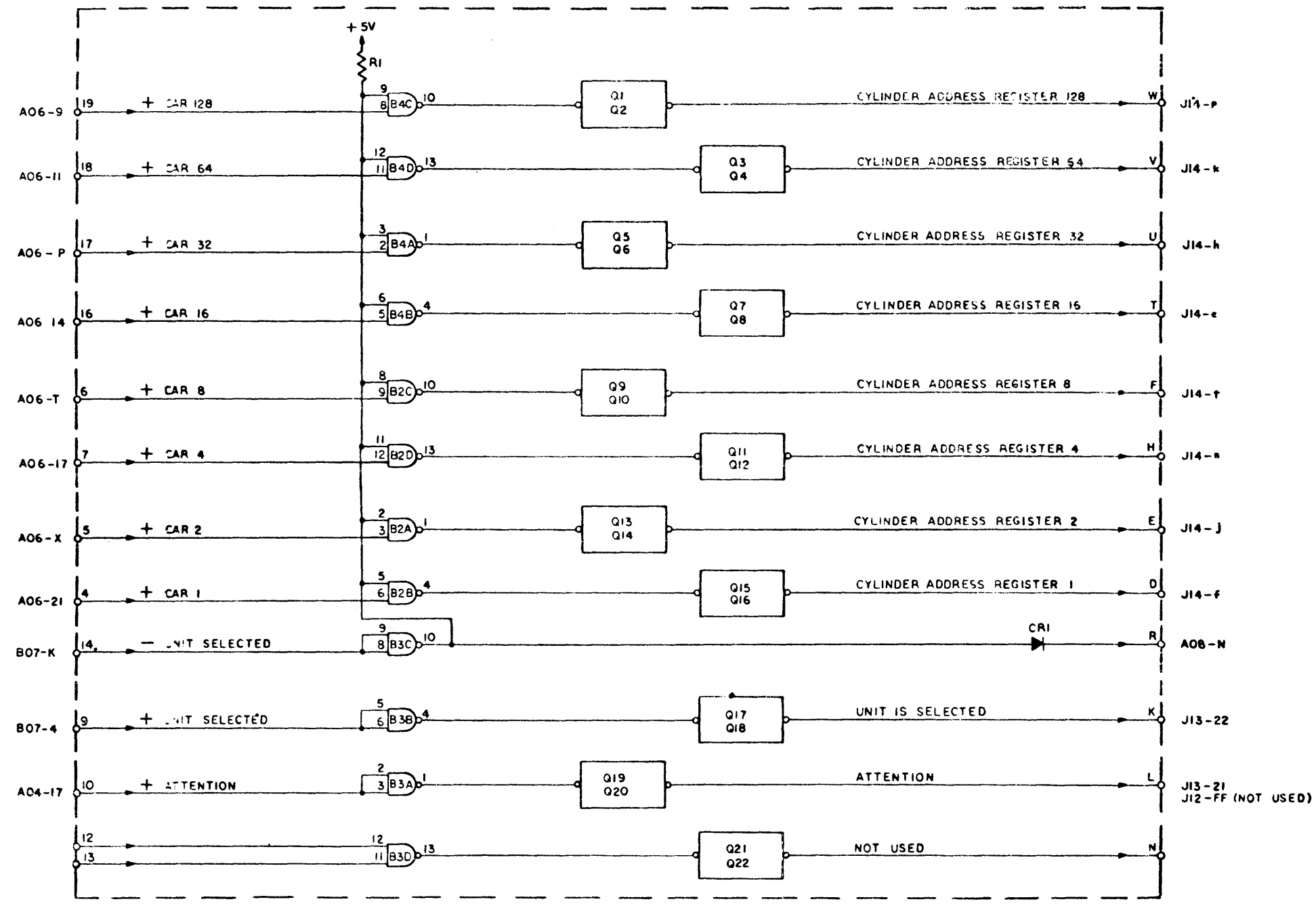
ASSEMBLY NO. 001931

DATE	DESIGNED BY	DESIGNED	PERFORMED BY
201154	E		
SYSTEM LOGIC DIAGRAM 660-1-3 CONTROL/SAFETY			
NONE			



201328

201328



- NOTES UNLESS OTHERWISE SPECIFIED
- CAR 1 THRU CAR 128 NOT WIRED ON MODEL 660-2.
  - ON MACHINES WITH TAMP P.C. BOARD EC LEVEL 487 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10 VOLTS ± .04 VOLTS.

1308  
(DRIV)

DATE	CHANGE NO.	DATE	CHANGE NO.	TECHNICAL APPROVAL	MEMOREX EQUIPMENT GROUP
7-29-69	416				NAME SYSTEM LOGIC DIAGRAM
12-2-69	556				LINE DRIVERS
1-23-70	865				DESIGN
JULY 70	1067				DETAIL
12-1-70	1244				CHECK
					APPROV

201328

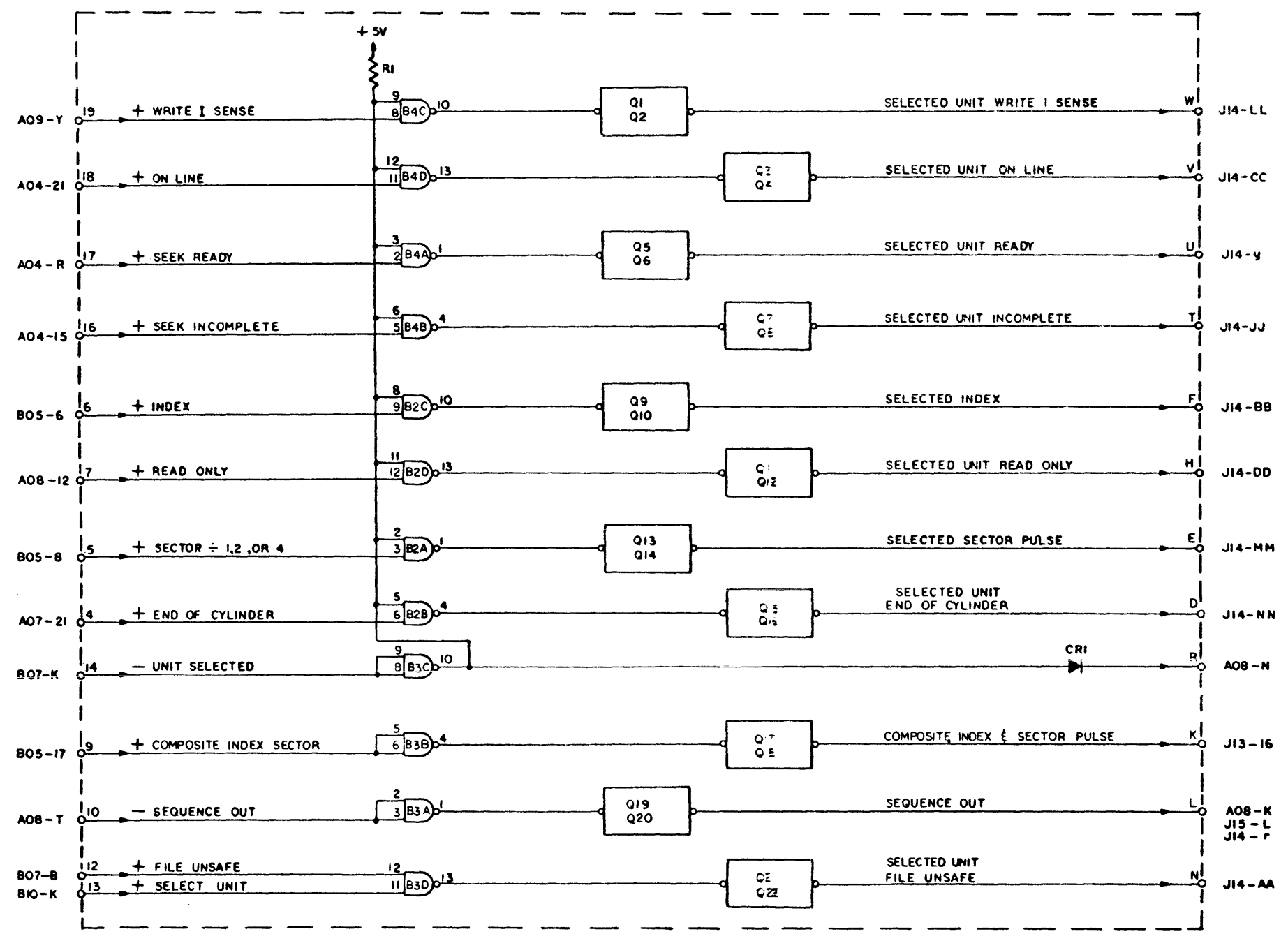
D

201328

25

201329

201329



NOTES: UNLESS OTHERWISE SPECIFIED  
1. ON MACHINES WITH TAMP P.C. BOARD EC LEVEL 487 OR GREATER, THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10VOLTS ± .04VOLTS

DATE	CHANGE NO.	DATE	CHANGE NO.	TECHNICAL APPROVAL	MEMOREX EQUIPMENT GROUP
7-29-69	416				NAME SYSTEM LOGIC DIAGRAM
12-2-69	556				LINE DRIVERS
APR 9, 70	865				DESIGN
JULY 70	1067				DETAIL
SEPT 71	1244				CHECK
					APPROV

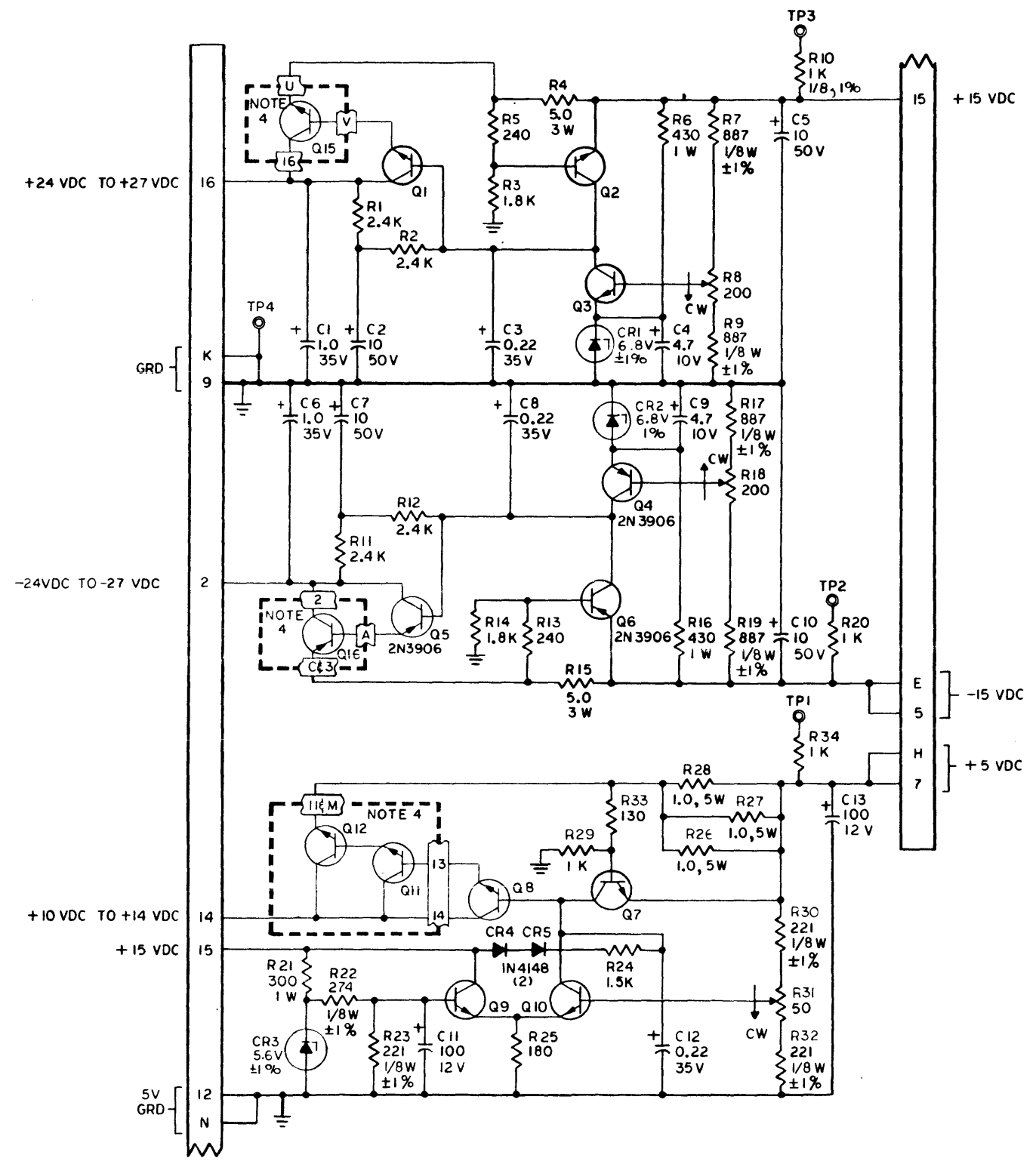
201329

26

001912

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660-1	001911	4-9-69	301		

001912



- NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%
  2. ALL CAPACITORS ARE IN UF, ±10%
  3. ALL TRANSISTORS ARE 2N3904
  4. Q11, Q12, Q15 & Q16 ON HEATSINK NO. 3

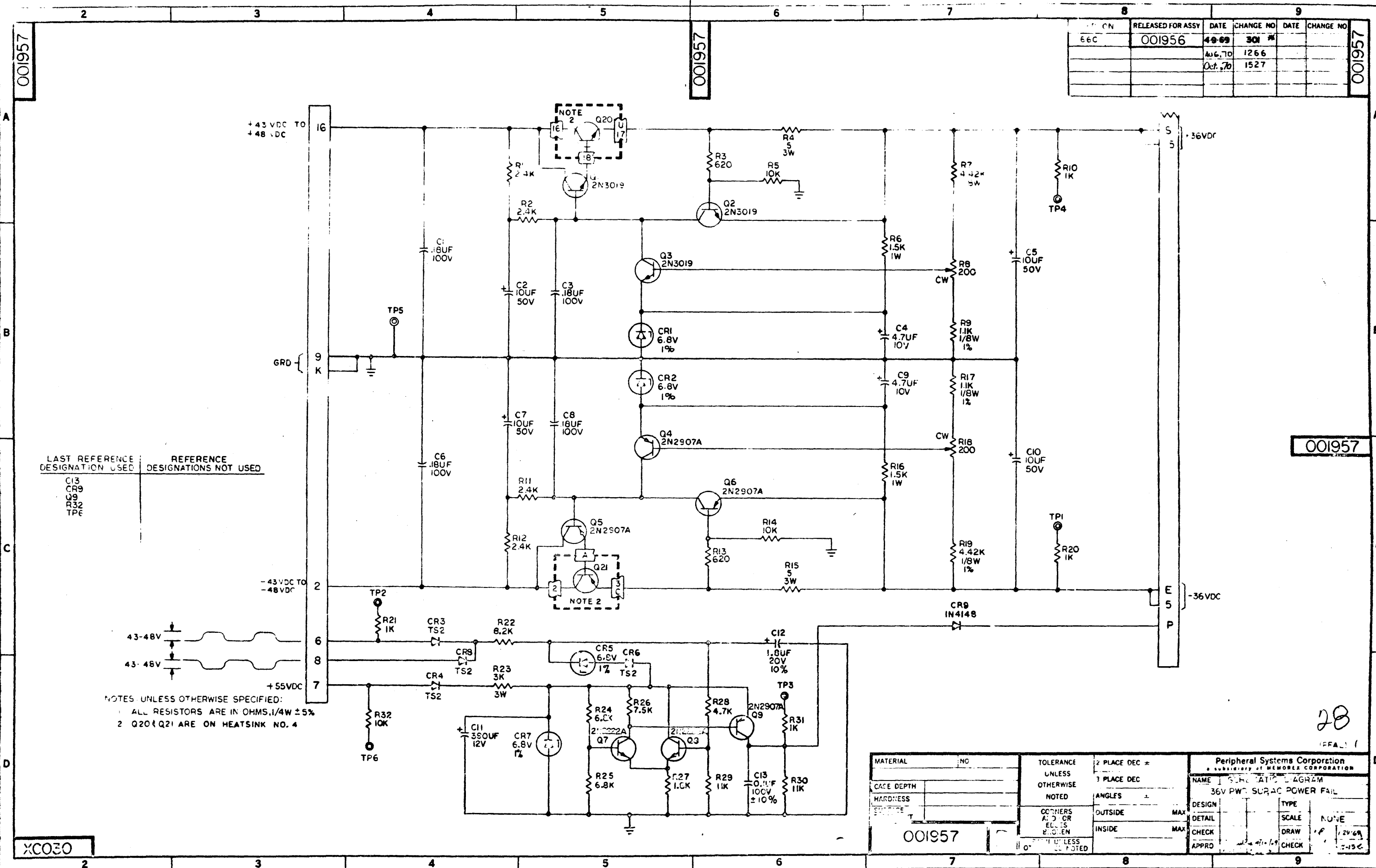
LAST REFERENCE DESIGNATION USED	REFERENCE DESIGNATION NOT USED
C13 CR5 Q12 R34 TP4	

MATERIAL		NO		TOLERANCE UNLESS OTHERWISE NOTED		2 PLACE DEC ±		3 PLACE DEC ±		ANGLES ±		CORNERS AND/OR EDGES BROKEN		RADI UNLESS OTHERWISE NOTED	
CASE DEPTH															
HARDNESS															
SURFACE TREATMENT															
001912		D													

Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION			
NAME SCHEMATIC DIAGRAM			
±15V & 5V POWER SUPPLY			
DESIGN		TYPE	
DETAIL		SCALE	NONE
CHECK		DRAW	3-12-69
APPRO		CHECK	3-12-69

XCO20

27



REV	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
66C	001956	4-9-69	301		
		Aug. 70	1266		
		Oct. 70	1527		

LAST REFERENCE DESIGNATION USED	REFERENCE DESIGNATIONS NOT USED
C13 CR9 Q9 R32 TPE	

NOTES UNLESS OTHERWISE SPECIFIED:  
 1 ALL RESISTORS ARE IN OHMS, 1/4W ±5%  
 2 Q20 & Q21 ARE ON HEATSINK NO. 4

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC	Peripheral Systems Corporation A SUBSIDIARY OF MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC	NAME   SCHEMATIC DIAGRAM	
HARDNESS			ANGLES	36V PWR SUR AC POWER FAIL	
SURFACE			CORNERS ALL OR EYES BLENDED	OUTSIDE MAX	INSIDE MAX
				DETAIL	TYPE
				CHECK	SCALE NONE
				APPRO	DRAW
					CHECK

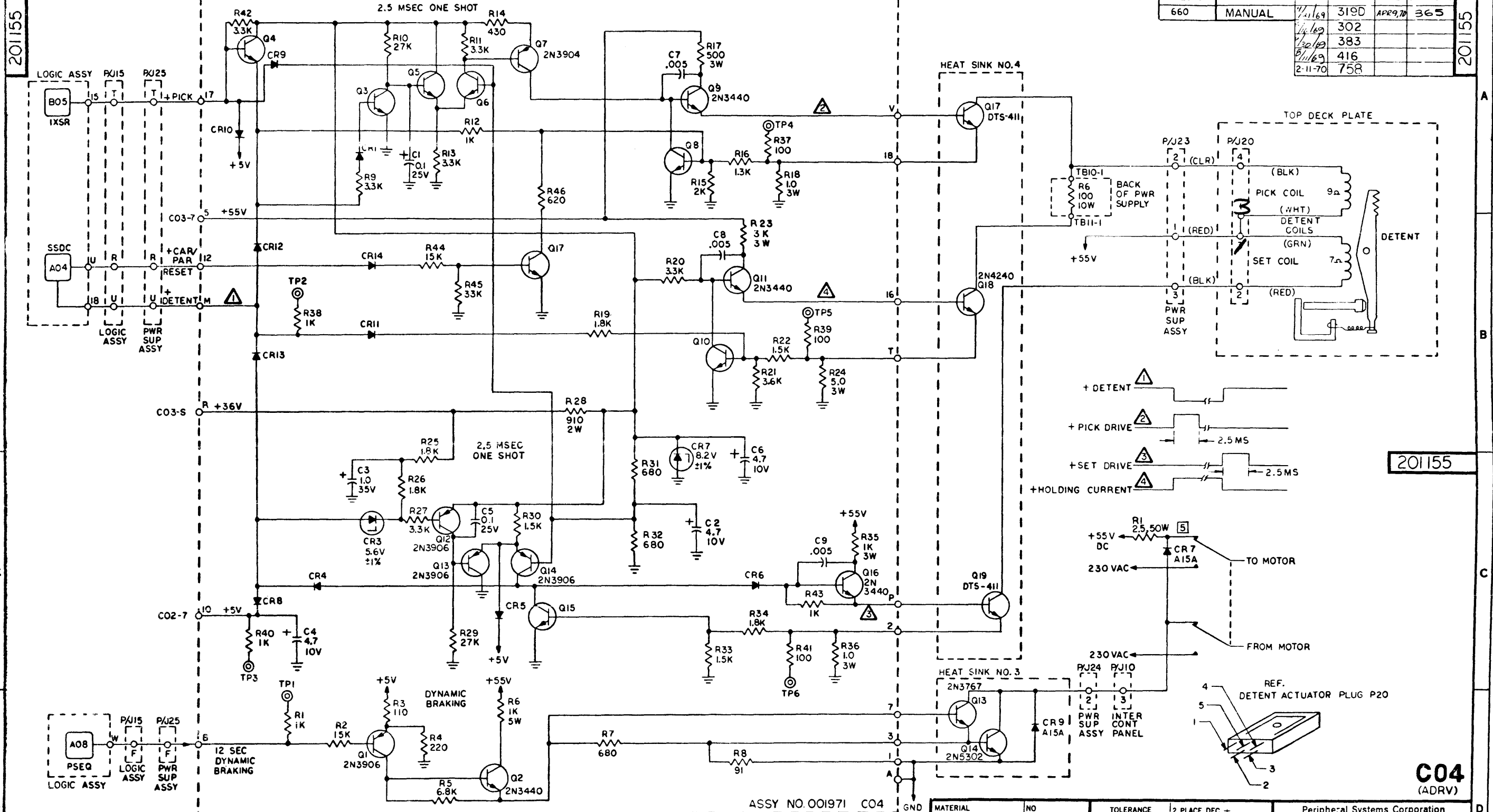
XCO30

001957

28  
(FFA) (

001957

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	MANUAL	7/1/69	319D	APR 9, 70	365
		1/20/69	302		
		8/11/69	383		
		2-11-70	416		
			758		



201155

- NOTES: UNLESS OTHERWISE SPECIFIED
- ALL RESISTORS ARE IN OHMS, 1/4W, ±5%
  - ALL CAPACITORS ARE IN MICROFARADS ±10%
  - ALL TRANSISTORS ARE 2N3904
  - ALL DIODES ARE IN4148
  - RESISTOR R1 IS SHORTED WITH DAYTON SPINDLE DRIVE MOTOR INSTALLED.
  - ON MACHINES WITH TAMP PC BOARD OF EC LEVEL 487 OR GREATER THE MAGNITUDE OF THE LOGIC SUPPLY VOLTAGE (+5V) IS 5.10 VOLTS ±0.04 VOLTS.

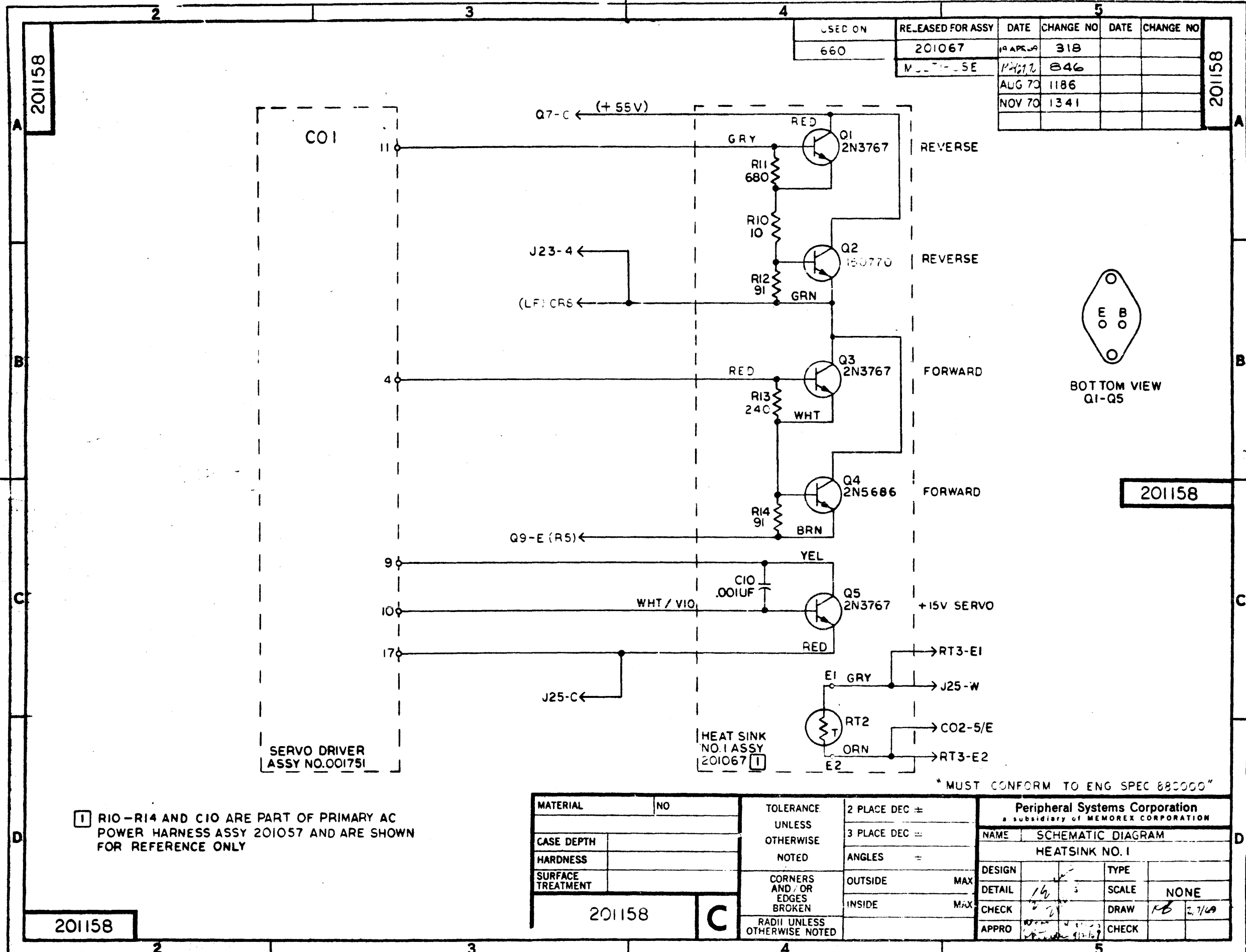
MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC ±	Peripheral Systems Corporation A SUBSIDIARY OF MEMOREX CORPORATION	
CASE DEPTH			3 PLACE DEC ±	NAME SYSTEM LOGIC DIAGRAM 660-1	
HARDNESS			ANGLES ±	ACTUATOR DRIVER	
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE
		RADI UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL	SCALE
				CHECK	DRAW
				APPRO	CHECK

201155

C04 (ADRV)

29

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	201067	19 APR 69	318		
	MULTI-USE	12/2/70	846		
		AUG 73	1186		
		NOV 70	1341		



1 R10-R14 AND C10 ARE PART OF PRIMARY AC POWER HARNESS ASSY 201057 AND ARE SHOWN FOR REFERENCE ONLY

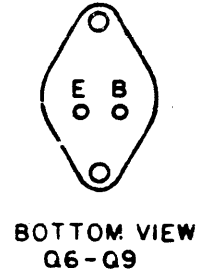
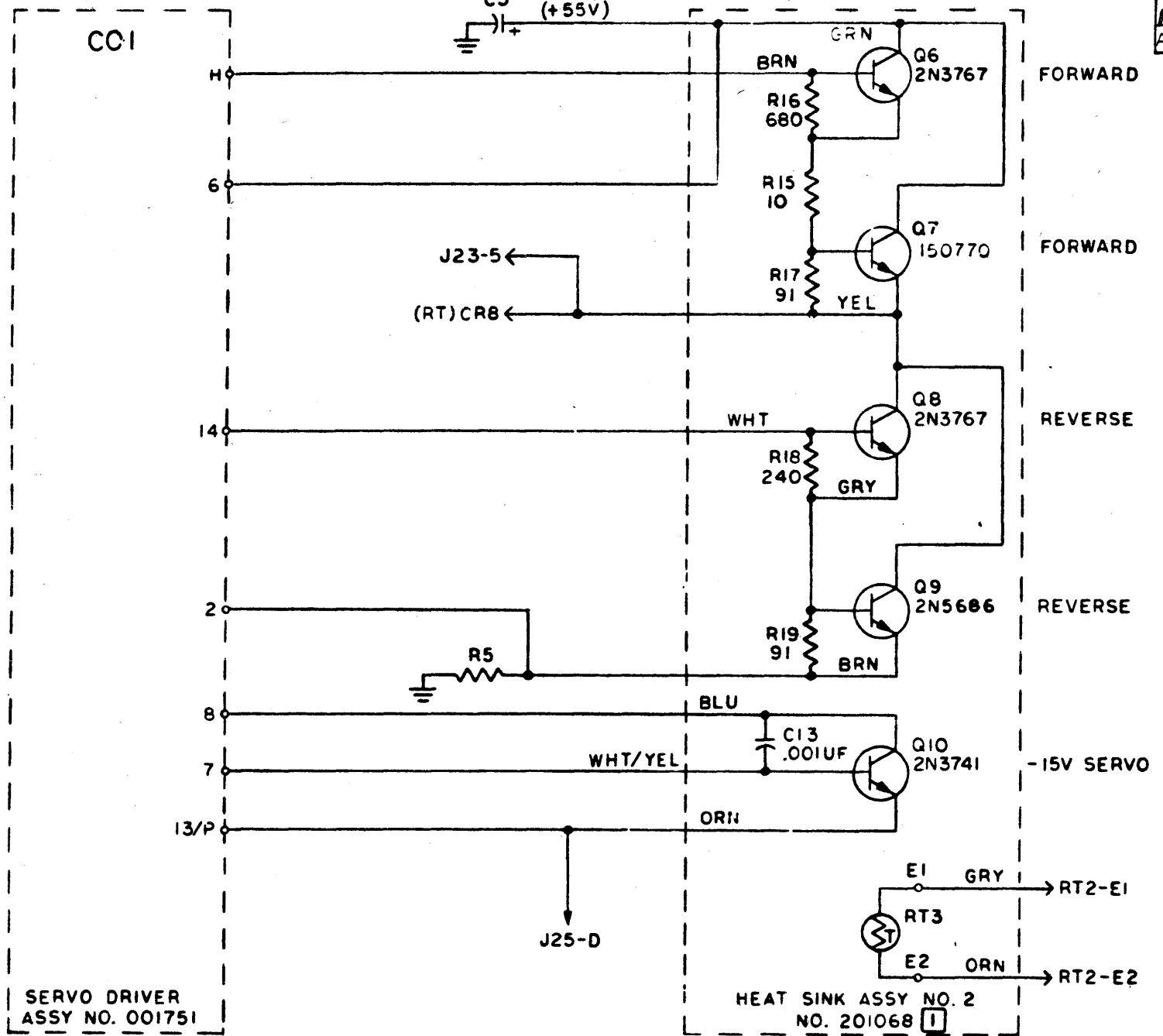
"MUST CONFORM TO ENG SPEC 880000"

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC =	3 PLACE DEC =	ANGLES =	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION			
CASE DEPTH						NAME SCHEMATIC DIAGRAM			
HARDNESS						HEATSINK NO. 1			
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	INSIDE MAX		DESIGN		TYPE	
		RADI UNLESS OTHERWISE NOTED				DETAIL	16	SCALE	NONE
	201158					CHECK		DRAW	KB 2/1/69
						APPRO		CHECK	

201159

USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	201068	19 APR 69	318	NOV 70	1341
	MULTI-USE	6-30-69	383		
		8-29-69	459		
		11/21/70	846		
		AUG 70	1186		

201159



201159

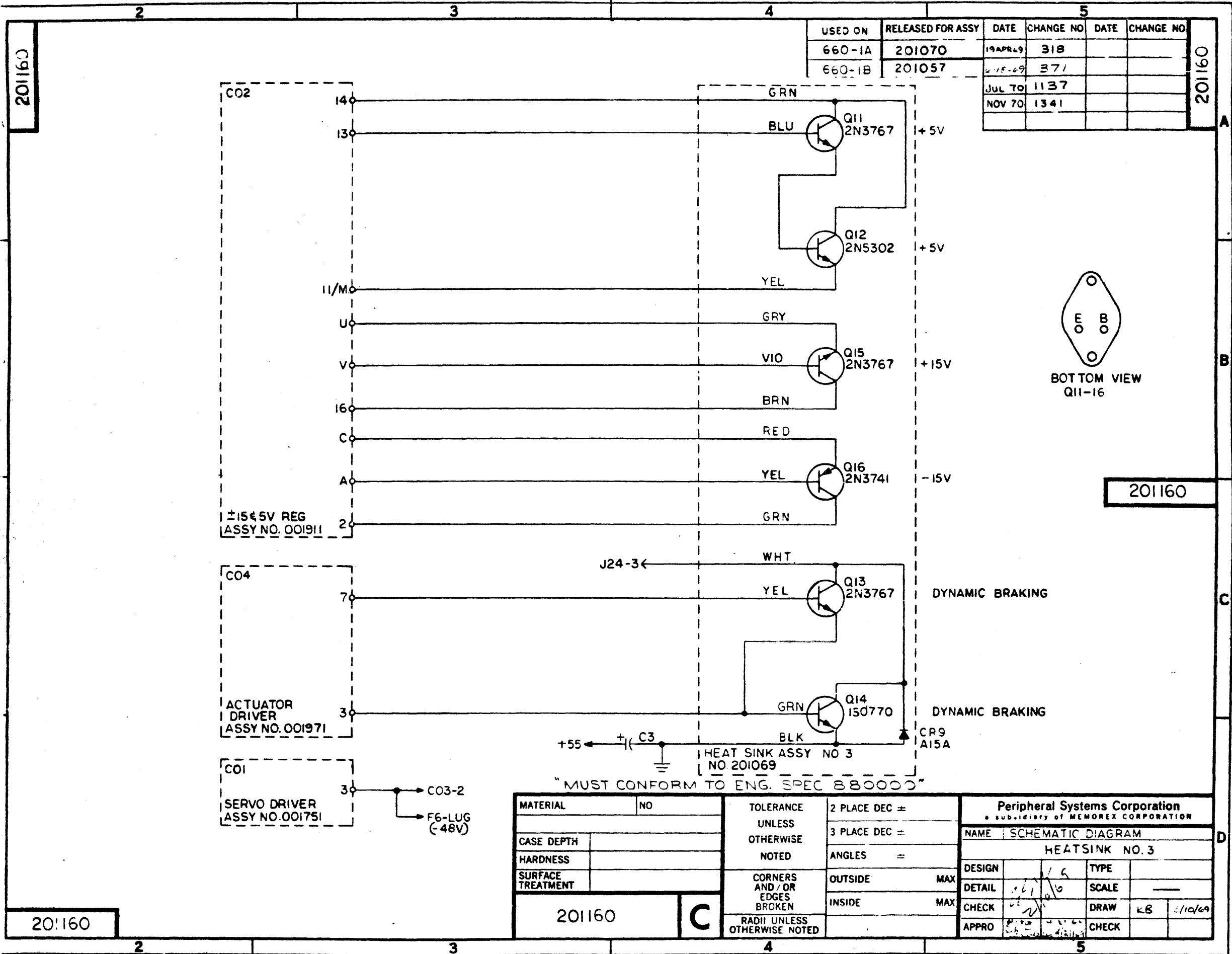
NOTES:

1 R15 - R19 AND C11 ARE PART OF PRIMARY AC POWER HARNESS ASSY 201057 AND ARE SHOWN FOR REFERENCE ONLY

\* MUST CONFORM TO ENG SPEC 830000 \*

201159

MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC =	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION	
			3 PLACE DEC = <td colspan="2">NAME SCHEMATIC DIAGRAM</td>	NAME SCHEMATIC DIAGRAM	
CASE DEPTH			ANGLES = <td colspan="2">HEATSINK NO. 2</td>	HEATSINK NO. 2	
HARDNESS			OUTSIDE MAX	DESIGN	TYPE
SURFACE TREATMENT			INSIDE MAX	DETAIL	SCALE
201159		C		CHECK	DRAW 7/26/69
		RADII UNLESS OTHERWISE NOTED		APPRO	CHECK



201160

201160

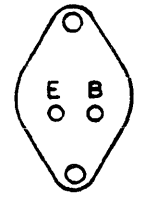
201160

201160

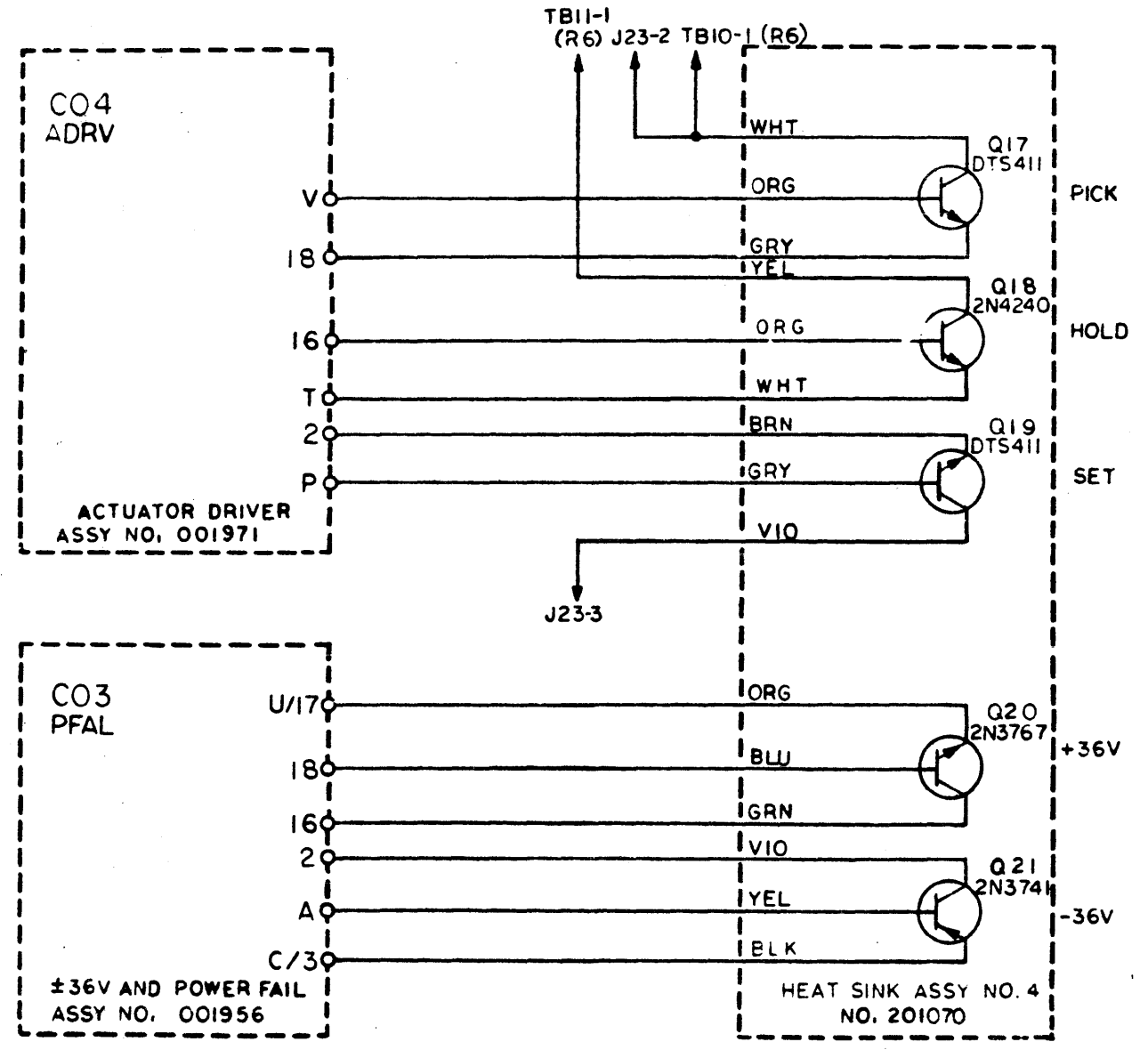
32



USED ON	RELEASED FOR ASSY	DATE	CHANGE NO	DATE	CHANGE NO
660	201070	19 APR 69	318		
	201057	11-13-69	527		
		NOV 70	1341		



BOTTOM VIEW  
Q17-Q21



201161

201161

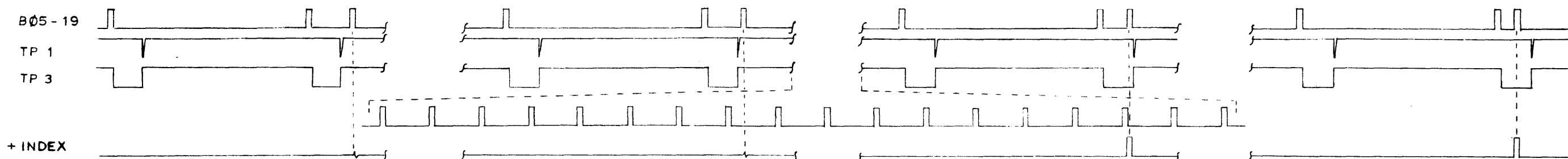
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201161

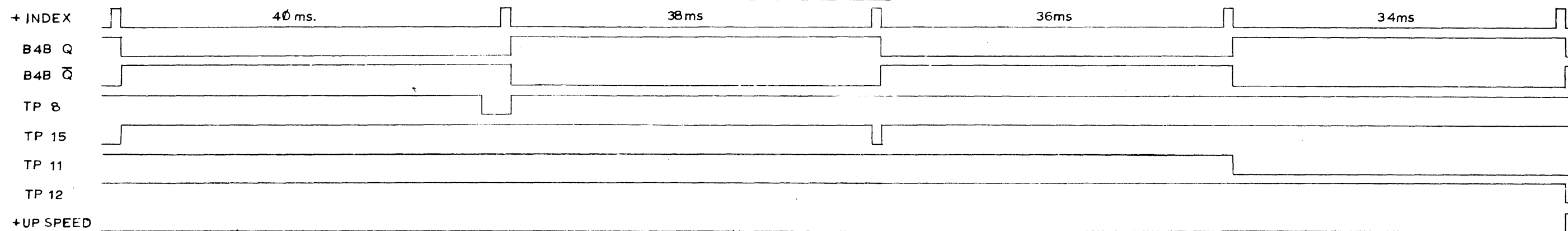
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MATERIAL	NO	TOLERANCE UNLESS OTHERWISE NOTED	2 PLACE DEC =	Peripheral Systems Corporation a subsidiary of MEMOREX CORPORATION			
CASE DEPTH			3 PLACE DEC =	NAME SCHEMATIC DIAGRAM			
HARDNESS			ANGLES =	HEAT SINK NO. 4			
SURFACE TREATMENT		CORNERS AND/OR EDGES BROKEN	OUTSIDE MAX	DESIGN	TYPE		
		RADI UNLESS OTHERWISE NOTED	INSIDE MAX	DETAIL	SCALE	NONE	
				CHECK	DRAW	FEB 1969	
				APPRO	CHECK		

INDEX AND SECTOR



UP TO SPEED TIMING



CYLINDER TRANSDUCER COUNT TIMING

