digital

RXO1

Engineering Drawings

Digital Equipment Corporation

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

SEQUENCE	
RXØ1 FLOPPY DISK DRIVE	B-DD-RXØ1-Ø
FLOPPY DISK CONTROL BOARD	D-CS-M7726-Ø-1
RXØ1 FIRMWARE LISTING	K-SP-RXØ1-0-2
READ/WRITE CONTROL BOARD	D-CS-M7727-Ø-1
H771 POWER SUPPLY	B-DD-H771-Ø
PLENUM/FAN ASSY. (OLD STYLE)	B-DD-7Ø135Ø3-Ø
PLENUM/FAN ASSY. (NEW STYLE)	B-DD-7015622-Ø

THIS IS PRINT SET ☐☐☐☐

UNIT VARIATIONS

VAR	TITLE	PRINT SET 1			
RXØ1-AA	SINGLE FLOPPY DISK, 115V,6Ø HZ	X			
RXØ1-AC	SINGLE FLOPPY DISK, LOW V, 5ØHZ	X			
RXØ1-AD	SINGLE FLOPPY DISK, HIGH V, 5ØHZ	X			
RXØ1-BA	DUAL FLOPPY DISK, 115V, 6Ø HZ	X			
RXØ1-BC	DUAL FLOPPY DISK, LOW V, 5ØHZ	X			
RXØ1-BD	DUAL FLOPPY DISK, HIGH V, 5ØHZ	X			
RXØ1-CA	ONE REPLACE DRIVE, 6Ø HZ	X			
RXØ1-CC	ONE REPLACE DRIVE, 5Ø HZ	X			
RXØ1-DA	RXØ1-BA W/O BEZEL ASSY	X			
RXØ1-DC	RXØ1-BC W/O BEZEL ASSY	X			
RXØ1-DD	RXØ1-BD W/O BEZEL ASSY	X			
RXØ1-FA	RXØ1-AA W/O PLENUM ASSY	X			
RXØ1-FC	RXØ1-AC W/O PLENUM ASSY	X			
RXØ1-FD	RXØ1-AD W/O PLENUM ASSY	X			
RXØ1-HA	RXØ1-BA W/O PLENUM ASSY	X			
RXØ1-HC	RXØ1-BC W/O PLENUM ASSY	X			
RXØ1-HD	RXØ1-BD W/O PLENUM ASSY	X			
RXØ1-JA	RXØ1-DA W/O PLENUM ASSY	X			
RXØ1-JC	RXØ1-DC W/O PLENUM ASSY	X			
RXØ1-JD	RXØ1-DD W/O PLENUM ASSY	X			
RXO1-LA	RXO1-BA FOR VX78(BC80D)	X			
RXO1-LC	RXO1-BC FOR VX78(BC80D)	X			
RXO1-LD	RXO1-BD FOR VX78(BC80D)	X			
RX01-VA	RX01 SINGLE FOR KC780 115, 60HZ	X			
RX01-VC	RX01 SINGLE FOR KC780 LOW V,50HZ	X			
RX01-VD	RX01 SINGLE FOR KC780 HIGH V,50HZ	X			

REVISIONS		
REV	CHG. NO.	DATE
A	RXØ1-2	6-76
B	RXØ1-3	7-76
C	RXØ1-6	12-76
D	RXØ1-8	5-77
E	RXØ1-12	12-77
F	RXØ1-13	6-78
H	RXØ1-ML13	7-78

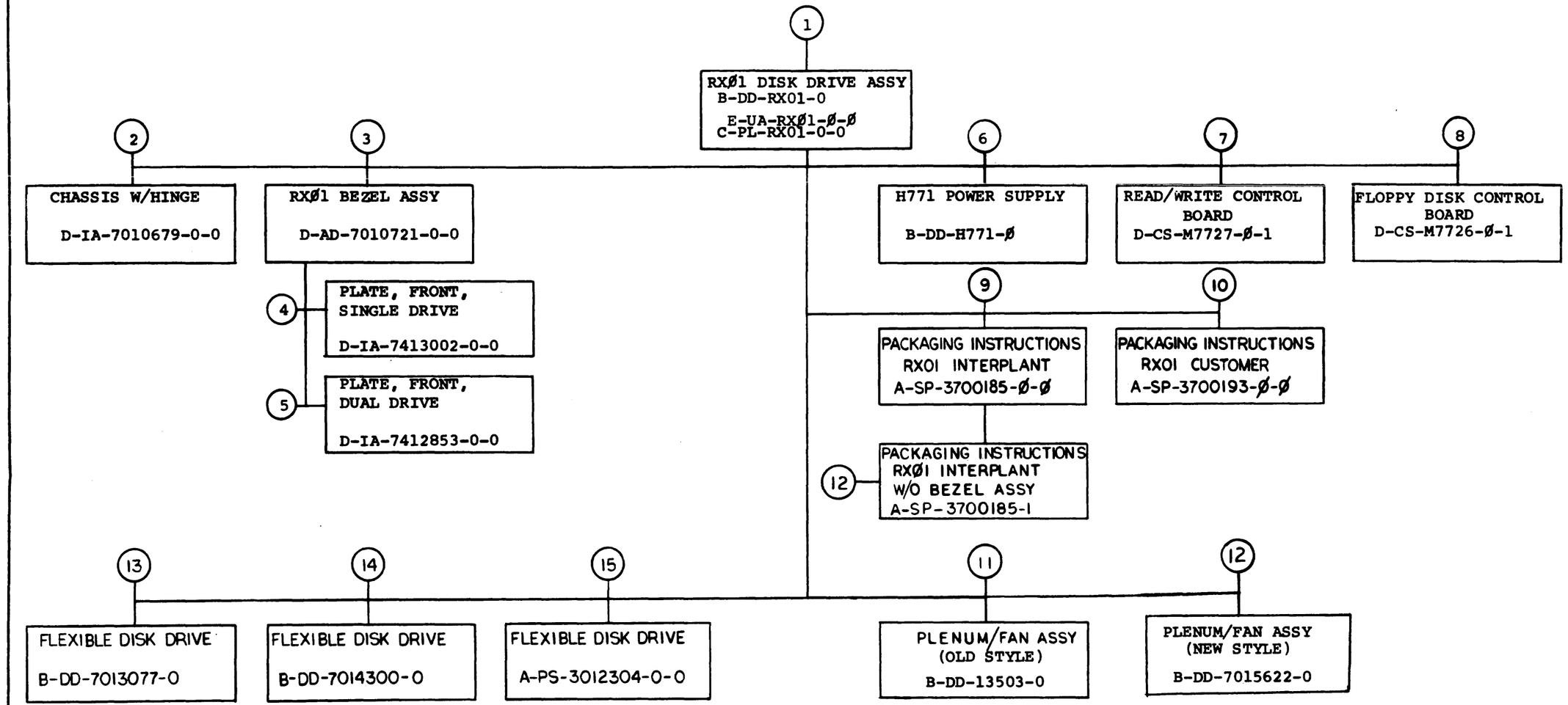
USED ON OPTION/MODEL	
RX8	
RX11	
LSI11	
SHEET 1 OF 3	

DRN. W. McCarthy	DATE 2/3/75	TITLE RXØ1 FLOPPY DISK DRIVE
CHK'D. McCarthy	DATE 5/29/75	
PROJ ENG.	DATE	
PROD.	DATE 6/3/75	SIZE B · CODE DD · NUMBER RXØ1-Ø · REV H
FIELD SERV.	DATE 6/12/75	DIST

DEC 16-(0351-1042-1A-M492

DRB 106

mc



TITLE		SIZE	CODE	NUMBER	REV
RXØ1 FLOPPY DISK DRIVE	SHEET2 OF 3	B	DD	RXØ1-Ø	H

DRB 107
DEC 16—(325)—1062—3—N871

MC

MECHANICAL

CUSTOMER PRINT SET	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
1		1	E-UA-RXØ1-Ø-Ø		5	RXØ1 FLOPPY DISK DRIVE ASSY	
			B-PL-RXØ1-Ø-Ø			RXØ1 FLOPPY DISK DRIVE ASSY(PL)	
			E-IA-7412666-0-0		1	COVER, TOP	
			D-IA-7010646-0-0		1	CABLE, EXTENSION, RXØ1	
			C-IA-7008612-0-0		1	CABLE, KEYBOARD	
			D-UA-BCØ5L-Ø-Ø		1	CABLE, JUMPER	
			D-IA-7010696-0-0		1	HARNESS, VOLTAGE VARIATION	
					1	BRACKET, SHIPPING, RXØ1	
			C-MD-7409479-0-0		1	PLATE, PRESSURE	
			C-MD-5509081-0-0		1	PANEL, LIGHT (RXØ1)	
		2	D-IA-7010679-0-0		1	CHASSIS W/HINGE	
			E-IA-7412665-0-0		1	CHASSIS, FLEXIBLE DISK DRIVE	
			C-MD-7413236-0-0		1	HINGE , LOGIC	
		3	D-AD-7010721-0-0		1	RXØ1 BEZEL ASSY	
			E-MD-7414506-0-0		1	BEZEL, RXØ1	
			A-PS-3612317-0-0		1	LOGO, RXØ1	
		4	D-IA-7413002-0-0		1	PLATE, FRONT, SINGLE DRIVE	
			C-SS-7413002-0-1		1	SILK SCREEN, SINGLE DRIVE	
		5	D-IA-7412853-0-0		1	PLATE, FRONT, DUAL DRIVEES	
			C-SS-7412853-0-1		1	SILK SCREEN, DUAL DRIVE	
C		6	B-DD-H771-Ø	*	3	H771 POWER SUPPLY	
			C-MD-7413350-0-0				
X		11	B-DD-7013503-0-0		3	PLENUM/FAN ASSY (OLD STYLE)	
		13	B-DD-7013077-0		3	FLEXIBLE DISK DRIVE	
		14	B DD 7014300-0		3	FLEXIBLE DISK DRIVE	
		15	A-PS-3012304-0-0		14	FLEXIBLE DISK DRIVE	
		16	B-DD-7015622-0-0		2	PLENUM/FAN ASSY NEW STYLE	

ELECTRICAL

CUSTOMER PRINT SET	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
1		1	B-DD-RXØ1-Ø	#	3	RXØ1 FLOPPY DISK DRIVE	
		1	C-MD-7413350-0-0		1	SHIPPING BRACKET	
			A-SP-RXØI-Ø-1		34	RXØI ENGINEERING SPECIFICATION	
C			K-SP-RXØI-Ø-2			RXØI FIRMWARE LISTING	
		12	A SP-3700185-1			PACK INSTR W/O BEZEL	
			A-PS-9905183			LAMINATED BUILDUP	
			A-PS-9905710-0-0			REGULAR SLOTTED CARTON	
			A-PS-9905712-0-0			PLYWOOD SUPPORT FIXTURE	
			A-PS-9905713-0-0			SCORED SHEET	
			A-PS-9905729-0-0			CARTON SEALING TAPE	
X		7	D-CS-M7727-Ø-1	*	6	READ/WRITE CONTROL BOARD	
			D-IA-5011370-0-0		1	ETCHED CIRCUIT BOARD (M7727)	
X		8	D-CS-M7726-Ø-1	#	9	FLOPPY DISK CONTROL BOARD	
			A-SP-M7726-Ø-7		3	ACCEPTANCE TEST PROCEDURE	
		9	A-SP-3700185-0-0			PACKAGING INST. INTERPLANT	
			A-PS-9905710-0-0			REGULAR SLOTTED CARTON	
			A-PS-9905711-0-0			ONE PIECE FOLDER	
			A-PS-9905712-0-0			PLYWOOD SUPPORT FIXTURE	
			A-PS-9905713-0-0			SCORED SHEET	
			A-PS-9905729-0-0			CARTON SEALING TAPE	
		10	A-SP-3700193-0-0			PACKAGING INST. CUSTOMER	
			A-PS-9905741-0-0			FULL TELESCOPE CAP	
			A-PS-9905740-0-0			FOAM PAD	
			A-PS-9905739-0-0			LAMINATED BUILDUP	
			A-PS-9905734-0-0			PLASTIC STRAPPING	

CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

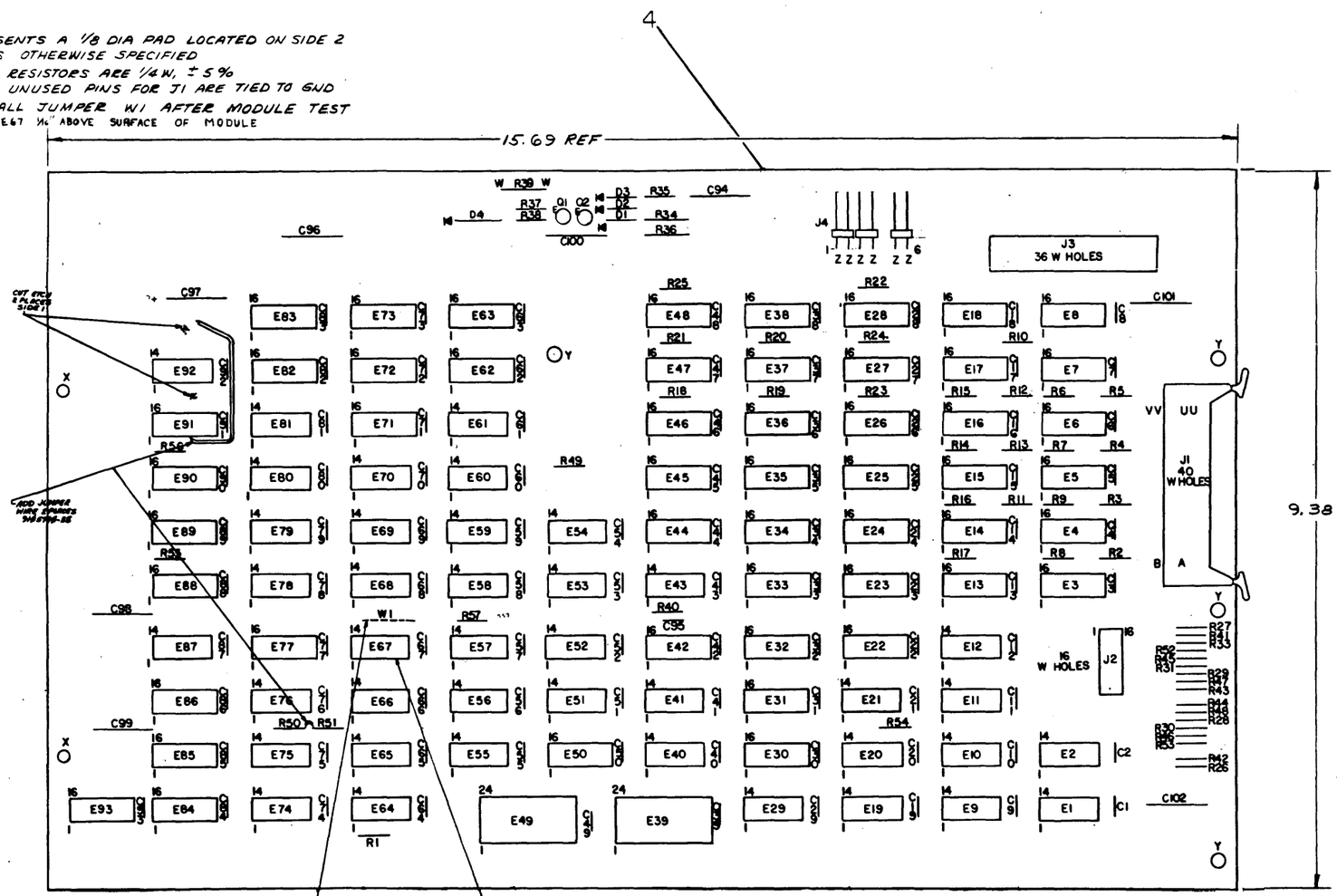
TITLE	SHEET	OF	SIZE	CODE	NUMBER	REV
RXØ1 FLOPPY DISK DRIVE	3	3	B	DD	RXØ1-Ø	H

DRB 108

MC

NOTES:

1. ◉ REPRESENTS A 1/8 DIA PAD LOCATED ON SIDE 2
2. UNLESS OTHERWISE SPECIFIED
   A. ALL RESISTORS ARE 1/4 W, ± 5%
   B. ALL UNUSED PINS FOR J1 ARE TIED TO GND
3. INSTALL JUMPER W1 AFTER MODULE TEST
4. MOUNT E67 1/16" ABOVE SURFACE OF MODULE



23-XXXA2	8	16
2102	9	18
8640	1	8
74175	8	16
74174	8	16
74161	8	16
74194	8	16
74123	8	16
74H103	11	4
74H106	13	5
7489	8	16
74150	12	24
7442	8	16
8266	8	16
74193	8	16
74154	12	24
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV.	CHANGE NO.	CHK	DRN	DATE
J	M7726-00007	H. DRAB	H. DRAB	4-2-77
H	M7726-00006	C. YOUSE	H. DRAB	4-4-76
F	M7726-00005	C. YOUSE	H. DRAB	3-31-76
E	M7726-00004	CHARLES YOUSE	CHARLES YOUSE	12-15-75
D	M7726-00003	C. YOUSE	C. YOUSE	12-15-75
C	M7726-00002	P. KOTSCHENTHER	A. CARLO	6/24/75
B	M7726-00001	P. KOTSCHENTHER	P. KOTSCHENTHER	5-5-75

FIRST USED ON OPTION MODEL: M7726

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

ETCH BOARD REV. B

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRW. Don Metzger	DATE 11/12/74	digital
CHK'D	DATE 1/9/75	
ENGR	DATE 1/21/75	TITLE FLOPPY DISK CONTROLLER
PROJ. ENG.	DATE 1/24/75	
PROD.	DATE	
NEXT HIGHER ASSY		
SCALE		SIZE D CODE CS NUMBER M7726-Ø-1 REV. J
SHEET 1 OF 9		DIST.

M7726-Ø-1 J

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7726-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7726-0-5	2
REF		MODULE ECO HISTORY	B-MW-M7726-0-6	3
1		ETCHED CIRCUIT BOARD	5011390	4
1	J3	RECEP 36 PIN (REWORK)	B-MD-5509 071-1	5
1	J2,	I.C SOCKET, 16 PIN GOLD, LOW PROFILE	1211813-02	6
1	R37	RES 10K ¼W 5% CC	1300479-00	7
8	C 94, C96 – C102	CAP 6.8 µf 35V 10% S.TANT	1005306-00	8
93	C1 - C93	CAP .01 µf 50V AXIAL CER	1001610-00	9
1	C95	CAP 12 PF 100V 5%	1002087-00	10
3	D1 - D3	DIODE IN4004	1105796-00	11
1	D4	DIODE IN746A 3.3V 5%	1104860-00	12
1	R 39	RES 100 ½W 5% CC	1300228-00	13
3	J4	HEADER, 2PIN (MALE)	1212204-00	14
8	R2, R4, R6, R8, R10 R12, R14, R16	RES 470 ¼W 5% CC	1300316-00	15
8	R27, R29, R31, R47, R52 R43, R41, R45	RES 390 ¼W 5% CC	1300309-00	16
5	R1, R49 - R51, R57	RES 3K ¼W 5% CC	1300432-00	17
5	R26, R28, R30, R38 R42, R44, R46, R48, R53	RES 180 ¼W 5% CC	1301322-00	18
8	R3, R5, R7, R9, R11 R13, R15, R17	RES 82Ø ¼W 5% CC	1301775-00	19
1	R35	RES 300 ¼W 5% CC	1301425-00	20
8	R18 – R25	RES 2K ¼W 5% CC	1302388-00	21
1	R34	RES 261 ¼W 1% MF	1302873-00	22
1	R36	RES 287 ¼W 1% MF	1305124-00	23
1	R40	RES 8.2K ¼W 5% CC	1303179-00	24
3	R54 – R56	RES 1K ¼W 5% CC	1300365-00	25
1	Q2	TRANS MX AA05	1510705-00	26
1	Q1	TRANS MX AA55	1510706-00	27
3	E19, E20, E21, E29 E40	I.C 7474	1905547-00	28
3	E9, E57, E59	I.C. 7400	1905575-00	29
2	E43, E60	I.C. 7410	1905576-00	30
1	E75	I.C. 7450	1905580-00	31
1	E55	I.C. 74H20	1905635-00	32
1	E54	I.C 7402	1909004-00	33
2	E68, E72	I.C. 74H00	1909056-00	34
2	E56, E70	I.C. 74H11	1909267-00	35
5	E58, E69, E78, E79, E82	I.C 74H74	1909667-00	36
2	E64, E76	I.C. 7404	1909686-00	37
1	E39	IC 74154	1909701-00	38
2	E1, E2	I.C. 8881	1909705-00	39
1	E61	I.C. 74H04	1909931-00	40
2	E74, E92	I.C. 7486	1910011-00	41
4	E88, E89, E90, E91	I.C 74193	1910018-00	42
2	E27, E37	I.C 8266	1909934-00	43
1	E22	I.C 7402	1910046-00	44
1	E65	I.C 7437	1910091-00	45
1	E49	I.C 74150	1910153-00	46
2	E11, E12	I.C 7408	1910155-00	47
2	E97, E98	I.C. 7489	1910396-00	48
1	E50	I.C 74H108	1910408-00	49
3	E80, E81, E87	I.C 74H103	1910409-00	50
1	E42	I.C. 74123	1910436-00	51

PARTS LIST

	REF DESIGNATION	DESCRIPTION	PART NO	ITEM
2	E45, E46	I.C 74194	1910623-00	52
8	E23, E24, E25, E26 E30, E31, E32, E36	IC. 74161	1910650-01	53
3	E84, E85, E86	I.C. 74174	1910652-00	54
1	E53	I.C 7427	1910878-00	55
3	E28, E38, E44	I.C. 74175	1910651-00	56
2	E10, E66	I.C. 8640	1911469-00	57
1	E33	I.C 2102 680 NS	2111318-02	58
				59
6	E35, E39, E62, E63 E73, E83	SAME IC SPACES		60
1	E67	CRYSTAL OSCILLATOR 20MHZ	1811660-00	61
4	E41, E71, E93, E52	I.C. 74S74	1910544-00	62
1	E51	I.C. 74H10	1909057-00	63
1	E77	I.C. 74H40	1905586-00	64
				65
N/R		#30 AWG SOLID WIRE (WEL)	9106740-55	66
1	J1	CONN 40 PIN RT ANG HDR	1209941-02	67
1	(J1)	LATCH, LEFT FOR RT ANG HDR	1209941-03	68
1	(J1)	LATCH, RIGHT FOR RT ANG HDR	1209941-04	69
1	E13	I.C 256 X 4 ROM FLD0L	23111A2	70
1	E3	I.C 256 X 4 ROM FLD0H	23121A2	71
1	E14	I.C 256 X 4 ROM FLD1L	23257A2	72
1	E4	I.C 256 X 4 ROM FLD1H	23258A2	73
1	E15	I.C 256 X 4 ROM FLD2L	23115A2	74
1	E5	I.C. 256 X 4 ROM FLD2H	23116A2	75
1	E16	I.C 256 X 4 ROM FLD3L	23117A2	76
1	E6	I.C. 256 X 4 ROM FLD3H	23118A2	77
1	E17	I.C 256 X 4 ROM FLD4L	23259A2	78
1	E7	I.C. 256 X 4 ROM FLD4H	23260A2	79
1	E18	I.C. 256 X 4 ROM FLD 5L	23121A2	80
1	E8	I.C. 256 X 4 ROM FLD 5H	23122A2	81
1	R33	RES 150 1/4W 5% CC	1300250-00	82

SPARE I.C. GATES

TYPE	LOCATION	PINS	DESCRIPTION
74H04	E61	12	INVERTER
7404	E64	12, 13	INVERTER
7464	E76	12, 13	INVERTER
7408	E11	1,2,3 8,9,10	2 INPUT AND
74H00	E72	1,2,3 4,5,6 8,9,10	2 INPUT NAND
7437	E65	8, 9, 10	2 INPUT NAND BUFFER
8881	E2	8, 9, 10	2 INPUT NAND OC.
74H10	E51	3,4,5,6	3 INPUT NAND
74H40	E77	1,2,4,5,6	4 INPUT NAND BUFFER
7402	E54	4,5,6	2 INPUT NOR
8640	E66	2,6,7 11,12,13	2 INPUT NOR RCVR
7427	E53	1,2, 12,13	3 INPUT NOR
7486	E52	4,5,6	2 INPUT XOR
7486	E74	1,2,3, 4,5,6	2 INPUT XOR
7474	E93	1,2,3,4,5,6	D TYPE FLIP FLOP
74H106	E58	1,2,3,4, 14,15,16	J K FLIP FLOP
74123	E42	1,2,3,4,13,14,15	ONE SHOT

ALLOWABLE SUBSTITUTIONS

PREFERRED			REPLACEMENT	
TYPE	ITEM #	P.N.	TYPE	P.N.
7489	48	1910396-00	3101A	1910653-00
7489	48	1910396-00	8225	1911162-00

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
FLOPPY DISK CONTROLLER	D	CS	M7726 – Ø – 1	J
SCALE	SHEET 2 OF 9	DIST.		

DEC FORM NO. 1969 137

ROM OUT 7
ROM OUT 6
ROM OUT 5
ROM OUT 4
ROM OUT 3
ROM OUT 2
ROM OUT 1
ROM OUT Ø

E27 8266 — MUX OUT 7, MUX OUT 6, MUX OUT 5, MUX OUT 4
E37 8266 — MUX OUT 3, MUX OUT 2, MUX OUT 1, MUX OUT Ø

COUNTER MOST SIG HALF — E26 74161 — CNTR OVFLW H
COUNTER LEAST SIG HALF — E36 74161 — C.O.
HIGH 1
INIT + PC AL
CI(1) H
CØ(1) H
CLK CNTR L
WBR CLK CNTR L
E56 74H11
P/O J3

SHIFT REG MOST SIG HALF — E45 74194 — SR MSB (1) H
SHIFT REG LEAST SIG HALF — E46 74194
SR LOAD H
CLK SR L
INIT + PC AL

WR ENB SCRATCH PAD MOST SIG HALF — E48 7489
ENB WR SCRATCH PAD LEAST SIG HALF — E47 7489
LD SCRATCH PAD L
+5V
R25, 2K
R24, 2K
R23, 2K
R22, 2K
R21, 2K
R2Ø, 2K
R19, 2K
R18, 2K

MEMORY BUFFER 74175 — E28
MEMORY BUFFER 74175 — E38
INST 1(1) L
INST Ø(1) L
SEL 3(1) H
SEL 2(1) H
SEL 1(1) H
SELØ(1) H
C1(1) L
CØ(1) L
INST 1(1) H
INST Ø(1) H
C1(1) H
CØ(1) H
INIT + PC AL
LD MB + CLK PC L
E61 74H04
C1(1) AH

SCRATCH PAD ADDR REGISTER 74175 — E44
INIT + PC AL
CLK SP ADDR REG L

CØ(1) L
C1(1) H
E54 74Ø2
SR LOAD H
E59 74ØØ
E59 74ØØ
CØ(1) H
SEP DATA(1) H
E60 74Ø

REVISIONS		
CHK	CHANGE NO.	REV.

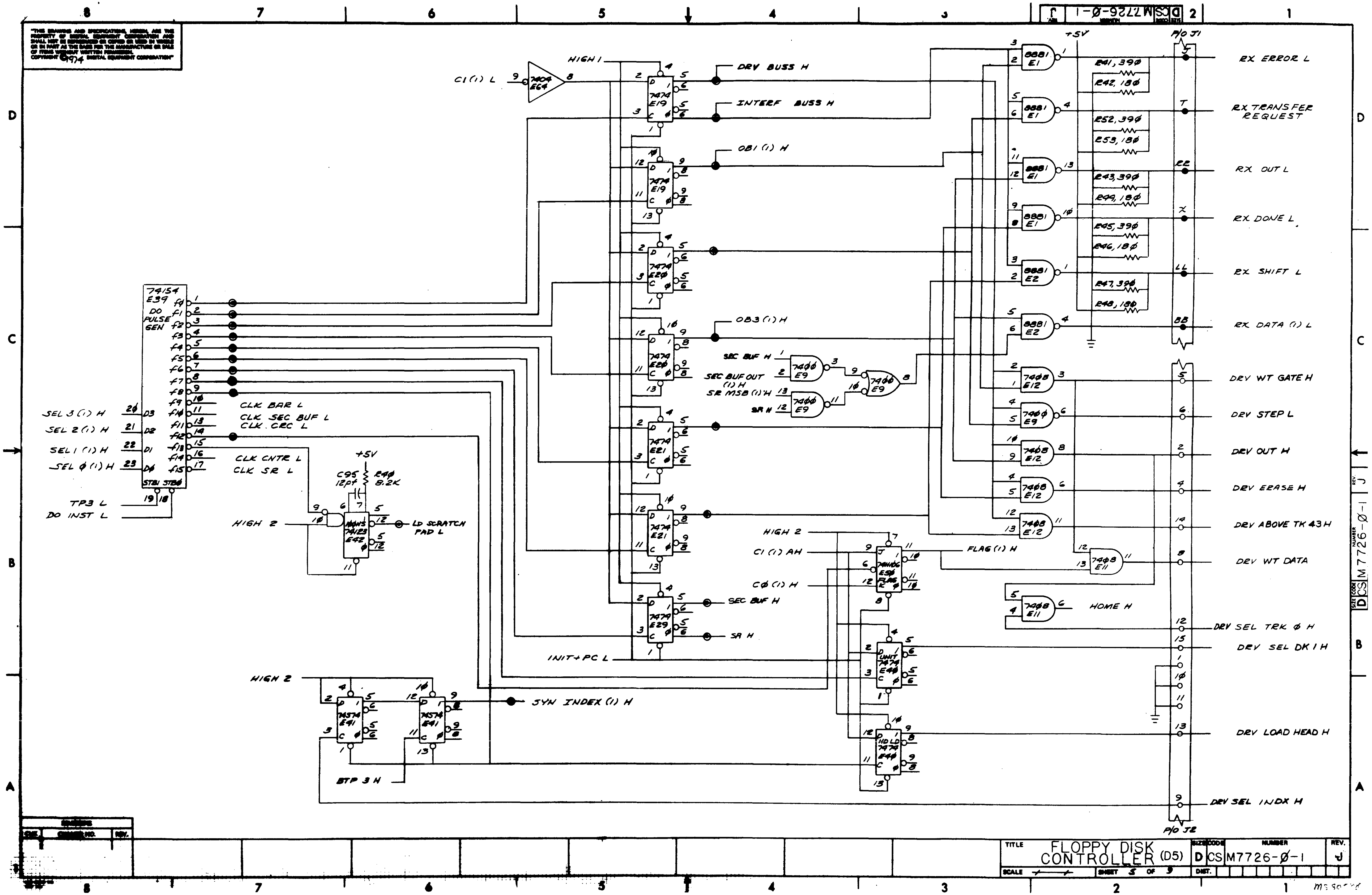
TITLE	SIZE	CODE	NUMBER	REV.
FLOPPY DISK CONTROLLER (D3)	D	CS	M7726-Ø-1	J
SCALE	SHEET 3 OF 9	DIST.		

HIGH 3
20 MHZ CLK
74H74 E82
HIGH 3
74H103 E87
END WIND L
HIGH 3
74S74 E71
74S74 E71
20 MHZ CLK
74H74 E82
74H11 E70
74H103 E81
MIS CLK (1) L
INIT + PC AL
74H103 E80
74H103 E80
INIT + PC AL
7402 E54
74H103 E81
SEP DATA (1) H
SEP DATA (1) L
74H11 E70
INIT + PC AL
P/O J2
DEV RAW DATA L
7404 E64
7437 E65
74H103 E87
74S74 E93
SEP CLK (1) H
BTP 3 H
HIGH 2
74H00 E72
74193 E89
BRW CRY
INIT + PC H
74193 E88
END WIND L
74193 E90
INIT + PC H
74193 E91
74161 E30
LSB BUFFER ADDR REG LS THIRD
MSB MSB
CLR
LD
CLK
CNT EN
CRY EN
CO
74161 E31
74161 E32
74S74 E33
EN
2Ø2 E33
SECTOR DATA BUFFER 1K RAM
SEC BUF OUT (1) H
DATA WRT IN
HIGH 1
74S74 E29
CØ (1) H
CLK SEC BUF L
CØ (1) L
INIT + PC L
C1 (1) A H
CLK BAR L
HIGH 1
SEC BUF OVFLW H
DEV BUSS H
7404 E76
DATA I L
7450 E75
SEP DATA (1) L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
FLOPPY DISK CONTROLLER (D4)	D	DCS	M7726-Ø-1	J
SCALE	SHEET 4 OF 9	DIST.		

DCS M7726-Ø-1 J


FLOPPY DISK CONTROLLER (D5)
D CS M7726-Ø-1
REV. J
SHEET 5 OF 9
C1(1) L
HIGH 1
DRV BUSS H
INTERF BUSS H
OB1 (1) H
OB3 (1) H
SEC BUF H
SEC BUF OUT (1) H
SR MSB (1) H
SR H
74154 E39 DO PULSE GEN
SEL 3 (1) H
SEL 2 (1) H
SEL 1 (1) H
SEL Ø (1) H
TP3 L
DO INST L
CLK BAR L
CLK SEC BUF L
CLK CRC L
CLK CNTR L
CLK SR L
HIGH 2
LD SCRATCH PAD L
INIT+PC L
SYN INDEX (1) H
BTP 3 H
C1 (1) AH
CØ (1) H
FLAG (1) H
HOME H
+5V
RX ERROR L
RX TRANSFER REQUEST
RX OUT L
RX DONE L
RX SHIFT L
RX DATA (1) L
DRV WT GATE H
DRV STEP L
DRV OUT H
DRV ERASE H
DRV ABOVE TK 43 H
DRV WT DATA
DRV SEL TRK Ø H
DRV SEL DK 1 H
DRV LOAD HEAD H
DRV SEL INDX H
P/O J1
P/O J2

ROM OUT 7
ROM OUT 6
ROM OUT 5
ROM OUT 4
ROM OUT 3
ROM OUT 2
ROM OUT 1
ROM OUT Ø

+5V
R1 3K
R2 470
R3 820
R4 470
R5 820
R6 470
R7 820
R8 470
R9 820
R10 470
R11 820
R12 470
R13 820
R14 470
R15 820
R16 470
R17 820

DISABLE ROMS L
7404 E64
7442 E22 FIELD DECODER
FLD 5 L
FLD 4 L
FLD 3 L
FLD 2 L
FLD 1 L
FLD Ø L

SEL 3(1) H
SEL 2(1) H
SEL 1(1) H
SEL Ø(1) H
FIELD COUNTER MSB LSB
JUMP L
74161 E23 LD CLR CLK CNT EN CRY EN C.O.
P/O J3

MUX OUT 7
MUX OUT 6
MUX OUT 5
MUX OUT 4
PROGRAM COUNTER MS HALF LSB
INIT + PC AL
74161 E25 CLR LD CLK CNT EN CRY EN C.O.

MUX OUT 3
MUX OUT 2
MUX OUT 1
MUX OUT Ø
PROGRAM COUNTER LS HALF LSB
INIT + PC L
PC LOAD EN L
LD MB + CLK PC L
HIGH 1
74161 E24 CLR LD CLK CNT EN CRY EN C.O.

FLD 5 L — E8
FLD 4 HI — E7
FLD 3 HI — E6
FLD 5 L — E18
FLD 4 LO — E17
FLD 3 LO — E16
FLD 2 HI — E5
FLD 2 L
FLD 1 HI — E4
FLD 1 L
FLD Ø HI — E3
FLD Ø L
FLD 2 LO — E15
FLD 2 L
FLD 1 LO — E14
FLD 1 L
FLD Ø LO — E13
FLD Ø L

A7 A6 A5 A4 A3 A2 A1 AØ
M3(1) M2(1) M1(1) MØ(1)
ENBI ENBØ

P/O J3
T2 V1 E2 D2 M2 K1 L1 C1
PC7(1) H
PC6(1) H
PC5(1) H
PC4(1) H
PC3(1) H
PC2(1) H
PC1(1) H
PCØ(1) H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE FLOPPY DISK CONTROLLER (D6)
SIZE D | CODE DCS | NUMBER M7726-Ø-1 | REV. J
SCALE | SHEET 6 OF 9 | DIST.

+5V
20 MHZ OSCILLATOR EG7
W1
NOTE 3
74H00 E77
20 MHZ CLK
74H74 E78
74H74 E79
HIGH 2
TP1 H
TP3 H
TP3 L
TP4 L
TP4 H
INIT + PC H
74H00 EG8
74H04 EG1
BTP 3 H
INIT + PC AL
74H11 E70
74H74 EG9
P/O J3
R49 3K
R50 3K
CONTIN L
HALT L
7404 E76
7400 E59
74H00 EG8
7410 EG0
HALT H
ERROR HALT ENABLE L
R51 3K
INTERF BUSS H
OB 1 (1) H
C0 (1) H
C1 (1) H
PRESET CEC L
CLK CEC L
SHIFT CEC L
C0 (1) L
C1 (1) L
SEP DATA (1) L
CEC 16 (1) L
7450 E75
7486 E92
CEC 1
CEC 2
CEC 3
CEC 4
74174 E84
CEC 5
CEC 6
CEC 7
CEC 8
CEC 9
CEC 10
74174 E85
CEC 11
CEC 12
CEC 13
CEC 14
CEC 15
CEC 16
74174 E86
CEC 16 (1) H
R54 1K
HIGH 1 (21 LOADS)
R55 1K
HIGH 2 (21 LOADS)
R56 1K
HIGH 3 (21 LOADS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
FLOPPY DISK CONTROLLER (D7)	D	CS	M7726-Ø-1	J
SCALE	SHEET 7 OF 9	DIST.		

+5V
P/O J1
RX RUN L
RX 12 BIT L
RX DATA (1) L
E31 390
E30 180
E29 390
E28 180
E27 390
E26 180
8640 E10
HIGH 2
BTP 3 H
74S74 E52
DATA I L
7404 E64
SEP DATA (1) L
SR MSB (1) H
MIS CLK (1) L
7486 E74
SRMSB EQ SEP DATA H
MIS CLK EQ SRMSB H
STB
74150 E49
D0 D1 D2 CONDITION D11 SELECTOR D13
SYN INDEX (1) H
SR MSB (1) H
CNTR OVFLW H
CRC 16 (1) H
HOME H
SEP CLK (1) H
SEC BUF OVFLW H
SEC BUF OUT (1) H
FLAG (1) H
OB3 (1) H
D3 D4 D5 D6 D7 D8 D9 D12 D14 D15 D1
S3 S2 S1 S0
SEL 3 (1) H
SEL 2 (1) H
SEL 1 (1) H
SEL 0 (1) H
P/O J2
DRV SEL
WT PROT L
P/O J1
RX INIT L
R33 150
8881 E2
DRV INIT + PC
P/O J4
+10 V
D1 IN4004
D2 IN4004
D3 IN4004
R34 261 1%
R35 300
R36 287 1%
R38 180
R37 10K
Q1 A55
Q2 A85
R39 100 1/2W
D4 IN746A 3.3V
P/O J3
B1 +7V
A2 +5V
C2 GND
8640 E66
INIT + PC H
7437 E65
INIT + PC L
INIT + PC A L
HIGH 2
INST DIS H
INST Ø (1) L
7402 E54
INST DIS L
INST 1 (1) L
7410 E43
DO INST L
INST Ø (1) H
7427 E53
7427 E58
WBR H
CBR L
CI (1) A H
CI (1) L
74H10 E51
74H10 E61
TP3 H
CNTR OVFLW H
7404 E69
7400 E57
7410 E43
CLK SP ADDR REG L
7400 E57
CNTR OVFLW H
74H11 E56
74H20 E55
74H11 E56
PC LOAD EN L
74H20 E55
LDMB ↑CLK PC L
7400 E57
TP4 H
WBR CLK CNTR L
JUMP L
+5V
R57 3K
MAINT DISABLE L
74H74 E58
INST DIS H
INST DIS L
TP4 L
INIT + PC A L
HIGH 2
C Ø (1) L
74H74 E68
CLK CNTR L
74H04 E61

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
FLOPPY DISK CONTROLLER (D8)	D	CS	M7726-Ø-1	J
SCALE —	SHEET 8 OF 9	DIST.		

THIS LIST GIVES THE SOURCE AND DESTINATIONS OF SIGNAL NAMES WITHIN THE M7726 PRINT SET. SIGNAL NAMES THAT DO NOT APPEAR ON THIS LIST ARE PRESENT FOR INFORMATION ONLY. THEY DO NOT INDICATE CONNECTIONS TO OTHER POINTS IN THE PRINT SET.

INTERFACE	REFERS TO SIGNALS ON THE INTERFACE BUSS
DRIVE	REFERS TO SIGNALS ON THE DRIVE BUSS
POWER SUPPLY	REFERS TO VOLTAGES FROM THE POWER SUPPLY
KM11	REFERS TO SIGNALS ON J3 THE MAINTANENCE CONNECTOR

SIGNAL NAME	ORIGIN	DESTINATION
BTP 3 H	D7-C1	D4-A5,D5-A6,D8-D6
CLK BAR L	D5-C7	D4-A3
CLK CNTR L	D5-B7	D3-B7,D8-A4
CLK CRC L	D5-C7	D7-B7
CNTR OVFLW H	D3-C5	D8-D4,D8-C6,D8-B4
CLK SEC BUF L	D5-C7	D4-B2
CLK SP ADDR REG L	D8-B3	D3-A4
CLK SR L	D5-B7	D3-B4
CONTIN L	KM11	D7-C7
CRC16 (1) H	D7-B1	D8-C6
CRC16 (1) L	D7-A1	D7-B7
C1 (1) AH	D3-A6	D4-B3,D5-B4,D8-D4,D8-C4
C1 (1) H	D3-A6	D3-C6,D3-B2,D7-B8
C1 (1) L	D3-A6	D5-D6,D7-B9,D8-D4,D8-B4
C0 (1) H	D3-A6	D3-C7,D3-A2,D4-B1,D5-B4,D7-B8
C0 (1) L	D3-A6	D3-B2,D4-B3,D7-B8,D8-B3
DATA I L	D8-D5	D4-A2
DISABLE ROMS L	TEST PAD	D6-D8
DO INST L	D8-B4	D5-B8
DRV BUSS H	D5-D4	D4-A4
DRV ERASE H	D5-B1	DRIVE
DRV OUT H	D5-C1	DRIVE
DRV LOAD HEAD H	D5-A1	DRIVE
DRV STEP L	D5-C1	DRIVE
DRV INIT + PC	D8-B6	DRIVE
DRV ABOVE TK 43 H	D5-B1	DRIVE
DRV RAW DATA L	DRIVE	D4-A8
DRV SEL DK 1 H	D5-B1	DRIVE
DRV SEL INDX H	DRIVE	D5-A1
DRV SEL TRK 0 H	DRIVE	D5-B1
DRV WT DATA	D5-B1	DRIVE
DRV WT GATE H	D5-C1	DRIVE
DRV SEL WT PROT L	DRIVE	D8-C8
END WIND L	D4-D3	D4-D8
ERROR HLT ENABLE L	KM11	D7-C7
OB1 (1) H	D5-D4	D7-B8
OB3 (1) H	D5-C4	D8-B6
PC 0 (1) H	D6-A1	KM11
PC 1 (1) H	D6-A1	KM11
PC 2 (1) H	D6-A1	KM11
PC 3 (1) H	D6-A1	KM11
PC 4 (1) H	D6-A1	KM11
PC 5 (1) H	D6-A1	KM11
PC 6 (1) H	D6-A1	KM11
PC 7 (1) H	D6-A1	KM11
PC LOAD EN L	D8-D1	D6-A8
ROM OUT 0	D6-D1	D3-C8
ROM OUT 1	D6-D1	D3-C8
ROM OUT 2	D6-D1	D3-C8
ROM OUT 3	D6-D1	D3-C8
ROM OUT 4	D6-D1	D3-C8
ROM OUT 5	D6-D1	D3-D8
ROM OUT 6	D6-D1	D3-D8
ROM OUT 7	D6-D1	D3-D8
RX DATA (1) L	D5-C1,INTERFACE	INTERFACE,D8-D8
RX DONE L	D5-D1	INTERFACE
RX ERROR L	D5-D1	INTERFACE
RX INIT L	INTERFACE	D8-B8
RX OUT L	D5-D1	INTERFACE
RX RUN L	INTERFACE	D8-D8
RX SHIFT L	D5-C1	INTERFACE
RX TRANSFER REQUEST	D5-D1	INTERFACE
RX 12 BIT L	INTERFACE	D8-D8
SEC BUF OVFLW H	D4-A1	D8-C6
SEC BUF OUT (1) H	D4-C1	D5-C4,D8-B6
SEC BUF H	D5-A4	D5-C4
SEL 0 (1) H	D3-A6	D5-C8,D6-C8,D8-B6,KM11
SEL 1 (1) H	D3-A6	D5-C8,D6-C8,D8-B6,KM11
SEL 2 (1) H	D3-B6	D5-C8,D6-C8,D8-B6,KM11
SEL 3 (1) H	D3-B6	D5-C8,D6-C8,D8-B6,KM11
SEP CLK (1) H	D4-B4	D8-C6
SEP DATA (1) H	D4-A5	D3-A2
SEP DATA (1) L	D4-B5	D4-A2,D7-A8,D8-C8
SR H	D5-B4	D5-C4
SR LOAD H	D3-B1	D3-C4
SR MSB (1) H	D3-D3	D5-C4,D8-C8,D8-C6
SYN INDEX (1) H	D5-A5	D8-C6
FLAG (1) H	D5-B3	D8-B6
FLD 0 L	D6-D6	D6-A3,D6-A2
FLD 1 L	D6-D6	D6-B3,D6-B2
FLD 2 L	D6-D6	D6-C3,D6-C2
FLD 3 L	D6-D6	D6-A6,D6-A4
FLD 4 L	D6-D6	D6-B6,D6-B4
FLD 5 L	D6-D6	D6-C6,D6-C4
HALT H	D7-C3	KM11
HALT L	KM11	D7-C7
HIGH 1	D7-C4	D3-D6,D3-B4,D3-C6,D3-C4,D4-A3 D6-B1,D5-D5,D6-A8
HIGH 2	D7-B4	D4-A5,D5-B7,D8-A7,D8-B4,D7-D5 D7-D4,D7-C4,D7-C5,D8-D5,D8-B3 D8-A5
HIGH 3	D7-B4	D4-D8,D4-C8,D4-B7,D4-D5,
NONE H	D5-B2	D8-C6
INIT +PC A L	D8-A4	D3-C6,D3-B4,D3-A4,D3-A7,D4-B6 D4-B5,D6-B8,D7-C5,D8-B2
INIT + PC H	D8-A4	D4-D5,D4-C5,D7-D4
INIT + PC L	D8-A4	D4-B3,D5-B5,D6-A8
INST 0 (1) H	D3-B6	KM11,D8-B5
INST 0 (1) L	D3-B6	D8-C5
INST 1 (1) H	D3-B6	KM11
INST 1 (1) L	D3-B6	D8-B5
INST DIS H	D8-B1	D8-C5
INST DIS L	D8-B1	D8-B5
INTERF BUSS H	D5-D4	D7-B8
JUMP L	D8-C3	D4-C8
LD MM + CLK PC L	D8-C1	D6-A4,D3-A8
LD SCRATCH PAD L	D5-A6	D3-B3
MAINT DIS L	TEST PAD	D8-B1
MIS CLK (1) L	D4-C4	D8-C8
MUX OUT 0	D3-C7	D6-A8
MUX OUT 1	D3-C7	D6-A8
MUX OUT 2	D3-C7	D6-A8
MUX OUT 3	D3-C7	D6-B8
MUX OUT 4	D3-C7	D6-B8
MUX OUT 5	D3-D7	D6-B8
MUX OUT 6	D3-D7	D6-B8
MUX OUT 7	D3-D7	D6-B8
TP3 H	D7-D3	D7-C6,D8-B4,D8-C5
TP3 L	D7-D3	D5-B8
TP4 H	D7-D2	D8-C3
TP4 L	D7-D3	D8-B2
WRR CLK CNTR L	D8-C2	D3-B7
20 MHZ CLK	D7-C5	D4-C8,D4-D7
GND	POWER SUPPLY	D1-A4
+5V	POWER SUPPLY	D1-A4,D8-A7
+7V	D8-A7	KM11
+10V	POWER SUPPLY	D8-B8

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RXØ1		PARTS LIST		

DRN	DATE 19 FEB. 76	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D	DATE 19 FEB. 76	
ENG	DATE 2/19/76	TITLE: FLOPPY CONTROLLER FIRMWARE
PROJ. ENG.	DATE 2/23/76	
PROD.	DATE 2/23/76	
NEXT HIGHER ASSEMBLY		SIZE K · CODE SP · NUMBER RXØ1-Ø-2 · REV.
SCALE		DIST.
SHEET 1 OF 1		

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRB 109

```
                        /RX01 FLOPPY CONTROLLER FIRMWARE


                        /THIS SYMBOL TABLE REPLACES THE NORMAL PAL SYMBOL TABLE AND DEFINES
                        /THE INSTRUCTIONS POSSIBLE BY THE RX01 CONTROLLER




                        /DO INSTRUCTIONS


          0002    SET=2
          0000    CLR=0
          0002    ONE=2
          0000    ZERO=0

          0000    IOB0=0                  /INTERFACE-DISK BUSS OUTPUT BUFFER
          0004    IOB1=4
          0010    IOB2=10
          0014    IOB3=14
          0020    IOB4=20
          0024    IOB5=24
          0030    IOB6=30

          0000    INTERF=CLR IOB0         /IOB0 SELECTS EITHER INTERFACE OR DISK BUSS.  CLR= INTERFACE
          0002    DISK=SET IOB0           /SET=DISK

                                          /INTERFACE BUFFER DEFINITIONS
          0004    ERR=IOB1                /SET TO INDICATE THAT AN RX01 ERROR HAS OCCURED
          0010    XREQ=IOB2               /SET TO REQUEST AN RX01 WORD TRANSFER
          0014    IOOUT=IOB3              /DIRECTION FOR DATA LINE.  SET=TO INTERFACE
          0020    DONE=IOB4               /SET TO INDICATE RX01 READYNESS TO ACCEPT A COMMAND
          0024    SHIFT=IOB5              /SHIFT FOR DATA LINE
          0030    SECDAT=IOB6             /SELECTS SOURCE FOR DATA OUT OF CONTROLLER ON DATA LINE
                                          /SET=SECTOR BUFFER   CLR=SHIFT REGISTER MOST SIG BIT

                                          /DISK BUFFER DEFINITIONS
          0004    WGATE=IOB1              /WRITE CURRET ENABLE WHEN SET
          0010    STPHD=IOB2              /HEAD STEP.  TWO PULSES REQUIRED FOR EACH TRACK
          0014    HDOUT=IOB3              /DIRECTION OF HEAD MOTION
          0020    EGATE=IOB4              /ERASE CURRENT ENABLE
          0024    LOWCUR=IOB5             /SPECIFIES WRITE CURRENT LEVEL

          0034    UNIT=34                 /SELECTS ONE OF TWO DRIVES.  UNIT (ZERO)(ONE)

          0040    UNHD=40                 /DEACTIVATES HEAD LOAD SOLONOID OF SELECTED DRIVE
          0042    LDHD=42                 /ACTIVATES HEAD LOAD SOLONOID OF SELECTED DRIVE

          0044    BAR=44                  /SECTOR BUFFER ADDRESS REGISTER CONTROL
          0001    LONG=1                  /FORMAT:  CLR BAR (SHORT)(LONG)
          0000    SHORT=0                 /SHORT PRESETS FOR COUNT OF 1024
          0002    INCR=2                  /LONG PRESETS FOR COUNT OF 4096
                                          /FORMAT:  INCR BAR    INCREMENT THE BUFFER ADDRESS REG.
```



```
          0050    WRTBUF=50               /SECTOR BUFFER WRITE CLOCK
          0003    START=3                 /FORMAT:  (START)(FIN) WRTBUF
          0000    FIN=0                   /A 750NS MINIMUM PULSE IS REQUIRED

                                          /CRC REGISTER CONTROL
          0054    CRC=54                  /FORMAT:  CRC (ONE)(ZERO)   SPECIFIES DATA TO
                                          /BE JAMMED INTO CRC GENERATOR/CHECKER
          0057    PRECRC=57               /PRESETS CRC REG TO ALL ONES
          0055    DATCRC=55               /SHIFTS SEPERATED DATA INTO CRC CIRCUIT

                                          /GENERAL PURPOSE FLAG CONTROL
          0060    FLAG=60                 /FORMAT:  FLAG (ON)(OFF)(TOG)
          0002    ON=2                    /SET FLAG
          0001    OFF=1                   /CLR FLAG
          0003    TOG=3                   /TOGGLE FLAG

          0064    LSP=64                  /LOAD OPEN SCRATCHPAD REG WITH CONTENTS OF SHIFT REG

          0070    LCT=70                  /LOAD COUNTER WITH CONTENTS OF NEXT ROM LOCATION
          0071    ESP=71                  /LOAD COUNTER WITH CONTENTS OF OPEN SCRATCHPAD
          0073    ICT=73                  /INCREMENT COUNTER

                                          /SHIFT REGISTER CONTROL
          0074    ROTATE=74               /FORMAT: ROTATE(ONE)(ZERO)
                                          /SHIFTS SHIFT REG TOWARDS MOST SIGNIFICANT BIT
                                          /WHILE INSERTING A ONE OR ZERO INTO THE LEAST
                                          /SIGNIFICANT BIT
          0075    LSR=75                  /LOAD SHIFT REGISTER WITH CONTENTS OF COUNTER
          0077    DATSR=77                /SHIFT REG TOWARDS MSB WHILE INSERTING SEPERATED
                                          /DATA INTO LSB
```

```
                        /BRANCH INSTRUCTIONS AND CONDITIONS

0100    BR=100          /FORMAT:  BR COND (T)(F)(ONE)(ZERO)
                        /IF CONDITION IS MET,  A BRANCH IS MADE WITHIN
                        /THE CURRENT FIELD USING THE CONTENTS OF THE
                        /NEXT ROM LOCATION AS THE BRANCH ADDRESS
                        /IF THE CONDITION IS NOT MET,  THE NEXT ROM LOCATION
                        /IS IGNORED AND THE FOLLOWING INSTRUCTION IS EXECUTED
0300    WBR=300         /FORMAT:  WBR COND (T)(ONE)
                        /THE COUNTER IS INCREMENTED WITH EVERY EXECUTION OF
                        /THIS INSTRUCTION,  THE WBR IS REPEATEDLY
                        /EXECUTED UNTILL EITHER THE COUNTER OVERFLOWS OR
                        /THE CONDITION IS MET.  IF THE CONDITION IS MET
                        /THE BRANCH IS MADE.  IF THE COUNTER OVERFLOWS
                        /THE BRANCH ADDRESS IS IGNORED AND THE NEXT INSTRUCTION
                        /IS EXECUTED
0000    F=ZERO          /REQUIRES THE CONDITION TO BE FALSE
0002    T=ONE           /REQUIRES THE CONDITION TO BE TRUE
0001    IND=1           /IF APPENDED TO THE JUMP, BR OR WBR INSTRUCTION,
                        /CAUSES THE BRANCH ADDRESS TO BE TAKEN FROM THE
                        /OPEN SCRATCHPAD RATHER THAN FROM THE NEXT ROM LOCATION

0000    RUN=0           /WHEN ASSERTED INDICATES THAT THE INTERFACE HAS
                        /SERVICED A TRANSFER REQUEST, OR THAT A COMMAND
                        /IS PENDING
0004    IOB3OT=4        /INTERF/DISK OUTPUT BUFFER BIT 3
0010    DATAIN=10       /BIDIRECTIONAL DATA LINE BETWEEN INTERFACE AND CONTROLLER
0014    INDX=14         /DRIVE INDEX LATCH
0020    SR7=20          /SHIFT REGISTER MOST SIGNIFICANT BIT
0024    COFL=24         /OVERFLOW (ALL ONES) OF THE COUNTER
0030    CRC16=30        /BIT 16 OF CRC GENERATOR/CHECKER
0034    HOME=34         /TRACK ZERO OF SELECTED DRIVE ANDED WITH HEAD
                        /DIRECTION BEING OUT
0040    WRTEN=40        /WRITE ENABLED STATUS OF THE SELECTED DRIVE
0044    SEPCLK=44       /SEPERATED CLOCK FROM DISK DATA
0050    XIIBIT=50       /ASSERTED IF INTERFACE TRANSFERS ARE TO BE AS
                        /12 BIT WORDS RATHER THAN 8 BIT BYTES
0054    DEQSR7=54       /SEPERATED DATA EQUAL TO SHIFT REG BIT 7
0060    BAROFL=60       /OVERFLOW CONDITION (ALL ONES) OF THE SECTOR BUFFER
                        /ADDRESS REGISTER
0064    MCEQSR=64       /MISSING CLOCK EQUAL TO SHIFT REG BIT 7
0070    BDATAO=70       /OUTPUT OF SECTOR BUFFER
0074    FLAGO=74        /STATE OF GENERAL PURPOSE FLAG
```



```
                        /SCRATCHPAD REGISTER SELECTION

0200    OPEN=200        /FORMAT: OPEN X  WHERE X IS ONE OF THE SCRATCHPAD REG
                        /THIS INSTRUCTION MAKES THE NAMED SCRATCHPAD
                        /ACCESSABLE VIA THE LSP AND ESP COMMANDS

0000    R0=0            /DEFINITIONS OF SCRATCHPADS BY R#
0004    R1=4
0010    R2=10
0014    R3=14
0020    R4=20
0024    R5=24
0030    R6=30
0034    R7=34
0040    R8=40
0044    R9=44
0050    R10=50
0054    R11=54
0060    R12=60
0064    R13=64
0070    R14=70
0074    R15=74

                        /DEFINITION OF SCRATCHPADS BY MNEUMONICS
0000    CURTK0=R0       /CURRENT TRACK ADDRESS OF DRIVE 0
0004    CURTK1=R1       /CURRENT TRACK ADDRESS OF DRIVE 1
0010    ERREG=R2        /DEFINITIVE ERROR CODE IF ANY
0014    STAT=R3         /STATUS WORD OF RX01
0020    TARTRK=R4       /TARGET TRACK OF CURRENT DISK ACCESS
0024    TARSEC=R5       /TARGET SECTOR OF CURRENT DISK ACCESS
0030    TEMPA=R6        /TEMPORARY STORAGE
0034    TEMPB=R7        /TEMPORARY STORAGE
0040    TEMPC=R8        /TEMPORARY STORAGE
0044    TEMPD=R9        /BIT 7 IS UNIT SELECT BIT.  0 MEANS UNIT 1
0050    TEMPE=R10       /BIT 7 IS HEAD LOADED BIT.  1 MEANS HEAD LOADED
0054    TEMPF=R11       /TEMPORARY STORAGE
0060    TEMPG=R12       /TEMPORARY STORAGE
0064    RTNB=R13        /RETURN ADDRESS FOR 3RD LEVEL NESTED SUBROUTINES
0070    RTNA=R14        /RETURN ADDRESS FOR 2ND LEVEL NESTED SUBROUTINES
0074    RTN=R15         /RETURN ADDRESS FOR 1ST LEVEL SUBROUTINES
```

```
                        /JUMP INSTRUCTION AND JUMP FIELD DEFINITIONS
                        
0202    JUMP=202                /FORMAT:  JUMP FX (IND)
                                /CAUSES A BRANCH TO ONE OF SIX ROM FIELDS (0-5)
                                /SPECIFIED BY X.  THE BRANCH ADDRESS IS TAKEN FROM
                                /THE ROM LOCATION FOLLOWING THE JUMP INSTRUCTION.
                                /IF IND IS APPENDED, THE BRANCH ADDRESS
                                /IS TAKEN FROM THE OPEN SCRATCH PAD
                        
0000    F0=0
0004    F1=4
0010    F2=10
0014    F3=14
0020    F4=20
0024    F5=24
```



```
                        
                        
                        
                        
                        
                        
                        
                        /TABLE OF DEFINITIVE ERROR CODES
                        
0010    KNXDV0=10               /DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
0020    KNXDV1=20               /DRIVE 1 FAILED TO SEE HOME ON INITIALIZE.  DOES NOT CAUSE ERROR
0030    KWRONG=30               /FOUND HOME WHEN STEPPING IN 10 TRACKS FOR INIT
0040    KERTRK=40               /TRIED TO ACCESS A TRACK GREATER THAN 76
0050    KHOMERR=50              /HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED
0060    KSELFER=60              /SELF DIAGNOSTIC ERR
0070    KNXHDR=70               /DESIRED SECTOR COULD NOT BE FOUND AFTER LOOKING
                                /AT 52 HEADERS
0100    KWPROT=100              /WRITE FUNCTION ATTEMPTED ON A WRITE PROTECTED DISK
0110    KTIMERR=110             /MORE THAN 40 MICROSECONDS AND NO SEPCLOCK SEEN
0120    KNXPRAM=120             /A PREAMBLE COULD NOT BE FOUND
0130    KNXIDAM=130             /PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME
0140    KHCRCER=140             /CRC ERROR ON WHAT APPEARED TO BE A HEADER.  ERROR IS NOT ASSERTED
0150    KTKSKER=150             /THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE
                                /WITH THE DESIRED TRACK
0160    KXSTRYS=160             /TOO MANY TRIES FOR AN IDAM
0170    KNODAM=170              /DATA AM NOT FOUND IN ALLOTTED TIME
0200    KDCRCER=200             /CRC ERROR ON READING THE SECTOR FROM THE DISK
0210    KPARER=210              /PARITY ERROR ON SOME WORD FROM THE INTERFACE
                        
```

```
                        /[ROUTINE: INITIALIZE]  IF A HOST PROCESSOR INITIAL... OR AN
                        /RX01 POWER LOW IS DETECTED, THE PC IS CLEARED AND THE RX01 TIMING
                        /STOPS.  UPON THE NEGATION OF INITIALIZE, TIMING RESUMES AND A SELF TEST OF
                        /INTERNAL DATA PATHS IS MADE.  IF AN ERROR OCCURS HERE,  ERROR AND
                        /DONE ARE SET, BUT ERREG IS NOT ALTERED.  THEN IF NO ERROR HAS OCCURRED AN ATTEMPT
                        /IS MADE TO RECALABRATE DRIVE 1 THEN DRIVE 0.  IF DRIVE 0 FAILS TO RECALIBRATE,
                        /THE ERROR CODE IS LOADED INTO ERREG AND ERROR IS SET.  IF DRIVE
                        /2 RECALIBRATES AND IS READY (DISK LOADED) SECTOR ONE OF TRACK ONE
                        /IS READ INTO THE SECTOR BUFFER.  IT IS POSSIBLE FOR A READ ERROR
                        /TO OCCUR WHILE READING THIS SECTOR.

          0000      *2000
                            DECIMAL

     3000 0210              OPEN ERREG      /CLEAR ERROR REGISTER
     0001 0064              LSP

     0002 0222              JUMP F4         /GO DO THE INITIALIZE DIAGNOSTIC ROUTINE
     0003 2352              TEST

     0004 0070  TSTRTN,     LCT             /RETURN FROM SUCCESSFUL DIAGNOSTIC ROUTINE
                            OCTAL
     0005 0004              4
                            DECIMAL
     0006 0075              LSR             /SET THE INIT DONE BIT OF STAT
     0007 0214              OPEN STAT
     0010 0064              LSP

     0011 0070              LCT             /SET UP SOME SCRATCHPAD REGISTERS
     0012 0377              -1
     0013 0075              LSR
     0014 0244              OPEN TEMPD      /UNIT 0 TO SOFT UNIT BIT
     0015 0064              LSP
     0016 0200              OPEN CURTK0     /NEG ZERO TO BOTH CURRENT TRACK ADDRESSES
     0017 0064              LSP
     0020 0204              OPEN CURTK1
     0021 0064              LSP

     0022 0074              ROTATE ZERO     /NEG ONE TO TARGET SECTOR
     0023 0224              OPEN TARSEC
     0024 0064              LSP
     0025 0220              OPEN TARTRK     /NEG ONE TO TARGET TRACK FOR INITIALIZE BOOTSTRAP
     0026 0064              LSP

     0027 0002              DISK            /SELECT DISK RUSS

     0030 0070              LCT             /CALL SUBROUTINE TO LOAD HEAD AND WAIT 25 MS
     0031 0034              RECAL1          /TO ALLOW POWER UP DRIVE SETTLE TIME
     0032 0222              JUMP F4
     0033 2145              DLY25

     0034 0036  RECAL1,     UNIT ONE        /SELECT UNIT ONE FOR RECALIBRATE

     0035 0214  RECAL0,     CLR HDOUT       /STEP HEAD IN 1" TRACKS TO ASSURE IT IS NOT BEHIND TRACK 0
```



```
     0036 0070              LCT
     0037 0365              -10-1
     0040 0075              LSR
     0041 0070              LCT
     0042 0045              IN10
     0043 0222              JUMP F4
     0044 2100              STEPHD

     0045 0226  IN10,       JUMP F5         /ERROR,  HOME WAS SEEN WHILE STEPPING IN,
     0046 2621              WRONG

     0047 0215              SET HDOUT       /STEP OUT AS MANY AS 80 TRACKS IN SEARCH OF HOME
     0050 0070              LCT
     0051 0257              -80-1
     0052 0075              LSR
     0053 0070              LCT
     0054 0060              RCALOK
     0055 0040              UNHD
     0056 0222              JUMP F4
     0057 2100              STEPHD

     0060 0202  RCALOK,     JUMP F0         /HOME WAS FOUND OK
     0061 0075              WHCHDR

     0062 0174              BR FLAGO F      /IF FLAG=0 RECALIBRATE WAS ON DRIVE 1
     0063 0070              NXDRV1

     0064 0070  NXDRV0,     LCT             /RECALABRATE FAILURE WAS ON DRV 0
     0065 0010              KNXDV0
     0066 0226              JUMP F5
     0067 2610              GOERDN

     0070 0070  NXDRV1,     LCT             /RECAL FAILURE WAS ON DRV 1, LOG ERROR
     0071 0020              KNXDV1          /AND CONTINUE RECALIBRATION
     0072 0075              LSR
     0073 0210              OPEN ERREG
     0074 0064              LSP

     0075 0176  WHCHDR,     BR FLAGO T      /IF FLAG=1 BOTH DRIVES HAVE BEEN RECALIBRATED
     0076 0372              PONRCL

     0077 0062              FLAG ON         /SET FLAG TO INDICATE DRV 0 IS BEING RECALIBRATED

     0100 0034              UNIT ZERO

     0101 0202              JUMP F0         /GO BACK AND RECALIBRATE DRV0
     0102 0035              RECAL0
```

```
                        /[SUBROUTINE: FINDTRACK]
                        /THIS SUBROUTINE IS USED TO LOCATE A SPECIFIED SECTOR. IT PICKS
                        /UP THE TRACK AND SECTOR ADDRESS FROM THE INTERFACE, CHECKS THAT
                        /THE TRACK ADDRESS IS LEGAL (NOT GREATER THAN 114 OCTAL.), MOVES THE
                        /HEAD OF THE SELECTED DRIVE TO THE SPECIFIED TRACK, VERIFIES
                        /TRACK POSITION, AND LOCATES THE CORRECT SECTOR. EXIT FROM
                        /THIS SUBROUTINE OCCURS AT WRITE TURN ON TIME OF THE SELECTED.
                        /SECTOR. ENTRANCE IS MADE WITH THE RETURN ADDRESS IN THE COUNTER


0103  0075    FINDTR, LSR             /SAVE THE RETURN ADDRESS
0104  0274            OPEN RTN
0105  0064            LSP

0106  0070            LCT             /CLEAR THE ERROR REGISTER
0107  0000            0
0110  0075            LSR
0111  0210            OPEN ERREG
0112  0064            LSP

0113  0244            OPEN TEMPD      /SOFT UNIT BIT TO SR
0114  0071            ESP
0115  0075            LSR

0116  0122            BR SR7 ONE      /IF SR=1  DRIVE 0 IS CURRENTLY SELECTED
0117  0127            UZERO

0120  0174    UONE,   BR FLAGO ZERO   /IF FLAG=0 DRIVE 1 IS DESIRED AND ALREADY SELECTED
0121  0141            USAME

0122  0034            UNIT ZERO       /DRIVE 0 IS DESIRED AND DRIVE1 WAS SELECTED,  SELECT 0

0123  0070            LCT             /SET UP SOFT UNIT SELECT AS DRIVE 0
                      OCTAL
0124  0200            200
                      DECIMAL

0125  0202            JUMP F0         /GO STORE SOFT UNIT BIT
0126  0134            UDIF

0127  0176    UZERO,  BR FLAGO ONE    /IF FLAG=1 DRIVE 0 IS DESIRED AND ALREADY SELECTED
0130  0141            USAME


0131  0036            UNIT ONE        /DRIVE 1 IS DESIRED BUT DRIVE0 IS SELECTED, SELECT DRIVE 1
0132  0070            LCT             /SET UP SOFT UNIT SELECT BIT AS DRIVE 1
0133  0001            0

0134  0075    UDIF,   LSR             /STORE SOFT UNIT SELECT BIT
0135  0064            LSP

0136  0074            ROTATE ZERO     /CLR SOFT HD LOAD BIT BECAUSE UNITS CHANGED
```



```
0137  0250            OPEN TEMPE
0140  0064            LSP

0141  0070    USAME,  LCT             /CALL GETWORD SUBROUTINE FOR THE SECTOR ADDRESS
0142  0145            PUTSEC
0143  0222            JUMP F4
0144  2000            GETWRD


0145  0070    PUTSEC, LCT             /MAKE FIRST BIT OF COMPLIMENTED SECTOR ADDRESS A 1 REGARDLESS OF DATA
0146  0370            -7-1
0147  0076            ROTATE ONE
0150  0126            BR COFL T
0151  0160            .+7
0152  0073            ICT
0153  0122            BR SR7 T
0154  0147            .-5
0155  0074            ROTATE ZERO
0156  0202            JUMP F0
0157  0150            .-7

0160  0224            OPEN TARSEC     /PUT THE TARGET SECTOR AWAY
0161  0064            LSP

0162  0070            LCT             /CALL GETWRD SUBROUTINE FOR TRACK ADDRESS
0163  0166            PUTTRK
0164  0222            JUMP F4
0165  2000            GETWRD


0166  0220    PUTTRK, OPEN TARTRK     /STASH THE TRACK ADDRESS
0167  0064            LSP

0170  0254            OPEN TEMPF      /START SETUP FOR COMPARING THE
0171  0064            LSP             /TARGET TRACK AND TRACK 76
0172  0260            OPEN TEMPG      /F= TARGET TRACK
0173  0070            LCT             /G= 77
0174  0262            -77-1
0175  0075            LSR
0176  0064            LSP

0177  0070            LCT             /CALL SUBR MAGCOM TO SEE IF TARGET TRACK
0200  0206            ILTRK           /IS GREATER THAN 114 OCTAL,  76 DECIMAL.
0201  0075            LSR
0202  0270            OPEN RTNA
0203  0064            LSP
0204  0226            JUMP F5
0205  2400            MAGCOM


0206  0202    ILTRK,  JUMP F0         /TARGET TRACK IS 77, ILLEGAL ADDRESS
0207  0242            ERTRK           /GO, REPORT THE ERROR
0210  0202            JUMP F0         /TARGET TRACK IS GREATER THAN 77
0211  0242            ERTRK           /GO, REPORT THE ERROR
```

```
                                OPEN TEMPD      /TARGET TRACK IS OK, GET THE DRIVE
                                ESP             /SELECT FROM TEMPD
                                LSR
                                OPEN CURTK0     /PRESELECT UNIT 0
                                DISK            /SELECT DISK RUNS
                                BR SR7 ONE      /WHICH UNIT SELECTED? BIT7=0 MEANS UNIT ONE
                                .+2             /ZERO, SKIP UNIT 1 SETUP
                                OPEN CURTK1
                                ESP             /PASS SELECTED CURRENT TRACK TO MAGCOM SUBR
                                LSR
                                OPEN TEMPG
                                LSP
                                OPEN TARTRK     /PASS TARGET TRACK TO MAGCOM SUBROUTINE
                                ESP
                                LSR
                                OPEN TEMPF
                                LSP
                                LCT             /CALL SUBROUTINE MAGCOM TO SEE IF TARGET
                                TRKEQ           /IS SAME AS CURRENT TRACK,  F=TARGET,  0=CURRENT
                                LSR
                                OPEN RTNA
                                LSP
                                JUMP F5
                                MAGCOM

ERTRK,  LCT
                                KERTRK          /TRIED TO ACCESS A TRACK GREATER THAN 76 DECIMAL
                                JUMP F5
                                GOERDN

TRKEQ,  JUMP F0         /TARGET EQUALS THE CURRENT TRACK, NO
                        /STEPS ARE REQUIRED
                        OPEN RTNA       /NOOP;  TARGET > ACTUAL RETURN
                        OPEN RTNA       /NOOP

BOOT,   OPEN RTNA       /TARGET IS LESS THAN ACTUAL, STEPS NEEDED ALSO START OF
                        LCT             /OF BOOT SUBROUTINE,  SET UP RETURN FROM DIF SUBR
                        STPOUT
                        LSR
                        LSP

                        OPEN TEMPD      /SOFT UNIT SELECT BIT TO SR7
                        ESP
                        LSR

                        OPEN CURTK1     /PRESELECT UNIT 1

                        BR SR7 ZERO     /SR7=0 MEANS UNIT ONE
```



```
                                .+2
                                OPEN CURTK0

                                ESP             /PASS SELECTED CURRENT TRACK TO DIFF SUBR VIA SR
                                LSR

                                OPEN TARTRK     /PASS TARGET TRACK TO DIF VIA CNTR
                                ESP

                                SET HDOUT       /ASSUME A STEP OUT

                                JUMP F5         /GO TO THE SUBROUTINE DIF TO CALCULATE THE STEPS NEEDED
                                DIF


STPOUT, JUMP F0         /TARGET TRACK IS LESS THAN
                        .+2             /THE ACTUAL,  MOVE OUT IS NECESSARY

                        CLR HDOUT       /TARGET IS GREATER THAN ACTUAL.  STEPS IN NEEDED

                        LCT             /COMPLEMENT OF STEPS REQUIRED IS IN THE
                        DUNSTP          /SHIFT REG.  SET UP RETURN FROM STPHD SUBR

                        UNHD            /UNLOAD HEAD BEFORE MOVING

                        JUMP F4         /CALL SUBROUTINE STEPHD
                        STEPHD


DUNSTP, JUMP F5         /HOME FOUND BEFORE LAST STEP TAKEN
                        HOMERR

                        OPEN TEMPD      /SOFT UNIT BIT TO SR7
                        ESP
                        LSR
                        OPEN TARTRK     /GET READY TO PASS TARGET TRK TO PROPER
                        ESP             /CURRENT TRACK

                        OPEN CURTK0     /OPEN PROPER CURRENT TRACK REGISTER
                        BR SR7 ONE      /BIT7=0 MEANS UNIT ONE
                        .+2
                        OPEN CURTK1

                        LSR             /UPDATE THE CURRENT TRACK ADDRESS
                        LSP


HDSETL, OPEN TARTRK     /HEAD IS SETTLED DETERMINE IF ABOVE TRACK 43 DECIMAL
                        ESP             /PASS TARGET TO MAGCOM VIA TEMPF
                        LSR
                        OPEN TEMPF
                        LSP

                        LCT             /PASS 44 TO MAGCOM VIA TEMPG
                        -44-1
```

```
 542   0331  0075          LSR
 543   0332  0260          OPEN TEMPG
 544   0333  0064          LSP
 545
 546   0334  0026          SET LOWCUR      /ASSUME TARGET GREATER THAN 43
 547
 548   0335  0070          LCT             /CALL MAGCOM SUBROUTINE
 549   0336  0344          ABV43           /RETURN ADDRESS
 550   0337  0075          LSR
 551   0340  0270          OPEN RTNA
 552   0341  0064          LSP
 553   0342  0226          JUMP F5
 554   0343  2400          MAGCOM
 555
 556
 557   0344  0202  ABV43,  JUMP F0         /NOOP F=G RETURN, ABOVE TRK 43
 558   0345  0346          .+1             /NOOP
 559
 560   0346  0202          JUMP F0         /F<G; ABOVE TRACK 43
 561   0347  0351          .+2
 562
 563   0350  0024          CLR LOWCUR      /F>G;  BELOW TRACK 43,  WRITE WITH HIGH CURRENT
 564
 565   0351  0070  CFINSE, LCT             /CALL FINDSEC SUBROUTINE TO LOCATE THE DESIRED SECTOR
 566   0352  0355          RFINTR
 567   0353  0206          JUMP F1
 568   0354  0714          FINDSE
 569
 570   0355  0274  RFINTR, OPEN RTN        /RETURN FROM FINDTR SUBROUTINE
 571   0356  0207          JUMP F1  IND
 572
 573
 574   0357  0250  NOSTPS, OPEN TEMPE      /NO STEPS REQUIRED
 575   0360  0071          ESP             /SOFT HEAD LOAD BIT TO SR7
 576   0361  0075          LSR
 577
 578   0362  0122          BR SR7 ONE      /IS HEAD LOADED?
 579   0363  0322          HDSETL          /YES, GO UPDATE CURRENT CONTROL
 580
 581   0364  0070          LCT             /NO, GO LOAD HEAD AND WAIT FOR 20MS SETTLE TIME
 582   0365  0322          HDSETL          /RETURN ADDR FROM DLY25 SUBROUTINE
 583   0366  0222          JUMP F4
 584   0367  2145          DLY25
 585
 586
 587   0370  0212  PFUNCT, JUMP F2         /POINTER FROM GETWORD SUBROUTINE TO
 588   0371  1236          FUNCT           /FUNCTION DECODE
 589
 590   0372  0226  PDNRCL, JUMP F5         /POINTER TO DRV RDY CHECK DONE AFTER RECALABRATE
 591   0373  2625          DNRCAL
 592
 593   0374  0000          0               /SPARE LOCATIONS
 594   0375  0000          0               /OPEN
 595   0376  0000          0               /OPEN
 596   0377  0000          0               /OPEN
```



```
 597                   /[ROUTINE: WRITE SECTOR]
 598                   /THIS ROUTINE TURNS ON WRITE GATE AT WRITE TURN ON TIME,
 599                   /WRITES A PREAMBLE OF 6 BYTES OF ZEROES, A DATA OR DELETED DATA MARK,
 600                   /THEN TURNS ON ERASE GATE.  ENTER WITH CNTR=100 IF
 601                   /DELETED DATA, CNTR=0 IF NORMAL DATA MARK.  THE DATA MARK, DATA FIELD,  CRC
 602                   /AND ONE BYTE POSTAMBLE ARE WRITTEN.  WRITE CURRENT IS TURNED OFF.
 603                   /511 MICRO SECONDS LATER ERASE CURRENT IS TURNED OFF.  A HEADER MUST
 604                   /THEN BE READ TO INSURE DISK IS STILL UP TO SPEED BEFORE  THE WRITE
 605                   /SECTOR FUNCTION IS COMPLETE.
 606
 607
 608
 609
 610   0400  0214  WRTSEC, OPEN STAT       /DEL DATA BIT TO STAT6
 611   0401  0075          LSR
 612   0402  0264          LSP
 613
 614   0403  0070          LCT             /CALL SUBROUTINE TO FIND DESIRED TRACK AND SECTOR
 615   0404  0407          S=GATE
 616   0405  0202          JUMP F0
 617   0406  0103          FINDTR
 618
 619   0407  0061  S=GATE, FLAG OFF        /ALWAYS START WRITING WITH WRITE FLOP CLEARED
 620
 621   0410  0140          BR WRTEN F      /GO REPORT ERROR IF NO WRITE ENABLE
 622   0411  0503          PRTERR
 623
 624   0412  0214          OPEN STAT       /DEL DATA BIT TO SR7 AND ENABLE WRT CURRENT
 625   0413  0071          ESP
 626   0414  0006          SET WGATE
 627   0415  0075          LSR
 628   0416  0074          ROTATE ZERO
 629
 630   0417  0234          OPEN TEMPB      /USE TEMPB FOR SECOND HALF DATA AM PATTERN
 631
 632   0420  0057          PRECRC          /JAM THE CRC GENERATOR WITH FIRST 6 BITS OF DATA AM
 633   0421  0056          CRC ONE
 634   0422  0056          CRC ONE
 635   0423  0056          CRC ONE
 636   0424  0056          CRC ONE
 637   0425  0056          CRC ONE
 638   0426  0054          CRC ZERO
 639
 640   0427  0120          BR SR7 ZERO     /DELETED DATA?
 641   0430  0460          DAMSUP          /NO, REGULAR DATA MARK
 642
 643   0431  0070          LCT             /YES, SECOND HALF OF DELETED DATA MARK TO CNTR
 644                       OCTAL
 645   0432  0325          325             /FLUX PATTERN
 646                       DECIMAL
 647
 648   0433  0054          CRC ZERO        /JAM LAST 2 BITS OF DELETED DATA MARK TO CRC GEN.
 649   0434  0054          CRC ZERO
 650   0435  0002          DISK            /NOOP
 651   0436  0002          DISK            /NOOP
```

```
                                
0437  0063    STASH,  TOG FLAG        /END OF THE FIRST 0 BIT
                                
0440  0075            LSR             /PUT SECOND HALF OF THE DESIRED MARK IN THE TEMPB
0441  0064            LSP
                                
0442  0070            LCT             /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
0443  0466            HLFDLY
0444  0075            LSR
                                
0445  0070            LCT             /STALL 1.8 MICRO SECONDS
0446  0374            -3-1
0447  0073            ICT
0450  0124            BR COFL F
0451  0447            .-2
0452  0002            DISK            /NOOP
                                
0453  0070            LCT             /SPECIFY 22 ZEROS TO BE WRITTEN BY WRTBS SUBROUTINE
0454  0351            -22-1
                                
0455  0063            TOG FLAG        /WRITE SECOND CLOCK TRANSITION
                                
0456  0212            JUMP F2         /CALL WRITE ZEROS SUBROUTINE
0457  1322            WRTBS
                                
0460  0070    DAMSUP, LCT             /LOAD SECOND HALF OF NORMAL DATA MARK
                        OCTAL
0461  0337            337
                        DECIMAL
                                
0462  0056            CRC ONE         /JAM LAST 2 BITS OF DATA MARK TO CRC GENERATOR
0463  0056            CRC ONE
                                
0464  0206            JUMP F1         /GO PUT AWAY THE SECOND HALF OF THE DATA MARK
0465  0437            STASH
                                
0466  0002    HLFDLY, DISK            /NOOP
                                
0467  0070            LCT
0470  0514            WRTDAM          /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
0471  0075            LSR
                                
0472  0070            LCT             /NOOP WASTE 2.8 MICRO SECONDS
0473  0351            -22-1           /NOOP
0474  0070            LCT             /NOOP
0475  0351            -22-1           /NOOP
                                
0476  0070            LCT             /SPECIFY 22 BITS TO BE WRITTEN BY WRTBS SUBROUTINE
0477  0351            -22-1
                                
0500  0063            TOG FLAG        /WRITE THE 25TH CLOCK TRANSITION
                                
0501  0212            JUMP F2         /CALL WRTBS SUBROUTINE
0502  1322            WRTBS
                                
```



```
0503  0070    PRTERR, LCT             /SET WRITE PROTECT BIT OF STAT BECAUSE A WRITE FUNCTION WAS ATTEMPTED ON
                                      /ON A WRITE PROTECTED DISKETTE
                        OCTAL
0504  0010            10
                        DECIMAL
0505  0075            LSR
0506  0214            OPEN STAT
0507  0064            LSP
                                
0510  0072            LCT             /ERROR CODE FOR WRT PROTECT ERROR
0511  0100            K-PROT
0512  0226            JUMP F5
0513  2614            GOERDN
                                
                                
                        /THIS ROUTINE WILL WRITE EITHER A DATA MARK OR A
                        /DELETED DATA MARK. THE FIRST HALF OF BOTH MARKS ARE
                        /IDENTICAL. THE SECOND HALF IS SPECIFIED BEFORE ENTRY BY
                        /PUTTING THE SECOND HALF BIT PATTERN IN TEMPB
                                
0514  0070    WRTDAM, LCT             /WASTE 2.8 MICRO SECONDS
0515  0375            -2-1
0516  0073            ICT
0517  0075            LSR
0520  0124            BR COFL F
0521  0516            .-3
                                
0522  0063            TOG FLAG        /WRITE A CLOCK BIT AS END OF 48TH ZERO
                                
0523  0070            LCT             /FIRST HALF OF DATA MARK PATTERN TO SR
                        OCTAL
0524  0352            352
                        DECIMAL
0525  0075            LSR
                                
0526  0070            LCT             /SET TRANSITION LOOP COUNTER FOR 8 LOOPS
0527  0370            -7-1
0530  0002            DISK            /NOOP
                                
0531  0120    AGAIN,  BR SR7 ZERO     /WHATS THE BIT?
0532  0562            A               /ZERO, NO TRANSITION
                                
0533  0044            CLR BAR         /ONE, RESET THE BUFFER ADDR REG TO 0
                                
0534  0063            TOG FLAG        /WRITE FLUX TRANSITION
                                
0535  0126    ABACK,  BR COFL T       /CHECK TRANSITION LOOP COUNT
0536  0543            SECHLF          /GO GET SECOND HALF
                                
0537  0074            ROTATE          /SHIFT NEXT TRANSITION TO SR7
                                
0540  0073            ICT             /BUMP TRANSITION LOOP COUNTER
                                
```

```
 762   0541  0206          JUMP F1          /DO ANOTHER LOOP
 763   0542  0531          AGAIN
 764
 765   0543  0234  SECHLF, OPEN TEMPB       /SECOND HALF OF DATA MARK TO SR
 766   0544  0271          ESP
 767   0545  0075          LSR
 768
 769   0546  0070          LCT              /SET TRANSITION LOOP COUNTER FOR 8 LOOPS
 770   0547  0370          -7-1
 771
 772
 773   0550  0120  AGAIN1, BR SR7 ZERO      /SHALL WE WRITE A TRANSITION?
 774   0551  0564          B                /NO
 775
 776   0552  0263          TOG FLAG         /YES
 777   0553  0002          DISK             /NOOP
 778
 779   0554  0126  BBACK,  BR COFL T        /DONE DATA MARK?
 780   0555  0566          WRTDAT           /YES, GO WRITE DATA
 781
 782   0556  0073          ICT              /NO, BUMP THE LOOP COUNTER
 783
 784   0557  0074          ROTATE           /BRING UP NEXT HALF BIT TO SR7
 785
 786   0560  0206          JUMP F1          /DO ANOTHER LOOP
 787   0561  0550          AGAIN1
 788
 789   0562  0206  A,      JUMP F1          /WASTE 2 CYCLES TO SKIP FLUX TRANSITION
 790   0563  0535          ABACK
 791
 792   0564  0206  B,      JUMP F1          /WASTE 2 CYCLES TO SKIP FLUX TRANSITION
 793   0565  0554          BBACK
 794
 795
 796
 797
 798                 /THIS ROUTINE WRITES THE CONTENTS OF THE SECTOR BUFFER.
 799
 800
 801   0566  0022  WRTDAT, SET EGATE        /TURN ON ERASE CURRENT AT START OF DATA FIELD
 802   0567  0073          ICT              /NOOP; WASTE 2 CYCLES
 803   0570  0073          ICT              /NOOP
 804
 805   0571  0170  DATAA,  BR BDATAO ZERO   /WHATS THE DATA BIT?
 806   0572  0615          C                /ZERO, GO WRITE NOTHING
 807
 808   0573  0056          CRC ONE          /ONE, UPDATE THE CRC WITH 1
 809
 810   0574  0063          TOG FLAG         /WRITE A DATA TRANSITION
 811   0575  0073          ICT              /NOOP FOR BIT CELL TIMING
 812
 813   0576  0162  CBACK,  BR BAROFL T      /DONE ENTIRE SECTOR?
 814   0577  0624          WRTCRC           /YES, GO WRITE THE CRC
 815
 816   0600  0046          INCR BAR         /NO, BRING UP NEXT DATA BIT FROM SEC BUFFER
```



```
 817
 818   0601  0070          LCT              /NOOP - WASTE 5 CYCLES WITH
 819   0602  0376          -2               /NOOP - A SELF TEST OF THE COUNTER
 820   0603  0073          ICT              /NOOP
 821   0604  0124          BR COFL F        /NOOP
 822   0605  0620          SELFER           /NOOP
 823
 824   0606  0063          TOG FLAG         /WRITE A CLOCK TRANSITION
 825
 826   0607  0070          LCT              /NOOP - WASTE 4 CYCLES WITH
 827   0610  0377          -1               /NOOP - A SELF TEST OF THE COUNTER
 828   0611  0124          BR COFL F        /NOOP
 829   0612  0620          SELFER           /NOOP
 830
 831   0613  0206          JUMP F1          /GO WRITE ANOTHER DATA BIT
 832   0614  0571          DATAA
 833
 834   0615  0054  C,      CRC ZERO         /UPDATE CRC WITH 0 AND SKIP DATA TRANSITION
 835   0616  0206          JUMP F1
 836   0617  0576          CBACK
 837
 838
 839   0620  0070  SELFER, LCT              /A SELF DIAGNOLTIC HAS FAILED
 840   0621  0060          #SELFER
 841   0622  0226          JUMP F5
 842   0623  2610          GOERDN
 843
 844
 845                 /THIS ROUTINE WRITES THE 16 BIT CRC GENERATED FOR THE
 846                 /PRECEEDING DATA FIELD.
 847
 848
 849   0624  0070  WRTCRC, LCT              /PRESET BIT COUNTER FOR 16 BITS
 850   0625  0357          -16-1
 851
 852   0626  0075          LSR              /NOOP WASTE 4 CYCLES AND SELF TEST THE SR
 853   0627  0002  E,      DISK             /NOOP
 854   0630  0120          BR SR7 ZERO      /NOOP
 855   0631  0620          SELFER           /NOOP
 856
 857   0632  0063          TOG FLAG         /WRITE A CLOCK TRANSITION
 858
 859   0633  0076          ROTATE ONE       /NOOP WASTE 6 CYCLES WITH MORE SELFTEST
 860   0634  0076          ROTATE ONE       /NOOP
 861   0635  0076          ROTATE ONE       /NOOP
 862   0636  0076          ROTATE ONE       /NOOP
 863   0637  0120          BR SR7 ZERO      /NOOP
 864   0640  0620          SELFER           /NOOP
 865
 866   0641  0130          BR CRC16 ZERO    /WHAT IS THE CRC BIT
 867   0642  0653          D                /ZERO, DO NOT WRITE ANYTHING
 868
 869   0643  0056          CRC ONE          /ONE, BRING UP THE NEXT BIT
 870
 871   0644  0063          TOG FLAG         /WRITE A DATA TRANSITION
```

```
                0645  0076          ROTATE ONE      /NOOP
                0646  0073  DBACK,  ICT             /BUMP THE BIT COUNTER
                0647  0126          BR COFL T       /DONE CRC YET?
                0650  0656          WRTPST          /YES, GO WRITE A POSTAMBLE
                0651  0206          JUMP F1         /NO, GO WRITE ANOTHER CRC BIT
                0652  0627          E
                0653  0054  D,      CRC ZERO        /BRING UP NEXT CRC BIT AND SKIP DATA TRANSITION
                0654  0206          JUMP F1
                0655  0646          DBACK

                      /THIS ROUTINE WRITES THE ONE BYTE POSTAMBLE, TURNS OFF
                      /WRITE CURRENT, DELAYS 511 MICRO SEC AND TURNS OFF ERASE
                      /CURRENT, IT UTILIZES THE WRITE ZEROES SUBROUTINE.

                0656  0070  WRTPST, LCT             /SETUP TO CALL WRT0S TO WRITE 8 BITS OF ZEROES
                0657  0666          CWGATE
                0660  0075          LSR
                0661  0070          LCT
                0662  0367          -8-1
                0663  0063          TOG FLAG        /WRITE LAST CLOCK TRANSITION OF THE CRC FIELD
                0664  0212          JUMP F2         /CALL THE SUBROUTINE WRITE ZEROES
                0665  1322          WRT0S

                0666  0004  CWGATE, CLR WGATE       /DISABLE WRITE CURRENT
                0667  0070          LCT             /CALL WRT0S FOR 127 BITS (511.2 MICRO SEC)
                0670  0676          CEGATE          /DELAY TO ERASE TURN OFF
                0671  0075          LSR
                0672  0070          LCT
                0673  0200          -127-1
                0674  0212          JUMP F2
                0675  1322          WRT0S

                0676  0020  CEGATE, CLR EGATE       /DISABLE ERASE CURRENT

                0677  0070          LCT             /CALL WRT0S FOR 25 BIT (101 MICRO SEC) DELAY
                0700  0706          READOK          /BEFORE TRYING TO READ
                0701  0075          LSR
                0702  0070          LCT
                0703  0346          -25-1
                0704  0212          JUMP F2
                0705  1322          WRT0S

                0706  0070  READOK, LCT             /CALL FIND HEADER ROUTINE TO INSURE
```



```
                0707  0712          GODONE          /THAT THE DISK IS STILL MOVING
                0710  0216          JUMP F3
                0711  1402          FINDHD

                0712  0212  GODONE, JUMP F2          /WRITE SECTOR FUNCTION IS COMPLETE
                0713  1206          OKDONE

                      /(SUBROUTINE: FINDSECTOR)
                      /SUBROUTINE TO FIND A SPECIFIC SECTOR.  ENTER WITH RETURN ADDRESS
                      /IN CNTR,  DESIRED TRACK ADDRESS IN TARTRK AND DESIRED SECTOR ADDRESS
                      /IN TARSEC.  THIS SUBROUTINE ASSUMES THAT THE TARGET TRACK HAS ALREADY
                      /BEEN REACHED.

                0714  0270  FINDSE, OPEN RTNA      /SAVE RETURN ADDRESS
                0715  0075          LSR
                0716  0064          LSP

                0717  0260          OPEN TEMPG      /PRESET SECTOR TRY COUNT TO 52 TRIES
                0720  0070          LCT
                0721  0313          -52-1

                0722  0075  AGAIN2, LSP             /STORE SECTOR TRY COUNT
                0723  0064          LSP

                0724  0070          LCT             /CALL SUBROUTINE TO FIND A HEADER
                0725  0730          CHKSEC
                0726  0216          JUMP F3
                0727  1402          FINDHD

                0730  0174  CHKSEC, BR FLAGO ZERO   /CORRECT SECTOR? FLAG=1 IF NO
                0731  0743          WAIT            /YES, GO WAIT FOR PREAMBLE

                0732  0260          OPEN TEMPG      /NO, RECALL SECTOR TRY COUNT AND INCREMENT IT
                0733  0071          ESP
                0734  0073          ICT

                0735  0124          BR COFL F       /52 TRIES MADE FOR SECTOR YET?
                0736  0722          AGAIN2          /NO, TRY ANOTHER SECTOR

                0737  0270  NXHDR,  LCT             /YES, CANNOT FIND THE SECTOR
                0740  0073          KNXHDR
                0741  0226          JUMP F5
                0742  2610          GOERDN

                0743  0070  WAIT,   LCT             /STALL 323.2 MICRO SECONDS TO WAIT FOR DATA PREAMBLE
                0744  0345          -26-1
                0745  0073          ICT
                0746  0124          BR COFL F
                0747  0745          .-2
                0750  0073          ICT
                0751  0124          BR COFL F
                0752  0750          .-2
                0753  0073          ICT
```

```
 982    0754  0124          BR COFL F
 983    0755  0753          .-2
 984
 985    0756  0270          OPEN RTNA       /RETURN FROM THIS SUBROUTINE AT WRITE TURN ON TIME
 986    0757  0203          JUMP F0 IND     /OF THE DESIRED SECTOR
 987
 988
 989
 990                 /[ROUTINE: READ SECTOR]
 991
 992    0760  0074  RDSEC,  ROTATE ZERO     /ZERO THE STAT
 993    0761  0074          ROTATE ZERO
 994    0762  0214          OPEN STAT
 995    0763  0064          LSP
 996
 997    0764  0070          LCT             /CALL THE FIND TRACK SUBROUTINE TO LOCATE DESIRED SECTOR
 998    0765  0770          GOREAD
 999    0766  0202          JUMP F0
1000    0767  0103          FINDTR
1001
1002    0770  0222  GOREAD, JUMP F4         /GO READ THE DATA FIELD
1003    0771  2167          READ
1004
1005
1006    0772  0000          0               /OPEN  FREE LOCATIONS
1007    0773  0000          0               /OPEN
1008    0774  0000          0               /OPEN
1009    0775  0000          0               /OPEN
1010    0776  0000          0               /OPEN
1011    0777  0000          0               /OPEN
```



```
1012                /[ROUTINE: DONE AND ERROR DONE]
1013
1014
1015    1000  0220  ERDONE, CLR DONE
1016    1001  0012          CLR XREQ
1017
1018    1002  0002          INTERF          /SELECT INTERFACE BUSS
1019
1020    1003  0006          SET ERR         /ASSERT ERROR LINE
1021
1022    1004  0212          JUMP F2         /SKIP NEXT INSTRUCTION
1023    1005  1007          .+2
1024
1025    1006  0204  OKDONE, CLR ERR         /NEGATE ERROR LINE
1026
1027    1007  0214          OPEN STAT       /OPEN STAT TO MOVE TO INTERFACE
1028
1029    1010  0071          ESP             /STAT OR ERRES TO SR
1030    1011  0075          LSR
1031
1032    1012  0024          CLR SHIFT       /CLEAR INTERFACE OUTPUT BUFFER
1033    1013  0022          CLR DONE
1034    1014  0010          CLR XREQ
1035
1036    1015  0000          INTERF          /SELECT INTERFACE OUTPUT BUSS
1037
1038    1016  0230          CLR SECDAT      /SELECT SR AS DATA LINE SOURCE
1039
1040    1017  0016          SET IOOUT       /DEFINE DATA DIRECTION AS OUT (TO INTERFACE)
1041
1042    1020  0070          LCT             /MOVE SR TO INTERFACE SERIALLY
1043    1021  0367          -8-1
1044    1022  0026          SET SHIFT
1045    1023  0024          CLR SHIFT
1046    1024  0073          ICT
1047    1025  0074          ROTATE ZERO
1048    1026  0124          BR COFL F
1049    1027  1022          .-5
1050
1051    1030  0014          CLR IOOUT       /NEXT TRANSFER WILL BE FROM INTERFACE
1052
1053    1031  0022  STDONE, SET DONE        /FUNCTION IS DONE
1054    1032  0070          LCT             /CALL GET COMMAND SUBROUTINE TO GET NEXT FUNCTION
1055    1033  0370          PFUNCT
1056    1034  0222          JUMP F4
1057    1035  2001          GETCMD
1058
1059    1036  0074  FUNCT,  ROTATE          /MOVE UNIT SELECT BIT TO SR7
1060    1037  0074          ROTATE
1061    1040  0074          ROTATE
1062    1041  0122          BR SR7 ONE      /FLAG IS ALREADY SET,  SAVE UNIT IN FLAG, ON=UNIT 0
1063    1042  1044          .+2
1064    1043  0061          FLAG OFF
1065
1066    1044  0074          ROTATE          /GET FIRST FUNCTION BIT TO SR7
```

```
1067
1068    1045  0120          BR SR7 ZERO
1069    1046  1066          FUNCT4          /FUNCTION 4 OR GREATER
1070
1071    1047  0074          ROTATE          /GET 2ND FUNCTION BIT
1072
1073    1050  0120          BR SR7 ZERO
1074    1051  1057          FUNCT2          /FUNCTION CODE IS 2 OR 3
1075
1076
1077    1052  0074          ROTATE          /GET LAST FUNCTION BIT
1078
1079    1053  0120          BR SR7 ZERO
1080    1054  1107          EMPTYBUF        /FUNCTION CODE 1
1081
1082    1055  0212          JUMP F2         /FUNCTION CODE 0
1083    1056  1110          FILLBUF
1084
1085    1057  0074  FUNCT2, ROTATE          /GET LAST FUNCTION BIT
1086
1087    1060  0120          BR SR7 ZERO
1088    1061  1105          PRDSEC          /FUNCTION CODE 3
1089
1090    1062  0070          LCT             /CLR CNTR BIT4 TO INDICATE NORMAL DATA
1091    1063  0000          0
1092    1064  0206          JUMP F1         /FUNCTION 2
1093    1065  0400          WRTSEC
1094
1095    1066  0074  FUNCT4, ROTATE          /GET 2ND FUNCTION BIT
1096
1097    1067  0120          BR SR7 ZERO
1098    1070  1076          FUNCT6          /FUNCTION CODE IS 6 OR GREATER
1099
1100    1071  0074          ROTATE          /GET LAST FUNCTION BIT
1101
1102    1072  0120          BR SR7 ZERO
1103    1073  1224          RDSTAT          /FUNCTION 5
1104
1105    1074  0212          JUMP F2
1106    1075  1243          CLRID           /FUNCTION 4=UNUSED
1107
1108    1076  0074  FUNCT6, ROTATE          /GET LAST FUNCTION BIT
1109
1110    1077  0120          BR SR7 ZERO
1111    1100  1275          RDEREG          /FUNCTION 7
1112
1113    1101  0070          LCT             /SET CNTR6 TO INDICATE DELETED DATA
1114                        OCTAL
1115    1102  0100          100
1116                        DECIMAL
1117    1103  0206          JUMP F1
1118    1104  0402          WRTSEC          /FUNCTION 6
1119
1120    1105  0206  PRDSEC, JUMP F1          /POINTER TO READ SECTOR FUNCTION
1121    1106  0760          RDSEC
```



```
1122
1123
1124
1125
1126
1127
1128
1129                    /[ROUTINES FILL AND EMPTY BUFFER]
1130
1131
1132    1107  0210  EMPTYBUF,SET IOOUT      /IOOUT IS CLEARED,  SET IT TO INDICATE DATA IS
1133                                          /MOVING TO THE INTERFACE
1134
1135    1110  0074  FILLBUF,ROTATE ZERO     /CLEAR STAT
1136    1111  0274          ROTATE ZERO
1137    1112  0214          OPEN STAT
1138    1113  0264          LSP
1139
1140    1114  0210          OPEN ERREG       /CLEAR ERREG
1141    1115  0264          LSP
1142
1143    1116  0261          FLAG OFF         /NOOP
1144
1145    1117  0044          CLR BAR SHORT    /ADDRESS THE 1ST BIT OF SECTOR BUFFER
1146
1147    1120  0070          LCT              /SET UP BYTE COUNT TO 128 (8 BIT) OR 64 (12 BIT)
1148    1121  0177          -128-1
1149    1122  0152          BR XIIBIT F
1150    1123  1126          .+3
1151    1124  0070          LCT
1152    1125  0277          -64-1
1153    1126  0230          OPEN TEMPA
1154
1155    1127  0106          BR IOBSOT T      /WHICH FUNCTION IS THIS?
1156    1130  1210          EMPTY1           /EMPTYBUF
1157
1158    1131  0012  XFRQ,   SET XREQ         /REQUEST DATA TRANSFER
1159
1160    1132  0073          ICT              /INCREMENT BYTE COUNT AND RESTORE
1161    1133  0075          LSR
1162    1134  0264          LSP
1163
1164    1135  0070          LCT              /CALL WAITRUN SUBR TO WAIT FOR DATA TRANSFER
1165    1136  1141          NEWORD
1166    1137  0222          JUMP F4
1167    1140  2312          WAITRN
1168
1169    1141  0230  NEWORD, OPEN TEMPA       /REOPEN THE BYTE COUNT REGISTER BECAUSE WAITRUN CLOSED IT
1170    1142  0070          LCT              /SET UP BIT COUNT IN CNTR TO 8 BITS OR 12 BITS
1171    1143  0367          -8-1
1172    1144  0152          BR XIIBIT F
1173    1145  1150          .+3
1174    1146  0070          LCT
1175    1147  0363          -12-1
1176
```

```
1177    1150  0124          BR IOB3OT F     /WHICH FUNCTION IS THIS?
1178    1151  1175          FILL1           /FILLBUF
1179
1180
1181    1152  0026  BYTEOUT,SET SHIFT       /EMPTYBUF,  MOVE A BYTE FROM SECTOR BUFFER
1182    1153  0046          INCR BAR        /TO INTERFACE SERIALLY
1183    1154  0024          CLR SHIFT
1184    1155  0073          ICT
1185    1156  0124          BR COFL F
1186    1157  1152          BYTEOUT
1187
1188    1160  0071          ESP             /CHECK BYTE COUNT
1189    1161  0124          BR COFL F
1190    1162  1131          XFRQ            /NOT DONE, GO REQUEST A DATA TRANSFER
1191
1192    1163  0012          SET XREQ        /DONE, REQUEST TRANSFER OF LAST BYTE
1193
1194    1164  0100          BR RUN F        /WAIT FOR TRANSFER COMPLETION
1195    1165  1164          .-1
1196
1197    1166  0010          CLR XREQ
1198
1199    1167  0212          JUMP F2         /EMPTYBUF FUNCTION IS COMPLETE
1200    1170  1006          OKDONE
1201
1202    1171  0050          FIN WRTBUF      /END SECTOR BUFR WRT PULSE (600 NS)
1203
1204    1172  0046          INCR BAR        /ADDRESS NEXT CELL OF SECTOR BUFFER
1205
1206    1173  0026          SET SHIFT       /SHIFT NEXT BIT FROM INTERFACE
1207    1174  0024          CLR SHIFT
1208
1209    1175  0053  FILL1,  START WRTBUF    /START SECTOR BUFR WRT PULSE
1210
1211    1176  0073          ICT             /LAST BIT OF BYTE?
1212    1177  0124          BR COFL F
1213    1200  1171          .-7             /NO, DO ANOTHER BIT
1214
1215    1201  0050          FIN WRTBUF      /LAST BIT, END SECTOR BUFR WRT PULSE
1216
1217    1202  0046          INCR BAR        /ADDRESS NEXT CELL OF SECTOR BUFFER
1218
1219    1203  0071          ESP             /CHECK BYTE COUNT
1220    1204  0124          BR COFL F
1221    1205  1131          XFRQ            /NOT DONE, GO GET ANOTHER BYTE
1222
1223    1206  0212          JUMP F2         /DONE FILLBUF FUNCTION
1224    1207  1006          OKDONE
1225
1226    1210  0032  EMPTY1, SET SECDAT      /SELECT SECTOR BUFR AS DATA LINE SOURCE
1227
1228    1211  0073          ICT             /INCREMENT AND SAVE THE BYTE COUNT
1229    1212  0075          LSR
1230    1213  0064          LSP
1231
```



```
1232    1214  0077          LCT             /SET UP THE BIT COUNT TO 8 BITS OR 12 BITS
1233    1215  0007          -8-1
1234    1216  0153          BR .IIBIT F
1235    1217  1152          BYTEOUT
1236    1220  0077          LCT
1237    1221  0363          -12-1
1238
1239    1222  0212          JUMP F2         /GO MOVE A BYTE TO INTERFACE
1240    1223  1152          BYTEOUT
1241
1242
1243
1244                /[ROUTINE: READ STATUS]
1245
1246
1247    1224  0200  RDSTAT, OPEN TEMPD      /SELECT THE SOFT UNIT SCRATCH PAD
1248
1249    1225  0036          UNIT ONE        /PRESELECT UNIT ONE
1250    1226  0077          LCT
1251    1227  0002          2
1252
1253    1230  0174          BR FLAGO ZERO   /WHICH UNIT?  FLAG=0=UNIT 1
1254    1231  1235          .+4             /UNIT 1,  SKIP UNIT 0 SETUP
1255
1256    1232  0034          UNIT ZERO       /SELECT UNIT ZERO
1257    1233  0077          LCT
1258                        OCTAL
1259    1234  0200          200
1260                        DECIMAL
1261
1262    1235  0075          LSR             /STORE SOFT UNIT BIT
1263    1236  0064          LSP
1264
1265    1237  0070          LCT             /CALL CHECKRDY SUBROUTINE, RETURN TO CLRID
1266    1240  1765          PNTRDY
1267    1241  0226          JUMP F5
1268    1242  2640          CHKRDY
1269
1270
1271
1272    1243  0214  CLRID,  OPEN STAT       /CLEAR INIT DONE BIT OF STAT
1273    1244  0071          ESP             /STATUS TO SHIFT REG
1274    1245  0075          LSR
1275
1276    1246  0061          FLAG OFF
1277    1247  0070          LCT             /END AROUND SHIFT OF FIRST 5 BITS
1278    1250  0372          -5-1
1279    1251  0122  ROT,    BR SR7 T
1280    1252  1256          .+4
1281    1253  0074          ROTATE ZERO
1282    1254  0212          JUMP F2
1283    1255  1257          .+2
1284    1256  0076          ROTATE ONE
1285    1257  0073          ICT
1286    1260  0124          BR COFL F
```

```
1287    1261  1251            .=8
1288
1289    1262  0176            BR FLAGO T      /IF FLAG IS SET THEN ROTATE IS DONE
1290    1263  1272            GODUN
1291
1292    1264  0062            FLAG ON         /IF NOT, CLEAR INIT DONE AND FINISH ROTATE
1293    1265  0074            ROTATE ZERO
1294    1266  0070            LCT
1295    1267  0375            -2-1
1296    1270  0212            JUMP F2
1297    1271  1251            ROT
1298
1299
1300    1272  0064    GODUN,  LSP             /RESTORE STAT AND GO DONE
1301    1273  0212            JUMP F2
1302    1274  1006            OKDONE
1303
1304                  /[ROUTINE: READ ERROR REGISTER]
1305
1306
1307
1308    1275  0210    RDEREG, OPEN ERREG
1309    1276  0212            JUMP F2
1310    1277  1010            OKDONE+2
1311
1312
1313                  /[SUBROUTINE: DELAY]. THIS SUBROUTINE PROVIDES DELAYS IN MULTIPLES
1314                  /OF .1MS. ENTER WITH RETURN ADDRESS IN THE SHIFT REG,
1315                  /AND MULTIPLIER IN THE COUNTER
1316
1317
1318    1300  0264    DELAY,  OPEN RTNB       /SAVE THE RETURN ADDRESS
1319    1301  0064            LSP
1320
1321    1302  0075            LSR             /MULTPLIER TO SHIFT REGISTER
1322
1323    1303  0070            LCT             /DELAY 490 CYCLES (98 MICRO SECONDS)
1324    1304  0205            -122-1
1325    1305  0073            ICT
1326    1306  0264            OPEN RTNB
1327    1307  0124            BR COFL F
1328    1310  1305            .-3
1329
1330    1311  0071            ESP             /MOVE MULTIPLIER TO CNTR VIA RTNB
1331    1312  0064            LSP
1332    1313  0075            LSR
1333    1314  0071            ESP
1334    1315  0064            LSP
1335
1336    1316  0073            ICT             /INCREMENT THE MULTIPLIER
1337
1338    1317  0124            BR COFL F       /ANY MORE .1MS LOOPS?
1339    1320  1301            DELAY+1         /YES, GO TO IT
1340
1341    1321  0223            JUMP F4 IND     /NO, RETURN FROM SUBROUTINE
```



```
1342
1343                  /[SUBROUTINE: WRITE ZEROES]
1344                  /THIS SUBROUTINE WRITES A SPECIFIED NUMBER OF ZEROS IF
1345                  /WRITE GATE IS ON, IF WRITE GATE IS OFF IT ACTS AS A
1346                  /DELAY OF N.5 BITS, ENTRANCE IS MADE WITH RETURN ADDRESS
1347                  /IN THE SR, NUMBER OF BITS IN THE CNTR, AND A CLOCK
1348                  /TRANSITION OCCURRING IMMEDIATLY PRIOR TO THE JUMP INTO
1349                  /THIS SUBROUTINE.
1350
1351
1352    1322  0274    WRTZS,  OPEN RTN        /SAVE RETURN ADDRESS
1353    1323  0064            LSP
1354
1355    1324  0075            LSR             /PUT BIT COUNTER IN SR
1356
1357    1325  0230            OPEN TEMPA      /TEMPA IS THE PATH THROUGH THE SP
1358
1359    1326  0070    LOOP,   LCT             /STALL 2.6 MICRO SECONDS
1360    1327  0374            -3-1
1361    1330  0073            ICT
1362    1331  0124            BR COFL F
1363    1332  1330            .-2
1364    1333  0064            LSP             /NOOP
1365    1334  0071            ESP             /NOOP
1366
1367    1335  0063            TOG FLAG        /WRITE A CLOCK TRANSITION IF WRT GATE IS SET
1368
1369    1336  0064            LSP             /PUT BIT COUNT IN THE COUNTER
1370    1337  0071            ESP
1371
1372    1340  0073            ICT             /INCREMENT BIT COUNT
1373
1374    1341  0075            LSR             /PUT UPDATED BIT COUNT BACK IN SR
1375
1376    1342  0124            BR COFL F       /DONE ALL BITS?
1377    1343  1326            LOOP            /NO
1378
1379    1344  0274            OPEN RTN        /YES, RETURN FROM SUBROUTINE
1380    1345  0207            JUMP IND F1
1381
1382
1383    1346  0222    PGOTIT, JUMP F4         /POINTER TO GETWORD FROM WAITRUN
1384    1347  2010            GOTIT
1385
1386
1387                  /[ROUTINE: INITIALIZE CONT.]
1388
1389    1350  0061    TEST2,  FLAG OFF        /CLEAR FLAG TO INDICATE R10 IS BEING TESTED
1390
1391    1351  0070    TEST1,  LCT             /LOOP TO TEST THAT SR IS 252 AND THAT
1392    1352  0372            -5-1            /IT CAN BE SHIFTED,
1393    1353  0120    TSTAGN, BR SR7 ZERO
1394    1354  1374            INTER1          /TEST FAILURE
1395    1355  0076            ROTATE ONE
1396    1356  0122            BR SR7 ONE
```

```
1397    1357  1374          INTER1          /TEST FAILURE
1398    1360  0074          ROTATE ZERO
1399    1361  0073          ICT
1400    1362  0124          BR COFL F
1401    1363  1353          TSTAGN
1402
1403    1364  0250          OPEN R10        /CONTENTS OF R10 TO SR,  SHOULD BE 125
1404    1365  0071          ESP
1405    1366  0075          LSR
1406
1407    1367  0074          ROTATE ZERO     /SHIFT SR ONCE TO CHANGE 125 TO 252
1408
1409    1370  0176          BR FLAGO ONE    /HAS R10 BEEN TESTED ALREADY?
1410    1371  1350          TEST2           /NO
1411
1412    1372  0202  TESTDN, JUMP F0        /YES, RETURN TO REMAINING INITIALIZE ROUTINE
1413    1373  0004          TSTRTN
1414
1415    1374  0006  INTER1, SET ERR        /SELF TEST ERROR, SET ERROR AND GO SET DONE
1416    1375  0212          JUMP F2
1417    1376  1031          STDONE
1418
1419    1377  0000          0               /OPEN
```



```
1420                  /[SUBROUTINE: FINDHEADER AND FIND DATA ADDRESS MARK]
1421                  /SUBROUTINE TO LOCATE A LEGAL HEADER (CORRECT CRC AND TRACK #)
1422                  /ENTER WITH THE RETURN ADDRESS IN CNTR.  ALSO ROUTINE TO FIND A DATA MARK
1423                  /OR DELETED DATA MARK.
1424
1425                                  /THIS ROUTINE LOCATES A SIX BYTE PREAMBLE OF ZEROES.
1426
1427
1428    1400  0264  FINDHD, OPEN RTNB       /STORE RETURN ADDRESS
1429    1401  0075          LSR
1430    1402  0064          LSP
1431
1432    1403  0230          OPEN TEMPA      /256 TO BAD START INNER COUNT
1433    1404  0072          LCT
1434    1405  0377          -1
1435    1406  0075          LSR
1436    1407  0064          LSP
1437
1438    1410  0234          OPEN TEMPB      /3 TO CNTR FOR BAD START OUTER COUNT,  768 BAD STARTS ALLOWED
1439    1411  0072          LCT
1440    1412  0374          -3-1
1441
1442    1413  0075  TRYAGN, LSR             /RESTORE BAD START COUNT
1443    1414  0064          LSP
1444
1445    1415  0045          CLR BAR LONG    /RESET FOR A COUNT OF 4096 AS PREAMBLE FAILURE COUNT
1446
1447    1416  0240          OPEN TEMPC      /24 TO CNTR AS ZERO BIT COUNT
1448    1417  0072          LCT
1449    1420  0347          -24-1
1450    1421  0075  MOREOS, LSR             /RESTORE ZERO BIT COUNT
1451    1422  0064          LSP
1452
1453    1423  0070          LCT             /PUT 0 IN SR7 FOR DATA COMPARISONS, ALSO CONSTANT FOR 40 MICRO SEC WAIT BRANCH
1454    1424  0067          -200-1
1455    1425  0075          LSR
1456
1457    1426  0346          WBR SEPCLK T    /WAIT 40 MICRO SECONDS FOR SEP CLK
1458    1427  1432          .+3
1459
1460    1430  0216          JUMP F3         /ERROR,NO SEP CLK
1461    1431  1667          TIMERR
1462
1463    1432  0154          BR DEQSR7 F     /WHAT IS SEP DATA?
1464    1433  1746          NOZERO          /ONE, GO CHECK PREAMBLE FAILURES
1465
1466    1434  0071          ESP             /ZERO FOUND, CHECK ZERO COUNT
1467    1435  0073          ICT
1468    1436  0124          BR COFL F
1469    1437  1421          MOREOS          /NEED MORE ZEROES FOR PREAMBLE
1470    1440  0061          FLAG OFF        /FOUND PREAMBLE, CLR FLAG TO INDICATE SEARCH FOR IDAM
1471
1472    1441  0045  GETDAM, CLR BAR LONG    /START SEARCH FOR IDAM OR DATA AM, BAR IS NOSTART COUNTER
1473
1474    1442  0070          LCT             /WAIT 40 MICRO SEC FOR SEP CLK
```

```
1475    1443  2067            -200-1
1476    1444  0346            *BR SEPCLK T
1477    1445  1450            .+3
1478    1446  0216            JUMP F3         /TIMING ERROR
1479    1447  1667            TIMERR
1480
1481    1450  0156            BR DEQSR7 T     /WHAT IS SEP DATA?
1482    1451  1755            NOTYET          /ZERO, GO DETERMINE IF TO MANY STARTS
1483
1484    1452  0164            BR MCEQSR F     /ONE, MISSING CLOCK?
1485    1453  1673            BADSRT          /YES, SHOULDN'T HAVE BEEN
1486
1487    1454  0057            PRECRC          /JAM 1ST TWO BITS OF CRC
1488    1455  0056            CRC ONE
1489    1456  0056            CRC ONE
1490
1491    1457  0070            LCT             /WAIT 40 MICRO SECONDS FOR SECOND CELL
1492    1460  0067            -200-1
1493    1461  0346            *BR SEPCLK T
1494    1462  1465            .+3
1495    1463  0216            JUMP F3
1496    1464  1667            TIMERR
1497
1498    1465  0156            BR DEQSR7 T     /DATA SHOULD BE 1, MISSING CLK SHOULD BE T
1499    1466  1673            BADSRT
1500    1467  0166            BR MCEQSR T
1501    1470  1673            BADSRT
1502
1503    1471  0056            CRC ONE         /JAM 3 MORE CRC BITS
1504    1472  0056            CRC ONE
1505    1473  0056            CRC ONE
1506
1507    1474  0070            LCT             /WAIT FOR THIRD BIT CELL
1508    1475  0067            -200-1
1509    1476  0346            *BR SEPCLK T
1510    1477  1502            .+3
1511    1500  0216            JUMP F3
1512    1501  1667            TIMERR
1513
1514    1502  0154            BR DEQSR7 F     /DATA SHOULD BE 0, MISSING CLK SHOULD BE F
1515    1503  1673            BADSRT
1516    1504  0164            BR MCEQSR F
1517    1505  1673            BADSRT
1518
1519    1506  2070            LCT             /CLEAR SR
1520    1507  0000            0
1521    1510  0075            LSR
1522
1523    1511  0070            LCT             /WAIT FOR 4TH BIT CELL
1524    1512  0067            -200-1
1525    1513  0346            *BR SEPCLK T
1526    1514  1517            .+3
1527    1515  0216            JUMP F3
1528    1516  1667            TIMERR
1529
```



```
1530    1517  0154            BR DEQSR7 F     /DATA SHOULD BE 0, MISSING CLK SHOULD BE F
1531    1520  1673            BADSRT
1532    1521  0002            LDMD            /NOOP FOR LONG SEP CLOCK
1533    1522  0002            LDMD            /NOOP FOR LONG SEP CLOCK
1534    1523  0164            BR MCEQSR F
1535    1524  1673            BADSRT
1536
1537    1525  0070            LCT             /WAIT FOR FIFTH BIT CELL
1538    1526  0067            -200-1
1539    1527  0346            *BR SEPCLK T
1540    1532  1533            .+3
1541    1531  0216            JUMP F3
1542    1532  1667            TIMERR
1543
1544    1533  0156            BR DEQSR7 T     /DATA SHOULD BE 1
1545    1534  1673            BADSRT
1546
1547    1535  0176            BR FLAGD T      /IF FLAG SET FINISH LOOKING FOR DATA AM
1548    1536  1675            DAM
1549
1550    1537  0164            BR MCEQSR F     /FINISH IDAM, MISSING CLK SHOULD BE F
1551    1540  1673            BADSRT
1552
1553    1541  0056            CRC ONE         /JAM 6TH CRC BIT OF IDAM
1554
1555    1542  0070            LCT             /WAIT FOR SIXTH BIT CELL
1556    1543  0067            -200-1
1557    1544  0346            *BR SEPCLK T
1558    1545  1552            .+3
1559    1546  0216            JUMP F3
1560    1547  1667            TIMERR
1561
1562    1552  0156            BR DEQSR7 T     /DATA SHOULD BE 1, MISSING CLK SHOULD BE F
1563    1551  1673            BADSRT
1564    1552  0164            BR MCEQSR F
1565    1553  1673            BADSRT
1566
1567    1554  0002            LDMD            /NOOP FOR LONG SEP CLOCK
1568
1569    1555  0056            CRC ONE         /JAM 7TH CRC BIT OF IDAM
1570
1571    1556  0070            LCT             /WAIT FOR SEVENTH BIT CELL
1572    1557  0067            -200-1
1573    1560  0346            *BR SEPCLK T
1574    1561  1564            .+3
1575    1562  0216            JUMP F3
1576    1563  1667            TIMERR
1577
1578    1564  0156            BR DEQSR7 T     /DATA SHOULD BE 1, MISSING CLK SHOULD BE T
1579    1565  1673            BADSRT
1580    1566  0166            BR MCEQSR T
1581    1567  1673            BADSRT
1582
1583    1570  0054            CRC ZERO        /IDAM FOUND, JAM LAST CRC BIT
1584
```

```
1585
1586
1587
1588
1589                        /THIS ROUTINE COMPARES THE HEADER TRACK ADDRESS TO THE
1590                        /DESIRED TRACK ADDRESS ON THE FLY.  IT IS ENTERED AFTER
1591                        /FINDING THE IDAM, ERREG BIT 0 IS SET IF AN ERROR IS DETECTED.
1592
1593
1594    1571  0220    HDRCOM, OPEN TARTRK     /TARGET TRACK ADDRESS TO SR
1595    1572  0071            ESP
1596    1573  0075            LSR
1597
1598    1574  0070            LCT             /SET BIT COUNTER TO 8
1599    1575  0367            -8-1
1600
1601    1576  0144    AGAIN3, BR SEPCLK F     /WAIT FOR BIT CELL
1602    1577  1576            .-1
1603
1604    1600  0156            BR DEQSR7 T     /SEP DATA EQUAL TO SR7?
1605    1601  1605            .+4             /NO, TRACK COMPARE ERROR
1606
1607    1602  0074            ROTATE ZERO     /YES, GET NEXT TRACK ADRESS BIT
1608    1603  0216            JUMP F3
1609    1604  1610            .+4
1610
1611    1605  0210            OPEN ERREG      /SET ERREG BIT 0 TO INDICATE TRACK ERROR
1612    1606  0076            ROTATE ONE
1613    1607  0064            LSP
1614
1615    1610  0055            DATCRC          /UPDATE THE CRC
1616
1617    1611  0073            ICT             /INCREMENT AND TEST THE BIT COUNTER
1618    1612  0124            BR COFL F
1619    1613  1576            AGAIN3          /GO DO NEXT BIT
1620
1621    1614  0070            LCT             /TRACK COMPARED, SET UP BIT COUNTER FOR  8 BYTE
1622    1615  0367            -8-1
1623
1624    1616  0144    AGAIN4, BR SEPCLK F     /WAIT FOR BIT
1625    1617  1616            .-1
1626
1627    1620  0061            FLAG OFF        /CLEAR FLAG FOR NEXT ROUTINE
1628    1621  0061            FLAG OFF        /NOOP FOR LONG SEP CLK
1629    1622  0061            FLAG OFF        /NOOP FOR LONG SEP CLK
1630    1623  0061            FLAG OFF        /NOOP FOR LONG SEP CLK
1631
1632    1624  0055            DATCRC          /UPDATE CRC
1633
1634    1625  0073            ICT             /INCREMENT AND TEST BIT COUNT
1635    1626  0124            BR COFL F
1636    1627  1616            AGAIN4          /GO DO ANOTHER BIT
1637                                          /CONTINUE
1638
1639
```



```
1640                    /THIS ROUTINE COMPARES THE HEADER SECTOR ADDRESS WITH THE
1641                    /TARGET SECTOR ADDRESS ON THE FLY.  IT IS ENTERED FROM
1642                    /THE TRACK COMPARE ROUTINE.  A MISMATCH WILL SET THE FLAG.
1643
1644
1645    1630  0224            OPEN TARSEC     /TARGET SECTOR ADDRESS TO SR
1646    1631  0071            ESP
1647    1632  0075            LSR
1648
1649    1633  0070            LCT             /SET UP BIT COUNTER FOR 8 BITS
1650    1634  0367            -8-1
1651
1652    1635  0144    AGAIN5, BR SEPCLK F     /WAIT FOR A BIT
1653    1636  1635            .-1
1654
1655    1637  0156            BR DEQSR7 T     /HOW DO THEY COMPARE?
1656    1640  1643            .+3             /BAD, GO SET THE FLAG
1657
1658    1641  0216            JUMP F3         /GOOD, SKIP THE ERROR FLAG.
1659    1642  1644            .+2
1660
1661    1643  0062            FLAG ON         /SET FLAG TO INDICATE MISMATCH
1662
1663    1644  0074            ROTATE ZERO     /BRING UP NEXT BIT
1664
1665    1645  0055            DATCRC          /UPDATE THE CRC
1666    1646  0073            ICT             /BUMP THE BIT COUNTER
1667    1647  0124            BR COFL F       /ALL BITS COMPARED?
1668    1650  1635            AGAIN5          /NO, LOOP BACK
1669
1670    1651  0070            LCT             /YES, SETUP TO WAIT FOR END OF
1671    1652  0347            -24-1           /CRC
1672
1673    1653  0144    AGAIN6, BR SEPCLK F     /WAIT FOR BIT
1674    1654  1653            .-1
1675
1676    1655  0074            ROTATE ZERO     /NOOP FOR LONG SEP CLK
1677    1656  0074            ROTATE ZERO     /NOOP FOR LONG SEP CLK
1678    1657  0074            ROTATE ZERO     /NOOP FOR LONG SEP CLK
1679    1660  0074            ROTATE ZERO     /NOOP FOR LONG SEP CLK
1680
1681    1661  0055            DATCRC          /UPDATE CRC
1682
1683    1662  0073            ICT             /BUMP THE BIT COUNTER
1684    1663  0124            BR COFL F       /ALL DONE?
1685    1664  1653            AGAIN6          /NO, LOOP BACK
1686
1687    1665  0226            JUMP F5         /YES, SO CHECK IF CRC IS ALL ZEROES
1688    1666  2515            CKHCRC
1689
1690
1691    1667  0070    TIMERR, LCT             /40 MICROSEC PASSED AND NO SEP CLOCK HAS SEEN
1692    1670  0110            KTIMERR
1693    1671  0226            JUMP F5
1694    1672  2610            GOERDN
```

```
1695
1696
1697    1673  0226    BADSRT, JUMP F5         /POINTER TO BADSTART ON IDAM OR DATA AM
1698    1674  2555            BDSRT
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708    1675  0166    DAM,    BR MCEQSR T     /MISSING CLK SHOULD BE T
1709    1676  1673            BADSRT
1710
1711    1677  0054            CRC ZERO        /JAM 6TH CRC BIT OF DATA AM
1712
1713    1700  0070            LCT             /WAIT FOR SIXTH BIT CELL
1714    1701  0067            -200-1
1715    1702  0346            WBR SEPCLK T
1716    1703  1706            .+3
1717    1704  0216            JUMP F3
1718    1705  1667            TIMERR
1719
1720    1706  0164            BR MCEQSR F     /MISSING CLK SHOULD BE F
1721    1707  1673            BADSRT
1722    1710  0042            LDMD            /NOOP FOR LONG SEP CLK
1723
1724    1711  0156            BR DEQSR7 T     /IF DATA=0 THEN LOOK FOR DELETED DATA AM
1725    1712  1727            DELDAT
1726
1727    1713  0056            CRC ONE         /JAM 7TH BIT OF DATA AM
1728
1729    1714  0070            LCT             /WAIT FOR SEVENTH BIT OF DATA AM
1730    1715  0067            -200-1
1731    1716  0346            WBR SEPCLK T
1732    1717  1722            .+3
1733    1720  0216            JUMP F3
1734    1721  1667            TIMERR
1735
1736    1722  0056            CRC ONE         /JAM LAST BIT OF DATA AM
1737
1738    1723  0154            BR DEQSR7 F     /DATA SHOULD BE 1
1739    1724  1742            ENDDAM          /FLAG IS SET TO INDICATE NORMAL DATA MARK
1740
1741    1725  0216            JUMP F3         /LAST DATA BIT WAS BAD
1742    1726  1673            BADSRT
1743
1744
1745    1727  0054    DELDAT, CRC ZERO        /JAM 7TH CRC BIT OF DEL DATA AM
1746
1747    1730  0070            LCT             /WAIT FOR 7TH CELL OF DEL DATA AM
1748    1731  0067            -200-1
1749    1732  0346            WBR SEPCLK T
```



```
1750    1733  1736            .+3
1751    1734  0216            JUMP F3
1752    1735  1667            TIMERR
1753
1754    1736  0061            FLAG OFF        /CLR FLAG TO INDICATE DELETED DATA MARK
1755
1756    1737  0054            CRC ZERO        /JAM LAST CRC BIT OF DEL DATA AM
1757
1758    1740  0154            BR DEQSR7 F     /DATA SHOULD BE 0
1759    1741  1673            BADSRT
1760
1761    1742  0164    ENDDAM, BR MCEQSR F     /MISSING CLK SHOULD BE F FOR BOTH DATA AMS
1762    1743  1673            BADSRT
1763
1764    1744  0222            JUMP F4         /GO PICK UP DATA FIELD
1765    1745  2266            DATA
1766
1767
1768    1746  0046    NOZERO, INCR BAR        /INCREMENT AND TEST PREAMBLE FAILURE COUNT
1769    1747  0160            BR BAROFL F
1770    1750  1416            TRYAGN+3        /OK, TRY AGAIN FOR A PREAMBLE
1771
1772    1751  0070    NXPRAM, LCT             /TOO MANY BITS WITH NO ZEROES
1773    1752  0120            KNXPRAM
1774    1753  0226            JUMP F5
1775    1754  2610            GOERDN
1776
1777
1778    1755  0046    NOTYET, INCR BAR        /INCR AND TEST IDAM OR DATA AM START FAILURE COUNT
1779    1756  0042            LDMD                    /NOOP FOR LONG SEP CLK
1780    1757  0160            BR BAROFL F
1781    1760  1442            GETDAM+1        /OK, TRY AGAIN
1782
1783    1761  0070    NXIDAM, LCT             /TOO MANY ZEROES WHILE LOOKING FOR START OF
1784    1762  0130            KNXIDAM         /IDAM OR DATA AM
1785    1763  0226            JUMP F5
1786    1764  2610            GOERDN
1787
1788
1789    1765  0212    PNTRDY, JUMP F2         /POINTERS FROM CHECKRDY SUBROUTINE TO RDSTAT ROUTINE
1790    1766  1243            CLRID
1791    1767  0212    PYSRDY, JUMP F2
1792    1770  1243            CLRID
1793
1794    1771  0212    PNORDY, JUMP F2         /POINTERS FROM CHECK RDY TO INITIALIZE ROUTINE
1795    1772  1006            OKDONE
1796    1773  0226            JUMP F5
1797    1774  2631            INTRDY
1798
1799    1775  0000            0               /OPEN
1800    1776  0000            0               /OPEN
1801    1777  0000            0               /OPEN
1802
```

```
1803                    /[SUBROUTINES: GETWORD AND GETCOMMAND]
1804                    /SUBROUTINE TO GET AN EIGHT BIT WORD FROM THE INTERFACE.
1805                    /IF TALKING TO A PDP8 INTERFACE IN 12 BIT MODE, THERE
1806                    /WILL BE FOUR MEANINGLESS BITS PRECEDING THE DESIRED EIGHT
1807                    /BIT WORD. ENTER THIS SUBROUTINE WITH THE RETURN ADDRESS
1808                    /IN THE COUNTER. EXIT WITH THE ONES COMPLIMENT OF THE
1809                    /DESIRED WORD IN THE SHIFT REGISTER. PARITY IS COMPUTED AND
1810                    /CHECKED ON ALL WORDS.
1811
1812
1813    2000  0012      GETWRD, SET XREQ          /REQUEST A WORD FROM INTERFACE
1814
1815    2001  0075      GETCMD, LSR               /STASH THE RETURN ADDRESS
1816    2002  0270              OPEN RTNA
1817    2003  0064              LSP
1818
1819    2004  2070              LCT               /CALL SUBR WAITRN TO WAIT FOR A WORD
1820    2005  1346              PGOTIT
1821    2006  0222              JUMP F4
1822    2007  2312              WAITRN
1823
1824    2010  0061      GOTIT,  OFF FLAG          /CLEAR FLAG FOR PARITY CHECK
1825
1826    2011  0004              CLR ERR           /IN CASE RUN WAS A RESPONSE TO DONE
1827    2012  0020              CLR DONE
1828
1829    2013  0070              LCT               /SET UP BIT COUNT IN CNTR,  8 BIT OR 12 BIT
1830    2014  0367              -8-1
1831    2015  0150              BR XIIBIT  F
1832    2016  2021              .+3
1833    2017  0070              LCT
1834    2020  0363              -12-1
1835
1836    2021  0112      WATDAT, BR DATAIN ONE     /WHAT IS THE DATA BIT?
1837    2022  2030              GOTONE            /ITS A ONE, GO SAVE IT
1838
1839    2023  0126              BR COFL T         /ITS A ZERO, WAS IT THE PARITY BIT (9TH BIT)?
1840    2024  2041              CHKPAR            /YES, GO CHECK PARITY
1841
1842    2025  0076              ROTATE ONE        /NO SAVE THE DATA BIT COMPLIMENTED IN SR
1843
1844    2026  0222              JUMP F4           /GO SHIFT UP ANOTHER BIT.
1845    2027  2034              NOTHER
1846
1847
1848
1849
1850    2030  2063      GOTONE, TOG FLAG          /COMPLIMENT THE PARITY GENERATOR
1851
1852    2031  0126              BR COFL T         /WAS IT THE PARITY BIT?
1853    2032  2041              CHKPAR            /YES, GO CHECK PARITY
1854
1855    2033  0078              ROTATE ZERO       /NO, SAVE THE COMPLIMENTED DATA BIT IN SR
1856
1857    2034  7026      NOTHER, SET SHIFT         /SHIFT PULSE AND INCREMENT BIT COUNT
```



```
1858    2035  0073              ICT
1859    2036  0024              CLR SHIFT
1860
1861    2037  0222              JUMP F4           /GO TEST THIS BIT.
1862    2040  2021              WATDAT
1863
1864
1865    2041  0176      CHKPAR, BR  FLAGO ONE     /WHERE THERE AN ODD NO. OF ONES?
1866    2042  2076              GOTWRD            /YES, PARITY WAS GOOD
1867
1868    2043  0214              OPEN STAT         /NO, STAT TO SR
1869    2044  0071              ESP
1870    2045  0075              LSR
1871
1872    2046  0070              LCT               /END AROUND SHIFT OF UPPER 5 BITS OF STAT IN SR
1873    2047  0372              -5-1
1874    2050  0122              BR SR7 T
1875    2051  2055              .+4
1876    2052  0074              ROTATE ZERO
1877    2053  0222              JUMP F4
1878    2054  2056              .+2
1879    2055  0076              ROTATE ONE
1880    2056  0073              ICT
1881    2057  0124              BR COFL F
1882    2060  2050              .-8
1883
1884    2061  0074              ROTATE ZERO       /CLEAR INIT DONE
1885    2062  0076              ROTATE ONE        /SET PARITY ERROR
1886
1887    2063  0122              BR SR7 T          /END AROUND SHIFT OF CRC ERROR BIT OF STAT IN SR
1888    2064  2070              .+4
1889    2065  0074              ROTATE ZERO
1890    2066  0222              JUMP F4
1891    2067  2071              .+2
1892    2070  0076              ROTATE ONE
1893
1894    2071  0064              LSP               /RESTORE STAT TO SCRATCH PAD
1895
1896    2072  0070              LCT               /ERRCODE FOR PARITY ERROR
1897    2073  0210              KPARER
1898    2074  0226              JUMP F5
1899    2075  2610              GOERDN
1900
1901    2076  0270      GOTWRD, OPEN RTNA         /WORD WAS GOOD, EXIT FROM GETWRD, GETCMD
1902    2077  0203              JUMP FE IND
```

```
1903
1904                    /[SUBROUTINE: STEPHEAD]
1905                    /THIS SUBROUTINE WILL STEP THE SPECIFIED NUMBER OF TRACKS IN THE
1906                    /SPECIFIED DIRECTION.  DIRECTION IS DETERMINED BY THE HD DIR FLOP
1907
1908                    /THE NUMBER OF STEPS IS IN THE SR.  RETURN ADDRESS IS IN THE CNTR.
1909                    /EXIT IS TO THE RETURN ADDRESS IF HOME IS DETECTED.  EXIT IS TO RETURN
1910                    /PLUS 2 IF THE LAST STEP HAS BEEN TAKEN.  AFTER THE LAST STEP IS TAKEN,
1911                    /THE HEAD IS LOADED AND A 25MS DELAY IS EXECUTED FOR HEAD SETTLE TIME
1912
1913
1914
1915
1916    2100  0270    STEPHD, OPEN RTNA       /STORE RETURN ADDR AND MOVE STEP COUNT TO CNTR
1917    2101  0064            LSP
1918    2102  0075            LSR
1919    2103  0071            ESP
1920    2104  0064            LSP
1921
1922    2105  0136    CKHOME, BR HOME T       /IS THE HEAD HOME?
1923    2106  2150            OUT             /YES, GO EXIT
1924
1925    2107  0073            ICT             /NO, INCREMENT STEP COUNT AND STORE IN TEMPA
1926    2110  0075            LSR
1927    2111  0230            OPEN TEMPA
1928    2112  0064            LSP
1929
1930    2113  0070            LCT             /PASS 30 TO DELAY SUBR FOR 3MS DELAY
1931    2114  2124            SECPLS
1932    2115  0075            LSR
1933    2116  0070            LCT
1934    2117  0341            -30-1
1935
1936    2120  0012            SET STPHD       /ISSUE STEP PULSE
1937    2121  0010            CLR STPHD
1938
1939    2122  0212            JUMP F2         /CALL DELAY SUBR
1940    2123  1300            DELAY
1941
1942    2124  0012    SECPLS, SET STPHD       /ISSUE SECOND STEP PULSE
1943    2125  0010            CLR STPHD
1944
1945    2126  0070            LCT             /CALL DELAY FOR 3MS DELAY
1946    2127  2135            DONSTP
1947    2130  0075            LSR
1948    2131  0070            LCT
1949    2132  0341            -30-1
1950    2133  0212            JUMP F2
1951    2134  1300            DELAY
1952
1953    2135  0230    DONSTP, OPEN TEMPA      /CHECK STEP COUNT
1954    2136  0071            ESP
1955    2137  0124            BR COFL F
1956    2140  2105            CKHOME          /NOT DONE, GO CHECK IF HOME
1957
```



```
1958    2141  0270            OPEN RTNA       /DONE STEPPING, INCREMENT RETURN ADDRESS BY 2
1959    2142  0071            ESP
1960    2143  0073            ICT
1961    2144  0073            ICT
1962
1963    2145  0270    DLY25,  OPEN RTNA       /STORE RETURN ADDRESS ALSO START OF 25MS DELAY SUBROUTINE
1964    2146  0075            LSR
1965    2147  0064            LSP
1966
1967    2150  0042    OUT,    LDHD            /LOAD HEAD
1968    2151  0250            OPEN TEMPE      /SET SOFT HD LOAD BIT
1969    2152  0070            LCT
1970                          OCTAL
1971    2153  0200            200
1972                          DECIMAL
1973    2154  0075            LSR
1974    2155  0064            LSP
1975
1976    2156  0070            LCT             /CALL DELAY SUBR FOR 25MS DELAY
1977    2157  2165            DONDLY
1978    2160  0075            LSR
1979    2161  0070            LCT
1980    2162  0000            -255-1
1981    2163  0212            JUMP F2
1982    2164  1300            DELAY
1983
1984    2165  0270    DONDLY, OPEN RTNA       /RETURN FROM STEP HEAD OR DELAY 25MS SUBROUTINE
1985    2166  0203            JUMP F0 IND
1986
1987
1988
1989
1990
1991
1992
1993                    /[ROUTINE: READ SECTOR CONT.]
1994
1995    2167  0070    READ,   LCT             /3 TO DATA MARK TRY COUNTER
1996    2170  0374            -3-1
1997    2171  0234            OPEN TEMPB
1998    2172  0075            LSR
1999    2173  0064            LSP
2000
2001    2174  0070            LCT             /STALL FOR 96 MICRO SEC (3 BYTES) TO AVOID WRT TURN ON SPLASH
2002    2175  0207            -120-1
2003    2176  0073            ICT
2004    2177  0062            FLAG ON         /SET THE FLAG TO SPECIFY DATA AM IN FIND AM ROUTINE
2005    2200  0124            BR COFL F
2006    2201  2176            .-3
2007
2008    2202  0073            ICT             /CLR COUNTER AND SR
2009    2203  0075            LSR
2010
2011    2204  0216            JUMP F3         /GO TRY FIND THE ADDRESS MARK
2012    2205  1441            GETDAM
```

```
2013
2014
2015                    /THIS ROUTINE FOLLOWS THE DISCOVERY OF A DATA MARK OR
2016                    /A DELETED DATA MARK,  IT MOVES THE NEXT 1024 BITS
2017                    /INTO THE SECTOR BUFFER, THEN PICKS UP AND CHECKS THE CRC.
2018
2019    2206  0044      DATA,   CLR BAR           /CLEAR THE BUFFER ADDRESS REGISTER
2020
2021    2207  0144              BR SEPCLK F       /WAIT FOR CLOCK
2022    2210  2207              .-1
2023
2024    2211  0053              START WRTBUF      /START THE WRITE PULSE FOR THIS BIT
2025
2026    2212  0055              DATCRC            /UPDATE THE CRC WITH SEP DATA
2027
2028    2213  0162              BR BAROFL T       /IS BUFFER FULL YET?
*2029   2214  2221              GETCRC            /YES, GO GET THE CRC
2030
2031    2215  0050              FIN WRTBUF        /NO, END THE WRITE PULSE
2032
2033    2216  0046              INCR BAR          /ADDRESS NEXT SECTOR BUFFER CELL
2034
2035    2217  0222              JUMP F4           /LOOP BACK FOR NEXT BIT
2036    2220  2207              DATA+1
2037
2038    2221  0050      GETCRC, FIN WRTBUF        /END THE WRITE PULSE FOR THE LAST BIT
2039
2040    2222  0070              LCT               /SET BIT COUNT TO 16 FOR 2 BYTE CRC
2041    2223  0357              -16-1
2042
2043    2224  0144              BR SEPCLK F       /WAIT FOR NEXT BIT
2044    2225  2224              .-1
2045
2046    2226  0042              LDMD              /4 NOOPS FOR LONG SEP CLOCK
2047    2227  0042              LDMD
2048    2230  0042              LDMD
2049    2231  0042              LDMD
2050
2051    2232  0055              DATCRC            /PUT CRC BIT IN THE CRC GENERATOR
2052    2233  0073              ICT               /INCREMENT AND TEST BIT COUNT
2053    2234  0124              BR COFL F
2054    2235  2224              .-9               /NOT DONE, GET ANOTHER
2055
2056    2236  0214              OPEN STAT         /STATUS TO SHIFT REG
2057    2237  0071              ESP
2058    2240  2075              LSR
2059
2060    2241  2122              BR SR7 T          /END AROUND SHIFT OF DRV RDY BIT OF STAT IN SR
2061    2242  2246              .+4
2062    2243  0074              ROTATE ZERO
2063    2244  0222              JUMP F4
2064    2245  2247              .+2
2065    2246  0076              ROTATE ONE
2066
2067    2247  0176              BR FLAGO T        /SET DEL DATA BIT OF STAT IF FLAG=0
```



```
2068    2250  2254              .+4
2069    2251  0076              ROTATE ONE
2070    2252  0222              JUMP F4
2071    2253  2255              .+2
2072    2254  0074              ROTATE ZERO
2073
2074    2255  0070              LCT               /END AROUND SHIFT OF NEXT 5 BITS OF STAT IN SR
2075    2256  0372              -5-1
2076    2257  0122              BR SR7 T
2077    2260  2264              .+4
2078    2261  0074              ROTATE ZERO
2079    2262  0222              JUMP F4
2080    2263  2265              .+2
2081    2264  0076              ROTATE ONE
2082    2265  0073              ICT
2083    2266  0124              BR COFL F
2084    2267  2257              .-8
2085
2086    2270  0070              LCT               /SET BIT COUNTER TO  16 FOR CRC TEST
2087    2271  0357              -16-1
2088
2089    2272  0132              BR CRC16 ONE      /IS THIS CRC BIT OK
2090    2273  2304              DCRCER            /NO, GO REPORT DATA CRC ERROR
2091
2092    2274  0054              CRC ZERO          /YES, BRING UP NEXT CRC BIT
2093
2094    2275  0073              ICT               /INCREMENT AND TEST BIT COUNTER
2095    2276  0124              BR COFL F
2096    2277  2272              .-5               /GO CHECK ANOTHER
2097
2098    2300  0074              ROTATE ZERO       /CRC WAS GOOD, CLR CRC ERR BIT OF STAT IN SR
2099
2100    2301  0064              LSP               /PUT THE STATUS WORD BACK IN SCRATCHPAD
2101
2102    2302  0212              JUMP F2           /EXIT TO DONE
2103    2303  1006              OKDONE
2104
2105    2304  0076      DCRCER, ROTATE ONE        /INSERT 1 INTO CRC ERROR BIT
2106
2107    2305  0064              LSP               /PUT THE STAT WORD BACK
2108
2109    2306  0070              LCT               /ERROR CODE FOR CRC ERROR
2110    2307  0200              KDCRCER
2111    2310  0226              JUMP F5
2112    2311  2610              GOERDN
```

```
2113                    /[SUBROUTINE: WAIT FOR RUN]
2114                    /THIS SUBROUTINE WILL WAIT FOR RUN,  IF 46MS ELAPSES, THE HEAD IS UNLOADED
2115                    /AND THE ROUTINE CONTINUES WAITING FOR RUN,  RETURN ADDRESS IS PASSED
2116                    /VIA THE COUNTER
2117
2118
2119    2312  0264      WAITRN, OPEN RTNB       /STASH THE RETURN ADDRESS
2120    2313  0075              LSR
2121    2314  0064              LSP
2122
2123    2315  0102              BR RUN T        /GOT RUN?
2124    2316  2347              GOTRUN
2125
2126    2317  0240              OPEN TEMPC      /PRESET LOOP COUNTER TO 0
2127    2320  0070              LCT
2128    2321  0000              0
2129
2130    2322  0075      BACK,   LSR             /RESTORE LOOP COUNT
2131    2323  0064              LSP
2132
2133    2324  0302              WBR RUN T       /TIME WHILE WAITING FOR FUN
2134    2325  2347              GOTRUN
2135    2326  0302              WBR RUN T
2136    2327  2347              GOTRUN
2137    2330  0302              WBR RUN T
2138    2331  2347              GOTRUN
2139    2332  0302              WBR RUN T
2140    2333  2347              GOTRUN
2141
2142    2334  0071              ESP             /INCREMENT AND TEST LOOP COUNT
2143    2335  0073              ICT
2144    2336  0124              BR COFL F
2145    2337  2322              BACK            /46MS NOT ELAPSED YET
2146
2147    2340  0250              OPEN TEMPE      /TIME IS EXPIRED (45.8 MS), CLEAR THE SOFT MDLD BIT AND UNLOAD THE HEAD
2148    2341  0073              ICT
2149    2342  0075              LSR
2150    2343  0064              LSP
2151    2344  0042              UNHD
2152
2153    2345  0120              BR RUN F        /WAIT FOR RUN, FOREVER IF NECESSARY
2154    2346  2345              .-1
2155
2156    2347  0010      GOTRUN, CLR XREQ        /IF RUN WAS RESPONSE TO XFREQ
2157
2158    2350  0264              OPEN RTNB       /RETURN FROM WAITRUN SUBROUTINE
2159    2351  0213              JUMP IND F2
2160
2161
```



```
2162                    /[ROUTINE: INITIALIZE CONT.]
2163                    /CONTINUATION OF THE INITIALIZE SELF TEST
2164
2165    2352  0070      TEST,   LCT             /LOAD R5 WITH TEST PATTERN 252
2166                              OCTAL
2167    2353  0252              252
2168                              DECIMAL
2169    2354  0075              LSR
2170    2355  0224              OPEN R5
2171    2356  0064              LSP
2172
2173    2357  0070              LCT             /LOAD R10 WITH TEST PATTERN 125
2174                              OCTAL
2175    2360  0125              125
2176                              DECIMAL
2177    2361  0075              LSR
2178    2362  0250              OPEN R10
2179    2363  0064              LSP
2180
2181    2364  0062              FLAG ON         /SET FLAG AND TEST IT
2182    2365  0176              BR FLAGO T
2183    2366  2371              .+3
2184    2367  0212              JUMP F2
2185    2370  1374              INTER1          /FLAG FAILURE
2186
2187    2371  0224              OPEN R5         /CONTENTS OF R5 TO SR,  SHOULD BE 252
2188    2372  0071              ESP
2189    2373  0275              LSR
2190
2191    2374  0212              JUMP F2         /GO CONTINUE INIT TEST IN FLD 2
2192    2375  1351              TEST1
2193
2194
2195    2376  0000              0               /OPEN
2196    2377  0000              0               /OPEN
```

```
2197                    /[SUBROUTINE: MAGNITUDE COMPARISON]
2198                    /THIS SUBROUTINE COMPARES THE EIGHT BIT NUMBERS IN REGISTERS F AND G
2199                    / EXIT IS TO THE RETURN ADDRESS IF F=G.  IF F<G, RETURN IS TO RTNA+2.
2200                    /IF F>G, RETURN IS TO RTNA+4.  CONTENTS OF F AND G ARE UNDEFINED AT
2201                    /THE END OF THE SUBROUTINE
2202
2203
2204
2205
2206    2400  0230      MAGCOM, OPEN TEMPA        /FOR BIT COUNT
2207
2208    2401  0070              LCT               /BIT COUNT IS 8
2209    2402  0367              -8-1
2210
2211    2403  0075              LSR               /RESTORE BIT COUNT
2212    2404  0064              LSP
2213
2214    2405  0254              OPEN TEMPF        /F TO SR
2215    2406  0071              ESP
2216    2407  0075              LSR
2217
2218    2410  0120              BR SR7 ZERO       /TEST F
2219    2411  2443              TSTG0             /ITS 0
2220
2221    2412  0076              ROTATE ONE        /ITS 1, BRING UP NEXT BIT
2222
2223    2413  0064              LSP               /RESTORE F
2224
2225    2414  0260              OPEN TEMPG        /G TO SR
2226    2415  0071              ESP
2227    2416  0075              LSR
2228
2229    2417  0120              BR SR7 ZERO       /TEST G
2230    2420  2432              GLESSF            /ITS 0, G IS LESS THAN F
2231
2232    2421  0074      NEXTG,  ROTATE ZERO       /ITS 1, BRING UP NEXT G BIT
2233
2234    2422  0064              LSP               /RESTORE G
2235
2236    2423  0230              OPEN TEMPA        /INCREMENT AND TEST BIT COUNT
2237    2424  0071              ESP
2238    2425  0073              ICT
2239    2426  0124              BR COFL F
2240    2427  2403              MAGCOM+3          /GO COMPARE ANOTHER BIT
2241
2242    2430  0270              OPEN RTNA         /ALL BITS COMPARED, NO DIFFERENCE
2243    2431  0203              JUMP FB IND
2244
2245    2432  0270      GLESSF, OPEN RTNA         /G IS LESS THAN F RETURN TO RTNA +4
2246    2433  0271              ESP
2247    2434  0073              ICT
2248    2435  0073              ICT
2249    2436  0273              ICT
2250    2437  0073              ICT
2251    2440  0075              LSR
```



```
2252    2441  0064              LSP
2253    2442  0203              JUMP FB IND
2254
2255    2443  0270      TSTG0,  ROTATE ZERO       /F WAS 0, BRING UP NEXT BIT
2256
2257    2444  0064              LSP               /RESTORE F
2258
2259    2445  0260              OPEN TEMPG        /G TO SR
2260    2446  0071              ESP
2261    2447  0275              LSR
2262
2263    2450  0120              BR SR7 ZERO       /TEST G
2264    2451  2421              NEXTG             /MATCHS F, GO BRING UP NEXT G BIT
2265
2266    2452  0270              OPEN RTNA         /G IS LESS THAN F,  RETURN TO RTNA +2
2267    2453  0271              ESP
2268    2454  0226              JUMP F5
2269    2455  2436              GLESSF+4
2270
2271
2272
2273                    /[SUBROUTINE: FIND TRACK CONT.]
2274
2275    2456  0070      HOMERR, LCT               /HOME FOUND BEFORE LAST STEP TAKEN
2276    2457  0050              KHOMERR
2277    2460  0226              JUMP F5
2278    2461  2610              GOERDN
2279
2280
2281                    /[SUBROUTINE: DIFFERENCE]
2282                    /THIS SUBROUTINE COMPUTES THE DIFFERENCE BETWEEN TWO EIGHT BIT
2283                    /NUMBERS. ENTER WITH THE RETURN ADDRESS IN RTN, A IN THE
2284                    /COUNTER AND B IN THE SHIFT REGISTER. EXIT IS MADE WITH THE
2285                    /COMPLIMENT OF THE DIFFERENCE IN THE SHIFT REGISTER.
2286                    /EXIT IS TO RTN IF A>=B.  EXIT IS TO RTN+2 IF A<B
2287
2288
2289
2290
2291    2462  0230      DIF,    OPEN TEMPA        /OPEN TEMPORARY PATH THRU THE SP
2292
2293    2463  0126              BR COFL T         /HAS A REACHED ALL ONES YET?
2294    2464  2501              DIFB              /YES, GO GET B FOR THE DIFFERENCE
2295
2296    2465  0064              LSP               /NO, GET B
2297    2466  0075              LSR               /A INTO SHIFT REG
2298    2467  0071              ESP               /B INTO COUNTER
2299
2300    2470  0126              BR COFL T         /HAS B REACHED ALL ONES YET?
2301    2471  2503              DIFA              /YES, GO GET A FOR THE DIFFERENCE
2302
2303    2472  0073              ICT               /INCREMENT B
2304    2473  0064              LSP               /, BRING BACK A
2305    2474  0075              LSR               /B INTO SHIFT REG
2306    2475  0071              ESP               /A INTO COUNTER
```

```
2307    2476  0073          ICT             /INCREMENT A
2308    2477  0226          JUMP F5         /GO BACK TO TEST A AGAIN
2309    2502  2463          DIF+1
2310
2311
2312    2501  0270  DIFB,   OPEN RTNA       /B IS THE COMPLEMENT OF THE DIFFERENCE
2313    2502  0203          JUMP F0 IND     /EXIT A>=B
2314
2315
2316    2503  2270  DIFA,   OPEN RTNA       /A IS THE COMPLEMENT OF THE DIFFERENCE
2317    2504  0071          ESP             /INCREMENT THE RETURN ADDRESS BY 2
2318    2505  0073          ICT
2319    2506  0073          ICT
2320
2321    2507  0064          LSP             /RESTORE RETURN ADDRESS TO SCRATCHPAD AND A TO BR
2322    2510  0075          LSR
2323    2511  0071          ESP
2324    2512  0064          LSP
2325    2513  0075          LSR
2326
2327    2514  0203          JUMP F0  IND    /EXIT A<B
2328
2329
2330                /[ROUTINE: FIND HEADER CONT.]
2331                /THIS ROUTINE CHECKS THE CRC, AND THE RESULTS OF THE TRACK
2332
2333                /AND SECTOR COMPARISONS.
2334
2335
2336
2337
2338    2515  0070  CKHCRC, LCT             /PRESET BIT COUNT TO 16 FOR CRC
2339    2516  0357          -16-1
2340
2341    2517  0132          BR CRC16 ONE    /IS CRC ZERO
2342    2520  2546          HCRCER          /NO, LOG ERROR AND TRY AGAIN
2343
2344    2521  0073          ICT             /YES, CRC GOOD SO FAR, BUMP BIT CNTR
2345
2346    2522  0054          CRC ZERO        /BRING UP NEXT CRC BIT
2347
2348    2523  0124          BR COFL F       /ALL BITS TESTED?
2349    2524  2517          .-5             /NO, BRANCH BACK
2350
2351    2525  0210          OPEN ERREG      /YES, CRC WAS GOOD, CHECK TRK COMP
2352    2526  0271          ESP
2353    2527  0075          LSR
2354
2355    2530  0270          LCT             /ROTATE BIT 0 TO BIT 7
2356    2531  0370          -7-1
2357    2532  0074          ROTATE ZERO
2358    2533  0073          ICT
2359    2534  0124          BR COFL F       /DONE ROTATING?
2360    2535  2532          .-3             /NO
2361
```



```
2362    2536  0122          BR SR7 ONE      /YES, WAS THERE A BAD COMPARE
2363    2537  2542          TKSKER          /YES, GO REPORT A TRACK SEEK ERROR
2364
2365    2540  0264          OPEN RTNB       /CORRECT TRACK, EXIT FROM FIND HDR SUBR
2366    2541  0207          JUMP F1 IND
2367
2368
2369
2370
2371    2542  0070  TKSKER, LCT             /HEADER CRC WAS GOOD BUT TRACK
2372    2543  0150          KTKSKER         /ADDRESS DID NOT COMPARE, MUST
2373    2544  0226          JUMP F5         /EXIT TO ERROR DONE
2374    2545  2610          GOERDN
2375
2376
2377    2546  0070  HCRCER, LCT             /HEADER CRC WAS NOT CORRECT
2378    2547  0140          KHCRCER
2379    2550  0075          LSR
2380    2551  0210          OPEN ERREG      /LOG THE ERROR
2381    2552  0064          LSP
2382
2383    2553  0226          JUMP F5         /GO TRY ANOTHER HEADER
2384    2554  2557          BADHDR
2385
2386
2387
2388
2389    2555  0170  BDSRT,  BR FLAGD T      /BAD START ON DATA AM OR IDAM?
2390    2556  2577          BADDAM
2391
2392    2557  0230  BADHDR, OPEN TEMPA      /IDAM, INCREMENT AND TEST BAD START INNER COUNT
2393    2560  0071          ESP
2394    2561  0073          ICT
2395    2562  0275          LSR
2396    2563  0064          LSP
2397    2564  0124          BR COFL F
2398    2565  2615          PTRYAG          /NO OVERFLOW, GO TRY ANOTHER HEADER
2399    2566  0234          OPEN TEMPB      /INCREMENT AND TEST BAD START OUTER COUNT
2400    2567  0071          ESP
2401    2570  0073          ICT
2402    2571  0124          BR COFL F
2403    2572  2615          PTRYAG          /NO OVERFLOW, GO TRY AGAIN
2404    2573  0070  XSTRYS, LCT             /TOO MANY TRIES FOR A HEADER
2405    2574  0160          KXSTRYS
2406    2575  0226          JUMP F5
2407    2576  2610          GOERDN
2408
2409
2410    2577  0234  BADDAM, OPEN TEMPB      /BAD START ON DATA AM, INCREMENT AND TEST BAD START COUNT
2411    2600  0071          ESP
2412    2601  0073          ICT
2413    2602  0075          LSR
2414    2603  0064          LSP
2415    2604  0124          BR COFL F
2416    2605  2617          PGETDA          /NO OVERFLOW GO TRY FOR DATA AM AGAIN
```

```
2417  2606  0070  NODAM,  LCT             /TRIED 3 IMES FOR DATA AM, GO FLAG THE ERROR
2418  2607  0170          KNODAM
2419  2610  0210  GOERON, OPEN ERREG
2420  2611  0075          LSR
2421  2612  0064          LSP
2422  2613  0212          JUMP F2
2423  2614  1000          ERDONE
2424
2425  2615  0216  PTRYAG, JUMP F3          /POINTER TO FIND AN IDAM
2426  2616  1413          TRYAGN
2427
2428
2429  2617  0216  PGETDA, JUMP F3          /POINTER TO FIND DATA AM
2430  2620  1441          GETDAM
2431
2432
2433
2434                /[ROUTINE: INITIALIZE CONT.]
2435  2621  0070  WRONG,  LCT             /HOME WAS FOUND WHILE STEPPING OUT
2436  2622  0030          K4RONG
2437  2623  0226          JUMP F5
2438  2624  2610          GOERDN
2439
2440  2625  0070  DNRCAL,   LCT          /CALL CHECK READY SUBROUTINE
2441  2626  1771          PNORDY
2442  2627  0226          JUMP F5
2443  2630  2640          CHKRDY
2444
2445  2631  0070  INTRDY, LCT             /DRV 0 IS READY CALL BOOT SUBROUTINE TO
2446  2632  0770          GOREAD          /MOVE TO TRACK 1, THEN GO TO READ ROUTINE TO
2447  2633  0274          OPEN RTN        /PICK UP SECTOR 1
2448  2634  0075          LSR
2449  2635  0064          LSP
2450  2636  0202          JUMP F0
2451  2637  0252          BOOT
2452
2453
2454
2455
```



```
2456                /[SUBROUTINE: CHECKREADY]
2457
2458                /SUBROUTINE TO CHECK THE SELECTED DRIVE TO SEE IF THE
2459                /DISK IS INSERTED AND UP TO SPEED.  THIS IS DONE BY CHECKING TO SEE IF
2460                /THE INTERVAL BETWEEN 2 INDEX PULSES IS BETWEEN 150 MS AND 180 MS.  RETURN
2461                /ADDRESS IS PLACED IN THE COUNTER BEFORE ENTRY.  NOT READY RETURN IS
2462                /TO THE RETURN ADDRESS.  READY RETURN IS TO THE RETURN ADDRESS PLUS 2
2463
2464
2465
2466                /
2467  2642  0274  CHKRDY, OPEN RTN        /SAVE RETURN ADDRESS
2468  2643  0075          LSR
2469  2644  0064          LSP
2470
2471  2645  0070          LCT             /2 TO CNTR FOR INDEX PASS COUNT
2472  2646  0375          -2-1
2473
2474  2647  0230          OPEN TEMPA      /FOR INDEX PASS COUNT
2475
2476  2650  0075  NEWPAS, LSR             /RESTORE INDEX PASS COUNT
2477  2651  0064          LSP
2478
2479  2652  0061          FLAG OFF        /CLOSE INDEX WINDOW
2480
2481  2653  0042          LDMD            /TO CLEAR INDEX FLOP
2482
2483  2654  0070          LCT             /FOR 15 TIMES THROUGH 10MS LOOP
2484  2655  0360          -15-1
2485
2486  2656  0234  STDLY,  OPEN TEMPB      /RESTORE OUTER COUNT
2487  2657  0075          LSR
2488  2660  0064          LSP
2489
2490  2661  0070          LCT             /FOR 40 TIMES THROUGH .25MS LOOP
2491  2662  0327          -40-1
2492
2493  2663  0240          OPEN TEMPC
2494  2664  0075  SPBACK, LSR             /RESTORE INNER COUNT
2495  2665  0064          LSP
2496
2497  2666  0070          LCT             /WAIT .25 MS FOR INDEX
2498  2667  2005          -250-1
2499  2670  0116          BR INDX T
2500  2671  2714          SAWIND          /FOUND INDEX
2501  2672  0073          ICT
2502  2673  0124          BR COFL F
2503  2674  2666          .-4
2504
2505  2675  0240          OPEN TEMPC      /INCREMENT AND TEST  INNER COUNT
2506  2676  0071          ESP
2507  2677  0073          ICT
2508  2700  0124          BR COFL F
2509  2701  2664          SPBACK
2510
```

```
2511    2720  0234            OPEN TEMPB      /INCREMENT AND TEST OUTER COUNT
2512    2721  0271            ESP
2513    2722  0073            ICT
2514    2723  0124            BR COFL F
2515    2724  2655            STDLY+1
2516
2517    2725  0176            BR FLAGO ONE    /WAS INDEX WINDOW OPEN?
2518    2726  2767            UNRDY           /YES, NO INDEX WITHIN 180MS
2519
2520    2727  0062            FLAG ON         /NO, OPEN WINDOW
2521
2522    2730  0070            LCT             /FOR 3 TIMES THROUGH 10 MS LOOP
2523    2731  0374            -3-1            /THE WINDOW IS 30 MS WIDE
2524
2525    2732  0226            JUMP F5         /GO LOOK FOR INDEX
2526    2733  2654            STDLY
2527
2528
2529    2734  0230    SAWIND, OPEN TEMPA      /INCREMENT AND TEST INDEX PASS COUNT
2530    2735  0271            ESP
2531    2736  0073            ICT
2532    2737  0124            BR COFL F
2533    2740  2646            NEWPAS          /THIS WAS 1ST INDEX, GO LOOK FOR SECOND
2534
2535    2741  0174            BR FLAGO ZERO   /THIS WAS 2ND INDEX, WAS THE WINDOW OPEN?
2536    2742  2767            UNRDY           /NO, INDEX OCCURRED TOO SOON
2537
2538    2743  0274            OPEN RTN        /YES, INDEX OCCURRED BETWEEN 150 AMD 180 MS, INCREMENT
2539    2744  0071            ESP             /RETURN ADDRESS BY 2
2540    2745  0073            ICT
2541    2746  0073            ICT
2542    2747  0075            LSR
2543    2750  0064            LSP
2544
2545    2751  0214            OPEN STAT       /SET DRV RDY BIT OF STAT IN SR
2546    2752  0071            ESP
2547    2753  0075            LSR
2548
2549    2754  0076            ROTATE ONE
2550
2551    2755  0061            FLAG OFF        /FLAG OFF TO INDICATE FIRST PASS
2552
2553    2756  0070    ROT3,   LCT             /END AROUND SHIFT OF THE NEXT 3 BITS OF STAT IN SR
2554    2757  0374            -3-1
2555    2760  0122            BR SR7 T
2556    2761  2765            .+4
2557    2762  0074            ROTATE ZERO
2558    2763  0226            JUMP F5
2559    2764  2766            .+2
2560    2765  0076            ROTATE ONE
2561    2766  0073            ICT
2562    2767  0124            BR COFL F
2563    2770  2760            .-8
2564
2565    2771  0176            BR FLAGO T      /WAS IT FIRST 3 OR LAST 3
```



```
2566    2772  2764            EXCHRY          /LAST, GO EXIT
2567
2568    2773  0140            BR WRTEN F      /UPDATE WRITE PROTECT BIT OF STAT IN SR
2569    2774  2764            .+4
2570    2775  0074            ROTATE ZERO
2571    2776  0226            JUMP F5
2572    2777  3001            .+2
2573    3000  0076            ROTATE ONE
2574
2575    3001  0062            FLAG ON         /GO SHIFT AROUND LAST 3 BITS
2576    3002  0226            JUMP F5
2577    3003  2736            ROT3
2578
2579    3004  0064    EXCHRY, LSP             /RESTORE THE STAT
2580
2581    3005  0274            OPEN RTN        /RETURN FROM CHKRDY SUBROUTINE
2582    3006  0217            JUMP F3 IND
2583
2584    3007  0214    UNRDY,  OPEN STAT       /CLEAR DRV READY BIT OF STAT IN SR
2585    3010  0071            ESP
2586    3011  0075            LSR
2587    3012  0074            ROTATE ZERO
2588
2589    3013  0226            JUMP F5         /GO UPDATE REST OF STAT IN SR
2590    3014  2735            ROT3-1
2591
2592    3015  0000            0               /OPEN
2593    3016  0000            0               /OPEN
2594    3017  0000            0               /OPEN
2595
2596
2597                  $
```

```
0000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
0100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

0200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
0300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

0400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
0500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

0600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
0700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

1000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
1100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

1200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
1300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

1400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
1500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

1600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
1700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

2000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
2100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

2200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
2300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

2400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
2500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

2600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
2700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

3000
3100

3200
3300

3400
3500

3600
3700
```



```
4000
4100

4200
4300

4400
4500

4600
4700

5000
5100

5200
5300

5400
5500

5600
5700

6000
6100

6200
6300

6400
6500

6600
6700

7000
7100

7200
7300

7400
7500

7600
7700
```

ERRORS DETECTED: 0

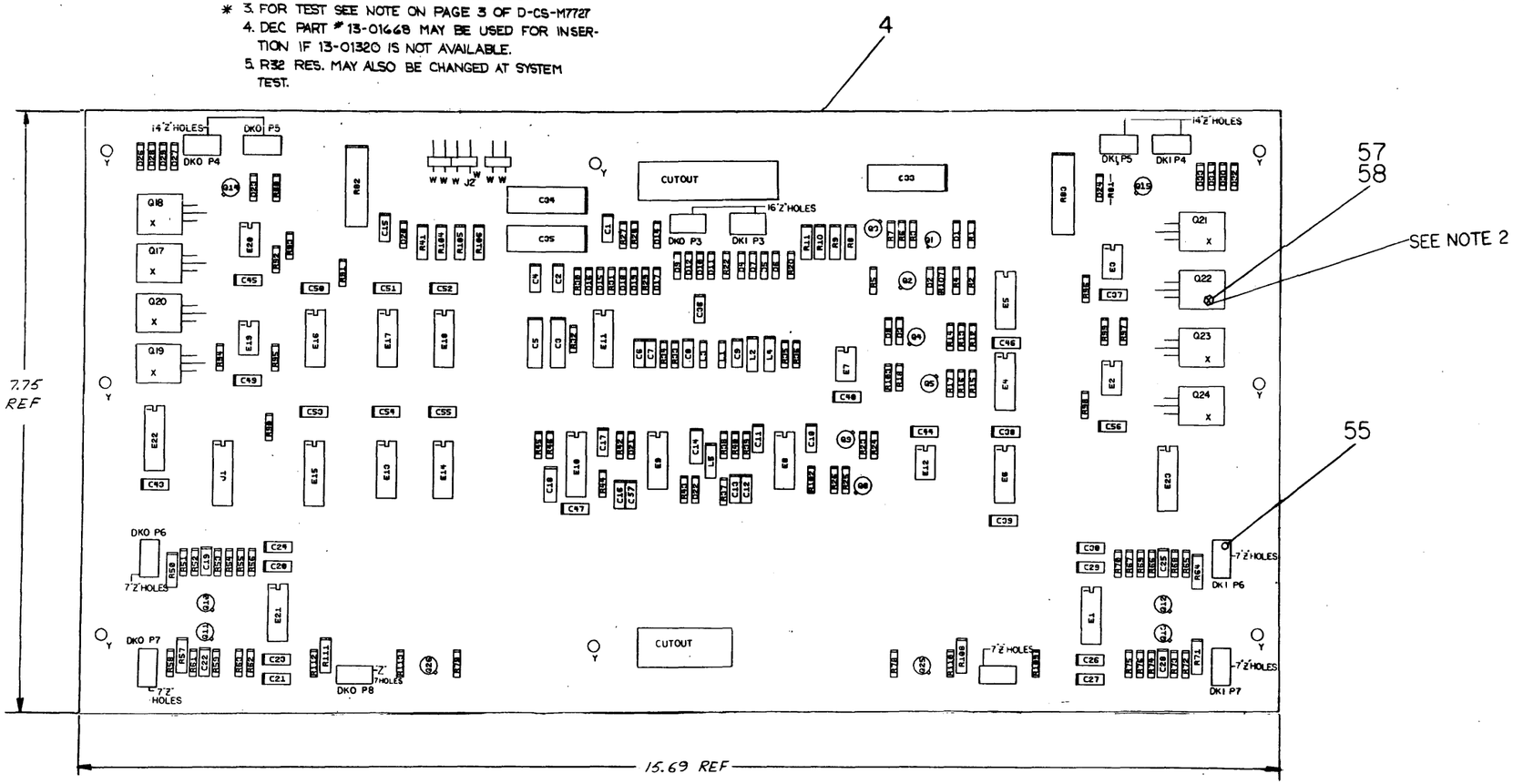
LINKS GENERATED: 0

RUN-TIME: 18 SECONDS

3K CORE USED

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE 1/4W, ±5%.
2. WASHER TO BE USED BETWEEN ITEMS 57 AND 58 WILL BE SUPPLIED WITH THE D49C8 TRANSISTOR ONLY BY G.E.. THE WASHER IS ONLY REQUIRED WHEN USING THE G.E. TYPE TRANSISTOR.
3. * FOR TEST SEE NOTE ON PAGE 3 OF D-CS-M7727
4. DEC PART # 13-01668 MAY BE USED FOR INSERTION IF 13-01320 IS NOT AVAILABLE.
5. R32 RES. MAY ALSO BE CHANGED AT SYSTEM TEST.



7473	11	4
75451	4	8
74157	8	16
75452	4	8
74123	8	16
IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		
IC PIN LOCATIONS		

REV.	REVISIONS	CHK	CHANGE NO.	DEC NO.	EIA NO.
B	C. YOUSE 10-8-75	M	M7727-00001		
C	W. SMITH		M7727-00002		
D	D. ZWICKER 1/14/77		M7727-00003		
E	H. DIAB		M7727-00004		

H. Diab (M) 3-2-78

FIRST USED ON OPTION MODEL: M7727

ETCH BOARD REV. B

SEMICONDUCTOR CONVERSION CHART

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DRN.	DATE 12/31/74
CHK'D	DATE 1/24/75
ENG.	DATE 1-24-75
PROJ. ENG.	DATE 1/24/75
PROD.	DATE 2/4/75
NEXT HIGHER ASSY	
SCALE	
SHEET 1 OF 6	

digital

TITLE: READ/WRITE CONTROL

SIZE	CODE	NUMBER	REV.
D	CS	M7727-0-1	E

DIST.

SIZE D CODE CS NUMBER M7727-0-1 REV. E

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
		X-Y COORDINATE HOLE LOCATION	K-CO-M7727-0-4	1
		ASSY/ DRILL HOLE LAYOUT	D-AH-M7727-0-5	2
		MODULE ECO HISTORY	B-MH-M7727-0-6	3
1		ETCHED CIRCUIT BOARD	D-IA-5011370-00	4
2	C17, C18	CAP 100 pf	1000016-00	5
1	C9	CAP 180 pf	1000020-00	6
2	C8, C14	CAP 220 pf	1000021-00	7
32	C1, C2, C4, C10, C11, C15 C16, C20, C21, C23, C24 C26, C27, C29, C30, C37, C38, C39, C40 C43 C44, C45, C46, C47 C49 - C59	CAP .01 µf	1001610-00	8
2	C3, C5	CAP 6.8 µf 35V	1005306-00	9
2	C34, C35	CAP 190 µf	1009433-00	10
1	C33	CAP 50 µf	1000080-00	11
4	C7, C6, C12, C13	CAP .047 µf	1010978-32	12
5	C19, C25, C22, C28, C36	CAP .005 µf	1001765-00	13
10	D4, D7, D9, D12, D14 D15, D16, D17, D18, D19	DIODE D671	1103309-00	14
8	D3, D5, D6 D8 D10 D11, D21, D22	DIODE D672	1105275-00	15
10	D23, D24, D26, D27 D28, D29, D30, D31 D32, D33	DIODE IN4004	1105796-00	16
1	D20	DIODE IN4742 12V	1109502-00	17
2	D1, D2	DIODE 5.1 V.	1110713-00	18
9	R90, R92 — R99	RES 150 1/4W 5%	1300250-00	19
4	R41, R104, R105, R106	RES 680 1/2W 5%	1300347-00	20
12	R6, R14, R17, R23, R24, R26, R46 R78, R79, R80, R81 R91,	RES 1K 1/4 W 5%	1300365-00	21
4	R8 — R11	RES 1.2K 1/2W 5%	1300385-00	22
6	R30, R57, R64, R71, R102, R111	RES 68 1/2W 5%	1309405-00	23
7	R13, R16, R53, R62 R68, R75, R102	RES 1.5K 1/4W 5%	1300391-00	24
4	R35, R36, R39, R40	RES 511 1/8W 1%	1302411-00	25
1	R5	RES 2.74K 1/8W 1%	1304868-00	26
11	R2, R4, R7, R12, R15 R18, R22, R25, R27 R42, R43	RES 3.3K 1/4W 5%	1300439-00	27
6	R1, R20, R21, R44 R45, R107	RES 10K 1/4W 5%	1300479-00	28
11	R3, R37, R38, R52 R58, R63, R66, R72 R76, R109 R112	RES 1.21K 1/8W 1%	1302871-00	29
1	R32	RES 220Ω 5% 1/4W	1300271-00	30 *
2	R33, R34	RES 4K 1/8W 1%	1303047-00	31
2	R28, R29	RES 34.8K 1/8W 1%	1303156-00	32
4	R51, R61, R65, R73	RES 10K 1/8W 1%	1303312-00	33
2	R82, R83	RES 100 5W 5%	1309094-00	34
2	R30, R31	RES 19.6 K 1/8W 1%	1309419-00	35
6	R55, R59, R67, R74 R116, R113	RES 4.64K 1/4W 1%	1304856-00	36

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
1	L5	CHOKE 1000 MH Y	1602729-00	37
2	L2, L4	CHOKE 33 MH Y	1601759-00	38
2	L1, L3	CHOKE 120 MH Y	1610663-00	39
1	E17	I.C. 7450	1905580-00	40
2	E16, E18	I.C. 7473	1905587-00	41
1	E14	I.C 7402	1909004-00	42
1	E13	I.C 7404	1909686-00	43
2	E4, E6	I.C 7408	1910155-00	44
3	E1, E9, E21	I.C. 1414	1910337-00	45
5	E2, E3, E12, E19, E20	I.C 75451	1910406-00	46
1	E10	I.C 74123	1910436-00	47
2	E8, E11	I.C. 72733	1910644-00	48
1	E15	I.C. 74157	1910655-00	49
1	E5	I.C. 7406	1910741-00	50
1	J1	I.C SOCKET 16 PIN	1211813-02	51
9	Q9 THRU Q15, Q25Q26	TRANS MXAA05	1510705-00	52
6	Q1 — Q5, Q8	TRANS MXAA55	1510706-00	53
8	Q17 — Q24	TRANS D44C8	1510421-00	54
86	"2" HOLES	WIRE WRAP PIN	1210385-01	55
3	J2	CONN 2 POS	1212204-00	56
8	"X" HOLES	SCREW, PAN HD 4/40 X 5/16	9006010-01	57
8	"X" HOLES	NUT, KEP 4/40 X 1/4 X 3/32	9006557-00	58
1	E7	I.C. 75452	1910695-00	59
4	R54, R56, R69, R70	RES 19.7K 1/4W 1%	1302941-00	60

REVISIONS

CHK	CHANGE NO.	REV.

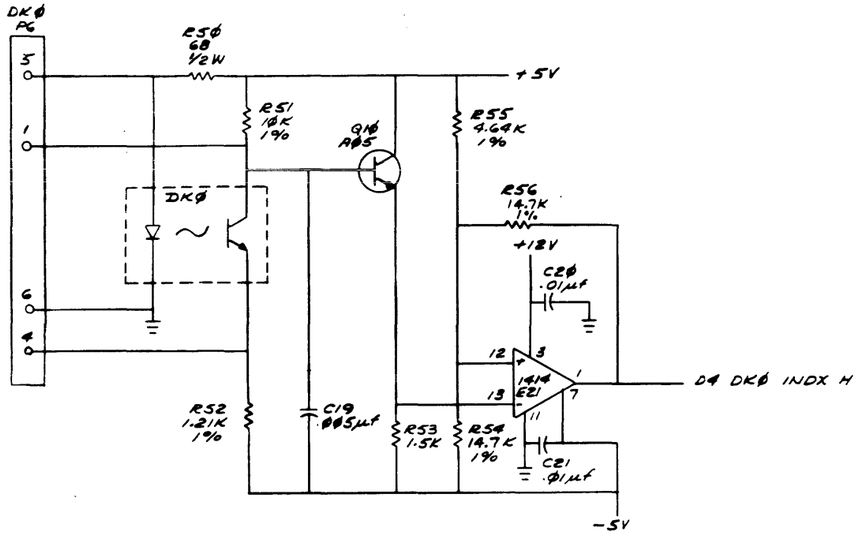
TITLE	READ/WRITE CONTROL	SIZE	CODE	NUMBER	REV.
SCALE	SHEET 2 OF 6	D	CS	M7727-0-1	E
		DIST.			

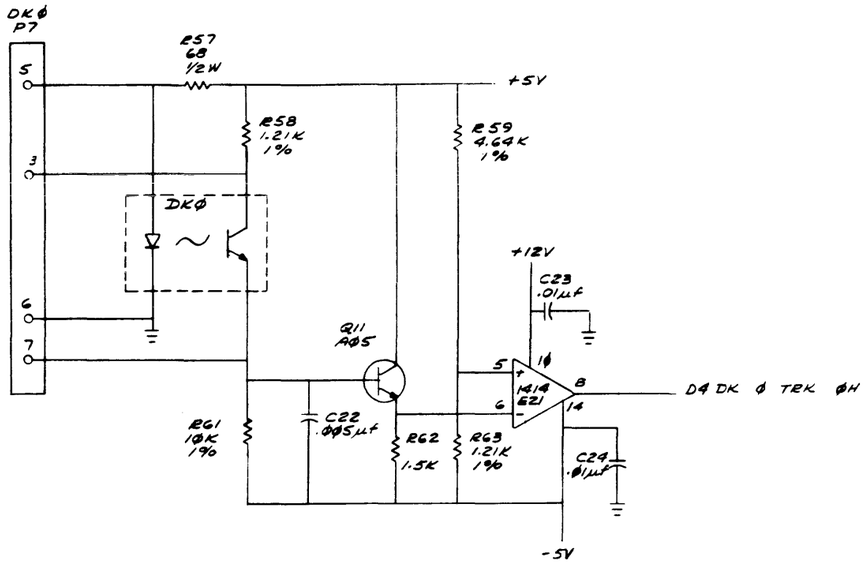
SIZE D CODE CS M7727-0-1 E

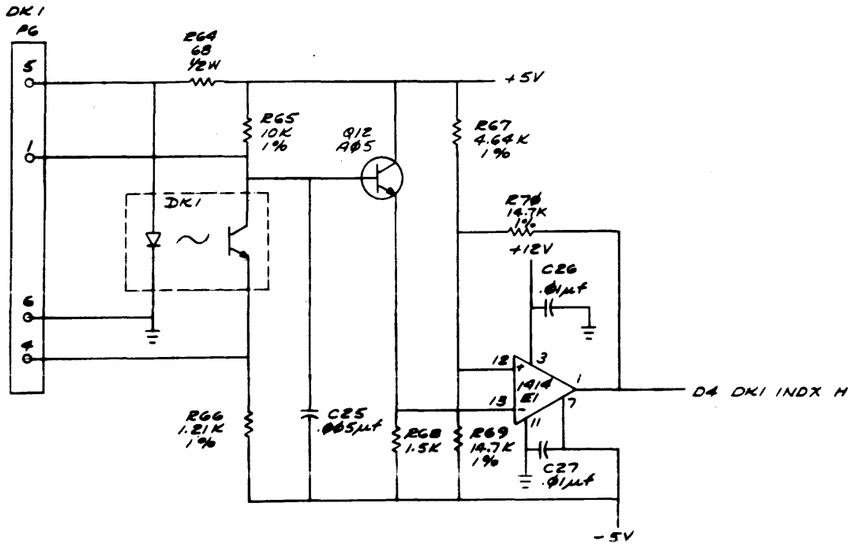
DG WT GATE H
DG ABOVE TK 43 H
DG SEL WT PROT L
DG ERASE H
DG WT DATA H
DG SEL DK Ø H
DG DC LO L
DG SEL DK 1 H
R/W BUS +
R/W BUS -
D3 RAW DATA L
+24V
+12V
+5V
-5V
R1 10K
R2 3.3K
R3 1.21K 1%
R4 3.3K
R107 10K
E5 2.74K 1%
R6 1K
R7 3.3K
R8 1.2K 1/2W
R9 1.2K 1/2W
R10 1.2K 1/2W
R11 1.2K 1/2W
C36 .005µf
R12 3.3K
R13 1.5K
R14 1K
R15 3.3K
R16 1.5K
R17 1K
R18 3.3K
R103 3.3K
R22 10K
R20 10K
R23 1K
R24 1K
R25 3.3K
R26 1K
R27 3.3K
R28 34.8K 1%
R29 34.8K 1%
R30 19.6K 1%
R31 19.6K 1%
C1 .01µf
R32, 560Ω — USE IF E11-7 IS < THAN 2.0
R32, 680Ω — USE IF E11-7 IS < THAN 2.6
R32, 820Ω — USE IF E11-7 IS < THAN 2.8 (Vp-p)
R32, 1.0K — USE IF E11-7 IS < THAN 2.8 (Vp-p)
R32, 2200Ω (NOMINAL)
R32, 1.5K — USE IF E11-7 IS > THAN 3.2 (Vp-p)
APPLY 12 MX BETWEEN E11-1 AND E11-14. THEN SELECT R32 FOR E11-7, OR E11-8 TO BE 2.0 TO 3.2 (Vp-p)
R104 680 1/2W
R105 680 1/2W
R106 680 1/2W
R241 680 1/2W
D20 IN4742
C15 .01µf
C17 100 pf
R244 10K
C18 100 pf
R245 10K
R246 1K
C2 .01µf
C3 6.8µf
C4 .01µf
C5 6.8µf
C6 .047µf
C7 .047µf
R233 464 1%
R234 464, 1%
L1 120µhy
L2 33µhy
L3 120µhy
L4 33µhy
C8 220pf
C9 180pf
R235 511 1%
R236 511 1%
C10 .01µf
C11 .01µf
R102 1.5K
C12 .047
C13 .047
R239 511, 1%
R237 1.21K 1%
R238 1.21K 1%
R240 511 1%
L5 1000 µhy
C14 220pf
C16 .01µf
D1 5.1V
D2 5.1V
Q1 A55
Q2 A55
Q3 A55
Q4 A55
Q5 A55
Q8 A55
Q9 A05
D10 672
D3 672
D5 672
D4 671
D6 672
D7 671
D8 672
D9 671
D11 672
D12 671
D14 671
D15 671
D16 671
D17 671
D18 671
D19 671
D21 672
D22 672
DK Ø HEAD P3
DK 1 HEAD P3
74Ø8 E4
74Ø4 E13
74Ø6 E5
74Ø8 E6
75452 E7
733 E11
733 E8
74123 E10
74Ø2 E14
1414 E9

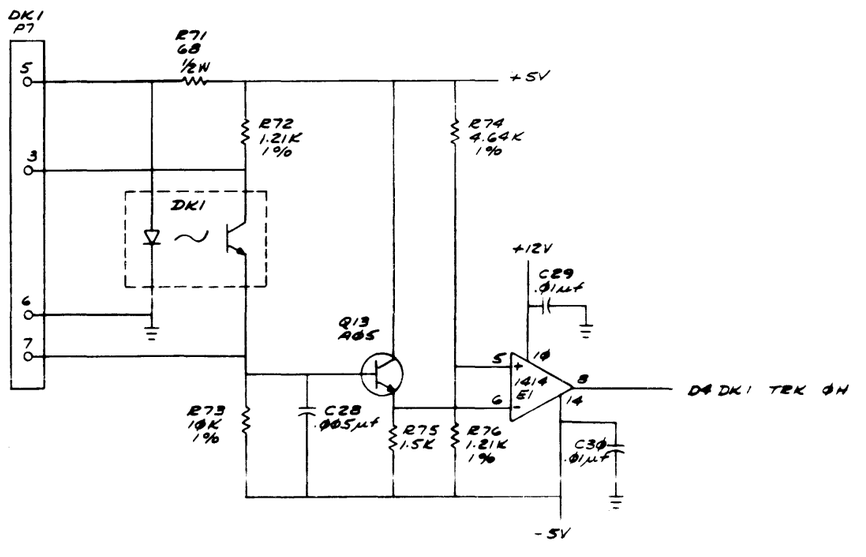
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE READ / WRITE CONTROL (D3)
SCALE —/—
SHEET 3 OF 6
SIZE D CODE CS NUMBER M7727-Ø-1 REV. E
DIST.









REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	READ / WRITE CONTROL (D4)	SIZE/CODE D CS	NUMBER M7727-Ø-1	REV E
SCALE		SHEET 1 OF 2	DIST.	

M7727-Ø-1 E
DCS

DS INIT L
DG SEL DK 1 H
DG STEP L
DG OUT H
DG SEL DK Ø H
DG DC LØ L
DS INIT L

E91 1K
E90 150
+5V
7473 E18
7473 E16
7450 E17
7402 E14
7404 E13
7451 E20
7451 E19
7451 E3
7451 E2
R92 150
R93 150
R95 150
R94 150
R96 150
R97 150
R98 150
R99 150
Q17 D44C8
Q18 D44C8
Q19 D44C8
Q20 D44C8
Q21 D44C8
Q22 D44C8
Q23 D44C8
Q24 D44C8
D29
D27
D26
D28
D33
D31
D30
D32
DK Ø P4
DK 1 P4
DK Ø HEAD STEPPER
DK 1 HEAD STEPPER
+24V

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
READ / WRITE CONTROL (D5)	D	DCS	M7727-Ø-1	E
SCALE —— SHEET 5 OF 6	DIST.			

DKØ PS

R111 68 1/2W

R112 1.21K 1%

R79 1K

R113 4.64K 1%

Q26 AØ5

+5V

74157 E15

DG SEL WT PROT L

D4DK1 TRK Ø H
D4DKØ TRK Ø H

DG SEL TRK Ø H

D4DK1 INDX H
D4DKØ INDX H

DG SEL INDX H

DG SEL DK Ø H

DG OUT H
DG ERASE H
DG WT GATE H
DG STEP L
D3 RAW DATA L
DG WT DATA H

I.C. SOCKET J1

DG DC LO L
DG SEL DK 1 H
DG ABOVE TK 43 H
DG LOAD HEAD H
DG SEL TRK Ø H
DG SEL INDX H

DK1 PS

R1Ø8 68 1/2W

R1Ø9 1.21K 1%

R78 1K

R11Ø 4.64K 1%

Q25 AØ5

7545I E12

7404 E13

7408 E6

DG SEL DK 1 H

DG LOAD HEAD H

DS INIT L

R8Ø 1K

R81 1K

+5V

Q14 AØ5

Q15 AØ5

DKØ HEAD LOAD SOLENOID

DKØ PS

D23 1N4ØØ4

+24V

R82 1ØØ 5W

DK1 HEAD LOAD SOLENOID

DK1 PS

D24 1N4004

R83 1ØØ 5W

J2

N/C
-5V
GND
+5V
+24V RETURN
+24V

+24V
+5V
-5V

C33 5Ø µF
C34 19Ø µF
C37-C4Ø C43-C47 C49-C56 .01UF
C35 19Ø µF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

SEQUENCE	
H771 POWER SUPPLY	B-DD-H771-Ø
H771-A CIRCUIT SCHEMATIC	D-CS-H771-A-1
H771-C CIRCUIT SCHEMATIC	D-CS-H771-C-1
H771-D CIRCUIT SCHEMATIC	D-CS-H771-D-1
RXØ1 POWER BOARD ASSY	D-AD-7010718-0-0
RXØ1 POWER SUPPLY BOARD	D-CS-5411398-0-1

THIS IS PRINT SET ☐☐☐☐

UNIT VARIATIONS		PRINT SET
VAR	TITLE	1
H771-A	RXØ1 POWER SUPPLY, 115V, 6ØHZ	X
H771-C	RXØ1 POWER SUPPLY, LOW VOLT, 5ØHZ	X
H771-D	RXØ1 POWER SUPPLY, HIGH V, 5ØHZ	X

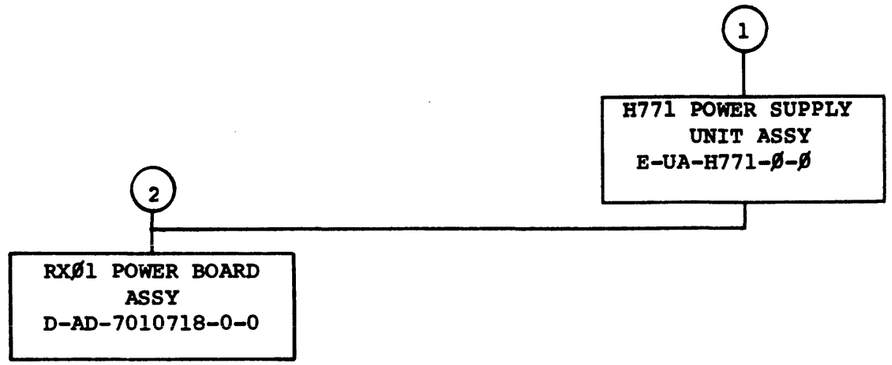
REVISIONS		
DATE	CHG. NO.	REV
7-75	H771-1	A
10-75	H771-2	B
11-75	H771-3	C
3-76	H771-4	D
1-78	H771-5	E

USED ON OPTION/MODEL	
RXØ1	

SHEET 1 OF 3

DRN. W. McCarthy	DATE 2/3/75	TITLE H771 POWER SUPPLY
CHK'D. W.F. McCarthy	DATE 6/13/75	
PROJ ENG.	DATE 6/13/75	
PROD.	DATE 6/13/75	SIZE B / CODE DD / NUMBER H771-Ø / REV E
FIELD SERV.	DATE 6/13/75	DIST

DRB 106



TITLE		SIZE	CODE	NUMBER	REV
H771 POWER SUPPLY	SHEET 2 OF 3	B	DD	H771-Ø	E

DRB 107
DEC 16-(325)-1062-3-N871

MECHANICAL

CUSTOMER PRINT SET				MFG.	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
1	-				1	E-UA-H771-Ø-Ø	E	2	H771 POWER SUPPLY ASSY	
						E-MD-7412667-0-0	D	1	CHASSIS, POWER SUPPLY	
						D-AD-7010680-0-0	C	1	TRANSFORMER ASSY,6Ø HZ	
						D-AD-7010704-0-0	E	1	TRANSFORMER ASSY, 5Ø HZ	
						C-AD-7010697-0-0	B	1	POWER CORD ASSY	
						D-IA-7010972-0-0	C	1	JUMPER	
						C-MD-7413344-0-0		1	BRACKET, FUSE MOUNTING	
						A-DC-7413403-0-0		1	DECAL, H771-A	
						A-DC-7414250-0-0	A	1	DECAL, H771-C	
						A-DC-7414251-0-0	A	1	DECAL, H771-D	
					2	D-AD-7010718-0-0		1	RXØ1 POWER BOARD ASSY	
						D-IA-7010854-0-0	C	1	READ/WRITE BOARD HARNESS	
						D-IA-7010853-0-0	B	1	DISK CONTROL BOARD HARNESS	

ELECTRICAL

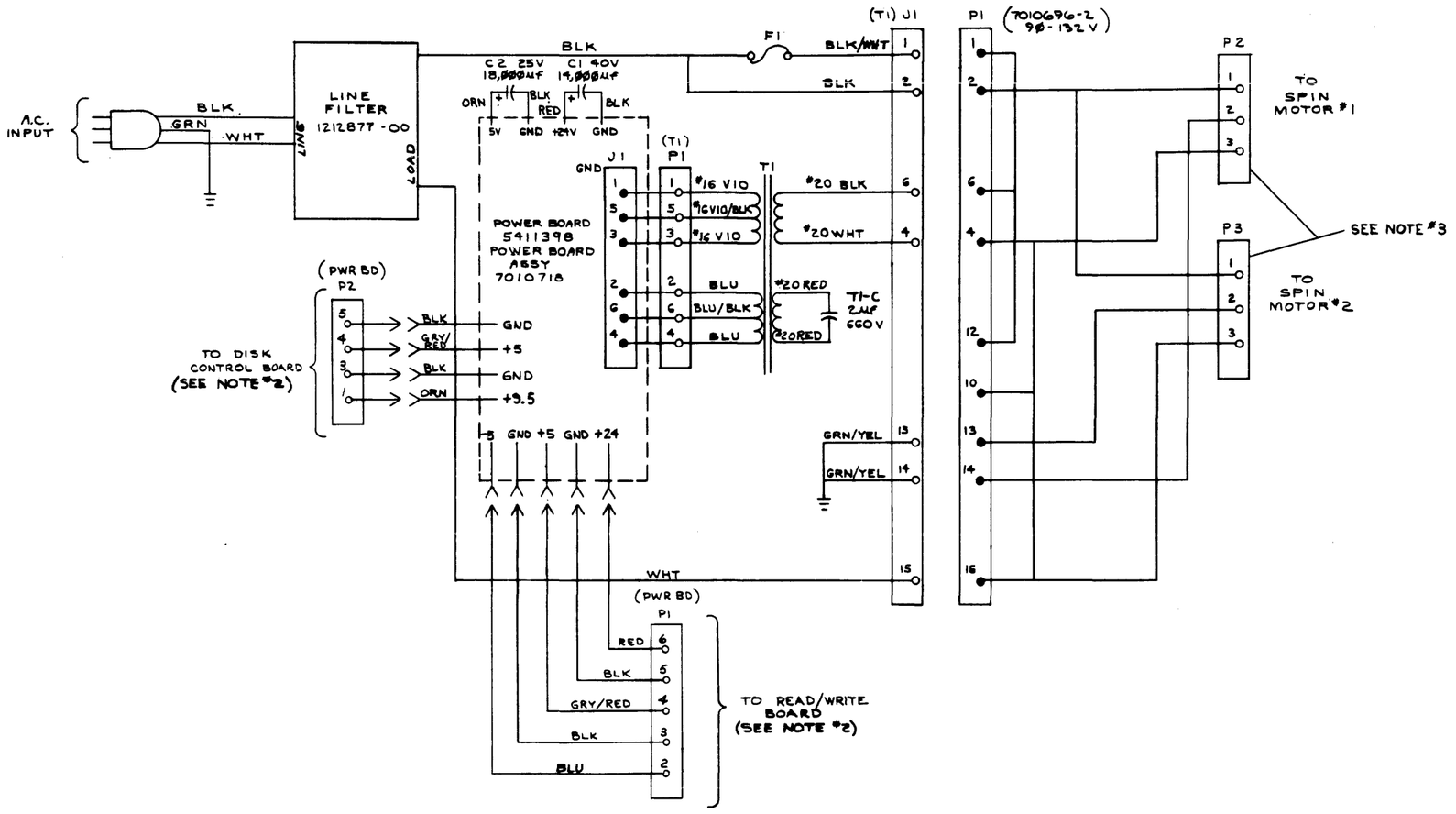
CUSTOMER PRINT SET				MFG	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X					1	B-DD-H771-Ø	E	3	H771 POWER SUPPLY	
X						D-CS-H771-A-1	B	1	H771-A CIRCUIT SCHEMATIC	
X						D-CS-H771-C-1	C	1	H771-C CIRCUIT SCHEMATIC	
X						D-CS-H771-D-1	C	1	H771-D CIRCUIT SCHEMATIC	
						A-SP-H771-Ø-1			ENGINEERING SPECIFICATION	
X					2	D-AD-7010718-0-0	*	1	RXØ1 POWER BOARD ASSY	
X						D-CS-5411398-0-1	*	1	RXØ1 POWER BOARD ASSY	

CUSTOMER PRINT SET CODES		TITLE		SIZE	CODE	NUMBER	REV
	X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED	H771 POWER SUPPLY	SHEET 3 OF 3	B	.DD	H771-Ø	E

DRB 108

DEC 16-(328)-1062-2D-R072

NOTES:
1. ALL WIRE TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.
2. SLOT BETWEEN P1-4 + P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 + P2-5 ALSO CONTAINS A DUMMY PIN.
3. NO DOUBLE CRIMPS ARE ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).

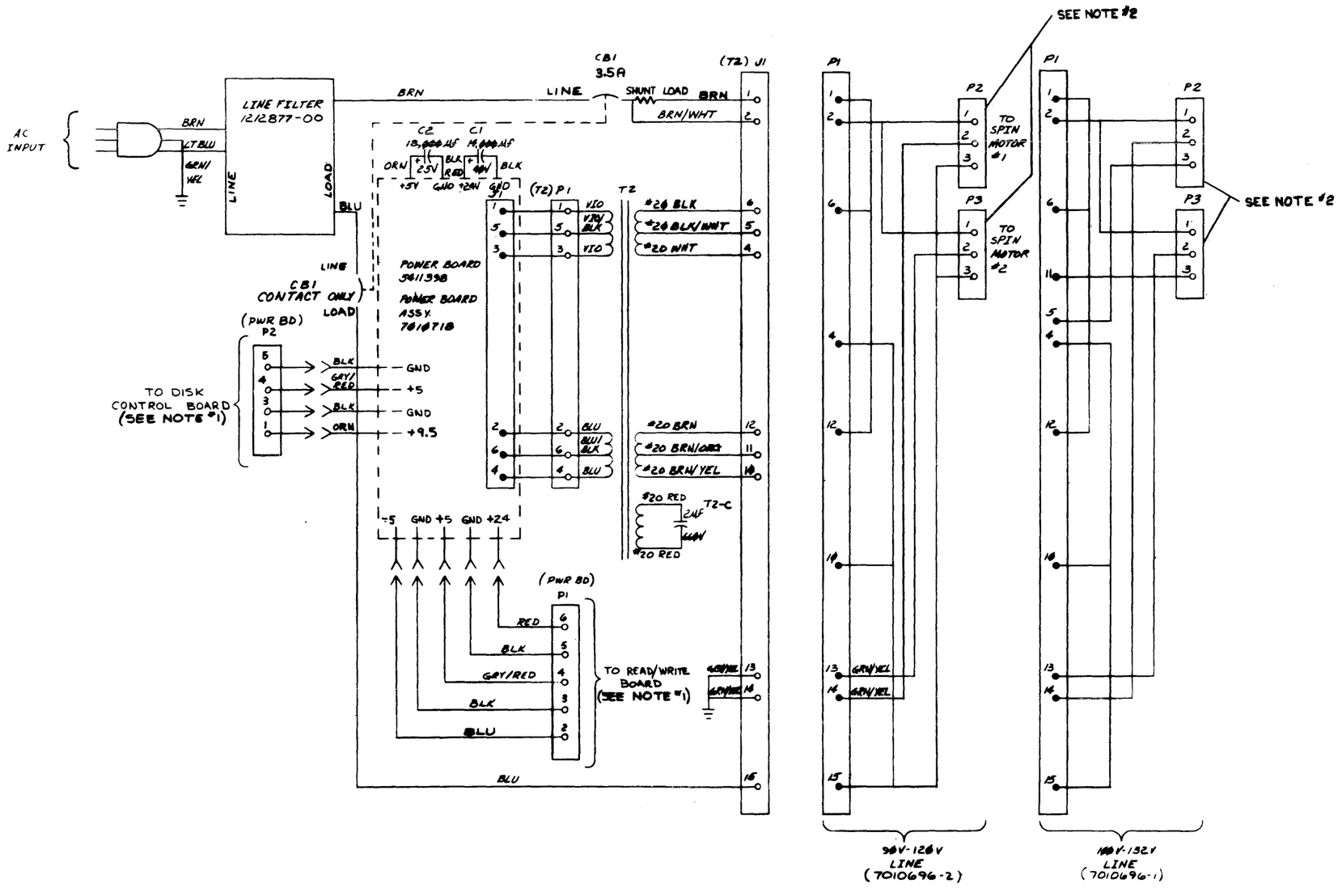


REVISIONS				
CHK	CHANGE NO.	REV.		
[illegible]	H771-00001	A	B. HAZEN	8-20-75
[illegible]	H771-00004	B	B. HAZEN	8-30-Nov-75

DRN. D.E. Olsen	1/22/75	FIRST USED ON: RXØ1
CHK'D W.F.M.C.	3/6/75	TITLE: H771-A POWER CONNECTIONS
ENG. B. Hazen	3-10-75	
PROJ. ENG. [illegible]	3-10-75	
PROD. [illegible]	3/18/75	
NEXT HIGHER ASSY. B-DD-H771-Ø		SIZE D · CODE CS · NUMBER H771-A-1 · REV. B
SCALE NONE		
SHEET 1 OF 1		DIST.

DEC FORM NO. DD 150-0

NOTES:
1. SLOT BETWEEN P1-4 AND P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
3. ALL WIRES TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.



REVISIONS		
ONE	CHANGE NO.	REV.
—	H771-00001 ORIGINATED	*
20	H771-00002	A
30	H771-00003	B
33	H771-00004	C

DRAW.		7-31-75
CHK.	E. REMICK	8-5-75
ENGR.		
PROJ. ENGR.		
PROG.		
NEXT HIGHER ASSY.		
B-DD-H771-B		
SCALE		
SHEET	1 OF 1	

FIRST USED ON: RX01

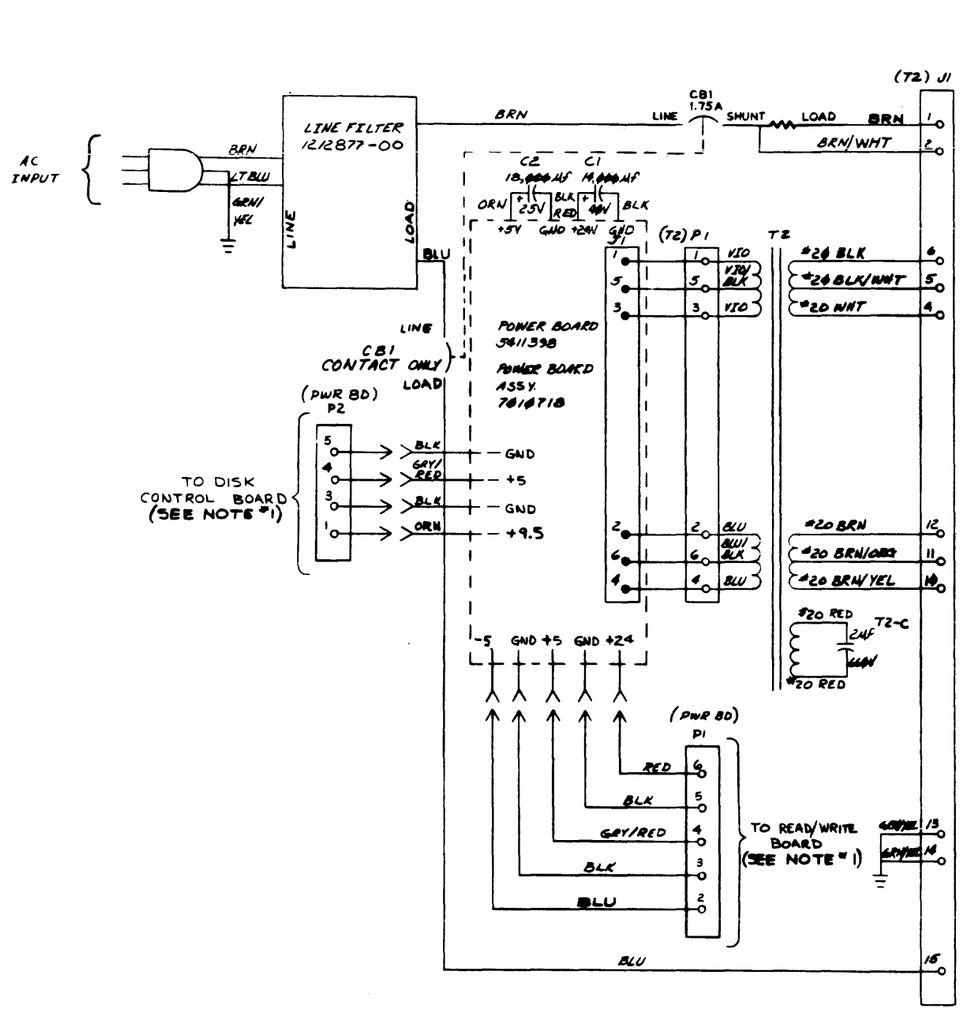
TITLE: H771-C POWER CONNECTIONS

SIZE	CODE	NUMBER	REV.
D	CS	H771-C-1	C

DIST.

CODE IDENT NO. CS — NUMBER H771-R-1

NOTES:
1. SLOT BETWEEN P1-4 AND P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
3. ALL WIRES TO BE #18AWG UNLESS OTHERWISE SPECIFIED.



REVISIONS			
ECO	CHANGE NO.	REV.	
—	H771-00001	*	ORIGINATED
	H771-00002	A	
	H771-00003	B	
	H771-00004	C	

DRN.	7-30-75
CHK'D	8-5-75
ENG.	8-12-75
PROJ. ENGR.	
PROD.	
NEXT HIGHER ASSY.	B-DD-H771-0
SCALE	
SHEET	1 OF 1

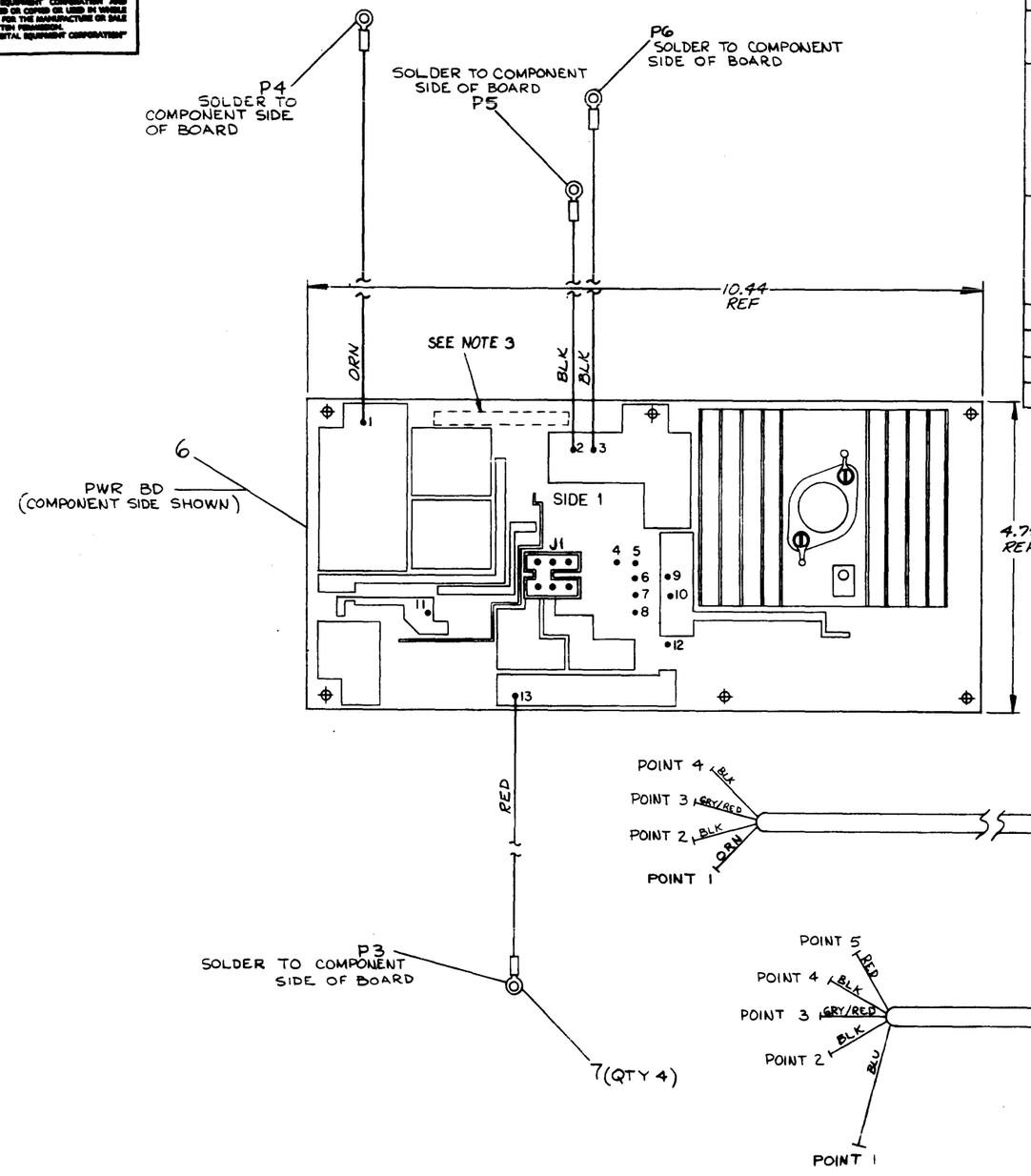
FIRST USED ON: RX01

TITLE: H771-D POWER CONNECTIONS

SIZE	CODE	NUMBER	REV.
D	CS	H771-D-1	C

DIST.

D CS H771-B-1 C



WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONN	FROM TERM	TO CONN	TO TERM	LENGTH
1	18	BLU	P1 POINT 1	—	PWR BD #11	SOLDER	—
	↓	BLK	P1 POINT 2	—	PWR BD #6	↓	—
		GRY/RED	P1 POINT 3	—	PWR BD #9		—
		BLK	P1 POINT 4	—	PWR BD #5		—
		RED	P1 POINT 5	—	PWR BD #12		—
2		ORN	P2 POINT 1	—	PWR BD #4		—
		BLK	P2 POINT 2	—	PWR BD #7		—
		GRY/RED	P2 POINT 3	—	PWR BD #10		—
	↓	BLK	P2 POINT 4	—	PWR BD #8		—
3	14	RED	P3	ITEM 7	PWR BD #13		13 IN ±.25
4	14	BLK	P5	ITEM 7	PWR BD #2		7 IN ±.25
5	14	ORN	P4	ITEM 7	PWR BD #1	↓	11 IN ±.25
4	14	BLK	P6	ITEM 7	PWR BD #3	SOLDER	9 IN ±.25

NOTES:

1. STRIP LENGTH FOR ITEMS 3, 4 & 5 ARE TO BE .16 LONG.
2. THE BLACK WIRES ON P1 & P2 CAN BE INTERCHANGED BETWEEN POINTS 5, 6, 7, & 8 ON THE POWER BOARD.
3. INK STAMP ASS'Y NO. 7010718 IN FIGURES, 13 HIGH WHERE SHOWN.

REVISIONS	CHK	CHANGE NO.	REV
		RX01-00001	A
		H771-00001	B

4	CONN, SOLDERLESS	9007928-00	7
1	POWER SUPPLY BOARD, RXØ1	D-ES-5411398-0-1	6
A/R	WIRE, #14 AWG, IPVC, ORANGE	9107370-33	5
A/R	WIRE, #14 AWG, IPVC, BLACK	9107370-00	4
A/R	WIRE, #14 AWG, IPVC, RED	9107370-22	3
1	HARNESS, DISK CONTROL BOARD	D-IA-7010853-0-0	2
1	HARNESS, READ/WRITE BOARD	D-IA-7010854-0-0	1
	DESCRIPTION	DWG./PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'	BLOCK OF ACCURACY	NOMINAL DIMENSION RANGE INCHES					
SURFACE QUALITY IN (CHECK ONE)		OVER 0 TO 6.3	OVER 6.3 TO 1.2	OVER 1.2 TO 4.8	OVER 4.8 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
MICROINCHES	MEDIUM ☐	±.005	±.008	±.012	±.020	±.024	±.04
	MACHINED ☐	±.012	±.016	±.025	±.04	±.063	±0.1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL SEE PARTS LIST

FINISH —

DWN	T. Phillips	12875
CHK'D	M. Cavanaugh	2/5/75
ENG.	[illegible]	3-18-75
PROJ. ENG.	[illegible]	3-18-75
PROD.	[illegible]	3/18/75
NEXT HIGHER ASSY.	E-UA-H771-Ø-Ø	
SCALE	1/1	
SHEET	1 OF 1	

FIRST USED ON H771

TITLE RXØ1 POWER BOARD ASS'Y

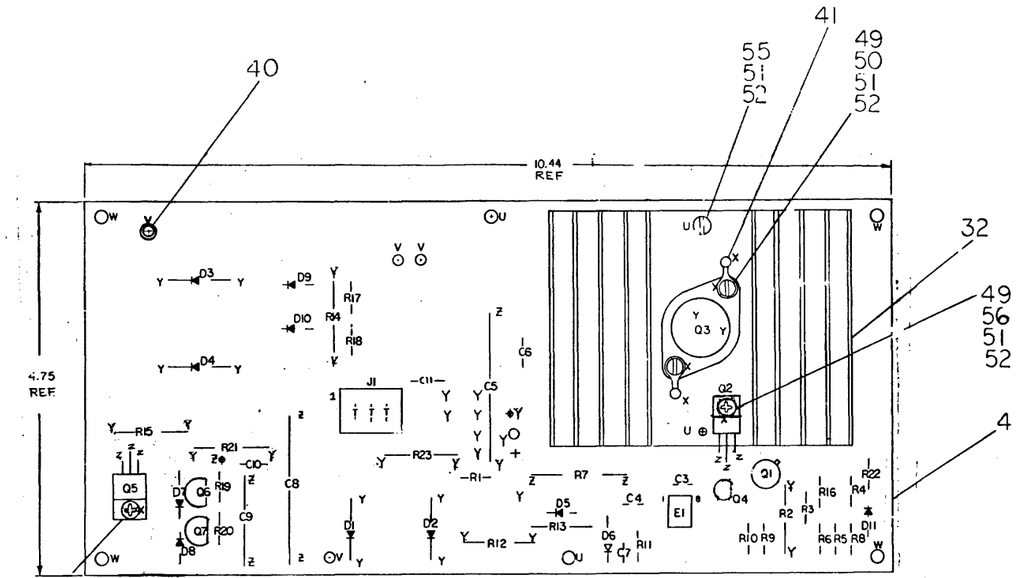
SIZE	CODE	NUMBER	REV.
D	AD	7010718-0-0	B

DIST.

DAD 7010718-0-0 B

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   A. ALL RESISTORS ARE 1/4W, 5%.
2. DOTTED AREAS COMPONENT NOT ON BOARD.
3. AT TIME OF MODULE ASSY, ITEM 49 SHOULD BE APPLIED BENEATH Q2, Q3 & Q5.
4. AT TIME OF ASSEMBLY, Q2, Q3 AND Q5 MOUNTING HARDWARE MUST BE TORQUED TO 4 TO 6 INCH POUNDS.
5. Q4, Q6 AND Q7 OUTLINES CORRESPOND TO GENERAL ELECTRIC TYPE TRANSISTORS.
6. FLAT RECTANGULAR WASHER SUPPLIED BY VENDOR TO BE MOUNTED UNDER Q2 AND Q5. SCREWHEAD.



QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-5411398-0-4	1
REF		SYMBOLLING HOLE LAYOUT	D-AH-5411398-0-5	2
REF		MODULE ECO HISTORY	B-MH-5411398-0-6	3
1		ETCHED CIRCUIT BOARD	5011397-00	4
3	C3, C4, C7	CAP .01 µf 100V 20% DISC	1001610-01	5
2	C5, C8	CAP 1000 µf 16V ELEC	1011849-02	6
3	C6, C10, C11	CAP .1 µf 100V 20% DISC.	1000090-00	7
1	C9	CAP 190 µf 12V 10% ELEC	1009433-00	8
2	D1, D2	DIODE AI88 (IN5624)	1110420-00	9
2	D3, D4	DIODE MR752	1110615-00	10
1	D5	DIODE IN4744 15V 10%	1105648-00	11
				12
2	D7, D6	DIODE 4M5.1Z1, 5.1V 1%	1105873-00	13
1	D8	DIODE D664	1100114-00	14
2	D9, D10	DIODE IN4004	1105796-00	15
1	D11	DIODE IN754A 6.8V 5%	1109991-00	16
1	E5,	RES 39 1/4W 5% CC	1302377-00	17
1	E6	RES 470 1/4W 5% CC	1300316-00	18
1	E7	RES .08 5W 3%	1311603-00	19
1	E8	RES 47 1/4W 5% CC	1300202-00	20
1	E9	RES 1M 1/4W 5% CC	1309595-00	21
1	E12	RES 270 2W 5% CC	1305380-00	22
1	E13	RES 511 3/4W 1%	1300324-00	23
1	E14	RES 10 2W 10% CC	1300172-00	24
1	E15	RES 180 1W 5% CC	1300262-00	25
1	E16	RES 10 1/4W 5% CC	1301317-00	26
				27
1	E18	RES 120 1/4W 5% CC	1300247-00	28
2	E19, E20	RES 1K 1/4W 5% CC	1300365-00	29
1	E22	RES 220 1/4W 5%	1300271-00	30
1	E21	RES 120 1W 5%	1301838-00	31
1		HEAT SINK	1212201-00	32
1	Q1	TRANS DEC 2219-2	1501883-00	33
1	Q2	TRANS D44C3	1510171-01	34
1	Q3	TRANS DEC 3715	1503068-00	35
2	Q4, Q6	TRANS 1MXAA05	1510705-00	36
1	Q5	TRANS D45N3	1510708-01	37
1	Q7	TRANS MXAA55	1510706-00	38
1	E1	I.C. DEC 301AN	1910282-00	39
4		EYELET	9007836-00	40
2		TERMINAL LUG, SOLDER	9009676-00	41
1	J1	CONNECTOR 6 PIN	1211342-06	42
				43
1	R4	RES 560 1/4W 5% CC	1301890-00	44
1	R23	RES 75 1W 5% CC	1305281-00	45
3	R1, R10, R11	RES 10K 1/4W 5% CC	1300479-00	46
1	R2	RES 390 2W 5% CC	1301869-00	47
1	R3	RES 620 1/4W 5% CC	1303178-00	48
A/R		THERMAL COMPOUND	9008258-00	49
2		SCREW 4-40 X 1/2	9006013-04	50
5		KEPNUT 4-40	9006557-00	51
5		WASHER FLAT 4-40	9006655-00	52
				53
1		SCREW 4-40 X 5/16 (PHILLIPS HD)	9006011-1	54
1		SCREW 4-40 X 7/16	9006012-04	55
1		SCREW 4-40 X 1/2 (PHILLIPS HD)	9006013-1.	56
1		RES. 2K 1/4W 5%	1301969-00	57

PARTS LIST

FIRST USED ON OPTION MODEL: RXO1

ETCH BOARD REV. D

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

301A	4	7
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV	CHANGE NO.	CHK	DATE	REVISIONS
B	5411398-00001	W. HAZEN	4-3-75	
C	5411398-00001	D. VEINOTT	7-18-75	
D	5411398-ML0003	C. YOUSE	16-24-75	
E	5411398-ML0004	D. CALDERAN	21 MAR 75	

DRN: Ron Metzger 11/27/74
CHK'D: [signature] 1/9/75
ENG: [signature] 1/9/75
PROJ. ENG: [signature] 1/9/75
MGR: [signature] 1-24-75
NEXT HIGHER ASSY
SCALE
SHEET 1 OF 2

digital

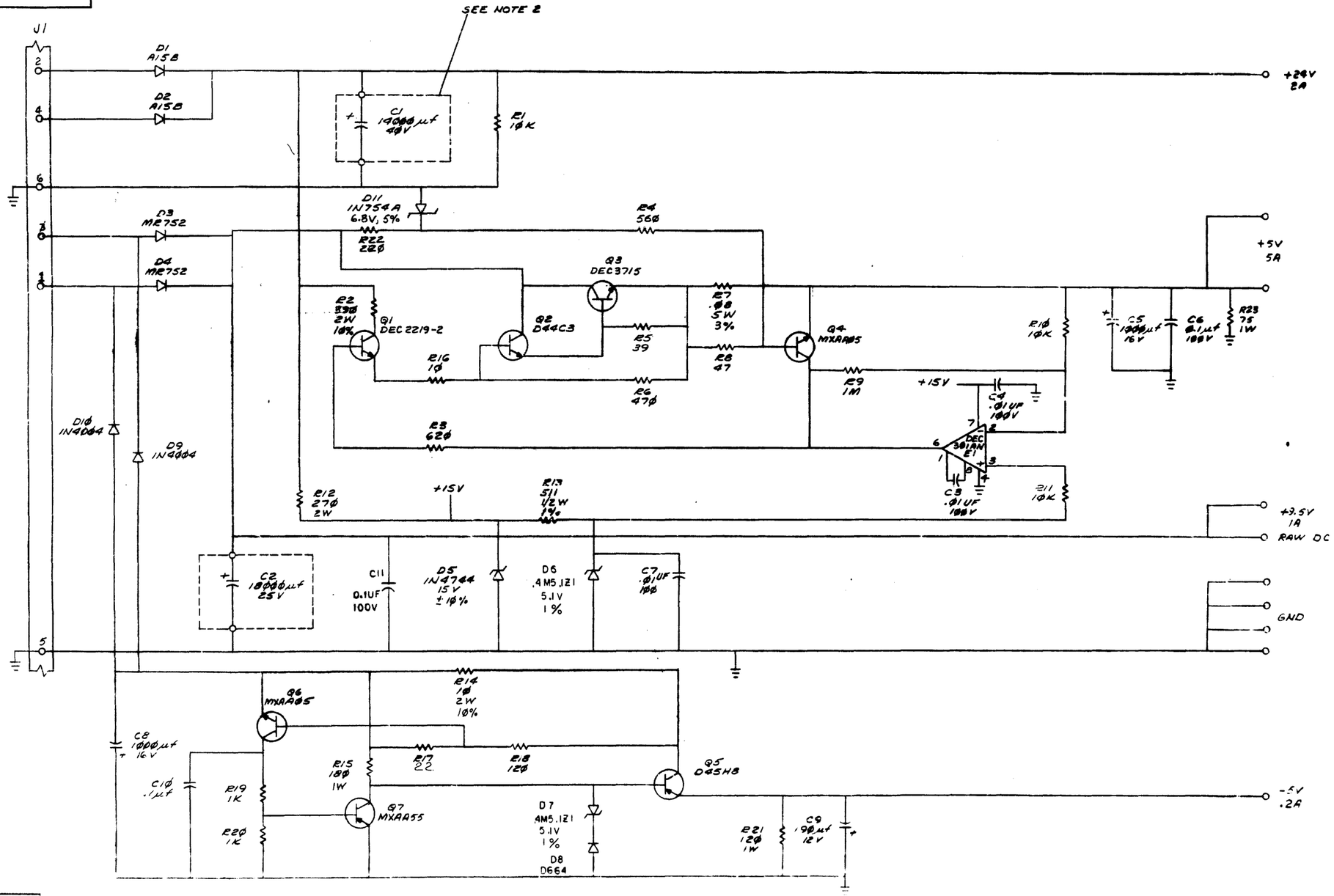
TITLE: RXO1 POWER SUPPLY

SIZE	CODE	NUMBER	REV.
D	CS	5411398-0-1	E

DIST.

5411398-0-1 REV. E

DEC FORM NO. DRD 139.8



REVISIONS		
CNR	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
RX01 POWER SUPPLY	D	CS	5411398-0-1	F
SCALE	SHEET 2 OF 2		DIST.	

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

SEQUENCE SEQUENCE

FOR FIELD MAINTENANCE PRINT SET
REFER TO MP 00284

THIS IS PRINT SET

UNIT VARIATIONS		PRINT SET
VAR	TITLE	
7013503-Ø	COOLING UNIT FOR DUAL RXØ1 115V	
7013503-1	COOLING UNIT FOR DUAL RXØ1 230V	
7013503-2	COOLING UNIT FOR SINGLE RXØ1 115V	
7013503-3	COOLING UNIT FOR SINGLE RXØ1 230V	
7013503-4	7013503-0 W/O PACKAGING	
7013503-5	7013503-1 W/O PACKAGING	
7013503-6	7013503-2 W/O PACKAGING	
7013503-7	7013503-3 W/O PACKAGING	

REVISIONS

REV	CHG. NO	DATE

USED ON OPTION/MODEL	
RXØ1	

SHEET 1 OF 2

DRN.		DATE 8-NOV-76
CHK'D.		DATE 11/23/76
PROJ ENG.		DATE 11/23/76
PROD.		DATE 11/23/76
FIELD SERV.		DATE 9 Nov 76

TITLE: RXØ1 PLENUM/FAN ASSY.

SIZE	CODE	NUMBER	REV
B	DD	7013503-0	

DIST

MR-0062-1A-16-R972-1325

DRB 106

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
	MP 00284	FIELD MAINTENANCE PRINT SET (MP)	-
	B-TC-7013503-0-1	FIELD MAINTENANCE PRINT SET (TC)	-
1	E-UA-7013503-0-0	PLENUM, FAN ASSY.	E/M
	D-IA-7013474-0-0	CABLE, PLENUM ADAPTOR	E/M
	C-IA-7417817-0-0	BRACKET, LEFT PLENUM MOUNTING	M
	C-IA-7417816-0-0	BRACKET, RIGHT PLENUM MOUNTING	M
	E-MD-7417815-0-0	PLENUM	M
	C-IC-7013503-0-2	PLENUM INTERCONNECTION DIAGRAM	E
	D-MD-7417958-0-0	INSERT, PLENUM	M
	A-SP-3700267-0-0	RXØ1 SUB-ASSY. PACKAGING KIT	M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

digital

TITLE		SIZE	CODE	NUMBER	REV
RXØ1 PLENUM/FAN ASSY.	SHEET 2 OF 2	B	DD	7013503-0	

EN-01062-2C 16-R376-(325)

DRB 108A

DRAWING DIRECTORY

FOR FIELD MAINTENANCE PRINT SET
REFER TO MP 00656

UNIT VARIATIONS

VAR	TITLE
7015622-Ø	COOLING UNIT FOR DUAL RXØ1 115V
7015622-1	COOLING UNIT FOR DUAL RXØ1 23ØV
7015622-2	COOLING UNIT FOR SINGLE RXØ1 115V
7015622-3	COOLING UNIT FOR SINGLE RXØ1 23ØV
7015622-4	7015622-0 W/O PACKAGING
7015622-5	7015622-1 W/O PACKAGING
7015622-6	7015622-2 W/O PACKAGING
7015622-7	7015622-3 W/O PACKAGING

REVISIONS
REV.
CHANGE NO.
CHK

USED ON OPTION/MODEL
RXØ1

DRN [illegible] DATE [illegible]
CHK'D E Kerrigan DATE 5 Jun 78
PROJ. ENG. H. Drab (DP) DATE 6-7-78
PROD. W Braun (DP) DATE 6-7-78

SHEET 1 OF 2

TITLE
RXØ1 PLENUM/FAN ASSY.

SIZE	CODE	NUMBER	REV
B	DD	7015622-0	

DIST.

DRB 106A

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
	MP 00656	FIELD MAINTENANCE PRINT SET (MP)	-
	B-TC-7015622-0-1	FIELD MAINTENANCE PRINT SET (TC)	-
1	E-UA-7015622-0	PLENUM, FAN ASSY	E/M
	D-IA-7013474-0-0	CABLE, PLENUM ADAPTOR	E/M
	E-MD-7420552-0-0	PLENUM	M
	C-IC-7013503-0-2	PLENUM INTERCONNECTOR DIAGRAM	E
	D-IA-7420846-0-0	INSERT, PLENUM	M
	A-SP-3700867-0-0	RXØ1 SUB-ASSY. PACKAGING KIT	M

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE

TYPE: E ELECTRICAL
M MECHANICAL
E/M ELECTRO/MECHANICAL

digital

TITLE	SHEET	SIZE	CODE	NUMBER	REV
RXØ1 PLENUM FAN ASSY.	2 OF 2	B	DD	7015622-0	

DRB 108A