348 MANUAL

TYPE 348 DISPLAY INTERFACE MANUAL

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SECTION I

INTRODUCTION

The Type 348 Display Interface allows operation of DEC Type 30A or 30E Displays from a PDP-6 computer. The Display Interface utilizes DEC System Modules contained in two standard mounting panels. In addition to the modules, the mounting panels contain the necessary connectors for the PDP-6 IO bus and a 50 pin Amphenol connector for the IO cable to the display.

The display interface accepts standard PDP-6 conditioning and data signals from the IO bus and converts these into signals acceptable by the Type 30 display. To the display, the interface looks like a PDP-1 Computer. Signals from the display are converted by the interface into signals that can be placed on the IO bus and used by the PDP-6 Computer. The interface includes provisions for operating a Light Pen if one is available on the display.

This manual is concerned only with the operation and maintenance of the display interface itself. Addition information about the PDP-6 Computer and the Type 30 Display can be obtained from the appropriate reference manuals.

SECTION II

INSTALLATION AND OPERATION

The Type 348 can be installed in the field as well as being factory installed during construction of a computer. Since the display interface consists of only two mounting panels, it is usually mounted in a bay containing other equipment. As a result, the physical location of the Type 348 will vary from system to system. If the required space is not available, an additional bay must be added to the system.

The 348 requires approximately one-half of the power supplied by a Type 728 power supply. If the required power is not already available, a 728 power supply must be added. If an additional supply is required, it should be connected to an existing power control to provide for local or remote application of power to the Type 348.

The two logic panels are mounted on the front (wiring side) of the selected cabinet. First remove the front doors and any interbay trim strips. Insert the mounting panels from the front side and secure them with screws through the mounting flanges into the riv-nuts provided in the vertical framework of the cabinet. The mounting panels can be installed with the modules in place. After securing the mounting panels, replace the trim strips and front doors. If an additional power supply is required, it is mounted on the inside of the plenum door at the back of the cabinet.

Power connection to the logic is made by means of the jumpers provided. In addition to the normal operating power, connection should be made to the marginal check power supply to provide for marginal checking of the display interface logic. The power wiring follows standard PDP-6 practice. Refer the PDP-6 Manual for details.

Connection to the PDP-6 IO Bus is made by plugging the four IO Bus cables into one of the two sets of connectors in the upper mounting panel. If the display interface is the last item on the bus, a terminator module must be placed in the second # connector. If the display interface is not to be the last item on the bus, the four IO cables to the next device are placed in the second set of IO Bus connectors.

The IO cable from the display is brought through the cable access hole in the bottom of the cabinet and plugged into the Amphenol connector mounted on the lower logic panel.

This completes the installation of the Display Interface, and it is ready for operation.

No action other than application of power is required to prepare the Type 348 for operation. If the power control used is set up for remote operation, the display interface will come on when the computer itself is turned on. In addition, the -15 Volt signal required for remote power operation of the display is supplied to the display through the display IO cable.

SECTION IV

THEORY OF OPERATION

This section describes the logical operation of the display interface. Standard DEC System Modules are used throughout. Detailed information about individual modules can be obtained from the DEC System Module Catalogue and from the Circuit Description section of the PDP-6 Maintenance Manual. The display interface logic is shown in three Block Schematics. Reference to the appropriate Block Schematic is made in the detailed logic description below. The Block Schematics are contained in Appendix B of this manual. Refer to the PDP-6 Maintenance Manual for a description of the symbols and drawing conventions used. Appendix A of this manual contains a glossary of the abbreviations and mnemonics used in the Block Schematics and the logic descriptions below.

GENERAL OPERATION

Figure 1 is a simplified Block Diagram of the Type 348 Display Interface. The unit includes a connection to the PDP-6 IO Bus, a connection to the display IO cable and three groups of logic, the Data Buffer (DB), the Control Register (CR) and the Control Logic (CL).

The IO Bus supplies control pulses to the control logic which in turn controls the transfer of data from the IO Bus to the Data Buffer and the transfer of condition (status) information to and from the IO Bus and the Control Register.

The Data Buffer, under control of the Control Logic, supplies data to the display. This data consists of a 10 Bit X coordinate word and a 10 Bit Y coordinate word which are used by the display to position the spot to be displayed on the CRT screen.

The Control Register contains several flip-flops that can be sensed, cleared and in some cases set, by PDP-6 IO commands. The Control Register supplies various control and information levels to the Control Logic and to the IO Bus. Some of the CR flip-flops can be controlled by signals from the display, providing control and information levels that are directly related to internal operations of the display itself.

The Control Logic utilizes pulses from the IO Bus, levels from the Control Register and pulses from the display to generate control pulses required for proper operation of the entire display system.

The following sub-sections will treat the Data Buffer, the Control Register and the Control Logic in that order. The PDP-6 IO connections and the display IO cable connections will be covered as they occur in descriptions of the three basic portions of the interface logic.

DATA BUFFERS

The Data Buffers are shown on drawing No. D-348-0-4. Since the two buffers (X and Y) are essentially identical, only the X buffer will be described in detail. The only real difference between the two buffers are the origins and destinations of the information that passes through them. The X buffer accepts information from the low order 10 Bits of the right half of a PDP-6

word and passes it on to the horizontal (X coordinate) buffer of the Type 30 display. The Y buffer accepts information from the low order 10 Bits of the left half of a PDP-6 word and passes it on to the vertical (Y coordinate) buffer of the Type 30 display.

Note that since the display interface contains flip-flop buffers for the X and Y information, this information is essentially double buffered, and the display interface Data Buffers may contain coordinate information for the next point to be displayed while the display itself is in the process of displaying information contained in its own horizontal and vertical buffers.

The X Data Buffer is made up of two 4220 modules. Since only 10 stages are required, all eight flip-flops of one module (B 18) are used, and only two flip-flops on the other module (B 17) are used. All flip-flops on both modules are cleared to their zero state by a clear X signal generated in the control logic to be described below.

The desired display information is inserted into the X buffer by means of the built in capacitor diode gates. The conditioning level at the capacitor diode gates is supplied by connection to the PDP-6 IO Bus. The set X pulse supplied by the Control Logic strobes the capacitor diode gates and sets the desired X buffer flip-flop to the one state. The output of the X Data Buffer is supplied through buffering resistors to the display. In the display, the X Data Buffer levels are applied to capacitor diode level inputs for the horizontal buffer. Note that these level inputs must be applied to the CD gates for approximately three microseconds before the read-in pulse to ensure proper transfer into the display buffer.

The outputs of the X buffer stages X_1 and X_9 are taken from the ground side of the flip-flop (i.e. ground equals logic 1). The most significant stage (X_0) uses -3 Volts to represent a logic 1. This is required by the internal logic of the display itself and reference should be made to the Type 30 manual.

CONTROL REGISTER

The Control Register logic is shown on drawing D-348-0-3. This portion of the logic supplies most of the communication between the PDP-6 Computer and the display interface. CONO (Condition Out) commands from the PDP-6 can set most of the flip-flops in the Control Register in order to establish the operating conditions of the display interface. IOB Status (CONI or Conditions In) commands from the PDP-6 can sense the state of all flip-flops in the Control Register in order to determine the current status of the display interface.

There are fourteen flip-flops in the Control Register. All flip-flops are Type 4217 in modules in locations A3, A4, and A5, plus two flip-flops on module A2. These are shown in area B1 through B8 of the Control Register print. All of the Control Register flip-flops are cleared by the DPI CONO clear signal generated in the control logic.

For convenience, the flip-flops in the Control Register will be described in left to right order.

The DIS Busy (Display Busy) flop indicates the current status of the display itself. The flop is set by the LDP (Load Display Pulse) signal and is cleared by the PDP (Display Done Pulse) signal. In other words, this flip-flop is set to the one condition whenever the display is in the process of locating and intensifying a particular spot on the face of the CRT. Note that LDP is a signal, generated by the display interface, that initiates action in the display itself. DDP is a signal, generated by the display, that signals the end of the display action.

LP Status (Light Pen status) is a flip-flop that is set to the one condition by the LPF (Light Pen Flag) signal from the display. Reference to the Type 30 Display Manual will show that LPF is generated only when the Light Pen has seen a spot of light during the time the display is intensifying a particular point on the CRT. LP Status is cleared by the CLPS (Clear Light Pen Status) signal. The CLPS signal is generated by an IOB Status signal from the PDP-6 IO Bus. Once LP Status has been set, it will remain in this condition until it has been examined by the program. Such examination can come as the result of a priority interrupt (the LP priority interrupt circuit is enabled by the one state of LP Status), or by programmed examination of the status of the display interface. If the program does not examine the status of the display interface, the LP status flop will remain set until the next IOB CONO clear of IOB Reset.

Note that the DIS Busy and LP Status flip-flop cannot be set by a CONO command from the computer. The other twelve flip-flops in the Control Register can be set by means of built in capacitor diode gates. The qualifying levels for the gates come from the indicated bits on the IO Bus.

The next stage in the Control Register is the DPI Status (Display Interface Status) flip-flop. When this flip-flop is in the one state, it indicates that the display interface is free to accept another data word from the computer. This condition can be determined by either a CONI command from the computer or through the priority interrupt system. DPI Status is the one condition enables the DPI priority interrupt decoder. DPI status is set to a one by the LDP signal. LDP is the signal that places the contents of the Data Buffers into the Display Buffer. Since the contents of the Data Buffers have been passed on to the display, the Data Buffers are now free to be cleared and reloaded with new data. DPI Status on a one indicates this condition. DPI Status is set to a zero by DPI DATAO clear. This signal is generated by a DATAO (Data Out) signal from the PDP-6 Computer. DATAO Clear occurs just before data from the computer is loaded into the Data Buffers. From this time until the next LDP signal, the display interface cannot accept another data word without destroying the information that has been placed in the Data Buffers. This condition is indicated by DPI Status in the zero state.

The Y Only and X Only flip-flops control the application of clear and set pulses to the Data Buffers. If one of these flip-flops is set to the one state, it will inhibit changes in the other Data Buffer. For example, if Y Only is set, the X Buffer cannot be changed.

The three INT (Intensity) flip-flops control the intensity of the spot displayed on the CRT if the Type 30 Display includes a variable intensity modification. There are eight intensity levels available, corresponding to the eight possible states of the

three INT flip-flops. The three flip-flops are treated as a two bit signed binary number. Negative numbers are in two's complement form. The most negative number (100) will produce the least intensity. The largest positive number (011) results in greatest intensity. The outputs of the three INT flip-flops are used in the Control Logic to gate pulse amplifiers that produce pulses to set the intensity register in the display.

The three LP PIA (Light Pen Priority Interrupt Assignment) flip-flops are used to assign a priority interrupt channel to the light pen signal. Any one of seven channels, corresponding to the octal numbers 1 through 7, may be assigned. Since there is no channel zero available, octal zero removes the light pen from the priority interrupt system. The outputs of the LP PIA flip-flops are decoded by a Type 4151 module. In addition to the LP PIA inputs, the LP status flip-flop must be in the one state to generate an output from the 4151. The output will appear as a ground level on one of seven lines corresponding to the octal number contained in the three LP PIA flip-flops. The 4151 output is placed on the IO Bus and, under the proper conditions, will cause an interrupt in the PDP-6 computer. Refer to the PDP-6 Maintenance Manual for detailed information on operation of the Priority Interrupt System.

The three DPI PIA flip-flops are used in the same manner as the LP PIA flip-flops. Note, however, that the output from the 4151 decoder in this case depends upon the DPI Status flip-flop being in the one state.

Note that IOB bits 24 through 35 are used as conditioning levels for the input gates to the control register flip-flops. This allows the computer, under programmed control, to establish the desired conditions in the display interface. In addition, the condition of the Control Register flip-flops can be placed on the IO bus using IOB bits 22 through 35. In this way, the computer can determine the status of the display interface. This is accomplished through the Type 4657 gates shown in area C1 through C8 of the Control Register Print. Each gate is associated with the control register flip-flop directly above it on the print. When a gate receives the proper qualifying signal from its flip-flop, and an IOB Status command is received fro the PDP-6, the status of the flip-flop is transmitted to the PDP-6 through the IO Bus.

CONTROL LOGIC

The display interface Control Logic is shown on drawing D-348-0-2. This portion of the interface utilizes pulses and levels from the PDP-6 Computer, levels from the control register, and pulses from the display to generate signals that control the transfer of data and status information to and from the computer and the display.

Since the PDP-6 IO Bus is common to all input-output devices, each device must continually sample the bus and determine when it has been addressed by an IO command. This function is performed by the Type 4118 module located in area C2 of the Control Logic print. Bits 3 through 9 of the PDP-6 IO commands are used to select the desired IO device. Depending on the device

number assigned (in this case 134), the zero or one outputs from the selected bits are fed into the 4118. When all of the 4118 inputs are at ground potential, a negative level is generated which qualifies various input gates and allows IO signals to pass from the PDP-6 computer into the display interface.

Note: Refer to the PDP-6 Maintenance Manual for detailed information about the PDP-6 IO commands and their actions.

There are two signals from the IO Bus which do not require device selection gating. One of these is the -15 Volt signal which indicates that power has been turned on in the Type 166 Arithmetic Processor. This signal is fed directly to the display to provide for remote operation of the display power control. The second signal is the IOB Reset which is fed into the 4606 pulse amplifier (B5) shown in area B2 of the print.

The normal operating sequence for the display interface starts with a CONO command from the PDP-6. This is followed by one or more DATAO commands. IOB Status commands may follow (or be interspersed with) the DATAO commands. The interface Control Logic associated with each of these computer commands will be described in the same order.

The CONO command is used to establish operating conditions within the display interface. The instruction in the PDP-6 generates two pulses: IOB CONO clear, followed (after one microsecond) by IOB CONO set. These signals are shown coming from the IO Bus in area B1 of the Control Logic print.

IOB CONO Clear, gated by the device decoder, is applied to a Type 4606 pulse amplifier and produces the DPI CONO Clear signal. Note that IOB Reset is applied to the same pulse amplifier without gating and produces the same output signal. DPI CONO Clear clears all of the flip-flops in the Control Register to the zero state. In addition, it clears the MOVE flip-flop is shown in area D4 of the Control Logic print, and its action will be described later.

IOB CONO Set, after gating, is applied to another 4606 (part of module B5) and produces DPI Cono Set. This signal is used in the Control Register to deposit the current status of the IO Bus into the Control Register flip-flops. In this way the computer can establish operating conditions for the display interface.

The DATAO command from the computer also generates two pulses: IOB DATAO clear and IOB DATAO set. Both of these pulses are gated by the output from the device selector.

IOB DATAO clear produces DPI DATAO Clear which is applied through capacitor diode gates to two type 4606 pulse amplifiers. The qualifying levels for the CD gates are supplied by the Y Only and X Only flip-flops in the Control Register. The resulting Clear X and Clear Y signals clear out the corresponding data buffers. Note that either one or both of these clear signals may be generated, depending upon the states of the Y Only and X Only flip-flops in the Control Register.

At this point, the CONO command has cleared the entire system and set the desired control register flip-flops to establish operating conditions. The DATAO Clear command has cleared the data registers and the system is ready to start transferring information to the display interface.

IOB DATA Set, gated by the device selector, is applied to a 4606 pulse amplifier (B6) shown in area C2 of the Control Logic print.

The pulse amplifier output (DPI DATAO Set) is applied through capacitor diode gates to two 4606 pulse amplifiers. The qualifying levels for the CD gates are supplied by the Y Only and X Only flip-flops in the Control Register. The resulting Set X and Set Y signals are used to transfer information from the IO Bus into the Data Buffers. The outputs of the buffer flip-flops are applied to capacitor diode gates at the input to the buffer registers in the display. Approximately three microseconds are required between setting of the data buffer flip-flops and reading into the display buffers. This allows for sufficient change in charge on the CD gate capacitors to ensure proper transfer of information into the display buffers.

The three microsecond delay required by the display buffer input gates is generated by a Type 4301 delay module shown in area C5 of the control logic print (module No. B4). The delay is triggered by DPI DATAO Set. The outputs of the delay module are a negative level (Pin J) for the duration of the delay time and a negative pulse (Pin E) that occurs at the end of the delay time. The use of these signals will be described below.

The DPI DATAO Set signal is gated by inverters shown in areas B6 and C6 of the control logic print. These inverters are part of a Type 4105 module located in B10. The lower inverter amplifies and inverts the zero output from the Dis Busy flip-flop in the control register. When DIS Busy is a zero (in other words the display is not in the process of displaying a point), the upper inverter is qualified and the DPI DATAO set signal can pass through it into a 4604 pulse amplifier module. The 4604 (module B11 shown in area B7 of the print) is connected to provide a one microsecond negative pulse output. This is the CDP pulse which is fed through the display IO cable to the display where it generates signals to clear the display buffers.

The 4604 output is also applied to the base input of one of the inverters on module B10. The emitter of this inverter is connected to the level output of the 4301 delay module. Since the delay is in progress at this time, the inverter is cut off and the signal path is closed.

DPI DATAO Set also sets the MOVE flip-flop to the one state. This is accomplished through a 4102 inverter module (A1) shown in area C4 of the print. The use of the MOVE flip-flop signal will be desribed later.

When the three microsecond delay produced by the Type 4301 delay module is completed, the negative output pulse is applied to an inverter on module B10. With DIS Busy in the zero state, this inverter can conduct, and the pulse is amplified and inverted and applied to a Type 4606 pulse amplifier (module B9) shown in area C7. The output of the PA is the negative LDP signal. LDP is applied to the display through the display IO cable and to several points in the display interface control logic and control register.

In the display, LDP is used to generate signals that load the display buffers and initiate all further display actions. At the end of the display actions, the display sends the DDP signal back to the display interface. Refer to the Type 30 Display Manual for details.

LDP is applied to the gated inputs of three Type 4606 pulse amplifiers (module B8) shown in areas A5 and A6 of the control logic print. The PA's are gated by the three intensity flip-flops in the control register. The PA outputs are fed through the display IO cable to the display's intensity register.

LDP also clears the MOVE flip-flop in the control logic and sets both the DIS Busy and DPI Status flip-flops in the control register to the one state. DIS Busy indicates that the display is in the process of displaying a point, and DPI Status indicates that the display interface is free to accept data for the next point to be displayed.

The action described so far is typical of that produced by the first DATAO command from the computer. Further action will be determined by one of two possible situations: the display will complete its action before the display interface is loaded with additional data or the display interface will be loaded before the display completes its action.

First consider the case when the display is completed before the interface is reloaded. In this case the conditions at the end of the display will be as indicated at the end of the initial action described above.

The DDP signal generated at the end of the display action is applied to the pulse amplifier in the control logic which generates CDP (Type 4604 module B11 in area B7). The CDP signal is generated and the display buffers are cleared. In addition, CDP (treated as a one microsecond negative level rather than a negative pulse) passes through an inverter and becomes a one microsecond wide ground level. Note that the signal can now pass through this inverter since the Type 4301 delay module is in its quiescent state and Pin J will be at ground, placing the emitter input of the inverter at ground. The one microsecond wide ground level output of the inverter is applied to the pulse input of the capacitor diode gate on the pulse amplifier which generates LDP. (Type 4606 module B9 in area C7). The level input of the CD gate is supplied by the one output of the MOVE flip-flop. At this time, however, MOVE is in the zero state, the CD gate is not qualified, and no further action results. Since no data has been loaded into the display interface, no action is desired. Any further display signals from the PDP-6 will produce the initial action described above.

Now consider the case when the display interface buffers are loaded by a DATAO command while the display is still in the process of displaying a spot. Again conditions are as described at the end of the initial action. In particular, note that the DIS Busy flip-flop is set to the one state.

The DATAO Clear and Set commands result in the clearing and setting of the X and Y buffers, the setting of the MOVE flip-flop, and the initiation of the three microsecond delay, all as described above.

The DIS Busy (Display Busy) flop indicates the current status of the display itself. The flop is set by the LDP (Load Display Pulse) signal and is cleared by the DDP (Display Done Pulse) signal. In other words, this flip-flop is set to the one condition whenever the display is in the process of locating and intensifying a particular spot on the face of the CRT. Note that LDP is a particular spot on the face of the CRT. Note that LDP is a signal, generated by the display interface, that initiates action in the display itself. DDP is a signal, generated by the display, that signals the end of the display action.

LP Status (Light Pen status) is a flip-flop that is set to the one condition by the LPF (Light Pen Flag) signal from the display. Reference to the Type 30 Display Manual will show that LPF is generated only when the Light Pen has seen a spot of light during the time the display is intensifying a particular point on the CRT. LP Status is cleared by the CLPS (Clear Light Pen Status) signal. The CLPS signal is generated by an IOB Status signal from the PDP-6 IO Bus. Once LP Status has been set, it will remain in this condition until it has been examined by the program. Such examination can come as the result of a priority interrupt (the LP priority interrupt circuit is enabled by the one state of LP Status), or by programmed examination of the status of the display interface. If the program does not examine the status of the display interface, the LP status flop will remain set until the next IOB CONO clear of IOB Reset.

Note that the DIS Busy and LP Status flip-flops cannot be set by a CONO command from the computer. The other twelve flip-flops in the Control Register can be set by means of built in capacitor diode gates. The qualifying levels for the gates come from the indicated bits on the IO Bus.

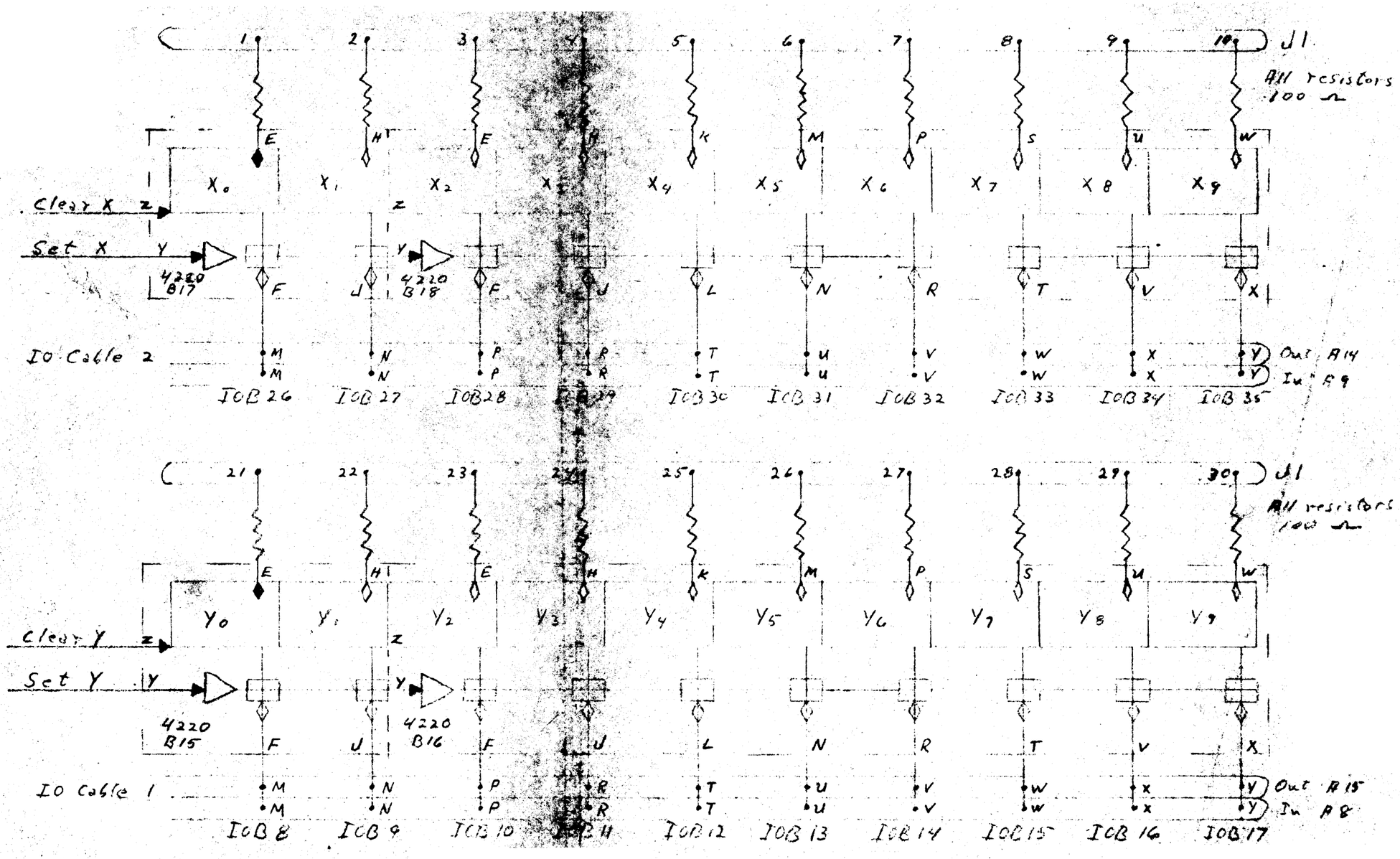
LDP produces the actions described above, and the display is again in the process of locating and intensifying a spot.

It is possible that DDP could occur less than three microseconds after DPI DATAO Set. In this case DDP will clear the DIS Busy flip-flop and the display buffers, but will not generate LDP. With DIS Busy in the zero state, the pulse at the end of the three microsecond delay will generate LDP and the display will again be placed in operation.

There is one more PDP-6 instruction which affects the display interface. This is the IOB Status or CONI instruction. The associated logic is shown in area A1 through A4 of the control logic print.

The IOB Status signal is a negative level approximately 2.5 microseconds wide. It is applied, along with the device selector gating level, to a Type 4113 inverting And gate (module B13). The gated output is amplified and inverted by two inverters on a Type 4102R module (b14) and becomes IOB DPI(A) and IOB DPI(B). These signals are applied to the Type 4657 in the control register and place the status of the control register flip-flops on the IO bus for the duration of the IOB Status signal.

In addition, IOB DPI(A) is applied to the positive pulse input of a 4606 pulse amplifier (Module B9). The pulse amplifier will respond to the positive going trailing edge of the input signal and produce a negative pulse signal (CLPS) that clears the light pen status flip-flop in the control register.



Display Interface Type 34B
Data Buffers

12/13/66
RJB

A 11 A12
In Out

IOB ← Status

IOB ← DPI(A)

IOB ← DPI(B)

4102 R B14

4118 B13

IOB Reset

4606 B5

J DPI CONO Clear

D D IOB CONO Clear

P DPI CONO Set

E E IOB CONO Set

DPI DATAO Clear

D D IOB DATAO Clear

DPI DATAO Set

C C IOB DATAO Set

IO Cable 4

A 10 A13
In Out

4118 B12

1 3 4
001 011 1

IOB Reset

-15 V to J1 Pin 48

IO Cable 3

Note: Clamped load must be removed

P Clear L P Status (CLPS)

4606 A9

4606 B7

Clear X

Clear Y

Y only

X only

4606 B8

To J1
Pin 41
Pin 42
Pin 43

LDP k

Int1'

Int2'

Int3'

4606 B6

Set X

Set Y

Y only

X only

DDP

4604 B11 1 µs

CDP

To J1
Pin 34

4103 A1

LDP w

Mask

DPI CONO Clear

4210 A2

H301 B4 3 msec

Dis Busy

4104 B10

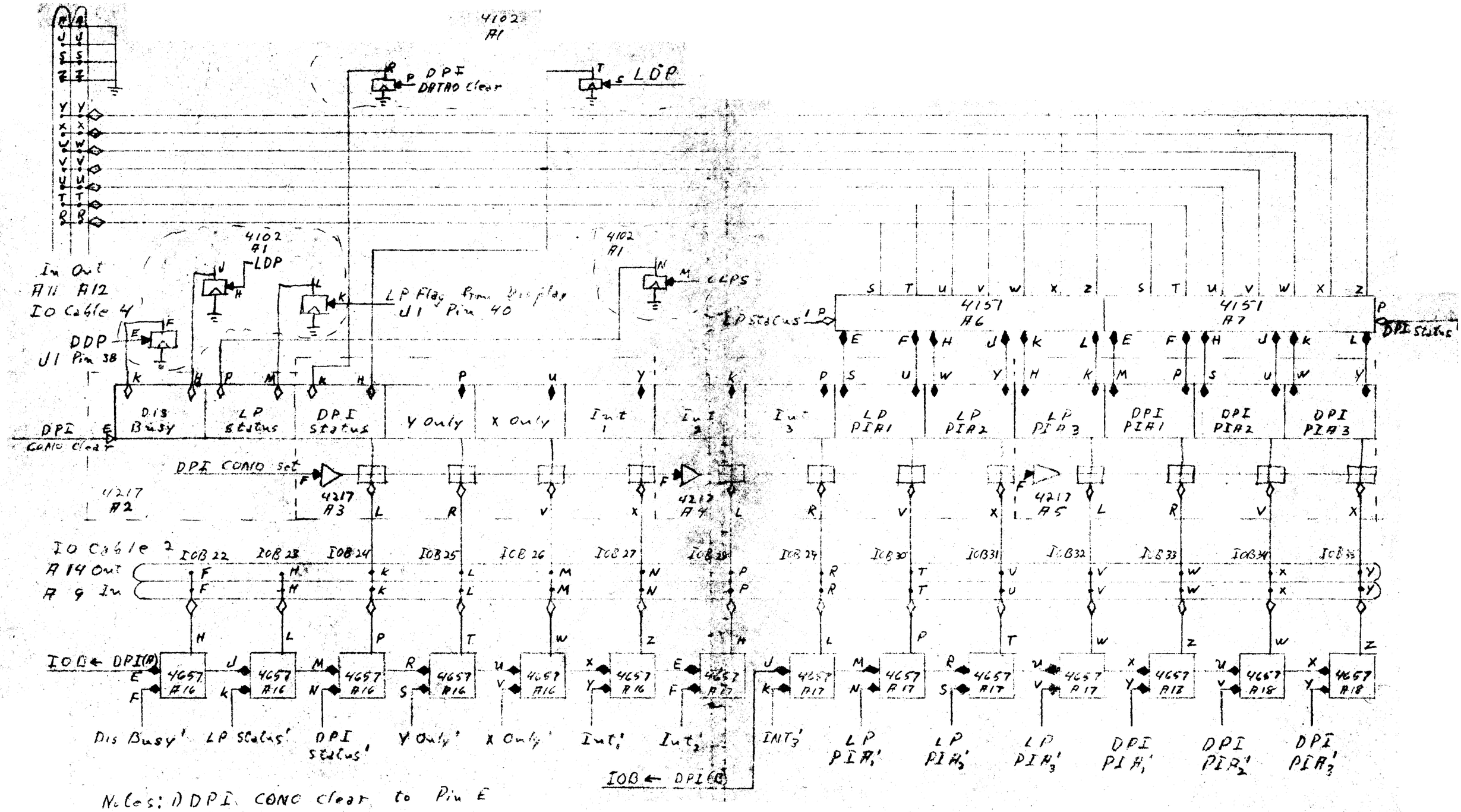
4606 B9

H LDP

To J1
Pin 36

Display Interface Type 34E
Control Logic

12/13/66
A1B



Notes: 1) DPI CONO clear to Pin E of all 4217's

2) Ground all complement inputs to 4217's

3) Ground Pins A, J, S, and Z on all IO Bus connectors

Display Interface Type 34B
Control Register
12/12/69
RJB

PDP6

Display Interface

Display

CONO

Power on (-15V) I/O c #3

Device Selection (7 bits) I/O cable #3

Display PI assign (33, 34, 35) I/O c #2

LP PI assign (30, 31, 32) I/O c #2

Intensity (27, 28, 29) I/O c #2

Transfer X only (26) I/O c #2

Transfer Y only (25) I/O c #2

CONO clear I/O c #4

CONO Set I/O c #4

CONI

Display busy (24) I/O c #2

LP signal (23) I/O c #2

IOB ← status I/O c #4

P.I.

Display done P.I. I/O c #4

LP signal P.I. I/O c #4

DATAO

" X coordinate (2 chrs 35) I/O c #2

Y coordinate (5 chrs 17) I/O c #1

DATAO clear I/O c #4

DATAO Set I/O c #4

Power on (-15V) 48

X Coordinate (10 levels) 1 - 10

Y Coordinate (10 levels) 21 - 30

Intensity (3 pulses) 41 - 43

Clear Display Pulse 34

Load Display Pulse 36

Display Done Pulse 38

LP Flag 40

LP status (saw a scope) 45

10 MC 47

Note: All signals carried by I/O cable between Display Interface and Display. No's indicate Connector pins used.