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Introduction

This publication contains additions and revisions to the information contained in the 1987 Semiconductor Databook Volume 1.

In order to properly reference the information in this publication, it is recommended that the following pages in the 1987 Semiconductor Databook Volume 1 be marked to note that changes exist.

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Part Identification Codes

The following identification codes are used with the devices in this databook.

780 Series

78xyz - xx

0 = Processors
1 = Coprocessor
2 = Memories
3 = I/O devices
4 = Reserved

5 = Controllers
6 = Graphic devices
7 = Bus interfaces
8 = Communications devices
9 = Reserved

- xx
GA = Gullwing
FA = Straight
PA = Pin grid array

DC Series

DCxyz

0 = Custom bipolar devices
1 = Custom bipolar devices

3 = MOS devices
5 = MOS devices

Cross-referencing of Semiconductor Products

Part Name	Part Number	Purchase Number	Description
DC003	DC003	19-12730-00	Dual-interrupt Circuit
DC004	DC004	19-12729-00	Register Selector (Protocol) Logic
DC005	DC005	19-13040-00	4-bit Transceiver
DC006	DC006	19-14035-00	Word Count/Bus Address Logic
DC010	DC010	19-14038-00	Direct Memory Access
DC013	DC013	19-14438-00	UNIBUS Request Logic
DC018	—	19-17043-00/1	Serializer/Deserializer
DC021	DC021	19-19015-00	Octal Bus Transceiver
DC022	—	19-17871-00	16-Word by 4-bit Register File
DC024	—	19-20116-01	Encoder/Decoder Logic
DC028	78701	19-22110-01	VAXBI Clock Driver
DC029	78702	19-22111-01	VAXBI Clock Receiver
DC102	—	19-13888-00	Equals Checker
DC301	—	21-12623-00	Dual Baud Rate Generator
DC309	—	21-15102-00	Reed Solomon Generator
DC310	DCT11	21-17311-01	DCT11 16-bit Microprocessor
DC319	DC319	21-17312-00	DLART
DC321	FPJ11	21-21858-00	FPJ11 Floating-point Accelerator
DC502	78680-GA	21-25011-01	Video Processor (VIPER)
DC323	78690-GA	21-21553-01	Video Control (ADDER)
DC324	78732-PA	21-21689-00	VAXBI BIIC
DC327	—	21-20852-AA	V-11 ROM/RAM
DC328	—	21-20851-AA	V-11 Instruction/Execution Logic
DC329	—	21-20850-AA	V-11 Memory Management Logic
DC330	—	21-20849-AA	V-11 Floating-point Accelerator Logic
DC333	78032-GA	21-20887-01, -04, -05, -06	MicroVAX 32-bit CPU
—	DCJ11-AC	57-19400-08	DCJ11 16-bit Microprocessor (15 MHz)
—	DCJ11-AA	57-19400-09	DCJ11 16-bit Microprocessor (18 MHz)

Part Name	Part Number	Purchase Number	Description
DC335	DCJ11	21-17679-00	DCJ11 16-bit Microprocessor
DC337	78132-GA	21-22797-01	MicroVAX Floating-point Unit
DC343	78743-PA	21-23838-01	VAXBI BCAI
DC344	78733-PA	21-23839-01	VAXBI BCI3
DC349	78808-GA	21-23458-01	Octal ART
DC5003	78584-GA	21-23864-01	Dynamic RAM Controller (DYRC)
DC358	78532-GA	21-24329-01	MicroVAX Direct Memory Access (DMA)
DC503	78610-GA	21-24941-01	Programmable Sprite Cursor
DC506	78516-GA	21-24330-01	MicroVAX Vectored Interrupt Controller (VIC)
ADVICE	ADVICE	—	MicroVAX Incircuit Evaluation/Emulation Unit

Recommended Operating Conditions

- Supply voltage (V_{DD}): 4.75 V to 5.25 V
- Active supply current: (I_{DD}): 700 mA (maximum)
- Temperature (T_A): 0°C to 70°C
- Relative humidity: 10% to 95% (noncondensing)
- Minimum airflow over chip: 250 linear feet/minute

Part Number Variations

Four variations of the MicroVAX 78032 are available. All variations operate at a maximum clock (CLKI) rate of 40 MHz. The Digital part numbers assigned to these are

Part Number	Package Leads
21-20887-01	formed
21-20887-04	unformed
21-20887-05	formed
21-20887-06	unformed

The functional restrictions of the 21-20887-01, and -04 versions are

—DMA requests that coincide with memory management activity or floating-point completion polling, may cause the MicroVAX CPU to missequence. To prevent this, the assertion of $\overline{\text{DMR}}$ signal should be synchronized with the deassertion of the $\overline{\text{AS}}$ signal to the chip.

—Interrupt requests that are asserted and then deasserted before being serviced (passive release) by the MicroVAX CPU, may cause the CPU to missequence. To prevent this, the $\overline{\text{IRQ}<3:0>}$ line should remain asserted until the chip acknowledges the request with the interrupt acknowledge cycle.

Clock Input Timing

Figure 38 shows the timing specifications for the CLKI input clock signal and Table 18 lists the timing parameters indicated on the diagram.

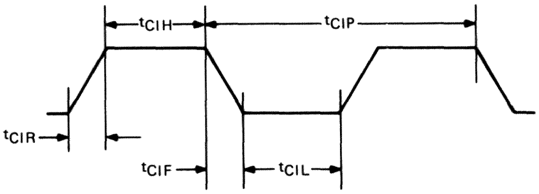


Figure 38 • MicroVAX 78032 CLK1 Timing Waveform

Table 18 • MicroVAX 78032 CLKI Timing Parameters

Timing Symbol	Signal Definition	Requirements (ns) Min.	Max.
t_{CIF}	Clock in fall time	—	4.5
t_{CIH}	Clock in high	8	—
t_{CIL}	Clock in low	8	—
t_{CIP}	Clock period	25	50
t_{CIR}	Clock in rise time	—	4.5

CPU Read and Write Cycle Timing

Figure 39 shows the timing sequence for the CPU read cycle and Figure 40 shows the timing sequence for the CPU write cycle. The parameters for the CPU read and write cycles are listed in Table 19.

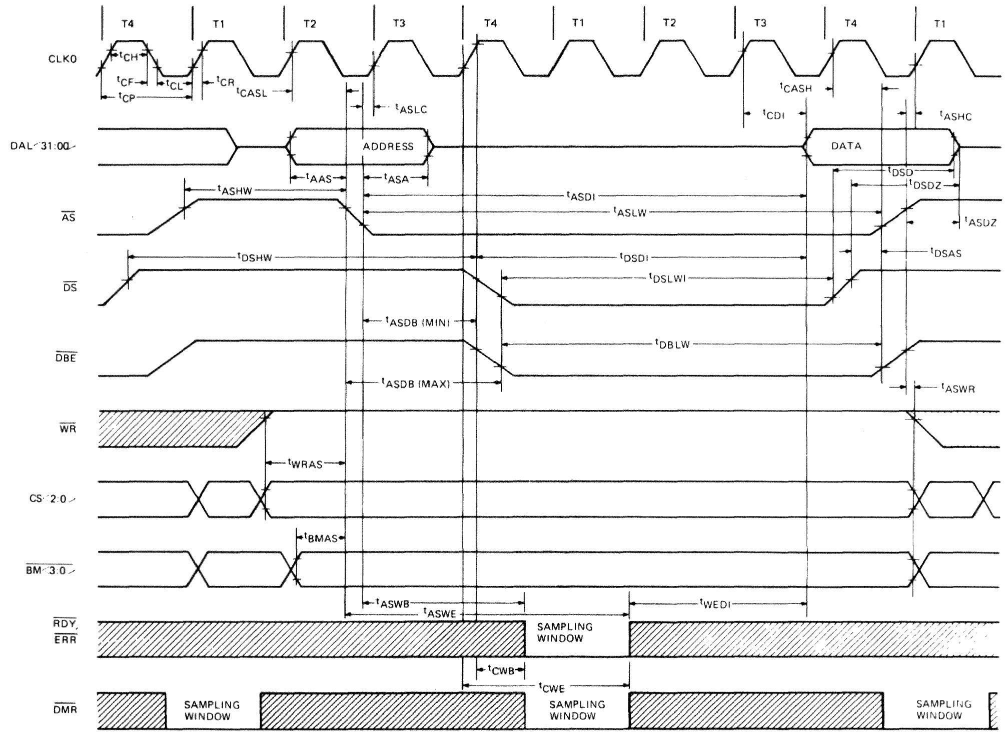


Figure 39 • MicroVAX 78032 CPU Read Cycle Timing Sequence

Table 19 • MicroVAX 78032 CPU Read and Write Cycle Parameters

Timing Symbol	Signal Definition	Requirements (ns) Min.	Max.
t_{AAS}	Address set up time to $\overline{\text{AS}}$ assertion	2P–28	—
t_{ASA}	Address hold time after $\overline{\text{AS}}$ assertion	2P–15	—
t_{ASHC}	$\overline{\text{AS}}$ rising through 2.0 V to CLKO rising through 0.8 V	P–23	—
t_{ASLC}	$\overline{\text{AS}}$ falling through 0.8 V to CLKO rising through 0.8 V	P–20	—
t_{ASDB}	$\overline{\text{AS}}$ assertion to $\overline{\text{DBE}}$ and $\overline{\text{DS}}$ (read) assertion	3P–15	3P+20
t_{ASDI}	$\overline{\text{AS}}$ assertion to read data valid[1]	—	11P–30+8PS
t_{ASDSO}	$\overline{\text{AS}}$ assertion to $\overline{\text{DS}}$ assertion (write)	5P–15	5P+20
t_{ASDZ}	$\overline{\text{AS}}$ and $\overline{\text{DBE}}$ deassertion to data three-state	—	2P–20
t_{ASHW}	$\overline{\text{AS}}$ deassertion width	3P	—
t_{ASLW}	$\overline{\text{AS}}$ assertion width	12P–15+8PS	
t_{ASWB}	$\overline{\text{AS}}$ assertion to beginning of $\overline{\text{RDY}}$, $\overline{\text{ERR}}$, and $\overline{\text{DMR}}$ sampling window[2]	—	(6P–45)+8PS
t_{ASWE}	$\overline{\text{AS}}$ assertion to end of $\overline{\text{RDY}}$, $\overline{\text{ERR}}$, and $\overline{\text{DMR}}$ sampling window[3]	6P+10+8PS	—
t_{ASWR}	$\overline{\text{WR}}$, $\overline{\text{BM<3:0>}}$, CS<2:0> hold time from $\overline{\text{AS}}$ deassertion	P–20	—
t_{BMAS}	$\overline{\text{BM<3:0>}}$ set up time before $\overline{\text{AS}}$ assertion	2P–25	—
t_{CASH}	CLKO rising through 2.0 V to $\overline{\text{AS}}$ rising through 0.8 V	P–7	P+15
t_{CASL}	CLKO rising through 2.0 V to $\overline{\text{AS}}$ falling through 2.0 V	P–9	P+16
t_{CDI}	CLKO rising through 2.0 V to read data valid	—	P–5
t_{CDO}	Write data hold time from CLKO rising through 2.0 V	P–15	—
t_{CF}	CLKO fall time	—	12.5
t_{CH}	CLKO high	(2P–25) x .5	—
t_{CL}	CLKO low	(2P–25) x .5	—
t_{CP}	CLKO period	50	100
t_{CR}	CLKO rise time	—	12.5[4]
t_{CWB}	T4 CLKO rising through 2.0 V to beginning of $\overline{\text{RDY}}$, $\overline{\text{ERR}}$, and $\overline{\text{DMR}}$ sampling window[2]	—	3P–45
t_{CWE}	T4 CLKO rising through 0.8 V to end of $\overline{\text{RDY}}$, $\overline{\text{ERR}}$, and $\overline{\text{DMR}}$ sampling window[3]	3P+15	—

Table 19 • MicroVAX 78032 CPU Read and Write Cycle Parameters (Cont.)

Timing Symbol	Signal Definition	Requirements (ns) Min.	Max.
t_{DBLW}	$\overline{DBE}$ assertion width	9P–20+8PS	—
t_{DOC}	Write data set-up time to CLKO rising through 0.8 V	3P–42	—
t_{DODS}	Write data set-up time to $\overline{DS}$ assertion	3P–30	—
t_{DSAS}	$\overline{DS}$ deassertion to $\overline{AS}$ and $\overline{DBE}$ deassertion	P–15	—
t_{DSD}	Read data hold time after $\overline{DS}$ deassertion	0	—
t_{DSDI}	$\overline{DS}$ assertion to read data valid[1]	—	8P–35+8PS
t_{DSDO}	Write data hold time from $\overline{DS}$ deassertion	3P–20	—
t_{DSDZ}	$\overline{DS}$ deassertion to read data high impedence	—	3P–20
t_{DSHW}	$\overline{DS}$ deassertion width	6P	—
t_{DSLWI}	$\overline{DS}$ assertion width (read)	8P–20+8PS	—
t_{DSLWO}	$\overline{DS}$ assertion width (write)	6P–20+8PS	—
t_{WEDI}	Sampling window end to read data valid	—	5P–25
t_{WRAS}	$\overline{WR}$, CS<2:0> set up time before $\overline{AS}$ assertion	3P–35	—

Notes:

[1] Read data is valid early enough if t_{ASDI} or t_{DSDI} or t_{CDI} is satisfied.

[2] Requirements for the beginning of the sampling window are satisfied if either t_{ASWB} or t_{CWB} is satisfied.

[3] Requirements for the end of the sampling window are satisfied if either t_{ASWE} or t_{CWE} is satisfied.

[4] t_{CH}, t_{CL}, and t_{CP} parameters are minimum for this value.

Table 20 • MicroVAX 78032 DMA Cycle Timing Parameters

Timing Symbol	Signal Definition	Requirements (ns)	
		Min.	Max.
t_{ASG}	$\overline{\text{AS}}$ and $\overline{\text{DBE}}$ deassertion to $\overline{\text{DMG}}$ assertion	4P–25	—
t_{CGH}	CLKO rising through 2.0 V to $\overline{\text{DMG}}$ rising through 0.8 V	P–7	P+16
t_{CGL}	CLKO rising through 2.0 V to $\overline{\text{DMG}}$ falling through 2.0v	P–7	P+18
t_{DMRG}	$\overline{\text{DMR}}$ to $\overline{\text{DMG}}$ latency	10P–25	60P+20+16PS
t_{DMRGU}	$\overline{\text{DMR}}$ to $\overline{\text{DMG}}$ latency with bus unlocked	10P–25	28P+20+8PS
t_{DMRH}[3]	$\overline{\text{DMR}}$ hold with respect to $\overline{\text{DMG}}$ assertion	0	—
t_{GDALZ}	$\overline{\text{DMG}}$ deassertion to external device three-state of DALS.	—	4P–20
t_{GDMR}	$\overline{\text{DMG}}$ assertion to $\overline{\text{DMR}}$ deassertion such that no more DMA cycles are requested	—	6P–45+ ((N–2) × 8P)[1]
t_{GHC}	$\overline{\text{DMG}}$ rising through 2.0 V to CLKO rising through 0.8 V	P–25	—
t_{GLC}	$\overline{\text{DMG}}$ falling through 0.8 V to CLKO rising through 0.8 V	P–23	—
t_{GLW}	$\overline{\text{DMG}}$ minimum assertion width	10P–25+ ((N–2) × 8P)[1]	—
t_{GSZ}	$\overline{\text{DMG}}$ assertion to three-state of $\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{DBE}}$, $\overline{\text{WR}}$. CS<2:0> and $\overline{\text{BM}\ <3:0>}$	-10	0
t_{GZ}	$\overline{\text{DMG}}$ deassertion to external device of three-state of $\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{DBE}}$, $\overline{\text{WR}}$, CS<2:0> <3:0> and $\overline{\text{BM}\ <3:0>}$	—	3P–20[2]

Notes:

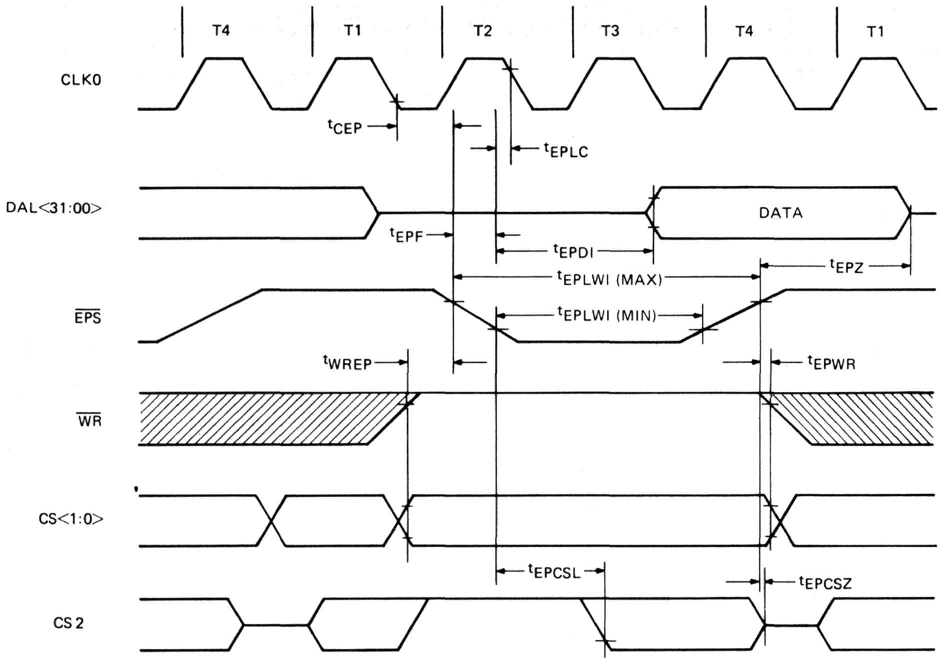
[1] The number of microcycles that occur during a DMA grant. A DMA grant is issued for a minimum of two microcycles.

[2] At the conclusion of a $\overline{\text{DMA}}$ grant the external logic must deassert the $\overline{\text{AS}}$, $\overline{\text{DS}}$, and $\overline{\text{DBE}}$ signals before the external bus drivers become a high impedance.

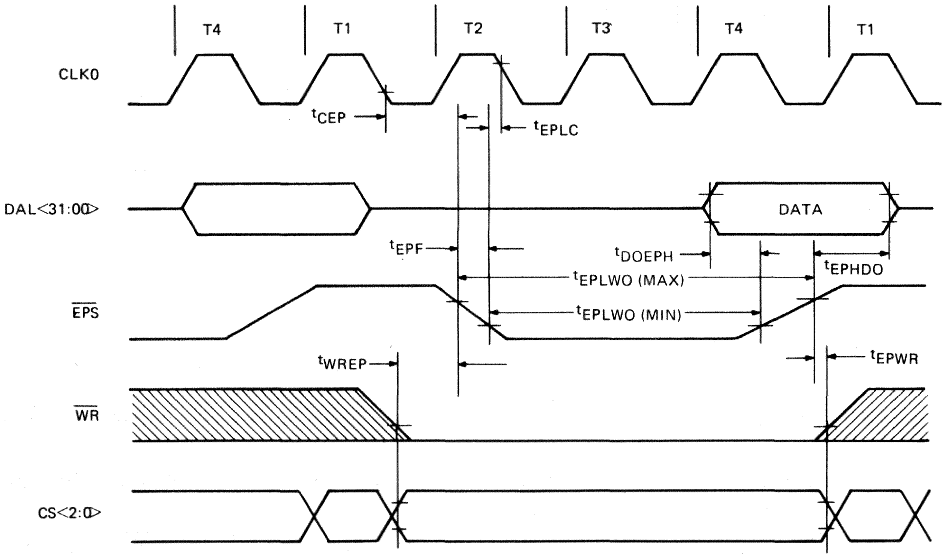
[3] If t_{DMRH} parameter is not met ($\overline{\text{DMR}}$ is deasserted before $\overline{\text{DMG}}$ is asserted), then $\overline{\text{DMR}}$ must not be reasserted for 2.5 microcycles (500 ns at maximum frequency).

External Processor Cycle Timing

Figure 42 shows the timing sequence for the external processor read and response timing and for the external processor write command timing. Table 21 lists the timing parameters for the symbols referenced on the diagrams.



External Processor Read/Response Timing



External Processor Write/Command Timing

Figure 42 ▪ MicroVAX 78032 External Processor Cycle Timing Sequence

Table 21 • MicroVAX 78032 External Processor Cycle Timing Parameters

Timing Symbol	Signal Definition	Requirements Min.	Max.
t_{CEP}	CLKO falling through 0.8 V to $\overline{\text{EPS}}$ falling through 2.2 V	P–5	P+19
t_{DOEPH}	Write data valid set up time to $\overline{\text{EPS}}$ deassertion	2P–35	—
t_{EPCSL}	$\overline{\text{EPS}}$ assertion to external processor assertion of CS2	0	3P–40
t_{EPCSZ}	$\overline{\text{EPS}}$ deassertion to CS2 high impedance by external processor	0	2P–20
t_{EPDI}	$\overline{\text{EPS}}$ assertion to read data valid	—	4P–40
t_{EPF}	$\overline{\text{EPS}}$ fall time from 2.2 V to 0.6 V	0	10
t_{EPHDO}	Write data hold time from $\overline{\text{EPS}}$ deassertion	2P–25	—
t_{EPLC}	$\overline{\text{EPS}}$ falling through 0.6 V to CLKO falling through 2.0 V	P–25	—
t_{EPLWI}	$\overline{\text{EPS}}$ assertion width (read)	4P–20	4P+20
t_{EPLWO}	$\overline{\text{EPS}}$ assertion width (write)	5P–20	5P+20
t_{EPWR}	$\overline{\text{WR}}$ and CS<1:0> hold time from $\overline{\text{EPS}}$ deassertion	P–20	—
t_{EPZ}	$\overline{\text{EPS}}$ deassertion to read data high impedance	—	3P–20
t_{WREP}	$\overline{\text{WR}}$ and CS<1:0> set up time before $\overline{\text{EPS}}$ assertion.	2P–35	—

Reset Timing

Figure 43 shows the timing sequence for the reset function of the processor and Table 22 lists the timing parameters for the symbols referenced on the diagram.

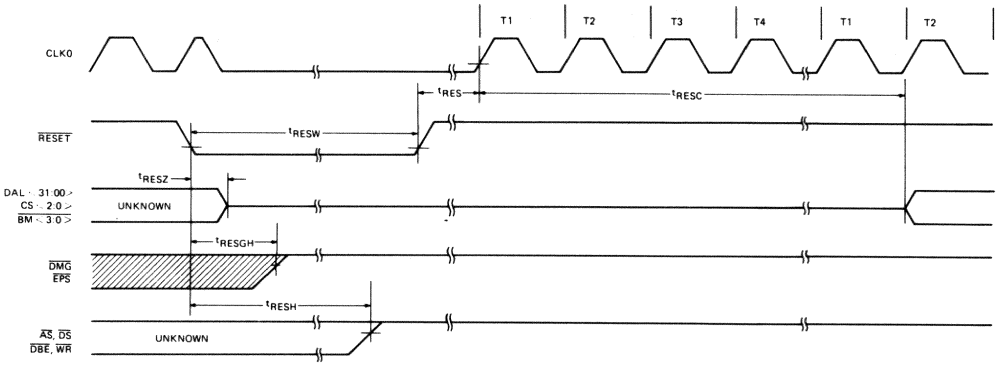


Figure 43 • MicroVAX 78032 Reset Timing Sequence

Table 22 • MicroVAX 78032 Reset Timing Parameters

Timing Symbol	Signal Definition	Requirements (ns)	
		Min.	Max.
t_{RES}	$\overline{\text{RESET}}$ deassertion to first CLKO pulse if $\overline{\text{RESET}}$ is deasserted synchronously	3P+10	3P+85
t_{RESC}	Number of CLKO periods from $\overline{\text{RESET}}$ deassertion until first DAL activity	32 periods	—
t_{RESGH}	$\overline{\text{RESET}}$ assertion to $\overline{\text{DMG}}$, $\overline{\text{EPS}}$ deassertion[1]	—	150
t_{RESH}	$\overline{\text{RESET}}$ assertion to $\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{DBE}}$, $\overline{\text{WR}}$ deassertion[2]	—	1.0 µs
t_{RESW}	$\overline{\text{RESET}}$ assertion width after V_{DD} = 4.75 V	3.0 ms	—
t_{RESWB}	$\overline{\text{RESET}}$ assertion width if V_{DD} has already been at 4.75 V for 3 ms when $\overline{\text{RESET}}$ is asserted	3.0 µs	—
t_{RESZ}	$\overline{\text{RESET}}$ assertion to DAL<31:00>, $\overline{\text{BM<3:0>}}$, CS<2:0> high impedence[3]	—	100

Notes:

[1] When the $\overline{\text{RESET}}$ level is asserted, the $\overline{\text{DMG}}$ and $\overline{\text{EPS}}$ signals become high and remain high.

[2] When $\overline{\text{RESET}}$ is asserted, $\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{DBE}}$ and $\overline{\text{WR}}$ outputs become a high impedance state and the levels become high by low current internal pull-ups.

[3] When the $\overline{\text{RESET}}$ level is asserted the $\overline{\text{BM<3:0>}}$ lines and CS<2:0> lines become high-impedance.

▪ Mechanical Specifications

The dimensions of the MicroVAX 78032 68-pin cerquad surface and socket mount packages are shown Appendix E.

Pin	Signal	Input/Output	Definition/Function
57	$\overline{\text{IAKEON}}$	output	Interrupt acknowledge enable out N—An active low pulldown output that connects together with the IAKEOP output to the $\overline{\text{IAKEI}}$ input of the next device in the daisychain or connects to the $\overline{\text{ERR}}$ input of the CPU.
39	$\overline{\text{CSEL}}$	input	Chip select—Enables read/write operations to the internal registers.
31	$\overline{\text{RESET}}$	input	Reset—Sets the VIC to a known initial state.
30	CLK	input	Clock—Used to generate the internal time states of the VIC.
10,11,29,44,49,60	V_{DD}	input	Voltage—5 V Power supply voltage.
12,32,48,58,59	V_{SS}	input	Ground—Ground reference
33–38	NC	—	No Connection

MicroVAX Bus Interface Signals

Data/Address lines (DAL<15:00>)—These lines are bidirectional and are used to transfer address and data between the VIC and the CPU. During internal VIC register access cycles, when the $\overline{\text{CSEL}}$ line is asserted, the DAL<15:00> lines transfer data to and from the internal registers. During the first part of an IACK cycle, the level of the pending interrupt being acknowledged is decoded from the low-order information on the DAL. During the response part of the IACK cycle when the pending interrupts on the IPL level being acknowledged are recognised and priority was passed by asserting IAKEI, the VIC transfers information from an Interrupt Vector (IVEC) register to DAL<15:00> if bit 01 of the Interrupt Vector register is clear. When bit 01 is set, an external vector must be made available from the interrupting device. Refer to the IVEC registers (0-15) for additional information. The DALs are driven by the VIC only when IAKEI is asserted, IAKEON is not asserted, and IVEC bit 0 is cleared. During all other conditions, the DALs are high-impedance during the IACK cycles.

Address strobe ($\overline{\text{AS}}$)—When asserted, this signal latches the information on the DAL<06:00>, CS<2:0>, and the $\overline{\text{WR}}$ lines into the VIC. This information is used internally to latch the PIRQ<15:00> line information for the duration of a read or interrupt acknowledge bus cycle that addresses the VIC.

Data strobe ($\overline{\text{DS}}$)—This signal is used by the VIC for data timing during internal register access cycles and interrupt acknowledge cycles. When writing to one of the internal registers, the assertion of this signal strobes the DAL<15:00> line data into the selected register. When reading an internal register, the assertion of this signal is used to transfer the contents of the selected register onto the DAL<15:00> lines. When responding to an interrupt acknowledge cycle, the assertion of this signal is used to transfer the contents of the appropriate interrupt vestor register onto the DAL<15:00> lines.

Write ($\overline{\text{WR}}$)—This signal is used with the CS<2:0> information by the VIC during CPU read, write, and interrupt acknowledge cycles to specify if the access to a VIC register is a read or write operation. A CPU-to-VIC write cycle is indicated if $\overline{\text{CSEL}}$ is asserted when $\overline{\text{WR}}$ is asserted and a write transaction is decoded from the CS lines.

Control status (CS<2:0>)—These lines and the $\overline{\text{WR}}$ input are decoded to determine the presence of a read, write, or interrupt acknowledge bus cycle. The bus cycle selections are listed in Table 2.

Table 2 • MicroVAX 78516 Bus Cycle Decoding*

CS Line			$\overline{\text{WR}}$	$\overline{\text{CSEL}}$	Bus Cycle
2	1	0			
H	X	X	H	L	Read
H	X	H	L	L	Write
L	H	H	H	X	Interrupt acknowledge

*H = high level, L = low level, X = either high or low level.

Ready ($\overline{\text{RDY}}$)—This signal is asserted by the VIC when its internal registers are accessed during a read or write cycle or during an interrupt acknowledge (IACK) cycle when the VIC is providing an interrupt vector. During IACK cycles, at least one ready slip will be generated to allow an interrupt acknowledge enable signal ($\overline{\text{IAKEI}}$, IAKEOP, or IAKEON) to propagate through the daisychain. The total number of ready slips that occur depends on the length of the daisychain. This is an open drain (pulldown) output capable of sinking 16 mA.

Interrupt Interface Signals

Peripheral interrupt request (PIRQ < 15:00 >)—These input lines are used by peripheral circuits to request an interrupt. When one or more of these lines are asserted and the interrupts are enabled, the VIC will assert the appropriate IRQ line(s). Mapping between each PIRQ line and the IRQ line is programmable by software though the IRQ Map registers. The interrupt request can be sensed by a signal level or edge or by the signal polarity. The sensing is programmable by the user. Unused PIRQ lines must be connected to a valid logic level.

Interrupt request ($\overline{\text{IRQ<3:0>}}$)—One or more of these lines will be asserted by the VIC when a PIRQ line is asserted and the interrupts are enabled. The IRQ Map registers determine which IRQ line is asserted for a particular PIRQ line. An IRQ line will be deasserted when all pending interrupts mapped to that IRQ line have been serviced. These are open drain (pulldown) outputs that require external pullup resistors.

Interrupt acknowledge ($\overline{\text{IACK}}$)—This signal is a result of decoding the CS<2:0> and the $\overline{\text{WR}}$ lines and will be asserted for all interrupt acknowledge cycles. The signal is not affected by the interrupt acknowledge daisychain signals. It allows the external logic to disable the memory transceivers during an interrupt acknowledge cycle.

External vector enable ($\overline{\text{XVEC}}$)—This signal is used by external logic when the VIC is requesting that the interrupting device transfer its vector to the CPU. During an interrupt acknowledge cycle when the vector is being supplied by an external device, the hardware supplying the vector must assert the $\overline{\text{RDY}}$ signal at the appropriate time. The assertion of the $\overline{\text{XVEC}}$ signal also indicates that the VIC has placed the DALs in the high-impedance state.

Daisychain Interface Signals

Interrupt acknowledge enable in ($\overline{\text{IAKEI}}$)—This input allows more than one VIC and other peripheral chips to be connected together in a daisychain. When this input is asserted, the VIC can respond to the current interrupt acknowledge bus cycle. This signal should be connected to a ground reference if the VIC is the highest priority device in the daisychain.

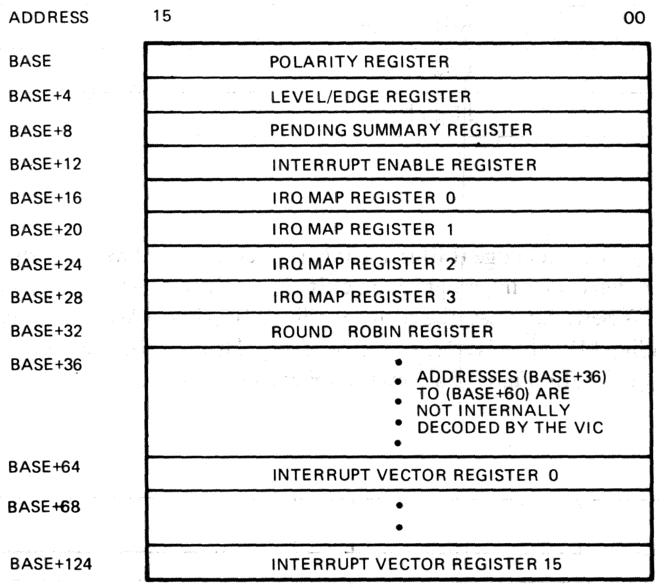
level. The CPU will respond with an interrupt acknowledge cycle that contains the priority level of the interrupt being acknowledged. The VIC then decodes the IACK cycle and IPL line information and if the VIC generated the interrupt and the $\overline{\text{IAKEI}}$ (daisychain input) signal is asserted, it selects the vector of the next PIRQ to be serviced for that IPL level. It then places that vector on the DAL< 15:00 > lines. If the VIC did not request the interrupt, it asserts the $\overline{\text{IAKEON}}$ (daisychain output) signal to allow the next devices in the daisy chain to be serviced. When the VIC is responding to an interrupt, it holds the $\overline{\text{IAKEON}}$ line from being asserted to prevent devices in the daisychain that have a lower priority from responding.

Registers

The VIC contains 16 interrupt vector registers and 9 interrupt control registers that allow each request to be individually configured by software. The internal VIC registers, shown in Figure 3, are accessible by the CPU and are used by software to configure the operation of the VIC. Each register consists of 16-bits and is located on a longword boundary. The base address is determined by external address decode logic. Direct access to the VIC registers is enabled when the $\overline{\text{CSEL}}$ signal is asserted and the VIC decodes the address on the DAL< 06:00 > lines to select the register to be accessed.

The Polarity, Level/Edge Interrupt Enable and Pending Summary registers are cleared by the assertion of the $\overline{\text{RESET}}$ input. Therefore, the VIC is programmed for the falling edge of PIRQ assertion and all interrupts are disabled. The IRQ Map and Interrupt Vector registers must be programmed before the interrupts are enabled.

NOTE: Only word access to the lower 16-bits of the longword are allowed to transfer data between the CPU and the VIC. Byte accesses and longword accesses are not allowed. Longword access may result in the CPU reading the incorrect data or lost data during a write cycle.



ADDRESS	15 00
BASE	POLARITY REGISTER
BASE+4	LEVEL/EDGE REGISTER
BASE+8	PENDING SUMMARY REGISTER
BASE+12	INTERRUPT ENABLE REGISTER
BASE+16	IRQ MAP REGISTER 0
BASE+20	IRQ MAP REGISTER 1
BASE+24	IRQ MAP REGISTER 2
BASE+28	IRQ MAP REGISTER 3
BASE+32	ROUND ROBIN REGISTER
BASE+36	ADDRESSES (BASE+36) TO (BASE+60) ARE NOT INTERNALLY DECODED BY THE VIC
BASE+64	INTERRUPT VECTOR REGISTER 0
BASE+68	• •
BASE+124	INTERRUPT VECTOR REGISTER 15

Figure 3 ▪ MicroVAX 78516 Register Address and Descriptions

Polarity register—The polarity (POL) is a read/write register that selects the polarity of the input used to assert a PIRQ<15:00> line. When a bit is set, the corresponding line is asserted by a low-to-high transition or by a high level. When a bit is clear, the corresponding line is asserted by a high-to-low transition or by a low level. The register format is shown in Figure 4.

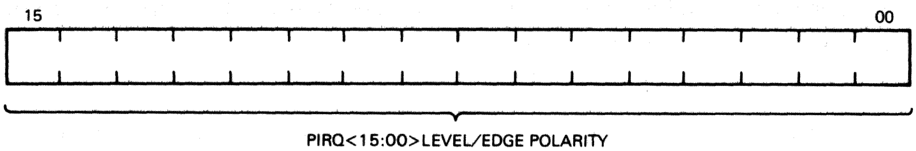


Figure 4 • MicroVAX 78516 Polarity Register Format

The POL register is used with the level/edge (LE) register to configure each PIRQ input. A PIRQ input may be configured to respond to a rising edge, a falling edge, a high level, or a low level signal. Table 3 shows the bit selections of the POL and LE registers and the resulting state of a PIRQ line. When the $\overline{\text{RESET}}$ line is asserted, the POL register is cleared.

Table 3 • MicroVAX 78516 PIRQ Input Line Configurations

POL Bit	LE Bit	PIRQ Asserted State
0	0	Falling edge
1	0	Rising edge
0	1	Low level
1	1	High level

Level/Edge register—The level/edge (LE) is a read/write register used to select the way in which a PIRQ<15:00> line detects an interrupt request. It allows the user to select either level or edge sensitive triggering. When a bit is set, the corresponding PIRQ line is level sensitive. When a bit is clear, the corresponding PIRQ line is edge sensitive. The polarity of the PIRQ line input is selected by the polarity register (POL). Figure 5 shows the LE register format.

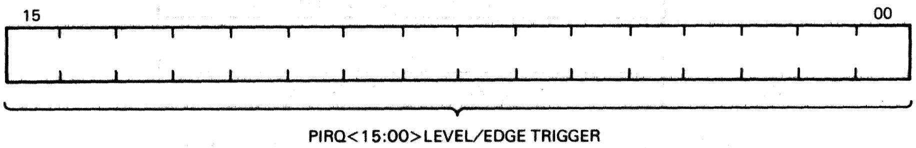


Figure 5 • MicroVAX 78516 Level/Edge Register Format

Level-sensitive inputs allow more than one device to be connected to a single PIRQ line by using a wired AND/OR structure. Once the correct polarity level is detected by the VIC, the corresponding interrupt pending bit is set in the pending summary register (PSR). The interrupt pending bit will remain set until the PIRQ line is cleared. Therefore, an interrupt acknowledge cycle from the CPU will not clear the interrupt pending bit in the PSR register until the PIRQ line is deasserted. If a wired AND/OR structure is used, an external pullup/pulldown resistor is required on the PIRQ line.

Edge sensitive inputs detect either a high-to-low (falling edge) or low-to-high (rising edge) transition. When the correct transition is detected, the corresponding bit in the PSR register will be set. When the $\overline{\text{RESET}}$ line is asserted, the LE register is cleared.

Pending Summary register—The pending summary register (PSR) is a read/clear register that provides a summary of the internal interrupt pending flags. When a bit is set, an interrupt request is pending for the corresponding PIRQ line. When a bit is clear, no interrupt is pending for the corresponding PIRQ line. When the VIC performs the IACK cycle, the corresponding PSR bit will be cleared if the coresponding bit in the LE register is cleared. If the corresponding bit in the LE register is set, the interrupting device must deassert its PIRQ line when serviced. The contents of the PSR register are latched during a read and IACK cycle. The register format is shown in Figure 6.

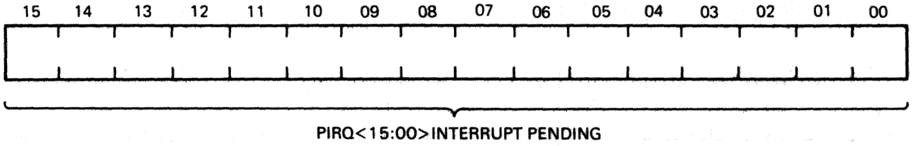


Figure 6 • MicroVAX 78518 Pending Summary Register Format

The VIC manages the setting and clearing the PSR register bits for level and edge sensitive PIRQ inputs as follows. When the $\overline{\text{RESET}}$ input is asserted, the PSR register is cleared.

- For level sensitive PIRQ inputs, the corresponding PSR bit will be set when the PIRQ line is asserted and cleared when line is deasserted.
- For edge sensitive PIRQ inputs, the corresponding PSR bit is set on the asserting edge of the PIRQ input. The PSR bit for a PIRQ input will be cleared by an interrupt acknowledge cycle that acknowledges the interrupt request of the corresponding PIRQ line, when the software clears the PSR bit by writing a zero into the appropriate bit, or when information is written into the LE register.

Interrupt Enable register—The interrupt enable (IEN) is a read/write register that is used to enable or disable the reporting of interrupts to the CPU by each PIRQ line. When a bit is set, it allows an interrupt request from the associated PIRQ line to generate an interrupt to the CPU. When a bit is clear, the associated PIRQ line is prevented from generating an interrupt to the CPU. The register format is shown in Figure 7.

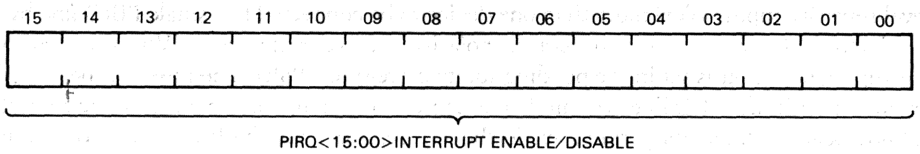


Figure 7 ▪ MicroVAX 78516 Interrupt Enable Register Format

The IEN register enables or disables the generating of an interrupt to the CPU and does not affect the detection of interrupts by the VIC. When a PIRQ line is asserted, the corresponding bit in the PSR register is set regardless of the state of the IEN bit for the PIRQ line. The IEN register provides the support for a software interrupt polling scheme. The register is cleared when the $\overline{\text{RESET}}$ input is asserted.

IRQ Map registers (0-3)—The interrupt request map (IMAP0 through IMAP3) are read/write registers that are used to select the IRQ line to be asserted by the VIC when a PIRQ line is asserted. When a bit in one of the IMAP registers is set, the corresponding PIRQ line is mapped to the associated IRQ line. The register format is shown in Figure 8. Each register corresponds to one of the IRQ outputs as defined in Table 4.

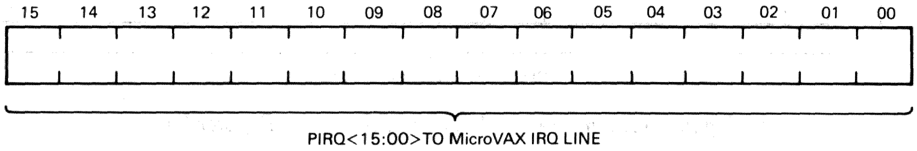


Figure 8 ▪ MicroVAX 78516 IRQ Map Registers (0-3) Format

Table 4 ▪ MicroVAX 78516 IMAP Register to IRQ Mapping

Register	**Line**
IMAP3	$\overline{\text{IRQ3}}$
IMAP2	$\overline{\text{IRQ2}}$
IMAP1	$\overline{\text{IRQ1}}$
IMAP0	$\overline{\text{IRQ0}}$

Example: If bit 3 of the IMAP1 register is set when the PIRQ3 line is asserted and the IEN register bit is set for this line, line IRQ1 will be asserted.

The IMAP registers are not initialized when the $\overline{\text{RESET}}$ line is asserted and the contents will be undefined until programmed by software.

Round Robin register—The round robin (ROBIN is a read/write register that is used to select either fixed or round robin priority mode of operation for each IRQ level. More than one bit may be set in this register at a time and the register controls only the PIRQ lines for the associated VIC. The register is cleared when the $\overline{\text{RESET}}$ input is asserted. The register format is shown in Figure 9. Table 5 describes the function of each bit.

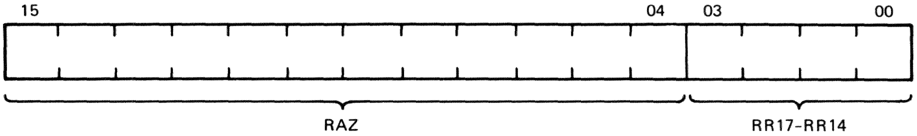


Figure 9 • MicroVAX 78516 Round Robin Register Format

Table 5 • MicroVAX 78516 Round Robin Register Description

Bit	Description
15:04	RAZ (Read as zeros)—Not used
03:00	RR17-RR14 (ROUND ROBIN IPL17-IPL14)—These bits select the priority mode for all interrupts mapped to lines $\overline{\text{IRQ<3:0>}}$. RR17 selects IRQ3 etc. When set, the round robin mode is selected. When cleared, the fixed mode is selected.

Interrupt Vector registers (0-15)—Each of the 16 interrupt vector (IVEC0 through IVEC15) registers is a read/write register that contains a fully programmable 16-bit vector. There is one IVEC register for each PIRQ line. Each register can select any location in the CPU System Control Block during the interrupt acknowledge cycle. The VIC automatically transfers the highest priority register information onto the DALs during the second half of the CPU IACK cycle. These registers can be read by software using a CPU read cycle. The register format is shown in Figure 10 and Table 6 describes the function of each bit.

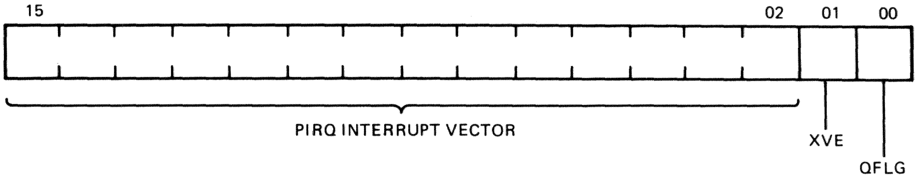


Figure 10 • MicroVAX 78516 Interrupt Vector Registers (0-15) Format

Table 6 • MicroVAX 78516 Interrupt Vector Registers (0-15) Description

Bit	Description
15:02	VECTOR (PIRQ interrupt vector)—This vector is the offset into the system control block (SCB) for the location of the interrupt routine.
01	XVE (External vector enable)—When set, the DAL<15:00> line drivers are disabled and the $\overline{\text{XVEC}}$ line is asserted during an IACK cycle, indicating that an external vector is to be supplied. When clear, the VIC will drive the contents of the IVEC register onto the DAL<15:00> lines during an IACK cycle.
00	QFLG (Normal/Q-bus processing flag)—Setting this bit causes the CPU to respond by setting its internal IPL to 17 (hexadecimal). This feature is useful for programming Q-bus systems. The status of bits 15:10 and the XVE bit 01 are ignored by the CPU. When clear, the CPU will service the interrupt normally.

These registers are not initialized when the $\overline{\text{RESET}}$ input is asserted and the contents of the register is undefined until programmed by software.

Interrupt Level Triggering and Edge Triggering

The sensing of an interrupt condition by the VIC may be programmed for each PIRQ input by the LE register. Each PIRQ line can be set to respond to either a signal level or to a signal transition (edge). The polarity of the sensed condition is also programmable.

In the edge-triggered mode, either a high-to-low or low-to-high transition on the PIRQ line will cause the VIC to latch the PIRQ line information. Further transitions on this PIRQ line will have no effect. After the acknowledgment of the latched assertion by the CPU, the VIC resets the latching mechanism allowing the user to again assert the interrupt with a proper transition on the PIRQ line. A latched PIRQ assertion may be cleared by writing to the LE register or by writing a zero to the corresponding bit of the pending status register.

In the level mode, the interrupting device must deassert the PIRQ input before the interrupt service routine ends to prevent the VIC from sensing the previous level and posting the same interrupt twice. During edge- or level-triggering, a bit in the pending summary register corresponding to that PIRQ line indicates the pending interrupt and if the interrupt is enabled, the VIC will assert the appropriate IRQ line as programmed in the IMAP register.

If the CPU responds to an interrupt caused by a edge-triggered signal, the completion of the IACK cycle will cause the VIC to clear the corresponding PSR register bit. If level-triggered mode was selected, the PSR bit would continue to reflect the PIRQ status.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Storage temperature range: –55°C to 125°C
- Active temperature range: 0°C to 70°C
- Power supply voltage (V_{DD} to V_{SS}): 0 V to 6 V
- Input or output voltage applied: –0.3 V to (V_{DD} +0.3 V)

Recommended Operating Conditions

- Temperature: 0°C to 70°C
- Power supply voltage: 4.75 V to 5.25 V
- Power dissipation: 1.0 W (maximum)

dc Electrical Characteristics

The dc input and output parameters for the VIC are listed in Table 7.

Table 7 • MicroVAX 78516 dc Input and Output Parameters

Symbol	Parameter	Test Conditions	Requirements		Units
			Min.	Max.	
V_{IH}	High-level input voltage		2.0	—	V
V_{IL}	Low-level input voltage		—	0.8	V
V_{OH}[1,2]	High-level output voltage	$I_{OH} = -400\ \mu A$	2.4	—	V
V_{OL}[1]	Low-level output voltage	$I_{OL} = 2.0$ mA	—	0.4	V
I_{ILC}	Input leakage current	$0 < V_{in} < (V_{DD} - 0.6\ V)$	—	30	A
I_{OLC}	Output leakage current	$0 < V_{in} < (V_{DD} - 0.6\ V)$	—	30	µA
I_{CCAC}[3]	Active supply current		—	100	mA
V_{OLOD1}[4]	Open drain pulldown low-level output voltage	$I_{OL} = 6.0$ mA	—	0.4	V

Symbol	Parameter	Test Conditions	Requirements Min.	Requirements Max.	Units
V_{OLOD2}[5]	Open drain pulldown low-level output voltage	$I_{OL} = 25$ mA	—	0.4	V
C_{in}	Input capacitance		—	15	pF
C_{out}	Output capacitance		—	20	pF

[1] Only one output may be shorted to either supply rail at one time and the duration of the short must be less than 2 seconds.

[2] This specification also applies to the open drain output on IAKEOP

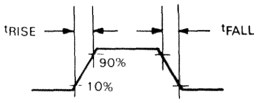
[3] All outputs floating, all inputs connected to either supply rail. The CLK input is fully swinging between both supply rails at 20 MHz.

[4] Applies only to the $\overline{\mathrm{IRQ}<3:0>}$ outputs.

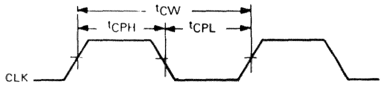
[5] Applies only to the $\overline{\mathrm{RDY}}$ and $\overline{\mathrm{IAKEON}}$ outputs.

ac Electrical Characteristics

Figure 16 shows the input signal and clock signal waveforms and the parameters are listed in Table 8.



CLOCK INPUT



INPUT SIGNAL

Figure 16 • MicroVAX 78516 Input and Clock Signal Timing

Table 8 • MicroVAX 78516 Input and Clock Signal Timing Parameters

Symbol	Definition	Requirements Min.	 Max.
t_{CPH}[1]	Input clock high	15 ns	—
t_{CPL}	Input clock low	15 ns	—
t_{CW}	Input clock period	50 ns	—
t_{RISE}	Input signal rise	—	15 ns[2]
t_{FALL}	Input signal fall	—	15 ns[2]

[1] V_{DD} must be greater than or equal to 4.75 V during this period.
[2] Measured between 10% and 90% levels.

Figure 17 and 18 show the signal timing and symbols for a register read cycle and register write cycle, respectively, between the CPU and VIC. Figure 19 shows the signal timing and symbols for an interrupt acknowledge cycle when the VIC responds with a vector and when the external device supplies the vector. Figure 20 shows the timing and symbols for a daisychain configuration when the interrupt priority is not passed to the VIC and when it is passed to the VIC. Figure 21 shows the signal timing and symbols for the PIRQ input to IRQ output signal generation. It also includes the $\overline{\text{RESET}}$ input signal timing. Table 9 lists and defines the symbols and parameters used on the figures. The following notes apply to the table information.

- (T) = input clock period (t_{CW})
- All units are nanoseconds (ns) except where indicated.
- All times are specified with a 100-pF capacitive load on the outputs.
- All times are measured at the 50 percent levels of the waveforms except where indicated.

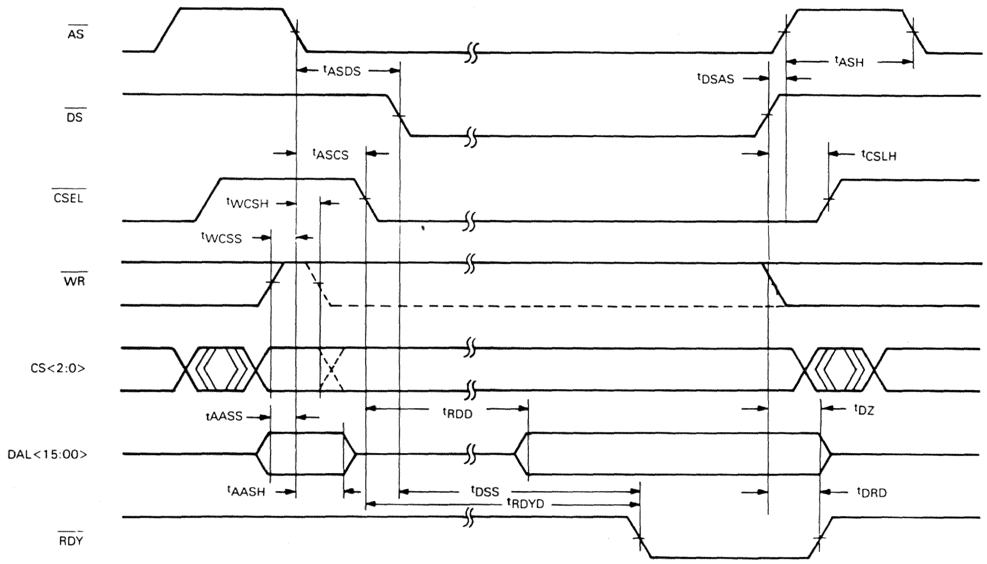


Figure 17 ▪ MicroVAX 78516 Register Read Cycle Timing

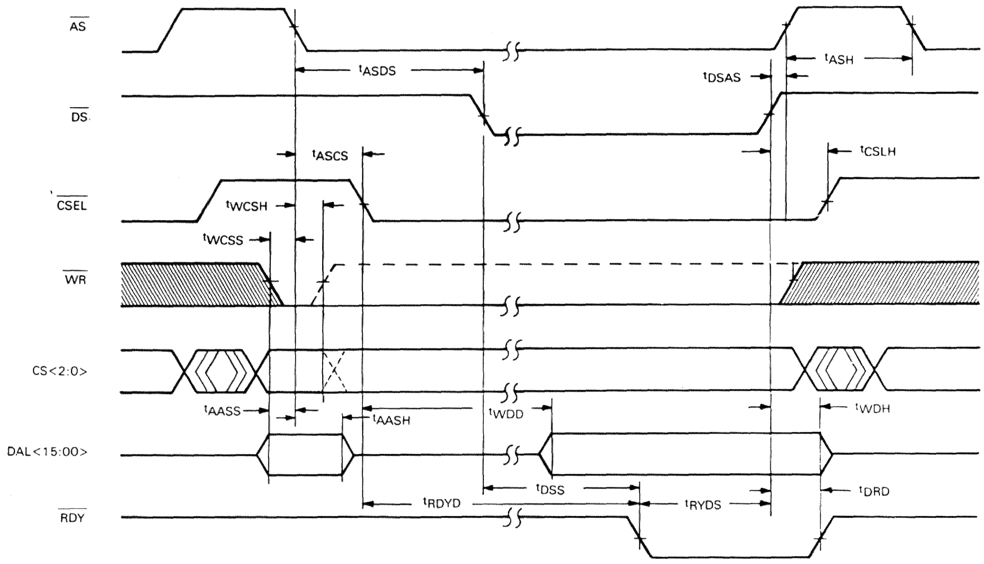
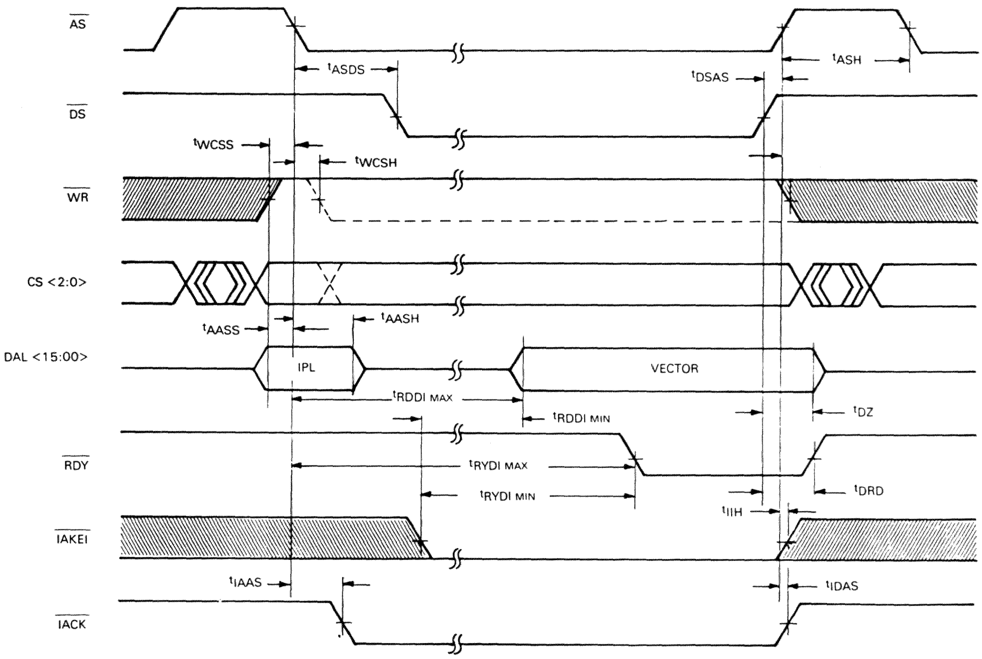
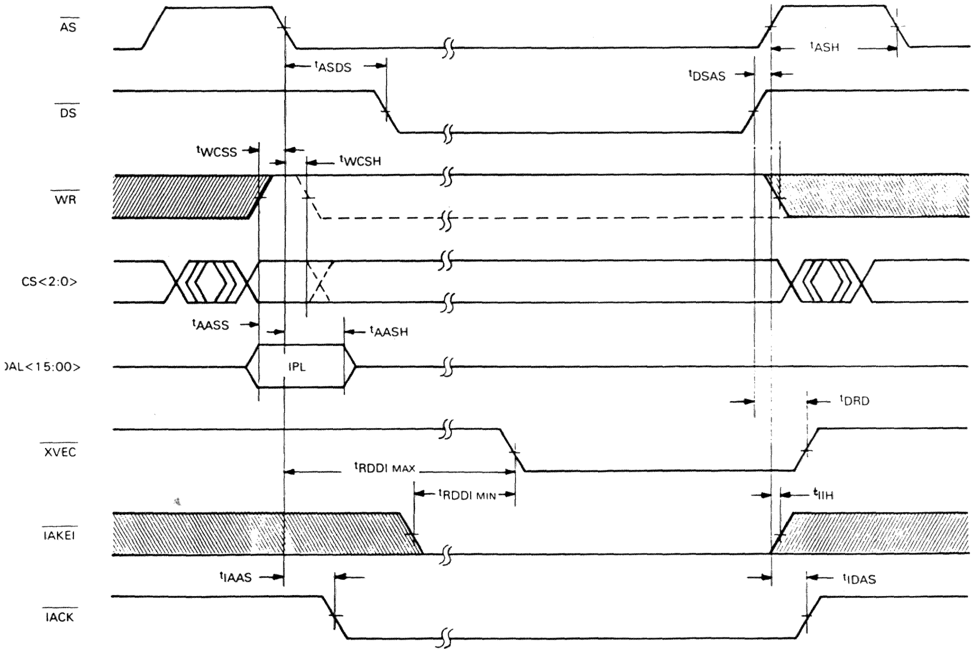


Figure 18 ▪ MicroVAX 78516 Register Write Cycle Timing



VIC SUPPLIES VECTOR



EXTERNAL DEVICE SUPPLIES VECTOR

Figure 19 ▪ MicroVAX 78516 Interrupt Acknowledge Cycle Timing

Table 9 • MicroVAX 78516 Signal Timing Parameters

Symbol	Definition	Requirements	
		Min.	Max.
t_{AASH}	DAL<06:00> hold after $\overline{AS}$ assertion	10	—
t_{AASS}	DAL<06:00> setup to $\overline{AS}$ assertion	15	—
t_{ASCS}	$\overline{CSEL}$ assertion after $\overline{AS}$ assertion	—	1 μs
t_{ASDS}	$\overline{DS}$ assertion after $\overline{AS}$ assertion	0	—
t_{ASH}	$\overline{AS}$ high after deassertion	1.5T	—
t_{CSLH}	$\overline{CSEL}$ hold after $\overline{AS}$ deassertion	10	—
t_{DRD}	$\overline{RDY}$ deassertion from $\overline{DS}$ deassertion	—	45
t_{DRDX}	$\overline{XVEC}$ deassertion from $\overline{AS}$ deassertion	—	45
t_{DSAS}	$\overline{AS}$ deassertion after $\overline{DS}$ deassertion	0	—
t_{DSS}	DS setup before $\overline{RDY}$ assertion	30	—
t_{DZ}	Read data high-impedance delay from $\overline{DS}$ deassertion	—	30
t_{ENA}[1]	$\overline{RESET}$ deassertion to VIC enabled internally	5T+250	—
t_{IAAS}	$\overline{IACK}$ assertion after $\overline{AS}$ assertion	1.5T	2T+30
t_{IDAS}	$\overline{IACK}$ deassertion after $\overline{AS}$ deassertion	0	50
t_{IDRD}	$\overline{IAKEO}$/IAKEOP deassertion from $\overline{AS}$ deassertion	—	60
t_{IIDmin}	$\overline{IAKEON}$/IAKEOP delay from $\overline{IAKEI}$ assertion ($\overline{IAKEI}$ asserted 7.5T or more after $\overline{AS}$)	25	—
t_{IIDmax}	$\overline{IAKEO}$/IAKEOP delay from $\overline{AS}$ assertion ($\overline{IAKEI}$ asserted less than 7.5T more after $\overline{AS}$)	—	8.5T+25
t_{IIH}	$\overline{IAKEI}$ hold after $\overline{AS}$ deassertion	0	—
t_{PIAD}[2]	PIRQ assertion to IRQ assertion delay	0	100
t_{PIDD}	PIRQ deassertion to IRQ deassertion delay (applicable to level triggering only)	—	150
t_{PMIN}	PIRQ minimum assertion width (applicable to edge triggering only)	90	—
t_{PRQS}	PIRQ setup (proper level/edge) before $\overline{AS}$ assertion	50	—
t_{RDD}	Read data delay from $\overline{CSEL}$ assertion	6.5T	7.5T+25
$t_{RDDImin}$	Read data or $\overline{XVEC}$ delay from $\overline{IAKEI}$ assertion ($\overline{IAKEI}$ asserts 7.5T or more after $\overline{AS}$)	6T	—
$t_{RDDImax}$	Read data or $\overline{XVEC}$ delay from $\overline{AS}$ assertion ($\overline{IAKEI}$ asserted less than 7.5T after $\overline{AS}$)	—	13.5T+25
t_{RDYD}	$\overline{RDY}$ delay from $\overline{CSEL}$ assertion	8.5T	9.5T+25

Symbol	Definition	Requirements Min.	 Max.
t_{RSTL}	Minimum $\overline{\text{RESET}}$ low time	200 µs	—
t_{RTZ}	$\overline{\text{RESET}}$ assertion to DALs high impedance	—	100
$t_{RYDImin}$	$\overline{\text{RDY}}$ delay from $\overline{\text{IAKEI}}$ assertion ($\overline{\text{IAKEI}}$ asserted 7.5T or more after $\overline{\text{AS}}$)	8T	—
$t_{RYDImax}$	$\overline{\text{RDY}}$ delay from $\overline{\text{AS}}$ assertion ($\overline{\text{IAKEI}}$ asserted less than 7.5T after $\overline{\text{AS}}$)	—	15.5T+25
t_{RYDS}	DS deassertion from $\overline{\text{RDY}}$ assertion	0	—
t_{WCSH}	CS<2:0>, $\overline{\text{WR}}$ hold after $\overline{\text{AS}}$ assertion	10	—
t_{WCSS}	CS<2:0>, $\overline{\text{WR}}$ setup to $\overline{\text{AS}}$ assertion	15	—
t_{WDD}	Write data delay from $\overline{\text{CSEL}}$ assertion	—	3.5T−5
t_{WDH}	Write data hold after DS deassertion	20	—

[1] The VIC requires 5T+250 ns after $\overline{\text{RESET}}$ is deasserted to complete its internal reset. The $\overline{\text{AS}}$ signal should not be asserted until after this delay.

[2] Maximum time is 100/150 ns unless a PIRQ line is asserted/deasserted during a read or IACK operation with the VIC. For this condition, the IRQS will assert/deassert for 100/150 ns after the completion of the read or IACK operation.

Mechanical Configuration

The MicroVAX 78516 is available as a 68-pin cerquad surface mount package or socket mount package. The physical dimensions of each package is contained in Appendix E.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device. The functional operation of the device at these or other conditions greater than indicated is not defined.

- Power supply voltage (V_{DD}): –0.5 V to 5.5 V
- Input or output voltage applied: V_{SS} –0.3 V to V_{DD} 0.3 V
- Storage temperature (T_S): –55°C to 125°C
- Relative humidity: 10% to 95% (noncondensing)

Recommended Operating Conditions

- Power supply voltage (V_{DD}): 5 V ±5%
- Supply current (I_{CC}) : 500 mA (maximum)
- Operating temperature (T_A): 0°C to 75°C

dc Electrical Characteristics

The dc electrical characteristics of the MicroVAX 78532 for the operating voltage and temperature ranges specified are listed in Table 21.

Table 21 • MicroVAX 78532 dc Input and Output Parameters

			Requiements		
Symbol	**Parameter**	**Test Condition**	**Min.**	**Max.**	**Units**
V_{IH}	High-level input voltage		2.0	—	V
V_{IL}	Low-level input voltage		—	0.8	V
V_{OH}	High-level output voltage	$I_{OH} = 400\mu A$ $C_L = 100$ pF	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	$I_{OL} = 3.2$ mA $C_L = 100$ pF	—	0.4	V
V_{OLOD}	Low-level output open-drain voltage* $\overline{\text{RDY}}$, $\overline{\text{ERR}}$ $\overline{\text{DMR}}$, $\overline{\text{IRQ<3:0>}}$, $\overline{\text{IRDY}}$, $\overline{\text{IERR}}$, $\overline{\text{IDMR}}$	$I_{OL} = 12.5$ mA, $C_L = 100$ pF	—	0.4	V

Symbol	Parameter	Test Condition	Requiements Min.	 Max.	Units
I_{LI}	Input leakage current	$0 < V_{in} < V_{DDI}$	−10	10	μA
I_{OL}	Output leakage current	$0.4 < V_{in} < V_{DDI}$	−10	10	μA
I_{CC}	Active supply current	$I_{out} = 0$, $T_A = 0°C$	—	500	mA
C_{in}	Input capacitance		—	10	pF

*Minimum pullup resistor = 470 ±5%.

ac Electrical Characteristics

The electrical characteristics for the signals used to control the information transfers to and from the MicroDMA are defined in the following paragraphs. The following notes apply to both the MicroVAX bus timing diagrams and the I/O bus timing diagrams and their associated tables.

- The timing parameters are specified in terms of the clock (CLKI) period, where CLKI = t_{CIP} = P. P is nominally 25 ns.
- All times are in nanoseconds except where noted.
- ac characteristics are measured with a purely capacitive load of 100 pF. Times are valid for loads of up to 100 pF on all pins.
- ac high levels are measured at 2.0 V, and ac low levels at 0.8 V.
- S = the number of slipped microcycles during a bus cycle. A MicroVAX bus microcycle is nominally 8P or 200 ns and the I/O bus microcycle is normally 4P or 100 ns.
- N = the number of MicroVAX and I/O bus microcycles in a DMA transfer. N has a minimum value of 2.

The following notes apply to the MicroVAX bus timing diagrams and their associated tables.

- The sampling window is used to sample the $\overline{RDY}$ and $\overline{ERR}$ asynchronous signals. The $\overline{RDY}$ and $\overline{ERR}$ signals are qualified by the assertion of the $\overline{AS}$ signal. The effect of these signals on the current bus cycle is as follows:
  1. The bus cycle concludes at the end of the current microcycle if the $\overline{RDY}$ or $\overline{ERR}$ signal is asserted throughout the sampling window while the $\overline{AS}$ signal is asserted.
  2. If a transition of the $\overline{RDY}$ or $\overline{ERR}$ signals occurs during the sampling window while the $\overline{AS}$ line is asserted, the result is indeterminate.
  3. PS = Clock period (P) times slipped microcycles (S).

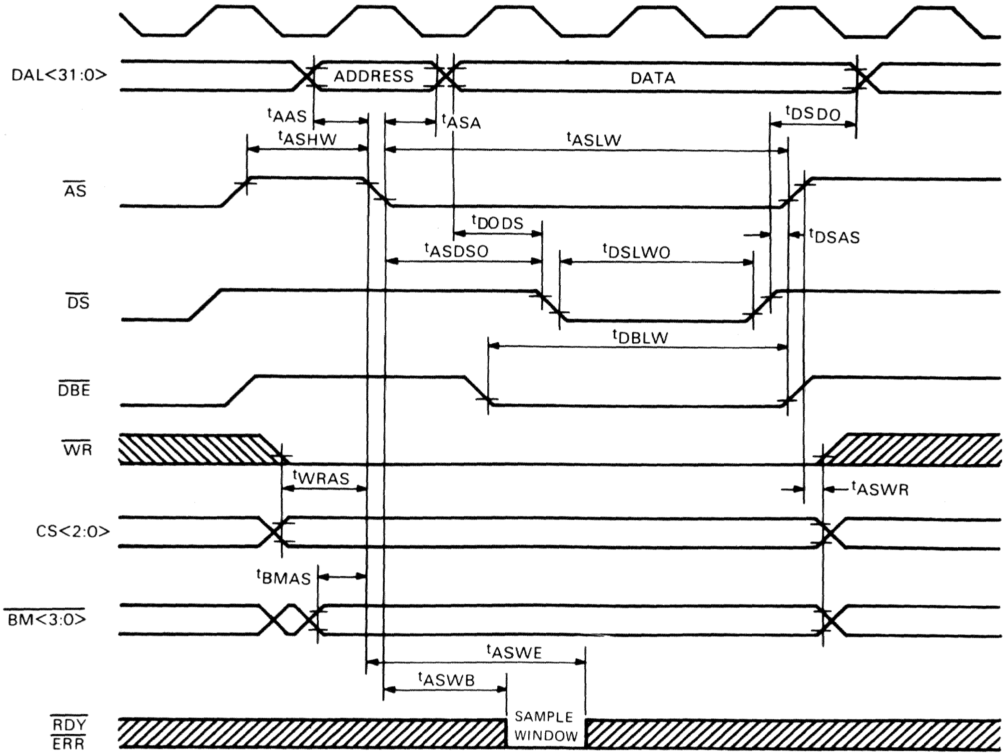


Figure 31 • MicroVAX 78532 MicroVAX Bus Master Write Cycle Timing

Table 23 • MicroVAX 78532 Bus Master Read and Write Cycle Timing Parameters

Symbol	Signal Definition	Requirements (ns)	
		Min.	Max.
t_{AAS}	DAL<31:00> address setup time to $\overline{\text{AS}}$ assertion	2P−28	—
t_{ASA}	DAL<31:00> address hold time after $\overline{\text{AS}}$ assertion	2P−15	—
t_{ASDB}	$\overline{\text{AS}}$ assertion to $\overline{\text{DBE}}$ and $\overline{\text{DS}}$ (read) assertion	3P−15	3P+20
t_{ASDI}	$\overline{\text{AS}}$ assertion to read data valid*		11P−30+8PS
t_{ASDSO}	$\overline{\text{AS}}$ assertion to $\overline{\text{DS}}$ assertion (write)	5P−15	5P+20
t_{ASDZ}	$\overline{\text{AS}}$ and $\overline{\text{DBE}}$ deassertion to busslave DAL<31:00> three-state	—	2P−20
t_{ASHW}	$\overline{\text{AS}}$ deassertion width	4P−25	
t_{ASLW}	$\overline{\text{AS}}$ assertion width	12P−15+8PS	

Symbol	Signal Definition	Requirements (ns)	
		Min.	Max.
t_{ASWB}	$\overline{\text{AS}}$ assertion to beginning of $\overline{\text{RDY}}$ and $\overline{\text{ERR}}$ sample window	—	6P−45+8PS
t_{ASWE}	$\overline{\text{AS}}$ assertion to end of $\overline{\text{RDY}}$ and $\overline{\text{ERR}}$ sample window	—	6P+10+8PS
t_{ASWR}	$\overline{\text{WR/BM}<3:00>}$/CS<1> hold time from $\overline{\text{AS}}$ deassertion	P−20	—
t_{BMAS}	$\overline{\text{BM}<3:00>}$ setup time before $\overline{\text{AS}}$ assertion	2P−25	—
t_{DBLW}	$\overline{\text{DBE}}$ assertion width	9P−20+8PS	—
t_{DODS}	DAL<31:00> write data setup time to $\overline{\text{DS}}$ assertion	—	3P−30
t_{DSAS}	$\overline{\text{DS}}$ deassertion to $\overline{\text{AS}}$ and $\overline{\text{DBE}}$ deassertion	P−15	
t_{DSD}	DAL<31:00> read data hold time after $\overline{\text{DS}}$ deassertion	0	—
t_{DSDI}	$\overline{\text{DS}}$ assertion to DAL<31:00> read data valid	—	8P−35+8PS
t_{DSDO}	DAL<31:00> write data hold time from $\overline{\text{DS}}$ deassertion	—	3P−20
t_{DSDZ}	$\overline{\text{DS}}$ deassertion to bus slave DAL<31:00> three-state on read bus cycles	—	3P−20
t_{DSHW}	$\overline{\text{DS}}$ deassertion width (read)	8P−50	—
t_{DSLWI}	$\overline{\text{DS}}$ assertion width (read)	8P−20+8PS	—
t_{DSLWO}	$\overline{\text{DS}}$ assertion width (write)	6P−20+8PS	—
t_{WEDI}	$\overline{\text{RDY}}$ internal sample window end to DAL<31:00> read data valid	—	5P−25
t_{WRAS}	$\overline{\text{WR}}$ and CS<1> setup time before $\overline{\text{AS}}$ assertion	3P−35	—

*Read data is valid if t_{ASDI} or t_{DSDI} conditions are satisfied.

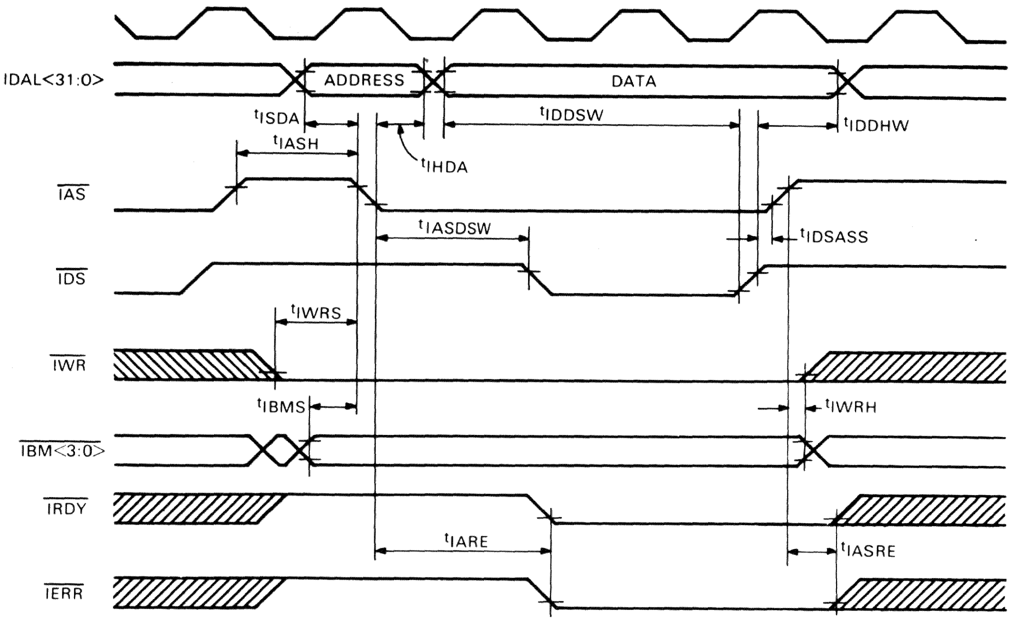


Figure 39 ▪ MicroVAX 78532 I/O Bus Slave Write Cycle Timing

Table 28 ▪ MicroVAX 78532 I/O Bus Slave Read and Write Cycle Timing Parameters

Symbol	Signal Definition	Requirements (ns) Min.	 Max.
t_{IASDSR}	Required $\overline{IAS}$ assertion to $\overline{IDS}$ assertion delay (read cycles)	3P–30	3P+25
t_{IASDSW}	Required $\overline{IAS}$ assertion to $\overline{IDS}$ assertion delay (write cycles)	5P–25	5P+25
t_{IASH}	$\overline{IAS}$ deassertion width	2P+25	—
t_{IASRE}	$\overline{IAS}$ deassertion to $\overline{IRDY}/\overline{IERR}$ deassertion	—	100
t_{IBMS}	$\overline{IBM<3:0>}$ setup time before $\overline{IAS}$ assertion	P–25	—
t_{IDDHR}	IDAL<31:00> data hold time after $\overline{IDS}$ deassertion (slave reads)	0	—
t_{IDDHW}	Required IDAL<31:00> hold time after $\overline{IDS}$ deassertion on MicroDMA bus-slave writes	35	—
t_{IDDSW}	Required IDAL<31:00> setup time before $\overline{IDS}$ deassertion on MicroDMA bus-slave writes	20	—
t_{IDSASS}	Required $\overline{IDS}$ deassertion to $\overline{IAS}$ deassertion delay	P–20	—

Symbol	Signal Definition	Requirements (ns) Min.	 Max.
t_{IDSDS}	$\overline{\text{IDS}}$ deassertion to IDAL<31:00> three-state	—	55
t_{IHDA}	Required IDAL<31:00> hold time after $\overline{\text{IAS}}$ assertion	35	—
t_{IRDR}	$\overline{\text{IRDY}}$ assertion to IDAL<31:00> data valid for MicroDMA bus-slave reads	P+35	—
t_{ISDA}	Required IDAL<31:00> setup time before $\overline{\text{IAS}}$ assertion	15	—
t_{IWRH}	$\overline{\text{IWR/IBM<3:0>}}$ hold time after $\overline{\text{IAS}}$ deassertion	P−25	—
t_{IWRS}	$\overline{\text{IWR}}$ setup time before $\overline{\text{IAS}}$ assertion	3P−50	—

I/O Bus DMA Cycle

Figure 40 is a timing diagram for the I/O bus DMA cycle. Table 29 lists I/O bus DMA cycle timing parameters.

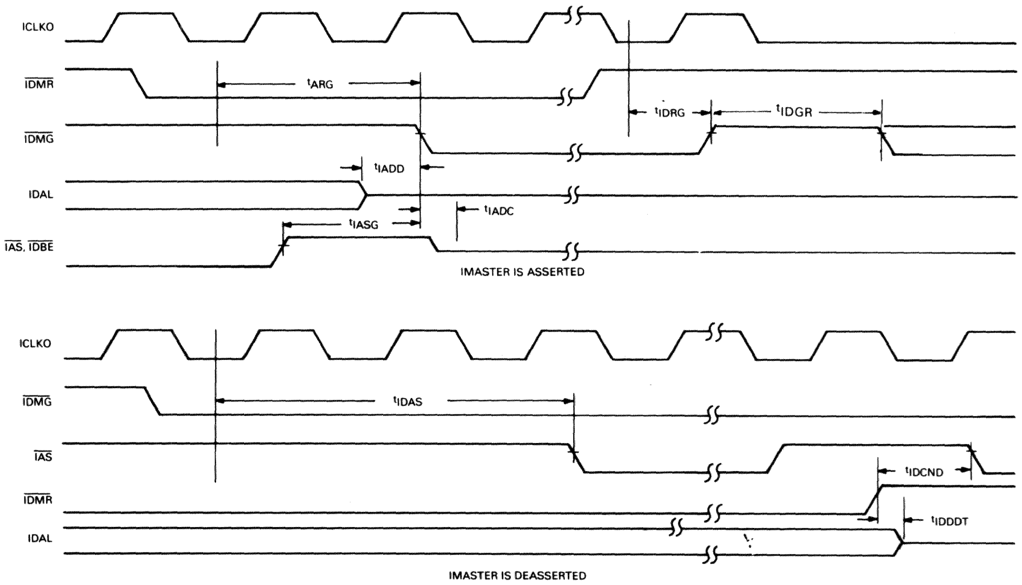


Figure 40 ▪ MicroVAX 78532 I/O Bus DMA Cycle Timing

Table 29 • MicroVAX 78532 I/O Bus DMA Cycle Timing Parameters

Symbol	Signal Definition	Requirements (ns)	
		Min.	Max.
t_{IADC}	Assert $\overline{\text{IDMG}}$ to $\overline{\text{IAS/IDS/IWR/IDBE/IBM<3:0>}}$ three-state	—	40
t_{IADD}	IDAL<31:00> three-state to assert $\overline{\text{IDMG}}$	—	2P+5
t_{IARG}	Asserted $\overline{\text{IDMR}}$ (internal) sample window end to $\overline{\text{IDMG}}$ assertion	6P	*
t_{IASG}	$\overline{\text{IAS}}$ and $\overline{\text{IDBE}}$ deassertion to $\overline{\text{IDMG}}$ assertion	4P−25	—
t_{IDAS}	Asserted $\overline{\text{IDMG}}$ (internal) sample window end to $\overline{\text{IAS}}$ assertion	—	10P+35+4PK†
t_{IDBM}	Asserted $\overline{\text{IDMG}}$ (internal) sample window end to $\overline{\text{IBM<3:0>}}$ assertion	—	9P+45+4PK†
t_{IDCND}	Deassert $\overline{\text{IDMR}}$ to $\overline{\text{IAS/IDS/IWR/IDBE/IBM<3:0>}}$ three-state	—	3P+35
t_{IDGR}	$\overline{\text{IDMG}}$ deassertion to $\overline{\text{IDMR}}$ reassertion	2P+10	—
t_{IDRG}	Deasserted $\overline{\text{IDMR}}$ (internal) sample window end to $\overline{\text{IDMG}}$ deassertion	—	2P+40

*Maximum value determine by latency specifications.
†K = The number of microcycles (0, 1, 2, 3, 4) that the sequencer is busy.

I/O Bus Transfer Request

Figure 41 shows the I/O bus transfer request signal timing and Table 30 list the timing parameters.

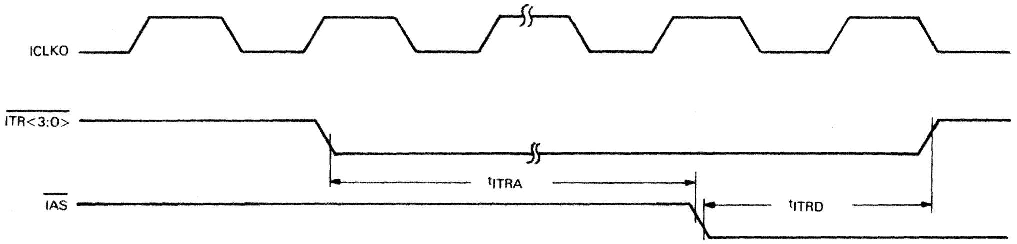


Figure 41 • MicroVAX 78532 I/O Bus Transfer Request Timing

Many system design requirements and options are included as integral parts of the chip. A high-performance processor using a four-level prefetch pipeline, resident memory management, floating-point arithmetic, console octal debugging technique (ODT), microdiagnostics, and clock generation provide efficient system functionality in a single package. The orthogonal instruction set allows fast and efficient programming to minimize development time and cost. The DCJ11 combines leadership system functionality with complete system software, a highly integrated design, and low-power consumption to allow new classes of microprocessor applications. A block diagram of the DCJ11 is shown in Figure 1.

▪ Signal and Pin Descriptions

The input and output signals and the power and ground connections for the DCJ11 60-pin DIP are shown in Figure 2 and defined in Table 1. These signals are briefly described in the table and a more detailed description of the signal functions is contained in the following paragraphs. The system interface refers to the user's application of the DCJ11 and must be capable of providing or receiving these signals.

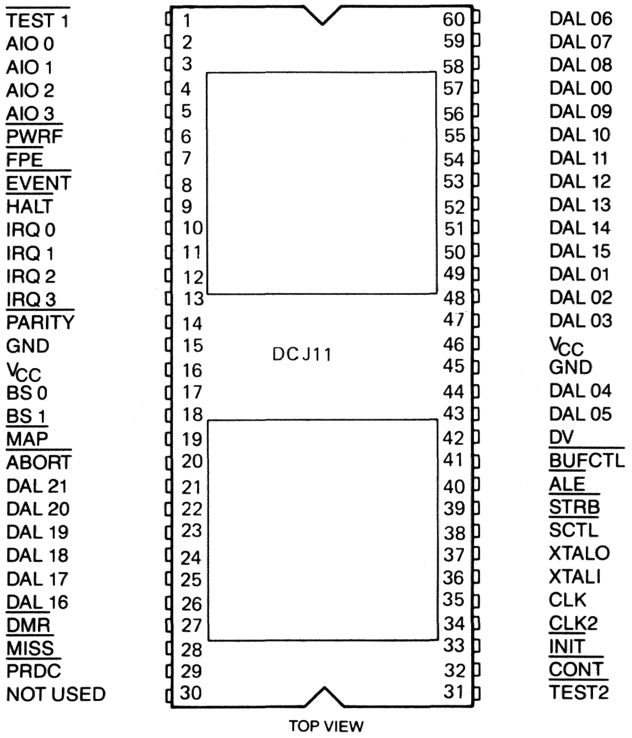


Figure 2 ▪ DCJ11 Pin Assignments

Table 1 • DCJ11 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
21-26, 43-44, 47-60	DAL<21:00>	input/output[1]	Data/address lines—Time-multiplexed data and address bus.
17-18	BS<1:0>	output[1]	Bank select—These time-multiplexed signals define the type of physical address on the data/address bus, and indicate if either a cache memory bypass or a force miss occurs.
19	$\overline{\text{MAP}}$	output[1]	Map—This time-mulitiplexed signal indicates if the I/O map is enabled or if a DMA grant occurs.
2-5	AIO<3:0>	output[1]	Address input/output—These signals indicate the type of transaction currently being executed, i.e., read, write, or IACK.
40	$\overline{\text{ALE}}$	output[1]	Address latch enable—Latches addresses, AIO codes, map enable signals, and the BS control signals.
41	$\overline{\text{BUFCTL}}$	output[1]	Buffer control—Indicates the direction of data on the DAL bus. The line is active (low) when the DCJ11 is not driving to the DAL bus.
38	$\overline{\text{SCTL}}$	output[1]	Stretch control—Identifies the extended portion of stretched cycles. The edges can be used to strobe data.
39	$\overline{\text{STRB}}$	output[1]	Strobe—General purpose strobe signal.
29	$\overline{\text{PRDC}}$	output[1]	Predecode strobe—Indicates when the prefetch buffer is being decoded as the next macroinstruction.
20	$\overline{\text{ABORT}}$	input/output[1]	Abort—Indicates that an abort condition exists, i.e., a memory management or address error, bus timeout, nonexistent memory, or parity error.
28	$\overline{\text{MISS}}$	input[1]	Miss—Reports the hit or miss status of the current cache memory entry lookup.
42	DV	input[1]	Data valid—Set to latch data into the DCJ11.
32	$\overline{\text{CONT}}$	input[1]	Continue—Used to terminate all extended cycles.
27	$\overline{\text{DMR}}$	input[1]	Direct memory access request—Used to force a current cycle to be extended.
10-13	IRQ<3:0>	input[1]	Interrupt Request <3:0>—Four maskable interrupt request lines.
9	$\overline{\text{HALT}}$	input[1]	Halt—A low-priority nonmaskable interrupt that forces the system into console mode.
8	$\overline{\text{EVENT}}$	input[1]	Event—A maskable interrupt that forces a trap through vector location 100.

Figure 3 shows the input and output signals grouped according to signal function.

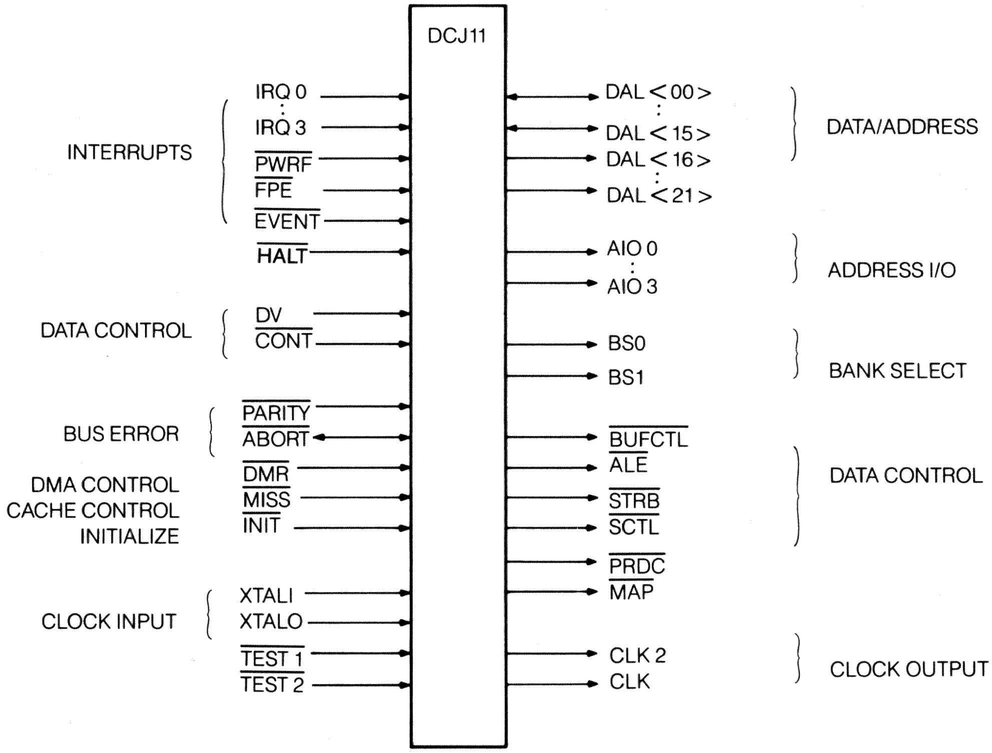


Figure 3 • DCJ11 Signal Functions

Data and Address Bus

Data and address bus (DAL<21:00>)—The data and address bus consists of 22 time-multiplexed data and address lines. The basic bus consists of DAL<15:00> and is bidirectional. The extended bus consists of DAL<21:16> and is used for outputs only. During the first half of each transaction, the DCJ11 provides either a physical address, the acknowledged interrupt level or a general purpose code. The physical address can use all 22 bits of the bus. The acknowledged interrupt level uses DAL<03:00> and the general purpose code uses DAL<07:00>. During the second half of the transaction, the DCJ11 transmits or receives data on the basic bus (DAL<15:00>). The extended bus lines (DAL<21:16>) are driven with test information when the $\overline{\text{BUFCTL}}$ signal is asserted. The data being transmitted or received depends on the type of bus transaction being performed and is described under bus operations.

Memory Management Register 0

The memory management register 0 (MMR0) provides memory management register control and records status. The format of the information in the MMR0 is shown in Figure 14 and the function of the information is described in Table 14.

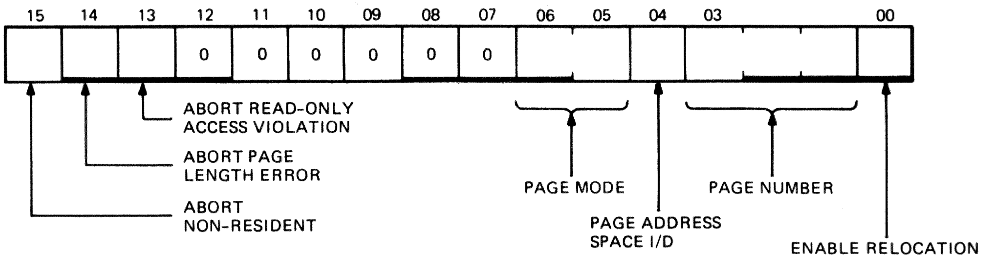


Figure 14 • DCJ11 Memory Management Register 0 Format

Table 14 • DCJ11 Memory Management Register 0 Description

Bits*	Description
15	Abort nonresident—Set by attempting to access a page with an access control field key equal to 0 or 2. It is also set by attempting to use memory relocation with an illegal processor mode (PSR 15:14 = 2).
14	Abort page length error—Set by attempting to access a location in a page with a block number (virtual address bits 12:06) that is outside the area authorized by the page length field of the page descriptor register for that page.
13	Abort read-only access violation—Set by attempting to write in a read-only page. Read-only pages have access keys of 1.
12:07	Not used.
06:05	Processor mode—A read-only bit that indicates the processor mode kernel/supervisor/user/illegal associated with the page causing the abort (kernel = 00, supervisor = 01, user = 11, illegal = 10). If the illegal mode is specified, an abort is generated and bit 15 is set.
04	Page space—A read-only bit that indicates the address space (I or D) associated with the page causing the abort (0 = I space, 1 = D space).
03:01	Page number—Read-only bits that contain the page number of the page causing the abort.
00	Enable relocation—When set, all addresses are relocated. When cleared, memory management is inoperative and addresses are not relocated.

*All bits can be read or written except as indicated.

Interrupts and Traps

The DCJ11 provides a set of trap, hardware, and software interrupt facilities. Four interrupt request lines allow the external hardware to interrupt the processor on four interrupt levels using an externally supplied vector. Eight levels of software interrupt requests are supported through use of the PIRQ register. Internally vectored traps are provided to flag error conditions. Table 17 identifies the DCJ11 asynchronous interrupts. The synchronous interrupts are listed in Table 18. The execution of a HALT instruction may cause different operations depending on the halt options determined during powerup and on the mode of operation.

In kernel mode, a halt option of 1 causes an illegal halt abort if the HALT instruction is executed. Bit 7 of the CPU error register is set and a trap is forced through vector 4. If the halt option is 0, execution of the HALT instruction places the system into console mode. Execution of the HALT instruction in user or supervisor mode causes an illegal halt abort.

The halt line usually has the lowest priority; however, it has highest priority during vector reads. This is to allow the user to break out of potential infinite loops. An infinite loop could occur if a vector has not been properly mapped during memory management operation.

The DCJ11 also responds to conditions that result in an abort of the current operation. Aborts can be generated externally or internally to the DCJ11. During an abort condition, the DCJ11 generates a vector address to select a service routine similar to an interrupt and trap condition. It responds immediately to the abort rather than waiting for the end of the current microcycle. The $\overline{\text{ABORT}}$ signal is asserted during the first half of the stretched cycle to indicate an internal abort condition. The internally and externally generated abort conditions are listed in Table 17.

Table 17 • DCJ11 Asynchronous Interrupts and Traps

Interrupt	Location	Vector Address	Priority Level*
Red stack trap (CPU error register bit 02)[1]	Internal	4	NM
Address error (CPU error register bit 06)[1]	Internal	4	NM
Memory management violation (MMR0 bits 13:15)[1]	Internal	250	NM
Timeout/nonexistent memory (CPU error register bits 04,05)[1]	Internal	4	NM
Parity error ($\overline{\text{PARITY}}$, $\overline{\text{ABORT}}$)[2]	External	114	NM
Trace (T bit) Trap (PSW bit 04)	Internal	14	NM
Yellow stack trap (CPU error register bit 03)	Internal 4	NM	
Powerfail (PWRF)	External	24	NM
FP exception (FPE)	External	244	NM
PIR 7 (PIRQ bit 15)	Internal	240	7
IRQ 7	External	User-defined	7

Interrupt	Location	Vector Address	Priority Level*
PIR 6 (PIRQ bit 14)	Internal	240	7
EVENT	External	100	6
IRQ 6	External	User-defined	6
PIR 5 (PIRQ bit 13)	Internal	240	5
IRQ 5	External	User-defined	5
PIR 5 (PIRQ bit 12)	Internal	240	4
IRQ 4	External	User-defined	4
PIR 3 (PIRQ bit 11)	Internal	240	3
PIR 2 (PIRQ bit 10)	Internal	240	2
PIR 1 (PIRQ bit 09)	Internal	240	1
Halt line (HALT)	External	None—Places system in console mode.	

*NM = Nonmaskable
[1] = ABORT
[2] = INTERRUPT or ABORT

Table 18 • DCJ11 Synchronous Interrupts

Interrupt	Vector Address
Memory Management	250
FP instruction exception (FPS bits 11:08,15)	244
PIRQ	240
Memory Parity Error	114
TRAP (trap instruction)	34
EMT (emulator trap instruction)	30
IOT (I/O trap instruction)	20
BPT (breakpoint trap instruction)	14
Timeout and reserved instruction	4

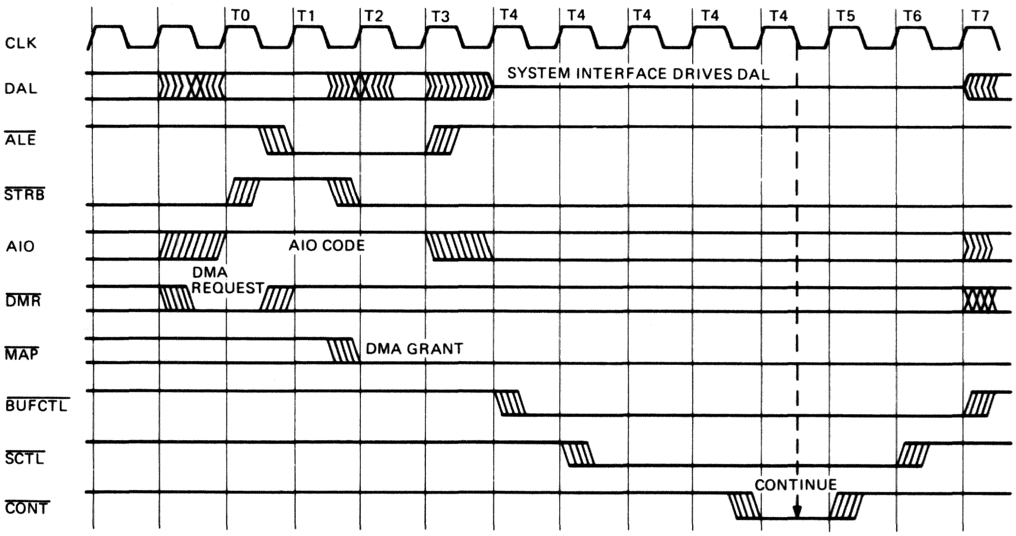


Figure 18 ▪ DCJ11 Stretched Non-I/O Timing Sequence

Bus Read Transaction

A bus read transaction shown in Figure 19 uses the DAL bus to read information from memory, I/O, and other addressable registers. These transactions may be instruction stream read, data stream read, or the read portions of read-modify-write. The type of read transaction being performed is identified by the AIO code. The DCJ11 reads words and if a byte is required, the complete word is read and the excess byte is ignored.

The DCJ11 reports memory management or address errors on the $\overline{\text{ABORT}}$ output during the nonstretched portion of the transaction. If the $\overline{\text{ABORT}}$ signal is asserted, the information on DAL, BS<1:0>, and $\overline{\text{MAP}}$ lines should be ignored and the bus transaction should not be started.

The read transaction is initiated by the assertion of $\overline{\text{ALE}}$. This signal latches the AIO code, the physical address on DAL bus, the BS<1:0>, and the $\overline{\text{MAP}}$ (I/O map enable) signal. The DCJ11 latches the data on the rising edge of the T3 during a nonstretched transaction. A bus read is completed in four periods when all of the following conditions exist.

- BS<1:0> set to zeros (memory reference)
- No cache bypass
- No cache force miss
- No DMA grant
- No abort during a demand read
- No cache miss reported on MISS

DMA Request and Grant Transaction

When the external system requests the use of the DAL bus or wants to stall the DCJ11, it asserts the $\overline{\text{DMR}}$ input. This disables the DCJ11 from the DAL bus and causes a stretched transaction. The DMR input is acknowledged after the I/O map information is on the $\overline{\text{MAP}}$ output. The $\overline{\text{DMR}}$ input is the DMA request and the $\overline{\text{MAP}}$ output is the DMA grant. These signals should be recognized during NOP or read transactions. The write transactions stretch beyond four periods and the DAL bus may contain write data. The DMA transfer stretches the transaction beyond eight periods by two period increments, until the DCJ11 receives the $\overline{\text{CONT}}$ signal to end the transaction.

Interrupt Acknowledge

The interrupt acknowledge transaction is used to acknowledge an interrupt request received through the IRQ<3:0> inputs. The vector address specified can be an internal predesignated address or an external address received on the DAL bus. The decoded interrupt level acknowledged is sent on the DAL<03:00> lines at the beginning of the transaction. The DAL<21:16> lines are set to one and DAL bits <15:04> are set to zero.

The interrupt acknowledge transaction shown in Figure 24, is initiated by the assertion of the $\overline{\text{ALE}}$ line that latches the AIO code and the acknowledged interrupt level. The transaction requires eight periods to read the vector address and can be stretched in two-period increments until the $\overline{\text{CONT}}$ input is asserted. The DV input is asserted to latch the interrupt vector address while the $\overline{\text{SCTL}}$ signal is asserted. An interrupt acknowledge cycle can be aborted during the stretched part of the cycle if the $\overline{\text{ABORT}}$ signal is asserted by external logic. The DCJ11 does not assert $\overline{\text{ABORT}}$ during the first part of the interrupt acknowledge cycle. If the abort occurs, the DCJ11 ignores the interrupt request and continues executing.

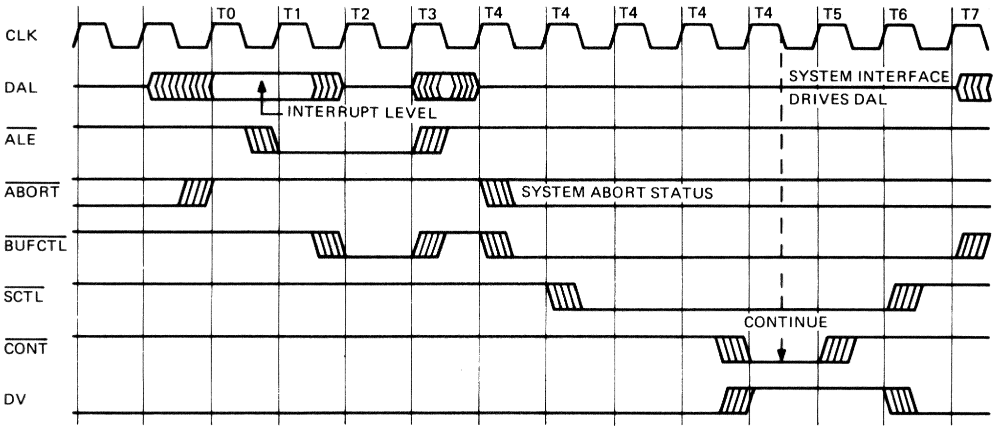


Figure 24 • Interrupt Acknowledge Cycle Timing Sequence

Table 31 • DCJ11 dc Input and Output Parameters

Symbol	Parameter	Test Condition	Requirements Min.	Requirements Max.	Units	Test Circuit
V_{IH}	High-level MOS input		70% V_{CC}	—	V	C1,C2
V_{IL}	Low-level MOS input		—	30% V_{CC}	V	C1,C2
V_{IHT}	High-level TTL input		2.2	—	V	C1,C2
V_{ILT}	Low-level TTL input		—	0.6	V	C1,C2
I_I	Input-leakage current non-Test inputs	$0\ V \eqslantless VI \eqslantless V_{CC}$ $V_{CC} = 5.25\ V$	−10	10	µA	C3,C4
I_{ILL}	Input current Test inputs	$V_{IN} = 0\ V$ $V_{CC} = 5.25\ V$	0.1	5.0	mA	C5
I_{OH}	Output current at high level	$V_{OUT} = V_{CC} -0.4\ V$	—	-2.0	mA	C1
I_{OL}	Output current at low level	$V_{OUT} = 0.4\ V$	2.0	—	mA	C1,C2
I_{OHT}	Output current at high TTL level	$V_{OUT} = 2.4\ V$	-2.0	—	mA	C2
I_{OSH}	High level sustainer current	$V_{OUT} = V_{CC} -1.0\ V$ $V_{CC} = 5.25\ V$	-0.2	-0.6	mA	C6
I_{OSL}	Low level sustainer current	$V_{OUT} = 1.0\ V$ $V_{CC} = 5.25\ V$	0.2	0.6	mA	C6
I_{OZ}	Output leakage current[1]	$0\ V \eqslantless VO \eqslantless V_{CC}$ $V_{CC} = 5.25\ V$	-10.0	10.0	µA	C8,C9
I_{CCSB}	Static power supply current[2]	$V_{CC} = 5.25\ V$	—	20.0	mA	C7
C_{in}	Input only capacitance[3]		—	7.0	pF	

Symbol	Parameter	Test Condition	Requirements		Units	Test Circuit
			Min.	Max.		
C_{IO}	Input/output capacitance[3]		—	15	pF	
C_{out}	Output capacitance[3]		—	15	pF	
C_{max}	DCJ11 capacitance plus external capacitance		—	100	pF	

[1] Applies only in the high-impedance condition.
[2] With $\overline{\text{TEST1}}$, $\overline{\text{TEST2}}$, and all outputs open circuit. All other inputs equal to V_{CC}.
[3] Sampled and guaranteed, but not tested. Does not apply to $\overline{\text{TEST1}}$ or $\overline{\text{TEST2}}$.

Table 32 • DCJ11 dc Signal Test Summary

Type	Name	Applicable dc Test
TTL input	IRQ<3:1>, $\overline{\text{HALT}}$, $\overline{\text{PWRF}}$, $\overline{\text{EVENT}}$, $\overline{\text{PARITY}}$ DV, $\overline{\text{MISS}}$, $\overline{\text{CONT}}$, $\overline{\text{DMR}}$, $\overline{\text{INIT}}$ and $\overline{\text{FPE}}$	V_{IHT}, V_{ILT}, I_I
TTL output	DAL<21:16>, AIO<3:0>, $\overline{\text{ALE}}$, $\overline{\text{BUFCTL}}$, $\overline{\text{SCTL}}$, $\overline{\text{STRB}}$, BS<1:0>, $\overline{\text{MAP}}$, and $\overline{\text{PRDC}}$	I_{OL}, I_{OHT}, I_{OZ}
MOS input	$\overline{\text{TEST1}}$ and $\overline{\text{TEST2}}$	V_{IH}, T_{IL}, I_{ILL}
MOS output	CLK and CLK2	I_{OH}, I_{OL}, I_{OZ}
TTL I/O	$\overline{\text{ABORT}}$*	V_{ILT}, I_{OL}, I_{OHT}, I_{OZ}, I_{OSH}
TTL I/O	DAL<15:00>	V_{IHT}, V_{ILT}, I_{OL}, I_{OHT}, I_{OZ}
Power	V_{CC}	I_{CCSB}

*$\overline{\text{ABORT}}$ must be driven with an open-collector driver because the DCJ11 has a pullup device that supplies I_{OSH}.

ac Electrical Characteristics

The timing references and signal parameters of the DCJ11 are shown in the following figures and tables. Figure 30 shows the input and output voltage waveform characteristics. The test conditions used to perform the ac measurements follow: Figure 33 shows the output load circuits referenced on the tables and used to perform the output measurements.

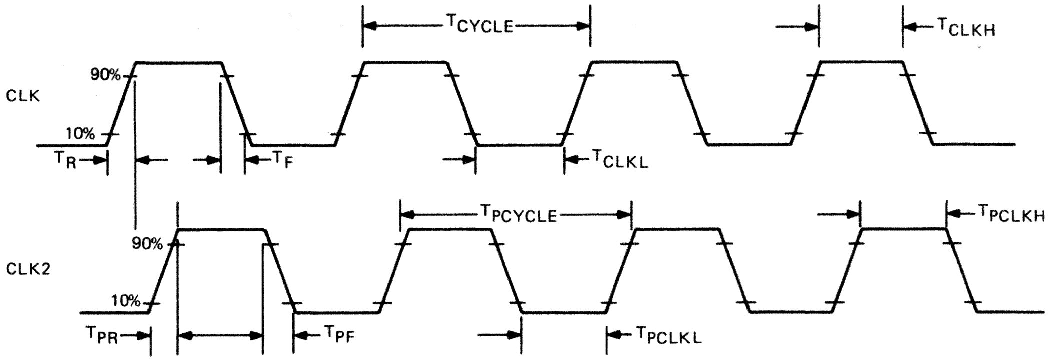


Figure 33 • DCJ11 Clock Output Timing Waveforms

Table 33 • DCJ11 Clock Output Timing Parameters

Symbol	Parameter	Requirements (ns) 15 MHz Min.	Max.	18 MHz Min.	Max.	Load Circuit[1]
t_{INITW}	$\overline{\text{INIT}}$ pulse width	10-clock periods	—	10-clock periods	—	
t_{SCTLLH}	Initialization interval	300	—	250	—	
t_{CYCLE}	CLK cycle time	67	—	55	—	Load C
t_{CLKH}	CLK high width	28	—	24	—	Load C
t_{CLKL}	CLK low width	28	—	24	—	Load C
t_R	CLK rise time	—	7	—	7	Load C
t_F	CLK fall time	—	7	—	7	Load C
t_{PCYCLE}	CLK2 cycle time	67	—	55	—	Load B
t_{PCLKH}	CLK2 high width	28	—	24	—	Load B
t_{PCLKL}	CLK2 low width	28	—	24	—	Load B
t_{PR}	CLK2 rise time	—	7	—	7	Load B
t_{PF}	CLK2 fall time	—	7	—	7	Load B

[1] Refer to Figure 31 for output load circuits used for the timing measurements.

Table 34 • DCJ11 Nonstretched Bus Read Timing Parameters

Symbol	Parameter	Requirements (ns) 15 MHz Min.	 Max.	 18 MHz Min.	 Max.	Reference	Load Circuit[1]
t_{AIOD}	AIO<3:0> delay	—	100	—	82	T−1.5	Load B
t_{DALD}	DAL valid delay	—	65	—	55	T−1, T1.5	Load B
t_{DALH}	DAL valid hold	5	—	5	—	T1.5, T3	Load B
t_{DIS}	DAL output disable	—	35	—	25	T1.5	Load A
t_{DMRS}	$\overline{\text{DMR}}$ setup[2]	30	—	20	—	T0	
t_{DMRH}	$\overline{\text{DMR}}$ hold[2]	20	—	20	—	T0	
t_{DS}	DAL<15:00> setup	35	—	20	—	T3	
t_{DH}	DAL<15:00> hold	5	—	10	—	T3	
t_{HMS}	MISS setup	30	—	20	—	T3	
t_{HMH}	MISS hold	10	—	10	—	T3	
t_{PD}	PRDC valid delay	—	50	—	50	T0	Load B
t_{PID}	PRDC inactive delay	—	50	—	50	T2	Load B
t_{SD}	Strobe active delay	0	35	0	35	Table 38	Load B
t_{SID}	Strobe inactive delay	0	35	0	35	Table 38	Load B

[1] Refer to Figure 31 for output load circuits used for the timing measurements.

[2] The setup and hold signal requirements ensure the recognition of the next sample point.

Table 35 • DCJ11 Stretched Bus Read and Write Timing Parameters

Symbol	Parameter	Requirements (ns)				Reference	Load Circuit[1]
		15 MHz		18 MHz			
		Min.	Max.	Min.	Max.		
t_{AIOD}	AIO<3:0> delay	—	75	—	82	T−1.5	Load B
t_{CNTS}	$\overline{\text{CONT}}$ setup[2]	30	—	20	—	T−3.5	
t_{CNTH}	$\overline{\text{CONT}}$ hold[2]	20	—	20	—	T−3.5	
t_{DALD}	DAL valid delay	—	65	—	55	T−1, T1.5	Load B
t_{DALH}	DAL valid hold	5	—	5	—	T 1.5, T3	Load B
t_{DIS}	DAL output disable	—	35	—	25	T 1.5, T4	Load A
t_{DMRS}	$\overline{\text{DMR}}$ setup[2]	30	—	20	—	T0	
t_{DMRH}	$\overline{\text{DMR}}$ hold[2]	20	—	20	—	T0	
t_{DVDH}	DAL<15:00> hold	35	—	25	—	DV deassert	
t_{DVDS}	DAL<15:00> setup	35	—	25	—	DV deassert	
t_{DVF}	DV fall time	—	15	—	15		
t_{DVH}	DV deassertion	—	0	—	0	T6.5	
t_{DVS}	DV deassertion	0	—	0	—	T4	
t_{DVW}	DV pulse width	35	—	25	—		
t_{PD}	$\overline{\text{PRDC}}$ valid delay	—	50	—	50	T0	Load B
t_{PID}	$\overline{\text{PRDC}}$ inactive delay	—	50	—	50	T2	Load B
t_{SD}	Strobe active delay	0	35	—	35	Table 38	Load B
t_{SID}	Strobe inactive delay	0	35	—	35	Table 38	Load B

[1] Refer to Figure 31 for output load circuits used for the timing measurements.

[2] The setup and hold signal requirements ensure the recognition of the next sample point.

Table 36 • DCJ11 GP Read and Write Timing Parameters

Symbol	Parameter	Requirements (ns)				Reference	Load Circuit[1]
		15 MHz		18 MHz			
		Min.	Max.	Min.	Max.		
t_{ABD}	$\overline{\text{ABORT}}$ delay	0	—	0	—		
t_{ABS}	$\overline{\text{ABORT}}$ drive	30	—	20	—	T–2.5	
t_{ABW}	$\overline{\text{ABORT}}$ width	$40 + t_{CLKH}$	—	$40 + t_{CLKH}$	—		
t_{AIOD}	AIO<3:0> delay	—	100	—	82	T–1.5	Load B
t_{CNTS}	$\overline{\text{CONT}}$ setup[2]	30	—	20	—	T–3.5	
t_{CNTH}	$\overline{\text{CONT}}$ hold	20	—	20	—	T–3.5	
t_{DALD}	DAL valid delay	—	65	—	55	T–1, T1.5	Load B
t_{DALH}	DAL valid hold	5	—	5	—	T1.5, T3	Load B
t_{DH}	DAL<15:00> hold	5	—	10	—	T3	
t_{DIS}	DAL output disable	—	35	25	—	T1.5, T4	Load A
t_{DMRS}	$\overline{\text{DMR}}$ setup[2]	30	—	20	—	T0	
t_{DMRH}	$\overline{\text{DMR}}$ hold[2]	20	—	20	—	T0	
t_{DS}	DAL<15:00> setup	35	—	20	—	T3	
t_{DVDH}	DAL<15:00> hold	35	—	25	—	DV deassert	
t_{DVDS}	DAL<15:00> setup	35	—	25	—	DV deassert	
t_{DVF}	DV fall time	—	15	—	15		
t_{DVH}	DV deassertion	—	0	—	0	T6.5	
t_{DVS}	DV deassertion	0	—	0	—	T4	
t_{DVW}	DV pulse width	35	—	25	—		
t_{HMS}	$\overline{\text{MISS}}$ setup	30	—	20	—	T3	
t_{HMH}	$\overline{\text{MISS}}$ hold	10	—	10	—	T3	
t_{PD}	$\overline{\text{PRDC}}$ valid delay	—	50	—	50	T0	Load B
t_{PID}	$\overline{\text{PRDC}}$ inactive delay	—	50	—	50	T2	Load B
t_{SD}	Strobe active delay	0	35	0	35	Table 38	Load B
t_{SID}	Strobe inactive delay	0	35	0	35	Table 38	Load B

[1] Refer to Figure 31 for output load circuits used for the timing measurements.

[2] The setup and hold signal requirements ensure the recognition of the next sample point.

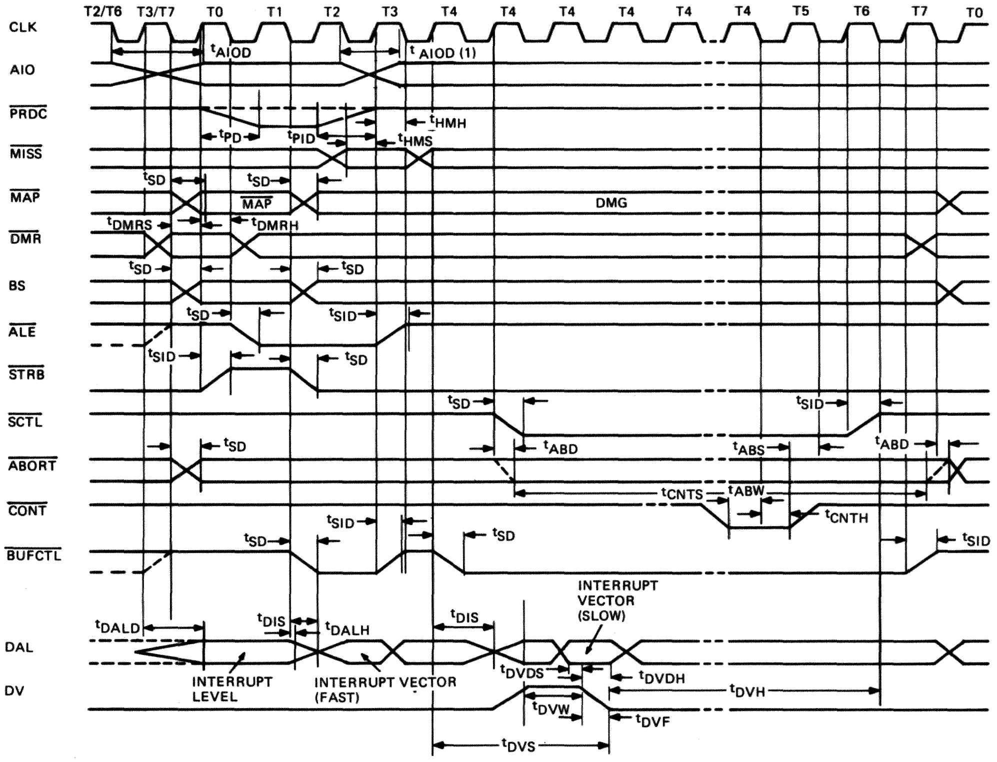


Figure 39 ▪ DCJ11 Interrupt Acknowledge Timing Sequence

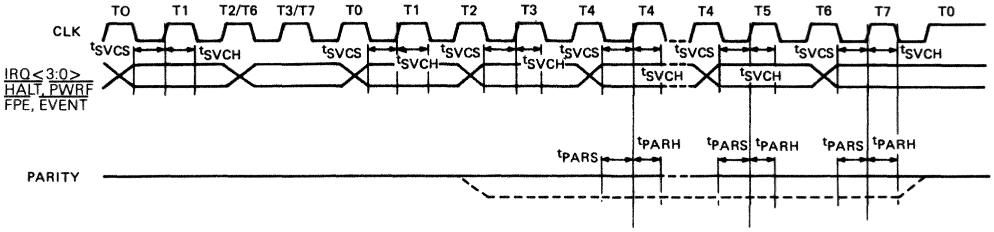


Figure 40 ▪ DCJ11 Interrupt Timing Sequence

Table 37 • DCJ11 Interrupt and Acknowledge Timing Parameters

Symbol	Parameter	Requirements (ns)				Reference	Load Circuit[1]
		15 MHz		18 MHz			
		Min.	Max.	Min.	Max.		
t_{ABD}	$\overline{\text{ABORT}}$ delay	0	—	0	—		
t_{ABS}	$\overline{\text{ABORT}}$ drive	30	—	20	—	T–2.5	
t_{ABW}	$\overline{\text{ABORT}}$ width	$40+t_{CLKH}$	—	$40+t_{CLKH}$	—		
t_{AIOD}	AIO<3:0> delay	—	100	—	82	T–1.5	Load B
t_{CNTS}	$\overline{\text{CONT}}$ setup[2]	30	—	20	—	T–3.5	
t_{CNTH}	$\overline{\text{CONT}}$ hold	20	—	20	—	T–3.5	
t_{DALD}	DAL valid delay	—	65	—	55	T–1, T1.5	Load B
t_{DALH}	DAL valid hold	5	—	5	—	T1.5, T3	Load B
t_{DIS}	DAL output disable	—	35	—	25	T1.5, T4	Load A
t_{DMRS}	$\overline{\text{DMR}}$ setup[2]	30	—	20	—	T0	
t_{DMRH}	$\overline{\text{DMR}}$ hold[2]	20	—	20	—	T0	
t_{DS}	DAL<15:00> setup	35	—	20	—	T3	
t_{DVDH}	DAL<15:00> hold	35	—	25	—	DV deassert	
t_{DVDS}	DAL<15:00> setup	35	—	25	—	DV deassert	
t_{DVF}	DV fall time	—	15	—	15		
t_{DVH}	DV deassertion	—	0	—	0	T6.5	
t_{DVS}	DV deassertion	—	—	0	—	T4	
t_{DVW}	DV pulse width	35	—	25	—		
t_{HMS}	$\overline{\text{MISS}}$ setup	30	—	20	—	T3	
t_{HMH}	$\overline{\text{MISS}}$ hold	10	—	10	—	T3	
t_{PARS}	$\overline{\text{PARITY}}$ setup	20	—	22	—	Figure 39	
t_{PARH}	$\overline{\text{PARITY}}$ hold[2]	20	—	22	—	Figure 39	
				—	50	T0	Load B
					50	T2	Load B
t_{SD}	Strobe active delay	0	35	0	35	Table 38	Load B
t_{SID}	Strobe inactive delay	0	35	0	35	Table 38	Load B

Symbol	Parameter	Requirements 15 MHz Min.	Max.	18 MHz Min.	Max.	Reference	Load Circuit[1]
t_{SVCS}	IRQ<3:0>, $\overline{\text{HALT}}$, $\overline{\text{PWRF}}$, $\overline{\text{FPE}}$, $\overline{\text{EVENT}}$ setup[2]	20	—	22	—	Figure 40	
t_{SVCH}	IRQ<3:0>, $\overline{\text{HALT}}$, $\overline{\text{PWRF}}$, $\overline{\text{FPE}}$, $\overline{\text{EVENT}}$ hold[2]	20	—	22	—	Figure 40	

[1] Refer to Figure 31 for output load circuits used for the timing measurements.

[2] The setup and hold signal requirements ensure the recognition of the next sample point.

Table 38 • DCJ11 t_{SD} and t_{SID} Parameter References

Signal	t_{SD} Reference Edge	t_{SID} Reference Edge
$\overline{\text{ALE}}$	T0.5	T3
$\overline{\text{STRB}}$	T1.5	T0
$\overline{\text{BUFCTL}}$	T1.5, first T4	T3, T-1
$\overline{\text{SCTL}}$	Second T4 or T5	T-2
BS	T-0.5, T1	
$\overline{\text{MAP}}$	T1.5	
$\overline{\text{ABORT}}$	T-0.5	

DC319-AA DL11 Compatible Asynchronous Receiver/Transmitter

• Features

- Hardware compatible with Digital's DL11 series of interfaces
- Asynchronous operation
- Overrun and framing error detection and break detection
- Compatible with both 8- and 16-bit data paths
- Internal baud rate generation from 300 baud to 38.4k baud
- Four realtime clock interrupt outputs.
- One stop bit only
- Common baud rate for both transmitter and receiver
- Single 5-volt power supply
- Single TTL clock

• Desciption

The DC319-AA is a Digital Link (DL11) compatible, asynchronous receiver/transmitter (DLART) designed for data communication between Digital's microprocessors and console terminals or communication devices. The DC319-AA, fabricated using N-channel MOS silicon technology, is contained in a 40-pin dual-inline (DIP) package that can be conveniently installed on a microprocessor module or interface module. Figure 1 is a block diagram of the DC319-AA DLART.

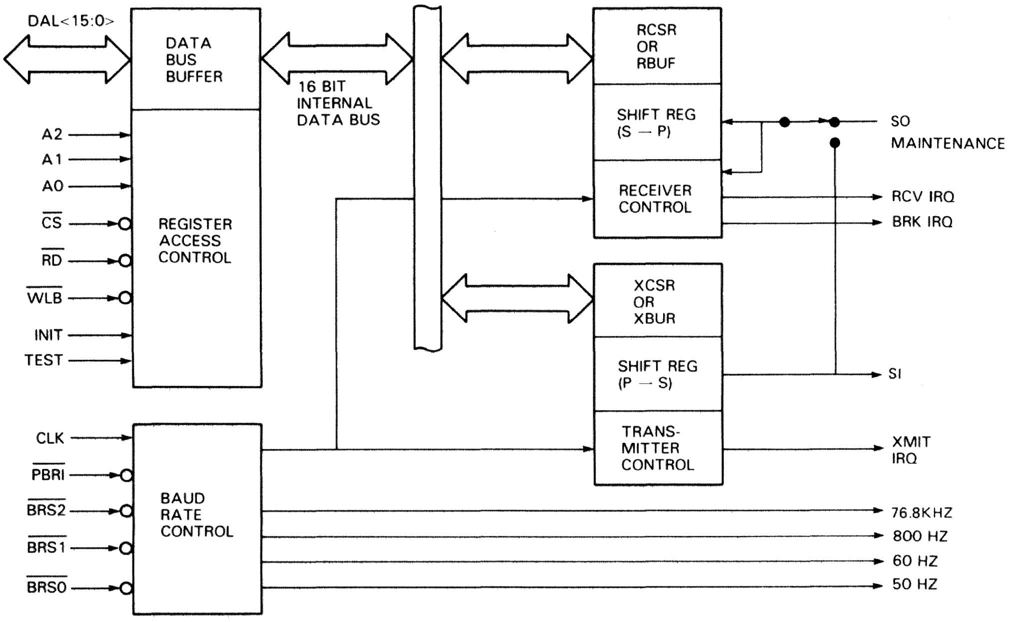


Figure 1 • DC319-AA DLART Block Diagram

Chipkit Description—The following LSI-11 chipkits are available and contain the components listed.

- DCK11-AA Program Control Bus Interface Chipkit
  - 1 DC003 Dual-interrupt Logic
  - 1 DC004 Register Selector Logic
  - 4 DC005 4-bit Transceiver Logic

- DCK11-AB Designer's Program Control Bus Interface Chipkit
  - 1 DC003 Dual-interrupt Logic
  - 1 DC004 Register Selector Logic
  - 4 DC005 4-bit Transceiver Logic
  - 1 W9512 Double-height, wire-wrappable module
  - 1 BC07-D 10-foot, 40-conductor, plug-in cable

- DCK11-AC DMA Bus Interface Chipkit
  - 1 DC003 Dual-interrupt Logic
  - 1 DC004 Register Selector Logic
  - 4 DC005 4-bit Transceiver Logic
  - 2 DC006 Word count/Bus Address Logic
  - 1 DC010 Direct Memory Access Logic
  - 1 W9512 Double-height, wire-wrappable module

- DCK11-AD Designer's DMA Bus Interface Chipkit
  - 1 DC003 Dual-interrupt Logic
  - 1 DC004 Register Selector Logic
  - 4 DC005 4-bit Transceiver Logic
  - 2 DC006 Word Count/Bus Address Logic
  - 1 DC010 Direct Memory Access Logic
  - 1 W9512 Double-height, wire-wrappable module
  - 1 BC07-D 10-foot, 40-conductor, plug-in cable

UNIBUS Devices

The UNIBUS is an asynchronous bus used with the PDP-11 and VAX processors. The UNIBUS devices facilitate the development of the bus interfaces.

DC013 UNIBUS Request Logic—The DC013 is a 16-pin DIP device that contains the logic required to perform bus requests and to gain control of the UNIBUS.

DC021 Octal Bus Transceiver—The DC021 is a 20-pin DIP device that contains eight bus transceivers used to transfer information between the UNIBUS and a user-developed interface.

Pin	Signal	Input/Output	Definition/Function
D12	$\overline{\text{II PBAD}}$	output	II Parity bad—Indicates that the parity is not valid during data transfers to and from the BIIC.
J14	$\overline{\text{II DMA PGOVF}}$	output	II DMA page overflow—Indicates that the DMA address register is full.
J13	$\overline{\text{II MAP PGOFV}}$	output	II Map page overflow—Indicates that the MAP address register is full.
N14	$\overline{\text{II DMA INC ENA}}$	input	II DMA increment enable—Allows the masterport DMA address register to be incremented.
M13	$\overline{\text{II MAP INC ENA}}$	input	II Map increment enable—Allows the masterport map address register to be incremented.
L3,C10,A14,M11	V_{CC}	input	Voltage—Power supply voltage.
P1,C12	V_{BB}	output	Voltage—Back-bias voltage.
C4,C7,C8,F3 G3,J3,K3,K12, K14,L12,M7,M8, N12	GND	input	Ground—Ground reference.

II Data (II D<31:00>)—Bidirectional data lines that connect to a transparent input latch. The latch is controlled by the $\overline{\text{II DS}}$ signal. The three-state drivers are enabled by the $\overline{\text{II OE}}$ input.

II Parity (II P<3:0>)—Parity bits associated with each of the four bytes on the II D<31:00> lines. Valid byte parity must be generated by the user and loaded into the BCAI on lines II P<3:0> when transferring data, addresses, or command/mask/status information into the BCAI. When loading 4-bit command/mask/status information, the parity generated must be for the complete byte, including the zeros in the unimplemented portion of the byte. The BCAI also generates parity for data loaded into the BCAI from the BIIC and compares the parity it generates to the BCI P0 bit. The $\overline{\text{II PBAD}}$ line is set if an error is detected regardless of the direction of data flow. The II parity bits are latched with the II D<31:00> information by $\overline{\text{II DS}}$ signal and enabled by $\overline{\text{II OE}}$ signal.

II Data Strobe ($\overline{\textbf{II DS}}$)—This signal controls the transparent latches for the II D<31:00> input data. The input latch is transparent when the $\overline{\text{II DS}}$ input is asserted and the information is latched when the signal is deasserted.

II Output Enable ($\overline{\textbf{II OE}}$)—Controls the output drivers for the II D>31:00> and II P<3:0> lines. When $\overline{\text{II OE}}$ is asserted, the contents of the II D<31:00> output latch are transferred to the II D<31:00> data bus. When it is deasserted, the II D<31:00> lines become a high-impedance state. Line $\overline{\text{II OE}}$ has a 50-μA pullup circuit so that if the pin is not connected, it will remain deasserted.

II Mask (II M<3:0>)—Controls the ability to perform an II operation to individual byte fields. When the selected II M<3:0> lines are deasserted, an II bus write operation for the corresponding byte field is suppressed and an II read operation returns all zeros including the parity bit. The mask information is latched by the assertion of the $\overline{\text{II AS}}$ line. Table 2 lists the II bus interface mask bit assignments.

Table 2 • VAXBI 78743 II Bus Mask Bit Assignments

II Mask lines*				Valid data	Valid parity
3	2	1	0		
1	1	1	1	II D<31:00>	II P<3:0>
0	0	0	1	II D<07:00>	II P0
0	0	1	0	II D<15:08>	II P1
0	1	0	0	II D<23:16>	II P2
1	0	0	0	II D<31:24>	II P3

*All other input combinations that specify the validity of the bytes on the II D<31:00> lines are allowed.

II Address (II A<6:0>)—Controls the selection of the internal registers in the register file. Refer to Figure 4 for the hexadecimal address values assigned to the registers. The II A<6:2> signals pass through a transparent latch controlled by $\overline{\text{II AS}}$ input and may be used in a latched or unlatched mode. Lines II A<6:2> are used to select the primary longword register being accessed and lines II A<1:0> control the byte offset multiplexers attached to the internal registers as listed in Table 3.

Table 3 • VAXBI 78743 Byte Offset

II A line*		Byte offset
1	0	
L	L	none
L	H	1
H	L	2
H	H	3

*H = high level, L = low level.

For registers within the dual octaword buffer, the bytes that extend beyond the primary longword register are contained in the next adjacent register (A<6:2> + 1) except when II A <6:2> = 00111. When the exception exists, the primary longword register is at the bottom of the buffer and the offset is transferred to the longword register addressed by 00000. For registers not in the dual octaword buffer, the bytes that are offset beyond the primary longword register are not written during write operations and are returned as all zeros on read operations.

II Address Strobe (II AS)—Controls the transparent latch for the II A<6:0> data and mask bits II M<3:0>. The input latch is transparent when $\overline{\text{II AS}}$ is asserted and latched when deasserted.

II Write Strobe (II WS)—Controls the writing of the internal register file. The input data from the transparent latches on lines II D<31:00> is loaded into the selected register during assertion of the $\overline{\text{II WR}}$ strobe. The deassertion of the selected II M<3:0> lines will inhibit the write operation for the corresponding byte field. When accessing the DMA octaword data buffers, the byte valid bit for the addressed location is set when its byte is written.

II Read Strobe (II RS)—Controls the read operations for the II bus port of the register file. The read operation is initiated when the $\overline{\text{II RS}}$ line is asserted and the resulting output data is held in the II D<31:00> output latch when the $\overline{\text{II RS}}$ signal is deasserted. Deassertion of the selected II M<3:0> lines will inhibit the read operation for the corresponding byte field.

II Clear Valid Byte (II CLRVB)—This signal is used to clear all the master port Byte Valid bits associated with the dual octaword buffer.

II Parity Select (II PSEL) – Selects which source of parity (user supplied or internally generated) is passed to BCI PO output when data is transferred to the BIIC. A low level selects user parity and makes the errors within the processor bus interface or the BCAI visible to the VAXBI bus. A high level selects the internal parity that always provides correct parity for the data being passed to the BCI bus. This signal is latched by the BCI AS line. If internal parity is selected and errors on the II bus cause bad parity, the PBAD line will be asserted when data is transferred from the BCAI to the BIIC even when good parity is indicated for the transfer from the BCAI to the BIIC.

II Parity Bad (II PBAD)—When set, it indicates one of two conditions:

- When transmitting data to the BIIC, the result of the internal parity generation from the BCI D<31:00> and BCI I<3:0> lines for this cycle do not agree with the parity bits associated with the 5 bytes being transmitted.
- When receiving data from the BIIC, the BCI PO line from the BIIC does not agree with the internal parity generated from the 5 bytes being received on the BCI D<31:00> and BCI I<3:0> lines.

II DMA Page Overflow (II DMA PGOVF)—Asserted to indicate that the DMA address register has reached the boundary of a 512-byte page.

II MAP Page Overflow (II MAP PGOFV)—Asserted to indicate that the MAP address register has reached the boundary of a 512-byte page.

II DMA Increment Enable (II DMA INC ENA)—Enables the low-order 9 bits of the master port DMA address register to be incremented by a value of 4, 8, or 16 as specified by the length field (bits 31:30 of the DMA address register) whenever the master port DMA address register is accessed by a BCI read operation.

II Map Increment Enable (II MAP INC ENA)—Enables the low-order 9 bits of the master port map address register to be incremented by a value of 4, 8, or 16 as specified by the length field (bits 31:30) of the map address register when the master port map address register is accessed by a BCI read operation.

BCI Bus Signals

Table 4 is a summary of the BCI bus signals that connect the BCAI to the BIIC interface. The signal functions are described in the paragraphs that follow.

Table 4 • VAXBI 78743 BCI Bus Interface Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
C2,D3,A1,C3, B2,A2,C5,B3, A3,B4,A4,B5, A5,C6,B6,A6, A7,B7,B8,A8, A9,B9,A10,A11, C9,B10,A12,B11, A13,B12,C11,B13	BCI D<31:00>	input/output	BCI Data <31:00>—Data lines that transfer data between the BCIA and the BIIC interface.

Pin	Signal	Input/Output	Definition/Function
E14,F13,D14, F12	BCI I<3:0>	input/output	BCI Information <3:0>—Information lines used to transfer command, mask, and status information between the BCAI and BIIC interface.
E13	BCI PO	input/output	BCI Parity—A parity indicator from the BIIC when data is received and to the BIIC when data is transferred to the the BIIC.
F14	$\overline{\text{BCI DS}}$	input	BCI Data strobe—Loads the information on the BCI D<31:00> and BCI I<3:0> lines into the BCAI.
D1,E3,C1,D2	BCI A<3:0>	input	BCI Address—Controls the selection of the internal registers in the register file.
E2	$\overline{\text{BCI AS}}$	input	BCI Address strobe—Controls the loading of the A<3:0> input information from the BIIC.
H12	$\overline{\text{BCI WS}}$	input	BCI Write strobe—Controls the writing or from the BIIC to the register file.
H13	$\overline{\text{BCI ENA WS}}$	input	BCI Enable write strobe—Enables the $\overline{\text{BCI WS}}$ input to the BCAI.
H14	$\overline{\text{BCI RS}}$	input	BCI Read strobe—Controls the read operation of the register file from the BIIC.
G14	$\overline{\text{BCI ENA RS}}$	input	BCI Enable read strobe—Enables the operation of the $\overline{\text{BCI RS}}$ signal from the BIIC.
C13	$\overline{\text{BCI ENA MLS}}$	input	BCI Enable A master latch strobe—Enables the operation of the $\overline{\text{BCI RS}}$ signal input from the BIIC.
B14	$\overline{\text{BCI ENB MLS}}$	input	BCI Enable B master latch strobe—Enables the operation of the $\overline{\text{BCI RS}}$ signal input from the BIIC.
E12	$\overline{\text{BCI MLS}}$	input	BCI Master latch strobe—Controls the operation of the transparent output register.
C14	$\overline{\text{BCI SLS}}$	input	BCI Slave latch strobe—Controls the transfer of information on the BCI D<31:00> and BCI I<3:0> lines to the BIIC.
D13	$\overline{\text{BCI ENA SLS}}$	input	BCI Enable slave latch strobe—Enables the operation of the $\overline{\text{BCI SLS}}$ input from the BIIC.
G12	$\overline{\text{BCI MDE}}$	input	BCI Master data enable–Controls the master output data from the BCAI to the BIIC.

Pin	Signal	Input/Output	Definition/Function
G13	BCI SDE	input	BCI Slave data enable—Controls the transfer of the slave data from the BCAI to the BIIC.

BCI Data (BCI D<31:00>)—Bidirectional data lines with a transparent input latch and two output latches. The input latch is controlled by the BCI DS line. The transmitters for the output latches are controlled by BCI MDE for the master data output latch and by the BCI SDE input for the slave data output latch.

BCI Information (BCI I<3:0>)—These lines are used to transfer SCMD, DCMD, and MCMD commands, mask, and status information to and from the BIIC. The lines are latched and enabled by the same signals as the BCI D<31:00> lines.

BCI Parity (BCI PO)—This bidirectional line receives the parity information when receiving data from the BIIC and it is compared to the parity from the internal parity generator. Internal parity is generated when the BCI D<31:00> and BCI I<3:0> lines are latched. When transmitting data, this line supplies user parity or internal parity, as selected by line II PSEL. If internal parity does not agree with externally supplied parity in either direction, the II PBAD line is asserted. The BCI PO information is latched and enabled the same as the BCI D<31:00> lines.

BCI Data Strobe (BCI DS)—Controls the transparent input latch for BCI D<31:00>, BCI I<3:0>, and BCI PO input data. The input latch is transparent when BCI DS is asserted and the information is latched when it is deasserted.

BCI Address (BCI A<3:0>)—Controls the selection of the internal register file registers. The BCI A<3:0> lines transfer through a transparent latch controlled by the BCI AS signal and may be used in a latched or unlatched mode.

BCI Address Strobe (BCI AS)—Controls the transparent latch for BCI A<3:0> input data and for II PSEL input. The latch is transparent when BCI AS is asserted and the information is latched when it is deasserted.

BCI Write Strobe (BCI WS)—Controls BCI bus write operations to the internal register file. The input data BCI D<31:00> from the input latch is loaded into the selected BCAI register during assertion of this signal.

BCI Enable Write Strobe (BCI ENA WS)—Gates the BCI WS level into the BCAI.

BCI Read Strobe (BCI RS)—Controls BCI bus read operations of the internal register file. The operation is initiated when BCI RS is asserted and the resulting data is held in an internal register upon the deassertion of BCI RS. The byte valid bits for the addressed register are reset when a byte within the DMA data buffer is read. The BCI ENA RS signal must be asserted or this line will be disabled.

BCI Enable Read Strobe (BCI ENA RS)—Gates the BCI RS signal into the BCAI.

BCI Master Latch Strobe (BCI MLS)—Controls the transparent output register for BCI D<31:00> and BCI I<3:0> master output data. The latch is transparent when BCI MSL is asserted and the information is latched when it is deasserted. Either the BCI ENA MSL or BCI ENB MLS signal must be asserted or this line will be disabled.

BCI Enable A Master Latch Strobe (BCI ENA MLS)—Gates the $\overline{\text{BCI MLS}}$ signal into the BCAI.

BCI Enable B Master Latch ($\overline{\text{BCI ENB MLS}}$)—Same function as the $\overline{\text{BCI MLS}}$ signal.

BCI Slave Latch Strobe ($\overline{\text{BCI SLS}}$)—Controls the transparent output latch for BCI D<31:00> and BCI I<3:0> slave output data. The latch is transparent when the $\overline{\text{BCI SLS}}$ is asserted and the information is latched when it is deasserted. The $\overline{\text{BCI ENA SLS}}$ signal must be asserted or this line is disabled.

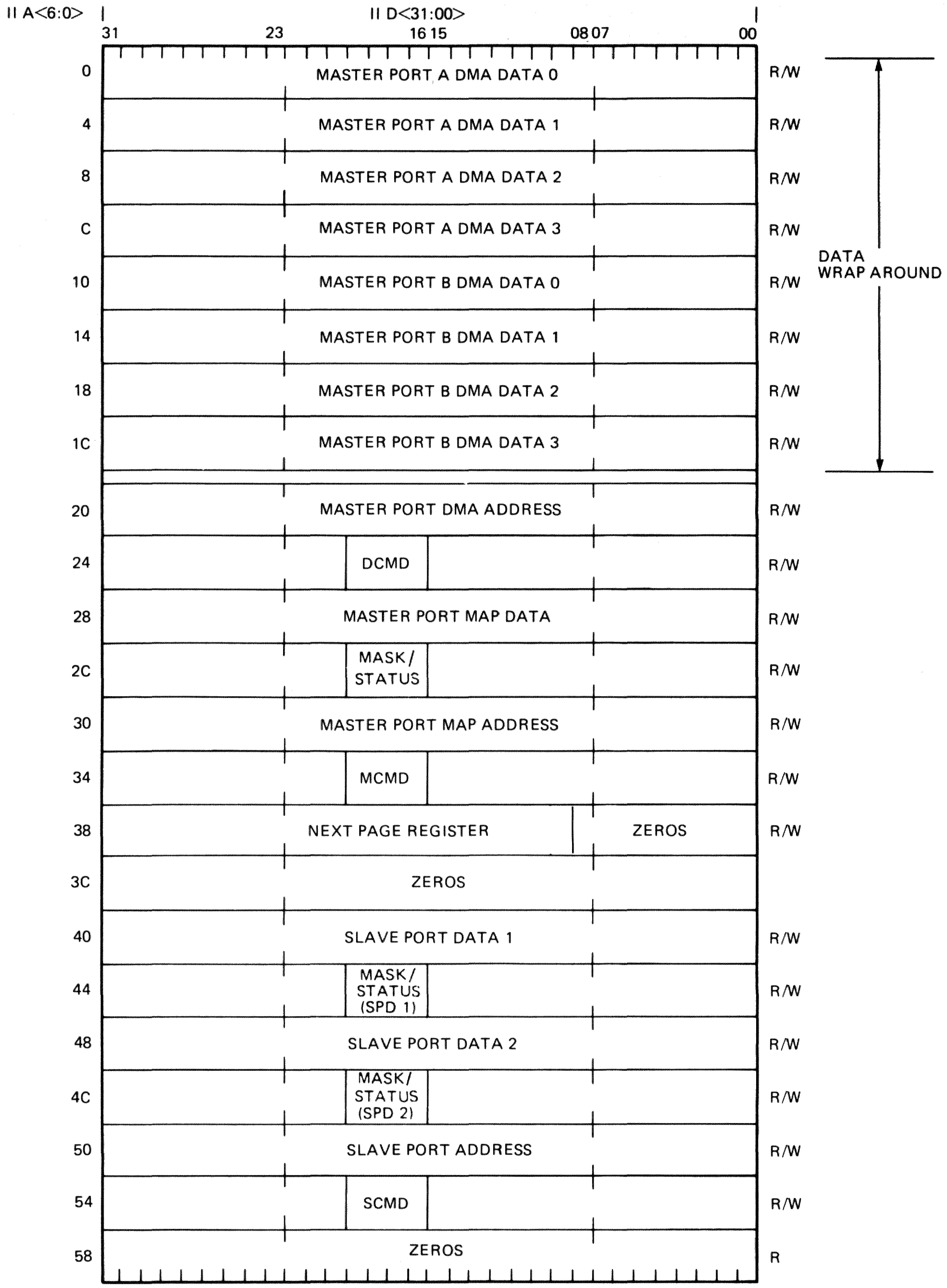
BCI Enable Slave Latch Strobe ($\overline{\text{BCI ENA SLS}}$)—Gates the $\overline{\text{BCI SLS}}$ signal into the BCAI.

BCI Master Data Enable ($\overline{\text{BCI MDE}}$)—Controls the transfer of the data in the master output latch to the BCI D<31:00> and BCI I<3:0> lines. This signal has an internal 50 µA pullup device so that the BCI D<31:00> and BCI I<3:0> lines remain a high impedance when the $\overline{\text{BCI MDE}}$ input is not connected.

BCI Slave Data Enable ($\overline{\text{BCI SDE}}$)—Controls the transfer of the data in the slave output latch to the BCI D<31:00> and BCI I<3:0> lines. This signal has an internal 50 µA pullup device so that the BCI D<31:00> and BCI I<3:0> lines remain a high impedance when the $\overline{\text{BCI SDE}}$ input is not connected.

General Register Addressing

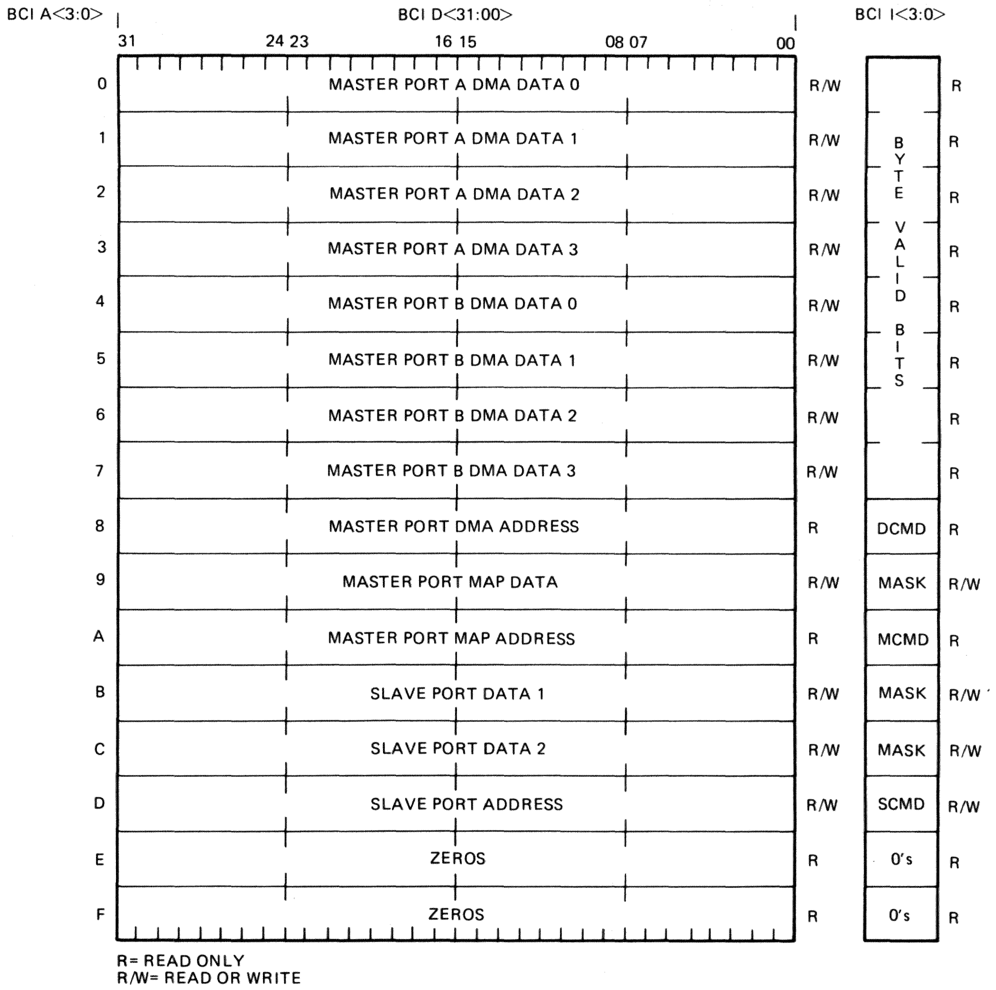
Figures 5 shows the memory map configuration and information of the BCAI registers when accessed by the II bus interface. Figure 6 show register memory map configuration and information of the BCAI registers accessed from the BCI bus interface. The hexadecimal address assignments and read/write capablities of each register are listed in the figures.



0	MASTER PORT A DMA DATA 0	R/W
4	MASTER PORT A DMA DATA 1	R/W
8	MASTER PORT A DMA DATA 2	R/W
C	MASTER PORT A DMA DATA 3	R/W
10	MASTER PORT B DMA DATA 0	R/W
14	MASTER PORT B DMA DATA 1	R/W
18	MASTER PORT B DMA DATA 2	R/W
1C	MASTER PORT B DMA DATA 3	R/W
20	MASTER PORT DMA ADDRESS	R/W
24	DCMD	R/W
28	MASTER PORT MAP DATA	R/W
2C	MASK/ STATUS	R/W
30	MASTER PORT MAP ADDRESS	R/W
34	MCMD	R/W
38	NEXT PAGE REGISTER / ZEROS	R/W
3C	ZEROS	
40	SLAVE PORT DATA 1	R/W
44	MASK/ STATUS (SPD 1)	R/W
48	SLAVE PORT DATA 2	R/W
4C	MASK/ STATUS (SPD 2)	R/W
50	SLAVE PORT ADDRESS	R/W
54	SCMD	R/W
58	ZEROS	R

R= READ ONLY
R/W= READ/WRITE

Figure 4 ▪ VAXBI 78743 II Bus Interface Register Memory Map



BCI A<3:0>	BCI D<31:00> (31 · 24 23 · 16 15 · 08 07 · 00)		BCI I<3:0>	
0	MASTER PORT A DMA DATA 0	R/W	BYTE VALID BITS	R
1	MASTER PORT A DMA DATA 1	R/W		R
2	MASTER PORT A DMA DATA 2	R/W		R
3	MASTER PORT A DMA DATA 3	R/W		R
4	MASTER PORT B DMA DATA 0	R/W		R
5	MASTER PORT B DMA DATA 1	R/W		R
6	MASTER PORT B DMA DATA 2	R/W		R
7	MASTER PORT B DMA DATA 3	R/W		R
8	MASTER PORT DMA ADDRESS	R	DCMD	R
9	MASTER PORT MAP DATA	R/W	MASK	R/W
A	MASTER PORT MAP ADDRESS	R	MCMD	R
B	SLAVE PORT DATA 1	R/W	MASK	R/W
C	SLAVE PORT DATA 2	R/W	MASK	R/W
D	SLAVE PORT ADDRESS	R/W	SCMD	R/W
E	ZEROS	R	0's	R
F	ZEROS	R	0's	R

R= READ ONLY
R/W= READ OR WRITE

Figure 5 • VAXBI 78743 BCI Bus Interface Register Memory Map

The registers within the file are grouped according to their supporting function. Support for the DMA port consists of a two octaword DMA transaction buffer, a command/address register with increment capability, and a next page frame (NPF) register. Support for the mapped master port consists of a command/address register with increment capability and a single longword data register with a mask/status register. Support for the slave port consists of a command/address register and two longword data registers, each with a mask/status register. A more detailed functional description of the registers is described.

dc Electrical Characteristics

Table 5 contains the dc electrical parameters for the input and outputs of the BCAI interface chip.

Table 5 • VAXBI 78743 dc Input and Output Parameters

Symbol	Parameter	Test Conditions	Requirements Min.	Requirements Max.	Units
V_{IH}	High-level input voltage		2.2	V_{CC}	V
V_{IL}	Low-level input voltage		-1.0	0.8	V
V_{OH}	High-level output voltage	$I_{out} = II\ I_{OH}$	2.7	—	V
V_{OL}	Low-level output voltage	$I_{out} = II\ I_{OL}$	—	0.5	V
I_{OH}	High-level output current	$V_{out} = II\ V_{OH}$	-400	—	mA
I_{OL}	Low-level output current	$V_{out} = II\ V_{OL}$	4.0	—	mA
I_I	Input current[1]		—	±20	μA
II_{LA}	Input current open latch[1]		-330	100	μA
I_{OS}	Output current short circuit[2]		—	-150	mA
I_{OE}	Enable line current	$\overline{\text{BCI MDE}}$, $\overline{\text{BCI SDE}}$, $\overline{\text{II OE}}$ inputs	50	200	μA
I_{DD}	Power supply current		—	500	mA
C_{IO}	Input/output capacitance	$0 < V_{IO} < V_{CC}$	—	10	pF

[1] Applies to the following three-state bidirectional signals: BCI D<31:00>, BCI I<3:0>, BCI P0, II D<31:00>, and II P<3:0>.
II_{LA} applies when the following inputs are open and I_I when closed: BCI A<3:0>, II M<3:0>, II A<6:0>, and II PSEL.

[2] Not more than one output must be short circuited at a time and the duration of the short must not exceed 1 second.

ac Electrical Characteristics

Figure 6 shows the signal timing for a read transaction from the BCI bus interface and Table 6 lists the timing parameters. Figure 7 shows the signal timing for a write transaction from the BCI bus interface and Table 7 lists the timing parameters. Figure 8 shows the signal timing for an address increment and Table 8 lists the timing parameters. The signal timing for a II bus interface read transaction is shown in Figure 9 and the timing parameters are listed in Table 9. Table 10 lists the timing parameters for a II bus interface write transaction shown in Figure 10.

Note

The propagation delays of the outputs assume a capacitance load of 50 pF. For loads greater than 50 pF, the following applies

$$t\ (50\ \text{pF} < C_{\text{load}} < 100\ \text{pF}) = t\ (50\ \text{pF}) + C_{\text{load}}/5.9 - 9.1$$

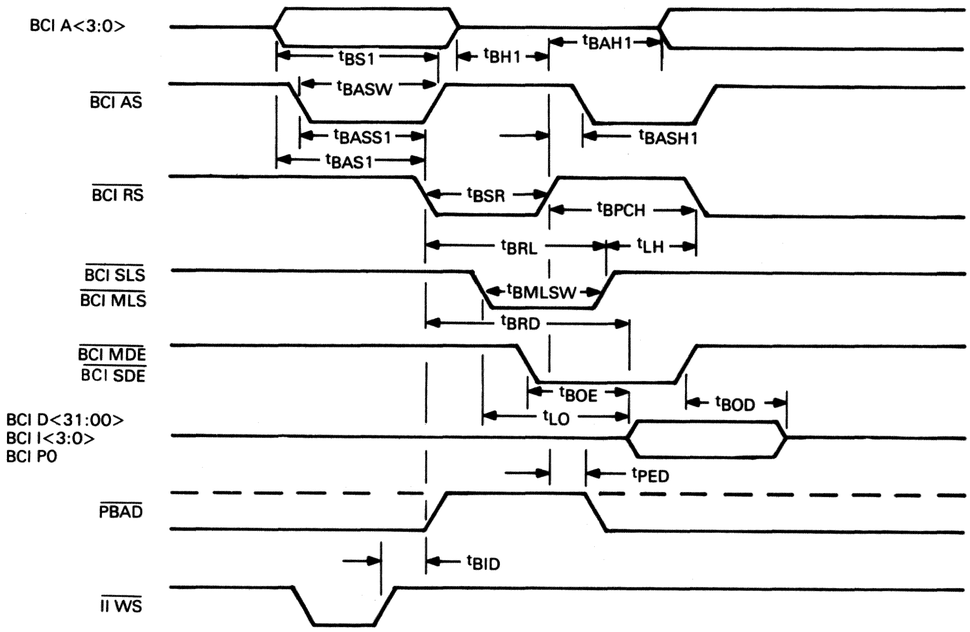


Figure 6 • VAXBI 78743 BCI Bus Interface Read Transaction Timing

Table 6 • VAXBI 78743 BCI Bus Interface Read Timing Parameters

Symbol	Definition	Requirements (ns) Min.	 Max.
t_{BS1}	BCI A<3:0> to $\overline{\text{BCI AS}}$ setup time	15	—
t_{BH1}	BCI A<3:0> to $\overline{\text{BCI AS}}$ hold time	10	—
t_{BASW}	BCI address latch strobe width	15	—
t_{BASS1}	$\overline{\text{BCI AS}}$ to $\overline{\text{BCI RS}}$ setup time	45	—
t_{BAS1}	BCI A<3:0> to $\overline{\text{BCI RS}}$ setup time	45	—

Symbol	Definition	Requirements (ns) Min.	 Max.
t_{BASH1}	$\overline{\text{BCI AS}}$ from $\overline{\text{BCI RS}}$ hold time	15	—
t_{BAH1}	BCI A<3:0> from $\overline{\text{BCI RS}}$ hold time	15	—
t_{BSR}	Read strobe width	90	—
t_{BPCH}	Preset width ($\overline{\text{BCI RS}}$ and $\overline{\text{BCI WS}}$ unasserted)	40	—
t_{BRL}	Output latch close time after read access	—	100
t_{BRD}	Read access time	—	110
t_{BMLSW}	$\overline{\text{BCI MLS}}$, $\overline{\text{BCI SLS}}$ strobe pulse width	25	—
t_{LH}	$\overline{\text{BCI MLS}}$, $\overline{\text{BCI SLS}}$ strobe hold time	15	—
t_{BOE}	BCI output enable time	—	40
t_{BOD}	BCI output disable time	—	40
t_{PED}	Parity error output delay	—	60
t_{LO}	Latch to output delay	—	50
t_{BID}	$\overline{\text{II WS}}$ deasserts to BCI read (same register)	0	—

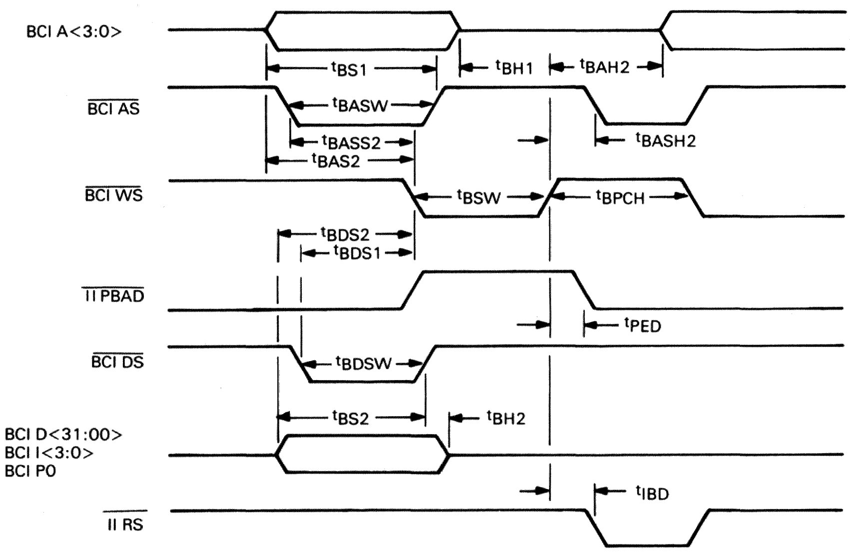


Figure 7 • VAXBI 78743 BCI Bus Interface Write Transaction Timing

Table 8 • VAXBI 78743 II Bus Interface Read Timing Parameters

Symbol	Definition	Requirements (ns) Min.	 Max.
t_{IS1}	II A<3:0> to $\overline{\text{II AS}}$ setup time	15	—
t_{IH1}	II A<3:0> to $\overline{\text{II AS}}$ hold time	10	—
t_{IASW}	II address latch strobe time	15	—
t_{IASS1}	$\overline{\text{II AS}}$ to $\overline{\text{II RS}}$ setup time	60	—
t_{IAS1}	II A<3:0> to $\overline{\text{II RS}}$ setup time	60	—
t_{IAH1}	II A<3:0> to $\overline{\text{II RS}}$ hold time	15	—
t_{IASH1}	$\overline{\text{II AS}}$ from $\overline{\text{II RS}}$ hold time	15	—
t_{ISR}	Read strobe width	45	—
t_{IPCH}	Preset width ($\overline{\text{II RS}}$ and $\overline{\text{II WS}}$ unasserted)	40	—
t_{IRD}	Read access time	—	90
t_{IOE}	II output enable time	—	40
t_{IOD}	II output disable time	—	40

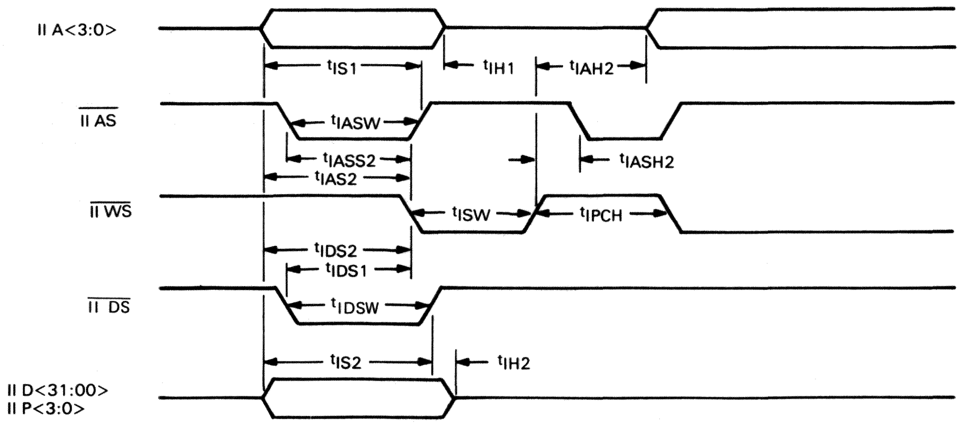


Figure 9 • VAXBI 78743 II Bus Interface Write Transaction

Table 9 ▪ VAXBI 78743 II Bus Interface Write Timing Parameters

Symbol	Definition	Requirements (ns) Min.	 Max.
t_{IS1}	II A<3:0> to $\overline{\text{II AS}}$ setup time	15	—
t_{IH1}	II A<3:0> to $\overline{\text{II AS}}$ hold time	10	—
t_{IASW}	II address latch strobe time	15	—
t_{IASS2}	$\overline{\text{II AS}}$ to $\overline{\text{II WS}}$ setup time	60	—
t_{IAS2}	II A<3:0> to $\overline{\text{II WS}}$ setup time	60	—
t_{IAH2}	II A<3:0> to $\overline{\text{II WS}}$ hold time	15	—
t_{IASH2}	$\overline{\text{II AS}}$ from $\overline{\text{II RS}}$ hold time	15	—
t_{IDS1}	$\overline{\text{II DS}}$ to $\overline{\text{II WS}}$ setup time	0	—
t_{IDS2}	II D<31:00> to $\overline{\text{II WS}}$	0	—
t_{ISW}	Write strobe width	45	—
t_{IPCH}	Preset width ($\overline{\text{II RS}}$ and $\overline{\text{II WS}}$ unasserted)	40	—
t_{IDSW}	II data strobe width	15	—
t_{IS2}	II D<31:00> and II P<3:0> to $\overline{\text{II DS}}$ setup time	15	—
t_{IH2}	II D<31:00> and II P<3:0> from $\overline{\text{II DS}}$ hold time	10	—

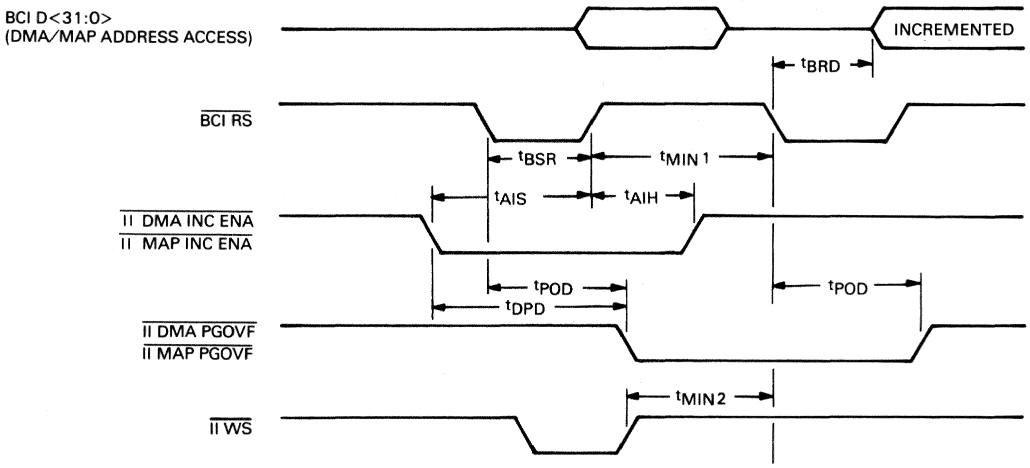


Figure 10 ▪ VAXBI 78743 BCI DMA and MAP Address Increment Timing

dc Electrical Characteristics

Table 10 contains the dc electrical parameters for the input and outputs of the BCI3 interface chip.

Table 10 • VAXBI 78733 dc Input and Output Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Requirements Max.	Units
High-level input voltage	V_{IH}		2.0	—	V
Low-level input voltage	V_{IL}		-0.5	0.8	V
High-level output voltage	V_{OH}	$I_{OH} = -400$ A	2.4	—	V
Low-level output voltage	V_{OL}	$I_{OL} = 2.4$ mA $I_{OL} = 4.0$ mA*	—	0.4	V
Input leakage current	I_{IL}	$0 V < V_{in} < 5.25 V$	-20	20	A
Output high-impedance leakage current	I_{ZO}	$0 V < V_{in} < 5.25 V$	-20	20	A
Supply current	I_{CC}		—	500	mA
Input capacitance	C_{in}	$\overline{\text{BCI MDE}}$, $\overline{\text{BCI SDE}}$	—	50	pF
		all other signals	—	10	pF
Output capacitance	C_{out}		—	10	pF

*Open-drain outputs

▪ Pin and Signal Descriptions

This section provides a brief description of the input and output signals and power and ground connections of the DC004 20-pin DIP. The pin assignments are identified in Figure 2 and the summarized in Table 1. The signal names shown in the diagram are for the condition where the DC004 is connected to the internal three-state bus of the DC005.

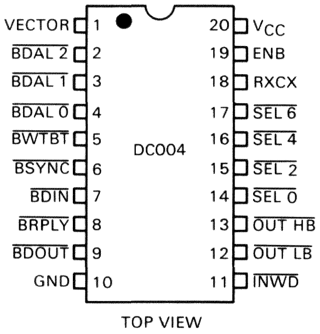


Figure 2 ▪ DC004 Pin Assignments

DC005 4-Bit Transceiver

▪ Features

- Used with the DC003 and DC004 circuits to implement a program control device interface.
- Used with the DC003, DC004, DC006, and DC010 circuits to implement a direct memory access interface.
- Functions as a bidirectional buffer between the device logic and computer bus.
- Includes comparison circuit for device address selection.
- Includes constant generator for interrupt vector address generation.
- Includes Q-bus drivers and receivers.

▪ Description

The DC005 4-bit transceiver, contained in a 20-pin dual-inline package (DIP), implements low-power Schottky technology and functions as a bidirectional buffer between a data bus and peripheral device logic bus. It includes a comparison circuit for device address selection and a constant generator for interrupt-vector address generation. It provides high-impedance inputs and high-drive, open-collector outputs to allow direct connection to a computer data bus structure. The bidirectional device port includes TTL inputs and three-state driver outputs. Figure 1 is a simplified logic diagram of the DC005.

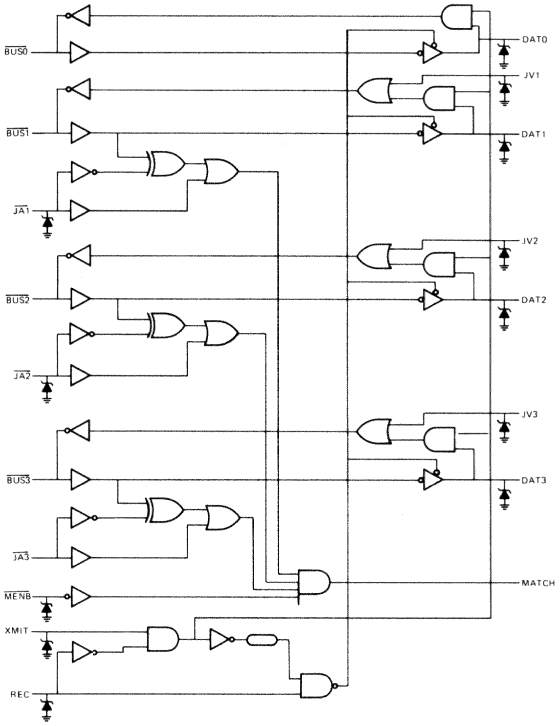


Figure 1 ▪ DC005 Simplified Logic Diagram