TMF

# MAGNETIC TAPE FORMATTER

## USER GUIDE

digital

EK-0TM03-UG-003

# TM03 Magnetic Tape Formatter

# User Guide

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# CHAPTER 1
# GENERAL INFORMATION

## 1.1 INTRODUCTION

The TM03 Magnetic Tape Formatter serves as an interface between various magnetic tape transports and any Massbus controller. It provides control, data, status, and error information between the Massbus controller and a standard 1.27 cm (1/2 inch) magnetic tape unit (slave) operating at 114.3, 190.5, or 317.5 cm/second (45, 75, or 125 in/second). The TM03 is capable of reading and writing magnetic tape for information interchange at 800 bits/inch NRZI or 1600 bits/inch PE (phase encoded). It also has a forward and reverse read and spacing capability. The TM03 formats data from the PDP-10 and PDP-11 processors* into tape frame characters and performs the reverse during a data read operation.

Aside from providing magnetic tape formatting, the TM03 offers the following features.

1. The TM03 provides automatic error correction of single-track errors in PE data (hardware controlled).

2. The TM03 provides automatic error correction of single-track errors in NRZI read data. (NRZI error correction is under software control and therefore does not occur automatically as does PE error correction.)

3. The TM03 provides automatic selection of either 800 bits/inch (NRZI) or 1600 bits/inch (PE) density during a read operation from BOT (beginning of tape).

4. The TM03 is capable of controlling from one to eight slaves. It should be noted that although the TM03 can handle tape speeds of 114.3, 190.5, and 317.5 cm/second (45, 75, 125 in/second), all slaves interfaced to any one TM03 must be operating at the same tape speed.

5. The TM03 writes an industry-compatible PE tape mark.

6. The TM03 performs extensive parity checking throughout all read and write data paths. In addition, the TM03 is equipped with self-contained maintenance mode operations which allow complete testing of all critical electronics under diagnostic control.

## 1.2 GENERAL DESCRIPTION

Figure 1-1 illustrates a TM03/tape transport system configuration. Each TM03 can control up to eight slave transports. In turn, each Massbus controller can control up to eight TM03 formatters. Thus, a maximum of 64 tape transports could be interfaced to a single Massbus controller.

Figures 1-2, 1-3, and 1-4 show the TM03 in typical transport environments. An H740-DA power supply is required to provide power for the TM03. Figure 1-5 illustrates the TM03 front panel. A POWER indicator illuminates when power is applied to the TM03 from the H740-DA power supply. The PHASE ENCODED indicator illuminates when the TM03 is in the PE mode during a read or write operation.

*Also the PDP-15 via a PDP-11 for interface to the Massbus (PDP-15 Unichannel).

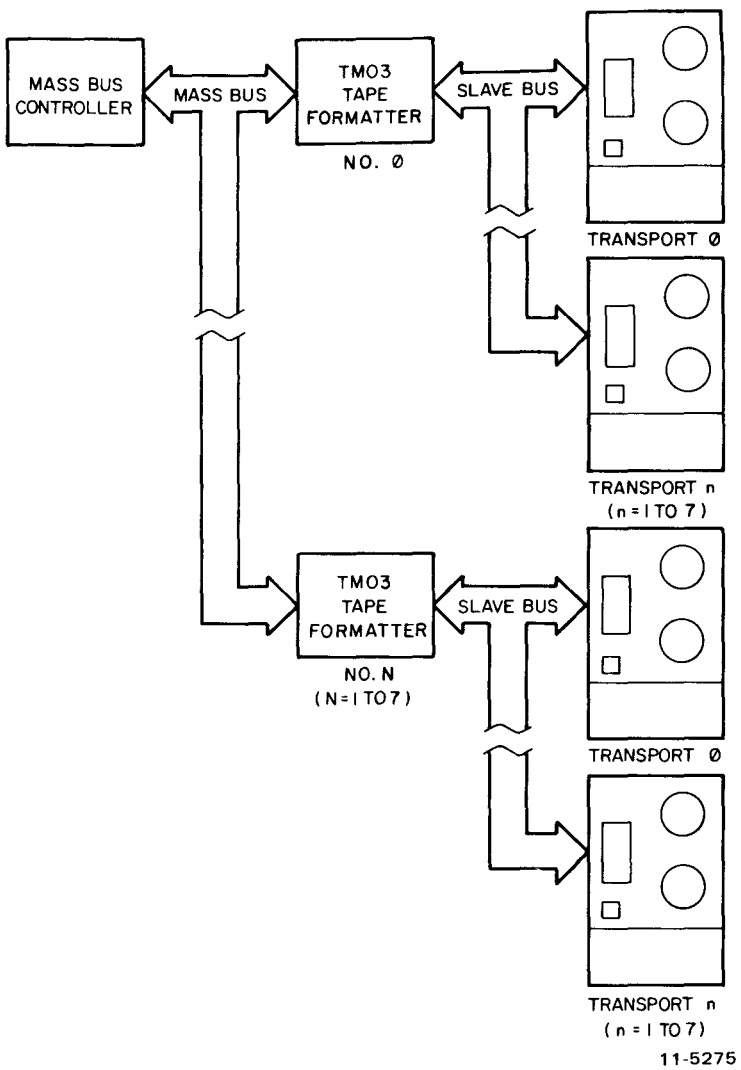



Figure 1-1 TM03 Tape Transport System Configuration

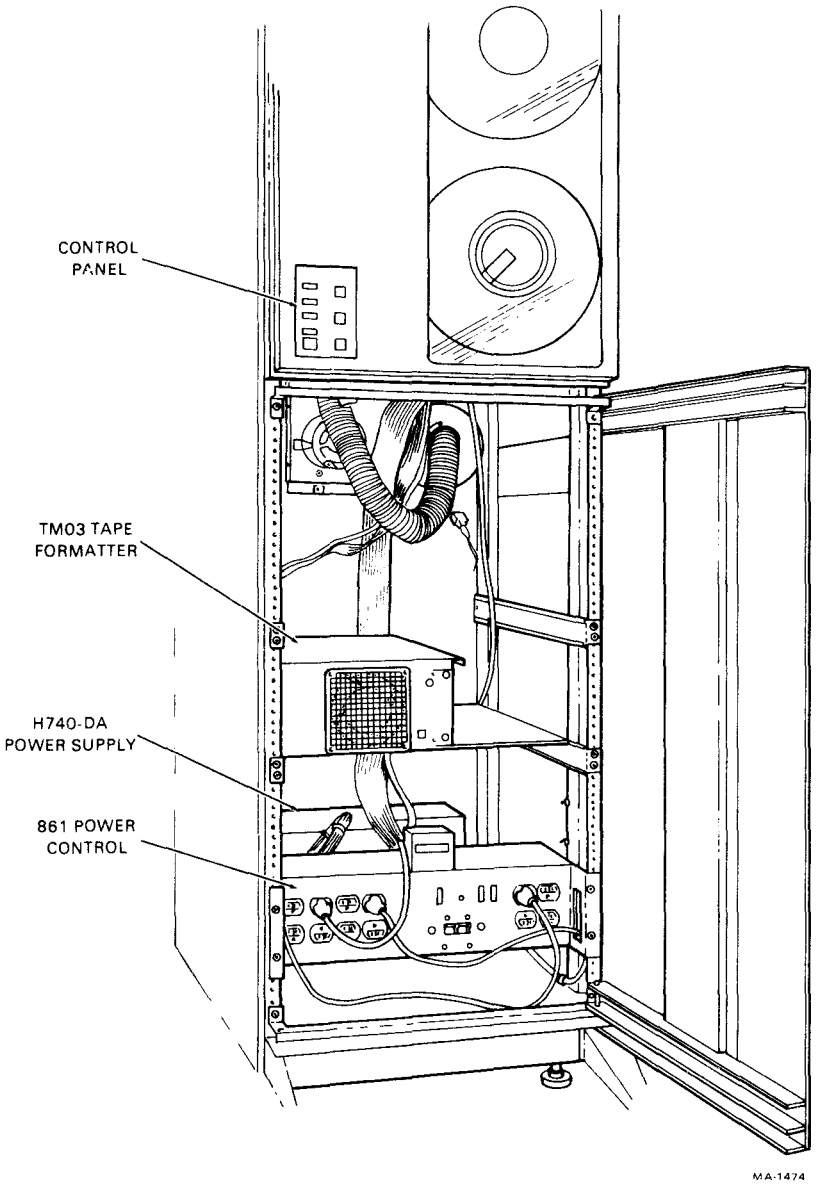



Figure 1-2 TM03 with TE16 Tape Transport in H950 Cabinet

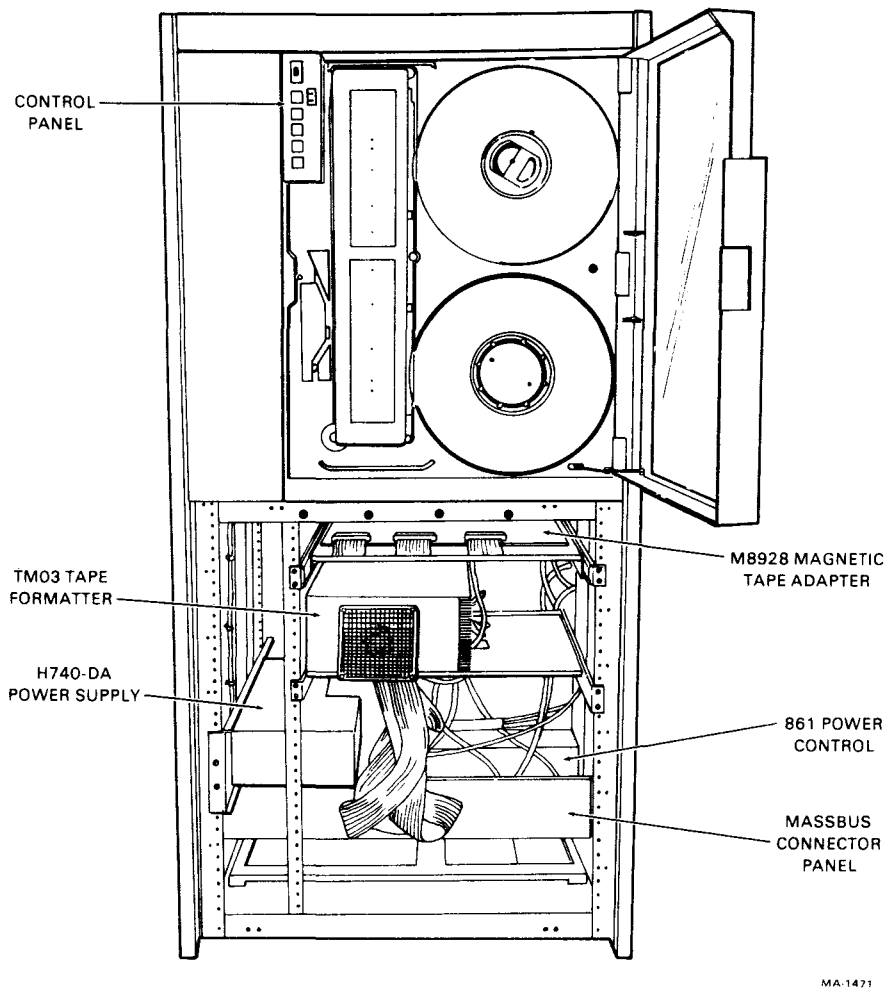



Figure 1-3 TM03 with TU45 Tape Transport in H9500 Corporate Cabinet

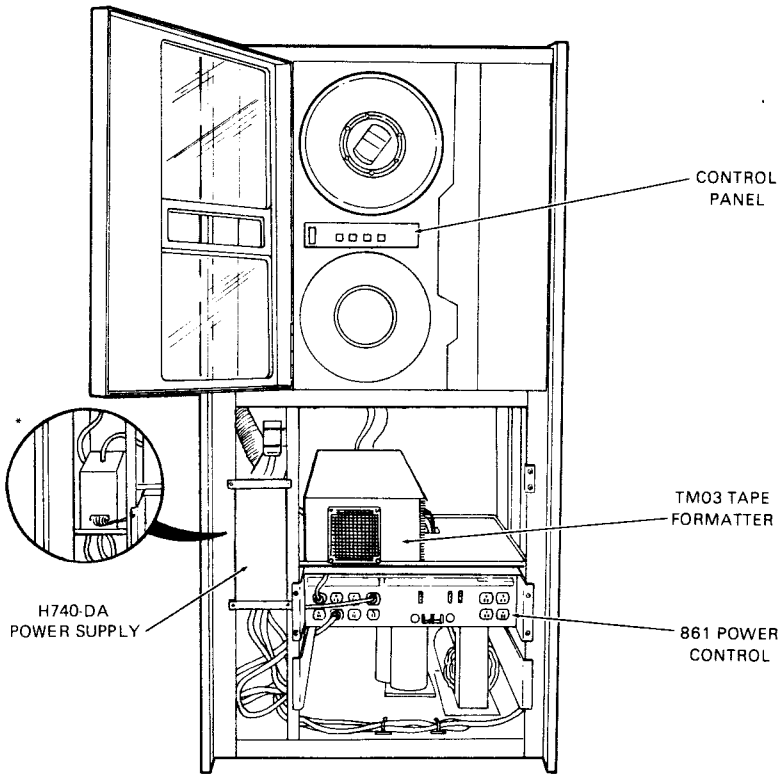



Figure 1-4 TM03 with TU77 Tape Transport in H9500 Corporate Cabinet

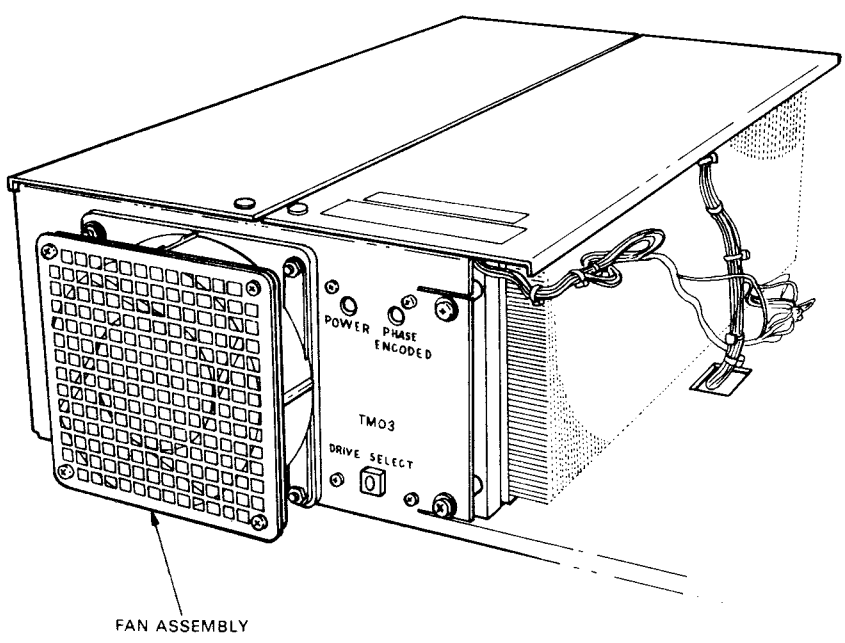



Figure 1-5 TM03 Front Panel

## 1.3 FUNCTIONAL DESCRIPTION

### 1.3.1 Introduction

The TM03/tape transport system (Figure 1-6) interfaces with the central processor unit (CPU) via the Massbus controller. However, the Massbus controller is almost transparent to the CPU, and the CPU operates as though it were controlling the drive directly.

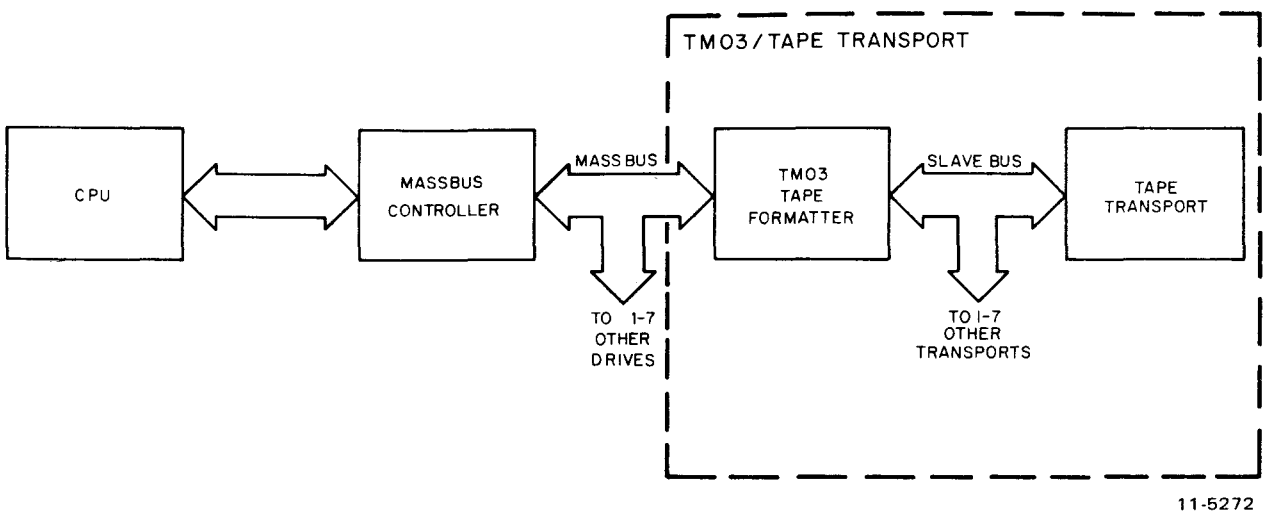



Figure 1-6 TM03 in a System Configuration

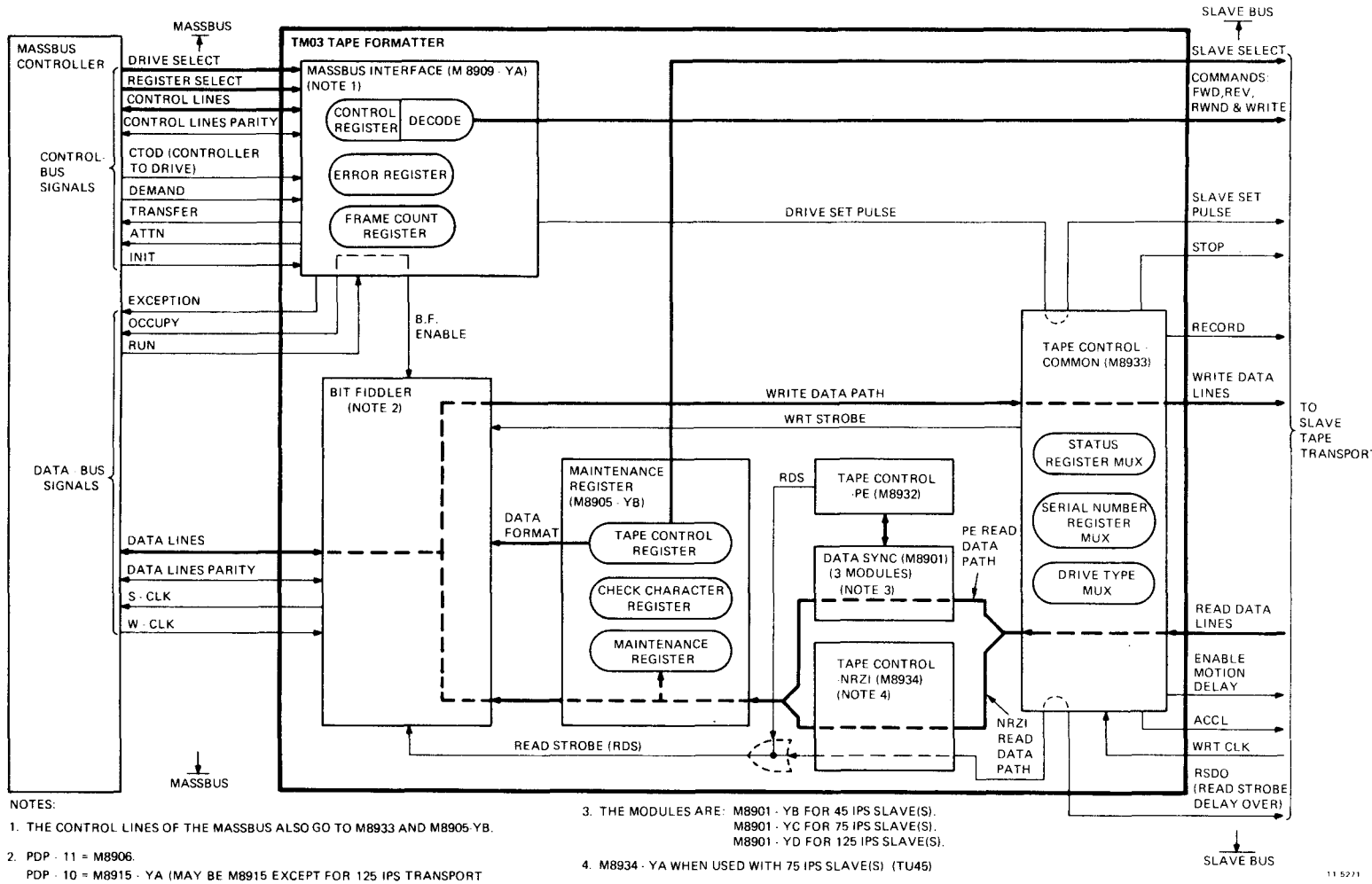
The TM03 interfaces with the Massbus controller via the Massbus. The Massbus consists of an asynchronous control bus with its associated control lines, and a synchronous data bus with its associated control lines. Transactions on the control bus control the TM03/transport and determine its status, while transactions on the data bus transfer data to or from the TM03/transport. Because the data and control buses operate independently, the Massbus controller can monitor drive status while a data transfer operation is being performed.

The TM03 can control up to eight tape transports via the slave bus. All transports controlled by a TM03 are "daisy-chained" on the slave bus (Figure 1-6). Essentially, this means that the transports are configured in parallel to each other. The slave bus consists of slave select lines, write data lines, read data lines, transport control lines, and various transport status lines.

### 1.3.2 System Operation

Figure 1-7 is a block diagram of the TM03, and shows the major functional groups, control lines, and data paths. The following paragraphs describe these functional groups.

**1.3.2.1 Massbus Interface Module (M8909-YA)** – The Massbus interface module interfaces the TM03 with the Massbus controller. It contains circuitry that decodes the drive select signals on the Massbus. If enabled by the proper drive select address code, the Massbus interface can carry on the "handshake" operations with the Massbus controller, which read and write TM03 registers. The most important of the TM03 registers is the control register (CS1), which is located in the Massbus interface. The Massbus controller writes the function code of the next operation to be performed into the control register. The Massbus interface decodes this register and generates the appropriate control signals (FWD, REV, RWND, WRITE) to control the slave and various TM03 functions.




NOTES:

1. THE CONTROL LINES OF THE MASSBUS ALSO GO TO M8933 AND M8905-YB.
2. PDP - 11 = M8906.
   PDP - 10 = M8915 - YA (MAY BE M8915 EXCEPT FOR 125 IPS TRANSPORT (TU77) WHICH MUST USE M8915 - YA).
3. THE MODULES ARE: M8901 - YB FOR 45 IPS SLAVE(S).
   M8901 - YC FOR 75 IPS SLAVE(S).
   M8901 - YD FOR 125 IPS SLAVE(S).
4. M8934 - YA WHEN USED WITH 75 IPS SLAVE(S) (TU45)

Figure 1-7 TM03 Basic Block Diagram

The Massbus interface module contains several other registers including an error register and a frame count register. The frame count register must be loaded prior to a space or write operation with the number (in 2's complement form) of records to be spaced or tape characters to be written. This register is incremented as the operation proceeds, and will terminate the operation with register overflow.

The Massbus interface decodes the control register to determine that a data transfer operation is to be performed. When this is the case, it generates OCC on the Massbus to notify the controller and other drives that it has occupied the data bus, and enables the bit fiddler.

**1.3.2.2 Bit Fiddler Module***– The bit fiddler interfaces the TM03 data paths to the Massbus controller; it contains circuitry that performs synchronous data transfers on the data bus of the Massbus.

The bit fiddler is enabled for operation by the Massbus interface with BF ENABLE. The mode of bit fiddler operation is determined by control lines FMT0–3 (tape character format), WRITE (direction of transfer, i.e., read or write), and FWD (direction of tape motion, i.e., forward or reverse). WRITE and FWD are decodes of the control register function bits. FMT0–3 are the tape control register format bits, and are decoded in the bit fiddler.

During a write operation, the Massbus controller places a data word on the data bus. When the bit fiddler is ready to accept this data word, it issues SCLK (sync clock) to the controller, which replies with WCLK (write clock).

Upon receiving WCLK, the bit fiddler strobes in the word on the data bus, performs a data bus parity check, disassembles the data word into 8-bit characters, and generates a vertical parity bit for each 8-bit character. After generating WCLK, the controller places the next data word on the data bus. When the bit fiddler has finished disassembling the previous data word, it issues another SCLK, receives another WCLK, and strobes in the next data word for disassembly. The process continues until all the data has been transferred (precluding occurrence of data errors or other failures).

During a read operation, the bit fiddler assembles 8-bit characters into data words. When the data word has been assembled, it is placed on the data bus along with a parity bit (DPA), and the bit fiddler generates an SCLK pulse. When the Massbus controller receives SCLK, it strobes in the data on the data bus. The bit fiddler continues to assemble data characters into data words, and notifies the controller that a data word is available by generating SCLK. As in a write operation the method of assembly is determined by the FMT0–3, WRITE, and FWD signals input to the bit fiddler.

**1.3.2.3 Maintenance Register Module (M8905-YB)** – The maintenance register module is part of the read data path; read data is multiplexed through the maintenance register module from the PE or NRZI read circuitry (M8901 or M8934) to the bit fiddler. The maintenance register module also contains the tape control register, the check character register, and the maintenance register. The tape control register contains slave select bits, which are translated to slave bus signals (SS 0–2) and determine which slave will perform the operations specified by the Massbus controller. This register also contains tape data format information. Therefore, the tape control register must be properly loaded by the Massbus controller prior to the specification of a particular functional operation.

The maintenance register module plays an important role in maintenance mode operation. By writing into the maintenance register (R03), the Massbus controller can select one of several maintenance modes. These modes allow:

1. Testing of various TM03 circuits independently of the slave transport
2. Testing of the TM03 under tighter operation criteria.

*M8915-YA, M8915, or M8906, depending on processor and transport.

**1.3.2.4 Tape Control-NRZI Module (M8934)*** – The tape control-NRZI module performs functions relating only to NRZI data storage and retrieval. During an NRZI read operation, the tape control-NRZI module is part of the read data path. When informed by the slave that a tape character is available [RSDO (read strobe delay over) asserted], the tape control-NRZI module generates RDS (read strobe) and strobes the tape character from the tape control common mode module (M8933) into an NRZI read latch. The output of the latch, multiplexed through the maintenance register module, becomes available to the bit fiddler.

During an NRZI read operation, the tape control-NRZI module also generates and checks LRCC (longitudinal redundancy check character) and CRCC (cyclic redundancy check character), checks vertical parity, detects tape marks (file marks), performs error correction of single track errors if the software so specifies, and determines that the minimum criteria for normal termination have been met.

During an NRZI write operation, the tape control-NRZI module generates the CRCC.

**1.3.2.5 Data Sync-PE Module (M8901)*** – The data sync module (one of three) is part of the PE read data path. It processes PE read data from the tape control common mode (TCCM) module (M8933), converting the PE information to binary and deskewing the data. It operates with the tape control-PE module (M8932) to detect preamble, data, postamble, and tape mark (TM). It also performs on-the-fly error correction of a single dead track based on vertical parity errors (VPE) detected by the tape control-PE module.

The data sync-PE module performs no write data path operations. However, it does a read-after-write during PE write operations.

**1.3.2.6 Tape Control-PE Module (M8932)** – During a PE read operation, the tape control-PE module operates with the data sync module to detect preamble, data, postamble, and TM. It also checks for vertical parity errors and PE format errors.

During a PE write operation, the tape control-PE module establishes the timing for writing preamble, data, and postamble.

**1.3.2.7 Tape Control Common Mode (TCCM) Module (M8933)** – The TCCM module contains tape control functions that are used by both PE and NRZI modes. The TCCM module generates clock waveforms used throughout the TM03 from a base clock frequency it receives from the selected slave transport.

When the control register is loaded with a function code requiring tape motion, the function code is decoded by the Massbus interface, and a FWD, REV, or RWND signal is applied to the slave bus. Soon after, a DRIVE SET pulse is generated by the Massbus interface to initialize TM03 circuitry. DRIVE SET pulse enters the TCCM module and produces SLAVE SET PLS and EMD (enable motion delay) – both of which are transmitted to the slave transport via the slave bus. SLAVE SET PLS initiates tape motion. EMD causes a preset to be applied on the read data lines of the slave bus by the slave transport and loads a motion delay counter in the TCCM with the preset. The counter is then upcounted to $2^{14}$, at which time ACCL is negated, indicating that the transport is assumed to be up to speed.

A similar motion delay is generated upon termination of a motion command, in which ACCL is asserted, and the TCCM issues STOP, causing the transport to cease tape motion.

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* M8934 and M8901-YB for 114.3 cm/second (45 inch/second) slaves (TE16).
M8934-YA and M8901-YC for 190.5 cm/second (75 inch/second) slaves (TU45).
M8934 and M8901-YD for 317.5 cm/second (125 inch/second) slaves (TU77).

During a read operation, read data is multiplexed from the slave bus read data lines through the TCCM module, to the data sync module (for PE) or tape control-NRZI module (for NRZI).

During a write operation, data is input to the TCCM module from the bit fiddler. The TCCM controls the timing for writing the LRCC and CRCC. It also contains a write multiplexer and write buffer, which:

1. Convert binary characters to PE mode
2. Multiplex 0s and 1s to write PE preambles and postambles
3. Multiplex the generated CRCC onto the write data path
4. Force IDB (identification burst) and TM (tape mark) character patterns onto the write data path.

Data in the TCCM write buffer is output via slave bus drivers on M8937 to the slave, along with REC. REC (record) is derived from WRT CLK, generated in the slave transport; its frequency depends on the mode (PE/NRZI) in which the write operation is performed.

## 1.4 RELATED DOCUMENTS

Table 1-1 lists documents related to the TM03 formatter.

**Table 1-1 Related Documents**

| Title | Document Number | Description |
|---|---|---|
| TE16/TE10W/TE10N DECmagtape Transport Maintenance Manual | EK-TE16-MM-001 | Theory and maintenance of TE16, TE10W, and TE10N tape transports |
| TE16/TE10W/TE10N DECmagtape Transport User Manual | EK-TE16-OP-001 | Description, installation and maintenance of the TE16, TE10W, and TE10N tape transports as applicable to a user |
| TU45A Magnetic Tape Subsystem Maintenance Manual | EK-TU45A-MM-001 | Theory and maintenance of TU45A tape transport |
| TU77 Magnetic Tape Transport Technical Manual, Volume 2 | EK-2TU77-TM-001 | Theory and maintenance of TU77 tape transport. |
| TU77 Magnetic Tape Transport User's Guide | EK-TU77-UG-001 | Description, installation, and operation of TU77 tape transport. |
| PDP-11 Peripherals Handbook | - | Provides register descriptions for RH Massbus controllers |
| H740-D Power Supply Maintenance Manual | DEC-11-H740A-A-D | Theory and maintenance of H740-DA power supply. (The -DA model differs from the -D model by an ac connector used to power the TM03 cooling fan.) |

**Table 1-1 Related Documents (Cont)**

| Title | Document Number | Description |
|---|---|---|
| RH10 Massbus Controller Maintenance Manual | EK-RH10-MM-002 | Theory and maintenance of RH10 Massbus controller |
| TJU16 Magnetic Tape Subsystem Maintenance Manual | EK-TJU16-MM-002 | Theory and maintenance of RH11 Massbus controller |
| TWU16 Magnetic Tape Subsystem Maintenance Manual | EK-TWU16-MM-PRE | Theory and maintenance of RH70 Massbus controller used with the PDP-11/70 |
| RH20 Massbus Controller Unit Description | EK-RH20-UD-001 | Description of RH20 Massbus controller |
| TM03 Magnetic Tape Formatter Technical Manual | EK-TM03-TM-001 | Description, installation, theory of operation, and maintenance of the TM03. |
| TM03 Formatter IPB | EK-TM03-IP | Illustrated parts breakdown of TM03. |
| RH780 Massbus Controller Technical Manual | EK-RH780-TM-001 | Theory and maintenance of RH780 Massbus controller |

## 1.5 UNIT SPECIFICATIONS

Table 1-2 provides the TM03 unit specifications.

**Table 1-2 Unit Specifications**

| Parameter | Specification |
|---|---|
| Maximum transfer rate between TM03 and slave | 240K bytes/second |
| Error detection | CRC error detection in forward and reverse read (NRZI).<br>Error correction of single track errors in NRZI and PE.<br>Vertical parity error detection throughout TM03. |
| Maximum record length | $2^{16}$ bytes, PE or NRZI |
| Minimum record length | 1 byte, PE; 13 bytes, NRZI (excluding tape mark) |
| Write lock | Dependent upon write lock signal from slave |
| Environment | |
| Operating | 10° to 40° C (50° to 104° F)<br>10 to 90 percent relative humidity<br>Wet bulb: 28° C (82° F) maximum<br>Dew point: 2° C (36° F), minimum |
| Non-operating | -40° to 66° C (-40° to 151° F)<br>0 to 95 percent relative humidity |

**Table 1-2 Unit Specifications (Cont)**

| Parameter | Specification |
|---|---|
| Altitude | |
| Operating | 2.4 km (8000 ft), maximum |
| Non-operating | 9.1 km (30,000 ft), maximum |
| Shock | |
| Operating | Shall withstand half-sine shock pulse of 10G, peak with 10 ± 3 ms duration |
| Non-operating | Shall withstand half-sine shock pulse of 40G, peak with 30 ± 10 ms duration, applied perpendicular to each of six surfaces |
| Vibration | |
| Operating | Shall withstand vibration of 0.0508 mm (0.002 inch) double amplitude (maximum) in the frequency range of 5 to 50 Hz |
| Non-operating | Shall withstand vibration of 0.25G peak, in the frequency range of 50 to 500 Hz |
| Power requirements | |
| DC | None |
| AC | 90–135/180–270 Vac, 47–63 Hz<br>0.3 kW |
| Installation | 16.83 cm (6-5/8 inch) panel height<br>48.3 cm (19 inch) rack mount |
| Shipping Weight | 20.412 kg (45 lb) (uncrated) |
| Reliability | Established by error rate of slave which is:<br>• Recoverable error rate*: less than one bit in $10^8$ reads<br>• Non-recoverable error rate*: less than one bit in $10^9$ reads |

* A recoverable error is defined as a read error that is recovered within eight successive retries. (Retries on the same spot do not increase the soft error tally; i.e., a read error on block no. 1, record no. 1, that required three retries to recover is recorded as one soft read error.) If the data is not recovered after eight successive retries (nine successive incorrect data transfers), it is counted as one hard error.

# CHAPTER 2
# PROGRAMMING INFORMATION

Chapter 2 contains programming information required by a user to program a system containing the TM03 formatter. The information provided pertains only to the TM03. Programming information pertaining to other system units can be found in the documentation applicable to these units. Table 1-1 lists the documents available on units that can interface with the TM03.

## 2.1 REGISTER FUNCTIONS AND FORMATS

The TM03 contains ten registers, some of which have been mentioned in Chapter 1. A summary of the TM03 registers is provided in Table 2-1. Any of the TM03 registers may be read to determine the status of the TM03/transport. Some of the registers may be written, thereby controlling functions and operating parameters.

The TM03 registers are read and written by performing "handshake" operations on the control bus of the Massbus. A register is loaded by the Massbus controller in the following manner.

1. The controller places the select code of the desired TM03 on the drive select lines.
2. The controller places a register select code on the register select lines.
3. It asserts CTOD (controller to drive).
4. It places data on the control lines.
5. The controller then asserts DEM.

The selected TM03 responds to DEM and CTOD asserted by loading the selected register with the data on the control lines. It then asserts TRA. The controller responds by negating DEM, which causes the TM03 to negate TRA; the write operation is thereby terminated.

A TM03 register is read in a similar manner except that CTOD is negated (step 3) and step 4 is eliminated. The selected TM03 responds to DEM asserted and CTOD negated by gating out the contents of the selected register onto the control lines. It then asserts TRA, which, when received by the controller, causes it to strobe in the data on the control lines and negate DEM. The TM03 responds by negating TRA, thereby terminating the operation.

The remainder of Paragraph 2.1 provides a more detailed description of the TM03 registers and their contents. It is primarily for reference, and may be skipped during a first reading.

**Table 2-1 TM03 Registers**

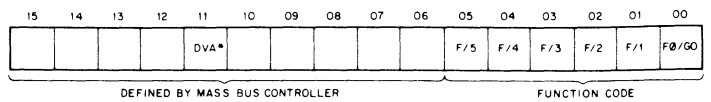
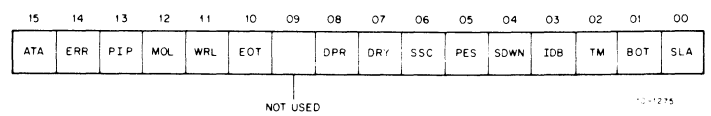
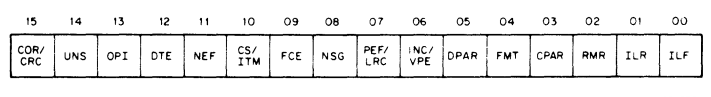
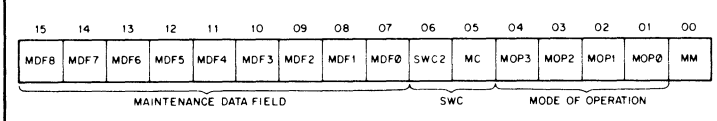
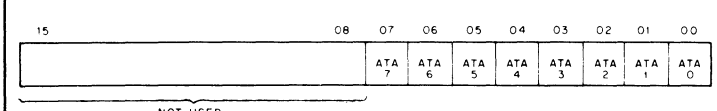
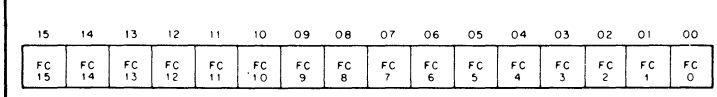
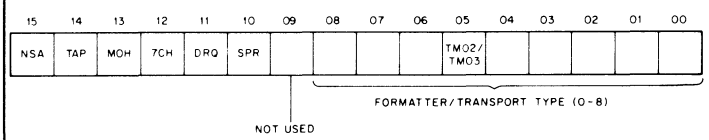
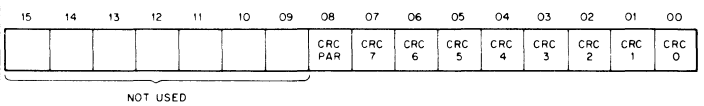
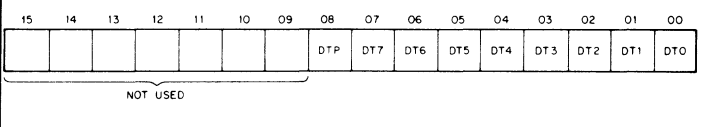
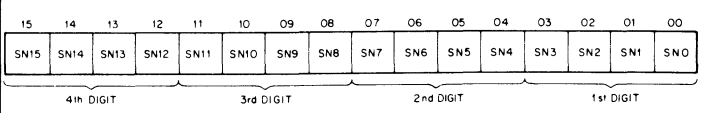
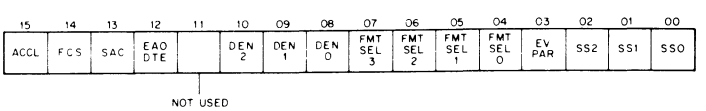
| Address Code (Octal) | Name | Type | Description |
|---|---|---|---|
| 00 | Control 1 (CS1) | Read/write | Contains the function code including the GO bit<br>  <br>*DRIVE AVAILABLE, HARDWIRED SET IN FORMATTER |
| 01 | Status (DS) | Read only | Contains all nonerror status information plus the error summary bit<br>  |
| 02 | Error (ER) | Read only | Contains all error indications<br>  |
| 03 | Maintenance (MR) | Read/write | Controls diagnostic functions<br>  |
| 04 | Attention Summary (AS) | Read/write | Indicates the attention active status of each TM03 (one bit/TM03)<br>  |
| 05 | Frame Count (FC) | Read/write | For a write data transfer operation, contains the 2's complement of the number of tape characters to be transferred.<br>For a space operation, contains the 2's complement of the number of records to be spaced.<br>For a read data transfer operation, contains the 2's complement of the number of characters read.<br>  |

**Table 2-1 TM03 Registers (Cont)**

| Address Code (Octal) | Name | Type | Description |
|---|---|---|---|
| 06 | Drive Type (DT) | Read only | Indicates the type of formatter and the type and status of the transport (e.g., existing formatter and transport with power applied)<br>  <br> |
| 07 | Check Character (CK) | Read only | For an NRZI operation, contains the CRC error character<br>  <br><br>For a PE operation, contains the dead-track indications<br>  <br> |
| 10 | Serial Number (SN) | Read only | Contains the last four digits of the transport serial number<br>  <br> |
| 11 | Tape Control (TC) | Read/write | Contains the transport selection and configuration codes<br>  <br> |

### 2.1.1 Control Register [(CS1) Register $00_8$]

The control register is a read/write register (Figure 2-1) which receives operational commands from the Massbus controller via the control bus. This register operates in conjunction with the tape control register to control the operation of the selected transport.

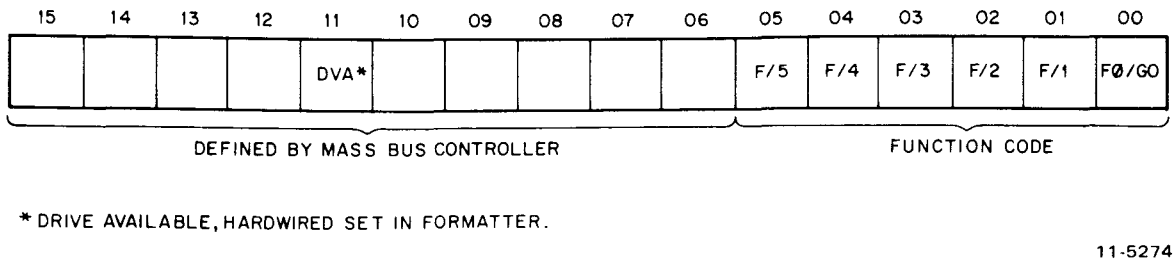



Figure 2-1 Control Register Format

The control register is shared with the Massbus controller. Bits 00 through 05 and bit 11 are located in the TM03. The remaining nine bits are located in the controller.

The TM03/transport responds to the 14 function codes listed in Table 2-2. If the control register is loaded with a function code (with GO bit set) that does not agree with those listed in the table, an illegal function error (ILF) is generated. Thus, an ILF is generated for codes $05_8$, $13_8$, $15_8$, $17_8$, $23_8$, $35_8$, etc., but not for $00_8$, $02_8$, $04_8$, $06_8$, $10_8$, $12_8$, etc.

**Table 2-2 Command Function Codes**

| Function Code F(0–5) (octal) | Operation | Description |
|---|---|---|
| 01 | No Op | Performs no operation. Clears GO bit in control register. |
| 03 | Rewind Off-Line* | 1. Initiates a rewind on selected transport and places it off-line.<br>2. Clears GO bit.<br>3. Sets the following bits in the status register:<br>Drive Ready (DRY)<br>Slave Status Change (SSC)<br>Attention Active (ATA) |
| 07 | Rewind | 1. Initiates a rewind to BOT marker on selected transport and clears the GO bit.<br>2. Sets DRY, PIP, and ATA bits in the status register during rewind.<br>3. When BOT is sensed, sets SSC and clears PIP. |

*Requires manual intervention to return transport on-line.

**Table 2-2 Command Function Codes (Cont)**

| Function Code F(0–5) (octal) | Operation | Description |
|---|---|---|
| 11 | Drive Clear | Similar to initialize. Resets all TM03 and selected transport logic. Does not affect unselected transports. |
| 21 | Read-In Preset | Presets the tape control register (R11) to select slave 0, odd parity, PDP-10 core dump format, and 800 bits/inch NRZI; then causes slave 0 to rewind. |
| 25 | Erase | Erases approximately 7.6 cm (3 inches) of tape. Clears GO bit and sets ATA on termination. |
| 27 | Write Tape Mark | Writes a special tape record on the selected transport. Clears GO bit and sets ATA bit on termination. |
| 31 | Space Forward | Moves tape forward (toward EOT) on the selected transport over the number of records specified by the frame count register. Aborts space operation if TM or EOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination. |
| 33 | Space Reverse | Moves tape in reverse (toward BOT) on the selected transport over the number of records specified by the frame count register. Aborts space operation if TM or BOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination. |
| 51 | Write Check Forward | Same as Read Forward. |
| 57 | Write Check Reverse | Same as Read Reverse. |
| 61 | Write Forward | Writes forward one tape record on the selected transport. Record length is determined by frame count register. Clears GO bit on command termination. |
| 71 | Read Forward | Reads forward one tape record on the selected transport. Clears GO bit on command termination. |
| 77 | Read Reverse | Reads reverse one tape record on the selected transport. Clears GO bit on command termination. |

### 2.1.2 Status Register [(DS) Register $01_8$]

The status register is a 16-bit, read-only register that stores the tape system status information. Figure 2-2 illustrates the status register format and Table 2-3 defines the bit positions. Although the status register multiplexer is located in the TM03, inputs to this multiplexer may be generated either by a selected transport, any transport, or the TM03 logic itself. Because of this fact, each bit position in Table 2-3 is identified by one or more of the following designators to indicate the origin of the input signal.

(SS) = Selected transport
(S) = Any transport
(M) = TM03 logic

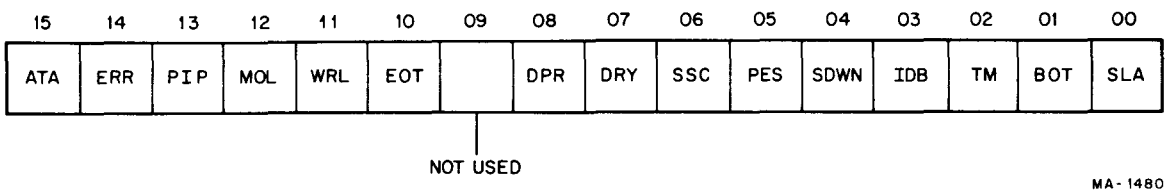



Figure 2-2 Status Register Format

**Table 2-3 Status Register Bit Positions**

| Bit Position | Name | Description |
|---|---|---|
| 00 (SS) | Slave Attention (SLA) | Indicates that a selected transport has come on-line. |
| 01 (SS) | Beginning of Tape (BOT) | Indicates that a selected transport has detected the BOT marker. |
| 02 (M) | Tape Mark (TM) | Indicates that a tape mark has been detected. Remains asserted until the next tape motion is initiated. |
| 03 (M) | Identification Burst (IDB) | Indicates that a phase-encoded (PE) identification burst has been detected. Asserted until a subsequent tape motion command is initiated. |
| 04 (SS) | Settle Down (SDWN) | Indicates that tape motion on the selected transport is stopping. |
| 05 (SS) | Phase-Encoded Status (PES) | Indicates that the selected transport is configured for PE operation. Is negated during NRZI operation. |
| 06 (S) | Slave Status Change (SSC) | Indicates that any transport has just gone on-line or off-line, or has completed a rewind operation. |

**Table 2-3 Status Register Bit Positions (Cont)**

| Bit Position | Name | Description |
|---|---|---|
| 07 (M) | Drive Ready (DRY) | Indicates that both the TM03 and the selected transport are ready to accept a command. |
| 08 (M) | Drive Present (DPR) | Hard-wired set. |
| 09 | Not used | |
| 10 (SS) | End of Tape (EOT) | Indicates that the selected transport has detected the EOT marker during forward tape motion. Is negated when the EOT marker is detected during reverse tape motion. |
| 11 (SS) | Write Lock (WRL) | Indicates that the selected transport is write protected. |
| 12 (SS) | Medium On-Line (MOL) | Indicates that the selected transport has tape loaded and is on-line. |
| 13 (M/SS) | Positioning in Progress (PIP) | Indicates that the selected transport is performing a tape motion operation. This bit is asserted by the TM03 (M) during a space or by the selected transport (SS) during a rewind. |
| 14 (M) | Composite Error (ERR) | Indicates that an error condition has occurred. Is asserted whenever any bit in the error register is set. |
| 15 (M) | Attention Active (ATA) | Is asserted whenever the ATTN interface signal is generated. Indicates one of the following:<br>1. The TM03 and the selected transport require servicing.<br>2. The TM03 and the selected transport have become ready after a nontransfer operation.<br>3. A transport status change has occurred. |

### 2.1.3 Error Register [(ER) Register $02_8$]

There are 16 different error conditions that can be detected in the TM03/transport system. The error register is a 16-bit, read-only register that stores all of the tape system error indications.

TM03/transport errors are categorized as Class A and Class B. A Class B error will terminate an in-progress data transfer; a Class A error will not. However, the Massbus controller is notified of any error during a data transfer by the immediate assertion of exception (EXC) on the Massbus. If the TM03/transport is not performing any operation, or is performing a rewind (i.e., the GO bit is clear), the controller is immediately notified of an error condition by the assertion of ATTN on the Massbus.

Figure 2-3 illustrates the error register format and Table 2-4 lists the error bit indicators.

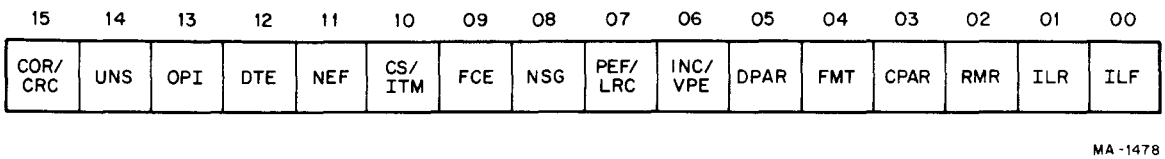



Figure 2-3 Error Register Format

**Table 2-4 Error Register Bit Indicators**

| Bit Position | Name | Description | Type |
|---|---|---|---|
| 00 | Illegal Function (ILF) | Indicates that an illegal function code has been transmitted. | Class B |
| 01 | Illegal Register (ILR) | Indicates that a read or write from a nonexistent register is attempted. | Class A |
| 02 | Register Modification Refuse (RMR) | Indicates that during a transport operation (GO = 1), a write into one of the registers is attempted. (Does not apply for the maintenance or attention summary registers.) | Class A |
| 03 | Control Bus Parity (CPAR) | Indicates that incorrect control bus parity is detected. | Class A |
| 04 | Format (FMT) | Indicates that a data transfer with an incorrect format code is attempted. When the M8915 bit fiddler is used, a FMT error could also indicate:<br>1. Microcode parity error<br>2. M8915 data parity error<br>3. Illegal microcode instruction | Class B |
| 05 | Data Bus Parity Error (DPAR) | Indicates that incorrect data bus parity has occurred. | Class A |

**Table 2-4 Error Register Bit Indicators (Cont)**

| Bit Position | Name | Description | Type |
|---|---|---|---|
| 06 | Incorrectable Data Error or Vertical Parity Error (INC/VPE) | During a PE read operation, indicates that one of the following has occurred:<br>1. Multiple dead tracks<br>2. Dead tracks without parity errors<br>3. Parity errors without dead tracks<br>4. Skew overflow<br>5. Parity error in bit fiddler.<br>During an NRZI read operation, indicates that a vertical parity error has occurred or that data has occurred after the skew delay is over. | Class A |
| 07 | Format Error or LRC Error (PEF/LRC) | During a PE read operation, indicates than an incorrect preamble or postamble is detected.<br>During an NRZI write operation, indicates that the LRCC read off the tape does not match the LRCC computed from the characters read off the tape. | Class A |
| 08 | Nonstandard Gap (NSG) | Indicates that a tape character is detected during the first half of the end-of-record gap while a write operation is in progress. Never set during a read operation. | Class A |
| 09 | Frame Count Error (FCE) | Indicates that a space operation has terminated and the frame counter is not cleared. Also asserted when the Massbus controller fails to negate RUN when the TM03 asserts EBL. | Class A |
| 10 | Correctable Skew or Illegal Tape Mark (CS/ITM) | During a PE read operation, indicates that excessive but correctable skew is detected. (This condition is only a warning and does not indicate bad data.)<br>During an NRZI read, indicates that characters not legally a tape mark have been read and recognized as a tape mark (e.g., such as a record less than the 10-character minimum). | Class A |
| 11 | Nonexecutable Function (NEF) | Indicates one of the following:<br>1. A write operation is attempted on a write-protected transport.<br>2. A space reverse, read reverse, or write check reverse is attempted when the tape is at BOT.<br>3. The DEN2 bit in the tape control register does not agree with the PES status bit during a write operation. | Class B |

Table 2-4 Error Register Bit Indicators (Cont)

| Bit Position | Name | Description | Type |
|---|---|---|---|
| | | 4. A space or write operation is attempted when FCS = 0 in the tape control register.<br>5. A write operation is attempted with DEN2 = 0 in the tape control register (NRZI mode) and the 2's complement of a number less than $13_8$ is in the frame count register.<br>6. The type of phase-locked loop modules (M8901-YB, YC, or YD) do not agree with the type of transport as specified by the drive type register. This indicates that the TM03 and the transport are not operating at the same tape speed. | |
| 12 | Drive Timing Error (DTE) | Indicates one of the following:<br>1. During a write operation, WCLK was not received from the Massbus controller in time to provide a valid tape character.<br>2. A data transfer (read/write) was attempted when the data bus of the Massbus was already occupied. | Class B |
| 13 | Operation Incomplete (OPI) | During a read/write or space operation, indicates that an end of record has not been detected within 7 seconds from command initiation. Also set during a read reverse or a space reverse if BOT is detected. | Class B |
| 14 | Unsafe (UNS) | Indicates one of the following:<br>1. A program-controlled operation is attempted on a selected transport that is not on-line.<br>2. An imminent power failure is detected (AC LO). | Class B |
| 15 | Correctable Data Error or CRC Error (COR/CRC) | During a PE read operation, indicates that a single dead track has occurred.<br>During an NRZI operation, indicates that the CRCC read off the tape does not match the CRCC computed from the data read off the tape. | Class A |

### 2.1.4 Maintenance Register [(MR) Register $03_8$]

The maintenance register (M8905-YB) is a 16-bit, read/write register (Figure 2-4) that allows complete diagnostic testing of the TM03 data paths and error detection circuitry. The maintenance register can configure the data paths into five wraparound loops, each loop testing certain TM03 circuits. The maintenance register data field is part of these loops, and is used to read or write test data into the TM03. Table 2-5 briefly describes the bits of the maintenance register.

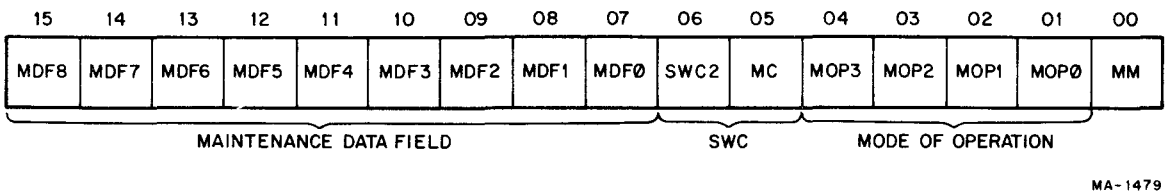



Figure 2-4 Maintenance Register Format

**Table 2-5 Maintenance Register Bit Positions**

| Bit Position | Name | Description |
|---|---|---|
| 00 | Maintenance Mode (MM) | When set, configures the TM03 for maintenance mode operation. |
| 01–04 | Maintenance Operation Code (MOP0–3) | Controls command execution during the maintenance mode. (MM and MOP function together to alter normal command execution during maintenance mode operation.) |
| 05 | Maintenance Clock (MC) | Controls data sequencing through the TM03 data path in maintenance mode. |
| 06 | Tape Speed Clock (SWC2) | A clock signal generated by the selected slave. Frequency depends on the tape speed of the selected slave. Used to monitor maintenance mode read operations. |
| 07–15 | Maintenance Data Field (MDF0–8) | Buffers the data generated during wraparound operations.<br>At the end of normal NRZI transfers, contains the LRC of the last record. |

### 2.1.5 Attention Summary Register [(AS) Register $04_8$]

The attention summary register (M8909-YA) is a read/write "pseudo-register" that consists of from one to eight bits, depending on the number of drives (TM03s) on the Massbus. The term "pseudo-register" refers to the fact that only one register bit position is physically contained in each TM03. This bit position reflects the state of the ATA status bit for that TM03. Hence, bit position 0 of the attention summary register is generated by the ATA bit of TM03 No. 0; bit position 1 is generated by the ATA bit of TM03 No. 1, and so on to bit 7. Bits 8 through 15 are not used.

Unlike the other TM03 registers, the attention summary register is directly selected by the controller without first addressing a particular TM03. Thus, for a single attention summary register read operation, every TM03 in the system responds by placing the state of its ATA bit in the appropriate bit position on the control bus and disabling its remaining 15 control bus transmitters. This control bus configuration appears as a single register output which collectively informs the controller of all TM03s that require attention (i.e., ATA = 1). The controller can then selectively examine the error or status registers of each of the affected TM03s to determine the cause of the individual attention conditions.

The controller can also write into the attention summary register; however, the significance of the bits being written is unusual. Writing a 1 into a bit position resets the ATA bit in the TM03 assigned to that bit position; however, writing a 0 has no effect. This unique writing scheme allows the controller to reset, after inspection, all summary bits that were set, without accidentally resetting those bits that may have become set in the meantime. The following table illustrates the effects of writing into an attention summary bit position.

| ATA Bit Before | Summary Bit Written | ATA Bit After |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

### 2.1.6 Frame Count Register [(FC) Register $05_8$]

The frame count register (M8909-YA) is a 16-bit, read/write register that counts tape events. During a data transfer operation (read/write), this register is incremented each time a tape character is transferred to or from the tape. However, during a space operation, this register is incremented each time a record is detected. The register output may be read by the controller at any time, but the controller can only write into this register when the transport is not performing a space operation or data transfer (GO negated).

For a write operation, the frame count register is loaded, prior to write initiation, with the 2's complement of the number of tape characters to be written. During the writing process, the frame count register is incremented each time a tape character is recorded. Normal write data transfer termination is accomplished when the frame count register overflows to zero. For a space operation, the frame count register functions similarly to a write, except it is loaded with the 2's complement of the number of records to be spaced and is then incremented each time a record is detected. Space termination is accomplished when the register overflows to zero. For a read operation, this register is automatically reset prior to read initiation. The register is then incremented each time a tape character is read. Thus, at the end of the read operation, the frame count register contains a count of the number of characters read.

### 2.1.7 Drive Type Register [(DT) Register $06_8$]

The drive type register (M8933) is a 16-bit, read-only register, the content of which identifies the particular type of formatter and transport being used. When a read from the drive type register is performed, the register output is applied to the appropriate multiplexer bit positions. Bits 0 through 8 (DT0–8) of the drive type register identify the type and status of the selected formatter and transport. If a nonexistent transport is selected or if the selected transport is not powered up, DT0–8 will contain $050_8$. If the selected transport is powered up, the drive type code will be $05X_8$, where X represents bits DT0, DT1, and DT2 and indicates the type of slave. Bits DT0 through DT8 are coded as shown below for the TM03. Neither INIT nor drive clear can affect bits DT0–8.

| DT8 | DT7 | DT6 | DT5* | DT4 | DT3 | DT2 | DT1 | DT0 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | = | Unselected slave |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | = | 114.3 cm/second (45 in/s), slave selected |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | = | 190.5 cm/second (75 in/s), slave selected |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | = | 317.5 cm/second (125 in/s), slave selected |

*DT5 will indicate the type of formatter being used.
DT5 = 0 = TM02
DT5 = 1 = TM03

Figure 2-5 illustrates the drive type register format and Table 2-6 briefly describes each bit position.

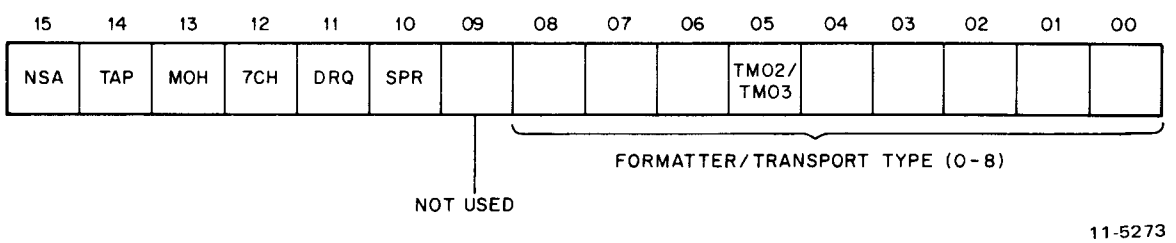



Figure 2-5 Drive Type Register Format

Table 2-6 Drive Type Register Bit Positions

| Bit Position | Name | Description |
|---|---|---|
| 00–08 | Drive Type (DT0–8) | Specifies the type of formatter and transport. |
| 09 | – | Spare bit. |
| 10 | Slave Present (SPR) | Asserted when a transport is powered up and has been assigned the selection code contained in the tape control register. |
| 11 | Drive Request Required (DRQ) | Always negated to indicate that the device is a single-port unit. |
| 12 | 7-Channel (7CH) | Always negated. The TM03 does not interface with 7-channel transports. |
| 13 | Moving Head (MOH) | Always negated to indicate that the device is not a moving head unit. |
| 14 | Tape Drive (TAP) | Always asserted to indicate that the device is a tape transport. |
| 15 | Not Sector Addressed (NSA) | Always asserted to indicate that the device is not sector addressable. |

### 2.1.8 Check Character Register [(CK) Register $07_8$]

The check character register (M8905-YB) is a 9-bit, read-only register that permits the programmer to check the validity of a data transfer. At the end of an NRZI read operation, this register contains the CRCC for that operation. Hence, the programmer can determine if the CRCC generator logic is functioning properly. At the end of a PE read operation, however, this register contains a dead track indication (DT = 1) of any track that may have dropped one or more bits during the operation.

Figure 2-6 illustrates the check character register format for both NRZI and PE modes.

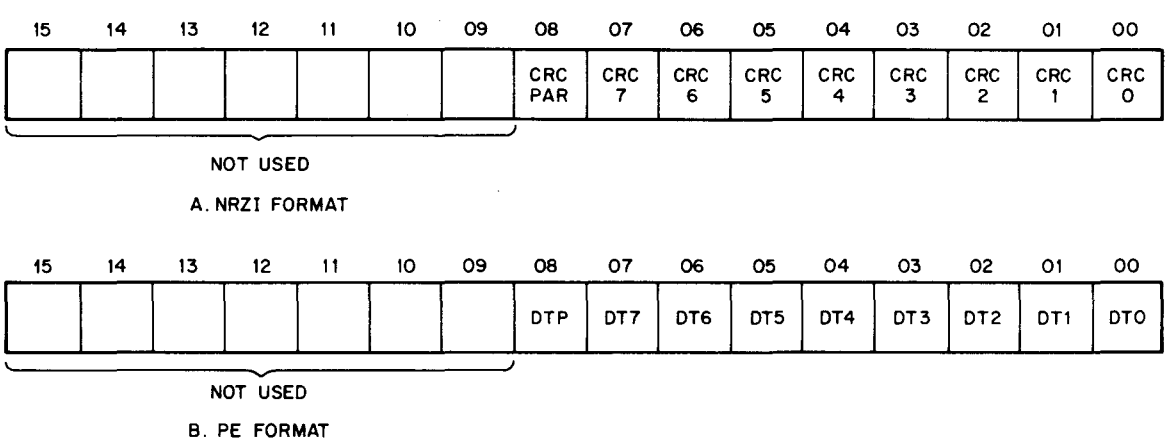



Figure 2-6 Check Character Register Format

### 2.1.9 Serial Number Register [(SN) Register $10_8$]

The serial number register is a 16-bit, read-only register that contains a BCD representation of the 4 least-significant digits of the transport serial number.

Figure 2-7 illustrates the serial number register format.

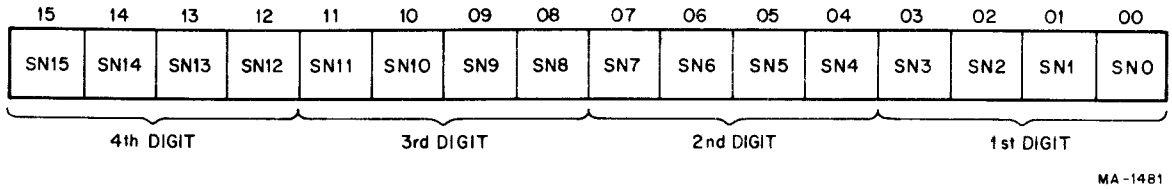



Figure 2-7 Serial Number Register Format

### 2.1.10 Tape Control Register [(TC) Register $11_8$]

The tape control register (M8905-YB) is a 16-bit, read/write register that selects an existing transport and configures it to a particular operational mode.

Figure 2-8 illustrates the tape control register and Table 2-7 briefly describes each bit position.

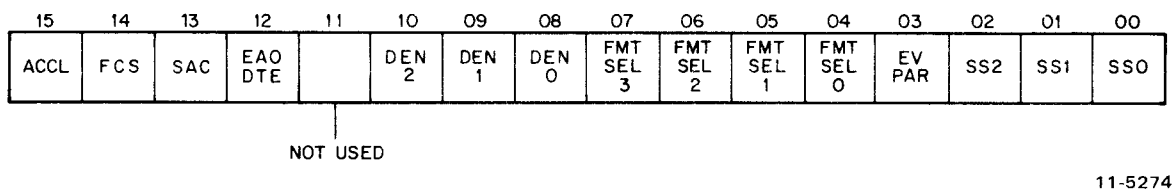



Figure 2-8 Tape Control Register Format

**Table 2-7 Tape Control Register Bit Positions**

| Bit Position | Name | Description |
|---|---|---|
| 00–02 | Slave Select (SS0–2) | Specifies the unit number of the transport to be used. |
| 03 | Even Parity (EV PAR) | When set for NRZI operation, even parity is written or read from tape. Ignored during PE operation. (PE operations are always odd parity.) |

**Table 2-7 Tape Control Register Bit Positions(Cont)**

| Bit Position | Name | Description |
|---|---|---|
| 04–07 | Format Select (FMT SEL0–3) | Specifies Massbus-to-tape character formatting during a write operation, or tape character-to-Massbus formatting during a read operation.<br><br>Format codes are as follows.*<br><br>0000–PDP-10 Format: "10-Core Dump"<br>0001–PDP-15 Format: "15-Core Dump"<br>0011–PDP-10 Format: "10-Compatible"<br>1100–PDP-11 Format: "11-Normal"<br>1101–PDP-11 Format: "11-Core Dump"<br>1110–PDP-15 Format: "15-Normal"<br>1111–PDP-11 Format: Reserved |
| 08–10 | Density Select (DEN0–2) | Specifies the tape character density during read or write operations as follows.†<br><br>**DEN2 DEN1 DEN0 Density (bits/inch)**<br><br>0 1 1 800 NRZI<br>1 0 0 1600 PE<br>1 0 1 Reserved<br>1 1 0 Reserved<br>1 1 1 Reserved |
| 11 | Not used | |
| 12 | Enable Abort on Data Transfer Errors (EAODTE) | When set, immediately aborts a write or read operation for one of the following errors.<br><br>1. COR/CRC – Error register bit 15.<br>2. PEF/LRC – Error register bit 7.<br>3. INC/VPE – Error register bit 6.<br>4. DPAR – Error register bit 5. |
| 13 | Slave Address Change (SAC) | Asserts whenever the slave select bits of the TC register are changed. Negates on the next drive set pulse. |

* 1. Codes 0000 and 0011 use an M8915 data formatting module.

2. Codes 1100 and 1110 use an M8906 data formatting module.

3. All other format codes are invalid. An invalid code causes a format error (FMT – error register bit 4) when a data transfer command with GO = 1 is loaded.

†DEN2 bit selects 800 or 1600 bits/in. DEN1 and DEN0 bits are not used. DEN codes $5_8$, $6_8$, and $7_8$ are reserved for future use.

Table 2-7 Tape Control Register Bit Positions(Cont)

| Bit Position | Name | Description |
|---|---|---|
| 14 | Frame Count Status (FCS) | Is normally set at the end of a write into the frame count register. However, if FCS = 0, and a space or write command with GO = 1 is loaded, a nonexecutable function (NEF) error is generated and the command is not executed. Is reset when frame count register overflows. |
| 15 | Acceleration (ACCL) | This read-only bit is asserted when the transport is not actively reading or writing data. |

## 2.2 DATA FORMATS

This section illustrates how the TM03 maps Massbus transfers onto tape during write operations and how tape characters are mapped onto the Massbus data lines during read operations. PDP-10, PDP-11, and PDP-15 processor bits are defined and the location of these bits during a Massbus transfer is shown. The pack/unpack format of the processor words into tape frames is shown for the various formatting modes.

### 2.2.1 Massbus/TM03 Transfers

Consider a single record that is to be read from or written on tape. Assume four Massbus transfers will occur during the writing (reading) of this record and that the contents of the first transfer will be $111111_8$, the contents of the second transfer will be $222222_8$, the third $333333_8$, and the fourth $444444_8$. If the write (or read) is in a forward direction, the four Massbus/TM03 transfers will be:

$111111_8$ - First transfer
$222222_8$ - Second transfer
$333333_8$ - Third transfer
$444444_8$ - Fourth transfer.

If the read is in a reverse direction, the four Massbus/TM03 transfers will be:

$444444_8$ - First transfer
$333333_8$ - Second transfer
$222222_8$ - Third transfer
$111111_8$ - Fourth transfer.

Words transferred between memory and the TM03 are formatted on the Massbus according to which processor is used. Two transfers are required to transmit a 36-bit PDP-10 word while only a single transfer is required for a 16-bit PDP-11 word or an 18-bit PDP-15 word. The word formats on the Massbus for the PDP-10, PDP-11, and PDP-15 are shown in Tables 2-8, 2-9 and 2-10. The 18 data lines on the Massbus are designated D0–D17.

Table 2-8 PDP-10 Massbus Word Format

| D17–D0 | Massbus Data Lines |
|---|---|
| B0–B17 | First Massbus Transfer* |
| B18–B35 | Second Massbus Transfer* |

B0 = MSB
B35 = LSB

*In read reverse, the order of Massbus transfers are reversed, i.e., B18–B35 = first transfer and B0–B17 = second transfer.

Table 2-9 PDP-11 Massbus Word Format

| D17 | D16 | D15–D0 | Massbus Data Lines |
|---|---|---|---|
| | | R15–R0 | Massbus Transfer |

R0 = LSB
R15 = MSB

Table 2-10 PDP-15 Massbus Word Format

| D17–D0 | Massbus Data Lines |
|---|---|
| N0–N17 | Massbus Transfer |

N0 = MSB
N17 = LSB

### 2.2.2 TM03/Tape Frame Packing

In a write operation, the processor data word in the TM03 is disassembled and packed onto tape in a number of tape characters or frames. The number of frames depends on the processor used and the mode of operation. In a read operation, the tape frames are read off tape (unpacked) and assembled into a data word for Massbus transfer. The packing/unpacking formats are shown in Tables 2-11 through 2-16 for the PDP-10, PDP-11, and PDP-15 processors in various format modes. During a read-reverse operation, the frames are read off tape in reverse order.

Table 2-11 PDP-10 Compatibility Mode – Format Code 0011

| Tape Frames | Tape Track Positions | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | TP | T7 (MSB) | T6 | T5 | T4 | T3 | T2 | T1 | T0 (LSB) |
| 1 | P | B0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 |
| 2 | P | B8 | B9 | B10 | B11 | B12 | B13 | B14 | B15 |
| 3 | P | B16 | B17 | B18 | B19 | B20 | B21 | B22 | B23 |
| 4 | P | B24 | B25 | B26 | B27 | B28 | B29 | B30 | B31 |

Table 2-12 PDP-10 Core Dump Mode – Format Code 0000

| Tape Frames | Tape Track Positions | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | TP | T7 (MSB) | T6 | T5 | T4 | T3 | T2 | T1 | T0 (LSB) |
| 1 | P | B0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 |
| 2 | P | B8 | B9 | B10 | B11 | B12 | B13 | B14 | B15 |
| 3 | P | B16 | B17 | B18 | B19 | B20 | B21 | B22 | B23 |
| 4 | P | B24 | B25 | B26 | B27 | B28 | B29 | B30 | B31 |
| 5 | P | 0 | 0 | 0 | 0 | B32 | B33 | B34 | B35 |

**Table 2-13 PDP-11 Normal Mode – Format Code 1100**

| Tape Frames | Tape Track Positions | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | TP | T7 (MSB) | T6 | T5 | T4 | T3 | T2 | T1 | T0 (LSB) |
| 1 | P | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| 2 | P | R15 | R14 | R13 | R12 | R11 | R10 | R9 | R8 |

**Table 2-14 PDP-11 Core Dump Mode – Format Code 1101**

| Tape Frames | Tape Track Positions | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | TP | T7 | T6 | T5 | T4 | T3 (MSB) | T2 | T1 | T0 (LSB) |
| 1 | P | ~~b~~ | ~~b~~ | ~~b~~ | ~~b~~ | R3 | R2 | R1 | R0 |
| 2 | P | ~~b~~ | ~~b~~ | ~~b~~ | ~~b~~ | R7 | R6 | R5 | R4 |
| 3 | P | ~~b~~ | ~~b~~ | ~~b~~ | ~~b~~ | R11 | R10 | R9 | R8 |
| 4 | P | ~~b~~ | ~~b~~ | ~~b~~ | ~~b~~ | R15 | R14 | R13 | R12 |

**Table 2-15 PDP-15 Normal Mode – Format Code 1110**

| Tape Frames | Tape Track Positions | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | TP | T7 (MSB) | T6 | T5 | T4 | T3 | T2 | T1 | T0 (LSB) |
| 1 | P | N2 | N3 | N4 | N5 | N6 | N7 | N8 | N9 |
| 2 | P | N10 | N11 | N12 | N13 | N14 | N15 | N16 | N17 |

**Table 2-16 PDP-15 Core Dump Mode – Format Code 0001**

| Tape Frames | Tape Track Positions | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | TP | T7 | T6 | T5 (MSB) | T4 | T3 | T2 | T1 | T0 (LSB) |
| 1 | P | ~~b~~ | ~~b~~ | N0 | N1 | N2 | N3 | N4 | N5 |
| 2 | P | ~~b~~ | ~~b~~ | N6 | N7 | N8 | N9 | N10 | N11 |
| 3 | P | ~~b~~ | ~~b~~ | N12 | N13 | N14 | N15 | N16 | N17 |

It is important to note that in any given transfer, the frame count register must contain the 2's complement of the number of frames required to transfer complete processor words to or from tape. For example, in the PDP-10 core dump mode shown in Table 2-12, it takes five tape frames to read or write a word on tape. The frame count register must be loaded with the 2's complement of 5 times the number of words read or written; e.g.,

A 25-word transfer = 25 × 5 = 125 tape frames
A 26-word transfer = 26 × 5 = 130 tape frames
A 27-word transfer = 27 × 5 = 135 tape frames.

## 2.3 COMMAND FUNCTIONS

There are 14 commands implemented by a TM03/transport system. The commands are listed and briefly described in Table 2-17. Function codes not listed in Table 2-17 are treated as illegal functions. Commands, other than drive clear, will be executed only if they are directed to an on-line transport.

Paragraphs 2.3.1 through 2.3.12 provide additional information about the command functions.

### 2.3.1 No-Op

This command causes immediate reset of the GO bit and assertion of DRY. No tape motion or status change occurs in the selected slave. No attention is generated.

### 2.3.2 Rewind, Off-Line

The selected slave begins rewinding and goes off-line. GO is reset and DRY, SSC, and ATA become asserted (SSC becomes asserted because the slave has gone off-line).

Operator intervention is required to bring the slave back on-line.

**NOTE**

**This command generates only one attention, whereas a rewind command may generate either one or two attentions.**

**Table 2-17 Command Functions**

| Function Code F (0–5) (octal) | Operation | Description |
|---|---|---|
| 01 | No Op | Performs no operation. Clears GO bit in control register. |
| 03 | Rewind Off-Line* | 1. Initiates a rewind on selected transport and places it off-line.<br>2. Clears GO bit.<br>3. Sets the following bits in the status register:<br>Drive Ready (DRY)<br>Slave Status Change (SSC)<br>Attention Active (ATA) |
| 07 | Rewind | 1. Initiates a rewind to BOT marker on selected transport and clears the GO bit.<br>2. Sets DRY, PIP, and ATA bits in the status register during rewind.<br>3. When BOT is sensed, sets SSC and clears PIP. |
| 11 | Drive Clear | Similar to initialize. Resets all TM03 and selected transport logic. Does not affect unselected transports. |

*Requires manual intervention to return transport on-line.

Table 2-17 Command Functions (Cont)

| Function Code F (0–5) (octal) | Operation | Description |
|---|---|---|
| 21 | Read-In Preset | Presets the tape control register (R11) to select slave 0, odd parity, PDP-10 core dump format, and 800 bit/inch NRZI; then causes slave 0 to rewind. |
| 25 | Erase | Erases approximately 7.6 cm (3 inches) of tape. Clears GO bit and sets ATA on termination. |
| 27 | Write Tape Mark | Writes a special tape record on the selected transport. Clears GO bit and sets ATA bit on termination. |
| 31 | Space Forward | Moves tape forward (toward EOT) on the selected transport over the number of records specified by the frame count register. Aborts space operation if TM or EOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination. |
| 33 | Space Reverse | Moves tape in reverse (toward BOT) on the selected transport over the number of records specified by the frame count register. Aborts space operation if TM or BOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination. |
| 51 | Write Check Forward | Same as read forward. |
| 57 | Write Check Reverse | Same as read reverse. |
| 61 | Write Forward | Writes forward one tape record on the selected transport. Record length is determined by frame count register. Clears GO bit on command termination. |
| 71 | Read Forward | Reads forward one tape record on the selected transport. Clears GO bit on command termination. |
| 77 | Read Reverse | Reads reverse one tape record on the selected transport. Clears GO bit on command termination. |

### 2.3.3 Rewind

The selected slave executes a rewind back to the reflective strip marking beginning of tape (BOT). Sequencing of a rewind command proceeds as follows.

1. When a rewind command is loaded with GO = 1, the TM03 first checks the settle-down (SDWN) bit in the status register.

   a. If SDWN = 0, the selected slave immediately begins rewinding.

   b. If SDWN = 1 (indicating that the selected slave is slowing to a halt after completion of a prior command) and the last command executed called for tape motion in the reverse direction, the selected slave immediately begins rewinding.

   c. If SDWN = 1 and the last command executed called for tape motion in the forward direction, the TM03 delays execution of the rewind until SDWN = 0, indicating that the selected slave has stopped.

2. As soon as the slave has recognized the rewind command, the TM03 returns to the ready state and DRY and ATA become asserted. In steps 1a and b above, the time from initiation of the control bus write sequence which loads the rewind command, until reassertion of DRY is 2 $\mu$s. In step 1c above, reassertion of DRY may not occur for up to 15 ms after initiation of the rewind sequence.

3. Once the selected slave reaches BOT, it will cause slave status change (SSC) and ATA to become asserted. If selected slave was already at BOT when the rewind command was loaded, the ATA condition generated in step 2 above and the ATA condition generated in this step will occur together.

4. The following examples will indicate the states of important status bits during a rewind sequence. (The possibility of SLA and SSC becoming asserted due to status changes in slaves other than the rewinding slave will not be treated.)

   a. During the time between reception of the rewind command and initiation of a rewind by the selected slave: DRY = 0, ATA = 0, SSC = 0, SLA = 0, SDWN = 0 or 1, PIP = 0

   b. After initiation of the rewind, if the selected slave was already at BOT: DRY = 1, ATA = 1, SSC = 1, SLA = 0, SDWN = 0, PIP = 0, BOT = 1

   c. After initiation of the rewind, if the selected slave was not at BOT: DRY = 1, ATA = 1, SSC = 0, SLA = 0, PIP = 1

   d. After completion of the rewind, if the selected slave was not already at BOT: DRY = 1, ATA = 1, SLA = 0, SSC = 1, SDWN = 0, PIP = 0, BOT = 1 (identical to case in step 4b above)

   Note that SSC is an indication of status changes in at least one slave. Thus, it should not be cleared until all slaves have been polled to confirm their status.

5. In a multi-slave system, the presence of rewinding slaves on the TM03 slave bus does not interfere with the execution of commands by selected slaves that are not rewinding. Any command recognized as a legal function by the TM03 may be issued to a rewinding slave if DRY = 1. If this is done, the following sequence of events will occur.

   a. When command is loaded, GO becomes asserted.

   b. Execution of command is deferred until rewind is complete (until PIP becomes negated); GO remains asserted.

   c. When rewind reaches completion, PIP becomes negated and SSC becomes asserted; command execution is initiated.

   d. When command reaches completion, ATA becomes asserted because of prior assertion of SSC.

### 2.3.4 Drive Clear

This command performs a reset on the TM03 and selected slave but does not affect unselected slaves. Unlike any other command, drive clear can be executed on the TM03/transport even if MOL = 0.

**2.3.4.1 Drive Clear Resets** – A drive clear command resets SLA in the selected slave, SSC if no other slaves have current attention-demanding conditions, TM, IDB, ERR, and ATA in the status register. The drive clear command also resets all but bit 6 of the maintenance register, FCS in the tape control register, all bits in the error register except bit 14 (UNS), and UNS if the TM03 is not experiencing a power-fail.

The time from reception of a drive clear command to reassertion of DRY is 2 $\mu$s. If drive clear is issued to a TM03 that is experiencing a power-fail, ATA and ERR will become asserted when DRY becomes asserted. Drive clear cannot affect a rewinding slave.

**2.3.4.2 Drive Clear versus Initialize (INIT)** – INIT differs from drive clear in the following aspects.

1. INIT may be issued at any time.
2. INIT affects all slaves, not just the selected slave.
3. INIT will abort any NRZI error correction cycle that may be in progress.

INIT resets GO in the control register; SLA (all slaves), SSC, TM, IDB, ERR, and ATA in the status register; all but bit 6 of the maintenance register; FCS in the tape control register; and all bits in the error register except bit 14 (UNS) and UNS if the TM03 is not experiencing a power-fail. INIT sets DRY. INIT will also clear all NRZI error correction cycles. INIT, like drive clear, requires 2 $\mu$s for completion. If the TM03 is experiencing a power-fail when INIT is issued, ATA and ERR will be asserted at the completion of the system reset.

INIT has no effect on a rewinding slave, but will immediately halt a slave that is executing any other command.

**NOTE**

**Issuing an INIT during a write operation destroys the record being written. The only safe recovery from INIT is a rewind.**

### 2.3.5 Read-In Preset

This command is intended to be used in bootstrap operations. Read-in preset does the following.

1. Presets the tape control register in the TM03 to select slave 0, odd parity, PDP-10 core dump format, and 800 bits/inch

2. Causes slave 0 to begin rewinding in accordance with the guidelines outlined in Paragraph 2.3.3

### 2.3.6 Erase

The selected slave writes an extended 7.6 cm (3 inch) interrecord gap and stops. ATA becomes asserted when DRY becomes asserted.

### 2.3.7 Write Tape Mark

The selected slave writes an extended 7.6 cm (3 inch) interrecord gap, an industry-compatible tape mark, and stops. ATA becomes aserted when DRY becomes asserted.

If a detectable tape mark was written (as is normally the case), TM (bit 2 of the status register) will be asserted at the completion of the operation.

### 2.3.8 Space Forward

The selected slave spaces forward (toward EOT) over the number of records specified by the contents of the frame count register. Detection of a tape mark (TM) or end of tape (END PT) causes a space command to be aborted. In this case, the frame count register reflects the number of records spaced over. (The register is not incremented by the tape mark.)

All data errors are inhibited during this operation. DRY becomes asserted when operation is complete and a valid interrecord gap found. ATA becomes asserted when DRY asserts.

Once the reflective marker indicating end of tape has been detected, it is possible to space forward *only* one record at a time. Attempts to space forward over more than one record (i.e., initiate space forward with a number other than -1 in the frame count register) will cause the transport to space over one record and halt, displaying frame count error in the error register.

### 2.3.9 Space Reverse

Space reverse is similar to space forward, except that detection of BOT or TM will abort the operation, and the direction of tape motion is in the reverse direction (toward BOT).

Whenever a space reverse is to be executed while END PT is asserted, it is advisable to space reverse over only one record at a time (as in Paragraph 2.3.8).

### 2.3.10 Read Forward/Write Check Forward

The tape system makes no distinction between these commands. The tape system reads one record. When either of these commands results in the detection of a tape mark, the following will occur.

1. In PE mode, no data transfers will be initiated by the TM03.

2. In NRZI mode, the TM03 will transfer both the tape mark character and its LRC character to the controller.

### 2.3.11 Read Reverse/Write Check Reverse

Read reverse/write check reverse is similar to read (write check) forward, with the following exceptions.

1. Data transfers occur as outlined in Paragraph 2.2.
2. Tape motion is in the reverse direction.
3. Regardless of mode, no data transfer will occur upon detection of a tape mark.

### 2.3.12 Write

In the write command, the transport writes one record while moving forward. The record length is controlled by the frame count register.

## 2.4 NRZI ERROR CORRECTION

Figure 2-9 is a simplified flow diagram of the error correction process. The process consists of three cycles.

1. Read the record in the forward direction and get a CRC error.

2. Read (or space) in reverse over the faulty record and attempt to compute the track in error.

3. If the track in error was computed (all errors are contained in a single track), make a forward read over the faulty record during which error correction is accomplished.

Figure 2-10 is a flow diagram of the NRZI error correction algorithm. During a NRZI read forward operation, data characters from tape are input into a CRC generator where a CRC character is developed. At the end of the record, the CRC character read from tape is compared to the generated CRC character. If a match is not obtained, a CRC error is asserted. The program then initiates the error correction process by changing the mode to reverse read or reverse space. The reverse space mode must be selected if it is desired to reverse the tape more than one record, e.g., to move the faulty record over the tape cleaner. If a reverse read was in progress when the CRC error was detected, the mode must be changed to forward read and the faulty record read again. The error correction process can be initiated only when a CRC error is sensed in a forward direction.

As the faulty record is reverse read (or reverse spaced), the track in error is computed. If more than one track is in error, the hardware will not select a faulty track and the error is determined to be uncorrectable. If the errors are all in the same track, a track in error is computed. In either case, the correction cycle portion of the error correction process is performed.

When the correction cycle is started, the tape must be positioned at the correct location (i.e., at the faulty record) so that the error correction is performed on the proper record. If the read reverse mode was chosen in the preceding paragraph, only one record (the faulty record) can be reverse read. An attempt to read reverse more than one record causes the hardware to abort the error correction process. If the space reverse mode was chosen, any number of records may be spaced while the error correction process is put on "hold." If the program spaced N records in reverse, it must space N–1 records forward before read forward is asserted. (The assertion of read forward initiates the correction cycle portion of the process.) Otherwise, the hardware will attempt the error correction on the wrong record.

If the error is uncorrectable, no correction will be accomplished during the correction cycle. The faulty record is reread and CRC error is again asserted. In this case, software retry procedures or other corrective action the program may direct will be instituted.

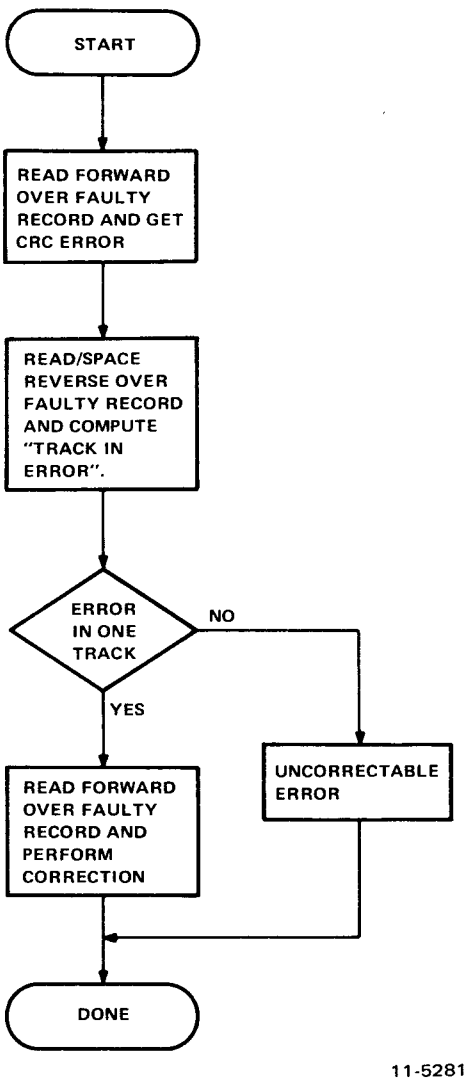



Figure 2-9 Simplified NRZI Error Correction Flow Diagram

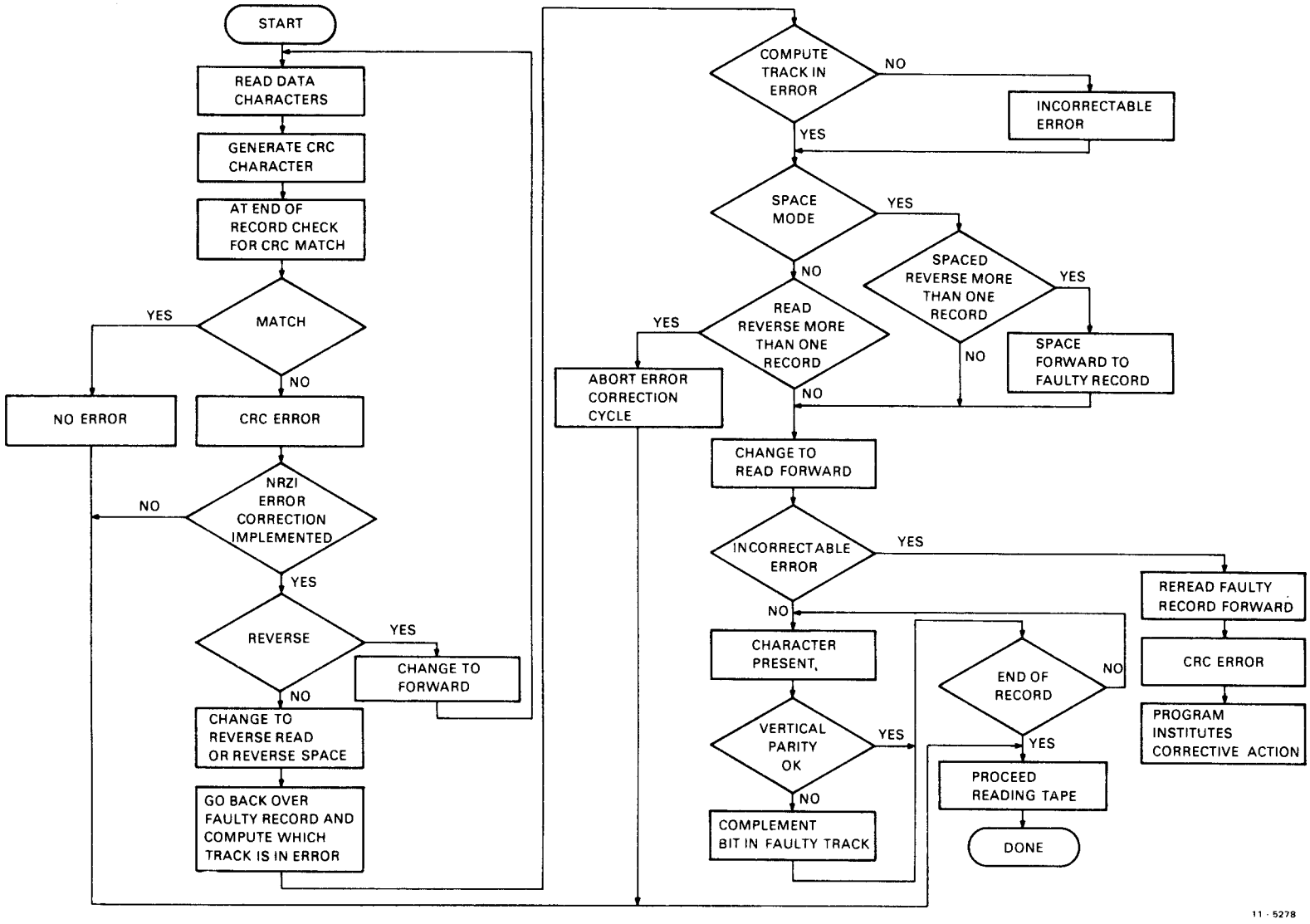



Figure 2-10 NRZI Error Correction Flow Diagram

If an erroneous track was detected, correction is accomplished during the correction cycle. This is done by checking each character for vertical parity. Any character having a vertical parity error has the bit corresponding to the track in error complemented. Thus, any number of errors are corrected so long as they all occur in the same track.

When the end of record is sensed, the error correction process is terminated and the reading operation is continued. It is significant to note that the CRC character is treated as part of the record and, therefore, is checked for vertical parity and, if necessary, corrected.

## 2.5 PROGRAMMING NOTES

Points to consider in programming the TM03 formatter are listed below.

### 2.5.1 NRZI Error Correction

1. If in reverse read when a CRC error is sensed, the mode must be changed to forward read. The error correction process is entered only when a CRC error is sensed in a forward direction.

2. When a forward CRC error is sensed, the direction must be changed to reverse to initiate the error correction process.

3. If reverse read is used in item 2 above, only one record can be read and then the direction must be changed to forward read.

4. If reverse space is used in item 2 above, any number of records (N) may be reverse spaced; however, N–1 records must be forward spaced before forward read is asserted.

5. If the error is uncorrectable, the program must dictate any corrective action.

### 2.5.2 Auto Density Select

1. The program does not control the read mode (density). The presence or absence of an ID burst on the tape selects either PE read or NRZI read for the entire tape.

2. The program can select either write PE or write NRZI at BOT but cannot switch modes at a later point on the tape.

3. If the mode (density) is changed and a rewind off-line command is given, a nonexecutable function error will result.

### 2.5.3 Other Notes

1. All slaves interfacing to a particular TM03 must be operating at the same speed.

# CHAPTER 3
# INSTALLATION

## 3.1 SITE PLANNING AND CONSIDERATIONS

Since the TM03 is always contained within a transport cabinet, the site planning aspects are accomplished when site planning for the cabinet is considered. The additional power required to supply the TM03 is 300 W.

## 3.2 UNPACKING

There are no unpacking instructions for the TM03 since it is shipped already mounted inside the transport cabinet. The TM03 cables may be shipped separately and are the only items that must be unpacked.

## 3.3 INSPECTION

Check inside the transport cabinet that the TM03 is securely mounted on its platform and that there is no apparent damage to the TM03 housing. Check that there are the proper number of BC06R-X cables of the correct length for the particular installation (X = length of cable). Check cables for damage both at the connectors and over the length of the cable body.

## 3.4 INSTALLATION PROCEDURES

Installation consists of cabling up either six or nine BC06R cables to the TM03. The number of cables depends on the number of TM03s in the system and the type of cabinet used. Three cables couple in the Massbus from the controller. Three more cables carry the Massbus out to the next TM03. If there is only one TM03 in the system, the Massbus may be terminated in the TM03 in which case the three "out" cables are not used. The last three cables carry the slave bus to the first slave transport, which is actually housing the TM03.

If the TM03 cables are already installed, there is no TM03 installation required; therefore, use the following instructions as applicable.

### 3.4.1 TM03 Cabling

1. Slide the TM03 out of the cabinet as shown in Figure 3-1.
2. Unscrew the two cover fasteners and remove the module cover.
3. Remove the six connector modules: M8937, M8908-YA, M8908, and the three M5903s.*
4. Connect the three BC06R Massbus cables (MBA, MBB and MBC), to the IN jacks on the three M5903* cards as shown in Figures 3-2, 3-3, and 3-4. Orient the connectors so that the smooth side of the cable is up and the colored stripes on the cables are toward the module handles (Figure 3-1).

*May be M5903-YAs.

5. If another TM03 is to be daisy-chained onto this one or if the TM03 is housed in a H9500 corporate cabinet, connect three BC06R cables to the OUT jacks on the three M5903* boards. The orientation of the three "out" cables is ribbed side up but with the colored stripe still toward the module handles.

6. If only one TM03 is used in the system and it is housed in a 48.3 cm (19 inch) H950 cabinet, insert an H870 terminator into each OUT jack or ensure that the Massbus cable cards are M5903-YAs.

7. Insert the three M5903* cards into the TM03, working from the bottom up, i.e., MBC cable card first.

8. Connect three BC06R slave bus cables to the jacks on modules M8908, M8908-YA, and M8937. Orient the connectors as in step 4, i.e., smooth side of cable up and colored stripes toward the module handles.

9. Insert the three connector modules into the TM03 working from the bottom up, i.e., M8908 first and M8937 last.

10. Secure the cable strain relief over the six BC06R cables as shown in Figure 3-1.

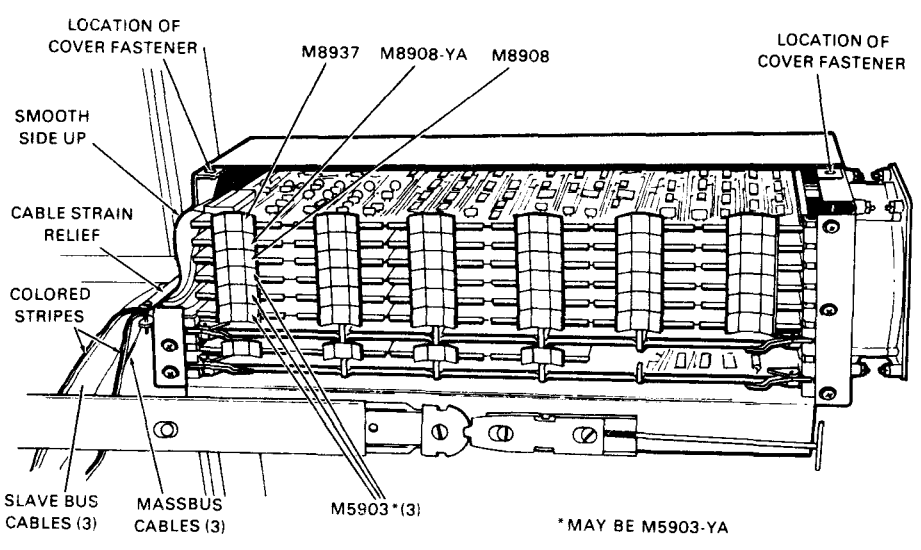
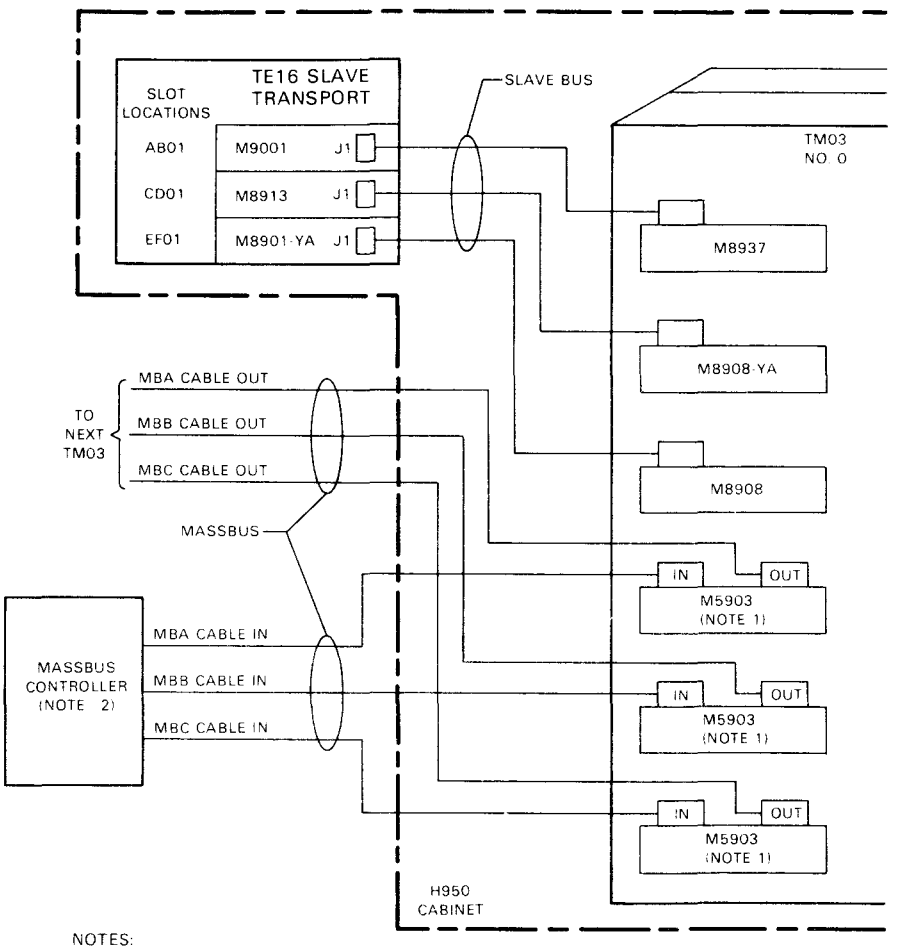



Figure 3-1 TM03 Formatter with Cover Removed

*May be M5903-YAs.




NOTES:

1. IF ONLY ONE TM03 IS USED IN SYSTEM, AN H870 TERMINATOR IS INSERTED INTO EACH OUT JACK, OR M5903-YA MODULES ARE USED WHICH PROVIDE MASSBUS TERMINATION.

2. RH10, RH11, RH20, RH70 OR RH780

MA4087

Figure 3-2 TM03 Cabling to a TE16 Slave Transport in an H950 Cabinet

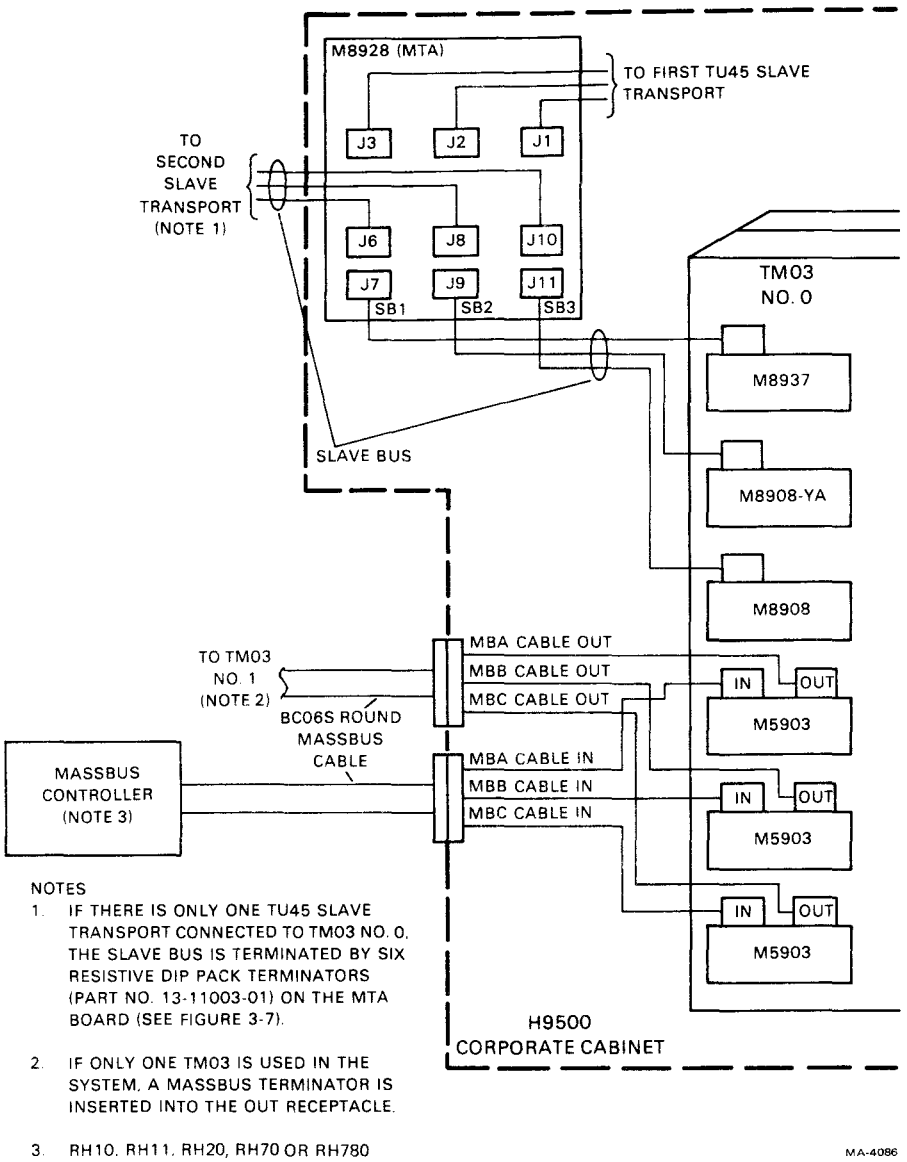



Figure 3-3 TM03 Cabling to an M8928 MTA Adapter Board in a TU45 Transport in an H9500 Corporate Cabinet

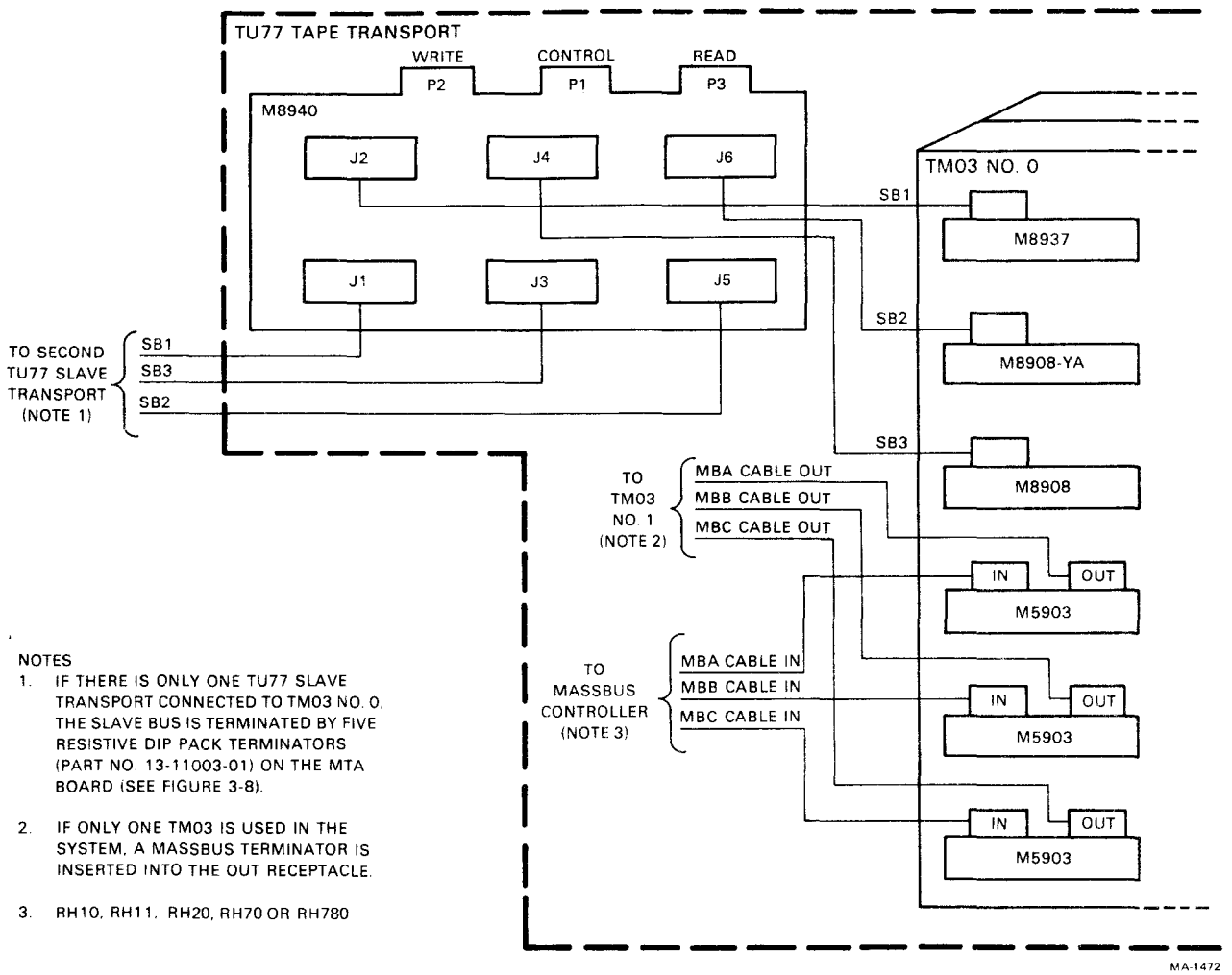



Figure 3-4 TM03 Cabling to an M8940 MTA Adapter Board in a TU77 Transport in an H9500 Corporate Cabinet

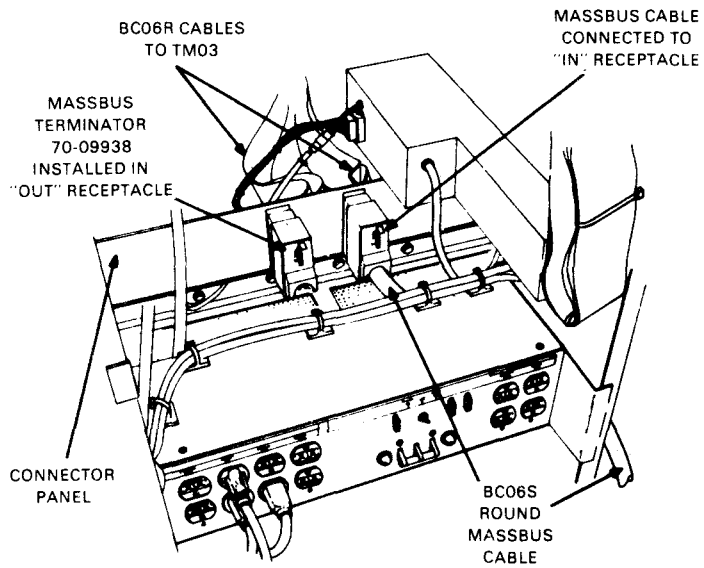
### 3.4.2 Massbus Cabling to Transport Cabinet

**NOTE**

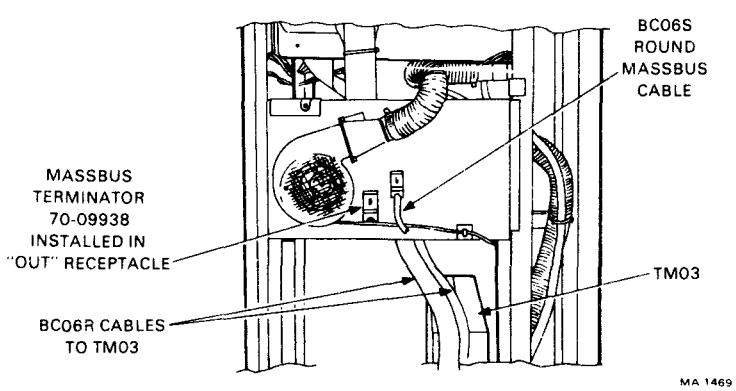
**In cabling up the Massbus, note that the maximum allowable length of the Massbus when used with TM03s is 36.9 m (120 ft).**

**3.4.2.1 H950 Cabinet** – Massbus cabling to the 48.3 cm (19 inch) H950 cabinet is usually via flat BC06R ribbon cables. The cables connect directly from the controller to the TM03 where the Massbus is either terminated or daisy-chained to the next TM03. Figure 3-2 illustrates this type of hookup.

**3.4.2.2 H9500 Corporate Cabinet** – Massbus cabling to the short H9500 corporate cabinet is via round BC06S cable which connects to a panel in the lower section of the TU45 cabinet (Figures 1-3 and 3-5a) and to the rear of the TU77 cabinet (Figure 3-5b). Three BC06R flat cables connect the Massbus from the "in" receptacle on the connector panel to the TM03. Three more cables carry the Massbus from the TM03 to the "out" receptacle on the connector panel where it is either terminated by a Massbus terminator (P/N 70-09938) or daisy-chained to the next H9500 cabinet via the BC06S round cable. Figures 3-3 and 3-4 illustrate this type of hookup.




a. Connector Panel in TU45 Transport




b. Connector Panel in TU77 Transport

Figure 3-5 External Cabling to Massbus Connector Panel in H9500 Corporate Cabinet

The BC06R cabling to the connector panel is shown in Figure 3-6. Note that cables MBA through MBC are installed from right to left on both the "in" and the "out" receptacles. Observe the smooth side/ribbed side and colored-stripe orientation shown in the figure.

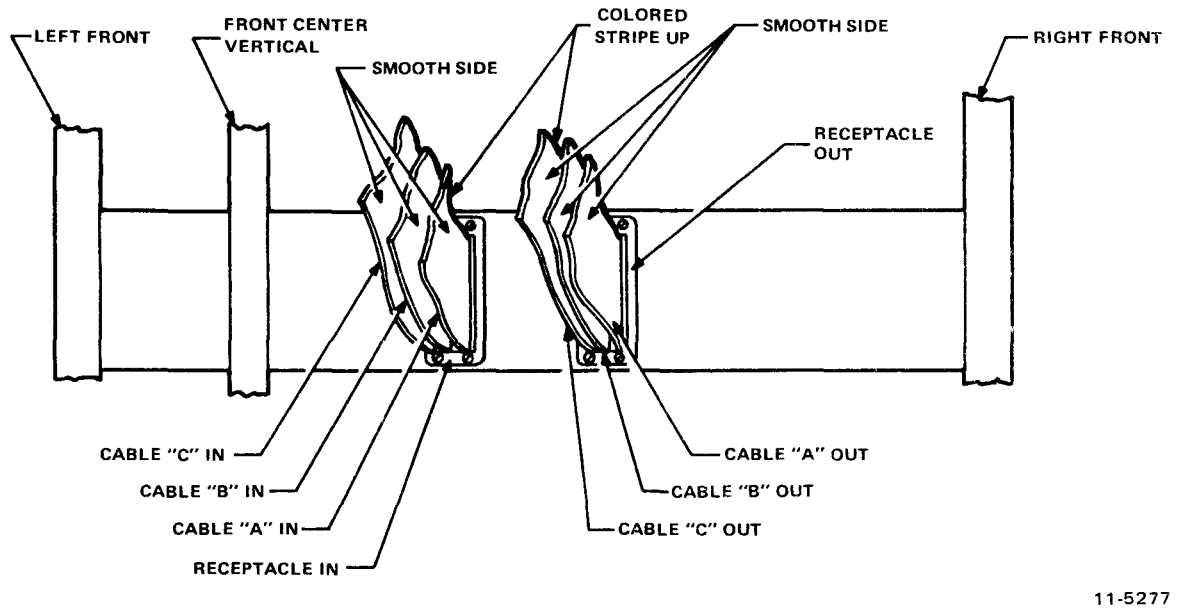



Figure 3-6 Internal Cabling to
Massbus Connector Panel in H9500 Corporate Cabinet

### 3.4.3 Slave Bus Cabling to Tape Transport

**3.4.3.1 TE16 Transport** - For cabling to a TE16 slave transport, connect the three slave bus cables to J1 on the TE16 cable cards (M9001, M8913, M8901-YA) as shown in Figure 3-2. Refer to the TE16/TE10W/TE10N user or maintenance manual (Paragraph 1.4) for cabling instructions and orientation on the TE16 cable cards.

**3.4.3.2 TU45 Transport** - An M8928 magnetic tape adapter board (MTA) is used to interface the TM03 to a TU45 tape transport. The MTA board is located on a shelf just above the TM03 (Figure 1-3). To cable up the M8928 MTA board, connect the three BC06R slave bus cables from the TM03 to J7, J9, and J11 as shown in Figures 3-3 and 3-7. Insert the connectors so that the cable's smooth side is up and the colored stripe is on the left as shown in Figure 3-7. The three cables connecting to the first slave transport (which houses the TM03) are type BC08R and connect to J1, J2, and J3. The BC08R cables are also connected with the smooth side up and the colored stripe on the left.

If there is only one slave transport connected to TM03 No. 0, terminate the slave bus by inserting six resistive DIP packs (P/N 13-11003-01) into the MTA board. If another slave transport is daisy-chained onto TM03 No. 0, connect three BC06R slave bus cables to J6, J8, and J10. These three cables are connected with the ribbed side up but with the colored stripe still on the left (Figure 3-7).

Refer to the TU45A maintenance manual for additional cabling information (Paragraph 1.4).

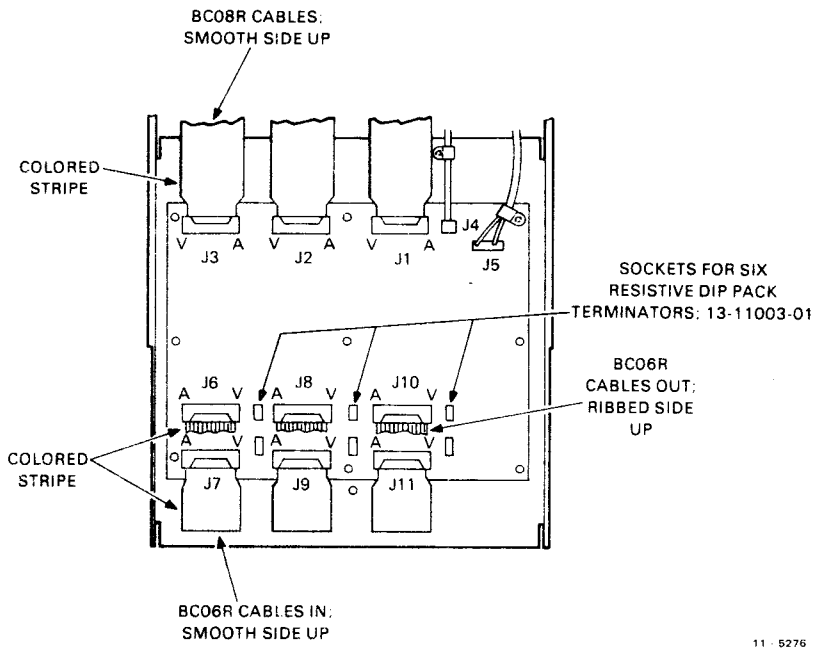



Figure 3-7 Cable Orientation on M8928 MTA Module

**3.4.3.3 TU77 Transport** - An M8940 tape magnetic adapter board (MTA) is used to interface the TM03 to a TU77 tape transport. The MTA board is plugged into the card cage assembly inside the TU77 cabinet. To cable the M8940 MTA board, connect the three BC06R slave bus cables from the TM03 to J2, J4, and J6 as shown in Figures 3-4 and 3-8. Insert the connectors so that the cable's smooth side is facing to the rear and the colored stripe is on the left as shown in Figure 3-8.

If there is only one slave transport connected to TM03 No. 0, terminate the slave bus by inserting five resistive DIP packs (P/N 13-11003-01) into the MTA board as shown in Figure 3-8. If another slave transport is daisy-chained onto TM03 No. 0, connect three BC06R slave bus cables to J1, J6, and J4. These three cables are connected with the ribbed side facing to the rear but with the colored stripe still on the left (Figure 3-8).

Refer to the TU77 user's guide or technical manual for additional cabling information (Paragraph 1.4).

## 3.5 ACCEPTANCE TESTING

The acceptance tests for the TM03 are the same as those for the particular transport being used with the TM03. If the transport acceptance tests are performed satisfactorily, then the TM03 has been installed and is operating properly. See Paragraph 1.4 for documents pertaining to the various transports that can interface with the TM03. Acceptance tests for the various transports are found in these documents.

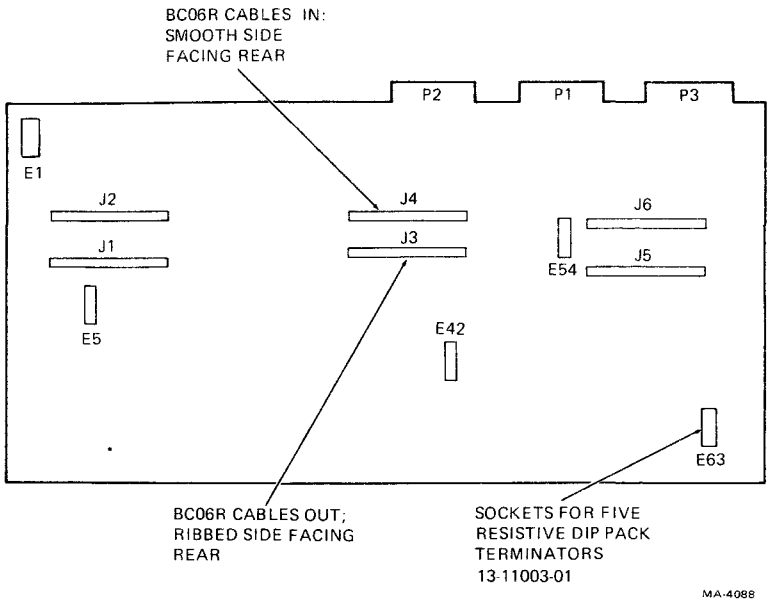



Figure 3-8 Cable Orientation on M8940 MTA Module

# APPENDIX A
# GLOSSARY

| Mnemonic | Meaning |
|---|---|
| ACCL | Acceleration |
| ADDR | Address |
| AEMD | Acceleration Enable Motion Delay |
| ANSI | American National Standards Institute |
| AS | Attention Summary |
| ASYC WRT | Asynchronous Write |
| ATA | Attention Active |
| ATTN | Attention |
| BCD | Binary Coded Decimal |
| BF | Bit Fiddler |
| BFFMTE | Bit Fiddler Format Error |
| BOT | Beginning of Tape |
| BPI | Bits Per Inch |
| 7CH | 7 Channel |
| CHK CHAR | Check Character |
| CK | Check Character |
| CLK | Clock |
| CLR | Clear |
| CMB PE | Control Massbus Parity Error |
| CNRZ | Tape Control NRZ |
| CNTR | Counter |
| CO | Carry Out |
| COMPER | Composite Error |
| COR | Correctable Data Error |
| CPA | Control Bus Parity |
| CPAR | Control Bus Parity Error |
| CPI | Characters Per Inch |
| CPU | Central Processor Unit |
| CRC | Cyclic Redundancy Check |
| CRCC | Cyclic Redundancy Check Character |
| CRCE | Cyclic Redundancy Check Error |
| CRCS | Cyclic Redundancy Check Strobe |
| CS | Control Status or Correctable Skew |
| CT | Count |
| CTOD | Controller to Drive |
| CWD | Control and Write Driver |
| DD TRK | Dead Track |
| DECL | Decelerate |
| DEM | Demand |
| DEN | Density |
| DIP | Dual In-Line Package |

| Mnemonic | Meaning |
|---|---|
| DPA | Data Parity |
| DPA TM | Data Parity Transmit |
| DPAR | Data Bus Parity Error |
| DPR | Drive Present |
| DRQ | Drive Request Required |
| DRV | Drive |
| DRY | Drive Ready |
| DS | Drive Status, Drive Select, or Data Sync |
| DT | Drive Type or Dead Track |
| DTE | Drive Timing Error |
| DVA | Drive Available |
| EAODTE | Enable Abort on Data Transfer Errors |
| EBL | End of Block |
| EMD | Enable Motion Delay |
| ENB | Enable |
| ENBL | Enable |
| END PT | End Point |
| ENV | Envelope |
| EOR | End of Record |
| EORS | End of Record Strobe |
| EOT | End of Tape |
| EPR | Error Pattern Register |
| ER | Error |
| ERDS | Enable Read Strobe |
| ERR | Composite Error |
| EV PAR | Even Parity |
| EXC | Exception |
| F | Function |
| FC | Frame Count |
| FCCLK | Frame Count Clock |
| FCE | Frame Count Error |
| FCS | Frame Count Status |
| FMK | File Mark |
| FMT | Format Error |
| FMT SEL | Format Select |
| FWD | Forward |
| ID | Identification |
| IDB | Identification Burst |
| ILF | Illegal Function |
| ILR | Illegal Register |
| INC | Incorrectable Data Error |
| INC ERROR | Incorrectable Error |
| INC PREAMBLE | Incorrect Preamble |
| ILCC | Illegal Check Character |
| INIT | Initialize |
| IPS | Inches Per Second |
| IRD | Interchange Read |
| IRG | Interrecord Gap |
| ITM | Illegal Tape Mark |
| LCTOD | Load Controller to Drive |
| LRC | Longitudinal Redundancy Check |
| LRCC | Longitudinal Redundancy Check Character |

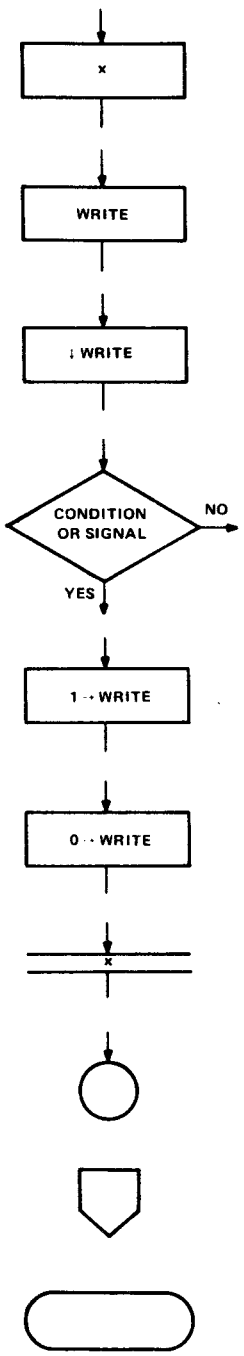
| Mnemonic | Meaning |
|---|---|
| LRCS | Longitudinal Redundancy Check Strobe |
| LSB | Least Significant Bit |
| (M) | TM03 Logic |
| MB | Massbus |
| MB XFR | Massbus Transfer |
| MBI | Massbus Interface |
| MC | Maintenance Clock |
| MCPE | Massbus Control Parity Error* |
| MDF | Maintenance Data Field |
| MM | Maintenance Mode |
| MMEOR | Maintenance Mode End of Record |
| MOH | Moving Head |
| MOL | Medium on Line |
| MOP | Maintenance Operation Code |
| MR | Maintenance Register |
| MSB | Most Significant Bit |
| MTA | Magnetic Tape Adapter |
| NED | Nonexistent Drive* |
| NEF | Non-Executable Function |
| NRZI | Non Return to Zero Inverted |
| NSA | Not Sector Addressed |
| NSG | Non-Standard Gap |
| OCC | Occupied |
| OCC TM | Occupied Transmit |
| OP | Operation |
| OPI | Operation Incomplete |
| P BF RUN | Preset Bit Fiddler Run |
| PAR | Parity |
| PE | Phase Encoded |
| PEF | Phase Encoded Format Error |
| PERR AND ONE DD TRK | Parity Error and One Dead Track |
| PES | Phase Encoded Status |
| PESB | Phase Encoded Status Buffered |
| PIP | Positioning in Progress |
| PLS | Pulse |
| POS | Postamble |
| POST PAT | Postamble Pattern |
| PRE | Preamble |
| PREVER | Previous Error |
| R | Register |
| RD | Read Data or Read |
| RDS | Read Strobe |
| REC | Record |
| REG | Register |
| REV | Reverse |
| RMR | Register Modification Refused |
| RS | Register Select or Reset |
| RSDO | Read Strobe Delay Over |
| RST | Reset |
| RWND | Rewind |
| RWS | Rewind Status |
| (S) | Any Transport |
| SAC | Slave Address Change |

*Controller signal.

| Mnemonic | Meaning |
|---|---|
| SB | Slave Bus |
| SCLK | Sync Clock |
| SDWN | Settle Down |
| SEL | Select |
| SHDN | Shutdown |
| SHDWN | Shutdown |
| SLA | Slave Attention |
| SLCT | Select |
| SN | Serial Number |
| SPR | Slave Present |
| SS | Slave Select |
| (SS) | Selected Transport |
| SSC | Slave Status Change |
| ST CLK | State Clock |
| STRB | Strobe |
| SWC | Selected Slave Clock |
| TAP | Tape Drive |
| TC | Tape Control |
| TCCM | Tape Control Common Mode |
| TCPE | Tape Control Phase Encoded |
| TM | Tape Mark |
| TMRK | Tape Mark |
| TMWIP | Tape Mark Write in Progress |
| TPMK | Tape Mark |
| TRA | Transfer |
| TRANS | Transition |
| TRK n* ERR | Track n* Error |
| TUR | Tape Unit Ready |
| UNS | Unsafe |
| VCO | Voltage Controlled Oscillator |
| VPAR | Vertical Parity Error |
| VPE | Vertical Parity Error |
| VRC | Vertical Redundancy Check |
| WB CLK | Write Buffer Clock |
| WCLK | Write Clock |
| WD | Write Data |
| WDBFO | Write Data Bit Fiddler Output |
| WDR | Write Data Record |
| WDWBO | Write Data Write Buffer Output |
| WFMK | Write File Mark |
| WRL | Write Lock |
| WRP | Wraparound |
| WRT CLK | Write Clock |
| WTMK | Write Tape Mark |

*n = track number

# APPENDIX B
# FLOWCHART GLOSSARY




x = Description of an event or action (lower case).

The signal level WRITE is asserted.

The signal level WRITE is negated.

If condition or signal is true flow follows YES branch, otherwise flow follows NO branch.

A flip-flop is set asserting WRITE.

A flip-flop is reset negating WRITE.

Delay. If delay is fixed x = amount of delay or delay range.

On page connector.

Off page connector.

Beginning or ending point of a flow diagram.

11-4781

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USER GUIDE
EK-0TM03-UG-003

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