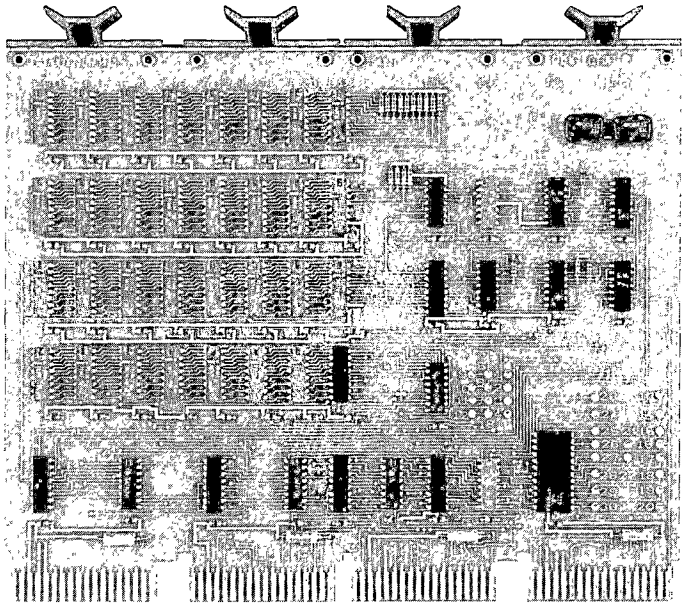
DIGITAL EQUIPMENT CORPORATION

MODULE DATA SHEET

LOGIC PRODUCTS

JULY 1974

M7344-YA,-YB,-YC Read/Write Memory Module



DESCRIPTION

The M7344 Read/Write Memory Module is a high-performance semiconductor memory unit manufactured by DIGITAL for use in random-access memories associated with minicomputer-based systems and microprocessor systems formed by Microprocessor Series (MPS) modules. This MPS module is one of a group of M Series modules designed to perform a range of industrial, laboratory, and commercial control and decision-making activities not previously considered as economic subjects for automation.

These modules are:

- M7344 Read/Write Memory Module
- M7341 Processor Module
- M7345 Programmable Read-Only Memory Module
- M7346 External Event Detection Module

Used together, these modules can form low-cost digital control systems which exhibit characteristics normally attributed to more costly minicomputer-based systems. MPS systems can serve as dedicated controllers, operate as a CPU in intelligent terminals, perform data acquisition and analysis tasks in the laboratory, and automate a host of industrial processes.

The M7344 Read/Write Memory Module provides a 1K, 2K, or 4K x 8-bit random access memory capacity along with all necessary timing, control, and decoding logic. This module is completely contained on a single quad, extended-length PC board. The module memory matrix is formed by up to 32 1024 x 1-bit static MOS MSI memory circuits. The nature of these MOS circuits precludes the need for external refresh logic.

The M7344 Read/Write Memory Module is available in three versions to satisfy varying memory capacity requirements. Model numbers identifying these memory versions are listed below:

- M7344-YA 1K x 8-bit capacity
- M7344-YB 2K x 8-bit capacity
- M7344-YC 4K x 8-bit capacity

All versions of the M7344 can be accessed by up to 16-bits of address data and are equipped with an address expansion line to implement multi-module memory systems having potential capacities of up to 128K 8-bit words. M7344 Read/Write Memory Modules also contain a jumper network which can be configured to permit assignment of a module within an application-defined address space.

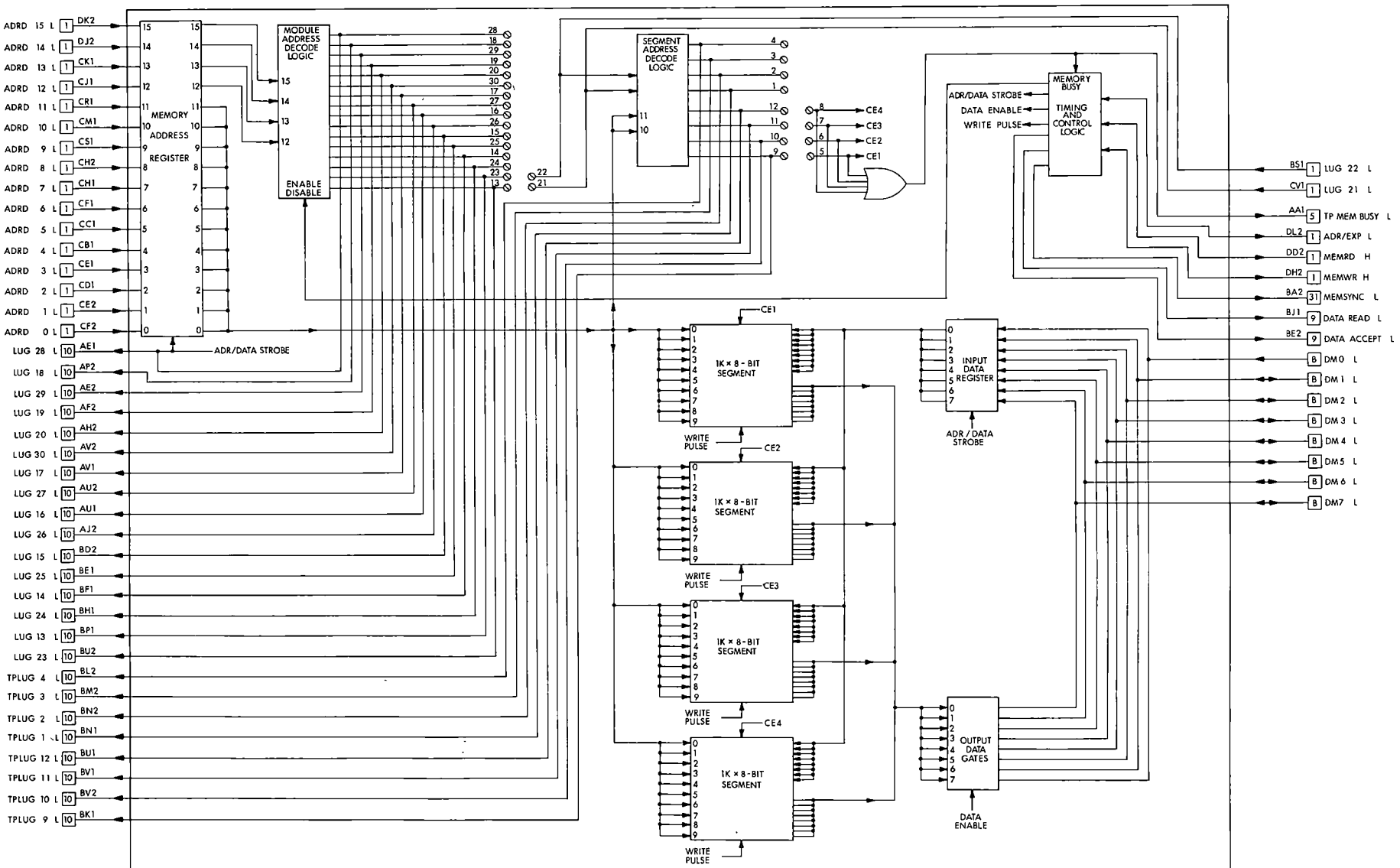


FIGURE 1. M7344 LOGIC BLOCK DIAGRAM

FEATURES

- Completely self-contained, fully decoded 8-bit read-write memory contained on standard quad, extended-length module.
- 16-bit memory address register plus dedicated address expansion line.
- Jumper network on module allows assignment of address space in 1K or 4K increments within 64K locations.
- All jumper lugs also brought out to module connector for alternative wire-wrap address space assignment.
- Memory cycle time (read cycle or write cycle) 1.15μs.
- Data ready, data accepted, and memory synchronization signals brought out on module connector for external use.
- A general-purpose memory module, the M7344 can be used with most any 8-bit minicomputer or microprocessor.
- Power requirement is +5 Vdc only.
- Memory module completely compatible with M7341 Processor Module 14-bit address.
- All inputs and outputs are TTL compatible.
- Module plugs into standard DEC H836 wire-wrap connector block backplane or equivalent.
- Memory is designed for both asynchronous and synchronous operation.
- All M7344 versions are pin-for-pin compatible with M7345 Programmable Read-Only Memory modules.

SPECIFICATION SUMMARY

Performance
Memory Type: N-channel static MOS
Data Word Size: 8 bits
Address Word Size: 16 bits plus address expansion line
Number of Words: 1024, 2048, or 4096
Memory Read or Write Cycle Time: 1.15μs minimum

Electrical
Input Logic Levels
  TTL Logical Low: 0.8 Vdc maximum
  TTL Logical High: 2.0 Vdc minimum
Output Logic Levels
  TTL Logical Low: 0.4 Vdc maximum
  TTL Logical High: 2.4 Vdc minimum
Data Bus Receivers/Drivers
  Logical Low: 0.7 Vdc maximum
  Logical High: 2.4 Vdc minimum
Address Bus Receivers
  Logical Low: 0.7 Vdc maximum
  Logical High: 2.4 Vdc minimum
Power Consumption
  M7344-YA: 1.2 A @ +5V, 6.0 W
  M7344-YB: 1.5 A @ +5V, 7.5 W
  M7344-YC: 2.2 A @ +5V, 11.0 W

Mechanical
Board Type: Quad-height, extended-length, single-width
Dimensions: 10.436 x 8.50 x 0.5 inches (26.5 x 21.6 x 1.27 cm)

Environmental
Ambient Temperature
  Operating: 5 to 50°C (41 to 122°F)
  Nonoperating: −40 to +66°C (−40 to +150°F)
Humidity: 10 to 95 percent, noncondensing

FUNCTIONS

Memory-Read Timing

The timing and control logic (see Figure 1) furnishes the signals necessary to time memory read and write operations. An associated processor asserts the level MEM RD H after providing the address of the memory location to be read. At the read/write memory module, the signal MEM RD H generates the internal signals ADR/DATA STROBE H and DATA ENABLE L.

The signal ADR/DATA STROBE H clocks the memory address register to store the address currently on the memory address bus ADRD00 L to ADRD15 L. This action initiates address decoding which enables assertion of DATA ENABLE L along with addressing of the memory location being read..

DATA ENABLE L, when asserted, enables the output gating network to place the data from the addressed location onto the bidirectional memory data bus DM0 L to DM7 L. Inspection of the timing diagram presented in Figure 2 will show that data becomes valid on the memory data bus 1.15μs after the assertion of MEM RD H.

Memory Write Timing

For a write operation, the address of the memory location to be written into is placed on the address bus ADRD00 L to ADRD15 L and must be stable for at least 150 ns prior to the assertion of MEM WR H (see Figure 2). Data to be written into the addressed location is placed on the bidirectional memory data bus DM0 L to DM7 L coincident with the signal MEM WR H.

As shown in Figure 2, the signal MEM WR H has a minimum period of 250 ns, and is asserted by an associated processor. Pulse-stretching circuitry in the M7344 timing and control logic uses the leading edge of MEM WR H to set a latch to store this signal.

Approximately 200 ns after the receipt of MEM WR H, this signal is ANDed with the decoded address to generate the internal 1-μs signal WRITE PULSE L. This pulse then enables the data stored in the data input register by the assertion of ADR/DATA STROBE (see Figure 1) to be written into the addressed memory location.

Note that the assertion of ADR/DATA STROBE H occurs at the same point in both a memory read and memory write operation to store and decode a memory address. During the 1-μs period of WRITE PULSE L, the signal ADR/DATA STROBE H is disabled to prevent any change in either address or data until the data stored in the data input register is written into the addressed memory location.

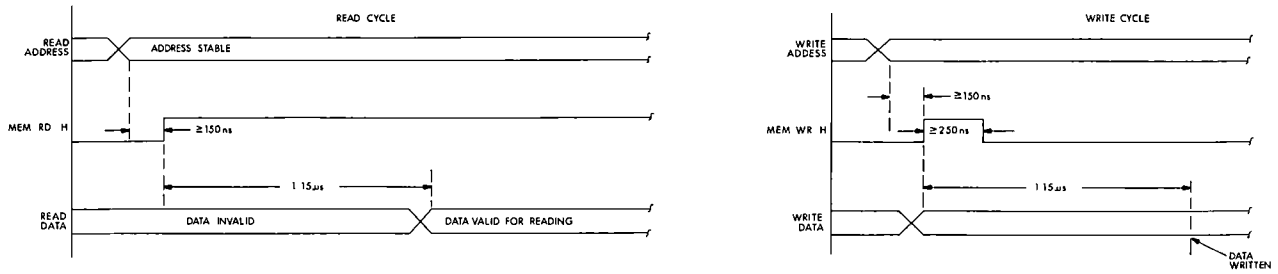


FIGURE 2. MEMORY TIMING DIAGRAM

Address Decoding

Input to the memory address decoding logic is an address furnished by an associated processor and loaded into the memory address register from the address bus ADRD00 L to ADRD15 L by the assertion of ADR/DATA STROBE H. Both the address bus and the memory address register can accommodate a 16-bit address to permit memory system capacities up to 64K. In addition, the input signal ADR/EXP L provides for implementing memory system capacities beyond 64K.

The ten low-order bits (ADRD00 L to ADRD09 L) of the memory address access the same location in each of the four 1K memory segments. The next high-order two bits (ADRD10 L and ADRD11 L) define the final magnitude of the addressed location and are decoded by the segment address decoding logic to assert one of the four signals CE1, CE2, CE3, or CE4. These signals enable the 1K segment which contains the location pointed to by the low-order 12 bits of the 14-bit address.

Note that each of the signals CE1, CE2, CE3, and CE4 is jumpered to permit assignment of address space in 1K multiples within the total memory system address space.

Memory Jumper Options

In order to address multiple module memory systems containing up to 64K locations, which implements the full accessing capacity of a 16-bit address field, all of the decoded states of bits ADRD13 L to ADRD15 L can be jumper-configured. As a consequence, each 4K module in a multiple module memory system can be uniquely jumpered to be assigned as a given set of 4K memory locations within a consecutive set of up to 16K locations.

Inspection of Figure 1 will show that the jumper network is configured to permit allocation of address space in 1K intervals within an address range of 4K to 8K formed by either one or two M7344 modules. In addition, each module can be assigned an address space of up to 4K within a total 64K address set. Each side of this jumper network is also brought out to the module edge fingers to permit address space allocation to be supplemented by wire wrap on the connector block.

Since the M7344 Read/Write Memory is electrically and logically compatible with the M7345 Programmable Read-Only Memory, these modules can be used together to form a contiguous RAM-PROM memory space.

SIGNAL SPECIFICATIONS

Input Signals

Symbol	*Description*	*Pin*	*Function*
CF2	Address Line 0	ADRD00 L	These 16 parallel input lines provide a 16-bit address for accessing the contents of an M7344 read/write memory module.
CE2	Address Line 1	ADRD01 L	
CD1	Address Line 2	ADRD02 L	
CE1	Address Line 3	ADRD03 L	
CB1	Address Line 4	ADRD04 L	
CC1	Address Line 5	ADRD05 L	
CF1	Address Line 6	ADRD06 L	
CH1	Address Line 7	ADRD07 L	
CH2	Address Line 8	ADRD08 L	
CS1	Address Line 9	ADRD09 L	
CM1	Address Line 10	ADRD10 L	
CR1	Address Line 11	ADRD11 L	
CJ1	Address Line 12	ADRD12 L	
CK1	Address Line 13	ADRD13 L	
DJ2	Address Line 14	ADRD14 L	
DK2	Address Line 15	ADRD15 L	

Input Signals (continued)

Symbol	*Description*	*Pin*	*Function*
DD2	Memory Read Control Signal	MEM RD H	When asserted, this input signal initiates the assertion of internal signals which initiate storage and decoding of the current address and the reading of data from the addressed location.
DH2	Memory Write Control Signal	MEM WR H	When asserted, this signal triggers the internal pulse WRITE PULSE L, initiates the storage and decoding of the current address and generates the internal signal WRITE PULSE L which is used to write data into an addressed location.
DL2	Address Expansion Line	ADR/EXP L	This signal allows expansion of the 64K address space.
BS1	Input to Module Address Space Selection Lug 22	LUG22 L	This input point provides for wire wrap implementation as an alternative to installation of jumpers on the module.
CV1	Input to Module Address Space Selection Lug 21	LUG21 L	This input point provides for implementation of address space allocation as an alternative to installation of jumpers on the module.

Output Signals

Symbol	*Description*	*Pin*	*Function*
BA1	Memory Synchronization Signal	MEM SYNC L	This signal permits asynchronous operation of the M7344 memory module.
BJ1	Data Ready for Reading	DATA READY L	This signal provides for synchronization of memory read operations.
BE2	Data to be Written has been Received	DATA ACCEPT L	This signal provides for synchronization of memory write operations.
BL2	Lug 4 Test Point	TPLUG4 L	These test points are the segment address selection lugs brought out to test operation of 1K memory segment.
BM2	Lug 3 Test Point	TPLUG3 L	
BN2	Lug 2 Test Point	TPLUG2 L	
BN1	Lug 1 Test Point	TPLUG1 L	
BU1	Lug 12 Test Point	TPLUG12 L	These test points are the segment address selection lugs brought out to test operation of 1K memory segments in a 4K address space.
BV1	Lug 11 Test Point	TPLUG11 L	
BV2	Lug 10 Test Point	TPLUG10 L	
BK1	Lug 9 Test Point	TPLUG9 L	
AA1	Memory Busy Test Point	TPMEM BUSY H	When High, the output from this test point indicates that the memory is busy performing a read or write operation.
AE1	Wire Wrap Pin Lug 28	LUG28 L	These output points, used in conjunction with input points LUG22 L and LUG21 L, provide for wire wrap allocation of address space as an alternative to the installation of jumpers on the module.
AP2	Wire Wrap Pin Lug 18	LUG18 L	
AE2	Wire Wrap Pin Lug 29	LUG29 L	
AF2	Wire Wrap Pin Lug 19	LUG19 L	
AH2	Wire Wrap Pin Lug 20	LUG20 L	
AV2	Wire Wrap Pin Lug 30	LUG30 L	
AV1	Wire Wrap Pin Lug 17	LUG17 L	
AU2	Wire Wrap Pin Lug 27	LUG27 L	
AU1	Wire Wrap Pin Lug 16	LUG16 L	
AJ2	Wire Wrap Pin Lug 26	LUG26 L	
BD2	Wire Wrap Pin Lug 15	LUG15 L	
BE1	Wire Wrap Pin Lug 25	LUG25 L	
BF1	Wire Wrap Pin Lug 14	LUG14 L	
BH1	Wire Wrap Pin Lug 24	LUG24 L	
BP1	Wire Wrap Pin Lug 23	LUG23 L	
BU2	Wire Wrap Pin Lug 13	LUG13 L	

Input/Output Signals

Symbol	*Description*	*Pin*	*Function*
AD2	Bidirectional Memory Data Bus Line 0	DM0 L	These are the eight parallel bidirectional data lines comprising the input/output data bus. Pull-up resistors required for proper operation; 180Ω to +5V, and 390Ω to ground.
AC1	Bidirectional Memory Data Bus Line 1	DM1 L	
AM2	Bidirectional Memory Data Bus Line 2	DM2 L	
AN1	Bidirectional Memory Data Bus Line 3	DM3 L	
BD1	Bidirectional Memory Data Bus Line 4	DM4 L	
BC1	Bidirectional Memory Data Bus Line 5	DM5 L	
BM1	Bidirectional Memory Data Bus Line 6	DM6 L	
BL1	Bidirectional Memory Data Bus Line 7	DM7 L	

SPECIAL WIRING

As shown in Figure 1 and discussed under FUNCTIONS, the M7344 Read/Write Memory Module is designed to respond to a 16-bit address field. As a consequence, a given module with 1K, 2K, or 4K of memory capacity can exist within a 64K address space.

Within these 64K locations, a 1K or 2K memory module can be configured to occupy a unique 1K or 2K address space in the 4K address space. In addition, this 4K address space can occupy any one of 16 groups of sequential 4K locations within the total 64K address space. Similarly, a 4K memory module can be configured to occupy a 4K block within an 8K address space, and this 8K address space can be located in the total address space.

An M7344 memory module can be assigned to occupy a given 4K or 8K address space in one of two ways:

1. By jumper-connecting specific module address space selection lugs (see Figure 3) which are part of a total set of split lugs provided on the module for the explicit purpose of address space assignment;

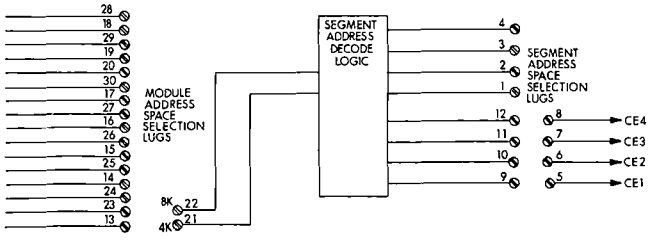


FIGURE 3. DESIGNATIONS FOR SPLIT LUGS PROVIDED FOR ADDRESS SPACE ASSIGNMENT

2. By wire wrapping the appropriate connector block pins which correspond to the specific edge connector fingers within the overall group of fingers allocated to address space assignment.

Within the module, each 1K segment can be assigned to one of the four 1K address spaces in a 4K space or in an 8K space through appropriate connection of the segment address space selection lugs (see Figure 3).

NOTE

This level of address space selection must be made with jumpers since the equivalent split lug points are not brought out to the edge connector.

In order to clarify the manner of assigning a memory module to a specific address space, a series of examples is presented which relate specific lug-to-lug connections to address space assigned. These examples require reference to Figure 3 and Table 1.

Table 1 shows the lug-to-lug and corresponding pin-to-pin connections for a 64K address space. However, the examples presented are, for purposes of clarity, concerned with the first or low order 16K address space. In principle, these examples are applicable throughout the full 64K address space, and differ only in the specific connections made between lugs 21 and 22 and the remaining Module Address Space Selection lugs (see Figure 3).

EXAMPLE 1: By placing a jumper between lug 13 and lug 21, an M7344-YC (4K) memory module will be assigned to locations 0 to 4095. In this case, the segment address selection lugs 9, 10, 11, and 12 should be connected to lugs 5, 6, 7, and 8 respectively in order to enable the four 1K memory segments comprising the 4K capacity.

TABLE 1
Address Space Allocation

Jumper Connection		Alternative Edge Connector/Wire Wrap Connection		Address Space Allocation			
				From Location		To Location	
From Jumper Lug	To Jumper Lug	From Pin	To Pin	Decimal	Octal	Decimal	Octal
21	13	CV1	BU2	0	0	4095	7,777
21	23	CV1	BP1	4096	10,000	8191	17,777
21	24	CV1	BH1	8192	20,000	12287	27,777
21	14	CV1	BF1	12288	30,000	16383	37,777
21	25	CV1	BE1	16384	40,000	20479	47,777
21	15	CV1	BD2	20480	50,000	24575	57,777
21	26	CV1	AJ2	24576	60,000	28671	67,777
21	16	CV1	AU1	28672	70,000	32767	77,777
21	27	CV1	AU2	32768	100,000	36863	107,777
21	17	CV1	AV1	36864	110,000	40959	117,777
21	30	CV1	AV2	40960	120,000	45055	127,777
21	20	CV1	AH2	45056	130,000	49151	137,777
21	19	CV1	AF2	49152	140,000	53247	147,777
21	29	CV1	AE2	53248	150,000	57343	157,777
21	18	CV1	AP2	57344	160,000	61439	167,777
21	28	CV1	AE1	61440	170,000	65535	177,777
22	13	BS1	BU2	0	0	4095	7,777
22	23	BS1	BP1	4096	10,000	8191	17,777
22	24	BS1	BH1	8192	20,000	12287	27,777
22	14	BS1	BF1	12288	30,000	16383	37,777
22	25	BS1	BE1	16384	40,000	20479	47,777
22	15	BS1	BD2	20480	50,000	24575	57,777
22	26	BS1	AJ2	24576	60,000	28671	67,777
22	16	BS1	AU1	28672	70,000	32767	77,777
22	27	BS1	AU2	32768	100,000	36863	107,777
22	17	BS1	AV1	36864	110,000	40959	117,777
22	30	BS1	AV2	40960	120,000	45055	127,777
22	20	BS1	AH2	45056	130,000	49151	137,777
22	19	BS1	AF2	49152	140,000	53247	147,777
22	29	BS1	AE2	53248	150,000	57343	157,777
22	18	BS1	AP2	57344	160,000	61439	167,777
22	28	BS1	AE1	61440	170,000	65535	177,777

EXAMPLE 2: By placing a jumper between lug 21 and lugs 23, 24 or 14, an M7344-YC memory module can be assigned to locations 4096 to 8191, 8192 to 12287, or 12288 to 16383 respectively. With any of these assignments, the segment address space selection lugs must be connected in the same manner as in Example 1.

EXAMPLE 3: Since 8K subsets of the overall 16K address space are defined by boundaries of the four constituent 4K address spaces, 1K memory module segments can be jumpered to occupy any one of six unique 8K spaces. Three of these 8K spaces are formed by adjacent 4K spaces and three are non-adjacent. The three 8K spaces formed by adjacent 4K spaces are defined in this example.

The 8K address space, 0 to 8191, is allocated to a module by installing a jumper between module address space selection lugs 21 and 13, and 22 and 23 on that module. The 8K address space, 4096 to 12287, is allocated to a module by installing a jumper between lugs 21 and 23, and lugs 22 and 24. Finally, to allocate the 8K space, 8192 to 16383, to a module, a jumper must be installed between lugs 21 and 24, and between lugs 22 and 14.

At this point, jumpers installed between specific segment address selection lugs can then assign the one, two, or four 1K segments on a module within the 8K address space allocated to that module. For example, with an M7344-YC (4K) module allocated to the 8K space 8192 to 16383, a jumper installed between lugs 9 and 5 assigns the first 1K segment to the address space 8192 to 9215. Similarly, a jumper installed between lugs 1 and 6 assigns the second 1K segment to the address space 12288 to 13311.

A jumper installed between lugs 7 and 11 assigns the third 1K segment to the address space 9216 to 10239. Finally, a jumper installed between lugs 8 and 2 assigns the fourth 1K segment to the address space 13312 to 14335.

It can be inferred from these examples that the 1K segments comprising a 1K, 2K, or 4K MPS system memory module can be assigned by jumper-installation to any one of the sixteen 1K slots in the 16K address space.

INPUT/OUTPUT SYMBOLOGY

The direction of signal flow is indicated by arrows on the signal lines. Arrows toward the module indicate input signals; arrows away from the module indicate output signals (see Figure 1 and Figure 4).

Fan-in and fan-out (in TTL unit loads) are indicated by the number contained in the box associated with each pin. A box containing the letter B designates that the associated signal line is connected to a bus.

INPUT—The fan-in designation box always precedes the pin designation.

OUTPUT—The fan-out designation box always follows the pin designation.

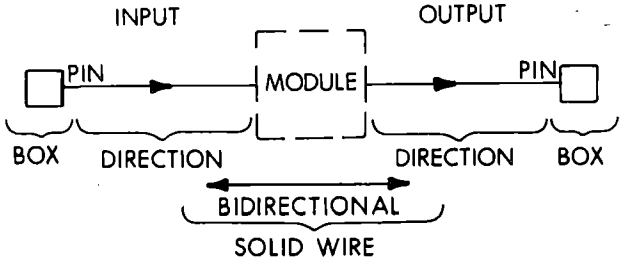


FIGURE 4. SIGNAL FLOW DIRECTION

POWER REQUIREMENTS

	VOLTS	POWER CONSUMPTION		VOLTAGE REGULATION	RIPPLE REGULATION	PINS	
		mA (max)	WATTS (max)			POWER	GROUND
M7344-YA	+5	1700	8.5	±5%	50 mV	AA2, BA2, CA2, DA2	AC2, AT1, BC2, BC1, CC2, CT1, DC2, DC1
M7344-YB	+5	2170	10.5				
M7344-YC	+5	3130	15.7				

digital

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