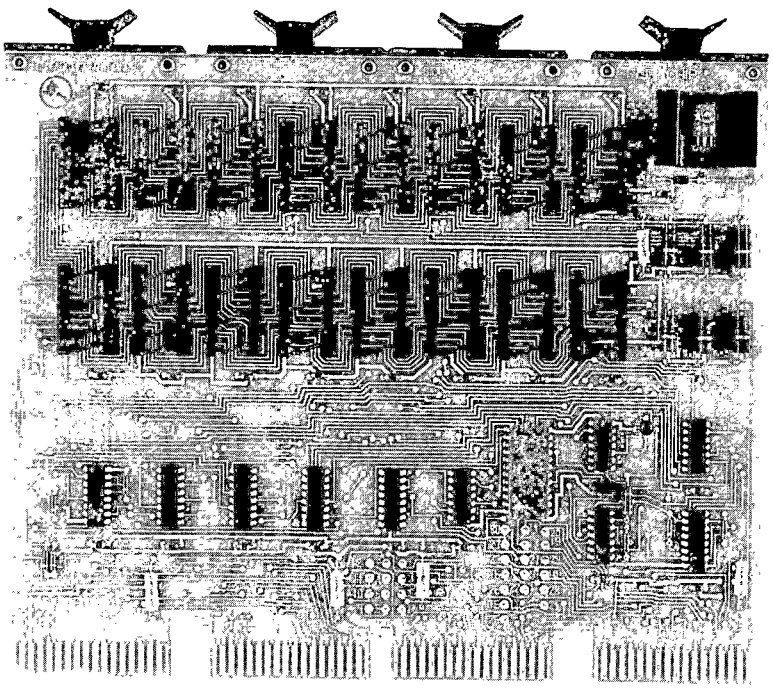
DIGITAL EQUIPMENT CORPORATION

MODULE DATA SHEET

LOGIC PRODUCTS

JULY 1974

M7345 Programmable Read-Only Memory Module



DESCRIPTION

The M7345 Programmable Read-Only Memory Module is a high-performance semiconductor memory manufactured by DIGITAL for use with read-only memory units in minicomputer-based systems, and microprocessor systems formed by Microprocessor Series (MPS) modules. This MPS module is one of a group of M Series modules designed to perform a range of industrial, laboratory, and commercial control and decision-making activities not previously considered as economic subjects for automation.

These modules are:

- M7345 Programmable Read-Only Memory Module
- M7341 Processor Module
- M7344 Read/Write Memory Module
- M7346 External Event Detection Module

Used together, these modules can form low-cost digital control systems which exhibit characteristics normally attributed to more costly minicomputer-based systems. MPS systems can serve as dedicated controllers, operate as a CPU in intelligent terminals, perform data acquisition and analysis tasks in the laboratory, and automate a host of industrial processes.

The M7345 Programmable Read-Only Memory module provides a read-only data storage capacity which can vary from 256 8-bit words to 4K 8-bit words in 256-word increments. This read-only memory capacity is formed by static MOS 256 x 8-bit PROM circuits which are electrically programmable and easily erasable by ultraviolet light. The memory is completely contained on a quad, extended-length module and includes sockets for the memory circuits, and all address decoding, control, and timing logic. The PROM circuits necessary to form the memory matrix are furnished as a separate item apart from the M7345 module.

Maximum PROM capacity is formed by 16 MSI memory circuits mounted in plug-in sockets and organized as 16 separate matrices, each containing 256 8-bit words. These 256 x 8-bit PROM circuits can be added as necessary to satisfy changing system requirements. Socket mounting also permits each circuit to be removed for erasure and reprogramming. A transparent quartz lid

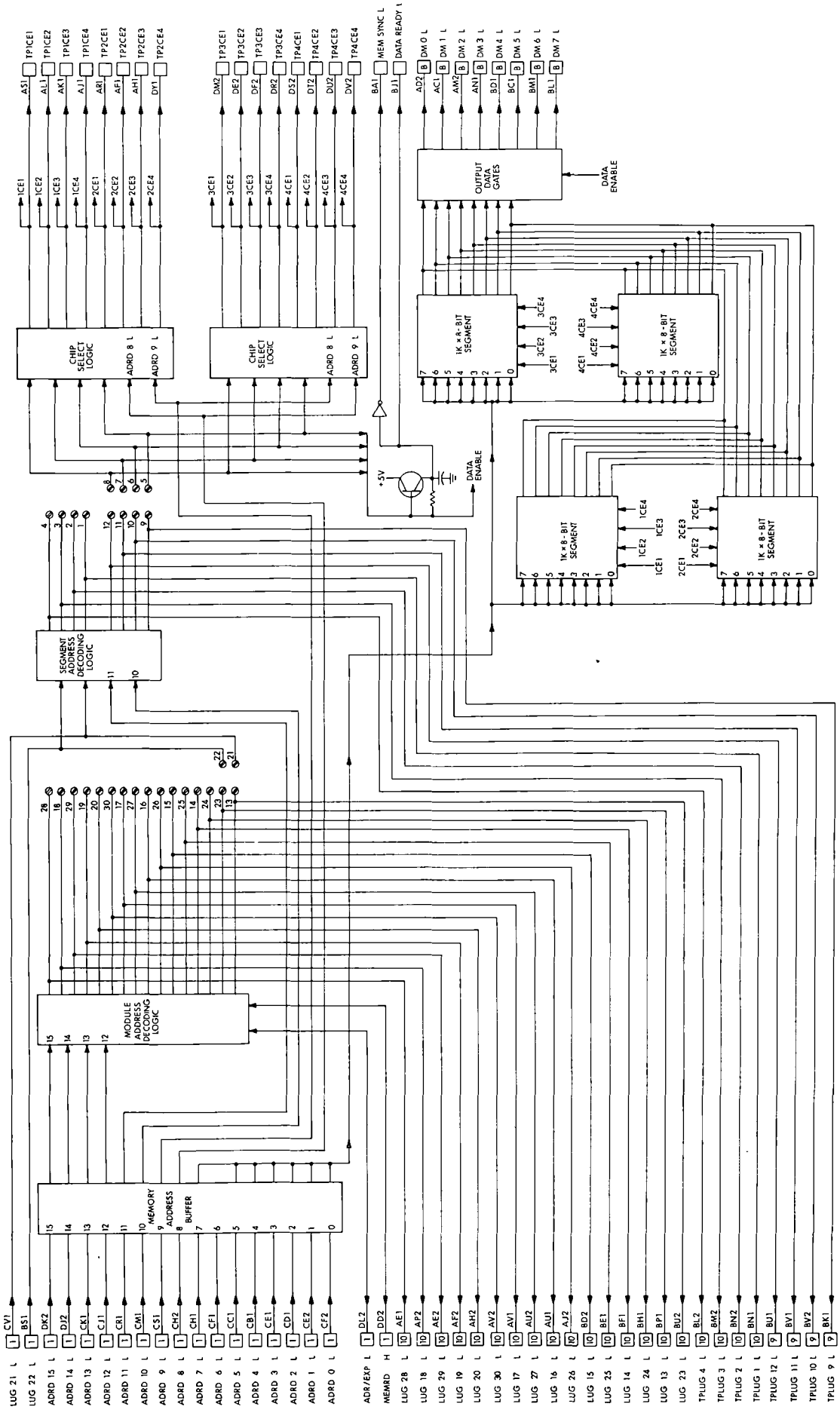


FIGURE 1. M7345 LOGIC BLOCK DIAGRAM

on each PROM circuit permits exposure to an ultraviolet light source for erasure of an existing bit pattern. A new bit pattern can then be electrically written.

FEATURES

- Completely self-contained, fully decoded programmable read-only memory contained on standard DIGITAL quad-height module.
- Memory capacity formed by 256 x 8-bit PROM circuits which are electrically programmable and erasable with ultraviolet light.
- All memory circuits socket-mounted on module for easy insertion and removal.
- Module accepts 16-bit memory address and is equipped with an address expansion line.
- Module memory capacity expandable from 256 to 4K locations in 256-word increments.
- Jumper network on module allows assignment of address space in 1K to 4K increments within 64K locations.
- Jumper network lugs also brought out to module connector for alternative wire-wrap address space assignment.
- Memory read cycle time 1.15 μs.
- Data-ready and memory-synchronizing signals brought out on module connector for external use.
- Memory module logic includes a complete integral general-purpose interface.
- A general-purpose memory module, the M7345 can be used with almost any 8-bit minicomputer or microprocessor.
- Programmable Read-Only Memory Module is pin-for-pin compatible with all versions of the M7344 Read/Write Memory Module.
- Input power requirements are +5 Vdc and −15 Vdc.
- All inputs and outputs are TTL-compatible.
- Module plugs into standard DEC H863 wire-wrap connector block backplane or equivalent.

SPECIFICATION SUMMARY

Performance

Memory Type: Static MOS
Data Word Size: 8 bits
Address Word Size: 14 bits, expandable to 16 bits plus address expansion line
Number of Words: Expandable, from 256 words to 4K words
Read Cycle: 1.15μs, nondestructive readout
Erasure Method: Ultraviolet light; 256 words erased per circuit exposed
Erasure Time: 10-minutes, maximum
Program Write Time: 2 minutes typical, per 256 words

Electrical

Input Logic Levels
  TTL Logical Low: 0.8 Vdc maximum
  TTL Logical High: 2.0 Vdc minimum
Output Logic Levels
  TTL Logical Low: 0.4 Vdc maximum
  TTL Logical High: 2.4 Vdc minimum
Data Bus Drivers
  Logical Low: 0.7 Vdc maximum
  Logical High: 2.4 Vdc minimum
Address Bus Receivers
  Logical Low: 0.7 Vdc maximum
  Logical High: 2.4 Vdc minimum
Power Consumption
  M7345 Module without PROMs: 350 mA @ +5V, 100 mA @ −15V; 3.7 W
  23-00A4-03 256x8-bit PROM Chip: 20 mA @ +5V, 70 mA @ −15V; 1.2 W
  M7345 with 1K Memory: 490 mA @ +5V, 300 mA @ −15V; 6.0 W
  M7345 with 2K Memory: 630 mA @ +5V, 530 mA @ −15V; 11.0 W
  M7345 with 4K Memory : 900 mA @ +5V, 1.0 A @ −15V; 19.5 W

Mechanical

Board Type: Quad-height, extended-length, single-width
Dimensions: 10.436 x 8.50 x 0.5 inches (26.5 x 21.6 x 1.27 cm)

Environmental

Ambient Temperature
  Operating: 5 to 50°C (41 to 122°F)
  Nonoperating: −40 to +66°C (−40 to +150°F)
Humidity: 10 to 95 percent, noncondensing

FUNCTIONS

Address and Control Decoding

Address inputs to the M7345 module (see Figure 1) are the 16 bits of the address bus (ADRD00 L to ADRD15 L), and the input signal ADR/EXP L which provides for address expansion.

As shown in Figure 1, the low-order eight bits, ADRD00 L to ADRD07 L, directly address each PROM circuit in the memory matrix. The remaining address bus bits (ADRD08 L to ADRD15 L) are input to the address and control decoding logic, which is enabled by the signal MEM RD L.

Address bits ADRD10 L and ADRD11 L are decoded to determine the 1K group within a 4K group containing the addressed location. ADRD08 L and ADRD09 L are decoded to point to the 256 x 8-bit PROM circuit within that 1K group containing the addressed location. The result of this decoding is the assertion of one of 16 chip-enable signals which causes the addressed PROM circuit to output data from the addressed location within 1.5 microseconds after the assertion of MEM RD H (see Figure 2); this data is present at the data output gates.

All chip-enable signals are wire-ORed to assert the internal signal DATA ENABLE which gates the data at the output data gates onto the memory data bus DM0 L to DM7 L. This same logic also asserts the external synchronizing signals MEM SYNC L and DATA READY L.

Bus address bits ADRD12 L and ADRD13 L are decoded to implement addressing of multiple module PROM systems having up to 16K locations. Address bits ADRD14 L and ADRD15 L are decoded to permit expansion of multiple module PROM systems beyond 16K locations up to 64K locations.

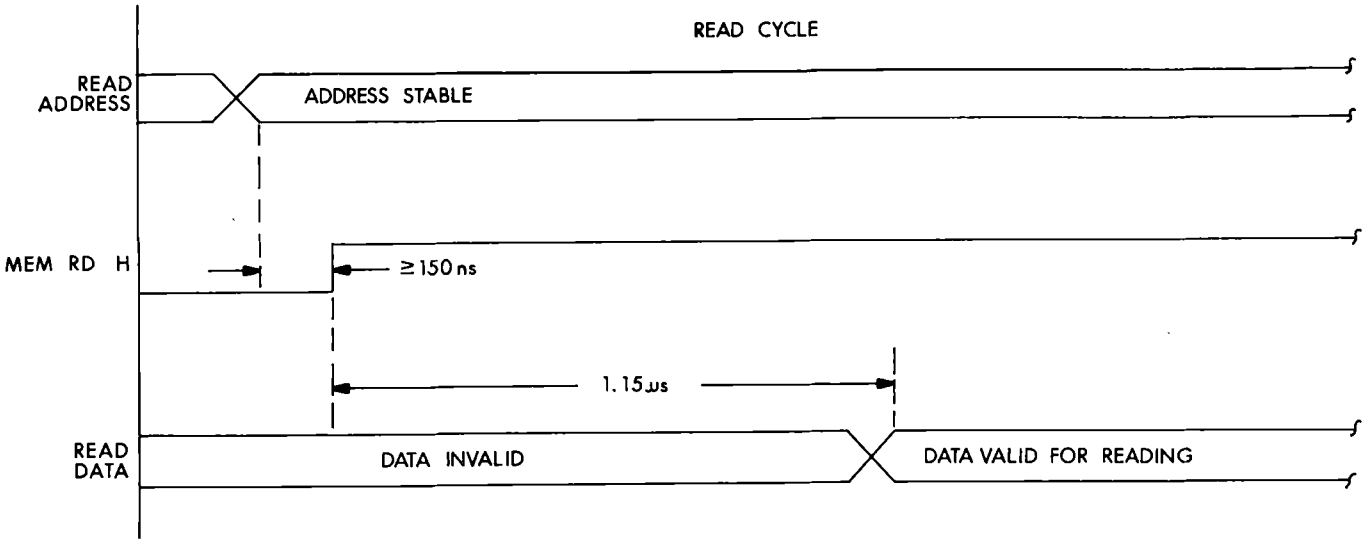


FIGURE 2. MEMORY TIMING DIAGRAM

Memory Jumper Options

In order to address multiple module memory systems containing up to 64K locations, which implements the full accessing capacity of a 16-bit address field, all of the decoded states of bits ADRD13 L to ADRD15 L can be jumper-configured. As a consequence, each 4K module in a multiple-module memory system can be uniquely jumpered to be assigned as a given set of up to 4K memory locations within a consecutive set of up to 64K locations.

Inspection of Figure 1 will show that the jumper network is configured to permit allocation of address space in 1K intervals within an address range of 4K to 8K formed by either one or two M7345 modules.

This jumper network is also brought out to the module edge fingers to permit address space allocation to be implemented by wire wrap on the connector block.

SIGNAL SPECIFICATIONS

Input Signals

Symbol	*Description*	*Pin*	*Function*
CF2	Address Line 0	ADRD00 L	These 16 parallel input lines provide a 16-bit address for reading instructions and data stored in an M7345 read-only memory module.
CE2	Address Line 1	ADRD01 L	
CD1	Address Line 2	ADRD02 L	
CE1	Address Line 3	ADRD03 L	
CB1	Address Line 4	ADRD04 L	
CC1	Address Line 5	ADRD05 L	
CF1	Address Line 6	ADRD06 L	
CH1	Address Line 7	ADRD07 L	
CH2	Address Line 8	ADRD08 L	
CS1	Address Line 9	ADRD09 L	
CM1	Address Line 10	ADRD10 L	
CR1	Address Line 11	ADRD11 L	
CJ1	Address Line 12	ADRD12 L	
CK1	Address Line 13	ADRD13 L	
DJ2	Address Line 14	ADRD14 L	
DK2	Address Line 15	ADRD15 L	

Input Signals (continued)

Symbol	*Description*	*Pin*	*Function*
DD2	Memory Read Control Signal	MEMRD H	When asserted, this input signal initiates the assertion of internal signals which initiate storage and decoding of the current address and the reading of data from the addressed location.
DL2	Address Expansion Line	ADR/EXP L	This signal allows expansion of the 64K address space afforded by the 16-bit address.
BS1	Input to Module Address Space Selection Lug 22	LUG22 L	This input point provides for wire-wrap implementation as an alternative to installation of jumpers on the module.
CV1	Input to Module Address Space Selection Lug 21	LUG21 L	This input point provides for implementation of address space allocation as an alternative to installation of jumpers on the module.

Output Signals

Symbol	*Description*	*Pin*	*Function*
BA1	Memory Synchronization Signal	MEMSYNC L	This signal permits asynchronous operation of the M7345 memory module in non-MPS systems applications.
BJ1	Data Ready for Reading	DATA READY L	This signal provides for synchronization of memory read operations in non-MPS systems applications.
BL2	Lug 4 Test Point	TPLUG4 L	These test points are the segment address selection lugs brought out to test operation of 1K memory segment in an 8K address space.
BM2	Lug 3 Test Point	TPLUG3 L	
BN2	Lug 2 Test Point	TPLUG2 L	
BN1	Lug 1 Test Point	TPLUG1 L	
BU1	Lug 12 Test Point	TPLUG12 L	These test points are the segment address selection lugs brought out to test operation of 1K memory segment in a 4K address space.
BV1	Lug 11 Test Point	TPLUG11 L	
BV2	Lug 10 Test Point	TPLUG10 L	
BK1	Lug 9 Test Point	TPLUG9 L	
AE1	Wire Wrap Pin Lug 28	LUG28 L	These output points, used in conjunction with input points LUG22 L and LUG21 L, provide for wire-wrap allocation of address space as an alternative to the installation of jumpers on the module.
AK2	Wire Wrap Pin Lug 18	LUG18 L	
AE2	Wire Wrap Pin Lug 29	LUG29 L	
AF2	Wire Wrap Pin Lug 19	LUG19 L	
AH2	Wire Wrap Pin Lug 20	LUG20 L	
AV2	Wire Wrap Pin Lug 30	LUG30 L	
AV1	Wire Wrap Pin Lug 17	LUG17 L	
AU2	Wire Wrap Pin Lug 27	LUG27 L	
AU1	Wire Wrap Pin Lug 16	LUG16 L	
AJ2	Wire Wrap Pin Lug 26	LUG26 L	
BD2	Wire Wrap Pin Lug 15	LUG15 L	
BE1	Wire Wrap Pin Lug 25	LUG25 L	
BF1	Wire Wrap Pin Lug 14	LUG14 L	
BH1	Wire Wrap Pin Lug 24	LUG24 L	
BP1	Wire Wrap Pin Lug 13	LUG13 L	
BU2	Wire Wrap Pin Lug 23	LUG23 L	
AS1	1CE1 Test Point	TP1CE1	These test points permit testing access to the internal chip-enable signals and are used only to test memory operation.
AL1	1CE2 Test Point	TP1CE2	
AK1	1CE3 Test Point	TP1CE3	
AJ1	1CE4 Test Point	TP1CE4	
AR1	2CE1 Test Point	TP2CE1	
AF1	2CE2 Test Point	TP2CE2	
AH1	2CE3 Test Point	TP2CE3	
DY1	2CE4 Test Point	TP2CE4	
DM2	3CE1 Test Point	TP3CE1	
DE2	3CE2 Test Point	TP3CE2	

Output Signals (continued)

Symbol	Description	Pin	Function
DF2	3CE3 Test Point	TP3CE3	These test points permit testing access to the internal chip-enable signals and are used only to test memory operation.
DR2	3CE4 Test Point	TP3CE4	
DS2	4CE1 Test Point	TP4CE1	
DT2	4CE2 Test Point	TP4CE2	
DU2	4CE3 Test Point	TP4CE3	
DV2	4CE4 Test Point	TP4CE4	

Input/Output Signals

Symbol	Description	Pin	Function
AD2	Memory Data Bus Line 0	DM0 L	These are the eight parallel data lines comprising the data memory bus.
AC1	Memory Data Bus Line 1	DM1 L	
AM2	Memory Data Bus Line 2	DM2 L	
AN1	Memory Data Bus Line 3	DM3 L	
BD1	Memory Data Bus Line 4	DM4 L	
BC1	Memory Data Bus Line 5	DM5 L	
BM1	Memory Data Bus Line 6	DM6 L	
BL1	Memory Data Bus Line 7	DM7 L	

HARDWARE/ACCESSORIES

The M7345 Programmable Read-Only Memory Module is supplied with sockets for a memory capacity of up to 4K, but without the dual in-line PROM circuits which plug into the sockets. These PROM circuits are available separately and may be ordered under the following nomenclature and part number:

NOMENCLATURE	DEC PART NUMBER
2048-bit Programmable Read-Only Memory (24-pin DIP)	23-00A4-03

DIGITAL also offers the MR873-A Microprocessor ROM Programmer which provides for the electrical writing of programs into 23-00A4-03 PROM circuits. This programmer operates in conjunction with any PDP-8 computer system having OMNIBUS construction. Such a configuration permits the reading in of an object program from an associated input device (e.g. a TTY), the examination and modification of this program, and the electrical writing of the resulting program into PROM circuits. Listings and paper tapes of the written program can also be obtained.

SPECIAL WIRING

As shown in Figure 1 and discussed under FUNCTIONS, the M7345 Programmable Read-Only Memory Module is designed to respond to a 16-bit address field. As a consequence, a given module with up to 4K of memory capacity can exist within a 64K address space.

Within these 64K locations, an M7345 memory module can be configured to occupy a unique 1K or 2K address space in the 4K address space. In addition, this 4K address space can occupy any one of four groups of sequential 4K locations within the total 16K address space. Similarly, a read-only memory module can be configured to occupy a 4K block within an 8K address space, and this 8K address space can be located in either the upper or lower half of the total 16K address space.

An M7345 memory module can be assigned to occupy a given 4K or 8K address space in one of two ways:

1. By jumper-connecting specific module address space selection lugs (see Figure 3) which are part of a total set of split lugs provided on the module for the explicit purpose of address space assignment.

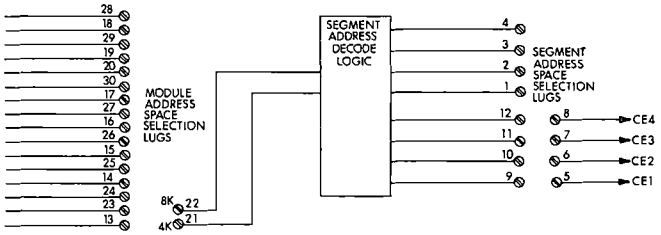


FIGURE 3. DESIGNATIONS FOR SPLIT LUGS PROVIDED FOR ADDRESS SPACE ASSIGNMENT

2. By wire wrapping the appropriate connector block pins which correspond to the specific edge connector fingers within the overall group of fingers allocated to address space assignment (see Table 1).

Within the module, each 1K segment can be assigned to one of the four 1K address spaces in a 4K space or in an 8K space through appropriate connection of the segment address space selection lugs (see Figure 3). Note that this level of address space selection must be made with jumpers since the equivalent split-lug points are not brought out to the edge connector. The actual set of 256 words addressed within a 1K segment is determined by the physical position of the PROM circuit on the board (see Figure 4). In order to clarify the manner of assigning a read-only memory module to a specific address space, a series of examples is presented which relate specific lug-to-lug connections to address space assigned. These examples require reference to Figure 3 and Table 1.

Table 1 shows the lug-to-lug and corresponding pin-to-pin connections for a 64K address space. However, the examples presented are, for purposes of clarity, concerned only with the first or low-order 16K address space. In principle, these examples are applicable throughout the full 64K address space, and differ only in the specific connections made between lugs 21 and 22 and the remaining Module Address Space Selection lugs (see Figure 3).

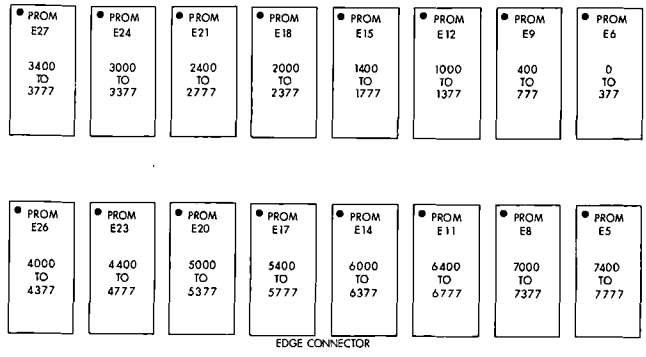


FIGURE 4. PHYSICAL LOCATION AND OCTAL ADDRESSES OF PROM CIRCUITS ON M7345 MODULE

NOTE:
The dot (•) at the upper LH corner of each PROM circuit designates the location of pin 1, and thereby specifies the orientation of each circuit to the corresponding plug-in socket.

CAUTION
When removing PROM circuits from sockets, be sure to use an industry approved IC removal tool in order to prevent damage to the PROM circuit.

TABLE 1
Address Space Allocation

Jumper Connection		Alternative Edge Connector/Wire Wrap Connection		Address Space Allocation			
				From Location		To Location	
From Jumper Lug	To Jumper Lug	From Pin	To Pin	Decimal	Octal	Decimal	Octal
21	13	CV1	BU2	0	0	4095	7,777
21	23	CV1	BP1	4096	10,000	8191	17,777
21	24	CV1	BH1	8192	20,000	12287	27,777
21	14	CV1	BF1	12288	30,000	16383	37,777
21	25	CV1	BE1	16384	40,000	20479	47,777
21	15	CV1	BD2	20480	50,000	24575	57,777
21	26	CV1	AJ2	24576	60,000	28671	67,777
21	16	CV1	AU1	28672	70,000	32767	77,777
21	27	CV1	AU2	32768	100,000	36863	107,777
21	17	CV1	AV1	36864	110,000	40959	117,777
21	30	CV1	AV2	40960	120,000	45055	127,777
21	20	CV1	AH2	45056	130,000	49151	137,777
21	19	CV1	AF2	49152	140,000	53247	147,777
21	29	CV1	AE2	53248	150,000	57343	157,777
21	18	CV1	AP2	57344	160,000	61439	167,777
21	28	CV1	AE1	61440	170,000	65535	177,777
22	13	BS1	BU2	0	0	4095	7,777
22	23	BS1	BP1	4096	10,000	8191	17,777
22	24	BS1	BH1	8192	20,000	12287	27,777
22	14	BS1	BF1	12288	30,000	16383	37,777
22	25	BS1	BE1	16384	40,000	20479	47,777
22	15	BS1	BD2	20480	50,000	24575	57,777
22	26	BS1	AJ2	24576	60,000	28671	67,777
22	16	BS1	AU1	28672	70,000	32767	77,777
22	27	BS1	AU2	32768	100,000	36863	107,777
22	17	BS1	AV1	36864	110,000	40959	117,777
22	30	BS1	AV2	40960	120,000	45055	127,777
22	20	BS1	AH2	45056	130,000	49151	137,777
22	19	BS1	AF2	49152	140,000	53247	147,777
22	29	BS1	AE2	53248	150,000	57343	157,777
22	18	BS1	AP2	57344	160,000	61439	167,777
22	28	BS1	AE1	61440	170,000	65535	177,777

EXAMPLE 1: By placing a jumper between lug 13 and lug 21, a read-only memory module will be assigned to locations 0 to 4095. In this case, the segment address selection lugs 9, 10, 11, and 12 should be connected to lugs 5, 6, 7, and 8, respectively, in order to enable the four 1K memory sectors comprising the total 4K capacity.

EXAMPLE 2: By placing a jumper between lug 21 and lugs 23, 24 or 14, a read-only memory module can be assigned to locations 4096 to 8191, 8192 to 12287, or 12288 to 16383, respectively. With any of these assignments, the segment address space selection lugs must be connected in the same manner as in Example 1.

EXAMPLE 3: Since 8K subsets of the overall 16K address space are defined by boundaries of the four constituent 4K address spaces, 1K memory module segments can occupy any one of six unique 8K spaces. Three of these 8K spaces are formed by adjacent 4K spaces and three are nonadjacent. The three 8K spaces formed by adjacent 4K spaces are defined in this example.

The 8K address space 0 to 8191 is allocated to a module by installing a jumper between module address space selection lugs 21 and 13, and 22 and 23 on that module. The 8K address space 4096 to 12287 is allocated to a module by installing a jumper between lugs 21 and 23, and lugs 22 and 24. Finally, to allocate the 8K space 8192 to 16383 to a module, a jumper must be installed between lugs 21 and 24 and between lugs 22 and 14.

At this point, jumpers installed between specific segment address selection lugs can then assign the one, two, or four 1K segments on a module within the 8K address space allocated to that module. For example, with a read-only memory module allocated to the 8K space 8192 to 16383, a jumper installed between lugs 9 and 5 assigns the first 1K segment to the address space 8192 to 9215. Similarly, a jumper installed between lugs 1 and 6 assigns the second 1K segment to the address space 12288 to 13311. A jumper installed between lugs 7 and 11 assigns the third 1K segment to the address space 9216 to 10239. Finally, a jumper installed between lugs 8 and 2 assigns the fourth 1K segment to the address space 13312 to 14335.

It can be inferred from these examples that the 1K segments comprising a 1K, 2K, or 4K MPS system read-only memory module can be assigned by jumper-installation to any one of the 1K slots in the total 64K address space.

INPUT/OUTPUT SYMBOLOGY

The direction of signal flow is indicated by arrows on the signal lines. Arrows toward the module indicate input signals; arrows away from the module indicate output signals (see Figure 1 and Figure 5).

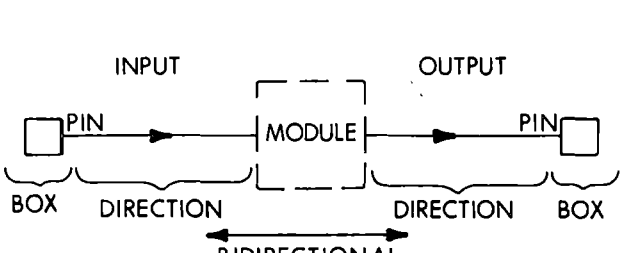


FIGURE 5. SIGNAL FLOW DIRECTION

Fan-in and fan-out (in TTL unit loads) are indicated by the number contained in the box associated with each pin. A box containing the letter B designates that the associated signal line is connected to a bus.

INPUT—The fan-in designation box always precedes the pin designation.

OUTPUT—The fan-out designation box always follows the pin designation.

POWER REQUIREMENTS

	POWER CONSUMPTION		VOLTAGE REGULATION	RIPPLE REGULATION	PINS	
VOLTS	mA (max)	WATTS (max)			POWER	GROUND
+5	1290	6.5	±5%	50 mV	AA2, BA2, CA2, DA2	AC2, AT1, BC2, BC1, CC2, CC1, DC2, DC1
−15	1085	16.3	±3%	50 mV	AB2	

digital
DIGITAL EQUIPMENT CORPORATION
COMPONENTS GROUP HEADQUARTERS
ONE IRON WAY, MARLBOROUGH, MASSACHUSETTS 01752
(617) 481-7400 TWX 710-347-0348
For detailed information about products and policies, call 800-225-9480 toll-free (USA only); Massachusetts residents call (617) 481-7400.

PRINTED IN U.S.A. 5804 00874 3987/M 16 10