PDP-X Technical Memorandum # 14

Title: Preliminary Memory Bus Description

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Index Key(s): Memory Bus
Bus
Parity
Memory

Distribution Key: A

Obsolete: None

Revision: None

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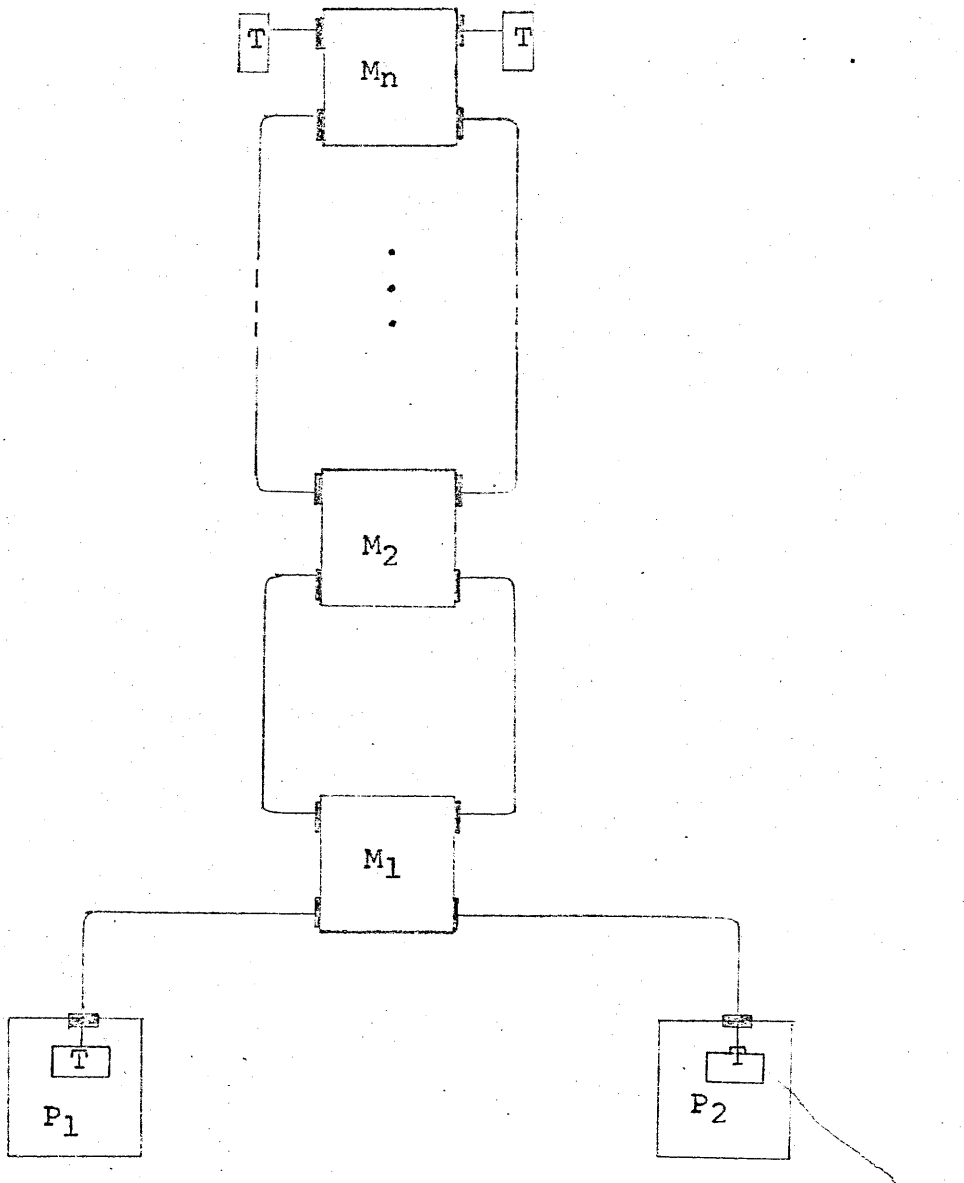
Introduction

The PDP-X memory bus is the interconnection facility between one processor module (or extremely fast IO device, standard or customer special) and one or more memory modules. Signals in the bus are interlocked to permit arbitrarily long lines without degrading performance when memory is close to the processor. The electrical properties of the memory bus are identical to the IO bus.

System Organization

The three modules which connect to the memory bus are a) the processor (an extremely fast IO device), b) the memory, and c) the arbiter. Each processor has one single ended port for connection to the memory system; each memory has two double ended ports as shown in accompanying Figure 1. The port to which the arbiter connects has priority, in the case of simultaneous request, over the other port. Note that any configuration with only one local memory system does not require an arbiter.

Figure 1

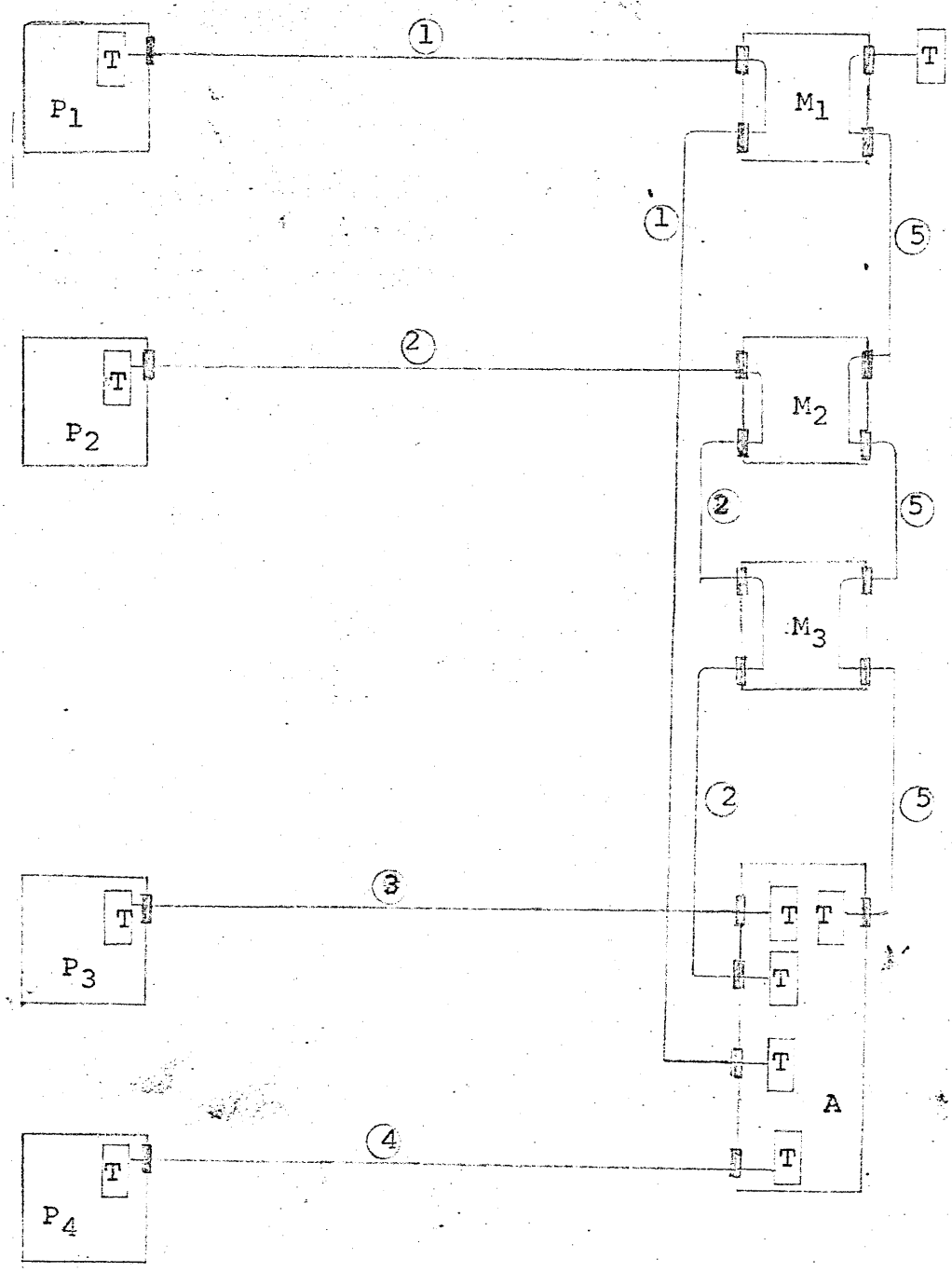


P = processor module
M = memory module
T = bus terminator

When there are two or more local memory systems, the arbiter is required. The arbiter multiplexes the second memory port so that it is available to all the processors. It contains 4 single ended input parts, one for each 4 possible processors, and a single output port. One arbiter may be plugged into the next to expand its capability in units of three.

Figure 2 gives a diagram of a hypothetical 4 processor system. The memory local to a processor is defined to be the memory which may be accessed without using the arbiter. All processors may be simultaneously communicating with their local memory; only one processor may, through the arbiter, have access to the entire memory system. The arbiter must be the last connection to the memory bus.

Figure 2



A = arbiter
Note - there are 5 busses shown above

When a processor makes a memory request, the request is examined by each memory. If no memory responds, the arbiter passes the request to the entire memory system. This system operates efficiently so long as processors normally communicate only with their local memories. The memory name space is arranged so that each processor sees its local memory starting at location 0 and extending consecutively upward to the installed capacity. Non-local memory is named consecutively upward from the top of local memory. Arbiter hardware, a simple map, is used on each input port to permit these naming conventions.

The arbiter determines that no local memory has responded by delaying the request signal and then using it to examine the ADDR EXIST line on the (local) bus. The arbiter forwards any requests for which no local address exists to the entire memory system along the common bus.

Signals

The signals on the bus include:

I_{0-24} - 20_{10} bidirectional address/data lines

$C_{0,1}$ - 2 control signals, processor to memory

C_0C_1	Operation
00	illegal
01	read/restore
10	clear/write
11	read/pause/write

RQ — memory request, raised (50 ns) after address and control information above is set up.

ADD RACK — address acknowledge, raised by the memory signifying that it has read in address and commenced.

RD RST — read restart, indicates that the memory has placed the requested information onto the data lines.

WR RST — write restart, indicates that the processor has placed the information to be written onto the data lines.

ADDR EXIST — address exists, rises within 100 ns of RQ when the memory recognizes the address. This signal is independent of memory being ready to perform a cycle.

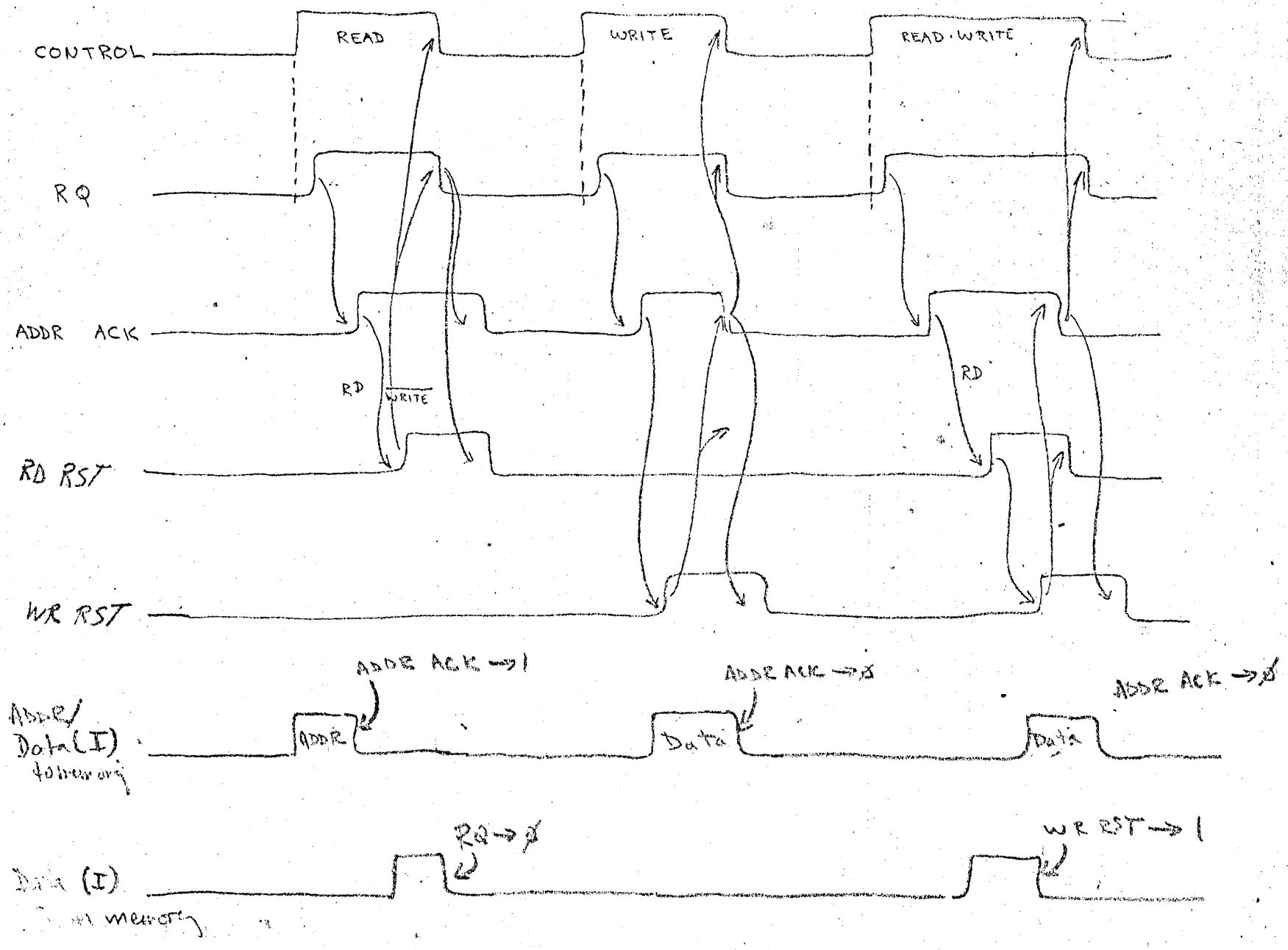

CONTROL
READ
WRITE
READ · WRITE
RQ
ADDR ACK
RD
WRITE
RD
RD RST
WR RST
ADDR ACK → 1
ADDR ACK → 0
ADDR ACK → 0
ADDR
Data
Data
Addr/
Data (I)
to memory
RQ → 0
WR RST → 1
Data (I)
memory

Figure 3

Pwr	remote turn on
Gnd	heavy ground wire interconnection

Parity

Parity is implemented for any local memory system by adding the parity control unit and an additional memory system (4k x 16-bits). The low order 12 address bits select a word in the parity memory, the high order 4 bits select one of the 16-bits which is the (odd) parity check bit. The memory cycle rate is not effected by the parity calculation since the parity memory runs 1/3 cycle behind the main memory. In case of parity error, the system (optionally) halts at the completion of the invalid cycle.

Special IO Devices

A special customer IO device may be substituted for a processor in any system where the data rate of the device warrants it. The memory bus interface seen by the device is, of course, identical to the interface seen by a processor; the same conventions and timing relations hold. Such devices have an additional interface to the IO bus for control purposes. Maximum data transfer rate along the memory bus is determined by the full memory cycle plus arbiter delay plus any cable delay to the device.