PDP-K TECHNICAL MEMORANDUM # 5

TITLE: PDP-11 Bus Devices on K Bus

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INDEX KEYS: I/O Bus
Device Addressing

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1.0 INTRODUCTION

The purpose of this memo is to investigate the feasibility of using PDP-11 devices on the K Bus and the possibility of using K Bus devices on the 11 Bus.

2.0 Questions to be considered in this discussion:

a. Can 11 type devices be used on K Bus?
b. Which 11 type devices can be used on the K?
c. What are the electrical and physical requirements for device interchangability?
d. What K devices could be used on the PDP-11?

General Discussion of:

a. Device address scheme
b. Interrupt sequence
c. Break address capability
d. Byte alignment in words

2.1 Can 11 devices be used on K Bus?

Yes, if we assume the electrical specs are the same for both buses and use the PA-PB lines on SP1 SP2 lines for Data Bits 17-16. All 72 pins of the bus connector are assigned.

2.2 Which 11 type devices can be used on the K?

Initial investigation shows that the character oriented devices should present no difficulty. They are: Teletype, Paper Tape, Card Reader, Line Printer (low speed), X-Y Scope display, Point Plotter (Calcomp type), and some A/D-D/A interfaces.

The NPR (DMA) devices which might be easily used (if modified) are: DecTape and Disk (RSØ9 Type). The modification to the controllers would be to provide the read/write paths to the 2 additional bits and assign them to the SP1-SP2 lines on the bus.

Conversations with Bruce Delagi indicate a willingness to consider making 18 data bits available on the Dec Tape and Disk (RSØ9) since they are already 18 bit devices. Jumpers or some similar enabling scheme would be used to provide the two extra data paths.

2.3 What are the electrical and physical requirements for device interchangability?

The Bus Driver/Receiver loading must be similar (see PDP-11 Handbook - figure 9.2) to the 11 bus. The maximum number of receivers permitted is currently set at 20.

The internal Unibus uses flexprint cable with 72 lines, 60 signals and 12 grounds. The lack of alternate grounds limits the speed at which lines may be switched without excessive crosstalk.

The Unibus Cable (BC11A) for use outside a mounting box has 120 conductor flexprint with alternate grounds. The PDP-11 maximum specified bus length, internal and external, is 50 feet. Maximum transfer rate on the 11 Unibus is one word every 750 nanoseconds.

To accomodate 18 Data bits on the Unibus, the two spare lines, SP1-SP2, would be used; thus leaving no spares. The internal K Bus could be wider than 60 signals (72 pin connector) but it would require giving up some ground pins or using three slots for cable connectors (108 pins).

The use of PDP-11 character type devices (TTY) could be accomplished by using the prewired option panel (DD11) and an adapter cable from K Bus devices. This assumes the K Bus cable is wider than the 11 bus.

I am assuming that the K Bus will need more than 60 signal lines, since a new system with no expansion capability would be undesirable.

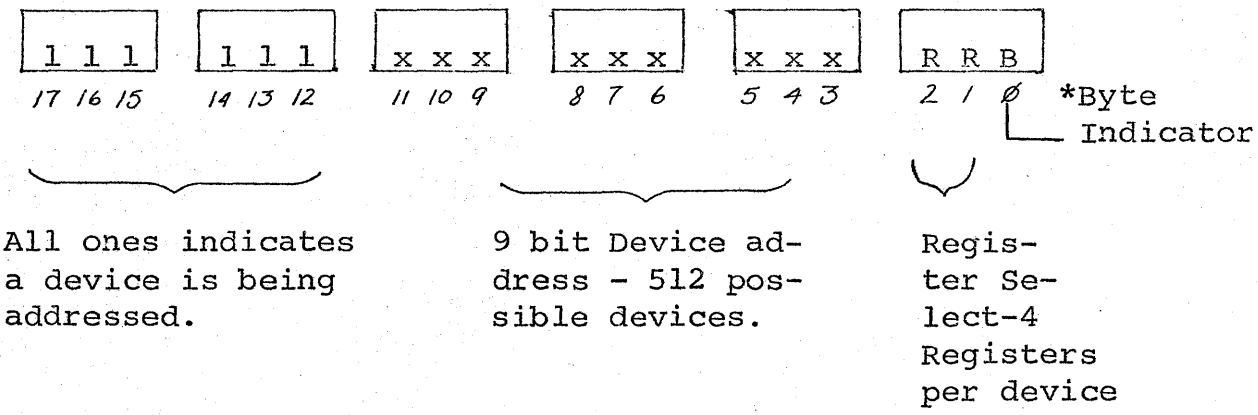
2.4 What K devices could be used on the PDP-11?

Since there are no devices in process for the K, this question really means; how many devices can be designed to work on the 11 and K? A further question is; how much engineering overhead is required to achieve compatibility? As indicated in 2.2, there are two devices now considered as possible to receive the 16/18 bit capability. A very brief investigation shows that very little control hardware would be required, and the cost of the two extra receivers and drivers would be small. The major problems would be layout space on the modules and a convenient method of enabling the 18 bit operation. Another consideration is the reluctance of the 11 Engineering group to assign data lines to the only two spare lines on the bus. If non-interference could be assured on the spare lines, this would not be a problem.

2.5 General Discussion:

Device Address Scheme.

With an 18 bit address and the desirability of addressing over 200K of memory, the following is proposed:



*The Byte Indicator would be used for character oriented devices such as TTY.

For character type devices the above scheme can look like the 11 bus addressing - Device Select, Register Select, and Byte Select (bit Ø). Data will be transferred to and from the least significant Data lines (15-8 or 7-Ø), controlled by Address bit Ø, to registers in the CPU, there to be handled by K Byte operators.

Interrupt Sequence.

On an INTR (interrupt) cycle from a device, the Break Address is put on the DATA lines. This address must be handled via the CPU and turned into a Stack Pointer. A typical INTR Sequence is handled via stack operations, hardware controlled, using the LIFO technique (see PDP-11 Handbook - page 8).

Break Address Capability.

The current Interrupt Control Module (M782) for the 11 bus is limited to a 6 bit Break Address (5 bits plus a variant). We could make our own version which would overcome this limitation, also if desired, the Break Address could be put on the Address lines instead of the PDP-11 method of using the Data Lines.

Byte Alignment in words.

As indicated earlier, the PDP-11 character devices generally use byte mode for data transfer. Typically, this is right justified (bits 7 - Ø) and is addressed as the Low Byte.

3.0 SUMMARY

There are many other considerations concerning device compatability not covered in this memo. Should we limit the K Bus to the speed of the Unibus? Are the controls for the Unibus adequate for the K? Looking at devices and bus speeds today, the answer is probably, yes. Looking three years hence, I am not quite sure we will be satisfied.

Discussions of the K indicate there may be two buses; high speed DMA bus and ordinary Unibus for routine devices. This leads to the need for a bus priority scheme in the I/O control.

Another possibility is the use of a PDP-11 for an I/O processor - all routine devices could be controlled by the 11. Data transfers with K memory via DMA. This approach eliminates the need for this memo.

There is an obvious economic advantage to having a group of peripherals which will work on the PDP-11 and K without modification. Against the advantages must be weighed the limitations of the 11 bus and the fact that there is no expansion capability.

A possible alternative might be to implement a bus scheme with the PDP-11 concept and the PDP-15 electrical characteristics. This would not permit the PDP-11 device modules to be plugged into the K bus directly, but would require minor changes to the receivers and drivers. This scheme should also contain more lines for expansion.

The intent of this memo was to investigate compatability between PDP-11 and K Buses. It would appear that I have raised more questions than answers. This memo might have been titled "What Price Compatability?" The overall "price" for compatability must include such questions as; will we be satisfied with the performance of a compatible bus in the future, and will we look back and wish we had done differently?